A Novel Integrated Doherty Power Amplifier at 28GHz

by Brendan Korba

**A thesis submitted to the Faculty of Graduate and Postdoctoral
Affairs in partial fulfillment of the requirements for the degree of**

Master of Applied Sciences
Electrical and Computer Engineering

Carleton University

Ottawa, Ontario

© 2021

Brendan Korba

Contents

1	Abstract	ix
2	Acknowledgements	x
3	Introduction	1
3.1	Motivation	1
3.2	The Role Of Power Amplifiers	2
3.3	High-Order Modulation Schemes and How they Effect Efficiency	2
3.4	Thesis Outline	3
3.5	Thesis Objective	3
4	Background	5
4.1	Backed-off Efficiency Improvement	5
4.1.1	Envelope Tracking (Envelope Trackig (ET))	6
4.1.2	Classic Doherty Amplifier Topology	8
4.2	Doherty Combiner	15
4.3	Works in Doherty Amplifiers at mmWave Frequencies	16
5	Design	24
5.1	Coupled Line Combiner	24
5.2	Combiner Layout and Simulation	27
5.3	Transistor Manifold Design	31
5.4	Theory	31
5.5	Biasing of transistors	35
5.6	Layout Comparison	38
5.7	Simulation Comparison	41
5.8	Top level PA Simulation	44
5.8.1	Small Signal Simulation	45

5.8.2	Large Signal Simulation	48
6	Layout	49
7	Testing of the Doherty Power Amplifier	51
7.0.1	Small Signal Simulation of overall Doherty Amplifier . . .	53
7.1	Future Work	56
8	Conclusion	58
8.1	Thesis Contributions	58
A	Matlab code for Main amplifier load modulation	63

List of Figures

1	Typical Envelope Tracking Topology	7
2	Current sources representing the main and peaking amplifier in a Doherty PA topology [7]	9
3	Typical Doherty Amplifier Topology	11
4	Ideal Doherty PAE and Device current draw [7]	12
5	PAE curve of ideal Doherty when implemented with Class B and C Amplifiers [7]	13
6	PAE curve of Doherty when implemented with nonlinear Class B and C Amplifiers [7]	14
7	Coupled line Doherty Combiner	15
8	Doherty Amplifier Topology implemented in [20] where IMN is the input matching network, PCN and IIN are delay lines, ISMN is the inter-stage matching network of each amplifier, and the OMN is the output matching network	17
9	Doherty Amplifier Topology implemented in [21]	18
10	Modified Hybrid Coupler Implemented in [21]	19
11	Schematic Diagram of Doherty Implemented in [27]	20
12	Transformer Based Doherty combiner	21
13	Transformer Based Doherty combiner With adaptive biasing cir- cuit to enhance turn on characteristics of auxiliary Power Ampli- fier (PA)	22
14	Coupled line Doherty combiner	24
15	Generic coupled line segment	25
16	Load Modulation of Main Amplifier	26
17	Coupled Line Doherty Combiner Laid out in GF 45nm RFSOI	28
18	Circuit used to characterize the Doherty action of the Combiners	29

19	Coupled line Doherty Combiner EM vs Ideal transmission Line Simulated Load Modulation where m1 and m3 are the backed off loading of the main amplifier and m2 and m4 are the full drive impedance.	30
20	Coupled line Doherty Combiner EM vs Ideal transmission Line Simulated Loss	31
21	Routing Parasitic Effects Illustrated[33]	32
22	Metal contact plan for Field Effect Transistor (FET) drain/source connections	34
23	The Two Types of FET Cells used in the FET manifold with contacts brought up to higher metal layers	35
24	f_{max} vs Current density of a unit cell transistor	36
25	Schematic of the three FET stack used in this project	37
26	First Attempt Transistor Manifold Layout, Layout A	39
27	Second Attempt Transistor Manifold Layout, Layout B	40
28	Dual Gate Contact Transistor Manifold Layout, Layout C	41
29	Loadpull Results of manifold style C PA	43
30	Block level schematic of the amplifier simulated with rectangles highlighting the portions that have been EM simulated	44
31	The Two Types of FET Cells used in the FET manifold	45
32	The μ and μ' factors of the PA	47
33	PAE of Schematic level Doherty amplifier over 26, 28, and 30GHz	48
34	layout of input of Doherty PA	49
35	layout of total Doherty PA	50
36	Image of test setup in lab	51
37	Die being probed on the bench	52
38	Measured input return losses of the two amplifier paths.	53

39	Measured and simulated input return losses of the two amplifier paths.	54
40	Measured and full em simulated small signal gain of the amplifier	55

Acronyms

C_{GD} Gate to Drain Parasitic Capacitance. 32, 40

C_{GS} Gate to Source Parasitic Capacitance. 32

I_{aux} Current supplied by the auxillary amplifier. 9

I_{main} Current supplied by the main amplifier. 9

I_{max} maximum drain current. 5, 6

P_{sat} Saturated output power. 6, 10, 36, 42

R_G Gate Access Resistance. 32, 33

R_{opt} Optimal Load Resistance for Desired Output Power or PAE. 5, 6

V_{DC} DC Voltage. 5

V_{DD} Drain supply voltage. 6

V_{DS} Drain to Source voltage. 35

V_{GS} Gate to Source voltage. 37

Z_{oe} even mode characteristic impedance of a coupled line section. 25, 26

Z_{oo} Odd mode characteristic impedance of a coupled line section. 25, 26

θ Electrical length of a coupled line section in radians. 25, 26

f_{max} Maximum operating frequency where unilateral gain is unity. 31, 32, 35,
36, 42, 58

f_t Maximum frequency where the current gain reaches unity. 31

gm Transconductance of FET. 32

ADS Advanced Design System - developed for high frequency mixed signal circuit design by Keysight. 28

BW A frequency range. 3

DPD A power amplifier linearization method where the signal is predistorted to compensate for the known nonlinear effects of the power amplifier. 3, 5, 7

EER Envelope Elimination and Restoration method of efficiency enhancement using phase and amplitude components of drive signal. 5, 8

EM Electro-Magnetic. 41, 42, 49

ET using the envelope of a modulated input signal to dynamically change the supply of the Power amplifier. i, 6–8

FEM Front End Module. 2, 56

FET Field Effect Transistor. iv, 8, 20, 31–34, 36–40, 42, 44, 53, 56

GF Semiconductor Foundry named Global Foundries. 27

HB Harmonic Balance - A large signal frequency domain simulator. 45, 48

PA Power Amplifier. iii, iv, ix, 1–3, 5, 7, 8, 10, 13–15, 17, 20, 22, 24, 31, 36, 38, 43–50, 56

PAE The percentage of power at the output relative to the input RF and DC power. 2, 3, 5–7, 11, 17, 19, 20, 41, 42, 45, 48

PAPR the ratio between the average and peak power of a modulated signal. 2, 6, 7

PDK Electronic tools for the simulation and layout of a semiconductor process.

49

QAM Quadrature Amplitude Modulation. 2

RF Radio Frequency. 1, 2, 51

RFSOI Radio Frequency optimized process in SOI provided by Global Foundries.

27

SNR The ratio of noise power to signal power, often given in dB. 1

SOI Silicone On Insulator - a transistor process. 34

WCDMA Style of communication network. 7

WIFI Wireless Fidelity, wireless area network based on the IEEE 802.11 standard. 2

1 Abstract

This thesis proposes a novel implementation of a Doherty power amplifier as a means to improve backed off power added efficiency when compared to a class B PA. The proposed Doherty output combiner boasts a 28.5% fractional bandwidth at a center frequency of 28GHz. The proposed Doherty amplifier was laid out and manufactured in 45nm RF SOI. The simulated version has a saturated output power of 21dBm and a backed off efficiency improvement of 7% compared to that of a comparable class AB amplifier with a peak PAE of 25%. While the final manufactured Doherty amplifier did not line up with simulated expectations the design of a novel Doherty combiner is shown in this thesis.

2 Acknowledgements

I would like to express my gratitude to my thesis supervisor John Rogers for his continued patience and support. Thank you for the opportunities and guidance you have provided. I would also like to thank Skyworks Solutions inc., without whom I would not have pursued a masters degree or have been able to do this work. Individuals at Skyworks such as Peter Chyurlia and Hassan Sarbishaei for their guidance and good humor throughout the process. To my father, how's this for procrastinating?

3 Introduction

3.1 Motivation

The continued demand for higher speed wireless communication has pushed the limits of what was possible with 4G standards. Sub 6GHz 5G and 5G mm-Wave communication standards have been proposed as a way to provide higher speeds and lower latency through higher carrier frequencies and broader bandwidths. The predicted data traffic of 2021 is to be three times that of 2016 [1]. With the roll-out of IMT-2020 almost here the arrival of Fifth Generation (5G) communication is immanent.[2]. Complementing the use of high-order modulation schemes will be the adoption of small cell densification, electronic beam forming, and the use of the millimeter-wave (mmWave) spectrum[3]. The adoption of all of these technologies will contribute to a higher channel capacity.

The size of antenna arrays shrinks at frequencies in the Ka band compared to lower cellular frequency bands, allowing for much larger array sizes. The use of larger array sizes helps to alleviate some of the challenges of using mmWave frequencies to communicate. These difficulties include the higher propagation loss, lower gain of single PA cells, lower antenna gain, and lower received Signal-to-Noise Ratio (SNR) due to array aperture size [4]. The major challenges of these higher frequencies will be gain and efficiency of the PA which constrain overall transmit power [3].

Using a large number of array cells comes at the cost of high power consumption. Combined with the fact that higher order modulation schemes have a higher Peak-to-Average Power Ratio (PAPR) means the peak efficiency of the Radio Frequency (RF) front end is underutilized.

3.2 The Role Of Power Amplifiers

The PA is a key part of an RF Front End Module (FEM) which takes care of the front end amplification, filtering and multiplexing of communication signals. The FEM plays a large role in the linearity, noise-figure and efficiency of the system, and PAs consume a large portion of its thermal and power budget. Department of defence and commercial mm-wave PAs can easily consume over half the overall system power [5]. Balancing the demands for linearity and efficiency in a FEM for different radios is important; this is especially true with PA design considerations. Mm-wave communication deployment has many barriers to overcome; efficiency and battery life extension are key concerns [3].

Different weight is given to efficiency or linearity of the PAs in a FEM depending on its application. For Wireless Fidelity (WIFI) routers linearity is paramount at the expense of efficiency [6]. Cellular handsets on the other hand prioritize having a high efficiency while maintaining an acceptable level of linearity.

3.3 High-Order Modulation Schemes and How they Effect Efficiency

High-order modulation signals are used to provide higher data rates but they come at the cost of larger Peak-to-Average Power Ratio (PAPR) signals. To maintain a linear output the power amplifier must be operated at a lower average output power than where it is most efficient. As the input drive power is reduced so that the PA is no longer saturated the Power Added Efficiency (PAE) drops dramatically. This higher PAPR causes there to be a large amount of time where the amplifier is delivering an output power far below its saturated power leading to a low average efficiency of the PA.

While using Quadrature Amplitude Modulation (QAM) and higher-order

modulation schemes allows for more bits/s per unit of Bandwidth (BW) [3], it requires a more linear PA to transmit the signal effectively. Because of this, highly nonlinear PAs are not used since they must be operated at such backed off power levels that the higher peak PAE is never realized. It is possible to use Digital Pre-Distortion (DPD) to improve the linearity of a higher efficiency class E or F PA but as the bandwidth and modulation complexity increases the power demands on the pre-distorter negate efficiency gains.

3.4 Thesis Outline

In this thesis a novel Doherty combiner is proposed and used in the design of a Doherty amplifier in 45nm RFSOI targeting the Ka band used in the proposed 5G communication standard. This Doherty combiner will help to address bandwidth limitations that are normally associated with the quarter wave transmission line of a classical Doherty amplifier.

Chapter two will outline the background and other methods to improving the backed off PAE of a power amplifier along with outlining other contributions to Doherty PA design at mmWave frequencies. Chapter three will present the Doherty amplifier design and simulation, the key differences in the Doherty combiner used in this work and, its development along with the transistor manifold design. Chapter four will cover the layout of the PA, measurement, back simulation to find causes for discrepancies in simulation compared to measurement. Chapter five presents conclusions from this work along with suggestions for future work on this topic.

3.5 Thesis Objective

The primary objective of this thesis is to implement a Doherty PA with novel Doherty combiner in the 45 nm RF-SOI from Global Foundries process with

the goal of 5G connectivity in the Ka-Band. In order to achieve this goal the novel combiner will be shown to work through simulation. Appropriate layout of the transistor unit cell and manifold so as to maintain high frequency gain is considered in this thesis. To test the idea of this novel Doherty circuit a Die is laid out and manufactured for testing.

4 Background

Improving the backed off efficiency of a power amplifier helps with the overall average efficiency of a radio system that transmits a signal with a peak to average ratio greater than one. Since the peak PAE of an amplifier occurs when it is fully saturated and in compression it cannot be used in this region for high data rate signals. For the majority of the operation of a PA the signal power will be below that required to fully saturate the PA. Therefore average PAE will be far less than the peak PAE of the amplifier.

4.1 Backed-off Efficiency Improvement

There are different methods by which the backed off efficiency of a PA can be improved. One method is to change the bias and supply voltage as a function of the input signal in the case of Envelope Tracking (ET) and Envelope Elimination and Restoration (EER). Another popular alternative is by using active load modulation to change the saturation point of the PA as a function of its input drive which is done in the case of an out-phasing or Doherty amplifier. In all of these methods the idea is to keep the PA near its saturation region while maintaining an acceptable level of linearity.

Many different theoretical approaches were proposed over the years but there are issues with implementing them practically, particularly in high volume production. DPD could help alleviate what is usually the largest issue with efficiency enhancement; linearity, high complexity and cost.[7]

The central theory of backed off efficiency improvements are to change an amplifiers saturation point at different input power levels. This will allow the peak power added efficiency to be achieved at different power levels. Consider an ideal class B amplifier with a load resistor resulting in a maximum signal $R_{opt} = 2 \frac{V_{DC}}{I_{max}}$. The fundamental component of the output is a sine wave with a

peak of $\frac{I_{max}}{2}$. The Saturated output power (P_{sat}) can be expressed as follows [8]:

$$P_{sat} = \frac{V_{DD}I_{max}}{4} \quad (1)$$

At peak output power the PAE would be $\pi/4$. Backing off the power by a factor of p we can state the PAE at that power backed off ratio is expressed as [8]:

$$PAE = \frac{\pi}{4p} \quad (2)$$

So a drop of 6dB ($p = 2$) in drive power would result in the efficiency dropping from 78.5% to 39.3%. One could adjust the load resistor relative to the power back-off and return to the peak efficiency. The load adjustment is [8]:

$$R_{opt} = \frac{V_{DD}}{I_{max}} 2p \quad (3)$$

The P_{sat} will then decrease with this new load resistance to [8]:

$$P_{sat} \approx \frac{V_{DD}I_{max}}{4p} \quad (4)$$

4.1.1 Envelope Tracking (ET)

Envelope tracking has continued to be used to achieve high efficiency in wireless transmitters with high PAPR. ET allows for greater power back-off by altering the supply voltage in Equation 3 to improve the average PAE. This technique

requires extra circuitry be added around a pre-existing PA [9]. The structure of an ET amplifier is to have a portion of the signal coupled away from the input path and filtered to find its envelope. The supply voltage of the amplifier is then modulated with the envelope of the input signal dynamically changing its saturation point. This topology can be implemented with a dynamic change in drain voltage or with discrete steps in supply voltage thus reducing circuit complexity[10]. The circuit topology is shown below in Figure 1

Figure 1: Typical Envelope Tracking Topology

Using this methodology the peak PAE can be achieved at multiple input power levels. By having the supply voltage track the input power of the amplifier the following PAE curves can be seen relative to the backed off power of the signal.

Utilizing this method it is possible to achieve efficiencies of up to 61% and 70% with Wide-band Code Division Multiple Access (WCDMA) signals exceeding a PAPR of 6.6dB [7], [10].

The effect of modulating a supply voltage can cause issues with linearity that is normally overlooked and assumed to be solved with DPD[9], [11]. When

the supply voltage is purposefully changed in the pursuit of higher efficiency it makes the job of DPD far more complex[7]. Implementing DPD in broader bandwidth modulation schemes such as those proposed for 5G would mean the DPD engine would consume significant power. This broader bandwidth also puts demand on the supply modulation circuitry as it must handle this higher bandwidth demand while still providing enough voltage and current for the PA [12]. This supply bandwidth limitation hampers the effectiveness of this approach for 5G applications.

4.1.2 Classic Doherty Amplifier Topology

The Doherty amplifier topology, originally introduced in 1936 provides an elegant method of improving back-off efficiency through active load modulation. When compared to EER and ET the Doherty amplifier does not require as many complex system components.

The concept behind the Doherty backoff efficiency enhancement is to have one amplifier that will saturate at two different output levels. This is done through active load modulation. If the load that the power FET drives is halved then the saturation point of the PA doubles[7].

Active load modulation is when the voltage across a current source is changed without changing the actual load impedance. Consider two voltage controlled current sources controlled by the same input voltage. The current sources; I_{main} and I_{aux} both drive a resistor R_L .

Figure 2: Current sources representing the main and peaking amplifier in a Doherty PA topology [7]

If at first I_{aux} provides no current, the voltage across R_L can be expressed as:

$$V = R_L I_{main} \quad (5)$$

Therefore the load experienced by the current source I_{main} can be expressed as:

$$Z_{main} = \frac{V}{I_{main}} \quad (6)$$

Now if I_{aux} and I_{main} both provide current to the load resistor the voltage can be expressed as:

$$V = R_L (I_{main} + I_{aux}) \quad (7)$$

using this expression for voltage in (6) the load experienced by the current source is:

$$Z_{main} = \frac{R_L (I_{main} + I_{aux})}{I_{main}} \quad (8)$$

The output of a transistor in a power amplifier to a first degree can be approximated as a controlled current source with a high output impedance.

This current source is normally then matched to the system impedance. So this phenomenon could be used by two transistors driving a load. If the transistors were to be sized equally the effective impedance loading the main transistor would change from R_L to $2R_L$ as the auxiliary transistor is turned on. If the biasing of the auxiliary transistor is done in a way that allows the main PA to saturate before the auxiliary transistor conducts then the main transistor would be presented with a different impedance once it begins to saturate.

If the saturated output power of a power amplifier to a first degree is expressed as:

$$P_{sat} = \frac{V_{DD}^2}{2R_L} \quad (9)$$

Then having the main PA be presented with a larger impedance once it is in saturation is not helpful as it would push the amplifier further into saturation. By using a matching network that provides an impedance transform equivalent to a quarter wavelength line, inverting the impedance presented to the main transistor; the main transistor will be presented with an impedance that will either be the load resistance or one half of the load impedance depending on the drive level of the auxiliary transistor. Generally speaking this impedance inverting network is implemented with a quarter wave transmission line. To ensure proper power combining at the load the phase shift caused by the impedance inversion network must be compensated by a phase shift at the input of the auxiliary path.

An example of a Doherty topology is shown in Figure 3. The main current source is presented with a quarter wave transmission line before the load which the auxiliary PA feeds directly. This offset allows for the appropriate load modulation. In this ideal case the auxiliary amplifier will not conduct until the main PA is approaching saturation.

Figure 3: Typical Doherty Amplifier Topology

For a classic Doherty amplifier the main and auxiliary amplifier is combined such that the load of the main amplifier at a specified backoff is more than the load at saturation by a decibel factor of γ . This load modulation is achieved with a Doherty combiner that inverts the impedance of the auxiliary amplifier. The backoff power factor γ is then related to the ratio of device peripheries α by the function[13].

$$\alpha = \sqrt{\gamma} - 1 \quad (10)$$

In a classical Doherty configuration α and γ would be 1 and 6dB respectively which would relate to identically sized devices for the amplifiers. This is because both the main and auxiliary amplifier are contributing equally to the saturated output power of the total Doherty amplifier.

The delay in load modulation can be done by leaving the auxiliary amplifier in a class C operating mode so it does not turn on until significant power is applied. Once backoff exceeds 6dB the auxiliary device ideally will turn off completely effectively halving the device size. This further improves PAE at low power levels. The combined output power is then a linear relationship with the input power. In reality if the combiner shows any loss through the paths that is not equal or the auxiliary amplifier turn-on characteristics are not ideal

this phenomenon will diminish quickly.

The classic and arguably simplest example of a Doherty topology is shown in Figure 3. The main amplifier is presented with a quarter wave transmission line before the load which the carrier feeds directly. This offset allows for the appropriate load modulation. In this ideal case the auxiliary amplifier will not conduct until the main amplifier is approaching saturation causing an increase in backed off PAE enhancement as shown in Figure 4 below.

Figure 4: Ideal Doherty PAE and Device current draw [7]

The original Doherty topology utilized tubes which gave the designer more control over the trans-conductance and maximum drain current [7]. These methods allow for better control over the behavior of the main and auxiliary amplifier. Practically speaking in a modern application the main amplifier could be realized with a class B PA. The use of a linear class C amplifier as a peaking device

would result in the auxiliary amplifier having a more sluggish turn on characteristic. This will lead to a variation in the main PA voltage after the peaking PA turns on causing a reduction of peak PAE. This will necessitate reducing the load impedance to maintain appropriate voltage swing. This causes the PAE roll-off to resemble that of a Class B PA. Figure 5 illustrates the PAE curves of an ideal Doherty amplifier when implemented with class B and C power amplifiers.

Figure 5: PAE curve of ideal Doherty when implemented with Class B and C Amplifiers [7]

Another solution would be to increase the size of the auxiliary device but this leads to a lower PAE of the auxiliary that detracts from the Doherty action [7]. One method of resolving this anemic supply of current from the auxiliary

amplifier is to accept that the Doherty action will not provide the twin peak PAE curve that is expected in the ideal example. Along with the fact that the turn on characteristics of the Auxiliary device will be non-linear causes the PAE curve to be drastically different. It is important to remember that there is still a benefit to the backoff power efficiency While this is not ideal it does still provide a benefit at power backoff relative to a Class AB PA [12].

Figure 6: PAE curve of Doherty when implemented with nonlinear Class B and C Amplifiers [7]

For the scope of this thesis the issue of auxiliary amplifier turn on approaches will not be addressed as solutions to the turn on characteristics of the peaking amplifier are vast.

4.2 Doherty Combiner

The Doherty combiner is the basis of the Doherty amplifier topology. The Doherty combiner serves two purposes to facilitate the Doherty amplifier topology: First, it combines the power of both the peaking and carrier amplifier at its output and second, it provides a method for the main amplifier to have its load modulated by the auxiliary amplifier. The optional third function a Doherty combiner can serve is to transform the load the Doherty PA is driving from what is normally 50 ohms into a different load impedance to realize the desired output power. Figure 7 below is an example of the classic Doherty combiner serving all three purposes by utilizing quarter wave transmission lines.

Figure 7: Coupled line Doherty Combiner

This straightforward version of the Doherty combiner has been implemented in PCBs [14] and lumped elements at lower frequencies for solving backoff efficiency issues in other communication standards [15].

Since the classic Doherty combiner requires the use of transmission lines that are related to the wavelength, the combiners are often large and lossy. Another issue with using quarter wave transmission lines as transformers is the bandwidth limitations that it brings[16]. Alternatives are proposed to provide ways of integrating the Doherty combiner in the PA die. Such suggestions include using lumped elements to create the required transmission lines to reduce

size. Since the size of a transmission line combiner depends on the wavelength of the band of interest using lumped elements can at times consume less space than the transmission line. Other implementations such as transformer based combiners[17], [18] provide a bandwidth and size advantage.

4.3 Works in Doherty Amplifiers at mmWave Frequencies

Backed off efficiency enhancement at mmWave frequencies have been explored in recent years most of which target the Ka band for emerging 5G standards. However Doherty based techniques are by far the most popular as they do not require high-speed/high-precision supply modulators or high speed baseband computation[19].

The following work by Giofrè in [20] was realized on a Gallium Nitride on Silicon (GaN-Si) technology with 100nm Gate lengths. The input splitter was implemented with a simple T-Junction while the output Doherty combiner was implemented with transmission lines.

Figure 8: Doherty Amplifier Topology implemented in [20] where IMN is the input matching network, PCN and IIN are delay lines, ISMN is the inter-stage matching network of each amplifier, and the OMN is the output matching network

Figure 8 shows the topology used by Giofrè in [20] to achieve a two watt saturated output power and a 6dB backed-off PAE of 30%. This amplifier was laid out with full transmission lines and consumes a die area of $6mm^2$. The amplifier was observed to have a frequency range from 27 to 29GHz.

The splitting and input phase offset of a Doherty amplifier can result in a loss of bandwidth. The topology used by Nguyen in [21] attempts to resolve the loss of bandwidth using a configurable input network by way of a re-configurable hybrid coupler on the input. Figure 9 below shows the overall Doherty PA topology.

Figure 9: Doherty Amplifier Topology implemented in [21]

The input combiner proposed in [21] modifies the relative phase difference between the main and auxiliary amplifier inputs to improve bandwidth and backed off PAE. This work unlike [22] does not rely on digital circuitry to control relative input phase, but instead uses a meandering hybrid coupler originally proposed in [23] by attaching shunt varactors to the outputs of the coupler allowing for improved bandwidth. Figure 10 shows the input coupler used in [21] to modify the relative input phase of each amplifier.

Figure 10: Modified Hybrid Coupler Implemented in [21]

The use of the meandering coupler method is shown to achieve a backed off PAE improvement from 26.5 to 29.5GHz. The peak and 6dB backoff PAE were 42% and 31% respectively with a gain of 11.8 dB and a saturated output power of 26.5dBm.

While the majority of prior works are fabricated in III-V technologies due to breakdown voltage challenges for high frequency transistors, CMOS and SOI are becoming a popular alternative[24]. The rise in popularity of SOI processes being used for high power high frequency circuits is due to CMOS and SOI being more mature technologies, and its per-die affordability [25], [26]. Prior works in SOI include [27] and [24] where integrated solutions are proposed either through the use of transmission lines or lumped elements. Implementations at higher frequencies such as 45GHz use transmission lines for the combining network[24].

The use of a synthesised output combiner method originally proposed in [28] was implemented in 45nm RFSOI by Global Foundries with symmetric power devices. The combiner synthesis approach used allows the combiner to both achieve the Doherty load modulation and proper impedance matching while taking into account the output capacitances of the FETs. This synthesised combiner was found to have lower insertion loss than its conventional counterpart. Figure 11 shows the circuit diagram used in [27].

Figure 11: Schematic Diagram of Doherty Implemented in [27]

The use of this synthesised Doherty combiner achieved a peak and 6dB back-off PAE of 40% and 28% respectively with a frequency range from 25 to 31GHz.

The use of transformers to implement a Doherty combiner has been proposed as a method to integrate the Doherty combiner onto the PA die while increasing

bandwidth. Originally suggested in [29] as a lower loss method to integrate a Doherty combiner the author uses a set of differentially driven transformers to achieve Doherty action. Using ideal components it can be seen that the transformer based Doherty combiner can achieve a $22\ \Omega$ impedance transform with an ideal efficiency of 74%. Figure 12 is a diagram of the transformer based Doherty combiner.

Figure 12: Transformer Based Doherty combiner

The transformer based Doherty combiner uses the parallel-series transformers to achieve the required phase shift and power combining requirements. The scattering matrix is shown below where M is the coupling factor of the transformers [17].

$$\begin{bmatrix} V_{MAIN} \\ V_{AUX} \\ V_{OUT} \end{bmatrix} = \begin{bmatrix} R_1 + j\omega L_1 & 0 & j\omega M \\ 0 & R_2 + j\omega L_2 & j\omega M \\ j\omega M & j\omega M & 2(R_2 + j\omega L_2) \end{bmatrix} \begin{bmatrix} I_{MAIN} \\ I_{AUX} \\ I_{OUT} \end{bmatrix} \quad (11)$$

Using this technique the combiner can achieve a 74% efficiency[29]. This topology was implemented in 90nm CMOS technology at 2.4GHz in [29]. The power amplifier built on this approach had a saturated output power of 20.5dBm and a PAE of 26.7% with a 10.8% backed off efficiency enhancement when compared to a normalized class B PA [29].

This technique of using a transformer based combiner was also implemented for use in the Ka band by Yen-Chin Chen in [30] in a 90nm CMOS process. The proposed design utilized two stage differential PAs for the main and auxiliary amplifiers with an adaptive bias network to improve the auxiliary turn on voltage. Figure 13 below shows a block diagram of the circuit used in [30].

Figure 13: Transformer Based Doherty combiner With adaptive biasing circuit to enhance turn on characteristics of auxiliary PA

This differential approach is able to achieve a 6dB backed off power added efficiency of 1.72 times that of a normalized class B PA (a PAE of 12.5%) with a frequency range from 29 to 42GHz. The use of transformers as a combining network was leveraged as a method of compensating for the low output impedance

of the auxiliary amplifier at this higher frequency range. This effective increase in output impedance helps to improve power leakage to the auxiliary amplifier [30].

5 Design

The novel Doherty combiner is designed from first principles by creating a mathematical model of the coupled lines sections as they relate to the impedance presented at each of the amplifiers output planes. The combiner is then simulated and laid out in an SOI metal stackup. Consideration was made to the method in which the FET array is laid out since at mmWave frequencies this will have an impact on RF performance.

5.1 Coupled Line Combiner

The difficulty with transformers at high frequencies is low self resonance when integrated on chip. Utilizing coupled lines in place of transformers it is possible to create a relatively wideband Doherty combiner. Figure 19 below is a diagram of the coupled line combiner topology.

Figure 14: Coupled line Doherty combiner

The combiner is made up of two coupled line sections. The first section (A) connects the main amplifier, load impedance and second coupled line. The second section(B) connects to the auxiliary amplifier. The coupled line combiner can also be used as the DC supply feed for the main and peaking PAs provided there is sufficient supply decoupling. The mathematical justification for this

combiner will be provided in the next section.

The impedance relations can be found using a general Equation matrix for coupled lines from Pozar [31].

Figure 15: Generic coupled line segment

The impedance matrix is found using the odd mode impedance, even mode impedances, and the electrical length of the transmission line segment; Z_{oo} , Z_{oe} , and θ respectively.

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} & Z_{14} \\ Z_{21} & Z_{22} & Z_{23} & Z_{24} \\ Z_{31} & Z_{32} & Z_{33} & Z_{34} \\ Z_{41} & Z_{42} & Z_{43} & Z_{44} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} \quad (12)$$

Where the Z parameters of the matrix are defined as:

$$Z_{11} = Z_{22} = Z_{33} = Z_{44} = \frac{-i}{2}(Z_{oe} + Z_{oo})\cot(\theta) \quad (13)$$

$$Z_{12} = Z_{21} = Z_{43} = Z_{34} = \frac{-i}{2}(Z_{oe} - Z_{oo})\cot(\theta) \quad (14)$$

$$Z_{13} = Z_{31} = Z_{24} = Z_{42} = \frac{-i}{2}(Z_{oe} - Z_{oo})\csc(\theta) \quad (15)$$

$$Z_{14} = Z_{41} = Z_{23} = Z_{32} = \frac{-i}{2}(Z_{oe} + Z_{oo})\csc(\theta) \quad (16)$$

The Z matrices are then reduced to two by two Z matrices by accounting for the terminations on the additional ports. These Z matrices were then converted to ABCD matrices to allow the overall response to be found. The shunt output capacitance of the transistors play a key role in resonating with the transmission lines and therefore must be accounted for even in the ideal case. Using the ABCD parameters for the shunt capacitance presented by the transistors outputs the entire system is now accounted for. The reference plane is set to the interface between the carrier amplifier output and the combiner network. The impedance found relative to the current driven by the auxiliary amplifier was then plotted in matlab, using the code shown in Appendix A.

(a) Real Load Modulation of Main Amplifier (b) Imaginary Load Modulation of Main Amplifier

Figure 16: Load Modulation of Main Amplifier

One can observe the load modulation transform as the load modulates from 40 to 20 ohms over a 28% bandwidth. This was achieved by selecting the

following parameters for the combiner and knowing the output capacitance of the main and auxiliary transistor was 200 fF. The output capacitance of the main and auxiliary transistor were determined with a simple scattering parameter test bench covered in chapter 5.10.

Parameter	Value
$Z_{odd} (\Omega)$	100
$Z_{oeven} (\Omega)$	12.5
$Z_{load} (\Omega)$	25

Table 1: Impedances chosen for ideal combiner

See appendix for full matlab code.

5.2 Combiner Layout and Simulation

The combiner was laid out on the three uppermost layers of metal in the Global Foundries (GF) 45nm Radio Frequency Silicone on Insulator (RFSOI) process. These layers were chosen as they had the largest width rule allowances and lowest loss due to their thickness. The width is necessary to achieve the appropriate the odd and even mode impedances for the coupled line segments. While it might have been possible to achieve a similar set of coupled lines on the lower levels, the higher loss of the lower metal layers and layout techniques that would be required to have appropriate odd and even mode impedances while also following the processes design rules would be unnecessarily complicated.

The combiner is folded so it can be accommodated on die since its unfolded length is over 700um. The folding of the combiner had minimal effect on RF performance while also being easier to accommodate on die. An indent is made in the folded combiner to make space for VDD decoupling capacitors that can attach to the ground ring of the combiner. The layout needed to have enough space near the grounding terminations to provide decoupling capacitors since those nodes will provide a DC path for the drain voltage on the main and

auxiliary amplifiers. Figure 19 below shows the final folded combiner layout.

Figure 17: Coupled Line Doherty Combiner Laid out in GF 45nm RFSOI

The Advanced Design System (ADS) multi layer line instance was used to find approximate dimensions of the desired transmission lines using ADS LineCalc tool. The combiner was then simulated using an AC simulation test bench where the main path was driven with a 1A ideal current source and the auxiliary path was driven with a swept ideal current source that ranged from 0 to 1 A. The main path impedance was monitored to observe the active impedance transform as the auxiliary current source increased. This is a simple method to test Doherty amplifiers in a simulator. Figure 18 below shows the test bench used to characterize the combiners.

Figure 18: Circuit used to characterize the Doherty action of the Combiners

The multi layer line idealized version of the combiner was then compared to the EM simulated layout of the combiner. Figure 19 Below shows the main amplifiers load modulation in both the coupled line model and EM simulated layout.

Figure 19: Coupled line Doherty Combiner EM vs Ideal transmission Line Simulated Load Modulation where m1 and m3 are the backed off loading of the main amplifier and m2 and m4 are the full drive impedance.

The load modulation is only half the story, the combiners loss over frequency and load modulation dictates how practical it can be. Figure 20 shows the combiner loss of the ideal transmission line combiner compared to the EMX simulated combiner.

Figure 20: Coupled line Doherty Combiner EM vs Ideal transmission Line Simulated Loss

One can see from Figures 19 and 20 that the proposed combiner provides approximately a 25% marginal bandwidth with a 77.6% efficiency.

5.3 Transistor Manifold Design

While the base transistor for any process is rated to a specific f_{max} by the foundry, the layout of any manifold that is attached to the transistor adds parasitics which impact its actual performance. Transistors have been measured with f_t s as high as 485GHz when using the lowest metal as a connection [32]. For PA designs the signal must pass through higher, thicker metal layers to handle the current that is being drawn. The designer must then attempt to maintain as much of the FET performance as possible while laying out their circuit in a practical fashion.

5.4 Theory

Considering a single transistor and the parasitic components that surround it, a first order relationship between f_{max} and parasitic elements shown in the

equation [33]. The parasitic capacitances are C_{gd} and C_{gdx} ; the gate-source capacitance and the drain source capacitance incurred through metal routing respectively, C_{gs} and C_{gsx} ; the gate-source capacitance and the drain source capacitance incurred through metal routing respectively. The parasitic resistances R_g , R_s , and R_d are access resistances to the gate, source, and drain respectively.

$$f_{max} = \frac{1}{4\pi} \sqrt{\frac{gm}{R_G C_{GD} (C_{GS} + C_{GD})}} \quad (17)$$

Knowing this, careful consideration must be taken in how to connect all the FET contacts for each gate to preserve as much of the frequency performance as possible. Parasitic capacitance is added as the gate, drain, and source contacts are connected to the higher level metals. Figure 21 below illustrates the effects of additional routing on adding to the paracitics of a FET array[32].

Figure 21: Routing Parasitic Effects Illustrated[33]

Inspecting Equation 17 the operating frequency of the transistor can be improved by the reduction of Gate Resistance (R_G) this can be done in a couple of ways. First, reducing the length of the individual gates would contribute to a reduced access resistance across the channel width. Second, contacting the gate of the FET from both sides reduces the gate access resistance by a factor of 4 as shown in Equation 18 when compared to 19 [8]. From a more intuitive perspective, not only are there twice the contact points to the gate but there is also effectively half the length of gate not contacted.

$$R_G = \frac{1}{12} \rho_s \frac{W}{L} \quad (18)$$

$$R_G = \frac{1}{3} \rho_s \frac{W}{L} \quad (19)$$

By adding an additional contact to the opposite side of the gate one can reduce the effect of Gate Resistance (R_G) by 4. This does come at the expense of additional gate to drain capacitance due to routing the additional gate contacts, but it will be determined in the next section that the trade-off of additional gate contacts is favorable.

Since the drain to source spacing on this 45nm gate width process is only 300nm and the three contacting metals combined are 450nm tall, the incurred source drain capacitance through how these metals are routed to the drain and source contacts of the FETs. Because of this the way in which the transistors are contacted by lower routing metals is worth careful consideration.

In order to mitigate source and drain contacts creating more parasitic capacitance the metal layers that contact them are stacked progressively to avoid the drain metal contacts from being adjacent to the source metal contacts. The

three lowest metals in this seven metal process are the only ones that can be narrow enough to contact the individual source and drain contacts. Figure 22 below shows a top down and side view of the metal contact plan for the drain and source.

Figure 22: Metal contact plan for FET drain/source connections

The FET stack is made from three 45nm Silicone On Insulator (SOI) FETs to take advantage of a larger supply voltage. The amount of gate area needed to handle the high current a power amplifier will need is vast. Because of that the FET stack is made up of multiple 20 finger 2.5 micron FET sub-cells.

Figure 23: The Two Types of FET Cells used in the FET manifold with contacts brought up to higher metal layers

5.5 Biasing of transistors

The transistor biasing was chosen based on the highest f_{max} of a single transistor. The transistors would be stacked as three to ensure the max V_{DS} was not exceeded. Assuming that the 2.5V supply voltage was equally distributed across each transistor a unit cell transistor was tested for f_{max} against current density using a drain source voltage of 0.83V. Figure 24 below shows the results of that simulation.

```

m1
indep(m1)=698E-4
plot_vs(fmax, CurrentDensity)=2.883E11
Vlow=0.475

```

Figure 24: f_{max} vs Current density of a unit cell transistor

The current density of $0.26 \text{ mA } \mu\text{m}^{-1}$ was chosen as it provides the best possible f_{max} for a given unit cell transistor.

The FETs for the two PAs will be stacked as three transistors to allow for a supply voltage of 2.5 V. This allows for a larger loading impedance to achieve P_{sat} . Below shows a simple schematic of the three FET stack.

Figure 25: Schematic of the three FET stack used in this project

Since there will be a stack of three transistors the bias for each individual transistor will be chosen to maintain a V_{GS} of 0.833 V across them. The three transistors M1, M2, M3 are biased with a voltage of 0.475 V, 1.31 V, and 2.14 V respectively. The bias voltage for these transistors will be supplied by a resistor of 300 k Ω to ensure no RF current ends up on the bias lines. Since the project is using FETs, the impact of this additional resistance in the dc bias path has minimal impact on biasing.

The size of the transistor was chosen based on the current handling specifications for the metals contacting the drain and sources. The lower four metal layers that contacts the FETs have a combined current handling capability of 0.55 mA/finger at 130 °C. The desired output power from each PA is 20dBm. So ideally the load resistance and by extension, peak drain current can be determined using the Equation 20.

$$I_{max} = \frac{4P_{out}}{V_{DD}} \quad (20)$$

The transistors were then oversized to provide additional ruggedness protection and help resonate out the combiner lines to achieve appropriate load modulation.

The full sized FETs were made up of the unit cell transistors. How these unit cells were connected was then found through an experimental process using the EM extracted results from different layout methods as discussed in Section 5.6

5.6 Layout Comparison

Three layouts were compared in this design. Each trying to mitigate different parasitic effects caused by the manifold layout. The FET stack was made from three SOI FETs the upper most array of which is a thick oxide variant that has higher ruggedness. The first layout, layout A was a straightforward iteration with minimal considerations for gate contact while trying to reduce the distance between each FET in order to keep the layout compact and neat. The decoupling capacitors for the upper transistors were chosen to be beside the FET array. Layout A is shown below in figure 26.

Figure 26: First Attempt Transistor Manifold Layout, Layout A

This layout is not complex and because of this, has some issues regarding the access impedance to the decoupling capacitors on the gate contacts of M2 and M3. The length from the gate contact of each finger of its respective decoupling capacitor is fairly long and could lead to ineffective decoupling of the upper gates.

The second iteration of the transistor array was focused on gate decoupling and even more grounding of the source and upper gate decoupling capacitors. Layout B was chosen to have the gate decoupling capacitors placed between the FETs to increase the effective Q of the decoupling capacitors and allow a more even effective capacitance to be presented to each fingers gate. The area above of the FET manifold was filled with with higher level metals to provide a better return path to ground.

Figure 27: Second Attempt Transistor Manifold Layout, Layout B

Layout C was created taking advantage of the double sided gate contact option in the provided Pcell FETs. This reduces the access resistance of the gates of the transistors at the risk of increasing C_{GD} . To reduce C_{GD} the drain to source connections were implemented on higher metal layers to increase the space between those and the gate contact routing layers. The decoupling capacitors were implemented on just one side after initial tweaking with how the return paths would affect the stability of the FET stack. Another advantage to layout C is the more distributed devices mean a larger area to dissipate heat.

Figure 28: Dual Gate Contact Transistor Manifold Layout, Layout C

5.7 Simulation Comparison

The three layouts were then simulated using EMX by Cadance, a two and a half Electro-Magnetic (EM) simulator based on Maxwells equations [34]. This type of simulator is used to capture the EM effects caused by the different layouts and how it affected performance. The simplest method to compare the three transistor manifolds was to load-pull simulate each to find the maximum possible saturated power and PAE. This is because the manifolds could cause

the ideal impedance to provide maximum P_{sat} to change.

The transistors and their parasitic metal contacts were extracted up until the third metal layer for the individual twenty finger FET unit cells. All layout above the third metal was EM simulated to observe how the connection of the FET unit cells would affect overall performance.

The double gate contact manifold yielded higher PAE and P_{sat} in the load-pull simulation and therefore was considered the best option. It did take up slightly more area but compared to the size of the combiner it is acceptable.

Parameter	Manifold A	Manifold B	Manifold C
f_{max} (GHz)	142.3	141.6	227.1
P_{sat} (dBm)	18.97	19.75	20.07

Table 2: Tabulated results of P_{sat} and f_{max} simulation tests

Observing the f_{max} and P_{sat} results above it was concluded that Manifold style C is the best for this application. The loadpull simulation of manifold C concluded that the P_{sat} of 20.07dBm can be achieved at $(11.3 + 9.3i) \Omega$.

PAE (thick) and Delivered Power (thin) Contours

indep(PAE_contours_p) (0.000 to 27.000)
indep(Pdel_contours_p) (0.000 to 25.000)

m2
indep(m2)=1
Pdel_contours_p=0.642 / 157.813
level=20.057, number=1
impedance = 11.301 + j9.320

Figure 29: Loadpull Results of manifold style C PA

5.8 Top level PA Simulation

Having the FET manifold and Doherty combiner laid out and extracted, a full simulation of the Doherty PA can be done. First, the PA building blocks determined in the above sections were placed in a block level schematic along with lumped elements having finite Q-factors.

Figure 30: Block level schematic of the amplifier simulated with rectangles highlighting the portions that have been EM simulated

The input match was achieved with a simple single pole series capacitor shunt inductor topology. The required phase shift at the input of the carrier amplifier was implemented with a $50\ \Omega$ transmission line with an electrical length of 45 degrees at 28 GHz.

The PA was simulated using a large signal and small signal test bench to evaluate performance and ensure stability. The parameters simulated in the

small signal test bench were the input match and stability. The large signal simulation was done using a Harmonic Balance (HB) simulation engine and PAE relative to an ideal class AB PA over output power.

5.8.1 Small Signal Simulation

The small signal input impedance of the block level Doherty PA were determined using the following test bench with an individual test port for the main and auxiliary amplifier respectively since the splitting will occur off die. Figure 31 below shows the input reflection coefficients of the main and auxiliary amplifiers.

(a) Reflection coefficient of the Main amplifier (b) Reflection coefficient of the Auxiliary amplifier

Figure 31: The Two Types of FET Cells used in the FET manifold

As shown above the main and peaking amplifiers are reasonably matched at 28GHz. Another important small signal parameter would be determining the

PAs stability. Small signal stability of PAs is usually determined using two port metrics such as a K-delta test or using the the metrics μ , and μ' [31]. Since the input split was to be achieved off die using a Wilkinson splitter on the lab bench, an ideal lossless RF splitter was used to determine the two port stability in simulation. This was determined using the factors μ and μ' to indicate that the input and output are unconditionally stable. This is because μ and μ' measure the distance from the center of the smith chart at the output and input of the amplifier to the nearest point of instability. Figure 32 below shows the stability parameters discussed, the simulation range encompasses the frequency range over which the transistors used might have gain.

Figure 32: The μ and μ' factors of the PA

Observing Figure 32 above one can conclude that the block level schematic of the PA is stable so far but will need to be checked under more severe circumstances later on.

5.8.2 Large Signal Simulation

Using a HB simulation test bench the Doherty amplifier was simulated.

Figure 33 below shows the PAE performance of the Doherty amplifier. Note the matching coloured traces on the PAE plot that represent the PAE curve of a standard class B PA normalized to the compressed PAE of the Doherty for comparison on backed off efficiency enhancement.

Figure 33: PAE of Schematic level Doherty amplifier over 26, 28, and 30GHz

It can be seen that the Doherty amplifier does provide a backed off PAE advantage over a normalized class B PA. The Gain saturation curve can be shown below as the PA is simulated over three tones; 26, 28, and 30GHz. it can be observed that the Doherty PA has a saturated output power of 21dBm.

6 Layout

The Doherty Power amplifier was then laid out using the provided Process Development Kit (PDK). The size of the layout was determined by the size of the 5 pin signal-ground-signal-ground-signal (SGSGS) probe wedge needed to bias the transistor stack along with the 5 pin ground-signal-ground-signal-ground (GSGSG) probe wedge for the main and auxiliary amplifier RF inputs. The input offset lines had to be adjusted to allow for the delay in routing to the transistor manifold input. The delay lines dimensions and spacing from the ground metals were verified to be 50 ohms at 28GHz using a sample length of line EM simulated separately. The shunt inductors needed for input matching the transistors were implemented using narrow lines to the ground area. The excess area was flooded with thick metal layers to improve signal return and reduce ground inductance.

Figure 34: layout of input of Doherty PA

The output combiner was laid out with the addition of a series inductor and shunt capacitor connecting the combiner output to the RF out pins. This is to adjust the impedance presented at the output of the combiner to be 25Ω for appropriate loads.

Figure 35: layout of total Doherty PA

7 Testing of the Doherty Power Amplifier

The amplifier was probe tested at Skyworks Solutions inc. using a series of probe wedges to provide both DC bias voltages and the RF input signals. The input of the Doherty is driven through a 5 pin GSGSG RF probe wedge with a high frequency source that is split by a wilkinson power divider. The output will be observed using a spectrum analyzer connected to a GSG RF probe at the output.

Figure 36: Image of test setup in lab

The die being contacted by the probe tips can be seen below in image 37.

Figure 37: Die being probed on the bench

The S-Parameters were determined by two ports of a four port Keysight network analyzer attached to the probe setup. The first input port was split evenly using a Wilkinson divider to attempt to provide even amplitude and phase to the two inputs. The calibration of the S-parameter test involved characterizing and de-embedding the probe tips. since there was no existing calibration structure available to calibrate the two input probes to a single output probe an approximate characterization was done. Only one RF path of the input GSGSG probe head was calibrated at a time, the resulting S-parameter files were averaged. The S-Parameters were taken at each of the inputs to the Doherty amplifier while terminating the other with a 50Ω termination. The input cables were similarly averaged as they were the same length and diameter. Below shows the input return loss of the main and auxiliary amplifier.

Figure 38: Measured input return losses of the two amplifier paths.

This does not align with the desired input insertion loss. the strange shape of the auxiliary amplifiers input return loss over frequency suggests that the calibration of the bench is off for the auxiliary path. The calibration and de-embedding of the probe station were re-done and the insertion loss of a near short from a single ended to single ended calibration structure was checked for both the main to RF out and auxiliary to RF out path but the insertion loss was 3dB through each path. The DC parameters of the amplifier were verified against that of the simulated Amp and were similar. This indicates there was an issue instead with the RF path of the circuit. Since the components were individually simulated with ideal interconnects between the input matching networks, FET stacks, supply decoupling, and Doherty combiner it is likely that the layout of all these parts and a perturbed return path for the RF signal is causing issues. Access to the lab bench was time limited and further debugging of the measurement results was not able to be done due to time limitations.

7.0.1 Small Signal Simulation of overall Doherty Amplifier

The input S11 of the main and auxiliary amplifiers were compared to that of the measured results. Below is a plot of the measured and full EM simulated input return losses of the amplifier inputs.

Figure 39: Measured and simulated input return losses of the two amplifier paths.

While different than that of the measured results this may be due to the inaccuracies of the calibration on both probe tips being electrically symmetrical at 28GHz. Comparing the gain of the measured amplifier against that of the simulated counterpart in Figure 40 shows that there is some discrepancy not captured. This could be that the test probes and splitter are not properly de-embedded or that the measurement results are incorrect in some fashion.

Figure 40: Measured and full em simulated small signal gain of the amplifier

The individual components of this thesis worked separately so the issue stems from how the full die layout was executed. With time constraints and the inability to enter the lab or office due to current limitations on lab access properly testing and fully capturing the causes of the discrepancies was not possible. If there were more time with access to the lab more work would be done to ensure all RF paths to and from the die were de-embedded along with insuring the main and auxiliary RF inputs were perfectly phase and amplitude aligned using a variable phase shifter and attenuator.

7.1 Future Work

The primary improvement would be to fix the current layout to ensure the PA operates as intended. The first step in this would be to re-design the amplifier from broken out FET stack, combiner, and input matching network to find a better implementation in layout. Moving forward, the sizing of devices for the main and peaking FET arrays could be optimized to improve PAE. A more compact or easy to implement combiner layout could be determined. This Doherty PA will need a broader bandwidth input match to fully take advantage of the output combiners improvement with regards to bandwidth. The use of an input driver on both the main and auxiliary amplifier will allow the PA to be implemented in a more practical sense. At higher frequencies differential amplifiers are used to improve return path loss, if the technique of using coupled transmission lines can be used to create a differential combiner then it could find its way into mmWave FEMs.

Implementing this Doherty amplifier in a flip chip configuration could be done although it would likely require a redesign of the output matching network along with some layout changes to accommodate the grounding bumps that one would want directly above the RF transistor manifolds to improve both source grounding and thermal sinking. The addition of the bumps to ground the sources of the FET stack would likely result in changes necessary to the output combiner and matching network since the loading of the main and auxiliary ports of the Doherty combiner. While it would be possible to do this work it would likely be best to have a functional prototype die that is probed first as the changes that would need to be made would likely be extensive.

The use of a multi-pole match for the input would greatly increase the bandwidth of the amplifier as it is currently a major limiting factor of the bandwidth of the simulated amplifier. This work could be combined with the design of an

on the input splitter to provide appropriately phased input signals to both the main and auxiliary amplifier. Doing both of these design activities at the same time could help with bandwidth improvement of the input matching network.

Originally the single-pole match was considered acceptable to allow for faster layout with less iteration but after isolating the combiner and output match in the full layout it can be seen that the bandwidth of the combiner when attached to the single pole output match from 25 to 50 Ω deteriorated the loading of the carrier amplifier along with the insertion loss of the combiner and matching network over frequency.

8 Conclusion

This thesis provided the mathematical proof (in appendix) and design of a mmWave Doherty combiner that would provide a backoff PAE improvement relative to a class AB amplifier of the same periphery. There is further work needed to tape out a functional die as the full layout of the amplifier must be revisited.

8.1 Thesis Contributions

The major contribution of this thesis is the proposed use of integrated coupled transmission lines to achieve Doherty combining action over a 28% bandwidth. Another contribution of this work is the development of a high f_{max} transistor manifold to maintain high gain at mmWave frequencies. The novelty of implementing a Doherty combiner with coupled lines is being patented by Skyworks Solutions inc application number 17/249328.

References

- [1] CISCO. “Global - 2021 Forecast Highlights”. In: *VNI Complete Forecast Highlights* (2016). Accesed 2021, https://www.cisco.com/c/dam/m/en_us/solutions/service-provider/vni-forecast-highlights/pdf/Global_2021_Forecast_Highlights.pdf.
- [2] International Telecommunication Union. “5G roadmap: challanges and opportunities ahead”. In: (2017). Accesed 2020, https://www.itu.int/en/ITU-R/seminars/rrs/RRS-17-Americas/Documents/Forum/1_ITU%20Joaquin%20Restrepo.pdf.
- [3] P. Gammel, D. Pehlke, D. Brunel, et al. *5G in Perspective A Pragmatic Guide to Whats Next*. Tech. rep. Woburn, MA, 2014.
- [4] Hossein Niknejad Ali M. Hashemi. *Advanced Techniques in RF Power Amplifier Design*. Norwood, MA: Artech House, 2002.
- [5] Tsay, J. Mayeda, J. Lopez, et al. “Broadband High-Efficiency mm-Wave 2.4-42.5GHz SiGe PA Design Using Stacked Versus Cascaded Topologies”. In: *IEEE Texas Symposium on Wireless and Microwave Circuits and Systems*. Texas, 2019.
- [6] Yazhou Wang and Randy Naylor. “Challenges in designing 5 GHz 802.11ac WiFi power amplifiers”. In: *2014 IEEE Topical Conference on Power Amplifiers for Wireless and Radio Applications (PAWR)*. 2014, pp. 16–18. DOI: 10.1109/PAWR.2014.6825745.
- [7] S. C. Cripps. *RF Power Amplifiers for Wireless Communications*. Norwood, MA: Artech House, 2006.
- [8] J.W.M. Rogers and C. Plett. *Radio Frequency Integrated Circuit Design*. Artech House microwave library. Artech House, 2010. ISBN: 9781607839804. URL: https://books.google.ca/books?id=mL%5C_dDPfWMxYC.

- [9] P. M. Lavrador, T. R. Cunha, P. M. Cabral, et al. “The Linearity-Efficiency Compromise”. In: *IEEE Microwave Magazine* 11.5 (Aug. 2010), pp. 44–58. ISSN: 1557-9581. DOI: 10.1109/MMM.2010.937100.
- [10] D. Kimball, J. J. Yan, P. Theilmann, et al. “Efficient and wideband envelope amplifiers for envelope tracking and polar transmitters”. In: *2013 IEEE Topical Conference on Power Amplifiers for Wireless and Radio Applications*. Jan. 2013, pp. 13–15. DOI: 10.1109/PAWR.2013.6490173.
- [11] G. Montoro, P. L. Gilabert, J. Berenguer, et al. “Digital Predistortion of Envelope Tracking Amplifiers driven by slew-rate limited envelopes”. In: *2011 IEEE MTT-S International Microwave Symposium*. June 2011, pp. 1–4. DOI: 10.1109/MWSYM.2011.5972693.
- [12] S. C. Cripps. *Advanced Techniques in RF Power Amplifier Design*. Norwood, MA: Artech House, 2002.
- [13] M. Özen, K. Andersson, and C. Fager. “Symmetrical Doherty Power Amplifier With Extended Efficiency Range”. In: *IEEE Transactions on Microwave Theory and Techniques* 64.4 (Apr. 2016), pp. 1273–1284. ISSN: 1557-9670. DOI: 10.1109/TMTT.2016.2529601.
- [14] A. Z. Markos, P. Colantonio, F. Giannini, et al. “A 6W Uneven Doherty Power Amplifier in GaN Technology”. In: *2007 European Conference on Wireless Technologies*. Oct. 2007, pp. 379–382. DOI: 10.1109/ECWT.2007.4404026.
- [15] S. Watanabe, Y. Takayama, R. Ishikawa, et al. “A broadband Doherty power amplifier without a quarter-wave impedance inverting network”. In: *2012 Asia Pacific Microwave Conference Proceedings*. Dec. 2012, pp. 361–363. DOI: 10.1109/APMC.2012.6421598.

- [16] T. Jensen, V. Zhurbenko, V. Krozer, et al. “Coupled Transmission Lines as Impedance Transformer”. In: *IEEE Transactions on Microwave Theory and Techniques* 55.12 (Dec. 2007), pp. 2957–2965. ISSN: 1557-9670. DOI: 10.1109/TMTT.2007.909617.
- [17] E. Kaymaksüt, B. François, and P. Reynaert. “Analysis and design of series combining transformers for integrated Doherty power amplifiers”. In: *2010 Asia-Pacific Microwave Conference*. Dec. 2010, pp. 1621–1624.
- [18] Aleksey A. LYALIN Kunal DATTA Reza KASNAVI. “Doherty power amplifier combiner with tunable impedance termination circuit”. US9800207B2. Aug. 13, 2014.
- [19] S. Hu, F. Wang, and H. Wang. “2.1 A 28GHz/37GHz/39GHz multiband linear Doherty power amplifier for 5G massive MIMO applications”. In: *2017 IEEE International Solid-State Circuits Conference (ISSCC)*. Feb. 2017, pp. 32–33. DOI: 10.1109/ISSCC.2017.7870246.
- [20] R. Giofrè, A. Del Gaudio, W. Ciccognani, et al. “A GaN-on-Si MMIC Doherty Power Amplifier for 5G Applications”. In: *2018 Asia-Pacific Microwave Conference (APMC)*. Nov. 2018, pp. 971–973. DOI: 10.23919/APMC.2018.8617664.
- [21] D. P. Nguyen, B. L. Pham, and A. Pham. “A Compact Ka-Band Integrated Doherty Amplifier With Reconfigurable Input Network”. In: *IEEE Transactions on Microwave Theory and Techniques* 67.1 (Jan. 2019), pp. 205–215. ISSN: 1557-9670. DOI: 10.1109/TMTT.2018.2874249.
- [22] R. Darraji, F. M. Ghannouchi, and M. Helou. “Mitigation of Bandwidth Limitation in Wireless Doherty Amplifiers With Substantial Bandwidth Enhancement Using Digital Techniques”. In: *IEEE Transactions on Microwave Theory and Techniques* 60.9 (Sept. 2012), pp. 2875–2885. ISSN: 1557-9670. DOI: 10.1109/TMTT.2012.2207910.

- [23] D. P. Nguyen, B. L. Pham, and A. Pham. “A compact 29% PAE at 6 dB power back-off E-mode GaAs pHEMT MMIC Doherty power amplifier at Ka-band”. In: *2017 IEEE MTT-S International Microwave Symposium (IMS)*. June 2017, pp. 1683–1686. DOI: 10.1109/MWSYM.2017.8058964.
- [24] A. Agah, B. Hanafi, H. Dabag, et al. “A 45GHz Doherty power amplifier with 23% PAE and 18dBm output power, in 45nm SOI CMOS”. In: *2012 IEEE/MTT-S International Microwave Symposium Digest*. June 2012, pp. 1–3. DOI: 10.1109/MWSYM.2012.6259632.
- [25] D. Y. C. Lie, J. C. Mayeda, and J. Lopez. “A short survey on recent highly efficient cm-Wave 5G linear power amplifier design”. In: *2017 IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS)*. Aug. 2017, pp. 13–16. DOI: 10.1109/MWSCAS.2017.8052848.
- [26] D. Y. C. Lie, J. Tsay, T. Hall, et al. “High-efficiency silicon RF power amplifier design – current status and future outlook”. In: *2016 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*. Aug. 2016, pp. 1–4. DOI: 10.1109/RFIT.2016.7578181.
- [27] N. Rostomyan, M. Özen, and P. Asbeck. “28 GHz Doherty Power Amplifier in CMOS SOI With 28% backoff PAE”. In: *IEEE Microwave and Wireless Components Letters* 28.5 (May 2018), pp. 446–448. ISSN: 1558-1764. DOI: 10.1109/LMWC.2018.2813882.
- [28] M. Özen, K. Andersson, and C. Fager. “Symmetrical Doherty Power Amplifier With Extended Efficiency Range”. In: *IEEE Transactions on Microwave Theory and Techniques* 64.4 (Apr. 2016), pp. 1273–1284. ISSN: 1557-9670. DOI: 10.1109/TMTT.2016.2529601.
- [29] E. Kaymaksüt and P. Reynaert. “A 2.4 GHz fully integrated Doherty power amplifier using series combining transformer”. In: *2010 Proceedings*

- of *ESSCIRC*. Sept. 2010, pp. 302–305. DOI: 10.1109/ESSCIRC.2010.5619704.
- [30] Y. Chen, Y. Lin, J. Lin, et al. “A Ka-Band Transformer-Based Doherty Power Amplifier for Multi-Gb/s Application in 90-nm CMOS”. In: *IEEE Microwave and Wireless Components Letters* 28.12 (Dec. 2018), pp. 1134–1136. ISSN: 1558-1764. DOI: 10.1109/LMWC.2018.2878133.
- [31] D.M. Pozar. *Microwave Engineering*. Addison-Wesley series in electrical and computer engineering. Addison-Wesley, 1990. ISBN: 9780201504187. URL: <https://books.google.ca/books?id=0XLFQgAACAAJ>.
- [32] S. Lee, B. Jagannathan, S. Narasimha, et al. “Record RF performance of 45-nm SOI CMOS Technology”. In: *2007 IEEE International Electron Devices Meeting*. Dec. 2007, pp. 255–258. DOI: 10.1109/IEDM.2007.4418916.
- [33] J. A. Jayamon, J. F. Buckwalter, and P. M. Asbeck. “Multigate-Cell Stacked FET Design for Millimeter-Wave CMOS Power Amplifiers”. In: *IEEE Journal of Solid-State Circuits* 51.9 (Sept. 2016), pp. 2027–2039. DOI: 10.1109/JSSC.2016.2592686.
- [34] S. Kapur and D. E. Long. “Modeling of Integrated RF Passive Devices”. In: *2010 Custom Integrated Circuits Conference*. Sept. 2010, pp. 1–8.

A Matlab code for Main amplifier load modulation

```
clear
clc
clf
```

```

syms z11 z12 z13 z14
syms zL Ze Zo V1 V3
syms I1 I3 I4 IA IC
syms f
Zo=100;
Ze=12.5;
zL=25;
cap=200e-15; %shunt output capacitance of transistors
%remove I2 and I4
%% reducing Z matrix for upper clin section
I2=-1*(I1*z12+I3*z14+I4*z13)/(z11 + zL);
K=0==(I1*z14+I2*z13+I3*z12+I4*z11);
I4=solve(subs(K),I4);
I2=subs(-1*(I1*z12+I3*z14+I4*z13)/(z11+zL));
%declaring the two voltages that we are interested in
V1=simplify(subs(z11*I1 + z12*I2 + z13*I3 + z14*I4));
V3=simplify(subs(z13*I1 + z14*I2 + z11*I3 + z12*I4));
%Building Z parameter matrix for upper Clin section
Za11=subs(V1,[I1,I3],[1,0]);%v1 in terms of I1
Za12=subs(V1,[I1,I3],[0,1]);%v1 in terms of I3
Za21=subs(V3,[I1,I3],[1,0]);%v3 with respect I1
Za22=subs(V3,[I1,I3],[0,1]);%V3 with respect I3
%% second clin section
syms I1b I2b I4b
%remove Ib4, Ib3=0
I4b=-1*(I1b*z14+I2b*z13)/z11;
V1b=subs(I1b*z11+I2b*z12+I4b*z14);

```

```

V2b=subs(I1b*z12+I2b*z11+I4b*z13);
%Buildint Z parameter matrix for lower Clin section
%the zparameter matrix is reversed compared to the voltage labelling of the
%coupled lines.
Zb22=subs(V1b,[I1b,I2b],[1,0])%v1 in terms of I1 2o-====-o
Zb21=subs(V1b,[I1b,I2b],[0,1])%v1 in terms of I2 1o-====-o
Zb12=subs(V2b,[I1b,I2b],[1,0])%v3 with respect I1
Zb11=subs(V2b,[I1b,I2b],[0,1])%V3 with respect I2
%% converting clin Z parameters to abcd parameters
%pozar 4th ed. page 192 abcd matrix from a Z param matrix
Aa=Za11/Za21;
Ba=(Za11*Za22-Za12*Za21)/Za21;
Ca=1/Za21;
Da=Za22/Za21;
ABCDa=[Aa , Ba ;
Ca , Da];
%pozar 4th ed. page 192
Ab=Zb11/Zb21;
Bb=(Zb11*Zb22-Zb12*Zb21)/Zb21;
Cb=1/Zb21;
Db=Zb22/Zb21;
ABCDb=[Ab , Bb ;
Cb , Db];
%% accounting for output chunt capacitance
%cap parameters
%shunt cap from page 190 pozar 4th ed
Acap=1;

```

```

Bcap=0;
Ccap=(1i*2*pi*cap*f);
Dcap=1;
ABCDcap=[Acap , Bcap ; Ccap , Dcap];
%% combining all ABCD matrices
ABCDtotal=ABCDcap*ABCDa*ABCDb*ABCDcap;
theta=2*pi*(299792458/f)/(8*299792458/28e9);
z11=-1i*0.5*(Ze+Zo)*cot(theta);
z12=-1i*0.5*(Ze-Zo)*cot(theta);
z13=-1i*0.5*(Ze-Zo)*csc(theta);
z14=-1i*0.5*(Ze+Zo)*csc(theta);
z11=subs(z11);
z12=subs(z12);
z13=subs(z13);
z14=subs(z14);
ABCDtotal=subs(ABCDtotal)
%% converting back to Z parameters
Z11=ABCDtotal(1,1)./ABCDtotal(2,1);
Z12=(ABCDtotal(1,1).*ABCDtotal(2,2)-ABCDtotal(1,2).*ABCDtotal(2,1))./ABCDtotal(2,1);
Z21=1./ABCDtotal(2,1);
Z22=ABCDtotal(2,2)./ABCDtotal(2,1);
Zin= 1/((1/(Z11 +(IA/IC)*Z12))+(1/1i*2*pi*cap*f))
IC=1;
IA=0:0.1:1;
figure(1)
hold on
%plotting real Portion of main amp

```

```

f=24e9;
plot(IA,real(double(subs(Zin))),'-o')
f=26e9;
plot(IA,real(double(subs(Zin))),'-+')
f=28e9;
plot(IA,real(double(subs(Zin))),'-d')
f=30e9;
plot(IA,real(double(subs(Zin))),'-*')
f=32e9;
plot(IA,real(double(subs(Zin))),':o')
grid on
legend('24GHz','26GHz','28GHz','30GHz','32GHz')
title('Main Real Impedance Transform Over Auxiliary Amp Turn On')
xlabel('Auxiliary Amp Current')
ylabel('Main Loading Impedance  $\Omega$ ')
hold off
%plotting imaginary portion of main amp
figure(2)
hold on
f=24e9;
plot(IA,imag(double(subs(Zin))),'-o')
f=26e9;
plot(IA,imag(double(subs(Zin))),'-+')
f=28e9;
plot(IA,imag(double(subs(Zin))),'-d')
f=30e9;
plot(IA,imag(double(subs(Zin))),'-*')

```

```

f=32e9;
plot(IA,imag(double(subs(Zin))),':o')
grid on
legend('24GHz','26GHz','28GHz','30GHz','32GHz')
title('Main Imaginary Impedance Transform Over Auxiliary Amp Turn
On')
xlabel('Auxiliary Amp Current(A)')
ylabel('Main Loading Impedance  $\Omega$ ')
hold off

```