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**EMITTER RESISTANCE AND CURRENT GAIN
IN RAPID THERMAL ANNEALED POLYSILICON EMITTER TRANSISTORS**

by

Gary F. Mackay

A thesis submitted to the
Faculty of Graduate Studies and Research
in partial fulfilment of the
requirements for the degree of

Master of Engineering

Ottawa-Carleton Institute for Electrical Engineering
Department of Electronics
Faculty of Engineering
Carleton University

January 1991

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**"Emitter Resistance and Current Gain in
Rapid Thermal Annealed Polysilicon
Emitter Transistors"**

submitted by Gary F. Mackay in partial fulfillment of
the requirements for the degree of Master of Engineering

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December 1990

ABSTRACT

This research concerns the investigation of rapid thermal annealing of insitu doped polysilicon emitter transistors. Electrical characteristics of furnace and rapid thermal annealed polysilicon emitter transistors are compared. The effects of rapid thermal annealing on emitter Gummel number, emitter resistance, and minority carrier back injection current are examined. Emitter metallization problems are discussed and acceptable metallization schemes outlined.

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TABLE OF SYMBOLS

SYMBOL	DESCRIPTION	UNITS
α_R	reverse common-base current gain	----
f_T	cutoff frequency	Hz
G_E	emitter Gummel number	s/cm^4
G_B	base Gummel number	s/cm^4
h_{FE}	forward d.d current gain	----
I_B	base current	A
I_{BO}	base saturation current	A
I_C	collector current	A
I_E	emitter current	A
J_B	base current density	A/cm^2
J_{BO}	base saturation current density	A/cm^2
J_{BK}	emitter back injection current density	A/cm^2
J_C	collector current density	A/cm^2
J_{CO}	collector saturation current density	A/cm^2
J_E	emitter current density	A/cm^2
J_f	diode forward current	A
J_{rev}	diode reverse leakage current density	A/cm^2
k	Boltzmann's constant	$1.38 \times 10^{-23} J/K$
n_i	intrinsic carrier concentration	$1.1 \times 10^{10}/cm^3$
q	elementary charge	$1.6 \times 10^{-19} C$
R_{BI}	intrinsic base resistivity	Ωcm^2
R_{BX}	extrinsic base resistivity	Ωcm^2
R_E	emitter resistivity	Ωcm^2
R_S	sheet resistivity	Ω/sq

T	absolute temperature	K
V_{EB}	base-emitter voltage	V
V_{EB}'	ideal emitter-base voltage	V
V_{EB1}	emitter-base voltage to determine J_{B0}	V
V_{CB}	collector-base voltage	V
V_{CE}	collector-emitter voltage	V
V_{CEO}	common emitter breakdown voltage	V
V_T	thermal voltage	25.9mv at 300K

CHAPTER 1

INTRODUCTION

Bipolar technology has been the technology of choice when high performance circuit design requires low noise, high speed and gain capability. However, bipolar transistors suffer from the disadvantages of high power consumption and low packing density, making integration at Very Large Scale Integrated Circuit (VLSI) levels unattractive. In the last five years Bipolar Complimentary Metal Oxide Semiconductor (BICMOS) technologies have offered a way of combining bipolar speed with Metal Oxide Semiconductor (MOS) power consumption, and have led to a resurgence of interest in bipolar devices.

Most modern bipolar and BICMOS technologies use polysilicon emitters, which have been found to give higher injection efficiency than conventional diffused or implanted emitters by suppressing the back injection component of the base current [PaBP85].

Previous work at Carleton and elsewhere has shown that annealing at temperatures of 900°C or greater is necessary to reduce the resistance of a polysilicon emitter to an acceptable level. However, when carried out for the length of time appropriate for conventional furnace processing,

this annealing has been shown to lower the emitter Gummel number ¹ G_E [Keye87].

The primary goal of this thesis was to determine whether rapid thermal annealing (RTA) of "insitu" doped polysilicon emitters could achieve the same reduction in emitter resistance obtained with conventional furnace anneals without incurring a loss in emitter Gummel number. To accomplish this goal, it was necessary to develop techniques for forming low resistance contacts to thin polysilicon emitter layers.

This thesis is organized as follows. Chapter 2 provides a brief summary of previous research on polysilicon emitter transistors, and on attempts to devise theoretical models accounting for the behavior of these devices. Chapter 3 reviews the techniques available for the electrical characterization of bipolar devices. Chapter 4 summarizes the experimental techniques used in depositing and annealing polysilicon emitter layers. Chapter 5 deals with the development of a reliable, low resistivity contact scheme for shallow polysilicon emitters. The electrical characteristics of the complete polysilicon emitter devices fabricated here are presented and analyzed in chapter 6. Chapter 7 presents a summary of the work.

¹ G_E and other parameters used to characterize bipolar transistors are discussed in detail in chapter 3.

CHAPTER 2

BACKGROUND

2.1 INTRODUCTION

This chapter provides a summary of previous research on polysilicon emitter transistors, both at Carleton University and elsewhere.

2.2 INITIAL WORK

In 1972, Takagi et al. [TNTK72] fabricated the first polysilicon emitter transistor when they utilized a doped polycrystalline silicon layer as a diffusion source to form a shallow emitter junction. Although Takagi et al. compared their devices with conventional metal emitter transistors they did not report any enhanced common emitter current gains (h_{FE}). In 1974-75 Graul et al. [GrGM76] reported surprisingly high emitter injection efficiencies and current gains for poly emitter structures compared with conventional transistors. In their devices, polysilicon was deposited undoped and subsequently implanted with arsenic followed by an anneal drive-in step. Maximum current gains observed were 3 to 7 times higher than for conventional transistors, with h_{FE} as high as 2000.

The explanation for the improved current gains of polysilicon emitter transistors has been the subject of considerable controversy. Graul et al. [GrGM75] observed that the current gains of polysilicon devices had a lesser sensitivity to temperature compared with the conventional bipolar transistor. Since the dominant factor that influences the temperature dependence of current gain in a bipolar transistor is the large band gap narrowing (due to the heavier doping) in the emitter compared to the base, Graul et al. concluded that the polysilicon had less deleterious heavy doping effects compared to single crystal silicon. They attributed the larger current gain observed in polysilicon emitter transistors to a smaller band gap narrowing in the polysilicon emitter.

In 1979 DeGraff and DeGroot fabricated devices in which an extremely thin (1 to 3 nm) oxide layer was grown in the emitter window prior to polysilicon deposition [DeDe79]. They found that the presence of this oxide layer greatly increased the emitter Gummel number, and attributed the improved performance to the existence of asymmetric tunnelling barriers for electrons and holes. Specifically, it was assumed that the probability for tunnelling through the interfacial oxide was less for electrons than for holes, leading to suppression of the hole back injection current.

In 1980 Ning and Isaac fabricated polysilicon emitter transistors in which the gain increased with increasing polysilicon thickness [NiIs80]. This result was clearly at odds with the tunnelling model of DeGraff et al. Ning et al. proposed that the suppression of hole back injection current observed for polysilicon emitters results from a reduced hole mobility in polysilicon compared to a monocrystalline material. Although it is well known that the mobility of majority carriers in polysilicon is reduced by the presence of grain boundary potential barriers, it is not clear that the same effects should apply to minority carriers. However, Ning and Isaac's results clearly demonstrate that transport in the polysilicon plays a part in controlling the characteristics of at least some polysilicon emitter devices.

2.3 PHYSICS GOVERNING HOLE BACK INJECTION CURRENT

Some insight into the mechanisms governing carrier flow in polysilicon emitters was provided by more detailed experimental work in the mid 1980's. Soerowirdjo and Ashburn demonstrated that the deliberate introduction of an interfacial oxide between the polysilicon and substrate could increase common emitter current gain by a factor of 10

compared to conventional transistors, but also found that a polysilicon emitter with no deliberately grown oxide could give a factor of three improvement in gain [AsSo83]. Chor, Ashburn and Brunnschweiler later showed that the presence of an interfacial oxide gave nearly an order of magnitude increase in emitter resistance [ChAB85].

2.4 STRUCTURAL STUDIES

More recently Patton et al. [PaPB86] have carried out a systematic study of the contributions to the base current in polysilicon emitter transistors with no intentional interfacial oxides between the polysilicon and monosilicon. Transmission Electron Microscopy (TEM) examination revealed the presence of an ultra-thin interfacial oxide. They found that the uniformity and, consequently, the blocking characteristics of the native oxide were strongly dependent upon the polysilicon doping level and post-deposition thermal treatments. Devices were annealed in an Argon ambient at temperatures ranging from 900°C to 1000°C for times of 30 minutes to 3 hours. A high base current was observed at the lower doping level, and was attributed to a high recombination rate at the grain boundaries in the polysilicon. Trapping sites resulting from the high concentration of defects and dangling bonds within the polysilicon are present at the grain boundaries. When

arsenic segregates to these dangling bonds, the density of trapping sites is reduced resulting in a further decrease in effective recombination velocity. Thus base current decreases as the doping level in the polysilicon increases. Patton et al. found that base current dependence on polysilicon thickness was observed only under certain circumstance in which the thin unintentionally grown oxide layer broke up.

The rupture of interfacial oxide layers during high temperature anneals was also reported by Jorgenson et al. [JBBA85], Wilson et al. [WJBH85], Patton et al. [PaBP86] and Wolstenholme et al. [WJAB87]. Wolstenholme examined the structure of the polysilicon/substrate interface using high resolution TEM and concluded that annealing at temperatures of 950°C or greater effectively broke up any interfacial oxide.

A study of the trade off between the junction depth and the epitaxial alignment of polysilicon emitters was conducted by Crabbe et al. [CHMP87]. They observed that to minimize arsenic out-diffusion and improve epitaxial alignment, high temperature anneals (greater than 1100°C) for shorter times are preferred over lower temperatures and longer times.

2.5 WORK AT CARLETON

At Carleton University, polysilicon emitter research has concentrated on low temperature processing and its consequences for device characteristics. Work began with the fabrication of the first true polysilicon emitter transistor, in which the emitter consists of "in-situ" doped polysilicon deposited at 625°C and subjected to no further annealing [RoTa86]. Since phosphorus diffusion is negligible at 625°C, the metallurgical base/emitter junction coincides with the polysilicon/substrate interface in such a device. True polysilicon emitters were found to give almost complete suppression of the hole back injection current, with emitter Gummel numbers G_E in excess of 10^{15} scm^{-4} (the best conventional transistors have G_E no greater than $5 \times 10^{13} \text{ scm}^{-4}$) [KeTa87]. With suitably light base doping, emitters of this kind provided common emitter current gains of over 30,000, the highest ever reported for silicon homojunction transistors [KeTa87]. Unfortunately, these devices also had high and frequently non-ohmic emitter resistances. At a collector current density of 500 Acm^{-2} , R_E was found to be $100 \text{ } \mu\Omega\text{cm}^2$ or greater, roughly two orders of magnitude higher than in a conventional transistor, and

high enough to severely degrade the performance of any digital circuit incorporating these devices.

Annealing in a conventional furnace at 900°C for 30 minutes was found to lower R_E to more acceptable levels (approximately $2 \mu\Omega\text{cm}^2$), but at a cost of a reduction in emitter Gummel number to approximately $3 \times 10^{14} \text{ scm}^{-4}$ [Keye87]. It seems plausible that the anneal cycle led to a restructuring of the polysilicon/silicon interface, lowering its resistance to electron flow while simultaneously decreasing its ability to block hole back injection.

2.6 RAPID THERMAL ANNEALING (RTA)

Annealing at temperatures of 900°C or greater can help reduce R_E in polysilicon emitters. However, it is also clear that annealing may reduce G_E . The primary goal of this thesis is to examine whether rapid thermal annealing can reduce R_E without degrading G_E .

Kermani et al. investigated the effect of RTA on arsenic and phosphorus implanted crystalline emitter transistors [KGLS87]. Due to a loss of emitter dopant (out-diffusion of arsenic), they found that the common emitter current gain values for arsenic emitters were low. Phosphorus emitters exhibited improved or comparable gains as compared to the conventional furnace annealed devices.

The effects of rapid thermal anneal temperature and time on emitter-base junction depth, emitter sheet resistance, base punch resistance and interfacial oxide integrity for transistors with arsenic-implanted polysilicon emitters were reported by Delfino et al. [DDRM89]. They found that the emitter depth and sheet resistance were strongly dependent upon RTA temperature. By contrast, RTA time has almost no effect on emitter depth, but causes the emitter sheet resistance to increase at the higher temperatures. They also found that the interfacial oxide

layer is not affected at an RTA temperature of 900°C, but it is disrupted and epitaxial alignment does occur at temperatures of 1000°C and above.

2.7 SUMMARY AND CONCLUSION

Polysilicon emitter transistors show an improved suppression in back injection hole current as compared to conventional devices. The mechanisms responsible for this improvement are still under debate. However, it is apparent that the polysilicon/substrate interfacial structure is important, as is post-deposition thermal treatment.

CHAPTER 3

TECHNIQUES FOR CHARACTERIZING BIPOLAR TRANSISTORS

3.1 INTRODUCTION

This chapter examines a variety of figures-of-merit for the performance of bipolar transistors, and their relation to the physical mechanisms underlying transistor operation. Emphasis is placed on the use of Gummel plots to determine junction integrity, the extent of hole back injection into the emitter, and the current densities at which high-level injection effects set in. Techniques for extracting parasitic emitter and base resistances are also reviewed.

3.2 GUMMEL PLOTS

In characterizing the electrical performance of the devices produced in this thesis, extensive use was made of "Gummel" plots: in which the logarithm of collector and base current density J_B and J_C as a function of base-emitter bias V_{BE} in forward active operation. An example is given in Fig. 3.1. Ideally, J_C and J_B obey laws of the form

$$J_C = J_{C0} e^{qV_{BE}/kT} \quad (3.1)$$

$$J_B = J_{B0} e^{qV_{BE}/kT} \quad (3.2)$$

FIGURE 3.1 GUMMEL PLOT FOR AN ANNEALED POLYSILICON
EMITTER TRANSISTOR
ANNEAL: 1000°C, 5 s
EMITTER AREA: 10 μm x 10 μm

and therefore appear as straight lines on the Gummel plot with a slope of $(\log_{10}(e)q/kT)$ decades/volt. In practice, departure from this ideal behavior occurs at low and high bias levels. At very low V_{EB} collector-base junction leakage current may dominate the characteristics, causing J_B and J_C to be independent of V_{EB} . At slightly higher V_{EB} a substantial component of J_B may result from recombination in the emitter-base space charge region, in which case J_B is given by

$$J_B = J_{B0} e^{qV_{EB}/nkT} \quad (3.3)$$

where $1 < n < 2$. At collector current densities above approximately 10^3 Acm^{-2} , emitter and base series resistance and/or high level injection effects such as base pushout (the Kirk effect) [WaGr83] cause J_B and J_C to fall below the values predicted by (3.1) and (3.2).

In modern bipolar transistors recombination in the neutral base is usually negligible under normal operating conditions. In this case collector current is given by

$$J_{CO} = qn_i^2/G_B \quad (3.4)$$

where the base Gummel number G_B is given by

$$G_B = \int_{\text{base}} N_A(x) dx / D_n(x) \quad (3.5)$$

where the integral is to be carried out across the quasi-neutral base. $N_A(x)$ is the dopant concentration and $D_n(x)$ is the electron diffusion coefficient within the base.

G_B is essentially the product of the integrated dopant in the neutral base and an average electron diffusion coefficient.

The base current is normally dominated by back injection of holes into the emitter. By analogy to (3.4), the base current can be written as

$$J_{BO} = q n_i^2 / G_E \quad (3.6)$$

where G_E is the emitter Gummel number. For a long uniformly doped monocrystalline emitter [DeSS77],

$$G_E = \int_0^{L_h} N_D(x) dx / D_h(x) \quad (3.7)$$

where $N_D(x)$ is the dopant concentration and $D_h(x)$ the hole diffusion coefficient within the emitter. L_h is the diffusion length of holes within the emitter. For a polycrystalline silicon or heterojunction emitter (3.7) does not apply, but G_E still serves as a useful figure-of-merit with which to compare different emitter structures. Unlike the common emitter current gain h_{FE} , G_E is independent of the base doping profile. The base saturation current density J_{B0} has sometimes been used as an alternative figure-of-merit to G_E , but J_{B0} is extremely sensitive to temperature, whereas G_E is not.

For a conventional diffused or implanted emitter, the maximum possible value of G_E is approximately $5 \times 10^{13} \text{ scm}^{-4}$ [GrGo83]. G_E can be increased to some extent by increasing the doping level in the emitter, but this approach is severely limited by Auger recombination and bandgap narrowing effects [Sze83].

3.3 EMITTER RESISTANCE

The emitter resistance R_E of conventional transistors is dominated by contact resistance. The contact resistivity of metal contacts to monocrystalline silicon can be made as low as approximately $0.25 \mu\Omega\text{cm}^2$, and is unlikely to pose problems even when devices are scaled down to submicron

geometries. However, theoretical and experimental results have indicated that much higher values may be obtained for polysilicon emitter devices. For this reason considerable effort was devoted to accurate measurement of R_E in the present work.

The two most commonly used dc methods for measuring R_E are the open collector method and the Ning and Tang method (which is a variation on the I_C - V_{BE} method) [FiBe81],[NiTa84].

3.3.1 Open Collector Method

In this method, the value of R_E is obtained by observing the base current as a function of collector-emitter voltage, V_{CE} , for a transistor with an open-circuit collector [Getr78]. Emitter current density is plotted against collector-emitter voltage V_{CE} . V_{CE} is related to J_E by the equation:

$$V_{CE} = kT/q \ln(1/\alpha_R) + I_E R_E \quad (3.3.1)$$

where α_R is the reverse common-base current gain. R_E is equal to the inverse of the slope of the J_E - V_{CE} curve.

Figure 3.2 illustrates the open collector method for measuring R_E on a polysilicon emitter device (the processing details of which will be discussed in chapter 4). I_B v.s. V_{CE} is plotted with open collector, the slope indicating emitter resistance at $7.1 \mu\Omega\text{cm}^2$. The low current "flyback" portion of the curve is caused by the decrease of the reverse active common-base gain at low currents. The slope of the curve should be determined as close to the "flyback" region as possible. At high currents, I_B versus V_{CE} departs from a straight line due to current crowding in the base.

It was found that R_E determined from (3.3.1) is a function of I_B . In some cases the slope at low current is about twice that at high current. This has also been reported by Sansen and Meyer (SaMe72). Physically, the resistance of the heavily doped emitter region should be independent of current.

3.3.2 The Ning and Tang Method

Ning and Tang [NiTa84] developed a method based on the measured deviation of base current from ideal behavior. At low currents I_C is ideal, i.e. proportional to $e^{qV_{BE}/kT}$. At high current levels a number of factors can contribute to I_C deviating from ideality : 1) base conductivity modulation (relative to the emitter), 2) emitter and base series

FIGURE 3.2 OPEN COLLECTOR METHOD FOR DETERMINING
EMITTER RESISTANCE

ANNEAL: 1000°C, 5 s

EMITTER AREA: 5 μm x 5 μm

SLOPE = $R_e \approx 7.1 \text{ uohmcm}^2$

resistance effects, 3) collector pushout and 4) quasi-saturation. Because of the very high emitter doping there is practically no emitter conductivity modulation.

Writing the ideal base current as

$$I_B = I_{B0} \times e^{qV_{EB}'/kT} \quad (3.3.2)$$

the actual bias V_{EB} which must be applied to achieve a given base current I_B differs from the bias V_{EB}' needed in the ideal transistor by an amount

$$V_{EB}' - V_{EB} = [-V_{EB} - (kT/q) \log(I_B/I_{B0})] \quad (3.3.3)$$

In cases where the base current is dominated by hole back injection into the emitter, I_B is proportional to $e^{qV_{EB}/kT}$ over several decades, so there is little difficulty in determining I_{B0} . However, in some of our devices the back injection is suppressed to such an extent that the region over which (3.3.2) applies is very limited. In this case I_{B0} was estimated from

$$I_{B0} = I_B(V_{EB1}) e^{-qV_{EB1}/kT} \quad (3.3.4)$$

where V_{EB1} is the bias point at which I_C just starts departing from ideal behavior and high current effects are present.

Neglecting current crowding, $V_{EB'}-V_{EB}$ is given by:

$$V_{EB'}-V_{EB} = R_E I_E + I_B R_{BI} + I_B R_{BX} \quad (3.3.5)$$

where R_E is the emitter resistance, R_{BI} the intrinsic base resistance and R_{BX} the extrinsic base resistance.

Rearranging (3.3.5)

$$(V_{EB'}-V_{EB})/I_C = (R_E+R_{BI}/h_{FE})+(R_E+R_{BX})/h_{FE} \quad (3.3.6)$$

Figure 3.3 shows a schematic of a polysilicon emitter transistor with emitter R_E , extrinsic base R_{BX} , and intrinsic base R_{BI} resistances. R_{BI} has been empirically shown to be proportional to h_{FE} at low currents [Tang80]. Theoretically, R_{BI} is proportional to h_{FE} at all current levels if the carrier mobility is independent of current level [Tang80]. Therefore R_{BI}/h_{FE} is a constant. In consequence, if $(V_{EB'}-V_{EB})/I_C$ is plotted as a function of $1/h_{FE}$, the slope gives (R_E+R_{BX}) and the intercept gives (R_E+R_{BI}/h_{FE}) . The ratio R_{BI}/h_{FE} can be determined by measuring base sheet resistance and h_{FE} at low current

FIGURE 3.3 SCHEMATIC ILLUSTRATING THE PHYSICAL ORIGINS OF THE SERIES RESISTANCES, R_E , R_{BI} and R_{BX}

levels. For a given geometric shape, the ratio R_{BI}/h_{FE} is independent of the physical dimensions of the emitter. For the transistors fabricated here R_{BI}/h_{FE} is typically 0.1Ω . Thus as R_E increases in scaling and becomes much larger than R_{BI}/h_{FE} , R_{BI} can be dropped from (3.3.6). In that case the intercept gives R_E and the slope gives $(R_E + R_{BX})$.

The significance of the resistance of the lightly doped extrinsic base, R_{BX} , was estimated by comparing transistors with zero clearance between the emitter and extrinsic base and those with a $5 \mu m$ clearance. If the series resistance of the extrinsic base is important devices with zero clearance should have an increased current handling capability. This was found not to be the case, indicating the relative insignificance of R_{BX} . This is shown in figure 3.4 which shows a Gummel plot for two devices (one has a clearance of $5 \mu m$, the other $0 \mu m$).

Figure 3.5 plots $(V_{EB}' - V_{BE})/I_C$ as a function of $1/h_{FE}$ for a typical polysilicon device with a sintered Al/Ti:W/TiSi₂ contact. The emitter has an area of $5 \mu m \times 5 \mu m$. The polysilicon was annealed at $1000^\circ C$ for a period of 8 secs while the TiSi₂ was formed at $700^\circ C$ for 5 secs. Maximum forward gain (h_{FE}) was measured at 1100 with $I_{B0} = 4.71 \times 10^{-21} A$. R_{BI}/h_{FE} was calculated to be approximately 0.1Ω . Extrapolation to $1/h_{FE}=0$ the emitter resistivity (R_E) was found to be 2 to $3 \mu\Omega cm^2$. From the

FIGURE 3.4 COMPARISON BETWEEN A DEVICE WITH A 0 μm CLEARANCE
BETWEEN EMITTER AND EXTRINSIC BASE AND ONE WITH 5 μm

EMITTER AREA = 5 μm x 5 μm

METALIZATION: Al/Ti

FIGURE 3.5 NING AND TANG METHOD FOR DETERMINING
EMITTER AND INTRINSIC BASE RESISTANCE

ANNEAL: 1000°C, 5 s

EMITTER AREA: 5 μm x 5 μm

INTERCEPT = $R_E = 3 \text{ uohmcm}^2$

SLOPE = $R_{BX} = 600 \text{ ohms}$

slope we find the extrinsic base resistance to be 600 Ω .

Additional curves were taken with external resistors inserted in the emitter and base leads. The slopes and intercepts were displaced by the appropriate amounts indicating the accuracy of the method. Figure 3.6 shows the results with and without a 2 Ω resistor added to the emitter. The 2 Ω resistor has caused the curve to be displaced upwards by 2.2 Ω , while the slope of the line has remained constant indicating that the extrinsic base resistance has not been affected. Figure 3.7 has the same transistor but with a 500 Ω resistor added to the base. The slope of the curve has been increased by 550 Ω . From the intercept of the graph emitter resistance was found to be 8 Ω corresponding to a normalized emitter resistivity of 2 $\mu\Omega\text{cm}^2$.

There are several disadvantages to the Ning and Tang method of determining R_E and R_{BX} . The method assumes an ideal exponential dependence of base current on bias voltage over at least part of the characteristic. However, as noted previously, many of our devices exhibited a non-ideal base current with substantial emitter-base recombination. It also assumes that the current flow remains essentially one-dimensional, even when high-level injection effects are present within the base.

FIGURE 3.6 NING AND TANG METHOD WITH A 2 ohm
RESISTOR INSERTED IN THE EMITTER LEAD

WITHOUT RESISTOR = $R_E = 2$ ohms

WITH RESISTOR = $R_E = 4.2$ ohms

FIGURE 3.7 NING AND TANG METHOD WITH A 500 ohm
RESISTOR INSERTED IN THE BASE LEAD

WITHOUT RESISTOR = $R_{BX} = 900$ ohms

WITH RESISTOR = $R_{BX} = 1450$ ohms

3.4 SUMMARY AND CONCLUSIONS

The best figure-of-merit to monitor back injection hole current is the emitter Gummel number which is obtained from the Gummel plot. Emitter resistance can be determined by two methods, the open-collector method and the Ning and Tang method. The Ning and Tang method also allows extrinsic and intrinsic base resistances to be measured.

CHAPTER 4

DEVICE FABRICATION TECHNIQUES

4.1 INTRODUCTION

This chapter begins with a brief overview of rapid thermal annealing (RTA) and discusses the operation of the Heatpulse 410 annealer used here. Fabrication details pertaining to test devices and polysilicon emitter transistors used throughout this dissertation are then considered.

4.2 RAPID THERMAL ANNEALING

Rapid thermal annealing and more generally, rapid thermal processing (RTP), developed as an outgrowth of laser annealing, which was intensively studied in the late 1970's. Not until the introduction of the incoherent lamp annealer was there a serious attempt to bring rapid annealing into the realm of semiconductor processing. Thermal incoherent lamp units offered, for the first time, a method of uniform isothermal heating of work pieces and a much faster overall wafer handling capability than lasers. The most significant point is that rapid thermal annealing eliminated the extremely high and localized temperature gradients

associated with laser spot scanning which often induced damage in materials.

Since end-wafer effects experienced in conventional furnaces are no longer a factor, rapid thermal process reactors should produce annealing results which are identical from wafer to wafer. This is enhanced by the relatively cold walls of the rapid thermal processor chamber which helps reduce contamination. The low volume of the enclosure within the heating chamber enables rapid gas composition changes. This has considerable potential for the fabrication of unique devices.

The second major advantage of Rapid Thermal Processing is due to the expanded time regime (to shorter times) available for processing. This increased time range, of more than two orders of magnitude, allows exploitation of the differences between kinetic properties of reactions which take place in structures undergoing processing. The goal of a process step is to promote a desired reaction such as film growth, dopant activation, defect removal or other, while attempting to minimize or prevent some undesired reaction (i.e. dopant diffusion) [Sedg86]. However, it may also take advantage of the variation of thermodynamic properties of one or both processes with temperature.

In Table 4.1 some of the current rapid thermal processing applications have been listed along with an indication of desired and undesired processes.

TABLE 4.1
SEMICONDUCTOR DEVICE APPLICATIONS

APPLICATION	DESIRED PROCESS	UNDESIRE D PROCESS
Shallow P+,N+ Doping	Extended Defect Removal	Dopant Diffusion
Silicide Contacts	High Conductivity	Dopant out Diffusion and Bridging
Al-Si Contacts	Form ohmic Contact	Al Spiking

On balance it must be stated that an intrinsic disadvantage to a rapid thermal processing reactor as compared to the conventional furnace is the great difficulty of achieving uniform temperature over a wafer and in monitoring temperature. This occurs in part because RTP equipment is designed to operate over a wide range of temperature. A process may call upon various annealing sequences which may include very rapid heating and cooling rates. In a high loss thermal system, unfortunately, changes in any of the above parameters tend to affect adversely the temperature uniformity.

4.3 THE HEATPULSE 410

The heating chamber of the Heatpulse 410 Rapid Thermal Processor contains upper and lower banks of high intensity tungsten - halogen lamps as shown in Fig 4.1 There are 10 lamps on the top and 11 on the bottom. The system efficiency is enhanced by a reflective plating on the chamber walls. The plating also enhances heating uniformity and ramp-up speed. Thermal processing takes place in a quartz isolation chamber. This quartz tube provides a contamination and oxygen-free environment. The wafer to be processed is placed on a quartz tray inside the isolation chamber. The wafer holder is of low thermal mass and very

high thermal conductivity, so that the contact of the wafer and holder does not produce a temperature gradient across the wafer or mechanically stress the wafer. This is necessary to prevent any displacement of crystal planes (slip) past each other as a result of thermally induced stress. The tray itself is cut away in the middle to reduce residual heating, as shown in Fig 4.2.

The Heatpulse 410 uses a responsive closed-loop temperature control system which incorporates two monitoring systems, the first being an optical pyrometer used when processing temperatures are above 800°C, and the second a thermocouple (type K, chromel-alumel) used when processing ranges are below 800°C. Process temperatures we are concerned with ranged from 700°C to 1100°C, so we made use of the optical pyrometer. Since pyrometer readings are emissivity-dependent, changes in wafer backside surface roughness or variations in substrate materials must be dealt with a recalibration of the pyrometer.

FIGURE 4.1 SCHEMATIC OF THE HEATPULSE 410

FIGURE 4.2 SCHEMATIC OF THE QUARTZ TRAY WAFER HOLDER

4.3.1 CALIBRATION OF THE HIGH TEMPERATURE PYROMETER

An optical pyrometer was used to monitor temperature throughout the wafer anneals. Calibration of the pyrometer was made using a thermocouple. To protect the thermocouple used within the Heatpulse 410 the pyrometer was calibrated at a relatively low temperature of 300°C to 450°C. In Fig. 4.3 the pyrometer was calibrated at 400°C with a blank wafer inside the quartz tube. When calibrating the pyrometer in such a fashion one has to keep in mind that the accuracy of the pyrometer is diminished once the temperature is below 500°C. The Heatpulse 410 pyrometer is claimed to be accurate to within $\pm 10^{\circ}\text{C}$. However, due to the nature of the equipment there was no way to check the absolute precision of the pyrometer. The rapid thermal processed transistors used throughout this thesis were annealed using half the wafer. For comparison the other half of the wafer was given a furnace anneal or no anneal. The thermal glass holder will not hold half a wafer so a blank wafer was placed under it to hold it in place. To improve the relative accuracy of the temperature measurements the same blank wafer was used each time.

FIGURE 4.3 CALIBRATION OF THE PYROMETER USING A
THERMOCOUPLE AND A BLANK WAFER

4.4 DEVICE PROCESSING DETAILS

4.4.1 POLYSILICON EMITTER TRANSISTOR

The mask set used to fabricate complete transistors contained devices with emitter areas ranging from $5 \times 5 \mu\text{m}^2$ to $10 \times 175 \mu\text{m}^2$. Fig 4.4 shows the transistor mask layout. A strip emitter with two base stripes on either side was chosen. Clearance between the emitter and extrinsic base windows varied from 0 to $5 \mu\text{m}$. Test structures to measure the extrinsic and intrinsic base sheet resistance, the polysilicon sheet resistance and the polysilicon-to-metal contact resistivity were also included.

A simplified diagram of the transistor structure used throughout the research is shown in Fig. 4.5. Transistors were fabricated on n-type silicon of (100) orientation. The n-type substrate acts as the collector. Resistivity of the collector region was maintained at 3-5 Ωcm corresponding to an impurity concentration of 10^{16} atoms/ cm^3 . To achieve an ohmic collector contact phosphorus was deposited on the wafer backside followed by a 950°C , 30 minute drive-in. The extrinsic base was formed by a heavy boron diffusion and drive-in to give a junction depth of $2.3 \mu\text{m}$. The intrinsic base was then formed by implantation of $^{11}\text{B}^+$. Implant doses ranged from 10^{12} to 5×10^{12} atoms/ cm^2 at energies of 30 keV

FIGURE 4.4 TRANSISTOR MASK LAYOUT

FIGURE 4.5 STRUCTURE OF A POLYSILICON EMITTER TRANSISTOR

to 100 keV. Implant damage was removed by a 1 hour low temperature anneal at 650°C, followed by a high temperature anneal for 30 minutes at 950°C. The polysilicon emitter was deposited at a temperature of 627°C and a pressure of 0.4 Torr by low pressure chemical vapor deposition (LPCVD) in a 20%:13.5% SiH₄-to-PH₃ ratio ambient and then wet etched to form the emitter structure. The polysilicon target thickness was 150 nm. The flow of each source gas was controlled independently by a mass flow controller, thereby allowing the silane/phosphine ratio to be easily adjusted. The flow settings for silane and phosphine were 41.2 and 0.223 sccm respectively. The pressure of the LPCVD system was controlled by the speed of the vacuum pump and therefore was affected by the temperature, total gas flow, and reaction rate. The deposition temperature was monitored by a thermocouple which is extended into the reactor just below the wafers. The crystal structure of the deposited silicon is critically dependent upon the deposition temperature. This is particularly true at temperatures close to the amorphous-polycrystalline transition. At temperatures below 580°C the as-deposited film is essentially amorphous. Accordingly the temperature profile was maintained as flat as possible (+/- 2°C) over the length of the furnace tube. Waechter [Waec87] conducted SIMS (Secondary Ion Mass Spectroscopy) measurements on similar devices under identical deposition conditions and found a dopant

concentration of 4×10^{20} phosphorus atoms/cm³ for similar flow conditions.

4.5 TEST STRUCTURES

In addition to complete polysilicon emitter transistors, various test structures were fabricated. These included Van der Pauw crosses to measure polysilicon sheet resistance, four terminal Kelvin resistors to measure the resistivity of metal contacts to polysilicon, and various polysilicon emitter diodes. Complete process specifications are given in Appendices 1,2 and 3.

4.5.1 SHEET AND CONTACT RESISTANCES

Polysilicon thicknesses of between 100 nm and 150 nm were deposited onto thermal oxidized wafers. A furnace anneal was done at 900°C for 30 min. in N₂. The polysilicon was patterned by wet etching and an insulating layer of oxide was deposited. Contact windows were opened in the oxide followed by titanium silicide formation and Al/Ti:W deposition. An alternative contacting scheme of Al/Ti was often used. (Metallization schemes are discussed in chapter 5.)

4.5.2 JUNCTION QUALITY

To measure junction quality and compare contact schemes polysilicon diodes with areas ranging from 4×10^{-6} to $8 \times 10^{-3} \text{ cm}^2$ were fabricated. Thermal oxide was grown on a 2 Ωcm p-type silicon wafer and windows were etched. Removal of any native oxide was accomplished by an RCA clean and flash 10% HF dip. A 100 nm layer of polysilicon was deposited by LPCVD using the same parameters as described above. The backs of the wafers were metallized with aluminum to serve as the substrate contact. Front contacts were made using metallizations outlined in the next chapter.

All device characteristics were measured using an HP4145A Semiconductor Parameter Analyzer.

4.6 SUMMARY AND CONCLUSIONS

A Heatpulse 410 rapid thermal processor was used to anneal the polysilicon emitter devices. The mask set used to fabricate the devices contained transistors with emitter areas ranging from $5 \times 5 \text{ } \mu\text{m}^2$ to $10 \times 175 \text{ } \mu\text{m}^2$. Test structures to measure the extrinsic and intrinsic base sheet resistance, the polysilicon sheet resistance and the polysilicon-to-metal contact resistivity were also included.

To measure junction quality and compare contact schemes diodes and other structures were fabricated. Electrical test results are presented in the next chapter.

CHAPTER 5

METALLIZATION

5.1 INTRODUCTION

Refractory metal silicides and thin film barriers to prevent Al diffusion have found widespread applications in silicon VLSI fabrication as interconnects and contacts. In MOS technology, silicides are used in both source-drain and gate regions to reduce not only interconnect resistance, but also series resistance of contacts and diffusion regions. In advanced bipolar technology, silicides are used on top of both the emitter and base polysilicon layers for the same reason.

Two silicide contacts (titanium and platinum) were investigated as a possible means of reducing contact resistance. The advantages and problems associated with each are discussed in the next section. Also discussed is the investigation of two diffusion barriers (Ti:W and TiN) which are used in shallow junction devices to prevent aluminum-silicon interdiffusion.

5.2 ALUMINUM

Aluminum is widely used as a contact metal in the semiconductor industry, but diffuses rapidly along polysilicon grain boundaries above 375°C [FOSS80]. As such, the standard post-deposition, 450°C anneal (commonly known as a sinter) will easily short a polysilicon junction that is contacted with aluminum.

To circumvent the aluminum/silicon interaction, early devices at Carleton used unsintered (thermally evaporated) aluminum contacts [RoTa85]. It was suspected that such a contact could be quite resistive and therefore account at least in part, for the observed poor current handling capability associated with the Carleton transistors [Rowl88]. Keyes found that unsintered aluminum contacts to unannealed polysilicon were indeed of poor quality with non-ohmic behavior [Keye87]. Contact resistivity was of the order of 2000 $\mu\Omega\text{cm}^2$. This behavior can likely be attributed to the presence of a thin native oxide layer at the silicon/aluminum interface. Unsintered aluminum contacts to annealed polysilicon exhibited similar non-ohmic behavior and large contact resistance values (1000 $\mu\Omega\text{cm}^2$).

5.3 Al/Ti

Titanium is a promising contact material for polysilicon junctions. It is thermally stable in contact with silicon up to a temperature of 550°C [KaNa76]. It has the lowest barrier height among the noble and refractory metals (about 0.5eV for n⁺ silicon) [OtTu80]. Titanium is an oxygen getter and will reduce the native oxide on silicon. In addition titanium can be thermally evaporated, avoiding e-beam evaporation and the associated radiation damage [TiCr82]. The high bulk resistivity of titanium (40 $\mu\Omega\text{cm}$) [Keyes87] implies a large emitter spreading resistance. For this reason a double metal aluminum/titanium metallization scheme was often used as a contact.

5.4 PLATINUM SILICIDE

Noble metal silicides such as platinum silicide have long been used to form both Schottky barrier diodes (SBD) [AnLp70] on lightly doped silicon and ohmic contacts to heavily doped material in bipolar technologies [KaLe65]. Typically 20 to 100 nm of platinum is sputtered onto a clean silicon surface and sintered prior to aluminum metallization. Contact resistivities of approximately 3 $\mu\Omega\text{cm}^2$ have been obtained for both p⁺ and n⁺ silicon. The low contact resistance is due to the low barrier height

of the Pt/p+ Si system (.25ev) and to the migration (snow plow) of donor impurities at the PtSi/n+ interface [CPGB82].

5.4.1 EXPERIMENT

70 nm of Pt was sputtered onto 150 nm of phosphorus doped polysilicon annealed for 20 mins at 900°C. Platinum silicide was formed by reacting the platinum and polysilicon at 590°C for 30 minutes in a nitrogen ambient. Patches of unreacted Pt remained on the polysilicon following the anneal. Several authors have reported the existence of an unreacted Pt film following the anneal [CBBN83], [CPGB82]. Severi et al. theorized that this partial reaction is due to the presence of small amounts of oxygen that inevitably diffuses into the furnace chamber from the external ambient [SGGC77]. They maintain that to achieve a complete reaction, sintering must be done in a vacuum.

Following the sintering treatment the unreacted platinum is etched in a hot (50°C to 75°C) solution of aqua regia. This mixture of acids attacks Pt preferentially. There exists some disagreement in the literature as to its effect on the PtSi films. We found that the chemical etch attacked the silicide layer leaving clear etch pits. Kingzett and Ladas report having similar difficulties with the aqua regia attacking PtSi [KiLa75]. They identified a

thin oxide layer on top of the silicide that prevented the attack on the silicide. When the oxide layer was etched in an HF solution they observed a very rapid etch of the PtSi film by the aqua regia. The existence of a protective oxide on sintered PtSi has also been confirmed by Rand and Roberts [RaRo74]. Alternatively Andrews and Mozabito investigated the possible contamination of PtSi by aluminum and magnesium during Pt sputter deposition. It is the presence of these contaminants, they argue, which leads to a gross attack on the silicide during the platinum etch in aqua regia.

A second difficulty was found associated with the formation of PtSi and the subsequent etch of unreacted Pt. Etching of the unreacted platinum does not always proceed to completion. Small patches of platinum could remain even after a prolonged treatment (10 minutes) in the aqua regia solution. At higher etching temperatures these Pt patches tended to decrease in number and size. However, higher temperatures also increases the risk that an attack on the PtSi film will result. Due to the problems associated with etching and patterning, PtSi formation by RTA was not investigated.

5.5 TITANIUM SILICIDE

Titanium silicide has many advantages for VLSI applications including ease of formation, low resistivity and high temperature stability. The lowest eutectic temperature for titanium silicide is 1330°C as compared to 830°C for PtSi [Mura83]. It has also been reported that native oxide that is present on the silicon substrate is broken up by the titanium/silicon reaction resulting in a relatively clean silicide/silicon interface.

Previous studies reported rapid diffusion of titanium along the grain boundaries during conventional thermal annealing [WaMc85]. A number of authors have shown that rapid thermal annealing up to 1100°C for 10 seconds results in the formation of low resistivity titanium silicide with virtually no penetration of titanium along the grain boundaries [NaPS86], [PDSK85].

Muraka and Fraser investigated the interaction between titanium and polysilicon at sintering temperatures ranging from 400°C to 1100°C in a conventional furnace. It was found that phosphorus doping of as much as 10^{21} atoms/cm³ does not affect the growth kinetics of titanium silicide [MuFr80]. Yu et al. however, found that arsenic doping of the polysilicon retarded the titanium-silicon reaction [YuDr89].

Two major problems are encountered with titanium silicide formation. First, in a conventional furnace, titanium will immediately react with any residual oxygen before the silicide can be formed. To prevent this, the furnace has to be evacuated below 10^{-8} Torr and back filled with ultrapure nitrogen or alternatively the titanium must be covered with another material (with which it does not react at the proposed annealing temperatures e.g. Mo) to protect it from oxygen [PDSG85]. The first alternative means that present day production furnaces cannot be utilized, while the second alternative increases the complexity of the device processing.

The second major problem involves the lateral growth of TiSi_2 that may lead to shorts. Salicided MOSFETs are particularly prone. To a large extent this can be reduced by annealing Ti in nitrogen. It has been shown that the annealing ambient plays a major role in the lateral growth.

Problems of oxide growth upon the Ti film and lateral growth of TiSi_2 during annealing can be avoided if the standard furnace anneal is replaced by a rapid thermal anneal. With the inherent short temperature cycle lateral growth of the silicide film is minimized as is the reaction with oxygen.

5.5.1 EXPERIMENT

5.5.2 SHEET RESISTANCE MEASUREMENTS

150 nm films of "in-situ" doped (phosphorus) and undoped polysilicon were deposited by LPCVD. To ensure a clean titanium/polysilicon interface an RCA clean followed by an HF dip preceded the deposition of 50 nm of titanium. Before sintering, the RTA chamber was flushed for 1-5 minutes with nitrogen. Titanium silicide was formed using various thermal cycles. Temperatures ranged from 700°C to 1100°C and times from 10 to 20 seconds. The unreacted Ti:N layer was etched in $\text{NH}_4\text{OH}/\text{H}_2\text{O}_2/\text{H}_2\text{O}$.

Fig. 5.1 shows the sheet resistance of titanium silicide films formed on phosphorus doped polysilicon as a function of sintering temperature. The annealing time was 10 seconds. Sheet resistance measurements were made using a four point probe as well as a Van der Pauw cross. As a result of silicide formation, the sheet resistance (R_s) of the phosphorus-doped polysilicon decreased from 150-200 Ω/sq to 2-4 Ω/sq . These results compare favorably with those of Narayan et al. who report R_s values of 2 Ω/sq for titanium silicide formed at 900°C [NSBF86]. Fig. 5.2

FIGURE 5.1 SHEET RESISTANCE OF TITANIUM SILICIDE vs. ANNEAL TEMPERATURE (DOPED POLYSILICON)

FIGURE 5.2 SHEET RESISTANCE OF TITANIUM SILICIDE vs. ANNEAL TEMPERATURE (UNDOPED POLYSILICON)

shows sheet resistance values as a function of temperature for titanium silicide formed upon undoped polysilicon. There is no evidence for retardation of silicide formation in phosphorus doped films.

5.5.3 SILICIDE THICKNESS

Table 5.1 shows silicide thickness as a function of sintering temperature. Silicide thickness was measured by etching half the wafer, first in $\text{NH}_4\text{OH}/\text{H}_2\text{O}_2/\text{H}_2\text{O}$ (to remove the unreacted titanium) and then in a 10% HF solution (to remove the silicide) and measuring the resulting step using a DEKTAK IIA profiler.

TABLE 5.1

SILICIDE THICKNESS AS A FUNCTION OF TEMPERATURE

TEMPERATURE	TIME	THICKNESS	
		DOPED	UNDOPED
700°C	20 sec	40 nm	40 nm
800°C	20 sec	60 nm	59 nm
900°C	20 sec	60 nm	60 nm
1000°C	20 sec	60 nm	60 nm

5.6 Al/TiSi₂ CONTACTED DIODES

Diodes fabricated as discussed in chapter 4 with an Al/TiSi₂ contacted emitter exhibited rectifying behavior before the post-metallization sinter. As expected, the post-metallization sinter (450°C for 20 minutes) destroyed the devices. Reverse bias leakage currents were measured on the largest devices (300x300 μm^2) to minimize any edge effects.

Fig. 5.3 shows a typical I-V characteristic of a Al/TiSi₂ contacted polysilicon emitter diode before the metallization sinter. The slope of the curve in the forward bias regime (.4V to .8V) is very close to the ideal diode characteristic with $n=1.1$ (eqn (5.1):

$$J_f = J_{f0} e^{qV/nkT}. \quad (5.1)$$

However, at lower bias the device deviated from ideality indicating that recombination within the space-charge region is dominant. There is some evidence of high series resistance in the characteristic of Figure 5.3 since the curve deviates from a straight line at about 1 A/cm².

FIGURE 5.3 CURRENT-VOLTAGE CHARACTERISTICS FOR A POLY EMITTER DIODE

AREA = 20 μm x 20 μm

METALLIZATION: Al/TiSi₂

TiSi₂ FORMED AT 900°C, 10 s

Reverse bias leakage currents were measured to be 10 nA/cm^2 at 10 V reverse bias. It is likely that the recombination/generation sites present at the polysilicon/single crystal interface are responsible for the large junction leakage current. These non-ideal effects may be the result of residual radiation damage produced by the electron-beam aluminum evaporation. At voltages greater than 10 kV, the electron beam will cause Al to emit K-shell x-rays that penetrate into the surface regions of the silicon resulting in the production of recombination/generation sites.

The contact resistance values measured in this experiment were quite high, typically $10 \text{ } \mu\Omega\text{cm}^2$ at 10^3 A/cm^2 . In a commercial process the target resistivity of a metal contact is typically about $1 \text{ } \mu\Omega\text{cm}^2$ or less [Sze83]. Figure 5.4 shows that a 450°C post-metallization sinter completely shorted the junction. It was therefore decided to add a diffusion barrier between the Al and TiSi_2 .

FIGURE 5.4 CURRENT-VOLTAGE CHARACTERISTICS FOR A POLY
EMITTER DIODE FOLLOWING A 450°C SINTER

AREA = 20 μm x 20 μm

METALLIZATION: Al/TiSi₂

TiSi₂ FORMED AT 900°C, 10 s

5.7 DIFFUSION BARRIERS

5.7.1 Al/Ti:W/TiSi₂

The concept of using Ti:W as a diffusion barrier between aluminum and silicon is well known [HOSS87]. The Ti:W barrier was first proposed by Cunningham et al in 1970 to improve the thermal stability and corrosion resistance of contacts with gold wire bonding [CuFH70]. Gbate et al of Texas Instruments used Ti₃:W₇ as a contact barrier in the fabrication of their Schottky Barrier and p-n junction diodes [GBFM78]. They used an Al/Ti:W/PtSi scheme to contact their devices, which typically had junction depths of less than 0.5 μm . Tungsten is used because it has a comparable thermal expansion coefficient to silicon. The addition of tungsten also increases the temperature at which silicidation occurs, thus adding to the reliability of the contact metallization system. Titanium is used because of its ability to reduce any native oxide present on the polysilicon, ensuring a more intimate contact. Hara et al used Rutherford backscattering spectroscopy (RBS) to study interfacial reactions of the Al/Ti:W/Si systems [HOSS87]. The following conclusions were obtained: 1. No interfacial reaction occurred and the interface was stable at temperatures below 480°C and at 500°C for 20 seconds (when the annealing was performed by RTA). Reactions did occur at

500°C for 40 seconds - that is aluminum diffused through the W:Ti layer into the Si substrate. 2. When annealing was performed by conventional furnace heating, interdiffusion did not occur at 480°C. However, it occurred at 500°C after 30 minutes for a 70nm thick Ti:W barrier layer.

5.7.2 Ti:W DIFFUSION BARRIER DIODES

Polysilicon emitter diodes were once again used to study the Al/Ti:W/TiSi₂ metallization scheme. Ti:W (10 wt % Ti in W) was sputter deposited onto TiSi₂ formed as discussed in the last section. The Ti:W barrier layer was measured to be 100 nm thick. Prior to Ti:W deposition the TiSi₂ surface was sputter etched to ensure a clean Ti:W/TiSi₂ interface. The Ti:W had a resistivity of 80 $\mu\Omega\text{cm}$ as deposited. Al was then thermally evaporated onto the Ti:W and patterned. The Ti:W was patterned using NH₄OH/H₂O₂/H₂O for 10 seconds with no apparent attack on the overlying aluminum.

Figures 5.5, 5.6 and 5.7 show typical IV characteristics for diodes with TiSi₂ formation temperatures ranging from 700°C to 900°C. Pre-sintered diodes deviated from ideality at low bias indicating large recombination within the space charge depletion region. This is probably due to unannealed radiation damage created during the front

FIGURE 5.5 PRE AND POST SINTER CHARACTERISTICS

AREA = 20 μm x 20 μm

METALLIZATION: Al/T:W/TiSi₂

TiSi₂ FORMED AT 700°C, 10 s

SINTER: 450°C, 20 mins

FIGURE 5.6 PRE AND POST SINTER CHARACTERISTICS

AREA = 20 μm x 20 μm

METALLIZATION: Al/T:W/TiSi₂

TiSi₂ FORMED AT 800°C, 10 s

SINTER: 450°C, 20 mins

FIGURE 5.7 PRE AND POST SINTER CHARACTERISTICS

AREA = 20 μm x 20 μm

METALLIZATION: Al/T:W/TiSi₂

TiSi₂ FORMED AT 900°C, 10 s

SINTER: 450°C, 20 mins

metallization. Leakage currents were on the order of 5×10^{-6} A/cm² at 10V reverse bias. Figures 5.6 and 5.7 show similar results, however the reverse bias leakage current is an order of magnitude smaller. This may be due to the higher temperatures used in the TiSi₂ formation (800°C and 900°C for figures 5.6 and 5.7 respectively as compared to 700°C for figure 5.5). The higher anneal probably caused the junction to move further away from the generation/recombination sites present at the polysilicon/silicon interface.

For comparison figures 5.5 to 5.7 also show the IV characteristics of a sintered diode. The most dramatic difference between the pre- and post-sintered devices is the reduction in depletion region recombination current seen at low forward voltage bias. The reverse bias leakage current was measured to be 10×10^{-7} A/cm² at 10 V reverse bias. This is a slight improvement over the pre-sinter characteristics. Sintered devices also showed an improvement in series resistance as indicated by the greater current handling capability (10 A/cm² for the post sintered device as compared to 1 A/cm² for the pre-sintered device). Very low contact resistance values of 2 $\mu\Omega$ cm² were measured on the post-sintered devices. Due to the considerable improvement in the performance of the sintered device as compared to its non-sintered counterpart, it was concluded that the above contact scheme would be acceptable.

5.7.3 Al/TiN/TiSi₂

Titanium nitride (TiN) has been suggested as a suitable contact barrier layer [MoBR87], [Witt81],[Ho89]. Its barrier characteristics have been studied for films obtained by evaporation, reactive sputtering and nitrogen implantation into evaporated Ti films.

Recently, Kaneko et al. reported that a TiN barrier between Al and Silicon can be formed in contact holes by exposure of TiSi₂ to an N₂ ambient at 950°C for 30 minutes [KKS87].

Several studies have investigated the interface reaction of titanium and silicon as well as the formation of TiN barriers. Morgan et al. [MoBR85] conducted Auger Electron Spectroscopy (AES) and TEM analysis of thin titanium silicide films reacted at temperatures ranging from 400 to 1100°C. Their results are as follows: During RTA of Ti/Si in nitrogen, Ti first absorbs residual oxygen from the ambient and then starts to become nitride at the surface and silicide at the substrate. The oxygen is snowplowed ahead of the silicide reaction front, first into unreacted titanium and then into substitutional sites in the FCC (face centered cubic) lattice of the δ -TiN forming at the surface.

This causes the nitride reaction to cease and permits the silicided region to be converted into large grain, low resistivity TiSi_2 . The $\text{TiN}_x\text{O}_y/\text{TiSi}_2$ bilayer thus formed displays good high temperature stability. However, during extended annealing in nitrogen, the oxygen in the surface layer is gradually replaced permitting nitrogen to diffuse through and convert TiSi_2 into TiN .

Ku et al. [KLLS87] used Rutherford Backscattering (RBS), Cross-sectional Transmission Electron Microscopy (EXTEM) and Auger Electron Spectroscopy (AES) to study the formation of the $\text{TiN}_x\text{O}_y/\text{TiSi}_2$ bilayer and Transmission Electron Diffraction (TED) to identify the different phases. In their study, titanium films of 75 nm thickness were sputter deposited on P-type (100) Si wafers. The wafers were first annealed at a relatively low temperature (650°C , 30 s, N_2 ambient). The titanium nitride and unreacted Ti were then selectively removed in $\text{H}_2\text{O}_2:\text{NH}_4\text{OH}:\text{H}_2\text{O}$ solution, followed by a high temperature RTA at 900°C or higher. They concluded that $\text{Al}/\text{TiN}/\text{TiSi}_2/\text{Si}$ has good thermal stability up to 500°C , for 30 mins in forming gas. No dislocation loops (continuous array of point defects within the single crystal silicon) or other lattice defects were detected in the Si substrate following the anneal.

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5.7.4 TiN DIFFUSION BARRIER DIODES

Once again polysilicon emitter diodes were used to analyze the Al/Ti:N/TiSi₂ contact system. 100 nm of titanium was sputter deposited on 200 nm of phosphorus doped polysilicon. Two procedures were followed in the attempt to grow a TiN diffusion barrier. Both processes involved a two step anneal. The first anneal was intended to promote the formation of TiSi₂ while the second anneal was to promote the growth of TiN. In the first experiment titanium silicide was formed by RTA at 700°C for 10 seconds in a nitrogen ambient, creating a 40 nm thick silicide. Directly following the silicide formation a second anneal (950°C, 10 seconds in nitrogen) was performed to convert the remaining Ti to TiN. Sintering these devices completely destroyed the junctions. It is thought that the Ti reaction did not go to completion thus leaving a 20 to 30 nm layer of unreacted titanium. The 1 μm aluminum layer would quickly consume the titanium during the furnace sinter and proceed to short the emitter/base junction.

The second procedure also involved a two step process. However, following the first anneal (700°C, 10 s) any unreacted Ti was etched off in H₂O/NH₄OH/H₂O₂. A second anneal (950°C, 10 s) was then performed in an attempt to promote the reaction

The first anneal creates a 40 nm thick silicide layer while the second anneal converts the top layer of that silicide to TiN. Sintering these devices did not destroy the emitter/base junctions confirming that a TiN barrier had been created. Figure 5.8 shows the diode characteristics prior to sintering while figure 5.9 presents post-sintering characteristics. Reverse leakage currents of 10^{-7} A/cm² at 10 V reverse bias are exhibited with little improvement on the sintered devices. Contact resistivities of $2 \mu\Omega\text{cm}^2$ were observed.

FIGURE 5.8 PRE SINTER CHARACTERISTICS FOR A POLYSILICON
EMITTER DIODE

AREA = 20 μm x 20 μm

METALLIZATION: Al/TiN/TiSi₂

TiSi₂ FORMED AT 700°C, 10 s

TiN FORMED AT 950°C, 10 s

FIGURE 5.9 POST-SINTER CHARACTERISTICS FOR A POLYSILICON
EMITTER DIODE

AREA = 20 μm x 20 μm

METALLIZATION: Al/TiN/TiSi₂

TiSi₂ FORMED AT 700°C, 10 s

TiN FORMED AT 950°C, 10 s

5.8 COLLECTOR CONTACTS

Collector contacts (backsides) were formed by e-beam aluminum ($0.50\ \mu\text{m}$) followed by a conventional furnace sinter of 450°C for 20 minutes in H_2 . Prior to the e-beam Al deposition the wafer backs were flash dipped in 10% HF to remove native oxide.

5.9 SUMMARY AND CONCLUSIONS

Two silicides, platinum and titanium were investigated. PtSi formation was often found to be incomplete, however TiSi_2 was successfully formed. Diodes contacted with Al/Ti:W/TiSi_2 or Al/Ti:N/TiSi_2 survived the post-metallization sinter, with the former metallization scheme giving slightly lower resistance and higher current handling capability. For those devices with a sintered Al/T:W/TiSi_2 contact, deviation from ideality occurred at 10^2A/cm^2 . In comparison Al/TiN/TiSi_2 contacted diodes deviated from ideality at $.3\text{A/cm}^2$. Contact resistance values as low as $2\ \mu\Omega\text{cm}^2$ were measured on the former diodes. It was decided further experiments involving sintered devices would use the Al/Ti:W/TiSi_2 contact scheme.

CHAPTER 6

POLYSILICON EMITTER TRANSISTOR CHARACTERISTICS

6.1 INTRODUCTION

This chapter presents and discusses the characteristics of polysilicon emitter transistors which were subjected to various anneal cycles. Emitter and intrinsic base resistance, polysilicon sheet resistance and emitter Gummel numbers are given as a function of anneal temperature and time. Several different polysilicon emitter transistor structures were fabricated to investigate the possible trade-off between G_E and R_E . Type A devices had unannealed polysilicon contacted with unsintered Al/Ti. Type B devices used furnace annealed polysilicon contacted with unsintered Al/Ti. Type C devices were made with rapid thermal annealed polysilicon with unsintered Al/Ti contacts, while type D had sintered Al/Ti:W/TiSi₂ contacts on rapid thermal annealed polysilicon.

6.2 POLYSILICON SHEET RESISTANCE

The structure of polysilicon films is influenced by dopants, deposition temperature, and post-deposition heat cycles. 150 nm of phosphorus doped polysilicon was deposited and sheet resistance measurements were taken using both a Van der Pauw cross and four point probe. The sheet resistance for 100 nm of unannealed polysilicon deposited at 627°C was typically 2500 Ω/sq . After a 900°C, 30 minute furnace anneal values of 180 Ω/sq were obtained. To achieve a comparable sheet resistance using RTA a temperature of 1050°C for 6 seconds must be used. Figure 6.1 shows sheet resistance as a function of temperature for a 6 s anneal.

6.3 TRUE POLYSILICON EMITTERS (TYPE A)

Emitter Gummel numbers G_E of devices formed with unannealed polysilicon deposited on HF cleaned interfaces showed a large variation. Adjacent devices exhibited drastically different characteristics. G_E values ranged from below 10^{13} s/cm^4 to 8×10^{15} s/cm^4 . Due to the non-ideal characteristics exhibited by these devices at low bias levels, J_{C0} was determined by extrapolation from a J_C value of 1 A/cm^2 on the Gummel plot to zero forward bias.

FIGURE 6.1 POLYSILICON SHEET RESISTANCE AS A FUNCTION
OF ANNEAL TEMPERATURE (TIME=6 seconds)

FIGURE 6.1 POLYSILICON SHEET RESISTANCE AS A FUNCTION
OF ANNEAL TEMPERATURE (TIME=6 seconds)

Figure 6.2 shows the Gummel plot of an unannealed polysilicon device. The $\log (J_B)$ curves for most devices exhibited slopes much less than q/kT . Presumably the back injection current is so strongly suppressed that the base current is dominated by recombination in the base-emitter depletion region. Extremely high current gains are often exhibited in these devices. Keyes [Keye87] reports h_{FE} values of 30,000 on devices with lightly doped bases. Due to the non-ideal behavior of J_B h_{FE} is not constant but increases with forward bias until J_C approaches 10^3 A/cm^2 .

Although HF dipped, unannealed transistors can give extremely high emitter Gummel numbers as well as extraordinary d.c. current gains they also exhibit high and often non-ohmic emitter resistances. Due to the non-ideal characteristics of these devices emitter resistance measurements (both the Ning and Tang method and the open collector method) were made difficult. Using the open collector method, R_E values for unannealed HF dipped devices varied from 100 to $600 \mu\Omega\text{cm}^2$ at a current density of 500 A/cm^2 . These values are at least two orders of magnitude larger than the emitter resistance expected for a conventional device. The high emitter resistance exhibited by the true polysilicon emitter transistor extremely limits the use of these devices.

FIGURE 6.2 GUMMEL PLOT FOR AN UNANNEALED POLYSILICON EMITTER TRANSISTOR, TYPE A DEVICE

EMITTER AREA = 5 μm x 5 μm

METALLIZATION: Al/Ti

$G_E = 4.3 \times 10^{15} \text{ s/cm}^4$, $h_{FE} = 2400$

No correlation was observed between emitter resistance and G_E as collector currents remained identical from device to device yet the base currents differed by as much as two orders of magnitude. Poor reproducibility from device to device and wafer to wafer may be due to the irregular growth of a thin interfacial native oxide prior to polysilicon deposition as suggested by DeGraff et al. [DeDe79], or to variations in the microstructure of the polysilicon/silicon interface even in the absence of interfacial oxide.

6.4 FURNACE ANNEALED EMITTERS (TYPE B)

Figure 6.3 shows a Gummel plot of a furnace annealed device (900°C for 30 minutes in N_2). Figure 6.4 compares an unannealed device with a furnace annealed device. Furnace annealed devices showed far less variation in G_E than the unannealed devices. G_E averaged approximately $1.0 \times 10^{14} \text{ s/cm}^4$ with current gains ranging from 700 to 5000. The lower G_E values as compared to type A devices suggest that a reordering of the polysilicon/substrate interface takes place during the 900°C anneal. This may involve the disruption of interfacial oxide layers or perhaps simply a reduction in disorder in the first few atomic layers of the deposited polysilicon. TEM studies performed by Patton et al. show that a 900°C anneal for 3 hours resulted in disruption of the interfacial oxide [PaBP86]. Similar

FIGURE 6.3 GUMMEL PLOT FOR A FURNACE ANNEALED DEVICE
(TYPE B DEVICE)

EMITTER AREA = $5 \mu m \times 5 \mu m$

METALLIZATION: Al/Ti

$G_E = 1.0 \times 10^{15} s/cm^4$, $h_{FE} = 3900$

FIGURE 6.4 COMPARISON OF AN UNANNEALED DEVICE WITH
A FURNACE ANNEALED DEVICE

EMITTER AREA = 5 μm x 5 μm

METALLIZATION: Al/Ti

A resolution test chart featuring several groups of horizontal and vertical lines of varying thicknesses. Each group is accompanied by a numerical value indicating the resolution. The values include 1.0, 1.1, 1.25, 1.4, 1.6, 1.8, 2.0, 2.2, 2.5, 2.8, 3.2, 3.6, 4.0, 4.5, 5.0, and 5.6. The chart is used to measure the resolving power of imaging systems.

MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS
STANDARD REFERENCE MATERIAL 1010a
(ANSI and ISO TEST CHART No. 2)

studies by Wolstenhome et al. [WJAB87] indicates that a 900°C anneal for 30 minutes will also disrupt native oxide.

During the fabrication of furnace annealed devices the advantage of using a Rapid Thermal Processor for device annealing and dopant activation became evident. Due either to excessive emitter diffusion through the base or the formation of collector pipes many of the furnace annealed devices developed emitter-collector shorts.

Emitter resistances as measured by the Ning and Tang method varied from 10 $\mu\Omega\text{cm}^2$ to 20 $\mu\Omega\text{cm}^2$. The relatively high emitter resistance as compared to the value 1-2 $\mu\Omega\text{cm}^2$ expected for conventional npn transistors is probably due to the unsintered Al/Ti contact.

6.5 RAPID THERMAL ANNEALED EMITTERS (TYPE C and D)

Annealing temperatures ranged from 900°C to 1000°C while times varied from 3 to 120 seconds. The longer annealing times (greater than 30 s) were chosen to simulate furnace annealing since many devices given an actual furnace anneal failed, presumably due to diffusion of emitter dopant through the base. However, many of the simulated furnace devices also failed.

Depending upon the temperature of the anneal G_E values were quite uniform from run to run. Devices given an anneal at 1000°C often showed less variation across the wafer than those annealed at a lower temperature. Many of the devices annealed at temperatures of 950°C or less had Gummel plots similar to the unannealed devices. G_E for these devices averaged 7×10^{14} s/cm⁴. Figure 6.5 shows a comparison of an unannealed device and one given a 900°C, 5 sec anneal. Both devices show almost total suppression of back injection current. Perhaps the anneal was not long enough to induce the reordering of the polysilicon/single crystal substrate believed to occur in furnace annealed devices. Variation of G_E across the wafer may also result from poor thermal uniformity within the heating chamber of the rapid thermal processor. This is typical of many early RTA processors, including the Heatpulse 410.

FIGURE 6.5 COMPARISON OF AN UNANNEALED DEVICE AND
A DEVICE GIVEN A 900°C, 5 s ANNEAL

EMITTER AREA = 5 μm x 5 μm

METALLIZATION: Al/Ti

Figure 6.6 illustrates a Gummel plot for a Type D device annealed at 1000°C for 3 seconds. Even for this short anneal time there is a dramatic improvement in device characteristics as compared to the unannealed devices. Base current suppression as evident in the unannealed device (or those devices given a lower anneal temperature) is not seen in the 1000°C annealed device ($n=1.1$). It appears that as in the case of the furnace annealed device a reordering of the polysilicon/single crystal substrate has taken place.

R_E , as measured by the Ning and Tang method ranged from 2.5 to 37 $\mu\Omega\text{cm}^2$ depending upon the deposition quality and the type of metallization. The lowest R_E values were found on those devices that had a sintered Al/Ti:W/TiSi₂ contact (type D devices). Figure 6.7 compares two devices on the same wafer. One device was contacted with sintered Al/Ti:W/TiSi₂, while the other device was contacted with unsintered Al/Ti. Current capability for the sintered device is an order of magnitude greater than for the unsintered device. Prior to silicide formation the polysilicon sheet resistance for the devices shown was 150-200 Ω/sq , comparable to furnace annealed polysilicon. This suggests that the high emitter resistance is due to the unsintered Al/Ti contact. Devices given a 1000°C anneal with a sintered Al/Ti:W/TiSi₂ contact had R_E values as low as 2 $\mu\Omega\text{cm}^2$, comparable to commercial npn transistors.

FIGURE 6.6 GUMMEL PLOT FOR AN RTA POLYSILICON EMITTER TRANSISTOR
ANNEAL = 1000°C, 3 s

EMITTER AREA = 5 μm x 5 μm

METALLIZATION: Al/Ti:W/TiSi₂ (SINTERED)

TiSi₂ FORMED AT 800°C, 3 s

$G_E = 1.3 \times 10^{14} \text{ s/cm}^4$, $h_{FE} \approx 300$

FIGURE 6.7 COMPARISON OF A DEVICE CONTACTED WITH SINTERED
 Al/Ti:W/TiSi₂ AND A DEVICE CONTACTED WITH UNSINTERED Al/Ti

EMITTER AREA = 5 μ m x 5 μ m

TiSi₂ FORMED AT 800°C, 10 s

Due to the scatter of data it is hard to determine if there is a correlation between G_E and R_E . For devices with unsintered Al/Ti contacts G_E seems to decrease as R_E decreases. Very low R_E values ($2-3 \mu\Omega\text{cm}^2$) were measured on those devices having a sintered Al/Ti:W/TiSi₂ contact, however they also had high G_E values. In some instances G_E was as high as $5.5 \times 10^{15} \text{ s/cm}^4$.

Figure 6.8 compares the Gummel plot for two devices, one with a base implant of $5 \times 10^{12} \text{ atoms/cm}^2$ and the other $2 \times 10^{12} \text{ atoms/cm}^2$. The base current characteristic for the low dose implant is less ideal than the higher doped device showing the non-reproducibility of RTA. Figure 6.9 presents the common emitter characteristics for the device with a base implant of $5 \times 10^{12} \text{ atoms/cm}^2$. BV_{CEO} was 60V, while the Early voltage was found to be 130 V.

FIGURE 6.8 COMPARISON OF TWO RTA DEVICES

EMITTER AREA = 5 μm x 5 μm

METALLIZATION: Al/Ti

BASE IMPLANT OF DEVICE #1: 5×10^{12} atoms/cm²

BASE IMPLANT OF DEVICE #2: 2×10^{12} atoms/cm²

FIGURE 6.9 COMMON EMITTER CHARACTERISTICS OF A RTA DEVICE

BASE CURRENT IN INCREMENTS OF 10 nA

EMITTER AREA = 5 μm x 5 μm

METALLIZATION: Al/Ti

ANNEAL: 1000°C, 3 s

BASE IMPLANT OF DEVICE 2×10^{12} atoms/cm²

6.6 SUMMARY AND CONCLUSIONS

Table 6.1 gives a summary of typical R_E and G_E as a function of anneal cycle. As expected unannealed devices (type A) exhibited high emitter Gummel numbers. They also exhibited the highest emitter resistances. Furnace annealed devices (type B) showed a drastic reduction in G_E (a factor of 25), but with a dramatic improvement in R_E . Devices given a RTA had emitter Gummel numbers values comparable to and in some instances higher than those achieved with furnace annealed devices. Very low R_E values were measured on those devices having a sintered Al/Ti:W/TiSi₂ contact.

TABLE 6.1

device type	temp °C	time s	hFE	G_E s/cm ⁴	R_E μΩcm ²
TYPE-A Al/Ti	---	----	4000	2.5×10^{15}	450
TYPE-B Al/Ti	900	1000	3900	1.0×10^{14}	18 12[Keye87]
TYPE-C Al/Ti	900	5	2500	4.0×10^{14}	35-60
Al/Ti	1000	8	1000	7.3×10^{14}	12-35
TYPE-D Al/Ti:W/TiSi ₂	1000	5	1600	2.2×10^{15}	2-4
Al/Ti:W/TiSi ₂	800	3	2200	5.5×10^{15}	8-14

There was no correlation between R_E and G_E for HF cleaned unannealed devices. These devices exhibited a wide range of G_E values. This may be due to the presence of a thin native oxide of variable and uncontrolled thickness at the polysilicon/silicon interface. High emitter resistance can also be attributed to the low activation of emitter dopant in unannealed material and the non-ohmic nature of Al/Ti contact to such material.

During furnace annealing, it appears that a reordering of the interface takes place, as indicated by the near-ideal base currents and the uniformity of G_E values across the wafer. Total suppression of back injection current is no longer in evidence. This may be due to the disruption of the interfacial oxide.

Devices given a 3 second, 1000°C anneal showed improved reproducibility indicating that interfacial reordering may take place even at these short anneals. Longer anneal times simply diffuse the emitter junction further into the base region. RTA temperatures less than 1000°C were apparently not sufficient to break up the interfacial native oxide and/or cause a reordering of the polysilicon/substrate interface. The wide variance of emitter Gummel numbers

across the wafer seen at lower RTA temperatures indicates that the native oxide has not been disrupted or interfacial realignment has yet to take place. This is supported to some extent by Crabbe et al. [CHMP87] (RTA cycles) and Patton et al. [PaBP86] (conventional furnace) who observed that for improved epitaxial alignment high temperature anneals ($>1050^{\circ}\text{C}$) for shorter times were preferred over lower temperatures and longer times.

Correlation between R_E and G_E was difficult due to the scatter of data. It appears that as R_E decreases G_E also decreases. Unannealed devices exhibited high G_E and R_E values. This is expected as unannealed devices with high G_E values would have high emitter resistance due to the native oxide present at the polysilicon-monocrystalline interface. Annealing these devices above 1000°C disrupts the native oxide reducing R_E . Epitaxial realignment could also be responsible for the decrease of G_E .

CHAPTER 7: SUMMARY AND RECOMMENDATIONS

7.1 SUMMARY

The main goal of this thesis was to investigate the dependence of polysilicon emitter resistance and Gummel number on annealing temperature and time, particularly in the rapid thermal annealing regime. To accurately study emitter resistance, it was first necessary to develop an emitter metallization scheme with low contact resistivity. Early work showed that unsintered Al/Ti contacts often dominated emitter series resistance [Keye87]. For this reason improved contact schemes using Ti:W and TiN diffusion barriers over titanium silicide were investigated. Sintered Al/Ti:W/TiSi₂ contacts gave very low contact resistivity values of $2 \mu\Omega\text{cm}^2$.

The emitter resistance R_E of true polysilicon emitter structures varied from 400 to $600 \mu\Omega\text{cm}^2$ (at a current density of 500 A/cm^2), corresponding to voltage drops of between 200 to 300mV. These values are at least two orders of magnitude larger than the emitter resistance expected for a conventional device and sufficiently high to restrict applications of the true polysilicon emitter structure

[KeTa87]. It was confirmed that the true polysilicon emitter transistor could give emitter Gummel numbers G_E in excess of 10^{15} s/cm⁴, allowing common emitter current gains of over 30,000 to be achieved in devices with lightly doped bases [KeTa87]. In contrast, commercial transistors with conventional implanted emitters typically give G_E values no greater than 5×10^{13} scm⁻⁴. The high Gummel number and current gain is a result of almost total suppression of back injected holes. The mechanism responsible for the suppression of back injection is unclear. A number of studies have suggested that the current gain enhancement is controlled by an interfacial native oxide (which invariably grows in the emitter window between final cleaning of the wafers and the start of the polysilicon deposition) acting as a tunneling barrier [DeDe79]. G_E values varied across the wafer suggesting that a non-uniform native oxide had indeed been formed.

Emitters formed from polysilicon, furnace annealed at 900°C for 20 mins had substantially lower resistances (10 to 20 $\mu\Omega\text{cm}^2$) than the unannealed devices, possibly due to disruption of an interfacial native oxide and/or interface reordering. These devices showed far less variation in emitter Gummel number across the wafer than the unannealed devices. G_E values averaged 1.0×10^{14} scm⁻⁴. The lower emitter Gummel numbers supply further evidence that restructuring of the polysilicon/substrate interface takes

place during the anneal. TEM studies performed by Patton et al. support this finding [PaBP85].

A drawback of furnace annealing is that it precludes the use of narrow base widths. The increased thermal budget often introduces diffusion effects as was seen in the destruction of many of our furnace annealed devices. Rapid thermal annealing results in far less diffusion of emitter dopant into the base, and may avoid the formation of collector pipes and other anomalous diffusion effects.

Devices annealed within a rapid thermal processor at temperatures in the range of 800-950°C and contacted with unsintered Al/Ti had emitter resistances of 35-60 $\mu\Omega\text{cm}^2$. The high emitter resistance may be due to a number of factors: 1. The unsintered contact; 2. failure to totally restructure the polysilicon/substrate interface and 3. low dopant activation of the as-deposited "insitu" doped polysilicon. In terms of polysilicon sheet resistance a 1050°C RTA for 6 secs is equivalent to furnace annealing at 900°C for 30 mins (150 Ω/sq), whereas a 900°C anneal for 6 secs results in sheet resistance two to three times greater. Low emitter resistances were obtained on sintered Al/Ti:W/TiSi₂ contacted devices annealed at 1000°C. R_E values of 2-3 $\mu\Omega\text{cm}^2$ were obtained, comparable to commercial npn transistors of similar dimensions. In terms of emitter resistance, temperature had a more dramatic effect than

time. Higher temperatures for shorter times resulted in lower emitter resistance than lower temperatures and longer times. At the high temperature anneal, interfacial realignment appears to take place similar to the furnace annealed devices. Native oxide may be disrupted resulting in decreased resistance. Emitters formed at 1050°C by RTA had higher G_E values than furnace annealed devices (in some cases they were comparable to and higher than G_E of unannealed devices). Uniformity problems often plagued those devices annealed at lower temperatures. It may be that for the short times associated with RTA, total oxide disruption fails to take place. Temperature uniformity within the chamber is probably the main source of this problem.

7.2 RECOMMENDATIONS

To reliably reproduce high emitter efficiencies a better understanding of the mechanism responsible for the back injection is required. Examination of HF cleaned and deliberately oxidized interfaces using XTEM for the presence of a disordered layer, oxide disruption and epitaxial realignment should be carried out.

A study of polysilicon emitter diffusion into the base would be important, i.e devices with narrow base widths

should be investigated. A SIMS analysis to measure dopant concentration and distribution within the emitter is necessary.

A logical next step is to measure the dynamic characteristics such as f_T and switching time in simple digital circuits. Integration of rapid thermal annealed poly emitter structures into a conventional CMOS process would also be of interest. BICMOS processes offer the low power and high device density of CMOS with the high speed and current drive of bipolar devices [INMM86].

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APPENDIX 1: RUN SHEET FOR POLYSILICON EMITTER TRANSISTORS

- 1) Field Oxide Growth
 - (a) RCA Oxide Growth
 - (b) Oxidation at 1100°C
 - 5 min pre heat
 - 10 min dry O₂
 - 15 min wet O₂
 - 10 min dry O₂
 - 30 min anneal m N₂
- 2) Open Extrinsic Base Windows
mask Cu-078-01
negative PR, etch until bare Si
- 3) Extrinsic Base Boron Diffusion
 - (a) RCA clean
 - (b) Pre-dep, 1000°C
 - 5 min pre heat
 - 5 min warm up O₂ + N₂
 - 10 min dope O₂ + N₂ + dopant
 - 10 min hold O₂ + N₂
 - 10 min cool
 - (c) Boron deglaze
30 sec dip in HF
 - (d) Drive In 1100°C
 - 5 min pre-heat
 - 10 min dry O₂
 - 15 min wet O₂
 - 5 min dry O₂
 - 10 min cool
- 4) Phosphorous Backside Getter
 - (a) strip oxide from wafer backs, RCA clean
 - (b) Pre-dop 100°C
 - 5 min pre heat
 - 5 min warm up O₂ + N₂
 - 10 min dope O₂ + N₂ + dopant
 - 5 min hold O₂ + N₂
 - 10 min cool
 - (c) Phosphorous Deglaze: 10 sec dip in HF
 - (d) Drive in 950°C
 - 5 min pre-heat
 - 20 min wet O₂
 - 5 min dry O₂
 - 10 min cool

- 5) Open Intrinsic Base Windows
negative PR, mask cu-078-02, wet etch
- 6) Implant Oxide Growth
 - (a) RCA Clean
 - (b) Oxidation 1000°C
5 min pre heat
30 min dry O₂ + HCl
5 min dry O₂
10 min anneal N₂
10 min cool
- 7) Intrinsic Base Implant
- 8) Base Implant Anneal
 - (a) RCA clean
 - (b) Low Temperature Anneal 650°C
60 min anneal N₂
 - (c) High Temperature Anneal 950°C
5 min pre heat
30 min anneal
10 min cool
- 9) First Polysilicon Deposition
 - (a) RCA clean
 - (b) Interface Treatment
10 sec HF dip, 10 min rinse in DI water and
blowdry

OR

HF dip as above followed by 10 min dip in solution of
HCl: H₂O₂:H₂O (1:1:6) at 80°C, 10 min rinse in DI and
blow dry.

Proceed Immediately to NEXT STEP

- (c) Polysilicon deposition at 627°C, SiH₄=PH₃ 160:1
pressure 0.4 Torr
- 10) Pattern Polysilicon
 - (a) RCA clean
5 min pre heat N₂
30 min anneal N₂
10 min cool
- 12) Open second emitter window - 05
positive PR, mask cu-078, wet etch

-
- 13) Second emitter deposition
 - (a) HF dip or chemical oxidation
 - (b) Deposit as per first deposition
 - 14) Pattern Second Polysilicon Layer
positive PR, mask cu-078-06, wet etch
 - 15) Optional Anneal
Rapid Thermal Anneal

or

Furnace
 - 16) Open Base Contact Windows
negative PR, wet etch, mask cu-078-07
 - 17) Base and Emitter metallization
Flash dip in HF to clear residual oxide
 - (a) Ti deposition by thermal evaporation to thickness of between 70 to 100 nm do not break vacuum after deposition.
 - (b) Al deposition by thermal evaporation to thickness of at least 0.5 nm

APPENDIX 2: RUN SHEET FOR POLYSILICON EMITTER DIODES

- 1) Open windows in oxide
Mask cu-060-01, negative PR
- 2) Optional oxidation
 - (a) Chemical oxidation
RCA clean, HF dip
immerse in $\text{HCl}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ (1:1:6), 10 mins
spin dry
 - (b) Thermal Oxidation
30 min oxidation O_2
30 min anneal N_2

Proceed Immediately to Poly deposition.

- 3) Polysilicon Deposition
627 $^{\circ}\text{C}$, $\text{SiH}_4:\text{PH}_3$ 160:1
pressure 0.4 Torr
Target thickness 1500-2000 Angstroms
- 4) Pattern Polysilicon
Mask cu-060-02, Positive PR, wet etch.
- 5) Post Polysilicon deposition Anneal
20 min 900 $^{\circ}\text{C}$, N_2 ambient
- 6) Front Contact
 - (a) deposit 300-400 Angstroms of Ti, thermally evaporated
 - (b) Form silicide in Rapid Thermal Process Unit
700 $^{\circ}\text{C}$, 3 to 10 secs.
 - (c) Etch Ti:N
 - (d) React with N_2 at 700 $^{\circ}\text{C}$ - 1000 $^{\circ}\text{C}$, 3 to 10 secs

or

Deposit 300 angstroms of Ti:W

 - (e) Deposit 1nm Al, thermally evaporated
- 7) Back Metalization
10% HF dip
.5 nm of Al, e-beam
- 8) Contact Anneal
459 $^{\circ}\text{C}$, H_2 ambient, 20 mins

APPENDIX 3: RUNSHEET FOR KELVIN RESISTORS

Starting Material : p<100>
1000 angstroms of thermal oxide

- 1) Polysilicon Deposition
SiH₄:PH₃ 160:1, 627°C
pressure = .28 TORR, time=3 hrs., target thickness
= 300 nm
- 2) Pattern polysilicon
positive PR, wet etch, mask cu-083-01
- 3) Optional Polysilicon Anneal
900°C, N₂ ambient, 30 mins
- 4) Deposit Oxide 100nm, undoped LOTOX
Recipe #1, Pressure = 0.32 Torr, SiH₄=25%, O₂= 27.5%
- 5) Open Oxide Windows, mask cu-083-02
negative PR
- 6) Deposit Metal
Vacuum evaporation, e-beam or thermal

APPENDIX 4: PROCESSING DETAILS OF WAFERS

WAFER	BASE IMPLANT	POLYSILICON	METALLIZATION
GM-50	40 keV, 10^{12}	900°C, 5s $G_E = 3.9 \times 10^{14}$ $h_{FE} = 2500$ $R_E = 59.3$ $R_S = 200$	Al/Ti unsintered
GM-52A	30 keV, 5×10^{12}	1000°C, 5s $G_E = 2.2 \times 10^{15}$ $h_{FE} = 2700$ $R_E = 46$ $R_S = 140$	Al/Ti unsintered
GM-52B	30 keV, 5×10^{12}	1000°C, 5s $G_E = 2.2 \times 10^{15}$ $h_{FE} = 1600$ $R_E = 3$ $R_S = 3$	Al/Ti:W/TiSi ₂ sintered TiSi ₂ 700°C, 5secs
GM-54	30 keV, 5×10^{12}	900°C, 8s $G_E = 1.1 \times 10^{15}$ $h_{FE} = 1600$	Al/Ti unsintered
GM-55A	30 keV, 5×10^{12}	no anneal $G_E = 2.4 \times 10^{15}$ $h_{FE} = 1950$	Al/Ti unsintered
GM-55B	30 keV, 5×10^{12}	900°C, 30s $G_E = 1.8 \times 10^{15}$ $h_{FE} = 4925$	Al/Ti
GM-56	30 keV, 5×10^{12}	900°C, 3s $G_E = 1.0 \times 10^{14}$ $h_{FE} = 400$	Al/Ti unsintered
GM-58A	30 keV, 5×10^{12}	900°C, 3s $G_E = 5.4 \times 10^{14}$ $R_E = 53$	Al/Ti unsintered

R_E = Emitter resistance in $\mu\Omega\text{cm}^2$
 G_E = Emitter Gummel number in s/cm^4
 R_S = Emitter sheet resistance in Ω/sq

APPENDIX 4: CONTINUED

WAFER	BASE IMPLANT	POLYSILICON	METALLIZATION
GM-58B	30 keV, 5×10^{12}	900°C, 3s $G_E = 5.4 \times 10^{14}$ $h_{FE} = 300$ $R_E = 10$ $R_S = 8$	Al/Ti:W/TiSi ₂ sintered
GM-62	30 keV, 5×10^{12}	950°C, 5s $G_E = 5.4 \times 10^{12}$ $h_{FE} = 3024$ $R_E = 30$	Al/Ti unsintered
GM-65	40 keV, 5×10^{12}	1000°C, 8s $G_E = 7.3 \times 10^{14}$ $h_{FE} = 676$	Al/Ti unsintered
GM-67	50 keV, 5×10^{12}	1000°C, 5s $G_E = 5 \times 10^{14}$ $h_{FE} = 3200$ $R_E = 35$	Al/Ti unsintered
GM-68	50 keV, 5×10^{12}	furnace $G_E = 5 \times 10^{13}$ $h_{FE} = 300$	Al/Ti unsintered
GM-69	50 keV, 2×10^{12}	900°C, 10s $G_E = 9.2 \times 10^{13}$ $h_{FE} = 4500$ $R_E = 35$ $R_S = 200$	Al/Ti unsintered
GM-70	50 keV, 2×10^{12}	furnace $h_{FE} = 700$	Al/Ti unsintered

END

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