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**INTER-DIE OPTICAL INTERCONNECTS USING
MICROMACHINED HOLOGRAPHIC LENS PLATES**

by

Christopher J. Reimer, B. Eng.

A thesis submitted to the
Faculty of Graduate Studies and Research
in partial fulfillment
of the requirements for the degree of

Master of Engineering

**Ottawa-Carleton Institute for Electrical Engineering
Department of Electronics
Faculty of Engineering
Carleton University**

October 1996

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ISBN 0-612-19504-X

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**"INTER-DIE OPTICAL INTERCONNECTS USING
MICROMACHINED HOLOGRAPHIC LENS PLATES"**

submitted by Christopher J. Reimer, B.Eng.
in partial fulfillment of the requirements for
the degree of Master of Engineering.

Thesis Supervisor

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June 1996

The information used in this thesis comes in part from the research program of Dr. Barry Syrett and Dr. Jacek Chrostowski (NRC-ITT). The research results appearing in this thesis represent an integral part of the ongoing research program. All research results in this thesis including tables, graphs and figures but excluding the narrative portions of the thesis are effectively incorporated into the research program and can be used by Dr. Syrett and his associates for education and research purposes, including publication in the open literature with appropriate credits given to Christopher Reimer. Matters of intellectual property may be pursued collaboratively with Carleton University and Dr. Syrett where and as appropriate.

Abstract

A design for an inter-die free-space optical link is given in this thesis, along with fabrication details on the creation of the micro-machined structures required to implement this link. An overview of various techniques for combining optical devices onto silicon substrates is given, along with a design of an OEIC, which was subsequently fabricated. In addition, an analysis of processing errors on holographic numerical aperture and efficiency is presented.

Acknowledgments

I wish to thank Dr. Barry Syrett and Dr. Jacek Chrostowski for being my thesis supervisors. Their help was appreciated throughout my project.

I would like to thank the National Research Council of Canada for allowing me to use their vast facilities while undertaking this research. I would also like to recognize the help of all the people in the Photonics section of the Autonomous Systems Laboratory at NRC, especially that from Les Chan, Ryan MacDonald, Simon Boothroyd, Bill Robertson and Ross Misner. I would also like to thank Lyall Berndt and Carol Adams of Carleton's integrated circuit fabrication facility.

On a more personal note, I would like to thank my family, and also Ian, Birkby and Minerva for their support.

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List of Symbols and Abbreviations

CW	Continuous Wave
DI	De-Ionized (water)
ECR	Electron Cyclotron Resonance (Etcher)
HOE	Holographic Optical Element
HMDS	Hexamethyldisilazane
IC	Integrated Circuit
LED	Light Emitting Diode
OE	OptoElectronic
OEIC	OptoElectronic Integrated Circuit
PR	Photoresist
RIE	Reactive Ion Etching
RCE LEDs	Resonant Cavity Enhanced Light Emitting Diode
VCSEL	Vertical Cavity Surface Emitting Laser
VLSI	Very Large Scale Integration (Integrated circuit)

1. INTRODUCTION

1.1 Introduction

Due to the continuously shrinking feature size of integrated circuits, the limiting factor in performance of current chips is increasingly becoming the interconnects, instead of the devices, transistors, themselves. This has been apparent since the mid nineteen eighties:

As switching components become smaller and less expensive, we begin to notice that most of our costs are in wires, most of our space is filled with wires, and most of our time is spent transmitting from one end of the wire to the other [1.1].

These phenomena can be seen in present day very large scale integrated (VLSI) circuits. In current high density VLSI chips, the area of the chip is typically determined by the interconnects, rather than the logic, or transistors themselves. This is due to the planar nature of the interconnection scheme used in current VLSI circuits. The average VLSI chip has two or three levels of low resistivity metal interconnects [1.2]. A greater number of interconnection levels is possible, and is being actively researched, but it is still a planar interconnection scheme and will only alleviate the interconnection problem temporarily [1.2]. Computer simulations have shown that with arbitrary, but constant, numbers of interconnect layers, growth rates of VLSI connection networks, independent

of chip area, are asymptotic as a function of the number of processing nodes (N) [1.3,1.4]. These simulations show that the area used by the logic increases with N , but the area used by the interconnects increases as N^2 . Obviously, as N increases, the majority of the area of the VLSI chip will be the interconnects.

Another limitation with VLSI chips, as these chips increase in size, and as their feature size is reduced, is due to the speed at which signals can travel down an electrical interconnect. Both resistance (R) and capacitance (C) of an electrical interconnect are proportional to the length (X) of the interconnect. The rise time (which is proportional to the product of resistance and capacitance) of a signal on this electrical interconnect is then proportional to X^2 , and the energy required to switch the state of the interconnect (which is proportional to capacitance) increases with X . As the minimum feature size decreases on a VLSI chip, the performance of the interconnects degrade as follows. If the VLSI chip is scaled down by a factor of M , the gate delay is reduced by a factor of M , and the switching energy is reduced by a factor of M^2 [1.5]. However, the rise time, or RC time constant, of the interconnect increases by a factor M^2 , for a fixed length of interconnect [1.5, 1.6]. Therefore, as VLSI chips become larger, the interconnects will become longer and this factor, along with the degradation of performance of electrical interconnects due to shrinking feature size will make interconnections even more problematic.

An additional problem with VLSI electrical interconnects is electromigration. As the feature size of the chip is reduced, by a factor of M , the cross-sectional area of the

conductors is reduced by a factor of M^2 , while the current is only reduced by a factor of M . This results in the current density increasing by a factor of M . This increase of current density causes damage, or erosion, to the conductor lattice itself, eventually causing a failure [1.6].

Finally, as the VLSI chips are reduced in size, the pitch between interconnect lines is reduced. This results in increased signal interference between interconnects due to crosstalk.

Electrical interconnects are becoming a limiting factor in some cases, and this has become apparent in technologies at the leading edge. As an example, Cray Research, Inc. has introduced the T90, a supercomputer system using an optically distributed clock. [1.7].

Optical interconnects have the ability to surmount all these drawbacks of electrical interconnects. The replacement of certain electrical interconnects with optical interconnects can result in increased communication speed, reduced area, reduced power consumption, increased fault tolerance, enhanced circuit testing capabilities, increased reliability, reduced cost and, eventually, dynamic interconnects [1.2, 1.6, 1.8-11].

1.2 Thesis Objectives

This thesis covers the technologies required to create an inter-die optical link as described in this thesis. The technologies required are the ability to place light sources, such as VCSELs or LEDs onto silicon dice, the creation and design of holographic reflective lenses, and the creation and design of micromachined structures that hold the holographic reflective lenses in the proper position. However, the technologies covered within this thesis are not limited to simple point to point optical communication links. The devices described within the thesis will also allow optical processing, point to multi-point communications, and numerous other applications.

The last technology, the creation and design of micromachined structures is the primary focus of the thesis, since the other two technologies are already being developed by numerous groups. Since micro-machining has never been tried before at the Carleton University fabrication facility, the majority of the thesis work was spent in developing a fabrication process that would create the micromachined structures.

In addition to the fabrication process, this thesis also presents a design for the holographic optical reflective lens, along with an analysis of the effects of processing errors on efficiency and numerical aperture of holographic lenses.

1.3 Inter-Die Optical Interconnect

The basic concept of the inter-die optical link is shown below:

Figure 1.1 Inter-Die Optical Link

The link simply consists of a free-space link formed by a light source, a detector, and two reflective lenses, the HOEs (Holographic Optical Element), to direct, collimate and focus the light. The HOE above the light source, whether it be an LED (Light Emitting Diode) or VCSEL (Vertical Cavity Surface Emitting Laser), focuses the light into a collimated beam, and directs it towards the HOE above the detector. The second HOE then reverses the effect of the first HOE, changing the collimated light into a converging beam, focusing the beam onto the detector.

Of course, since the entire link is formed on Si dice, various circuitry can be placed on the dice, allowing control of the light source, and also allowing processing of the data received on the other die.

A collimated beam is the most suitable method of transmitting light in a point to point link, since a collimated beam's width does not expand significantly as the beam propagates. This will minimize the power loss in the optical link, as well as keeping the size of the receiving HOE down to a reasonable size. At the detector, the collimated beam of light is focused into a point, where the detector lies. Focusing the light to a point allows the creation of a detector with a smaller active area, which minimizes capacitance, and therefore maximizes the data rate the optical link can handle.

The structure that hold the HOEs into position consists of three micromachined plates that are attached to the silicon die only by a hinge. By fabricating the wave plates flat, normal micro-fabrication techniques can be used to create them, since micro-fabrication techniques are unsuitable for growing three dimensional structures. The hinges allow the creation of three-dimensional structures by folding up two-dimensional structures off the surface of the die [1.12-14]. In this case, three plates interlock, one plate having the holographic reflective lens etched into its surface being held precisely at a 45° angle by two support plates. This can be seen in Figure 1.2, where one support plate is not shown for clarity.

Figure 1.2 Waveplate

The central waveplate is supported by a simple tab and slot arrangement. A tab on the central waveplate fits into a slot on the support waveplate, holding the central plate at a 45° angle.

2. INTEGRATION OF OPTICAL DEVICES ON SILICON

2.1 Introduction

In order to make the waveplates useful, a light source, typically being an LED or VCSEL would need to be placed onto the silicon wafer. There are a number of ways of integrating light sources onto silicon, each with their own set of advantages and disadvantages. One of the processes that will be described in the following sections was used to create a prototype OEIC (Opto-Electronic Integrated Circuit), which will be described as well.

2.2 Hybrid Integration Techniques

There are basically three ways of integrating optical devices onto silicon: direct epitaxy [2.1, 2], flip chip bonding [2.3-5] and thin film hybrid integration [2.6-13]. Direct epitaxy involves growing optical materials, such as GaAs, GaAlAs, InGaAlAs, InP, etc. on top of silicon. Some of the issues with this technique are the lattice mismatch, which occurs when the spacing between the atoms differs from one material to another, between the silicon substrate and the deposited semiconductor. The mismatching results in strained materials, either in tension or compression, with higher defects, which is a problem that grows with thicker layers. A method of overcoming this

problem involves the use of vicinal substrates. These are specially prepared substrates, which typically involve a number of etches and a heat cycle [2.14]. Another difficulty is that the substrate and grown semiconductor typically have differing thermal expansion coefficients. This forces all processing after the semiconductor epitaxial layer has been deposited to occur at low temperatures. The higher the temperature in latter processing steps, the greater the potential for crystal defects in both the epitaxial layer and the host substrate. In addition, there is silicon circuit thermal degradation due to the additional processing of the epitaxial semiconductor. Also, the silicon circuitry can be degraded due to the vicinal substrate as well. Finally, there is also the issue of the lifetime of the III-V devices grown on the silicon.

Another method of integrating optical devices onto silicon involves flip chip bonding. In this method solder bumps electrically connect the front faces of the silicon circuit and the optoelectronic devices.

Figure 2.1 Flip Chip Bonding

With this technique, the growth substrate must be optically transparent, and the electrical contacts must be bump bonded on the face of the OE device. However, this technique also has problems with cycling temperatures, as the OE device and the silicon wafer typically have different thermal expansion coefficients. Under large enough temperature cycles, the bump bonds will shear. This problem grows with size of the optical device.

Figure 2.2 Epitaxial Lift Off

A third technique of integrating optical devices on silicon is thin film hybrid integration. This technique can be done a number of different ways. As with flip chip

bonding, the silicon IC can be made on a standard process. One method of creating the thin film devices is epitaxial lift-off. This procedure follows these basic steps, as shown in Figure 2.2.

The initial bonding between the epilayer and the host substrate is just Van der Waals bonding, which can be problematic since devices can slip during thermal cycling, or during high acceleration. The sacrificial etch layer can be selectively etched from the epilayer of interest, if the sacrificial layer has a high Al composition. An etchant comprised of HF:H₂O (10% HF) will etch Al_xGa_{1-x}As (where $0.6 < x < 1$) 10^8 times faster than Al_xGa_{1-x}As (where $0 < x < 0.4$).

Figure 2.3 Selective Substrate Removal

Alternatively, selective substrate removal could be used to generate thin film devices as well. This process follows the steps shown in Figure 2.3.

For the selective substrate removal, the GaAs substrate can be etched from a AlAs stop etch layer using $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2$ (1:100), and then the AlAs stop etch layer can be removed using HF, whose etching characteristics compared to GaAs were described above for the epitaxial lift-off process.

Selective substrate removal can also be done for InP based devices. The InP substrate can be etched from an InGaAs or InGaAsP stop etch layer using HCL of $\text{HCL}:\text{H}_3\text{PO}_4$ (3:1) solution. The stop etch layer can be removed, if it is not part of the device, using an $\text{HF}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ (1:1:10) solution.

A problem with some of the above processes is exposing the epilayers to selective etches, which do etch the layer, albeit slowly. One method of eliminating this problem is mesa etching of the epilayers. This technique will protect the epilayers from selective etchants. In addition, this technique will also reduce the size of the devices, which will reduce the effect of differing thermal expansion coefficients.

Figure 2.4 Mesa Etching of Epitaxial Layers

Once the thin film device has been created, and removed from its growth substrate, there are a number of ways of integrating the thin film to its host substrate. One method of accomplishing this is bonding before substrate separation. This technique enables processing of both sides of the thin film devices while the devices are under substrate support. However, this method makes alignment to features on the host substrate quite difficult, as both the host and the growth substrate are typically opaque. Although IR aligning can be accomplished in most cases.

Figure 2.5 Bonding before Growth Substrate Removal

Another method of integration involves the use of a transfer diaphragm. This integration technique allows alignment with respect to features on the host substrate without etching, since the transfer diaphragm, if made from 4 μm mylar, is transparent. In order to get the devices to stick to the mylar, plasma etching of one side of the mylar is done to create dangling bonds, which provide the requisite stickiness. Also this technique allows coating of both sides of the thin film device while the device is under support. This allows various bonding options, including metal/metal bonding, which can provide electrical contact as well as preventing device slippage, which occurs with Van der Waals bonding.

Figure 2.6 Transfer Diaphragm Integration

A major advantage of thin film devices, which are on the order of a couple of microns thick, is that they appear almost monolithic on the host substrates. This allows standard fabrication processes to complete the integration of the thin film device, including vacuum coating of metals or dielectrics, CVD (Chemical Vapor Deposition) of dielectrics, photolithography, wet and dry etches, such as plasma etching, ECR (Electron Cyclotron Resonance) etching and RIE (Reactive Ion Etch) etching.

2.3 Prototype OEIC

Figure 2.7 Prototype OEIC CAD Layout

In order to apply these hybrid techniques, a prototype OEIC was designed by the author, and built. The silicon IC was designed using Magic 6.4, which was running on a PC running Linux. The chip itself was fabricated by MOSIS on their 2.0 μm TinyChip[®] process. The thin film resonant cavity enhanced LEDs (RCE LEDs) were fabricated by the Georgia Institute of Technology's Electronic Engineering division, where the thin film RCE LEDs were integrated with the MOSIS IC, as well. The prototype circuit consisted of two RCE LEDs, two Si BJT detectors, 2 LED drivers, a 4 bit counter with a

reset, a 6 bit pseudo-random bit stream generator with a reset, and a comparator. Figure 2.7 is picture of the CAD layout of the circuit, and Figure 2.8 photograph of the circuit itself.

Figure 2.8 Prototype OEIC

Note that the circuit layout describes only the top half of the chip. The functionality of the circuit is depicted in the block diagram, Figure 2.9.

Figure 2.9 Block Diagram of Prototype OEIC

The prototype chip was designed to simplify the testing by integrating a simplified self testing mechanism on the chip itself. The OEIC was designed to generate a pseudo-random bit stream, 63 bits in length, which would drive either one of the RCE LEDs. If the output of the LED is redirected back into the appropriate detector, the comparator will compare the detected optical information with the bit stream that was used to drive the RCE LED. Any bit errors discovered would increment the counter. This circuitry would allow a simple BER measurement of the device. In addition, either LED can be driven from an outside source, either through the onboard driver or by directly modulating the LED itself. Also, the output of either detector can be directed to an output pin.

3. REFLECTIVE 45° HOLOGRAPHIC LENS

3.1 Introduction

A holographic lens introduces a controlled spatially varying phase shift to incident light. This phase shift can convert an optical spherical wavefront, such that emitted from LEDs and VCSELs, into a collimated beam. This effect is not any different than what a normal lens accomplishes. However, a holographic lens can accomplish the same effect that a normal lens can accomplish in a lens thickness as thin as the wavelength of the light it is focusing, but only at that wavelength of light. This thinness of a holographic lens makes it amenable to creation by fabrication processes, where film growth and etching is only realistically possible in dimensions of the order of a few microns [3.1]

3.2 Reflective 45° Holographic Lens Design

The spatially varying phase shift that a holographic lens causes to an incident beam of light can be determined by finding the phase difference between the incident wavefront of light and the desired wavefront. These calculations can be simplified by assuming the holographic lens is transmissive instead of reflective. A diagram depicting the setup of an HOE is shown in Figure 3.1.

Figure 3.1 Setup of Holographic Lens

Since VCSELs and LEDs can be approximately represented by point sources of light, the incident wavefront to the lens can be represented by a spherical wavefront. The reflected wavefront will be a planar wavefront, a collimated beam, which will minimize beam spreading as the light propagates to the detector's holographic lens. At the other side of the optical link, at the detector, the second holographic lens then reverses the effect of the first lens. This lens converts the collimated beam into a converging spherical wavefront. The only difference between the two lenses may be the vertical location, y , of the focal point. This would cause the detector to have a different lens, but the procedure detailed below will be the same for both holographic lenses.

First of all, the incident and transmitted wavefronts must be described mathematically. The electric field of a point source is:

$$E_{pt} = E_{pto} \operatorname{Re}(e^{j\omega t - jkr}),$$

where $r = \sqrt{(x' - x'_o)^2 + (y' - y'_o)^2 + (z' - z'_o)^2}$

The electric field of a plane wave going through the transmissive lens is:

$$E_{pl} = E_{plo} \operatorname{Re}(e^{j\omega t - jk(y' \sin \alpha - x' \cos \alpha)})$$

Since the holographic lens has to introduce a phase difference equal to the difference between the phase terms of the point source and the plane wave, subtracting the phase terms of the above two equations will give the phase shift required. However, since a continuum of phase shifts cannot be created easily, a finite number of digitized phase shifts is used instead. The number of phase shift levels is equal to 2^L , where L is the number of mask layers used. That leads to the following formula, describing the locus of points with an integral number, n, of the minimum phase shift introduced by the hologram.

$$\frac{n\lambda}{2^L} = -y' \sin \alpha + \sqrt{x'^2 + (y' - y'_o)^2 + z'^2} \quad [1]$$

With some algebraic manipulation, the boundaries between the digitized phase levels can be represented by the following:

$$\frac{(y' - y'_c)^2}{a^2} + \frac{(z' - z'_c)^2}{b^2} = 1 \quad [2]$$

$$\begin{aligned}
y'_c &= \frac{2^L y_o' - n\lambda \sin \alpha}{2^L \cos^2 \alpha} \\
b^2 &= \left(\frac{n\lambda}{2^L} \right)^2 - x_o'^2 - y_o'^2 + \left(\frac{n\lambda \sin \alpha - 2^L y_o'}{2^L \cos \alpha} \right)^2 \\
a^2 &= \left(\frac{b}{\cos \alpha} \right)^2
\end{aligned} \tag{3}$$

Note that z'_c will be zero if the point source is directly below the center of the hologram. As can be seen from the above equations, the hologram will consist of non-concentric ellipses. Programs based on Equation 3 that generate files suitable for mask creation for these holograms have been developed [3.2].

The etch depth required for a binary phase reflective holographic lens is simply $\lambda/4$, irrespective of α . This is due to each point of light incident on the virtual reflective surface acting as a Huygen's wavelet, as shown in Figure 3.2. Figure 3.3 depicts an example of a two mask hologram tilted at 45° .

Figure 3.2 Huygen's Wavelets and Virtual Reflective Surfaces

An example of a four phase hologram is shown in Figure 3.3.

Figure 3.3 Four phase 45° Collimating Hologram

3.3 Analysis of Holographic Lenses

Holographic lenses fabricated with discrete levels are an approximation of a continuously curved surface, and as such, they do not focus as much light as a "perfect" lens. Due to this effect an important property of holographic lenses is their efficiency, which compares the power focused from a holographic lens to a "perfect" lens [3.3].

Figure 3.4 Holographic Lens Cross-section

As seen from section 3.2, holographic lenses consists of elliptical (circular for lenses perpendicular to the light being focused) steps.

Assume that at the center of each step, as shown in Figure 3.4, a perfect phase correction is performed on the incident light. It then follows that at either edge of each step the light has a phase error equal to $\lambda/2^{L+1}$, or $\pi/2^L$ where L is the number of mask levels used to generate the hologram. In addition, each step will reflect light having a phase range of $\lambda/2^L$.

Using a simplifying approximation that an equal amount of optical intensity is incident over the different optical path lengths on one step, the problem of calculating efficiency can be done in a one dimensional analysis. By looking at the cross-section of a hologram created by two masks the efficiency can be calculated by integrating the light reflected from the step that is in phase with the light receiving the "perfect" phase correction. The light reflected from the step can be described by the following equation, where the real part is in phase with the "perfectly" phase corrected light.

$$E_{step} = E_o \left(\cos \left(\frac{2\pi(P - P_o)}{\lambda} \right) + j \sin \left(\frac{2\pi(P - P_o)}{\lambda} \right) \right)$$

The efficiency can therefore be written as:

$$\begin{aligned}
 \eta &= \frac{\left(\int_{P=P_o - \frac{\lambda}{2^{L+1}}}^{P=P_o + \frac{\lambda}{2^{L+1}}} \operatorname{Re}[E_{step}] dP \right)^2}{\left(\int_{P=P_o - \frac{\lambda}{2^{L+1}}}^{P=P_o + \frac{\lambda}{2^{L+1}}} \operatorname{Abs}[E_{step}] dP \right)^2} = \frac{\left(E_o \int_{P=P_o - \frac{\lambda}{2^{L+1}}}^{P=P_o + \frac{\lambda}{2^{L+1}}} \cos\left(\frac{2\pi(P - P_o)}{\lambda}\right) dP \right)^2}{\left(E_o \int_{P=P_o - \frac{\lambda}{2^{L+1}}}^{P=P_o + \frac{\lambda}{2^{L+1}}} \sqrt{\cos^2\left(\frac{2\pi(P - P_o)}{\lambda}\right) + \sin^2\left(\frac{2\pi(P - P_o)}{\lambda}\right)} dP \right)^2} \\
 &= \frac{\left(\int_{P=P_o - \frac{\lambda}{2^{L+1}}}^{P=P_o + \frac{\lambda}{2^{L+1}}} \cos\left(\frac{2\pi(P - P_o)}{\lambda}\right) dP \right)^2}{\left(\int_{P=P_o - \frac{\lambda}{2^{L+1}}}^{P=P_o + \frac{\lambda}{2^{L+1}}} dP \right)^2} = \frac{\left(\int_{P=P_o - \frac{\lambda}{2^{L+1}}}^{P=P_o + \frac{\lambda}{2^{L+1}}} \cos\left(\frac{2\pi(P - P_o)}{\lambda}\right) dP \right)^2}{\left(\frac{\lambda}{2^{L+1}} - \left(-\frac{\lambda}{2^{L+1}}\right) \right)^2} \\
 &= \left(\frac{2^L}{\lambda} \int_{P=P_o - \frac{\lambda}{2^{L+1}}}^{P=P_o + \frac{\lambda}{2^{L+1}}} \cos\left(\frac{2\pi(P - P_o)}{\lambda}\right) dP \right)^2
 \end{aligned}$$

After integration, this equation simplifies down to:

$$\eta = \left(\frac{2^L \sin\left(\frac{\pi}{2^L}\right)}{\pi} \right)^2 \quad [4]$$

The results of this formula are depicted in Chart 3.1:

Chart 3.1 Efficiency versus Mask Levels

As can be seen from Chart 3.1, the efficiency goes up by 3 dB, from 40% to 81% from one mask to two, but additional mask levels introduce minimal gains.

Another important property of all lenses is the numerical aperture of a lens (NA). This parameter is the sine of the largest angle of light incident on a lens that is still properly focused, as shown in Figure 3.5.

Figure 3.5 Numerical Aperture of a lens

In holographic lenses, the numerical aperture increases with the size of the hologram, as with normal lenses. However, as a holographic lens gets larger, the width of the outer steps decreases. Therefore, the numerical aperture of a holographic lens is related to the minimum feature size of the process creating the lens.

With a hologram that is perpendicular to the incident light, the relationship between the numerical aperture and the minimum feature size is depicted in Figure 3.6.

Figure 3.6 Numerical Aperture for a Holographic Lens

The minimum feature size, mfs , of a hologram is proportional to the rate at which the optical path length changes with respect to the radial distance from the center of the hologram. The feature size is also related to the number of mask levels used, since the minimum feature size decreases by a factor of two with each additional mask layer.

$$mfs = \left| \frac{dy}{dP} \right|_{\min} \frac{\lambda}{2^L}$$

Figure 3.7 shows relationship between y and P , which is quite simple for a hologram that is perpendicular to the direction of light propagation, also called an on-axis hologram.

Figure 3.7 Relationship between P , y and θ for an On-Axis Hologram

This relationship between P , y and θ are also described mathematically by the following set of equations:

$$\begin{aligned}
y &= \sqrt{P^2 - d^2} \\
\frac{dy}{dP} &= \frac{P}{\sqrt{P^2 - d^2}} \\
\sin \theta &= \frac{y}{P} = \frac{\sqrt{P^2 - d^2}}{P} \\
\frac{dy}{dP} &= \csc \theta
\end{aligned}$$

Since $\csc \theta$ is monotonically decreasing for increasing θ , until $\pi/2$, which is the maximum θ can be in a physical system with a flat hologram, the minimum dy/dP can be replaced by one over the numerical aperture of the hologram.

$$\left| \frac{dy}{dP} \right|_{\min} = |\csc \theta_{\max}| = \frac{1}{|\sin \theta_{\max}|} = \frac{1}{NA}$$

$$mfs = \frac{\lambda}{2^L NA} \quad [5]$$

Equation 5 states the relationship between the minimum feature size and numerical aperture for an on-axis hologram.

In the case of a tilted, or off-axis hologram, the relationship between the minimum feature size and the numerical aperture is the same as the on-axis hologram for the axis within the plane of the hologram that is perpendicular to the direction of propagation of

the incident light, or axis_p . However along the axis within the plane of the hologram perpendicular to the previously described axis, or axis_{np} , the relationship between the minimum feature size and numerical aperture is different. These two axes, axis_p and axis_{np} are depicted in Figure 3.8.

Figure 3.8 Axes of Interest with the Plane of an Off-Axis Hologram

Looking at an off-axis hologram on its side, as depicted in Figure 3.9, the equations describing the optical path lengths for axis_{np} can be easily determined:

Figure 3.9 Relationship between P , θ and y for an Off-Axis Hologram

As in the case of an on-axis hologram, the minimum feature size, mfs , of a hologram proportional to the rate at which the optical path length changes with respect to the radial distance from the center of the hologram. Therefore, the initial formula for an off-axis hologram for axis_{np} is still:

$$mfs = \left| \frac{dy}{dP} \right|_{\min} \frac{\lambda}{2^L}$$

For axis_{np} the relationship between P and y is a little more complicated than for axis_p, as shown by the following set of equations:

$$P_1 = \frac{d \cos \alpha}{\cos(\alpha + \theta)}$$

$$P_2 = -d \cos(\alpha) \sin(\alpha) \tan(\alpha + \theta)$$

$$P = P_1 + P_2 = \frac{d \cos \alpha}{\cos(\alpha + \theta)} - d \cos(\alpha) \sin(\alpha) \tan(\alpha + \theta)$$

$$y = d \cos(\alpha) \tan(\alpha + \theta)$$

$$\frac{dP}{d\theta} = d \cos(\alpha) [\sec(\alpha + \theta) \tan(\alpha + \theta) - \sin(\alpha) \sec^2(\alpha + \theta)]$$

$$\frac{dy}{d\theta} = d \cos(\alpha) \sec^2(\alpha + \theta)$$

$$\frac{dP}{dy} = \frac{dP}{d\theta} \frac{d\theta}{dy} = \frac{d \cos(\alpha) [\sec(\alpha + \theta) \tan(\alpha + \theta) - \sin(\alpha) \sec^2(\alpha + \theta)]}{d \cos(\alpha) \sec^2(\alpha + \theta)}$$

$$\frac{dP}{dy} = \frac{dP}{d\theta} \frac{d\theta}{dy} = \sin(\alpha + \theta) - \sin \alpha$$

Chart 3.2 Abs [dy/dP] versus θ

The range of $\alpha+\theta$ that is valid for a physical system is from $-\pi/2$ to $\pi/2$, which, in the case of α being $\pi/4$, limits θ to be within $-3\pi/4$ to $\pi/4$. Within these limits, the absolute value of dy/dP is monotonically decreasing for the absolute value of θ increasing, as shown in Chart 3.2. The minimum absolute value of dy/dP occurs at the most negative θ . With a light source that is symmetric about the $\theta = 0$ axis, the relationship between the minimum feature size and the numerical aperture can be written as:

$$mfs = \left| \frac{dy}{dP} \right|_{\min} \frac{\lambda}{2^L} = \frac{\lambda}{2^L [\sin(\sin^{-1}(NA) - \alpha) + \sin \alpha]} \quad [6]$$

Equation 6 describes the relationship between the minimum feature size of an off-axis hologram along axis_{np} and the hologram's numerical aperture.

Chart 3.3 Normalized Minimum Feature Size versus θ for $\alpha = 45^\circ$

Chart 3.3 compares the relationship between θ , where $\sin \theta = NA$, and the minimum feature size for the two axes, $axis_p$ and $axis_{np}$. In the case of α being 45° , $axis_p$ will always have the more critical minimum feature size. Therefore, in the case of α being 45° , the minimum feature size of the hologram is along $axis_p$, which is given by Equation 7.

$$mfs = \frac{\lambda}{2^L NA} \quad [7]$$

3.4 Effects of Processing Errors on Hologram Efficiency

The analysis done in section 3.3 assumes that the hologram was perfectly created. However, the processing steps used to create these holograms could introduce errors into the holographic patterns, reducing the effectiveness of its focusing capabilities.

The errors that could be introduced into the holograms are etch depth errors, alignment errors between mask layers (assuming multiple mask layers are used), exposure errors and curvature of the wave plates [3.3].

On a binary phase hologram, the electric field intensity at the focus can be thought of as having two components, one component having no phase shift from the hologram, and the other component having a π phase shift from the hologram. Assuming that equal

light intensities are incident on either phase of the hologram, the power at the focus of the hologram would be:

$$P = (E_0 + E_\pi)^2 = 2E_0^2$$

However, if there was an error, e , in the phase correction of the nominally π corrected light, the power would be:

$$P = \left(E_0 + E_\pi \cos\left(\frac{2\pi e}{\lambda}\right) \right)^2$$

Normalizing this equation to one for a perfect hologram, the efficiency due to the etch depth error for both transmissive and reflective lenses are given by Equation [8], where $r = 0$ for transmissive lenses and $r = 1$ for reflective lenses.

$$\eta = \frac{\left(1 + \cos\left(\frac{2\pi 2^r e}{\lambda}\right) \right)^2}{4} \quad [8]$$

The reflective lenses will magnify the etch error by a factor of two, since the light travels the depth of the etch twice with a reflective lens, once when it is incident to the hologram and again after it is reflected from the hologram.

Chart 3.4 Etch Depth Error versus Efficiency

As shown in Chart 3.4, a -3 dB loss in efficiency in a reflective hologram occurs with an etch error of $\pm 0.091 \lambda$. This would be the minimum etch accuracy required in a binary phase hologram. However, for multiple level holograms, the accuracy of all etches would have to increase significantly in order to achieve the marginal increases of efficiency that each additional mask layer theoretically allows. In order to derive an equation describing the minimum required etch accuracy, the efficiency with etch error is assumed to be the efficiency of a perfectly etched hologram with one less mask layer. The following formula will give the minimum required tolerance in etch depth in order to achieve this assumption. The efficiencies η_L and η_{L-1} are given by Equation [4], found in section 3.3.

$$\frac{\eta_L}{\eta_{L-1}} \left(\frac{1 + \cos\left(\frac{2\pi 2^r e}{\lambda}\right)}{2} \right)^2 = 1$$

$$e = \frac{\lambda}{2\pi 2^r} \cos^{-1} \left(\frac{\sin\left(\frac{\pi}{2^{L-1}}\right)}{\sin\left(\frac{\pi}{2^L}\right)} - 1 \right) \quad [9]$$

Again, in Equation [9], $r = 0$ for a transmissive lens, and $r = 1$ for a reflective lens.

Chart 3.5 Required Etch Accuracy versus Number of Mask Levels

As can be seen in Chart 3.5, the requirements for the reflective lenses are always more stringent than for transmissive lenses, in addition to the additional etch accuracy required for greater numbers of mask levels.

Misalignment of multiple mask layers can also cause reductions in efficiency. However, an exact calculation of the reduction in efficiency that a particular alignment

error on a particular hologram with a particular incident optical power distribution would be very complicated. To create a relatively simple alignment requirement, a few approximations are required.

Alignment errors only affect the holographic phase steps when the alignment shift has a directional component perpendicular to the phase steps. Obviously an alignment shift will affect most of the hologram, but some parts of it, whose steps run parallel to the alignment shift, will be totally unaffected. By assuming that the alignment error is normal to all phase steps on the hologram, the problem of calculating efficiency is reduced significantly. In addition, given the required numerical aperture of the hologram, the minimum feature size of the hologram will be used to determine the efficiency.

Figure 3.10 depicts an alignment error of distance e , on hologram created by two mask levels.

Figure 3.10 Alignment Errors on a Two Mask Hologram

The calculation of efficiency can be done as it was in section 3.3, in Equation [4], where the efficiency of multiple level holograms was calculated. The error, e , is expressed as a phase error in the cosine terms, given by the following simple relationship.

$$\Delta P = \frac{e\lambda}{2^L mfs} = \frac{e\lambda}{4mfs}$$

$$\begin{aligned}
\eta &= \frac{1}{\lambda^2} \left[\int_{P=P_{o1}-\frac{\lambda}{8}}^{P=P_{o1}+\frac{\lambda}{8}-\Delta P} \cos\left(\frac{2\pi(P-P_{o1})}{\lambda}\right) dP + \int_{P=P_{o2}-\frac{\lambda}{8}}^{P=P_{o2}+\frac{\lambda}{8}-\Delta P} \cos\left(\frac{2\pi(P-P_{o2})}{\lambda}\right) dP + \right. \\
&\quad \left. \int_{P=P_{o2}+\frac{\lambda}{8}}^{P=P_{o2}+\frac{\lambda}{8}} \cos\left(\frac{2\pi(P-P_{o2})}{\lambda} + \frac{\pi}{2}\right) dP + \int_{P=P_{o1}-\frac{\lambda}{8}}^{P=P_{o1}+\frac{\lambda}{8}-\Delta P} \cos\left(\frac{2\pi(P-P_{o3})}{\lambda}\right) dP + \right. \\
&\quad \left. \int_{P=P_{o4}-\frac{\lambda}{8}}^{P=P_{o4}+\frac{\lambda}{8}-\Delta P} \cos\left(\frac{2\pi(P-P_{o4})}{\lambda}\right) dP + \int_{P=P_{o4}+\frac{\lambda}{8}}^{P=P_{o4}+\frac{\lambda}{8}} \cos\left(\frac{2\pi(P-P_{o4})}{\lambda} + \frac{\pi}{2}\right) dP \right] \\
&= \frac{1}{\lambda^2} \left(2 \int_{P=-\frac{\lambda}{8}}^{P=\frac{\lambda}{8}-\Delta P} \cos\left(\frac{2\pi P}{\lambda}\right) dP + 2 \int_{P=\frac{\lambda}{8}-\Delta P}^{P=\frac{\lambda}{8}} \cos\left(\frac{2\pi P}{\lambda} + \frac{\pi}{2}\right) dP + 2 \int_{P=-\frac{\lambda}{8}}^{P=\frac{\lambda}{8}-\Delta P} \cos\left(\frac{2\pi P}{\lambda}\right) dP \right)^2 \quad [10] \\
&= \frac{1}{\pi^2} \left(\sqrt{2} + \sin\left(\frac{\pi}{4} + \frac{\pi e}{2mfs}\right) + 2 \sin\left(\frac{\pi}{4} - \frac{\pi e}{2mfs}\right) - \sin\left(\frac{3\pi}{4} - \frac{\pi e}{2mfs}\right) \right)^2
\end{aligned}$$

Equation [10] already includes the 81% efficiency for a perfectly formed two mask hologram.

Chart 3.6 Efficiency versus Alignment Error for a Two Mask Hologram

Similar equations can be easily determined for multiple mask holograms, based on the previous example. It is interesting to note that for multiple mask holograms, misalignment in the finer masks is more detrimental to the efficiency of a hologram than masks of less finesse for that same hologram.

Exposure errors have a similar effect on holograms as alignment errors do. Instead of a shift in an alignment mask, the phase step that a mask is supposed to create may be wider, or smaller than it is supposed to be. Figure 3.11 depicts this situation.

Figure 3.11 Exposure Errors

Calculating the efficiency of a hologram depicted in Figure 3.11 is very similar to the efficiency calculations performed for alignment errors, given in Equation [10].

$$\begin{aligned}
 \eta &= \frac{1}{\lambda^2} \left(\int_{P=P_{o1}-\frac{\lambda}{8}}^{P=P_{o1}+\frac{\lambda}{8}+\Delta P} \cos\left(\frac{2\pi(P-P_{o1})}{\lambda}\right) dP + \int_{P=P_{o2}-\frac{\lambda}{8}+\Delta P}^{P=P_{o2}+\frac{\lambda}{8}-\Delta P} \cos\left(\frac{2\pi(P-P_{o2})}{\lambda}\right) dP + \right. \\
 &\quad \left. \int_{P=P_{o2}+\frac{\lambda}{8}-\Delta P}^{P=P_{o2}+\frac{\lambda}{8}} \cos\left(\frac{2\pi(P-P_{o2})}{\lambda} + \frac{\pi}{2}\right) dP + \int_{P=P_{o3}-\frac{\lambda}{8}}^{P=P_{o3}+\frac{\lambda}{8}+\Delta P} \cos\left(\frac{2\pi(P-P_{o3})}{\lambda}\right) dP + \right. \\
 &\quad \left. \int_{P=P_{o4}-\frac{\lambda}{8}+\Delta P}^{P=P_{o4}+\frac{\lambda}{8}-\Delta P} \cos\left(\frac{2\pi(P-P_{o4})}{\lambda}\right) dP + \int_{P=P_{o4}+\frac{\lambda}{8}-\Delta P}^{P=P_{o4}+\frac{\lambda}{8}} \cos\left(\frac{2\pi(P-P_{o4})}{\lambda} + \frac{\pi}{2}\right) dP \right) \\
 &= \frac{1}{\lambda^2} \left(2 \int_{P=-\frac{\lambda}{8}}^{P=\frac{\lambda}{8}+\Delta P} \cos\left(\frac{2\pi P}{\lambda}\right) dP + 2 \int_{P=\frac{\lambda}{8}-\Delta P}^{P=\frac{\lambda}{8}} \cos\left(\frac{2\pi P}{\lambda} + \frac{\pi}{2}\right) dP + 2 \int_{P=-\frac{\lambda}{8}+\Delta P}^{P=\frac{\lambda}{8}-\Delta P} \cos\left(\frac{2\pi P}{\lambda}\right) dP \right)^2 \quad [11] \\
 &= \frac{1}{\pi^2} \left(\sqrt{2} + \sin\left(\frac{\pi}{4} + \frac{\pi e}{2mfs}\right) + 2 \sin\left(\frac{\pi}{4} - \frac{\pi e}{2mfs}\right) - \sin\left(\frac{3\pi}{4} - \frac{\pi e}{2mfs}\right) \right)^2
 \end{aligned}$$

The result of Equation [11] is the same as Equation [10], for a two mask hologram. As with Equation [10], Equation [11] already includes 81% efficiency of a two mask hologram.

The final processing error that can occur to these holograms is a curvature in the waveplates. This situation is very similar to an etch error, with the exception that the phase errors occur at all phase steps, instead of only those steps actually etched and only

on the outer elliptical phase steps. Obviously curvature of the waveplates will reduce the numerical aperture of the hologram.

Given a required numerical aperture and focal length, the required maximum curvature can be determined from the following procedure. Figure 3.12 illustrates the definition of curvature, while Figure 3.13 depicts the relationship between x , y , NA and f .

Figure 3.12 Definition of Curvature

Figure 3.13 Relationship between NA, f , x and y

The light being reflected from the outer rings of the hologram will have optical path length error given by the following equations, assuming R is much larger than y :

$$\begin{aligned}
x^2 + y^2 &= R^2 \\
(R - \Delta P)^2 + y^2 &= R^2 \\
\Delta P &\cong \frac{y^2}{2R} \\
y &= \frac{f \tan \theta}{\cos \alpha} = \frac{f \tan(\sin^{-1} NA)}{\cos \alpha} \\
\Delta P &\cong \frac{(f \tan(\sin^{-1} NA))^2}{2R \cos^2 \alpha}
\end{aligned}$$

The efficiency of the light being reflected from the outer phase rings of the hologram depend on how far out of phase they are with respect to the light being reflected by the center of the hologram. The efficiency of the outer rings of the hologram can easily be calculated by Equation [12] as:

$$\eta = \left(\cos \left(\frac{2\pi \Delta P}{\lambda} \right) \right)^2 = \left(\cos \left(\frac{\pi (f \tan(\sin^{-1} NA))^2}{\lambda R \cos^2 \alpha} \right) \right)^2 \quad [12]$$

With a maximum drop in efficiency of -3 dB, the minimum radius of curvature of the waveplates will be given by Equation [12].

$$R = \frac{4(f \tan(\sin^{-1} NA))^2}{\lambda \cos^2 \alpha} \quad [12]$$

The waveplates being built were designed to hold reflective two mask holograms with a focal length of $25\text{ }\mu\text{m}$, $\alpha = 45^\circ$, a numerical aperture of 0.259, for $\lambda = 850\text{ nm}$. Applying these numbers to the equations above give the hologram a nominal efficiency of 81% and a minimum feature size of $0.821\text{ }\mu\text{m}$. The equations also suggest a minimum accuracy on the etch depth of 77 nm , a maximum mask misalignment or exposure error of $0.19\text{ }\mu\text{m}$, and a minimum radius of curvature for the waveplate of $422\text{ }\mu\text{m}$.

4. FABRICATION OF MICRO-MACHINED HINGED LENS PLATES

4.1 Introduction

Since details required for fabricating micro-machined structures were not available to the author, much of the work in this thesis involved creating a process that could generate the micro-machined waveplates. Therefore, this chapter will describe, in detail, the process developed to create the micromachined plates.

Holograms were not included into the fabrication run, in order to make developing a process for the creation of the wave plates simpler.

4.2 Outline of Fabrication Steps

The wave plates were built with a four mask layer process. The first layer that was deposited was a phosphorous doped oxide, which was then patterned to create "dimples" in the surface of the oxide that do not extend down to the silicon wafer surface.

Figure 4.1 First Oxide Layer

These dimples are created so that the polysilicon layer that is placed on top of it will have protrusions that will hold the waveplate off the surface of the silicon wafer once the oxide is etched away. This is done to make the assembly of the waveplates feasible, since both the polysilicon and the silicon wafer are optically smooth, and any contact between them will have a significant, in comparison to the strength of the material, Van der Waals force holding them together. In addition, these waveplates were created without any automated means of assembly, again to simplify the development of a workable process. So the dimples were also created to assist in the manual assembly of the waveplates.

The next step is to place a layer of undoped polysilicon on the wafer. This layer is then patterned into the wave plates which will be the parts freely rotating from the plane of the wafer at the end of the process.

Due to the low temperature of the polysilicon deposition, the reason for which will be explained in a following section, the polysilicon does not flow during the deposition, so the dimples etched into the oxide layer also exist in the polysilicon. The waveplates patterned into this polysilicon layer are perforated to quicken the final release etch of oxide. The perforations allow the oxide etch to flow through them, instead of just allowing the etchant to flow under plates. In addition, one side of the waveplates is patterned into a hinge pin, around which the waveplate will rotate.

Figure 4.2 First Poly-Silicon Layer

Another layer of phosphorous doped oxide is then deposited on the polysilicon. This layer's purpose is to physically isolate the second polysilicon layer from the first polysilicon layer, which was described above. After this layer is patterned, the layer also shapes the second polysilicon layer, which will be described below, into the hinge loops which surround the hinge pin and contact the silicon wafer. Again, the deposition

temperature of the oxide is too low for the oxide to flow, so the surface irregularities of the polysilicon layer below it, such as the perforations, will appear on the surface of the oxide as well. The patterning of the oxide creates holes in the oxide that extend through the hinge holes of the first polysilicon layer and through the first oxide layer, exposing the silicon wafer itself.

Figure 4.3 Second Oxide Layer

Next, a layer of polysilicon is deposited. This layer is etched into the hinge loops, which surround the hinge pins, without contacting the hinge pins. The hinge loops also directly contact the silicon wafer through the holes etched through the oxide layers. These hinge loops are the structure that prevents the waveplates from being washed away during the final release etch.

Figure 4.4 Second Polysilicon Layer

The final release etch is then performed on the wafer. This etch removes all the oxide, causing the wave plates to have no direct connection with the wafer, thereby releasing the waveplates. The perforations in the first polysilicon layer, as discussed previously, allow this etch to occur more quickly. Also, the dimples, which were discussed previously, now come into effect, holding the waveplate off the surface of the wafer, preventing significant Van der Waals bonding. The dimples also allow the manual construction of the waveplates to occur more easily, as a probe tip can slide under the raised waveplates.

Figure 4.5 Final Release Etch

4.3 Design of Waveplates

The waveplates were designed with multiple variations, to determine which design would provide the best results using Carleton University's circuit fabrication facility. The initial design variables were plate size, hinge size, perforation size, hinge hole size, and angle of waveplate. There were also subgroups of 90° large waveplates with large and small supports, and 45° plates with box or slot side supports. This resulted in 56 different waveplate designs. Figure 4.6 - Figure 4.9 show four of the designs, representing all the different variations.

Figure 4.6 Large Waveplate, 90° with small supports, small perforations, thin hinge pin, small hinge holes

Figure 4.7 Small Waveplate, 45° slot, large perforations, thick hinge pin, large hinge holes

Figure 4.8 Large Waveplate, 90° with large supports, thick hinge pins, small perforations, large hinge holes

Figure 4.9 Large Waveplate, 45° box, large perforations, thin hinge pin, large hinge holes

4.4 Fabrication Specifics

The first task after designing the waveplates was the creation of the masks for the actual fabrication process itself. Photomasks were initially generated, and a contact print was made of the polysilicon photomask layers, in order to get a photographic inversion. Next the photomasks were used in a step and repeat camera which optically reduced the photomasks by a factor of ten. The inversion of the polysilicon mask layer was required in order to use the positive photoresist, HPR-504, which has a higher resolution than the negative photoresist.

The developing of the generated photomasks was done for 4 minutes at 68° F. The contact mask for the first polysilicon mask was exposed for 2.1 seconds and the contact print for the second polysilicon mask was exposed for 2.5 seconds. Both contact masks were developed for 4 minutes at 68° F. The difference in the times was due to reduce the slight hazing that occurred in the transparent areas adjacent (within $< 1 \mu\text{m}$) to opaque areas. The step and repeat camera's light source's voltage supply was set to 590 V for the second polysilicon mask, and at 540 V for the other three mask layers. The developing of the 590 V exposed plates was done for 3 minutes and 55 seconds at 68° F, and the 540 V exposed masks were developed for 3 minutes and 45 seconds. The difference in exposure and developing time was again used reduce the hazing effect of small transparent patterns on first polysilicon mask and both the oxide masks. The exposing and developing of the stepped down photo-masks was quite critical, as the

minimum feature size, 2.5 μm , that was being used pushed at the boundaries of the mask generation capabilities of the equipment available. On the best masks, the smallest alignment marks (1.25 μm square, used to estimate resolution capabilities of the masks) were apparent.

Once the masks were generated, the next step was the first oxide deposition. A phosphorous doped oxide was chosen to be deposited, with 5% phosphorous content by mass. The phosphorous doping was added to achieve a faster release etch, as phosphorous doped oxide etches considerably faster than undoped oxide. In certain cases, the phosphorous doped oxide was etched approximately 8 times faster than undoped oxide. The oxide was deposited instead of grown, due to thicknesses of oxide used in the process (up to 3.5 μm). Also some papers indicated that the annealing of certain undoped polysilicon layers embedded in phosphorous doped oxide would have less inherent strain. Low strain is critically important in micro-machining, as released structures with excessive strain will collapse or warp.

The phosphorous oxide deposition rate was found to be 230 $\text{\AA}/\text{min}$, with a gas flow rate consisting of 16.4% of 200 standard cm^3/min of SiH_4 , 55.0% of 200 standard cm^3/min of O_2 , and 40.4% of 200 standard cm^3/min of PH_3 . The deposition occurred at a temperature of 405°C and at a pressure of 300 mtorr. The target thickness was 2.25 μm , corresponding to a 98 minute deposition time.

Following the oxide deposition the photolithography for the dimples was done. The standard procedure for photolithography was as follows: first, a pre-bake of all wafers was done at 200°C for at least 1 hour to remove any water. Then the wafers were flooded with HMDS, spun for 3 seconds at 1000 rpm, and then spun for 30 seconds at 4000 rpm. The wafers were then baked at 105°C for 1 minute. Then the wafers were flooded with HPR 504 and then spun for 3 seconds at 1000 rpm and then spun for 30 seconds at 4000 rpm. Again the wafers were baked for 1 minute at 105°C. The wafers were then exposed to the first oxide mask in the aligner for 2.5 seconds and then developed in a 50-50 mix of de-ionized water and positive photoresist developer for 45 seconds. Finally a post bake of 5 minutes at 125°C was done on all the wafers. Some other additional details are given in appendix C.

The wafers were then etched in Siloxide etch for 1.5 minutes. The etch rate of the Siloxide etch was determined to be 9800 Å/min, for this particular oxide. This corresponded to a 4900 Å, or 0.49 µm etch depth. The wafers were then stripped of photoresist in a solution of Caro's acid, details of which can be found in Appendix C, for 10 minutes, then rinsed in de-ionized water for 10 minutes.

Next, the wafers were pre-furnace cleaned, using a very short, 3.5 second HF dip, and then placed in the furnace of polysilicon deposition. Since low, actually no, stress polysilicon was desired, the deposition temperature of the polysilicon was set at 605°C. This temperature forms small grain sized polysilicon with low or no stress [4.1, 4.2]. The silicon source used in the polysilicon deposition was silane, SiH₄. The polysilicon was

deposited for 120 minutes, with a deposition rate of $125 \text{ \AA}/\text{min}$. This resulted in a $1.5 \text{ }\mu\text{m}$ thick polysilicon layer.

The short HF dip was used to prevent the excessive removal of the oxide. If the summed thickness of the two oxide layers and the first poly silicon layer is less than the diagonal length of the hinge pin cross-section, then the plate would not be able to rotate freely, this can be seen in Figure 4.10. In addition, if the oxide is cleared from the wafer then, of course, the waveplates, made from the first polysilicon layer would be deposited directly onto the wafer, and the wave plates would be unable to move.

For rotational freedom:

$$d_1 + d_2 + d_3 > x_1$$

Figure 4.10 Hinge Pin Rotational Clearance

The next step was to pattern the polysilicon. The same photolithography steps used for the dimples was used again for this layer, with the following exceptions. The HMDS was spread on the wafers for 6 seconds at 1000 rpm and then spun for 30 seconds at 4000 rpm. The photoresist was spread for 6 seconds at 1000 rpm and it was then spun for 30 seconds at 7000 rpm. The wafers were then exposed for 4 seconds on the aligner.

The faster than normal photoresist spinning was done to reduce the thickness from about 1.2 μm to around 0.9 μm . This reduction in photoresist thickness made it more feasible to open the small perforations on the waveplates. The difficulty in opening the small perforations was due to the slight hazing that occurred in small transparent areas of the mask, which was discussed in the mask making procedure previously.

Next, the polysilicon was etched in the ECR etcher. However, the wafers were baked for 10 minutes at 140 °C to remove any water from the photoresist as well as cause extensive cross-linking within the photoresist, details of which are given in Appendix C. The ECR was set up as follows. The gas pressure was set to 1.2 mtorr, the wafer substrate temperature was set to -65°C, the microwave power was set to 400 W, the RIE power was initially set at 10 W. The gas flows were initially set at 18 standard cm^3/min for argon, 2 standard cm^3/min for SF_6 , and 0.68 standard $\text{cm}^3/\text{minute}$ for O_2 . These ECR parameters do an adequate job of uniformly etching the wafers, however this etch does leave a stringer, as shown in the SEM picture, Figure 4.11.

Figure 4.11 Polysilicon Etch Showing Stringer Effect

The stringers are more problematic in the second poly layer. This will be discussed further on, but stringers can cause problems with the first poly layer as well, by blocking hinge holes and perforations. The stringers were reduced by increasing the RIE power of the ECR etcher for the last 1/3 of the etch. The increased power was set indirectly by increasing the DC voltage in the plasma field from approximately 28 V to 50 V. However, increasing the RIE power also caused an increase in "bulls-eye" effect on the etch; this was seen as an increased etch rate near the center of the wafer compared to the edge of the wafer. In order to keep the etch uniform, the O₂ gas flow was reduced to

around 0.62 standard cm³/min during the higher powered phase of the etching process. Additionally, the O₂ levels were dropped at the very end of the etch, as the polysilicon was clearing from oxide beneath it. Dropping the O₂ gas flow to 0.15 standard cm³/min during this phase of the etch seemed to reduce the stringers as well.

Again, the photoresist was stripped using Caro's acid. The wafers were then pre-furnace cleaned, with the HF etch modified again. The HF acid was diluted to one part in 100, and the wafers were etched in this solution for 5 seconds. This reduced HF step is used to reduce the amount of oxide removed from the field. As discussed previously, if too much oxide is removed, the hinge pin would not have enough clearance to rotate freely within the hinge loop. Also, if the bare silicon wafer is exposed by an excessive HF etch, then the first poly layer will bridge to the silicon layer in subsequent depositions, making the waveplates immovable.

The second oxide layer was then deposited upon the wafers. The same furnace and gas parameters were used from the first oxide deposition, with the exception of the temperature, which was raised to 410°C. This increase in furnace temperature was done to speed up the time the furnace took to reach 405°C, since the furnaces take considerable time to stabilize their temperature to within $\pm 8^\circ\text{C}$. The deposition took 130 minutes, corresponding to a 3.0 μm film thickness.

The next step was another photolithography session, in which the HMDS and PR were both spread for 3 seconds at 1000 rpm, and then spun for 30 seconds at 4000 rpm.

The extra resolution given by spinning the photoresist faster, as done for the first polysilicon layer was not done due the excessive thickness of oxide that was to be etched, and the corresponding photoresist etch rate. The total oxide needed to be etched was 55,000 Å. If the thinner photoresist was used, the photoresist would be etched completely away before the oxide etch would have been complete. The wafers were then exposed for 6 seconds, and then developed for a minute.

Figure 4.12 Comparison of Etches for Second Oxide Etch

The next step was to etch the oxide in the hinge holes, in order to provide an anchor for the hinge loops. Due to the extreme depth of the etch, which is the sum of the first and second oxide layers, or 5.5 μm , and the need for an anisotropic etch, RIE (Reactive Ion Etching) was used for this etch. The need for anisotropy stems from the proximity of the hinge pin to the hole that is etched in the oxide. If the first poly layer, the hinge pin, is exposed during the oxide etch, which could result from anisotropic

etching, the hinge loop and the hinge pin could bond together, thus immobilizing the waveplates.

Immediately before the RIE was done, the wafers were baked again at 140 °C for 10 minutes. The reasons for this are explained in Appendix C. The RIE etcher was set up as follows. The power level was set at 350 W, which corresponds to about 0.27 W/cm². The pressure was set to 120 mtorr, CHF₃ was used as the etching agent, at a flow of 15 standard cm³/min. The etch rate for this particular oxide is 700 Å/min, which corresponded to an etch time of 78.5 minutes. However, subsequent HF etch step during pre-furnace cleans had reduced the oxide depth to be etched to 45,000 Å. This corresponded to an etch time of 64.3 minutes. However, the actual etch time was set to 75 minutes, which allowed extra time to perfectly clear the bottom of the window of oxide. This is an important consideration, since the hinge loop must be bonded securely to the silicon wafer as it must hold itself and the wave plate to the wafer. The initial photoresist etch rate was found to be around 120 Å/min for short etches, but this etch rate became smaller as etch times increased. This was thought to be due to cross-linking in the photoresist, caused by the heat of etching, which transformed the photoresist into a tougher material, thereby reducing the etch rate as the etch progressed.

Figure 4.13 is a SEM photograph of a cross section of a pair of hinge holes. As can be seen, the etch is extremely anisotropic. The "horns" seen at the top are the result of the photoresist not standing up to the lengthy etch. This was most likely due to the ease which the photoresist could flow off the raised portions of the hinge pin before it

was baked. This problem was only due to the excessive etch time, due to the large oxide thickness which was used to help ensure success during these initial fabrication runs. Later fabrication runs will have much reduced oxide thicknesses, thereby eliminating the need for long etches and therefore eliminating this problem.

Figure 4.13 SEM picture of the Anisotropic Etch of the Hinge Loops

Figure 4.14 is a SEM photograph is of the same pair of hinge holes, but with the SEM looking at the electron back-scatter, which shows the different materials much better. The completely encapsulated hinge pin in the middle can be easily seen. This

shows that the next polysilicon layer will not have a chance to bridge to the first layer, which would, of course, prevent the movement of the waveplates.

Figure 4.14 SEM Electron Back-scatter Picture of the RIE Etch

After the hinge holes were etched, the photoresist was removed using Caro's acid again, details of which can be found in Appendix C. Another pre-furnace clean was done, this time a 30 second 1:100 dilute HF etch was used. The 30 seconds was the time required to cause the scribe channels, which were also formed in this step, to become hydrophobic, as the bare silicon wafer became exposed.

The second polysilicon deposition was then done. This deposition followed the same routine as the first polysilicon layer, including the film thickness, which was again 1.5 μm .

The photolithography of the second polysilicon layer consisted of the standard 3 second spread at 1000 rpm for both HMDS and photoresist, and a 30 second spin at 4000 rpm. The exposing was done for 3 seconds, with a developing time of 30 seconds. Again, the wafers were baked immediately before the etching process for 10 minutes at 140°C.

The wafers were then etched in the ECR etcher. It was found that any stringers formed at this stage are extremely detrimental to the mobility of the waveplates. This etching step requires more experimentation in order to remove these stringers. Methods of doing this could include over-etching after the polysilicon has cleared from the oxide, increasing the RIE power at the end of the etch, and changing the gas flows (notably O_2). Addition consideration on this problem will be discussed in the section discussing future work.

The reason that the second polysilicon layer's stringers are so detrimental, is due to the places they form, and the fact that they are above the waveplates. The stringers form along the edges of the waveplates, around the hinge holes, around the perforations, and they all tend to be linked together by thin films of polysilicon. This resulted in a

"net" being thrown across all the waveplates, holding them down. These effects can be seen in the following SEM photograph, Figure 4.15.

Figure 4.15 Detrimental Polysilicon Stringers

After the second polysilicon layer was etched, the photoresist was again stripped with Caro's acid. The wafers were then cleaved into dice, since the waveplates would be damaged if they were already released while the wafer was being cleaved into dice. Finally, the dice were then placed into non-dilute HF acid for 5 minutes to remove the sacrificial oxide layers.

At this point the waveplates should have been free to move, but due to the second polysilicon layer's stringers this was not the case. A two minute plasma etch at 100 W at 0.100 torr, with CHF_3 and O_2 being the etchant was done to reduce these stringers. After this stage, it became easier to articulate the plates. However, even after this stage the stringers still existed. Additional plasma etching would have removed them completely, but the plasma etching had already thinned the hinge pins considerably at this point. Presumably, once the polysilicon etching technique is perfected, this final plasma etch step would be redundant.

The results of this fabrication run are depicted in the following SEM photographs, Figure 4.16, Figure 4.17 and Figure 4.18.

Figure 4.16 is a picture of a large 90° wave plate. The white specks seen in front of the wave plate are actually the second polysilicon layer's stringers that formed above each of the perforations. The darker circles in each corner of the main waveplate are the dimples. The X seen in front of the waveplate are actually scratch marks left from the probing tips used to lift the waveplates into position.

Figure 4.16 Constructed Large 90° Waveplate

Figure 4.17 is a picture of a large 45° wave plate with the tab and slot arrangement of support. During the construction process, one of the probing tips broke the left most hinge loop of the main waveplate. The shadows of the plates seen on the surface of the wafer are from the wave plates masking the wafer during the plasma etching step used to reduce the stringers.

Figure 4.17 Constructed Large 45° Waveplate

From the photograph in Figure 4.18, it can be easily seen that the problem of creating stress free polysilicon has been achieved, due to the lack of curvature of the waveplate. The loop of material hanging on the left side of the wave plate is a second polysilicon layer stringer.

Figure 4.18 Stress Free Polysilicon

The construction of the waveplates was done manually with a probing station and four micro-actuated probe tips. The dimples gave enough clearance that the sharpest probe tips could slide under the waveplates, allowing the construction to take place. It was found that the second polysilicon layer's stringer still held the plates down even after the plasma etch. Due to this effect, the plates had to be "nudged" with the probe tip in order to break the hold the stringer's had on the plates.

4.5 Future Fabrication Enhancements

As stated previously this fabrication run was more of a "proof of concept" run, and there are a number of changes in the process that would need to take place in order for this technique to have practical value.

Figure 4.19 Hinge Pin Looseness

A number of waveplate designs had been done, 56 of them. While it was found that wave plates with larger hinge holes were easier to actuate, it was much more difficult

to put them into position due to the huge amount of "slop" that the small hinge pin and large hinge loop allow. This can be seen in the following SEM photograph, in Figure 4.19.

Similarly, the larger hinge holes were easier to actuate, but they also allowed excessive slop which made the construction difficult. The smaller hinge holes are better at keeping the whole structure at a precise angle, which would be necessary of an optical link.

The choice between the thin or thick hinge pin depends upon thickness of the polysilicon layers. The thin hinge pins were extremely slight in this fabrication run due to the final plasma etch stage, which caused excessive sidewall etching that reduced the width of the $2.5\mu\text{m}$ hinge to around $0.5\mu\text{m}$. However, it would be preferable if this plasma etch stage could be reduced or eliminated, since this would result in a hinge pin that would be closer to a circular cross-section. A hinge pin that is more circular would allow a tighter hinge loop, which would reduce the amount of play the waveplate would experience, compared to a hinge pin with a more rectangular cross-section. The reduction in hinge pin size can be seen in the following SEM picture, in Figure 4.20.

Figure 4.20 Hinge Pin Size Reduction

The tab and slot method of supporting 45° plates was preferred to the tab and box shape. It was found that the slot arrangement provided much better angular control of the main waveplate, while not increasing the construction difficulty appreciably.

The perforations themselves could be completely eliminated, since it was found that large alignment marks, 8 times the area of the large waveplates, that had no perforations would release as well, albeit with a longer final HF etch stage. This would

allow the placement of holograms on the waveplates, with no interference from the perforations.

The choice of oxide layer thicknesses would have to be evaluated, taking in account the hinge pin size, and the loss of oxide during the pre-furnace clean HF etch stage, and etch stages that over-etch into the oxide. Obviously the amount of clearance that a hinge pin has in the hinge loop is a function of the first polysilicon layer thickness, the two oxide layer thicknesses, the width of the hinge pin, and distance between the hinge pin and the hinge loop. What makes these calculations difficult, is that the isotropy of many of the etch stages, and the loss of oxide due to the HF etch stages, change these distances as compared to what one would expect from the mask layers. Careful analysis and a more detailed characterization of the entire process would be required in order to determine an optimum oxide layer thickness.

5. FUTURE WORK

Initially, a couple of issues need to be addressed about this process, besides the points mentioned in the previous section. One of these issues is the need for manual construction of the waveplates into their locked position [5.1]. This is totally unfeasible for practical applications.

Figure 5.1 Spring Clip Concept

The first step in an automated process of assembly is to raise the main waveplates to approximately the right position. This can be accomplished by using a spring clip,

shown in Figure 5.1. The clip would snap in place once the wave plate is near the right position. The spring clip can be fashioned out of the second poly layer, so adding this feature will not introduce another mask layer.

One concern with this technique is that the middle waveplate must be locked into position before the support plates are brought up. This could be accomplished by placing photoresist above the support plates before the release etch. This would allow the main waveplate to be released first. The actual method of erecting the plates themselves is quite simple. Slight agitation of the main waveplates, once they are released will cause the waveplates to swing around, and when they swing into the correct position, the spring clip will lock the main waveplates into their correct position. Then the photoresist would be removed from above the support plates, after which, the remaining oxide surrounding the support waveplates would be removed. Then the wafer would be agitated again, causing the support plates to lock into the proper position, since they would have spring clips as well. At this point, the waveplate groups would be locked into their correct position, without any need for manual assembly.

In order for this technique to work, the play in the hinges, as mentioned previously must be reduced considerably, or else the plates could lock into position incorrectly, which would not properly hold the main waveplate at the desired angle. Obviously, the stringers would need to be eliminated as well, to allow free waveplate movement after the release etch was done.

Another issue that needs to be addressed, is the integration of the holograms into this process. Transmissive bi-amplitude holograms should prove to be easy to integrate, since the procedure to create them would be the same as for the perforations. Reflective phase holograms will require more work, most likely in the area of precisely end-pointing the etches, in order to achieve the desired phase shift. Experience in aligning multiple mask layers, which would be required for greater than bi-phase holograms has been achieved at Carleton as quaternary phase holograms have been created, albeit in silicon oxide, not polysilicon.

Finally, after the previous two issues have been dealt with, integration of optoelectronic components must be addressed. Various methods of accomplishing this have been outlined in a previous section. However, the work mentioned before was largely accomplished outside of Carleton University and similar techniques would need to be learned here.

6. CONCLUSIONS

The results of the fabrication run has proven that it is feasible to create the required micromachined structures for the optical link described herein this thesis. Various technological hurdles have been surpassed, including, but not limited to, the creation of stress free polysilicon layers, techniques for etching thick polysilicon and oxide layers, release of micromachined structures, fabrication of micro-hinges, and the actual interlocking of simple hinged plates into more complex structures. Basically, the work of this thesis has formed, and proved the concept of a number of basic building blocks that can be used to create various devices or systems, such as free space optical communication links and optical benches upon a chip.

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PM-1 3 1/2" x 4" PHOTOGRAPHIC MICROCOPY TARGET
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Appendix A Standard Fabrication Procedures

RCA Clean

An RCA clean is used to clean the wafers of impurities that may contaminate a furnace, before deposition is done.

1. Place wafers in a solution of $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ 1:1:5 by volume at $80 \pm 5^\circ\text{C}$ for 10 minutes, followed by a 10 minute de-ionized (DI) H_2O rinse. This removes residual organic contaminants
2. Place wafers in a solution of $\text{HCl}:\text{H}_2\text{O}_2$ 1:1:6 by volume at $80 \pm 5^\circ\text{C}$ for 10 minutes, followed by a 10 minute DI H_2O rinse. The step forms soluble complexes of transition metals.
3. Place wafers in a 1 to 10% HF solution for 30 seconds at room temperature, followed by a 10 minute DI H_2O rinse. This step removes thin oxide layers grown in steps 1 and 2. This step may actually increase particulate and transition metal contamination.

HPR 504 Photolithography Procedure

These are the basic steps used during photolithography using HPR 504. Note that steps 2 3 and 4 must be done right after one another for each individual wafer, as well as steps 5,6 and 7. Also, all wafers should have completed step 4 before proceeding to step 5. Steps 1 through 10 should be completed within a days time.

Photoresist is an organic chemical, wafers should NOT sit for any extended period of time with photoresist on them if any sort of reasonable or reproducible results are desired. Photoresist will change as time progresses into something infinitely more painful to deal with.

1. Bake the wafers for 2 hours at 250 °C to remove water from the silicon surface.
2. Blow the wafer with compressed N₂ to remove particulate matter.
3. Flood the wafer with hexamethyldisilazane (HMDS). Spread the HMDS by spinning it at 1000 rpm for 3 seconds, then spin the wafer for 30 seconds at 4000 rpm.
4. Bake the wafer at 105 ± 5 °C for 1 minute to dry the HMDS and remove HMDS fumes from the wafer.

5. Blow the wafer with compressed N_2 to remove particulate matter.
6. Flood the wafer with the photoresist, which in this case is HPR 504. Spread the photoresist by spinning it at 1000 rpm for 3 seconds, then spin the wafer for 30 seconds at 4000 rpm. This will give a photoresist thickness of approximately $1.2\ \mu\text{m}$. Spinning the wafers faster will reduce the thickness, and spinning slower will give greater photo resist thickness. Spinning the wafers at 7000 rpm for 30 seconds will give a photoresist thickness of approximately 850 nm.
7. Bake the wafer at $105 \pm 5\ ^\circ\text{C}$ for 1 minute to dry the photoresist.
8. Expose the wafers in the aligner. The exposure settings are determined by the mask. However, 3.5 seconds gives reasonable results.
9. Develop the wafers in a 50% solution of positive photoresist developer and DI H_2O for a time period determined by the mask. However 40 seconds gives reasonable results. Rinse wafers for 10 minutes in DI H_2O .
10. Harden the photoresist by baking the wafer for 3 minutes at $125 \pm 5\ ^\circ\text{C}$.

11. Immediately before etching bake wafer for 10 minutes at 140 ± 5 °C. This step can replace 10 if the etching is to take place immediately after the photolithography. This step will cause the photoresist to undergo cross-linking which will make it resist etching better. The step will also remove and water which the photoresist will absorb. However, these temperatures are nearing the temperature at which the photoresist will start flowing. Care must be taken at this stage.

Caro's Acid

Caro's Acid is used to strip photoresist from wafers after the processing has been accomplished. It consists of a 10 minute 100 ± 5 °C $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ 25:1:25 soak followed by a 10 minute rinse in DI H_2O . This technique will only work if there is no underlying metal layers, as this solution will etch metal as well.

END

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FIN