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A Comparative Study of Adiabatic Circuit Techniques Towards Asynchronous Adiabatic Systems

by

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partial fulfillment of the requirements for the degree of

Master of Applied Science

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Ottawa, Ontario

September, 2004

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Abstract

To keep up with the recent trend towards portable and handheld computing, designers are forced to explore some means to increase the battery life of such devices. In this scenario, low-power circuit techniques have a promising potential of research. This thesis is focused on investigating the current level of development and achievements in this area. Performance issues and low power benefits offered by some low-power circuit techniques are analyzed in detail. After a brief review of main sources of power dissipation in conventional circuits and the modern techniques used to improve the power efficiency of the circuits, two extremely low-power techniques namely charge-sharing and adiabatic logic are investigated in detail.

Review of the charge-sharing circuits revealed that at the current stage of development, overheads associated with the practical implementation of this technique are not trivial as compared to the power saving these circuits are offering. Important adiabatic circuits are evaluated in a uniform test environment and a custom IC has been designed and fabricated using a standard 0.18 μ m CMOS technology to support the results and conclusions drawn from the work with the help of chip measurements. To further explore the possibilities to reduce the power dissipation of adiabatic logic circuits, charge-recovery power clock generators have been investigated in detail. A second chip has been designed to examine full adiabatic systems including power clock generators.

Based on the results of above mentioned investigations, a new type of circuit concept that combines the potential benefits of asynchronous operation and adiabatic logic has been proposed. A third chip has been designed and fabricated as a proof of the concept. After some implementation level modifications to the initially proposed solution it is demonstrated that as compared to conventional CMOS more than 35% of power can be conserved with the proposed Asynchronous Adiabatic Logic.

Acknowledgements

After thanking almighty Allah, the compassionate and the merciful, who gifted me all the abilities to learn and explore this universe, I like to express my sincere gratitude to Dr. Maitham Shams, who guided this work and helped whenever I was in need. He has been generous with his knowledge, patience and encouragement throughout.

The work on this thesis has been an inspiring, often exciting, sometimes challenging, but always interesting experience. It has been made possible by many other people, who have supported me.

I like to acknowledge the support of the all the faculty and staff members at Department of Electronics, Carleton University. I would also like to express my sincere thanks to Dr. Leonard MacEachern for his invaluable support and advice.

I would also like to acknowledge Ontario government for OGS scholarship that provides me enough financial support to make it possible for me to concentrate on the research work.

I am indebted to all of my friends and fellow graduate students; Irfan Kadri, Atif Shamim, Moeed Israr, Muhammad Usama, to name a few, who supported me at every stage of the educational and social life in Canada.

I can not forget to be grateful for the help of my immediate family members and relatives including all of my brothers, my sisters, and especially my aunt and her family in each and every step of my life.

Last but certainly not least, I would like to show my gratitude to my parents. My father's wishes, encouragement and continued optimism about me in his life are has always provided me enough energy and motivation to face any challenge in life. Words are not sufficient to express my feelings of esteem to my mother for her continued moral and emotional support and everything she did for me. Whenever I need her she was with me. Without her, I might not be at this position where I am today. I dedicate this thesis to my mother and my father.

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List of Abbreviations and Nomenclature

<i>AAL</i>	<i>Asynchronous Adiabatic Logic</i>
<i>AAS</i>	<i>Asynchronous Adiabatic System</i>
<i>ADCPL</i>	<i>Adiabatic Differential cascode voltage switch with Complementary Pass- transistor Logic</i>
<i>ADCVSL</i>	<i>Adiabatic Differential Cascode Voltage Switch Logic</i>
<i>ADL</i>	<i>Adiabatic Dynamic Logic</i>
<i>ADMOS</i>	<i>Adiabatic MOS</i>
<i>ADSL</i>	<i>Adiabatic Differential Switch Logic</i>
<i>ANPD</i>	<i>Adiabatic NP-Domino</i>
<i>APDL</i>	<i>Adiabatic Pseudo-Domino Logic</i>
<i>BNCR</i>	<i>Bootstrapped CMOS Charge Recovery Logic</i>
<i>bRERL</i>	<i>Bootstrapped RERL</i>
<i>C or C_L</i>	<i>Load Capacitance</i>
<i>C&R</i>	<i>Control and Regeneration</i>
<i>CAMOS</i>	<i>Complementary Adiabatic MOS</i>
<i>CMOS</i>	<i>Complementary Metal Oxide Semiconductor</i>
<i>CMOSP18</i>	<i>TSMC 0.18μm CMOS Technology</i>
<i>CP-BCRL</i>	<i>Complementary Pass-transistor Bootstrapped Charge Recovery Logic</i>
<i>CPNCL</i>	<i>CMOS Pass-gate No-race Charge- recycling Logic</i>
<i>CPU</i>	<i>Central Processing Unit</i>
<i>CRDL</i>	<i>Charge Recycling Differential Logic</i>
<i>CRRDL</i>	<i>Charge Recovery-Recycling Differential Logic</i>
<i>DAPDL</i>	<i>Differential Adiabatic Pseudo-Domino Logic</i>
<i>DDR</i>	<i>Double Data Rate</i>

<i>D-HRDL</i>	<i>Dynamic -HRDL</i>
<i>DVD</i>	<i>Digital Versatile Disc</i>
<i>ECRL</i>	<i>Efficient Charge Recovery Logic</i>
<i>ER</i>	<i>Energy Recovery</i>
E_{source}	<i>Energy Delivered By Supply</i>
f	<i>Switching Frequency</i>
<i>FBMOS</i>	<i>Forward Body bias Metal Oxide Semiconductor</i>
f_c	<i>Clock Frequency</i>
<i>FCPCL</i>	<i>Race-free CMOS Pass-gate Charge-recycling Logic</i>
<i>GHz</i>	<i>giga Hertz</i>
G_{off}	<i>Equivalent Trans-Conductance Transistor</i>
<i>HRDL</i>	<i>Half Rail Differential Logic</i>
<i>HRPGDL</i>	<i>Half-Rail Pass Gate Differential Logic</i>
<i>IACMOS</i>	<i>Improved Adiabatic CMOS</i>
<i>IAPDL</i>	<i>Improved Adiabatic Pseudo-Domino Logic</i>
<i>IAPDL-4PH</i>	<i>Four Phase Improved Adiabatic Pseudo-Domino Logic</i>
<i>IC</i>	<i>Integrated Circuit</i>
<i>IECRL</i>	<i>Improved ECRL</i>
I_i	<i>Instantaneous Current</i>
I_L	<i>rms Current</i>
$I_{leakage}$	<i>Leakage Current</i>
<i>IPAL-2N</i>	<i>Improved PAL-2N</i>
<i>IPGL</i>	<i>Improved Pass-Gate Logic</i>
I_{sc}	<i>Short Circuit Current</i>
k	<i>Transistor Characteristic Transconductance</i>
<i>LSCR</i>	<i>Low-Swing Charge Recycling</i>
<i>MCRPL</i>	<i>Modular Charge-Recycling Pass transistor Logic</i>
<i>MEMS</i>	<i>Micro Electro Mechanical Systems</i>

<i>MHz</i>	<i>mega Hertz</i>
<i>MP3</i>	<i>Multimedia Audio Compressed Data Format</i>
<i>NCDL</i>	<i>No-race Charge-recycling Differential Logic</i>
<i>NEMS</i>	<i>Nano Electro Mechanical Systems</i>
<i>NERL</i>	<i>NMOS Energy Recovery Logic</i>
<i>n-FET</i>	<i>n-Type Field Effect Transistor</i>
<i>NMOS</i>	<i>n-Type Metal Oxide Semiconductor</i>
<i>nRERL</i>	<i>NMOS RERL</i>
$\emptyset$	<i>Supply Signal</i>
<i>PAL</i>	<i>Pass-transistor Adiabatic Logic</i>
<i>PAL-2N</i>	<i>Pass-transistor Adiabatic Logic -2N</i>
P_{avg}	<i>Average Power</i>
<i>PCB</i>	<i>Printed Circuit Board</i>
<i>PCGs</i>	<i>Power Clock Generators</i>
<i>PDA</i>	<i>Personal Digital Assistant</i>
<i>PFAL</i>	<i>Positive Feedback Adiabatic Logic</i>
<i>p-FET</i>	<i>p-Type Field Effect Transistor</i>
P_L	<i>Power of Individual Clock Phase</i>
<i>PMOS</i>	<i>p-Type Metal Oxide Semiconductor</i>
P_{SC}	<i>Short Circuit Power</i>
P_{static}	<i>Static Power</i>
P_{sub}	<i>Subthreshold Power</i>
<i>PVT</i>	<i>Process, Voltage and Temperature</i>
Q	<i>Electrical Charge</i>
Q_L	<i>Quality Factor of Inductor</i>
<i>QSERL</i>	<i>Quasi-static Energy Recovery Logic</i>
<i>RAM</i>	<i>Random Access Memory</i>
<i>RERL</i>	<i>Reversible Energy Recovery Logic</i>
<i>SCAL</i>	<i>Source coupled Clocked Adiabatic Logic</i>

<i>SCAL-D</i>	<i>Dynamic SCRL</i>
<i>SCRL</i>	<i>Split-level Charge-Recovery Logic</i>
<i>SOC</i>	<i>System On Chip</i>
<i>SOI</i>	<i>System On Insulator</i>
<i>SPDL</i>	<i>Split-level Pre-charge Differential Logic</i>
<i>TAPDL</i>	<i>Transmission-gate interfaced Adiabatic Pseudo-Domino Logic</i>
T_d	<i>Time Delay</i>
<i>TF</i>	<i>Test Fixture</i>
t_f	<i>Fall Time</i>
<i>TG</i>	<i>Transmission Gate</i>
t_r	<i>Rise Time</i>
V	<i>Supply Voltage</i>
V_C	<i>Capacitor Voltage</i>
V_d	<i>Diode Forward Drop</i>
V_{dd}	<i>Supply Voltage</i>
V_{GS}	<i>Gate to Source Voltage In MOS Transistors</i>
<i>VHDL</i>	<i>Very High Speed Integrated Circuits (VHSIC) Hardware Descriptive Language</i>
V_i	<i>Instantaneous Voltage</i>
V_{in}	<i>Input Voltage</i>
<i>VLSI</i>	<i>Very Large Scale Integration</i>
V_{out}	<i>Output Voltage</i>
V_T or V_t	<i>Transistor Threshold Voltage</i>
V_{th}	<i>Threshold Voltage</i>
V_{Tn}	<i>Threshold Voltage of nFET</i>
V_{Tp}	<i>Threshold Voltage of pFET</i>
α	<i>Switching Activity</i>

Chapter 1

Introduction

This chapter provides an introduction and explains the focus of this thesis and the motivation behind this work. The organization of the thesis is also explained briefly.

1.1 Introduction

In the past, high speed, small area and low cost were the major concerns of VLSI designers, whilst power considerations were only of secondary importance. In recent years, however, the growth of personal computing devices such as portable computers and real time audio and video based multimedia products and wireless communication systems such as personal digital assistants and mobile phones has required designers to make low power consumption a very high priority in many applications.

In the absence of low-power design techniques, portable and handheld products would suffer from very short battery life, while packaging and cooling them would be very difficult. These factors lead to an unavoidable increase in the cost of the product. In addition, reliability is affected by power consumption. Usually, high power dissipation

implies high temperature operation, which, in turn, may induce several failure mechanisms in the system. Finally, from the environmental viewpoint, the lower the power dissipation of a product, the less the electricity that is consumed and the lower the impact on global environment.

The design of low-power integrated circuits requires an in-depth understanding of the target technology, system architecture, and circuit techniques to achieve the target specifications and the minimum power dissipation on a wider range of operating speeds.

1.2 Focus of the thesis

The focus of this thesis is to explore the potential of the key low power techniques and try to invent a better low power solution or improve the existing solution to get the maximum possible power saving out of it, along with the other performance parameters. To achieve the objectives, circuits using adiabatic logic circuit technique and charge sharing techniques are classified, reviewed, and simulated to compare the power dissipation and usable frequency range. A test chip that has been fabricated consists of different adiabatic circuits to verify the simulated results and usability of the logic styles. The fabrication technology is 0.18 μ m CMOS (CMOSP18). To further explore the potential of adiabatic logic style, a second chip has been fabricated consisting of a full adiabatic system with charge recovery power clock generators. An Asynchronous Adiabatic Logic (AAL) has also been proposed along with the methodology to reduce the power dissipation and abolish the requirement of generating multiple clocks and eliminate the difficulty of routing them. A third IC has been fabricated to prove the idea of AAL.

1.3 Thesis motivation

Low power is the key consideration in the modern circuit design. Mobile computing devices such as laptop computers, personal digital assistants (PDAs), mobile gaming consoles, portable MP3 players, portable DVD players, photo storage and reviewing devices, and cellular phones among the others are getting increasing popularity. Not to mention battery operated implantable biomedical devices such as implantable defibrillator which improve the quality of life and reduce sufferings are becoming an integral part of our society. It is not very convenient for the patient and a high risk is involved in the process of replacing the batteries of such devices. Also the applications like deep-space probes or deep-sea monitoring and data collection systems suffer from limited battery life due to the unavailability or insufficiency of sunlight. All these issues and incidents such as the one recently reported in IEEE Spectrum magazine [1], invite the engineers and scientists to explore the potential of extremely low power systems and to invent solutions to help reducing the sufferings of the humanity in general and benefit the field of science and engineering in particular.

In the research presented in this thesis, amongst the low-power design techniques, charge-sharing and adiabatic logic circuit techniques are chosen to explore their potential as a long term power efficient circuit's solution. The limitations to reduce the power dissipation in these techniques are mainly related to the technological issues such as leakage and sub-threshold currents. Hence as technology advances, charge-sharing logic and adiabatic logic designs seems to have stronger potential to provide long lasting solution for power conscious designs.

1.4 Organization of the thesis

There are seven chapters in the thesis. These are organized as follows:

In Chapter 2, the requirement of low power circuits is explained and an overview of low-power techniques is presented. A detailed discussion on charge-sharing and adiabatic logic technique is included in this chapter.

Chapter 3 consists of prominent charge-sharing circuits and the advantages and problems associated with individual charge-sharing techniques.

Chapter 4 introduces various adiabatic logic styles. The classification and performance comparison of the adiabatic logic circuits, evaluated on a uniform test environment, is presented in detail in this chapter.

Chapter 5 presents the performance review of full adiabatic system including adiabatic power clock generators (PCGs). Classification and an extensive performance comparison of different power clock generators are detailed in this chapter.

Based on the reviews and performance comparison presented in earlier chapters, Chapter 6 introduces the concept and a novel implementation of the idea to save power, called Asynchronous Adiabatic Logic (AAL).

Chapter 7 outlines the conclusions and contributions drawn from this work. Also offered are suggestions for future research that may be carried out in this area.

Appendices contain information about test fixtures, Printed Circuit Boards (PCB), chip layouts, component schematics, pin-out diagrams, and layout diagrams.

Chapter 2

Low-Power Circuit Techniques

This chapter briefly discusses the sources of power dissipation in conventional CMOS circuits and some commonly used low power circuit techniques. To maintain focus of the thesis, only adiabatic and charge-sharing circuit technique are presented in detail. The basic operations of adiabatic and charge-sharing circuits are discussed in this chapter. This discussion helps to understand the operation of charge-sharing circuits reviewed in Chapter 3 and that of adiabatic logic circuits in Chapter 4. A discussion of complete adiabatic system with power clock generator (PCG) is presented later in Chapter 5 to avoid repetition. A survey of the literature on adiabatic logic circuits and charge-sharing circuit techniques is presented at the end of the corresponding sections of this chapter in the form of tables.

2.1 Low power ICs; needs and challenges

Reducing power dissipation of electronic equipment has become a prime concern in recent years. The current trend towards portable computing has made the battery life a major issue. As we already discussed in Chapter 1 that the growing demand of the applications such as implantable biomedical devices, deep space and deep sea probes for scientific data collection, among the others, leads to an immense requirement of extremely low power circuits. Besides the portable computing devices and applications without the access of the main power source, increasing density of integrated circuits has led IC power dissipation to approach the limit of inexpensive packaging technology. The cooling problem for a given logic technology is not one that can be solved by mere engineering cleverness in one's cooling system design, as there exist absolutely fundamental and unavoidable quantum-mechanical limits on the rate at which entropy can be exported from a system of given size by a coolant flow of given power [2]. Table 2.1 and Table 2.2 are illustrating the 2003 Semiconductor Industry Association (SIA) semiconductor technology roadmap [3] for the power dissipation of ICs. We can see that the total power consumption continues to increase, despite the use of a lower supply voltage. The increased power consumption is driven by higher chip operating frequencies, the higher interconnect overall capacitance and resistance and the increasing gate leakage of exponentially growing and scaled on-chip transistors [3].

Table 2.1 Power Supply and Power Dissipation - Near-term Years [3]

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU / ASIC Metal 1 Pitch (nm)	120	107	95	85	76	67	60
MPU / ASIC ½ Pitch (nm)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm)	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
Power Supply Voltage (V)							
V_{dd} (high-performance)	1.2	1.2	1.1	1.1	1.1	1.0	1.0
V_{dd} (Low Power, high V_{dd} Transistors)	1.0	0.9	0.9	0.9	0.8	0.8	0.8
Allowable Maximum Power							
High-performance with heatsink (W)	149	158	167	180	189	200	210
Cost-performance (W)	80	84	91	98	104	109	114
Battery (W) – (low-cost/hand-held)	2.1	2.2	2.3	2.4	2.5	2.6	2.7

Table 2.2. Power Supply and Power Dissipation - Long-term Years [3]

Year of Production	2010	2012	2013	2015	2016	2018
Technology Node	hp45		hp32		hp22	
DRAM ½ Pitch (nm)	45	35	32	25	22	18
MPU / ASIC Metal 1 Pitch (nm)	54	42	38	30	27	21
MPU / ASIC ½ Pitch (nm)	45	35	32	25	22	18
MPU Printed Gate Length (nm)	25	20	18	14	13	10
MPU Physical Gate Length (nm)	18	14	13	10	9	7
Power Supply Voltage (V)						
V_{dd} (high-performance)	1.0	0.9	0.9	0.8	0.8	0.7
V_{dd} (Low Power, high V_{dd} Transistors)	0.7	0.7	0.6	0.6	0.5	0.5
Allowable Maximum Power						
High-performance with heatsink (W)	218	240	251	270	288	300
Cost-performance (W)	120	131	138	148	158	168
Battery (W) – (low-cost/hand-held)	2.8	3.0	3.0	3.0	3.0	3.0

Figure 2.1 Thermal dissipation of the integrated circuits verses cooling cost [4].

The graph in Figure 2.1 from Intel® [4] is illustrating a rapidly increasing cooling cost of the modern ICs and microprocessors. Not only that cooling of VLSI integrated circuits is becoming very expensive, passive cooling will no more an option as the shrinking process technology is leading to higher and higher circuit densities. The graph in Figure 2.2 [5] shows the power densities in some of the microprocessor in a chronological order and a comparison with some common hot objects to facilitate to imagine the degree of hotness.

From this graph it is evident that not only power delivery will be a problem, removing the heat from the ICs will be a bigger problem. Imagine trying to cool down the microprocessor inside your computer dissipating the power per unit area comparable to the power density of a nuclear reactor! Power dissipation has become a major

microprocessor design constraint, so much so that it threatens to limit the amount of hardware that can be included on future microprocessors and how fast it can be clocked [5,6]. Designers of handheld devices are already quite familiar with the difficulties in meeting ever-increasing performance demands while maintaining reasonable battery life and small product form-factors. However, the increasing packaging, cooling, and power distribution costs, as well as reliability issues, associated with increasing power dissipation in high-end systems also threatens their future viability.

Figure 2.2 Increasing circuit power densities with the advancement in the technology on time scale [5].

Considering the need and urgency of the low power circuits, the technical challenges at the chip level are to achieve the following:

- Minimum possible power dissipation while circuit is operating in the active mode

- Extremely low power dissipation in the standby mode.
- Robustness against Process, Voltage and Temperature (PVT) variations
- Better noise immunity, and
- Acceptable speed and other performance parameters

2.2 Sources of power dissipation in conventional circuits

There are two major sources of power dissipation in conventional CMOS circuits each one being affected by different factors and influencing the system in a different way. These sources are the static power consumption, which mainly affects a system in a standby mode, and the dynamic power consumption, which dominates when the system is in an active mode.

2.2.1 Static power

Static power dissipation can be attributed to two main factors:

- a) Leakage currents due to the reverse biased p-n junctions between source or drain and the substrate. This component of power is usually quite small (for a 1 million transistor chip it would be in the order of $1mW$) but can be significant in some applications like memory chips.
- b) Sub-threshold conduction, which is an important source of power dissipation in a sleep mode. Sub-threshold currents are very small but are exponentially dependent on many parameters (*temperature*, $(V_{GS} - V_T)$) and this means that, in certain circumstances, sub-threshold conduction can be very important.

2.2.2 Dynamic power

Dynamic power dissipation can also be attributed to two causes:

- a) The load capacitance charging and discharging during circuit switching, and
- b) Short-circuit power consumption (or consumption due to direct-path currents) which occurs during switching when a direct path exists between the supply rails.

Dynamic power dissipation depends on the input and output rise and fall times, the load capacitance, the sizes of transistors, power supply voltage, and the frequency of operation.

2.3 Factors to be considered

2.3.1 Supply voltage

Dynamic power in conventional CMOS circuits is proportional to the square of the supply voltage; the earliest forms of low-power design involved the basic practice of reducing the power supply voltage, either in the entire design or in certain parts. The attractiveness of this approach was, and still is, the quadratic relationship between the supply voltage and the resulting power consumption. Hence as an elementary technique designers always try to find means of reducing supply voltage, V_{dd} . Today, this approach is no longer enough and in some cases – such as sub-threshold leakage – counter productive. Also reduction of V_{dd} leads to worse speed performance, especially when $V_{dd} \leq V_{Tp} + V_{Tn}$. Where V_{Tp} and V_{Tn} are the threshold voltages of p-FET and n-FET respectively.

2.3.2 Switched capacitance

The effective capacitance takes account of the average capacitance being switched every clock cycle. It is the product of switching activity and physical capacitance. Hence to reduce the effective capacitance, hence dynamic power dissipation, one has to find the means to reduce the physical capacitance and switching activity. However, in new process technologies, the reduction in parasitic capacitances due to the smaller geometries resulted in less dynamic power.

2.3.3 Switching activity

A node does not necessarily make transitions in every clock cycle; it depends on the nature of the circuit, the type of processing that it is carrying out and the statistics of the signals that the circuit is processing. Switching activity is the probability of a node being changed in a clock cycle.

The switching activity is a function of the nature and the statistics of the input signals. If the inputs do not change within a time period, no switching will occur and hence switching activity, $\alpha=0$, which leads to a zero dynamic power dissipation.

Circuit structure is very important in the presence of spurious transitions (glitches) which consume power unnecessarily. For example, the switching activity in dynamic CMOS logic is high because the circuit is pre-charged and discharged every clock cycle when the output is low and this occurs even when the signals driving the gate are unchanged. On the other hand, with static CMOS the switching activity depends entirely on the statistics of the input signals and, hence, can be high or low.

2.3.4 Physical capacitance

The dynamic power dissipation is directly proportional to the physical capacitance of the circuit. This physical capacitance comes from the transistor parasitic capacitance and the interconnect capacitance.

Physical capacitance can be reduced by many techniques such as using less logic, smaller transistors, fewer and shorter wires where possible and so on. Many techniques have been proposed at all design levels such as resource sharing [94], logic minimization [95], and common sub-expression extraction [96]. However, we may not reduce the capacitance arbitrarily because this can lead to undesirable results. For example, reducing transistors sizes implies less physical capacitance but reduces the current driving capability at the same time and this leads to a performance loss. Reduced performance is often unacceptable but even if it is not, it is usually more desirable to scale the supply voltage since this contributes to scaling power dissipation quadratically.

The overall conclusion is that it is not possible to optimize these factors independently and a detailed examination of the complete solution is required to ensure that the greatest power benefits are obtained [8].

2.4 Power Dissipation in Conventional CMOS

2.4.1 Static power in CMOS

Static Power consumption of normal CMOS circuits is ideally equal to zero. But there is always a leakage current present flowing through the reverse-biased diode

junction of the transistor, located between the source or drain and the substrate. Although very little, but subthreshold current also take part in the total static power dissipation. Hence, the static power dissipation can be expressed as:

$$\begin{aligned} P_{Static} &= P_{Leakage} + P_{Sub} \\ &= I_{Leakage} V_{dd} + P_{Sub} \end{aligned} \quad (2.1)$$

Where P_{Static} is total static power, $P_{Leakage}$ is leakage power, $I_{Leakage}$ is leakage current, and P_{Sub} is subthreshold power. For detailed mathematical expression for static power dissipation, please refer to [97]. The contribution of static power consumption is small in general and often can be ignored. For the device sizes under consideration, the leakage current typically ranges between $0.1nA$ and $0.5nA$ at room temperature. For a die with 1 million devices operated at a supply voltage of 5V this results in a power consumption of 0.5 mW which is still relatively low [10].

Figure 2.3. (a) An ordinary CMOS inverter. Given an input logic value A , the inverter computes its inverse A' . With more complex networks of p -FETs and n -FETs, arbitrary inverting logic functions of multiple inputs can be similarly implemented. (b) Dynamic behavior of CMOS. The n -FET conducts significantly when V_{in} is above the threshold voltage V_{Tn} , and the p -FET conducts when V_{in} is below the level $V_{dd} + V_{Tp}$, where V_{Tp} is negative.

The values of leakage currents increase with increasing junction temperature in an exponential fashion. At 85°C which is a common junction temperature limit for commercial hardware, the leakage currents increase by a factor of 60 over their room-temperature values [11].

A more important potential source of static power dissipation in CMOS is the sub-threshold current of the transistors that rises exponentially with $V_{GS}-V_T$ in the off state. The closer the threshold voltage is to zero volts, the larger the leakage current at $V_{GS}=0$ and the larger the static power consumption. To offset this effect, the threshold voltage of devices is generally kept above 0.5V in current technologies [10].

2.4.2 Dynamic power in conventional CMOS

Dynamic power consumption is the result of the circuit capacitance charging and discharging and is the dominant component of power consumption in conventional CMOS circuits. The general formula for the dynamic power consumption in a static CMOS inverter shown in Figure 2.3 is,

$$P_d = \alpha f_c C_L V_{dd}^2 \quad (2.2)$$

Where,

- C_L is the total capacitance on the gate output node.
- f_c is the clock frequency.
- α is the switching activity.

Figure 2.4. Energy dissipation in conventional CMOS. Whenever a node is switched by connecting it to a constant voltage supply V , such as across the CMOS inverter in Figure 2.3, the transfer of the charge $Q = CV$ from the constant-voltage source to the node capacitance C results in an energy dissipation of $\frac{1}{2}CV^2$, where V is the voltage swing and C is the capacitance being switched. $\frac{1}{2}CV^2$ also stored in C . Total energy extracted from supply is CV^2 .

2.4.2.1 Short-circuit power consumption

When a conventional static CMOS gate is switched, for a short time, both PMOS and NMOS networks conduct simultaneously. During this time, there is a short circuit current between V_{dd} and ground that resulting in short-circuit power dissipation.

There are many publications to date presenting different mathematical models of short circuit dissipation for conventional CMOS [9, 12]. In its most fundamental state, i.e. by definition the short-circuit power dissipation P_{SC} caused by a short-circuit current I_{SC} which flows from the supply to ground during a transition period of input signals can be mathematically represented as[12],

$$P_{SC} = \alpha f V_{dd} \int_{1 \text{ Cycle}} I_{SC} dt \quad (2.3)$$

Where α is the switching activity, f is the switching frequency and V_{dd} is the supply voltage.

The short-circuit power dissipation increases as we decrease the threshold voltage of transistors for maintaining high speed operation under the reduction on supply voltage. Hence, the estimation of the short-circuit power dissipation is important for accurate estimation of total power dissipation to design high performance VLSI [13]. The short-circuit current I_{SC} is affected by many other factors such as the transition time of the input signal, the output load, and the sizes of transistors that make up the logic gate among the other [14].

In [15] simulation of a CMOS inverter circuit shows a linear relationship between the short-circuit dissipation and the input rise and fall time. It is also shown that, if the output signal and input signal have equal rise and fall times, the short circuit dissipation will be less than 20% of the total dissipation. If the inverter is more lightly loaded, causing output rise and fall times to be short compared to the input rise and fall times, then the short-circuit dissipation will increase to the same order of magnitude as the dynamic dissipation. Therefore to minimize dissipation, an inverter should be designed in such a way that the input rise and fall times are less than or about equal to the output rise and fall times in order to guarantee a relatively small short-circuit dissipation. For well-designed circuits, the short circuit power consumption can be less than 10% [10] of the total power. It can be larger in some circumstances, for example, for slow input signals.

In [16] the effects of increasing the output loading and the effects of deteriorating input signal slope are examined. Effects on different sources of power dissipation are illustrated as follows,

Effects of increasing the load capacitance of a CMOS gate:

- short circuit power consumption decreases
- dynamic power consumption increases
- the sum of these two components increases

Effects of increasing the rise time of the input signal of a CMOS gate:

- short circuit power consumption increases
- dynamic power consumption remains unchanged
- the sum of these two components increases

2.5 Low-power techniques

When CMOS technology was introduced it was believed that the power consumption problem was solved. Since then, because of increasing circuit complexity and speed, without low power techniques, the current CMOS technology is approaching the situation when the density of the circuit will be limited by the power consumption. To solve this problem scientists and researchers came up with different process and circuit based solutions such as,

- ***Process shrinking*** – With every new process generation, the entire lateral, and some of the vertical dimensions are scaled down. This has an immediate impact on

- reducing power dissipation, as well as increasing circuit speed. The primary effect of process scaling is to reduce all the capacitances, which provides a proportional decrease in power and circuit delays. Device sizes can be reduced to keep delay constant over process scaling, which will yield an even larger reduction in power dissipation reduction.
- ***Voltage scaling*** – Scaling of the power supply voltage to a lower value is also an effective way of reducing power, up to a certain point. There are many limiting factors that restrict the voltage scaling to go further down such as speed, noise figure and leakage current among the others.
 - ***Clock management*** – Clock signal distribution in processors can take up about 30% of total power expended in a processor. This makes it a tempting target for power saving. We can turn off the clock in parts of the processor where and when it is not being used by clock gating. This not only saves clock power but also the logic which is switched. Instead of clocking on, say only, the rising edge of the clock pulse we can halve the frequency and trigger on rising and falling edges, like in Double Data Rate (DDR) memory. Even more effectively we can use a technique called "half swing clocks" to reduce the voltage swing of the clock signal. Finally, we can slow down the clock when we don't need all the capability of the processor. Or we can do away with a clock, at least in part, by using asynchronous computing in portions of the device where we can organize logic without using a clock [18].
 - ***Shut off or slow down processor when not being heavily used*** - We can suspend, or "put to sleep" a processor when it isn't being used. This essentially means if the CPU

is not doing useful work save the program state in RAM, or more deeply to disk and shut the CPU down. Generally speaking the more power we save the longer the latency to return to full performance. Note that the operating system support is needed for many of these schemes. Previous versions of Intel and AMD mobile chips can reduce the clock frequency by 100 Hz when not utilized where as Transmeta LongRun along with the new mobile processor chips from Intel and AMD reduces the clock frequency and supply voltage on the fly depending on the load [18].

- **Reducing switching activity** – This is a design optimization approach to reduce the power dissipation by minimizing the switching activity while implementing logical blocks to perform the same logical operation. Reducing switching activity is an active area of research [98].
- **Downsizing all non-critical paths** – is another effective way to minimize the power. Using minimum size transistors in non critical paths reduces the parasitic capacitance of the transistors hence avoids unnecessary power dissipation.
- **Parallelism** – is a commonly used low power circuit technique. Using parallelism we achieve low power in trade off with the circuit area [99].
- **Charge-sharing** – is a relatively new and under-development circuit technique. Charge-sharing logic circuits are capable to conserves about half of the energy which otherwise be wasted to the ground like in conventional circuits.
- **Adiabatic logic** - is another relatively new idea in term of circuit implementation to achieve low power. In adiabatic circuits power has been saved by slow switching of

the transistor during the logical transitions. In a full adiabatic system which includes charge recovery power clock generator, a part of the supplied energy can be recycled back to the power supply to further exploit the power saving potential of the adiabatic logic.

The logic style of digital circuits influences the speed, size, the power dissipation and the wiring complexity. In this thesis our focus is on the logic styles to reduce the power. In the following sections we will discuss the Charge-sharing and Adiabatic logic technique in detail.

2.5.1 Charge-sharing technique

2.5.1.1 Basic operation

Charge-sharing is a power reduction technique which re-uses the charge stored in the evaluation phase for pre-charging phase. The nodes are partially charged in the pre-charge phase and, so, require less power to charge the pull-up node to V_{dd} during evaluation. The concept of charge-sharing is illustrated in Figure 2.5. In the evaluation phase, as shown in Figure 2.5(a), one output node is charged fully, whereas, the opposite node is completely discharged. In the pre-charge phase instead of disposing all the charge of the fully charged node to ground, the two output nodes are connected together through a switch, as shown in Figure 2.5(b). It allows the fully charged node to share the charge with the other node. In the next evaluation phase then the pull-up node has to be charged only half way up, whereas the charge on the pull down node will be drained to ground. Hence, under ideal conditions, charge sharing can reduce power consumption up to 50% as compared to conventional dynamic logic.

Mathematically we are saving energy during the charging of a capacitance C to V_{dd} level, when the charge Q is transferred, using two voltage steps instead of one (Figure 2.6). When charging C to V_{dd} level in one voltage step, the energy delivered by the voltage source E_{source} is

$$E_{source} = Q \cdot V_{dd} \quad (2.4)$$

Figure 2.5 . Concept of charge-sharing technique:

(a) evaluation phase; and (b) pre-charge phase

Figure 2.6 Charging of Capacitor C to V_{dd} level in one or two voltage steps.

During charging C to V_{dd} level in two voltage steps, without using charge-sharing the energy delivered by the voltage source is reduced to,

$$E_{Source1,2} = \frac{1}{2}Q\frac{1}{2}V_{dd} + \frac{1}{2}QV_{dd} = \frac{3}{4}QV_{dd} \quad (2.5)$$

Further power reduction is achieved by the combination of two step charging and charge sharing. The first part of the energy in Equation (2.5) is gained through the charge sharing. Only the charging from $V_{dd}/2$ to V_{dd} is done by the voltage source. Two steps charging combined with charge sharing, yields to a 50% reduction of the energy delivered by the voltage source compared to one step charging in conventional CMOS.

$$E_{Source1,2} = \frac{1}{2}QV_{dd} = \frac{1}{2}CV_{dd} \quad (2.6)$$

2.5.1.2 Publication list of charge-sharing circuits

Table 2.3. Chronological list of publications on charge-sharing circuits

<i>Year</i>	<i>Reference</i>	<i>Logic Style</i>	<i>Comments</i>
1996	[19]	CRDL	First Charge-Sharing Logic
1997	[20]	HRDL	Improved PED performance, no extra supply needed for biasing
1997	[21]	D-HRDL	Resolved PED problem using 4 clock phases
1999	[22]	CPNCL	More efficient solution of PED, uses only 2 clock phases
1999	[23]	NCDL	A variant of CPNCL
2000	[24]	MCRPL	A variant of HRDL using modular approach
2001	[25]	SPDL	Functionally better but with many overheads such as device count.
2001	[26]	HRPGDL	Another variant of HRDL using 3 clock phases.
2001	[27]	LSCR	-
2001	[28]	CRRDL	An attempt to combine charge-sharing and adiabatic logic techniques.
2002	[29]	ADSL	-
2003	[30]	FCPCL	Overall better performance but low drivability due to pass transistor logic.

2.5.2 *Adiabatic technique*

2.5.2.1 *Adiabatic switching*

Adiabatic circuit technique is a different means to reduce dynamic power dissipation. The main idea is to conserve the energy that would otherwise be dissipated as heat. As described in Section 2.5.1 for conventional CMOS all the energy drawn from the supply voltage is used only once before being discarded. Adiabatic circuits while implemented with charge-recovery power clock generators allow the recycling of energy to reduce the total energy drawn from the power supply. Logic circuits have to be reorganized to make this approach practical.

The term adiabatic is usually used to describe a thermodynamic process that exchanges no heat with the environment. Here, the process is the transfer of electric charge between nodes in a circuit, and any energy dissipated as a result of this transfer is spread into the environment as heat. As is the typical use of the term in thermodynamics, fully adiabatic and, thus, completely dissipation-less operation is an ideal condition that may be approached as the logic switching is slowed down. A power dissipation improvement with increased switching time is, therefore, the defining property of adiabatic switching. In many cases, the dissipation for a certain charge transfer is composed of an adiabatic component and a non-adiabatic one, only the former will decrease when the process is slowed down. Such a partially adiabatic system will not operate completely without dissipation, regardless of how slowly it is operated [8].

$$P_{\text{Adiabatic System}} = P_{\text{Adiabatic Losses}} + P_{\text{Non-Adiabatic Losses}} \quad (2.7)$$

2.5.2.2 Basic operation and mathematical analysis of adiabatic circuits

The core insight behind all adiabatic circuits is that the CV^2 minimum dissipation in conventional CMOS circuits is due primarily to the fact that such circuits charge a node by connecting it to a constant voltage supply. Two possible solutions to avoid this situation are,

Constant current source — one alternative means that one might think of for charging up a capacitive load is to instead use a constant current power supply, operating at some appropriate current over some desired length of time. Refer to Figure 2.7. Let C be the load capacitance, V the voltage swing, R the resistance in the charging pathway, and t the charging time of the node. Then the charge delivered is $Q=CV$, the current should be $I=Q/t$, and the energy dissipated in the circuit is,

$$\begin{aligned} E_{diss} &= \int p dt = \int i^2 R dt = I^2 R t = \left(\frac{Q}{t} \right)^2 R t \\ &= \frac{Q^2}{t} R = \frac{(CV)^2}{t} R = CV^2 \frac{RC}{t} \end{aligned} \quad (2.8)$$

Figure 2.7. Charging a node to voltage V via a constant current over a time t . Compare with conventional CMOS. In this case, the dissipation is not $\frac{1}{2} CV^2$, but rather $CV^2 RC/t$, which becomes arbitrarily small as the charging time t is increased.

Figure 2.8. Compare with Figure 2.7. Instead of an ideal current source, we have power supply that provides a voltage signal ϕ that ramps up from 0 to V over a time t . Instead of an ideal resistor, we have turned-on CMOS transistor, with gate voltage biased at some value $V_G > V + V_T$ that allows the transistor to conduct well over the entire voltage range from 0 to V , with an approximate effective resistance of R . For $t \gg RC$, $E_{diss} \approx CV^2 RC/t$; for $t \ll RC$, $E_{diss} \approx CV^2$.

Note that this dissipation scales down proportionally as the charging time increases.

Voltage ramps —when charging nodes in CMOS logic circuit this constant current produced can be closely approximated by using a turned-on transistor in place of the resistor, and using a power supply with a linear voltage ramp in place of the constant current source. (See Figure 2.8) An exact analysis of the energy dissipation in this circuit is more complex, but it can be shown to approach that of the constant current circuit very closely when $t \gg RC$. At the opposite extreme, when $t \ll RC$, the dissipation approaches that of an ordinary constant-supply-voltage switching circuit. For the slope of the voltage ramp please see Figure 2.9 and [31] for more detailed discussion.

Figure 2.9. Voltage curves for slow and fast adiabatic charging using a voltage ramp. If the supply signal ϕ ramps up much faster than the characteristic RC time of the circuit, then the load voltage V_L will lag behind the ramp and approach the supply level in a characteristic exponential-decay curve. When ϕ reaches its peak, the voltage difference across the transistor is still almost the full swing V , leading to the dissipation being almost $\frac{1}{2} CV^2$. On the other hand, if ϕ ramps up very slowly, V_L will track it, with only a small lag V_{DS} that is determined by the rise time, the transistor's characteristic trans-conductance k , and the drive voltage $V_{dr} = V_G - V_T$.

The same basic technique can also be used to discharge a logic node, with the supply voltage ramping the other way, from the logic level V back down to 0. Note however that these low-dissipation characteristics are only maintained as long as we charge and discharge all nodes only using this technique. If, on the other hand we ever turn on a transistor when there is a voltage difference across it, there will be $\frac{1}{2} CV^2$ dissipation, as in any switching circuit. So in a fully adiabatic logic circuit, we need the rule that a transistor can only be turned on if there is no voltage difference across it.

One might object that in this technique we are merely moving the dissipation from inside the circuit to the power supply which must generate this swinging logic signal. But, as we will see later in Chapter 5, there are a number of ways to generate the

necessary signal using a resonant element, in which circuit energy oscillates back and forth between the on-chip capacitance and off-chip inductance. If the resonant frequency is low and the off-chip elements have a high quality index, the off-chip elements need not dissipate significant energy either [9].

The above discussion outlines the basic principles of adiabatic circuits, but does not get into the details of how to build such circuits using those principles. There are now a number of different adiabatic logic techniques available for doing this. In Chapter 4 we will review and evaluate the performance parameters of some prominent adiabatic logic styles.

2.5.3 Optimal rising and falling time for the adiabatic clocks

Consider Equation (2.8) representing power dissipation in adiabatic charging. It can be concluded that reducing operation speed, i.e. by increasing t , the power consumption could be decreased extreme down to zero. However, if static losses are considered, too, a limit for the achievable minimum power consumption occurs, stating an optimum charging time with minimal power consumption, which is not infinity, in opposition to what Equation (2.8) is suggesting. Figure 2.10 is illustrating the total power dissipation of adiabatic circuits as a function of both static and dynamic power helps to explain it further.

Figure 2.10. Total energy dissipation vs. ramp rise time

To find the optimal value of charging and discharging time for minimum power dissipation, a linear network model giving the reason for such losses together with a closed formula for the prediction of the power consumption of such a circuit is introduced in [32]. From this formula the optimum charging time and minimal power consumption can be derived, in closed form, too. Further it is presented in [32] that for such circuits with static losses the well-known linear charging ramps do not represent the optimal waveform for charging with low losses. The optimal waveforms can be derived using variational calculus. By comparing the predicted energy losses to simulation results gained by using the models of a standard CMOS process, it is shown that the linear model holds in the interested range of charging time, giving a rather precise description. The formula derived in [32] for the minimum power dissipation using optimal waveform is given as,

$$E_{\min} = \sqrt{\frac{25}{18}} V_{dd}^2 C \sqrt{R(RG_{off}^2 + G_{off})} \quad (2.9)$$

Where, V_{dd} is supply voltage, C is the node capacitance, R is the equivalent resistance of the charging transistors and G_{off} is the equivalent trans-conductance of the logic transistors. Figure 2.11 shows the reference circuit, its equivalent model and the shape of optimal waveform for this circuit. Further details on optimal waveforms for minimum power dissipation can be found in [32].

Figure 2.11. (a) Charging of capacitor with static transistor dissipation, (b) Linear model of charging with static dissipation, (c) Proposed optimal waveform.

2.5.4 CMOS-Adiabatic-CMOS interface

Different adiabatic logic families have been proposed, requiring different clocking schemes. For these circuits to be used with existing CMOS circuits, an interface circuit is required to match the logic levels on two sides. This will enable the designer to utilize the strengths of both conventional CMOS and adiabatic circuits together on a single chip. For this purpose, an interface circuit has been proposed in [33], designed to cater for a group of adiabatic logic families [40, 41, 46]. It can be used to convert the signals from CMOS to APDL logic family, and vice versa. The circuit is shown in Figure 2.12.

Figure 2.12. Schematic diagram for the interface circuit to convert signals between CMOS and adiabatic circuits [33].

The synchronization clocks, ϕ and $\bar{\phi}$, are similar to the square pulses used in the clock supply generator [34]. These pulses are synchronized with the clock supply signals used in the proposed adiabatic circuits [40, 41, 46]. With this interface circuit, dual rail outputs can be derived using a single rail input signal. For more details of the adiabatic-CMOS and CMOS-adiabatic logic interface circuit, please refer to [33].

2.5.4.1 Publication list of adiabatic logic circuits

Table 2.4. Chronological list of some publications on adiabatic logic circuits

<i>Year</i>	<i>Reference</i>	<i>Logic Style</i>	<i>Diode or Transistor Based</i>	<i>Number of clocks</i>
1994	[35]	SCRL	Transistor	20
1994	[36]	2N2P-2N	Transistor	8
1994	[37]	2N-2N2D	Diode	2
1995	[38]	ADL	Diode	4
1995	[39]	2N2P / 2N-2N2P	Transistor	4
1995	[40]	APDL	Diode	2
1996	[41]	TAPDL	Diode	2
1996	[42]	CAMOS/ADMOS	Transistor	2/4
1996	[43]	PFAL	Transistor	4
1996	[44]	ER Circuits	Diode	4
1996	[45]	ECRL	Transistor	4
1997	[46]	IAPDL	Diode	2
1997	[47]	QSERL	Diode	2
1997	[48]	FBMOS	Transistor	_*
1997	[49]	PAL	Transistor	4
1998	[50]	IAPDL-4 ϕ	Diode	4
1998	[51]	IECRL	Transistor	4
1998	[52]	PAL-2N	Transistor	4
1998	[53]	BNCRL	Transistor	4
1998	[54]	RERL	Transistor	16
1999	[55]	IPAL-2N	Transistor	1
1999	[56]	bRERL	Transistor	16

<i>Year</i>	<i>Reference</i>	<i>Logic Style</i>	<i>Diode or Transistor Based</i>	<i>Number of clocks</i>
1999	[57]	ADCPL	Transistor	2
1999	[58]	NERL	Transistor	4
2000	[59]	nRERL	Transistor	16
2000	[60]	ADCVSL	Transistor	_*
2001	[61]	IPAL / IPGL	Transistor	4
2001	[62]	DAPDL	Diode	2
2001	[63]	QSERL	Diode	2
2001	[64]	ANPD	Transistor	_*
2001	[65]	SCAL	Transistor	1
2001	[66]	SCAL-D	Transistor	1
2001	[67]	CP-BCRL	Transistor	_*
2001	[68]	ECRL (2)	Transistor	4
2002	[69]	PFAL	Transistor	4
2002	[70]	IACMOS	Transistor	_*
* No information about clocking scheme is available in the corresponding publications				

2.6 Summary

In this chapter the need and challenges of low power circuits has been described. A brief discussion of the sources of power dissipation in conventional CMOS is presented. A comprehensive list of low power circuit techniques is discussed very briefly following an extended discussion of charge-sharing and adiabatic logic techniques. A list of charge-sharing and adiabatic circuits published in recent years has also been presented in the form of tables with comments on the most prominent feature of the publication.

Chapter 3

Review of Charge-Sharing Logic Circuits

Energy efficient circuit design is one of the crucial requirements for future consumer devices. Recently, several techniques are published utilizing charge-sharing for low power circuits. In this chapter we review the performance of foremost charge-sharing logic styles. Advantages, problems and overheads associated with each technique are discussed and compared with other circuit techniques.

3.1 Introduction

Reducing power dissipation of electronic equipment has become a prime concern in recent years. Lately several charge-sharing logic techniques have been proposed to realize low power computation with high noise margin. Charge-sharing is a power reduction technique which re-uses the charge stored in the evaluation phase for pre-charging phase. The basic concept of charge-sharing circuits is as illustrated in Section 2.6.1. In this chapter some practical charge-sharing circuits proposed in recent years are presented and the strengths and weaknesses of each logic style have been

reviewed one by one. Table given at the end of the chapter is summarizing the key performance and circuit parameters of each charge-sharing circuit.

3.2 Performance review

In recent years, several circuits have been proposed using charge-sharing technique, such as Charge Recycling Differential Logic (CRDL)[19], Half Rail Differential Logic (HRDL) [20], Dynamic Half Rail Differential Logic (D-HRDL) [21], Half Rail Pass-Gate Differential Logic (HRPGDL) [26], CMOS Pass-Gate No-race Charge Recycling Logic (CPNCL) [22], Split-Level Pre-charge Differential Logic (SPDL) [25], CMOS Charge Recovery and Recycling Differential Logic (CRRDL) [28], and Race-Free CMOS Pass-Gate Charge Recycling Logic (FCPCL) [30]. In this section the characteristics and problems associated with these circuits are presented in a chronological order.

Charge Recycling Differential Logic (CRDL): Charge Recycling Differential Logic (CRDL) [19], as shown in Figure 3.1(a) is the initial circuit that introduced the charge-sharing technique. CRDL offers the same dynamic performance as DCSL [71] with improved power performance. For cascaded operation, CRDL requires two phase clocking scheme with additional latches to be inserted between all stages. CRDL offers race free operation regardless of any overlap between clock phases. Also, half-swing transition draws less current, reducing the supply rail bounce due to the inductive effects (di/dt). However, a major problem associated with CRDL is the pre-evaluation discharge as explained in Figure 3.2. Another concern in adopting CRDL as a low power technique is the high biasing voltage needed to raise the threshold voltage of PMOS transistors to

more than $V_d/2$. In CMOS 0.18 μm process (TSMC CMOSP18) with $V_{dd} = 1.8\text{V}$, 3 volt supply is needed to raise the PMOS threshold voltage to that level.

Figure 3.1 NAND gate implementation in (a) CRDL and (b) HRDL logic

Half Rail Differential Logic (HRDL): To solve the problem of pre-evaluation discharge in CRDL, Half Rail Differential Logic (HRDL) [20] is proposed, as shown in Figure 3.1(b). HRDL also improves over CRDL technique by dispensing with the need to provide a separate high-voltage supply to bias the n-wells. The problem of pre-evaluation discharge is attempted to be solved by introducing the control circuitry between each stage consisting of transistors M9 to M14, as shown in Figure 3.1(b). However, HRDL still faces the potential problem of pre-evaluation discharge since it utilizes a common driving signal to turn on the pull-down evaluation tree. However pre-evaluation discharge does not occur if the evaluation chain is sufficiently short and the input signals arrive prior to the pull down signal. For long evaluation chains, the driving signal needs to be delayed with respect to the data signals to avoid this hazard.

Pre-Evaluation Discharge:

In a chain of logic gates where evaluation takes place on a clock transition, the pre-charged output nodes of the following gates connected in series may be discharged, if the clock signal arrives ahead of the evaluation signals. This occurs when the logic input signals are held at their pre-charge level of $V_{dd}/2$ and the early arrival of the clock turns on the conducting transistor to ground. As a result, the recycled charge held at the output nodes is lost.

This timing diagram explains the charge evaluation problem in 2-input NAND gates implemented in logic styles such as CRDL [19] and HRDL [20]. According to the degree of signal skews and implemented functions, these circuits may experience either pre-discharging (i.e. situation 1) or wrong evaluation (i.e. situation 2). The pre-evaluation problem becomes worse as input signal skew or fan-in increases. The pre-evaluation phenomenon results in increased power consumption and delay which, in turn, may cause fatal malfunctions [22].

Figure 3.2. Description of Pre-Evaluation Discharge

Dynamic Half Rail Differential Logic (D-HRDL): A modified version of HRDL is proposed by the same authors called Dynamic Half Rail Differential Logic (D-HRDL) [21], as shown in Figure 3.3(a). D-HRDL cascade logic circuits runs on four phase clocks. D-HRDL eliminates the pre-evaluation discharge, as each cascaded stage relies on a different phase of clock for evaluation. This means that the logic between stages is pipelined and don't require any additional latches as in the case of CRDL. Also, unlike CRDL, all n-wells in D-HRDL are conventionally biased to V_{dd} . D-HRDL runs faster than CRDL. The additional speed is obtained at the expense of two additional clock phases.

Figure 3.3. Charge-sharing logic (a) D-HRDL and (b) HRPDDL

Half Rail Pass-Gate Differential Logic (HRPGDL): Another variant of HRDL is Half Rail Pass-Gate Differential Logic (HRPGDL) [26], HRPDDL uses the cross coupled inverters similar to HRDL for charge-sharing, but employs multi-phases to control the data flow and uses pass-gate logic instead of NMOS logic to reduce transistor count and speed up its operation. HRPDDL uses three clock phases as compared to four phase operation of HRDL. However, the complement of each clock phase is also required.

Figure 3.4. NAND gates designed in different charge-sharing logic styles

CMOS Pass-Gate No-race Charge Recycling Logic (CPNCL): As compared to Dynamic-HRDL and HRPDDL, CMOS Pass-Gate No-race Charge Recycling Logic (CPNCL) [22] - illustrated in Figure 3.4(a) - provides a more efficient solution to the problem of pre-evaluation discharge by utilizing only two clock phases. CPNCL becomes more effective for low power implementation of high fan-in functions under real chip environment with input signal skews. Thus, CPNCL makes it possible to implement random logic without extra design overhead. However, CPNCL requires supply voltage higher than $3V_{th}$ (threshold voltage) and it suffers from lower drivability due to using NMOS pass-transistor evaluation tree. Also, for a 2-input NAND gate, when both inputs are high, short-circuit paths exist in the CPNCL structure leading to high power consumption.

Split-Level Pre-charge Differential Logic (SPDL): Unlike the previous structures, Split-Level Pre-charge Differential Logic (SPDL) [25], shown in Figure 3.4(b), separates the NMOS complementary logic tree from the output load. Thus, it can decrease the propagation delay. Moreover, it can increase reliability because the asymmetry of the tree does not significantly affect the offset voltage of the output driver. The second advantage is that the pull-up and pull-down transistors in the output driving paths are not turned on at the same time during the evaluation phase. This raises the energy efficiency by eliminating short-circuit current. It also decreases the probability of the wrong or meta-stable state. The third advantage lies in the driving capability of the pull-up and pull-down transistors. In case of the CRDL and HRDL, gate nodes of these output driving transistors are pre-charge to half V_{dd} for the charge sharing. In the SPDL, the gate-to-source voltages of the output driving transistors can be maximized to V_{dd} or

ground level by pre-charge circuitry, enhancing the driving capability. Only the output nodes of the output driver are pre-charge to half V_{dd} for charge sharing.

CMOS Charge Recovery and Recycling Differential Logic (CRRDL): The introduction of CMOS Charge Recovery and Recycling Differential Logic (CRRDL) [28] is an attempt to get advantage of both charge-sharing and adiabatic logic technique to achieve optimum low power performance. Besides the theoretically attractive idea, operational needs of CRRDL don't full-fill the requirements of both adiabatic logic and dynamic logic technique. Increased structural complexity limits the maximum operational frequency of the circuit. Requirement of large slope clock and control signals causes the energy to dissipate non-adiabatically.

Race-Free CMOS Pass-Gate Charge Recycling Logic (FCPCL): Race-Free CMOS Pass-Gate Charge Recycling Logic (FCPCL) [30], as illustrated in Figure 3.4(c), is the most recent charge sharing technique. It demonstrates better power-delay product compared to its precedes. FCPCL eliminates the overhead of the control logic associated with most charge-sharing circuits. It not only reduces the structural complexity, but also enhances the performance of the circuit. FCPCL use pass-transistor logic style along with a regenerator without a controller. The use of regenerator makes the circuit insensitive to signal skew.

3.3 Conclusion

This review of the circuits using charge-sharing technique to achieve low-power dissipation shows that in comparison to conventional CMOS dynamic logic, significant amount of power can be saved without compromising the other performance parameters

such as speed and tolerance to the signal skews. However, the circuit complexity and, in some circuits, the requirement of extra clock phases to eliminate the pre-evaluation discharge and to increase the efficiency, are the obvious overheads of charge-sharing logic circuits. Table 3.1 shows a comparison of different charge-sharing NAND gates based on the data presented in the indicated publications.

Table 3.1. Comparison of Charge-Sharing NAND Gates

<i>Logic Style</i>	<i>Year</i>	<i>Device Count*</i>	<i>P_{avg}</i> (μW)	<i>T_d</i> (ns)	<i>P_{avg} x T_d</i> (fJ)	<i>Reference(s)</i>
DCSL [#]	1984	13	173	0.49	85	[28], [30]
CRDL	1996	18	143	0.42	60	[28], [30]
HRDL	1997	18	134	0.59	79	[28], [30]
D-HRDL	1997	14	137	0.48	65	[21]±
CPNCL	1999	13	96	0.69	66	[22], [30]
HRPGDL	2001	12	36.8	0.95	35	[26] ±
CRRDL	2001	19	17.8	1.51	27	[28]
SPDL	2001	20	109.9	0.49	54	[25] ±
FCPCL	2003	13	43.5	0.34	14.7	[30]
[#] For comparison only, not a charge-sharing circuit						
* Device count includes the controller circuit						
± Calculated and scaled from the graphs for comparison						

In some cases, adequate technical information was not found in the literature to operate the circuits within the standard simulation environment. Due to this reason simulation based performance comparison is not provided here.

3.4 Summary

In this chapter review of different charge-sharing circuits has presented. Various techniques are discussed and their advantages and problems are explained. Investigation revealed that the area of charge-sharing circuits is still under development. One would like to see more practical measures, characterization, and applications of these circuits. The amount of power saving charge-sharing circuits are offering is not enough for the modern low-power applications as compared to the overheads of the technique, such as area and multiple clock phase operation. Not only the generation, distribution of multiple clock phases in modern highly integrated circuits are big design overheads.

Chapter 4

Comparative Analysis of Adiabatic Logic Styles

Over the past decade, different adiabatic logic styles for low-power applications have been published. In this chapter we compare and analyze the performance and energy dissipation of various adiabatic logic circuits in a uniform test environment. The test benches are laid out in CMOSP18 0.18 μ m CMOS technology and a test chip has been fabricated to compare the power savings and other performance parameters of different adiabatic logic styles. The presented results are mainly based on physical measurements and post layout simulations.

4.1 Introduction

In applied physics, an adiabatic process is defined as any process that is asymptotically isentropic (thermodynamically reversible), that is, whose total entropy generated tends towards zero in some appropriate limit, typically, of low speed and improved isolation of the system. As the most famous example, asymptotically reversible

heat engines were first described by Carnot in 1825 [72], and were shown by him to provide the maximum possible thermodynamic efficiency. Part of the cycle of Carnot's engines involved processes with no heat flow, and this lack was the original and literal meaning of the term "adiabatic." But today, we would call the entire Carnot cycle adiabatic, in the more general applied-physics sense of the term, which has departed from the literal meaning. Of course, no real physical process can be arranged to be absolutely perfectly isentropic (with entropy generated being exactly zero) since there will always be some nonzero base rate of unwanted dissipative interactions with the environment (e.g., quantum tunneling, cosmic rays, asteroid impact). However, in practice, if the goal is to minimize the energy dissipation of some process, much can be done to bring the expected dissipation of the process as close to zero as is possible, within the constraints of the available technology. The field of adiabatic circuits applies the general concepts of adiabatics to the design of low-power electronic circuits in particular, consisting primarily today of digital MOSFET-based switching circuits [2].

Development of adiabatic logic, as an approach to reduce the energy consumption of digital circuits, has become a major focus of research [2, 29, 92]. The advances in compact, practical adiabatic computing circuits, which demonstrate significant energy savings, promise new horizons in using such techniques for low-power systems. Although the concept and history of adiabatic logic is more than 50 years old, the most significant development transpired during the last decade [2]. The explicit use of the term adiabatic in connection with the design of nearly reversible low-power switching circuits was first made by Koller and Athas of ISI, at the 1992 Workshop on Physics and Computation in Dallas [73]; this event can be considered the formal birth of adiabatic

circuits, as a well-defined discipline named by these two words. However, the same general circuit design concepts were also studied in the late 1970's and early 1980's by Edward Fredkin and Tomasso Toffoli at MIT [74], and by Carver Mead [75], Richard Feynman [76], and Charles Seitz and colleagues at Caltech [77]. Even earlier was work on similar techniques by Boyd Watkins of Philco-Ford (a then-subsiary of Ford Motor) published in JSSC in 1967 [78], though Watkins did not explicitly mention the connection between his specific circuits, and the more general phenomenon of reversible, adiabatic processes.

Figure 4.1. Basic blocks of adiabatic logic systems

In this chapter a comparative study of the adiabatic logic styles found in the literature has been presented. We classify different adiabatic logic styles based on their power-saving technique. Adiabatic systems, in their complete form, consist of two major components, the logical block and the charge-recovery block, as shown in Figure 4.1. The charge-recovery block is part of the power supply or clock generator circuit. Analysis of the simulated and measured results for the most significant adiabatic logic

styles has been reported in this chapter. Note that these adiabatic styles cannot be directly compared based on the data presented in the corresponding publications, due to the disparity in the simulators, technologies, simulation environments, and testing techniques used. A test chip has been designed and fabricated based on the test benches described in this paper and the reported results are primarily from chip measurements and post layout simulations.

4.2 Classification of adiabatic circuits

Based on their output charging mechanisms, which amount to different levels of energy savings, adiabatic circuits can be divided into diode-based and transistor-based adiabatic circuits.

4.2.1 Diode-based adiabatic circuits

Adiabatic circuits of this class use a diode-based configuration to reduce the power dissipation. The energy dissipation in a conventional CMOS logic circuit is $C_L V_{dd}^2$ per cycle, where C_L is the load capacitance and V_{dd} is the power supply voltage. The energy extracted in an adiabatic charging through a diode, on the other hand, is $C_L V_{dd} V_d$, where V_d is diode's built-in potential [79]. Thus, irrespective of the charging and discharging periods, the maximum possible energy saving in diode-based adiabatic circuits, compared to conventional CMOS gates, is limited to V_{dd}/V_d . Some of the adiabatic logic styles in this category are 2N-2N2D [37], Adiabatic Dynamic Logic (ADL) [38], Improved Adiabatic Pseudo-Domino Logic (IAPDL) [46], and Dual-rail Adiabatic Pseudo-Domino Logic (DAPDL) [62]. The representative diode-based logic styles included in our study are shown in Figure 4.2.

Figure 4.2. (a-d) Some diode-based adiabatic NAND gates; and their (e-f) clocking schemes

4.2.2 Transistor-based adiabatic circuits

Transistor based adiabatic logic styles dissipates energy essentially due to the threshold voltage drop, V_t , across MOS transistors for the charging and discharging of the output nodes. Considering that the energy dissipation of a transistor-based adiabatic logic gate is $C_L V_t^2$, its energy saving over a conventional CMOS gate equals $(V_{dd}/V_t)^2$. Some examples of the logic circuits belonging to this category are 2N-2P, 2N-2N2P [39] Positive Feedback Adiabatic Logic (PFAL) [43], Pass-transistor Adiabatic Logic (PAL) [49], Clocked Adiabatic Logic (CAL) [80], and Improved Pass-Gate adiabatic Logic (IPGL) [61], as shown in Figure 4.4.

(a) CAL

(b) PAL

(c) 2N-2P, 2N-2N2P, IPGL & PFAL

Figure 4.3. (a-c) Clocking schemes for transistor-based adiabatic logic styles

(a) 2N-2P

(b) 2N-2N2P

(c) PFAL

(d) PAL

(e) CAL

(f) IPGL

Figure 4.4. (a-f) Some transistor-based adiabatic NAND gates

4.3 Test-bench setup

To compare the adiabatic logic styles impartially, a uniform test bench is used, as shown in Figure 4.5. The test environment consists of a chain of 32 NAND gates implemented in TSMC CMOSP18 0.18 μ m CMOS technology. Minimum size NMOS and PMOS transistors are used in all logic gates to minimize the energy dissipation. Our simulation results at the schematic level indicate that using larger transistors adversely affects the energy dissipation because of the increased transistor capacitance. Moreover, by using similarly-sized transistors, the capacitive loading condition is the same in all circuits. The clock signal swing equals the supply voltage, V_{dd} . Different adiabatic logic styles need different number of clock phases to enable cascading of several stages. For the circuits we simulated, one, two, and four clock phases are needed for the cascaded operation. Hence, the least common multiple of the required number of clock phases, that is, 4 or multiple of 4 stages of NAND gates should be cascaded together for a fair comparison of these logic gates. To minimize the error of on-chip power measurement, we choose to cascade 32 stages together. The NAND gates are connected in a closed loop, so that there is no need to generate the input signals externally. As illustrated in Figure 4.5(a) and Figure 4.5(b), logic gates can be connected in two fashions.

In the test-bench setup shown in Figure 4.5(a), the outputs appraise the same logic value at each evaluation cycle. We call this the non-toggle mode; whereas we call the test setup in Figure 4.5(b) the toggle mode, because the outputs assess a different logic value at every evaluation cycle. The non-toggle mode represents the circuit behavior when there is no activity or no input changes. The toggle mode represents the case of maximum switching activity and, hence, the maximum power dissipation. The average of these two

is a reasonable figure of merit for evaluating power dissipation. The performance of the chain is, then, observed for frequencies between 10 Hz and 10 GHz. The logic gates with relatively higher load capacitances fail to function properly at higher frequencies due to insufficient charging and discharging time. Power dissipation of the test circuit is calculated by taking average of the instantaneous value of the current, I_i , supplied by the power and clock sources multiplied by the corresponding instantaneous value of the supplied voltage, V_i . Power dissipation is calculated on average data activity by taking the average of the toggle mode and non-toggle mode power dissipations. Each circuit is simulated for 25 complete clock cycles. To eliminate the initial circuit instability effects while calculating power dissipation, the initial five clock cycles are not taken into account.

Figure 4.5. Test-bench setup consisting of a closed-loop chain of logic gates: (a) Non-toggle mode of operation, (b) Toggle mode of operation, and (c) A logic unit block composed of several straight-connected logic gates.

4.4 Test chip fabrication –ICFCUMA1

A test chip has been designed, fabricated, and tested containing NAND gates of different adiabatic logic styles, connected in a closed self signal generating loop with off-chip power and clock signals. Closed loop of adiabatic NAND gates has been layed-out in the same fashion as described in the test bench setup in Section 4.3. Fabrication was needed as a proof of concept and to present the results in the scientific conferences and journals. Measurements from the fabricated chip are very helpful to explore the feasibility of designing low power logic circuits. The fabricated chip's (ICFCUMA1) microphotograph can be seen in Figure 4.6. For the detailed description of design schematic, layout and test fixtures please refer to Appendix A.

Figure 4.6. Microphotograph of the test chip ICFCUMA1

4.5 Performance comparison

4.5.1 Comparison of diode-based logic circuits

Amongst various published diode-based adiabatic circuits, some imperative logic styles are simulated using the test-bench setup described in Section 4.3. Schematics of the diode-based NAND gates are shown in Figure 4.2. As illustrated in Figure 4.2(b) and similar to the circuit presented in [62], instead of diodes, we have used diode-connected MOSFETs. Diode-connected MOSFETs are often more convenient and more efficient than diodes when implemented in standard CMOS technologies. Figure 4.7 shows the power dissipation of the diode-based adiabatic NAND gates for average (50%) data activity verses the clock frequency of operation.

Figure 4.7. Power dissipation at average (50%) data activity versus frequency of operation for diode-based adiabatic circuits

According to the results, ADL logic consumes the lowest amount of energy compared to the other diode-based adiabatic gates. However, this logic style does not produce differential outputs and, hence, is not functionally equivalent to the logic styles with differential outputs. Also, due to its non-differential output and even number of clock phases ADL logic can not be operated in the toggle mode, which gives it an advantage in power estimation over other logic styles as power dissipation in toggle mode is higher than in non-toggle mode. ADL can perform efficiently at a wide range of frequencies, ranging from 10Hz to over 1GHz, with full output swing.

Due to its low output node capacitance, 2N-2N2D logic style cannot function properly at low frequencies. It has the simplest structure among the differential logic styles and its energy consumption is less than half as that of conventional CMOS. Because of its NMOS-only structure, 2N-2N2D does not have a full output swing, which further decreases with increasing the clock frequency.

IAPDL is an improved version of APDL [40] logic family. It is the most power inefficient logic in our comparison group. IAPDL's imbalanced structure causes high power dissipation while using minimum transistor sizing. Power dissipation of IAPDL at lower frequencies can be reduced by increasing the transistor sizes of the evaluation tree, but it further increases the power dissipation at frequencies more than 100MHz. IAPDL is utilizing an external signal, CA, synchronized with the clock, to control the so-called isolation transistor, M3, as depicted in Figure 4.2(c) [46]. The presence of this signal improves the high frequency operation limit of the circuit. At low frequencies, power dissipation of IAPDL is dominated by the control signal CA due to its sharp rising and falling slopes.

Table 4.1. Comparison of diode-based adiabatic logic styles

<i>Logic Style</i>	<i>Transistors</i>	<i>Clock phases</i>	<i>Minimum Operational Frequency (Hz)</i>	<i>Power Dissipation @ 100MHz (Toggle mode) (μW)</i>
2N-2N2D	8	2	10K	0.747
ADL	3	4	10	NA
IAPDL	8	2	10	2.98
DAPDL	10	2	10	2.75
CMOS*	4	1	10	2.74
* conventional CMOS listed for comparison				

At middle frequency range, when the slope of input signals is comparable to the control signal CA, circuit consumes relatively less energy and shows a linear behavior with respect to the frequency of operation. At high frequencies, IAPDL gates' power dissipation is dominated by the unbalanced output node capacitance due to the asymmetrical gate structure of IAPDL.

DAPDL is the latest circuit in the series of pseudo-domino adiabatic logic (APDL) gates. It is a dual-rail input differential logic. This logic style does not require any additional control signal for the isolation transistor. Its balanced structure makes it possible to function properly at lower frequencies as compared to IAPDL. DAPDL consumes less energy than IAPDL. Balanced structure also allows DAPDL to function properly having minimum size transistors. Generally Adiabatic Pseudo Domino Logic family has poor energy efficiency. As shown in Figure 4.2(f), 2N-2N2D, IAPDL and DAPDL, all needs the same type of clocking scheme for the cascaded operation. Figure

4.8 is illustrating the current waveform of the clock at the same time interval for all of these logic styles. Current waveform clearly shows a much higher current, hence higher power dissipation of the IAPDL and DAPDL logic styles.

Figure 4.8. Current waveform of the clock for IAPDL, DAPDL and 2N-2N2D logic styles.

Table 4.2. Dynamic power dissipation of diode-based adiabatic logic styles on average (50%) data activity

Logic Style	Power Dissipation @ 100MHz Toggle mode (Watt)	Power Dissipation @ 100MHz Non-toggle mode (Watt)	Average Power Dissipation @ 100MHz (Watt)
2N-2N2D	7.47E-07	7.35E-07	7.41E-07
ADL	--	9.25E-08	9.25E-08
IAPDL	2.98E-06	1.70E-07	1.57E-06
DAPDL	2.75E-06	4.35E-07	1.59E-06
CMOS*	2.74E-06	1.81E-11	1.37E-06
* conventional CMOS listed for comparison			

4.5.2 Comparison of transistor-based logic circuits

The NAND gate schematics of the prominent logic styles and corresponding clocking schemes of the transistor-based adiabatic logic family are shown in Figure 4.3 and Figure 4.4. Figure 4.9 illustrates the power dissipation per cycle against the frequency of operation for these gates in our toggle mode test environment, whereas Figure 4.10 shows the power consumption of the circuits working in non-toggle mode. 2N-2P, which is also proposed in [45] as ECRL, has one of the simplest circuit structure. It uses four phase clocks to control cascades. The non adiabatic switching event occurs during a brief interval in the beginning of the evaluation phase. In toggle mode, it has slightly higher power dissipation than others, whereas in non-toggle mode its power consumption is lower than other circuits in the comparison group except PAL logic.

Table 4.3. Comparison of transistor-based adiabatic logic styles

<i>Logic Style</i>	<i>Transistors</i>	<i>Clock phases</i>	<i>Minimum Operational Frequency (Hz)</i>	<i>Power Dissipation @ 100MHz (Toggle mode) (μW)</i>
2N-2P	6	4	100	0.766
2N-2N2P	8	4	10	0.805
IPGL	10	4	100	0.311
PAL	6	2	10K	0.375
PFAL	8	4	10	0.337
CAL	10	1	10K	0.657
CMOS*	4	1	10	2.74
* conventional CMOS listed for comparison				

2N-2N2P is an improved version of 2N-2P. As a result of having a cross-coupled inverter SRAM-cell like sensing structure, 2N-2N2P logic gate can operate at higher frequencies compared to 2N-2P. This structure also gives the advantage of non-floating data valid over 100% of the hold phase, which is a problem with 2N-2P logic and most of the diode-based logic circuits.

IPGL structure is an improved version of 2N-2P logic to eliminate any non-adiabatic losses during the charging phase by avoiding threshold voltage drop, but still have some non-adiabatic loss in the recovery path. It consumes less power than most of other adiabatic circuits at the cost of area and complexity.

Figure 4.9. Power dissipation versus frequency of operation for transistor-based adiabatic circuits operating in toggle mode

Figure 4.10. Power dissipation versus frequency of operation for transistor-based adiabatic circuits operating in Non-toggle mode

Figure 4.4(e) shows a NAND gate designed in CAL, a modified version of 2N-2N2P to make it able to operate on single clock phase instead of four phases which is a major drawback in most of the adiabatic logic styles. The main structural difference between CAL and 2N-2N2P is the path control switches in the pull-down tree. In CAL, cascaded structures are controlled by a single-phase clock and two square-wave control signals C_x and $\overline{C_x}$. In terms of their operating speed, CAL gates are comparable to 2N-2N2P gates at higher frequencies, but can not work properly at frequencies less than 10 KHz as the single clock operation provides enough delay to the output dynamic nodes to discharge fully before every evaluation cycle. CAL logic shows medium level power efficiency. In non-toggle mode it consumes the similar power as IPGL and PFAL. CAL circuits attain half the throughput of corresponding 2N-2N2P circuits, however, because they enable logic evaluation in alternate clock cycles.

Table 4.4. Dynamic power dissipation of transistor-based adiabatic logic styles
on average data activity

<i>Logic Style</i>	<i>Power Dissipation @ 100MHz Toggle mode (Watt)</i>	<i>Power Dissipation @ 100MHz Non-toggle mode (Watt)</i>	<i>Average Power Dissipation @ 100MHz (Watt)</i>
2N-2P /ECRL	7.66E-07	9.93E-08	4.32E-07
2N-2N2P	8.05E-07	1.7E-07	4.87E-07
IPGL	3.11E-07	3.15E-07	3.13E-07
PAL	3.75E-07	1.41E-07	2.58E-07
PFAL	3.37E-07	3.31E-07	3.34E-07
CAL	6.57E-07	3.01E-07	4.79E-07
CMOS*	2.74E-06	1.81E-11	1.37E-06
* conventional CMOS listed for comparison			

PAL logic, as shown in Figure 4.4(d), has the least structural complexity. It is similar to 2N-2P, except the ground node is connected to the clock in order to eliminate non-adiabatic energy consumption. PAL achieves fully adiabatic operation at the cost of reduced output swing at high-speed operation. A major advantage of cascaded PAL gates are two-phase clock operation as compared to the four phases, most adiabatic logic circuits operates on. Comparatively PAL shows best power performance. However, PAL logic gates suffer the drawback of undesired capacitive couplings, since the output node, which should remain at zero, is kept floating.

PFAL is an improved version of PAL logic. It has an additional pair of cross coupled pull-down NMOS transistor which eliminates the floating output problem. It also improves the frequency performance of the logic. A drawback of PFAL over PAL is the

need of four clock phases similar to 2N-2P, 2N-2N2P and IPGL for cascaded operation. PFAL can be operated from, as low as, 10Hz to more than 1GHz frequency range. As shown in Figure 4.4(c), PFAL shows very low energy dissipation. Power dissipation of PFAL can further be reduced by connecting the PMOS substrate to the clock which allows better recovery through the substrate diode and eliminates the need of DC power (V_{dd}) line.

Table 4.3 shows a comparison between the key performance parameters of the transistor-based adiabatic NAND gates. While looking at the parametric values presented in Table 4.3, it is evident that adiabatic logic styles consumes about three to nine times less power as compared to the conventional CMOS logic. Comparison of the dynamic power consumption of transistor-based logic styles, operating at 100MHz based on the average data activity, is shown in Table 4.4.

Figure 4.11. Power dissipation at average (50%) data activity versus frequency of operation for transistor-based adiabatic circuits

4.6 Effect of transistor sizing in adiabatic gates

In our simulation setup we used the minimum transistor size for all the transistors in all the logic styles in the comparison group to not give any un-due advantage to a logic style on another, as discussed in Section 4.3. Properly sizing the transistors in any logic style may improve the power dissipation and other performance parameters. In [81] authors have discussed the transistor sizing of PFAL [43] logic in detail. As in Figure 4.12, the authors have shown that in modern technologies leakage and adiabatic losses are dominant as compared to non-adiabatic losses.

Figure 4.12. a) Typical energy dissipation of adiabatic circuits in former technologies. Beside the leakage loss at low frequencies and the adiabatic loss at high frequencies, the non-adiabatic dynamic losses also affect the energy consumption. b) In modern technologies, the reduced threshold voltage lowers the non-adiabatic losses and therefore only the leakage and the adiabatic losses have to be considered. Both mainly depend on the p-channel transistor width. The arrows show the expected dependence for increasing width [81].

Figure 4.13. Energy dissipation versus operating frequency for a PFAL inverter with a load capacitance of 10fF in a $0.13\mu\text{m}$ CMOS technology. Enlarging the p -channel transistor width the energy dissipation is reduced at high frequencies and is increased at low frequencies. The shaded layer represents the theoretical minimum for static CMOS without the effect of leakage currents [81].

Figure 4.14. Energy dissipation versus PMOS width for a PFAL inverter in a $0.13\mu\text{m}$ CMOS technology for different operating frequencies. a) At low frequencies wider PMOS give rise to larger leakage losses. b) At high frequencies a minimum for the energy dissipation between $W_p = 1\mu\text{m}$ and $W_p = 3\mu\text{m}$ can be observed. With a PMOS transistor width $W_p = 2\mu\text{m}$ the energy consumption is reduced by a factor of two [81].

Figure 4.13 is depicting the effect of sizing PMOS charging transistors in PFAL inverter verses the frequency of operation and the energy dissipation per cycle. It can be concluded from the graphs that there is an optimal value of PMOS transistor width at which the energy dissipation is minimum and after that value it will again starting to rise. Where as Figure 4.14 is illustrating the same data for a range of frequencies as a two dimensional graph between width of PMOS transistor and the dissipated energy.

Hence by means of PFAL logic, it is demonstrated that proper transistor sizing helps to extend the usability of adiabatic logic gates to save energy at higher frequencies. However, it will increase the power dissipation as the node capacitance will be higher for larger transistors. For layout tools a mathematical formula has been derived in [81] for optimal transistor sizing. For further details please refer to [81].

4.7 Conclusion

Figure 4.15 is illustrating the energy consumption of the adiabatic NAND gates on average (50%) data activity operating in the linear region of the power verses frequency curve as shown in the graphs of Figure 4.7 and Figure 4.11.

Many of the early adiabatic circuit designs, from Watkins [78] on, used diodes in the charge return path. To the extent that the diode drop is less than logic voltage swings, so that the diode losses are much less than non-adiabatic $\frac{1}{2}CV^2$ losses, this approach may still be useful in the short run, but it must eventually be abandoned when we need still greater energy efficiency. As far as circuits of adiabatic pseudo domino logic (APDL) family are concerned, we already have shown that they are most energy inefficient logic

styles among the other adiabatic circuits. The only diode-based circuits showing good performance are ADL and 2N-2N2D. As we discussed before that due to single ended structure ADL logic is not directly comparable with the other logic styles in our comparison group. However, besides its use of diodes for smaller circuits, where differential outputs are not required, ADL can be the logic of choice.

Figure 4.15. Energy consumption of adiabatic logic NAND gates based on average data activity

On the other hand, transistor based adiabatic circuits are generally showing much better power dissipation. The results indicate that the PAL logic outperforms other adiabatic logic styles in terms of energy efficiency and complexity of structure. It also operates on only two clock phases. But PAL suffers from the floating output node problem during the charging phase. Also it is observed that the PAL logic does not

function properly at lower frequencies. PFAL overcomes both of these weaknesses of PAL logic, but it operates on four clock phases, which is a considerable overhead in practical system design. CAL logic can also be a good choice mainly because of its single clock operation.

4.8 Summary

In this chapter, we have compared different adiabatic logic styles found in the literature and reported the results. The comparisons are based on a uniform test environment of a chain of closed-loop NAND gates. A test chip has been fabricated and the results presented in this chapter are mainly from chip measurement. All simulations are performed at the post-layout level using CMOS18, 0.18 μ m CMOS technology. The performance and power dissipation of the logic styles are evaluated for frequencies of 10Hz to GHz range.

Chapter 5

Adiabatic Systems with Charge-Recovery Power Clock Generators

In addition to the previous chapter where we only discussed the logical part of an adiabatic system, in this chapter we will evaluate the performance of a full adiabatic system including power clock generators (PCGs). As the performance of adiabatic logic styles is already evaluated, in this part of the thesis the emphasis is on the PCGs and the performance of the whole adiabatic system using a particular type of PCG.

5.1 Introduction to energy-recovery PCGs

As illustrated in Figure 5.1, a complete adiabatic system consists of adiabatic logic gates and energy-recovery power clock generator (PCG). PCG plays an important role in the over all efficiency of an adiabatic system. A key aspect in the evaluation of the potential and the perspectives of adiabatic logic families is the performance of complete system, including the PCG. A carefully designed adiabatic clock driver can reduce the power consumption of the system significantly.

Figure 5.1. Basic blocks of adiabatic logic systems

5.2 Classification of adiabatic PCGs

There are two main types of adiabatic clock generators, Step Wise Charging (SWC) Clock Generators and Resonant Clock Generators. Resonant Clock Generators can further be divided into Synchronous and Asynchronous types. We will go through each of them in some detail and will discuss the performance parameters and design issues related to each of them.

Figure 5.2. Classification of energy-recovery power clock generators.

5.3 PCGs test bench setup

To evaluate the performance of adiabatic PCGs following test methodology was utilized. To evaluate the efficiency of the PCG itself, an equivalent adiabatic logic load for which the PCG is to be designed is connected to the PCG output as shown in Figure 5.3(a). Equivalent adiabatic load is an RC series load as described in [82], where $R = P_L / I_L^2$ and $C = 1.414 I_L / \pi V_{dd} f_c$. P_L is the power dissipation of each clock phase, I_L is rms current, V_{dd} is peak voltage of the power clock and f_c is output clock frequency. Power dissipation of the whole system and the power consumed by load has been measured. The ratio of these two values determines the conversion efficiency of the PCG.

$$\text{Conversion Efficiency}_{PCG} = \frac{\text{Power Dissipation}_{RC \text{ Load}}}{\text{Power Dissipation}_{\text{Adiabatic System}}} \quad (5.1)$$

Further, to determine the amount of charge recovery, PCG is connected to the adiabatic logic circuit to form an adiabatic system, as illustrated in Figure 5.3 (b). Charge recovery has been calculated by comparing the power dissipation of adiabatic logic while controlled with non-adiabatic power clock drivers with the power dissipation of the logic controlled by charge- recovery PCG.

$$\text{Energy Efficiency}_{\text{Adiabatic System}} = \frac{\text{Power Dissipation}_{\text{Adiabatic System}}}{\text{Power Dissipation}_{\text{Adiabatic Logic}}} \quad (5.2)$$

Adiabatic logic part in this full adiabatic system test bench has been connected in the same manner as described in Section 4.3 and can also be seen in Figure 5.3.

Figure 5.3. PCG test-bench setup: (a) with RC load, (b) with adiabatic Logic
(c) Inverting mode, (d) Non-inverting mode
(e) A logic unit block composed of several straight-connected logic gates.

5.4 Test chip fabrication – ICFCUMA2

A test chip has been designed and fabricated using 0.18 μ m CMOS technology, CMOSP18. The design of the fabricated circuits is based on the design criteria discussed in Section 5.3. Different 2 and 4 phase charge-recovery PCGs has been fabricated. To make a fair comparison of the PCGs; PAL and PFAL NAND gates has been used as the logical blocks to evaluate the performance of 2 and 4 phase PCGs, simultaneously. The fabricated chip's (ICFCUMA2) layout can be seen in Figure 5.4. For the detailed description of design, schematic, layout, pin-out of the chip, and test fixtures, please refer to Appendix A.

Figure 5.4. Layout of the test chip ICFCUMA2

5.5 Performance evaluation of PCGs

5.5.1 Stair-case or step-wise charging power clock generators

A Step Wise Charging (SWC) adiabatic driver is presented in [83]. It charges the output nodes in N steps using supply voltages V_1 to V_N . To charge the load, switches are briefly closed one after another. So, the charging process takes place in N equal steps. In each step the amount of charging extracted from the supply receives its charge packet q back, except for V_N whose share is dumped to ground. Hence, in every charging-discharging cycle, the net energy dissipated is $E = QV = C_L V^2 / N$. Since multiple supply voltages are complicated and impractical, in an improved version, all are replaced by capacitors, except V_N , as shown in Figure 5.5(a). The two circuits behave identically. A finite state machine (FSM) is needed to control the switches. A single phase SWC clock driver has been designed and simulated. Results presented in Table 5.1 shows that it is not a very efficient clock driver. The efficiency of SWC will be better if it is utilized to drive much larger number of stages as compared to what we have simulated, that is, 32 stages. This will cause the overhead of control logic to be distributed over more number of stages to minimize the power dissipation. Another SWC adiabatic driver is reported in [84], as illustrated in Figure 5.5(b), has been simulated. This adiabatic driver is capable of producing 4 triangular clock phases. Due to large number of control signals it requires more complex FSM. Our simulation results in Table 5.1 showing that it is a very low efficiency clock driver. However, it needs smaller load balance capacitances as compared to single phase SWC driver and it can be used to drive the loads at comparatively higher frequencies. SWC circuit seems to be suitable only for driving large loads, such as buses,

at low frequencies. The energy required to operate the switches and large size of capacitors prohibits high frequency operation of SWC based PCGs. A major advantage of SWC clock drivers, however, is that they can be easily integrated on-chip and requires no inductors as compared to the resonant clock drivers.

Figure 5.5. Step-wise charging clock drivers (a) single phase, and (b) four phase

5.5.2 Resonant power clock generators

The main specifications for an adiabatic PCG is the capability to recover the energy stored in the load capacitances, and a high power conversion efficiency defined as the ratio of the power delivered to the load to the total power used by the system. Oscillators based on LC resonant circuits can meet these requirements and therefore ensures that the complete adiabatic system provides significant power savings with respect to its conventional CMOS counterpart [82]. Several energy-recovery resonant clock drivers are proposed in the literature. Due to the clock generation and routing overheads we are not going to discuss the PCGs with large number of clock phases or which requires special control logic, such as Phase Locked Loop (PLL). Resonant clock generators can further be divided into two groups, that is, Asynchronous and Synchronous Clock Generators.

5.5.2.1 Asynchronous resonant PCGs.

Asynchronous PCGs requires no external control signal. 2N and 2N2P asynchronous PCGs are proposed in [38, 85] and are illustrated in Figure 5.6(a) and Figure 5.6(c). The structure of these PCG is based on gm oscillator. They generate two complementary sinusoidal clocks and can also be tuned to generate two-phase almost non overlapping clocks required for 2N-2N2D, and APDL logic family. These oscillators are sensitive to their capacitive load variations in different cycles of the system operation which results in frequency instability. In addition they can not be used to generate more than two clock phases. 2N2P needs only one inductor as compared to 2N. As can be seen in Table 5.1, 2N2P is more efficient both in terms of conversion efficiency and the charge

recovery. A four phase asynchronous PCG is presented in [86], as shown in Figure 5.6(e). Besides its capability to generate four clock phases, it has several overheads associated with its operation, such as, use of four inductors and the need of schottky diodes. The conversion efficiency of this PCG is low; however, it shows good charge-recovery performance.

Figure 5.6. Resonant adiabatic power clock generators (Continue...)

Figure 5.6. Resonant adiabatic power clock generators

5.5.2.2 Synchronous resonant PCGs.

Synchronous counterparts of 2N and 2N2P PCGs are discussed in [82] and depicted in Figure 5.6(b) and Figure 5.6(d). They are free from the problems associated with asynchronous PCGs; however, they require external control signals. 2N requires two non-overlapping clocks as shown in Figure 5.6(b), whereas 2N2P needs two additional clocks which are complement of the two used for 2N. An added advantage of 2N and 2N2P over their asynchronous versions is the smaller size of transistors. As the transistors are controlled from external signals, the size of the transistors can be kept much smaller. A four-phase synchronous adiabatic PCG is presented in [87] and can be seen in Figure 5.6(f). This PCG generates the trapezoidal clock phases. The advantage of this circuit is the need of only one inductor to generate all four clock phases. The idea of using single rotating inductor is shown in Figure 5.6(f-2). The whole system consists of three main parts; the controller, PCG, and the adiabatic logic, as illustrated in Figure 5.6(f-1).

Controller is used to drive the PCG to virtually rotate the inductor. Structure of PCG is illustrated in Figure 5.6(f-3). Rotation of inductor to transfer the energy between various clock phases is achieved by sequentially switching the transmission gates (TG). This is a very practical and useful design, but the power dissipation overhead of the controller restricts its use to drive smaller systems.

In conclusion, asynchronous PCGs are much larger in area especially at higher frequencies and their oscillation frequencies are affected by the variation in the load. Asynchronous PCGs are more dissipative as compared to their synchronous counterparts; however, they require no additional control signal for their operation. When cautiously designed, at lower frequencies and for smaller systems, asynchronous PCGs can be more practical to implement. However at higher frequencies and with larger systems, synchronous clock generators will exhibit much better power performance. SWC clock generators, on the other hand, have better potential to be utilized for totally integrated large system applications working at lower frequencies.

Table 5.1. Comparison of Adiabatic PCGs at 100MHz

<i>PCG</i>	<i>PCG Conversion Efficiency (%)</i>	<i>Charge Recovery (%)</i>
<i>SWC</i>	11.1	19.1
<i>SWC-4θ</i>	7.2	42.4
<i>2N Synchronous</i>	60.1	27.3
<i>2N Asynchronous</i>	39.9	21.1
<i>2N2P Synchronous</i>	62.0	60.7
<i>2N2P Asynchronous</i>	43.2	44.4
<i>4θ Asynchronous</i>	32.8	56.3
<i>4θ Synchronous</i>	19.2	52.8

5.6 Conclusion

In this chapter, we have evaluated the performance of full adiabatic system including charge-recovery power clock generators found in the literature and reported the results. The comparisons are based on a uniform test environment of a chain of closed-loop NAND gates driven by energy-recovery power clock generators. Simulations are performed at the schematic and layout levels using 0.18 μm CMOS technology. The performance and power dissipation of the logic styles are evaluated for the frequency range of 10 Hz to GHz range. Performance of PCGs has been evaluated as a separate unit to find out the charge recovery capabilities as well as the power conversion efficiency of the clock generators. In the other part, power clock generators are simulated as a part of adiabatic system for recovering energy. For large adiabatic totally integrated systems running at lower frequencies, we recommend SWC clock generators; where as for low frequency, medium size systems, asynchronous resonant charge recovery power clock generators are more efficient. Synchronous resonant charge recovery power clock generators are more efficient for larger systems working at high frequencies. Our simulation results, as given in Table 5.1, shows that more than 60% power conversion efficiency and charge recovery can be achieved with the help of power clock generators.

5.7 Summary

In this chapter we have discussed the classification and design of different energy-recovery power clock generators. The performance of different PCGs has been evaluated in a uniform test environment through simulations and by means of a fabricated chip. The results have shown that in general PCGs are the biggest overheads for the adiabatic logic

system. However an efficiently designed PCG may helps to improve the power dissipation of an adiabatic system significantly.

Chapter 6

Asynchronous Adiabatic Logic

In this chapter a new idea and its practical implementation to achieve low power dissipation in CMOS circuits has been presented namely “Asynchronous Adiabatic Logic (AAL)”. The requirements, advantages and the evaluation of the new logic are discussed in detail and the performance of the AAL based system has been evaluated and compared against its CMOS counterpart.

6.1 Problems in earlier adiabatic systems

As evaluated in Chapter 5, power clock generators (PCGs) are the prevalent overhead for the adiabatic systems and mutilate all the low-power advantage from the adiabatic logic part by consuming a large portion of the total power in the clock generation circuitry. Although PCGs also helps to recover the part of energy supplied to the adiabatic logic, but as we learned in the previous chapter, their operational overhead is usually much more than what they help to recycle, especially in low to medium scale systems. Power dissipation of PCGs is more an issue for the implementation of smaller adiabatic circuits. Because of the large area requirement, on-chip noise issues and low

quality factor, using on-chip inductors for fully integrated PCG is not very efficient. To get the better performance of LC tank based PCG, using off-chip high Q_L inductor is the most viable option which is incompatible with the current trend towards fully integrated system on-chip (SOC) approach.

In addition to the PCG issues, routing multiple clocks for adiabatic circuits all over the chip is not very convenient and raises a number of cost, performance and viability issues. It is getting more and more difficult in the modern highly dense circuits to deal with the issues of routing a single clock only, for the conventional CMOS circuits, in contrast to the requirement of generating and handling the routing and performance and validity issues of multiple clock phases in adiabatic circuitry. In a modern VLSI and ULSI systems using conventional techniques, it is practically impossible to keep the phase shift constant between the multiple clock phases all over the chip. Utilizing other techniques such as phase lock loop (PLL) and delay lock loop (DLL) further increases the overheads of the system and if not eliminate, reduce the lower-power efficiency of the adiabatic system significantly.

To get rid of the problems related to clock generation and inheriting problems of synchronous clock routing, a new solution is proposed to combining the benefits of the adiabatic logic circuits with that of asynchronous logic systems. Going asynchronous not only eliminates the need of PCGs, hence all the problems associated with the generation and routing of the clocks, it also bring all the benefits intrinsically associated with an asynchronous design such as low power and reliable logical operation among the others.

6.2 Advantages of going asynchronous

Much of today's logic design is based on two major assumptions: all signals are binary, and time is discrete. Both of these assumptions are made in order to simplify logic design. By assuming binary values on signals, simple Boolean logic can be used to describe and manipulate logic constructs. By assuming that time is discrete, hazards and feedback can largely be ignored. However, as with many simplifying assumptions, a system that can operate without these assumptions has the potential to generate better results [88].

Asynchronous circuits keep the assumption that signals are binary, but remove the assumption that time is discrete. This has several possible benefits [88]:

No clock skew - Clock skew is the difference in arrival times of the clock signal at different parts of the circuit. Since asynchronous circuits by definition have no globally distributed clock, there is no need to worry about clock skew. In contrast, synchronous systems often slow down their circuits to accommodate the skew. With decreasing feature sizes, clock skew is becoming a much greater concern.

Lower power - Standard synchronous circuits have to toggle clock lines, and possibly precharge and discharge signals, in portions of a circuit unused in the current computation. For example, even though a floating-point unit on a processor might not be used in a given instruction stream, the unit still must be operated by the clock. Although asynchronous circuits often require more transitions on the computation path than synchronous circuits, they generally have transitions only in areas involved in the current

computation. Note that there are techniques being used in synchronous designs to address this issue as well.

Average-case instead of worst-case performance - Synchronous circuits must wait until all possible computations have completed before latching the results, yielding worst-case performance. Many asynchronous systems sense when a computation has completed, allowing them to exhibit average-case performance. For circuits such as ripple-carry adders where the worst-case delay is significantly worse than the average-case delay, this can result in substantial savings.

Easing of global timing issues - In systems such as a synchronous microprocessor, the system clock, and thus system performance, is dictated by the slowest (critical) path. Thus, most portions of a circuit must be carefully optimized to achieve the highest clock rate, including rarely used portions of the system. Since many asynchronous systems operate at the speed of the circuit path currently in operation, rarely used portions of the circuit can be left un-optimized without adversely affecting system performance.

Better technology migration potential - Integrated circuits will often be implemented in several different technologies during their lifetime. Early systems may be implemented with gate arrays, while later production runs may migrate to semi-custom or custom ICs. Greater performance for synchronous systems can often only be achieved by migrating all system components to a new technology, since again the overall system performance is based on the longest path. In many asynchronous systems, migration of only the more critical system components can improve system performance on average, since performance is dependent on only the currently active path. Also, since many

asynchronous systems sense computation completion, components with different delays may often be substituted into a system without altering other elements or structures.

Automatic adaptation to physical properties - The delay through a circuit can change with variations in fabrication, temperature, and power-supply voltage. Synchronous circuits must assume that the worst possible combination of factors is present and clock the system accordingly. Many asynchronous circuits sense computation completion, and will run as quickly as the current physical properties allow.

Robust mutual exclusion and external input handling - Elements that guarantee correct mutual exclusion of independent signals and synchronization of external signals to a clock are subject to meta-stability [89]. A meta-stable state is an unstable equilibrium state, such as a pair of cross-coupled CMOS inverters with inputs and outputs hanging at $\frac{1}{2}V_{dd}$, which a system can remain in for an unbounded amount of time [90]. Synchronous circuits require all elements to exhibit bounded response time. Thus, there is some chance that mutual exclusion circuits will fail in a synchronous system. Some asynchronous systems can wait an arbitrarily long time for such an element to complete, allowing robust mutual exclusion. Also, since there is no clock with which signals must be synchronized, asynchronous circuits more gracefully accommodate inputs from the outside world, which are by nature asynchronous [88].

6.3 Proposed solution -Asynchronous Adiabatic Logic (AAL)

As mentioned in section 6.2, to eliminate the problems associated with the earlier adiabatic systems, a new implementation of combining the low-power capabilities of adiabatic logic with low power, free from global clock operation of asynchronous circuits

has been proposed. As far as the idea is concerned, researchers are working on this direction to combine the advantages of both adiabatic and asynchronous circuits from several years, especially under Intl. Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS) forum [91]. Even a practical attempt is recently reported in [92] but there are known performance and other issues with the proposed solution such as the overhead of the control circuitry have not been included in the reported power dissipation of the system, which is misleading.

6.3.1 Basic Idea of AAL

The basic idea of the proposed AAL is as illustrated in the block diagram of Figure 6.1. The overall system consists of two main blocks, logical block and control and regeneration block. As opposed to the conventional synchronous adiabatic circuits, instead of driving each adiabatic logic unit with an externally supplied clock phase, each block is derived using control signal generated with the help of the logical output of the previous stage, which at the same time is the input to the current logical stage.

Figure 6.1. Block diagram of the proposed AAL

6.3.1.1 Logical block

The logic part of the proposed AAL consists of adiabatic logic. Potentially, it can be any differential adiabatic logic circuit. For the purpose of initial validation of the concept, 2N-2N2P adiabatic logical blocks have been used in the implementation of our AAL.

6.3.1.2 Control and Regeneration (C&R) block.

This block is the key to the concept of AAL. The architecture of this block mainly depends on the type of logical block used in AAL. C&R generates the control signal for the next logical block using the output signal of the previous stage. The regeneration part makes sure that the signal is strong enough to be able to drive the next logical block.

6.3.2 Implementation of AAL

For the initial testing, 2N-2N2P logic has been used as the logical block and many different kinds of simple and complex C&R structures has been designed and tested to get the best power efficiency of the system. A simple implementation of the AAL is depicted in Figure 6.2. It is a chain of inverters, where the logical part is 2N-2N2P and the control part of the C&R block consists of pass gate logic and regeneration part is made of conventional CMOS logic.

Figure 6.2. Initial implementation of AAL

PAL logic was also tried to be implemented in AAL but because of the known issue of floating output in the discharge phase and large leakage current in case of long asynchronous delays, it consumes a large amount of energy. CAL logic needed additional control signals which increase the overheads on the C&R block. Hence although 2N-2N2P is not the most efficient adiabatic logic in terms of power dissipation, it has been chosen as the logical block of AAL so that more attention can be paid to design and optimize the C&R block.

6.3.2.1 Design of C&R Block

Several designs of C&R block have been tried out, as can be seen in Figure 6.3.

The design in Figure 6.3 (a) was the first trial implementation of C&R block using the transmission gates. Besides its proper logical functionality as control unit, there is no path available to discharge the output node below V_{in} of the NMOS in transmission gate as the same signals used as the input are used to control the transmission gates. To solve this problem a modified form, as given in Figure 6.3 (b), has been simulated but due to the high power dissipation of the inverter and energy loss through the pull down n-FET, the overall power efficiency of the system is severely effected.

Another simpler implementation of C&R block is as shown in Figure 6.3 (c) using pass gates. This configuration fails to attain the high output level to V_{dd} . To charge the output to full V_{dd} , a modified form, as illustrated in Figure 6.3 (d), has been simulated but still the low drivability of pass gates makes it difficult to use this configuration as C&R block. It is also difficult to control the slope of the output control signal after going through the CMOS regenerator portion.

Figure 6.3. Different designs attempts of Control and Regeneration (C&R) block

Finally the most common OR gate implementation in a conventional CMOS has been chosen to implement as the C&R block, as given in Figure 6.3 (e). The NOR portion of the gate is acting as the control part where as the NOT portion is not only making the desired logical inversion, but at the same time is performing the regeneration of the signal. The simple structure of the conventional CMOS OR makes it easy to tweak the sizing of transistors to get the desired charging and discharging time and hence slope of the output control signal. The downside of using conventional CMOS OR is its high power dissipation due to non-adiabatic operation which is seems to be un-avoidable in all implementation of C&R block for the AAL discussed in this section.

6.4 Chip Fabrication -ICFCUMA3

A test chip for AAL has been fabricated as a proof of concept in CMOS18 0.18 μ m technology. The layout of ICFCUMA3 can be seen in Figure 6.4. ICFCUMA3 consists of closed loop chain of different adiabatic NAND gates as the logical block and conventional CMOS OR as C&R block.

Figure 6.4. Layout of AAL chip (ICFCUMA3)

6.5 Performance of AAL

The post layout simulations shows that the power dissipation of the AAL logic in its original proposed form is higher than conventional CMOS at average data activity, as can be seen in Figure 6.5. The main overhead is still the C&R block. In addition to the poor low-power performance, higher slope of the output control signal of C&R block is limiting to achieve the full performance of the adiabatic logic. Increasing the length of the C&R block transistors produces lower slope output but the power dissipation of the C&R block itself is steeply increased due to higher resistance and increased leakage.

Figure 6.5. Comparison of the power dissipation of AAL and conventional CMOS NAND gates

6.6 Modified configuration of AAL

To boost the efficiency of the overall AAL system, a new approach has been proposed for the efficient implementation of relatively large circuits. In practical operation of circuits, many logical blocks receive data, evaluate logic and produce the valid output approximately at the same time. Hence, instead of using a separate C&R block for every logic unit, only one C&R block of appropriate size can be used for all the logical blocks supposed to evaluate the logic at the same time. This concept can be seen in Figure 6.6. This helps to reduce the overall power dissipation of the system by eliminating the unnecessary C&R blocks.

Figure 6.6. Block diagram of the proposed modified AAL

Figure 6.6 shows the implementation of the AAL at block diagram level. The logical blocks that are supposed to make the evaluation together are derived using a single control signal. Hence, only one C&R block is required to drive those logical blocks. Depending on the number of logical units to be controlled by a single C&R block, the transistor sizes of the C&R block should be adjusted to maintain the drivability or fan-out. The output of the slowest logical block should be utilized as the input to the next C&R block. The number of logical blocks derived by a single C&R block in a system is flexible and doesn't have to be same for all the C&R blocks, as can be seen in the block diagram above. The outputs of the logical units derived by a single C&R can be feed as an input to any of the logical unit in the immediate next group of logical blocks. The larger the number of logical blocks derived by a single C&R block the more power efficient implementation it is.

6.6.1 Implementation based on the modified approach

For the proof of the concept 4, 8 and 16 bit adders has been implemented in AAL logic with 2N-2N2P as the logical block and conventional CMOS OR as the C&R block. The schematic of the 4 bit AAL adder can be seen in Figure 6.7. For the comparison of the power dissipation, corresponding 4, 8 and 16 bit adders in conventional CMOS are also been simulated. A 4 bit adder implementation in conventional CMOS is shown in Figure 6.8. Table 6.1 lists the power dissipation of conventional CMOS and AAL adders at different frequencies.

In Figure 6.7 a fast-carry 4 bit adder implemented in AAL has been illustrated. All the logical blocks are divided into 4 groups and have been implemented using

2N-2N2P adiabatic logic. A two input NAND gate in 2N-2N2P adiabatic logic can be seen in the zoomed part of Figure 6.7. C&R block is implemented using conventional CMOS OR as can also be seen in the other zoomed region of the figure. The first group of logical blocks is operated using an external control signal. The other three groups are derived by the C&R blocks. The input to the C&R block is taken from the slowest logical unit in a particular group. All three C&R blocks are highlighted to distinguish them from the rest of the circuit. 8 and 16 bit AAL adders have also been simulated using the same structure of 4 bit adder connected in series. Figure 6.8 illustrates the implementation of the 4 bit fast-carry adder designed in conventional CMOS logic using the same design structure used to implement AAL adder.

6.6.1.1 Performance comparison of AAL and conventional CMOS adders

The simulation results of both AAL and conventional CMOS adders are as presented in Table 6.1. The power dissipation of all simulated adder structures can also be seen graphically in Figure 6.9 for operating frequencies as low as 10MHz and as high as 200MHz. It can be noticed that the power dissipation of the AAL adders at lower frequencies is higher than conventional CMOS adders. This is mainly because of the high leakage current and non-optimized delays of the logical blocks and C&R block for this particular implementation. However, with increasing input data rate the power efficiency of the AAL adders is improving in a non-linear fashion, as can be observed in Figure 6.9 or from the data presented in Table 6.1.

Figure 6.7. 4 Bit fast-carry AAL adder using 2N-2N2P as logical block and conventional CMOS as control and regeneration block.

Figure 6.8. 4 Bit fast-carry adder implementation in conventional CMOS

Table 6.1 Comparison of Adiabatic vs. CMOS fast-carry adders

Frequency	10 MHZ	100 MHZ	200MHZ
<i>Conventional CMOS (μW)</i>			
4 bit	14.81	123.9	251.7
8 bit	30.75	260.4	529.0
16 bit	62.68	533.3	1084
<i>Asynchronous Adiabatic Logic (AAL) (μW)</i>			
4 bit	25.166	96.142	173
8 bit	52.285	212.77	342.456
16 bit	106.0616	442.516	686
<i>Synchronous Adiabatic Logic (2N-2N2P) (μW) without PCG</i>			
4 bit	5.100	44.09	81.193
8 bit	9.919	88.87	181.724
16 bit	21.104	176.67	358.75

Figure 6.9. Comparison of the power dissipation of AAL and conventional CMOS fast-carry adders

Figure 6.10. Simulated waveforms of 16-bit AAL fast-carry adder. Clk1 is input control signal also connected to the carry-in Cib. Ci is connected to ground.

Table 6.2 Area overhead of AAL vs. conventional CMOS fast-carry 4 bit adders

Logic Style	No. of Transistors	On Chip Area* (μm^2)
Conventional CMOS	240	~1440
AAL	342	~2008
Difference	102	568 **
* Including signal routing		
** AAL is 39.5% larger		

The implementation of adder in AAL logic as in Figure 6.7 is failed to operate in GHz range; hence all simulation have been done at the highest frequency of 200MHz. The high frequency operation of the AAL adder can be improved by optimizing the associated signal delays of logical and C&R blocks and more precise control of the slope of the control signal. We choose not to optimize any of the implementation in any manner to remains at a fair comparison level. In addition, potentially much higher power efficiency can be achieved by carefully controlling the slope of the control signal.

As shown in, on the down side of AAL we have a large on-chip area overhead associated with AAL. But considering the gain in power efficiency, which is more than 35% at higher frequency (Table 6.1, 16 bit adders at 200MHz), it is an acceptable value. The area of AAL can be reduced by trying to implement other logical blocks than 2N-2N2P, such as PAL logic.

6.7 Conclusion

The simulation results of the adders implemented in proposed AAL are very promising and have shown an intense potential to be the way-to-go for the designers of power aware systems. Optimizations of the logic delays and more precise control over the slope of the control signal can make the AAL a power efficient logic. Evolution of technologies such as SOI or MEMS based switches to limit the leakage currents at lower speeds will be very helpful for the power efficient operation of our proposed design and the very low frequency operation of adiabatic logic circuits.

6.8 Summary

In this chapter a new circuit design approach has been proposed based on the idea of combining the benefits of asynchronous systems with those of adiabatic logic style. A fast-carry adder has been implemented in the proposed logic and compared with an equivalent conventional CMOS fast-carry adder. The results are encouragingly in favor of the AAL structure.

Chapter 7

Concluding Remarks

In this chapter we summarize the conclusions and point to the important areas for future research along the lines of this thesis. Further, we list the contributions that have arose from this work.

7.1 Conclusions

The foremost goal of this research work is to conserve energy through achieving higher power efficiency in electronics circuits. At the beginning of this thesis the need and potential in the area of low-power circuits has been outlined. The main sources of power dissipation in conventional circuit approaches are pointed out. A detailed discussion on the two promising low-power circuit techniques, charge-sharing logic, and adiabatic logic is presented.

Pros and cons of the key charge-sharing circuits have been discussed. It is found that the logic overheads such as on-chip area and multiple clock management are significant as compared to the power saving and other performance advantages charge-sharing circuits are offering.

Performance of foremost adiabatic logic circuits is evaluated using a uniform test environment and a custom designed chip and the results are presented in detail. Based on the performance comparison, key problems associated with the practical implementation of the corresponding adiabatic circuits have been singled out. Chip measurements and simulated results demonstrated that upto nine times power saving can be achieved using adiabatic logic.

To further exploit the potential of adiabatic logic, full adiabatic systems with power clock generators to get the advantage of charge-recovery has been designed and evaluated. For small scale systems, based on the power they consume as compare to the power they help to recover, it is found that PCGs are themselves a design and performance overhead. However, for large scale logic implementations, significant amount of power can be retrieved as the overhead associated with the PCGs will be trivial when divided over a larger number of logic units.

In all of the low-power techniques evaluated in this thesis, clock management appears to be the bottle neck for the performance of the system. To solve this problems a new circuit technique to coalesce the benefits of adiabatic and asynchronous circuits, named Asynchronous Adiabatic Logic or AAL in short, has been proposed to completely get rid of the clock. Based on the proposed solution some circuits has been designed and simulated and after some modifications to the implementation of originally proposed logic, it is demonstrated that using AAL, more than 35% of power can be saved as compared to the conventional CMOS logic.

7.2 Future work possibilities

Considering the time and availability of resources the future work possibilities in continuation of this work can be divided into near term and long term goals.

7.2.1 Near term prospective

There is still room to further increase the efficiency of the proposed AAL system. The possible areas to focus on are as follows,

- Successful design of a fully or partially adiabatic C&R block will be the key to improve the power efficiency of the whole AAL system.
- As discussed in Section 4.7, optimizing the size of adiabatic logic units will further help to reduce the power dissipation.
- As already mentioned in Section 4.8 and Section 6.4.2, 2N-2N2P logic is not the most efficient adiabatic logic and is initially used only to concentrate more on the design and optimization issues of C&R block. Hence, a more efficient adiabatic logic style such as IPGL and PAL can either be used directly or modified a little to be utilized as the logical block in the proposed AAL to further push its efficiency to an optimum point.
- Design and fabrication of a full functional chip consists of some applications implemented in the AAL will help to explore the potential and usability of this design approach for the commercial low-power devices.

- Based on the success of the test chip there is a high potential of the commercial adoption of the proposed design methodology. Hence, the relevant patents can be obtained to protect the intellectual property (IP) rights.

7.2.2 Long term potential

- If the test chip, proposed in the short term goals, demonstrate significant performance advantage over the conventional approaches considering all the overheads of the new logic such as large area, work can be done to utilize the proposed design methodology to make a stand alone processing unit which can be used as the processing part of a bigger design such as implantable bio-medical devices, deep space probes, under sea instrumentation and sensors or mobile applications such as portable multimedia players and laptops among the others. Designs can also be made available as IP blocks for single chip full system integration.
- Considering the evolution of technology, future devices like single electron transistors fabricated using Nano Electro Mechanical System (NEMS) [93] will help us to efficiently control the sources of power dissipation such as leakage current and parasitic capacitances. Having those technologies available, we will be able to get most out of the adiabatic logic and AAL approaches at a very wide range of frequencies.

7.3 List of contributions

The contributions arising from this work are as follows:

- First detailed comparison of charge-sharing has been made and advantages and problems associated with different charge-sharing logic circuits have been documented.
- Considering the available literature, first time the comparison and performance evaluation of the most prominent adiabatic logic circuits has been done with the help of exclusively designed and fabricated chip for this purpose.
- Performance of different power clock generators (PCGs) for adiabatic circuits has been evaluated in a full adiabatic system implementation. A second chip has been designed and fabricated for this purpose.
- Based on the comparison and performance evaluations of different low power techniques, a new implementation of a the concept of combining the power of asynchronous circuits with that of adiabatic logic has been proposed, named Asynchronous Adiabatic Logic "AAL". A third chip has been designed and fabricated for the proof of concept and a modified form of AAL has been implemented and simulated showing very promising power efficiency.

7.3.1 Contribution in the form of publications

Following is the list of those publications arises from this research work.

1. Arsalan, M., Shams, M., "Performance Review of Charge Recycling Logic Circuits", IEEE Canadian Conference of Electrical and Computer Engineering (CCECE), pp. 1919-1922, May 2004.

2. Arsalan, M., Shams, M., "An Investigation into Transistor-Based Adiabatic Logic Circuits", IEEE Northeast Workshop on Circuits and Systems (NEWCAS), pp. 1-4, June 2004.

3. Arsalan, M., Shams, M., "Charge-Recovery Power Clock Generators for Adiabatic Logic Circuits" Accepted Paper, 8th IEEE International Multitopic Conference (INMIC), 2004.

4. Arsalan, M., Shams, M., "Comparative Analysis of Adiabatic Logic Styles" Accepted paper, IEEE VLSI Design 2005

In addition to the publications listed above, one article for IEEE journal of solid state circuits and one conference paper are in advance stages of completion.

Appendix A

Experimental ICs; Design, Fabrication, and Test

This Appendix presents a road-map of the fabricated chips. Three different ICs have been fabricated during the course of this research. A detailed description of each chip including, technology, implemented circuit, chip layout, extracted view, chip microphotograph, test fixture and test-bench is presented in this section.

A.1 Road-map of the fabricated chips

Table A.1 lists the major details of the fabricated ICs.

Table A.1 Roadmap of the fabricated chips

<i>Design Name</i>	<i>Technology</i>	<i>Area</i>	<i>Package Type</i>	<i>Year</i>	<i>Test Fixture</i>
ICFCUMA1	TSMC CMOSP18	1mm x 1mm	CFP24	Nov 2003	CFP24TF (PCB-TF2)
ICFCUMA2	TSMC CMOSP18	0.75mm x 0.75mm	CFP24	March 2004	CFP24TF (PCB-TF2)
ICFCUMA3	TSMC CMOSP18	1.13mm x 0.49mm	Loose Dice	March 2004	Analytical Probe Station (APS)

A.2 ICFCUMA1

This chip has been designed to test the functionality and compare the performance of most prominent adiabatic logic styles in a uniform test environment, as discussed in section 4.3 of this thesis.

A.2.1 Layout of ICFCUMA1

A.2.2 Extracted view of ICFCUMA1

A.2.3 Microphotograph of ICFCUMA1

A.2.4 Pinout of ICFCUMA1

Table A.2 Pinout details of ICFCUMA1.

<i>Pin # on Dice</i>	<i>Pin # on Package</i>	<i>Signal</i>	<i>Description</i>
1	1	Vbias	Control voltage for input analog buffers
2	2	Gnd	0V - Ground
3	3	Vdd1	1.8V – Adiabatic Circuit Supply
4	4	Ck1	Clock Phase 1
5	5	Gnd	0V – Ground
6	6	Ck2	Clock Phase 2
7	7	Ck3	Clock Phase 3
8	8	Gnd	0V – Ground
9	9	Ck4	Clock Phase 4
10	10	Vdd2	3.3V supply for analog input buffers
11	11	Vss	Ground
12	12	Out	Output
13	13	Outb	Inverted (differential) output
14	14	Gnd	0V – Ground
15	15	Vdd	1.8V – Supply for power ring.
16	16	X2	Select line 2 of 3:8 decoder
17	17	Gnd	0V – Ground
18	18	X1	Select line 1 of 3:8 decoder
19	19	X0	Select line 0 of 3:8 decoder
20	20	Gnd	0V – Ground
21	21	NC	Not connected
22	22	Vdd	1.8V – Redundant supply for power ring.
23	23	Gnd	0V - Ground
24	24	NC	Not connected

A.2.5 Test Fixture of ICFCUMA1

CMC's standard test fixture 2 (TF2) has been used for the testing of ICFCUMA, as shown in Figure A.1.

Figure A.1. Test Fixture 2 (TF2)

A.2.6 Design Description of ICFCUMA1

ICFCUMA1 consists of seven different adiabatic logic circuits, listed in Table A.3. All of the circuits are adiabatic NAND gates implemented in a manner described in the test-bench setup, Section 4.3. This chip has been designed to be tested using standard packaging (CFP24) and test fixture (TF2) provided through Canadian Microelectronics Corporation (CMC). While using TF2, we can only use 12 pins for I/O signals whereas other 12 are ground and supply connections. Each adiabatic circuit requires 2 to 4 pins for external clock signals to operate, 2 pins for differential output and 1 for supply voltage for substrate bias. To overcome this shortage of I/O signal pads on-chip analog multiplexer for signal output and de-multiplexers for input signals have been designed.

Only one 3 to 8 line decoder has been utilized to control all the multiplexers and demultiplexers. Appropriate analog and digital buffers have also been designed for all the I/O signals including clocks.

Table A.3 Logic Circuit Selection on ICFCUMA1

Logic Style	Output (Low)	X0	X1	X2
2N-2N2D	7	0	0	0
DAPDL	6	0	0	1
PAL	5	0	1	0
2N-2P	4	0	1	1
PFAL	3	1	0	0
2N-2N2P	2	1	0	1
IPGL	1	1	1	0
None*	0	1	1	1
* Test mode				

A.2.7 Testing Methodology of ICFCUMA1

To precisely measure the power dissipation of all the adiabatic circuits, considering the multiplexed signal routing and unavoidable use of high power dissipation analog and digital buffers for I/Os, the following strategy has been adopted.

There are total 8 signal lines available for logic circuits implementation using 3-8 line multiplexers and de-multiplexers. Instead of connecting all of the multiplexer and demultiplexer inputs and outputs to the adiabatic circuits, one of the connection is left floating. The substrate biasing power supply for p-FETs of all adiabatic logic has also been multiplexed and implemented separately from other circuit supplies. Now, before measuring the power dissipation of a particular adiabatic circuit, provided all the supply and clock signal connected and running, the decoder is first switched to the test mode ($X_0 = 1$, $X_1 = 1$, $X_2 = 1$) as listed in Table A.3. After measuring the power in that mode, which accounts to the on-chip overheads of I/O buffering and any leakages etc, the decoder is set to switch to the desired address to measure the power dissipation of a particular adiabatic circuit. The difference of these two gives a very precise measure of the power dissipation of adiabatic circuits only.

A.3 ICFCUMA2

The second chip has been designed to test the performance and functionality of adiabatic PCGs implemented in a full adiabatic system as described in Section 5.3.

A.3.1 Layout of ICFCUMA2

A.3.2 Extracted view of ICFCUMA2

A.3.3 Pin out of ICFCUMA2

Table A.4 Pinout details of ICFCUMA2.

<i>Pin # on Die</i>	<i>Pin # on TF</i>	<i>Signal</i>	<i>Description</i>
1	1	LA	External inductor pad A
2	2	Gnd	Ground
3	3	Vdd Ckts	1.8V Supply for circuits to be tested
4	4	Ck1	Control/ synchronization signal for PCGs
NA	5	NA	Not available
6	6	Ck2	Control/ synchronization signal for PCGs
7	7	Out	Output signal
NA	8	NA	Not available
9	9	Outb	Inverted (differential) output
10	10	Vdd 1.8V	1.8V supply for power ring
11	11	Gnd	Ground
12	12	X1	Select line 1 of 2:4 decoder
13	13	X0	Select line 0 of 2:4 decoder
14	14	Gnd	Ground
15	15	NC	Not connected
16	16	Clk	External clock phase 1
NA	17	NA	Not available
18	18	Clkb	External clock phase 2
19	19	Vdd 3V	3V supply for analog input buffers
NA	20	NA	Not available
21	21	Vbias	Control voltage for input analog buffers
22	22	Vdd 1.8V	Redundant 1.8V supply for power ring
23	23	Gnd	Ground
24	24	LB	External inductor pad B

A.3.4 Test Fixture of ICFCUMA2

This chip has been designed to be tested using the same test fixture as used for the first chip ICFCUMA1.

A.3.5 Design Description of ICFCUMA2

ICFCUMA2 consists of three power clock generators with appropriate adiabatic logic implemented as a full adiabatic system and an adiabatic logic circuit closed loop array driven from external clock signals, implemented in the same fashion as described in Section 5.3.

This chip is designed to be packaged and tested using the same package (CFP24) and test fixture (TF2) as was utilized for ICFCUMA1. Due to the smaller available chip area ($750\mu\text{m} \times 750\mu\text{m}$), hence to save the space, instead of making all 8 ground pads required for CFP24 package, only 4 of them has been layed-out on the chip. Hence in the packaged chip there are 4 not connected pins.

To efficiently use the area and available I/Os, the same multiplexing technique has been used as was in ICFCUMA1. All the analog multiplexers and de-multiplexers and analog and digital I/O buffers has been reconfigured and layed-out using the specific needs of ICFCUMA2, keeping the same design techniques as utilized in previous chip.

Two resonant synchronous (2N and 2N2P) PCGs with PAL as logical block and one stepwise synchronous PCG (4ϕ , single inductor) with PFAL as logical block have been implemented on the chip. Only PAL logic driven from external clocks has also been implemented to facilitate the performance measurement of clock generation part only.

A.3.6 Testing Methodology of ICFCUMA2

2 to 4 line analog multiplexers and de-multiplexers have been used in this chip. Again instead of implementing 4 adiabatic systems, only 3 has been implemented and the forth place has been left floating to be able to measure the power dissipation of adiabatic system only, neglecting all the on and off chip controlling and other overheads. Off-chip inductor has been used for all PCGs due to limited area and other practical design issues such as single value and low quality factor, among the others. As mentioned in design description, a PAL logic closed loop cluster is also layed-out, driving from external clock signals to facilitate the performance measurement of PCGs only. The efficiency of the full adiabatic system and that of PCG is measured using the formulas as given in Section 5.3.

A.4 ICFCUMA3

This chip has been designed as a proof of concept for the proposed asynchronous adiabatic logic (AAL), as discussed in section 6.3 of this thesis.

A.4.1 Layout of ICFCUMA3

A.4.2 Extracted view of ICFCUMA3

A.4.3 Pin out of ICFCUMA3

Table A.5 Pinout details of ICFCUMA3.

<i>Pin Number</i>	<i>Signal</i>	<i>Description</i>
<i>Top probing pad (left to right)</i>		
1	Vdd IPGL	Supply for IPGL based AAL
2	GND	Ground
3	Ctrl IPGL	External control signal for AAL
4	GND	Ground
5	Outb	Inverted output
6	Out	Output
7	GND	Ground
8	Vdd	Supply for the buffers
<i>Bottom probing pad (left to right)</i>		
1	Vdd PFAL	Supply for PFAL based AAL
2	GND	Ground
3	Ctrl PFAL	External control signal for PFAL based AAL
4	GND	Ground
5	Outb	Inverted output
6	Out	Output
7	GND	Ground
8	Vdd	Supply for the buffers

A.4.4 Test Fixture of ICFCUMA3

This chip is designed to be tested using Analytical Probing Station. Hence the chip is to be tested in the form of loose die.

A.4.5 Design Description of ICFCUMA3

This chip consists of two different implementations of initially proposed asynchronous adiabatic logic, as discussed in section 6.3. C&R block in both of the implementation is conventional CMOS OR gate, whereas the logical block for the first is IPGL and for the second is PFAL logic. OR gates are separately optimized for both designs to handle the control signal delay.

A.4.6 Testing Methodology of ICFCUMA3

This chip has been designed to be tested using Analytical Probing Station (APS) to avoid all the parasitic components associated with the packaging. Separate power supplies are used for the main circuit and for the other control and other overheads, such as I/O buffers. No multiplexing is used due to the availability of ample number of I/O pads.

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