A Novel Clock Distribution System with Injection Locked Rotary Traveling Wave Oscillator and Built-In Self-Test

By

Zhanjun Bai, B.Eng., M.A. Sc.

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Abstract

The thesis implemented a clock distribution system with novel Injection Locked Rotary Traveling Wave Oscillators (IL-RTWOs) and Built-In Self-Test (BIST). Both trans-conductance injection locking and pulse injection locking techniques are explored. The combination of switched Metal-Insulator-Metal capacitors (MIM-caps) and a novel use of Complementary Varactor Pairs (CVPs) target a 1.7 GHz to 2.0 GHz frequency tuning range and 100 kHz frequency resolution. The Complementary Varactor Pairs (CVPs) implemented for RTWO phase tuning achieves 56° phase tuning range and 0.34° worst case phase tuning resolution. The RTWO scheme is implemented in IBM's 130 nm CMOS technology. The RTWO free running phase noise is -126dBc/Hz at 1MHz offset from 2 GHz operating frequency. With the injection locking techniques, the RTWO inband phase noise is further reduced. This project also describes a Built-In Self-Test (BIST) circuit used to verify and tune the timing integrity of the clock distribution system. The die area is limited by the outer parameter of the RTWOs – leaving internal space for other circuits. The BIST circuit occupies 0.025 mm^2 chip area. The BIST circuit allows testing of the integrity of the clock distribution system at speed by determining if the system clock skew can be tolerated or needs adjustment. The clock distribution network consumes a total of 26.5 mA current from a 1.14 V power supply. The close-in spurs of the IL-RTWO are 79 dB lower than the output spectrum. The IL-RTWO attains an inband phase noise performance of -132 dBc/Hz at 100 kHz offset from 2.039 GHz output and its integrated rms jitter from 1 kHz to 40 MHz offset frequency is 39 fs. The pulse and transconductance injector circuits are analyzed and measured and it

is shown that the pulse injector tends to achieve better phase noise performance. To the author's best knowledge, the implementation of CVPs and injection locked techniques on RTWO, and the implementation of this BIST technique to determine clock integrity of an injection locked clock distribution network have not been explored previously.

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List of Abbreviations

ATE	Automated Test Equipment
BIST	Built-In Self-Test
CMOS	Complementary- Metal- Oxide- Semiconductor
CP	Charge Pump
CQFP	Ceramic Quad Flat Pack
CUT	Circuit Under Test
CVP	Complementary Varactor Pair
DCO	Digitally Controlled Oscillator
DEM	Dynamic Element Matching
DNL	Differential Non-Linearity
DRC	Design Rule Check
g_m	Transconductance
IC	Integrated Circuit
ILO	Injection Locked Oscillator
INL	Integral Non-Linearity
IL-RTWO	Injection Locked Rotary Traveling Wave Oscillator
LSB	Least Significant Bit
LVS	Layout Versus Schematic
MIM	Metal-Insulator-Metal

MOM	Metal-Oxide-Metal
MSB	Most Significant Bit
ncap	N+ polysilicon gate over n-well with a thin oxide structure
PCB	Printed Circuit Board
PN	Phase Noise
PRBS	Pseudo Random Binary Sequence
PSS	Periodic steady state simulation engine
PVT	Process Voltage Temperature
Q	Quality factor
RTWO	Rotary Traveling Wave Oscillator
TPG	Test Pattern Generator
VCO	Voltage Controlled Oscillator

Chapter 1 : Introduction

The introduction focuses on the overview of the project, motivation and technical contributions. It also specifies and outlines the thesis organization.

1.1 Motivation

The conventional balanced H-tree and grid structure clock distribution techniques become less effective as clock frequencies increase in multi-GHz systems. This is due to the interconnect variations, load mismatch, and process variations [1] – [4]. Liu et al. [3] observed that interconnect variations alone account for 25% deviation of the clock skew in a gigahertz microprocessor from its nominal value. Time-varying supply noise is also injected into the clock path, which worsens the timing margin [3]. Moreover, large scale digital circuits clocked at speed create correlated digital noise. This digital switching noise is propagated into the oscillator power supply and substrate, which significantly degrades the oscillator performance and introduces more skew into the clock signal. In the planning stages, it is critical to differentiate the impact of the above design parameters on clock skew. However, this is difficult to achieve because of the complex relationship among these different dependent and independent design parameters [1] – [4].

Motivated by greater economies of scale, higher levels of integration and faster operating frequencies, CMOS feature sizes continue to scale according to Moore's law from the submicron to the nanometer range. While digital circuits immediately benefit from such scaling, analog, mixed-signal and RF circuit designers are faced with challenges in achieving the same scaling benefits. Lower supply voltages and short

channel effects such as reduced output impedance, hot-carrier effects and velocity saturation complicate the design of scaled analog circuits. Thus it is apparent that an analog circuit that can be transposed to an equivalent mixed-signal circuit which maximizes the digital to analog circuit ratio will more readily and expeditiously benefit from continued CMOS scaling. Such circuits will benefit from lower cost due to reduced die size, and lower power as a result of lower parasitic capacitances. The proposed pulse injection locked RTWO with BIST is highly digital which can be readily shifted to more advanced technologies.

1.2 Thesis Focus

This thesis focuses on the implementation of the Injection Locked Technique on Rotary Traveling Wave Oscillators (IL-RTWOs) and the Built-In Self-Test technique (BIST). Both the transconductor injector and the narrow pulse injection are explored. This research also strives to develop a purely digital Built-In Self-Test (BIST) circuit to detect clock skew which will be eliminated by phase tuning an Injection Locked- RTWO (IL-RTWO). In addition, a large amount of the digital circuits and clock tree buffers are implemented on-chip and clocked by the RTWOs. These digital filters produce correlated digital noise which makes the design similar to a real micro-system.

1.3 Thesis Organization

This thesis contains seven chapters.

Chapter 1 gives the project overview, the project motivation and technical contributions are also proposed.

Chapter 2 provides an overview of on-chip noise sources. The Clock Skew and Uncertainties, Built-In Self-Test (BIST), Injection Locked Oscillators and Rotary Traveling Wave Oscillator are discussed.

Chapter 3 presents the detailed Injection Locked Rotary Traveling Wave Oscillator (IL-RTWO) and Built-In Self-Test (BIST) design.

Chapter 4 presents the IL-RTWO and BIST simulation results.

Chapter 5 presents the layout of the IL-RTWOs and BIST circuit.

Chapter 6 presents the IL-RTWO and BIST measurement results.

Chapter 7 presents the conclusion drawn from this work and future works.

1.4 Thesis Contributions

At the completion of the research several contributions in the field of clock distribution system have been achieved. The contributions are as follows,

- Injection locked RTWO architecture is fully integrated in CMOS that is highly digital in nature and scales with device size. This leads to a high Q and low phase noise oscillator. The RTWO is much less sensitive to the switching noise, power supply noise and substrate noise than LC-oscillator.
- A novel clock distribution scheme which allows clocking the micro-system at high frequency only locally instead of clocking the system at high frequency all over the clock distribution path, thus eliminating the hierarchical clock buffers

and reducing their related clock jitters and power consumption.

- Implementation of Complementary Varactor Pairs (CVPs) on the RTWO is a novel concept. By properly choosing the size of CVPs, ultra-fine step capacitance can be achieved which results in precise frequency and phase resolution even in a large feature size CMOS process, thus reducing the phase noise.

- The incorporation of the BIST can be used to detect clock skews; therefore on chip communications can be achieved. The clock skews detected by the BIST circuit are adjusted by the on-chip CVPs controlled by either an on-chip or off-chip micro-controller.

- Both transconductance injector and pulse injector are presented. The proposed pulse injection locked RTWOs are highly digital and achieve better phase noise performance than tranconductance injection locked RTWOs. The digital pulse injection locked circuit described in this thesis can be readily implemented in more advanced digital technologies.

- The IL-RTWOs offer a scalable architecture with low-skew clock distribution over an arbitrary chip area. This clock distribution network will benefit from lower cost due to reduced die size with increased operating frequency. The architecture is extendable to an n-element RTWO array.

- The proposed clock architecture was designed for multiple applications. For example, in mixed signal ICs, the clock challenges are even more severe, where 1 ps skew budget may be required to clock a high performance DAC array or parallel ADCs. Therefore, the 650fs phase tuning resolution achieved in this

design could be implemented to clock the above DAC array or parallel ADCs. The proposed architecture can also be applied to clock phased arrays antennas [105], interleaved data-converters [116], [152], [153], high speed SERDES [156], high performance microprocessors [154] and other digital systems [155].

1.5 Publications and Awards

The Injection Locked Rotary Traveling Wave Oscillator with transconductance injector has initially been reported at the 2014 IEEE International Symposium on Circuits and Systems (ISCAS) [115]. This paper was evaluated as the highest quality paper and invited to submit an extended paper to the IEEE Transactions on Circuits and Systems I.

The Built-In Self-Test circuit developed in this project facilitates the on-chip communication between different clock domains. The test instrument requirement and cost are both reduced. The phase tuning technique and Built-In Self-Test technique has been reported in the IEEE Transactions on Circuits and Systems II (TCAS II) [151].

The conducted mathematical analysis of unlocked RTWO phase noise in Chapter 2 along with measurements in Chapter 6 explored the free running RTWO phase noise performance. The mathematical analysis in chapter 3 showing the relationship between the rising/falling time, duty cycle of a rectangular waveform and its fundamental-to-n^{th}-harmonic ratio. The injection pulse width is optimized to provide sufficient injection power based on the analysis. These have been submitted to the Journal of Solid State Circuit.

The fabricated chips have been demonstrated and presented at CMC TEXPO 2013 and CMC TEXPO 2014. This work was winner of the 2014 Strategic

Microelectronics Council (SMC) of ITAC Industrial Collaboration Award (with a $3,000 prize), for having the presentation with the best demonstrated research activity arising from university-industry collaboration which produced substantive results with commercial potential.

1.5.1 Publications and Awards in Refereed Conference Proceedings

The following is a list of articles and awards containing various aspects of the work presented in this thesis:

[a] Z. Bai, X. Zhou and R. Mason, "A Novel Injection Locked Rotary Traveling Wave Oscillator," IEEE International Symposium on Circuits and Systems, pp. 1768 – 1771, June 2014**. (Evaluated as the highest quality paper (distinguish paper award) and invited to submit a TCAS-I paper)**

[b] CMC Microsystems 2014 Annual Symposium - Winner of the 2014 Strategic Microelectronics Council (SMC) of ITAC Industrial Collaboration Award.

Comments from Industrial and Academic Judges:

- **World-leading benchmark performance**
- **Clear value proposition**
- **Critical component for clock generation**
- **Depth and breadth of technical merit**
- **Commercialized as licensed I.P.**
- **Well presented with strong expertise and enjoys his field**

1.5.2 Publications in Refereed Journals

[c] Z. Bai, X. Zhou, R. Mason and G. Allan, "Low Phase Noise Clock Distribution Network using Rotary Traveling Wave Oscillators and Built-In Self-Test Phase Tuning Technique," *IEEE Trans. Circuits Syst. II*, vol. PP, issue 99, 2014.

[d] Z. Bai, X. Zhou and R. Mason, "A Low Phase Noise Injection Locked Rotary Traveling Wave Oscillator," *IEEE Trans. Circuits Syst. I*, invited journal paper submitted

[e] Z. Bai, X. Zhou and R. Mason, "A 2 GHz Injection Locked Rotary Traveling Wave Oscillator for Clock Distribution Network," *IEEE , J. Solid-State Circuits,* submitted

Chapter 2 : Different Clock Distribution Scheme Discussions

At the beginning of this chapter, the noise sources and noise coupling mechanism that affects the clock distribution networks are discussed. The on-chip noise decoupling and cancellation techniques are also explored. Next, the problems caused by the conventional clock buffering, such as high power consumption, are discussed. The proposed solution to these difficulties, the use of an injection-locked rotary traveling-wave oscillator, is also presented. Finally, the challenge of testing the circuit at its full design speed is treated, with a discussion on Built-In Self-Test (BIST) circuitry in the design of the project.

2.1 Noise coupling mechanism

Fig. 2.1 shows the noise coupling mechanism. Assume coupling occurs at a fast switching digital block (noise generator) and is received in a sensitive analog or RF block (noise receiver). The coupling occurs due to the capacitive and resistive nature of the substrate. This could result in significant degradation of the analog/RF blocks because of sharing the same substrate with the digital circuits. The substrate behaves essentially as a noise conduction medium. The analog/RF circuits could be built on separate substrates or glasses in order to minimize noise coupling between them, however, this increases cost [4], [5].

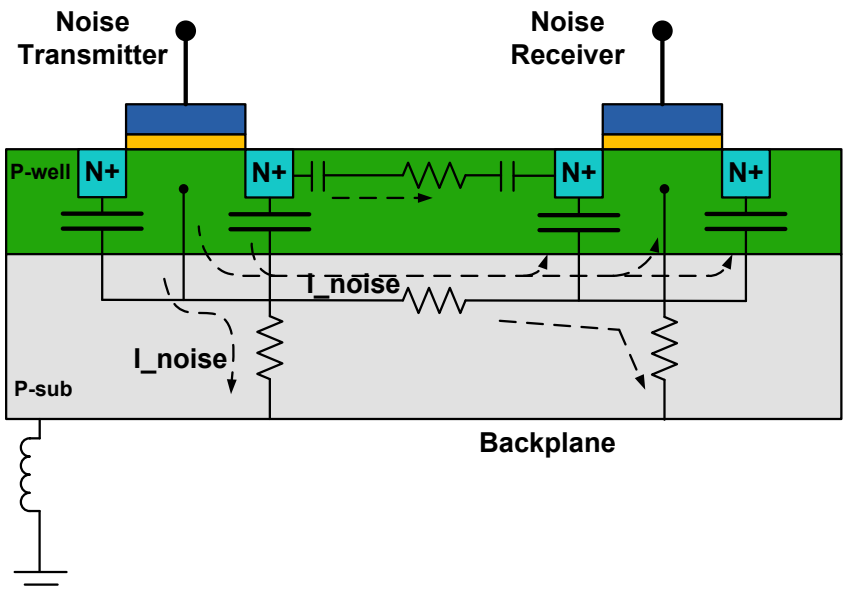

Fig. 2.1. Noise coupling mechanism [4]

2.2 Capacitive Injection

All the on-chip transistors are capacitively coupled to the substrate through their p-n junction depletion capacitance. Also, all the interconnections and routings have capacitance to the substrate and the result is capacitively coupled substrate current. In addition, the analog nodes can have high impedance. Therefore, the injection currents caused by large amount of digital circuits can have a significant effect on analog circuit performance [4], [5].

2.3 Inductive Noise

The power supply leads, package bonding wires and Printed Circuit Board (PCB) traces are inductive. These inductive components together with capacitively coupled substrate current can cause large glitches which can be expressed as $L*\frac{di}{dt}$ noise. Also, the

substrate inductance shown in Fig. 2.1 can aggravate the problem. Therefore, these inductive noises effect needs to be minimized in the design [6].

2.4 Power Supply Noise

The clock distribution delay variation is proportional to the distribution latency which depends on the number of buffer stages. Power supply droop caused by di/dt and power supply switching noise are two significant sources. Therefore, decoupling capacitors are used extensively to reduce the power supply droop and noise effects. Wong et al. [19] studied improving the processor timing margin by enhancing its immunity to power supply noise. This method compensates the clock delay against the data delay [19]. An all-digital dynamically adaptive clock distribution mitigates the impact of high-frequency supply voltage droops on microprocessor performance is discussed in [8], [9] [140] – [144]. The design integrates a tunable-length delay prior to the global clock distribution to prolong the clock-data delay compensation in critical paths during a supply voltage droop. In [10], the author uses an adaptive PLL concept to achieve optimal clock data compensation across a wide range of PVT and operating conditions. This was accomplished by an automated supply-noise sensitivity tracking loop which constantly monitors any timing errors occurring in a critical path replica circuit.

2.5 On-chip noise de-coupling and cancellation.

The power supply noise and substrate noise can be suppressed by using decoupling capacitors. Decoupling capacitance is implemented to attenuate noise coupling from one portion of a chip to another. Decoupling capacitance can transfer the power supplies' noise to nearby circuit and thus lower the peak current drawn across the

package inductance. The symmetrical decoupling capacitors are added to the chip in the design both to reduce the on-chip power supply noise and to satisfy the DRC metal density requirements [1], [7].

Another way to suppress power supply noise is by using a feed-forward noise cancelling technique in [11]. A further example is the deterministic crosstalk cancellation scheme for single-ended parallel receivers presented in [12]. However, these techniques increase the circuit complexity and require more design effort.

To further improve noise immunity, differential circuits are highly recommended over single-ended circuits in noisy environments [13], [99]. The noise appears as a common-mode signal on the differential outputs due to its random nature. Therefore, the differential noise signal is typically several orders of magnitude smaller than a single-ended implementation of the circuit. Therefore, the project designs differential circuits that have a higher degree of immunity to common mode noise.

2.6 Clock Skew and Uncertainties

In addition to noise signal due to the above sources, clock skew and clock uncertainty must be addressed. In order to illustrate the concept of clock skew and clock uncertainties, the concept of clock duty cycle needs to be defined first. Duty cycle is defined as the relative percentage of the clock high phase time versus clock period. The clock duty cycle distortion is subtracted directly from the total available clock period. Cycle based sequential designs using edge-triggered flip-flops are more immune to clock duty cycle distortion. Therefore, the single edge triggered flip-flops will be used in this

project to maximize digital circuit speed and provide more immunity to clock duty cycle distortion.

2.7 Static and Dynamic Clock Uncertainties

Clock uncertainties can be divided into static uncertainty and dynamic uncertainty. Static uncertainty varies very slowly with time which can be explained by on-die process variations, power supply and temperature variations, and the crosstalk noise [15]. The dynamic uncertainty varies with time which is illustrated by the power supply induced delay variation. The sources of static and dynamic clock uncertainties are summarized in table 2.1. Static clock uncertainties can be tuned out by careful pre-silicon analysis and design. However, the pre-silicon analysis is time consuming and iterative.

A timing histogram will result as one of the clock edges is sampled repeatedly with an ideal reference signal. The timing diagram exists characterized by a mean value and peak-to-peak range as shown in Fig. 2.2. The difference between the mean of two consecutive edges is defined as t_{skew}. The single edge peak-to-peak difference is defined as t_{jitter}. It should be noted that t_{skew} is static uncertainty and t_{jitter} is dynamic uncertainty.

Table 2.1 Sources of static and dynamic clock uncertainties

Clock uncertainties	Sources
Static (clock skew)	On-die process variations and mismatches Loading variations and mismatches
Dynamic (clock jitter)	Voltage droop and dynamic voltage variations Temperature gradient Jitter due to the reference clock

The clock uncertainties introduced by the Process, Voltage and Temperature (PVT) variations, and the uncertainties caused by reference signal generator are all encompassed in the term "jitter". The voltage variation caused by digital switching circuits is the dominant source of the dynamic uncertainty. The power supply voltage droop and the reference clock jitter are common to the entire clock distribution path and impact the setup time constraint by modulating the clock cycle time. The temperature variation has a minor effect on clock skews as shown in Fig. 2.3 [15] based on survey results. The trend of clock jitter as a function of cycle time is shown in Fig 2.4. Minimizing the reduction of effective clock cycle time due to jitter is critical for performance reasons [15].

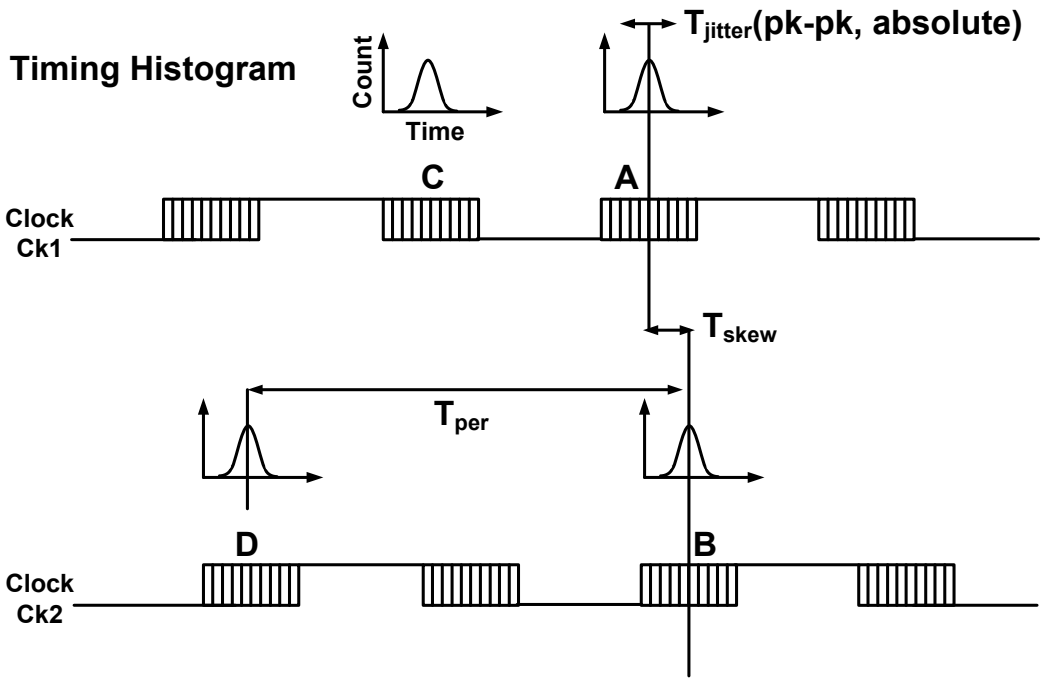

Fig. 2.2. Clock skew and jitter definitions [15]

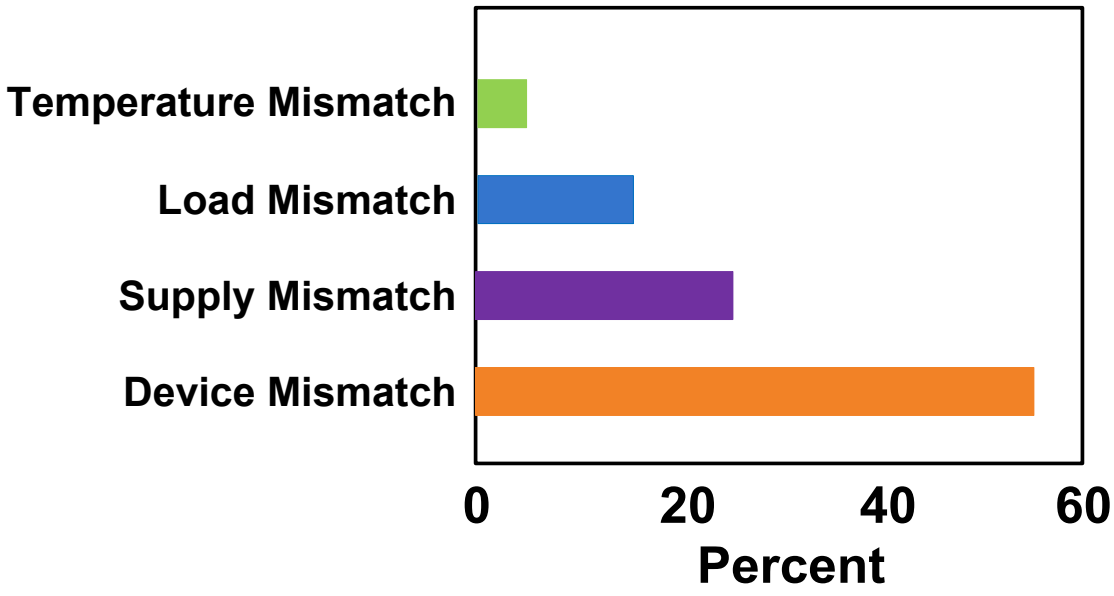

Fig. 2.3. Factors affecting clock skew [15]

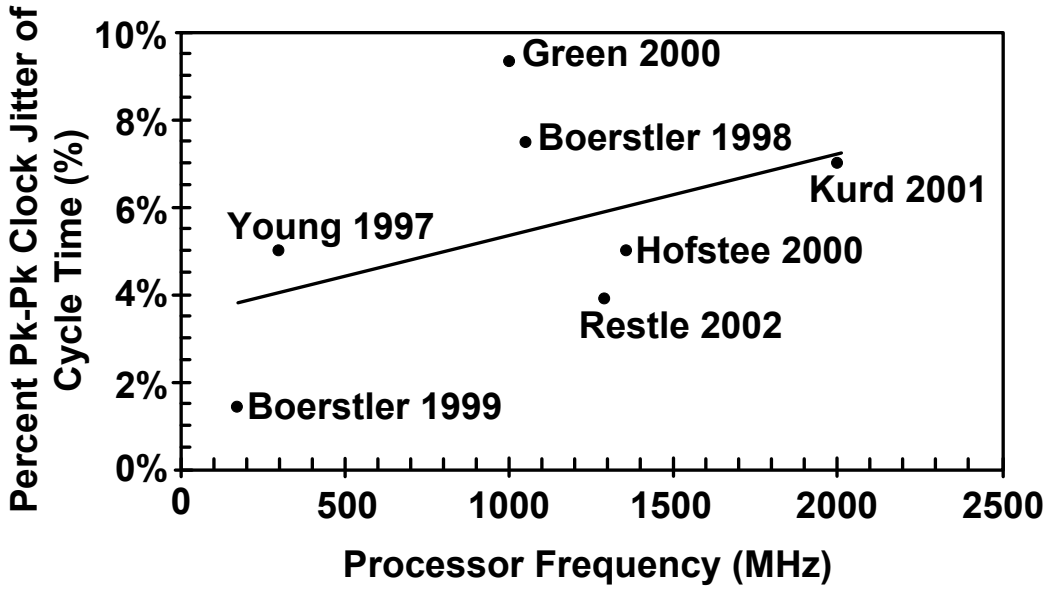

Fig. 2.4. Pk-pk clock jitter as a fraction of clock cycle time vs. processor frequency [15]

2.8 Periodic Clock Jitter

Period jitter, in particular, is the most important type of jitter in global clock distribution design which directly impacts the available time for logic operation in synchronized circuits. The power supply noise injected into the global clock drivers can worsen the timing margin of the critical path by modulating periodic jitter. It is critically important to differentiate and understand the impact of different design parameters on period jitter in the planning stage of global clock distribution. However, it is hard to achieve due to the complex relationship between different independent/dependent design parameters such as the power supply variations, clock driver size variations and mismatch, interconnects variations, number of buffer stages, temperature, process corners, etc [17]. Saint-Laurent and Swaminathan [18] presented an approximate model of delay variation in interconnect dominated paths. Wong et al. [19] formulated a period jitter expression based on a homogeneous delay line assumption. In the proposed design, the shortest clock period among all time varying clock period, the worst case period jitter, has been chosen as the maximum clock period to avoid timing failures.

2.9 Clock distribution scheme discussion

In a conventional clock distribution scheme, a single clock source is fed through hierarchies of clock buffers and interconnects as shown in Fig. 2.5a. However, the combination of high target frequencies and significant physical variations makes it very difficult to satisfy the strict clock skew requirements [20], [24] in modern VLSI designs.

Silicon photonics is a solution for on-chip optical clock distribution. The work in [72] developed an adhesive bonding process to integrate silicon nanomembranes onto

silicon chips. The single-mode strip waveguide was implemented and fabricated on adhesively bonded silicon membrane. A grating-coupled H-tree optical distribution is demonstrated. This optical distribution achieves an insertion loss of 13.9dB, and a 3dB bandwidth of 880GHz. An electro-optical system for an RF-clock distribution is presented in [73]. It achieves an added timing jitter of less than 10fs and a clock drift of 50fs RMS over 26 hours. The RF signal is distributed through a transceiver topology with intensity modulation on a 1,550nm coplanar wave. The work in [73] compensated the temperature and the vibration-induced fiber group delay by adjusting the wavelength of the laser and making use of the fiber chromatic dispersion. In [74], a novel clock distribution scheme using an optical null header (ONH) was developed. The ONH was inserted between the Optical Time Domain Multiplexing signal pulses with a repetition rate equal to the clock frequency. This enabled channel identification and fast yet robust clock recovery. The lower limit of the timing jitter in an optical clock distribution network due to shot and thermal noise using a realistic photo detector model is derived in [75]. The work in [76] explored the lower limit of timing jitter due to optical and thermal noise for the transmission of pulses as a clock signal. This paper analyzed clock distribution networks in silicon photonics by providing pulse trains to electronic circuits. The simulation results that study showed that multiple electronic circuits on a silicon chip can be synchronized by optical pulses with femtosecond precision. In [84], a new technique of injecting clocks optically onto CMOS chips without the use of a receiver amplifier is presented. The benefits of such a direct approach are discussed and the technique is experimentally demonstrated. In the same paper, the authors compare a receiver-less optical clock distribution and an electrical clock distribution in a fan-out-of-

four clock tree to evaluate the timing and power benefits of the optical approach for modern microprocessors. The receiver-less direct injection of optical clocks to trans-impedance receiver based injection are also compared within the same clock distribution network.

Meanwhile, reference [78] show experimental results of clock recovery from return-to-zero (RZ) format data by using injection locking of a free-running optoelectronic oscillator (OEO) circuit. The clock recovery performance at ~1.25 Gb/s is analyzed in terms of timing jitter, phase noise and locking bandwidth. Reference [79] developed an all-optical clock generation without a conventional clock recovery circuit and pulse source. This proposed circuit achieved low-power penalty operation in comparison with a conventional scheme.

These optical clock distribution methods might be commonly packaged in the future; however, they are not commonly used in today's commercial products. Special processing steps are required to bond these optical and photonic devices on silicon chips. Also, the processing technologies they used are not standard technologies. This results in significantly increased cost and makes the optical and photonic clock distribution techniques difficult to commercialize.

Modern micro-processors consist of billions of transistors which create large amounts of correlated digital noise. As clock frequencies increase, the digital switching noise, power supply noise and substrate noise are injected into the sensitive oscillator circuits degrading their performance and adding timing uncertainties [21], [24]. Loading mismatch and interconnections also increase the time uncertainties. Liu et al. [3]

observed that interconnect variations alone account for 25% of the deviation of the clock skew in a gigahertz microprocessor from its nominal value. Therefore, the clock tree distribution and interconnects have to be balanced accurately which requires a very stringent layout budget of the entire chip. Methods to design balanced clock distribution networks have been reported [28], but these methods result in zero skew only when there are no process, temperature, or supply voltage variations. However, the PVT variations and mismatch cannot be eliminated and result in greater clock skew challenges in more advanced technologies [25], [28]. There has been serious attention devoted to de-skewing clock distribution networks [146] – [148]. Nevertheless, it is very difficult to distribute a low-skew clock signal without skew reduction circuitry due to intra-die process variations [29].

Clock distribution delay (latency) is another key component that contributes to the overall clock uncertainties. A clock network has to rely on a series of clock buffers for gain and signal propagation in order to drive the final clock loading and to traverse the distances needed to reach the loads. In a modern processor, there might be more than 20 clock buffer stages. This can result in nanoseconds of latency [16]. Also, the skew and jitter variations will grow with the square-root of the number of distribution buffering stages. This formulation can be applied to any pair of clocks sharing a common point of clock divergence. The sum of the skew and jitter variation coefficients is between 5% and 10% for modern process technologies [15]. As a result, minimizing clock distribution latency is another primary design objective irrespective of the distribution topology [14]. It is obvious that more buffer stages introduce more clock skew and jitter; this situation deteriorates quickly with higher clock frequency. Also, skew and jitter reduction

techniques results in higher power consumption. Therefore, this research targets the development of a clock distribution scheme with less jitter and skew, resulting in less power consumption for a fixed target performance [8], [30].

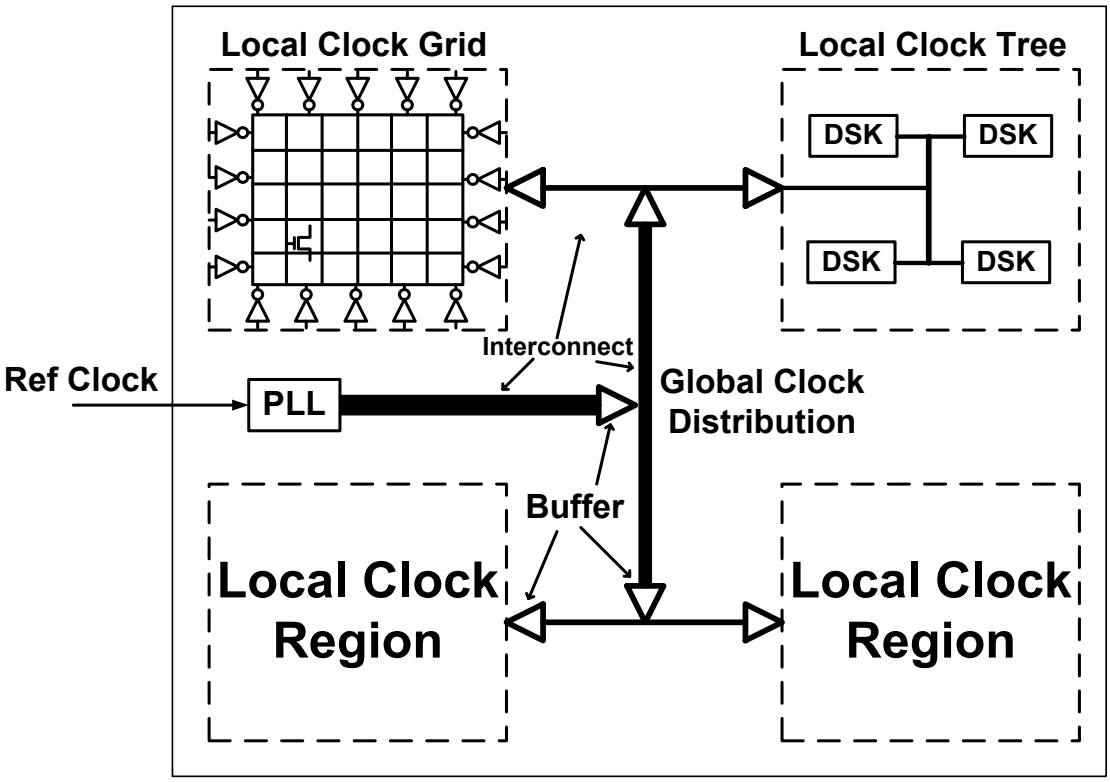

Fig. 2.5a. Conventional global clock distribution

The grid clock distribution technology that is also commonly implemented has much larger parasitic capacitance than the conventional clock tree as shown in Fig. 2.5a. A grid has a lower resistance than a tree between two end nodes, and hence can reduce the skew. However, all the interconnections and routings add substrate noise current due to parasitic substrate capacitance [21] - [23]. This results in increased power consumption and limits the clock speed. Passive and active deskew methods [31], [21], [26], [27] have

also been employed to compensate skew after chip fabrication. However, this results in increased chip complexity and manufacturing cost.

In addition, in order to reduce jitter, the interconnect wires in the global clock distribution network need to be well shielded from other noise sources, usually by sandwiching them between Vdd/ground wires and layers. Shielding inevitably increases the parasitic capacitance of the clocking network, which means more and larger clock buffers, and hence larger power dissipation to drive them. In turn, having more buffer stages introduces another source of jitter, and the situation deteriorates quickly with faster clock speed. For example, a 10th generation 16-core SPARC64™ processor for mission critical UNIX servers uses an H-tree clock distribution network with shield wires and achieves an average 20ps clock skew is shown in [32].

This type of approach becomes problematic when designing large-scale systems due to power consumption. However, power and process variations are two important factors that limit VLSI circuit performance [33]. The clock distribution network delivers the clock signal from the clock source to all the clock loads located over the entire chip. When chip dimension and clock load increase, conventional clock networks consume large amounts of power, which can be more than 20% of total chip power even with power reduction techniques [46]. This power is becoming increasingly significant as frequencies scale well beyond the gigahertz limits. Therefore, the design of low-power global clock distribution networks has become one of the major challenges for the IC industry [38].

The clock distribution network's power consumption is caused mainly by the frequent charging/discharging of loading capacitance and the power leakage through buffer stages. Different methods are proposed in [34]–[37] to reduce power consumption by minimizing clock network size. The clock gating methods are also implemented by switching off the inactive portion of the circuit to lower power consumption. An energy recovering scheme for 40% savings in clocking power with 40% driver active area reduction is demonstrated in [47]. In [48], the global clock system operates in a resonant-clock mode for energy-efficient operation over a desired frequency range and a conventional, direct-drive mode to support low-frequency operation. This dual-mode feature was implemented with minimal area impact to achieve both reduced average power dissipation and improved power-constrained performance. The solutions for integrating and optimizing the clock distribution and power consumption networks all the way to circuit level have also been investigated and proposed in [49]. However, these approaches are limited by the fundamental characteristics of charging/discharging power dissipation in conventional clock distribution network.

Techniques based on LC resonant oscillation have been proposed to further reduce clocking power which inserts inductors into the clock network to recover the energy lost during the discharging of the network. Chan et al. have recently proposed a resonant-load clock distribution technique that generates uniform-phase and uniform-amplitude clock signals [39]-[41]. However, the local clock distribution which contributes most clock power dissipation has not been addressed. A clock network with standing-wave oscillators is proposed in [42]. However, the clock amplitudes vary at different locations. Wood et al. have presented a resonant clocking scheme, called rotary

clock shown in Fig. 2.5b [43]. The RTWO has the unique property of sustaining a traveling wave while achieving low power and low phase noise [43]. The RTWO clock signal propagates along the ring without termination so that the energy is recirculated which reduces the charging/discharging power dissipation. Reference [44] shows rotary clocks can reduce power dissipation by 70% compared to conventional clock networks. The rotary traveling-wave oscillator implemented with differential linear transmission lines are implemented in [33] which enables the generation of square waves with reduced number of stages, while still maintaining the capability to produce multiphase signals. The RTWOs with different transmission line width and spacing have been implemented to optimize power consumption and minimize RTWO phase noise in [52]. The amplification stage limitations of RTWO are studied by [51] which demonstrated the relation between the frequency limit and the amplification stage [51].

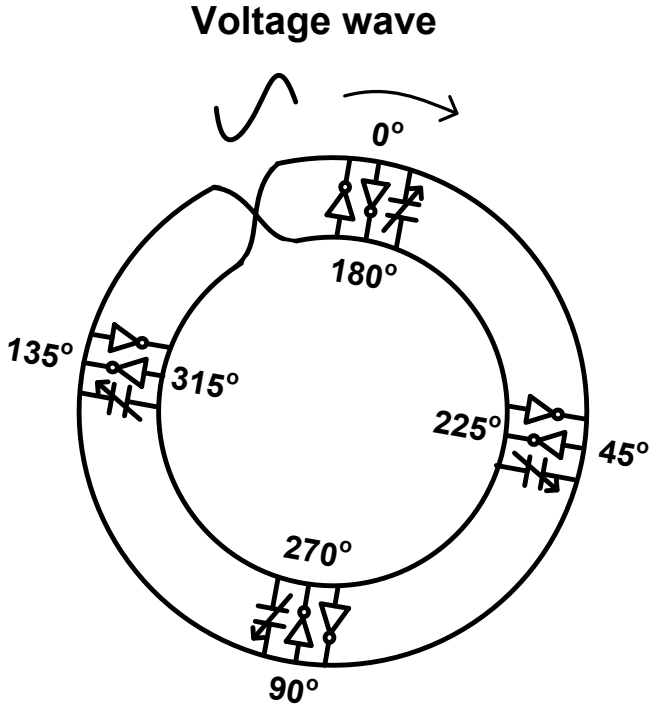

Fig. 2.5b. The RTWO schematic

The signal propagates along a transmission line in an RTWO; multiple-phase signals are easily available by tapping off the signals from different transmission line positions. Reference [53] reports an 18 GHz RTWO with I/Q outputs. Reference [54] achieves a 15/30 GHz dual-band VCO by using half-quadrature signals available from the RTWO. A 102 GHz Rotary Traveling Wave Oscillator is also implemented by tunable composite Right/Left Hand Transmission lines in [55]. An array of distributed oscillators for millimeter-wave phased-arrays combines LO generation and distribution, leading to a phase noise improvement that is proportional to the number of array elements as shown in [56]. The process variation sensitivities of Rotary Traveling Wave Oscillators are also explored in [57] which requires long interconnects with varying geometric shape segments on the chip. These prior works demonstrate the potential advantage of the RTWO for high frequency and low phase noise applications.

The novel low-jitter phase-locked clock generation and distribution methodology uses resonant standing wave oscillators (SWOs). Clock distribution is done by routing the resonant ring chip-wide in a "comb" like manner [58]. However, this work does not talk about the adjustment of phase and clock skews. A Ku-Band High Output Power Multiphase Rotary Traveling-Wave VCO in SiGe BiCMOS is discussed in [59], which explores a multiphase 18 GHz RTWO with eight different phases. However, this work did not talk about the phase error detection and calibration. The RTWO phase accuracy can be easily deteriorated due to the RTWO layout asymmetry and device mismatch. This limited the RTWO's practical usage. This is illustrated in the quadrature signal generation which requires less than 3° to 5° of phase resolution in modern wireless standards. Therefore, it is expected to achieve high phase resolutions in modern wireless

applications. This results in iteration in circuit design and a stringent layout budget [61]. In [60], a clock distribution network that emphasizes flexibility and layout independence is presented which mitigates the effect of intra-die temperature and process variances. However, it does not achieve a large phase tuning range and high phase tuning resolutions. In this research, a novel clock distribution scheme with Injection Locked Rotary Traveling Wave Oscillators (IL-RTWOs) is proposed. The non-uniform capacitor distribution, which controls the propagation speed of the traveling wave, is introduced to increase both the RTWO phase tuning range and fine-tune the RTWO phase. This new distribution scheme avoid many of the problems discussed above, such as the high power consumption, capacitance (with its potential to introduce noise) and timing uncertainty associated with large number of buffers. In addition, the RTWO injection points are phase synchronized by the external reference signal at the zero crossing points. There are however phase differences at the other tapping points due to process variations. These variations can be tuned out by adjusting the RTWO phase tuning words. This greatly simplifies the RTWO design as the routing does not have to be perfectly symmetric if the phase tuning can cover the overlap between the tapping points. Different RTWO tapping points are chosen using MUXs to increase the phase tuning range.

2.10 Overview of Injection locked oscillators

Injection locking is a special type of forced oscillation. If a large enough periodic signal is injected into an oscillator, then it will "pull" the oscillator to that frequency. Studied by Adler [67], Kurokawa [68], and others [69]–[71], these effects have found increasingly great importance since they manifest themselves in many of today's frequency synthesis techniques. Injection locking can be useful in a number of

applications which require high efficiency integer frequency synthesis, including frequency division [163], [164], quadrature generation [165], [166], clocking networks for high frequency data converters [152] and oscillators with fine phase resolutions [116]. Low phase noise frequency multiplication can be achieved with this technique by using a low noise reference signals to sub-harmonically injection lock a free running oscillator.

The injection locking phenomenon has been studied by mathematicians and scientists [77]–[80]. The oscillator injection locking range, also called synchronization range, is commonly described by a frequency range across which injection locking holds. This range is a function of the oscillator circuit parameters, as well as, the relative power or amplitude of the synchronization signal. If the frequency of the synchronization signal (or one of its harmonics) is placed inside the oscillator synchronization range, the oscillator is said to be injection locked. This results in the oscillator frequency becoming locked to the injection signal or its harmonic.

Frequency multiplication has been realized by several different architectures [81]–[83]. Low phase noise, high frequency oscillators can be achieved with this technique by using high Q and low noise reference signals to sub-harmonically injection lock a free running oscillator. Due to the weak injection signal and its limited locking range, the oscillator free running frequency needs to be fine-tuned to be close to the sub-harmonic of the reference signal for the successful injection locking.

2.11 Overview and Motivations of Built-In Self-Test Implementation

To determine whether a circuit, such as a clock distribution network, is functioning properly, it must somehow be tested. However, this can be problematic with

circuits operating at ever-higher frequencies. This section discusses some of the problems with testing an RTWO-based clock network and the proposed built-in self-test implementation, which aims to overcome these difficulties.

Automatic Test Equipment (ATE) speeds have always lagged Circuit Under Test (CUT) speeds. Therefore, high-speed circuits are tested at a much lower speed than their design specifications [89], [90]. It also should be considered that the pin and probing limitations of ATEs limit the test result's accuracy. Therefore, an on-chip test mechanism is highly desired to fulfill the at-speed testing requirement of complex SoCs. In addition to the test challenges, achieving and validating circuit performance is becoming more difficult.

With manufacturing processes progressing into finer geometries, various factors in the fabrication process will cause considerable deviation from the nominal circuit behavior. The performance of an integrated analog/RF circuit is more susceptible to the effects of process variations, noise coupling, and temperature fluctuation. However, the above factors are very difficult to consider or model due to their probabilistic and environment-dependent nature. Therefore, violation of noise margin appears on long interconnects which can only be verified using on-chip approaches. As the chip complexity and frequency increase, it is becoming more difficult to achieve an adequate interconnect test using current techniques. Signal integrity is often degraded as a signal travels through an interconnection. This results in integrity loss and leads to functional error and reliability loss. In order to avoid signal integrity loss, more design margin is required. This, however, means larger area, more power and more redundancy [16].

Several RF BIST functions are feasible with the all-digital transmitter and digital receiver as illustrated by [91]. For example, an all-digital defect-oriented testing of a PLL is described in [92]. An on-chip jitter analyzer of a PLL is described in [93], which uses large additional area. An on-chip implementation of the phase trajectory error analyzer in a frequency-shift keying (FSK) transmitter is reported in [94]. The phase error between demodulated RF output and reference input are measured, where the BIST circuit also adjusts the PLL loop gain via charge pump current. However, the case of this approach is a significant amount of additional circuitry. [95]

The rising cost of fast automated test equipment and growing integrated circuit complexity requires the application of Built-In Self-Test (BIST) techniques [96]. Various compensation and calibration needs are performed by the SoC internally and independently. Also, the test could be done at the simulation stage before the chip is actually fabricated. The external test equipment requirement is reduced which lowers the test cost. In addition, different test structures can be built on the same chip, allowing better fault coverage. However, the BIST increases the complexity of the circuit design. The extra BIST circuit together with its related pins requires additional on-chip space which also needs to be considered. Furthermore, it takes time to debug the BIST circuit in the measurements. The flexibility of the BIST circuit needs to be carefully considered in the design stage.

2.12 BIST Design Prototype

This research also strives to develop a purely digital Built-In Self-Test (BIST) circuit to detect clock skew which will be eliminated by phase tuning an Injection

Locked- RTWO (IL-RTWO). The proposed high level BIST block diagram is shown in Fig. 2.6, a TPG (test pattern generation) circuit generates the pseudorandom patterns to stimulate possible defects in the CUT. This design will employ a Pseudo Random Pattern Generator (PRPG) to generate test patterns that are applied to the device's internal scan chain. An ORA (output response analyzer) circuit observes the outputs and analyzes their validity. A multiple input Signature Analyzer (SA) will be applied for obtaining the syndrome to these input patterns in the proposed design. An incorrect SA result indicates a defect in the test circuitry which is discussed in the next session. Using inexpensive built-in noise and skew detection cells we will offer efficient on-chip architecture to capture and scan out the occurrences of noise and skew violations. The test result is checked by the skew detector. The detected skew messages are sent to the micro-controller. The micro-controller is used to adjust the clocks and de-skew the circuit under test and send another random test pattern to confirm whether the de-skew was successful or not.

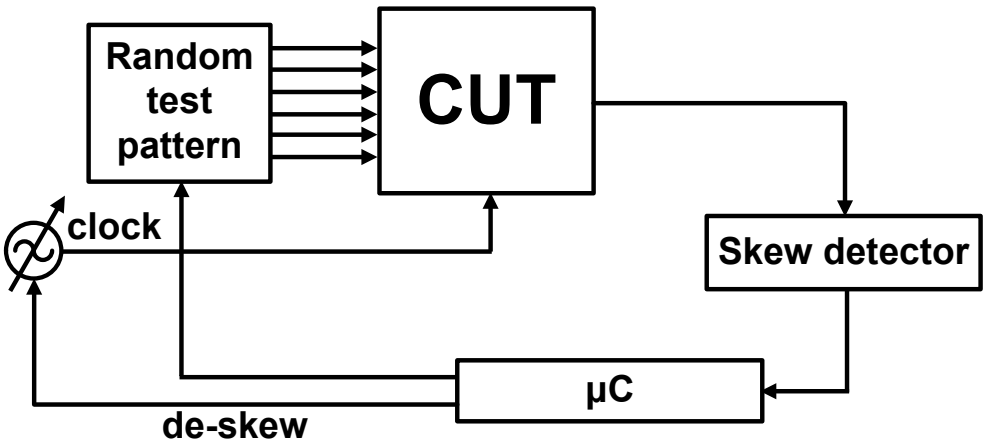

Fig. 2.6. BIST circuit prototype

Chapter 3 : Design of Injection Locked RTWO with BIST

This thesis proposes a scalable and efficient frequency multiplication technique that synthesizes a multi-phase clock with finely adjustable output taps. It uses an Injection Locked-Rotary Traveling Wave Oscillator (IL-RTWO) with switched capacitors and Complementary Varactor Pairs (CVPs) to achieve a 1.7 GHz to 2 GHz tuning range and to implement the fine phase adjustment. For each tap, the RTWO phase tuning range and worst case resolution are 58° and 0.34° respectively. Locked to a clean 679 MHz reference, it has a phase noise performance of -132 dBc/Hz at 100 kHz offset from 2.039 GHz. It achieves a single sideband integrated rms jitter of 39 fs from 1 kHz to 40 MHz offset, for a $Jitter^2$*Power Figure Of Merit (FOM) of -253 dB. The proposed injection locked RTWO is much simpler and has better jitter performance than a Phase Locked Loop. The excellent jitter capability is an enabler for high performance applications such as next generation (400 Gbps) SERDES systems, and high performance data-converters [152]. In addition to reducing the power consumption, the reduced number of global clock buffers results in reduced sensitivity to of power supply noise. Therefore, less jitter is generated and accumulated in the clock network. In mixed signal ICs, the clock challenges are even more severe, where 1 ps skew budget may be required to clock a high performance DAC array or parallel ADCs [167]. Additionally, the clock can be both a victim and an aggressor against sensitive analog signals. As a result, the proposed architecture has a number of applications in both digital and mixed-signal Integrated Circuits (ICs) which require low-power, multi-phase output clocks of very-fine precision. Some examples include phased arrays [116], interleaved data-converters [152], [153], high speed SERDES [156], high performance microprocessors [154] and other digital systems [155].

This proposed architecture focuses on the following three aspects: First, the implementation of injection locking on RTWOs attains efficient frequency multiplication with low additive noise, low integrated rms jitter and low FOM. The measured phase noise, integrated rms jitter and FOM are superior to other reported works in this frequency range and scale well to finer process nodes. The phase noise is limited by the phase injector circuit and the overall RTWO tank Q. The second aspect of the project discusses the application of Vernier type digitally controlled Complementary Varactor Pairs (CVPs) on RTWOs to minimize the unit switchable capacitance without introducing dithering spurs, thus increasing the frequency and phase tuning resolution without sacrificing phase noise. This increased frequency resolution enables the RTWO free running frequency to be close to the injection frequency, which requires less current to achieve injection locking. The implementation of injection locking and CVPs on RTWOs has only been explored in [115]. This increased frequency resolution can also be used to fine tune the oscillator output phase while at the same time providing wide built-in de-skew range. Third, this thesis also describes a Built-In Self-Test (BIST) technique used to verify and tune the timing integrity of a clock distribution system implemented with Injection Locked Rotary Traveling Wave Oscillators (IL-RTWOs). The BIST circuit allows testing of the integrity of the clock distribution system at speed by determining if the system clock skew can be tolerated or needs adjustment. The clock deskew is achieved with the phase tuning characteristics between different clock domains. The proposed injection locking scheme enables the architecture to relax the clock skew and jitter performance requirements in multi-GHz micro-systems. In addition, the entire injection locked clock distribution network together with its BIST circuitry are scalable

and will benefit at higher clock frequencies. The implementation of this BIST technique to determine clock integrity of an injection locked clock distribution network and the application of CVPs and injection locking techniques on RTWOs have not been explored previously.

3.1 Injection Locked RTWO with BIST scheme

With increasing SoC data rates, clock jitter is emerging as a problem in the latest digital systems, which must deal with increased crosstalk, process variations, coupling noise, etc. [149], [150] as discussed in Chapter 2. Measuring the clock jitter using external or internal high-speed test equipment is becoming increasingly difficult and expensive. These are challenges in urgent need of solutions.

To this end, this research strives to develop a purely digital Built-In Self-Test (BIST) circuit to detect clock skew which will be eliminated by phase tuning an Injection Locked- RTWO (IL-RTWO). The proposed IL-RTWOs attain particularly low inband phase noise. The incorporation of the BIST circuits takes advantage of on-chip communications to detect clock skew. The BIST circuit does not rely on external test equipment and allows the chip to be tested more easily and efficiently.

The injection locked clock distribution scheme with BIST is shown in Fig. 3.1. The proposed RTWO clock distribution network is intended to be used for global clock distribution. A local clock mesh is required within each RTWO as shown in Fig. 3.1. A low frequency clock is used instead of a conventional high-speed clock to drive the global clock network, with the high frequency clocks generated locally [30], thus reducing the top level buffers on the global clock distribution path. Compared to

conventional clocking based on balanced H-tree and grid structures, this scheme enables local clock domains to have higher (nf_0) clock speed than the global clock (f_0). This result in significant improvements in terms of power consumption, clock skew, and jitter [30].

The proposed clock scheme takes advantage of a simple ILO circuit instead of multiple power-hungry PLLs for frequency multiplication. In conventional clock distribution schemes, the global clock signal needs to be driven from rail to rail throughout the whole network in order to minimize jitter. This results in more buffers to be inserted into the clock network and increases power consumption. The proposed ILOs can achieve low jitter with small input signal amplitude. This further reduces the number of clock buffers required on the global tree and result in better jitter performance and less power consumption [30]. The reduced amount of deskew buffers also reduces their vulnerability to power supply noise. Therefore, less jitter generation and accumulation appears in the clock distribution network.

This reduced amount of jitter allows more timing margin for clock recovery of a faster clock speed. The improvement in jitter and skew can also be used to allow the logic circuit to operate at a lower power supply and reduce power dissipation from all the logic gates for a given design specification [30]. More importantly, IL-RTWOs provide a built-in mechanism for deskew. Because of the built-in deskew capability of IL-RTWOs, it can be expected that an injection-locked clock tree has much more freedom in its physical design (i.e. layout). The benefits will become more evident as future processors incorporate more and more cores.

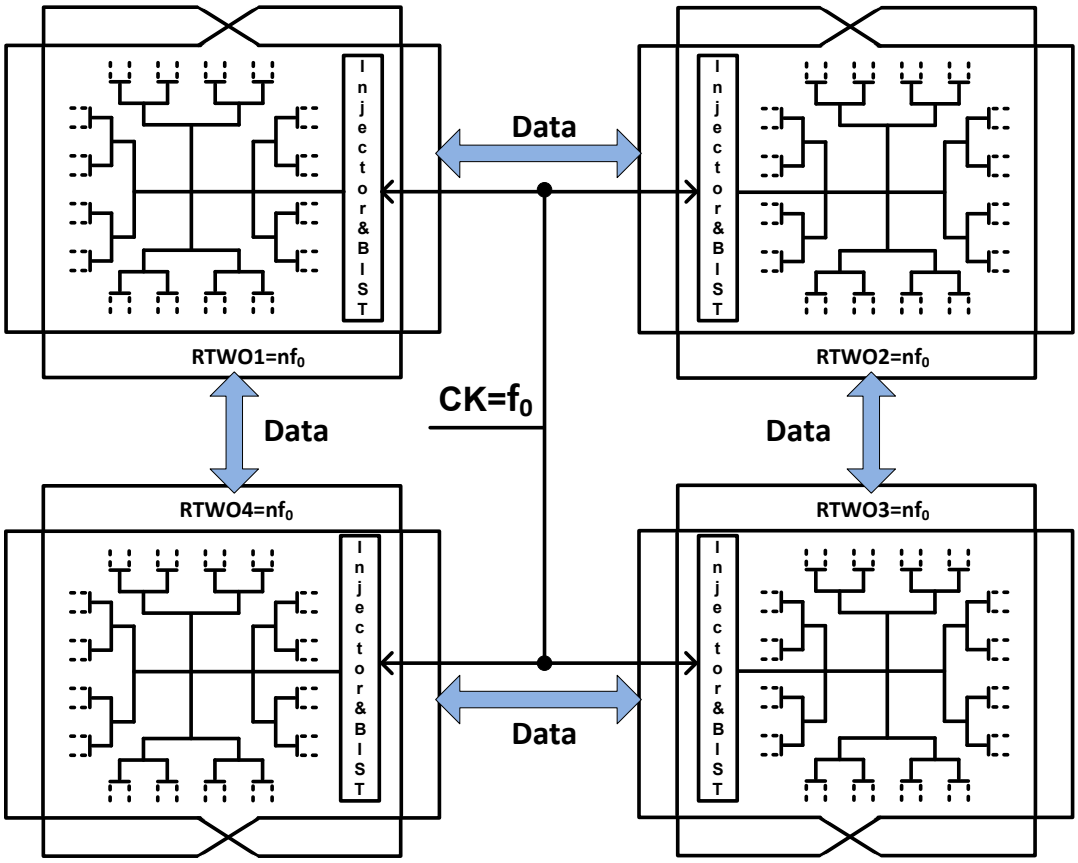

Fig. 3.1. The injection locked clock distribution scheme with BIST

3.2 The RTWO Design

The RTWO will be implemented with 16 rf-line stages. The rfline device with an accurate high frequency model is supported by IBM 130 nm technology. It is used as an inductive element for applications requiring low inductance and high quality factor. The rfline consists of the topmost MA layer in parallel over BFMOAT (P-substrate). The ground plane of the model needs to be connected to an RF ground rather than the substrate. The width of the transmission line ranges from 4 mm to 25 mm. The transmission line length ranges from 100 μm to 1,500 μm. Two or more short transmission lines are required to connect in series if a longer line is desired. The 16 rf-

lines form a folded differential transmission line loop to save space and achieve symmetry. The RTWO period is the time the wave spends traveling through the differential transmission line loop. Inverter pairs are connected back-to-back and attached to the RTWO ring to compensate for the energy loss and sustain the oscillation as shown in Fig. 3.2. When the power supply is on, a voltage wave begins to travel either clockwise or counter clockwise around the loop. The rotation direction is determined by the path that has lower impedance at the beginning of the oscillation [13], [99]. Large size inverter pairs increase the driving power, but also increase the oscillator load. Therefore, the size of inverter pairs needs to be optimized.

The RTWO is a pseudo differential structure. The digital switching noise will appear as a common mode signal on the RTWOs' inverter pair inputs but its effect will be greatly reduced by the low common mode gain of the inverter pairs. Also, the digital switching noise will appear on the power supplies of the RTWO's, however, they will only affect the phase noise at the zero crossing points of the RTWO's inverter outputs. The RTWO resonator can sustain high frequency harmonics due to the implementation of its inverter pairs and microstrip lines. The RTWO outputs are fast rail to rail square wave signals with fast slew rates and small zero crossings times. This results in reduced phase noise as shown in reference [63]. The above factors significantly reduced the influence of digital switching noise on the phase noise performance of the RTWO. Therefore, digital blocks can be placed near or inside the RTWO and the separation space required between the sensitive analog components and digital blocks is greatly reduced [97]. An RTWO provides access to any phase of gigahertz-rate square waves with uniform amplitude and low jitter along the complete closed path of the loop. This provides

another advantage because the RTWO output signal amplitudes are the same over the entire loop. For an LC oscillator, the signal amplitudes vary at different locations [61]. In addition, the large on-chip inductor is replaced by higher Q and low power consumption rf-lines [101], [102].

3.3 Proposed RTWO Injection Locking Techniques

Injection locking is a special type of forced oscillation. If a large enough periodic signal is injected into an oscillator, then it will "pull" the oscillator to that frequency. In the proposed design, the reference injection signal is running at 615 MHz ± 50 MHz and its fifth harmonic will be injected into the oscillator. Both the traditional trans-conductance injector and the novel narrow pulse width injector are implemented on this chip as shown in Fig. 3.2 and Fig. 3.3. Since the oscillators are injection locked with one of the odd harmonics of the injection source, its phase noise performance within the locking bandwidth is dictated by the injection source. The estimated phase noise degradation is 20logN where, $N = \omega_{o,i}/\omega_{ref}$, $\omega_{o,i}$ is the injection locked frequency and ω_{ref} is the frequency of the injection source [103].

The RTWO injection points are also phase synchronized by the external reference signal at the zero crossing points. Given approximately equal geometric tapping points around the periphery of the ring, it is possible to get many phases of the clock signal [25]. Multi-phase clocks are common requirements in systems, where they may be used for edge combination /multiplication [152], phase interpolation [153], multi-phase logic [97], etc. Due to process variations, layout differences, and/or on-chip gradients (both static and dynamic), there will be inevitable unintended offsets between the various clock

phases around the loop. These variations can be tuned out by adjusting the RTWO phase tuning words. This also greatly simplifies the RTWO design as the routing does not have to be perfectly symmetric if the phase tuning can cover the overlap between the tapping points. Different RTWO tapping points are chosen using MUXs to increase the phase tuning range.

3.4 Trans-conductance injection locking technique

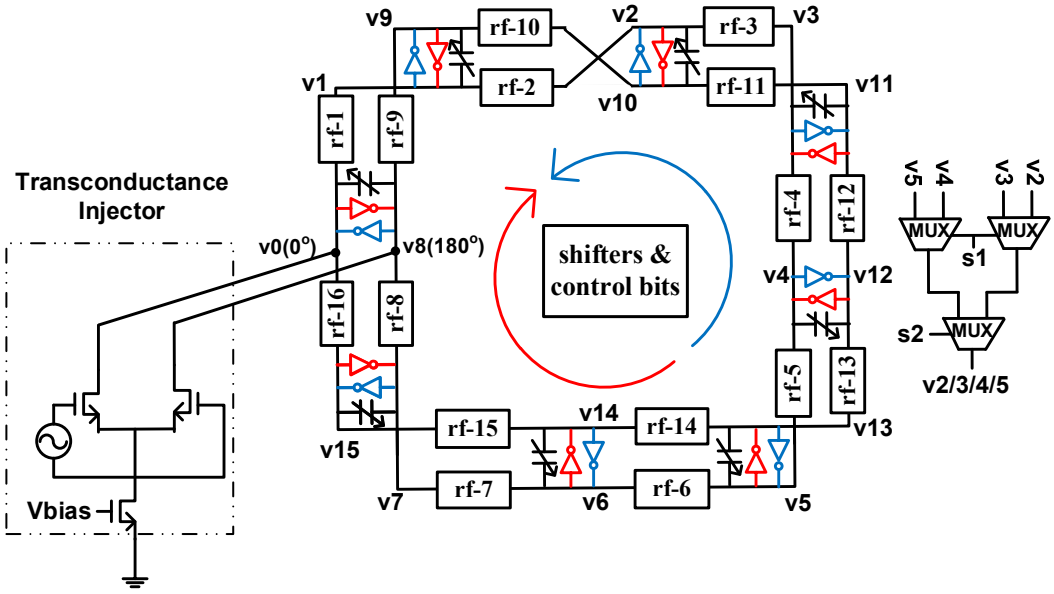

Fig. 3.2a. The RTWO with trans-conductance injector

The differentially connected trans-conductor [104]-[109] is employed to provide the desired odd harmonic and is operated in the strong inversion region. The differential input voltage is converted to a current by the transconductor and fed directly into the RTWO core (v0 and v8) as shown in Fig. 3.2a. The transconductor transistors are sized to provide sufficient injection current while minimizing RTWO loading and power consumption. When the RTWO output swing is close to the mid-rail, both transconductor transistors are open. Therefore, they both can inject current into the RTWO. However,

this time window is short, therefore, the differential transistors are sized to provide sufficient injection current and locking bandwidth while minimizing RTWO loading and power consumption. The RTWO is biased at only half supply voltage (~750mV) at the zero crossing points. This can make it difficult to maintain strong inversion operation, especially when lower power supply voltages are offered in more advanced processes.

3.5 Pulse injection locking technique

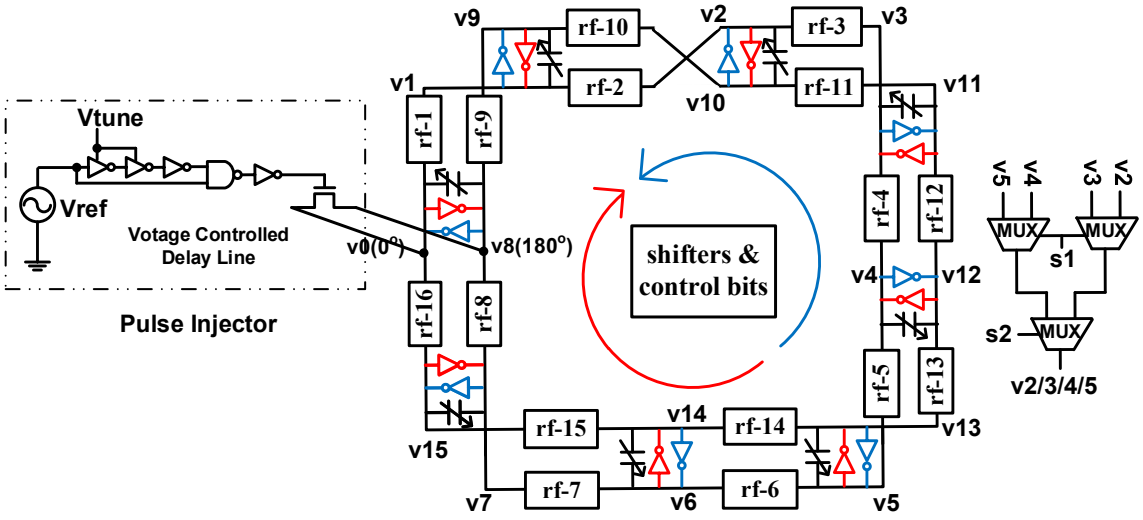

Fig. 3.2b. The RTWO with pulse injector

The pulse injection locking technique is achieved using a pulse injector that contains a Voltage Controlled Delay Line as shown in Fig. 3.2b. The injection pulse is generated by a pulse generator circuit where the pulse width is controlled by a voltage controlled delay line. The pulse is injected into the RTWO tank through the drain and source of an NMOS switch placed across the RTWO differential outputs.

A large NMOS shorting switch increases the injection current strength at the expense of increasing the loading on the pulse generation circuit and therefore increases power consumption, as well as, the rise and fall times of the pulse signal. This lowers the average tank Q which increases RTWO phase noise and power consumption. The injection power at a certain harmonic is a function of both the pulse width and its rising and falling times. Therefore, the shorting switch transistor size needs to be optimized.

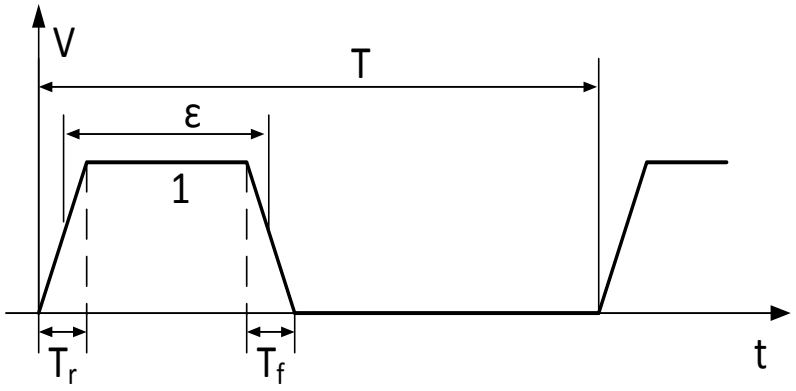

Fig. 3.3. A Real time domain waveform f(t)

In order to capture the impact of finite rise/fall- time and duty cycle on the magnitude of the constituting harmonics of a non-ideal square wave f(t), a trapezoidal wave such as Fig. 3.3 is analyzed. Its amplitude is normalized to 1V to facilitate the

theoretical analysis. The square wave has an effective pulse width of ε in period T, with the rise- and fall- time of Tr and Tf, respectively. Relying on the Fourier transform calculation of its second derivative as Appendix A, the Fourier Transform of the non-ideal square wave f(t) is derived as

$$F(j\omega) = \frac{1}{(j\omega)^2} H(j\omega) = \varepsilon e^{-jn\omega_0 \frac{\varepsilon+\delta}{2}} \frac{sin\left(\frac{n\omega_0\delta}{2}\right)}{\frac{n\omega_0\delta}{2}} \frac{\sin\left(\frac{n\omega_0\varepsilon}{2}\right)}{\frac{n\omega_0\varepsilon}{2}}$$

$$= \varepsilon e^{-jn\omega_0 \frac{\varepsilon+\delta}{2}} sinc\left(\frac{n\omega_0\delta}{2}\right) \operatorname{sinc}\left(\frac{n\omega_0\varepsilon}{2}\right)$$

where we assume $\delta = T_r = T_f$ for simplification.

Then, the n^{th} harmonic amplitude or coefficient of Fourier series derived from one period Fourier Transform is

$$C_n = \frac{1}{T} F(j\omega) = \frac{\varepsilon}{T} e^{-jn\omega_0 \frac{\varepsilon+\delta}{2}} sinc\left(\frac{n\omega_0\delta}{2}\right) \operatorname{sinc}\left(\frac{n\omega_0\varepsilon}{2}\right)$$

And due to $\omega_0 = 2\pi f_0 = \frac{2\pi}{T}$, the n^{th} harmonic coefficient is given as

$$C_n = \frac{1}{T} F(j\omega) = \frac{\varepsilon}{T} e^{-jn\pi \frac{\varepsilon+\delta}{T}} sinc\left(n\pi \frac{\delta}{T}\right) \operatorname{sinc}\left(n\pi \frac{\varepsilon}{T}\right)$$

$$\Rightarrow \quad C_{n\_real} = \frac{\varepsilon}{T} \cdot \cos\left(-n\pi \frac{\delta+\varepsilon}{T}\right) \cdot sinc\left(n\pi \frac{\delta}{T}\right) \cdot \operatorname{sinc}\left(n\pi \frac{\varepsilon}{T}\right)$$

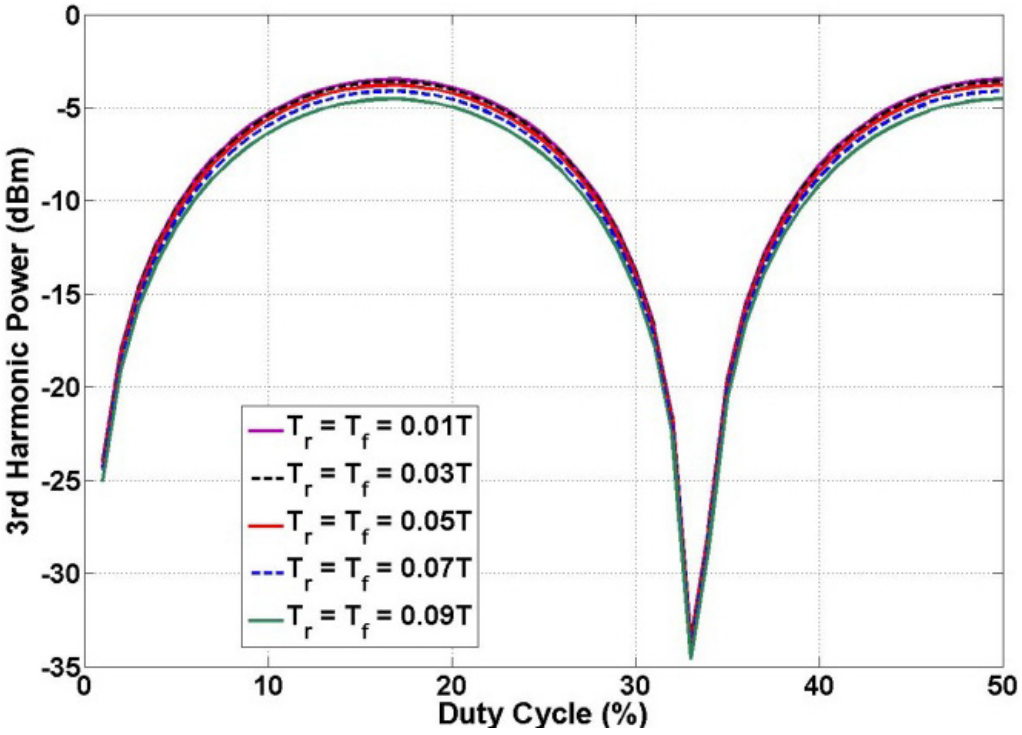

Fig. 3.4. Third harmonic power versus fundamental power

In this design, the duty cycle of the pulse injection circuit was adjusted to maximum injection harmonic power. Fig. 3.4 depicts the 3rd harmonic power of the Fourier coefficient as a function of the normalized rise/fall time and duty cycle. The 3rd harmonic power has been calculated relative to the nominal time domain waveform whose amplitude swing is 0V - 1V. The rise/fall time and duty cycle are normalized relative to the period of the fundamental (T). Fig. 3.4 shows that the 3rd harmonic power reaches its peak (~4dB attenuation) for approximately 18% duty cycle and 1% rise/fall time. It is interesting to note that the 3rd harmonic power does not change significantly for rise/fall times that are less than 10% of the duty cycle. Therefore, the tunable pulse width can be adjusted from 10% to 15% of the reference signal duty cycle depending on the injection locking requirements.

When the switch is turned on, the tank nodes are shorted and very little current passes through the tank. This reduces the residual phase shift errors which are present when using transconductor injection technique [110]-[113]. The transconductance injector discussed in section 3.3 suffer from process and mismatch variations; as a result, this shorting method discussed in this section tends to have better immunity to the supply and substrate noise and better phase noise performance [110]-[113]. The pulse injection technique offers another advantage in that it avoids the DC biasing problem associated with a differential transconductor and low supply voltage.

3.6 RTWO Frequency Tuning

The oscillator free running frequency is tuned using a 7-bit binary controlled high Q switched MIM-cap bank and 45 groups of low capacitance digitally thermometer coded Complementary Varactor Pairs (CVPs) as shown in Fig. 3.5. These MIM-caps and CVPs can also be used for phase tunings. The combination of large binary controlled MIM-caps and smaller thermometer coded varactor pairs supports a wide tuning range and excellent frequency resolution while maintaining high Q. In this 130nm CMOS IBM technology, the minimum MIM-cap value is 60fF and it is subject to a large relative process variations. For this design, 127fF capacitors were chosen as the smallest MIM-cap to achieve good matching. The CVPs are employed for medium, fine and ultra-fine frequency tunings.

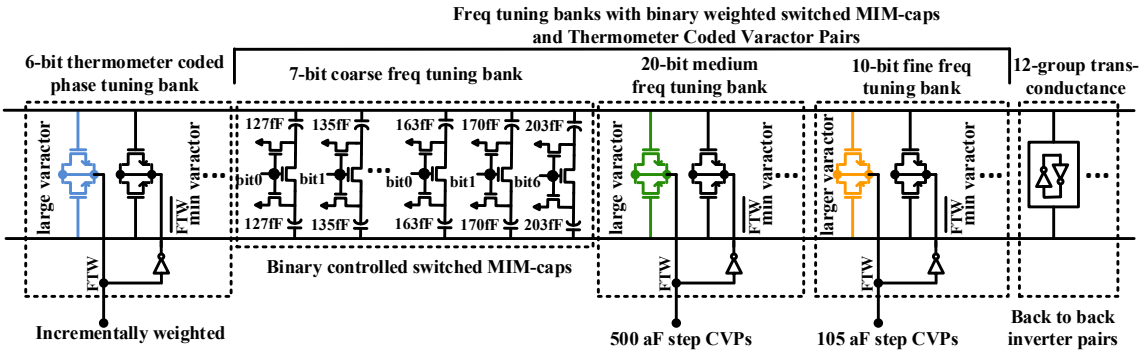

Fig. 3.5. The frequency and phase tuning banks for single rf-line stage

The MIM-caps are switched in and out of the circuit by changing the digital control bits. The equivalent capacitance is roughly proportional to the MIM-cap area. Therefore, it is not the W/L ratio, but the W×L product that is important [132]–[139]. The coarse tuning band has a tuning range of 300MHz and a frequency resolution of 1.7MHz. The coarse tuning MIM-caps are implemented with incrementally weighted MIM-caps (127fF, 135fF, 143fF, … 163fF, 170fF, 203fF) and these MIM-caps are binary controlled.

The RTWO oscillation frequency f_0 is calculated as [63]

$$f_0 = \frac{1}{2N\sqrt{L_{diff}C_{diff}}} \qquad (3.1)$$

where L_{diff} and C_{diff} denote the lumped inductance and capacitance of each of the N segments [61], [63]. The frequency step size can be expressed as:

$$\frac{df_0}{dC_{diff}} = -\frac{1}{2N\sqrt{L_{diff}C_{diff}}} * \frac{1}{2C_{diff}} = \frac{\Delta f}{\Delta C} \qquad (3.2)$$

where Δf is the frequency step size, ΔC is the ultra fine tuning delta capacitance. To achieve a 20kHz frequency resolution, the thermometer coded varactor step size is calculated by (3.3):

$$\Delta C = \left| \frac{-\Delta f}{f_0} * 2C_{diff} \right| = 15aF \qquad (3.3)$$

where f_0 is the nominal frequency. Therefore, the 12aF step capacitance achieved in the next session (session 3.7) should be small enough to satisfy the target 20kHz frequency resolution.

3.6.1 Adjust the RTWO Free-Running Frequency under PVT Variations

The RTWO free running frequency can be tuned with an on-chip micro-processor as shown in Fig. 3.6 [104]. The basic approach is to use a subsampling switch to mix the free running frequency down to a low frequency and measure it with an ADC. When the free running frequency is an exact harmonic of the crystal frequency the mixed down signal will be at DC. The free running frequency is measured using the ADC output and μP and then the μP adjusts the free running frequency by controlling the CVPs of the oscillator. This approach only requires a simple switch, low resolution ADC and basic 8 bit μP which will require very little space using an advanced CMOS process. The free running frequency is tuned at startup which eliminates any process variations from chip to chip. Normally, the oscillator would not require tuning for temperature and voltage variations as these can be accommodated by the wide locking bandwidth of the oscillator which was measured at 15MHz for oscillators on our test chip. If desired, a temperature sensor and/or supply voltage sensor could be put on the chip and read by the μP which

could then adjust the CVP's of the oscillator either based on frequency readings done during testing or using the tuning circuit in Fig. 3.6. For the latter case, the injection locking would need to be disabled momentarily to tune the free running frequency. The tuning algorithm and the complete SOC transceiver presented in [104] have been commercialized and is now in mass production and being used for both commercial and automotive applications.

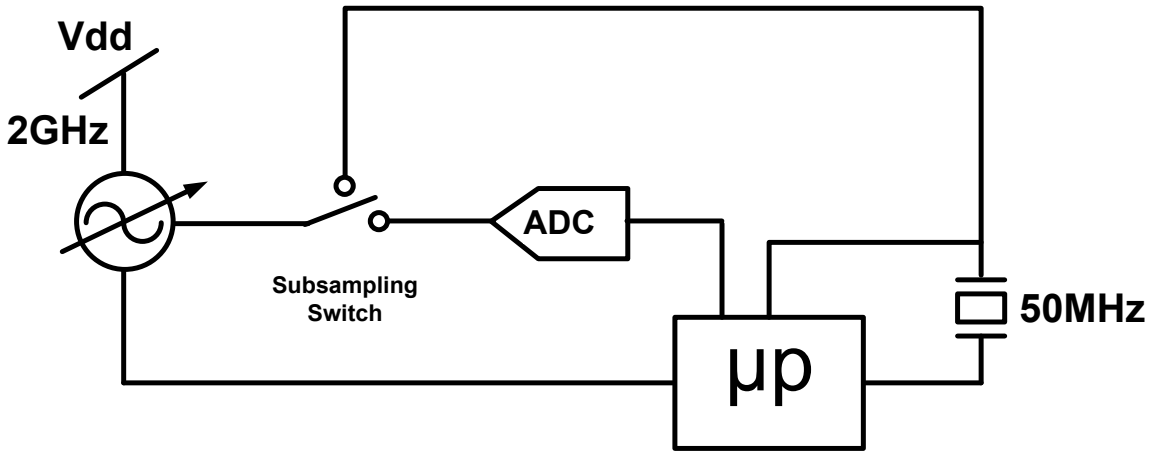

Fig. 3.6. Oscillator Free Running Frequency Tuning Algorithm

3.7 Complementary Varactor Pair (CVP) design

Some researchers have focused on minimizing the unit switchable capacitor. It is a useful method to utilize two different sizes of NMOS varactor to obtain a smaller unit capacitance [118]. Although it is possible to design with very small differences in sizes between two varactors, this method is susceptible to process variations. This pair of NMOS varactors is vulnerable to mismatch due to different sizes of varactors. The other

approach of minimizing the unit switchable capacitor is using different kinds of MOSFET varactors with identical sizes.

To obtain a small △Cmin on the

be implemented in the most advanced CMOS processes such as expensive 90nm [119] and 65nm [120] technology. This becomes a great impediment for the application of DCOs in low-cost commercial wireless transceivers. Moreover, although the frequency resolution of the DCO can be enhanced by sigma-delta dithering, a smaller frequency resolution requires a high dithering frequency of the modulator [119]. However, the higher clock frequency of the modulator will consume much more power, which is not preferred from portability standpoint.

In this project, a novel Complementary Varactor Pair is applied to achieve an ultra-small step capacitance (CVP) as shown in Fig. 3.7. The CVP consists of minimum size varactors A and larger varactors B with differential digital control signals. The capacitance of varactor A and B are defined as C_A^{high} and C_B^{high} when they work in the flat inversion region and as C_A^{low} and C_B^{low} when in flat depletion region [132]–[139]. The CVP takes advantage of the difference in capacitance deltas to achieve a small step capacitance [121]. The minimum switched capacitance based on standard varactor voltages is calculated to be 20aF as follows:

$$C_{pair}^{high} = FTW * C_A + \overline{FTW} * C_B = C_A^{high} + C_B^{low} \quad (3.4)$$

$$C_{pair}^{low} = \overline{FTW} * C_A + FTW * C_B = C_A^{low} + C_B^{high} \quad (3.5)$$

$$\Delta C_{min} = \left(C_A^{high} - C_A^{low}\right) - \left(C_B^{high} - C_B^{low}\right) \quad (3.6)$$

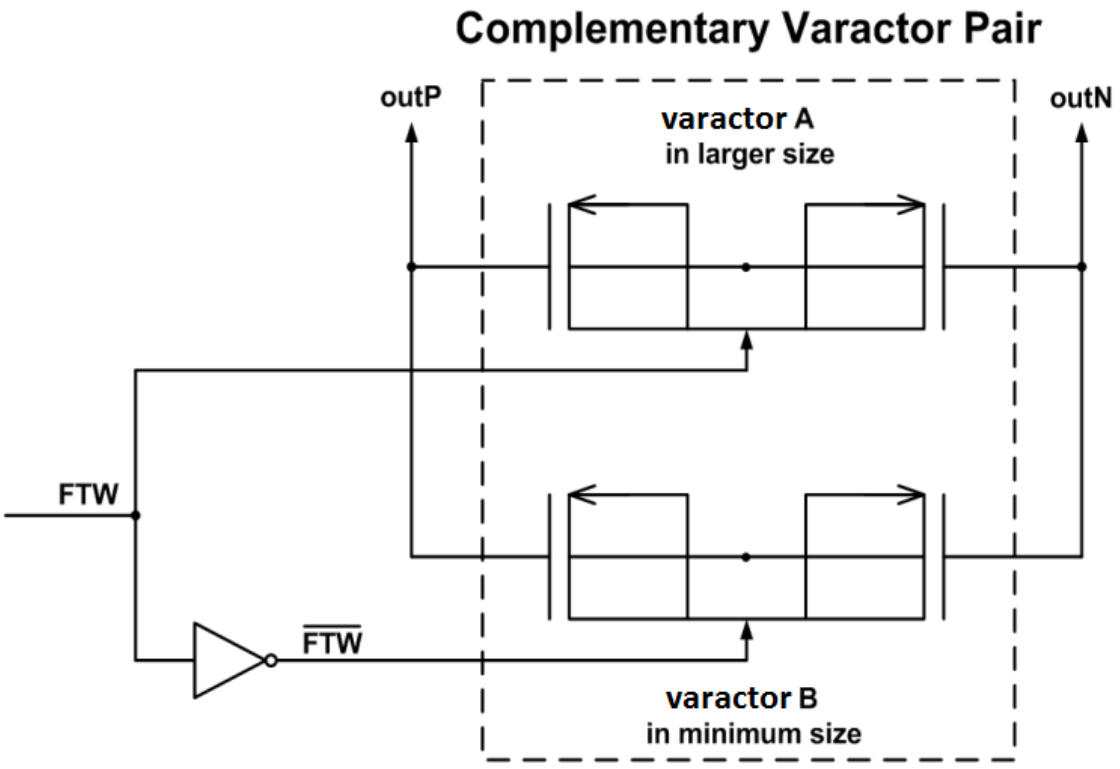

Fig. 3.7. Complementary Varactor Pair scheme

It can be seen that by properly choosing the size of varactor A, the proposed varactor pair can provide a much smaller switched capacitance than the traditional minimum size varactor. Therefore a very fine frequency resolution and low phase noise can be achieved even in a large size CMOS process. Simulation results in a 130nm process show that by choosing the width of the varactor A to be 1μm and the length to be 300nm, simultaneously the width of the varactor B to be 1.01μm and the length to be 300nm, the switched capacitance of the proposed varactor pair equals 24aF. The characterization of the ultra-fine tuning CVPs is shown in Fig. 3.8. This plot shows the ultra-fine-tuning step capacitance is 24aF, which is close to the standard calculation. The CVPs result in a much smaller capacitance delta compared to the minimum size varactor absolute capacitance. The CVPs are differentially connected to the RTWO, therefore, the

effective tuning step capacitance is counted on the difference between the two ends which is equals to 12aF.

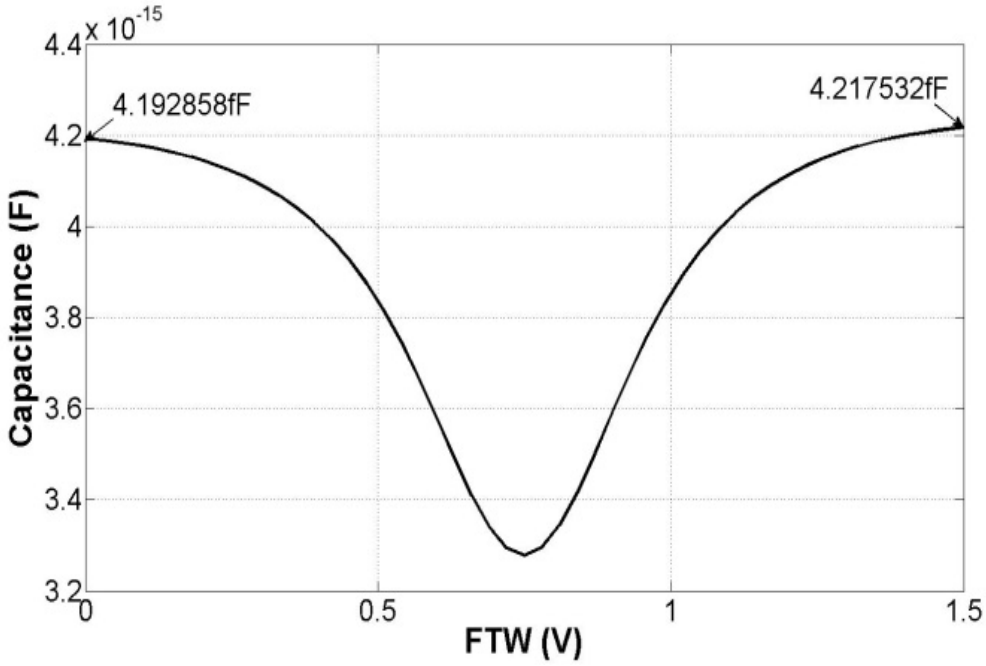

Fig. 3.8. The Ultra-Fine Tuning CVP Characterization

3.8 RTWO Phase Tuning

In synchronous circuit design, it is critical to ensure that the clock signals at different points on the die are in phase. Otherwise, incorrect circuit operation occurs.

Since the traveling wave phase shift is calculated as

$$\Theta = \beta * l \qquad (3.7)$$

where l is the total length of the folded transmission line loop; β is the propagation constant which is expressed as

$$\beta = 2 * \pi * f * \sqrt{L_{diff} * C_{diff}} \qquad (3.8)$$

The traveling wave phase can be expressed as

$$\Theta = 2 * \pi * f * l * \sqrt{L_{diff} * C_{diff}} \qquad (3.9)$$

As a result, the phase tuning steps are calculated as below,

$$\frac{\partial \Theta}{\partial C} = \frac{\Delta \Theta}{\Delta C} = \pi * f * l * \sqrt{\frac{L_{diff}}{C_{diff}}}$$

$$\Delta \Theta = \pi * f * l * \sqrt{\frac{L_{diff}}{C_{diff}}} * \Delta C \qquad (3.10)$$

Based on (20), the clock de-skew can be accomplished by varying the loading capacitance across the RTWO ring.

In this design, the phase tuning is controlled by the five-bit incrementally weighted CVPs shown in Fig. 3.4. The inverter pairs force the phase shift at any differential points to be 180°. In the proposed clock distribution network, the differential injection points are designated as reference points with clock phase ϕ = 0 or ϕ = 180° instead of choosing arbitrary points as in [43]. By increasing the phase tuning capacitances from stages v1 to v4 and decreasing the capacitances from stages v5 to v8 by the same amounts, results in a decreased traveling wave propagation delay and an increased phase shift from stage v1 to stage v4. As a corollary, the travelling wave signal speeds up across stage v5 to stage v8 and thus decreasing that phase shift [59], [61]. However, the total capacitance across the ring is constant and the oscillation frequency

stays the same. As a result, these digitally controlled CVPs support a wide phase tuning and de-skew range.

The transmission line - capacitor ladder is modeled as an LC low pass filter to allow the deviation of an equation for the phase shift of each transmission line stage. Its ABCD matrix can be written as,

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & Z_L \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ Y_C & 1 \end{bmatrix} = \begin{bmatrix} 1 + Z_L Y_C & Z_L \\ Y_C & 1 \end{bmatrix}$$

Then the S21 function is given by [1],

$$S_{21} = \frac{2}{1 + Z_L Y_C + {Z_L}/{Z_O} + Y_C Z_O + 1}$$

$$= \frac{2}{2 - \omega^2 LC + {j\omega L}/{Z_O} + j\omega C Z_O}$$

where L, C and Z_0 represent the total inductance, total capacitance and characteristic impedance of one section ladder network.

Since $L = {Z_O}^2 C$, S_{21} can be expressed as,

$$S_{21} = \frac{2}{2 - \omega^2 {Z_O}^2 C^2 + 2j\omega Z_O C}$$

The phase shift of each distributed ladder is calculated as,

$$\Theta = -arctan \frac{2\omega Z_O C}{2 - \omega^2 {Z_O}^2 C^2}$$

The total inductance consists of transmission line inductance and top metal layer interconnection inductance. According to Wheeler's theory [168] and Walker [169], the strip line inductance on a lossy substrate can be categorized as self-inductance and mutual inductance [170]. The self and mutual inductances are given by (22) and (23) as follows,

$$L_{TEM_{self}} = l\frac{\mu_0}{4\pi}\ln\left\{1+\frac{32h^2}{w^2}\left[1+\sqrt{1+\left(\frac{\pi w^2}{8h^2}\right)^2}\right]\right\} \quad (22)$$

$$L_{mdiff} = l\frac{\mu_0}{\pi}\ln\left\{\frac{\pi s}{w+t_C}+1\right\} \quad (23)$$

where l is the length of the transmission line,

w is the width of the transmission line,

h is the height from transmission line to GND plane, which is filled with SiO2,

s is the separation between parallel transmission lines,

t_C is the thickness of the transmission line.

The single section of the transmission line network was characterized using ADS Momentum as shown in Fig. 3.9. The simulated s-parameters were imported into Cadence to compare with the rf-line model of the IBM library. The total capacitance is made up of the parasitic capacitance of the inverter pairs, frequency and phase tuning capacitor banks, frequency tuning MIM caps, parasitic capacitance of the switches, and the transmission line parasitic capacitance as shown in Fig. 3.10.

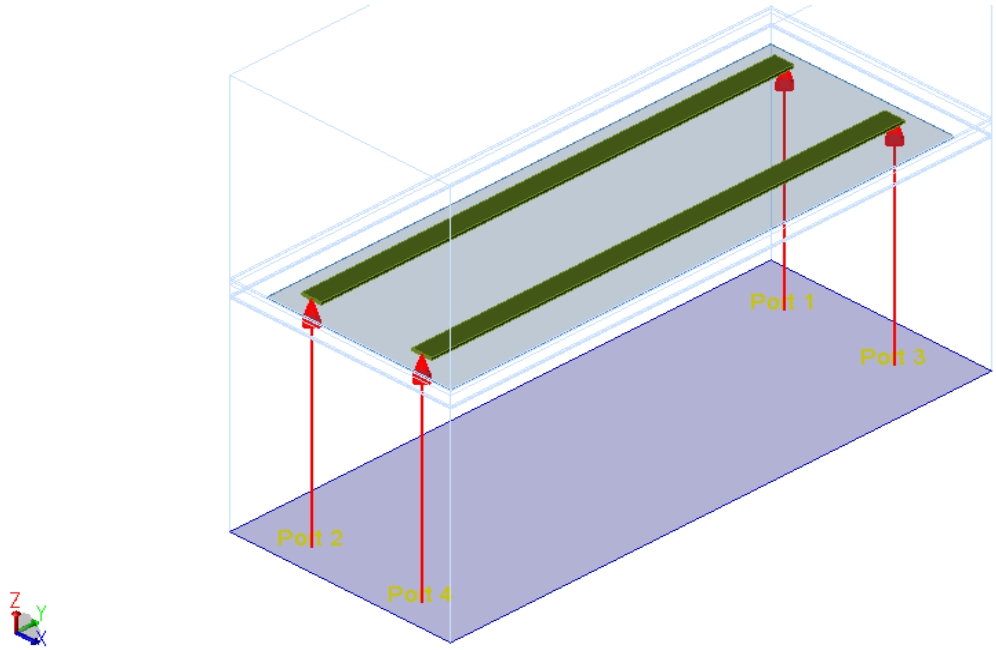

Fig. 3.9. One section Transmission line characterization – 3D Preview in Agilent Momentum

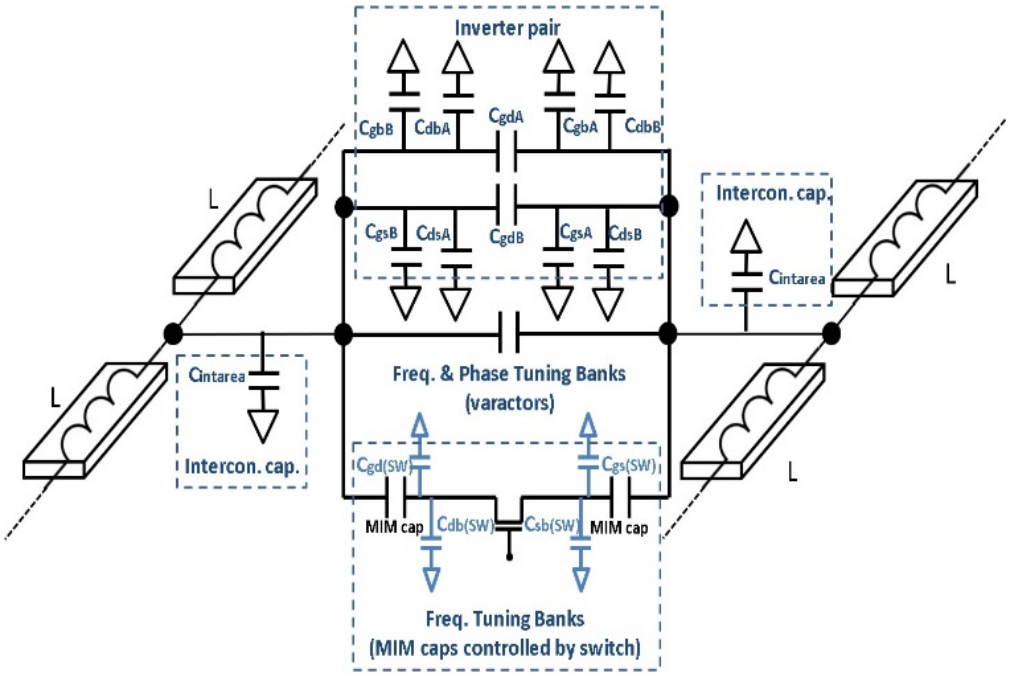

Fig. 3.10. One section RTWO network model (All Parasitic Capacitances are included)

3.9 Free running RTWO Phase Noise Analysis

The analysis and design of a 54 GHz oscillator is implemented by a rotary traveling wave oscillator with quadrature outputs, and coupled to the other units through standing-wave oscillators in [62]. A phase noise analysis for distributed oscillators based on impulse-sensitivity functions (ISF) is introduced and applied to study the proposed oscillator and arrays in.

In this section, a more detailed and complete analysis of the free running RTWO phase noise is developed. The free running RTWO phase noise, consisting of thermally induced noise and flicker noise, is derived. By using the approach in [61], [64], [65], these two noises are divided into three categories: 1) thermally induced resonator noise; 2) thermally induced inverter pair noise; and 3) inverter pair noise induced by flicker noise.

3.9.1 Thermally induced resonator noise

The phase noise analysis focuses on offset frequencies (ωm) close to the frequency of oscillation (ω0). Therefore, the noise current originated by the distributed resonator can be represented by a single resistor, which has impedance Rp at the oscillation frequency (ω0). The input impedance of a lossless λ/4 shorted transmission line at ω0 + ωm (assuming ω0 >> ωm) is given by [61],

$$Z(\omega_0 + \omega_m) = +jZ_0 \tan(\beta l_q)$$

$$= +jZ_0 \tan\left(\frac{2\pi}{\lambda_m} * \frac{\lambda}{4}\right)$$

$$= +jZ_0 \tan\left(\frac{2\pi(\omega_0 + \omega_m)}{2\pi v_p} * \frac{2\pi v_p}{4\omega_0}\right)$$

$$= -jZ_0 \cot\left(\frac{\pi}{2} * \frac{\omega_m}{\omega_0}\right)$$

$$\approx -j\sqrt{\frac{L}{C}}\ \frac{2\omega_0}{\pi\omega_m} \qquad (3.11)$$

where lq and Z_0 are the length and characteristic impedance of the λ/8 shorted transmission line. The oscillation frequency is determined by,

$$f_0 = \frac{v_p}{8l_q} = \frac{1}{8l_q\sqrt{L_0C_0}} = \frac{1}{8\sqrt{LC}} \qquad (3.12)$$

$$\sqrt{C} = \frac{\pi}{4\omega_0\sqrt{L}} \qquad (3.13)$$

Merging (Eq.3.12) into (Eq.3.13), the input impedance is re-written as,

$$|Z(\omega_0 + \omega_m)| = \frac{4\omega_0^2 L}{\pi^2\omega_m} \qquad (3.14)$$

The resonator consists of the parallel circuit of Rp and $Z(\omega_0 + \omega_m)$. Therefore,

$$\left|\frac{R_p Z(\omega_0 \pm \omega_{3dB})}{R_p + Z(\omega_0 \pm \omega_{3dB})}\right| = \frac{R_p}{\sqrt{2}}$$

$$R_p = |Z(\omega_0 \pm \omega_{3dB})|$$

The quality factor of the λ/8 resonator is derived by the 3-dB bandwidth definition as,

$$Q = \frac{\omega_0}{2\omega_{3dB}} = \frac{\pi^2 R_p}{8L\omega_0} \qquad (3.15)$$

In this design, the simulated λ/8 resonator Q is approximately 19. Substituting (3.15) into (3.14), the input impedance of a lossless λ/8 shorted transmission line at $\omega_0 + \omega_m$ (assuming $\omega_0 \gg \omega_m$) is written as,

$$|Z(\omega_0 + \omega_m)| = \frac{R_p \omega_0}{2Q\omega_m} \qquad (3.16)$$

Assuming half of the noise contributes to Phase Modulation (PM) and the spectral density of the current noise is $(\overline{i_n^2}) = 4kT/R_p$. Then SSB phase noise at offset frequency ω_m is given by [63],

$$\mathscr{L}_{\text{tank}}(\omega_m) = |Z(\omega_0 + \omega_m)|^2 \frac{\overline{i_n^2}}{2} / (\frac{V_0^2}{2})$$

$$= \frac{1}{4} * \left(\frac{(4*R_p)\omega_0}{2Q\omega_m}\right)^2 \frac{4kT/(4*R_p)}{V_0^2}$$

$$= \frac{4kTR_p}{V_0^2} (\frac{\omega_0}{2Q\omega_m})^2 \qquad (3.17)$$

where $V_0 = 4I_{Dsat}R_p/\pi$ is the differential voltage amplitude at the fundamental frequency and I_{Dsat} is the saturation current supporting full swing.

3.9.2 Thermally induced Inverter pair noise

The inverter pair current noise flows into the resonator, where it is sampled within a finite time window width at every zero crossing. The spectral density of MOSFET current noise is given by,

$$\overline{i_n^2} = 4kT\gamma g_m \frac{2T_s}{T_0} \qquad (3.18)$$

where γ is the channel noise coefficient, g_m is the current source trans-conductance, T_s and T_0 represent the sampling time and oscillation period.

The total noise due to the inverter pair is given by,

$$\overline{i_n^2} = \overline{i_{nNtotal}^2} + \overline{i_{nPtotal}^2} = 4kT\gamma G_m \quad (3.19)$$

where $\gamma = (\gamma_N + \gamma_P)/2$ and $G_m = (g_{mN} + g_{mP})/2$.

Instead of supplying a large current (e.g. I_{Dsat}) to support a rail-to-rail swing as in a Ring oscillator, inverter pairs in RTWOs only contribute a small amount of current (ΔI) to compensate for the single stage transmission line network loss. The PMOS and NMOS transconductance are designed to be the same. Therefore, the inverter pair transconductance is calculated as,

$$G_m = \mu_n C_{ox} \frac{W_N}{L} \Delta I R_L \quad (3.20)$$

Assuming, the RTWO rising and falling times are symmetrical, the inverter pairs supply current within a short time window (T_s) [64]. Based on the fast-switching approximation, the noise sampling window to resonating period ratio is deducted as,

$$\frac{2T_s}{T_0} = 2\frac{\Delta I}{I_{Dsat}}\frac{I_{Dsat}}{S}\frac{\omega_0}{2\pi} = \frac{\Delta I \omega_0}{\pi S} \quad (3.21)$$

where S is the slope of output waveform.

Since the noise around the zero crossing produces pure phase noise [65], [66], then from (Eq.3.17) and (Eqs.3.19-3.21), the inverter pair induced phase noise is derived as,

$$\mathscr{L}_{\text{inv\_Thermal}}(\omega_m) = \frac{4kTR_p}{V_0^2}\left(\frac{\omega_0}{2Q\omega_m}\right)^2 \gamma G_m \frac{\Delta I \omega_0 R_p}{\pi S} \qquad \text{(Eq.3.22)}$$

Therefore, the thermally induced phase noise in the λ/8 section of the RTWO is summarized as,

$$\mathscr{L}_{\text{RTWO\_Thermal}}(\omega_m) = \frac{4kTR_p}{V_0^2}\left(\frac{\omega_0}{2Q\omega_m}\right)^2 \left(1 + \gamma G_m \frac{\Delta I \omega_0 R_p}{\pi S}\right) \quad \text{(Eq.3.23)}$$

3.9.3 Inverter pair noise induced by flicker noise

The transistor gate voltage noise induced by flicker noise is given as $\overline{v_{gn}^2} = K/WlC_{ox}f$, where K is a constant depending on device characteristics. W and l are the transistor's width and length. The induced transistor drain current noise is calculated as $\overline{i_{ng}^2} = g_m^2 \overline{v_{gn}^2}$. The PMOS transistor width is sized to be twice that of the NMOS transistor width ($W_P = 2W_N$). As a result, the spectral density of the inverter pair injected current noise is summarized as,

$$\overline{i_{ninv}^2}^{\frac{1}{f}}(f_m) = \frac{1}{2}\left(\overline{i_{ngN}^2} + \overline{i_{ngP}^2}\right) = \frac{\pi K\left(g_{mN}^2 + g_{mP}^2/2\right)}{W_N l C_{ox}\omega_m} \qquad \text{(Eq.3.24)}$$

Similar to the above derivation, the sampled noise current from the inverter pair is,

$$\overline{i_{nsinv}^2}^{\frac{1}{f}}(f_m) = \frac{\pi K\left(g_{mN}^2 + g_{mP}^2/2\right)}{W_N l C_{ox}\omega_m}\frac{2T_s}{T_0} = \frac{K\left(g_{mN}^2 + g_{mP}^2/2\right)\Delta I \omega_0}{W_N l C_{ox}\omega_m \pi S} \quad \text{(Eq.3.25)}$$

Then the SSB phase noise due to the flicker noise of inverter pair in the λ/8 RTWO section is derived as,

$$\mathscr{L}_{\text{inv}}{}^{1/f}(\omega_m) = \frac{1}{V_0^2}\left(\frac{\omega_0 R_p}{2Q\omega_m}\right)^2 \frac{K(g_{mN}^2+g_{mP}^2/2)\Delta I\omega_0}{W_N l C_{ox}\omega\pi S}$$

3.10 Current Source Design

A typical current source is designed to supply bias current to the oscillator as shown in Fig. 3.11. The level of the bias current decides the dc bias level and output amplitude of the oscillator. For testing purposes, M1 was sized to be the same as M2 so that the external current source is approximately the same as the oscillator bias current (assuming both devices are in strong inversion). The bias current is supplied by placing a tunable resistor between the voltage supply and the drain of transistor M2. A capacitor may be added between the gate of the NMOS transistor M1 and ground [126]-[131]. This provides some noise filtering at the gate of the oscillator current source. Both M1 and M2 are sized to be 50μm and matched to M3 to save power and leave a large voltage swing for the RTWO. Transistor M2 is always in the strong inversion region; transistor M1 is designed to have a 300mV voltage drop and a 100mV turn on voltage.

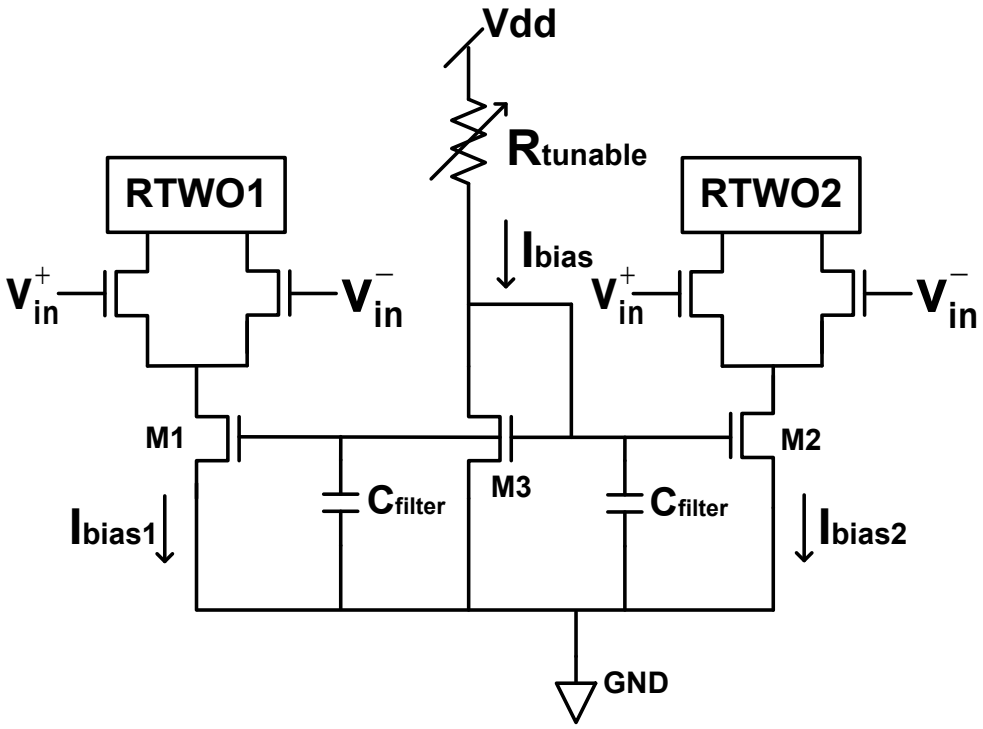

Fig. 3.11. DCO Current Source

Ideally, the current versus drain to source voltage curve is flat in the region. This is equivalent to having an infinite output resistance, since the current does not change when V_{DS} changes. In reality, there is a dependence of I_{DS} on V_{DS}, so there is a finite output resistance. This dependence appears as λ which ranges from approximately 0.1 for short channel devices to 0.01 for long channel devices. According to the drain current formula, $I_{DS} = \frac{1}{2} * k' * \frac{W}{L}(V_{GS} - V_t)^2(1 + \lambda V_{DS})$. Short channel means larger λ, which results in larger drain current. When we increase L, and then V_{GS} must be made larger and V_{DS} must also be made larger to satisfy the saturation region. So less voltage headroom remains. At the same time, the output current will decrease. So we need to either increase V_{DS} or increase W (more layout area) to compensate. In order to achieve high output

impedance and constant biasing current, the M1 and M2 transistor lengths are sized to be 400nm instead of the minimum transistor length.

3.11 RTWO rotation direction

Once started, the traveling wave can rotate either clockwise or counter clockwise due to process variations and noise uncertainties. The rotation direction will be determined by the path that has lower impedance at the beginning of the oscillation [13], [99]. Once a wave becomes established, it takes little power to sustain it, because unlike a ring oscillator, the energy that goes into charging and discharging MOS gate capacitance becomes transmission line energy, which is recirculated in the closed electromagnetic path [53]. In this design, the rotation direction of the RTWO is not important as the BIST circuit discussed in the following sessions can be used to detect either clockwise or counter clockwise rotation direction. The BIST circuit is implemented to find the minimum and maximum clock skews of different RTWOs, and the designer only needs to plot the BER versus clock skew curve and pick up the middle point as the optimum clock skew. The BIST calibration mechanism is exactly the same for both clockwise and counter clockwise RTWO rotations.

3.12 BIST design

Clock skew can result in hold violations or cycle slipping when transferring data from an early clock to a late clock, or setup time violation depending on skew between clocks. The skew violation mechanism with its corresponding circuit is illustrated in Fig. 3.12. The minimum and maximum propagation delays between the first flip-flop output Q_1 and the second flip-flop input D_2 are defined as t_{min} and t_{max} as shown in Fig. 3.12a)

and Fig. 3.12b). t_{prop} is the $clock_1$ high to Q_1 valid time. Cycle slipping happens when the clock skew is larger than the sum of the t_{prop} and t_{min}.

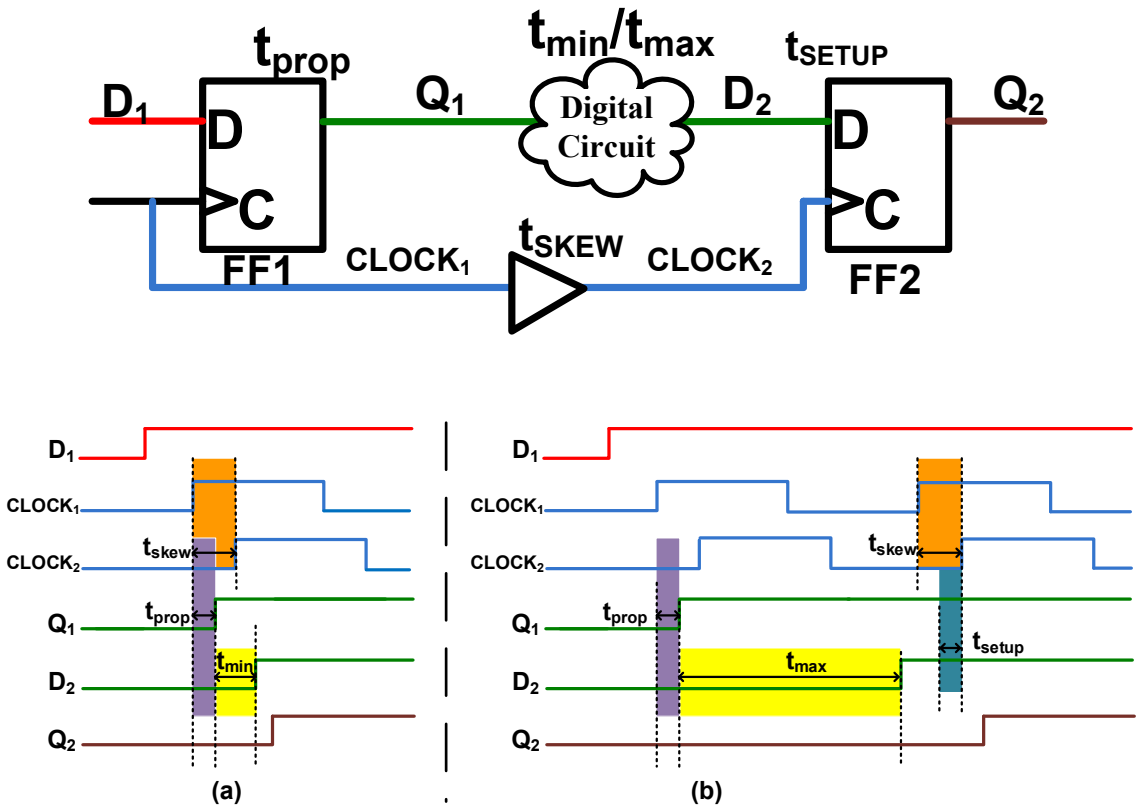

Fig. 3.12a. Cycle slipping caused by positive clock skew violation

Fig. 3.12b. Setup time violation caused by negative clock skew

The right $clock_2$ skew margin t_{skewP} is calculated based on nominal schematic simulation, as follows:

$$t_{skewP} = t_{prop}(27\ ps) + t_{min}(37\ ps) = 64\ ps \qquad (3.26)$$

Similarly, the clock_2 starts losing bits with the increase of left clock_2 skew due to D_2 setup time violation. The left clock skew margin (t_{skewN}) is calculated as,

$$t_{skewN} = t_{prop}(27\ ps) + t_{max}(379\ ps) + t_{setup}(30\ ps)$$

$$- \ T(541\ ps) = -105\ ps \qquad (3.27)$$

where T (1.85 GHz) is the period of the RTWO clock output. If the clock skew is kept between these limits (with appropriate PVT margin), then data transfer between domains will be safe. It should be noted that the t_{max} and t_{min} are purposely designed with worst case maximum and minimum delays.

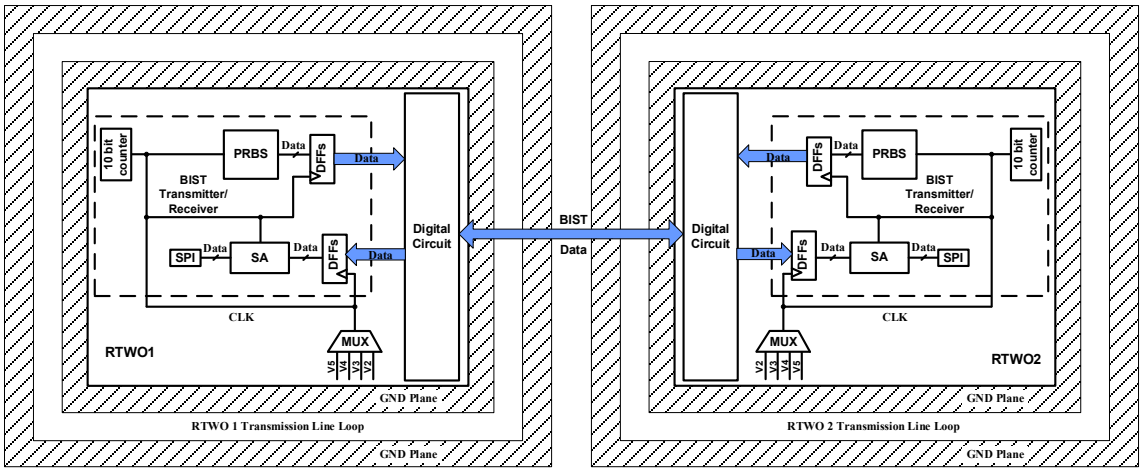

Fig. 3.13. Detailed BIST architecture

The digital and BIST circuits clocked by the RTWOs are placed inside the transmission line loops and so they do not influence the overall die size, as shown in Fig. 3.13. Various test patterns are generated on-chip by a Pseudo Random Binary Sequence clocked with RTWO1. The generated patterns pass through data path to arrive at RTWO2. The received data is resampled by Flip-Flops located on RTWO2. The SA

produces a result from the received PRBS data. A 10-bit counter is used to gate the pattern generation, transfer and signature analysis so that they can be read from the serial-parallel interface (SPI) after the BIST is triggered. The correct result (expected result) is received when the clock skew stays within the minimum and maximum skew margins ($t_{skewN} < t_{skew} < t_{skewP}$). Bit errors appear as the RTWOs' phase is adjusted outside the t_{skew} limits. The result is read by an external micro-controller, which is used to adjust the skew or phases by tuning the on-chip Complementary Varactor Pairs (CVP) control words in the RTWOs.

In this design, the skew or phase tuning is controlled by five-bit incrementally weighted CVPs. The inverter pairs force the phase between their differential outputs to be 180°. In the proposed clock distribution network, the differential injection points are designated as reference points with clock signal delay t = 0 and t = T/2 (i.e., clock phase $\phi = 0$ or $\phi = 180°$) instead of choosing arbitrary points as in [86]. Increasing the phase tuning capacitances from stages v1 to v4 and decreasing the capacitances from stages v5 to v8 by the same amounts, it results in a decreased traveling wave speed and an increased phase shift from stage v1 to stage v4. As a corollary, the travelling signal speeds up across stage v5 to stage v8 and thus decreasing that phase shift [61]. However, the total capacitance across the ring is constant and the oscillation frequency stays the same. Different RTWO tapping points are chosen using MUXs to increase the phase tuning range.

Due to limited silicon design space, only two RTWOs were placed on the current test chip. The ideal number of RTWOs for a given design is application specific. For

large chip area there would tend to be a larger number of major circuit blocks which could each be placed within their own RTWO. Similarly, smaller chip area will tend to have a smaller number of major circuit blocks and would therefor use a smaller number of RTWOs. It is still possible to use a smaller number of RTWOs for a larger chip design which will result in reduced power savings. For smaller chip area, it is not recommended to use a large number of RTWOs as the silicon overhead of the RTWO rings and diminishing power savings are not justified. It should also be noted that the RTWO ring size can be increased or decreased as needed by varying the fixed loading capacitance in the ring. The fan-out of the clock network can be adjusted as needed by varying the transmission line width which varies the transmission line losses. If the transmission line width is increased the losses are reduced and the clock buffer can drive a larger fan-out at the cost of extra area for the global clock tree routing. If more RTWOs are required, the designer has to calibrate each RTWO to the other RTWOs. The BIST procedure is the same, except more steps are required. An example of four RTWOs calibration is shown in Fig. 3.14.

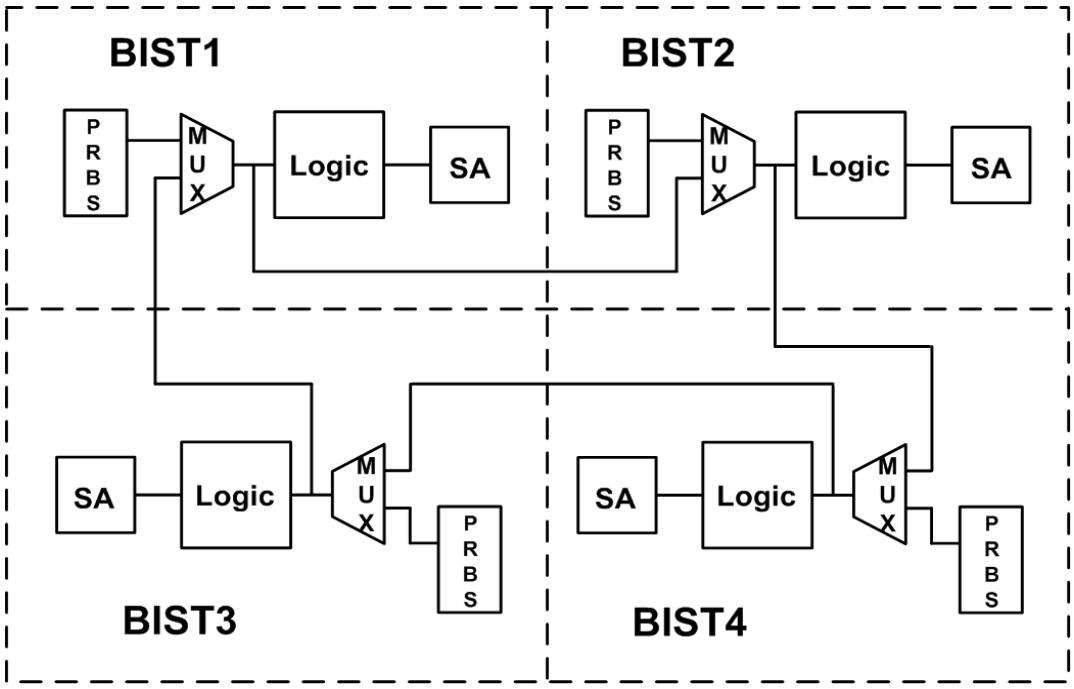

Fig. 3.14. Four RTWOs BIST Calibration Architecture

The BIST calibration algorithm scan through the BER curve with different clock skews to find the two corners where errors start increasing as shown in Fig. 3.15 below. The dashed lines in Fig. 3.15 represent different scan steps and the PRBS is running for 1,000 clock cycles per step. For example, a simple algorithm could take thirty equally spaced steps. More steps could be chosen to achieve higher resolution. For a thirty step algorithm, the PRBS is running for 1,000 clock cycles per step. Therefore, the total calibration time per BIST pair is calculated as:

$$500\,\frac{ps}{cycle} * 1{,}000\ cycles * 30\ steps = 15\ \mu s$$

The number of BIST pairs required is calculated as

$$Nbist = \sum_{i=1}^{N-1} i = N * (\frac{N}{2} - 1) + N/2, \qquad (3.28)$$

where N is the number of RTWOs on a specified chip area.

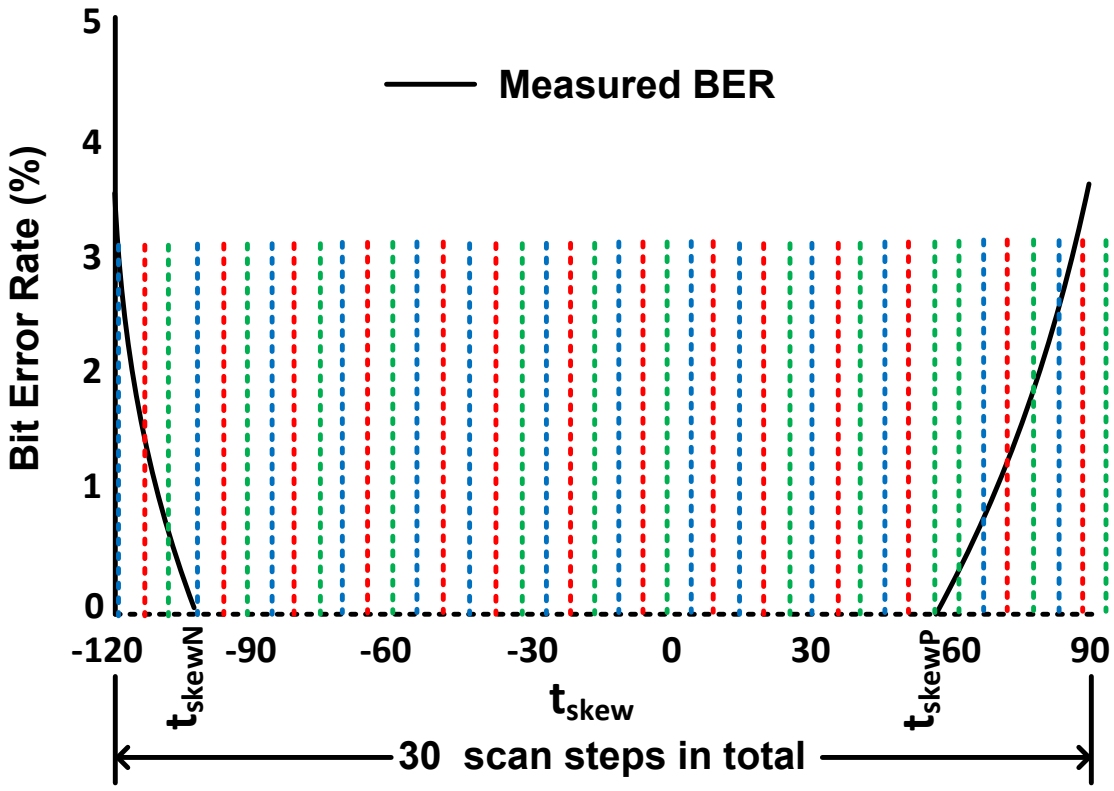

Fig. 3.15. BER Curve with 30 Scan Steps In Total

Assuming N RTWOs on the chip, therefore, the number of BIST pairs required is addressed as $Nbist = N * (\frac{N}{2} - 1) + N/2$ and N/2 independent pairs can be calibrated in parallel, therefore, the amount of calibration time is calculated as

$$t = \left[Nbist/(\frac{N}{2})\right] * t_{bist} = (N-1) * t_{bist} \qquad (3.29)$$

Where t_{bist} is the calibration time required for single BIST pair (15 µs as derived above). For example, with 16 RTWOs, the chip will require 120 BIST pairs and the total BIST calibration time is calculated as $15 * 15\ \mu s = 225\ \mu s$.

Only one buffer was used for each RTWO tapping point, which has better noise rejection than a large buffer chain. The RTWOs' outputs are large swing signals (0 to 1.5 V) with small rise/fall times and are therefore less sensitive to noise. The nominal phase difference between adjacent tapping points is 22.5º. The phase tuning range is limited by the number of tapping points chosen. For test purposes, only 4 tapping points were chosen. The phase tuning range can be increased by choosing more tapping points from RTWO rings.

The proposed BIST technique can be used to tune out process variations, interconnect variations and load mismatch by adjusting clock skew between the above two edges. True single phase clock Flip-Flops are used to maximize the digital circuit speed as shown in Fig. 3.16.

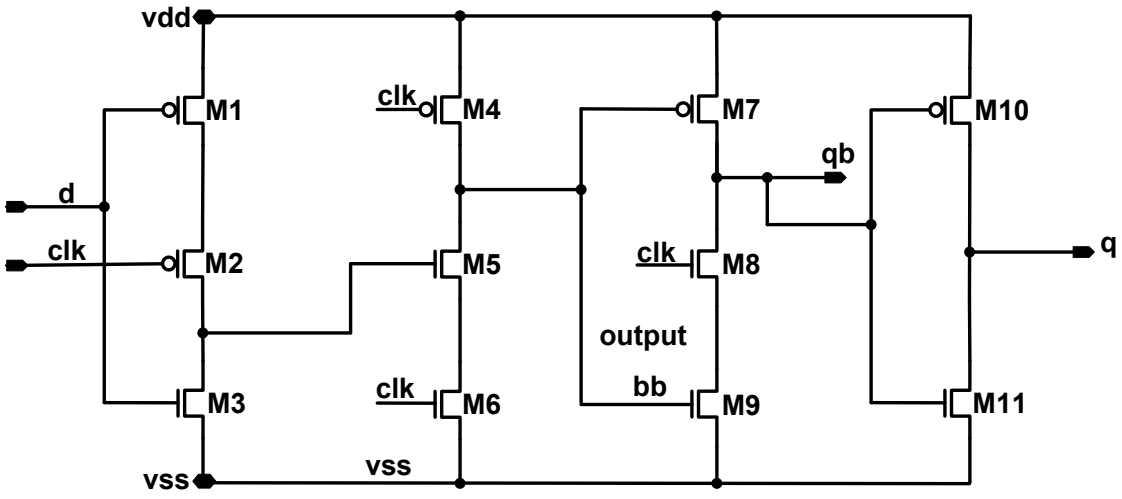

Fig. 3.16. The Single edge triggered flip flop

3.13 Correlated Digital Noise Generation

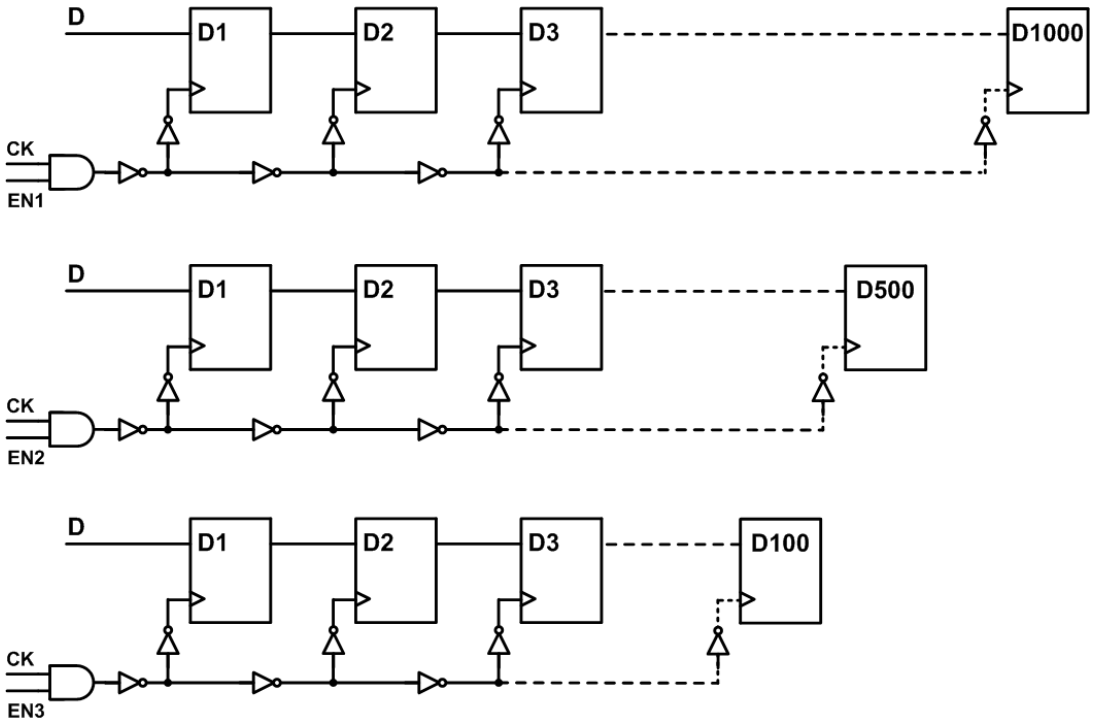

Fig. 3.17. Correlated digital noise generation circuit

The local digital circuits will be clocked by the high frequency RTWOs at 2GHz. large amount of the digital circuits and clock tree buffers are implemented on-chip and clocked by the RTWOs. These digital circuits produce correlated digital noise which makes the design similar to a real micro-system as shown in Fig. 3.17. Different scale digital circuits are switched on and off to test the RTWO phase noise immunity to the correlated digital noise. the digital filter circuits and Pseudo Random Binary Sequence in this process can only run up to 2.5GHz. This limited the size of the RTWO.

Chapter 4 : Injection Locked Clock Distribution Network Simulation Results

The global clock distribution is a critical element particularly in designs with large chip area. Consider a large 28mm x 28mm chip area, using a conventional bufferd H-tree with a 16 branch tree for the global clock network and using 2x minimum width M5 and M6 layers for the clock routing, the optimize buffer spacing and size in the 130nm process used for the RTWO design is 100μm and 40X minimum size transistors (The buffer spacing and size is optimized to keep clock signal rise/fall times to less than 20% of clock cycle and minimize clock delay in the clock tree). With this buffer spacing and size the global clock network power dissipation is 773mW at 2GHz (schematic simulation without extracted layout parasitics). A 16 RTWO global clock network (includes RTWOs, injectors and clock buffer) would dissipate only 184mW (schematic simulation without extracted layout parasitics) while reducing the clock jitter and eliminating the process variations in the global clock tree which provides additional timing margin for the local clock tree.

4.1 RTWO Built with Lumped Components and Uniform Loading Capacitors

A discrete component RTWO was built first in ADS based on [61], [63]. The discrete component oscillators with both uniform and varied loading capacitance are discussed. The differential transmission line can be modelled by an LC ladder equivalent circuit.

The lumped component RTWO with uniform loading capacitance is shown in Fig. 4.1 where the R is the equivalent lumped load of each of the 4 segments. $L = 0.15nH$ and $C = 6.6pF$ are the lumped inductance and capacitance. The discrete RTWO simulation result is shown in Fig. 4.2 which shows the 360° phase shift happened at 3.772GHz. Therefore, the RTWO oscillation frequency is 3.772GHz which is a bit lower compared to the RTWO frequency calculation equation (3.1). It should be noted that the -Gm cells are not ideal component which introduce some extra delays and lowers the oscillation frequency a bit. The lumped RTWO transient simulation results from different tapping points are shown in Fig. 4.3 where linear components are used and the power rails are not fixed.

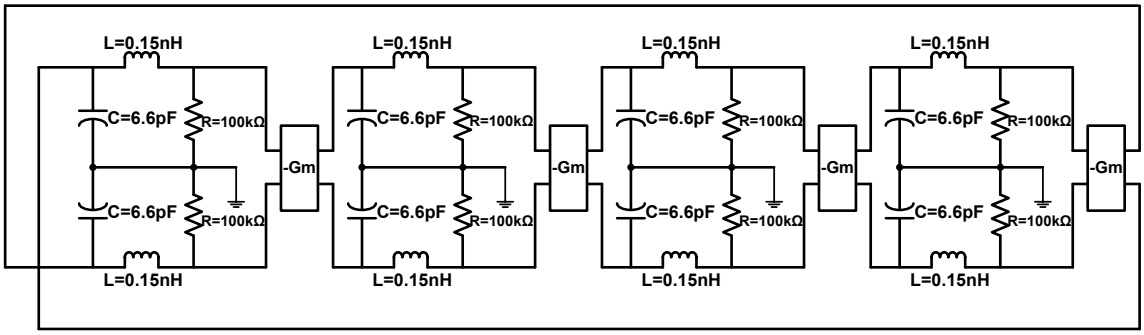

Fig. 4.1. The RTWO built with lumped components

Fig. 4.3 shows that the output signal amplitude is uniform over the 4 lumped segment stages. Also, the phase shift between each segment is 45º. The output signal starts with standing wave oscillations and evolved to a traveling wave after 20ns. The clock signal delay t and the clock signal phase shift θ can be calculated using the equation θ/360 = t/T. Therefore, the 45º phase shift corresponds to approximately 33ps (0.125*T) clock skew. This also agrees with the simulation result shown in Fig. 4.2 and Fig. 4.3. In

Fig. 4.3, the wave is sinusoidal since the transconductance in Fig. 4.1 is not enough to sustain enough harmonics. This is a practical limit on the number of harmonics the RTWO can sustain. In this design, the author only target for a 2GHz RTWO. Therefore, the optimized inverter pairs are implemented in the design to supply sufficient transconductance for square wave outputs while maintaining less power consumption and minimize RTWO load for a high overall Q. If a higher RTWO output frequency is desired, the designer will manage to make the output waveforms to be as square as possible.

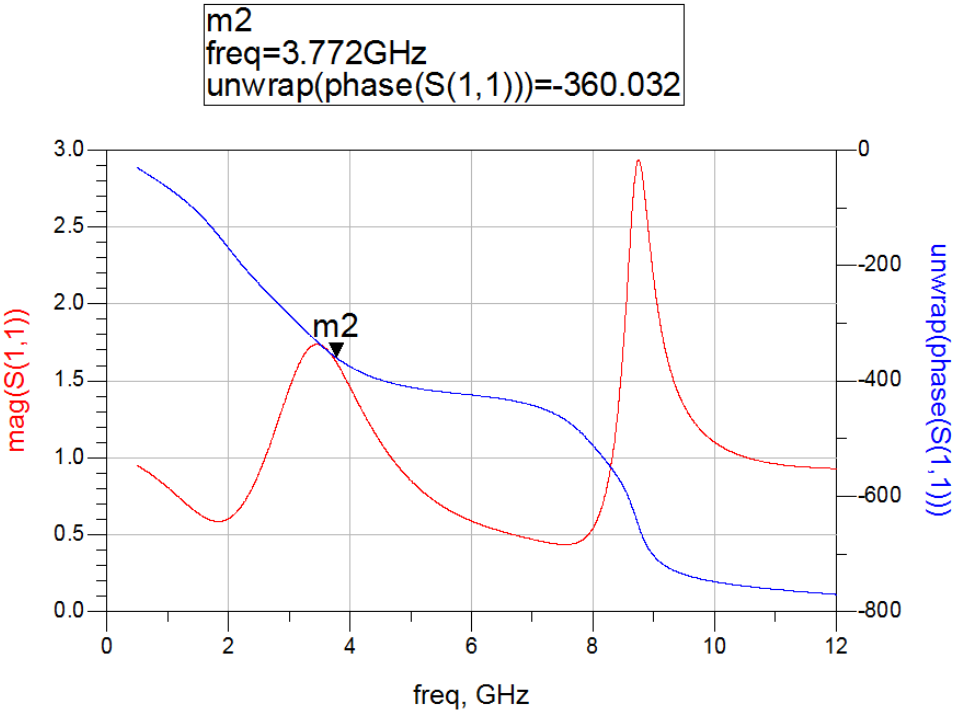

Fig. 4.2. The lumped components RTWO frequency simulation result

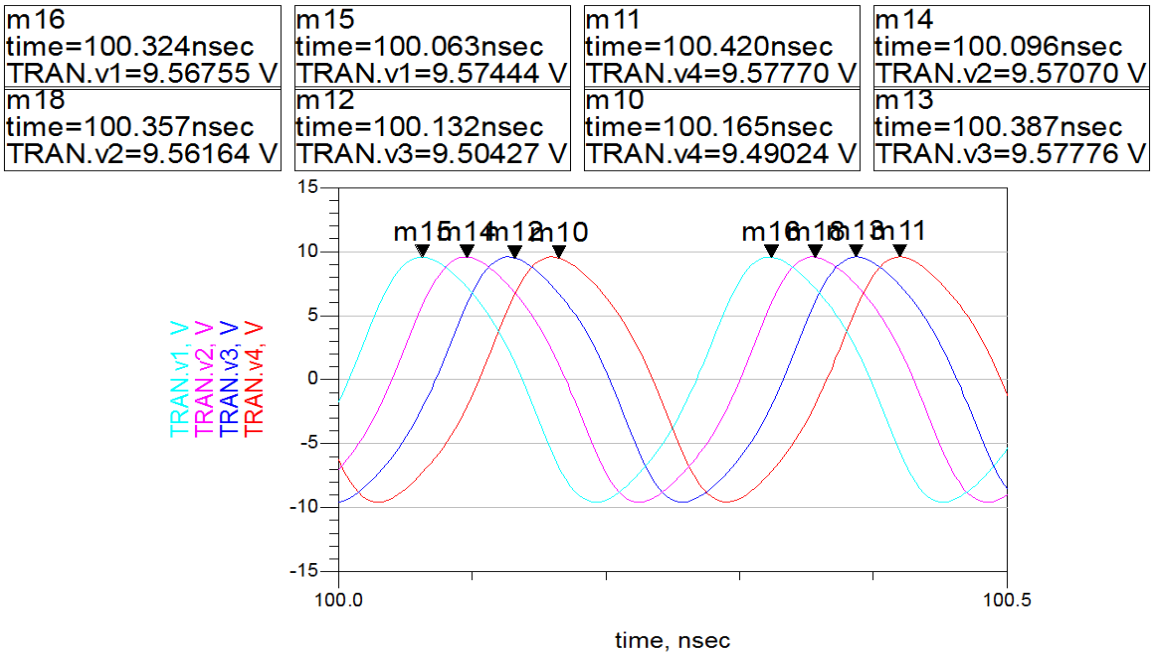

Fig. 4.3. Phase shift of lumped components oscillator with same loading capacitance

4.2 RTWO Built with Lumped Components and Different Loading Capacitors

The discrete RTWO with different lumped capacitance transient simulation is also run and the simulation result is shown in Fig. 4.4. Fig. 4.4 shows that the output signal amplitude varies with the variation of loading capacitance over different segments. Also, the phase shift between each segment is uneven which depends on the loaded capacitor value as shown in Fig. 4.5.

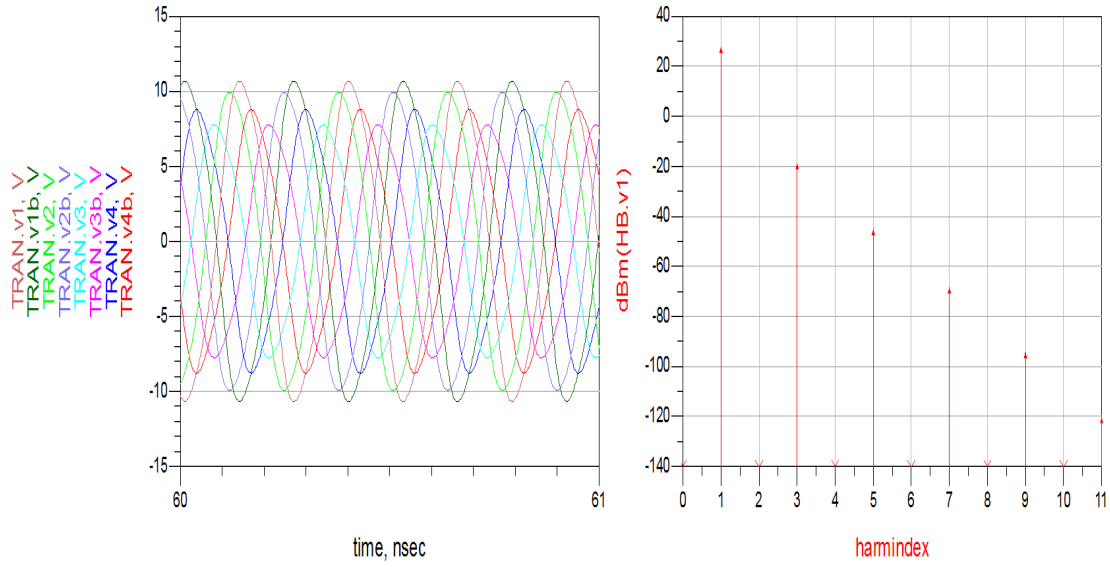

Fig. 4.4. Lumped components oscillator with different loading capacitance transient simulation

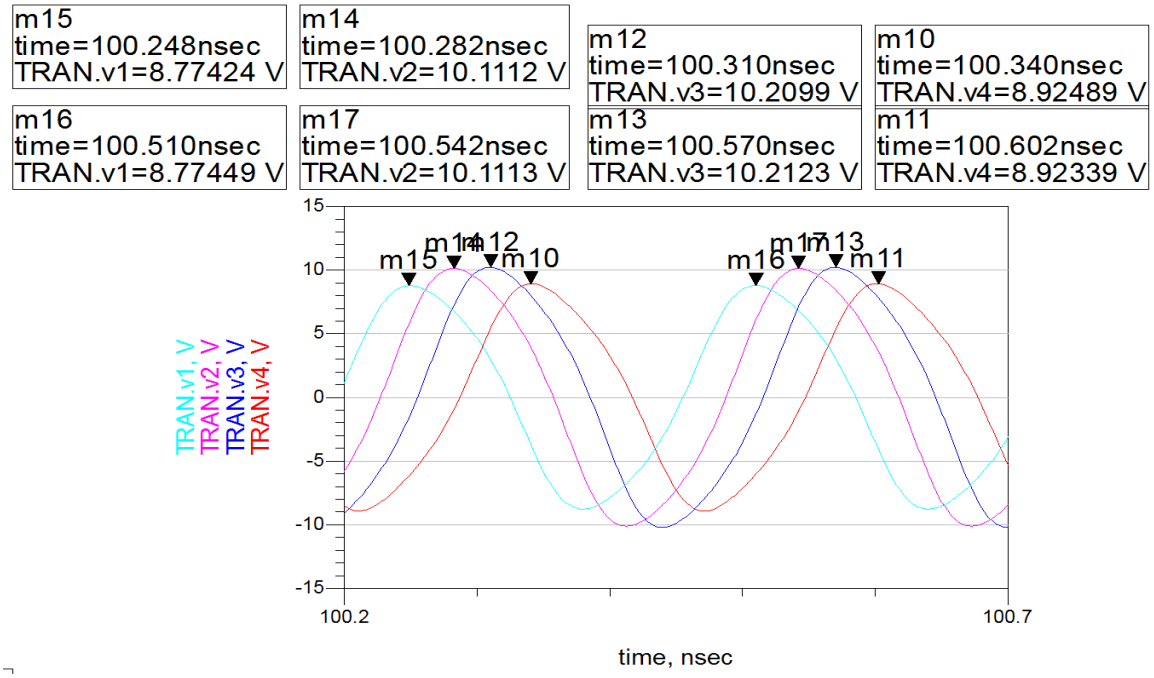

Fig. 4.5. Phase shift of the lumped component oscillator with different loading capacitance

4.3 The RTWO Transient Simulation Results in Cadence

Since the ADS simulation works as expected, the RTWO is built with the micro-strip line offered in the IBM library at the target frequency and its transient simulation is run in Cadence. Proper connection to the ground node of the rfline during simulation is critical to achieve accurate simulation results. The ground node must be connected to an ideal AC ground in order to provide accurate simulations. This ideal ground connection does not represent an actual physical connection to the P-substrate below the rfline and therefore should not contain series resistance representing the resistance present between the rfline and any adjacent substrate contacts [101], [102]. The requirement for an ideal AC ground represents a limitation of modeling a distributed structure with a lumped element circuit [101], [102]. The sixteen stage RTWO structure is implemented and the simulation result is shown in Fig. 4.6. Fig. 4.6 shows the zero crossing points of the output signals are sharp. This helps to reduce the RTWO jitter noise. The RTWO output frequencies are all at 2.04GHz and the phase shift between each segment is 22.5° $(360^{\circ}/16)$.

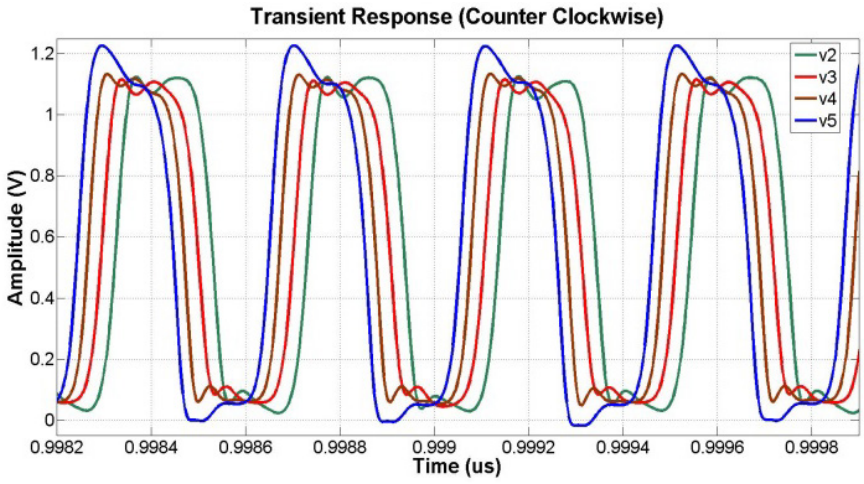

Fig. 4.6. Transient response for clock wise rotation

4.4 RTWO Medium Frequency Tuning Result

The RTWO output frequency is tuned upwards as the amount of switching MIM-caps and CVPs loading each segment of the RTWO tank is reduced as shown in Fig. 3.4. Conversely, the RTWO output frequency is tuned down by increasing the MIM-caps and the CVP capacitance of the RTWO tank. These MIM-caps and CVPs can also be used for phase tunings. Therefore, the RTWO free running frequency and phase can still be tuned after being injection locked. The simulated frequency tuning range is more than 25% of the oscillator center frequency. The switched MIM-caps have a minimum step size of 3.5 fF giving a frequency resolution of 1.5MHz. The medium and fine resolution tuning bank can achieve 500aF and 120aF step capacitance respectively. This corresponds to 400kHz and 100kHz frequency resolutions.

4.5 RTWO Phase Tuning Simulation Result

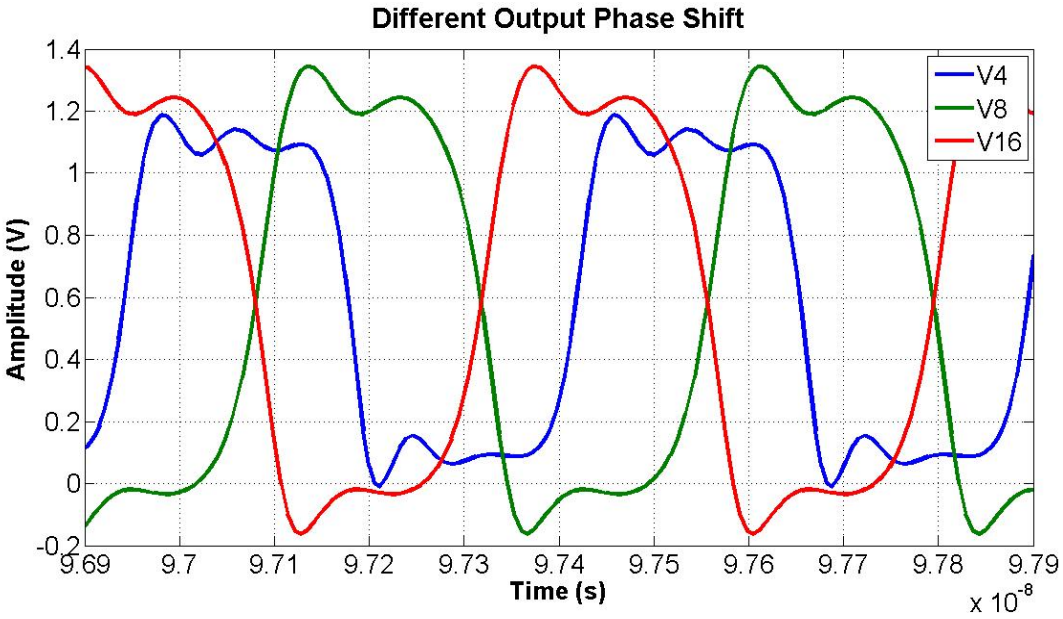

Fig. 4.7a. Transient Response for Phase Tuning

As illustrated in Fig. 4.7a, the oscillation frequencies across v1 to v15 are all 2.102 GHz; the phase shift between v0 to v4 is 75.29 ° and the phase shift between v4 and v8 is 104.71°. The phase shift is controlled by the five-bit incrementally weighted complementary varactors pairs. These varactors pairs attain 30 degree phase tuning range and 2 ° phase resolution.

The single transmission line stage phase shift is calculated to be 21.71° based on the analysis in session 3.8. This calculated phase shift lower than the simulation results by 2.95%. The transient simulation waveforms of the minimum phase tuning step at tapping point v5 are shown in Fig. 4.7b. Here v5 at both Phase Tuning Word 1 (PTW1) and Phase Tuning Word 2 (PTW2) is operating at 2.01 GHz, and the simulated phase difference between PTW1 and PTW2 is 0.27°. The minimum phase tuning step is calculated to be 0.26°, which is 0.1° lower than the simulation result shown in Fig. 4.7b.

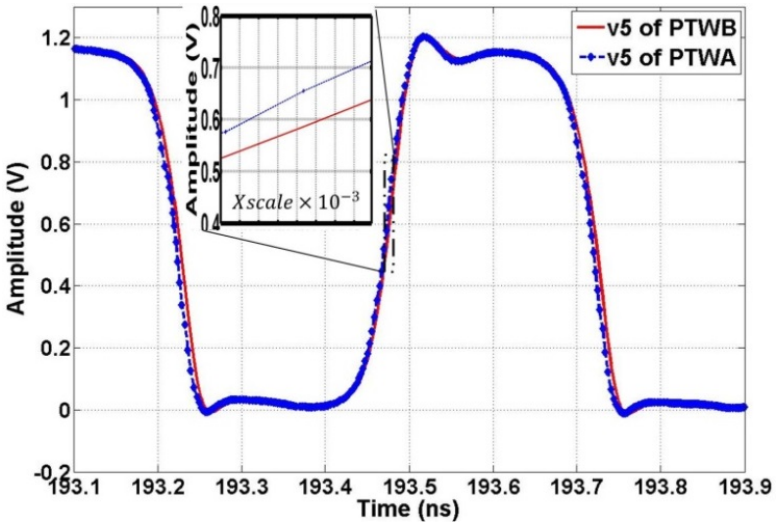

Fig. 4.7b. The simulated transient waveforms of the RTWO minimum phase tuning step at tapping point v5

It is worth mentioning that the phase tuning causes the free running frequency to drift due to noise. But with the injection locking technique implemented on this RTWO, which locks the oscillator output frequency to the sub-harmonic of the external reference signal.

The output signal phase shift is a function of the frequency difference between the injection locked frequency and free running frequency within the locking range. This enables the phase shift to be fine-tuned by tuning the RTWO free running frequency. In [105], [106], the clock de-skew can only be controlled by fine tuning the oscillator free running frequency. In this work, the relative phase difference and de-skew clocks on different RTWOs are controlled by phase tuning varactors and fine tuning the RTWO free running frequency. This allows a wide phase tuning range and high phase tuning resolution. It should be noted that the above two phase tuning mechanisms are inter-related.

4.6 RTWO Phase Noise Simulation Results

The phase noise at the minimum (2GHz) and maximum free running frequency (3GHz) are plotted in Fig. 4.8, which shows that both the phase noises at 1MHz offset frequency are less than -120dBc/Hz. This is due to the high overall RTWO tank Q.

The RTWO generates full swing square waves, which are sharp transient signals. This also contributes to the reduction of clock jitter and phase noise. Once the oscillator is injection locked, the oscillator phase noise performance is dominated by the injection source within the locking bandwidth and it will track the free running oscillator outside the locking bandwidth.

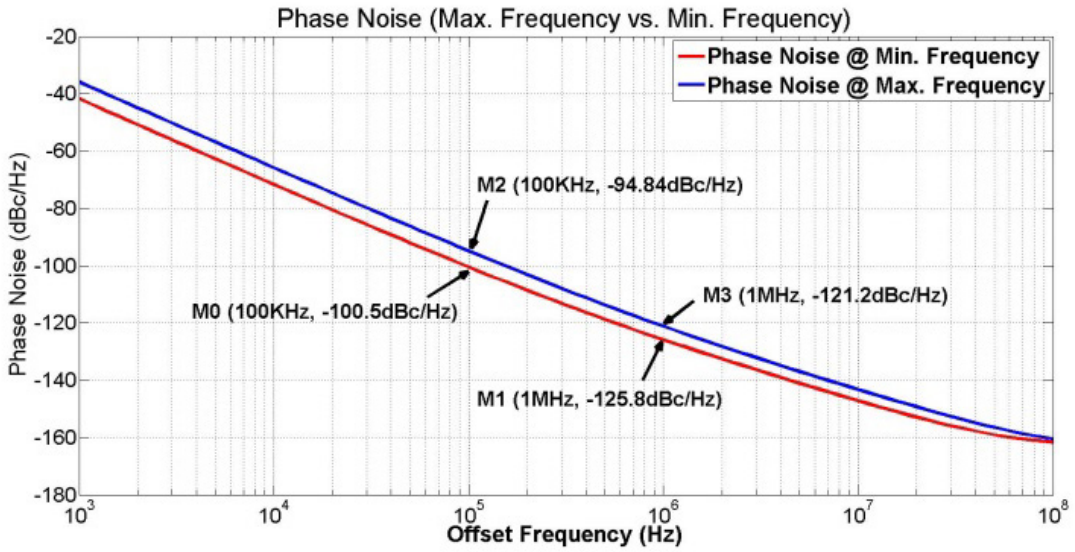

Fig. 4.8. The RTWO free running phase noise

The predicted free running RTWO SSB phase noise is plotted together with simulated phase noise at 2GHz in Fig. 4.9. Fig. 4.9 shows that the simulated and predicted phase noise results are similar. There is only 1dB of phase noise deviation between results up to 10MHz offset frequency. The simulated phase noise starts to be dominated by white noise at offset frequencies above 10MHz, this is out of the modeling range.

The predicted free running RTWO SSB phase noise is plotted together with simulated phase noise at 2GHz in Fig. 4.9. Fig. 4.9 shows that the simulated and predicted phase noise results are similar. There is only 1dB of phase noise deviation between results up to 10MHz offset frequency. The simulated phase noise starts to be dominated by white noise at offset frequencies above 10MHz, this is out of the modeling range.

The simulated phase noises at 100kHz and 1MHz offset from the 2GHz output frequency are -100.8dBc/Hz and -126.9dBc/Hz, respectively. This is limited by the overall RTWO tank Q. The RTWO generates fast rail to rail signals, which reduces the amount of power supply noise coupled into the oscillator. This also contributes to the reduction of clock jitter and phase noise.

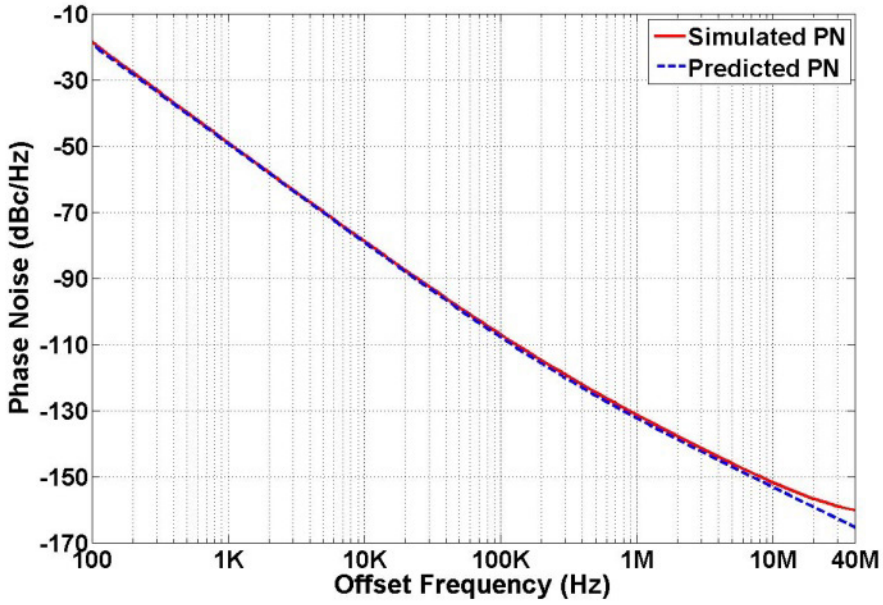

Fig. 4.9. Predicted vs Simulated RTWO free running Phase Noise comparison at 2 GHz

Chapter 5 : The Clock Distribution Network Layout Implementation

In this chapter, layout issues such as matching and noise, stray resistance, symmetry and layout rules are discussed. The layout cells implemented in this design and full layout views are also presented.

5.1 Layout Matching and Noise

The circuit elements and interconnection wiring are defined in the layout stage which is used to produce the photographic masks used in the manufacturing process. The approximate transistor parasitics are estimated by designers before and after the layout stage.

For high quality circuit performance, matching and noise layout issues need to be considered in the layout stage. The layout matching could be done by dividing larger objects into several unit-sized components connected together. Also, the MIM-caps need to be square shaped to minimize errors in capacitor ratios due to over etching. In addition, the MIM-caps' bottom plates (lower metal plate) usually have more noise coupled in from the substrate and therefore should be used for less critical nodes. Therefore, a lower metal plate is always used to reduce coupling from the substrate. Different power supplies should be used for analog and digital circuits and ideally should be star connected off-chip. Any unused space can be filled with contacts to the substrate and wells which are used as bypass capacitors [130].

5.2 Stray Resistance

In the layout of analog transistors, it is important to have an accurate aspect ratio. The stray resistance (that is, the resistance in series with drain and source) needs to be minimized by using multi-gate fingers. Also, via contacts added along the active regions reduce the series trace resistance. For wide transistors, it is worthwhile to split the layout into parallel connections [145]. Inter-finger connections need to be used in the layout to minimize noise and stray resistance. Therefore, the same numbers of NMOS or PMOS fingers are used in order to apply inter finger connections in the layout [45], [88].

5.3 Techniques to reduce parasitics on the Designed RTWO Layout

The inverter pairs and the NMOS differential pair and the NMOS current source are connected by using multi-gate finger connections. The NMOS current mirror transistors are split into 10 fingers, the poly layer gates are connected to the metal layer first by using multiple contacts, and then these gates are connected together by using metal layers. The metal lines used to connect the gates are designed to be short and thick to reduce stray resistance. Inter-finger connections are used in the layout of the above cells [130].

In the coarse tuning band, the switch resistance needs to be low. Therefore, the routing resistance must be minimized. The wiring between MIM-caps is made to be short and wide. In the CVP tuning bands, symmetric layout style is implemented to get matching for fine tuning steps and minimize parasitics caused by wiring. The power lines need to supply power for all these on chip transistors, they need to be much wider than the other wires. The RTWO routings are 100μm from the power supplies to avoid the coupling effect. Also, the buffer stage is powered by two separate power supplies to

compensate for DC drops across the power supply rail. In addition, Electrostatic Discharge (ESD) protection is implemented on transistor input gates to protect transistors from being destroyed by electrostatic discharges.

5.4 Full Layout Views

The RTWOs are designed and laid out using a folded structure both to save space and achieve symmetry as shown in Fig. 5.1. The control lines are also routed both inside and outside of the RTWOs and there is a 50μm separation required between these control lines based on the process design rules. A single RTWO together with its control line routing takes 3.325 mm^2 (1.9mm*1.75mm) of chip area. Only two RTWOs are implemented due to the limited on-chip space. Also, a 100μm separation between these two RTWOs is required to avoid interference between RTWOs and this separation space is also used for reference injection signal path. A total of 44 pads are required to debug and facilitate the measurements for different frequencies, phase tuning, and frequency injection locking.

The unused space is filled with additional contacts from power supply to substrate which are used as bypass capacitors. This increases bypass capacitance and minimize power supply noise coupling through the substrate. In this design, different power-supply connections are used for RTWO and digital circuits. The power-supply interconnects are separated since they do not have zero impedance. Digital noise (glitches) are injected into the digital power supply and the surrounding substrate when digital circuits switch on/off. Therefore, separate pins are used for the positive power supply and ground for both the digital and analog circuits. In addition, multiple pins are used for additional power supply and ground for the clock distribution network.

Two chips were fabricated. The first test chip required 6.25 mm^2 of on-chip space and implemented one IL-RTWO. The full layout view of the first chip is shown in Fig. 5.2. The second chip was an implementation of the clock distribution network with BIST circuitry as shown in Fig. 5.3. The second chip contains approximately 80,000 transistors with a total of $10mm^2$ of on-chip area.

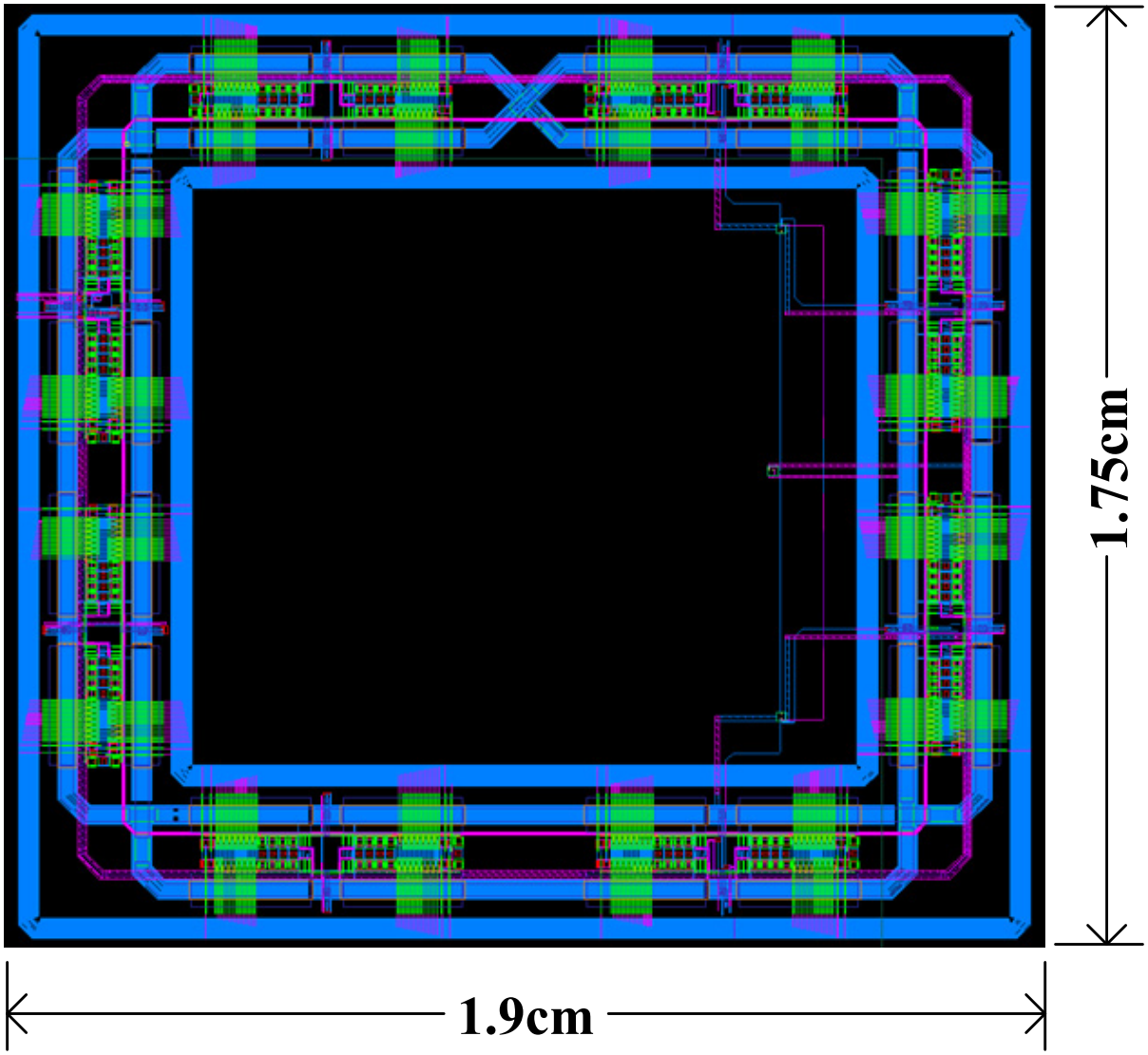

Fig. 5.1. Single RTWO layout

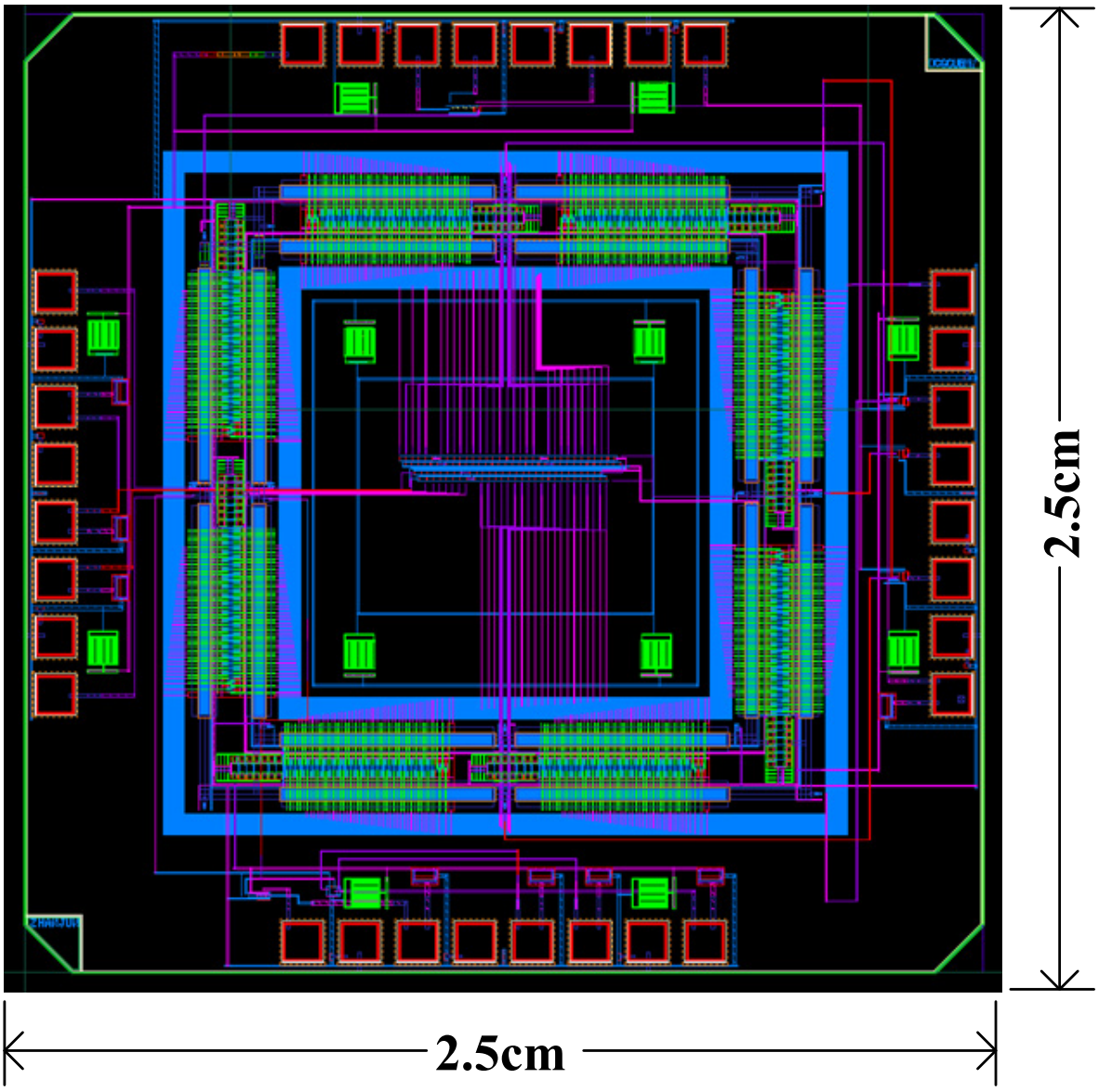

Fig. 5.2. The full layout view of one IL-RTWO

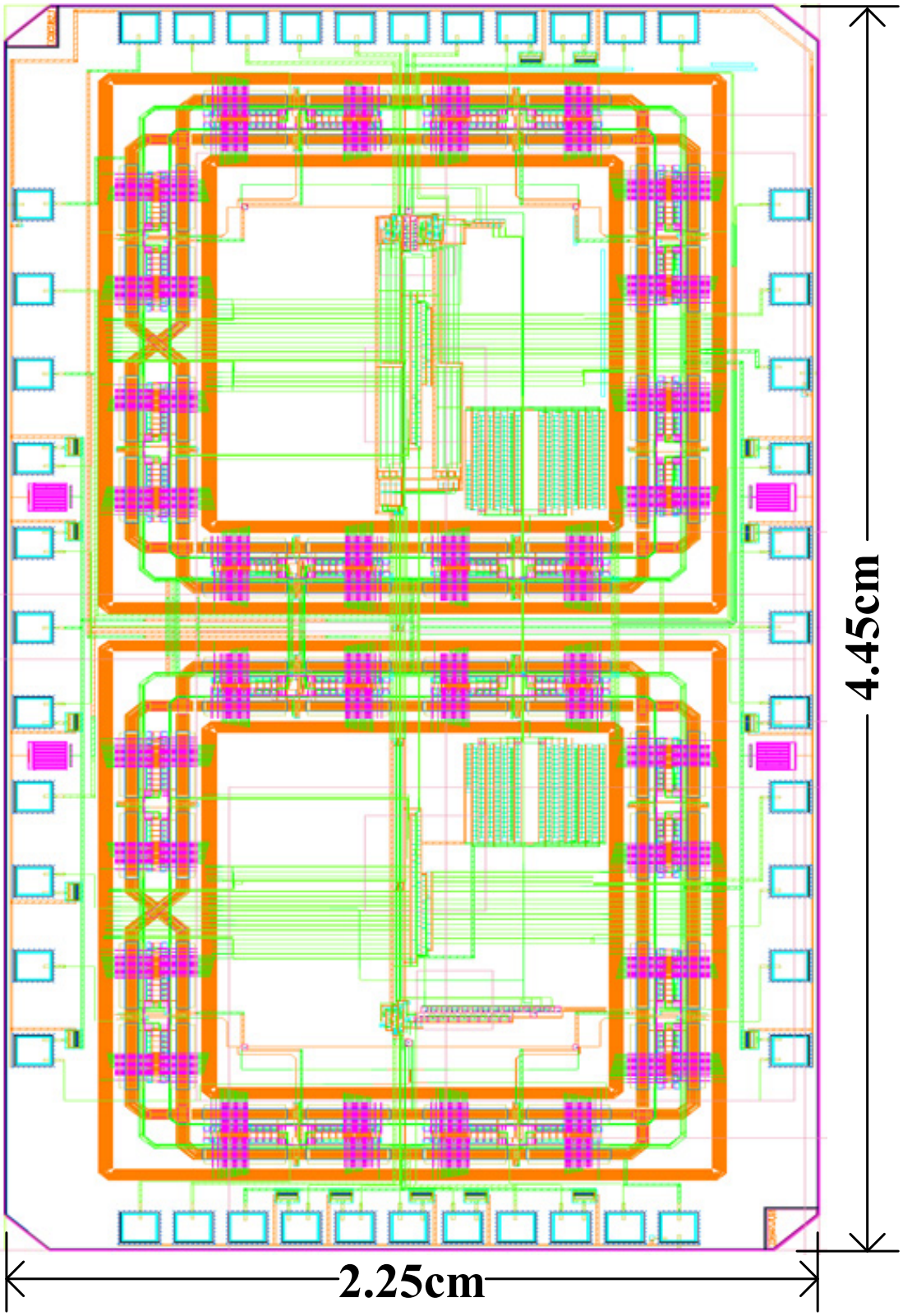

Fig. 5.3. The full layout view of the optimized IL-RTWOs and BIST

Chapter 6 : Prototype Implementation and Measurement Results

Two prototype chips have been fabricated in the standard 130-nm CMOS process to validate the main concepts in the proposed architecture. The first test chip implemented one IL-RTWO. The second chip implemented the clock distribution network with BIST circuitry. This second chip design is an extension of the first chip [115] with the optimization of the transmission line loop layout, buffer power supplies, PCB layout and on-chip parasitics, as well as, the addition of a large amount of digital test circuitry. The measurement setup is also optimized. A single poly-silicon, eight metal layers with two top level thick metals were available in the selected metallization option in this main stream process. Rf-lines made extensive use of the top two thick metal layers. Only a single IL-RTWO was implemented in the first prototype chip. Two optimized IL-RTWO elements together with the BIST circuit were integrated in the second prototype chip due to limited silicon design space available through the Canadian Microelectronics Corporation (CMC). Each RTWO-element consisted of a differential current injector, a pulse injector, an oscillator and buffer stages. Symmetrical decoupling caps were added to both chips to reduce the on-chip power supply noise and to satisfy the Design Rule Check (DRC) metal density requirements. The injection transconductor was directly coupled onto the oscillator tank while receiving its DC bias current through the centre tap of the differential oscillator tank. Both chips were packaged in a 44-pin Ceramic Quad Flat Package (CQFP) and mounted on a custom Printed Circuit Board (PCB). Both chips' I/O and power pads were arranged such that the functionality of each RTWO-element outputs can be fully monitored.

A 4-layer custom PCB was designed to test both chips. In order to reduce the cost, the top part of the PCB board is used to test the single IL-RTWO chip and the bottom part is designed for the optimized RTWOs with BIST circuit. The top and bottom layers of the PCB board are used for the signal path and the 2nd and 3rd layers are used for power supply and ground. This minimized the coupling effect and provided good decoupling between power and ground planes. A tunable resistor was soldered to the PCB to supply a tunable bias current for the RTWO injector. The PCB layout and the fabricated PCB are shown in Fig. 6.1 and Fig. 6.2.

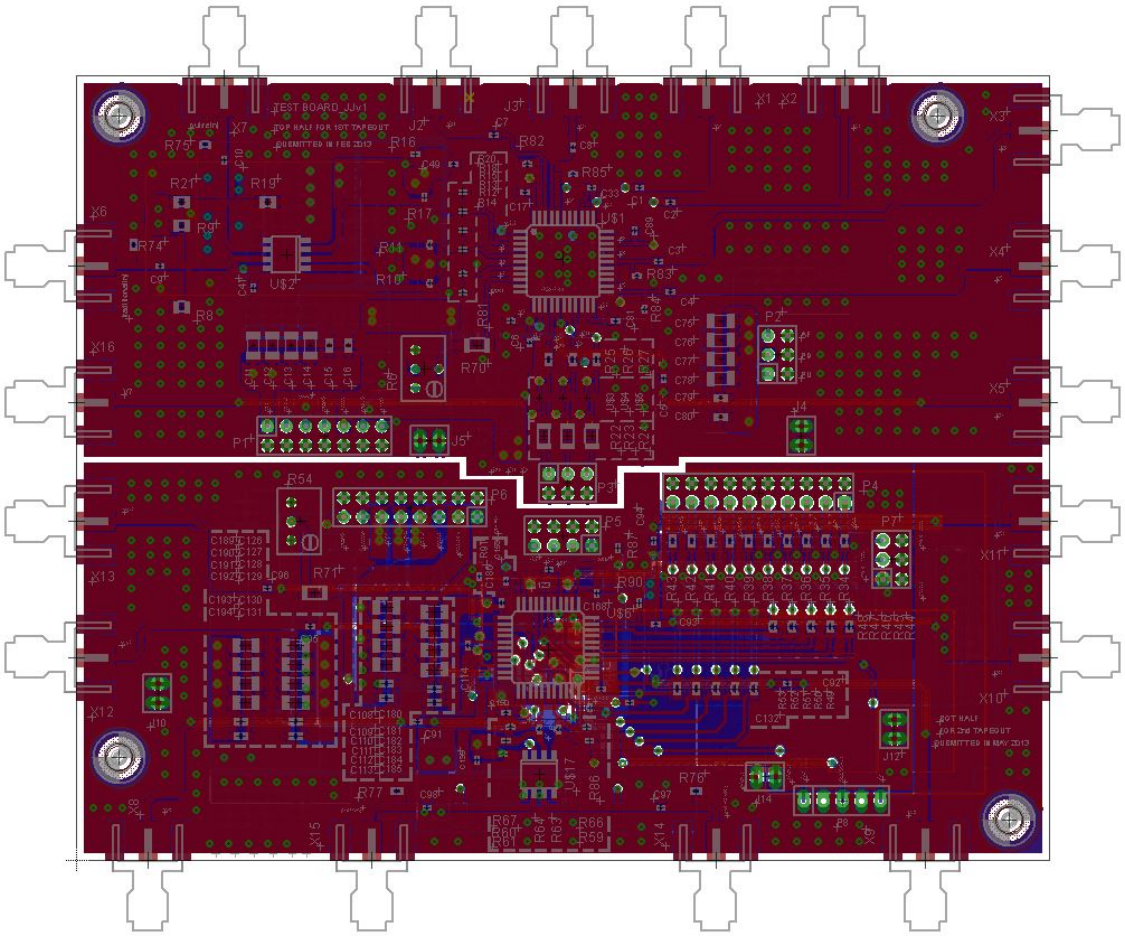

Fig. 6.1. The 4-layer customized PCB layout

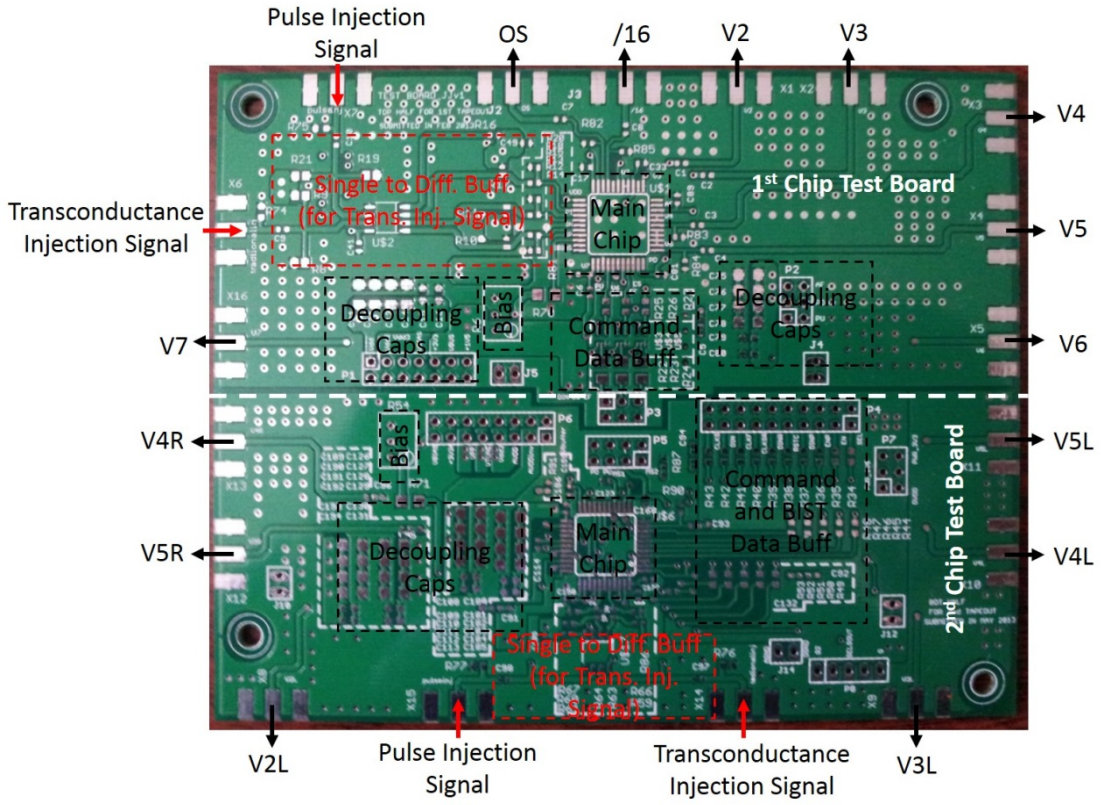

Fig. 6.2. The fabricated PCB

6.1 Model of Off-chip Parasitics

The off-chip parasitics are modelled as shown in Fig. 6.3. The 44 pin Ceramic Quad Flat Pack (CQFP) was chosen as the chip package. In simulation, the on-chip routing and bond pad parasitic capacitance and routing capacitance between bond pad and oscillator outputs are estimated to be 0.5pF in total based on [102]. The capacitance between bond wires is estimated to be less than 100fF and the serial parasitic inductance of the bond wires is estimated as 2nH with a Q of 50 [102]. Therefore, its parallel parasitic resistance is calculated to be 68Ω. Each pin package and PCB trace has a parasitic capacitance of 2pF and 3nH series parasitic inductance. The parasitic

capacitance introduced by the wiring of Complementary Varactor Pairs (CVPs) could be reduced with more careful layout.

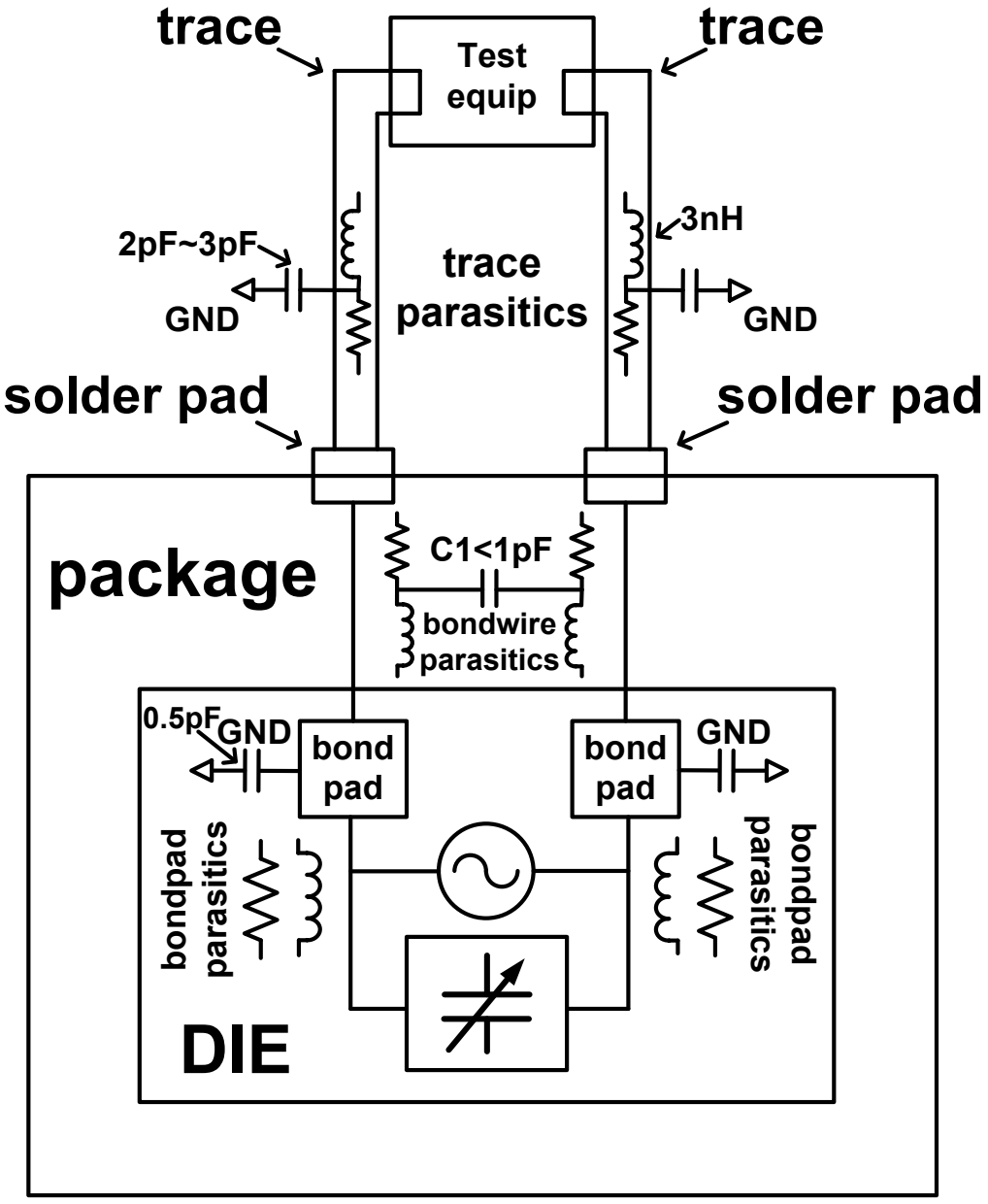

Fig. 6.3. Off-chip parasitics model

6.2 First Chip (Single IL-RTWO) Measurement Results

Fig. 6.4 shows the first chip micrograph of the IL-RTWO together with its test bench. The first chip occupies 2.5mm×2.5mm area and the RTWO ring requires 1.64mm×1.64mm of die area. In the free running mode, the RTWO is biased with a 1.2V supply and the oscillator core current is 11.3mA. The packaged chip together with all the off-chip components are mounted on the top part of the PCB board as shown in Fig. 6.5. The first chip phase noise plot under injection locking is plotted in Fig. 6.6. It shows the RTWO phase noise performance is dominated by the injection source within its 15MHz locking bandwidth. The IL-RTWO phase noise is -126dBc/Hz at a 100kHz offset frequency and -132dBc/Hz at 3MHz offset frequency. The IL-RTWO achieves an 89fs integrated rms jitter from 10kHz to 40MHz offset frequency.

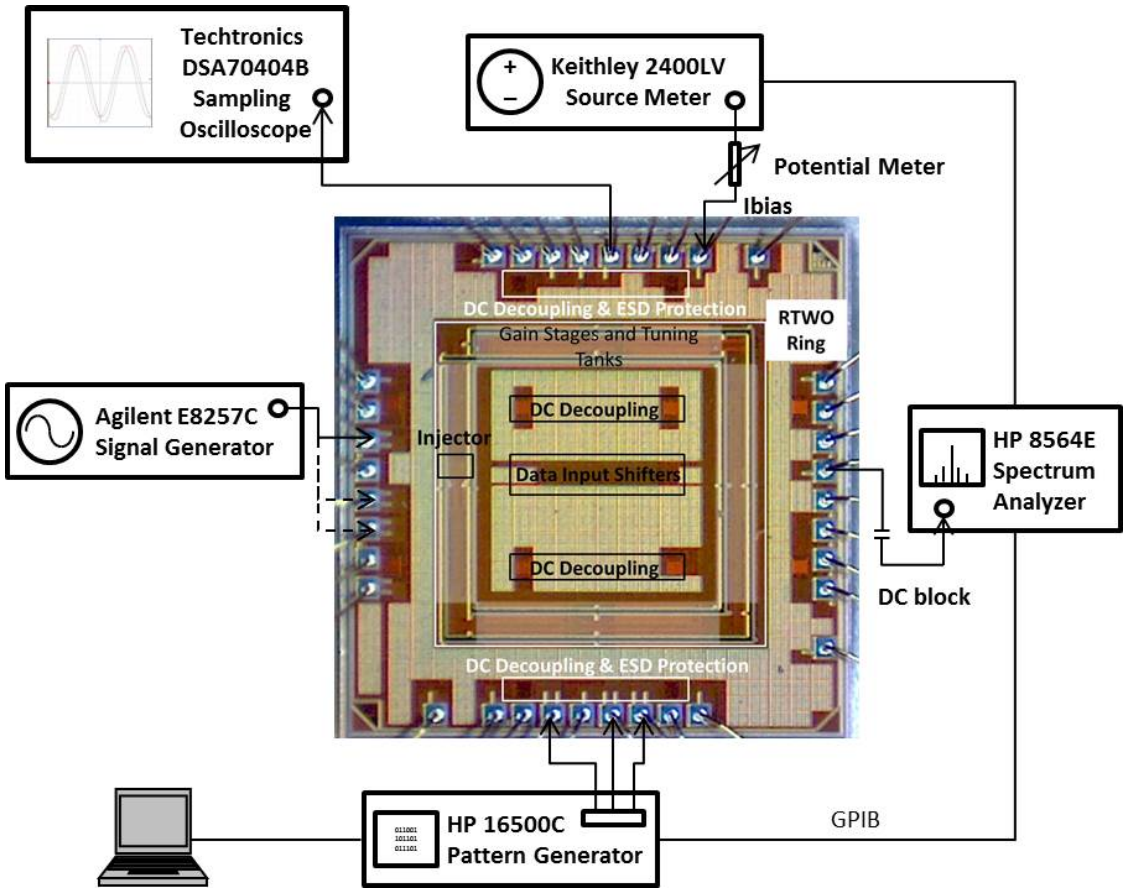

Fig. 6.4. First chip micrograph of the IL-RTWO together with its test bench

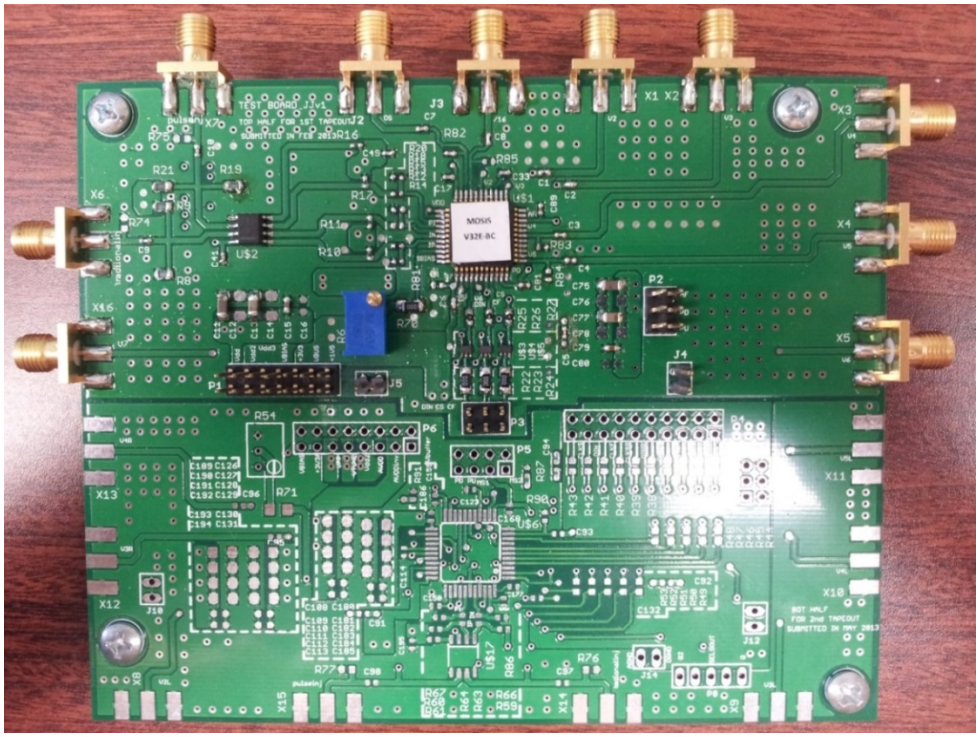

Fig. 6.5. The packaged chip with all the off-chip components mounted on the PCB board

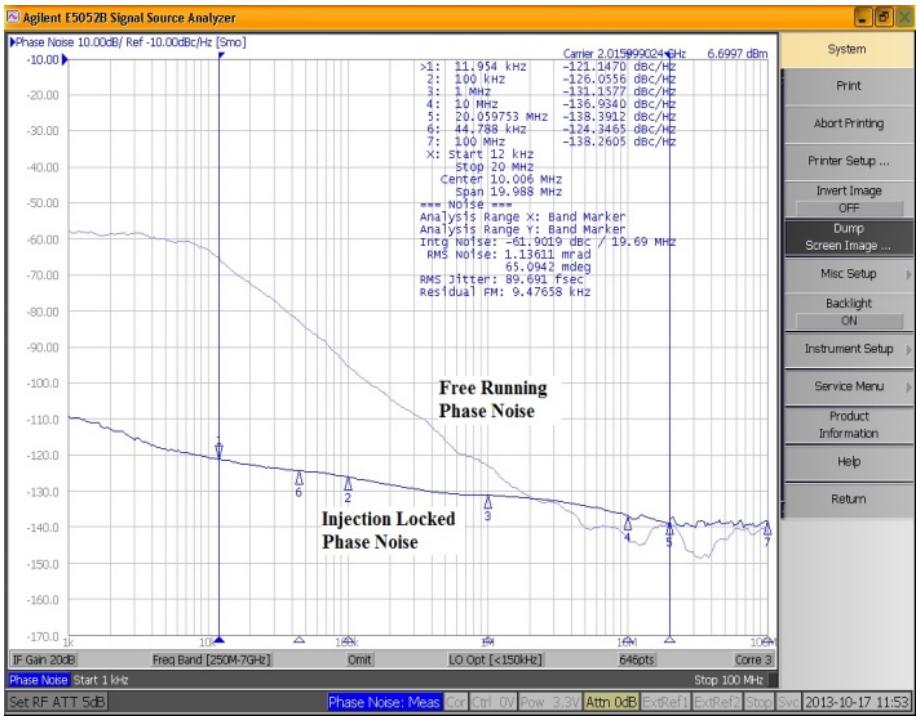

Fig. 6.6. Measured first chip RTWO phase noise under injection locking

6.3 Second chip measurement result – with both RTWOs optimized together with the BIST circuit

In Fig. 6.7, a photomicrograph of the 4.4mm × 2.25mm optimized IL-RTWOs with BIST can be seen. Fig. 6.8 shows the details of the frequency and time-domain measurement setup for the two RTWO-elements. A Rohde & Swarchz (R&S) SMA 100A signal generator is the source of the injection signal for the two RTWO elements. An off-chip single input to differential output buffer was used to realize differential injection signals from the signal generators. Despite the available differential outputs on the chip, only single-ended measurements were performed in both frequency and time domains. The frequency control bits were produced by an HP16500C data generator. The output signals were monitored by a Techtronics DSA70404B sampling oscilloscope in

the time domain and the HP8564E spectrum analyzer was used to observe the output spectrum. Keithley 2400LV Source Meters were employed to vary the power supply voltage and tune the injection pulse width. In the two RTWO-element test chip, the BIST pair takes a total area of 0.025 mm^2 in 130nm technology using larger than minimum size transistors.

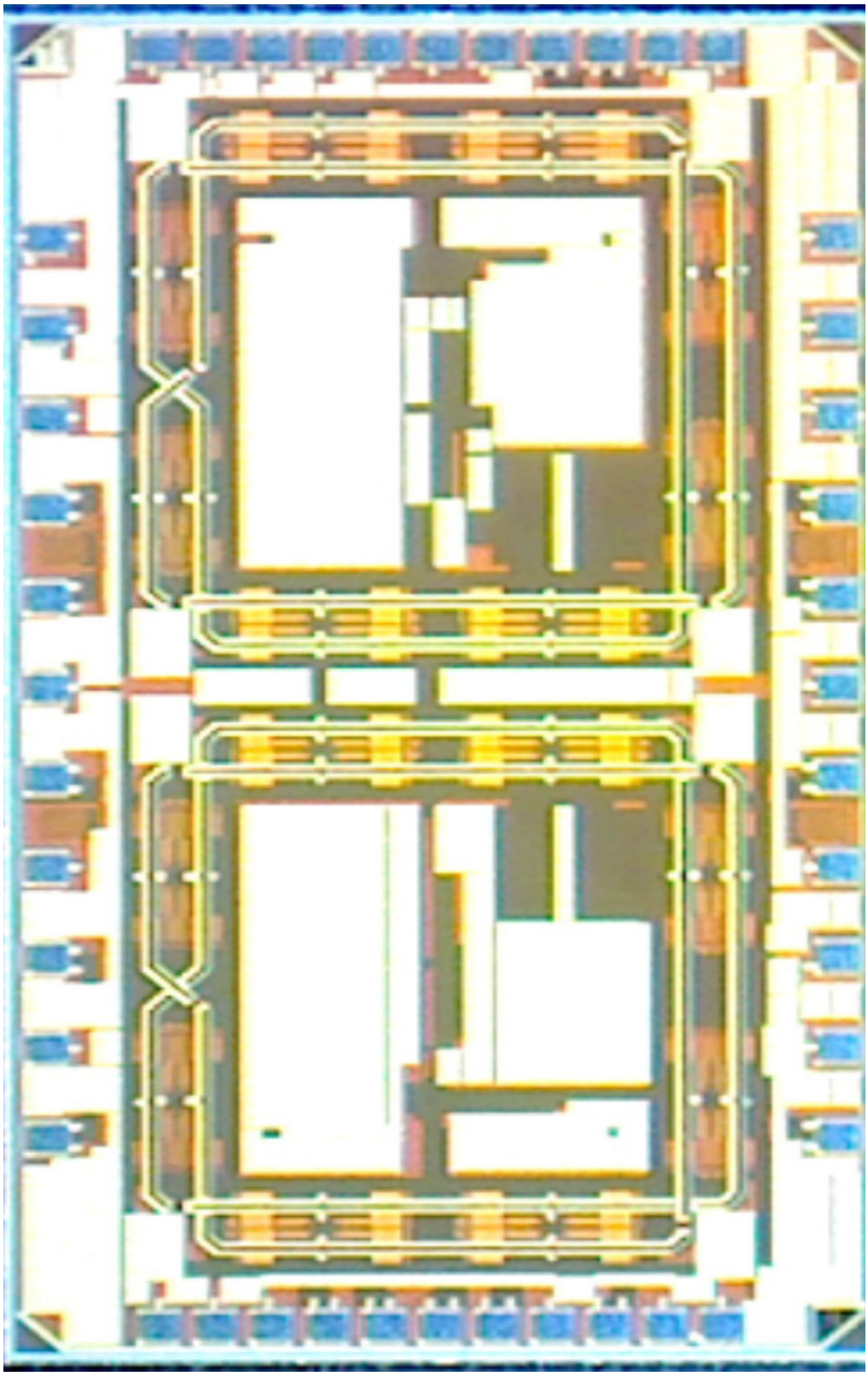

Fig. 6.7. Microchip of the IL-RTWOs with BIST under a microscope

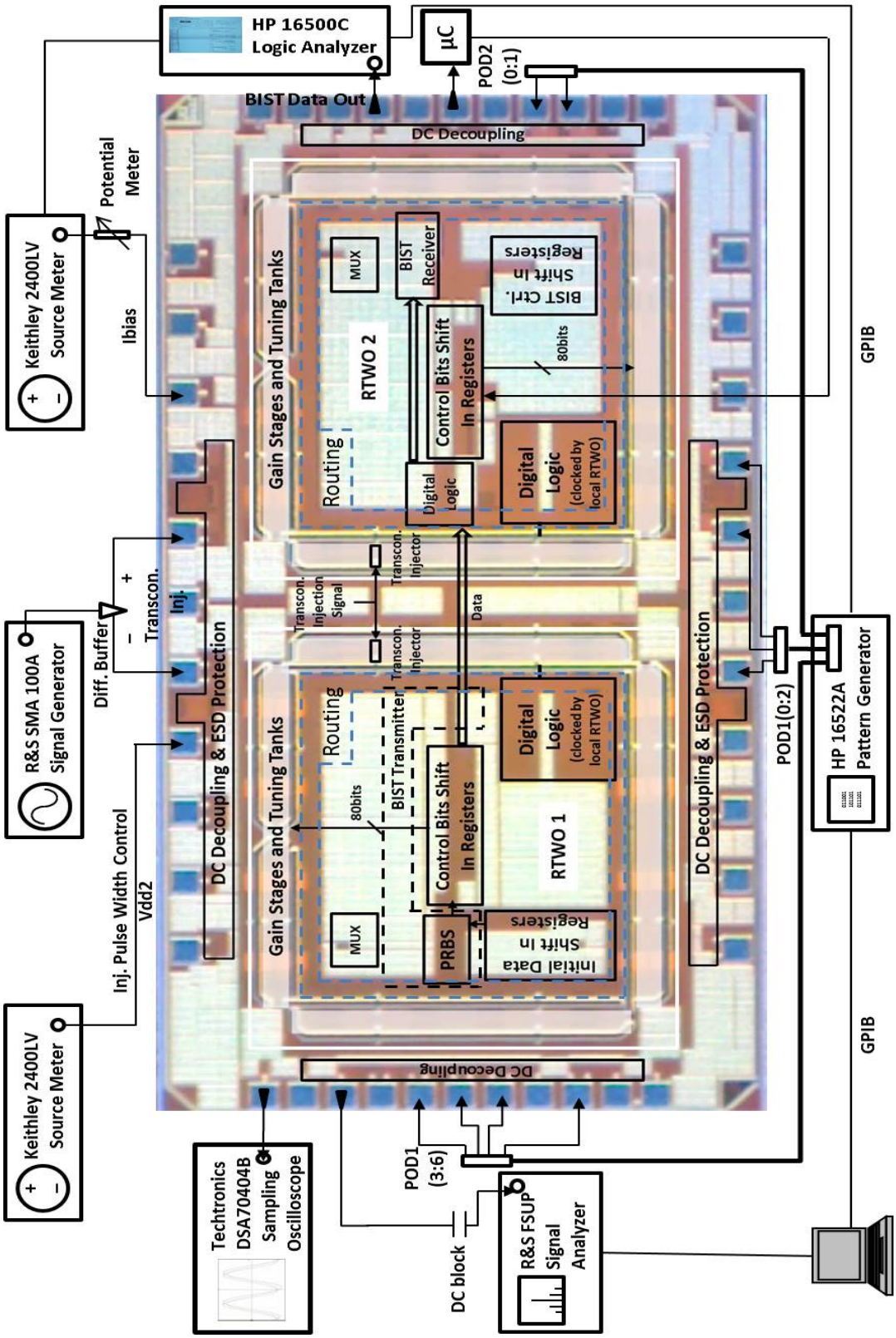

Fig. 6.8. Micrograph of the chip and its frequency and time domain measurement set up

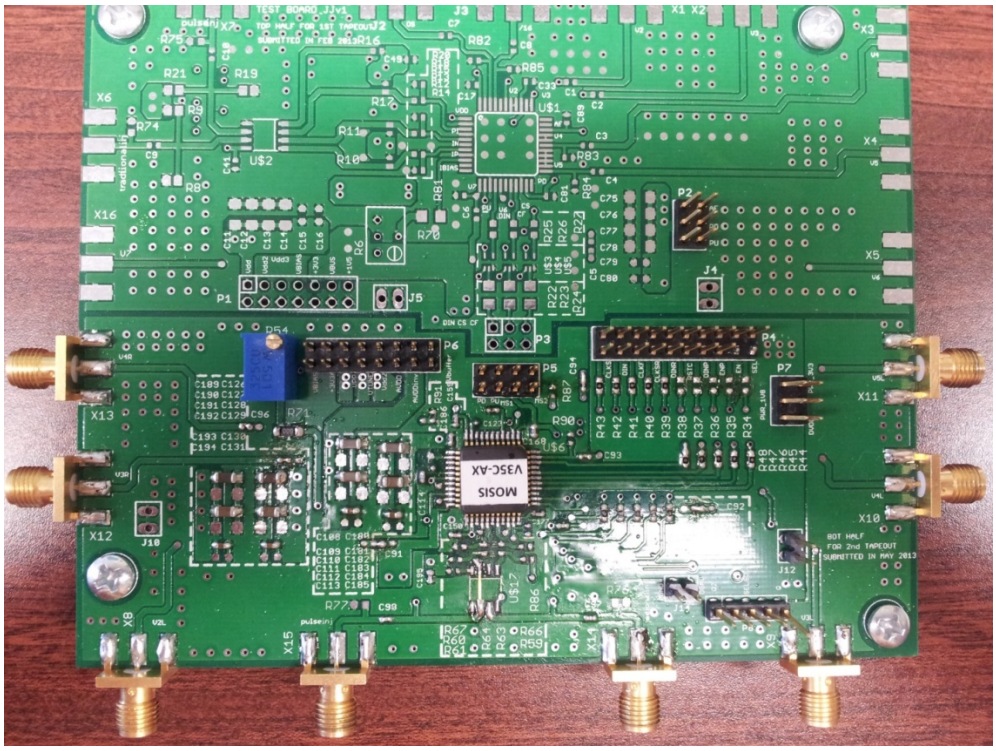

Fig. 6.9. The packaged second chip with all the off-chip components mounted on the PCB

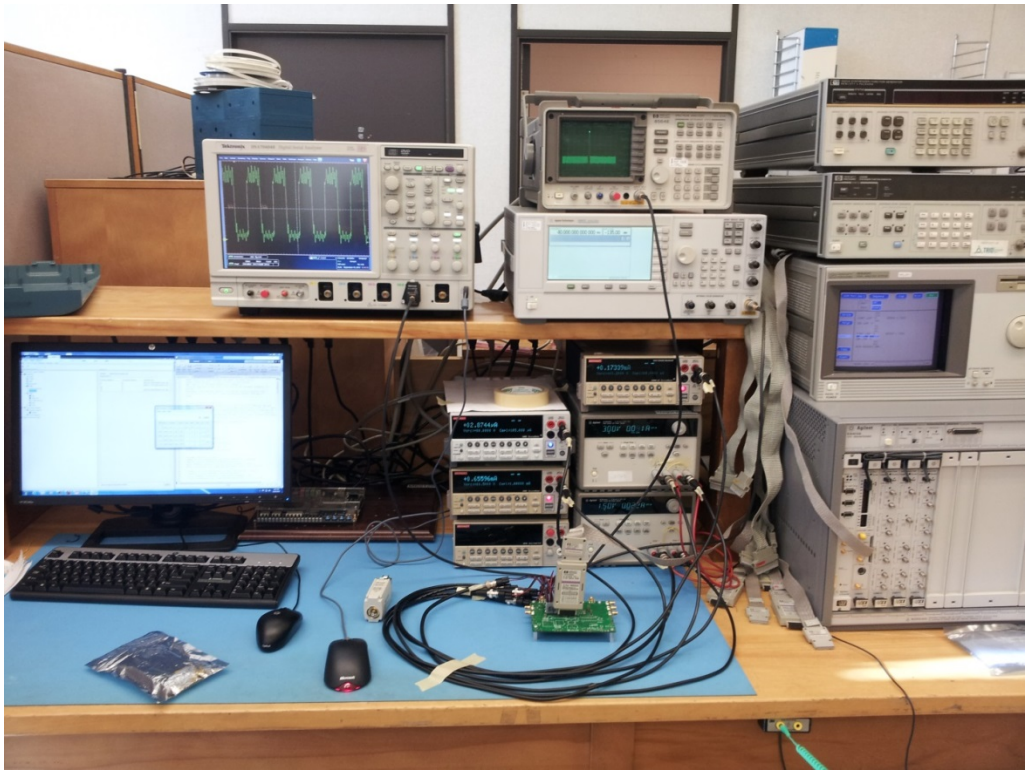

Fig. 6.10. A picture of the mounted chip under test

6.3.1 Optimized RTWOs' Free Running Frequency and Tuning Range

The optimized RTWOs have a coarse frequency tuning step of 1.2MHz, a medium frequency tuning step of 300kHz and a fine frequency tuning step of 100kHz. Therefore, three medium tuning steps are required to cover one coarse tuning step and three fine tuning steps are required to cover one medium tuning step. The medium tuning output frequency has deviations from the desired output frequency and the oscillator output frequency is not linearly related to the medium tuning codes; therefore, a Look Up Table (LUT) is required for calibration. Both the coarse tuning deviations and the frequency non-linearity can be calibrated by choosing the correct coarse, medium and fine tuning code combination from the LUT. The design provides frequency overlap to guarantee monotonicity. The tuning banks are sensitive to the capacitor process variations. The final frequency tuning plot is shown in Fig. 6.11.

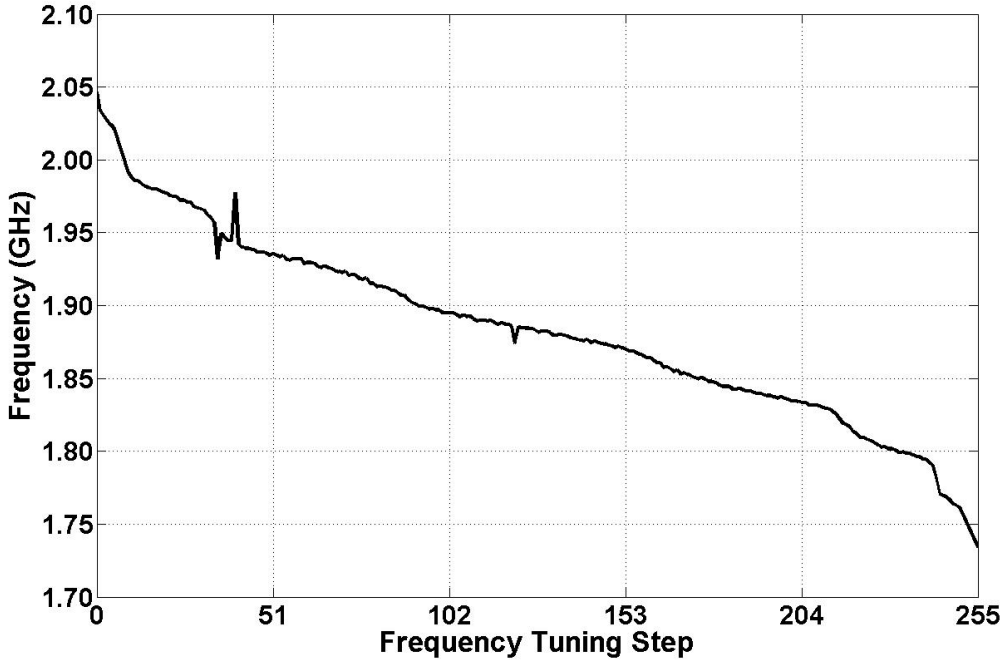

Fig. 6.11. 2nd chip final frequency tuning plot

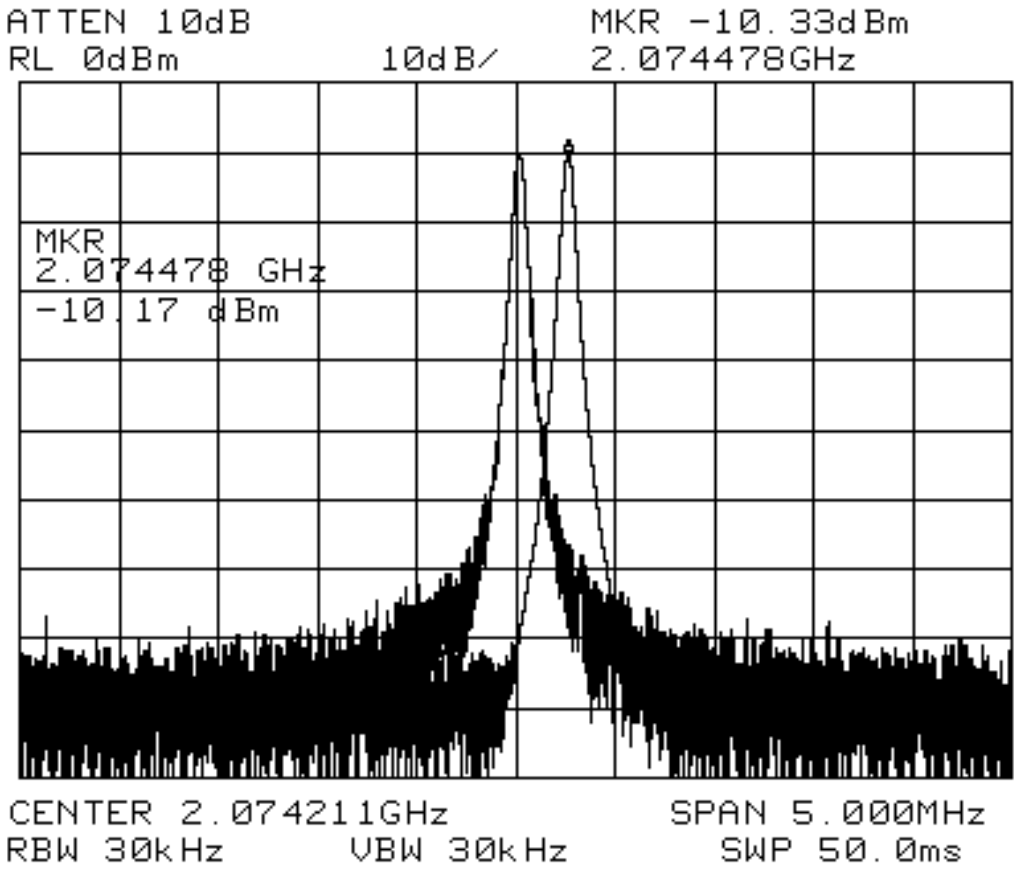

Fig. 6.12. Optimized RTWOs' output spectrum

Simulations indicate single ended power level of -9.3dBm into a 50Ω. There is a combined attenuation of less than 1dB at 2GHz due to the bonding wires and PCB traces. An output power level of approximately -10dBm has been predicted. This is in good agreement with the measured output power of -10.3dBm in Fig. 6.12 at one of the RF ports. The medium frequency tuning step is also measured in Fig. 6.12. The output frequency difference between the two outputs is 300kHz which agrees with the expected medium frequency tuning step.

6.3.2 Phase Noise and Integrated Jitter Measurements

The measurement of the phase noise on a spectrum analyzer should also be carefully considered. Due to the limitation of the test equipment, the noise power is normally not integrated over a 1-Hz bandwidth. The spectrum analyzer down converts the incoming signal to baseband through an analog IF filter and a digital video filter as shown in Fig. 6.13. Therefore, the phase noise reading depends on the IF filter resolution bandwidth (RBW) in a spectrum analyzer [126]. Therefore, a phase noise reading of -100 dBc with an RBW of 10Hz in a spectrum analyzer would be -90dBc with an RBW setting of 100Hz.

The video filter bandwidth (VBW) filters noise for easier identification and measurement of low-level signals. The VBW can be made less than 1% of the RBW. The Power Spectrum Density (PSD) reading is normally SSB, therefore, proper sweep settings are required to obtain symmetric sideband measurement. It should be noted that sweeping too fast can result in an uncalibrated display of sidebands [126].

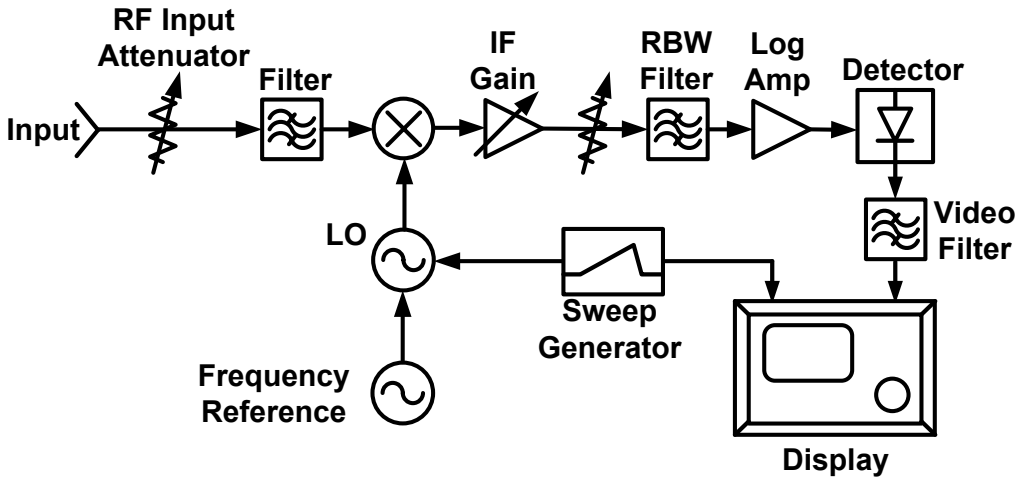

Fig. 6.13. Spectrum Analyzer basic block diagram. [126]

The measured free running phase noise is plotted in Fig. 6.14 and compared to the simulation results. It is believed that the approximately 6 dB increase in phase noise is due primarily to power supply noise, the parasitics caused by PCBs and extractions and the accuracy of the noise model.

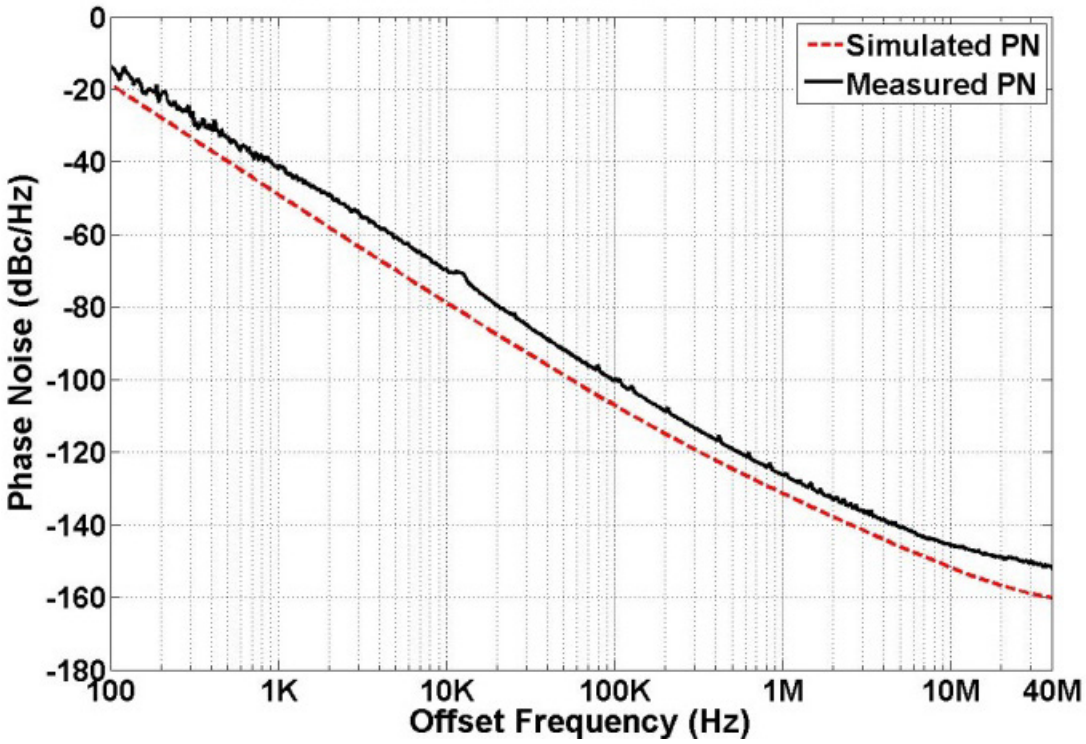

Fig. 6.14. Simulated schematic phase noise and measured RTWO free running phase noise comparison at 2GHz output

A 679MHz reference signal from the Rohde & Schwarz signal generator and one buffer are required instead of many high frequency (2.04GHz) buffers (typically found in classic clock distribution networks) are distributed through the injector. The RTWOs can be injection locked with a square wave of -10dBm but typically the injection signal on-chip would be a full swing 0 to 1.5V signal which can supply an injection power of more than 10dBm (the RTWOs' input impedance is designed to be close to 50Ω). The

measured free running phase noise versus the pulse injection locked phase noise is shown in Fig. 6.15. Fig. 6.15 shows the unlocked RTWO phase noise is -126dBc/Hz @ 1MHz offset frequency.

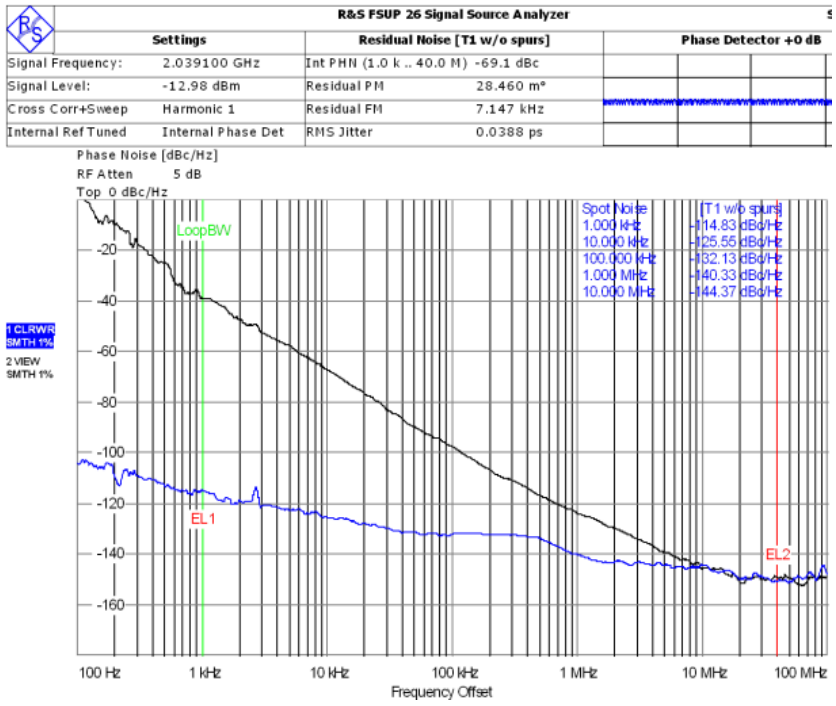

Fig. 6.15. Measured pulse injection locked phase noise vs free running phase noise

Fig. 6.16 and 6.17 compare the injection locked phase noise vs. the reference signal source phase noise using pulse injection and trans-conductance injection respectively. The injection locked phase noise measurements were performed on one of the RTWOs while both RTWOs were injection locked using a third harmonic signals. For Figs. 6.16 and 6.17, the blue curve is the injection locked phase noise and the black curve is the reference signal phase noise. The RTWOs are injection locked at 2.039GHz and their phase noise performance is dominated by the injection source within its locking bandwidth. For the pulse injection locked RTWO (Fig. 6.16), the rms jitter at 2.039GHz is 39fs from 1kHz to 40 MHz offset frequency. The transconductance and pulse injection

locked RTWOs have inband phase noise of -128dBc/Hz and -132dBc/Hz at 100kHz offset frequency from the 2.039GHz output frequency. The phase-noise performance of the injected third-subharmonic signal (i.e., 679MHz) was measured to be -143dBc/Hz at 100kHz offset frequency. The performance of prior art is listed in Table 6.1 for comparison. Table 6.1 shows the IL-RTWO achieves the best integrated rms jitter, phase noise and Figure Of Merit (FOM) at its operating frequencies.

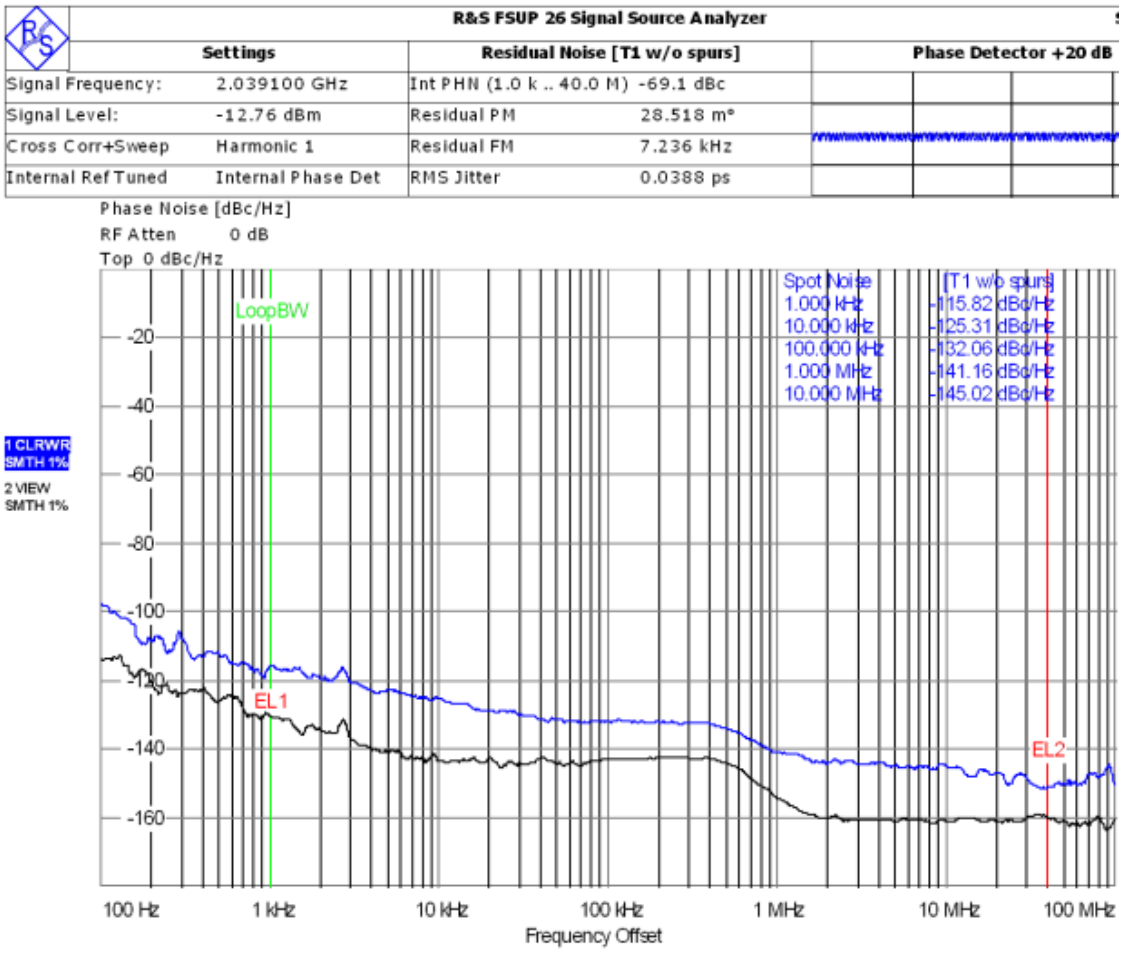

Fig. 6.16. Measured Pulse injection locked phase noise vs signal source phase noise

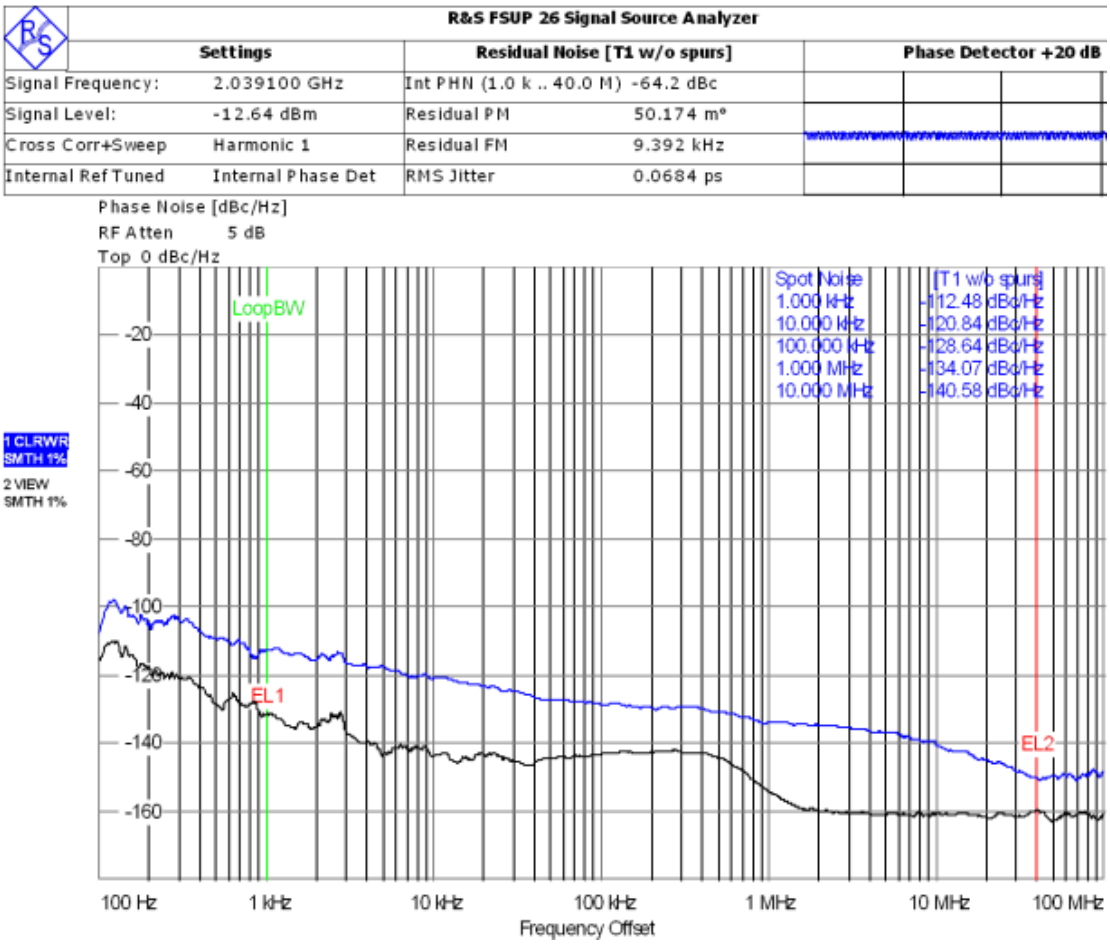

Fig. 6.17. Measured trans-conductance injection locked phase noise vs signal source phase noise

Table 6.1 Performance and comparison

	[61]	[110]	[113]	[98]	[100]	[114]	[117]	This work
Output Freq (GHz)	3.5	3.2	1.6	2.1	2.4	2.2	2.4	2
PN,100kHz offset freq (dBc/Hz)	-94	-122	-110	-103	-70	-125	-124	-132
PN,1MHz offset freq (dBc/Hz)	-121	-127	-117	-134	-104	-124	-129	-141
RMS jitter	N/A	130fs (0.1k~40 MHz)	678fs (1k~40M Hz)	N/A	N/A	150fs (10k~40 MHz)	145fs (1K~40 MHz)	39fs (1k~40 MHz)
Power (mW)	50	28.6	5.1	28	37.5	2.5	22.7	30.2
Die Area (mm^2)	0.56	0.4	0.06	3.4	1.73	0.18	0.64	1.04
architecture	RTWO	LC oscillator	Ring oscillator	LC oscillator	Ring oscillator	LC oscillator	LC oscillator	RTWO
FOM (dB)	N/A	-243	-236	N/A	N/A	-252	-246	-253
Tech.	0.11 µm CMOS	0.13µm CMOS	0.13µm CMOS	0.18µm CMOS	0.13µm CMOS	0.18µm CMOS	0.18µm CMOS	0.13µm CMOS

The phase noise plot with power supply variations from 1.25V to 1.5V are shown in Fig. 6.18, where the injection locked RTWO phase noise increases by 1.57dB at 100kHz offset frequency with a worst case 1.25V supply.

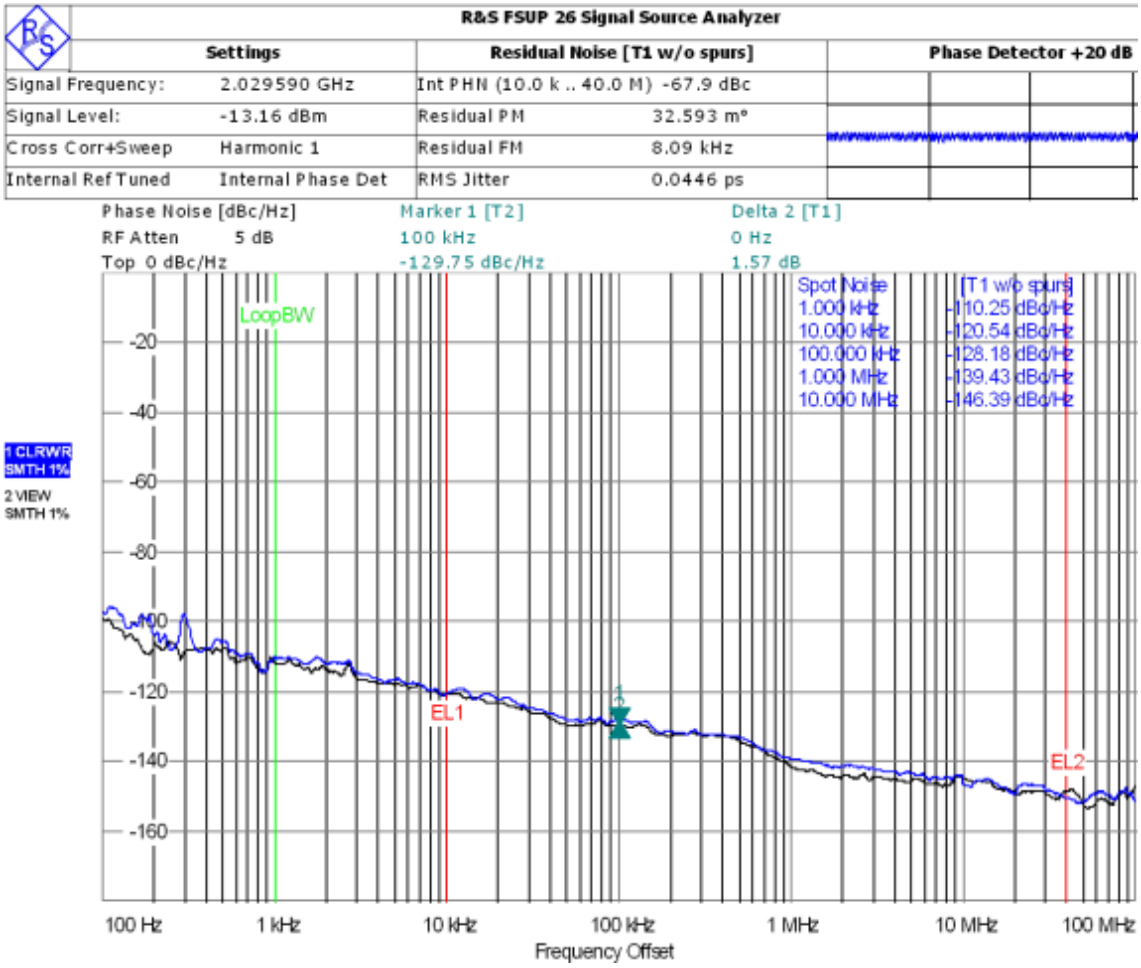

Fig. 6.18. Phase noise plots with power supply varies from 1.25 V to 1.5 V

Local digital circuits are clocked by the two RTWOs at 2GHz to test the RTWOs' phase noise immunity to correlated digital noise. The measurement result is shown in Fig. 6.19. Fig. 6.19 shows that the phase noise performance degrades by only 0.37dB at 100kHz offset frequency when digital noise from 1,000 inverters and 350 flip flops (12,000 transistors in total inside each RTWO) are clocked by the local RTWOs.

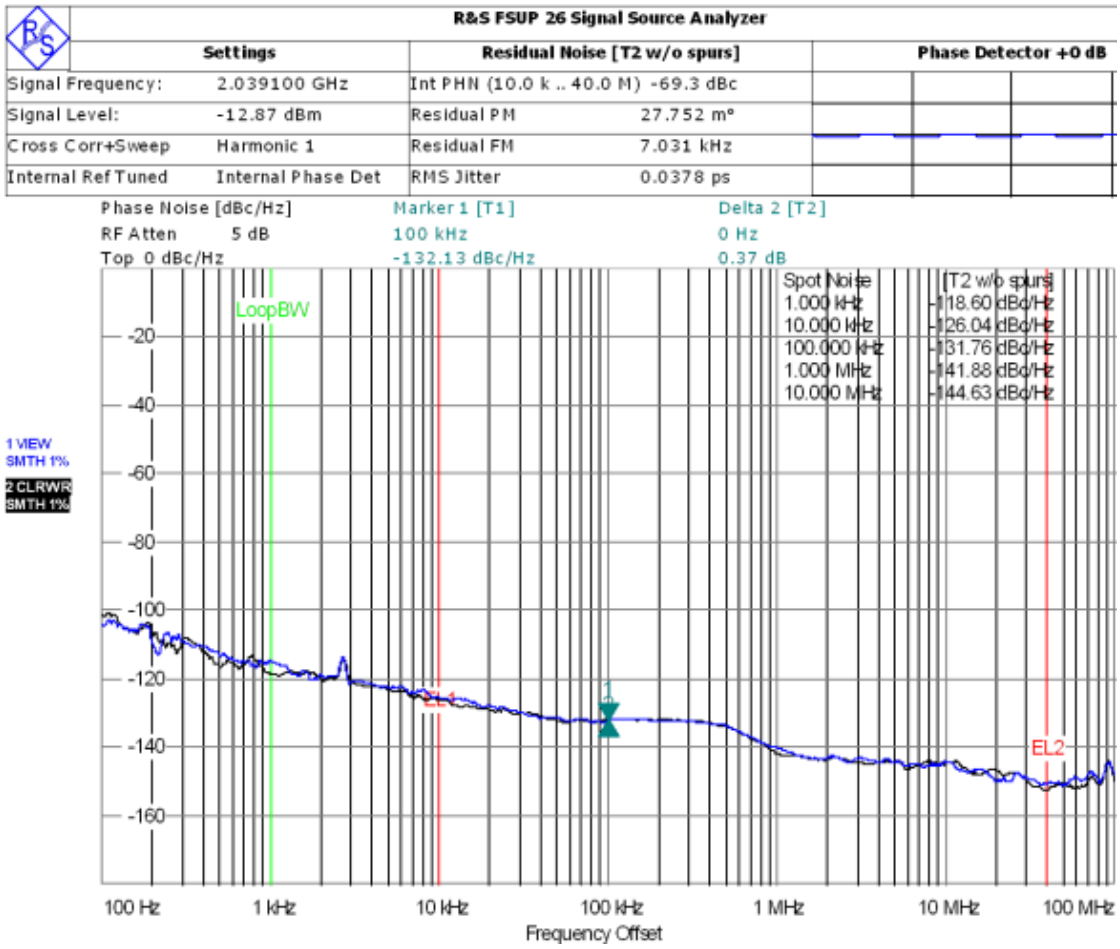

Fig. 6.19. Phase noise plots with digital switching noise on/off

The injection locked RTWO output spectrum with 40MHz bandwidth is shown in Fig. 6.20. Fig. 6.20 shows there are no spurs above -79 dBc. The wideband spectrum of the IL-RTWO is shown in Fig. 6.21. Fig. 6.21 shows there are some intermodulation products between the reference frequency and the IL-RTWO output frequency from the offset by the reference frequency (the reference frequency is 37dB below the output frequency power as shown in Fig. 6.21). However, the intermodulation products are more than 47dB below the output frequency power.

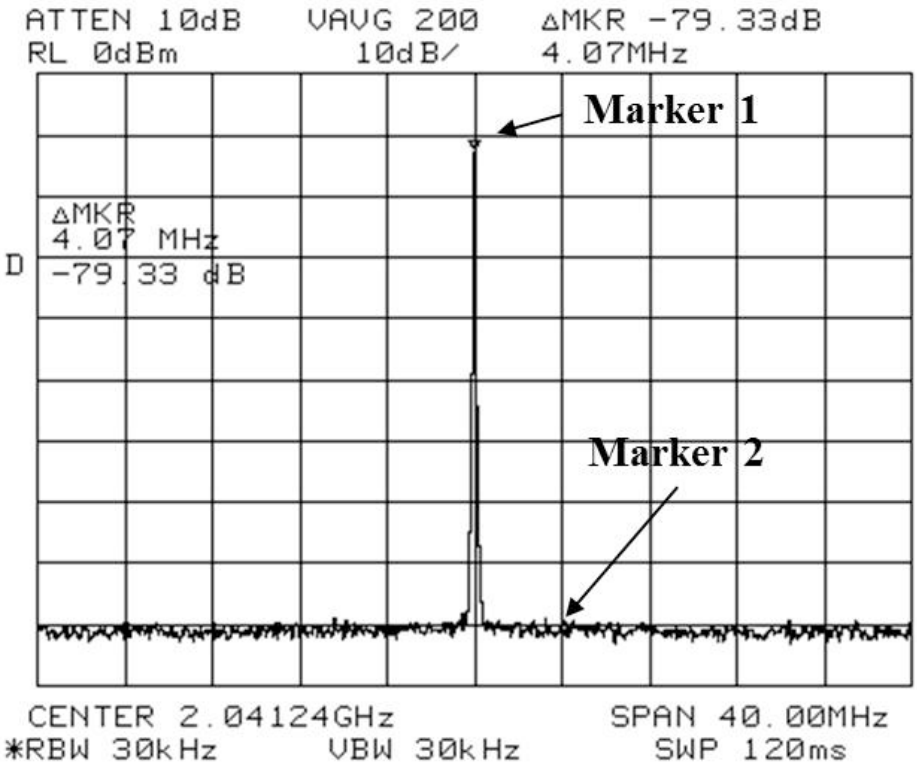

Fig. 6.20. Injection Locked RTWO output spectrum with 40 MHz bandwidth

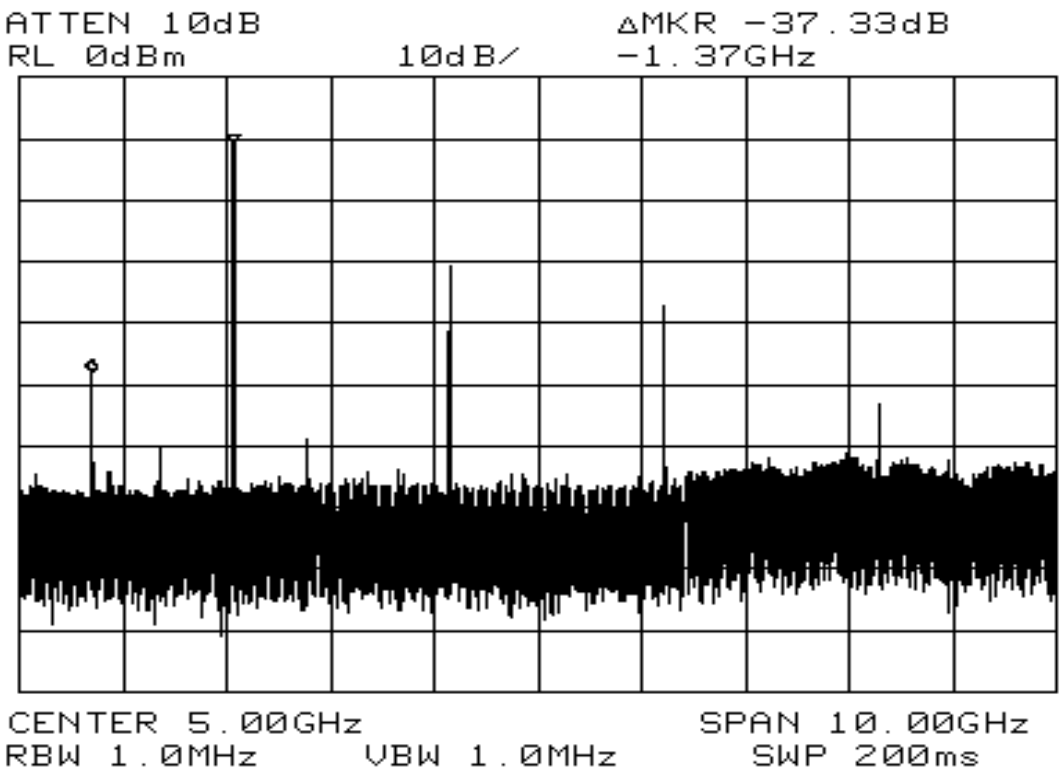

Fig. 6.21. The IL-RTWO broadband spectrum

6.3.3 Phase Shift Measurements of One RTWO-element

With the two RTWO-elements simultaneously running on the same die, element to element delta phase shift measurements were made possible. Phase shift measurements have been performed for one RTWO-element relative to an external 679MHz synchronized reference. The spectra of the output signals were monitored by the HP8564E spectrum analyzers while the two time-domain signals and their relative phase relationships were monitored by a Techtronics DSA70404B sampling oscilloscope. The tests were fully automated and set by a MATLAB program which was developed to control the programmable Keithley power supplies. The fact that, with this proposed technique, the oscillator does not need to operate near the edge of its locking bandwidth

explains the observed relative independence of the obtained phase shift from the phase noise performance.

The injection locked RTWO transient waveforms at Phase Tuning Word A (PTWA) and Phase Tuning Word B (PTWB) are shown in Fig. 6.22 and Fig. 6.23. Fig. 6.22 and Fig. 6.23 show the transient waveforms at tapping points v4 and v5 at an oscillator frequency of 2.04GHz. The delay between v4 and v5 changes from 31.25ps to 30.87ps. The use of multiple tapping points and variable CVP sizes results in more than 58° of RTWO phase tuning range with a 0.34° worst case phase tuning resolution. This directly translates into 80ps of clock deskew range and a worst case skew variation step size of 0.47ps at 2.04GHz. The phase resolution measurement is limited by the test equipment. The absolute phase shift between different tapping points is uneven due to the mismatch in the signal path. However, in a clock distribution network, it is the difference in phases that is critical rather than the absolute phase shift.

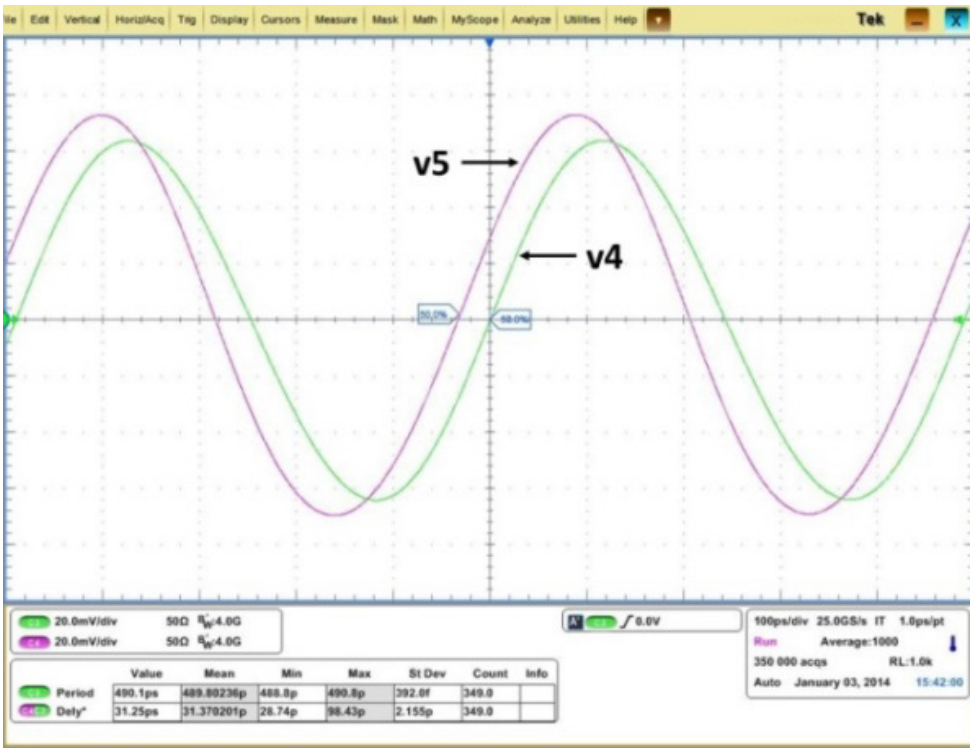

Fig. 6.22. Measured Injection locked transient waveform PTWA

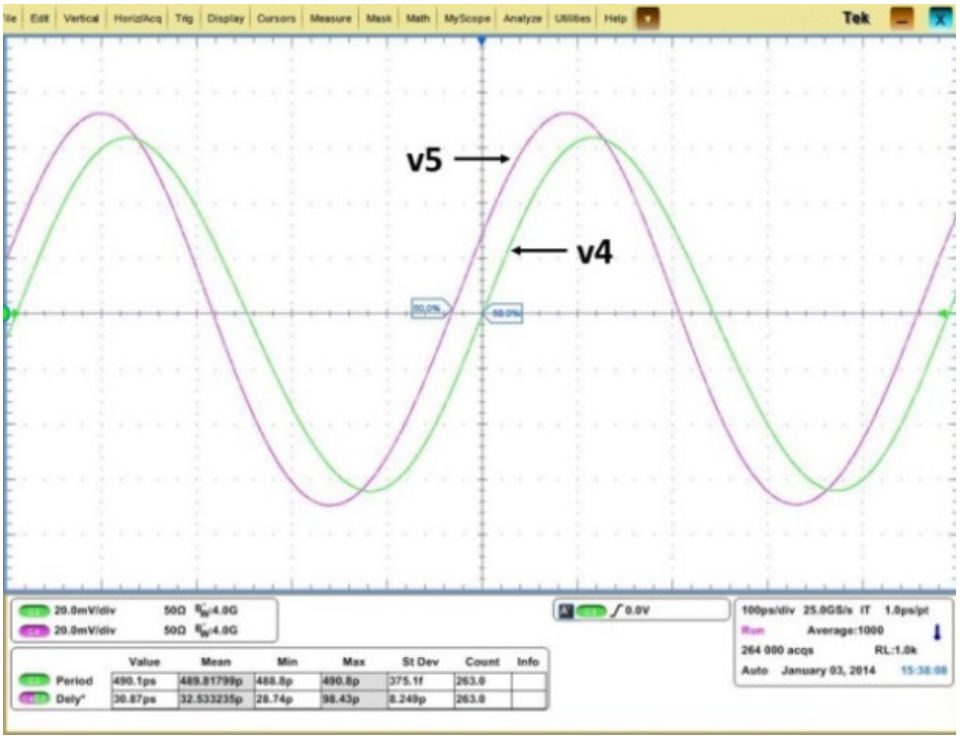

Fig. 6.23. Measured Injection locked transient waveform at PTWB

It is worth mentioning that there is an output amplitude difference between v4 and v5, which is caused by the amplifiers that buffer the signals off-chip. The effect of output amplitude variation on phase measurements is minimized by directly AC coupling to the DSA70404B sampling oscilloscope and measuring the signal at the zero crossing points.

6.4 The BIST simulation and measurement results

The calibration flow chart of the BIST circuit is shown in Fig. 6.24. The initial words are loaded into the PRBS first. Next, the counter is reset. Then, the enable signal rising edge triggers the PRBS clocked with RTWO1. The PRBS generates data for fixed number of clock cycles which is counted by the 10-bit counter located on RTWO1. When the enable signal goes low, the PRBS stops generating data and the counter is frozen. The SA data is prepared for the SPI controller and shifted out for comparison. If it is correct, true counter counts up by one; otherwise, the false counter counts up by one. This procedure is repeated multiple times and a Bit Error Rate (BER) is cal-culated.

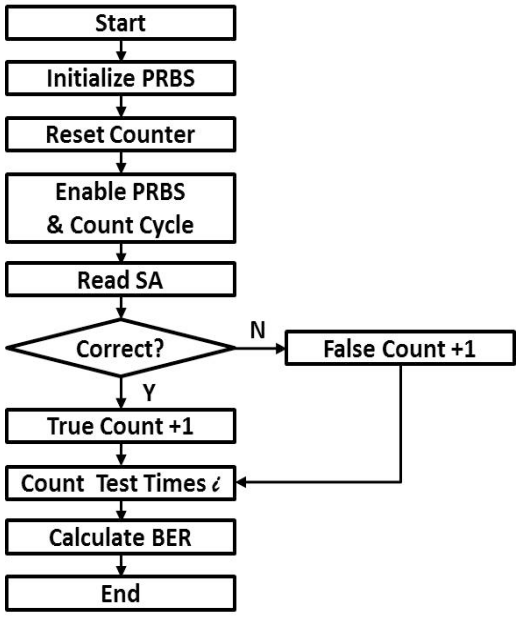

Fig. 6.24. The calibration flow chart of the BIST

The current design uses 15 test patterns. This can easily be extended using a larger PRBS. During calibration, the pattern generator is typically run multiple times (1000 times for each test). The direction of the RTWO output phase is known by varying the CVP's capacitance. As the capacitance before a given taping point in the ring is increased, the output signal is delayed and phase increased [59], [61]. To maintain the same free running frequency the total CVP capacitance is held constant but phase at different points is varied by adjusting the CVPs. Given that the direction of the phase is known, an algorithm can simply step from minimum phase to maximum phase by adjusting the CVPs and selecting the appropriate tapping point. The algorithm can scan from the minimum phase to maximum phase and at each step the BER is measured. The ideal phase is selected to be at the center of minimum BER section of the curve. To ensure low BER, only the phase tuning range should be important. However, at higher speeds, higher phase resolution is required. The high phase resolution is required to accurately determine the knees of the BER curve. With smaller phase tuning steps, the distance to the center point of the BER curve can be more accurately determined. This design targets to plot the BER curve to an accuracy of 1e-3. The designer only needs to find the approximate center of the curve which is the central clock skew point between the knees of the BER curve as show in Fig 6.25. From simulations, the maximum allowed clock skew without incurring skew violations is +64/-105 ps from its central value.

The simulated and measured BIST BER results are shown in Fig. 6.25. The measured BIST results are +59/-102 ps from its central value. In the test, the BIST calibration algorithm scans through the BER curve with different clock skews to find the

two corners where errors start increasing. A simple algorithm with thirty equally spaced steps is taken and the pattern generator is typically run 1,000 clock cycles at each scan step. This results in 15µs calibration time for each RTWO pair ($500\frac{ps}{cycle} * 1{,}000\ cycles * 30\ steps = 15\mu s$).

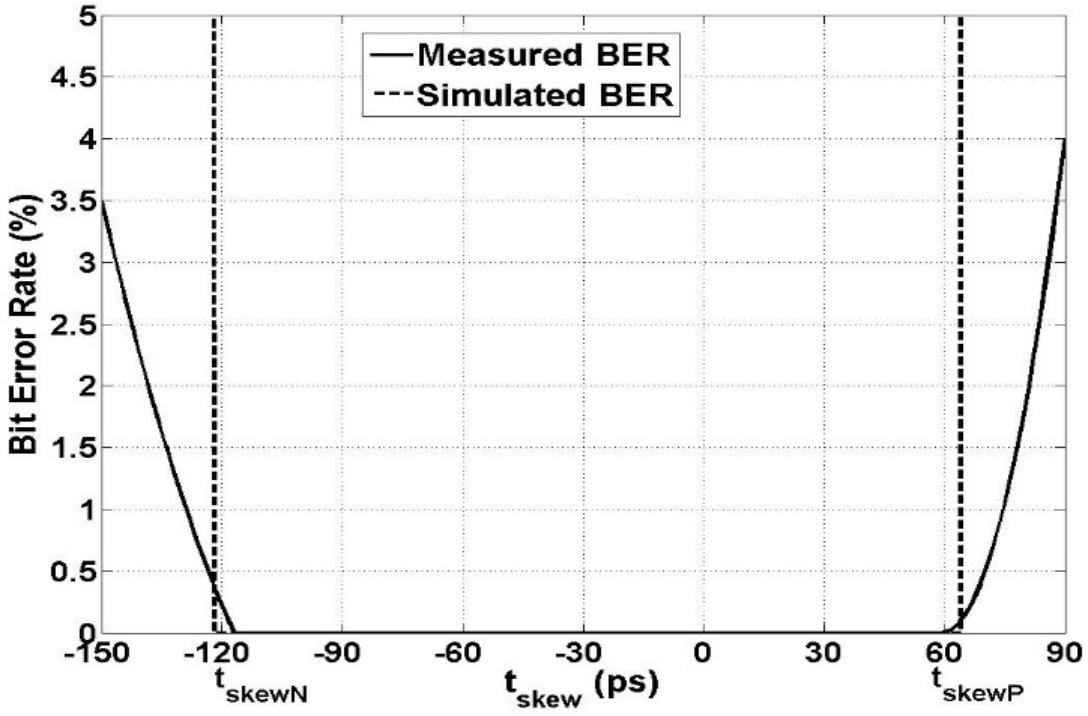

Fig. 6.25. BIST measurement result

Normally, BIST would only be performed during startup. By using BIST and centering the operating point between the minimum and maximum delays designer provide a large margin for variation in skew with temperature or voltage. For some applications, if the temperature and voltage skew variation is greater than the available skew margin it may be possible to stop the digital circuits and rerun the BIST calibration, however, this design does not anticipate that this would be commonly used.

For a specified chip area, N RTWOs could be implemented and the number of BIST pairs required is calculated as,

$$Nbist = N * (\frac{N}{2} - 1) + N/2$$

N/2 independent pairs can be calibrated in parallel, therefore, the total calibration time for N RTWOs is calculated as,

$$t = \left[Nbist/(\frac{N}{2})\right] * t_{bist} = (N-1) * t_{bist}$$

where t_{bist} is the single BIST pair calibration time. For example, with a 16 RTWO network the total BIST calibration time would be 225 us assuming 15 μs per BIST pair.

6.5 The measurement results summary

The implementation of an IL-RTWO with BIST has been presented. The first chip focused on high frequency resolution and explored the CVP and injection locking techniques implementations with RTWO. A 20kHz frequency resolution RTWO with -126dBc/Hz phase noise @100kHz from 2GHz operating frequency is achieved. The second chip explored a clock distribution network with Injection Locked Rotary Traveling Wave Oscillators (IL-RTWOs) and BIST technique. The RTWOs are optimized in the second chip and the BIST technique is explored to detect and adjust clock skews in the developed clock distribution network. The optimized RTWOs achieve a phase noise performance of -132dBc/Hz @100kHz from 2.04GHz operating frequency. Both transconductance injection locking and pulse injection locking techniques are explored. The reported phase noise, integrated rms jitter and FOM are the best at its operating frequency. The pulse injection locking technique tends to achieve better phase noise performance which agrees with the discussion in session 3.5. The Complementary Varactor Pairs (CVPs) implemented for RTWO phase tuning achieves 56° phase tuning

range and 0.34° worst case phase tuning resolution. The BIST technique are successfully implemented to detect clock skews. To the author's best knowledge, the implementation of CVPs and injection locked techniques on RTWOs, and the implementation of this BIST technique to determine clock integrity of an injection locked clock distribution network have not been explored previously.

Chapter 7 : Conclusion

Clock jitter and skew play critical roles in clock distribution design. However, the accurate evaluation of jitter for a given clock tree topology is not only complicated to establish but also exceedingly time consuming due to many different dependent/independent parameters such as power supply noise, clock driver size, physical structures of interconnects, number of clock stages, etc.

To this end, this project proposes the IL-RTWOs with BIST for clock distribution network. The proposed architecture is a sound choice to simplify the clock distribution structure and reduce cascaded buffers and their related jitter and power consumption in multi-GHz clock processors. This research also strives to develop a purely digital Built-In Self-Test (BIST) circuit to detect clock skew which will be eliminated by phase tuning the Injection Locked- RTWOs (IL-RTWOs). The incorporation of the BIST circuit takes advantage of on-chip communications. The BIST circuit does not rely on external test equipment and allows the chip to be tested more easily and efficiently. This clock distribution network will benefit from lower cost due to reduced die size with increased operating frequency.

With the continuous trend of smaller devices and lower voltage supplies scaling the traditional mostly analog designs become increasingly difficult, thus new architectures which are efficient and readily ported to new technologies are highly desirable. Because of its fully digital nature, the pulse injection locked RTWO can be scaled down with finer geometry CMOS processes at higher operating frequencies; higher frequency and phase resolutions can be achieved by using smaller varactors

available in more advanced processes. Also, both the trans-conductance and pulse injection locked RTWO can be mostly shifted to more advanced technologies.

Furthermore, the IL-RTWOs offer a scalable architecture with low-skew clock generation over a large chip area. The design proposes an efficient architecture to capture and correct the occurrence of skew violations by using an inexpensive built-in circuit. The clock deskew is achieved with the phase tuning characteristics between different clock domains. The digitally controlled CVPs support high frequency resolution and a wide built-in de-skew tuning range.

7.1 Accomplishments

This thesis presents a low power injection locked clock distribution scheme focused on precise clock de-skewing and low phase noise performance. The clock deskewing is achieved by tuning the phase characteristics of the different clock domains (i.e. RTWOs). The proposed injection locking scheme enables the architecture to relax the clock skew and jitter performance requirements in multi-GHz micro-systems. The digitally controlled CVPs support high frequency resolution and a wide built-in de-skew tuning range. The reported phase noise, integrated rms jitter and FOM are the best in its class. The proposed pulse injection locked RTWOs are mostly digital and achieve better phase noise performance than tranconductance injection locked RTWOs. The digital pulse injection locked circuit described in this technique can be easily implemented in more advanced digital technologies. The IL-RTWOs offer a scalable architecture with low-skew clock distribution over an arbitrary chip area. This clock distribution network will benefit from lower cost due to reduced die size with increased operating frequency.

7.2 Future Work

Having successfully demonstrated the feasibility of the proposed architecture and its potential advantages to the observed evolution trend of future integrated clock distribution architectures, a number of improvements could be done in future research based on the current architecture.

The number of RTWO elements on a specified chip area could be optimized to require less injection power. Different RTWOs located on the specified area could be injection locked to different harmonics of the reference signal depending on the requirement of the local clocks. On the local H-tree buffered clock distribution path, extra circuitry could be added to dynamically remove any skew that may result due to intra-die processing variations [157], [158]. The clock distribution scheme can also be implemented using injection-locked ring oscillators (ILRO) with multiple clock phases. This technique requires less on-chip space at the compensation of increased phase noise. The global clock signal could be also distributed at a lower optimum supply voltage. To maintain the speed of the system, a dual supply voltage (dual-VDD) clock distribution network would be required. Level converters would be utilized to restore the standard full swing clock signal at the leaves of the low voltage clock distribution network [159].

As the clock frequency increases, clock skew is increased by the PVT variations associated with device scaling. Challenges such as low Q-factor of the tuning varactors and switched capacitors result in a sharp degradation in the resonator Q. A large bias current and high transconductance (g_m) are needed to maintain a given oscillation amplitude and to satisfy the startup condition. An Automatic Gain Control (AGC) could be implemented to adjust the g_m of the inverter pairs at start up over an industrial

temperature range of -40 to 85°C. Process and temperature compensation techniques for minimizing the variation of the free-running frequency of an oscillator could also be implemented. Since g_m has a weak dependency on current in strong inversion, it can primarily be increased by enlarging the width of the inverter pairs. The quality factor of the capacitive and inductive tuning elements is sharply degraded at higher frequencies, and hence become the predominant factor in the overall tank. This also requires the use of exorbitantly large transistors to provide sufficient transconductance, and therefore compensate for the losses incurred in the LC-tank. These lead to significant capacitive loading effects that sharply reduce the RTWO tuning range. The large switch MIM-caps cannot be used any more at high frequencies since they excessively load the oscillator. The CMOS technology is also impacted by process, voltage and temperature variations (PVT) that necessitate extra frequency tuning margin. Therefore, both rf-line length and CVPs may need to be tuned to adjust the oscillation frequencies at 20GHz or above. This may result in a decreased Q and increased phase noise and power consumption. These are issues that would need to be addressed in the future design.

According to the linear time-variant PN model [161], a square waveform (sharp transitions at zero-crossings and flat area during on/off state of g_m transistors) of the oscillation voltage across the tank results in a lower rms value of the impulse sensitivity function (ISF) and less circuit noise contribution to the PN. [160]. Therefore, the inverter pairs used to sustain the RTWO oscillation need be optimized to sustain as many harmonics as possible. The simultaneous g_m and impedance matching technique could also be implemented to the inverter pairs for better phase noise performance [162]. The output buffer stage could be designed as differential structure for better noise rejection. It

also should be noted that, the parasitic capacitance will play a more significant effect at high oscillation frequencies and smaller step capacitance is required to achieve the same frequency resolution.

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Appendices

Appendix A: Fourier Transform Calculation

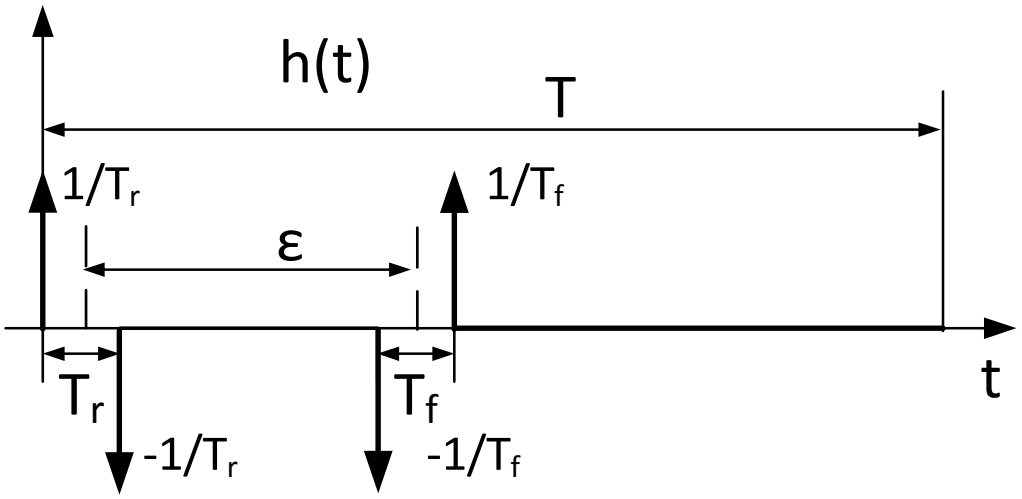

Fig. Appendix 1. Second derivatives of f(t)

The second derivative of the non-ideal square wave f(t) (Fig. 1) is taken in time domain as shown in Fig. 2. In order to derive the Fourier series coefficients of the wave f(t), the Fourier transform (H(jω)) of its second derivative is calculated as following for further derivation of Fourier transform F(jω).

$$
\begin{aligned}
H(j\omega) &= \int_0^T \frac{d^2 f(t)}{dt^2} e^{-jn\omega_0 t} dt \\
&= \int_{0^-}^{0^+} \frac{1}{T_r}\delta(t) e^{-jn\omega_0 t} dt + \int_{T_r^-}^{T_r^+} -\frac{1}{T_r}\delta(t - T_r) e^{-jn\omega_0 t} dt \\
&\qquad + \int_{(\varepsilon+\frac{T_r-T_f}{2})^-}^{(\varepsilon+\frac{T_r-T_f}{2})^+} -\frac{1}{T_f}\delta\left(t - (\varepsilon + \frac{T_r - T_f}{2})\right) e^{-jn\omega_0 t} dt \\
&\qquad + \int_{(\varepsilon+\frac{T_r+T_f}{2})^-}^{(\varepsilon+\frac{T_r+T_f}{2})^+} \frac{1}{T_f}\delta\left(t - (\varepsilon + \frac{T_r + T_f}{2})\right) e^{-jn\omega_0 t} dt \\
&= \frac{1}{T_r} e^0 - \frac{1}{T_r} e^{-jn\omega_0 T_r} - \frac{1}{T_f} e^{-jn\omega_0 (\varepsilon + \frac{T_r - T_f}{2})} + \frac{1}{T_f} e^{-jn\omega_0 (\varepsilon + \frac{T_r + T_f}{2})}
\end{aligned}
$$

where ω=nω0. For simplification, we assume δ = Tr = Tf , then

$$H(j\omega) = \frac{1}{\delta}\left[1 - e^{-jn\omega_0\delta} - e^{-jn\omega_0\varepsilon} + e^{-jn\omega_0(\varepsilon+\delta)}\right]$$
$$= \frac{1}{\delta}e^{-jn\omega_0\frac{\varepsilon+\delta}{2}}\left[e^{jn\omega_0\frac{\varepsilon}{2}}\left(e^{jn\omega_0\frac{\delta}{2}} - e^{-jn\omega_0\frac{\delta}{2}}\right)\right.$$
$$\left. - e^{-jn\omega_0\frac{\varepsilon}{2}}\left(e^{jn\omega_0\frac{\delta}{2}} - e^{-jn\omega_0\frac{\delta}{2}}\right)\right]$$

Because $\sin\left(n\omega_0\frac{\delta}{2}\right) = \frac{e^{jn\omega_0\frac{\delta}{2}} - e^{-jn\omega_0\frac{\delta}{2}}}{2j}$, H(jω) can be re-written as

$$H(j\omega) = \frac{2j}{\delta}e^{-jn\omega_0\frac{\varepsilon+\delta}{2}}\sin\left(n\omega_0\frac{\delta}{2}\right)\left(e^{jn\omega_0\frac{\varepsilon}{2}} - e^{-jn\omega_0\frac{\varepsilon}{2}}\right)$$
$$= \frac{-4}{\delta}e^{-jn\omega_0\frac{\varepsilon+\delta}{2}}\sin\left(n\omega_0\frac{\delta}{2}\right)\sin(n\omega_0\frac{\varepsilon}{2})$$

Appendix B: Layout Cells

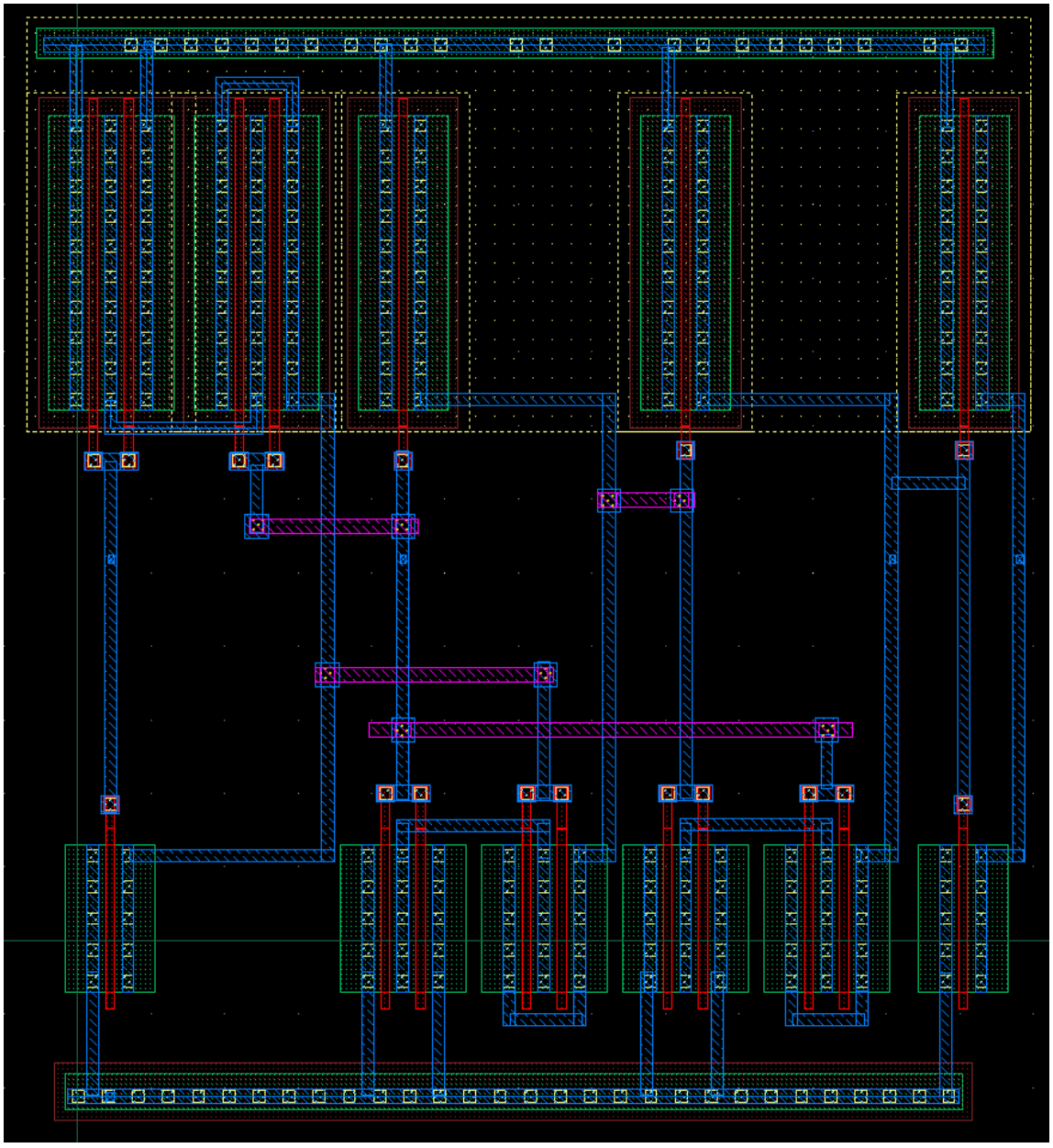

Fig. Appendix 2. The single phase edge triggered flip-flop

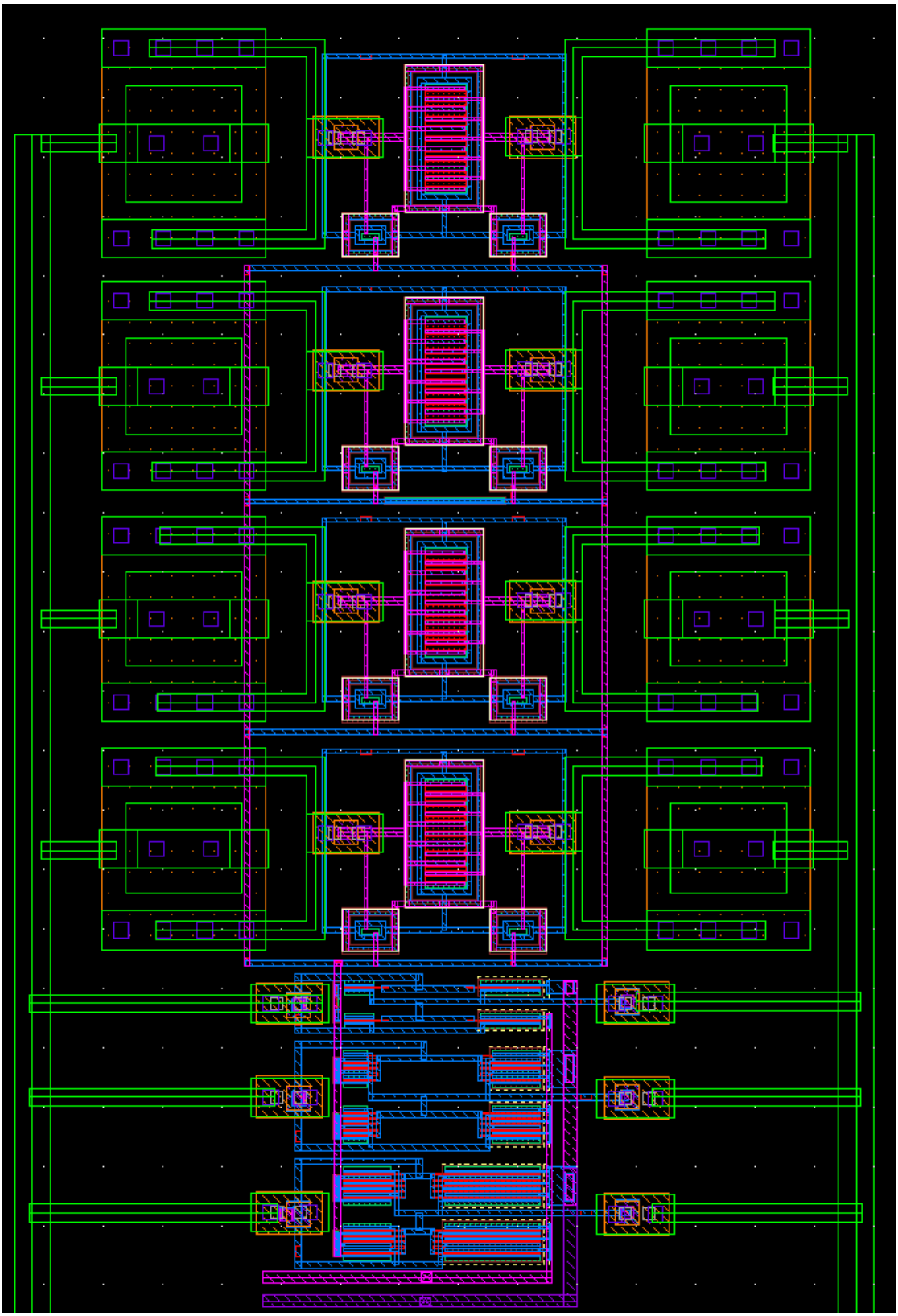

Fig. Appendix 3. Single stage loading MIM-caps and inverter pairs

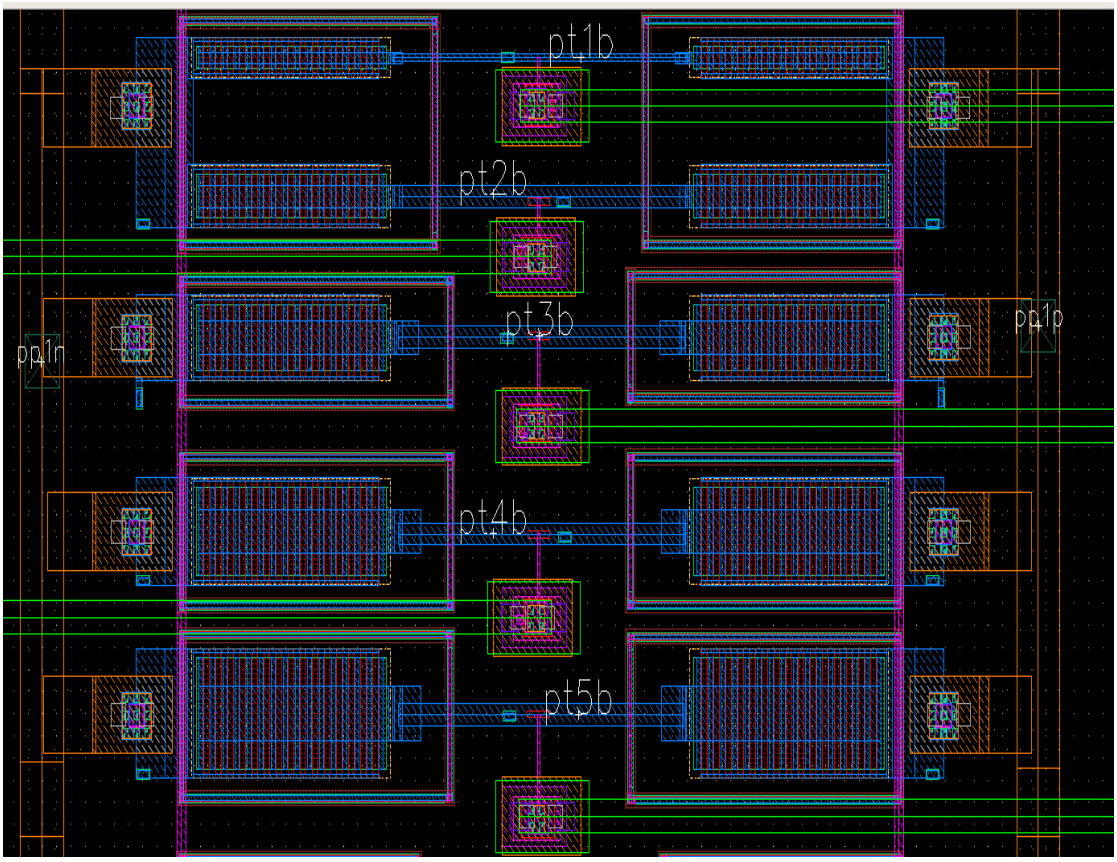

Fig. Appendix 4. The layout view of the RTWO phase tuning bank with CVPs

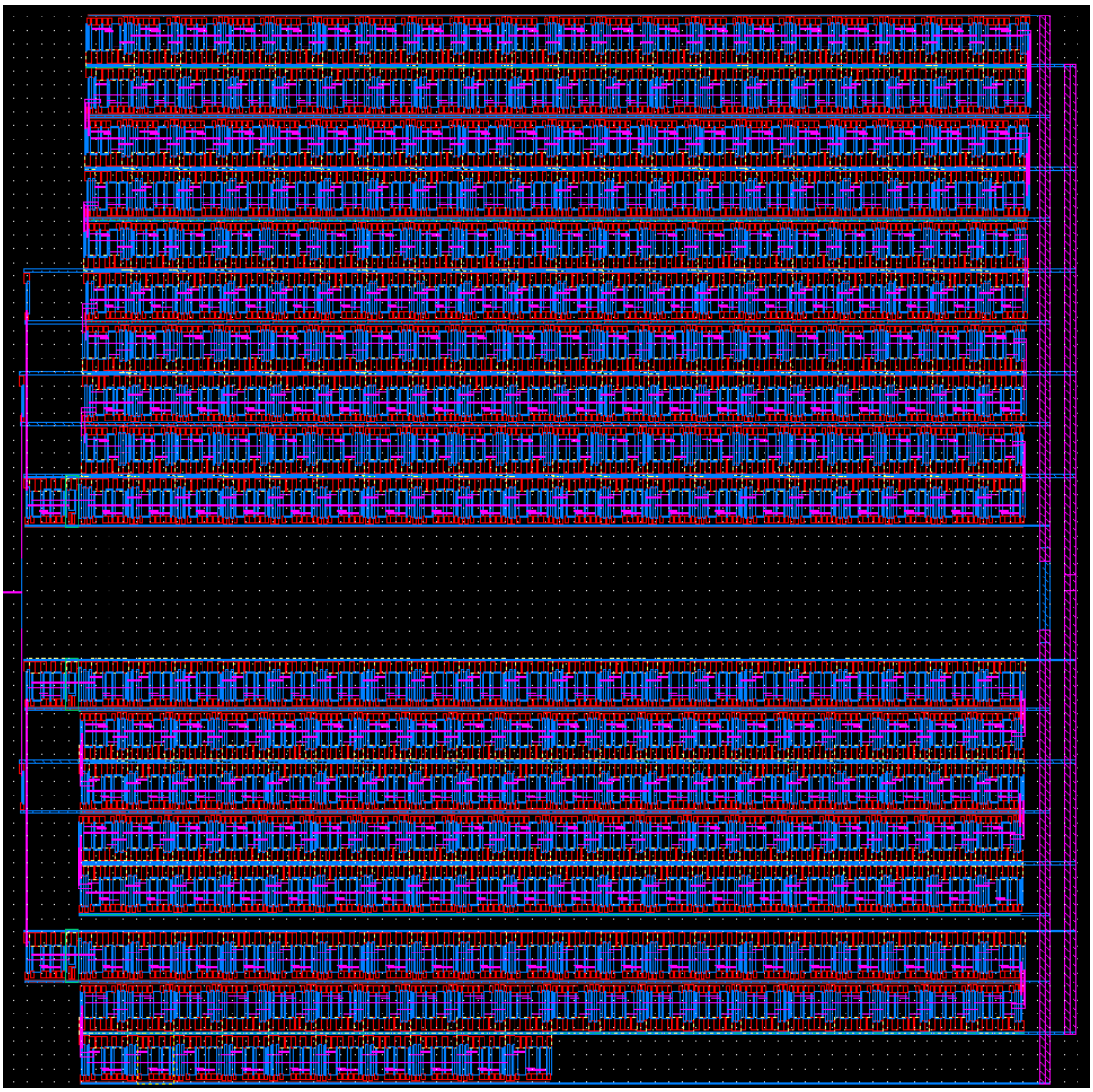

Fig. Appendix 5. Digital switching circuit layout

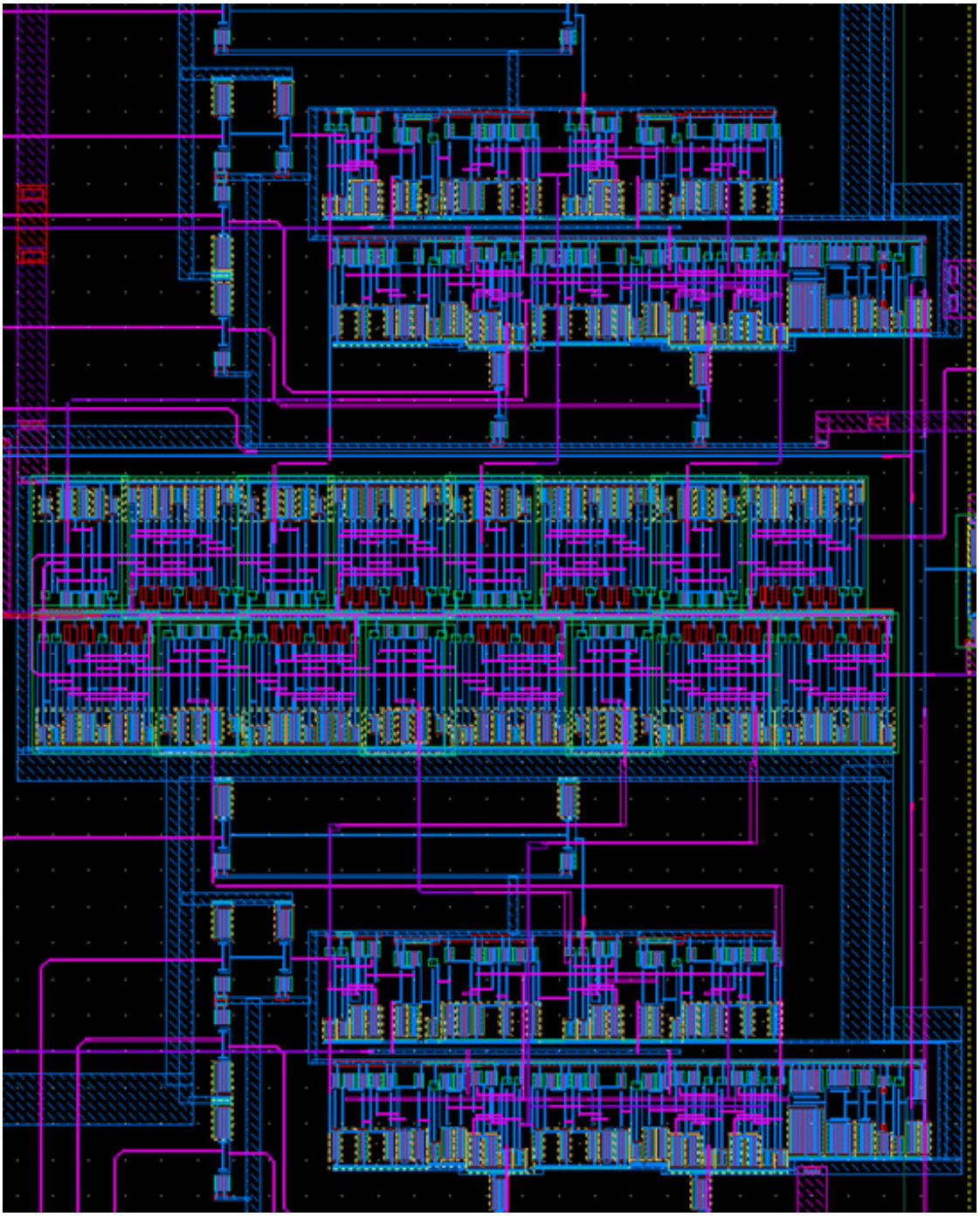

Fig. Appendix 6. Signature Analyzer layout

Appendix C: Automatic Test System Matlab Code

```
%RTWO Tuning Word tuning Frequency. v1
%Phase Tuning bits pt5 - pt1 set as '11000' in this version
%MIM code b6 - b0 increases binarily,i.e. decimal + 1
%Varactor code ff20 to ff1, tt10 to tt1, ss15 to ss1 increases
thermally, i.e.
%decimal + 2^i
%Equipment: Logic Analyzer HP16500C (with Pattern Generator HP16522A
card
%in the rear slot), GPIB Addr 7; Spectrum Analyzer HP8564E, GPIB Addr
18
clear;

%Initial value and clk definition
b=0; %Initial decimal value for b6 to b0,all '0',smallest cap load
ff=1048575; %Initial decimal value for ff20 to ff1,all '1',smallest cap
load
tt=1023; %Initial decimal value for tt10 to tt1,all '1',smallest cap
load
ss=32767; %Initial decimal value for ss15 to ss1,all '1',smallest cap
load
pt=24; %Initial decimal value for pt5 to pt1, '11000' in binary
ptbin=dec2bin(pt,5); %Convert decimal pt to binary ptbin

clksL='0';
clksH='1'; %set clks binary low and high

clkfL='0';
%clkfH='1'; %set clkf binary low and high


%Equipment GPIB Initialization
P=gpib('ni',0,7); %Assign the ni0 board in Matlab ICT to HP16500C
fopen(P); %Connect HP16500C to Matlab controller
set(P,'EOSMode','read&write'); %Set HP16500C EOSMode to R&W
set(P,'EOSCharCode','LF'); %Set HP16500C EOSCharCode to low level mode

S=gpib('ni',0,18); %Assign the ni0 board in Matlab ICT to HP8564E
fopen(S); %Connect HP8564E to Matlab controller
set(S,'EOSMode','read&write'); %Set HP8564E EOSMode to R&W
set(S,'EOSCharCode','LF'); %Set HP8564E EOSCharCode to low level mode


%Select Pattern Generator Card HP16522A and initial setup
fprintf(P,':SELECT 3'); %Select Pattern Generator
fprintf(P,':FORMAT:CLOCK INT,1E-6'); %Choose internal clock and set the
clock period as 1us
fprintf(P,':FORMAT:MODE HALF'); %Choose half channel mode, values
required for POD1, POD3, POD5

fprintf(P,':FORMAT:LABEL "Lab1",POS,0,0,#B00000111'); %Assign POD1 last
3 bits to Label 1, i.e. din, clks, clkf
```

```
%fprintf(P,':FORMAT:LABEL "din",POS,0,0,#B00000100'); %Assign POD1 3rd
bit to lable din, data type positive, POD5 & POD3 not used
%fprintf(P,':FORMAT:LABEL "clks",POS,0,0,#B00000010');%Assign POD1 2nd
bit to lable clks, data type positive, POD5 & POD3 not used
%fprintf(P,':FORMAT:LABEL "clkf",POS,0,0,#B00000001');%Assign POD1 1st
bit to lable clkf, data type positive, POD5 & POD3 not used

%fprintf(P,':SEQ:REMOVE ALL'); %Clear sequence lines in pattern
generator HP16522A
%pause(5);
%fprintf(P,':SEQ:REMOVE ALL'); %Clear sequence lines in pattern
generator HP16522A
%pause(5);

%Spectrum Analyzer HP8564E center frequency and span setup for MIM cap
%tuning
fprintf(S,'CF 2GHz'); %Set Spectrum Analyzer HP8564E center frequency
as 2GHz
fprintf(S,'SP 1GHz'); %Set Spectrum Analyzer HP8564E span as 1GHz
fprintf(S,'MKTRACK ON'); %Turn on the signal track of the Spectrum
Analyzer
%pause(2);
%Pattern Generator Sequence start

for i=1:32 %For 128 MIM tuning combination, 0(11111) to 127(11111)

    fprintf(P,':SEQ:REMOVE ALL'); %Clear sequence lines in pattern
generator HP16522A
    pause(5);
    fprintf(P,':SEQ:INSERT 4, NOOP, "#B000"'); %Need 1st line to let
repeat loop insert
    %Initial sequence with all 3 bits zeros, 200 cycles
    fprintf(P,':SEQ:INSERT 3,REPEAT,200,"#B000"'); %REPEAT generate 3
lines in the sequence: -START LOOP '0' REPEAT 200 TIMES -000 -END LOOP
'0'

    %pt5 to pt1 '11000' sequence definition
    fprintf(P,':SEQ:INSERT 6, NOOP,
"%s"',strcat(ptbin(1),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 7, NOOP,
"%s"',strcat(ptbin(1),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 8, NOOP,
"%s"',strcat(ptbin(2),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 9, NOOP,
"%s"',strcat(ptbin(2),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 10, NOOP,
"%s"',strcat(ptbin(3),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 11, NOOP,
"%s"',strcat(ptbin(3),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 12, NOOP,
"%s"',strcat(ptbin(4),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 13, NOOP,
"%s"',strcat(ptbin(4),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 14, NOOP,
"%s"',strcat(ptbin(5),clksL,clkfL));
```

```
    fprintf(P,':SEQ:INSERT 15, NOOP,
"%s"',strcat(ptbin(5),clksH,clkfL)); %Matlab convert decimal to binary
will put the lowest bit in our mind as the 1st bit of the string

    %All zeros isolation for different tuning banks
    fprintf(P,':SEQ:INSERT 16,REPEAT,10,"#B000"'); %Takes 17,18,19
lines in the sequence

    %ss15 to ss1 smallest load all '1' sequence definition
    ssbin=dec2bin(ss,15);
    fprintf(P,':SEQ:INSERT 19, NOOP,
"%s"',strcat(ssbin(1),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 20, NOOP,
"%s"',strcat(ssbin(1),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 21, NOOP,
"%s"',strcat(ssbin(2),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 22, NOOP,
"%s"',strcat(ssbin(2),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 23, NOOP,
"%s"',strcat(ssbin(3),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 24, NOOP,
"%s"',strcat(ssbin(3),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 25, NOOP,
"%s"',strcat(ssbin(4),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 26, NOOP,
"%s"',strcat(ssbin(4),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 27, NOOP,
"%s"',strcat(ssbin(5),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 28, NOOP,
"%s"',strcat(ssbin(5),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 29, NOOP,
"%s"',strcat(ssbin(6),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 30, NOOP,
"%s"',strcat(ssbin(6),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 31, NOOP,
"%s"',strcat(ssbin(7),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 32, NOOP,
"%s"',strcat(ssbin(7),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 33, NOOP,
"%s"',strcat(ssbin(8),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 34, NOOP,
"%s"',strcat(ssbin(8),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 35, NOOP,
"%s"',strcat(ssbin(9),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 36, NOOP,
"%s"',strcat(ssbin(9),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 37, NOOP,
"%s"',strcat(ssbin(10),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 38, NOOP,
"%s"',strcat(ssbin(10),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 39, NOOP,
"%s"',strcat(ssbin(11),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 40, NOOP,
"%s"',strcat(ssbin(11),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 41, NOOP,
"%s"',strcat(ssbin(12),clksL,clkfL));
```

```
    fprintf(P,':SEQ:INSERT 42, NOOP,
"%s"',strcat(ssbin(12),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 43, NOOP,
"%s"',strcat(ssbin(13),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 44, NOOP,
"%s"',strcat(ssbin(13),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 45, NOOP,
"%s"',strcat(ssbin(14),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 46, NOOP,
"%s"',strcat(ssbin(14),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 47, NOOP,
"%s"',strcat(ssbin(15),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 48, NOOP,
"%s"',strcat(ssbin(15),clksH,clkfL));

    %All zeros isolation for different tuning banks
    fprintf(P,':SEQ:INSERT 49,REPEAT,10,"#B000"'); %Takes 50,51,52
lines in the sequence

    %tt10 to tt1 smallest load all '1' sequence definition
    ttbin=dec2bin(tt,10);
    fprintf(P,':SEQ:INSERT 52, NOOP,
"%s"',strcat(ttbin(1),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 53, NOOP,
"%s"',strcat(ttbin(1),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 54, NOOP,
"%s"',strcat(ttbin(2),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 55, NOOP,
"%s"',strcat(ttbin(2),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 56, NOOP,
"%s"',strcat(ttbin(3),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 57, NOOP,
"%s"',strcat(ttbin(3),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 58, NOOP,
"%s"',strcat(ttbin(4),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 59, NOOP,
"%s"',strcat(ttbin(4),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 60, NOOP,
"%s"',strcat(ttbin(5),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 61, NOOP,
"%s"',strcat(ttbin(5),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 62, NOOP,
"%s"',strcat(ttbin(6),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 63, NOOP,
"%s"',strcat(ttbin(6),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 64, NOOP,
"%s"',strcat(ttbin(7),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 65, NOOP,
"%s"',strcat(ttbin(7),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 66, NOOP,
"%s"',strcat(ttbin(8),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 67, NOOP,
"%s"',strcat(ttbin(8),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 68, NOOP,
"%s"',strcat(ttbin(9),clksL,clkfL));
```

```
    fprintf(P,':SEQ:INSERT 69, NOOP,
"%s"',strcat(ttbin(9),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 70, NOOP,
"%s"',strcat(ttbin(10),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 71, NOOP,
"%s"',strcat(ttbin(10),clksH,clkfL));

    %All zeros isolation for different tuning banks
    fprintf(P,':SEQ:INSERT 72,REPEAT,10,"#B000"'); %Takes 73,74,75
lines in the sequence

    %ff20 to ff1 smallest load all '1' sequence definition
    ffbin=dec2bin(ff,20);
    fprintf(P,':SEQ:INSERT 75, NOOP,
"%s"',strcat(ffbin(1),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 76, NOOP,
"%s"',strcat(ffbin(1),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 77, NOOP,
"%s"',strcat(ffbin(2),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 78, NOOP,
"%s"',strcat(ffbin(2),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 79, NOOP,
"%s"',strcat(ffbin(3),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 80, NOOP,
"%s"',strcat(ffbin(3),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 81, NOOP,
"%s"',strcat(ffbin(4),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 82, NOOP,
"%s"',strcat(ffbin(4),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 83, NOOP,
"%s"',strcat(ffbin(5),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 84, NOOP,
"%s"',strcat(ffbin(5),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 85, NOOP,
"%s"',strcat(ffbin(6),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 86, NOOP,
"%s"',strcat(ffbin(6),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 87, NOOP,
"%s"',strcat(ffbin(7),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 88, NOOP,
"%s"',strcat(ffbin(7),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 89, NOOP,
"%s"',strcat(ffbin(8),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 90, NOOP,
"%s"',strcat(ffbin(8),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 91, NOOP,
"%s"',strcat(ffbin(9),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 92, NOOP,
"%s"',strcat(ffbin(9),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 93, NOOP,
"%s"',strcat(ffbin(10),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 94, NOOP,
"%s"',strcat(ffbin(10),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 95, NOOP,
"%s"',strcat(ffbin(11),clksL,clkfL));
```

```
    fprintf(P,':SEQ:INSERT 96, NOOP,
"%s"',strcat(ffbin(11),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 97, NOOP,
"%s"',strcat(ffbin(12),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 98, NOOP,
"%s"',strcat(ffbin(12),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 99, NOOP,
"%s"',strcat(ffbin(13),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 100, NOOP,
"%s"',strcat(ffbin(13),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 101, NOOP,
"%s"',strcat(ffbin(14),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 102, NOOP,
"%s"',strcat(ffbin(14),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 103, NOOP,
"%s"',strcat(ffbin(15),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 104, NOOP,
"%s"',strcat(ffbin(15),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 105, NOOP,
"%s"',strcat(ffbin(16),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 106, NOOP,
"%s"',strcat(ffbin(16),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 107, NOOP,
"%s"',strcat(ffbin(17),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 108, NOOP,
"%s"',strcat(ffbin(17),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 109, NOOP,
"%s"',strcat(ffbin(18),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 110, NOOP,
"%s"',strcat(ffbin(18),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 111, NOOP,
"%s"',strcat(ffbin(19),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 112, NOOP,
"%s"',strcat(ffbin(19),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 113, NOOP,
"%s"',strcat(ffbin(20),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 114, NOOP,
"%s"',strcat(ffbin(20),clksH,clkfL));

    %All zeros isolation for different tuning banks
    fprintf(P,':SEQ:INSERT 115,REPEAT,10,"#B000"'); %Takes 116,117,118
lines in the sequence

    %b6 to b1 smallest load all '1' sequence definition
    bbin=dec2bin(b,7); %Convert decimal b to bianry bbin
    fprintf(P,':SEQ:INSERT 118, NOOP,
"%s"',strcat(bbin(1),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 119, NOOP,
"%s"',strcat(bbin(1),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 120, NOOP,
"%s"',strcat(bbin(2),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 121, NOOP,
"%s"',strcat(bbin(2),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 122, NOOP,
"%s"',strcat(bbin(3),clksL,clkfL));
```

```
    fprintf(P,':SEQ:INSERT 123, NOOP,
"%s"',strcat(bbin(3),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 124, NOOP,
"%s"',strcat(bbin(4),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 125, NOOP,
"%s"',strcat(bbin(4),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 126, NOOP,
"%s"',strcat(bbin(5),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 127, NOOP,
"%s"',strcat(bbin(5),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 128, NOOP,
"%s"',strcat(bbin(6),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 129, NOOP,
"%s"',strcat(bbin(6),clksH,clkfL));
    fprintf(P,':SEQ:INSERT 130, NOOP,
"%s"',strcat(bbin(7),clksL,clkfL));
    fprintf(P,':SEQ:INSERT 131, NOOP,
"%s"',strcat(bbin(7),clksH,clkfL));

    %All zeros isolation for different tuning banks
    fprintf(P,':SEQ:INSERT 132,REPEAT,5,"#B000"'); %Takes 133,134,135
lines in the sequence
    %fprintf(P,':SEQ:INSERT 359, NOOP, "#B000"');
    %fprintf(P,':SEQ:INSERT 360, NOOP, "#B000"');
    %fprintf(P,':SEQ:INSERT 361, NOOP, "#B000"');
    %fprintf(P,':SEQ:INSERT 362, NOOP, "#B000"');
    %fprintf(P,':SEQ:INSERT 363, NOOP, "#B000"');

    %clkF set high, chip load data
    fprintf(P,':SEQ:INSERT 135, NOOP, "#B001"');
    fprintf(P,':SEQ:INSERT 136, NOOP, "#B001"');
    fprintf(P,':SEQ:INSERT 137, NOOP, "#B001"');

    %All zeros initial bus when end sequence
    fprintf(P,':SEQ:INSERT 138,REPEAT,4,"#B000"'); %Takes 139,140,141
lines in the sequence

    %Sequence setup for MIM binary tuning end
    fprintf(P,':RMODE SINGLE'); %Sequence run mode set as single run
    fprintf(P,':START'); %Pattern generator start output sequence data
    pause(10); %Pause 20s for Pattern Generator data transmission
    fprintf(P,':STOP'); %Stop pattern generator

    %i=1;

    fprintf(S,'MKPK HI'); %Search for the peak
    pause(2);

    %Query frequency and power value from Spectrum Analyzer
    freqtemp=query(S,'MKF?'); %Return frequency (string type value) of
peak mark to temp variable
    powertemp=query(S,'MKA?'); %Return power amplitude (stringtype
value) of peak mark to temp variable

    %Convert value type and assign to matrix
```

```
    result(i,1)=b; %Assign code to 1st column of the matrix 'result'
    result(i,2)=str2num(freqtemp); %Assign frequency value (convert
string to number) to 2nd column of the matix 'result'
    result(i,3)=str2num(powertemp); %Assign power value (convert string
to number) to 3rd column of the matrix 'result'
    %pause(5); %Pause 10s for Spectrum Analyzer waveform information
transmission

    b=b+1;
end
code=result(:,1);
frequency=result(:,2);
power=result(:,3);
resultsortfreq=sortrows(result,2); %Sort table 'result' based on
frequency
codesort=resultsortfreq(:,1);
freqsort=resultsortfreq(:,2);

Fig.;
plot(code,frequency); %Plot code vs. frequency

Fig.;
plot(freqsort,codesort); %Plot frequency vs. code

Fig.;
plot(code,power); %Plot code vs. power
```