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**An 8 Bit BiCMOS Subranging
Flash Analog to Digital
Converter**

by

Jim Seto, B.A.Sc.

**This thesis is submitted to the
Faculty of Graduate Studies and Research
in partial fulfillment of the
requirements for the degree of**

Master of Engineering

Ottawa Carleton Institute for Electrical Engineering

**Department of Electronics
Faculty of Engineering
Carleton University
Ottawa, Ontario**

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"An 8-Bit BiCMOS Subranging Flash Analog to Digital Converter"

submitted by Jim Seto in partial fulfillment of the requirements for the degree of Master of Engineering.

Prof. M.A. Copeland
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October 1991

Abstract

In this thesis, the design of an 8-bit BiCMOS subranging flash analog to digital converter is described. An investigation into alternative high performance A/D architectures is presented. Based on this study, a novel subranging architecture is described. From the technology and circuit perspective, design considerations for such a subranging A/D converter are covered. A detailed study is performed of the speed limiting factors in the key element, the high speed comparator. From this analysis, a detailed design of a BiCMOS comparator is presented. The simulation results are supported with preliminary test measurements of an early version of this comparator. The validity of this study is supported with complete simulations and layout of the subranging A/D converter. The final layout results are then compared with other published high speed A/D converter designs.

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List of Symbols and Abbreviations

A to D	Analog to Digital
A/D	Analog to Digital
ADC	Analog to Digital Converter
AGND	Analog Ground
BiCMOS	Bipolar-Complementary Metal Oxide Semiconductor
CMOS	Complementary Metal Oxide Semiconductor
dB	Decibel
D/A	Digital to Analog
DAC	Digital to Analog Converter
DNL	Differential Non-Linearity
f_S	Sampling Frequency
INL	Integral Non-Linearity
LSB	Least Significant Bit
MOS	Metal Oxide Semiconductor
MSB	Most Significant Bit
S/H	Sample and Hold
SAR	Successive-Approximation Register
SNR	Signal to Noise Ratio
V_{FS}	Full Scale Voltage

Chapter 1

Introduction

1.1 Thesis Motivation

With the emergence of optical fiber, many new applications have arisen to exploit the high bandwidth transmission capabilities of this medium. One of these is the optical transmission of video, for which a growing interest in high speed analog to digital conversion has arisen. This interest is driven by applications that require high speed A to D conversion to be more cost effective than previously.

To date, the speed of A to D converters has been dictated by what the technologies they are based upon have to offer. In the context of this thesis, "the technology" is a shorthand term for the VLSI fabrication technology. This term does not describe a fixed entity but an evolving one, as fabrication techniques improve continuously. For the most part, speed improvements in A/D converters have come from the speed enhancements of the technologies (such as shorter gate lengths), not from better architectures. This has been the trend for the past decade. The existing architectures today are limited by the capabilities of the technology used. With no radically different technologies, no new architectures have emerged. This is starting to change with the maturity of the BiCMOS process. Analog MOS processes have allowed one class of A/D conversion to prosper, specifically charge re-distribution architectures. Bipolar processes have also been useful for another class of A/D conversion, flash

A to D converters. With BiCMOS, many opportunities of combining the advantages of MOS and bipolar are now possible, opening the door for new families of A/D converter architectures. One such class is the subranging or multi-step flash A/D converter. Although subranging architectures have existed in both CMOS and bipolar processes for many years, these architectures have been limited by the capabilities of the technology.

The emergence of BiCMOS presents the opportunity to meet the new demand for high speed A to D conversion. This is the motivating factor behind this thesis. The objective of this work is to study a class of high speed analog to digital converters called the subranging flash A/D converter and to present an 8-bit BiCMOS A/D converter that exploits a novel architecture in the new high performance technology. Given this novel architecture and a complete design of the A/D converter, its advantages can then be compared with existing designs that are being used to meet the applications that require high speed conversion.

1.2 Background

Conceptually, analog to digital converters are easy to understand. The input to an A/D converter is an analog signal and the output is a digital representation of this signal. As simple as this may seem, the actual circuitry required to implement this function is very complex. This data conversion process can be viewed as having two distinct parts. First an analog signal must be sampled, and secondly it must be quantized. Both sampling and quantizing deal with approximating the analog signal, one in time and the other in amplitude. To understand how an analog to digital converter works, it is important to understand the theory behind sampling and quantizing and how these functions affect the performance of data converters.

1.2.1 Sampling

The amplitude of an analog signal is continuous in time. When it is applied to a sample and hold circuit, the resulting signal is a sampled representation of the original analog signal (Figure 1.2-1). The amplitude remains constant for the duration t_n . After the sample is taken, the spectrum of the sampled signal is the convolution of the spectrum of the original analog signal and the spectrum of the sampling signal (Figure 1.2-2). The resulting waveform consists of spectra of the original signal, repeated at integer frequency multiples of the sampling rate. If the sampling rate is low relative to the baseband signal being sampled, the spectrum of the original signal

and its images may fold over onto each other (Figure 1.2-3). These aliasing effects are undesirable and make it very difficult to recover the original signal. These problems are avoided if the sampling rate is greater than twice the bandwidth of interest. This is referred to as the Nyquist Rate. In addition to the sampling action, Figure 1.2-1 shows a holding action after the sample is taken. In the context of A/D conversion this has no consequence on the frequency spectrum, except as caused by delay, because the result of the A/D conversion corresponds to the original samples.

Sampled Waveform
Figure 1.2-1

Figure 1.2-2
Spectrum of Sampled Waveform

Figure 1.2-3
Aliasing Effects of Sampled Waveform

1.2.2 Quantization

Once a signal is sampled, it must be quantized. This is the process of mapping the sampled analog signal into discrete levels that can be translated into a digital word (Figure 1.2-1). Depending on the resolution of the quantizer (ie number of bits), the quantized signal should be a close approximation of the amplitude of the original sampled signal.

The process of quantizing a signal will always result in quantization noise. This is unavoidable because the quantized signal is an approximation of the original signal. The difference between the quantized signal and the original signal is the quantization noise. The higher the resolution, the higher will be the signal to quantization noise ratio.

Differential and integral linearity are two figures of merit that all data converters are rated by. The local deviation of the converter output from the ideal is referred to as differential linearity. The overall deviation of the converter from the ideal is referred to as integral linearity. A poor quantizing procedure in a converter will translate into poor differential or integral linearity. This could be inherent in the algorithm for the conversion or in errors that manifest themselves in the design (eg; inaccurate reference voltages, poor offset voltage characteristics in the components, etc...).

Figure 1.2-1
Quantization

1.3 Thesis Overview

The development and design of a subranging flash A to D converter in a new technology requires research into many areas. This work will be covered in the subsequent chapters. Some insight into the thesis and a brief overview of some of the basic principles behind data conversion are presented in this chapter.

Chapter 2 reviews the implementation of existing high performance A to D converters. Analysis of these architectures and their limitations lead to an understanding of the advantages they have to offer. This knowledge is then utilized in the actual design of a high speed A to D converter using a novel architecture.

Chapter 3 presents the design considerations for implementing a subranging flash A to D converter. From a circuit perspective, a detailed analysis of traditional technologies leads to an understanding of how a subranging architecture can best be implemented. Next, design considerations for the basic building block common to all subranging A to D converters, the high speed comparator, are presented.

In Chapter 4, the actual design of an 8 bit BiCMOS subranging flash A to D converter is presented. Due to time constraints and limited access to silicon, the design could not be fabricated. The only component for which fabrication was possible was on an early

version of the high speed comparator, which is the heart of the subranging A/D converter. Preliminary test measurements demonstrate the principles behind the comparator and led to further design improvements. The thesis is thus primarily a design study of a BiCMOS subranging A/D converter, including a detailed layout. This involves discussions of the novel architecture that has been developed, with simulations. The final layout allows us to compare these results with published results. This complete design and layout also permits us to establish many points about the validity of the design and to provide information such as capacitive loading which makes the simulations more valid.

Finally in Chapter 5, conclusions and recommendations for future work are presented.

Chapter 2

Alternative High Performance Analog to Digital Converter Architectures

2.1 Introduction

This chapter will deal with the analysis and operation of existing high performance analog to digital converters in more traditional technologies. The knowledge and insight gained from this study is carried over into the actual design of a BiCMOS analog to digital converter. Many of the principles and underlying fundamentals of these existing architectures can be applied directly to the design. As well, an understanding of their limitations is very useful, in order to avoid their shortcomings.

In the context of this thesis, high performance A/D converters are defined as high speed, accurate, and high bandwidth converters. Given this definition, narrow bandwidth converters such as over-sampled A/D converters and less accurate architectures such as cyclic A/D converters are excluded from the analysis in this chapter.

The first class of high performance A/D converters to be analyzed is the successive-approximation architecture. This class of converter is by far the most popular of all the different families. The next class to be examined will be the flash A/D converter. Finally, the last class will be the subranging family. Many variations of the "classical"

subranging architecture have been published to date and these will be reviewed.

2.2 Successive-Approximation Technique

Conceptually, successive-approximation converters are easy to understand. The underlying principle is a trial and error process of approximating the analog input signal with a digital code. This is accomplished within a feedback loop whose input is an approximation of the input signal. This process is continued successively until the final digital word is reached.

The key components (Figure 2.2-1) in a successive-approximation A/D converter are a D/A converter, a voltage comparator and a successive-approximation register (SAR). The D/A converter forms the feedback loop around the comparator and the SAR block. The comparator output controls the behaviour and the contents of the SAR which is the input to the D/A block.

The operation of this type of converter is as follows. Initially, the contents of both the shift register and the holding register within the SAR block are cleared. The first step of the conversion process determines the MSB. This is achieved by setting the first trial bit in the holding register to 1, while the rest of the bits are cleared. This is the input to the D/A block, and a corresponding voltage signal (V_O) is now compared with the analog input (V_A). If the output state of the comparator does not change, then the input signal (V_A) is greater

than the approximation (V_O) and the 1 is retained for the MSB. If the comparator state does change, then a 0 is inserted as the MSB.

Figure 2.2-1
Successive Approximation Register A/D Converter

For the next cycle, the second most significant bit is determined in a similar fashion. By inserting a 1 into the next bit in the holding register, the entire process is repeated. This trial and error approximation of the signal proceeds until all bits are determined in N successive cycles.

The decision-making process of whether to keep the trial 1 or to clear the bit is controlled by the voltage comparator and the N -bit sequencer in the SAR block. Each bit is determined by shifting the

trial bit from the MSB to the LSB. The result of each approximation cycle is stored in the holding register. The digital output is not valid until the whole conversion step is complete, which means all bits from the MSB to LSB must be evaluated. Additional logic is also necessary to start and stop the process. As well, control logic is required to gate the digital output only when it is valid.

The concept of successive approximation (Figure 2.2-2) can be represented as a decision tree where each branch represents an approximation of the input signal. As each branch is traversed from left to right, a closer and closer representation of the input signal is achieved. Each approximation requires 1 clock cycle, so for an N-bit successive-approximation A/D converter, N clock cycles are required for an entire conversion process.

When compared to serial architectures such as dual-slope A/D converters, only N clock cycles are required, versus 2^N clock cycles for serial architectures. This is a substantial speed improvement and conversion rates for successive-approximation A/D converters as fast as 400 nS are now possible [1].

The performance limitations of this class of A/D converter are primarily due to the characteristics (speed, resolution and linearity) of the D/A section that forms the feedback loop. One the most important requirements for the D/A section is the monotonicity of this block. Missing codes in the digital output will result if there are

Figure 2.2-2
Decision Tree for SAR A/D Converter

any non-monotonic characteristics. The design of this block is crucial in a successive-approximation A/D converter.

The design of this block is crucial in a successive-approximation A/D converter. There are many design alternatives for implementing the D/A section. The type of D/A block to be implemented will depend on the application, the degree of integration required and the technology available. Some common D/A implementations use binary-weighted current sources [2] or the R-2R resistor ladder approach [3]. These techniques use current steering principles and consume large amounts of power. These two implementations are primarily utilized in successive-approximation A/D converters that are fabricated in bipolar processes. However, by far the most popular D/A scheme used within a SAR D/A converter is the charge-sharing D/A converter approach, used in a MOS process with capacitors.

2.2.1 Charge-Redistribution A/D Conversion Principles

The operation of charge-redistribution A/D converters [4,5] is based upon the fundamental principle of charge conservation. The simplicity and accuracy of this basic analog design approach is the reason why this technique is so popular. The main component of a charge-scaling DAC is a binary-weighted capacitive ladder network. It is this block that forms the feedback loop to the comparator and the SAR, when implemented within a successive-approximation A/D converter.

The operation of such a block (Figure 2.2-3) can be viewed as having three distinct steps. Firstly, all top plates in the capacitor array are grounded by S_A (Figure 2.2-3(a)) and all bottom plates are connected to the analog input, V_A . The total capacitance of the array is:

$$C_{\text{TOTAL}} = C + \frac{C}{2} + \frac{C}{4} + \frac{C}{8} + \frac{C}{16} + \frac{C}{16} = 2C$$

By charging the capacitors through the bottom plate, a charge Q_X that is proportional to V_A is stored on the top plate. This first step is referred to as the sample mode.

In the next step, called the hold mode, the switch S_A from the ground to the top plates is opened. All switches on the bottom plates are then individually grounded (Figure 2.2-3(b)). Because the charge

Q_X has been stored on the capacitors, the potential (V_X) of the top plate is now equal to $-V_A$ (a negative value of the input).

The final step is referred to as the redistribution mode. At this point, the successive-approximation process can begin (Figure 2.2-3(c)). To start, the first switch S_1 is connected to V_{ref} and the rest remain grounded. This first switch represents the MSB. By connecting the largest capacitor (C) to V_{ref} , the voltage V_X (which equals $-V_A$) is now increased by $1/2 V_{ref}$ because C is one half C_{TOTAL} .

$$V_X = -V_A + \frac{V_{ref}}{2}$$

This node voltage is connected to the comparator, and if the output state changes, the value of the MSB is interpreted as "0". The comparator logic is "1" if $V_X < AGND$ and a "0" if $V_X > AGND$. This is equivalent to the following interpretation:

$$\text{if } V_X < AGND \quad \text{then } V_A > \frac{V_{ref}}{2}$$

therefore $MSB = 1$ and

$$\text{if } V_X > AGND \quad \text{then } V_A < \frac{V_{ref}}{2}$$

therefore $MSB = 0$

At this point, the first clock cycle has determined the MSB value. In the next clock cycle, another bit is determined in a similar fashion. By connecting the bottom plate of the next largest capacitor to V_{ref}

and comparing the polarity of the resulting value of V_X , the second most significant bit is determined. In this second cycle, $V_{ref}/4$ is added to V_X :

$$V_X = -V_A + b_{MSB} * \frac{V_{ref}}{2} + \frac{V_{ref}}{4}$$

This process continues until all N bits have been determined. For a digital output of 01100 (Figure 2.2-3(c)), all capacitors that correspond to a "0" are completely discharged. The original Q_X on the top plates has been redistributed across only the capacitors that correspond to a "1".

At the end of this process, all parasitic capacitances associated with the bottom plate switches are either discharged to ground or charged by V_{ref} . Charge Q_X on the top plates is not leaked away. This eliminates the non-linearity effects from these parasitic capacitances and results in an accurate D/A converter. As well, these switches can now be made large. This allows for shorter charging and redistribution periods.

In this conversion process the voltage on the top plates (V_X) converges towards "0" (AGND), which is its initial value. This implies that any parasitic capacitances associated with the ground switch (S_A), the top plates, and the comparator, do not corrupt Q_X . This total parasitic capacitance present during the sample mode

Figure 2.2-3

is virtually the same after the redistribution mode, so its net effect is almost negligible.

The key to the accuracy of this charge redistribution technique is the matching characteristics between the elements that make up the voltage or charge dividers. For this reason, capacitor arrays are favorable for such an application. For a monolithic realization of such a block, high quality linear capacitors can be easily fabricated. The inherent matching properties of capacitors are superior [6] to other elements, such as resistors.

2.3 Full Flash A/D Conversion Principles

Of all the different analog to digital conversion architectures, full flash A/D converters are the most simple and the fastest. This simplicity and speed is accomplished at the expense of area and power consumption. Full flash A/D converters are often referred to as parallel A/D converters because one clock cycle is required for one conversion.

For this type of architecture, one analog comparator is necessary for every quantization level in the digital word [7]. As well, a fixed reference level is required for each quantization step. For an N-bit A/D converter (Figure 2.3-1), $2^N - 1$ comparators and $2^N - 1$ separate fixed reference voltages are required. The $2^N - 1$ decision levels for such a design are normally created by a resistor divider that spans between minimum and full scale voltage. Although the concept of this parallel technique is very simple, the complexity of the implementation increases rapidly with an increase in resolution (ie; number of bits) [8,9]. This exponential increase in the circuit components translates to a proportional growth in the area and power requirements. As an example, an 8-bit full flash A/D converter will require 255 comparators and 255 reference levels. To date, 10-bit full flash A/D converters represent the practical limit of this architecture.

Figure 2.3-1
Full-Flash A/D Converter

Aside from the 2^N-1 comparators in a full flash A/D converter, further encoding is required to translate the comparator outputs into a binary digital word. The inputs to the encoder are 2^N-1 bits. Depending on the value of the analog input signal, all comparator outputs with reference voltages greater than the input signal will be a logical "0", while all the comparator outputs with reference voltages less than the input will be logical "1". This translation from a thermometer coding scheme to a binary word occurs in the encoding block and requires digital circuitry to operate in a parallel fashion. At the end of the clock cycle, the final encoded digital word is latched into a holding register.

All inputs to the 2^N-1 comparators are connected to one analog input signal. The total input capacitance of all these nodes represents a significant load for the analog signal to drive. Consequently, an analog buffer is always necessary to drive the input signal. Depending on the technology, the value of the input capacitance on the comparators will change as a function of the voltage level. This change can be non-linear and has implications on the design of the comparators and the analog buffer. Section 3.2.2 gives more details.

With 2^N-1 comparators and a resistor string with the same number of taps, the layout of such a design is extremely important. Signal delays arising from the interconnect can manifest themselves in the form of distortion for the analog input signal that must reach every comparator. As well, interconnect resistance between the reference ladder and the comparator inputs can alter the value of the reference

voltages. In the extreme case, the inherent monotonicity of a resistor divider can be compromised. This is especially true with high resolution converters, where the quantization steps are particularly small.

Biasing of the resistor divider and the comparators are also non-trivial tasks. The resistor divider must be able to drive the changing input capacitances of all the comparators. Bias currents for $2^N - 1$ comparators represent an extremely large power requirement. This is particularly evident when compared to a SAR architecture which requires only one comparator.

2.4 Subranging Flash A/D Conversion Principles

A subranging flash A/D converter can be viewed as being a hybrid of a SAR and a full flash A/D converter. The previous two analog to digital architectures have many advantages in terms of accuracy or speed. However, they also have disadvantages. The combination of elements of a SAR and a full flash A/D converter to make up a subranging A/D converter retains the inherent advantages of both, while many of the disadvantages are overcome. A subranging flash A/D architecture can offer an ideal balance between power, area, speed and accuracy.

Many of the elemental blocks necessary for a subranging A/D converter (Figure 2.4-1) are the same as for a SAR or a full flash A/D converter. The architecture consists of two low resolution flash converters (MSB and LSB sections), a DAC block, a gain stage, and subtractor. For such a design only two clock cycles are required for the complete conversion process. This is a significant improvement over a SAR design. Because the conversion process is partitioned into two clock cycles, the number of comparators required decreases dramatically when compared to a full flash converter. A sample and hold block is necessary in this architecture because the input must remain the same for the duration of two clock cycles.

During the first clock cycle, the input signal is sampled and held. As well, the first conversion occurs. From this conversion, the first M significant bits are determined. This first conversion is implemented

Figure 2.4-1
Subranging Flash A/D Converter

with an M bit flash. It contains 2^M comparators and resistors and its operation is the same as for a full flash converter. The transfer function of this MSB section can be represented as:

$$H_{MSB} = \frac{V_{in}}{V_{FS}} = \frac{d_1}{2^1} + \frac{d_2}{2^2} \dots + \frac{d_m}{2^m}$$

This binary output is fed back into an M-bit DAC. The output of this block is:

$$V_{DAC} = H_{MSB} \cdot V_{FS}$$

This analog value is then subtracted from V_{in} and amplified through a gain block.

$$V_{LSB} = A(V_{in} - V_{DAC})$$

At this point, the second clock cycle begins and the remaining bits are determined using the second flash converter. This second flash conversion determines the L remaining bits and has a transfer function of the form:

$$H_{LSB} = \frac{V_{LSB}}{V_{FS}} = \frac{d_{N-M+1}}{2^{N-M+1}} + \frac{d_{N-M+2}}{2^{N-M+2}} \dots + \frac{d_{N-M+L}}{2^{N-M+L}}$$

The complete transfer function of the entire subranging converter is:

$$H_{Total} = H_{MSB} + \frac{H_{LSB}}{A} = \frac{V_{in}}{V_{FS}}$$

where $A = 2^M$

$$H_{\text{Total}} = \frac{d_1}{2^1} + \frac{d_2}{2^2} + \dots + \frac{d_n}{2^n} = \frac{V_{\text{in}}}{V_{\text{FS}}}$$

For an 8-bit converter, $M = L = 4$ and two 4-bit flash converters are required. Each 4-bit flash converter will contain 15 ($2^{N/2}-1$) comparators for a total of 30 ($2*(2^{N/2}-1)$) comparators. When compared to a full flash converter, 255 (2^N-1) comparators are required. This is an eight-fold reduction in circuit complexity, power and area. When compared to the successive approximation converter, two clock cycles instead of eight (N) cycles are required for a complete conversion. This is a reduction in conversion time of four hundred percent, demonstrating the obvious advantages of a subranging architecture. This architecture is referred to as the classical subranging flash A/D converter.

Variations of this classical subranging architecture already exist. Techniques such as pipelining [10] have been applied to further improve the speed of operation. Multiplexing of one flash converter for both clock cycles has been applied to reduce area and power [11,12]. Coarse and fine (accurate) comparators have been attempted to eliminate the gain stage and to improve accuracy [13]. As well, many subranging architectures employ error correction to handle missing codes that may arise from the transition of the MSB section to the LSB section. This usually requires the overlapping of the digital outputs of the MSB and LSB section. This involves redundant comparators in one or both sections.

Various degrees of success have been demonstrated with these different versions of a subranging flash A/D converter. Chapter 4 will describe a novel subranging flash A/D converter that further exploits the advantages of such an architecture.

2.5 Conclusions

Alternative high performance analog to digital conversion techniques have been presented in this chapter. Successive approximation register-type A/D converters offer accuracy, but at the expense of speed. Full flash A/D converters offer speed but are not area efficient and consume large amounts of power. The classical subranging flash A/D converter is a combination of both these techniques, so a more ideal balance of accuracy, area, speed and power is possible. The fundamental principles behind these alternative techniques will now be applied directly to the design of a novel subranging architecture.

Chapter 3

Design Considerations for Subranging Flash A to D Architectures

3.1 Introduction

In this chapter, design considerations for a subranging flash A/D converter will be investigated, including a study of each elemental block. For a monolithic realization, the base technology is a key factor in the design of the circuitry. The technology alternatives will also be explored from a circuit perspective. An understanding of the design trade-offs for the elemental blocks and the technology alternatives that are possible is then applied directly to the design of a subranging flash A/D converter.

3.2 Technology Aspects

The monolithic realization of A/D converters have been dominated by the two mainstream processes; CMOS and bipolar. From these two base processes, a third has emerged, BiCMOS. Each technology has its own inherent advantages.

A CMOS process has many features that are exclusive to this technology and the same can be said for a bipolar process. A BiCMOS process combines these two into one versatile whole. When both options are available on a chip, an understanding of what each option

has to offer will lead to the best possible circuit implementation. A new high performance BiCMOS technology will be used that will permit the realization of the new subranging architecture.

3.2.1 CMOS Technology

For the past decade, CMOS processes have been dominant technology for LSI and VLSI designs. This dominance is driven by applications that require large volumes of circuits in a cost-effective fashion. A CMOS process is an ideal technology for such a requirement since high packing density and low power consumption are the two main attributes. The popularity of the CMOS process as the technology of choice for digital circuit designers has arisen from the demand for more and more digital functionality within a given die size.

Fundamentally, all digital circuits must discern the logical states of true or false. This representation is accomplished in a CMOS process with switches that can be turned on or off (logical "1" or "0"). The attraction of a CMOS process is that power (ie current) is not necessary for a digital gate to remain in either logical state of "1" or "0" since current is only consumed during the transition from one state to another. The advantage of this simple behaviour cannot be underestimated. This feature permits the integration of complex digital block with only a marginal increase in power consumption. Fully complementary devices (n and p-channel MOS transistors) in CMOS process make such a characteristic possible.

MOSFET devices have been evolving to smaller and smaller transistor sizes which helps to minimize the power consumption. However, the primary motivation is to achieve higher packing densities and faster speeds of operation. Smaller geometries also result in smaller capacitor parasitic values. To date, gate lengths of 0.8 microns represent the state of the art in CMOS technology.

Aside from the digital design advantages, CMOS has also been successfully exploited for many analog applications; specifically for sampled-data. This is due to the inherent characteristics of MOSFET devices. Switched-capacitor filter designs are only possible with a technology that can provide analog building blocks that have high input resistances. Specifically, proper use of operational amplifiers in virtual ground or feedback configurations requires the inputs (positive and negative) to be high impedance. This requirement is met very easily with field-effect-transistors. The value of the input resistance (r_i) for a MOS operational amplifier (typically a MOS differential pair) is very close to infinite since the gate of a MOSFET is controlled by a gate voltage, not a current. Hence, theoretically, the input resistance is infinite. In practice, there may be small leakage currents through the polysilicon gate but nevertheless, this value is still many orders of magnitude smaller than the base currents necessary for the operation of a bipolar transistor. Gate leakage currents in a MOS device are a reflection of the quality of the fabrication process, specifically, the growth of the gate oxide. For a high performance process, the leakage currents are negligible.

A MOS transistor can be viewed as a voltage-controlled current source. This is apparent in the equations that characterize a MOS device and in its small signal model (Figure 3.2-1).

Linear Region:
$$i_d \approx \frac{\mu_n C_{ox} W}{L} * (V_{gs} - V_t - \frac{V_{ds}}{2}) * V_{ds}$$

Saturation Region:
$$i_d \approx \frac{\mu_n C_{ox} W}{2L} * (V_{gs} - V_t)^2$$

where:

- μ_n = mobility constant
- C_{ox} = gate oxide capacitance
- W = gate width
- L = gate length
- V_t = threshold voltage
- V_{gs} = gate-source voltage
- V_{ds} = drain-source voltage

Figure 3.2-1

Small-Signal Model of a MOS Device

MOS saturation small-signal parameters:

$$g_m = \frac{\partial i_d}{\partial V_{gs}} = \frac{\mu_n C_{ox} W}{L} * (V_{gs} - V_t)$$

$$r_i = \infty$$

$$g_d = \frac{\partial i_d}{\partial V_{ds}} \quad g_{mb} = \frac{\partial i_d}{\partial V_{sb}}$$

where:

- g_m = transconductance
- r_i = input resistance
- g_d = drain conductance
- g_{mb} = body conductance

The inherent characteristic of infinite input resistance is also advantageous in the design of A/D converters. CMOS technologies have been successfully used in the implementation of all types of A/D converters (SAR, full flash and subranging). The analog circuitry necessary for a charge redistribution-based SAR architecture is primarily related to the design of the comparator. The digital circuitry for the control logic and the holding register is ideally implemented in a CMOS process. The availability of high quality switches and linear capacitors in an analog CMOS process lends itself very well to a successive approximation A/D converter.

Full flash converters designed in a pure CMOS technology are also possible. The key analog component in this architecture is the

comparator and will be the key in the subranging flash A/D converter as well. In designing CMOS comparators to be used for an A/D converter, the matching characteristics of MOS devices must be taken into consideration. In fact, techniques such as offset cancellation (or autounnulling) [2] are necessary to eliminate the offset voltages inherent to MOS transistors. Section 3.3.2 has more details.

3.2.2 Bipolar Technology

While the CMOS technology has been the dominant choice for large scale digital integrated circuit design, the bipolar technology has continued to be the choice for many other monolithic designs. A bipolar process is ideally suited for applications that require high voltage, low noise or high speed. A bipolar transistor has characteristics that are well suited for many linear (analog) applications.

For optimizing an analog building block such as an operational amplifier, the individual small-signal parameters (Figure 3.2-2) are the most important design parameters to understand. One of the more important parameters is the transconductance parameter (g_m) of the transistor. The transconductance parameter is the relative change in collector (drain) current as a function of the change in the base-emitter (gate-source) voltage (MOS equivalents are in brackets). When compared to a MOS transistor, the transconductance parameter of a bipolar device is typically several orders of magnitude greater.

Figure 3.2-2
Small-Signal Model of a Bipolar Device

Bipolar small-signal parameters:

$$g_m = \frac{\partial i_c}{\partial V_{be}} = \frac{qI_c}{kT}$$

$$r_\pi = \frac{\beta}{g_m} \quad r_o = \frac{1}{\left(\frac{kT}{qV_A}\right) * g_m}$$

where:

g_m = transconductance

r_π = input resistance

β = drain conductance

r_o = output resistance

k = Boltzman's constant

T = temperature

q = charge

V_a = early Voltage

V_{be} = base-emitter voltage

This higher g_m , combined with the higher output resistance (r_o) of a bipolar transistor, is the reason why the intrinsic gain ($r_o g_m$) of these devices is so much higher than for MOS devices. This inherent characteristic is the primary reason this technology is so favourable for analog design.

Aside from being beneficial for the intrinsic gain of a transistor, the high output resistance (r_o) is also desirable for biasing networks or current sources. Stable, constant quiescent bias currents ensure proper DC operating conditions for operational amplifiers. When compared to a MOS transistor, the output resistance is higher for a bipolar device. A comparison of transistor I-V characteristics for typical devices, (Figures 3.2-3 and 3.2-4) demonstrates how the forward active region for a bipolar device (saturation region for MOS) is much flatter. As V_{ce} changes, the quiescent operating current (I_c) does not change as much as the MOS counterpart (I_{ds}).

In terms of noise performance, bipolar transistors are better than MOS transistors. This is another reason this technology is better suited for analog applications. The phenomena of flicker noise (commonly called $1/f$ noise) is more prevalent in a MOS technology. This noise component arises from the energy states that are trapped in the gate oxide/silicon interface. These trapped states can release or trap electrons from the channel and thus contribute to the noise energy at low frequencies. There is no gate oxide in a bipolar device, so this type of flicker noise is not present. As well, the thermal noise

Figure 3.2-3
Transistor Characteristics of an NMOS Device
W/L: 4 / 0.8 μm

Figure 3.2-4
Transistor Characteristics of a Bipolar NPN Device
Emitter size: 4 X 0.8 μ m

component for a bipolar transistor is lower than for a MOS device. This is true for a given current, because the transconductance is so much higher.

$$\text{Thermal Noise for MOS:} \quad (V_{nT})^2 = 4kT * \frac{2}{3g_m} * \Delta f$$

$$\text{Thermal Noise for bipolar:} \quad (V_{nT})^2 = 4kT * (r_b + \frac{1}{2g_m}) * \Delta f$$

where: V_{nT} = thermal noise voltage
 r_b = base resistance
 f = frequency

Another important characteristic necessary for analog design is good matching of transistor differential pairs. Input-referred offset voltage (V_{off}) is the differential input voltage necessary to restore the output voltage (V_{out}) to zero (Figure 3.2-5). An offset voltage can arise from process variations and photolithographic resolution variations. Given these factors to be the same for both technologies, a MOS differential pair will still have an offset voltage that is an order of magnitude greater than for a bipolar device. This larger offset in a MOS differential pair is due to the $(\frac{V_{gs} - V_t}{2})$ term, which is much greater than the $(\frac{kT}{q})$ term present in a bipolar device.

Bipolar

$$V_{off} = \left| \frac{kT}{q} \left[\frac{\Delta R}{R} + \frac{\Delta I_s}{I_s} \right] \right| \approx 1 \text{ mV}$$

MOS

$$V_{off} = \left| \Delta V_t + \left[\frac{V_{gs} - V_t}{2} \right] \left[\frac{\Delta R}{R} + \frac{\Delta(W/L)}{(W/L)} \right] \right| \approx 5-10 \text{ mV}$$

where:

- V_{off} = offset voltage
- R = load resistance
- I_s = saturation current

Figure 3.2-5
Offset Characteristics of a MOS and Bipolar Device

When signal levels are extremely small, bipolar differential pairs are the obvious choice for such applications. This will be important to our choice of circuit topology for the subranging flash A/D converter.

Normal forward active operation of a bipolar device requires the base-emitter junction to be forward biased. The collector-base junction must be reversed biased so that carriers injected by the emitter are collected as they are swept across the base. If the collector-emitter voltage is lowered, a "threshold" is crossed where the collector-base junction is no longer reverse biased. When this collector-base junction becomes forward biased, carriers are also injected into the base from the collector which is in the opposite direction to those injected from the emitter resulting in a build up of charge stored in the base region. This condition is called saturation. The charge build up is seen as a varying, non-linear input capacitance by any signal connected to the base. This saturation characteristic of a bipolar transistor is an undesirable phenomena and is a disadvantage of using bipolar devices. The charge build up in the base degrades the speed of operation because a finite time is required to remove the charge when the transistor exits from the saturation condition. For maximum performance using bipolar transistors, care is taken to avoid entering the condition of hard saturation. As long as this is maintained, bipolar devices can be exploited for many analog applications.

3.2.3 BiCMOS Technology

The advantages of a CMOS and a bipolar technology have been presented in the previous two sections. Both processes have unique qualities that are desirable for the design of a monolithic A/D converter. From these two basic processes, a new technology, BiCMOS, has emerged. As the name implies, this new versatile technology is a mixture of bipolar and CMOS design capabilities. Such a technology allows the implementation of an A/D converter to be fully optimized. The novel subranging architecture to be presented in Chapter 4 will be implemented in a new high performance BiCMOS process [14]. The layout, design rules and models will be based on this process.

This high performance process has not been optimized for one process, at the expense of the other. The process flow has been engineered to permit optimal performance for both CMOS and bipolar devices, when used in both analog and digital circuitry. As a consequence of this, the process flow is more complex and more mask layers are necessary. This is the trade-off for having a high performance technology.

For the MOS transistors, many features have been included. A twin well process has been adopted, for minimal compromise in the n and p-channel device characteristics. The minimum length is 0.8 microns. This aggressive feature size allows for high packing density and fast switching speeds. Lightly doped drains are part of every MOS transistor, to minimize any hot electron mechanisms that can affect

the reliability [15]. A buried layer is also an integral part of the CMOS process flow. Parasitic resistances are minimized with this layer and the MOS phenomena of latch-up is controlled. High quality polysilicon to polysilicon linear capacitors are also part of this process, to allow sampled-data analog circuits such as switched capacitor filters.

From the bipolar perspective, many features in this BiCMOS process qualify it to be a high performance technology. The basic element is a high speed NPN transistor with an f_t of 8 GHz. An 0.8 micron polysilicon emitter is used to achieve high current gains. Collector resistance is minimized with a buried layer and an heavily doped n^+ plug (sinker). As well, high resistance polysilicon resistors are part of this process. This allows for smaller resistor sizes and well matched resistor dividers.

To exploit these many device features, a triple level planarized metallization process is implemented in this BiCMOS technology. High packing densities and low resistance interconnect permit optimized layouts.

3.3 Circuit Aspects

The circuit elements used in an analog to digital converter will depend on the architecture that is used. For a SAR-type implementation, a large portion of the converter is digital logic that controls the conversion process. For a full flash converter, the $2^N - 1$ comparators will be the largest portion of the design. In terms of accuracy and resolution, a key circuit in any of these architectures will be the comparator.

3.3.1 Comparator

A comparator is a circuit that compares one analog signal with another analog signal (normally a reference voltage) (Figure 3.3-1). The output is a binary signal based upon the comparison. Many design considerations must be balanced. Ideally a comparator must have high gain, so that it can resolve small input signals and translate them to full-rail binary signals. Equally as important, a comparator must be very fast (ie; short propagation delays) so that it can operate at high speeds. Speed and gain are conflicting design criteria, so the relative importance of each must be considered. Power, area, stability, noise and offset are other factors that cannot be neglected.

Figure 3.3-1

In many applications, the binary output signal of a comparator is connected to some digital circuitry. In such a case, it is desirable to have the output synchronous to the digital logic. For this reason, many comparators have a clock associated with their operation. With a clocked comparator, the output is only valid at a certain time and the output is held at the previous logical state prior to the start of this period. Conversely, the output of a continuous comparator can change at any time. For the subranging converter to be implemented in Chapter 4, both types of comparators are required.

As previously mentioned, gain or amplification of a comparator is very important. Because it is only the final digital output level that is relevant, the amplification does not necessarily have to be linear nor

continuous in time. Consequently, a comparator can be designed using non-linear gain stages or with cascaded gain stages to distribute the amplification. Stability is not important because there is no closed loop in an analog sense.

In terms of basic comparator design approaches for A/D converters, three generic topologies have been commonly used. These three approaches can be categorized as single stage amplifiers, multi-stage amplifiers (cascading of single stage amplifiers) and regenerative sense amplifiers (cross-coupled single stage amplifiers). A single stage amplifier is the simplest type of comparator. Such an amplifier abstracted to a simple equivalent circuit is shown in Figure 3.3-2(a), would require transistor sizes to be very large, to achieve the necessary gain. Multi-stage amplifiers (Figure 3.3-2(b)) allow partitioning of the overall gain, so large devices are not necessary. However, each gain stage will result in additional delay.

Figure 3.3-2

Regenerative sense amplifiers (Figure 3.3-2(c)) can provide a very good balance between area, speed and gain[16]. However, they do require clocking for proper functionality. The key to the operation of this configuration is to establish an imbalance on the input node voltages of the cross-coupled gain stages (as a function of the input signals to the comparator). So long as this criteria is met when the amplifier is clocked, the resulting output will reflect the input voltage differences. This description is precisely how a clocked comparator must function. The amplification is non-linear and discontinuous in time but this is acceptable for our application. Such a regeneration technique is the most popular choice for A/D converters. The speed of operation and small area are other strong reasons for its dominance.

3.3.1.1 CMOS Comparator Design

The concept of regeneration in a comparator has been implemented in a CMOS technology [16]. However, comparators designed purely in a CMOS process can be large. Due to low transconductance (g_m) and smaller output resistance (r_o), the geometry (W/L) must increase to achieve intrinsic gains comparable to a bipolar counterpart. As well, CMOS differential pairs require compensation for large offset voltages inherent to this technology. Despite this undesirable sensitivity to mismatches, CMOS comparators have been successfully implemented.

The sensitivity to mismatch has been attacked by employing offset cancellation (or autonulling) techniques [17]. The technique involves

storing the offset voltage of an amplifier onto a capacitor and summing this voltage with the input signal to cancel the offset (Figure 3.3-3). During the ϕ_1 period, the amplifier is in unity gain feedback configuration. As a result, the offset potential of the amplifier is stored across the capacitor, C_{offset} . This potential lies in between the virtual ground node and true ground. During the ϕ_2 period, the actual input signal is applied to the circuit and the stored offset voltage is summed into the circuit. This is very effective for eliminating the large offset voltage characteristic of MOS differential pairs. Such a technique is only possible in a CMOS technology because of the nearly infinite input resistance of MOS transistors which allows the offset voltage to be sampled onto C_{offset} . In CMOS sampled-data applications, non-overlapping clocks, high quality switches and capacitors are readily available so additional elements are not necessary.

Figure 3.3-3

The above autonulling principles can apply to A/D converters. However, additional time is necessary to perform the autonulling process and this contributes to the overall conversion time. In a high

speed application, it is desirable to avoid this step, if possible. For this reason and because other alternatives are available in the BiCMOS process, a purely CMOS comparator will not be adopted.

3.3.1.2 Bipolar Comparator Design

Clocked comparators using a bipolar regenerative sense amplifier have seen widespread use in full flash A/D converters [16]. Such an implementation can also be applied to a subranging flash architecture. This section will be a detailed analysis of a classical bipolar comparator. The analysis will focus on the delay through such a topology.

The configuration of a basic bipolar comparator consists of a preamplifier and a regenerative sense amplifier (Figure 3.3-4(a)). During the ϕ_1 phase (sample phase), the preamplifier samples the input signals using the Q1-Q2 differential pair. During the ϕ_2 phase (hold phase), the resulting differential output voltage is applied to the cross-coupled transistor pair Q3-Q4. The clock phases ϕ_1 and ϕ_2 are non-overlapping clocks. Transistors Q5 and Q6 are used to steer the tail current I_{EE} to and from the latch or preamplifier.

The preamplifier is necessary to isolate the regenerative sense amplifier from the input analog signal. Without this stage, any large transitions or spikes on the input signal may cause errant state changes on the regenerative latch. As well, the preamplifier serves a second purpose. The analog signal connected to the comparator must drive many other comparators and it is important to minimize the input capacitance seen by this signal. By having a preamplifier stage between the signal and the regenerative sense amplifier, the

Figure 3.3-4

larger load capacitance of the cross-coupled latch is isolated from the signal.

Given such a topology, the dynamic performance of this circuit can now be examined. An understanding of its behaviour and its limitations will lead to an improved design in Chapter 4. In a high speed application such as ours, the delay through the comparator must be minimized. This allows for faster clock rates or shorter overall conversion times.

Before the start of the hold phase, the output signals from the preamplifier will have settled to their final values. Based on this differential voltage, the final comparator output levels are then regeneratively determined. The time required for the transition from the start of the hold phase to final output level is called the regeneration time. This delay can be determined by analyzing the cross-coupled latch and the load resistor connected to it (Figure 3.3.-4(b)).

Given the small signal model of a cross-coupled pair of bipolar transistors (Figure 3.3-4(c)), the S-domain characteristic equation that defines the change in the output ($V_{o2}-V_{o1}$) as a function of the differential input voltage ($V_{i2}-V_{i1}$) is:

$$\begin{aligned}
0 = & s^2 r_b (C_\pi C_\mu + C_\pi C_L + C_L C_\mu) + \\
& s (C_\pi (1 + \frac{r_b}{R_L}) + C_\mu (4 + \frac{r_b}{R_L} - g_m r_b) + C_L) \\
& - (g_m - \frac{1}{R_L})
\end{aligned}$$

Assuming $r_b \ll r_\pi$, an approximate solution for the regeneration response is given by:

$$(V_{o2} - V_{o1}) \approx A_L * (V_{i2} - V_{i1}) * (\exp(t/T_{reg}))$$

where: A_L = amplifier gain

$$T_{reg} = \frac{(C_\pi(r_b + R_L) + C_\mu(4R_L + r_b(1 + R_L g_m)) + C_L R_L)}{(g_m R_L - 1)}$$

When $R_L \gg r_b$, the regeneration time constant simplifies to:

$$T_{regeneration} \approx \left(\frac{C_{total}}{g_m} \right) * \left(\frac{g_m R_L}{g_m R_L - 1} \right) \quad \{3.3-1\}$$

where: $C_{total} = C_\pi + C_L + 4C_\mu$

Appendix 1 provides a detailed derivation of the above equations.

Figure 3.3-5

During the ϕ_1 phase (sample phase), the preamplifier (Q1-Q2) samples the input signals (Figure 3.3-5(a)). The collector currents through each transistor are given by:

$$I_{C1} = \frac{\alpha I_{EE}}{(1 + \exp(\frac{-qV_{in}}{kT}))}$$

$$I_{C2} = \frac{\alpha I_{EE}}{(1 + \exp(\frac{qV_{in}}{kT}))}$$

where $V_{in} = V_{i1} - V_{i2}$

The small signal linearized model of this input stage (Figure 3.3-5(b)) can be used to determine its dynamic behaviour. The output load capacitance is approximated by C_{total} as defined in equation (1-a). Given the total current (I_{EE}), the node voltages of the collectors are:

$$V_{O1} = V_{CC} - \alpha R_L I_{EE} - (I_{C1} R_L - \alpha R_L I_{EE}) * [1 - \exp(\frac{-t}{R_L C})]$$

and

$$V_{O2} = V_{CC} - (I_{C2} R_L) * [1 - \exp(\frac{-t}{R_L C})]$$

At the start of the sample phase, node V_{O1} and V_{O2} are at the steady-state polarities, as determined by the previous regeneration phase. During the sample phase, these two nodes must first recover from these voltage extremes. This recovery time can be determined by solving for t when $V_{O1} = V_{O2}$:

$$\frac{[1 - \exp(\frac{-t}{R_L C})]}{1 + \exp(\frac{qV_{in}}{kT})} = \frac{[1 + \exp(\frac{-qV}{kT}) * \exp(\frac{-t}{R_L C})]}{1 + \exp(\frac{-qV_{in}}{kT})}$$

See Appendix 2 for detailed derivations.

$$\exp\left(\frac{-t}{R_{LC}}\right) = \frac{1}{2} * \left[1 - \frac{\exp\left(\frac{-qV}{2kT}\right)}{\exp\left(\frac{qV}{2kT}\right)} \right]$$

$$\frac{-t_{rec}}{R_{LC}} = \ln \left[\frac{1}{2} (1 - \exp\left(\frac{-qV}{kT}\right)) \right]$$

For an 8 bit A/D converter, using a 5 volt supply, 1/2 LSB resolution would correspond to a 3 mV step. With this as an input voltage, the recovery time is given by:

$$t_{rec} = 2.87 R_{LC} C_L = \frac{2.87(V_{out})C_T}{I_{EE}}$$

With the tail current of I_{EE} , the regeneration time is given by:

$$t_{reg} = \frac{2kTC_T}{qI_{EE}}$$

At room temperature, this delay is:

$$t_{reg} = \frac{0.057C_{Total}}{I_{EE}}$$

In assuming an output swing ($V_{O1} - V_{O2}$) of 1 volt for this bipolar comparator, the recovery time is over forty times greater than the regeneration time (Figure 3.3-6).

$$t_{rec} \gg t_{reg}$$

The overall speed of the comparator is governed by the recovery time, not by the regeneration time. This can be reduced by increasing the tail current. However this is an undesirable trade-off, if power consumption is an important constraint in the overall design. This formal analysis of a typical bipolar comparator has highlighted the delay limiting characteristics of such a design.

$$T_{recovery} \gg T_{regeneration}$$

Figure 3.3-6

3.4 Conclusions

The design considerations for a subranging flash A/D converter have been presented. The trade-offs between the base technologies were discussed. A CMOS technology offers high density, low power and capabilities for sampled-data design techniques. A bipolar process offers low offset voltages, high gain and low noise performance. A BiCMOS process is an ideal combination that can be exploited in the design of a high speed analog to digital converter. This will be presented in Chapter 4. The circuit aspects of a CMOS comparator and a bipolar comparator have also been discussed. Alternatives available in a BiCMOS process have created new comparator designs. One such technique using MOS switches and capacitors to sample the input, instead of preamplification, will be presented in Chapter 4. This will be the key component in the novel architecture that will also presented in Chapter 4.

Chapter 4

Design of an 8 Bit BiCMOS Subranging Flash Analog to Digital Converter

4.1 Introduction

In the previous chapters, the architectural alternatives for high speed A/D converters in the context of the capabilities of the VLSI fabrication technology were presented. In this chapter, these considerations will be applied to the design of a high speed BiCMOS subranging flash analog to digital converter. Particular emphasis will be placed on a high speed BiCMOS comparator. This will be the key component in the novel architecture that will also be discussed in this chapter. The subranging flash A/D design that will be presented will exploit the full potential of a BiCMOS technology.

4.2 High Speed Comparator Design

BiCMOS comparator designs are becoming more and more popular [18,19]. This section is a detailed study and design of such a comparator [18]. It offers high speed and low power. The analysis will focus on the delay through this element and how each aspect of the BiCMOS technology is utilized to achieve superior performance.

The regenerative sense amplifier is comprised of a differential pair Q1 and Q2 (Figure 4.2-1(a)). Two cross-coupled capacitors C3 and C4 provide positive feedback. The tail current for the bipolar differential pair is supplied by a capacitor C5. All the MOS devices

function as switches for which they are ideally suited. Assuming adequate settling, no voltage drops are experienced across the source and drain of a MOS device. This is not the case if bipolar switches are used. The capacitors C1 to C5 are high quality linear poly/poly2 sandwiches. The differential pair are NPN devices which offer low offset voltage characteristics.

During the sample phase ϕ_1 (Figure 4.2-1(b)), the input voltages are sampled onto the four capacitors (C1 to C4) and the bases of the NPNs. The PMOS devices M3 and M4 are turned on and this ties the collectors of Q1 and Q2 to Vdd. As well, during this phase, C5 is charged to the full rail voltage. The emitters of Q1 and Q2 are open in this phase and the NPN differential pair is inactive.

During the regeneration phase ϕ_2 (Figure 4.2-1(c)), the sampling switches M1 and M2 are open and one side of C5 is connected to the emitter node shared by Q1 and Q2. The other side of the capacitor is connected to Vss. The charge stored on C5 is steered between Q1 and Q2. Because of the cross-coupling of C3 and C4, the voltage difference stored on C1 to C4 is regeneratively amplified at the collector nodes of Q1 and Q2. The collector nodes (vout1 and vout2) are the outputs of this sense amplifier. During each clock cycle, only a fixed amount of charge is used and steered between Q1 and Q2. There is no steady-state current flowing through the emitters as is the case with many bipolar differential pairs. As well, power is only

consumed during one half the clock cycle when C5 is being charged up. These two factors minimize the power consumption.

To analyze the delay characteristics of this sense amplifier, the small-signal linearized model of the design during the regeneration phase must be evaluated (Figure 4.2-2).

Linearized model of regenerative sense amplifier

Figure 4.2-2

The following S domain characteristic equation for this model defines the change in the output ($V_{o2}-V_{o1}$) as a function of the differential input voltage ($V_{i2}-V_{i1}$):

$$0 = s[(C_\mu + C_3 + C_1 + C_\pi)(C_3 + C_L + C_\pi) - (C_3 - C_\pi)^2] - g_m(C_3 - C_\mu) + (C_3 + C_L + C_\mu)/r_\pi$$

The response for this equation is:

$$(V_{o2}-V_{o1}) = A_L * (V_{i2}-V_{i1}) * (\exp(t/T_{reg}))$$

where: A_L = amplifier gain

$$T_{reg} \approx \frac{[C_1 + C_\pi + C_L + C_L(C_1 + C_\pi)/C_3]}{g_m}$$

See Appendix 3 for a detailed solution.

Recalling that the time constant for the classical bipolar regenerative sense amplifier (equation 3.3-1) was given by:

$$T_{regeneration(bipolar)} \approx \left(\frac{C_\pi + C_L + 4C_\mu}{g_m} \right) * \left(\frac{g_m R_L}{g_m R_L - 1} \right)$$

since the second term is very close to unity.

$$T_{reg(bipolar)} \approx \left(\frac{C_\pi + C_L + 4C_\mu}{g_m} \right)$$

In the BiCMOS comparator, if the C_μ term is ignored, the regeneration time constant for the BiCMOS comparator is :

$$T_{reg(bicmos)} \approx \frac{[C_1 + C_\pi + C_L + C_L(C_1)/C_3]}{g_m}$$

Depending on the values of the sampling capacitors C_1 and C_3 , this time constant is only slightly larger than for the bipolar comparator. Recall that the limiting factor in the classical bipolar regenerative sense amplifier was the recovery time and not the regeneration time. In this BiCMOS design, there is no recovery time. By using sample-data techniques (ie MOS switches and capacitors), no

preamplification is used in this sense amplifier. This allows the clock periods to approach the regeneration time constant. A higher speed of operation is now possible.

This approach to the regenerative sense amplifier is only possible in a BiCMOS process. The inherent advantages of a MOS and bipolar technology are used to their full extent.

4.2.1 Design

The above principles have been applied to the design of a high speed BiCMOS comparator (Figure 4.2-3). This will be the key component in the novel architecture that will be presented in the next sections. In designing the comparator, the following were the key requirements:

- i) A large common mode input range to encode large input voltage signals. For this design a 3 Vp-p signal using a 5 volt supply will be the goal.
- ii) Resolution of at least $1/2$ LSB for an 8 bit converter. For this design $1/2$ LSB = 5 mV.
- iii) Fast output slew rate.
- iv) Low power consumption.
- v) CMOS compatible output levels to interface to digital control logic.

The input stage for this comparator is the BiCMOS regenerative sense amplifier described in the previous section. All switches are full complementary MOS transmission gates with both p and n channel devices sized the same. This was done to minimize any charge injection inherent to MOS switches turning off.

Figure 4.2-3

Schematic of BICMOS Comparitor

12-3

CMOS Comparator

The outputs of the regenerative amplifier are fed into a current-switch latch. Source followers (ML1 and ML2) are used to buffer the sense amplifier output to the latch. The buffer also provides the correct level-shift necessary for the latch.

Two BiCMOS inverters drive the outputs of the latch. This was done for high drive capability and to achieve CMOS compatible levels. The design is balanced and fully differential. Both an output and its complement are generated and are necessary as part of the optimized encoding scheme to be used in the 8 bit subranging flash A/D converter (see Section 4.4).

4.2.2 Layout and Simulation Results

The high speed comparator has been designed and a layout has been completed in the high performance BiCMOS process described in Section 3.2.3 (Figure 4.2-4). The values for $C1 = C2$ are 0.2 pF and $C3 = C4$ are 0.1 pF. These values were selected so they would be as small as possible for high speed operation and yet still be the dominant values in the regeneration time constant. If the values were any smaller, the junction capacitances of the bipolar devices could possibly dominate. From a manufacturing perspective this may lead to less reproducible results. The load capacitance (C_L) is the total of the collector to substrate capacitance, the source-drain capacitance of the PMOS devices (M4 and M3), and the gate capacitance of the source followers (ML1 and ML2).

Figure 4.2-4
Layout of BiCMOS Comparator

Simulation results confirm that there is no recovery time in this design. This can be seen in Figure 4.2-5 where the internal collector nodes (VCQ1 and VCQ2) are shown. During the sample phase VCQ1 and VCQ2 are pulled to Vdd. In this simulation, the reference voltage (2.50V) is held constant and the input signal changes from 2.4 volts to 2.503 volts. When the clock is high, the inputs are sampled and when the clock is low, the voltage difference is regeneratively amplified. This simulation also demonstrates how the comparator can resolve a voltage difference of 3 mV. A similar simulation was performed where the input signal changed from 2.4 volts to 2.497 volts (ie; 3 mV below the reference voltage) and the output did not toggle. The design target of 5 mV resolution has been achieved. Since there is no recovery time, the speed of this comparator can now approach the regeneration time constant. Simulations with clock rates as fast as 120 MHz have been performed.

The output stage of this design uses two BiCMOS inverters. These BiCMOS drivers ensure adequate drive capability for any combinatorial logic that they may be connected to. The output levels are not full-rail but are high and low enough for CMOS logic levels. This can be seen in Figure 4.2-6, where the outputs from the simulation are shown. VOL is limited to a V_{be} above Vss and VOH is limited to $V_{dd} - V_{CE(Q85)}$. The output slews to a valid logic level within 2 nS, giving a slew rate of approximately 2000 V/ μ s.

Figure 4.2-5
Simulation Results of High Speed Comparator

Figure 4.2-6

Simulation Results of High Speed Comparator

The following are the simulated characteristics of the high speed BiCMOS comparator:

Area	240 X 80 μm
Max. Frequency of Operation	120 MHz
Input Capacitance	300 fF
Slew Rate	2000 V/ μs
VOH/VOL	4.2/0.6 V
Current Consumption	1 mA
Resolution	+/- 3 mV
Common Mode Input Range	1 to 4 V
Supply	5 V
Power	5 mW

Direct comparisons of high speed comparators used in A/D converters are difficult because specific comparator results are often omitted and only results of the overall designs are published. Thus extracting direct figures of merit of the individual comparators used in these designs becomes impossible. However, there are a few publications showing the state of the art in high speed comparators. In terms of area, the size is less than one half [16] or comparable [18] to other published CMOS or BiCMOS designs. The impact of this small area becomes obvious when the comparator design is incorporated into the overall A/D converter. See Section 4.10 for final results.

In terms of power consumption the circuit is also comparable to other low power comparators [16,18]. Still lower current

consumption in this design is possible if lower output voltages and a smaller storage capacitor are used. Ultimately the architecture (ie; how many comparators are used) will have the strongest bearing on the total current consumption.

Clock rates of 100 MHz [16] and 200 MHz [18] have been published to date. These represent the state of the art for low power comparators. Pure bipolar comparator designs can achieve faster clock rates but the power consumption is typically an order of magnitude greater. The final result achieved in this BiCMOS design was 120 MHz. This is an acceptable speed for the architecture that this comparator will be used in, and at a reasonable power.

4.3 Architecture

The following is a circuit description of an 8 bit subranging flash A/D converter that exploits the capabilities available in a BiCMOS technology and uses the high speed regenerative sense amplifier design described in Section 4.2. This design employs a novel architecture for performing the two-step flash conversion. Some of the features of this design and implementation are :

- i) The design is implemented in an 0.8 micron high performance BiCMOS process.
- ii) Compared to a classical subranging A/D converter, fewer comparators are used (12 vs 32). Eight are high speed latching comparators and four are simpler non-latching continuous comparators.
- iii) One level of multiplexing and decoding is used to minimize delays
- iv) Digital error correction is performed between transition from the coarse to fine encoding section.
- v) A simple and accurate D/A implementation is used. No amplification is needed.
- vi) An optimized encoding scheme is used to minimize area.
- vii) The design has very simple timing requirements. High speed non-overlapping clocks are synthesized internally.
- viii) Eight bit resolution is achieved using a single 5V supply.

ix) Pipelining is used to reduce the conversion time.

This design consists of many distinct blocks (Figure 4.3). Each block will be described in further detail in the next sections. The assumption is that the analog input signal is centered around analog ground (2.5V). The maximum input signal is 3 V_{p-p}, centered on AGND. Two clock cycles are required in this design for one analog to digital conversion. The design goal is a clock rate of 40 MHz. One analog to digital conversion will be performed in 50 ns.

During the first clock cycle, the first four bits are determined. The most significant bit (D7) is determined by comparing the input signal with AGND. Depending on the outcome, the correct MSB reference voltage references are connected to the bank of comparators (Figure 4.3.2). In parallel with this operation, the inputs to a bank of eight high speed latching comparators are connected to the input signal and a three bit flash A/D conversion for bits D6 to D4 begins. All of the above must occur within the period T₁, (Figure 4.3.4) which is only of 12.5 ns duration. The speed of the comparator and the sampling of the reference voltages and V_{in} through the Mux Decoder will be the critical path for this timeslot. On the falling edge of T₁, the comparators are latched and three bits (D6, D5, D4) are encoded. At this point, the 1st four bits are known.

During T₂, a D/A conversion is performed and this value is subtracted from the input signal. Given the three bits (D6, D5, D4), the location of the resistor-tap voltage which the input signal lies

above is known. It is this tap voltage that is subtracted from the input, leaving a residual voltage. This $V(\text{residue})$ is used as the input voltage for the next clock cycle. Ideally, this residual voltage will lie somewhere within one segment of the MSB ladder. Once $V(\text{residue})$ is known, it is sampled onto the bank of comparators.

For the next 12.5 ns period (T3), a block that is called Sub Range Finder (SRF) is used to determine the approximate location of $V(\text{residue})$. Three simple, non-latching, continuous comparators are used to segment one section of the MSB ladder into four smaller segments (Figure 4.3.3). $V(\text{residue})$ will lie somewhere in one of the four possible smaller segments. The outputs of these three comparators are used to control the Mux Decoder. This connects the LSB resistor ladder to the bank of 8 high speed comparators. The ranges that these resistor taps span overlap each other and are wider than the smaller segments defined by SRF. With the SRF (2 bits) and the LSB section (3 bits), five bits are encoded and only four bits actually are needed. The third bit (D2) is determined in two locations (the SRF and LSB section). This redundancy is part of the error correction capability of this design. During the last 12.5 ns period (T4), the LSB reference voltages are sampled onto the eight comparators and the last three bits, D2, D1, D0 are encoded. The critical areas will be the delay through the Mux Decoder and the speed of the comparators.

If $V(\text{residue})$ lies within the four sub-section defined by the SRF sections, no correction is performed. The function of the SRF section

is to direct the LSB section to the approximate location of $V(\text{residue})$. Because it is a guess or estimate of $V(\text{residue})$, it is possible for the actual value to lie outside of the SRF sub-section. When this happens, error correction is performed on D3, D2. Either a "01" is added or subtracted to or from these two bits. Addition or subtraction are very simple combinatorial functions that can be implemented digitally. If no error correction is required, D3, D2 are left unmodified. This error correction will occur during timeslot 1 (T1). This happens in parallel, as the input signal is sampled for the next conversion. This is the only section that is pipelined. At the end of T1, the eight bit output, B(7:0) is valid and held until the next T1 time slot.

Figure 4.3.1
Block Diagram

Range Finder & MSB Encoding

Figure 4.3.2

$$A = \overline{\text{SRF3}} \cdot \overline{\text{SRF2}} \cdot \overline{\text{SRF1}}$$

$$B = \text{SRF3} \cdot \overline{\text{SRF2}} \cdot \overline{\text{SRF1}}$$

$$C = \text{SRF3} \cdot \text{SRF2} \cdot \overline{\text{SRF1}}$$

$$D = \text{SRF3} \cdot \text{SRF2} \cdot \text{SRF1}$$

Sub-Range Finder and Mux Decoder

2

of/de

2

PM-1 3½"x4" PHOTOGRAPHIC MICROCOPY TARGET
NBS 1010a ANSI/ISO #7 EQUIVALENT

PRECISIONSM RESOLUTION TARGETS

PIONEERS IN METHYLENE BLUE TESTING SINCE 1974

Microl

10000 COUNTY ROAD 2, BURNING WOOD, OH 44029, USA
TEL: 612 435 7000 FAX: 612 435 7001 T/L: 848888440

Timing

Figure 4.3.4

4.4 Bank of Comparators

In this 8-bit subranging architecture, two 3-bit flash conversions are performed. The first conversion is a coarse comparison that encodes the 7th, 6th and 5th most significant bits. The second flash is a fine comparison that encodes the last 3 bits. Both 3-bit flash conversions share the same bank of eight high speed BiCMOS comparators. This is possible because the comparator was designed to meet the common mode input range needed for the coarse comparison and to have enough resolution for the least significant bit during the fine comparison. By multiplexing these comparators, area and power consumption are minimized. This does impose more design constraints on the high speed comparator but these design requirements have been met, as shown in Section 4.2.

The input signal is compared with eight different reference voltages (Figure 4.4.1). The outputs of the comparators are a logic low when the input signal is less than the reference voltage. When the input signal is greater than the reference voltage, the output is a logic high. This sequence of zeros and ones is referred to as a thermometer code. From the perspective of minimizing the encoding logic to translate this to the proper three bits, it is desirable to have the output represented as a bubble code. A bubble code is a sequence of ones with only one zero in the voltage range where the input signal was in between the reference voltages. This thermometer code can be easily translated to a bubble code if the comparator provides a complement to its output. Without the complement available, larger and slower

Bank of high speed comparators with optimized encoding
Figure 4.4.1

EXOR gates or additional inverters may be necessary. An optimized encoding scheme is achieved by this simple addition to the comparator design and area and overall delay are minimized.

4.4.1 Simulation Results

The bank of high speed comparators with the optimized encoding scheme has been simulated. A resistor divider with eight equally spaced taps establishes the reference voltages to the comparators. The simulation results in Figure 4.4-2 show the resistor ladder spanning between V_{max} (4.0 volts) and AGND (2.5 volts). The input signal changes from 2.6 volts to 3.2 volts and then to 2.7 volts. All eight comparators must compare this changing input level with their respective reference voltage. The large transient spikes on the reference voltages show the current that is being drawn from the resistor divider to charge the sampling capacitors in the comparators. So long as these transients settle before the voltage difference is regeneratively amplified, there is no cause for concern.

The optimized encoding scheme must map the outputs to the correct bit. This is shown in Figure 4.4-3 where only one bit is ever a logical one. This corresponds to the voltage range of the reference voltages that the input signal lies between. The output of this block is fed into the error correction block (see Section 4.8). In the error correction block, the bubble code is mapped to the appropriate three bit code. The actual implementation is an inverse of a true bubble code (ie; all zeroes except for a single one). This was done so NOR gates could be

used within the error correction block, thus further minimizing the area. Depending on whether it is the fine or coarse comparison, these three bits are either clocked into the MSB latches or retained for any error correction that is necessary in the LSB section.

Figure 4.4-2
Simulation Results of Bank of Comparators
Input Signals

Figure 4.4-3
Simulation Results of Bank of Comparators
Output of Encoding Section

4.5 D/A block

After the first 3-bit flash conversion, the 7th, 6th and 5th bits (D6, D5, D4) are known. The sign bit (D7) is also known at this time. The four bits (D7, D6, D5, D4) are used to select the resistor-tap voltage below which the input signal lies. This is the intermediate digital to analog conversion that all two-step flash converters must perform.

The selection process is simply a 16:1 multiplexor comprised of MOS transmission gates. The resistor race track that is used by this D/A block is the same one used for the coarse comparison. By using MOS transmission gates in the multiplexor, there will be no voltage drop across these switches when steady-state is reached. This ensures an accurate digital to analog conversion.

The selected tap voltage is subtracted from the input, leaving a residual voltage (Figure 4.5.1). This $V(\text{residue})$ is used as the input voltage for the next clock cycle. Once $V(\text{residue})$ is known, it is sampled onto the bank of comparators. This residual voltage is never more than 1/16th the full-scale input voltage swing of 3 Vp-p.

In this D/A and subtraction process, there is no amplification. Amplification is one technique used [20] to overcome shortcomings in the comparators such as poor resolution or offset characteristics. However adding gain can introduce other problems such as longer times needed for outputs to slew and settle.

For reasons of fast overall conversion speed, no amplification is used. With no amplification, the output does not slew beyond 1/16th the full-scale input voltage of 3 Vp. This allows for faster settling times. The residual voltage is centered around analog ground which ensures the operational amplifier does not operate with large voltage excursions. Because no amplification is used, the offset characteristics of the operational amplifier used to perform the subtraction are very important. The amplifier used for this application is a high bandwidth BiCMOS design (BW = 180 MHz). The input referred offset is less than 1 mV.

D/A block

Figure 4.5.1

Aside from the offset characteristics of the amplifier, mismatches between any of the resistive elements used in the subtraction will modify the residual voltage. The series resistance from the 16:1 multiplexor must be taken into account. This is done by including

dummy switches in the feedback path and in the path of the input signal. The size and layout of the dummy switches are exactly the same as the transmission gates used in the multiplexor.

4.5.1 Simulation Results

Simulations have been performed to demonstrate how the residual voltage is derived. In Figure 4.5-2, the input signals are initially 2.7 volts and 2.6 volts. The difference is 100 mV, and when centered around AGND the residual voltage is 2.6 volts. In this simulation, the input voltages change to 2.75 volts and 2.70 volts respectively. As soon as these input levels change, the output begins to slew to the new voltage difference. The final residual voltage is 2.55 volts (50 mV + AGND). The simulation results show that the output settles to the final residual voltage in time for it to be sampled for the fine comparison. The residual voltage is also required for the continuous comparators within the SRF block. The output of the D/A block is still slewing when it is being compared within the SRF block. This is permissible because the comparison performed in the SRF is an approximation of the residual voltage. As well, the resolution for the two bits (D4, D3) to be encoded is relatively coarse (4 LSB/SRF-bit). When a comparison is performed in the SRF block, the residual voltage has settled sufficiently. See Section 4.6 for more details.

Figure 4.5-2
Simulation Results of D/A Block

4.6 Sub-Range Finder

For this novel 8-bit architecture, three continuous, non-latching comparators are used to encode two bits (D3 and D2). Before the final 3-bit flash is performed, this intermediate step is executed. This step is used to steer the bank of high speed comparators to the correct resistor tap voltages needed for the fine comparison.

During timeslot 3, the Sub-Range Finder block compares the residual voltage with three voltages that are spaced apart by $1/64$ th the full-scale voltage. These reference voltages (Figure 4.6-1) are derived from three additional resistor taps on the positive MSB resistor race track (See Section 4.7 for more details on the resistor race tracks). The two bits (D3 and D2) that are encoded are used to select the appropriate switches in the Mux Decoder to close. This connects the correct LSB tap voltages to the bank of high speed comparators. A similar optimized encoding scheme is used to translate the three outputs to a 2-bit word.

4.6.1 Continuous Comparator

The continuous comparator used in the SRF block is the same as the one used during timeslot 1 to determine if the signal is a positive or negative value. This comparator is simply an NPN bipolar differential pair with a BiCMOS output stage that drives to CMOS compatible levels (Figure 4.6-2). The tail current for the differential pair is supplied by an NPN bipolar device. The resolution of this comparator

needed in the SRF block is relatively coarse. Each SRF resistor tap is 4 LSB wide apart. The offset voltage of the comparator must be less than half of this amount (ie ≈ 20 mV). This is easily achievable with a bipolar differential pair (See Section 3.2.2 for more details). Both an output and its complement are synthesized. A clocked comparator is not necessary in this application. At the end of timeslot 3, the encoded 2-bit word is clocked into latches. The latched outputs are used in the error correction block.

Figure 4.6-1

Figure 4.6–2
Schematic of Continuous Comparator

4.6.2 Simulation and Layout Results

This continuous comparator has been designed and a layout has been completed (Figure 4.6-3). Simulation results show a delay from the time the input signal crosses the reference voltage to when the output settles to the new logical state of only 4 nS (Figure 4.6-4). This delay is not excessive since the two encoded bits are not clocked into the latches until the end of timeslot 3, which like the other timeslots is 12.5 ns wide. The output voltage swing is not full-rail but these levels are sufficient for the encoding logic that is connected to the comparators. The current consumption is approximately 2 mA.

Figure 4.6-3
Layout of Continuous Comparator

Figure 4.6-4
Simulation Results of Continuous Comparator

4.7 Resistor Race Tracks

Three resistor race tracks are used in this 8 bit A/D converter. All are low resistance polysilicon resistors. Two are the positive and negative MSB resistor ladders used during the coarse 3-bit flash. The resistor ladders are segmented into eight equally valued resistors, each of value $250\ \Omega$. Depending on whether the input signal is positive or negative, one of these ladders is connected to the bank of high speed comparators. The positive MSB ladder has three additional taps between the first segment and AGND. These are used by the SRF block. The negative MSB ladder is connected between AGND and $V_{\min}$ (1 volt reference). The positive ladder is connected between $V_{\max}$ and AGND (4 volt reference). The third resistor ladder is the LSB ladder used for the fine 3-bit flash. This resistor race track contains 18 taps (each one being $115\ \Omega$). It is connected between $V_{\max}(\text{lsb})$ and AGND. Care was taken to minimize resistor mismatching. This was done by laying out one resistor element and repeating it many times to create the complete resistor ladder. As well, by using less than minimum width geometries, sensitivity to resistor mismatches and offsets is diminished.

4.8 Mux Decoder

To save on power and area, the bank of high speed comparators is multiplexed between the coarse and fine comparisons. The trade-off in using this approach is that additional switches are required for the selection process between coarse and fine comparison

(Figure 4.8-1). As well, inherent to this novel architecture, additional switches are necessary because the span of voltages that are selected for the fine comparison overlap each other. This is part of the error correction capability of this architecture (See Section 4.9 for more details). The selection of whether to sample the input signal or the residual voltage is also handled in this block.

For the Mux Decoder block, the basic transmission gate was designed and implemented as a slice, allowing the gates to be butted beside each other. This slice is repeated fifty times. The control logic to select which switches to close is incorporated into the error correction and control logic block.

The transmission gates used are complementary MOS (n channel and p channel) devices. The most critical aspect for this block is the delay introduced by having these switches between the reference voltages and the comparators. A design criteria of less than 5 nS for the output voltage to settle to its final value was chosen. This would still give sufficient time for the voltages to be sampled by the high speed comparators. The analog signals being selected (reference voltages, input signal or residual voltage) are passed through only one level of multiplexing, minimizing any delays to the signals.

Figure 4.8-1

4.8-1 Simulation Results

The largest voltage excursion that the Mux Decoder must switch between is the transition from the positive to negative MSB ladder. The longest settling times would result from this operation and this served as the simulation condition to evaluate the settling characteristics of the Mux Decoder. The load capacitance for each switch is the drain capacitance of all the switches (five) connected to each output node and the sampling capacitors inside the comparator. These were all lumped together and added. Simulations show (Figure 4.8-2) that with this worst case voltage swing and load capacitance, the output settles to its final voltage within 4 nS. All eight reference voltages are switched simultaneously from the positive MSB ladder ($V_{\max} = 4.0\text{V}$ and $V_{\min} = \text{AGND}$) to the negative MSB ladder ($V_{\max} = \text{AGND}$ and $V_{\min} = 1.0\text{V}$).

During the transition, the voltage levels momentarily rise above their initial voltages and then begin to settle to their new values. This is characteristic of the clock feedthrough component that is coupled from the gate to source/drain overlap capacitances of the transmission gates. It is not an issue so long as the final reference voltages settle to their correct value within the the design criteria of 5 nS.

Figure 4.8-2
Simulation Results of Mux Decoder

4.9 Digital Error Correction and Control

This block is the digital controller that sequences all the events in this novel subranging architecture. All timing and control logic is synthesized in this block. Error correction and the latching of the final encoded 8-bit word are also handled with this digital circuitry.

The combinatorial gates, latches and adders used in this design are from a high-speed family of library cells available with this BiCMOS technology. The cells are all MOS devices. Cell layouts and worst case digital models are available for routing and digital simulations.

4.9.1 Clocking strategy

The crucial non-overlapping clocks to this architecture were synthesized internally [21](Figure 4.9-1). The input is a 50/50 duty cycle clock and the outputs are the four timeslot pulses (T1, T2, T3, T4). The non-overlap time between pulses is approximately 2.5 ns, as shown in the simulations (Figure 4.9-2). On the falling edge of T1, the first 4 bits are available for latching. These bits are clocked into latches with an inverted and delayed version T2 (ie. T2D_B). This ensures the bubble code is correct and the proper bits are clocked. After this occurs, the D/A and subtraction process begins during T2. During T3, the residual voltage is compared in the SRF block. On the falling edge of T3 the two encoded bits (D3 and D2) are clocked into latches. These bits are used to select the LSB taps to be connected to the bank of eight comparators.

Non-overlapping clocks

Figure 4.9-1

Horizontal Scale: 10 nS/div

Figure 4.9-1
Simulation Results of Non-Overlapping Clocks

During T4, the final 3-bit flash is performed. On the falling edge of T4, the last three bits are available to be latched. This latching is done with an inverted and delayed version of T1 (ie. T1B_D). During T1, the entire process repeats. As well any error correction is performed in parallel with the sampling of a new signal. This pipelining of events minimizes the conversion time. On the falling edge of T1, the 8-bit word is latched into an output register.

4.9.2 Error Correction

As mentioned in Section 4.3, digital error correction is performed on the bits encoded by the SRF block and the fine comparison. Recall that the eight taps selected for the fine comparison span a voltage range that is wider than the span of a SRF sub-section (Figure 4.9-3). The 2 bits (D3 and D2) encoded by the SRF block can take on four possible codes (00, 01, 10 and 11). These codes may be modified depending on the 3-bit encoded sequence from the second flash conversion. Remembering that the SRF block provided an approximation of the residual voltage, it is possible for the two bits encoded to be incorrect. If they are incorrect, the true voltage range of the residual voltage would be in the SRF sub-section immediately above or below the encoded sub-section. This is the situation when error correction is performed and it is by the fine comparison that determines whether or not to perform any correction.

If the encoded sequence from the second flash is 111 or 110, the residual voltage must lie in the sub-section above the encoded SRF word. In this scenario, the SRF word is modified by adding 01 to the 2-bit word. If the encoded sequence from the second flash is 001 or 000, the residual voltage must lie in the sub-section below the encoded SRF word. In this scenario, the SRF word is modified by subtracting 01 from the 2-bit word. If the encoded sequence from the second flash is none of the above scenarios, error correction is not necessary. This is interpreted as the SRF word is correct. The D1 bit from the second flash is inverted to map this bit to the proper count. The D0 bit remains unchanged. The D3 and D2 bits are the results of the addition or subtraction.

The process of deciding whether or not to perform error correction requires very simple digital control logic and is based on the encoded 3-bit flash. Digital addition or subtraction of 01 from the SRF word are also very simple operations. The digital error correction can only occur after the second 3-bit flash has completed. The three bits from this flash are valid after timeslot 4. The error correction process occurs during timeslot 1 of the next cycle of this analog to digital conversion algorithm.

4.10 Final results

All sections described in the previous sections have been captured in schematics and the layout has been completed for the entire design. Flat transistor-level comparisons between the schematics and the layouts have been established to ensure correspondance of all elements. Simulation models, standard cells and design rules for the BiCMOS technology have been incorporated into the toolset used for this design. All simulations, layout and verification were performed on this one platform.

Post-layout simulations of the extracted layouts have been performed. This back annotation with parasitic capacitive elements ensures the integrity of the layout and design. Post-layout simulations are used to study the effects and mechanisms that are not modelled with sub-circuits created from transistor-level schematics. Some examples of these mechanisms include; interconnect loading that adds delay to all signal tracks, AC coupling mechanisms such as clock feedthrough from parasitic capacitors, and additional loading from adjacent blocks (ie; all gate capacitances or source/drain capacitances from blocks that an output fans out to). Post-layout simulations also ensure the functionality is not compromised by metal tracks that can cross over cells and thus potentially short circuit nodes. Back annotation of parasitic elements and subsequent simulations of the major blocks is a very important process that translates directly into quality and confidence in the entire A/D converter.

This subranging A/D converter contains over 2000 elements (transistors, capacitors and resistors). A simulation of the complete 8-bit subranging A/D converter could not be performed within a reasonable time. The necessary computing resources and the convergence difficulties inherent with such a large transistor-level simulation were the main limiting factors. The major blocks were simulated over process and temperature. This adds further to the confidence in the design presented.

The BiCMOS technology used has triple level metal capability and this has been exploited for the power distribution and for maximum interconnected routing capability. This is reflected in the density that has been achieved in the final layout (Figure 4.10-1). All drawn gate lengths are rectangular to allow for accurate modelling. Only characterized and modelled NPN devices available from the technology library were used. All capacitors used are derived from one basic capacitor unit. All resistor dividers were also assembled from one common resistor element. This ensures proper matching and modelling of the capacitors and resistors.

Care was taken to minimize the interconnect of all crucial analog signals. In the layout, the signal path for the analog lines were treated with the highest priority. This is reflected in the floorplanning of the overall design and in the layout of the Mux Decoder, which is pitch-matched to the bank of high speed comparators.

Figure 4.18-1
B-BR BICMOS Subranging Flash A/D Converter

Separate digital and analog supply lines were used. This minimizes possible coupling of digital noise to the analog blocks through the supply lines. No noisy digital tracks have been placed over the analog blocks. The high speed clock for the comparators is shielded to ground, providing protection for the analog signals that must cross this track. All capacitors have a shield between the bottom plate and the substrate minimizing any substrate noise which might couple into the sampling capacitors in the comparators.

Due to time constraints and limited access to silicon, the entire design could not be submitted for fabrication. However, a preliminary version of the high speed comparator has been fabricated (Figure 4.10-2). The BiCMOS technology that it was fabricated in was an early version of the existing process flow and this design is different from the final implementation. Nevertheless some preliminary measurements have been carried out.

Measurements were performed to establish the functionality of the test circuit. Figure 4.10-3 is a plot of the measured waveforms. The reference signal is at AGND (2.5V) and the input signal is a waveform that crosses this reference threshold. When the clock is high, the input signals are sampled. After the falling edge of the clock, the comparator output follows the input signal. Output signal levels are near the rails. This demonstrates the principles behind the regenerative sense amplifier used in this BiCMOS comparator.

The clock rate for the measurements in Figure 4.10-3 is 20 MHz. Higher clock rates could not be examined because of high frequency oscillations and because of reflections of signals which distorted the input and output signals. These problems are most likely due to inadequate matching of termination and line impedances or from coupling mechanisms between the unshielded clock and signal lines. To perform full speed testing, a test jig providing proper shielding and termination would be required. As well, high speed test equipment suitable for the input and output levels of this comparator are necessary. These items were not available at the time when measurements were being performed.

Only low speed testing of this early version of the comparator has been performed. Preliminary measurements revealed that the common-mode input range of this comparator was only 2.3 volts. This is insufficient for the design target of encoding a 3 V_{p-p} signal with 8-bits resolution. Further analysis through simulations revealed that with signals near the desired V_{min} (1V), the output of the regenerative sense amplifier fell outside of the input range of the latch stage.

Upon discovery of this shortcoming, the comparator was redesigned by centering the input range of the latch stage around the output levels of the regenerative sense amplifier. This was accomplished by changing the values of the load resistors (R1 and R2) in the latch. The final version of the high-speed comparator has been resubmitted for

fabrication. However, processing has not been completed so devices are not available for characterization.

Because of the design error and because the BiCMOS process that it was fabricated in has changed, no further characterization was performed on this early version of the comparator. As well, a lack of proper high speed test equipment made full speed testing impossible.

Figure 4.10-2
Photomicrograph of High Speed BiCMOS Comparator

Vertical Scale 5 volts/div

Horizontal Scale 20 nS/div

Figure 4.10-3
Measured Results of BiCMOS Comparator

The expected performance of the complete subranging A/D converter was obtained from simulations, including the use of back annotated information from the full layout. The following is a summary of the expected specifications:

Area	0.810 by 1.020 mm
Resolution	8 bits
Current consumption	20 mA
Supply Voltage	5 volts
Operating Speed	40 MHz
Conversion Time	50 nS
Input Range	1 to 4 volts (AGND = 2.5V)
Power	100 mW

These specifications can now be compared to published literature. Table 4.10-1 is a summary of the performance of some published high speed A/D converters. These examples represent state of the art converters with operating speeds of less than 50 MHz and with resolutions of less than 10 bits. Higher speed and resolution converters have been published but these typically operate with higher voltages and consume tremendous amounts of power. For these reasons, these converters have been omitted from this comparison.

	Area	Resolution	Power	Voltage	Conversion	Technology	Number of
	[mm ²]	[bits]	[mW]	Supply	Speed		Comparators
				[volts]	[MHz]		
1) Sugimoto et.al.[22]	26	8	500	5	10	3µm BiCMOS	64
2) Tsugaru et. al. [19]	19.68	10	700	5	40	0.8 µm BiCMOS	64
3) Kumamoto et. al.[23]	7.88	8	180	5	30	1.5µm CMOS	256
4) Shimizu et. al.[20]	25	10	900	10	20	3µm Bipolar	128
5) Fukushima et.al[24]	2.10	8	105	5	40	1.4 µm CMOS	57
6) Ishikawa et. al.[25]	13.76	8	600	5	50	1µm CMOS	48
7) Tsuji et. al. [17]	2.88	8	50	5	20	0.8µm CMOS	32
8) Matsuura et. al. [26]	7.56	8	200	5	20	2 µm CMOS	32
9) Seto	1.8	8	100	5	40	0.8µm BiCMOS	12

In terms of area, the BiCMOS subranging A/D converter of this thesis is the smallest. It uses the fewest number of comparators to achieve a comparable level of resolution. The density achieved is a reflection of the technology, the architecture and the floorplanning. The final layout is more than six times smaller than some of the published results [19,25].

The power consumption of this A/D converter is also one of the lowest. This is due to the low power comparator presented in Section 4.2 and in the number of comparators necessary for this novel architecture. The power requirements are as much as five times lower than some of the published results [22,25].

The novel architecture presented in this chapter uses the fewest number of comparators. This is significant in terms of the buffer or sample and hold circuitry that is in front of every A/D converter. With so few comparators, the total capacitive or resistive load presented to the buffer is the lowest of all the architectures summarized. In the extreme case of a full-flash converter [23], the sample and hold block must buffer the analog signal to 256 comparators. With this architecture, the design constraints on the sample and hold block are less demanding.

Because of the small area and low power, this subranging A/D converter can be used as an analog macro within a larger mixed analog/digital monolithic integrated circuit. The high resolution and

speed of this design permits it to be used in many areas such as video or high bandwidth telecommunications applications.

When all these factors such as low comparator count, small area, low power consumption, high speed and accuracy are taken into account, the overall advantage of this design are very obvious. Other designs may offer better performance in one or two areas, but none offer the balance of this design.

4.11 Conclusions

The central topic of this thesis has been dealt with in this chapter. The research and study described in previous chapters has been applied to the design of a novel subranging A/D converter in a high performance BiCMOS technology.

A detailed design study of the BiCMOS high-speed comparator has been discussed. Simulation results have demonstrated the operation of this design with clock rates of greater than 100 MHz. The novel 8-bit subranging architecture has been described in detail. The entire A/D converter has been designed and laid out. Detailed simulations of all the key blocks have been performed and shown to function as necessary.

Preliminary measurements were performed on an early version of the BiCMOS comparator. These measurements demonstrate the principles behind the regenerative sense amplifier used in the

comparator. From these test measurements, a design error was uncovered. The common-mode input range was insufficient for the design goal. This shortcoming has been corrected in the final design.

A comparison with published state of the art A/D converters has shown an area improvement by as much as a factor of six times with the subranging A/D converter presented in this chapter. As well, with the low power comparator and the novel architecture, a reduction in power by as much as five times was achieved over other designs with comparable operating speeds and resolution. The overall balance of this design is superior to the other designs.

Chapter 5

Conclusions

5.1 Summary

An objective of this thesis has been to study a class of high speed analog to digital converter and to explore the advantages to be gained in the design of such a converter in a new technology. The emergence of BiCMOS as a viable technology and the demand for high speed A/D converters has served as the motivation for this work. The fulfillment of this objective requires investigation into many different topics.

An introduction and the motivation for this thesis was presented in Chapter One. In Chapter Two, architectural alternatives for high performance A/D converters were investigated. The operation of successive approximation register A/D converters was presented. Full flash A/D converters were also reviewed, and the principles behind the family of subranging flash A/D converters were discussed in detail. Presenting the advantages and disadvantages of each architecture was a central part of this chapter. This served to provide the reader with an understanding of the alternatives that are available for high speed analog to digital conversion.

The design considerations for a subranging flash A/D converter were presented in Chapter 3. A review of the design alternatives from the perspective of the technology selection was investigated. The trade-

offs between CMOS and bipolar processes were discussed. This led to the discussion of the BiCMOS technology that was used in this design study. Next, the key circuit component in a subranging A/D converter, the comparator, was investigated. The crucial delay limiting factors in a classical bipolar comparator were studied. This led to an understanding of which areas in a comparator design could be improved upon.

A major objective of this thesis has been to design a high speed BiCMOS comparator and to apply it to a novel subranging architecture. This detailed design study has been presented in Chapter Four. The BiCMOS comparator was analyzed and studied in detail, and simulation and layout results were presented. A novel BiCMOS subranging flash A/D converter that uses this comparator was then presented. Detailed simulations were performed on all the crucial blocks, and preliminary measurements of an early version of the comparator were presented. This demonstrated the principles behind the BiCMOS regenerative sense amplifier. Final layout results of the entire A/D converter were presented. With a complete layout, a comparison was drawn with other state of the art high speed A/D converters. An area improvement by as much as a factor of six times was shown, and a reduction in power by a factor of five times was achieved over other A/D converters with similar speed and resolution. The overall balance of this design was shown to be superior to all others in the comparison.

Due to time constraints and limited access to silicon, the novel architecture presented in Chapter Four could not be fabricated. However, by carrying the A/D converter through completely to the layout stage, in a new BiCMOS technology, a high level of confidence has been established in the comparisons drawn and in the validity of this design.

5.2 Recommendations for Future Work

The most obvious recommendation is that the subranging flash A/D converter designed in this thesis should be fabricated and tested. The processing and further development costs involved would have to be justified by the need for such an A/D converter in a application context. An 8 bit, 40 MHz A/D converter with low power and chip area could be a key component, for example, as part of a monolithic low power digital radio receiver. An architecture for such a monolithic digital radio could well be conceived which did its conversion at this sampling rate and bit accuracy, and no such component presently exists.

In the application example mentioned, and in other applications such as digital video transmission, the requirement for higher performance and lower power and area will continue. Higher resolution and lower operating voltage are design constraints that will apply pressure to the existing architectures and technologies. The emergence of full complementary bipolar devices in a BiCMOS technology can create

new opportunities for higher speed comparator designs. This is another area where further work would be warranted.

Throughout this thesis, there has been little mention of how the non-idealities of the circuit components affect the overall performance of the design. This is because it is very difficult to study these phenomena with existing simulators, given the circuit complexity and the time domain nature of A/D converters. Modelling these non-ideal behaviours in the context of a complete design is an area that has seen very little attention because of present computer and software limitations. Study of the causes of non-linearities, distortion, and conversion errors is either impossible or computationally prohibitive with present transistor-level simulators. Research and development into techniques and simulators that can handle these problems is another area that can be investigated.

Appendix 1

The following is the S domain solution for the characteristic equation of the differential output voltage ($V_{o2}-V_{o1}$) during the regeneration phase ϕ_2 :

Linearized model of a classical bipolar regenerative sense amplifier

Convention: current flowing into a node is positive

Currents at node V_{o1}

$$i_1 + i_5 = g_m V_{i2} + i_3 + i_4 \quad (1)$$

Currents at node V_{i1}

$$0 = i_5 + i_2 + i_6 + i_7 \quad (2)$$

Currents at node V_{o2} :

$$i_7 = g_m V_{i1} + i_8 + i_9 + i_{10} \quad (3)$$

Currents at node V_{i2} :

$$i_{10} = i_{11} + i_{12} + i_1 \quad (4)$$

Current equations:

$$i_1 = (V_{i2} - V_{o1})sC_\mu$$

$$i_2 = \left(\frac{V_{i1}}{r_\pi} \right)$$

$$i_3 = (V_{o1})sC_L$$

$$i_4 = \left(\frac{V_{o1}}{R_L} \right)$$

$$i_5 = \left(\frac{V_{i1} - V_{o1}}{r_b} \right)$$

$$i_6 = (V_{i1})sC_\pi$$

$$i_7 = (V_{i1} - V_{o2})sC_\mu$$

$$i_8 = (V_{o2})sC_L$$

$$i_9 = \left(\frac{V_{o2}}{R_L} \right)$$

$$i_{10} = \left(\frac{V_{o2} - V_{i2}}{r_b} \right)$$

$$i_{11} = \left(\frac{V_{i2}}{r_\pi} \right)$$

$$i_{12} = (V_{i2})sC_\pi$$

from equation {1}, solve for V_{o1} :

$$(V_{i2} - V_{o1})sC_\mu + \left(\frac{V_{i1} - V_{o1}}{r_b} \right) = g_m V_{i2} + (V_{o1})sC_L + \left(\frac{V_{o1}}{R_L} \right)$$

$$V_{o1} = \frac{(V_{i2}(s r_b C_\mu - g_m r_b) + V_{i1})}{\left(1 + \frac{r_b}{R_L} + s r_b C_\mu + s r_b C_L \right)} \quad \{5\}$$

from equation {2}, solve for V_{i1} :

$$0 = \left(\frac{V_{i1} - V_{o1}}{r_b} \right) + \left(\frac{V_{i1}}{r_\pi} \right) + (V_{i1})sC_\pi + (V_{i1} - V_{o2})sC_\mu$$

$$V_{i1} = \frac{(V_{o2}(s r_b C_\mu) + V_{o1})}{\left(1 + \frac{r_b}{r_\pi} + s r_b C_\pi + s r_b C_\mu \right)} \quad \{6\}$$

from equation {3}, solve for V_{o2} :

$$(V_{i1} - V_{o2})sC_{\mu} = g_m V_{i1} + (V_{o2})sC_L + \left(\frac{V_{o2}}{R_L}\right) + \left(\frac{V_{o2} - V_{i2}}{r_b}\right)$$

$$V_{o2} = \frac{(V_{i1}(s r_b C_{\mu} - g_m r_b) + V_{i2})}{\left(1 + \frac{r_b}{R_L} + s r_b C_{\mu} + s r_b C_L\right)} \quad \{7\}$$

from equation {4}, solve for V_{i2} :

$$\left(\frac{V_{o2} - V_{i2}}{r_b}\right) = \left(\frac{V_{i2}}{r_{\pi}}\right) + (V_{i2})sC_{\pi} + (V_{i2} - V_{o1})sC_{\mu}$$

$$V_{i2} = \frac{(V_{o1}(s r_b C_{\mu}) + V_{o2})}{\left(1 + \frac{r_b}{r_{\pi}} + s r_b C_{\pi} + s r_b C_{\mu}\right)} \quad \{8\}$$

Subtract equation {5} from {7} and solve for $(V_{o2} - V_{o1})$:

$$V_{o2} - V_{o1} = \frac{(V_{i2} - V_{i1}) * (1 + g_m r_b - s r_b C_{\mu})}{\left(1 + \frac{r_b}{R_L} + s r_b C_{\mu} + s r_b C_L\right)} \quad \{9\}$$

Subtract equation {6} from {8} and solve for $(V_{i2} - V_{i1})$:

$$V_{i2} - V_{i1} = \frac{(V_{o2} - V_{o1}) * (1 - s r_b C_{\mu})}{\left(1 + \frac{r_b}{r_{\pi}} + s r_b C_{\pi} + s r_b C_{\mu}\right)} \quad \{10\}$$

Substitute $(V_{i2} - V_{i1})$ from equation {10} into {9}

$$V_{o2} - V_{o1} = \frac{(V_{o2} - V_{o1}) * (1 + g_m r_b - s r_b C_{\mu})(1 - s r_b C_{\mu})}{\left(1 + \frac{r_b}{r_{\pi}} + s r_b C_{\pi} + s r_b C_{\mu}\right)\left(1 + \frac{r_b}{R_L} + s r_b C_{\mu} + s r_b C_L\right)}$$

$$V_{o2} - V_{o1} = \frac{(V_{o2} - V_{o1}) * N}{D} \quad \{11\}$$

$$\text{where } N = \left(\frac{1}{r_b} + g_m - sC_\mu(2 + g_m r_b) + s^2 r_b (C_\mu)^2 \right)$$

$$D = \left(\left(\frac{1}{r_b} + \frac{1}{r_\pi} + \frac{1}{R_L} + \frac{r_b}{r_\pi R_L} \right) + \right. \\ \left. s \left(C_\pi \left(1 + \frac{r_b}{R_L} \right) + C_\mu \left(2 + \frac{r_b}{R_L} + \frac{r_b}{r_\pi} \right) + C_L \left(1 + \frac{r_b}{r_\pi} \right) \right) + \right. \\ \left. s^2 r_b (C_\pi C_\mu + C_\pi C_L + C_L C_\mu + C_\mu^2) \right)$$

The characteristic equation is determined by setting {11} to zero:

$$(V_{o2} - V_{o1}) * D = (V_{o2} - V_{o1}) * N$$

$$0 = (V_{o2} - V_{o1}) * (D - N)$$

$$0 = s^2 r_b (C_\pi C_\mu + C_\pi C_L + C_L C_\mu) + \\ s \left(C_\pi \left(1 + \frac{r_b}{R_L} \right) + C_\mu \left(4 + \frac{r_b}{R_L} + \frac{r_b}{r_\pi} - g_m r_b \right) + C_L \left(1 + \frac{r_b}{r_\pi} \right) \right) \\ - \left(g_m - \frac{1}{r_\pi} - \frac{1}{R_L} - \frac{r_b}{r_\pi R_L} \right)$$

typically $r_b \ll r_\pi$

$$0 = s^2 r_b (C_\pi C_\mu + C_\pi C_L + C_L C_\mu) + \\ s \left(C_\pi \left(1 + \frac{r_b}{R_L} \right) + C_\mu \left(4 + \frac{r_b}{R_L} - g_m r_b \right) + C_L \right) \\ - \left(g_m - \frac{1}{R_L} \right) \quad \{12\}$$

Given the general 2nd order equation of:

$$As^2 + Bs + C = 0$$

Assuming the constant A is very small, this equation can be approximated as a simple first order system of the form:

$$Bs + C = 0$$

$$s + \frac{C}{B} = 0$$

The solution to this first order system is:

$$y(t) = K \exp(-t/T) \quad \text{where:} \quad \begin{array}{l} T = B/C \\ K = \text{constant} \end{array}$$

substituting the variables from (12) into the above will give:

$$(V_{o2} - V_{o1}) = A_L * (V_{i2} - V_{i1}) * (\exp(t/T_{\text{reg}}))$$

where: $A_L = \text{ampifier gain}$

$$T_{\text{reg}} \approx \frac{(C_{\pi}(1 + \frac{r_b}{R_L}) + C_{\mu}(4 + \frac{r_b}{R_L} - g_m r_b) + C_L)}{(g_m \frac{1}{R_L})}$$

$$T_{\text{reg}} \approx \frac{(C_{\pi}(r_b + R_L) + C_{\mu}(4R_L + r_b(1 + R_L g_m)) + C_L R_L)}{(g_m R_L - 1)}$$

When $R_L \gg r_b$, the regeneration time constant simplifies to:

$$T_{\text{reg}} \approx \left(\frac{C_{\text{total}}}{g_m} \right) * \left(\frac{g_m R_L}{g_m R_L - 1} \right)$$

where: $C_{\text{total}} = C_{\pi} + C_L + 4C_{\mu}$

Appendix 2

The following is the S domain solution for the characteristic equation of the differential output voltage ($V_{o2}-V_{o1}$) during the sample phase ϕ_1 :

$$I_{C1} = \frac{\alpha I_{EE}}{(1 + \exp(\frac{-qV_{in}}{kT}))} \quad (1)$$

$$I_{C2} = \frac{\alpha I_{EE}}{(1 + \exp(\frac{qV_{in}}{kT}))} \quad (2)$$

Given:

$$V_{o1} = V_{cc} - \alpha R_L I_{EE} - (I_{C1} R_L - \alpha R_L I_{EE}) * [1 - \exp(\frac{-t}{R_L C})] \quad (3)$$

and

$$V_{o2} = V_{cc} - (I_{C2} R_L) * [1 - \exp(\frac{-t}{R_L C})] \quad (4)$$

substitute (1) and (2) into (3) and (4) respectively:

$$V_{o1} = V_{cc} -$$

$$\frac{[\alpha I_{EE} R_L - \alpha R_L I_{EE} * \exp(\frac{-t}{R_L C}) - \alpha I_{EE} R_L * ((1 + \exp(\frac{-qV_{in}}{kT})) * (\exp(\frac{-t}{R_L C})))]}{[1 + \exp(\frac{qV_{in}}{kT})]}$$

(5)

$$V_{o2} = V_{cc} - \frac{\alpha I_{EE} R_L [1 - \exp(\frac{-t}{RLC})]}{1 + \exp(\frac{qV_{in}}{kT})} \quad (6)$$

When $V_{o2} = V_{o1}$:

equate {5} and {6}

$$\frac{[1 - \exp(\frac{-t}{RLC})]}{1 + \exp(\frac{qV_{in}}{kT})} = \frac{[1 + \exp(\frac{-qV}{kT}) * \exp(\frac{-t}{RLC})]}{1 + \exp(\frac{-qV_{in}}{kT})}$$

$$0 = 2\exp(\frac{-t}{RLC}) + \exp(\frac{2qV}{kT}) - 1 + 2\exp(\frac{-t}{RLC})\exp(\frac{qV}{kT})$$

$$2\exp(\frac{-t}{RLC}) = 1 - \exp(\frac{2qV}{kT}) + 2\exp(\frac{-t}{RLC})\exp(\frac{qV}{kT})$$

$$\exp(\frac{-t}{RLC}) = \frac{1}{2} * [1 - \frac{\exp(\frac{-qV}{2kT})}{\exp(\frac{qV}{2kT})}]$$

$$\exp(\frac{-t}{RLC}) = \frac{1}{2} * [1 - (\exp(\frac{-qV}{kT}))]$$

$$\frac{-t}{RLC} = \ln [\frac{1}{2} (1 - \exp(\frac{-qV}{kT}))]$$

if $V = 3 \text{ mV}$, at Room Temperature

$$t_{\text{recovery}} = 2.87R_L C$$

Appendix 3

The following is the S domain solution for the characteristic equation of the differential output voltage ($V_{o2}-V_{o1}$):

Linearized model of regenerative sense amplifier

Convention: current flowing into a node is positive

Currents at node V_{o2}

$$i_1 = i_2 + g_m V_{i2} + i_4 \quad (1)$$

Currents at node V_{o1}

$$i_5 = g_m V_{i1} + i_7 + i_8 \quad (2)$$

Currents at node V_{i1} :

$$i_8 = i_1 + i_9 + i_{11} \quad (3)$$

Currents at node V_{i2} :

$$i_4 = i_{14} + i_{13} + i_{12} + i_5 \quad (4)$$

Current equations:

Assume $r_b = 0$

$$i_1 = (V_{i1} - V_{o2})sC_3$$

$$i_2 = (V_{o2})sC_L$$

$$i_3 = g_m V_{i2}$$

$$i_4 = (V_{o1} - V_{i1})sC_\mu$$

$$i_5 = (V_{i2} - V_{o1})sC_4$$

$$i_6 = g_m V_{i1}$$

$$i_7 = (V_{o2})sC_L$$

$$i_8 = (V_{o1} - V_{i1})sC_\mu$$

$$i_9 = (V_{i1})sC_1$$

$$i_{10} = (V_{i1})/r_\pi$$

$$i_{11} = (V_{i1})sC_\pi$$

$$i_{12} = (V_{i2})sC_2$$

$$i_{13} = (V_{i2})/r_\pi$$

$$i_{14} = (V_{i2})sC_\pi$$

from equation (1), solve for V_{o2} :

$$(V_{o2})(sC_3 + sC_L + sC_\mu) = (V_{i1})sC_3 - g_m V_{i2} + (V_{i2})sC_\mu$$

$$V_{o2} = \frac{(V_{i1}sC_3 + (-g_m + sC_\mu)V_{i2})}{s(C_3 + C_L + C_\mu)} \quad [5]$$

from equation (2), solve for V_{o1} :

$$(V_{i2})sC_4 - g_m V_{i1} + V_{i1}sC_\mu = V_{o1} (sC_4 + sC + sC_\mu)$$

$$V_{o1} = \frac{(V_{i2}sC_4 + (sC_\mu - g_m)V_{i1})}{s(C_4 + C_L + C_\mu)} \quad [6]$$

from equation {3}, solve for V_{i1} :

$$(V_{o1})sC_{\mu} + (V_{o2})sC_3 = V_{i1}(sC_{\mu} + sC_3 + sC_1 + sC_{\pi} + 1/r_{\pi})$$

$$V_{i1} = \frac{s(V_{o1}C_{\mu} + V_{o2}C_3)}{(s(C_{\mu} + C_3 + C_1 + C_{\pi}) + 1/r_{\pi})} \quad \{7\}$$

from equation {4}, solve for V_{i2} :

$$(V_{o2}sC_{\mu} + V_{o1}sC_4) = V_{i2}(sC_{\mu} + sC_4 + sC_2 + sC_{\pi} + 1/r_{\pi})$$

$$V_{i2} = \frac{s(V_{o2}C_{\mu} + V_{o1}C_4)}{(s(C_{\mu} + C_4 + C_2 + C_{\pi}) + 1/r_{\pi})} \quad \{8\}$$

Subtract equation {5} from {6} and solve for $(V_{o2} - V_{o1})$:

$$V_{o2} - V_{o1} = \frac{(V_{i2} - V_{i1})(sC_{\mu} - s(C_3 - g_m))}{s(C_3 + C_L + C_{\mu})} \quad \{9\}$$

Subtract equation {7} from {8} and solve for $(V_{i2} - V_{i1})$:

recall $C_3 = C_4$ and $C_1 = C_2$

$$V_{i2} - V_{i1} = \frac{(V_{o2} - V_{o1})(sC_{\mu} - sC_3)}{(s(C_{\mu} + C_3 + C_1 + C_{\pi}) + 1/r_{\pi})} \quad \{10\}$$

Substitute $(V_{i2} - V_{i1})$ from equation {10} into {9}

$$V_{o2} - V_{o1} = \frac{(s(C_{\mu} - C_3)s(C_{\mu} - C_3 - g_m/s))}{(s(C_{\mu} + C_3 + C_1 + C_{\pi} + 1/r_{\pi})s(C_3 + C_L + C_{\mu}))}$$

$$V_{o2} - V_{o1} = \frac{(V_{o2} - V_{o1}) * N}{D} \quad \{11\}$$

where $N = (C_{\mu} - C_3)(C_{\mu} - C_3 - g_m/s)$

$$D = ((C_{\mu} + C_3 + C_1 + C_{\pi} + 1/r_{\pi}s)(C_3 + C_L + C_{\mu}))$$

The characteristic equation is determined by setting [11] to zero:

$$(V_{o2} - V_{o1}) * D = (V_{o2} - V_{o1}) * N$$

$$0 = (V_{o2} - V_{o1}) * (D - N)$$

$$0 = s[(C_{\mu} + C_3 + C_1 + C_{\pi})(C_3 + C_L + C_{\pi}) - (C_3 - C_{\pi})^2] - \dots$$

$$g_m(C_3 - C_{\mu}) + (C_3 + C_L + C_{\mu})/r_{\pi}$$

Given the general 1st order equation of:

$$Bs + C = 0$$

Assuming the constant A is very small, this equation can be approximated as a simple first order system of the form:

$$Bs + C = 0$$

$$s + \frac{C}{B} = 0$$

The solution to this first order system is:

$$y(t) = K \exp(-t/T) \quad \text{where:} \quad \begin{array}{l} T = B/C \\ K = \text{constant} \end{array}$$

substituting the variables from [12] into the above will give:

$$(V_{o2} - V_{o1}) = A_L * (V_{i2} - V_{i1}) * (\exp(t/T_{reg}))$$

where: $A_L = \text{ampifier gain}$

$$T_{reg} \approx \frac{[(C_{\mu} + C_3 + C_1 + C_{\pi})(C_3 + C_L + C_{\pi}) - (C_3 - C_{\pi})^2]}{g_m(C_3 - C_{\mu}) - (C_3 + C_L + C_{\mu})/r_{\pi}}$$

Typically r_{π} is very large and a further approximation can be made by ignoring the second term in the denominator. As well, if C_{μ} is ignored, then the regeneration time constant simplifies to:

$$T_{reg} \approx \frac{[C_1 + C_{\pi} + C_L + C_L(C_1 + C_{\pi})/C_3]}{g_m}$$

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