A High Frequency Receive Equalizer

By

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Abstract

In this thesis the design of high frequency linear equalizers are considered. Various architectures are reviewed and a design for a 10 Gbps equalizer based on an active delay cell is proposed.

The delay cell is implemented using a modified Cherry Hooper architecture that utilizes active negative feedback to obtain an adjustable bandwidth from 9GHz to 15GHz with a nominal bandwidth of 12.4GHz. By avoiding the use of broadbanding techniques, such as peaking inductors, silicon area is greatly reduced. The optimized delay cell occupies an area of $93\mu\text{m}$ by $42\mu\text{m}$, has a measured gain of 0.3 dB, and is critically damped to limit peaking to 0dB.

The multiplier is a low power 1.2V CMOS design. The multiplier can be digitally controlled without the use of a digital to analog converter and has 32 possible gain settings from -1 to +1. To achieve negative gain an inverting switch is used at the input of the multiplier, reducing loading at the summing node by 50%. As the bandwidth bottleneck occurs at the summing node, this allows for higher frequency operation or an increase in the number of multipliers per summing node. The measured gain errors are less than 2%, linearity errors are less than 3%, and the power consumption is 1.5mW.

Finally, the delay cell and multiplier are combined to form an eight tap feed forward equalizer. A broadbanding inductor is designed and added at the summing node to increase the bandwidth of the equalizer. Simulation with equalization show a 48% and 28% improvement in horizontal and vertical jitter respectively compared to simulations without equalization.

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Abbreviations

BJT	Bipolar Junction Transistors
CML	Current Mode Logic
DAC	Digital Analog Converter
DSP	Digital Signal Processing
FFE	Feed Forward Equalizer
FIR	Finite Impulse Response
Gbps	Giga Bit Per Second
ISI	Inter-symbol Interference
LMS	Least Mean Square
MDAC	Multiplying Digital to Analog Converter
MIM	Metal Insulator Metal
MMF	Multi-Mode Fiber
MMIC	Monolithic Microwave Integrated Circuit
PCB	Printed Circuit Board
RFIC	Radio Frequency Integrated Circuits
SRF	Self Resonant Frequency

Chapter 1 Introduction

1.1 Motivation for this Work

To accommodate the increasing data rate that is present in today's technology, the engineering community is continuously challenged with addressing new and changing issues associated with high frequency data transmission. One particular issue of importance is overcoming the increasingly detrimental effects of the transmission medium as data rates increase.

At low frequency, the connecting medium often has negligible effect on the transmission of data. This medium may simply be a connecting copper wire or a copper trace on a printed circuit board (PCB). As technology advances, data rates increase, and the medium of transmission evolves. Today's mediums encompass a wide variety of materials including, but not limited to, air, fiber, and copper. Each medium has its own distinct properties with notable advantages and disadvantages. However, all exhibit increased distortion as data rates increase. The solutions designed to address distortion are as varied as the problem itself. However, one notable solution is equalization.

Equalization can be implemented in a variety of ways, but all solutions must remove distortion from the transmitted/received signal introduced by the medium of transmission. The principal motivation for this research is to examine a specific type of receive equalization known as continuous time equalization which is implemented using a finite impulse response (FIR) filter.

1.2 Contributions

This work contributes to the knowledge of equalizer design by providing insight into the design of building blocks required for an equalizer implementation. Specifically, in this work new architectures are proposed for the multiplier and active delay cell. Specifica-

tions are defined and two circuits were designed and fabricated. Based on these results, it has been shown through this work that 10 Gbps equalization can be achieved through the use of building blocks based on active transistors. This provides an alternative architecture to the area intensive LC architecture.

Results of this research have been published in three conference papers [11], [12] and [13].

1.3 Thesis Overview

This thesis is organized as follows. First a review of equalizers and distortion is presented in Chapter 2. This review involves a discussion of the impulse response of a medium and how it is related to selecting an appropriate equalizer architecture. A literature review of existing passive and active architectures for receive equalizers is presented in Chapter 3. In Chapter 4 an LC equalizer, based on an architecture presented in Chapter 3 is explored further and a design, with proposed enhancements is presented and simulated. In Chapter 5 new architectures are proposed for the design of an active delay cell and multiplier that are the building blocks for an equalization filter. The delay cell and multiplier were fabricated and lab results are presented in Chapter 6. Chapter 7 focuses on simulations of a complete equalizer based on the components proposed in Chapter 5. Finally, conclusions are presented in Chapter 8.

Chapter 2 Background

2.1 Inter-Symbol Interference

As signals are transmitted through a medium, such as air or copper, different frequencies tend to propagate at different speeds due to the frequency response of the medium. This results in amplitude and phase variations between the transmitted and received signal, which leads to inter-symbol interference (ISI). ISI has the effect of impeding the receiving circuitry's ability to distinguish between a one or a zero and can result in data errors. This effect is illustrated in Figure 1.

Figure 1. Illustration of inter-symbol interference (ISI).

The input in Figure 1 is a square wave bit stream. The transmission medium introduces distortion and effectively lowpass filters the input signal. The resulting output signal, although clearly lowpass filtered, is correctly interpreted for the first four bits based on the receive reference level. However, after a string of three ones, the output cannot drop below the reference level in time to register a zero with the receive circuitry. As a result, the receive circuit will incorrectly interpret this data as a one. This effect is most prominent in fiber applications where there is a potential for long strings of ones or zeros. In

other forms of communication, such as chip-to-chip communication, data encoding such as 8b/10b encoding, is used to reduce this effect. 8b/10b encoding effectively DC balances the data string so that in a group of ten bits there is roughly an equal number of ones and zeros.

To reduce the effect of ISI an equalizer can be used at the transmitting or receiving end to control the overall pulse shape of the received data [1]. This re-shaping of the data reduces the transmission effect of the medium, which in turn reduces the ISI allowing an increase in data rates or the physical distance of transmission. As an example, equalizers can increase the data rate in chip-to-chip communication by compensating for the high frequency loss of the connecting copper traces between chips. This work focuses specifically on receive equalizers.

2.2 Categories of Receive Equalizers

There are generally four categories of receive equalizers for data rates over 1 Gbps: passive-component equalizers, active continuous-time equalizers using split-path amplifiers, active equalizers using discrete-time FIR filters and active equalizers using continuous-time FIR filters[2]. This work focuses on the design of continuous-time FIR filters as shown in Figure 2. When used in equalization, such a filter is often referred to as a feed-forward equalizer (FFE).

Figure 2. N-tap FIR filter.

Figure 2 represents an N tap FIR transversal filter where the required number of stages, N, depends of the characteristics of the transmission medium. A medium that introduces large amounts of distortion will require a large number of taps to recover the transmitted signal by reducing the ISI. However, in practice the number of taps is limited due to the increased capacitive load at the summing node. In addition, as extra delay cells are added there is a reduction of bandwidth as the poles of the delay cells are cascaded. As the bandwidth falls below the data rate, the equalizer's lowpass frequency response will effectively add to the lowpass filtering of the channel and the received signal will deteriorate even further. Hence, there is a limit to the feasible number of taps. For effective removal of ISI, the impulse response of the channel must be studied and the architecture of the equalizer selected on the basis of the response. This point is discussed further in the following sections.

2.3 Impulse Response

Every channel, regardless of the medium of transmission, has a specific impulse response the characteristics of which are often quite different. It is possible to categorize the impulse response into different sections: the main symbol, pre-cursor and post-cursor distur-

tion. The main symbol is the point of maximum power and indicates the transmitted data. Pre-cursor distortion is distortion that occurs before the main symbol and post-cursor distortion is distortion that occurs after the main symbol. This is illustrated in Figure 3.

Figure 3. Example impulse response.

As previously stated, every channel exhibits different distortion. For example a back-plane medium is often dominated by post-cursor distortion and the pre-cursor distortion is usually negligible. However, a multi-mode fiber (MMF) commonly exhibits strong elements of both pre-cursor and post-cursor distortion. As a result of these differences, the optimal receive architecture for each situation varies. These architectures are explored further in the next section.

2.4 Feed Forward and Decision Feedback Equalization

The filter shown in Figure 2 is commonly referred to as a feed forward equalizer (FFE). Often, to accommodate vastly different impulse responses of the channel, equalizers are created using more than just the FFE. Such an equalizer is illustrated in Figure 4.

Figure 4. A feed forward and decision feedback equalizer.

The equalizer in Figure 4 is composed of two sections: the previously discussed FFE and a decision feedback equalizer (DFE). The weights of the multiplier ($C_0, C_1, \dots, C_{N_{FFE}}$ and $C_{10}, C_{11}, \dots, C_{N_{DFE}}$) are variable resulting in many possible configurations.

The FFE is most effective at removing the ISI arising from pre-cursor distortion, and the DFE is most effective at removing the ISI created by post-cursor distortion. Therefore, an optimal architecture for a MMF would consist of both a FFE and a DFE to deal with the strong effects of both pre and post cursor distortion. An equalizer design strictly for backplane equalization where the distortion is mainly post-cursor may only consist of a DFE.

2.5 Adaptive Equalization

Even mediums of the same material and the same physical dimensions often have different impulse responses. For example, two backplane traces of the same length may be routed differently, thus experiencing a different capacitive loading. As a result they may exhibit different impulse responses. Thus, a single configuration of tap delays and weights is not optimal for all situations. In response to variations such as these, algorithms have been developed that dynamically reconfigure the transversal filter by varying the multiplier tap weights in response to a changing environment. Such filters are referred to as adaptive equalizers.

A common algorithm for an adaptive equalizer is the Least Mean Square (LMS) Algorithm. This is an iterative approach to minimize the error in the received signal by reconfiguring the filter. Successive adjustments to the tap weights reduce the error based on a step size μ . Large values of μ lead to a fast convergence of the algorithm, while smaller values of μ lead to slower but more accurate convergence[1]. As expected, this is a trade off that depends on the specifications of the design.

The LMS algorithm can be operated with a training sequence where a received training signal is compared to a known bit stream and the weights are adjusted accordingly. Alternatively, the LMS algorithm can be used for blind equalization for which a training sequence is not required and decisions are made on the bases of assumed correct past decisions.

Chapter 3 Literature Review

This section is intended to review recent developments in continuous time equalizer design. After an extensive search of IEEE publications it was determined that there are very few publications in this area. As a result, the literature review is restricted to three papers that were published between February of 2000 and March of 2005. The selected circuits are designed for equalization in different applications but are similar in the fact that they are all implemented using a continuous time transversal filter that can adjust tap weights to compensate for distortion due to the channel. A summary of the performance of each can be seen in Table 1. All papers listed in Table 1 are discussed, but the majority of the discussion focuses on [4] and [5].

Table 1: Summary of different equalizer performance

Ref	Year	Process	Data Rate	Power	Size	Taps	Fractionally Spaced	Tap Delay	f_t
[3]	2000	0.8 μ m GaAs MESFET	2.5 Gbps	-	-	5	Yes	-	20 GHz
[4]	2003	0.18 μ m BiCMOS	10 Gbps	40mW	3mm x 1.5mm	7	Yes	50ps	120 GHz
[5]	2005	0.25 μ m CMOS	1 Gbps	45mW	0.33mm x 0.27mm	6	Yes	125ps	-

3.1 Transversal Equalizers

All three of the selected papers accomplish equalization through the use of a transversal filter as illustrated in Figure 2. Referring to the selected papers listed in Table 1, [3] and [4] implement the transversal filter using an architecture based on a LC distributed amplifier and a Gilbert Cell Multiplier. In [5] the transversal filter is implemented using active circuits. A current mode biquad is used for the delay and a multiplying digital to analog converter (MDAC) is used for the gain.

3.2 The Distributed Amplifier Transversal Filters

The distributed amplifier has typically been used for radio frequency integrated circuit (RFIC) or monolithic microwave integrated circuit (MMIC) applications. This coupled with its wideband characteristics makes it ideally suited for high frequency data communications. Reference [3] originally introduced the Gilbert Cell as a multiplier for equalization, which allows a positive and a negative gain setting. The filter is configured as a 5 tap fractionally spaced equalizer that is designed for 2.5 Gbps data transmission. Published results show that the filter does output a relatively clean eye, but the paper only describes its input as a pseudorandom binary sequence. Without knowing the parameters of the input eye, the equalizers ability to open an eye is unknown and it is difficult to quantify the performance of this equalizer. However, this paper does make an important contribution in the advancement of distributed amplifiers as transversal filters through the addition of the Gilbert Cell multiplier. This allows for a phase reversal of the signal enabling positive or negative gain, which allows for better filter adaptation to the channel and in turn improved ISI removal performance.

Reference [4] is an improvement of the distributed amplifier in [3] offering 7 fractionally spaced taps and a data rate of 10 Gbps over fiber. It is believed that the majority of the improvement in bandwidth can be attributed to the migration of the design from a $f_t = 20$ GHz process in [3] to a $f_t = 120$ GHz process in [4].

The delay line is implemented with an LC ladder constructed with spiral inductors and metal insulator metal (MIM) capacitors. The time delay of each stage is 50ps which leads to a total dispersion coverage of 350ps for a seven tap filter.

As in [3], the multiplier is again based on the Gilbert Cell Multiplier architecture. However, two significant improvements have been proposed. First, the input from the delay cell is buffered with a constant current emitter follower. This ensures constant loading of the LC transmission line. Also, the gain of the Gilbert Cell is varied by adjusting the bias current of the multiplier. This means the Gilbert Cell is effectively operating as a vari-

able gain amplifier. The variable gain adds extra resolution to the tap settings, resulting in a filter that can better adapt to the channel characteristics and hence more effectively remove distortion.

The ambiguity in reporting results in [3] are avoided in [4] as both the input and output eye for a 10 Gbps data stream are shown and the output eye offers noticeable improvement. It is also interesting to note in this design that the output of the individual taps exhibit significant peaking for the taps early in the delay chain, which is reduced to significant attenuation at the end of the chain. This peaking behavior is an inherent problem with LC delays and the uneven tap response may lead to less than optimal solution when converging with a blind adaptation algorithm, such as the LMS algorithm.

It is also important to note that due to the physical size of the inductors, LC delay elements require a large silicon area for implementation. This may not present a significant problem in academic research, but in industry the extra area required for inductors may represent a multi-million dollar investment in silicon real estate. Thus, within industry, there is a push to achieve comparable data rates using active circuitry, which generally requires less area. This leads to incorporation of the third paper dealing with active circuit delay elements, even though the achieved data rate is much lower.

3.3 Active Circuit Transversal Filters

The 1 Gbps equalizer presented in [5] is specifically designed and optimized for cable equalization. This is accomplished through the use of a transversal filter similar to that illustrated in Figure 2, which is implemented using a differential continuous-time current-mode biquad filter for the delay element and a MDAC for the multiplying cells. This architecture is quite different than [3] and [4] but the goal of constructing a transversal filter to remove ISI is common among all three.

The delay element for the filter is implemented using a CMOS current-mode biquad filter that has a variable delay of 100ps to 300ps (nominally 125ps). The delay element also has a varying 3dB bandwidth of 800 MHz to 2.1 GHz depending on its bias current. As the delays are cascaded, the bandwidth at the end of the chain is reduced as extra taps are added. When the weights are optimally configured for equalization, this paper reports a bandwidth of 690 MHz at the output of the last tap. For a 1 Gbps signal, a maximum frequency of 500 MHz occurs if there is an alternating one-zero pattern.

The multiplier is designed to be controlled with a five bit digital signal. This direct digital control removes the requirement for a digital-to-analog converter (DAC) to control the gain. One of the five bits is a sign bit, which sets the gain to be either positive or negative. The remaining four bits allow sixteen discrete gain settings, either positive or negative depending on the sign bit. The goal of the discrete gain is to allow enough resolution so that a controlling algorithm, such as the LMS algorithm, can converge to the optimal setting of gain weights.

In addition to this, a CMOS only approach lends itself to the possibility of reduced power by lowering the supply voltage as technologies improve. Of course this must also be balanced with the other effects of lowering the supply voltage, such as reduced gain, reduced headroom, and less voltage range for common mode variations.

The reported eye results illustrate significant opening of the eye from input to output. The output jitter is reported as less than 100ps, but the input jitter is not reported so improvement can only be quantified by the estimation of the input eye versus the output eye plots.

The power of this equalizer is low compared to [4] but it must also be noted that [4] is operating at 10X the frequency of the active circuit implementation. The silicon area required for the active solution (0.33mm x 0.27mm) is quite reduced from that required by the LC filter solution (3mm x 1.5mm).

3.4 Conclusions

The papers presented in this review are not intended to cover the entire equalization field, but serve as a snapshot of some of the more interesting architectures used for continuous time equalization.

From this literature survey it was interesting to note the differences between the active circuit approach and the LC approach. The results reported in Table 1 contain many empty spaces and it is difficult to compare the performance of the equalizers on a one-to-one basis. From a data rate point of view, the LC implementation in [4] does indeed achieve the fastest data rate of the three. After an extensive search of IEEE publications, a circuit based on an active implementation could not be found that matched this data rate. From this, one may be inclined to say that LC implementations are preferred for achieving high data rates. However, before making such a statement a more extensive search that involves un-published industry research of inductor-less equalizers, and patented designs is required. Unfortunately, this is a very competitive field and at this time, published results and documented implementations are difficult to find.

As frequencies increase, the inductor size will become physically smaller. At some point the size may be reduced enough that the LC approach becomes suitable for most applications. Presently however, the optimal architecture for an equalizer can only be determined after a careful analysis of the distortion, the data rate required, the tap spacing, and the silicon area and power available.

Chapter 4 LC Equalizer

In this chapter the design of an equalizer based on the LC delay element presented in [4] is considered. The equalizer is an implementation of the transversal filter illustrated in Figure 2 with $N=7$. The design is implemented in the IBM SiGe 5nm bipolar process.

4.1 Architecture

The block level schematic used to implement the filter previously illustrated in Figure 2 is shown in Figure 5:

Figure 5. An equalizer block diagram.

The architecture used for the delay cell and Gilbert Cell Multiplier can be seen in Figure 6 and Figure 7 respectively.

Figure 6. An LC delay circuit.

Figure 7. A Gilbert Cell Multiplier.

4.2 Design Procedure

This equalizer is a fractional equalizer which means the delay of each delay element is a fraction of the bit period. For a 10 Gbps data rate, the clock frequency is 10 GHz, but the maximum frequency of the data stream is one bit per clock period, or 5 GHz. This is illustrated in Figure 8.

Figure 8. Clock rate and maximum data rate.

Only the data stream is received and processed by the equalizer. The output of the equalizer is used by a clock and data recovery system to recover and recreate the associated clock.

This design is based on the reference paper [4] and a delay time of $T/2$ was selected where T is equal to the bit period, or 100ps for a 10 Gbps signal

The characteristic impedance of the delay cell is given by:

$$Z_o = \sqrt{\frac{L}{C}} = 50 \, \Omega \quad (1)$$

The time delay is given by:

$$\tau = \sqrt{LC} = 50\text{ps} \quad (2)$$

The design procedure began with determining the inductor and capacitor required for a 50Ω characteristic impedance and 50ps delay. To satisfy these specifications a 500fF capacitor and a 1.25nH inductor were required. However, these values reflect a single-ended LC delay as illustrated in Figure 9.

Figure 9. A Single-ended delay.

These values were then manipulated and optimized in simulation to account for parasitics and to fit the two stage differential delay as illustrated in Figure 6. The differential delay is much more representative of a transmission line than a single stage delay. The final values used for the delay cell are listed in Table 2.

Table 2: LC delay component values

Component	Calculated	Final
L_{11}	625 pH	625 pH
L_{12}	625 pH	625 pH
L_{21}	625 pH	625 pH
L_{22}	625 pH	625 pH
C_1	62.5 fF	-
C_2	125 fF	77fF
C_3	62.5 fF	-

The calculated values were optimized in simulation and capacitors C_1 and C_3 were reduced to account for parasitic capacitance of the multiplier, which loads the delay cell.

The inductor was selected from the IBM SiGe 5am bipolar process kit. The dimensions were varied until the inductance equaled 625pH and are listed in Table 3.

Table 3: Inductor parameters

Component	Value
L	625 pH @ 5GHz
Q	14.6 @ 5 GHz
SRF	43 GHz
Outer Dimension	136 μ M
Turns	2.5
Metal Width	10 μ M
Metal Spacing	5 μ M

The inductor was then simulated in Cadence using the S-parameter analysis and the test bench illustrated in Figure 10.

Figure 10. Inductor test bench.

Using equations (3) and (4) in the Spectre calculator the value of inductance and quality can be plotted against frequency as seen in Figure 11 and Figure 12

$$L = (0.159 * \text{imag}((ZM(1) / \text{xval}(\text{imag}(ZM(1))))) = \frac{\text{Im}[Z_{ind}]}{2\pi F} \quad (3)$$

$$Q = (\text{imag}(ZM(1)) / \text{real}(ZM(1))) = \frac{\text{Im}[Z_{ind}]}{\text{Re}[Z_{ind}]} \quad (4)$$

Figure 11. Inductor inductance characterization results.

Figure 12. Inductor Q characterization results.

The Gilbert Cell was designed according to RF design procedures as outlined in [6] in Chapter 6. However, during optimization, the quad transistors (Q_{21} , Q_{22} , Q_{23} , & Q_{24} in Figure 7) were reduced to minimum size to minimize the parasitic loading on the transmission lines. As a result they are no longer optimally sized for noise and may become the dominant noise contributors in the Gilbert Cell.

The input emitter follower buffers were biased with 1.5mA to allow for a gain of approximately 0dB up to and above 5 GHz. It may be possible to reduce this current with further optimization.

4.3 Equalizer Simulation

Once the Gilbert cell and the delay cell were complete, the equalizer shown in Figure 5 was simulated. For the eye simulations, a low pass filtered pseudo random bit pattern (PRBS7) was used to create an input eye. However, regardless of the tap settings it was impossible to get an eye improvement using the equalizer. An example of the input and output eye diagrams can be seen in the following figure.

Figure 13. Ineffective eye opening.

From this eye diagram it is clear that the output eye exhibits more jitter than the input eye, and as a result, the equalizer is closing the eye rather than opening it.

After a detailed investigation it was determined that the 3-dB response of the equalizer itself was below the data rate. Thus, not only was the equalizer not opening the eye, its low pass frequency response was effectively adding to the lowpass filtering of the channel and as a result the received signal was deteriorated even further.

The parasitic loading due to the multiplier was already reduced as much as possible through the use of minimum size devices. As a result, broadbanding techniques were required to extend the bandwidth. Peaking inductors were used to negate the parasitic capacitance at the output and can be seen in Figure 14.

Figure 14. LC equalizer with peaking inductors.

The pre-peaking inductor frequency response of the equalizer is illustrated in Figure 15. Figure 16 illustrates the effect as the values of the peaking inductor are swept.

Figure 15. Frequency response before peaking inductors added.

Figure 16. Frequency response after peaking inductors were added.

The peaking inductors extend the bandwidth but also add a gain peak at approximately 3 GHz. Based on simulated results illustrated in Figure 16, 4 nH peaking inductors were selected as they result in the most constant inductance below the peaking frequency.

The 3 dB frequency before the peaking inductors were added was only 4.5 GHz, which is below the rate of 10 Gbps or 5 GHz. After the peaking inductors were added, the 3dB frequency was increased to 7.5 GHz. This is above the frequency of the data rate and greatly improved the equalizer performance.

Filter coefficients were optimized through trial and error in simulation. It is recognized that this method may not yield the optimal tap setting, but through iterative simulations a tap settings that resulted in an eye opening was achieved. The final tap settings are listed in Table 4.

Table 4: Final Tap Settings

	Sign	Weight (I_w)
Tap 1	-1	50 μ A
Tap 2	1	50 μ A
Tap 3	1	1000 μ A
Tap 4	1	4000 μ A
Tap 5	1	0 μ A
Tap 6	1	0 μ A
Tap 7	1	0 μ A

The equalizer performance with peaking inductors can be seen in Figure 17, with results specified in Table 5.

Figure 17. Simulated eye opening ability.

Table 5: Jitter results

	Before Equalization	After equalization	Improvement
Horizontal Jitter	37.2 ps	19 ps	51%
Vertical Jitter	0.4 UI	0.28 UI	30 %

4.4 Conclusions

The performance of the LC equalizer indicates that it does indeed remove jitter from an input data stream and effectively opens a degraded eye. The actual amount of improvement required depends on the specifications of the intended application. However given the large silicon area required for such a design ($0.33 \times 0.27 \text{ mm}^2$ reported in [4]) it is the goal of this research to design a 10 Gbps equalizer based on active delays rather than the area intensive LC delay. This work is discussed further in Chapter 5 with fabricated results reported in Chapter 6. Chapter 7 uses the architectures presented in Chapter 5 as building blocks for simulations of an active 10 Gbps equalizer.

Chapter 5 Active Equalizer

5.1 Active Equalizer

The LC equalizer discussed in the previous chapter is based on the transversal filter illustrated in Figure 2. It effectively reduces jitter that is present on the 10 Gbps input data stream however the inductors used in the delay cell make it a very area intensive design. This may prove to be a prohibitive factor in industry where silicon space is expensive. The goal of this chapter is to introduce a delay and multiplier circuit based on active circuitry, thus minimizing the silicon area required. As with the previous LC design, the active equalizer structure is also based on the transversal filter illustrated in Figure 2.

5.2 Delay Design

As delay cells are cascaded to form a delay line, the total bandwidth at the output (BW_{tot}) is reduced according to the following equation:

$$BW_{tot} = BW_c \sqrt[m]{2^{\frac{1}{n}} - 1} \quad (5)$$

where m is equal to 2 for first-order stages and 4 for second-order stages and n is the number of identical stages having bandwidth per cell of BW_c [7]. Thus if a total bandwidth of 5 GHz is required for an eight tap FIR transversal filter created with second-order delay cells, each delay cell must have a bandwidth of at least 9.12 GHz.

To achieve this, the architecture presented in [7] was modified and the resulting modified Cherry-Hooper architecture is shown in Figure 18.

This aspect of the design is explored further in Section 5.2.1. R_{deg} is added to improve the linearity of the circuit and C_1 and C_2 are used to account for parasitic capacitive loading.

The transistor sizing is optimized for high bandwidth, however, as bandwidth increases the time delay from input to output decreases. To maximize the delay bandwidth product and achieve the required time delay, two of the modified Cherry-Hooper gain stages illustrated in Figure 18 are cascaded together to form a single delay cell. This changes the number of stages used in equation (5) from 8 to 16, resulting in a minimum individual delay cell bandwidth of 10.9 GHz. If the bandwidth of the delay cell falls below this, the final taps of the transversal filter will become bandwidth limited and become ineffective in removing distortion.

5.2.1 Delay Cell Analysis

The circuit illustrated in Figure 18 can be represented by the block diagram in Figure 19.

Figure 19. Block diagram of delay cell.

From this diagram, the following transfer function can be obtained:

$$\frac{V_{out}}{V_{in}} = \frac{\left(\frac{R_1}{1 + g_{m1}R_{deg}} \right) \left(\frac{g_{m1}}{R_2 C_1 C_2} \right)}{s^2 + s \left(\frac{R_1 C_1 + R_2 C_2}{R_1 R_2 C_1 C_2} \right) + \frac{1 + g_{mf} R_1}{R_1 R_2 C_1 C_2}} \quad (6)$$

where $R_1/(1+g_{m1}R_{deg})$ is the reduction in gain due to the degeneration. Using this transfer function the second-order parameters, such as the damping coefficient (ζ), the DC gain (A_{vo}), and the natural frequency (ω_n) can be determined as follows:

$$\zeta = \frac{R_1 C_1 + R_2 C_2}{2\sqrt{R_1 R_2 C_1 C_2 (1 + g_{mf} R_1)}} \quad (7)$$

$$A_{vo} = \left(\frac{g_{m1} R_1}{1 + g_{mf} R_1} \right) \left(\frac{R_1}{1 + g_{m1} R_{deg}} \right) \quad (8)$$

$$\omega_n^2 = \frac{1 + g_{mf} R_1}{R_1 R_2 C_1 C_2} \quad (9)$$

Careful examination of these equations reveals that both the delay cell gain and bandwidth are dependant on the gain of the active feedback (g_{mf}). Assuming a constant resistance R_1 , the delay cell gain (A_{vo}) is inversely proportional to $1 + g_{mf} R_1$ and the delay cell bandwidth (ω_n^2) is proportional to $1 + g_{mf} R_1$. Thus, as g_{mf} increases, the delay cell bandwidth increases and its gain decreases. This forms the mechanism that allows gain to be traded for bandwidth.

5.2.2 Delay Cell Specifications

The specifications for the delay cell were developed in collaboration with a company that is researching proprietary products for fiber equalization. The resulting specifications are listed in Table 6.

Table 6: Delay Cell Specifications

	Specification			Units
	Min	Nominal	Max	
Supply voltage	1.6	1.8	1.9	V
Input: Maximum Signal Amplitude	25	50	200	mV _{peak} Diff
Output: Maximum Signal Amplitude	10	50	200	mV _{peak} Diff
Data rate		10		Gbps
Variable gain	-5		10	dB
Variable bandwidth	5		7	GHz
Delay	30	33	35	ps

The delay presented in this chapter has a time delay of $T/3$ which differs from the $T/2$ delay discussed in Chapter 3. The $T/3$ delay leads to better convergence when used with blind adaptation whereas the $T/2$ delay is often used when there is a training sequence. The delay cell proposed in this chapter is designed for the purpose of blind equalization, thus a $T/3$ time delay was selected.

5.3 Multiplier Design

In addition to high bandwidth, the continuous time FIR filter also requires a multiplier that has variable gain and is linear.

Variable gain is achieved through the use of individual gain stages that are switched on or off by the digital control as illustrated in Figure 2. The block level diagram of the multiplier is shown in Figure 20.

Figure 20. Block diagram of the Multiplier.

The gain stages are binary weighted so that various combinations of stages will allow the gain to be increased from a gain of 0 to a maximum gain of 1 with a gain step size of $1/15$. The negative gain is achieved through the swap switch which is illustrated in Figure 21.

Figure 21. A swap switch.

This switch inverts the input signal by crossing the input wires. This removes the requirement for an extra four gain stages with inverted outputs to obtain the negative gain and effectively reduces the potential parasitic loading at the summing node by 50%. The swap switch transistors (M_{11} , M_{12} , M_{21} and M_{22}) must be large so that their resistance is low enough to prevent the input signal from being attenuated. However, the transistors must not be so large that they present a significant input capacitive load on the driving delay stage, thus limiting the frequency response.

5.3.1 Multiplier Implementation

In an attempt to explore alternative low power/low voltage CMOS multiplier designs, the gain stages were implemented using an LNA architecture as shown in Figure 22.

Figure 22. LNA Gain Stage.

This specific LNA architecture has the advantage of combining the differential pair and the current source thus reducing the headroom required and making it ideal for low voltage applications.

The sizing of the differential pair transistors (M_1 & M_2) in Figure 22 is crucial to the operation of the multiplier. As this cell is driven by a delay cell (as illustrated in Figure 2) it is important to keep the input capacitance low and avoid a potential bandwidth bottleneck at the delay multiplier interface. However, the gain of the multiplier pair is roughly proportional to the square root of the width to length ratio (W/L) of the differential pair and the bias current. So to keep the input pair small requires extra current to meet the gain specifications. Thus, a careful analysis is required to determine the optimal balance between capacitive input loading, gain, and power. In addition to this, the cascode transistors (M_3 & M_4) increase the effective bandwidth by reducing the Miller Effect. Furthermore, by keeping the cascode transistors smaller than the input transistors (M_1 & M_2) the parasitic load on the summing node can be minimized.

The gain of each stage is set based on the following gain equation for low noise amplifiers according to [1]:

$$Gain = \frac{g_m R_L}{1 + g_m R_{deg}} \quad (10)$$

When implemented with high g_m transistors, such as bipolar, the denominator can be simplified as follows assuming that $g_m R_{deg} \gg 1$:

$$Gain \cong \frac{g_m R_L}{g_m R_{deg}} \cong \frac{R_L}{R_{deg}} \quad (11)$$

Using CMOS transistors, the achievable g_m is much smaller and the assumption made in (11) does not hold. As a result the gain cannot be set through resistor degeneration alone and both current and the W/L ratio of the differential pair must be varied to obtain the required gains. Thus the gain is no longer determined by a resistor ratio and process

variation will have a significant effect on the gain of the multiplier. Given that the multiplier is in a feedback loop controlled by a DSP algorithm, reduced or increased gain will affect the dynamic range, but is acceptable as long as the multiplier remains linear. However, if the multiplier becomes non-linear, or non-monotonic, it is possible that the FIR filter may not stabilize. Thus for such a design, it is important to maintain linearity even with process variations. To facilitate this, each gain stage is a scaled version of the previous stage. All transistors are matched and the number of fingers in transistors M_1 and M_2 , and M_3 and M_4 are scaled as required. The degeneration resistor in Figure 22, R_{deg} , is also scaled and built from unit resistors that are physically similar. With a proper layout, this leads to a well matched circuit and a very linear multiplier as the different gain stages are switched in.

5.3.2 Multiplier Specifications

As with the delay cell, The specifications for the multiplier were developed in collaboration with a company that is researching proprietary products for fiber equalization. The resulting specifications are listed in Table 7.

Table 7: Multiplier specifications

	Specification			Units
	Min	Nominal	Max	
Supply voltage	1.08	1.2	1.32	V
Input: Maximum signal amplitude	25	100	200	mV _{peak} Diff
Output: Maximum signal amplitude	10	100	200	mV _{peak} Diff
Number of gain Steps		32		
Gain accuracy	-3		3	%
Gain linearity		Monotonic		
Data rate		10		Gbps
Bandwidth	5			GHz

The supply voltage has been reduced to 1.2V in an attempt to save power. The required resolution, or number of gain steps, requires a detailed analysis to determine the resolution that leads to the best filter convergence. For the purpose of this research, this information was obtained from industry.

The filter settings are typically set by a controlling algorithm such as a LMS algorithm. This algorithm cycles through the gain settings to find the optimal convergence point. If the gain is non-monotonic it is possible that the non-linearity may cause the controlling algorithm to become confused which may result in a non-optimal solution or non-convergence. To avoid this, the gain must be monotonic.

Chapter 6 Experimental Results

6.1 Delay Experimental Results

A cascade of eight delay cells was fabricated in a $0.13\mu\text{m}$ BiCMOS technology. This effectively represents the delay line portion of the FFE illustrated in Figure 2 with $N=8$. A capacitive load was added at the output of each delay cell, which corresponds to typical capacitances introduced by a multiplier load in an equalizer implementation. The layout of the delay cell is shown in Figure 23 and the fabricated circuit is illustrated in Figure 24.

Figure 23. Layout of delay cell.

Figure 24. Fabricated delay circuit.

The complete layout size, which is determined by pin count, occupies an area of $500\mu\text{m} \times 1600\mu\text{m}$. A single delay cell occupies an area of only $93\mu\text{m} \times 42\mu\text{m}$.

In the intended application the delay cell does not have to interface with off chip components, however, for testing purposes a 50Ω input signal originates off chip, and a driver is required to drive the 50Ω test equipment. A multiplexer was also incorporated to calibrate out losses and extra time delay associated with the test cables and the driver. The test setup is illustrated in Figure 25.

Figure 25. Block diagram of test setup.

To characterize the relation between the active feedback gain and the delay cell gain and bandwidth, the bias current of the feedback was varied from $100\mu\text{A}$ to $350\mu\text{A}$. The resulting effect is shown in Figure 26 and Figure 27, which illustrates both simulated and measured results at the output of the delay cell. Driver and cable loss are calibrated out.

Figure 26. Delay cell gain versus active feedback bias current.

Figure 27. Delay cell bandwidth versus active feedback bias current.

From these results it is clear that delay cell bandwidth does increase at the expense of gain, as the active feedback current/gain is increased. The bandwidth is slightly reduced at the output of the delay chain, but still allows for a range of 4.3 GHz to 6.9 GHz. Referring to equation (5), this results in an available bandwidth range per delay cell of 9.3 GHz to 15 GHz.

The simulated input versus output amplitude of one gain cell is shown in Figure 28. This plot shows that with a 200mV peak differential input, the output is approximately 175mV. This is 12.5% compression, which is equivalent to the 1dB compression point. It is important to note that since this experiment consisted of 16 cascaded cells, with each cell set to unity gain, the linearity of an individual delay cell is higher than that of the cascaded delay line.

Figure 28. Plot of the output amplitude versus the amplitude of the applied signal at the input.

As random data is transmitted, its power is spread over the frequency spectrum. As a result, if there is peaking in the transfer function of the delay cell, data at different frequencies will see different gains. This problem is magnified as the gain stages are cascaded and the peaking error is multiplied. To minimize this effect, the amplifier was optimized to be critically damped, thus suppressing any peaking behavior.

The simulated and measured S_{21} response of the delay chain, which illustrates peaking and bandwidth, is shown in Figure 29. The frequency response of the driver has been calibrated out and only the output of the delay chain is reported. The current in the active feedback is set to the nominal value of 250 μA .

Figure 29. AC magnitude response of delay chain.

The measured bandwidth of 5.7 GHz is lower than the simulated bandwidth of 6.7 GHz, but is still above the required bandwidth of 5 GHz. Using equation (1) this translates into a 12.6 GHz bandwidth per delay cell. The active feedback current can be adjusted to increase the bandwidth, but at this setting the frequency response is already above the minimum bandwidth requirement for an eight-tap 10 Gbps equalizer.

The time delay of the delay chain is illustrated in the Figure 30. Given this is the time delay of 8 cells, the delay of a single cell can be determined to be $261 \text{ ps}/8 = 32.6 \text{ ps}$.

Figure 30. Time delay.

The time delay was measured with the variable frequency set to approximately 6 GHz at the output of the delay line. Although it has not been measured, it is expected that the time delay will vary as the bandwidth is adjusted.

Further research of the delay cell should also involve examination of the variation of time delay and variation of the phase as the input frequency is swept. This measurement is often referred to as group delay.

Because the delay cell has a feedback path, stability must be examined. Referring to Figure 19, stability was examined by opening the loop at the output of the emitter follower. This node was then loaded with the same loading it would experience in a closed loop. This provides an open loop simulation that accurately reflects the closed loop loading. Using Cadence's Spectre simulator, the open loop magnitude and phase were simulated and the resulting plots are illustrated in Figure 31.

Figure 31. Open loop magnitude and phase.

Gain margin is determined by measuring the gain at the point the phase inverts or reaches 180° . This is illustrated in Figure 31 and the results are reported in Table 8. Phase margin is determined by measuring the phase at the point the gain decreases below 0dB and subtracting it from 180° . In this case, the feedback gain is always below 0dB thus phase margin is not applicable.

Table 8 Gain and Phase Margin

	Simulated
Gain Margin	24.8 dB
Phase Margin	Not applicable

As a general rule of thumb for stability, a gain margin of 10-20dB is desirable. This is clearly achieved in this design.

6.1.1 Delay Summary

A summary of the results for the eight cascaded delay cells can be seen in Table 9.

Table 9: Summary of Delay Line Results

	Specified	Simulated	Measured	Estimated Single Delay cell	Units
Supply voltage	1.8	1.8	1.8	1.8	V
Current		52	45.6	5.7	mA
Variable gain	-5 → 10	-2.5 → 20	-4 → 17	0.4 → 2.1	dB
Variable bandwidth	5 → 7	4.7 → 7.6	4.2 → 6.9	9 → 15	GHz
Delay	264	264	261	32.6	ps

The measured gain and frequency are slightly reduced, but correlate well with simulated results. The time delay is very near the expected value and only differs by 1.2%.

The power is slightly reduced, which may be a result of inaccurate mirroring of currents. This in turn may be a contributing factor to the reduced gain and frequency. It is also important to note that this design was optimized for functionality and not for power savings.

6.2 Multiplier Experimental Results

A single multiplier was fabricated in a $0.13\mu\text{m}$ CMOS technology with a capacitive load equivalent to a four-tap system at the summing node. The layout of the chip is shown in Figure 32 with the insert illustrating a zoomed view of the multiplier and driver circuit.

Figure 32. Layout of multiplier circuit.

The complete layout occupies an area of $1600\mu\text{m} \times 450\mu\text{m}$, but the multiplier itself occupies an area of only $90\mu\text{m} \times 332\mu\text{m}$.

In the intended application the multiplier does not have to interface with off chip components, however, for testing purposes a 50Ω input signal originates off chip, and a driver is required to driver the 50Ω test equipment. This test setup is illustrated in Figure 33.

Figure 33. Block diagram of test setup.

When simulated as an on chip multiplier with a high impedance input source, the multiplier has an S_{21} response shown in Figure 34.

Figure 34. Simulated on chip multiplier.

This simulation illustrates the relatively high bandwidth of the multiplier when operating on chip.

Using the test setup illustrated in Figure 33, with the 50Ω source, lack of wideband 50Ω input matching and the on chip driver, the simulated 3dB point is reduced. Including these effects in simulation returns a 3dB point of 3.7 GHz as illustrated in Figure 35.

Figure 35. Simulated versus measured S_{21} of multiplier and driver.

Figure 35 also illustrates the measured magnitude response. The 3dB point is reduced to approximately 3 GHz. This is a reflection of the fact the measured data not only includes the on chip multiplier performance but also represents the loss and capacitive loading due to probing and testing cables.

Overall, given the relatively good correlation of simulated and measured data, it is reasonable to expect that the high frequency response of the on chip multiplier is slightly reduced from simulated results. This would lead to a 3dB bandwidth of approximately 6.5 GHz. However, without an improved on chip matching it is difficult to make such predictions with certainty.

The measured and simulated peak output signal amplitude versus gain setting is plotted in Figure 36. The circuit was driven with a 2 GHz input with a 100mV peak differential signal swing, and the circuit was digitally stepped through all positive gains from 0 to a maximum voltage gain of 1. This illustrates that the measured multiplier gain also tracks simulated results quite closely. From these results it is possible to conclude that the multiplier is monotonic and gain errors are less than 2%. The largest linear deviation occurs around the mid-point of the gain where the binary setting changes from 0111 to 1000. At this point gain is most sensitive to mismatch errors, but even with this sensitivity, the gain error is still below 2%.

Figure 36. Output amplitude variation with gain setting.

The gain error between gain setting seven (0111) and eight (1000) is a result of ΔW mismatches between the least significant three gain stages and the most significant gain

stage. To ensure that this mismatch does not lead to non-monotonic performance Monte-Carlo simulations varying transistor mismatches were analyzed. For these simulations the transistor mismatch was varied in one hundred runs for gain setting seven and eight. The results of the simulations are illustrated in Figure 37.

Figure 37. Monte Carlo simulation of differential input transistor with ΔW mismatch.

The Monte Carlo results in Figure 37 clearly illustrate that even with the transistor mismatch the output voltage of the gain setting seven does not increase above the output voltage for the gain setting eight. This ensures monotonic behavior.

Figure 38 illustrates the linearity at the output of the delay cell as the amplitude of the input signal is swept for the maximum gain setting. It is expected that most signals received by the equalizer will be in the range of 50mV to 150mV peak differential.

Figure 38. Linearity with increasing input signal.

Measured results indicate that at low voltages the multiplier is quite linear and measured results are closely correlated to simulated results. At 100mV the output signal is compressed by approximately 3% compared to the simulated 2% compression.

6.2.1 Multiplier Summary

A summary of the results can be seen in Table 10.

Table 10: Summary of Multiplier Results

	Specified	Simulated	Measured	Units
Supply voltage	1.2	1.2	1.2	V
Power		1.8	1.5	mW
Linearity	Monotonic	Monotonic	Monotonic	
Linearity error (at 100mV)	< 3%	2	3	%
Gain error	2%	1	2	%
3dB bandwidth	5	7.5	6.5	GHz

The measured linearity and gain errors are within the acceptable specified range. As expected the largest gain errors are centered around the mid-point of the gain where the binary setting changes from 0111 to 1000. Further research into this sensitivity should involve characterization of many parts to ensure that the signal remains monotonic as transistor mismatch varies.

As well, for testing purposes, further versions of this design should include an on chip multiplexer as included with the delay cell. This will help calibrate out cable and driver losses.

Chapter 7 Active Equalizer Simulations

7.1 Architecture

The equalizer presented in this section is an implementation of the transversal filter previously illustrated in Figure 2. The delay and multiplier cells consist of the designs introduced in Chapter 5 with a few minor modifications. To reduce the parasitic loading on the delay cell the AC coupling capacitor used in the multiplier was reduced from 10pF to 5pF and the width of the transistors used for the swap switch, illustrated in Figure 21, was reduced by 50%. The delay cell resistors, R_1 in Figure 18, were reduced from 300 Ω to 295 Ω . This reduced the gain of the delay chain from 2.5dB to 0dB with an active feedback current of 250 μ A. A top-level schematic for the eight-tap equalizer is illustrated in Figure 39.

Figure 39. Active equalizer schematic.

This implementation does not include a gain control loop or DC offset correction. These circuits are required for a full implementation of an equalizer. The total gain of the delay chain is very sensitive to process and temperature variations as gain errors are cascaded. Thus, a minor increase or decrease in delay cell gain may result in signal compression or clipping at the end of the chain. Also, with process variation, small width and length variations can occur in the transistors, which result in DC offset. This variation is statis-

tically random, but if the situation occurs where the DC offsets add, the delay cells may cease to operate correctly. Since component variation is a random process, it can only be modeled using Monte Carlo simulations. The simulated offset at the output of the a single delay cell can be seen in Figure 40.

Figure 40. DC offset at output of delay cell based on Monte Carlo simulation of transistor variations.

As the DC offset increases past $\pm 10\text{mV}$, the output of the delay cell will become compressed and distorted. This leads to an increase in the ISI and the equalizer begins to fail. From the results presented in Figure 40, it is clear that without DC offset correction, 5%

of the equalizers fall into this category. In addition, 30% of the remaining equalizers that exhibit a $\pm 10\text{mV}$ to $\pm 5\text{mV}$ offset will have degraded performance. Thus, DC offset correction is required.

The multiplier was originally optimized for four multipliers per summing node but the equalizer presented in Figure 39 has 8 multipliers per tap. To accomplish this, peaking inductors were required to increase the bandwidth.

7.2 Peaking Inductors

The architectures of the delay cell and multiplier were selected and carefully optimized for high frequency performance to specifically avoid the use of area hungry peaking inductors. This was driven primarily by the desire to save silicon area as the problem is compounded given inductors would be required for each stage of the eight tap filter.

Peaking inductors were used at the summing node to increase the bandwidth by nullifying the parasitic capacitance associated with the multipliers. This required only a single set of peaking inductors and the associated area required was considered acceptable.

7.2.1 Inductor Design

In the design of peaking inductors the self resonant frequency (SRF) is of utmost importance. Above the SRF the inductor is not only ineffective in nullifying the parasitic loading capacitance but its capacitive characteristics add to the loading, reducing the bandwidth even further. The desired response of a peaking inductor is a relatively constant inductance over the frequency range of interest and a SRF that is significantly higher than the data rate. The inductor is not specifically optimized to achieve high Q.

For this equalizer, an inductor of approximately 1.4nH was required. This number is derived from both estimated parasitic capacitance and silicon area optimization. The layout of the peaking inductor can be seen in the Figure 41 with dimensions listed in Table 11.

Figure 41. Inductor layout.

Table 11: Inductor Dimensions

Parameter	Value
Length	40 μm
Width	40 μm
Metal Width	1 μm
Metal Spacing	1 μm
Turns	5.75
Inductor metal	Metal 5
Under pass metal	Metal 4

The characterization of the inductor was conducted according to the procedure presented in [6] in chapter 5. This required de-embedding structures as illustrated in Figure 42.

Figure 42. Inductor de-embedding structures.

This de-embedding allows for the mathematical removal of the parasitic capacitance and resistance associated with the probing pads and pins. The Matlab code used for de-embedding is presented in Appendix A. To create a model of the fabricated inductor for Cadence simulations, the measured de-embedded S-parameter data was imported into a H-spice curve fitting script. This curve fitting script was used to obtain component values for the inductor model illustrated in Figure 43. Solved component values are listed in Table 12. See Appendix B for H-spice curve fitting script.

Figure 43. Inductor model.

Table 12: Component Values Obtained from Curve Fitting

Component	Value
L_S	729 pH
R_S	26.3 Ω
R_{P1}	1405 Ω
R_{P2}	488.9 Ω
C_{P1}	1.31 fF
C_{P2}	3.43 fF
C_{BR}	6.584 fF

The measured and modeled inductor results can be seen in Figure 44 and Figure 45.

Figure 44. Measured and modeled inductance.

Figure 45. Measured and modeled Q.

From these results it is apparent that the model closely matches the measured data. The network analyzer used for characterization had a maximum frequency of 40 GHz. This does not capture the SRF of the inductor, but does illustrate that the inductance is relatively stable up to 30 GHz. Given a maximum data frequency of 5 GHz, the inductor performance was deemed acceptable. It is also noticeable that the Q is not very high, however, as previously stated a high Q inductor is not the goal when designing peaking inductors.

7.3 Simulation Results

For simulation purposes, the equalizer was implemented as previously illustrated in Figure 39. Before simulating eye opening ability, the delay chain and multiplier were characterized to ensure a gain of 0dB with no peaking and a minimum bandwidth that is above 5 GHz.

The AC response of the delay line was simulated and the results can be seen in Figure 46.

Figure 46. Delay chain characterization.

As expected the bandwidth is reduced as the delay elements are cascaded. The bandwidth at the output of the first delay is approximately 11 GHz, which is reduced to 6 GHz at the output of the eighth stage. These results are slightly reduced from the measured results reported in Chapter 6. This is a result of the increased capacitive loading of the multiplier compared to the assumed capacitive loading used in test chip to characterize the delay cell. The gain has been slightly reduced by adjustments to R_1 in Figure 18 and is approximately 0dB at the output of all delay elements. As in the experimental results, peaking is limited to 0dB.

The multipliers were characterized by turning on a single multiplier, with a gain setting of 0dB, and measuring the frequency response at the summing node. All eight multipliers are connected to the same summing node, which also contains peaking inductors to reduce the parasitic loading and increase the bandwidth at that node. Using separate simulations the response curves for taps 1, 3, 5, and 8 were recorded and are presented in Figure 47

Figure 47. Summing node characterization.

As the selected tap increases the bandwidth decreases. This decrease is not due to the multipliers but rather to the frequency reduction of the delay line as the tap value increases. The bandwidth is lowest when the eighth multiplier is used. Simulated results

indicated the bandwidth is approximately 5.5 GHz, which is still above the maximum data rate of 5 GHz. A slight gain variation is evident and can be attributed to the loading of different taps of the delay chain. The gain variation is limited to less than -0.3dB which results in a reduction of a 100mV signal to 96.6mV. This small reduction was deemed acceptable.

Finally, to quantify the equalizers ability to remove distortion, an input signal based on multi-mode fiber signal characterization was input to the equalizer and the output eye was recorded. The tap setting for the equalizer is listed in Table 13.

Table 13: Equalizer Tap Setting

Tap	Gain	Digital Gain Setting
1	0	0 0000
2	-2/15	1 0010
3	1	0 0001
4	-5/15	1 0100
5	1/15	0 0001
6	-2/15	1 0010
7	0	0 0000
8	0	0 0000

The input waveform can be seen in Figure 48 with the input and output eye diagram illustrated in Figure 49 and Figure 50 respectively.

Figure 48. Degraded input signal.

Figure 49. Input eye diagram.

Figure 50. Output eye diagram.

The output eye clearly removes some of the jitter present on the input. A summary of the results can be seen in Table 14.

Table 14: Summary of Equalizer Results

	Before Equalization	After equalization	Improvement
Horizontal Jitter	36 ps	18.9 ps	48 %
Vertical Jitter	0.32 UI	0.23 UI	28 %

The amplitude of the output signal (approximately $35\text{mV}_{\text{peak}}$) is noticeably reduced from the input amplitude (approximately $75\text{mV}_{\text{peak}}$). This is a result of the overall summation of the positive and negative multiplier gains listed in Table 13. A summation of all the positive and negative gains results in a net gain of $7/15$. Applying this gain to the 75mV input signal results in a 35mV output signal, which matches the simulation results.

7.4 Conclusions

This chapter presents an equalizer based on active building blocks that achieves 10 Gbps equalization. The structure of the filter is based on the equalizer previously illustrated in Figure 2, with $N=8$, and is created using the delay cell and multiplier proposed in Chapter 5. The multiplier was originally optimized for four taps per summing node. To achieve eight taps as proposed in this chapter, inductive peaking was required to reduce the capacitive loading at the summing node.

Characterization of the equalizer indicates that the bandwidth of the filter is above the maximum data transmission rate, thus is sufficient for 10 Gbps equalization. This fact is verified through simulation by supplying a data stream to the equalizer that forms a degraded eye at the input. The equalizer is then configured to remove the maximum amount of distortion and simulations show a 48% and 28% improvement in horizontal and vertical jitter respectively compared to simulations without equalization.

Chapter 8 Conclusions

This work examines high frequency feed forward linear equalization from the point of view of an active transistor and LC implementation. An LC equalizer was designed and simulated demonstrating its potential use as a high frequency equalization solution. However, due to the large silicon area required by the inductors an alternative solution that requires less area was proposed. It has been shown through this work that 10 Gbps equalization can be achieved through the use of building blocks based on active transistors. The design of a delay cell and a multiplier were presented and fabricated. The measured and simulated results of the circuits demonstrated reasonable agreement.

In simulation, the building blocks were then configured to form an equalizer and it was demonstrated that the equalizer can effectively remove distortion from a 10 Gbps signal reducing horizontal jitter by 48% and vertical jitter by 28%.

Results of this research have been published in three conference papers [11], [12] and [13].

8.1 Future work

Future work involves fabricating the active equalizer proposed in Chapter 7 and obtaining measured results. This work could also involve implementation of a gain control and DC offset correction for the delay chain.

Further work could also involve a detailed study of group delay and linearity of the delay chain.

Appendix A

Matlab De-embedding Code

- This script is used to remove the measured parasitic resistance and capacitance associated with the test structures used for inductor characterization.

```
% -----
% sp_2_L_deembed.m
% -----
% Justin Abbott
% Jan 2005

% Summary
% -----
% File reads in S-Parameter lab data for an inductor and it's
% de-embedding structures (open and short). This de-embedding
% data is then used to mathematically remove parasitic
% capacitance from the inductor. The inductance is then
% calculated and plotted vs frequency.

% Required
% -----
% Remove all headings from the data files so that Matlab can
% read in the data
%
% Reference
% -----
% J W.M. Rogers and Calvin Plett,
% "Radio Frequency Integrated Circuit Design"
% Artech House Inc. May 2003.
% Page: 116 & 135
% Sparameter conversions on Page:92
% -----
clear all;

% *****
% READ IN DATA

% Laptop
% dir_ind = 'D:\My Documents\Univ-Thesis\Chip 2 - TN1003\Data - Inductor
Lab\Chip 1\';
% dir_ind = 'A: ';
% dir_ind = 'D:\My Documents\Univ-Thesis\Chip 2 - TN1003\Data - Inductor
Lab\Chip 1\';

% PC
```


Appendix A

```
%dir_ind = 'C:\Documents and Settings\Justin.JA-HOME-PC\My Documents\Univ-Thesis\Chip 2 - TN1003\Data - Inductor Lab\Chip 1\';
dir_ind = 'C:\Documents and Settings\Justin.JA-HOME-PC\My Documents\Univ-Thesis\Chip 1 - TN1001\Data - Inductor\Inductor Jan 31\Gennum 2\';

% dir_deembed = 'D:\My Documents\Univ-Thesis\Chip 2 - TN1003\Data - Inductor Lab\De-Embed Tn1001';
% dir_deembed = dir_ind;
dir_deembed = 'C:\Documents and Settings\Justin.JA-HOME-PC\My Documents\Univ-Thesis\Chip 2 - TN1003\Data - Inductor Lab\De-Embed Tn1001\';

ind_file = 'data02.s1';           % Ind S Parameters
%ind_file = 'short.s1';
open_file = 'data00.s1';         % open S parameters
short_file = 'data01.s1';        % short S parameters

ind_file = fopen(strcat(dir_ind,'\ ',ind_file));
open_file = fopen(strcat(dir_deembed,'\ ',open_file));
short_file = fopen(strcat(dir_deembed,'\ ',short_file));

% Read in Data
ind_data = fscanf(ind_file,'%g %g %g %g %g %g %g %g %g %g',[9 inf]); % x =
sparameters
ind_data = ind_data';
open_data = fscanf(open_file,'%g %g %g %g %g %g %g %g %g %g',[9 inf]); % x
= sparameters
open_data = open_data';
short_data = fscanf(short_file,'%g %g %g %g %g %g %g %g %g %g',[9 inf]); %
x = sparameters
short_data = short_data';

[row col] = size(ind_data);

% Create Output File
% outFile = fopen('C:\Documents and Settings\Justin.JA-HOME-PC\My Documents\Univ-Thesis\Chip 1 - TN1001\Data - Inductor Lab\DeEmb Spara.xls','w');
outFile_RI = fopen('C:\Documents and Settings\Justin.JA-HOME-PC\My Documents\Univ-Thesis\Chip 2 - TN1003\Data - Inductor Lab\DeEmb Spara RI.xls','w'); %Real and Imag
outFile_MP = fopen('C:\Documents and Settings\Justin.JA-HOME-PC\My Documents\Univ-Thesis\Chip 2 - TN1003\Data - Inductor Lab\DeEmb Spara MP.xls','w'); %Mag and Phase

%outFile = fopen('D:\My Documents\Univ-Thesis\Chip 2 - TN1003\Data - Inductor Lab\DeEmb Spara.xls','w');

% *****
% DE-EMBEDD
```

Appendix A

```
% Extract Complex S parameters from file
for x = 1:row
    %Create Frequency Array
    f(x,1) = ind_data(x,1);

    %-----
    %INDUCTOR
    % Extract Complex S parameters from INDUCTOR file
    % Note: (x,1) forces row vectors
    s11_ind(x,1) = (ind_data(x,2) + ind_data(x,3)*i);
    s21_ind(x,1) = (ind_data(x,4) + ind_data(x,5)*i);
    s12_ind(x,1) = (ind_data(x,6) + ind_data(x,7)*i);
    s22_ind(x,1) = (ind_data(x,8) + ind_data(x,9)*i);

    % Solve for Inductor Y parameters.
    y11_ind(x,1) = (1/50)*((1+s22_ind(x))*(1-
s11_ind(x))+s12_ind(x)*s21_ind(x))/((1+s11_ind(x))*(1+s22_ind(x)) -
s12_ind(x)*s21_ind(x));
    y12_ind(x,1) = (1/50)*(-
2*s12_ind(x))/((1+s11_ind(x))*(1+s22_ind(x)) - s12_ind(x)*s21_ind(x));
    y21_ind(x,1) = (1/50)*(-
2*s21_ind(x))/((1+s11_ind(x))*(1+s22_ind(x)) - s12_ind(x)*s21_ind(x));
    y22_ind(x,1) = (1/50)*((1+s11_ind(x))*(1-s22_ind(x)) +
s12_ind(x)*s21_ind(x))/
((1+s11_ind(x))*(1+s22_ind(x)) -
s12_ind(x)*s21_ind(x));

    % Solve for Inductor Z parameters - page 92 in RFIC Text Book
    z11_ind(x,1) = 50*((1+s11_ind(x))*(1-
s22_ind(x))+s12_ind(x)*s21_ind(x))/((1-s11_ind(x))*(1-s22_ind(x)) -
s12_ind(x)*s21_ind(x));
    z12_ind(x,1) = 50*(2*s12_ind(x))/((1-s11_ind(x))*(1-s22_ind(x)) -
s12_ind(x)*s21_ind(x));
    z21_ind(x,1) = 50*(2*s21_ind(x))/((1-s11_ind(x))*(1-s22_ind(x)) -
s12_ind(x)*s21_ind(x));
    z22_ind(x,1) = 50*((1+s22_ind(x))*(1-
s11_ind(x))+s12_ind(x)*s21_ind(x))/((1-s11_ind(x))*(1-s22_ind(x)) -
s12_ind(x)*s21_ind(x));

    % Solve for z_port_ind
    z_port1_raw(x,1) = z11_ind(x,1) -
z12_ind(x,1)*z21_ind(x,1)/z22_ind(x,1);
    z_port2_raw(x,1) = z22_ind(x,1) -
z12_ind(x,1)*z21_ind(x,1)/z11_ind(x,1);

    %-----
    %OPEN
    % Extract Complex S parameters from OPEN file
    s11_open(x,1) = (open_data(x,2) + open_data(x,3)*i);
    s21_open(x,1) = (open_data(x,4) + open_data(x,5)*i);
    s12_open(x,1) = (open_data(x,6) + open_data(x,7)*i);
    s22_open(x,1) = (open_data(x,8) + open_data(x,9)*i);
```

Appendix A

```
% Solve for OPEN Y parameters.
y11_open(x,1) = (1/50)*((1+s22_open(x))*(1-
s11_open(x))+s12_open(x)*s21_open(x))/((1+s11_open(x))*(1+s22_open(x)) -
s12_open(x)*s21_open(x));
y12_open(x,1) = (1/50)*(-
2*s12_open(x))/((1+s11_open(x))*(1+s22_open(x)) -
s12_open(x)*s21_open(x));
y21_open(x,1) = (1/50)*(-
2*s21_open(x))/((1+s11_open(x))*(1+s22_open(x)) -
s12_open(x)*s21_open(x));
y22_open(x,1) = (1/50)*((1+s11_open(x))*(1-s22_open(x)) +
s12_open(x)*s21_open(x))/((1+s11_open(x))*(1+s22_open(x)) -
s12_open(x)*s21_open(x));

%-----
%Short
% Extract Complex S parameters from short file
s11_short(x,1) = (short_data(x,2) + short_data(x,3)*i);
s21_short(x,1) = (short_data(x,4) + short_data(x,5)*i);
s12_short(x,1) = (short_data(x,6) + short_data(x,7)*i);
s22_short(x,1) = (short_data(x,8) + short_data(x,9)*i);

% Solve for short Y parameters.
y11_short(x,1) = (1/50)*((1+s22_short(x))*(1-
s11_short(x))+s12_short(x)*s21_short(x))/((1+s11_short(x))*(1+s22_short(
x)) - s12_short(x)*s21_short(x));
y12_short(x,1) = (1/50)*(-
2*s12_short(x))/((1+s11_short(x))*(1+s22_short(x)) -
s12_short(x)*s21_short(x));
y21_short(x,1) = (1/50)*(-
2*s21_short(x))/((1+s11_short(x))*(1+s22_short(x)) -
s12_short(x)*s21_short(x));
y22_short(x,1) = (1/50)*((1+s11_short(x))*(1-s22_short(x)) +
s12_short(x)*s21_short(x))/((1+s11_short(x))*(1+s22_short(x)) -
s12_short(x)*s21_short(x));

% Solve for short Z parameters.
z11_short(x,1) = 50*((1+s11_short(x))*(1-
s22_short(x))+s12_short(x)*s21_short(x))/((1-s11_short(x))*(1-
s22_short(x)) - s12_short(x)*s21_short(x));
z12_short(x,1) = 50*(2*s12_short(x))/((1-s11_short(x))*(1-
s22_short(x)) - s12_short(x)*s21_short(x));
z21_short(x,1) = 50*(2*s21_short(x))/((1-s11_short(x))*(1-
s22_short(x)) - s12_short(x)*s21_short(x));
z22_short(x,1) = 50*((1+s22_short(x))*(1-s11_short(x)) +
s12_short(x)*s21_short(x))/((1-s11_short(x))*(1-s22_short(x)) -
s12_short(x)*s21_short(x));
%-----
%-----

% Remove Parallel Parasitics by Subtracting Y_open
```

Appendix A

```
y11_dut(x,1) = y11_ind(x,1) - y11_open(x,1);
y12_dut(x,1) = y12_ind(x,1) - y12_open(x,1);
y21_dut(x,1) = y21_ind(x,1) - y21_open(x,1);
y22_dut(x,1) = y22_ind(x,1) - y22_open(x,1);

y11_short_prime(x,1) = y11_short(x,1) - y11_open(x,1);
y12_short_prime(x,1) = y12_short(x,1) - y12_open(x,1);
y21_short_prime(x,1) = y21_short(x,1) - y21_open(x,1);
y22_short_prime(x,1) = y22_short(x,1) - y22_open(x,1);

% Create Z parameters for DUT
z11_dut(x,1) = y22_dut(x,1)/(y11_dut(x,1)*y22_dut(x,1)-
y12_dut(x,1)*y21_dut(x,1));
z12_dut(x,1) = -y12_dut(x,1)/(y11_dut(x,1)*y22_dut(x,1)-
y12_dut(x,1)*y21_dut(x,1));
z21_dut(x,1) = -y21_dut(x,1)/(y11_dut(x,1)*y22_dut(x,1)-
y12_dut(x,1)*y21_dut(x,1));
z22_dut(x,1) = y11_dut(x,1)/(y11_dut(x,1)*y22_dut(x,1)-
y12_dut(x,1)*y21_dut(x,1));

% Create Z parameters for Y short prime
z11_short_prime(x,1) = y22_short_prime(x,1)/(y11_short_prime(x,1)*y22_short_prime(x,1)-
y12_short_prime(x,1)*y21_short_prime(x,1));
z12_short_prime(x,1) = -y12_short_prime(x,1)/(y11_short_prime(x,1)*y22_short_prime(x,1)-
y12_short_prime(x,1)*y21_short_prime(x,1));
z21_short_prime(x,1) = -y21_short_prime(x,1)/(y11_short_prime(x,1)*y22_short_prime(x,1)-
y12_short_prime(x,1)*y21_short_prime(x,1));
z22_short_prime(x,1) = y11_short_prime(x,1)/(y11_short_prime(x,1)*y22_short_prime(x,1)-
y12_short_prime(x,1)*y21_short_prime(x,1));

% Subtract series Parasitics from DUT
z11_final(x,1) = z11_dut(x,1) - z11_short(x,1); % ignores short
- open parasitics (negligible)
z12_final(x,1) = z12_dut(x,1) - z12_short(x,1);
z21_final(x,1) = z21_dut(x,1) - z21_short(x,1);
z22_final(x,1) = z22_dut(x,1) - z22_short(x,1);

% z11_final(x,1) = z11_dut(x,1) - z11_short_prime(x,1); % in-
cludes short - open parasitics
% z12_final(x,1) = z12_dut(x,1) - z12_short_prime(x,1);
% z21_final(x,1) = z21_dut(x,1) - z21_short_prime(x,1);
% z22_final(x,1) = z22_dut(x,1) - z22_short_prime(x,1);

% Create De-embedded Sparameters
```

Appendix A

```

        s11_deembed(x,1) = ((z11_final(x,1)-50)*(z22_final(x,1)+50)-
z12_final(x,1)*z21_final(x,1))/((z11_final(x,1)+50)*(z22_final(x,1)+50)-
z12_final(x,1)*z21_final(x,1));
        s12_deembed(x,1) = 2*
z12_final(x,1)*50/((z11_final(x,1)+50)*(z22_final(x,1)+50)-
z12_final(x,1)*z21_final(x,1));
        s21_deembed(x,1) = 2*
z21_final(x,1)*50/((z11_final(x,1)+50)*(z22_final(x,1)+50)-
z12_final(x,1)*z21_final(x,1));
        s22_deembed(x,1) = ((z11_final(x,1)+50)*(z22_final(x,1)-50)-
z12_final(x,1)*z21_final(x,1))/((z11_final(x,1)+50)*(z22_final(x,1)+50)-
z12_final(x,1)*z21_final(x,1));

        % Solve for port
        z_port1(x,1) = z11_final(x,1) -
(z12_final(x,1)*z21_final(x,1))/z22_final(x,1);
        z_port2(x,1) = z22_final(x,1) -
(z12_final(x,1)*z21_final(x,1))/z11_final(x,1);

        %Solve for L, R, & Q
        R(x,1) = real(z_port1(x,1));
        L(x,1) = imag(z_port1(x,1))/(2*pi*f(x,1));
        Q(x,1) = abs(imag(z_port1(x,1)))/abs(real(z_port1(x,1)));

%      % Convert L to nH
        L(x,1)=L(x,1) * 1e9;

        % Output De-Embedded S Parameters

fprintf(outFile_RI,'%16s\t%16s\t%16s\t%16s\t%16s\t%16s\t%16s\t%16s
\n',f(x,1),
                                real(s11_deembed(x,1)),
imag(s11_deembed(x,1)),real(s12_deembed(x,1)),
imag(s12_deembed(x,1)),real(s21_deembed(x,1)),
imag(s21_deembed(x,1)),real(s22_deembed(x,1)), imag(s22_deembed(x,1)));

fprintf(outFile_MP,'%16s\t%16s\t%16s\t%16s\t%16s\t%16s\t%16s\t%16s
\n',f(x,1),
abs(s11_deembed(x,1)),
angle(s11_deembed(x,1))*180/3.14,
abs(s12_deembed(x,1)),
angle(s12_deembed(x,1))*180/3.14,
abs(s21_deembed(x,1)),
angle(s21_deembed(x,1))*180/3.14,
abs(s22_deembed(x,1)),
angle(s22_deembed(x,1))*180/3.14 );

end

% Find SRF
% x=3;
% for x = 3:row
%     if (L(x,1) == max(L))
%         SRF=x;
%     end
% end

```

Appendix A

```
% *****
% PLOT L AND Q

%Plot Inductance
figure(1);
grid;
subplot(211)
semilogx(f,L);
ylabel('Ind (nH)');
title('Inductance Vs Freq');
%axis([min(f) max(f) -0.5 2 ]);
axis([0.1e9 1e11 -0 4 ]);

grid;

%Plot R
% subplot(212)
% semilogx(f,R);
% xlabel('Frequency (Hz)'); ylabel('R');
% title('R Vs Freq');
% axis([0.5e9 1e11 -0 100 ]);
% grid;

%Plot Q
subplot(212)
semilogx(f,Q);
xlabel('Frequency (Hz)'); ylabel('Q');
title('Q Vs Freq');
axis([0.5e9 1e11 -0 7 ]);
grid;
% *****

x=1;
fclose('all');
```

Appendix B

Hspice Optimization Code

- This script is used to calculate the ideal component values used in Figure 43 to model a measured inductor.

```
.option acct nomod post=2

.net v(p2) vin rout=50 rin=50

vin p1 0 AC 1

L1      p1      3      Ls
R1      3        4      Rs
R2      4        5      Rs
L2      5        p2     Ls
Cs1     p1      1      Cp1
Cs2     p2      2      Cp2
Rs1     1        0      Rp1
Rs2     2        0      Rp2
Cbr1    p1      4      Cbr
Cbr2    4        p2     Cbr

.param
+ Ls = OPT1(2n,.1n,100n)
+ Rs = OPT1(0.5,.1,10k)
+ Rp1 = OPT1(200,.1,100k)
+ Rp2 = OPT1(200,.1,100k)
+ Cp1 = OPT1(0.327p,.001p,10p)
+ Cp2 = OPT1(0.315p,.001p,10p)
+ Cbr = OPT1(.02p,.0001p,10p)

.AC data=measured optimize=opt1
+ results=comp1,comp2,comp3,comp4,comp5,comp6,comp7,comp8
+ model=converge
.model converge opt relin=1e-4 relout=1e-4 close=10 itropt=30
.measure ac comp1 err1 par(s11m) s11(m)
.measure ac comp2 err1 par(s11p) s11(p)
.measure ac comp3 err1 par(s12m) s12(m)
.measure ac comp4 err1 par(s12p) s12(p)
.measure ac comp5 err1 par(s21m) s21(m)
.measure ac comp6 err1 par(s21p) s21(p)
.measure ac comp7 err1 par(s22m) s22(m)
.measure ac comp8 err1 par(s22p) s22(p)
.ac data=measured
*.print par(s11r) s11(r) par(s11i) s11(i)
*.print par(s12r) s12(r) par(s12i) s12(i)
*.print par(s21r) s21(r) par(s21i) s21(i)
```

Appendix B

```
*.print par(s22r) s22(r) par(s22i) s22(i)
*.print z11(r) z11(i) z11(m) z11(p)
*.print z22(r) z22(i) z22(m) z22(p)
*.print z12(r) z12(i) z12(m) z12(p)
*.print z21(r) z21(i) z21(m) z21(p)

.data measured
FREQ      s11m      s11p      s12m      s12p      s21m      s21p      s22m      s22p
5.0000000000E+07  3.5127200000E-01  1.0693870000E+00  6.4661080000E-01
                 -3.7733800000E-01  6.5390110000E-01  -3.9799180000E-01
                 3.5063710000E-01  3.7068410000E-01
2.5000000000E+08  3.5013200000E-01  1.1549200000E+00  6.4769580000E-01
....

.enddata
.param freq=100MEG,s11m = 0 , s11p = 0, s12m = 0, s12p = 0, s21m =0,
+s21p =0, s22m =0 , s22p = 0
.end
```


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