A Balanced Monolithic Oscillator with Low Phase Noise Performance

by

Leonard Dauphinee

A thesis submitted to the Faculty of Graduate Studies and Research
in partial fulfillment of the requirements for the degree of Doctor of Philosophy
in Engineering

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Abstract

A new balanced LC voltage controlled oscillator topology is presented for monolithic implementation in either wireless or wireline applications. A design methodology is presented to optimize phase noise performance and power consumption of the proposed topology. An original idea is also proposed for a normalized figure of merit to enable the comparison of the measured or simulated performance of different VCO architectures. The measured performance of the proposed oscillator topology compares favourably with present state of the art when the proposed figure of merit is used. Excellent correlation was also achieved between measured and simulated performance using modern simulation tools.

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Table of Contents

CHAPTER 1	<i>Introduction</i>	<i>1</i>
	1.1 The Challenge	3
	1.2 Digital Radio Receivers	6
	1.3 What is Phase Noise?	7
	1.3.1 Phase Noise Requirements for Radio Receivers.	9
	1.3.2 Other VCO Requirements for Digital Radio	11
	1.4 Classes of Oscillator Circuits	12
	1.5 Contributions and Thesis Outline	14
CHAPTER 2	<i>Oscillator Phase Noise Models</i>	<i>17</i>
	2.1 Device Noise Sources	17
	2.2 Circuit Noise Mechanisms	20
	2.3 Linear Time Invariant Noise Model	22
	2.4 The Nonlinear Mechanisms of Phase Noise Sidebands	25
	2.4.1 Transient/Fourier Analysis of Phase Noise	27
	2.5 Linear Time Varying Phase Noise Theory and Linear LC Oscillators 29	
	2.5.1 The Ideal Oscillator	36
	2.5.2 The Hajimiri Method (Green's Function Method)	38
	2.5.3 Details of Hajimiri's Method	39
	2.5.3.1 Spurious Tones	41
	2.5.3.2 Stationary Noise Processes	43
	2.5.3.3 Cyclostationary Random Processes	44
	2.6 Floquet Multipliers and Commercial Phase Noise Simulators	46
CHAPTER 3	<i>The Design, Analysis, & Simulation of LC Resonator Oscillators</i>	<i>49</i>
	3.1 Oscillator Circuit Analysis	50
	3.2 Common LC Resonator Oscillator Topologies	50
	3.3 Which Colpitts Biasing Scheme?	52
	3.4 The Common Collector Colpitts	54
	3.4.1 Linear Analysis of Common Collector Colpitts Oscillator	56
	3.4.1.1 SPICE AC Analysis	61
	3.5 A Balanced LC Colpitts Oscillator	62
	3.6 Designing the Balanced Colpitts Oscillator for Low Phase Noise	

	65
3.6.1 Inductor Selection	66
3.6.2 Selecting the Collector Load Impedance	66
3.6.3 The Choice of Capacitor Ratio	68
3.6.4 Oscillator Bias Current	76
3.7 Class C Circuit Operation and Active Device Sizing	84
3.8 Simulation of Final Design Performance	86
 CHAPTER 4	
<i>Measurements and Results</i>	<i>90</i>
4.1 Phase Noise Versus Bias Current	92
4.2 Phase Noise Sideband Measurements	97
4.3 Phase Noise versus Device Headroom	100
4.4 Phase Noise versus Tuning Voltage	101
4.5 Oscillator Figure of Merit	102
4.5.1 Comparison of Existing Art	105
 CHAPTER 5	
<i>Conclusions</i>	<i>111</i>
5.1 Summary	111
5.2 Further Research	112

List of Tables

TABLE 1-1	System Requirements of Common Radio Standards	10
TABLE 1-2	Phase Noise Requirements of other Non-Telephony Radios . .	11
TABLE 3-1	Feedback ratio versus Capacitor ratio	70
TABLE 3-2	Phase noise versus size of Q1 and Q2	86
TABLE 4-1	Capacitor and feedback ratios of experimental prototypes. . .	91
TABLE 4-2	State of the Art Integrated VCO Performance	107

List of Figures

FIGURE 1-1	Superheterodyne or Direct Conversion Receiver	6
FIGURE 1-2	Oscillator Phase Noise	8
FIGURE 1-3	Reciprocal Mixing of Phase Noise Sideband with Adjacent Channel	9
FIGURE 1-4	Balanced Ring Oscillator	12
FIGURE 2-1	BJT small signal equivalent circuit with noise sources	20
FIGURE 2-2	Leeson's Model	23
FIGURE 2-3	Spectrum of Leeson/Scherer Equation	24
FIGURE 2-4	Linear and Nonlinear Contributions to Phase Noise at Offset Δf	28
FIGURE 2-5	Ideal LC Tank	30
FIGURE 2-6	Impulse Injected at Maximum Tank Voltage	31
FIGURE 2-7	Impulse Injected at Zero Tank Voltage	31
FIGURE 2-8	Phase Impulse Response	39
FIGURE 2-9	Conversion of noise source to phase noise sideband	42
FIGURE 3-1	Conventional LC Oscillator Topologies	51
FIGURE 3-2	Possible Configurations of the Colpitts Oscillator	53
FIGURE 3-3	Common Collector Colpitts with Collector Load	55
FIGURE 3-4	Common Collector Oscillator Analysis	57
FIGURE 3-5	Coplanar Spiral Inductor Quality Factor versus Frequency for 4.8nH	60
FIGURE 3-6	Peak Quality Factor versus Inductance	60
FIGURE 3-7	Imaginary and Real components of Z_{in}	61
FIGURE 3-8	The Making of a Balanced Common Collector Colpitts Circuit	63
FIGURE 3-9	Balanced VCO Schematic	63
FIGURE 3-10	More Detailed VCO Schematic	64
FIGURE 3-11	Double Π model of 4.8nH inductor in Nortel's 0.8 μ m Process	66
FIGURE 3-12	VCO Test Setup	67
FIGURE 3-13	Phase Noise and Tank Voltage versus Feedback Ratio for constant frequency and bias current	71
FIGURE 3-14	Phase Noise and Restoring Current versus Feedback Ratio for constant frequency and bias current	72
FIGURE 3-15	Total output noise versus feedback ratio	73
FIGURE 3-16	Top four phase noise contributors versus feedback ratio	74
FIGURE 3-17	Shot Noise and Thermal Noise of Resonator by Percentage of Contribution	75
FIGURE 3-18	Phase Noise at 100kHz Offset Versus Bias Current for Various Feedback Ratios	77

FIGURE 3-19	Phase Noise @100kHz Offset versus Bias Current for Feedback Ratio of 0.32	78
FIGURE 3-20	Output Noise and Tank Voltage versus Bias Current for Feedback Factor of 0.32	79
FIGURE 3-21	Output Noise Versus Bias Current for Feedback Ratio of 0.32.	79
FIGURE 3-22	Phase Noise and Oscillation Frequency Versus Bias Current for Feedback Ratio of 0.32	81
FIGURE 3-23	Oscillation Frequency Versus Bias Current for Various Feedback Ratios	81
FIGURE 3-24	Phase Noise with supply voltages of 2.5V, 3V and 5V	82
FIGURE 3-25	VCO Schematic with RF Chokes	83
FIGURE 3-26	Phase Noise Performance for 3V supply with and without RF Chokes	84
FIGURE 3-27	Oscillation Frequency and Phase Noise Versus Control Voltage	87
FIGURE 3-28	Increased tuning range with maximum size varactor	88
FIGURE 3-29	Phase noise degradation due to increased tuning range	89
FIGURE 4-1	Circuit layouts of the oscillators with four different capacitor ratios.	92
FIGURE 4-2	Measured Phase Noise versus Bias Current for the Four Feedback Factors	93
FIGURE 4-3	Measured and Simulation Phase Noise Data versus Bias Current	95
FIGURE 4-4	Oscillation Frequency Measurements versus Bias Current for the Four Capacitor Ratios	96
FIGURE 4-5	Measured and Simulated Oscillation Frequency versus Bias Current	96
FIGURE 4-6	Measured Spectrum of Oscillator	97
FIGURE 4-7	Phase Noise Sideband Measurement	98
FIGURE 4-8	Simulated and Measured Phase Noise Sidebands	99
FIGURE 4-9	Simulated and Measured Phase Noise Sidebands over 1 Decade	99
FIGURE 4-10	Measured Phase Noise Performance Versus Voltage Supply and with RF Choke	100
FIGURE 4-11	Measured and Simulated Phase Noise Performance versus Tuning Voltage	101
FIGURE 4-12	Measured and Simulated Oscillation Frequency versus Tuning Voltage	102
FIGURE 4-13	Figure of Merit of State of the Art VCOs	108
FIGURE 4-14	FOMQ of State of the Art VCOs	108

Glossary of Terms

AC.....	Alternating Current
AM	Amplitude Modulation
BER.....	Bit Error Rate
BiCMOS	Bipolar Complementary Metal Oxide over Semiconductor
BJT	Bipolar Junction Transistor
CML	Current Mode Logic
DC.....	Direct Current
DECT	Digital European Cordless Telephone
ECL.....	Emitter Coupled Logic
FDMA.....	Frequency Division Multiplex Access
GaAs	Gallium Arsenide
GPS.....	Global Positioning System
IF.....	Intermediate Frequency
ISF.....	Impulse Sensitivity Function
JFET	Junction Field Effect Transistor
LNA	Low Noise Amplifier
LO.....	Local Oscillator
LTI.....	Linear Time Invariant
LTV.....	Linear Time Variant
MESFET.....	Metal Semiconductor Field Effect Transistor
MOSFET.....	Metal Oxide Semiconductor Field Effect Transistor
NF.....	Noise Figure
PM.....	Phase Modulation
Q	Quality Factor
RF.....	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
RMS	Root Mean Squared
SONET	Synchronous Optical Network
SNR.....	Signal to Noise Ratio
VCO	Voltage Controlled Oscillator
WLAN	Wireless Local Area Network
xDSL.....	Digital Subscriber Line (Generic)

An oscillator is an important component which is employed in any type of system that requires a time or frequency reference. Electronic oscillators were developed for use in communication circuits shortly after Marconi transmitted the first electromagnetic encoded messages across the Atlantic Ocean in 1901. Marconi's first transmission sent broadband spark gap signals over a wireless channel. It was soon discovered that this type of communication link would not work in the presence of another transmitter and that narrowband signals would be required to allow multiple receivers/channels. This is what we now refer to as frequency division multiplexing (FDMA). FDMA was made possible by the development of the oscillator by Edwin Armstrong in 1913, who discovered the effect of positive feedback [Hag96].

Since Armstrong's discovery the development of data communications and telecommunications has grown exponentially. In fact, it has been speculated that the era of explosive growth for the personal computer is over. The computing power of today's personal computer is no longer the bottleneck in user perceived performance. The bottleneck has now shifted outside the computer to the network connecting one computer to another. In the same way that personal computers replaced mainframe computers as the dominant technology, networking technology will replace personal computers. As well the consumer market has demanded that data communication and telecommunication services be obtained on the same terminal over either a wireless or wireline medium. Both wireless

and wireline applications require high performance fully integrated solutions in order to maintain pace with this explosive market and to press the already thin price and performance margins to their absolute limit. The requirement for the transmission of digitized data has created a tremendous competition in industry for any advantage in the electronic communication sector.

The staggering growth of requirements for the transmission of digitized information can be divided into wireless applications and wireline applications. Wireline refers to the transmission of data, video or voice over a medium such as coaxial cable, twisted pair (xDSL), and fibre optic cable (SONET) and is associated with both telecommunication networks (i.e. the telephone) and data communication networks (i.e. the internet). In wireline transmission the data does not normally share the frequency spectrum with other channels or interferers and so it is known as broadband communication. Some notable exceptions to this are cable tuners and home networking which are wireline applications which share the frequency spectrum and employ FDMA to provide multiple channels. The emphasis for wireline data communications is to achieve high data transmission rates, make them faster and maintain their robustness to errors.

In contrast, wireless transmission must share the frequency spectrum with other transmitters, channels, interferers, and atmospheric noise. Thus wireless channels are specified to use a limited or comparatively narrow bandwidth for data transmission, which limits the maximum data rate as proven by Claude Shannon's channel capacity theorem. Wireless applications include cellular telephones, cordless telephones, global positioning systems (GPS), and wireless local area networks (WLAN). Benefits of wireless systems include portability and the low cost of installing infrastructure. Wireless data links have been mainly used for telecommunication, but demand from the consumer market is driving the growth of portable data communication and networking. In fact, wireless LAN products are projected to be the largest growth market in 2003 [Ele03]. The development

thrust in wireless terminals is on improved portability and higher data rates. The ultimate wireless terminal is physically small, lightweight, inexpensive, provides a long operating time, has a long transmission range, is reliable and robust to the presence of other wireless terminals and is capable of adapting to multiple standard protocols. These requirements point to an efficient, fully integrated radio design which consumes minimal power from a single low voltage rechargeable battery supply. However, fully monolithic transceivers for either wireless or wireline applications have proven difficult to realize. One component in particular that has been difficult to fully integrate is a low phase noise voltage controlled oscillator, which is a component common to both wireless and wireline transceivers.

A key performance index for any oscillator is its signal to noise ratio (SNR). In wireless applications, where the terminal is in the presence of interferers (other terminals or base stations), the oscillator is used as a frequency reference. Therefore, the spectral purity is of importance and the required SNR is specified in the frequency domain as an oscillator phase noise specification. In contrast, wireline applications employ oscillators as a time reference for the task of clock recovery and specify the SNR requirement in the time domain as a clock jitter specification. Both of these SNR requirements are affected by the same noise sources. However, the dominant noise source for jitter and phase noise can be different. This thesis will only focus on achieving low phase noise performance in oscillators for a wide variety of applications. In general, oscillator topologies with very good phase noise performance also achieve low jitter performance for wireline applications.

1.1 The Challenge

The focus of this research has been to study the design issues of monolithic oscillators, and to develop an monolithic voltage controlled oscillator with low phase noise performance that may be used as a building block for a variety of applications. The intent

of the work is to gain a better understanding of the low phase noise oscillator design and possible design trade-offs through an exploration of the available design space.

This work is also applicable to wireline applications. Wireline applications specify clock jitter as an important system requirement which is the time domain equivalent of oscillator phase noise. The requirements of wireline applications can be as severe as wireless application in terms of power consumption and low supply voltage because many transmitter or receivers may be integrated into a single integrated circuit.

Until recently, oscillator circuits were only integrated for relatively low frequency and high phase noise tolerant applications. More commonly, both wireless and wireline applications employed discrete devices and off-chip high quality factor passive components to achieve the required performance. Achieving low phase noise performance at frequencies over 1 Gigahertz has been difficult for a number of reasons. The basic problem is that phase noise performance is inversely proportional to the voltage controlled oscillator's (VCO) fundamental frequency. Higher frequencies oscillations require more power consumption and are noisier than at lower frequencies. In addition, the bandwidth performance of the active devices had been an obstacle, until the last few years when improvements in process technologies have resulted in dramatically increased device f_T . In fact, it is at the point now where the quality of the integrated passive components rather than the active components is generally the limitation in radio frequency integrated circuits (RFIC). One important difference between integrated and discrete solutions is that the quality factor (or Q) of the integrated passive components is about an order of magnitude poorer than their discrete brethren. The noise contributions associated with this lower Q can be the limiting factor for the phase noise performance, but the relative importance of various phase noise sources in a given design has not been well understood. Therefore, achieving the required performance in an integrated design with lower quality

passives will require a better understanding of the limitations of oscillator phase noise to minimize the noise contributions.

To this end, the advantages of integrated circuit design must be fully exploited to benefit a monolithic solution. A fully integrated transceiver can require less expensive packaging than a discrete/hybrid design and may have lower parasitic components allowing a higher frequency of operation since the parasitic components are less significant. One alternative to a fully integrated oscillator implementation is to use a multichip module which employs a flip chip package technique and a printed resonator. However, this solution is significantly more expensive than a fully integrated solution for large volume products [Dav98]. The lower cost packaging plus the lower component cost reduces the overall cost of a fully integrated solution. Another benefit of integrated circuits is the availability of matched balanced circuits which provide better on chip noise immunity to common noise sources. Balanced circuit can also provide larger differential voltage swings.

This work was targeted to use available bipolar junction transistor (BJT) technologies provided by the Technology Access and Applications Group at Nortel. Bipolar devices are known to be less noisy than either metal oxide semiconductor field effect transistor (MOSFET) devices or gallium arsenide (GaAs) metal semiconductor field effect transistor (MESFET) devices, which both have higher flicker noise corners that are characteristic of surface controlled devices. A high flicker noise corner dominates oscillator phase noise sidebands for frequencies close to the fundamental. Junction field effect transistor (JFET) devices, like BJTs, have a low flicker noise typical of buried channel devices and also have a high input impedance which would make them attractive for oscillator circuits. However, JFET devices are not widely available in commercial integrated processes because their process variation is difficult to control.

1.2 Digital Radio Receivers

FIGURE 1-1 Superheterodyne or Direct Conversion Receiver

Frequency conversion architectures, as shown for example in Figure 1.2, dominate present state-of-the-art digital radio designs even though they too were developed by Armstrong in 1920. The basic principle of frequency conversion is a nonlinear operation, namely the multiplication of two signals, such as the radio frequency (RF) signal and the local oscillator (LO) signal above. Such multiplication in its simplest form is illustrated by the trigonometric function given in (1-1), where f is the frequency of the respective signals.

$$\begin{aligned} \cos 2\pi f_{RF}t \cdot \cos 2\pi f_{LO}t &= \frac{1}{2} \cos 2\pi(f_{RF}t - f_{LO}t) \\ &\quad + \frac{1}{2} \cos 2\pi(f_{RF}t + f_{LO}t) \end{aligned} \quad (1-1)$$

The local oscillator (LO) function is generally realized by a frequency synthesizer which produces the LO frequency through a voltage controlled oscillator (VCO) locked to a crystal reference. The LO provides a frequency reference to the mixer which converts the radio frequency (RF) to an intermediate frequency (IF) corresponding to the sum and difference of the LO and RF frequencies. The mixer output is filtered to choose either the higher or lower frequency as the intermediate frequency. From the intermediate frequency further signal processing filters and demodulates the desired RF channel to provide the

digital data. The advantage of this architecture, over filtering and demodulating the RF signal directly, is that translating the desired RF signal to a lower frequency eases the signal processing requirements of the filters and demodulator. If an electronically tunable LO is employed (i.e. a voltage controlled oscillator), this system allows different channels to be translated to the same fixed IF signal path. Often radio designs employ multiple mixing stages to improve the rejection of unwanted signals. This same architecture can be used as either a superheterodyne or direct conversion radio. A large difference between the RF frequency and the LO frequency reduces the image rejection filter requirements for a superheterodyne receiver. In a direct conversion (or zero IF or homodyne) receiver, the LO frequency is equal to the desired RF frequency channel and an IF is produced at 0 Hz (DC). The benefit of the direct conversion receiver is that it does not have an image frequency and eases filtering constraints. However, if there is a slight frequency error between the RF frequency and the LO frequency, the IF signal will be corrupted by aliasing.

1.3 What is Phase Noise?

An ideal oscillator would be a component which would provide a periodic function with a desired frequency and amplitude. For example, the function of an ideal sine wave oscillator would be described by (1-2).

$$v(t) = A_o \cos(2\pi f_o t) \quad (1-2)$$

Since this fictitious component is the ideal reference its amplitude (A), frequency (ω), or phase (ϕ) do not vary over time, temperature, humidity, shock, vibration, power supply variation, load or any other process that can change the oscillator parameters. However, real components have either random or unwanted periodic noise which modulate the

properties of an oscillator circuit. A more realistic expression of a sine wave oscillator is defined in (1-3).

$$v_n(t) = [A_o + \varepsilon(t)] \cos[2\pi f_o t + \phi(t)] \quad (1-3)$$

This equation implies that oscillators are modulated by noise to produce amplitude modulation (AM) and phase modulation (PM). Due to their nonlinear behaviour, all electronic oscillators employ some type of amplitude limiting which suppresses the AM modulation term, $\varepsilon(t)$ to a large extent. If $\phi(t)$ is assumed to be a small-signal and Gaussian, the oscillator signal is phase modulated by this noise. This phase modulation produces noise skirts around the carrier frequency in the output spectrum where, instead of producing an ideal line spectrum, the energy is spread over a frequency range as shown in Figure .

FIGURE 1-2 Oscillator Phase Noise

These non-ideal noise skirts are known as the phase noise of the oscillator and are generally described as the power in a 1 Hz sideband at a specified offset frequency (f_m) relative to the power in the fundamental carrier (f_0). The oscillator phase noise is typically specified in units of decibels relative to the carrier power per Hertz (dBc/Hz).

1.3.1 Phase Noise Requirements for Radio Receivers

The focus on oscillator phase noise is due to the fact that the phase noise specification is often the most difficult requirement to meet for radio receivers. A disadvantage of both superheterodyne and direct conversion architectures is the reduction in the received SNR due to reciprocal mixing of an adjacent channel with the power of the phase noise sideband of the LO. Consider a superheterodyne receiver where an adjacent channel is being transmitted at a frequency offset f_m from the desired RF channel as shown in Figure . The adjacent channel mixes with the phase noise energy of the oscillator at an offset f_m , to mix to the same IF as the desired channel. This reduces the signal-to-noise ratio (SNR) and thus, the bit error rate (BER) performance of a digital radio receiver. The worst case situation is the minimum allowable desired RF signal in the presence of the maximum allowable adjacent RF channel signal.

FIGURE 1-3 Reciprocal Mixing of Phase Noise Sideband with Adjacent Channel

The phase noise requirements of each radio protocol are dependent on the required specifications such as channel separation, minimum sensitivity, and maximum output

power. The closer the adjacent channel is to the desired RF channel, the greater the reduction in the received SNR. Table 1-1 shows the requirements of various receiver types in order of increasing difficulty. The digital European cordless telephone (DECT) is the easiest protocol listed in Table 1-1 and demonstrates that cordless phone standards require less stringent phase noise requirements than cellular standards.

TABLE 1-1 System Requirements of Common Radio Standards

	DECT	CT-2	GSM	IS-54 (NADC)
Category	cordless	cordless	cellular	cellular
Access	TDMA/ FDMA/TDD	FDMA/TDD	TDMA/ FDMA/TDD	TDMA/ FDMA/TDD
RF Frequency	1.9 GHz	900 MHz	900 MHz	900 MHz
Number of RF Channels	10	40	124	833
Data Rate per RF Channel	1.152 Mb/sec	72 kb/sec	270.8 kb/sec	48kb/sec
Tuning Range	15.55 MHz	3.9 MHz	25 MHz	25 MHz
Channel Separation	1.728 MHz	10 kHz	200 kHz	30 kHz
Peak Power	250 mW	10 mW	3 W	3 W
Phase Noise dBc @ 100 kHz	-74	-105	-109	-125
Other Phase Noise Land- mark	-131 dBc/Hz @ 5.184 MHz	-125 dBc/Hz @ 1 MHz	-139 dBc/Hz @ 3 MHz	-145 dBc/Hz @ 1 MHz

In addition to wireless telephony, demand has grown for untethered communication to computers and peripherals. Table 1-2 highlights the VCO requirements for two of these radio standards [Sam02]. The transmission frequency of both of these applications is higher than the telephony requirements which adds to the challenge of the phase noise requirement.

TABLE 1-2 Phase Noise Requirements of other Non-Telephony Radios

Standard	Center Frequency (MHz)	Bandwidth	Phase Noise @ 3MHz (dBc/Hz)
Bluetooth	2440	3.3%	-119
WLAN	5250	5.7%	-116

1.3.2 Other VCO Requirements for Digital Radio

In addition to the phase noise requirements, the VCO must meet other requirements for digital radio applications. First and foremost is the frequency of oscillation. The oscillator must be capable of providing the required local oscillator frequency to mix the desired RF channel to the specified IF frequency. This requires a process technology that is capable of achieving an f_T and f_{MAX} of at least an order of magnitude above the required oscillation frequency.

The VCO must also provide an adequate output level to drive a double balanced mixer and the prescaler or divider of a frequency synthesizer. State of the art active mixers and frequency synthesizers require differential signals to improve their performance in the rejection of common mode noise and interference. A large local oscillator signal is required by the mixer to maximize its conversion gain, which directly affects the noise figure and performance of the receiver. Buffer stages may be used to boost the VCO output, but such stages should be minimized because they add to the noise floor as well as consume valuable current. A typical Gilbert cell mixer requires a local oscillator input of between -5 to 0 dBm to provide adequate noise figure performance for cordless telephone applications [Mac97]. A state of the art emitter coupled logic (ECL) or current mode logic (CML) based frequency synthesizer requires a differential local oscillator input with a swing of 200 mV [Bax96].

The VCO must also operate with a low voltage power consumption to meet the requirement of portability and to maximize the terminal's battery life. The battery cells are a significant percentage of the weight of portable terminals and a low voltage supply of 3 volts, or even 1.5 volts, would only require one or two battery cells to power the terminal. Keeping the current consumption low will increase the terminal operational battery life.

1.4 Classes of Oscillator Circuits

An oscillator is a circuit which uses positive feedback to store and dissipate energy as a periodic function. Electronic oscillators are classified as ring, relaxation, or resonator based circuits, which describes the basic oscillation mechanics of the circuits. Ring oscillators use a cascade of bistable circuits to produce an undefined state when an odd number of inverting stages are connected in a ring. The switching waveform propagates around the stages in the ring, thus the name. There must be an odd number of stages if single-ended circuits are used, whereas, any number of stages greater than two can be used for ring oscillators using balanced stages where the extra inversion can be realized for an even number of balanced stages by reversing the outputs of one stage as shown in Figure 1-4.

FIGURE 1-4 Balanced Ring Oscillator

Whereas the ring oscillator uses multiple stages to delay the switching waveform around the ring, the relaxation oscillator performs this function in a single stage by using an

energy storage component such as a capacitor or inductor. Using positive feedback an active circuit periodically charges and discharges energy from the energy storage device.

The resonator or harmonic oscillator takes the energy storage idea to another level, where a resonator device is used to store the energy. Common types of electronic resonators are an LC tank, a piezoelectric crystal, a surface acoustic wave device, a distributed transmission line, or a dielectric puck. When injected with an impulse of energy an ideal resonator will oscillate at a frequency dependent on its physical parameters. In the case of an ideal LC tank circuit, there is a energy exchange between the magnetic field of the inductor and the electric field of the capacitor. During oscillation, the current of the inductor injects charge on the capacitor which changes the voltage of the capacitor. The voltage of the capacitor is also across the inductor which changes the magnetic flux of the inductor and therefore its current.

The energy in an ideal resonator will be stored indefinitely, however, in real resonators the energy is dissipated gradually over time due to thermal losses. Positive feedback in an active circuit is used to compensate for the thermal losses of energy to maintain the level of oscillation. The storage of energy leads to a definition of how efficiently a component or circuit stores energy. This definition is named the quality factor or Q of the device as defined in (1-4).

$$Q = \omega \cdot \frac{\text{Peak Energy Stored}}{\text{Average Energy Dissipated}} \quad (1-4)$$

The phase noise of both ring and relaxation oscillators is relatively poor in comparison to resonator oscillators because all the energy is dissipated during each cycle. The high quality factor of resonator VCO's is the main reason for their low phase noise. The resonator's high Q means that very little energy is lost to thermal losses which means that the self-contained thermal noise of the resonator is minimal. The low phase noise also benefits from the fact that only minimal active circuitry is required to restore the energy

each cycle. The dominant limitation of realizing a VCO with an integrated resonator is that the Q of integrated resonator is very low. Therefore, the challenge is to better understand the mechanics of oscillator phase noise and develop integrated circuits which take advantage of this understanding to minimize the phase noise. All of these points will be expanded upon in subsequent chapters.

1.5 Contributions and Thesis Outline

The contribution of this work is to present a new balanced VCO design that can be realized as a monolithic solution for many types of applications. Theory, simulations, and experiments will demonstrate how to optimize the circuit for the phase noise performance versus power consumption. Also, the idea of a normalized figure of merit (FOM) is proposed to enable designers to compare the measured or simulated performance of different VCO architectures.

We must have a detailed understanding of oscillator phase noise and its properties to achieve the above goals. Only then will the designer be able to properly evaluate an oscillator circuit for its noise performance. Chapter 2 reviews noise and its applicability to oscillator performance. Existing methods of modeling oscillator phase noise are discussed along with comments to provide insights into minimizing oscillator phase noise.

Once the designer has an understanding of phase noise mechanics, this knowledge can then be applied along with intuitive circuit design skills to evaluate various circuit topologies to choose an oscillator circuit that exhibits low phase noise performance. Chapter 3 details the oscillator operation and analyzes common oscillator circuits. Various analysis methods are reviewed as they apply to oscillator circuit design. This chapter also reviews some of the methods used to simulate oscillator phase noise including the details of analyzing an oscillator with a controversial linear time variant phase noise method

based on Green's Function Method, the Hajimiri Method. This method is included for the insight it gives into the complex problem of predicting phase noise, although other insights are also presented.

Chapter 4 presents a new balanced oscillator topology based on insights gained in previous chapters. Simulations and experimental measurements of this circuit are discussed and compared to present state of the art circuits. Conclusions and recommendations for further research conclude the thesis in Chapter 5.

Oscillator design has been going through a tumultuous period in the past ten years as a result of the explosion of interest in developing monolithic radio transceivers. When the research for this thesis had begun the traditional method of discrete oscillator design was referred to as "black magic" to the uninitiated. Of course, to experienced RF designers, oscillator design is not magic but a significant amount of time and experience spent on trial and error in building oscillators, measuring their performance, and observing trends in performance. This design methodology did not rely on computer simulation but relentless prototyping. Often the discrete design did not have to be optimized to achieve the required phase noise performance because of the high quality factor of available discrete resonators. This type of design methodology, at the discrete level but especially at the integrated level, requires a great deal of fine tuning, time and "tweaking" of components and the design. While this is a viable solution for hybrid or discrete realizations, however, integrated circuit technologies have fabrication times measured in months and do not have the luxury of having extremely high quality components. Integrated inductor quality factor is on the order of 5 to 10 as opposed to 50 to 200 for discrete components. The quality factor of passive components can roughly be related to area since a large storage device can store more energy and, if designed correctly, will only dissipate a very small fraction of the energy stored [Lar98]. The design of high

performance integrated VCO's requires getting the absolute most from the low quality components, and therefore it is essential that the design be optimized for performance.

The importance of oscillator phase noise for radio receiver performance was stated in the previous chapter. The ability to design circuits which meet the required performance is based on the presumption that mathematical models which predict the circuit performance are available. This chapter reviews existing theories, models and definitions of oscillator phase noise, as well as the behaviour of linear time varying systems.

2.1 Device Noise Sources

The mechanics of oscillator phase noise can be attributed to the frequency conversion property of nonlinear or linear time varying systems [Car90, DeS97, Haj98]. The power spectral density of each noise source is frequency translated to produce an unwanted noise close to the fundamental oscillation frequency. Before looking at the existing models for the mechanics of oscillator phase noise, the sources of noise must be fully understood.

Practical passive and active components generate noise and may be modeled as lumped or distributed noise sources. The three types of device noise that are important to bipolar circuit design are thermal noise, shot noise, and flicker noise. MOSFET and MESFET devices are similar except that they have a channel noise source rather than a shot noise source.

Thermal noise is related to the random thermal motion of electrons and its power spectral density is directly proportional to temperature and an equivalent resistance. All practical devices, passive or active, have a thermal noise component which can be modeled as either a current or voltage source (2-1).

$$\overline{i_n^2(t)} = \frac{4kT}{R}\Delta f \quad \text{or} \quad \overline{v_n^2(t)} = 4kTR\Delta f \quad (2-1)$$

Shot noise is associated with the fluctuation of carriers across a PN junction and is based on Poisson's probability density function [Pap91]. Shot noise sources are found in diodes and bipolar transistors and their power spectral density is directly proportional to the current flowing through the PN junction (2-2) [Mas93].

$$\overline{i_n^2(t)} = 2qi(t)\Delta f \quad (2-2)$$

Flicker noise, or 1/f noise, is found in all active devices as well as some types of passive devices. The origin of flicker noise is not well understood and it is difficult to measure or model accurately. Flicker noise is related to the direct current (DC) of the device and its power spectral density is inversely proportional to frequency (2-3). In fact, it is generally not well characterized for integrated circuit processes, if it is even modeled at all. The model is based on an empirical model rather than on a physical based model [Mas93]. This is unfortunate because flicker noise is the limiting factor in the SNR for low frequency designs as well as in-close phase noise of oscillators. The $1/f^3$ slope in the phase noise skirts of Figure is due entirely to 1/f noise [Ven90].

$$\overline{i_n^2(t)} = k_f \frac{I_f^{a_f}}{f^b} \Delta f \quad (2-3)$$

A white stationary noise source is defined as a random process whose statistical characteristics remain invariant over time and whose power spectral density is equal at all

frequencies. Thermal noise can be considered a white stationary process if the resistance and the temperature remain constant with time. This can also be said for shot noise, if the current across the pn junction remains constant with time. Flicker noise is stationary if the DC current of the device is constant over time but it is not white because the power spectral density varies with frequency. Flicker noise is also referred to as pink noise which is an analogy to an optical system which reddens white light due to higher energy at the lower visible frequencies [Lee98].

If the statistical characteristics of a noise source vary periodically with time, then this source is referred to as cyclostationary. A cyclostationary noise source can be decomposed into the product of a white stationary noise and a periodic scaling function with a maximum value of unity as shown in (2-4).

$$i_n(t) = i_{n0}(t) \cdot \alpha(\omega_0 t) \quad (2-4)$$

Therefore,

$$\overline{i_n^2(t)} = \overline{i_{n0}^2(t)} \cdot \alpha^2(\omega_0 t) \quad (2-5)$$

By definition, $\overline{i_{n0}^2(t)}$ is equal to the maximum mean square noise power of $\overline{i_n^2(t)}$. Cyclostationary noise models are required for the types of sources mentioned above when their statistical noise properties vary periodically with time. For example, if the current across the pn junction of a bipolar device varies periodically, both the shot noise and the flicker noise are cyclostationary sources.

FIGURE 2-1 BJT small signal equivalent circuit with noise sources

Figure shows a bipolar transistor small signal equivalent circuit where the various current generators (except $g_m V_{BE}$) describe the noise sources discussed above [Mas93].

2.2 Circuit Noise Mechanisms

In addition to device noise sources there are mechanisms within the circuit that need to be understood and minimized. One source of phase noise is a circuit mechanism which converts amplitude modulation (AM) noise to phase modulation (PM) noise. The transfer function of these mechanisms is referred to as the AM to PM sensitivity or $K_{AM \rightarrow PM}$. This sensitivity is usually specified in units of Megahertz/Volt (MHz/V). For example, a voltage or current perturbation in the circuit caused by a noise source may modulate the capacitance, inductance, or resistance of the loaded tank circuit of the oscillator during the period of oscillation, which will in turn modulate the instantaneous frequency of the oscillator. Therefore the result is an AM modulation being converted to phase noise. Probably the most well known AM to PM sensitivity of the VCO is K_{VCO} which describes

the transfer function of the control voltage to the oscillator frequency. The control voltage is used to tune the VCO frequency and K_{VCO} is dependent on the tuning range of the VCO. K_{VCO} can be one of the dominant noise sources in a VCO [Rog00]. The range of K_{VCO} can vary from less than 10 MHz/V to more than 100 MHz/V and is a function of the VCO tuning range. Ring oscillators have the widest tuning ranges and, therefore, the largest control voltage sensitivities, whereas, resonator based oscillators have the narrowest tuning ranges and the lowest K_{VCO} . One way to minimize this noise mechanism is to design the VCO with the narrowest tuning range that still meets the application requirement and to minimize the device noise sources that drive the VCO control voltage. Other techniques include differential varactors [Fon02a], multi-band frequency ranges [Fon02b], and employing complementary process (e.g. CMOS) [Fon02c].

Another class of noise mechanisms that is challenging to model and often overlooked is coupled interference. Examples of these mechanisms include power supply coupling, DC bias coupling, and substrate coupling from other circuits or noise sources. These noise sources can vary widely from white stationary random noise to discrete spurious tones.

Spurious tones can be modeled in the form of (2-6).

$$i_n(t) = I_0 \cos(\omega_n t) \quad (2-6)$$

The strategy for minimizing these noise mechanisms is to reduce the coupling to the noise source. This may mean improving the power supply rejection ratio (PSRR), minimizing current mirror ratios, or shielding the substrate with guard rings.

2.3 Linear Time Invariant Noise Model

Leeson published the first paper which modeled oscillator phase noise and provided some empirical insight into the design of low phase noise oscillators [Lee66]. This model has been the basis for a number of subsequent oscillator phase noise models, which have added subtle extensions or modifications to account for higher order effects [Rob82, Cra95, Boo89, Jan97]. Leeson's equation (2-7) is based on linear assumptions and models the oscillator as feedback loop consisting of a linear amplifier with a resonant tank circuit in the feedback path as shown in Figure . $\mathcal{L}(f_m)$ is the phase noise at the output, in units of dBc/Hz. In the figure, β is the transfer function of the resonator and A is the assumed linear amplifier.

$$\mathcal{L}(f_m) = 10 \cdot \log \left[\frac{FkT}{2P_0} \left(1 + \left(\frac{f_0}{2Q_L f_m} \right)^2 \right) \right] \quad (2-7)$$

where,

F = active device noise factor

k = Boltzmann constant

T = temperature (K)

P_0 = output power (W)

f_0 = oscillator center frequency (Hz)

Q_L = loaded resonator quality factor

f_m = frequency offset from carrier (Hz)

FIGURE 2-2 Leeson's Model

This model assumes that the model meets the Barkhausen criterion, where the open loop gain is equal to unity and the open phase response is 0 degrees, both at the resonant frequency. In this model, the amplifier accounts for any losses in the resonant tank circuit to make the open loop gain unity.

Leeson's equation was developed from empirical measurements of oscillator phase noise and is based on *a posteriori* data fitting. Scherer modified Leeson's equation to account for the appearance of flicker noise which is shown in (2-8) below [Sch79].

$$\mathcal{L}(f_m) = 10 \log \left[\frac{FkT}{2P_0} \left(1 + \left(\frac{f_0}{2Q_L f_m} \right)^2 \right) \left(1 + \frac{f_c}{f_m} \right) \right] \quad (2-8)$$

The model of the Leeson/Scherer equation was developed from empirical measurements of oscillator phase noise and is also based on *a posteriori* data fitting. It assumes that phase noise of an oscillator can be approximated by the three piecewise linear sections shown in the graph below. Figure plots the Leeson/Scherer equation for the low Q case where $f_c < f_0/(2Q_L)$. For the high Q case $f_c > f_0/(2Q_L)$, the slope of the second linear section in Figure 2-3 would be $1/f$ instead of $1/f^2$.

The model predicts a noise floor which relates the noise from all sources in the circuit (FkT) to the carrier power (P_0). The noise factor F is an empirical scaling factor used to fit

the measured noise floor to the model. The noise floor also includes a factor of $1/2$ to reflect the prediction of Boltzmann's equipartition theorem, which assumes that the noise is equally divided between phase and amplitude contributions [Fey63].

Leeson's equation assumes that the phase noise intersects the noise floor at an offset frequency of $f_0/(2Q_L)$ and that the $1/f^3$ phase noise corner frequency corresponds to the device flicker noise corner frequency. It has been proposed that neither of these two assumptions has any theoretical basis [Lee98].

FIGURE 2-3 Spectrum of Leeson/Scherer Equation

Although Leeson initially developed his linear model empirically, others have shown that it is possible to determine the oscillator noise factor [Rog00]. Despite the empirical origin of Leeson's equation, it does predict some basic design issues of low phase noise oscillators. The model indicates that to minimize phase noise the signal magnitude of the oscillator should be maximized (P_0) and the loaded quality factor of the resonator be maximized (Q_L). Loaded quality factor is defined as the quality factor of the resonator as it is loaded by the circuit rather than the resonator in isolation. The dominant load of the resonator is the active device which provides the restoring energy to the tank but it may also include other loads such as DC bias circuits. It also suggests that the contribution of

the active devices (F) be minimized. However, the model does not indicate how to optimize any of these parameters. In particular, the noise factor (F) is not due to one device but the combination of all devices in the circuit and will change with choice of oscillator topology. An intuitive approach would include starting with the highest quality passive components, and maximizing the fundamental frequency component. However, this cannot be achieved at the cost of increasing the noise of active components because a high fundamental component means higher harmonics, and any harmonics allow more noise sources to mix near the fundamental. Ultimately this model is of limited use except to estimate how phase noise performance scales with its parameters to compare oscillator measurements.

2.4 The Nonlinear Mechanisms of Phase Noise Sidebands

Empirical development, intuition, and experience can only provide a limited amount of insight into low phase noise oscillator design. An accurate model is required in order to accurately compare oscillator circuit topologies or to optimize a circuit for low phase noise. As discussed in the section above, a linear time invariant model cannot accurately model the behaviour of oscillator phase noise.

There is one commonality to the many theories of how phase noise sidebands are generated in oscillator circuits. Basically noise power from an infinite number of frequencies is converted to the oscillator output at the offset frequency of interest. Either the noise source is corrupting the node of interest directly or is coupled through the circuit transfer function with an associated gain or attenuation. One easily identifiable contribution is the noise power which is already existing at that frequency. This source is referred to as the linear noise source since it can be explained by linear transfer theory.

Other noise sources arise at other frequencies and are frequency converted. One theory suggests that device nonlinearities are an obvious method of frequency conversion, where the nonlinearity can be approximated by the following power series (2-9), where $I(t)$ is the current through the nonlinear element, and $V(t)$ is the voltage across it.

$$I(t) = aV(t) + bV^2(t) + cV^3(t) + \dots \quad (2-9)$$

If we neglect the DC bias terms, and assume the independent signal is

$$V(t) = V_1 \cos(\omega_1 t) + V_2 \cos(\omega_2 t) \quad (2-10)$$

the first term of (2-9) becomes

$$aV(t) = aV_1 \cos(\omega_1 t) + aV_2 \cos(\omega_2 t) \quad (2-11)$$

and the second term of (2-9) becomes

$$\begin{aligned} bV^2(t) = & \frac{b}{2}[V_1^2 + V_2^2 + V_1^2 \cos(2\omega_1 t) + V_2^2 \cos(2\omega_2 t) \\ & + 2V_1 V_2 [\cos((\omega_1 + \omega_2)t) + \cos((\omega_1 - \omega_2)t)]] \end{aligned} \quad (2-12)$$

(2-12) shows the second order intermodulation terms, which produce the new frequencies $2\omega_1$, $2\omega_2$, $\omega_1 + \omega_2$, and $\omega_1 - \omega_2$. There is also a DC bias shift from the second order nonlinearity, which changes the operating point of the device. In a practical oscillator circuit this bias shift moves the operating point which helps to reduce the device gain to meet the Barkhausen criterion [Smi86]. That is, it reduces the loop gain to unity so that the oscillator amplitude stops growing.

The third term of (2-9) becomes

$$\begin{aligned}
cV^3(t) = & \frac{c}{2}(V_1^3 \cos(3\omega_1 t) + V_2^3 \cos(3\omega_2 t)) \\
& + 3V_1^2 V_2 [\cos((2\omega_1 + \omega_2)t) + \cos((2\omega_1 - \omega_2)t)] \\
& + 3V_1 V_2^2 [\cos((2\omega_2 + \omega_1)t) + \cos((2\omega_2 - \omega_1)t)] \\
& + 3(V_1^3 + 2V_1 V_2^2) \cos(\omega_1 t) \\
& + 3(V_2^3 + 2V_1^2 V_2) \cos(\omega_2 t)
\end{aligned}
\tag{2-13}$$

(2-13) shows the third order intermodulation terms, which produce the new frequencies $3\omega_1$, $3\omega_2$, $2\omega_1 + \omega_2$, $2\omega_1 - \omega_2$, $2\omega_2 + \omega_1$, and $2\omega_2 - \omega_1$. The third order nonlinearity also produces fundamental frequency terms which have the effect of reducing the amplitude of the fundamental.

2.4.1 Transient/Fourier Analysis of Phase Noise

The overall effect of the device nonlinearity for an oscillator circuit is that the active device behaves as a mixer which converts noise power from different frequencies to the frequency of interest, offset from the fundamental as shown in Figure . The mixing coefficients or conversion gain of the noise power or spurious tones is dependent on the nodal transfer function or circuit topology. This means that different noise sources will have different mixing coefficients. Leeson's model disregards this mechanism and tries to lump all the individual mixing coefficients into the noise factor term, F. Therefore, even if the Leeson's noise factor was derived, it would only be valid for a single topology at a single biasing condition.

FIGURE 2-4 Linear and Nonlinear Contributions to Phase Noise at Offset Δf

Another evolution in modeling the phase noise of an oscillator uses the above knowledge and a nonlinear simulator. The linear and nonlinear behaviour of the oscillator circuit is accurately modeled in the nonlinear transient analysis of a SPICE-type simulator. This simulator analysis has been used as the basis for the phase noise simulation of oscillator circuits as reported in references [Raz96] and [DeS97]. Both of these methods each model a noise source as a sinusoid at a frequency of interest with an the amplitude representing the root mean squared (RMS) value of the power spectral density of the corresponding source. A sinusoid is used because pseudo random noise is very difficult to model properly in the time domain and it would also require extremely long simulation times. A nonlinear time domain simulation is then computed by SPICE and the output of the oscillator is Fourier transformed. The carrier to sideband power ratio shows the contribution of that particular noise source at that frequency. Due to the small amplitudes of noise sources and the finite resolution of discrete Fourier transforms, the sinusoidal noise sources may be scaled if linearity is maintained. The mixing coefficient becomes nonlinear as the noise sinusoidal signal representing the noise source is increased. The method explained in reference [Des97] computes the contributions of all noise sources using multiple sources with one simulation but requires an extremely careful choice of noise source frequencies and simulation time step.

The disadvantage of both of these methods results when all of the circuit noise sources cannot be represented by stationary power spectral densities or spurious signals. Bipolar devices contain cyclostationary noise sources which would be very difficult to model with a sinusoid source because the mean squared value of the noise has to change with time. A possible solution would be to amplitude modulate the sinusoid source with the same periodicity of the cyclostationary source. However, the phase of the modulation must correspond exactly with the phase of the cyclostationary source. This phase alignment would be extremely difficult to control in an oscillator time domain simulation where the time to steady state operation is a function of many circuit parameters.

On a final note, this method is useful for benchmarking other simulation models and measurements. It is also useful for ring oscillators where the cyclostationary noise behaviour is not dominant [Haj98].

2.5 Linear Time Varying Phase Noise Theory and Linear LC Oscillators

Leeson's equation and its amendments provide a general system level of insight into the phase noise behaviour of oscillators. However, additional analysis is required to gain insight into the actual mechanics of oscillator phase noise. The linear model discussed in Section 2.3 does not identify the contributions due to the various noise sources to the overall phase noise of the oscillator. The fundamental problem with a linear time invariant (LTI) system is that it cannot properly model the mechanics of noise conversion because practical oscillators are inherently nonlinear [Car90]. In other words, an LTI system cannot produce new frequencies different from the input signal. Recently, a linear time variant (LTV) model for oscillator phase noise was proposed by Hajimiri [Haj98, Lee98]. In contrast to a LTI system, the LTV system may produce new frequencies and provides a more complete model of the frequency translation of noise in oscillators. This theory

converges with other proposed theories [DeS97, Rav96] on the mechanics of how noise sources can be frequency translated about the fundamental to produce oscillator phase noise. Before describing Hajimiri's general method of determining oscillator phase noise, it is useful to fully understand the underlying principles behind this method.

The fundamental basis of the LTV model is that the response of an oscillator to noise is time varying. This can be demonstrated by considering a simulation of an ideal parallel LC tank circuit shown in Figure . The simulation values of the inductor and capacitor are 5 nH and 5 pF, respectively. The circuit is injected with an initial energy impulse to cause the circuit to oscillate with a constant steady state amplitude. A noise source, modeled as a random impulse of nodal current, is injected in parallel with the tank circuit at time τ . If τ corresponds to when the tank voltage is at a maximum, the amplitude of the oscillation is changed but the signal phase is unchanged (Figure). However, if the “noise” impulse corresponds to a tank voltage of zero, the amplitude is unchanged but the phase is shifted (Figure). Current impulses at other points in the waveform produce both amplitude and phase changes. This simulation clearly indicates that a linear LC circuit has a time varying impulse response when just amplitude or phase is being observed.

FIGURE 2-5 Ideal LC Tank

FIGURE 2-6 Impulse Injected at Maximum Tank Voltage

FIGURE 2-7 Impulse Injected at Zero Tank Voltage

It can be shown that the maximum phase and minimum amplitude shift occur when the tank voltage is zero, and the minimum phase and maximum amplitude shift occur when

the tank voltage is maximum. A similar demonstration can be stated for injecting flux in series with the inductor and observing the changes relative to the inductor current waveform.

In contrast, a passive LC resonant circuit is linear time invariant if the initial conditions are zero. That is, if there is no flux or charge stored in the tank circuit, the impulse response of an LC resonant circuit is linear time invariant. However, if initially there is flux or charge stored in the LC tank circuit then the impulse response is linear time variant, because the previous unperturbed oscillation serves as a fixed reference which makes the phase or amplitude response relative to this reference time varying.

Further insight into the time varying behaviour of the LC tank is gained by considering the differential equation of this circuit, given in (2-14).

$$C \frac{dV}{dt} + \frac{1}{L} \int V dt = \Delta q \cdot \delta(t) \quad (2-14)$$

where Δq is the amount of charge injected during the impulse which is given by (2-15),

$$\Delta q = \int i_n(t) dt \quad (2-15)$$

Setting $\omega_0^2 = 1/(LC)$, (2-14) becomes

$$\frac{dV}{dt} + \omega_0^2 \int V dt = \frac{\Delta q}{C} \cdot \delta(t) \quad (2-16)$$

There is also a relationship between the magnetic flux of the inductor and the tank voltage which is given by the following equations, where Φ is defined as the total linked flux. That is, if the inductor has N turns, the actual physical flux is multiplied by N:

$$\Phi = \int V dt \quad (2-17)$$

$$\Phi' = \frac{d\Phi}{dt} = V \quad (2-18)$$

$$\Phi'' = \frac{d^2\Phi}{dt^2} = \frac{dV}{dt} \quad (2-19)$$

Therefore, (2-16) can be rewritten as

$$\frac{d^2\Phi}{dt^2} + \omega_0^2\Phi = \frac{\Delta q}{C} \cdot \delta(t) \quad (2-20)$$

Taking the Laplace transform of (2-20) gives (2-21). Observe the initial conditions of (2-21)!

$$s^2\mathcal{L}\{\Phi\} - s\Phi(0) - \Phi'(0) + \omega_0^2\mathcal{L}\{\Phi\} = \frac{\Delta q}{C} \cdot \mathcal{L}\{\delta(t)\} \quad (2-21)$$

Solving for $\mathcal{L}\{\Phi\}$

$$\mathcal{L}\{\Phi\} = \left(\frac{s}{s^2 + \omega_0^2} \cdot \Phi(0) \right) + \left(\frac{\Phi'(0)}{\omega_0} \cdot \frac{\omega_0}{s^2 + \omega_0^2} \right) + \left(\frac{\Delta q}{C\omega_0} \cdot \frac{\omega_0}{s^2 + \omega_0^2} \right) \quad (2-22)$$

Taking the inverse Laplace transform of (2-22) gives

$$\Phi = \Phi(0)\cos\omega_0 t + \left(\frac{\Phi'(0)}{\omega_0} \sin\omega_0 t \right) + \left(\frac{\Delta q}{C\omega_0} \sin\omega_0 t \right) \quad (2-23)$$

Finally,

$$V(t) = \frac{d\Phi}{dt} = -\Phi(0)\omega_0 \sin\omega_0 t + \left(V(0) + \frac{\Delta q}{C} \right) \cos\omega_0 t \quad (2-24)$$

This shows that $V(t)$ consists of in-phase (I) and quadrature (Q) components whose coefficients are determined by the value of the tank voltage and the magnetic flux at the time of the current impulse. It also shows that the voltage at the time of impulse is stepped by $\Delta V = (\Delta q)/C$, which is expected for a capacitor.

If we set the initial conditions equal to zero then (2-24) produces (2-25)

$$V(t) = \left(\frac{\Delta q}{C} \right) \cos \omega_0 t \quad (2-25)$$

where the current impulse produces a sinusoidal waveform with the amplitude proportional to the charge injected and inversely proportional to the capacitance.

We will next consider cases when the initial conditions are not equal to zero. The function $V(\tau)$ is defined in terms of τ to show the relationship between the initial conditions $V(0)$ and $\Phi(0)$. If we let

$$V(\tau) = V_p \cdot \sin(\omega_0 \tau) \quad (2-26)$$

then (2-27) is produced from the relationship of (2-17)

$$\Phi(t) = -\frac{V_p \cos(\omega_0 \tau)}{\omega_0} \quad (2-27)$$

now,

$$V(t, \tau) = ((V_p \cos \omega_0 \tau) \cdot \sin \omega_0 t) + \left(V_p \sin \omega_0 \tau + \frac{\Delta q}{C} \right) \cos \omega_0 t \quad (2-28)$$

Therefore, when $V(\tau) = V_p$ (viz. $V(\tau)$ is maximum), $\Phi(\tau) = 0$ and (2-28) becomes,

$$V(t) = \left(V_p + \frac{\Delta q}{C} \right) \cos \omega_0 t \quad (2-29)$$

This shows that if the impulse is injected when the tank voltage is a maximum, then $V(t)$ will still be in phase with the signal before the impulse was applied but the amplitude will be changed by $(\Delta q)/C$. Therefore, there is no phase change in the signal for an impulse injected when the tank voltage is maximum as was demonstrated in Figure . Equation (2-29) also corresponds to the maximum amplitude change for (2-24).

When $V(0) = 0$, $\Phi(0) = -1/\omega_0$ and (2-28) becomes,

$$V(t) = (V_p \cdot \sin \omega_0 t) + \left(\frac{\Delta q}{C} \cdot \cos \omega_0 t \right) \quad (2-30)$$

The maximum excess phase shift ϕ between a nonimpulsed resonant tank and an impulsed resonant tank circuit occurs when (2-30) is set equal to zero and solved for $\omega_0 t$. Therefore,

$$\text{Max}|\phi| = \left| \tan^{-1} \left(\frac{-\Delta q}{V_p C} \right) \right| \cong \frac{\Delta q}{V_p C} = \frac{\Delta V}{V_p} = \frac{\Delta q}{q_{\max}} \quad (2-31)$$

From the expression above, some general insights which are similar to Leeson's model can be inferred into the phase noise of a linear LC tank circuit. The maximum excess phase is proportional to the magnitude of the noise sources and is inversely proportional to the fundamental oscillation level. The excess phase is also inversely proportional to the capacitance but if the same analysis is performed for a noise voltage in series with the inductor it will be found that the excess phase is inversely proportional to the inductance. Since $\omega_0 = 1/(\sqrt{LC})$, this indicates that the maximum excess phase must increase with frequency.

It may not seem obvious why only a phase change, without an amplitude change, would occur when the tank voltage is zero even though a “noise” current is being injected. However, since the tank voltage is zero there cannot be a net power or energy change, as can be seen from $\text{Power} = \text{Voltage} \times \text{Current} \cdot \cos \alpha$ which is in units of energy/time (where α is the phase angle between the voltage and the current). The injected current can only inject charge on the capacitor because the inductor will not allow an instantaneous current change. The greatest power/energy change is produced when the product of tank voltage and “noise” current are greatest.

The “noise” impulse current increases or decreases the charge on the capacitor depending on the direction of the current, where $\Delta Q = i \cdot \Delta t$. This charge impulse instantly changes the voltage of the capacitor, from the relationship $\Delta V = (\Delta Q)/C$.

Since the tank voltage is 90° out of phase with the inductor/capacitor current, the maximum tank voltage corresponds to zero inductor/capacitor current. When the impulse occurs at the maximum voltage, the charge impulse effectively gives the capacitor a “new” initial starting voltage or maximum voltage. The tank circuit then continues oscillating with the same phase except that the amplitude has been altered because the energy has changed, from the relationship $\text{Energy} = (1/2)CV_{Max}^2$.

2.5.1 The Ideal Oscillator

The previous section on linear time varying systems points to some important characteristics of the ideal oscillator. First and foremost is that the oscillator must store as much energy as possible in the resonator in either current in the inductor or voltage in the capacitor. All noise is related to the level of the fundamental so the larger the fundamental the better. Of course, this also means that the power consumption will increase. The nodal

voltages are limited by the supply voltage, the breakdown voltages of the device, device self-limiting and, in the case of bipolar devices, device saturation.

The resonator Q must be maximized which reduces the resonator noise floor and reduces the power consumption of the active device. The lower power consumption will also reduce the shot noise of the bipolar devices.

It was noted previously, that the maximum phase shift occurs when a “noise” impulse is injected when the tank voltage is zero. No phase shift occurs when the impulse is injected when the tank voltage is maximum. Therefore, in the ideal oscillator, the active devices should be dormant most of the time and only inject a restoring current (and noise) into the tank when the voltage is maximum [Lee98]. This corresponds to the device operating in class C mode which is characteristic of the Colpitts type oscillator discussed in the next chapter. Some references [Rhe90] state that the optimum phase noise is achieved by operating the devices in class A mode. This seems to be incorrect. Class A mode does lower the amount of mixing products but the amplitude of the oscillator is much smaller.

Ring oscillators exhibit the class C property, however the devices switch on and inject noise current at the zero crossing which is the worst possible time. This fact indicates one reason why ring oscillators have poorer phase noise performance than resonator oscillators.

The analysis above demonstrates that a noise source produces both an amplitude and a phase noise in a LTV system. However, a practical oscillator has a nonlinear active device in a positive feedback loop which maintains the amplitude of the oscillator either through device or supply self-limiting or automatic gain control (AGC). Therefore, it is assumed that the amplitude impulse response can be disregarded since a high performance oscillator will suppress amplitude modulations [Cra94]. This point also stresses the importance of using limiting amplifiers to buffer the output of the VCO.

Finally, the phase noise is directly proportional to the magnitude of the noise sources, which should be minimized. To achieve this, a noise analysis which can determine the contribution of each individual noise source is required. This would enable the designer to detect and minimize the dominant noise sources using a design methodology similar to LNA design.

2.5.2 The Hajimiri Method (Green's Function Method)

Although named Hajimiri's method by Lee [Lee98], this method is just the application of the well known Green's function method which was developed over 150 years ago [Fey63]. A Green's function is defined as the response of a linear system, including periodic linear time varying systems, to an impulse function. The method of analyzing the forced response of a linear system to a series of impulses is called the Green's function method. Hajimiri recognized that practical oscillator circuits have a time varying phase impulse response and that the phase response is linear if the impulse amplitude is small [Haj98]. He used the theory of Green's function method to define a model based on the LTV system, in which the oscillator is composed of an amplitude impulse response and a phase impulse response.

The boundary conditions employed in Hajimiri's method result in narrowband assumptions which restrict the method to only modeling close-in noise sidebands. This limitation must be strictly observed when analyzing oscillator circuits.

2.5.3 Details of Hajimiri's Method

The important details of Hajimiri's method will be reviewed in this section since this method is relatively new and some detailed understanding of the underlying assumptions is key to understanding its limitations.

The first assumption that this method makes is the amplitude impulse response of an oscillator can be disregarded because it is suppressed by the amplitude restoring function due to the nonlinearities of the active devices. The phase impulse response is modeled as a time varying function of τ as shown in Figure .

FIGURE 2-8 Phase Impulse Response

where,

$$h_{\phi}(t, \tau) \triangleq \frac{\Gamma(\omega_o \tau)}{q_{max}} u(t - \tau) \quad (2-32)$$

The term $\Gamma(\omega_o \tau)$ is defined as the impulse sensitivity function (ISF) and is a periodic function embedded in the nonlinear behaviour and the topology of the oscillator circuit. Hajimiri has chosen that the impulse function is scaled to q_{max} which gives the equation defined in (2-32) the units of Coulomb⁻¹.

The definition is based on simulations that Hajimiri performed which demonstrated that the phase impulse response is time varying and is approximately linearly proportional to the input signal as defined in (2-33) if the magnitude of the impulse is small enough.

$$\phi(t) \propto \frac{\Delta q}{q_{max}}. \quad (2-33)$$

However, it was also demonstrated in the previous section that for the ideal LC circuit

$$\phi(t) \propto \frac{\Delta q}{CV_p} = \frac{\Delta V}{V_p} = \frac{\Delta q}{q_{max}} \quad (2-34)$$

For reasons to be specified later, this thesis will redefine the phase impulse response as (2-35) where the term $\Upsilon(\omega_0\tau)$ has units of Coulomb⁻¹.

$$h_\phi(t, \tau) \triangleq \Upsilon(\omega_0\tau) \cdot u(t - \tau) \quad (2-35)$$

The output excess phase as a function of a noise source $i(\tau)$ is found from the following convolution integral (2-36), which holds true for any linear system (time invariant or time varying) [Str82].

$$\phi(t) = \int_{-\infty}^{\infty} h_\phi(t, \tau) i(\tau) d\tau = \int_{-\infty}^t \Upsilon(\omega_0\tau) i(\tau) d\tau \quad (2-36)$$

Since $\Upsilon(\omega_0\tau)$ is a periodic function it may be expanded into a Fourier series as in (2-37).

$$\Upsilon(\omega_0\tau) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos(n\omega_0\tau + \theta_n) \quad (2-37)$$

Substituting (2-37) into (2-36) produces

$$\phi(t) = \frac{c_0}{2} \int_{-\infty}^t i(\tau) d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^t i(\tau) \cos(n\omega_0\tau) d\tau \quad (2-38)$$

Hajimiri also demonstrated that the noise sources “close” to a harmonic of the oscillation frequency make the largest contribution to the oscillator noise sidebands [Haj98]. The definition of “close” will be defined in more detail later in the thesis. For now, the definition of “close” makes the assumption that $\Delta\omega \ll \omega_0$. This is a limitation of this method in that this narrowband assumption does not allow the prediction of the oscillator noise floor.

As explained in section 2.1, three categories of noise sources must be considered for oscillator phase noise. The noise $i(\tau)$ may be either a stationary source, a cyclostationary source, or a spurious tone.

2.5.3.1 Spurious Tones

For a spurious tone close to an integer multiple of the oscillation frequency (including DC), $i(t)$ is modeled as,

$$i(t) = I_{n'} \cos[(n'\omega_0 + \Delta\omega)t] \quad (2-39)$$

Substituting (2-39) into (2-38) yields (2-40).

$$\begin{aligned} \phi(t) = & \frac{c_0}{2} \int_{-\infty}^t I_{n'} \cos[(n'\omega_0 + \Delta\omega)\tau] d\tau \\ & + \sum_{-\infty}^{\infty} \sum_{-\infty}^t c_n \int_{-\infty}^t I_{n'} \cos[(n'\omega_0 + \Delta\omega)\tau] \cos(n\omega_0\tau) d\tau \end{aligned} \quad (2-40)$$

When we use the narrowband assumption $\Delta\omega \ll \omega_0$, the expression is dominated when $n' = n$ and (2-40) is approximated by (2-41).

$$\phi(t) \approx \frac{I_n c_n \sin(\Delta\omega t)}{2\Delta\omega} \quad (2-41)$$

The conversion from the excess phase of (2-41) to a phase noise sideband makes another narrowband assumption, where it is assumed that the phase function $\phi(t)$ produces a narrowband phase modulation which is modeled in Figure 2-42 and (2-42) [Man87].

$$V(t) = \cos[\omega_0 t + \phi(t)] \quad (2-42)$$

FIGURE 2-9 Conversion of noise source to phase noise sideband

Substituting (2-41) into (2-42) and defining the modulation amplitude as $\epsilon = (I_n c_n)/(2\Delta\omega)$ produces (2-43).

$$V(t) = \cos[\omega_0 t + \epsilon \sin(\Delta\omega t)] \quad (2-43)$$

which can be expanded to (2-44)

$$V(t) = [\cos(\omega_0 t) \cdot \cos(\epsilon \sin \Delta\omega t)] - [\sin(\omega_0 t) \cdot \sin(\epsilon \sin \Delta\omega t)] \quad (2-44)$$

The functions $\sin x \cong x$ and $\cos x \cong 1$ are valid for the assumption of $x \ll 1$. In the case of a noise source, the amplitude is considered to be very small. Therefore we can assume $\epsilon \ll 1$, which produces the following equation.

$$V(t) = [\cos(\omega_0 t)] - \epsilon [\sin(\omega_0 t) \cdot \sin(\Delta\omega t)] \quad (2-45)$$

(2-45) expands to (2-46),

$$V(t) = \cos \omega_0 t - \frac{\epsilon}{2} [\sin(\omega_0 + \Delta\omega)t + \sin(\omega_0 - \Delta\omega)t] \quad (2-46)$$

This equation (2-46) is comprised of the fundamental oscillator frequency plus two sidebands at $\omega_0 \pm \Delta\omega$. From this, the power of the carrier to a single sideband is calculated by (2-47)

$$P_{SBC}(\Delta\omega) = 10 \cdot \log \left(\frac{I_n^2 C_n}{4\Delta\omega} \right)^2 \quad (2-47)$$

The C_n term can be interpreted as the conversion gain of the noise power near that harmonic, where C_0 represents the conversion gain for noise powers near DC. The definition of how close the frequency must be to the harmonic is a function of the effective ω_β of the mixing device which must include the effects of parasitic and circuit components. The noise power is only valid for frequencies that are offset from a harmonic of the fundamental by less than $\omega_\beta/2\pi$.

(2-47) can be compared to simulations using the method outlined in section 2.4 to benchmark this method.

2.5.3.2 Stationary Noise Processes

Next consider the case of a random current which has a white stationary power spectral density of $\overline{i_n^2}/\Delta f$, where,

$$\overline{i_n^2}/\Delta f = I_n^2/2 \quad (2-48)$$

Substituting (2-48) into (2-47) produces the single sideband phase noise for a stationary noise source.

$$\mathcal{L}\{\Delta\omega\} = 10 \cdot \log \frac{\left(\frac{\overline{i_n^2}}{\Delta f} \sum_{n=0}^{\infty} c_n^2 \right)}{(4\Delta\omega^2)} \quad (2-49)$$

Parseval's equation (2-50) is used to relate the Fourier coefficients of (2-49) to the root mean squared power.

$$\sum_{n=0}^{\infty} c_n^2 = \frac{1}{\pi} \int_0^{2\pi} |Y(x)|^2 dx = 2Y_{rms}^2 \quad (2-50)$$

Substituting (2-50) back into (2-49) yields the single sideband phase noise as:

$$\mathcal{L}\{\Delta\omega\} = 10 \cdot \log \left[\frac{\left(\overline{i_n^2} / \Delta f \right) \cdot Y_{rms}^2}{2 \cdot \Delta\omega^2} \right] \quad (2-51)$$

Hajimiri's model also includes an expression to incorporate the $1/f^3$ phase noise region produced by flicker noise. This expression will not be repeated in this work as bipolar devices have a very low flicker noise corner which will be suppressed by the loop bandwidth of a phase locked loop [Wol91].

2.5.3.3 Cyclostationary Random Processes

Substituting a cyclostationary noise source which has been decomposed into its stationary component and its normalized periodic scaling function (2-4) into (2-36) yields:

$$\phi(t) = \int_{-\infty}^t \alpha(\omega_0\tau) i_{n0}(\tau) \Upsilon(\omega_0\tau) d\tau \quad (2-52)$$

Since $\alpha(\omega_0\tau)$ and $\Gamma(\omega_0\tau)$ are periodic over of the same interval, a new term, $\Upsilon_{eff}(\omega_0\tau)$, can be defined which results in an effective current sensitivity function.

$$\Upsilon_{eff}(\omega_0\tau) = \alpha(\omega_0\tau) \cdot \Upsilon(\omega_0\tau) \quad (2-53)$$

The cyclostationary scaling function can be extremely important for modeling an oscillator circuit which has shot noise. Depending on the phase of the cyclostationary function, this effect may reduce the current sensitivity function and thus the phase noise contribution.

Substituting (2-53) into (2-52) yields

$$\phi(t) = \int_{-\infty}^t i_{n0}(\tau) \Upsilon_{eff}(\omega_0\tau) d\tau \quad (2-54)$$

Similar to the white stationary noise source, the SSB phase noise of a cyclostationary noise source is given by (2-55).

$$\mathcal{L}\{\Delta\omega\} = 10 \cdot \log \left[\frac{\left(\overline{i_n^2} / \Delta f \right) \cdot (\Upsilon_{eff})_{rms}^2}{2 \cdot \Delta\omega^2} \right] \quad (2-55)$$

2.6 *Floquet Multipliers and Commercial Phase Noise Simulators*

As opposed to Hajimiri, Demir et. al. develop a time domain method of oscillator phase noise simulation that does not assume the amplitude perturbations were insignificant [Dem98, Dem99, Dem00]. This method makes use of non-Monte Carlo time domain simulation as opposed to other methods [Bol92, Mac94, Klo95] which require Monte Carlo-like simulations. Monte Carlo-like methods employ nonlinear stochastic differential equations that describe the current and voltage of noise sources and several hundred simulations of the oscillator over many periods where the noise power is integrated and FFTs are used to produce the phase noise. Although reputedly accurate, the Monte Carlo-like methods are not feasible for practical circuits due to computation time [Demir98].

Demir's method is similar to Hajimiri's in that it is based on describing the oscillator as a time varying linear system. However, Demir uses some rather involved linear algebraic calculations that are derived from Floquet theory [Cad98, Kun00]. The first step is finding the periodic steady state of the oscillator and then linearizing around this trajectory in order to perform the small signal analysis. The resulting time-varying linear system is used to calculate the noise power spectral density. Demir classifies the oscillator noise perturbations into two types, those which create phase slippage (Hajimiri-like) and those responsible for time-damped fluctuations. These time-damped fluctuations are derived from the combination of amplitude noise and the limit cycle behaviour of the oscillator. These two types of noise perturbations are not strictly orthogonal and can be interdependent.

The solution of small signal analysis of a single operating point with constant coefficients is a straight forward exercise in linear algebra. This is the method that simulators use to solve the small signal analysis of circuits. A much less known fact is that analogous results hold true for the case of periodic coefficients. The essential idea for such a generalization

was proposed by G. Floquet in 1883 and is referred to as Floquet theory. The resemblance between solutions to ordinary differential equations with constant and periodic coefficients is due to the fact that periodic coefficients can be transformed by a substitution of variables into an equation with constant coefficients which can then be solved by linear algebra [Dem98, Dem99, Dem00].

Although it has been argued many times that Hajimiri's linear time varying phase noise theory is flawed in its modeling of phase noise because of the assumption of ignoring the amplitude response due to noise impulses [Dem97, Dem98, Kun99], the results of LTV theory do provide many insights into oscillator design which have been verified by measurement [Haj98]. This cannot be said for Demir's work with Floquet multipliers which proposes an accurate mathematical solution for oscillator phase noise but does not provide any insight or intuition into oscillator design, just a solution.

This being said, the benefit of Demir's research has been its integration into Cadence's Spectre RF phase noise simulation. Before Demir's research, there were several commercial simulators that claimed to accurately simulate oscillator phase noise but reported evidence showed quite the opposite. Many of these simulators were pessimistic in their phase noise predictions of oscillator circuits [Poo97a, Poo97b]. The pessimism of phase noise simulation was unique among circuit simulators where measured performance is generally poorer than simulated performance. In 1997, Poore reported the measured phase noise performance of LC oscillators that was as much as 10 to 20 dB better than predicted by simulators [Poo97a, Poo97b, Des97].

Today Cadence SpectreRF is considered to be a fast and accurate tool to predict oscillator phase noise [Heg01, Cad98, Zan98]. However, in some circuits the Floquet multiplier may not converge to unity and the solution cannot be resolved. Known limitations of the simulator include any oscillator that does not have a stable periodic steady state [Cad98]. Other problem circuits are oscillators which have a significant large signal response at

frequencies other than the fundamental and its harmonics which may be caused by some types of varactor diodes, AGC circuitry, and bias circuitry [Cad98]. The presence of subharmonic or aperiodic components in the large signal response of an autonomous circuit requires the foreknowledge of which frequency components are important. Still other problem circuits include properly constructed Colpitts oscillators which may exhibit chaotic as well as subharmonic behaviour. Presently, the accurate simulation of oscillator phase noise is not a trivial exercise with even the best CAD tools. For example, a bipolar design that reported using SpectreRF for phase noise optimization, demonstrated better measured phase noise performance than simulated [Zan98].

Other types of simulators include harmonic balance based simulators which like Volterra series based oscillators are only accurate for quasi-linear circuits. As the circuit behaviour becomes more nonlinear, the finite set of frequencies required to model the waveform grow exponentially and the accuracy degrades. In fact, this class of simulators will not always converge to a solution for ring oscillators, which are very nonlinear in their operation.

In summary, the simulation of phase noise performance of oscillators is not elementary. It can be difficult to calibrate the simulator to predict measured results. In this case, it is not a predictor of oscillator phase noise performance but a useful tool once calibrated for dissecting the performance of the circuit under scrutiny and finding a more optimized set of parameters.

The Design, Analysis, & Simulation of LC Resonator Oscillators

Since 1998 several simulators and methods have been postulated to accurately predict phase noise performance. However, the limitations of these tools still require a thorough understanding of oscillator performance to develop a circuit topology which exhibits optimal performance. What is needed is the development of general purpose integrated oscillator topology that has been optimized for low phase noise performance. Many integrated designs have reported their phase noise performance, however, they have not made a clear presentation of the performance trade-offs in the design.

In the previous chapter, LTV theory demonstrated that the properties of LC harmonic oscillators are analogous to those of an ideal oscillator and why they have an advantage over ring oscillators in phase noise performance. In this chapter, a new VCO topology is developed based on circuit intuition, an understanding of noise sources, phase noise mechanics, and existing phase noise models to provide the designer with useful insights into the design of oscillators for low phase noise. Common oscillator circuits are reviewed and the design methodology of a new balanced oscillator circuit is detailed.

3.1 *Oscillator Circuit Analysis*

There are two schools of thought on the principles of LC oscillator operation. The oscillator can be thought of as a positive feedback loop consisting of an active amplifying device and a frequency selective feedback. The conditions for oscillation are met when the open loop transfer function of the circuit produces unity gain and a phase shift of 0° at a single frequency, which is commonly referred to as the Barkhausen criterion [Gre84]. The other model, also known as the van der Pol system, partitions the circuit into two separate single port networks, a lossy frequency selective network and a negative resistance network. The negative resistance cancels the real losses of the frequency selective network at a single frequency leaving the imaginary components to resonate. Either model can be applied to an oscillator circuit and the choice of either is only a matter of convenience for analysis [Ale97]. These analyses assume that a linear method is applicable to the steady state oscillator operation. However, the steady state operation of an oscillator circuit is highly nonlinear because of large nodal voltages which are very much in the large-signal regime. Linear analysis does provide accurate modeling as to whether a resonator circuit will oscillate and will also allow us to approximate the oscillation frequency. The modeling of oscillator start-up is accurate because the nodal voltages of the circuit can be considered small signal at start-up and the circuit can be well represented by a linear model. As the oscillation amplitude subsequently grows, the oscillation frequency will shift from that predicted by linear analysis with the amount of shift dependent upon how nonlinear the operation has become. This shift is caused by a bias shift in the device which changes the parasitics parameters of the active device.

3.2 *Common LC Resonator Oscillator Topologies*

LC resonator oscillators were chosen as the focus of this research because they are favoured for low phase noise performance. A survey of common LC harmonic oscillator

topologies is shown in Figure without appropriate biasing or grounding [Rho88]. The decision as to which topology is most suited for low phase noise performance in an integrated circuit implementation can be based on an empirical knowledge of the process and of realization issues that come with monolithic integration. Some of this reasoning follows. The final choice for implementation was the Colpitts oscillator.

The Hartley configuration is the dual of the Colpitts circuit, but is less attractive for integration because of the greater number of inductors required by the circuit. The quality factor of spiral coplanar inductors is much less than that of the metal-insulator-metal (MIM) capacitors of most generic technologies. Leeson's model indicates that the loaded Q of the circuit must be maximized to minimize the oscillator phase noise. The highest circuit Q is only achievable by utilizing the highest quality components available and minimizing the number of low Q components. This reasoning also excludes the tuned input/tuned output topology, which requires two inductors.

FIGURE 3-1 Conventional LC Oscillator Topologies

Presently, integrated transformers have been realized by either the close coupling of two vertically aligned spiral coplanar inductors implemented in the two top metal layers of a planar process [Lon96a] or by interweaving the primary and secondary windings in the top metal layer [Zan98]. The quality factor of either of these integrated transformers is lower than that of a single inductor. In the first realization, the primary winding is implemented in the top metal layer which is relatively thick with a low resistivity. The secondary winding is implemented in a thinner metal layer which has a higher resistivity, which increases its loss. The second metal layer is also closer to the substrate and suffers from higher substrate coupling losses. The interwoven transformer suffers from a lower inductance value per unit length because the spacing of the turns are an order of magnitude larger. The same value of inductance requires more turns and is a physically larger inductor, which will result in higher losses. Therefore, oscillator topologies that utilize transformers were not considered as candidates for low phase noise integrated oscillators.

Both the Colpitts and the Clapp-Gouriet circuits are candidates for high performance integrated implementations. The Clapp-Gouriet circuit is known to provide better spectral purity and phase noise performance but the capacitor in series with the inductor provides a challenge for DC biasing [Ale98]. Another major disadvantage of the Clapp-Gouriet circuit is that the tuning range is smaller than that of the Colpitts circuit [Kra80].

3.3 Which Colpitts Biasing Scheme?

The Colpitts oscillator circuit was chosen as the foundation of this design based on the above arguments. This circuit can be configured into one of three different DC biasing schemes depending on which terminal of the active device is grounded. Figure shows the common collector circuit in the common base, common emitter, and common collector biasing topologies.

FIGURE 3-2 Possible Configurations of the Colpitts Oscillator

The performance of ideal realizations of the three configurations is equivalent as shown in Figure [Ale98]. The only exception is the common emitter topology which requires a component, such as an RF choke, to allow DC biasing of the collector and decoupling of the oscillation signal from the power supply. The DC biasing requirement eliminates the common emitter topology as an attractive circuit for integration, as a high inductance RF choke is not realizable in a monolithic process. If a resistor is used instead of the RF choke as the bias component, it will reduce the Q of the resonator, unless the value is made large, which would then require a very large supply voltage.

The practical implementation of these circuits must consider the output loading of subsequent stages. Ultimately, the oscillator circuit will be required to drive a circuit load. In some cases, the circuit would be loaded by the input of test equipment. In the digital radio implementation, the oscillator circuit drives a mixer and the prescaler of a synthesizer either directly or indirectly. In some cases, a buffer stage, gain stage or limiting stage must be applied to the output of the oscillator before driving these circuits.

Any node of the circuits can be used to drive the required load. Coupling the load directly to the resonator may de-Q or cause load pulling of the resonator, which would degrade the phase noise performance of the oscillator. Based on this argument, it is desirable to isolate the resonator from the load. The common collector circuit can drive a load which is isolated from the resonator with the addition of a load on the collector as shown in Figure 3-3. This load must also provide DC biasing and may be realized as a resistor, RF choke, inductor, or a parallel LC tank. In contrast, the common base or common emitter topologies do not readily facilitate driving a load with the common terminal of the device.

3.4 *The Common Collector Colpitts*

Figure 3-3 shows the common collector colpitts with a load resistor R_C inserted in the collector to provide an output V_{out} uncoupled from the resonant tank by the active device Q_1 . The parallel LC resonator of the Colpitts circuit is the equivalent capacitance of the series combination of C_π and C_e in parallel with the inductor L_I . As was described earlier, real LC resonators are lossy and require an active device to restore the lost energy. Positive feedback and an active device are required to inject the restoring energy into the resonator. The bipolar device Q_1 in the common collector Colpitts senses the voltage across C_π and injects a proportional current on to the emitter capacitor C_e which is labelled as $I_{restore}$ in Figure 3-3. This injected current increases the voltage of C_e and therefore C_π , which produces a positive feedback. The oscillation is initiated when the circuit is powered and the noise of the tank circuit is amplified by this positive feedback and is fed back into the tank circuit to create a resonance at the resonator's natural frequency.

FIGURE 3-3 Common Collector Colpitts with Collector Load

One disadvantage of the common collector Colpitts as shown in Figure 3-3 is the low impedance voltage bias required for the node labelled V_{bias} . It is very difficult at RF frequencies to provide a zero impedance voltage source and any resistance of that source will degrade the quality factor of the inductor L_1 . This difficulty is resolved when the balanced version of this oscillator is discussed later.

The intrinsic device capacitance $C_{\pi Q1}$ (not shown) is a nonlinear function of the junction voltage. This is the same type of nonlinear capacitance that a varactor diode exploits to achieve a voltage variable capacitance. This nonlinear capacitance results in a direct phase modulation or phase noise of the fundamental oscillation frequency when a large signal is applied across the junction. The amount of phase modulation can be reduced by adding a large external linear capacitance in parallel with the device to dominate the overall effective $C_{\pi eff}$ where, $C_{\pi eff} = C_{\pi Q1} + C_{\pi}$. This is convenient because the ratio of C_{π}/C_e determines the amount of positive feedback for the active device, with a larger C_{π}/C_e ratio reducing the amount of feedback. This means that the active device senses a smaller component of the tank voltage. Less feedback allows a larger tank voltage before the device self limits. The self limiting is a result of the bias shift and the third order

desensitization which results from a large enough signal swing across C_π . Note that the nonlinear device capacitance is a secondary nonlinear effect since the nonlinearity of the oscillator circuit discussed in section 2.4 is the dominant nonlinear effect.

Recalling Leeson's equation it can be understood from the above argument that not only does a large linear external value of C_π help reduce unwanted phase modulation but it also maximizes the tank energy which reduces phase noise. This leads to a trade-off in terms of choosing the device size. Increasing the device size increases the nonlinear capacitance $C_{\pi QI}$ but also reduces the intrinsic base resistance which can be a dominant noise source in series with the inductor.

3.4.1 Linear Analysis of Common Collector Colpitts Oscillator

The negative resistance model is convenient for analyzing the linear behaviour of the common collector Colpitts circuit [Ven90]. The circuit of Figure can be viewed as a series RLC resonant circuit where the input impedance of the circuit is approximated by (3-1).

$$Z_{in} \cong j\omega L + R_b + \frac{1}{j\omega C_{\pi eff}} + \frac{1}{j\omega C_e} - \frac{g_m}{\omega^2 C_{\pi eff} C_e} \quad (3-1)$$

In this equation, the term R_b is comprised of the inductor series resistance as well as the intrinsic base resistance, and $C_{\pi eff}$ includes both the intrinsic transistor capacitance $C_{\pi QI}$ and the externally added capacitance C_π [Dau97].

FIGURE 3-4 Common Collector Oscillator Analysis

Linear theory predicts that the circuit will oscillate when the series impedance of the circuit is equal to zero. The expression (3-1) can be set equal to zero and separated into the real and imaginary components, producing (3-2) and (3-3).

$$R_b - \frac{g_m}{\omega^2 C_{\pi eff} C_e} = 0 \quad (3-2)$$

$$j\omega L + \frac{1}{j\omega C_{\pi eff}} + \frac{1}{j\omega C_e} = 0 \quad (3-3)$$

These equations determine the oscillation condition of the common collector Colpitts circuit. However, in this case an actual nonlinear oscillator circuit would not start. The practical oscillator circuit requires a gain margin [Boo89] to start reliably and requires that the real component of Z_{in} to be negative, which will occur when the inequality given in (3-4) is satisfied.

$$\frac{g_m}{\omega^2 C_{\pi eff} C_e} > R_b \quad (3-4)$$

An estimate of the oscillation frequency can be obtained by solving the imaginary component which is given by (3-5) and (3-6).

$$\omega_0 = \frac{1}{\sqrt{LC_{eff}}} \quad (3-5)$$

where C_{eff} is given by (3-6).

$$C_{eff} = \frac{C_{\pi eff} C_e}{C_{\pi eff} + C_e} \quad (3-6)$$

The inequality of (3-4) indicates several properties about the oscillation of this circuit. For a fixed resistor of R_b , the start-up of oscillation is dependent on the small signal g_m of the active device. Small-signal transconductance is also directly proportional to the DC collector current of the active device. Therefore there exists a minimum bias current to achieve oscillation. The inequality also indicates that as the oscillation frequency is increased, more bias current is required to start oscillation. In fact, substantially more current is required since the condition for oscillation is proportional to the square of the frequency. This shows that high frequency oscillators of this type will consume more power than comparatively lower frequency designs. This can be understood somewhat, as follows: A higher oscillation frequency by a ratio of K can be achieved with C_{eff} a factor of K smaller, and L a factor of K smaller. With Q the same, the equivalent parasitic resistances of C_{eff} and L will be a factor of K smaller, suggesting the same power at the higher frequency. But the series resistance of the transistor base is not reduced, so higher currents are required for oscillation conditions.

The inequality of (3-4) also seems to indicate a possible design trade-off where the bias current required for oscillation is proportional to the product of the capacitors $C_{\pi\text{eff}}$ and C_e . Reducing the overall effective capacitance will reduce the required current for oscillation but would increase the required inductance for the same oscillation frequency. This choice has the advantage of reducing the shot noise of the device. However, the quality factor of coplanar spiral inductors available in modern processes is not constant with inductance or frequency and there exists an optimum inductance value. The quality factor of coplanar spiral inductors increases with frequency as $\omega L/R$ but then drops off as the losses due to the substrate and skin effect increase with frequency, as shown in Figure for an inductor designed in Nortel's 0.8 μm BICMOS process [Lon96]. Therefore, a frequency exists where the quality factor is a maximum. The magnitude and the frequency of the maximum quality factor vary with the inductor size. Figure 3-5 shows the quality factor for different inductance values. This plot shows that not only does the peak Q occur at a different frequency but the Q also differs with inductance value. For example, the 7 nH inductor consists of 6 turns and a length of 237 microns, whereas the 4.8 nH inductor consists of 5 turns and a length of 203 microns. The longer length of the 7 nH inductor increases the DC resistive losses, which lowers the overall Q . The operating frequency of the larger inductor is lower as well, because the larger area increases the capacitance and lowers the self-resonant frequency. It is important to choose the inductance with the maximum Q because it is usually the limiting factor in the unloaded Q of integrated resonators. In Nortel's process, inductor Q 's are less than 5 at 1.5 GHz, whereas, the Q 's of metal-insulator-metal capacitors and junction diode varactors were measured to be greater than 20. The method used to maximize the inductor Q is an iterative process which uses a coplanar spiral inductor model program called GEMCAP [Lon96].

FIGURE 3-5 Coplanar Spiral Inductor Quality Factor versus Frequency for 4.8nH

FIGURE 3-6 Peak Quality Factor versus Inductance

3.4.1.1 SPICE AC Analysis

The above linear analysis of the Colpitts circuit uses simplifying models and assumptions and ignores device and circuit parasitics. To achieve a better model of the circuit the AC analysis of HSpice 96.1 can be used to plot the real and imaginary parts of the impedance Z_{in} . In this way, the minimum bias current for the start-up of oscillation can be determined. Figure plots the real and imaginary parts of the impedance of a common collector Colpitts oscillator looking into the inductor as in Figure . The real component of Z_{in} is much less than zero when the imaginary component is equal to zero. This indicates the oscillator would be operating in a very nonlinear mode with a large amount of positive feedback. The imaginary component crosses zero impedance at 1.5 GHz, which corresponds to the linear approximation of the oscillation frequency.

FIGURE 3-7 Imaginary and Real components of Z_{in}

3.5 *A Balanced LC Colpitts Oscillator*

One of the advantages of integrated circuits has been the ability to exploit the noise immunity properties of balanced or differential circuits. This was the main motivation behind developing a balanced LC resonator oscillator. Noise or interference that is common to both signals is suppressed when the difference of the signals is used. Integrated circuits are able to provide the matched devices or components that are required for balanced circuits and the number of components does not generally affect the cost of silicon in balanced circuits.

Additionally, high impedance bias nodes can be used in balanced circuits instead of low impedance nodes, which are difficult to realize as discussed above in section 3.4. Balanced circuits can provide 3 dB more output power than the equivalent unbalanced circuit without increasing the voltage supply or, conversely, provide the same output power as the equivalent unbalanced circuit at a lower supply voltage. This characteristic is extremely beneficial for low power applications which use high speed devices with low breakdown voltages. In terms of oscillator circuits, balanced oscillators enable the circuit to drive the mixer and ECL logic directly without a lossy balun or other unbalanced to balanced component.

A balanced common collector Colpitts circuit is formed by joining two single-ended circuits together as detailed in Figure . The two capacitors labelled C_e can be combined into one smaller capacitor. As mentioned above, this configuration allows high impedance biasing to be used for the common inductor node. An added benefit of the high impedance bias at this node is elimination of common mode oscillation. This additional simultaneous oscillation, called squegging, would be at a different frequency and would waste signal power and produce spurious noise products. However, since the common mode circuit includes the resistance of the high impedance bias point in the AC circuit path, the negative resistance term will never exceed the equivalent resistance. The bias point will be

at virtual ground for the fundamental and odd order harmonic currents, but even order harmonics will see the full resistance to ground. This is especially important for packaging integrated circuits where inductive bonding and parasitic capacitances could produce ground bounce and excite common mode oscillations.

FIGURE 3-8 The Making of a Balanced Common Collector Colpitts Circuit

FIGURE 3-9 Balanced VCO Schematic

The balanced oscillator schematic shown in Figure has varactor diodes added in parallel with C_{ee} to provide voltage controlled tunability. A back-to-back varactor configuration is used to prevent the varactors from being forward biased by the RF signal. A high resistance impedance is also used in series with the tuning voltage to reduce common mode oscillation.

The capacitance ratio of C_{ee} and the varactor diodes can be adjusted to change the tuning range. The oscillator should be designed to use the minimum tuning range which satisfies the application as well as component and process tolerances. The tuning range corresponds to the gain of the VCO, and any noise at the tuning voltage input is amplified by this gain.

Figure 3-10 shows more detail of the circuit topology including the load under test. The current sources are realized by transistors Q_3 and Q_4 which are mirrored to the diode connected Q_5 . The outputs are AC coupled by capacitors labelled C_{ac} to the equivalent test loads R_{test} .

FIGURE 3-10 More Detailed VCO Schematic

3.6 *Designing the Balanced Colpitts Oscillator for Low Phase Noise*

The experimental prototype used to validate the low phase noise performance of the topology proposed above is a 1.5 GHz oscillator implemented in Nortel's 0.8 μ m BiCMOS process. The bipolar devices in this technology have an f_T of 11 GHz and are optimized for digital applications using a voltage supply of 5V. As a result, these devices have a large base resistance in comparison to bipolar processes developed specifically for RF applications. Large devices are therefore required to reduce the noise contribution from the base resistance as it is in series with the inductor of the resonant tank of the oscillator. Even large devices such as the 45X device (45 times the smallest device in the library) still have a base resistance of approximately 8 Ω .

Although simulation tools were not mature enough to offer an accurate simulation solution when the experimental prototypes were being designed and fabricated [Poo97], they have improved their accuracy as reported in the literature [Zan98, Heg01] and are presented here to support the design decisions presented in this chapter. The theoretical insights from LTV analysis are useful but as a simulation method the implementation is cumbersome. LTV simulations require many individual transient simulations for each noise source to generate the sensitivity function. The measurement of the phase differences can also be fraught with error as exact zero crossings and exact measurements are difficult with discrete time simulators. The theory however appears sound and hopefully the method will be implemented into a commercial simulator. Based on this reasoning, Cadence's SpectreRF was used to simulate the oscillator performance.

A power supply voltage of 3V was used in the oscillator design although the performance with different power supply voltages is explored later in the chapter. The following sections detail the methodology used to choose the component values of the proposed oscillator to minimize the phase noise.

3.6.1 Inductor Selection

As mentioned above, the inductor is one of the most important components of the oscillator because of the low quality factor achievable in fully integrated designs and its domination of the resonator's loaded Q. The inductance which was optimized by Long [Lon95] for maximum Q using GEMCAP (GEneral Microstrip Coupling Analysis Package) and fit to a compact double Π model shown in Figure for simulation. The optimum inductance value was found to be 4.8nH with a Q of 4.7 at the desired frequency of 1.5 GHz.

FIGURE 3-11 Double Π model of 4.8nH inductor in Nortel's 0.8 μ m Process

3.6.2 Selecting the Collector Load Impedance

One of the advantages of the balanced common Colpitts oscillator is that it can drive loads directly without a buffer amplifier. A load resistance of 50 Ω was chosen to enable the VCO to drive standard 50 Ω test equipment directly without any impedance transformation. A test setup for measuring VCO performance is shown in Figure . The RF input to the phase noise meter is a 50 Ω input and the RF combiner requires 50 Ω on each port to function correctly. Terminating the collectors into a load resistance of 50 Ω achieves

this requirement. Referring to Figure 3-10, the value of resistors labelled R_C as well as resistors labelled R_{test} is 50Ω .

FIGURE 3-12 VCO Test Setup

Irrespective of accommodating test equipment, a larger resistance load on the collector increases oscillator output power and voltage swing but reduces the voltage headroom of the collector-base junctions of the active devices Q_1 and Q_2 . The voltage headroom on the collector-base junction is important because it determines the maximum bias current before the active devices Q_1 and Q_2 enter the saturation operating region. As the bias current of an oscillator circuit is increased, the devices do not enter the saturation operating region from their DC voltage levels but from the AC signal swing of the collector and base for a portion of the oscillation period. Some minimal forward biasing of the collector-base junction is not catastrophic to the phase noise performance. However, full saturation of the devices occurs for a V_{BC} greater than a few hundred millivolts. In this region, both junctions of the device are completely forwarded biased which significantly increases the base current and base shot noise. Full saturation of the devices also limits the maximum oscillator tank voltage and must be avoided for low phase noise designs.

An LC parallel resonator in parallel with the collector load resistor if centered at the fundamental oscillator frequency would filter harmonic output and provide additional DC and AC voltage headroom on the collector-base junction. However, it also doubles the required die area and was not considered for this experiment.

3.6.3 *The Choice of Capacitor Ratio*

An infinite number of C_π/C_{ee} capacitance ratios can be used to produce the chosen oscillation frequency for a fixed inductance value. However, this section will demonstrate that the choice of the capacitor ratio and the operating bias current have a significant effect on the phase noise performance of the oscillator.

From a simple signal level viewpoint, the capacitor ratio determines the feedback factor of the oscillator which is defined in (3-7) where C_e is the single-ended equivalent of C_{ee} or $C_e = 2C_{ee}$.

$$n = \frac{C_e}{C_e + C_\pi} \quad (3-7)$$

The feedback factor is the amount of tank voltage that is sensed by the bipolar device and amplified to produce the restoring energy to the resonant tank. Larger values of C_π , and correspondingly smaller values of C_{ee} and therefore C_e , capacitively tap less voltage from the resonant tank and allow higher tank voltages. The tank voltage is defined as the voltage potential between the bases of each active device Q_1 and Q_2 .

The capacitance C_π of the capacitance ratio is a composite of an extrinsic C_π component plus the intrinsic $C_{\pi Q1}$ of the active device which is dependent on device operating point and is linear with bias current from (3-8).

$$C_{\pi Q1} \approx \frac{g_m}{\omega_T} - C_c \quad (3-8)$$

The intrinsic C_π of the active device is not insignificant because large device sizes in the target technology are required to reduce the effect of the base resistance. The parasitic $C_{\pi Q1}$ component can even dominate the $C_{\pi eff}$ depending on the ratio of C_π/C_e and the bias current.

The capacitive divider network can also be viewed as transformer-like where the feedback factor, n , determines the equivalent transformer turns ratio between the resonant tank circuit loading and the active device [Cla71]. As the feedback factor n is increased, where $0 < n < 1$, the transformed impedance of the active device's r_π across the resonator is decreased with the maximum loading of the active device being r_π . Smaller feedback factors decrease the loading of r_π reaffirming the above argument that smaller values of n allow larger tank voltages.

Recalling the inequality (3-4) which describes the linearized real impedance of the oscillator, the negative resistance would be maximum when $C_\pi = C_e$ keeping C_{eff} constant. This corresponds to a feedback ratio of 0.5 and produces oscillation conditions in the circuit at the lowest possible bias current. This feature can be exploited in designs in which power consumption is the principal requirement.

Phase noise simulations were performed for a variety of capacitor ratios as listed in Table 3-1 to explore the design space. The capacitor values were chosen to hold effective

capacitance and thus the oscillator frequency constant. The oscillator drew a bias current of 3.6mA and 3 volts was applied to the tuning port for simulations of all capacitor ratios.

TABLE 3-1 Feedback ratio versus Capacitor ratio

n	C_{π}/C_e	Percentage of C_{π} from active device parasitic
0.81	0.24	100%
0.61	0.64	68%
0.43	1.32	51%
0.32	2.12	41%
0.26	2.90	34%
0.21	3.73	29%
0.18	4.49	26%
0.16	5.28	23%
0.14	6.08	21%
0.13	6.93	19%
0.11	7.71	17%

The phase noise performance of various capacitor ratios is plotted in Figure 3-13. The lowest phase noise was achieved for the feedback ratio of 0.26 although the phase noise only varies less than 1 dB over the feedback ratio range of 0.16 to 0.32. The maximum peak to peak tank voltage is also plotted in Figure 3-13 and shows that the maximum tank voltage increases with decreasing feedback ratio. Intuitively, it would seem that phase noise would decrease as the tank voltage is increased as it does in Figure 3-13 but the maximum tank voltage does not correlate with the minimum phase noise.

FIGURE 3-13 Phase Noise and Tank Voltage versus Feedback Ratio for constant frequency and bias current

The phase noise and the maximum restoring current is plotted in Figure 3-14 versus the feedback ratio. This figure indicates correlation between phase noise performance and maximum restoring current. The largest peak restoring current is achieved with a feedback ratio of 0.32. Recalling the discussion of the ideal oscillator and insights from LTV modeling the ideal oscillator would operate in class C and its restoring current pulse would be a narrow pulse and which would also be in phase with the maximum tank voltage. It would also be beneficial if this narrow pulse had the maximum amplitude to maximize the restoration energy for a fixed bias current. Based on these arguments, these conditions would produce the lowest phase noise performance while drawing the minimum power consumption. The plots in Figure 3-14 appear to add further support to this argument.

FIGURE 3-14 Phase Noise and Restoring Current versus Feedback Ratio for constant frequency and bias current

Figure 3-15 plots the total output noise at a 100kHz offset from the fundamental frequency versus the feedback ratio. The total output noise is defined as the absolute value of only the output noise of the circuit as opposed to the phase noise which is the magnitude of the output noise relative to the magnitude of the oscillation signal power.

The total output noise is lowest at a feedback ratio of 0.32 oscillator, although the output noise for a ratio of 0.26 is nearly as low.

FIGURE 3-15 Total output noise versus feedback ratio

The simulated output referred noise is dominated by the same four noise sources across all feedback ratios. These four noise sources account for greater than 80% of the total output referred noise of the circuit and include the thermal noise of the resonator, the thermal noise due to the base resistance of the active devices driving the resonator, the collector shot noise of the same active devices, and the thermal noise of the emitter degeneration resistance of the current sources biasing the active devices driving the resonator.

Figure 3-16 shows that the thermal noise of the resonator reduces with the feedback ratio but the other three noise sources reach their lowest levels for the feedback ratio of 0.32. The thermal noise of the resonator is not actually being reduced as the feedback ratio is decreased. The output referred contribution of the resonator thermal noise is decreasing with a decreasing feedback ratio because the tank voltage is increasing. Simultaneously, the contribution of the collector shot noise is reducing with an increasing feedback ratio

due to the cyclostationary behaviour and the reduction of the conduction angle of the active device as predicted by LTV theory [Haj98]. The conduction angle refers to the period of time that the active device is turned on and produces shot noise. Figure indicates that a feedback ratio exists between 0.32 and 0.43 where the thermal noise contributed from the resonator is equal to the shot noise contribution. In an analogy to LNA noise figure optimization, this may be a optimum ratio for phase noise and would produce the lowest total output referred noise.

FIGURE 3-16 Top four phase noise contributors versus feedback ratio

The mechanisms of the oscillator cause the tank voltage to increase with decreasing feedback but the voltage across the active device, V_{π} , decreases proportionally with the feedback factor. This relationship causes the output voltage of the oscillator, V_{out} , at the collectors of the active devices to peak somewhere between a feedback factor of 0.21 and 0.32. The peak in V_{out} adds additional insight into explaining why the signal to noise ratio peaks near this range of feedback factors.

FIGURE 3-17 Shot Noise and Thermal Noise of Resonator by Percentage of Contribution

Hajimiri hypothesized that the optimal capacitor ratio of C_{π}/C_e is four based on LTV simulations and experimental measurements of a 100MHz single-ended common base Colpitts oscillator realized in a discrete implementation [Haj98]. His reported optimal capacitor ratio corresponds to a feedback ratio of 0.2 and concurs with a common designers rule of thumb documented by DeMaw but DeMaw's guidance does not give any reasoning for the ratio [DeM82]. Hajimiri's hypothesis is also based on the reasoning that as n increases the tank voltage decreases but the conduction angle of the of the active device decreases.

The above simulations indicate that the optimal capacitor ratio is not a constant for all designs as hypothesized by Hajimiri. In fact, this work shows an analogy to LNA design where the active device is optimized by tuning the device size and the bias current for minimum noise figure. The device size and bias current for minimum noise figure are only

valid for that particular topology and technology and must be re-optimized for a different topology or technology. Another analogy to LNA design is that when the minimum noise figure is achieved the dominant noise sources contribute roughly equally to the noise figure (viz. the thermal noise due to the base resistance and the shot noise of the collector would contribute equally in minimum noise figure LNA). In the case of oscillator design, the capacitor ratio can be tuned to minimize the output referred noise and this occurs when the thermal noise of the resonator and the shot noise of the active restoring devices contribute to the phase noise equally.

3.6.4 Oscillator Bias Current

The next step in the design of the oscillator is tuning the bias current for minimum phase noise. The simulated phase noise at a 100kHz offset is plotted versus bias current in Figure 3-18 for various feedback ratios. Figure 3-18 shows that the phase noise reaches the lowest level for a feedback ratio of 0.32. The figure also indicates that as the feedback ratio increases from 0.11 to 0.81 the bias current required to reach the minimum phase noise is increased. For feedback ratio greater than 0.32 the output voltage begins to decrease and the noise begins to increase which explains why the phase noise performance suffers for larger ratios despite burning even more bias current.

FIGURE 3-18 Phase Noise at 100kHz Offset Versus Bias Current for Various Feedback Ratios

Figure 3-19 plots the phase noise at a 100kHz offset versus oscillator core bias current for the feedback ratio of 0.32. The phase noise reaches a minimum phase noise of -105.7 dBc/Hz for a bias current of 9.65 mA. Figure 3-19 also demonstrates that phase noise performance can be traded for power consumption. This is an important property of the proposed oscillator that can be exploited by designers. The power consumption of the oscillator can be tuned to meet the phase noise performance required by the intended specifications without wasting power.

FIGURE 3-19 Phase Noise @100kHz Offset versus Bias Current for Feedback Ratio of 0.32

The phase noise improves with increasing bias current because the tank voltage is increasing proportionally with bias current whereas the output referred noise is nearly constant until 10mA when it increases at a rate much faster than the tank voltage as shown in Figure 3-20. The tank voltage increases with DC bias current as more restoring current is dumped onto C_{ee} . The reason for the dramatic increase in noise after 10mA is that the voltage swings on all three nodes of the active device have become so large that both the active device and its respective current source are fully in saturation and their collector-base junctions are fully turned on. Full saturation causes not only a dramatic increase in collector shot noise and base shot noise but the conversion gain noise of upconverted DC sources becomes a dominant noise contributor. Figure 3-20 shows the abrupt change in collector shot noise and thermal noise due to the current source degeneration.

FIGURE 3-20 Output Noise and Tank Voltage versus Bias Current for Feedback Factor of 0.32

FIGURE 3-21 Output Noise Versus Bias Current for Feedback Ratio of 0.32.

Recent research [Sam01] reports that oscillator phase noise due to low frequency upconversion can be optimized by minimizing the sensitivity of the oscillation frequency to bias current $\frac{\partial f_o}{\partial I_{bias}}$. The dependence of frequency on bias current comes from the fact that the oscillator frequency is not only dependent on the resonator but also by the loop phase delay θ of the active devices as defined in (3-9) [Cla71].

$$f_o = \frac{1}{2\pi\sqrt{LC}} \left(1 - \frac{\theta}{2Q} \right) \quad (3-9)$$

The phase delay θ depends on the bias current of the active devices due to the transistor transit time where $\tau_T \approx \frac{C_\pi}{g_m}$ and g_m is a function of bias current. This also explains why the phase noise increases as the C_π becomes dominated by the nonlinear intrinsic capacitance of the device for large feedback factors.

The simulated oscillation frequency versus the bias current of the oscillator is plotted along with the phase noise in Figure 3-22. The oscillation frequency initially increases at low bias currents due to the decreased transit time of the device. However, at higher currents C_π increases due to the base push out effect and the oscillator frequency reduces with frequency. Sam01 reports that choosing a large enough device size increases the bias current where $\frac{\partial f_o}{\partial I_{bias}} = 0$ will minimize the phase noise due to low frequency upconversion.

His research showed that for his architecture the phase noise reached a minimum at the minimum frequency sensitivity bias current. The oscillator circuit proposed here does not appear to be as sensitive to the same effects and the minimum phase noise is limited by the voltage headroom of the active devices. However, Figure 3-23 shows that a feedback ratio of 0.32 has the flattest frequency response to bias current out to where the lowest phase noise performance occurs at approximately 10mA.

FIGURE 3-22 Phase Noise and Oscillation Frequency Versus Bias Current for Feedback Ratio of 0.32

FIGURE 3-23 Oscillation Frequency Versus Bias Current for Various Feedback Ratios

Simulation of the proposed circuit with the supply voltage raised to 5 volts and lowered to 2.5V provides further evidence to support the argument that the phase noise performance is limited by active device voltage headroom. Increasing the voltage supply to 5 volts increases the active device headroom and increasing the bias current where the active devices enter full saturation. Decreasing the voltage supply to 2.5 volts reduces the headroom and reduces the bias current where full saturation occurs. Figure 3-24 shows that the phase noise is degraded for a supply voltage of 2.5 volts and improved for a supply voltage of 5 volts. In each case, the minimum phase noise performance occurs just before the collector-base junction of the oscillator active device and the active device of the current source are fully saturated. It should be noted that the DC bias design was not scaled for operation at lower voltages and circuit operation at 2.5V is non-optimal.

FIGURE 3-24 Phase Noise with supply voltages of 2.5V, 3V and 5V

If an RF choke is added across the collector load, as in Figure 3-25, the large inductance of the choke will look like a nearly zero impedance at DC and a very large impedance at the oscillation frequency. The large impedance at the oscillation frequency does not

appreciably reduce the overall load impedance and produces the same output level. The low DC impedance of RF choke allows the majority of the bias current to flow through the choke rather than the collector resistance. Some miniscule current will still flow through the collector resistor because of resistive parasitics of the RF choke. The net result of the low DC impedance of the RF choke is an increase in the active device voltage headroom and an increase in the bias current where full saturation occurs.

FIGURE 3-25 VCO Schematic with RF Chokes

The disadvantage of using the RF choke is that it is not a possible to implement it as an integrated component and cannot be used by fully integrated designs. However, it may be employed as a solution if the performance improvement warrants the cost of the extra non-integrated components and the extra package pin count for system on a chip designs. A large value integrated LC tank tuned to the oscillation frequency could be used instead of the RF choke to achieve equivalent phase noise performance. The disadvantage as already previously mentioned above is increased die area.

The improvement in voltage headroom due to the addition of the RF chokes is not as dramatic as from increasing the voltage supply from 3 volts to 5 volts because the voltage

drop across the collector load is only 250 mV for an oscillator bias current of 10 mA. Figure shows that the simulated performance of the RF chokes and a 3 volt supply is marginally better than a 3 volt supply without RF chokes pulling up the output. The performance is not as good as using the 5 volt supply which supports the fact that the increase in voltage headroom is not as large. If the circuit requirement is constrained by voltage supply this may be an acceptable solution to achieve a slight phase noise improvement.

FIGURE 3-26 Phase Noise Performance for 3V supply with and without RF Chokes

3.7 Class C Circuit Operation and Active Device Sizing

The large tank voltage produces a large voltage signal swing across the base-emitter junction of the active device which causes it to operate in class C mode. In Class C operation the device is periodically in the cutoff region where the base, collector, and emitter currents are all zero. It also results in the device producing zero base and collector

shot noise during the cutoff region. The phase noise due to shot noise can be minimized if the device is in cutoff during the AC zero crossing point of the tank voltage as suggested by LTV oscillator theory. The harder the device is driven, the longer it is in cutoff, and the greater the reduction in the shot noise component. Correspondingly, the price that is paid is increased power consumption.

Operating the active device in Class C mode helps to reduce the cyclostationary shot noise sources but sizing the active device is important to reduce stationary noise sources. Larger active devices improve phase noise performance in two ways. Firstly, a larger device reduces the sensitivity of the oscillation frequency to bias current by displacing the base push out effect (or Kirk effect) to higher bias currents [Gre84, Sam01]. The second benefit of increasing the device size is the reduction of the series base resistance which can be a major noise contributor.

Phase noise simulations were run using the above optimized circuit where the size of Q_1 and Q_2 were varied from a 15X sized device to a 75X sized device. The bias current for all device sizes was held constant at 8.6 mA near the optimal bias current of 9.65 mA in the above simulations. The external C_π was adjusted for each device size to maintain a constant effective capacitance and oscillation frequency. The simulated results in Table 3-2 indicate that the 45X device produced the lowest phase noise but was not significantly better than the 30X device. A 45X device corresponds to a bipolar npn device with a $0.8 \times 180 \mu\text{m}^2$ emitter area. The improvement in phase noise performance with increasing device size is attributed to increasing the point of onset of the base pushout effect and the reduction in the intrinsic base resistance [Sam01]. The degradation in further device size is attributed to the increasing percentage of the nonlinear capacitance. As the device size is

increased, the intrinsic C_π of the device increases and the value of the externally added C_π must be reduced to keep the effective capacitance and oscillation frequency constant.

TABLE 3-2 Phase noise versus size of Q1 and Q2

Device Size	Phase Noise (dBc/Hz)
15X	-102.4
30X	-104.9
45X	-105.0
60X	-103.6
75X	-103.0

Overall the simulation data of Table 3-2 indicates that the proposed oscillator topology is not as sensitive to device size as it is to the capacitor ratio and the bias current.

3.8 Simulation of Final Design Performance

Simulation of the final design versus control voltage shows the operation of the circuit as a voltage controlled oscillator. Figure 3-27 plots the oscillation frequency versus control voltage and indicates that the oscillator has a frequency range of 47 MHz or 3%. The control voltage is defined here as the reverse bias voltage across the tuning diode as opposed to being referenced to ground as opposed to the actual nodal voltage of the tuning port. The voltage range of the oscillator without forward biasing the tuning diodes is 2 volts which results in an average VCO sensitivity of 23.5 MHz/V.

FIGURE 3-27 Oscillation Frequency and Phase Noise Versus Control Voltage

The low tuning range of only 3% is due to the low percentage of C_{ee} contributed by the varactor diode capacitance. In this design, the varactor diode capacitance comprises 25% of the total C_{ee} capacitance. A 3 volt supply allows the varactor diode to vary its capacitance over a 2:1 range but because it only make ups a small percentage of the total emitter capacitance C_{ee} only varies by 12.5%. To achieve a larger tuning range, the varactor diode can be increased while reducing the amount of fixed C_{ee} . For example, if the varactor diode capacitance was increased to 100% of the total C_{ee} capacitance, the tuning range would increase to the maximum range. Note that larger tuning ranges may exhibit degraded phase noise performance due to AM to PM conversion of the modulation source noise and care should be taken to use the minimum range.

Figure 3-27 also plots the simulated phase noise and shows that the simulated phase noise performance degrades as the control voltage approaches zero with a degradation of approximately 4 dB. The increase in phase noise as the control voltage approaches zero is due to the nonlinearities of the tuning diodes causing increased VCO gain as the voltage potential across the diode approaches zero [Rog00].

FIGURE 3-28 Increased tuning range with maximum size varactor

Figure 3-28 shows that if the maximum size varactor diode is used the tuning range can be increased from 3% to 15%. The price that is paid is a slight degradation in phase noise performance as shown in Figure 3-29.

FIGURE 3-29 Phase noise degradation due to increased tuning range

In the next chapter, the simulated performance will be compared to experimental measurements of monolithic prototypes.

The previous chapter proposed a new balanced oscillator topology based on the common collector Colpitts oscillator circuit. The topology was optimized for low phase noise performance based on a methodology utilizing circuit intuition, an ideal oscillator model based on the results of LTV theory, and Cadence's nonlinear oscillator simulation. This chapter discusses the implementation of the proposed oscillator topology in a monolithic realization and reports the measured performance of the experimental prototypes. The measured performance is also compared to the simulated performance performed in the previous chapter to aid in the analysis of the measured results. The idea of an oscillator figure of merit is proposed to enable a fair and accurate comparison of oscillator efficiency and performance. This figure of merit, which has been adopted by industry, is used to benchmark the performance of this oscillator to the present state of the art.

4.0 Circuit Implementation

The proposed oscillator topology was implemented with the inductance value, device size, and collector load as outlined in the previous chapter. The topology was realized with four different capacitor ratios (see Table 4-1) to explore their effect on phase noise performance on the proposed oscillator circuit. As in the simulations, the capacitor values were chosen to maintain the same effective capacitance and thus a constant oscillation frequency. Each

implementation also utilized a variable bias current to investigate the trade-off between power consumption and phase noise performance and the ability to tune this parameter for maximum performance.

TABLE 4-1 Capacitor and feedback ratios of experimental prototypes.

Design	Feedback Ratio	Capacitor Ratio
ZA28_1	0.32	2.12
ZA28_2	0.21	3.73
ZA28_3	0.16	5.28
ZA28_4	0.11	7.71

The physical layout of the circuits is very important to achieve the performance predicted by simulation. Particular attention must be paid to minimizing the inductive, resistive, and capacitive parasitic effects of the physical layout for all RF routes. Copious amounts of inductive and capacitive parasitics will effect the accuracy of the oscillation frequency and, in the case of this topology, can alter the capacitor ratio. Resistive parasitics reduce voltage headroom and routes connecting inductors can degrade their quality factor. Another important point to observe in the layout is the differential symmetry of the circuit. The layout choices were somewhat constrained by the pad order and locations which were chosen to allow both wafer probe testing as well as packaged device testing.

FIGURE 4-1 Circuit layouts of the oscillators with four different capacitor ratios.

The circuit layout of the four designs are shown in Figure where each oscillator uses approximately 0.5mm^2 of die area. Initially, dice from each design were wafer probe tested for functionality and performance using a spectrum analyzer. Functional dice from each capacitor ratio were then packaged in a commercially available microwave package for testing. All of the oscillator measurements were then performed on the Hewlett Packard HP4352B VCO/PLL Signal Analyzer.

4.1 Phase Noise Versus Bias Current

The oscillation frequency and phase noise performance at an offset frequency of 100 kHz was measured with the phase noise meter for each of the four capacitor ratios. The tester

mode of the phase noise meter was used for the measurements which measures the oscillation frequency and phase noise at a fixed offset frequency rather than the slower analyzer mode which measures the full phase noise sideband of interest. The measurement was averaged over 512 measurements to increase the accuracy of the phase noise measurements. Measurements were made starting at a bias current of 2.5 mA with the bias current increased by 0.25 mA until the phase noise measurement was well past the best performance. For this set of measurements both the supply voltage and the tuning voltage were fixed at 3 volts.

FIGURE 4-2 Measured Phase Noise versus Bias Current for the Four Feedback Factors

Figure 4-2 plots the phase noise at a 100 kHz offset frequency versus bias current for the four different capacitor ratios. The measurements confirm the simulation data that the feedback factor of 0.32 has the best phase noise performance of the four designs. It also confirms that the lowest phase noise performance of -105.4 dBc/Hz occurs at a bias current near 9.5 mA.

The measured phase noise data is plotted with the simulated data in Figure 4-3 which shows excellent correlation between measured and simulated phase noise performance. The largest differential between measured and simulated phase noise performance occurs at both low currents and high currents. The discrepancy at low currents may be due to a lower tank quality factor and larger polysilicon resistances than simulated which would increase the thermal noise sources. Another source may be higher flicker noise of the active devices than modeled by simulation. The discrepancy at high currents is attributed to inaccuracies of the active device model for the full saturation operating region.

Other sources of error may be due to inaccuracies of the simulation method, device model inaccuracy, asymmetrical differences in the physical layout, and capacitor ratio mismatches. As is evident from the physical layout in Figure , a unit capacitor was not utilized for the capacitor components and as a result of this oversight capacitor values are not as accurate as possible. Building all capacitors from the same unit capacitor size (viz. a 100fF unit capacitor) would produce the most accurate capacitor ratioing but since the device C_π and the varactor diode also contribute to the capacitor ratio there is still a certain degree of inaccuracy even using a unit capacitor.

FIGURE 4-3 Measured and Simulation Phase Noise Data versus Bias Current

A plot of the measured oscillation frequency versus bias current is plotted in Figure 4-4. The measured data validates the simulations and shows the frequency initially increasing slightly with bias current and then rapidly falling off with phase noise performance. Figure 4-5 shows that the measured oscillation frequency is approximately 4 to 5% lower than simulated. The discrepancy is most likely due to extraneous parasitics of the physical layout. The measured frequency also falls off at a faster rate with bias current than the simulated data. The accelerated drop off in frequency with bias current is probably due to inaccuracies in the active device models especially in the fully saturated region.

FIGURE 4-4 Oscillation Frequency Measurements versus Bias Current for the Four Capacitor Ratios

FIGURE 4-5 Measured and Simulated Oscillation Frequency versus Bias Current

4.2 Phase Noise Sideband Measurements

To compliment the tester mode measurements, the phase noise sideband was measured for the circuit with a feedback factor of 0.32 at a bias current of 9.5 mA which was the condition that reported the lowest phase noise performance in the previous section. The spectrum output measured on the phase noise meter is shown in Figure 4-6. The measurement shows a measured output power of -1.045 dBm which is attenuated by MA/Com Power Combiner that has an insertion loss of 1.0 dB producing an actual output power of 0.045 dBm.

FIGURE 4-6 Measured Spectrum of Oscillator

FIGURE 4-7 Phase Noise Sideband Measurement

A phase noise measure for the same circuit and operating point is shown in Figure 4-7. For comparison the simulated phase noise sideband is plotted along with the measured phase noise sideband for the same operating point in Figure 4-8. There is excellent correlation between the simulated and measured performance between 20 kHz to 5 MHz as is evident in Figure 4-9 where the data is plotted over one decade. Below 20 kHz the flicker noise dominates the measured phase noise performance, whereas the flicker corner does not occur in the simulated phase noise until 2 kHz. Clearly the flicker noise models of the BATMOS process are inaccurate. Above 5 MHz the measured phase noise is limited by the noise floor of the phase noise meter.

FIGURE 4-8 Simulated and Measured Phase Noise Sidebands

FIGURE 4-9 Simulated and Measured Phase Noise Sidebands over 1 Decade

4.3 Phase Noise versus Device Headroom

Simulations indicated that the phase noise performance was limited by voltage headroom of the active devices. Simulations also showed that increasing the voltage supply or using RF chokes on the output which increase voltage headroom improve the phase noise performance. Simulations also indicate the opposite as well where phase noise performance was degraded with loss of voltage headroom by the lower supply voltage.

FIGURE 4-10 Measured Phase Noise Performance Versus Voltage Supply and with RF Choke

Figure 4-10 plots the measured phase noise of the design with a feedback factor of 0.32 with a 2.5, 3 and 5 volt voltage supply. The measured phase noise is also plotted for a 3 volt supply with RF chokes from a bias tee shunted across the output to the supply voltage. Figure 4-10 shows that measured phase noise performance does scale with supply voltage. It also shows that increasing the headroom with RF chokes shunting the output to the supply voltage also improve the phase noise performance. In fact, the RF chokes on the

output produce phase noise performance that is nearly equivalent to that of the 5 volt supply.

4.4 Phase Noise versus Tuning Voltage

The measured and simulated phase noise performance is plotted versus the tuning voltage in Figure 4-11 for a feedback ratio of 0.32 at a bias current of 9.5 mA. As confirmed by simulation the phase noise is degraded as the tuning voltage is lowered. Simulations show that the degradation is due to increased contributions due to the common resistance used to drive the tuning voltage. As mentioned previously, this resistance is required to reducing squegging effects due to simultaneous differential and common mode oscillations.

FIGURE 4-11 Measured and Simulated Phase Noise Performance versus Tuning Voltage

Figure plots the measured and simulated oscillation frequency versus tuning voltage and indicates that the oscillator has a tuning range of approximately 3%.

FIGURE 4-12 Measured and Simulated Oscillation Frequency versus Tuning Voltage

4.5 Oscillator Figure of Merit

A method of comparing oscillator performance was first reported in 1997 [Dau97a] to enable an accurate comparison between oscillators of different frequencies in which their phase noise performance was specified at different offset frequencies. This figure of merit was based on the application of Leeson's equation (2-7) and relates oscillator frequency (f_o), oscillator phase noise ($L(f_m)$) and offset frequency at which it is measured (f_m), and RF output power (P_o). Power consumption (P_{DC}), which is not directly specified in Leeson's equation, was added to the figure of merit because it is an important parameter which indicates the efficiency of the design.

Leeson's equation is restated in linear form as (4-1) and assumes that $Q_L \ll 100$ and $f_c \ll f_m$.

$$L(f_m) \cong \frac{FkT}{8P_o} \left(\frac{f_o}{Q_L f_m} \right)^2 \quad (4-1)$$

The figure of merit is then derived from Leeson's equation by grouping the performance metrics of interest on the right hand side of (4-2) .

$$FOM = \frac{8Q_L^2}{FkT} = \left(\frac{f_o}{f_m} \right)^2 \frac{1}{L(f_m) \cdot P_o} \quad (4-2)$$

As an empirical figure of merit equation (4-2) does not really make sense as it penalizes a high output power. Equation (4-2) also does not consider the power consumption of the oscillator which is an important performance metric. Therefore, equation (4-2) was modified to scale properly with the DC to RF efficiency of the oscillator resulting in equation (4-3) .

$$FOM = \left(\frac{f_o}{f_m} \right)^2 \frac{P_o}{L(f_m) \cdot P_{DC}} \quad (4-3)$$

Since its introduction, the oscillator figure of merit was modified with the removal of the oscillator RF output power P_o [Kin99]. The modified figure of merit shown in logarithmic form in (4-4) is now prevalent throughout the industry [Kin99, Plo00, Heg01]. The removal of the oscillator output power can be justified by its dependence on the technology of implementation. Integrated CMOS oscillators for instance are not required to drive low impedance loads on-chip so output power is not as important as voltage swing.

$$FOM = 10 \cdot \log \left(\left(\frac{f_o}{f_m} \right)^2 \frac{1}{L(f_m) \cdot P_{DC}} \right) \quad (4-4)$$

The oscillator figure of merit of (4-4) rewards oscillators that obtain low phase noise performance while consuming minimal power.

Equation (4-2) also states:

$$FOM = \frac{8}{kT} \cdot \frac{Q_L^2}{F} \quad (4-5)$$

or after dropping the constant $\frac{8}{kT}$,

$$FOM \propto \frac{Q_l^2}{F} \quad (4-6)$$

Equation (4-6) reaffirms the properties of optimal oscillator design. It indicates that oscillator performance is proportional to the square of the resonator loaded Q. This underlines why great research effort is being expended in the improvement of passive component quality factor. Increasing the loaded Q not only reduces the sources of noise directly but it also reduces the amount of energy needed to maintain a given tank energy. The increased Q, in effect, allows the circuit to maintain the same signal level with less noise at a lower power consumption. Equation (4-6) also implies that the performance is inversely proportional to Leeson's oscillator noise factor. In other words, the performance is proportional to the signal to noise ratio where the optimal design obtains the largest oscillator amplitude with minimal noise contribution from all noise sources.

The figure of merit proposed in (4-4), although widely used, does not fairly compare oscillator topologies when Q enhancing technologies are implemented in the circuit realization. Q enhancing technologies include the use of bond wires for inductors [Cra95, Hit97, Sve00, Sve90a, Heg01, Kuc01] and processes which implement either thicker top metallization [Van99, Jac02, Li02] or copper top level metallization [Rog01]. A further

modification to the figure of merit was proposed which groups the loaded quality factor with the performance metrics of interest in (4-2) [Zan01a]. The resulting figure of merit in (4-7) normalizes the performance with respect to loaded resonator Q .

$$FOMQ = 10\log\left(\left(\frac{f_o}{f_m}\right)^2 \frac{1}{L(f_m) \cdot P_{DC} \cdot Q_L^2}\right) \quad (4-7)$$

By including the loaded quality factor of the resonator in the figure of merit above, (4-6) now becomes (4-8) .

$$FOMQ \propto \frac{1}{F} \quad (4-8)$$

(4-8) simply states that $FOMQ$ is an inverse function of Leeson's oscillator noise factor. The $FOMQ$ in (4-7) gives us a accurate means of comparing oscillators based only on the circuit topology, the implementation of the circuit (circuit layout with parasitics), and the process technology (Si bipolar, CMOS, SiGe HBT, GaAs HBT, etc.).

4.5.1 Comparison of Existing Art

Since 1995 there has been an enormous increase in the number of fully integrated VCO's reported in the literature which has coincided with the growth of wireless communications and the desire for fully integrated digital radios. It is difficult to compare measured VCO phase noise performance directly when they have different oscillation frequencies, output powers, power consumption, tuning range, and the circuits are realized in different technologies which load the circuit differently. To complicate matters further, the offset frequency is often not the common standard of 100 kHz. Although Leeson's equation is not theoretically grounded well enough for designing oscillators directly, it is an accurate enough basis to provide a useful method of scaling VCO performance for comparison as

detailed in the above figure of merits. Table 4-2 lists a representative sample of the state of art integrated oscillator performance. The widely adopted FOM is listed for all oscillators and plotted in Figure . The FOMQ is listed in Table 4-2 but the inductor Q is used for the computation instead of the loaded resonator Q . The loaded resonator Q is seldom reported and the inductor Q is generally the limiting factor in loaded resonator Q and gives a ceiling on the achievable resonator Q .

Designs with the highest FOM are the most efficient topologies/technologies in terms of phase noise and power consumption. The FOMQ removes the benefit of inductor technology and allows the raw comparison of the Lesson's noise factor of the topology and technology.

TABLE 4-2 State of the Art Integrated VCO Performance

Reference	L(fm)	f_m (kHz)	P (mW)	f_o (GHz)	FOM	Q	FOMQ	Technology	Inductor Comments
Cra95	-115	200	24	1.76	180.09	9.8	160.26	0.7 μ m CMOS	bond wire
Ali96	-101	100	10	0.913	170.21			25GHz bipolar	spiral
Rou96	-100	100	30	0.850	163.82			1 μ m CMOS	spiral
Soy96	-92	100	54	2.36	162.13	8	144.07	12 GHz bipolar	spiral
Cra97	-116	600	6	1.80	177.76	5.7	162.64	0.7 μ m CMOS	spiral
Dau97	-105	100	28	1.50	174.05	4.69	160.63	0.8 μ m bipolar	spiral
Hit97	-94	100	5	1.80	172.12	13	149.84	25 GHz bipolar	bond wire
Jan97	-105	100	40.5	1.10	169.75	9	150.67	15GHz bipolar	spiral
Wak98	-123	600	43.2	1.90	176.66	8	158.60	40 GHz bipolar	spiral
Zan98	-136	4700	32.4	2.00	173.47	4	161.43	25GHz bipolar	spiral
Van99	-118	2000	0.8	1.30	175.23	16	151.14	bipolar SOA	spiral Q=16
Zan99	-139	4700	29.7	1.56	174.69	6	159.13	25GHz bipolar	spiral
Cop00	-100	100	17.5	3.91	179.41	12	157.83	47 GHz SiGe	spiral
Kle00	-129	3000	18	2.40	174.51	10	154.51	75 GHz SiGe	spiral
Rog00	-103	100	10.56	1.70	177.37	5.5	162.57	25 GHz bipolar	spiral
Sve00	-119	600	12	1.30	174.92	4.5	161.86	0.35 μ m CMOS	spiral + bond wire
Sve00a	-120.5	600	2	1.90	187.50	35	156.62	0.35 μ m CMOS	bond wire
Voi00	-87	100	50	26.0	178.31	14	155.39	47 GHz SiGe	spiral
Heg01	-153	3000	9.25	1.20	195.38	13	173.10	0.35 μ m CMOS	2.5 μ m metal Q=13
Kuc01	-114	100	12.2	2.05	189.37			0.25 μ m CMOS	bond wire
Rog01	-106	100	18.15	2.00	179.43	17	154.82	25 GHz bipolar	Cu spiral Q=17
Sam01	-104	100	14	2.60	180.84	8	162.78	20 GHz bipolar	Q=8
Zan01	-104	100	14	2.50	180.50	8	162.44	20 GHz bipolar	Q=8
Jac02	-104	100	29.7	6.30	185.26			47 GHz SiGe	4 μ m metal
Li02	-108.5	1000	280	47.3	177.53	9	159.46	70 GHz SiGe	2.8 μ m metal
Rog02	-103	100	21	2.20	176.63	7	159.72	25 GHz bipolar	spiral

FIGURE 4-13 Figure of Merit of State of the Art VCOs

FIGURE 4-14 FOMQ of State of the Art VCOs

The data from Figure shows that the oscillator figure of merit has been improving greatly in the last several years. The top performers make use of exotic techniques or specialized processes like the use of bond wire inductance in the resonator [Cra95, Hit97, Sve00, Sve00a, Heg01, Kuc01], processes with specialized top metal thickness [Van99, Jac02, Li02], or exotic metals like copper [Rog01]. Figure 4-14 which plots the FOMQ also confirms that most of the improvement has been in the quality factor of the resonator passive components with the exception of Heg01.

The performance reported in this work is referenced as Dau97 and ranks in the top 8 designs based on FOMQ. It should also be noted that Dau97 is within 2dB (as FOM and FOMQ are based on logarithmic scales) of the all of the top 8 designs except for the Heg01 design. It should also be noted that FOMQ does not compensate for the noise figure of the active devices and that as stated in Chapter 3 the Nortel BATMOS process is not optimized for RF applications. A more advanced RF specific process may improve the FOMQ of the proposed topology placing it closer to the top performers. The designs Cop00, Voi00, and Li02 are also based on the differential common Colpitts topology and though implemented in RF specific process their performance may not be optimized for maximum FOMQ using the proposed methodology.

The Hegazi design [Heg01] is demonstratively better than all reported design to date and benefits from several factors. In general, CMOS VCO's have outperformed bipolar VCO's as reported in the literature even with their higher flicker corners. The benefit of CMOS is reported to be that the oscillation frequency of the designs are insensitivity to bias current disturbances[Sam01]. Another benefit of CMOS is due to the larger linear input range of the active devices. This allows the full resonator voltage to be presented across the active device without having to capacitively or inductively step down the voltage. The physical parasitics are reduced without the extra components and the resonator quality improved.

The Heg01 design makes further improvements on the CMOS design by further filtering noise from the bias current to attain its performance.

5.1 Summary

The work presented in this thesis proposes a new balanced oscillator architecture which demonstrates low phase noise performance while consuming minimal power while realized in a fully integrated implementation. Based on a widely accepted figure of merit, the performance is favourable in comparison to the present state of the art. The proposed circuit has met its goal of serving as a general purpose architecture and the performance of the experimental prototypes meets the requirements for several applications including cable modem applications, set top box television tuners, cordless phones, GPS receivers, and some types of wireless LAN transceivers. The topology has even been implemented by others in RF oriented technologies at higher frequencies and has produced similar state of the art performance [Cop00, Voi00, Li02].

This work also was the first to propose the use of an oscillator figure of merit to enable an accurate comparison of the key performance metrics of different oscillator architectures regardless of frequency. The figure of merit originally proposed in this work has been modified slightly [Kin99] and is now widely accepted in the literature. Still others have modified the figure of merit by adding tuning range, resonator Q, and other parameters to showcase their particular oscillator [Ham01, Zan01a]. The figure of merit has proven to be a very useful tool for comparing efficient oscillator topologies for low power applications.

A general methodology was detailed to target the lowest phase noise performance using the proposed topology from a chosen technology and supply voltage. This methodology was verified through the simulation and measurement of the proposed topology. The methodology is based on the description of an ideal oscillator topology and the application of an LTV analysis to model the phase noise mechanisms of the circuit. Cadence's SpectreRF simulation tool was used as the simulator in the design methodology. Although this simulator proved to be accurate and much faster than a technique such as LTV simulation, the simulator often had convergence issues depending on the operating point. Manipulation of the convergence parameters was required to get convergence for all operating points and led to a piecewise solution. Recently, harmonic balance simulators have promised improved convergence while maintaining accuracy [Ngo00, Ngo00a].

Performance trade-offs were discussed to tune the performance of the design to the application requirements where it was demonstrated that phase noise performance of the proposed topology can be scaled with power consumption. It was also shown that device saturation will limit the ultimate phase noise performance. Certain applications, which are not power budget limited or voltage limited, may be able take advantage of larger supply voltages and higher bias currents to achieve improved phase noise performance. These are designs in which the importance is on absolute phase noise performance regardless of power consumption rather than achieving the highest figure of merit.

5.2 *Further Research*

The result of this work should be extended to other Colpitts topologies and other technologies. The implementation of the proposed topology and design methodology into other topologies would allow a direct comparison of the technologies without masking by the topology. The implementation of other topologies in the same technology would allow the direct comparison of topologies without masking by the technology.

Some of the recently reported circuit ideas should also be implemented in the common collector Colpitts architecture to improve the FOMQ. Two such ideas are the inclusion of inductive filtering in the current source [Heg01] and the noise shifting Colpitts current source proposed by [Apa02]. This would also allow further comparison between CMOS and bipolar technologies.

There is increasing interest in the use of direct downconversion radio architectures to reduce power and complexity. To assist with this goal, further research should also investigate the modification of the proposed architecture into a quadrature architecture as these circuits have suffered in phase noise performance in the past [Jac02].

Finally, the performance of a CMOS implementation of the architecture should be investigated and evaluated against the performance of the commonly used cross-coupled differential LC CMOS oscillator [Haj99, Heg01]. Standard digital CMOS is the cheapest, widely available technology and allows the highest levels of integration. An even more challenging goal, will be the design of low phase noise oscillators at voltage supplies of 1V or lower. The voltage supplies of digital CMOS technologies are scaling proportionally to the minimum feature size due to limitations of the breakdown voltages. Voltage supplies of 1V or less will lower the oscillation amplitude and reduce the achievable phase noise performance, as well as, reduce the voltage swing available for the tuning range [Sam02].

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