# SILICON PHOTONICS: COUPLING, PROPAGATION AND MODULATION OF LIGHT IN SILICON

by

KUAN PEI YAP

A Thesis Submitted to
The Faculty of Graduate Studies and Research
in Partial Fulfillment of the Requirements
for the Degree of
Doctor of Philosophy

Ottawa-Carleton Institute for Electrical and Computer Engineering
Department of Electronics
Carleton University
Ottawa, Ontario, Canada

May 2009

*Your file Votre référence*
*ISBN: 978-0-494-52089-5*
*Our file Notre référence*
*ISBN: 978-0-494-52089-5*

# Abstract

Several technical challenges remain to be addressed for making silicon photonic chips a manufacturing commodity. These challenges include coupling light in and out of the photonic chip with minimum optical loss, propagating light in the silicon-on-insulator (SOI) waveguides with low scattering loss, as well as modulating light with a reliable actuation mechanism that is well understood. The objective of this thesis research is to develop a silicon photonic chip with integrated passive (*e.g.* routing) and active functions (*e.g.* modulation). To achieve the thesis objective, these technical challenges must be addressed.

The challenge of reducing coupling loss between the optical fibers and SOI waveguides can be addressed by using couplers or mode converters in combination with high quality optical facets. An etch-and-cleave method has been developed in this research to fabricate high quality facets with vertical sidewalls at the desired locations on the SOI wafers, in order to reduce coupling loss. The challenge of reducing propagation loss due to scattering in the SOI waveguides can be addressed by minimizing roughness at the waveguide sidewalls. A scattering loss measurement technique using integrated optical star couplers has been developed to allow efficient collection of loss data, and a robust low-loss SOI waveguide fabrication process has been demonstrated successfully. To accomplish modulation function in the silicon photonic chip, the thermo-optic effect and heat flow dynamics in silicon have been studied extensively using a finite-difference simulator. As a result of the simulation study, a set of design and optimization guidelines for SOI thermo-optic switches based on Mach-Zehnder Interferometer (MZI) configuration has been established, which can be a relevant and useful guide to optical switch designers.

# Acknowledgements

I would like to thank my supervisor Siegfried Janz for his inspiration, guidance and patience throughout the course of my graduate studies. I am also very grateful to my thesis supervisor, Professor Barry Syrett, for his advice and restless efforts in providing crucial financial support for me to continue my study. Without their support, the completion of this thesis would not have been possible.

I am also very lucky to have learned and received countless helps from a pool of exceptionally talented people from the Optoelectronics and Nanfabrication groups in the Institute for Microstructural Sciences (IMS) at the National Research Council of Canada (NRC). There are so many who have made key contributions to my research: Jens Schmid, Philip Waldron, André Delâge, Adam Densmore, Dan-Xia Xu, Boris Lamontagne, Jean Lapointe, Pavel Cheben, Margaret Buchanan, Phillip Chow-Chong, Pedro Barrios, Mark Malloy, Hue Tran, and many others. My sincere thanks go to André, Boris, Jens, Phil and Adam for their enthusiasm in answering my many trivial questions about theory and experiments in optics, and for their consistent encouragement that kept me staying on course in my pursuit to complete this thesis. A special thank should also go to Edith for her assistance with optical measurement and the forever friendly smiles on her face.

Of course this thesis would not have been completed without insightful advice and many innovative ideas from my thesis committee, especially from Professor Tom Smy and Professor Garry Tarr. The thermal simulation software used in the study of thermo-optic modulation in this thesis was developed by Prof. Smy. On setting up and familiarizing with the simulation software, I have also received invaluable help from my fellow classmates Dritan Celo and Peter Chyurlia.

Many thanks to Ms. Blazenka Power and Peggy Piccolo who have always been extremely helpful with the administrative tasks in the department, making my life as a

graduate student much more delightful and less worrisome. I want to thank all my friends in the university: Lingyun Xiong, Chengkun Cheng, Ksenia Yadav, Bashir Morshed, Hoang Nguyen, Sandy Ng, Michael Riemer, Simon Frederick and Dale Armstrong, who have motivated me on many occasions by sharing their knowledge and stories about graduate studies. I am also very thankful to my close friends Eng Kooi Lim, Chiew Leong Saw, Jacky Teh, Angelina Lee-Chan and Joy Chen, for their support, their friendship and many cherishing moments in life together.

I want to thank my sisters Vicki, Rose and my brother Mike for their love, understanding and encouragement. Finally and most of all, I dedicate this thesis to my late parents, Ik Kim and Sok Ching, both passed away during the course of this Ph.D. study. For their unconditional love and unwavering support, this thesis is part of their legacies.

# Table of Contents

# List of Figures

# List of Tables

# List of Acronyms

| | |
|---|---|
| **AFM** | Atomic Force Microscopy |
| **AWG** | Arrayed Waveguide Gratings |
| **BOX** | Buried Oxide |
| **CWG** | Channel Waveguide |
| **DC** | Direct Current |
| **FDM** | Finite Difference Method |
| **FMM** | Film Mode Matching |
| **GRIN** | Graded Index |
| **ICP** | Inductively-Coupled Plasma |
| **MZI** | Mach-Zehnder Interferometer |
| **NMP** | n-Methyl Pyrrolidone |
| **OADM** | Optical Add-Drop Multiplexing |
| **OXC** | Optical Cross-Connect |
| **PECVD** | Plasma Enhanced Chemical Vapor Deposition |
| **ROADM** | Reconfigurable Optical Add-Drop Multiplexer |
| **RWG** | Ridge Waveguide |
| **SEM** | Scanning Electron Microscopy |
| **SOI** | Silicon-On-Insulator |
| **TE** | Transverse Electric |
| **TM** | Transverse Magnetic |

# Statement of Thesis Contributions

The results of this thesis will contribute to the understanding of technical challenges associated with the development of silicon photonic chips. The challenges include coupling light into and out of the photonic chip with minimum optical loss, guiding light in SOI waveguides with low scattering loss, as well as modulating light to accomplish switching and routing functions. A number of passive and active devices have been designed, fabricated and characterized, which can be used as basic building blocks for a silicon photonic chip. A list of publications from the results of this thesis research is given in the next section. The author's specific contributions to the research are as follows.

***Contributions on the topic of input-output coupling***

The input-output coupling of light to and from the on-chip waveguides has been studied in this thesis (as presented in Chapter 2). A novel etch-and-break fabrication process for optical facets and trenches has been developed successfully and demonstrated experimentally. The major contributions of the author in this project are the full-time involvement in process development, device fabrication and optical testing. More specifically, the idea of depositing a layer of Al on the end faces of the exposed waveguides during deep trench etching was proposed by the author, and the fabrication of the test samples was completed in part by the author, with the help from B. Lamontagne

at NRC. This project was completed with one conference presentation and seven publications (one first-author journal paper and six co-author journal and conference papers).

***Contributions on the topic of waveguide scattering loss***

The waveguide scattering loss issue has also been addressed in this thesis (as presented in Chapter 3). Key process improvement steps have been developed by the author to significantly reduce the scattering loss in an optimized SOI waveguide fabrication process employing e-beam lithography and Cr hardmask. For this Cr hardmask process, the author introduced an oxygen ashing step that is proven effective in removing resist residues in between any two closely-spaced waveguides. An effective loss-measurement technique using optical star coupler has also been demonstrated experimentally by the author, through fabricating all test samples, performing optical testing, sidewall roughness measurement using SEM and theoretical modeling using Payne-Lacey scattering loss equation. The author has modified the Payne-Lacey model to calculate the scattering loss in ridge waveguides by introducing a scaling factor to account for the variation in the etch depth of the waveguides. The author has also successfully correlated the measured sidewall roughness with measured optical scattering loss using the modified Payne-Lacey model, which is an original contribution to the theory of scattering loss in ridge waveguide.

This project has been completed with two international conference presentations

and two journal publications. The two conference presentations include an oral presentation given in the *SPIE Photonic West Conference*, San Jose in January 2007, and an award-winning poster presentation in the *SPIE Microelectronics, MEMS, and Nanotechnology Conference* at Canberra, Australia in December 2007.

***Contributions on the topic of thermo-optic modulation***

The design and simulation of 1×1 Y-branch MZI SOI switches have been accomplished through the study of thermo-optic modulation in Si (as presented in Chapter 4). Several material and geometrical parameters have been studied by the author through optical and thermal simulation and have been found to be instrumental in the optimization of speed and power consumption of the switches. The author is the first to propose the use of silicon nitride upper cladding layer to improve the switching speed, and to demonstrate that increasing MZI arm spacing can reduce power consumption. The effect of device scaling on the switching performance has also been accomplished by the author, which is an important aspect of design for more compact Si thermo-optic switches or modulators, in response to the demands for miniaturization of photonic chips (as presented in Chapter 5). The author is the first to show that power-scaling or speed-scaling trend follows a parabolic curve, and that there is an optimum waveguide geometry corresponding to an optimum switching speed and power.

Process development of the SOI thermo-optic switches were completed and a number of testable samples were fabricated by the author. The test results of the power

consumption of the samples agree very well with the simulation, therefore validating the procedures and accuracy of the simulation by the author. The contributions of the author in the study of thermo-optic switches are in device design, optical and thermal simulations, device fabrication, optical testing and device optimization through simulation.

# List of Publications

1. **K. P. Yap**, A. Delâge, J. Lapointe, B. Lamontagne, P. Waldron, J. H. Schmid, B. A. Syrett, and S. Janz, "Correlation of scattering loss, sidewall roughness and waveguide width in silicon-on-insulator (SOI) ridge waveguides", *IEEE J. Lightwave Technology*, accepted, Feb 2009.

2. J. H. Schmid, A. Delâge, J. Lapointe, B. Lamontagne, S. Janz, P. Cheben, A. Densmore, D.-X. Xu and **K. P. Yap**, "Thin-film interference effect in scattering loss of high-index-contrast planar waveguides", *IEEE LEOS Meeting 2008,* paper ThP2, Newport Beach, CA, Nov 2008.

3. J. H. Schmid, A. Delâge, B. Lamontagne, J. Lapointe, S. Janz, P. Cheben, A. Densmore, P. Waldron, D. -X. Xu and **K. P. Yap**, "Interference effect in scattering loss of high-index-contrast planar waveguides caused by boundary reflections", *Optic Letters*, vol. 33, no. 13, pp. 1479-1481, Jul 2008.

4. **K. P. Yap**, J. Lapointe, B. Lamontagne, A. Delâge, S. Janz, B. Syrett, "Process development of integrated SOI star couplers for waveguide scattering loss measurement", *SPIE Proc. Microelectronics, MEMS, Photonics and Nanotechnology IV*, vol. 6800, no. 680014, pp. 1-12, Jan 2008.

5. **K. P. Yap**, A. Delâge, B. Lamontagne, S. Janz, D. -X. Xu, J. Lapointe, P. Waldron, J. Schmid, P. Chow-Chong, E. Post, B. Syrett, "Scattering loss measurement of SOI waveguides using 5x17 integrated optical star coupler", *SPIE Proc. Photonics West: Silicon Photonics II*, vol. 6477, no. 64770J, pp. 1-11, Feb 2007.

6. S. Janz, P. Cheben, D. Dalacu, A. Delâge, A. Densmore, B. Lamontagne, M.-J. Picard, E. Post, J. H. Schmid, P. Waldron, D.-X. Xu, **K. P. Yap**, W. N. Ye, "Microphotonic elements for integration on the silicon-on-insulator waveguide platform", *IEEE J. Sel. Topics on Quan. Elec.,* vol. 12, no. 6, pp. 1402-1415, Nov/Dec 2006.

7. S. Janz, P. Cheben, A. Delâge, A. Densmore, B. Lamontagne, E. Post, J. Schmid, P. Waldron, D. -X. Xu, **K. P. Yap**, W. N. Ye, "Silicon microphotonic waveguide technology for sensing, spectroscopy and communications," in *Science and Technology of Dielectrics for Active and Passive Photonic Devices, eds. P. Mascher, D. Misra, K. Worhoff, 2006 ECS Meeting, Electrochemical Society*

*Transactions*, vol. 3, no. 11, pp. 61-78 (2006).

8. **K. P. Yap**, B. Lamontagne, A. Delâge, S. Janz, A. Bogdanov, M. Picard, E. Post, P. Chow-Chong, M. Malloy, D. Roth, P. Marshall, K.Y. Liu, and B. Syrett, "Fabrication of Lithographically-defined Optical Coupling Facets for SOI Waveguides by ICP Etching", *J. Vacuum Sci. & Tech. A,* vol. 24, no. 3, pp. 812-816, May/Jun 2006.

9. A. Delâge, S. Janz, B. Lamontagne, A. Bogdanov, D. Dalacu, D. -X. Xu, and **K. P. Yap**, "Monolithically Integrated Asymmetric Graded and Step-index Couplers for Microphotonic Waveguides," *Optics Express*, vol. 14, no. 1, pp. 148-161, Jan 2006.

10. S. Janz, A. Delâge, B. Lamontagne, A. Bogdanov, D. Dalacu, D.-X. Xu, and **K. P. Yap,** "Monolithically integrated graded-index waveguide input couplers for silicon photonics," at *SPIE Photonics West: Silicon Photonics Conference*, San Jose, CA, Jan 2006.

11. S. Janz, B. Lamontagne, A. Delâge, A. Bogdanov, D. Dalacu, D. –X. Xu, and **K. P. Yap**, "Single Layer a-Si GRIN Waveguide Coupler with Lithographically Defined Facets," *IEEE Proc. Group IV Photonics,* pp. 129-131, Sep 2005 (CD-ROM, Institute of Electrical and Electronics Engineers, Piscataway, NJ, 2005).

12. S. Janz, P. Cheben, A. Delâge, B. Lamontagne, M. -J. Picard, D. –X. Xu, **K. P. Yap**, and W. N. Ye, "Enabling Technologies for Silicon-based Microphotonics," in *Integrated Photonics Research and Applications/Nanophotonics for Information Systems Topical Meetings on CD-ROM* (The Optical Society of America, Washington, DC, 2005), paper IMB1.

13. S. Janz, A. Bogdanov, P. Cheben, A. Delâge, B. Lamontagne, M.-J. Picard, D.-X. Xu, **K.-P. Yap**, W.N. Ye, "Silicon-based Integrated Optics: Waveguide Technology to Microphotonics," (invited), *Materials Research Society Proceedings*, vol. 832, (Materials Research Society, 2005).

# CHAPTER 1

# INTRODUCTION

## 1.1. MOTIVATION FOR SILICON PHOTONICS RESEARCH

Photonics is the technology associated with generation, processing, transmission and detection of signals that are carried by photons [1.1]. The principal photonic devices are lasers, waveguides, modulators, detectors and optical fibers [1.1, 1.2]. In the past decades, photonic technology has become increasingly important in many applications [1.1-1.6], such as optical interconnects for telecommunication and data communication, health care and pharmaceuticals, green and sustainable energy, environmental monitoring and national security etc. The global photonics industry is projected to worth US$493 billion in revenue by 2020 [1.7, 1.8].

The recent explosion in internet and data communication has expedited the footsteps of globalization [1.2, 1.3, 1.9]. Communication bottlenecks are now no longer confined by the speed within a computer, but rather the rate at which data can travel between a processor and the outside world [1.3]. The need to transmit data exceeding the rate of 1 Gb/s [1.2] and at a larger bandwidth demands a technology that can overcome the limitations of the copper-wire based electrical interconnects. To fulfill this need, optical interconnects has emerged as the replacement technology. In fact, over the last

decades, fiber-optic communication links have rapidly replaced copper cables in the long haul and metropolitan communication networks that are running over 0.1 to 80 km. This trend has now expanded steadily into the local area networks (LAN), which are running over a shorter distance of 1-100 m. At this distance, because the cost of implementation for fiber-optic links is relatively competitive, both copper and optical interconnects coexist.

The future of optical interconnects in the shorter distance networks of 100 m or less, such as rack-to-rack, board-to-board or even chip-to-chip, rests on the ability to develop more efficient and lower cost optical solutions in place of the existing copper interconnects [1.2-1.6]. Existing photonic devices in the fiber-optic links consist of expensive discrete components that are mostly fabricated using III-V compound semiconductors, such as gallium arsenide (GaAs) or indium phosphate (InP), and electro-optic crystal such as lithium niobate ($LiNbO_3$). Because the components are manufactured discretely and assembled with very little automation, the cost of production for these photonic devices is high. The goal of high-efficiency low-cost optical solutions can only be achieved by mass producing integrated photonic chips using wafer-level automation, in the same manner that the silicon microelectronic integrated circuits are produced.

While silicon industry can provide the apparent cost benefit in mass-producing photonic integrated circuits, its mature technological infrastructure in micromachining and chip packaging offers an additional thrust to the goal of wafer-level manufacturing. The availability of this infrastructure supplies a low cost assembly line to the realization

of silicon photonic commercialization. For instance, micromachining techniques to create U-grooves and V-grooves in a silicon substrate for passive alignment of optical fibers are readily available, and packaging techniques such as flip chip bonding and pin-grid array (PGA) packaging of silicon chips are already widely used in production.

Intel's vision for integrating a tera-scale system starting from a silicon photonic chip is the best example to illustrate the concept of future optical interconnects [1.4], as shown in Fig. 1.1(a).

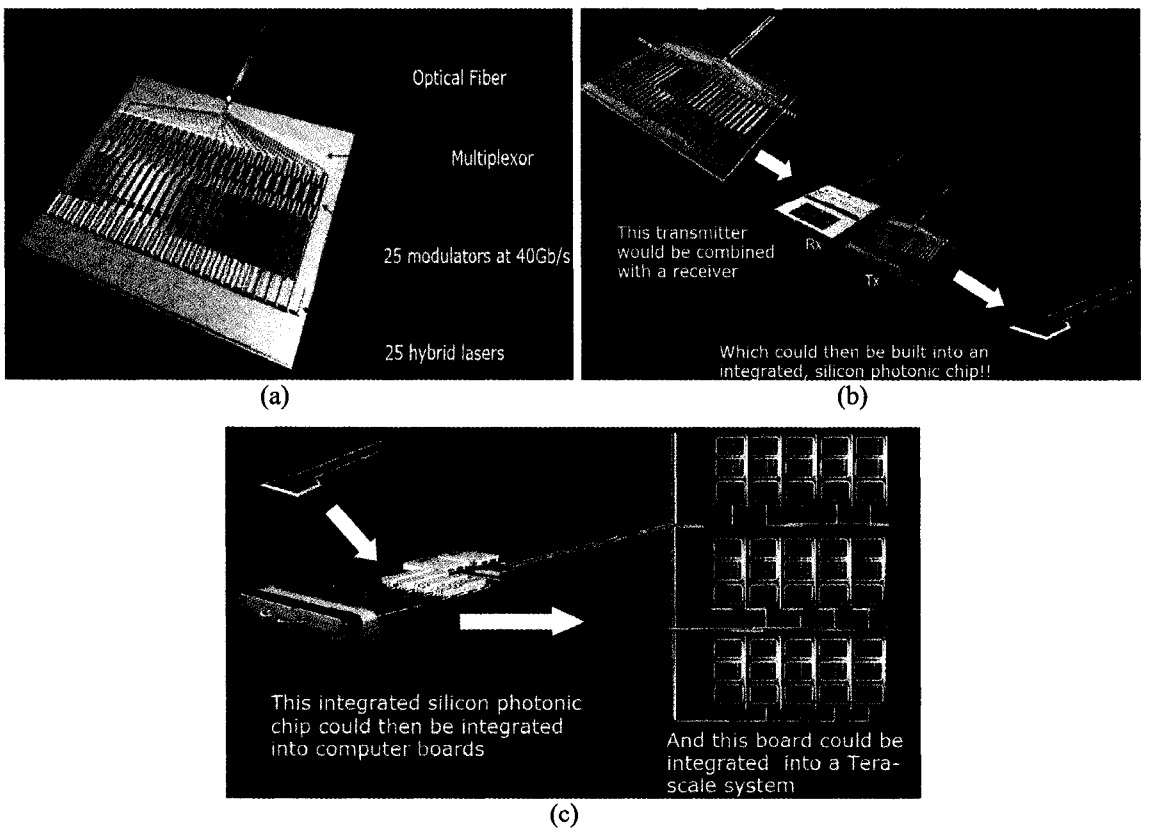



Fig. 1.1. Intel's vision of a tera-scale system with optical interconnects made of silicon-photonic chips [1.4].

Intel envisions the realization of a monolithically integrated silicon tera-hertz

transmitter constructed by 25 lasers and modulators modulating at 40 Gb/s. Transmitting the multiplexed signals from the 25 modulated lasers to an optical fiber, this transmitter can be combined with a receiver that receives multiplexed signals from another optical fiber, into an integrated silicon photonic chip, as shown in Fig. 1.1(b). The integrated silicon photonic chip could then be incorporated into a computer board, which could be further integrated into a tera-scale system, as shown in Fig. 1.1(c). This system will encompass all on-chip, chip-to-chip and board-to-board optical interconnects running at tera-hertz rate with ultra-high level of integration and functionality.

In short, the major driving force of silicon photonics is its compatibility with the mature silicon IC manufacturing [1.2-1.6, 1.10-1.11], leading to a convergence of technological sophistication and economics-of-scale.

## 1.2. ADVANTAGES AND LIMITATIONS OF SILICON PHOTONICS

Silicon has in fact many creditable optical properties that favor photonics integration. The bandgap at 1.1 eV renders silicon transparent at the 1.55 μm telecommunication wavelength, which makes silicon waveguides perfect for guiding the light at this wavelength without absorption loss. Silicon photonic devices are compatible with CMOS fabrication and therefore can be integrated with the microelectronic circuits. These silicon photonic devices offer advantages of scalability to very small size and the ability to control light at sub-wavelength scale [1.12]. As the wavelength of the light guided in a medium scales inversely with the refractive index, $n$, of the medium, the dimensions of photonic devices that are limited by interference and diffraction effect will

also scale inversely with $n$. Given an index of $n$ = 3.476 at the telecommunication wavelength of $\lambda$ = 1550 nm, in silicon the effective wavelength of the guided light is $\lambda/n$, or approximately 450 nm. This implies that many photonic devices such as diffraction gratings can be made smaller in silicon than in other materials with lower refractive index, i.e. silica with a refractive index of 1.45.

In addition, compared to other waveguides, a distinguishing property of silicon waveguide is the tight optical confinement made possible by the high index contrast between the silicon core ($n$ = 3.4) and silicon oxide ($n$ = 1.4) cladding. This high index contrast ($\Delta n$ = 2) allows the miniaturization and large-scale integration of photonic devices, because the tight optical confinement minimizes the bending loss and therefore permits smaller devices with sharper bend radius [1.6,1.12,1.13]. For instance, it is possible to fabricate array waveguide gratings (AWG) in a silicon chip with a few millimeters in dimension [1.12]. The high index contrast also makes silicon ideal for realization of photonic crystal devices, as the optical confinement minimizes radiation into the substrate and reduces optical loss [1.2, 1.5, 1.6]. The feature size of these silicon integrated photonic devices would be on the order of 0.5-2 μm [1.2, 1.3]. This dimension requirement is easily achievable by processing equipment in today's silicon electronic industry. Even for the fabrication of photonic crystal devices, current state-of-the-art deep UV steppers and plasma etchers have the full capacity to print feature size down to 65 nm [1.5, 1.6]. As a result, a myriad of high performance passive devices has been realized [1.2, 1.5, 1.6, 1.12, 1.14].

The tight optical confinement and the reduction of diffraction limit in silicon waveguides give the photonic designer the ability to manipulate light at sub-wavelength scale. This ability opens up a large window of opportunity for unique applications in the discipline of nanophotonics and biophotonics [1.5, 1.12, 1.15].

Other advantages of silicon photonics are the existence of refractive index modulation mechanisms and nonlinear optical effects. Refractive index modulation mechanisms such as the thermo-optic effect (which will be discussed in details in Chapter 4 and 5) and plasma dispersion effect (through free carriers injection) [1.2, 1.3, 1.5, 1.6] enable the creation of silicon modulators or switches that can modulate optical signals. Nonlinear effects such as Raman scattering (1000 times stronger than those in glass fiber) present possible means to construct optical amplifier and wavelength converters in silicon [1.5, 1.6].

While many silicon passive photonic devices have been developed, the lack of efficient light sources, including both light emitting diodes (LEDs) and electrically-pumped silicon lasers, has become a major deficiency in the integration of passive and active silicon photonic devices [1.5]. Due to the indirect bandgap of silicon [1.2, 1.3, 1.5, 1.6], radiative recombination of electrons and holes is very inefficient. Without these light sources, a complete suite of the photonic components cannot be realized through monolithic integration on a silicon chip [1.5]. Nevertheless, even without on-chip laser or LEDs, a silicon chip is still an excellent platform for hybrid integration with III-V light sources because of the various micromachining technologies developed that can facilitate alignment and assembly of III-V light sources on chip [1.4, 1.5].

The bandgap energy of 1.1 eV in silicon has also prevented the realization of high-responsivity silicon photodetectors capable of detecting 1550 nm wavelength light [1.3, 1.16]. The bandgap energy limits the detectable wavelength to below 1.1 μm [1.3, 1.5, 1.16]. In order to extend the detection range to 1.55 μm, germanium (Ge) layers were grown on silicon (Si) substrates [1.13, 1.17, 1.18]. Companies such as Luxtera and BAE System have shown great interest in the integration of these Ge-on-Si photodetectors with other silicon photonic devices [1.5].

Another limitation of the optical properties of silicon is the absence of strong electro-optic effects desirable for refractive index modulation. The strong Pockels effect responsible for ultra-fast modulation in $LiNbO_3$ crystal is absent in silicon [1.3, 1.5]. Nevertheless, high speed silicon modulators are still realizable using charge inversion effect in a MOS capacitor or generation of free carriers in a *pn* junction, as demonstrated by Intel [1.19], Luxtera [1.20] and other researchers [1.5, 1.6]. On the other hand, thermo-optic silicon modulators and switches operated in the range of microsecond to millisecond are suitable candidates for many telecom applications that require low power, medium speed switching, such as optical cross-connect (OXC) and optical add-drop multiplexing (OADM) [1.2, 1.3, 1.13].

## 1.3. TECHNICAL CHALLENGES OF SILICON PHOTONICS INTEGRATION

Although silicon photonics appears to be an emerging technology for various applications in communication, imaging, medical diagnosis, and many other areas, new

technical challenges have been encountered in the integration of silicon photonic devices and will have to be addressed in order for the integrated silicon photonic chip to be functional. Among all, there are three major challenges that are becoming more prominent as the feature size of the devices shrinks. The first challenge is the high coupling loss resulted from the modal mismatch and facet reflection between silicon waveguides and the external glass fiber waveguides. To illustrate this effect, one may consider a silicon-on-insulator (SOI) structure, as shown in Fig. 1.2(a).

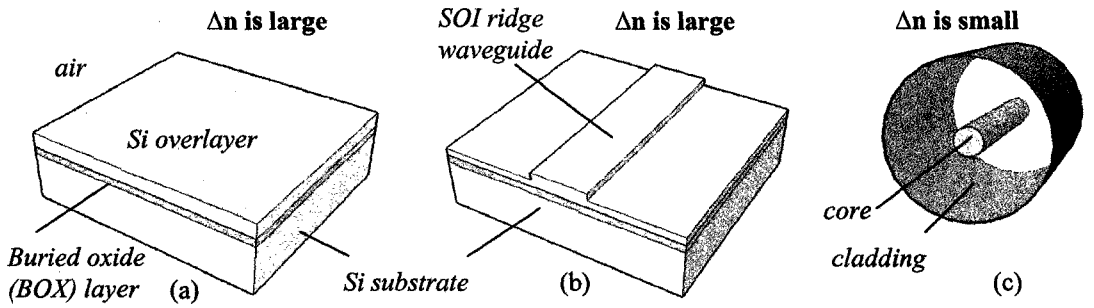



Fig. 1.2. Schematic views of (a) an SOI slab waveguide, (b) an SOI ridge waveguide, and (c) a silica glass fiber waveguide.

This three-layer SOI structure is essentially an optical waveguide, because light can be confined and guided within the high-refractive-index, top silicon slab layer by total internal reflection. The refractive index contrast of this SOI slab waveguide is relatively high, $\Delta n = 2$. As mentioned previously, in this high index contrast system, light is tightly confined vertically in the Si core layer. A ridge waveguide can be formed by etching a rectangular strip partially into the Si layer, as shown in Fig. 1.2(b). If the etch depth and the ridge width are controlled carefully, a single mode waveguide can be

obtained. The width of these single-mode SOI ridge waveguides is generally in the order of 1 μm and the mode size is also in the same order because of the tight optical confinement.

On the contrary, a glass fiber waveguide which consists of circular core and cladding layers usually has a larger mode size of 8 to 10 μm, because of the low index step between core and cladding [1.12]. As shown in Fig. 1.2(c), a typical glass fiber waveguide will have an index contrast of about one percent (eg. $n_{core}$ = 1.462, $n_{clad}$ = 1.44). The low index contrast limits the size of the core to above 3 μm [1.12] to prevent the mode from delocalizing and expanding into the cladding. At the same time, the core size is also limited by the single-mode criterion [1.16, 1.21] to be kept below about 6 μm [1.12]. As a result, most commercially available single-mode glass fiber waveguides are guiding light with a mode size of approximately 8 to 10 μm. When the SOI ridge waveguides are butt-coupled to the single-mode glass fiber waveguides, their mode size difference (or modal mismatch) results in a significant loss in optical power.

Another major contributor to the coupling loss is the reflection and scattering at the input/output optical facets. An optical facet is the edge of a silicon photonic chip where the waveguide end faces are defined. To transmit the light from a glass fiber waveguide into an SOI waveguide with low optical loss, the SOI waveguide end face needs to be smooth in texture, vertical, and precisely aligned to the fiber waveguide. Similarly, to transmit the light out of the SOI waveguide into a photodetector, the waveguide end face at the output facet also needs to be smooth and vertical. This requires

both input and output optical facets to be smooth and vertical. The existing method to prepare smooth and vertical facets is to polish them after dicing. In wafer-level manufacturing of photonic chips, this method becomes labor-intensive and costly. Cleaving of a wafer to obtain smooth facets is also difficult because the cleaved facets of SOI wafers can be rough and non-vertical due to the ductile fracture in the buried oxide layer. Overcoming the technical challenge of preparing smooth optical facets with a less labor-intensive, manufacturing-compatible technique is therefore a crucial step towards the high-volume production of silicon photonic chips. The study of SOI waveguide coupling loss will be addressed in Chapter 2, and a technique to prepare the optical facets will be introduced.

In addition to this coupling loss, two other main technical challenges associated with the design and fabrication of SOI waveguides are scattering loss and sensitivity to the polarization state of the incoming light. The scattering loss is caused by the presence of roughness at the interface between core and cladding layer, and increases rapidly with index contrast and decreasing waveguide width [1.2, 1.12, 1.22]. The challenge is therefore to minimize the scattering loss by reducing the roughness, through refining pattern-transfer processing steps involving lithography and dry etching. The characteristics of waveguide roughness and the optimization of processes to reduce it will be addressed in detail in Chapter 3.

The polarization sensitivity, on the other hand, is concerned with the dependence of the waveguide effective index and mode shape on the polarization of the light. The effective index difference for the two polarization states, one whose electric field vector

is parallel to the waveguide plane (known as transverse electric, or TE mode), and the other whose field vector is perpendicular to the waveguide plane (known as transverse magnetic, or TM mode), can be as large as $10^{-2}$ in SOI waveguides [1.10]. This large difference is a result of the large discontinuity in the dielectric constant at the interface between Si waveguide and its surrounding. Because of this large discontinuity, the profiles of the guided modes can vary strongly with the polarization state. This implies that the coupling loss, propagation loss and dispersive response of the guided modes in the SOI waveguide will vary with the polarization state of the incoming light. However, the polarization dependence of SOI waveguides can be controlled by the geometry and stress in the waveguide core. It is possible to choose the film stress and waveguide dimensions to minimize this polarization dependence. D. –X. Xu *et al.* from NRC have studied the effect of film stress on the polarization sensitivity of SOI waveguides extensively and have proposed the use of polarization management techniques [1.23, 1.24]. The merits of their studies are, however, beyond the scope of this thesis.

## 1.4. MINIATURIZATION OF SILICON PHOTONIC CHIPS

Due to the investment by global photonic industry and government agencies in the past decade, research groups over the world have successfully developed electro-optic modulators with modulation frequencies of 10-100 Gb/s, ultrafast Ge-on-Si photodetectors, efficient fiber-to-waveguide couplers and Raman lasers on Si [1.5]. In order to continue advancing the frontier of current silicon photonics research, there is an ongoing push toward miniaturization of photonic components to afford a larger scale of

integration on Si chips. The critical step in achieving this larger scale integration is the scaling of basic Si or SOI waveguides to submicron dimension. When the SOI waveguides are scaled down to this dimension, the characteristics of light propagating in the waveguides change dramatically. Modulation of light in these submicron SOI waveguides is also significantly different from the larger waveguides. Understanding the characteristics of light propagation and modulation in Si as the waveguide scales down to submicron dimension is therefore an important aspect of our research. In particular, the impact of device scaling on waveguide scattering loss will be discussed in Chapter 3, while the effect of device scaling on thermo-optic modulation in SOI switches will be addressed in details in Chapter 5.

## 1.5. THESIS OBJECTIVES

This research aims to address the key technical challenges associated with the development of a basic silicon photonic chip which integrates both passive and active devices in a single SOI platform, capable of performing general optical functions such as routing, power splitting, multiplexing or demultiplexing, modulation and switching. There are three main aspects to this research:

(i) To study the issue of coupling between on-chip waveguides and external optical fibers (or focusing optics), in relation to optical losses caused by modal mismatch, reflection and scattering at the chip-air interfaces; and to improve the fabrication process of optical facets that facilitate the function of the on-chip couplers.

(ii) To investigate the issue of waveguide propagation losses caused by light

scattering in the presence of roughness at the waveguide sidewalls; to develop an effective technique to measure the propagation (or scattering) losses; and to optimize waveguide fabrication process for loss improvement.

(iii) To exploit the thermo-optic effect in Si for the use in modulation and switching functions, and to study the effect of material and geometrical parameters on the switching speed and power requirement, as the device is scaled to submicron dimension.

## 1.6. ORGANIZATION OF THESIS

An introduction to the motivation of current research has been given in Chapter 1. In this chapter, the thesis objectives are defined according to the three main aspects of research: coupling, propagation and modulation of light in the silicon chips. The first aspect of this research, which is the fundamental problem associated with coupling light in and out of the silicon chips, is address in Chapter 2. The second aspect of the research, which is the propagation of light in the silicon waveguides, is described in Chapter 3. The propagation losses caused by scattering of light at the waveguide sidewalls in the presence of roughness are discussed in details. The third aspect of this research, which is the modulation of light by thermo-optic effect in silicon is described in Chapter 4. The existing technologies for thermo-optic switches and modulators are reviewed. The main focus of Chapter 4 is on the design of the SOI thermo-optic switches, including material selection and geometrical parameters that affect both speed and power requirement of the devices. A substantial part of the chapter concentrates on discussing simulation results of

the thermo-optic switches, while the remaining part provides a brief summary of the fabrication process and test results of the fabricated switches. The subject of thermo-optic modulation is further explored in Chapter 5, which provides an insight to the effect of device miniaturization on the performance of thermo-optic switches. Optimization of device parameters and balancing their tradeoff in device performance as the silicon chip reduces in size are the major topics of this chapter. Finally, a summary of the original accomplishments and implications of this thesis is provided in Chapter 6, together with some recommendations for further research.

# CHAPTER 2

# INPUT-OUTPUT COUPLING

A fundamental issue in silicon photonics is the reduction of optical insertion loss. There are two primary constituents to the optical insertion loss: (i) coupling loss, incurred when light is transmitted into and out of SOI waveguides either to a glass fiber or the focusing optics; and (ii) propagation loss, due to scattering and absorption in the waveguides. This section reviews the causes of coupling losses and some methods proposed in the literature to reduce these losses. In addition, a new technique is proposed to fabricate high quality optical input/output facets with vertical sidewalls, which can be precisely positioned. The precise positioning of these facets is important for the performance of many couplers or mode converters that are used to reduce modal mismatch and coupling loss, which will be discussed in the following session.

## 2.1. LITHOGRAPHICALLY-DEFINED OPTICAL FACETS

In most of the applications where a single-mode operation is required, the SOI waveguide width is designed to be in the order of a micron or sub-micron [2.1, 2.2]. On the contrary, a normal single-mode optical fiber has a mode size of at least 8 to 10 μm in diameter [2.3, 2.4, 2.5]. As a result of this difference in size, direct coupling of a mode

between an SOI waveguide and a single-mode fiber results in a high coupling loss [2.3]. Theoretically, because this mode size difference is a factor of 10 to 100, typical coupling loss between normal single-mode optical fiber and single-mode SOI waveguide could be as high as 20 dB [2.4]. Strong reflection due to index mismatch at any waveguide-fiber interface can also deteriorate the coupling efficiency. Likewise, significant scattering from a rough interface will further increase the coupling loss. Therefore, a low-loss and low-reflectivity mode coupler is needed to facilitate input-output coupling of the SOI waveguides to the optical fibers.

Coupling efficiency between fibers and waveguides can be improved using tapered or inversely tapered two-dimensional couplers to convert the mode [2.3, 2.4, 2.5, 2.6], or by using photonic crystal and grating couplers [2.7] that often contain 100 nm-size features, which require advanced lithographical tool to pattern. In addition to these two-dimensional coupler structures, vertically tapered three- dimensional waveguide couplers created by grey scale lithography have also been fabricated [2.8].

An alternative approach to the inversely tapered coupler technology would be to use a planar graded index (GRIN) lens based on either a stepwise index profile [2.9], or a quadratic index profile, fabricated on amorphous $Si_xO_y$ stacks [2.10, 2.11]. However, coupling in these planar devices demands the accurate material thickness and alignment of the center plane of the GRIN lens to the center of the waveguide core, thus introduces considerable difficulties in material growth, fabrication and packaging (e.g. alignment) process. In order to overcome these difficulties, researchers in NRC have proposed a monolithically integrated, asymmetrical half-GRIN waveguide coupler [2.12]. This

coupler consists of a half-GRIN lens that is grown directly on top of the waveguide, for example, an amorphous Si lens on the SOI waveguide, that is capable of focusing and coupling light from an optical fiber into the waveguide, as shown in Fig 2.1.

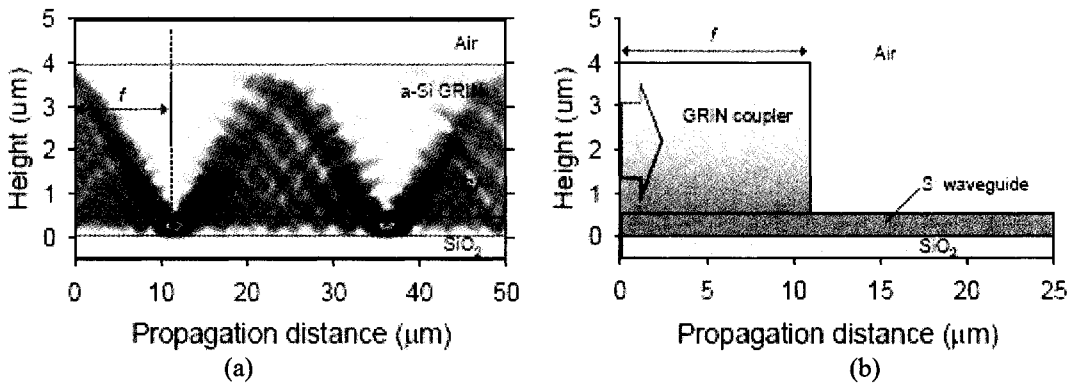



Fig. 2.1. (a) Simulated optical intensity distribution of TE polarization in a half-GRIN waveguide coupler. (b) A schematic of this coupler consisting of a 0.5 μm Si waveguide core and a 3.5 μm amorphous Si GRIN layer with a focal length *f* from the input facet [2.12].

The intensity of light coupled into this half-GRIN coupler varies periodically with the coupling length. The maximum coupling efficiency is achieved when the GRIN coupler has a total length of *f*, measured from the input facet, as shown in Fig. 2.1(a). 88% of the light is coupled into the underlying Si waveguide core when the distance between GRIN lens and the facet is optimized [2.13]. Therefore it becomes crucial to devise a technique that can precisely define the location of the facets with respect to the coupler.

To date optical facets are created on photonic chips via dicing and polishing to provide the interfaces for either coupling in or out of the waveguides, or for dropping in active components such as lasers and photodetectors in the case of hybrid integration

[2.14]. Regardless of the usage, the major challenge in preparing the facets is in refining the facet texture and profile in order to optimize the input-output coupling efficiencies. This is because optical interconnects on photonic chips are generally established by butt-coupling glass fibers from the sides of the chips through the facets, unlike the electrical interconnects on microelectronic chips which are established from the top of the chip via wire bonding or flip-chip bonding. The conventional process of fabricating these facets in silicon includes dicing, mechanical lapping and polishing steps as well as many other intermediate adhering, detaching and cleaning steps that are tedious, low yield and costly. Eliminating these lapping, polishing and intermediate steps for optical facet preparation is therefore key to making advanced photonic components a manufacturable commodity [2.15], especially in a high-volume manufacturing environment which demands low-cost and high-throughput fabrication.

A new manufacturing solution to replace labor-intensive dice-and-polish process scheme is therefore necessary. Wafer separation following a preferred crystallographic plane by cleaving is an attractive solution, given the simplicity of processing. Unfortunately, SOI wafers cannot be cleaved as readily as their III-V compound semiconductor counterparts because of the higher ductility of the buried oxide compared to the brittle III-V semiconductor materials. Silicon also prefers to cleave along <111> direction at an angle to the wafer plane, instead of <110> direction that is parallel to the (100) wafer plane. The separated facets of a cleaved SOI wafer often possess curved end faces with rough texture and non-vertical sidewalls, as opposed to the straight and smooth end faces of III-V semiconductor facets. One way to address this problem is to "pre-

form" high quality facets on the wafer prior to, instead of during cleaving. To this end, an effective method to create these preformed facets would be by using dry etching techniques to fabricate trenches (two facets per trench) on a wafer scale. After etching the desired optical facets, the SOI wafer could then be snapped and separated without risking the facet quality.

Apart from simplifying the processing steps, the need for accurate placement of optical facets at desired locations is another challenge for the fabrication. For instance, an optical facet must be located at the tip of an inversely tapered coupler to avoid significant leakage of the evanescent mode to the substrate [2.3, 2.16], or as mentioned in the previous section, at the correct distance from the focal plane of a half-GRIN waveguide coupler to ensure efficient coupling [2.12]. The amorphous Si based GRIN couplers show optimum coupling at a focal distance of only 15 μm, implying that the optical facet must be created at a 15 μm distance from the focal plane of the coupler, perhaps with a maximum alignment tolerance of ±1 μm. Such alignment accuracy is difficult to achieve with the conventional processes because of the problem with dicing misalignment and over-polishing.

Other than controlling the focal length, optical facets with controlled depth and high optical quality can be made in a Si trench, allowing insertion of active components, filters [2.17, 2.18] and micromechanical switches [2.19] to achieve hybrid integration. In these applications [2.17, 2.18, 2.19], both facets of the trench must be vertical, smooth and uniform in profile and texture. In order to assure that the filters can be inserted and

secured properly in these high aspect ratio trenches, the width of such trenches has to be in the range of 10 to 20 μm while the depth has to be more than 40 μm [2.17]. A high plasma density, low pressure inductively-coupled plasma (ICP) system with wider operating windows and better control of ion energy for etching is therefore well suited for etching such deep trenches in SOI. ICP-based etch systems offer a high Si etch rate and excellent selectivity over resist, metal or dielectric mask materials [2.17].

In designing an optical facet, the primary objective is to minimize coupling loss by optimizing facet angle, reducing off-axis misalignment and end face roughness. The coupling loss caused by an inclined facet-angle could be determined by calculating the overlap integral of the fundamental SOI waveguide mode with the fiber mode. In the calculation, the wave front of the fiber mode profile has to be modified to include the effect of refraction through a non-vertical facet. Assuming negligible off-axis misalignment between the fiber and waveguide, the excess loss due to deviation in the facet angle in the $y$-direction with respect to the vertical plane is equal to the loss caused by the facet angle in the $x$-direction (orthogonal to $y$). The excess coupling loss at any given facet angle (along either $x$ or $y$-direction) within the range of $10^{o}$, based on the coupling from a single mode fiber of 10 μm diameter to an SOI waveguide of 3 μm width, has been calculated by A. Delâge in the National Research Council of Canada (NRC). As shown in Fig. 2.2, the calculated result shows that a $2^{o}$ facet angle will only cause an extra 0.2 dB coupling loss. A large facet angle of $9^{o}$ will be required to cause a 3 dB loss [2.20]. The low susceptibility to coupling loss from the variation in the etched

facet angle therefore offers a large margin to the etching process.

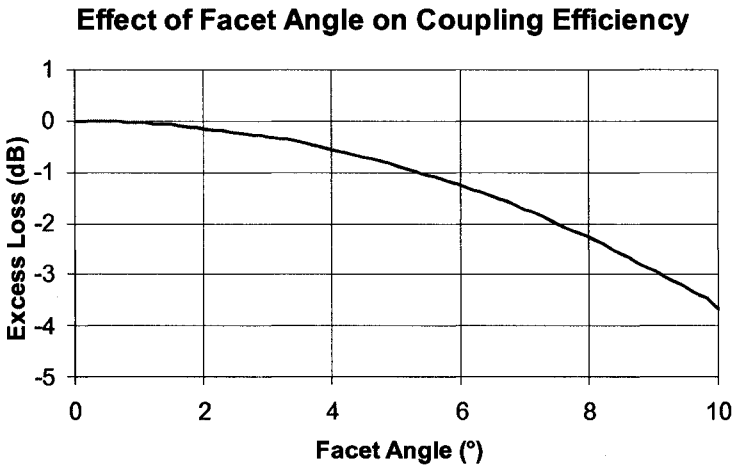



Fig. 2.2. Simulation of the effect of facet angle on coupling loss [2.20].

In this research, a novel etch-and-break method has been successfully developed to create all required facets with good optical quality and vertical sidewalls at designated locations on SOI wafers. The facets are prepared by patterning and etching trenches in the SOI wafers using lithography and ICP etching techniques [2.20]. This method produces facets that are easily separable by breaking the etched trenches, therefore significantly reducing the time and cost of fabrication. The facets can also be created along any direction parallel to the wafer plane by lithography, thus allowing a large degree of freedom in optical design.

## 2.2. FABRICATION AND TESTING OF OPTICAL FACETS

The process of creating optical facets is schematically illustrated in Fig. 2.3.

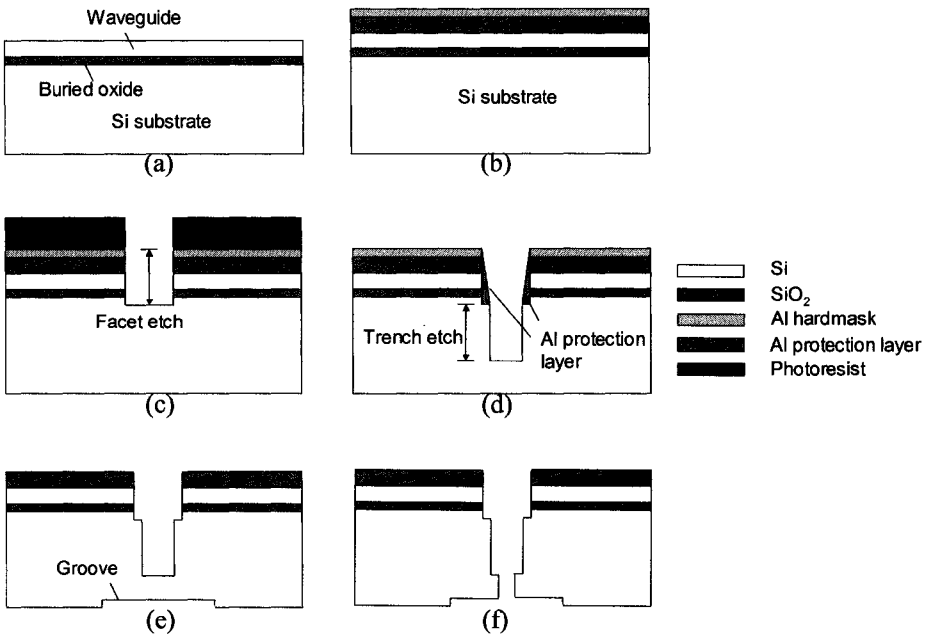
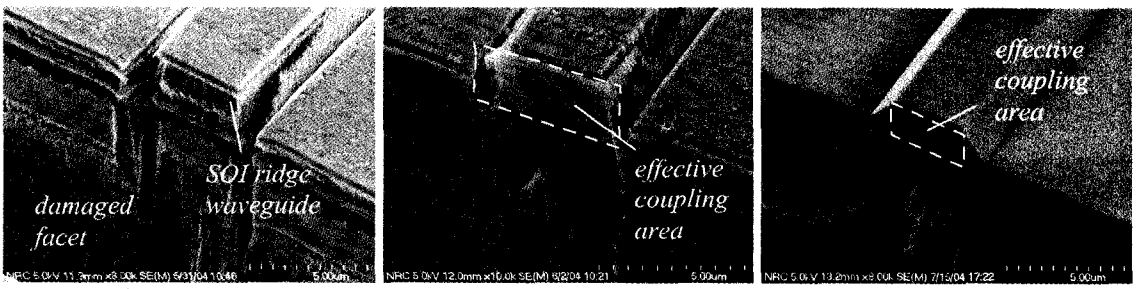



Fig. 2.3. Fabrication process steps of optical facets: (a) formation of SOI waveguides, (b) deposition of PECVD $SiO_2$ and Al on SOI waveguides as protection layers, (c) optical facets patterning by lithography and ICP etching, (d) evaporation of Al at a high tilt angle to protect the facets, followed by deep trench etch, (e) removal of all Al layers in E6 solution, followed by grooves formation at the wafer back side, and (f) break to separate the facets along the etched trench [2.20].

The process development of the optical facets was performed on SOI wafers with a 2.2 μm Si top layer and 0.4 μm buried oxide (BOX) layer. SOI ridge waveguides were patterned by e-beam lithography using a lift-off process and were subsequently dry etched in an ICP etcher with a $SF_6$-$C_4F_8$ chemistry or wet etched in a KOH solution. The resultant waveguides from the dry etch process have a rectangular shape while the wet etched waveguides are trapezoidal with a sidewall angle of 54°. To improve coupling efficiency, the waveguide width was adiabatically tapered from the nominal width of 2 μm to 3 μm at the facets with a taper length of 250 μm.

Prior to the formation of optical facets, a bilayer consisting of PECVD oxide and sputtered Al was deposited on top of the SOI ridge waveguides, as shown in Fig. 2.3(b), to protect the waveguides from erosion during the subsequent deep etching. A thick positive photoresist (PR) was then spun on and 10 μm-wide optical trenches with facets orthogonal to the waveguides were patterned using a contact aligner. Since the printing accuracy of these facets on the SOI samples is mainly limited by the alignment precision of the contact aligner, this fabrication technique offers a positioning accuracy of ±1 μm. After developing the PR, optical facet windows were opened for deep ICP etching.

Previous work at NRC has shown that one-step deep etching through the stack of Si and $SiO_2$ layers in ICP etcher using a fluorine-based chemistry often causes damage to the unprotected waveguide end faces in the etched facets because of plasma attack. A typical example of a damaged etched facet is shown by the SEM image in Fig. 2.4(a).




(a) (b) (c)

Fig. 2.4. (a) A damaged facet by plasma attack during the one-step deep etch, (b) A partially damaged facet from a two-step etch because of insufficient protection with thin Al coating, (c) An etched facet with smooth waveguide end faces because of sufficient Al protection (the wet-etched waveguide has a trapezoidal profile).

An idea to avoid such damages is to divide the one-step etching process into two parts to shorten the exposure of waveguide end faces to the plasma. In addition, a protective layer should be coated onto the waveguide end faces prior to the second etch to prevent plasma attack. This idea of protective coating suggested by the author has lead to the final etching process co-developed by B. Lamontagne and the author, as illustrated in Fig. 2.3. The deep etching process was eventually divided into two parts: (i) a facet etch and (ii) a trench etch. In the first part, optical facets were etched to a depth of approximately 4 μm through the stack of sputtered Al, PECVD oxide, Si waveguide, BOX layer and Si substrate at room temperature, as shown in Fig. 2.3(c). To assure verticality and minimum plasma attack on the facets, a $SF_6$-$O_2$ mixture (30 sccm $O_2$ :10 sccm $SF_6$) was used as the major etching gas. This etching gas along with an optimum amount of $C_4F_8$ (40 sccm), were able to enhance the etch rate of $SiO_2$ and the formation of a passivating fluorocarbon polymer layer on the facet during etching. This facet etch step terminated once the etch depth reached 1 to 2 μm into Si substrate under the BOX layer.

In the second part of trench etching, the first step was to deposit a thin Al layer on the facets at a tilt angle of 75° by thermal evaporation, as shown in Fig. 2.3(d). This is a critical step to assure smoothness and integrity of the etched facets, because the Al coating acts as a protection layer on the end faces of the waveguides, which are vulnerable to plasma attack during the subsequent trench-etch step. To assure sufficient coverage and protection, the SOI samples were subjected to this Al thermal evaporation

twice, over a 180° rotation. The large deposition angle of 75° (with respect to the normal of the wafer surface) was crucial to assure a sufficient thickness (approximately few tens of nanometer) of Al coating on both facets for protection, while keeping the Al thickness at the bottom of the trenches at minimum. A short dip of the sample in the E6 chemical solution was enough to remove the bottom Al without removing the Al protection layer on the facets. When the Al coating was deposited at low deposition angle, there was insufficient protection on the waveguide end faces. As a result, the subsequent trench-etch step damaged the etched facet especially at the area near to the upper corners of the ridge waveguides, as shown in Fig. 2.4(b).

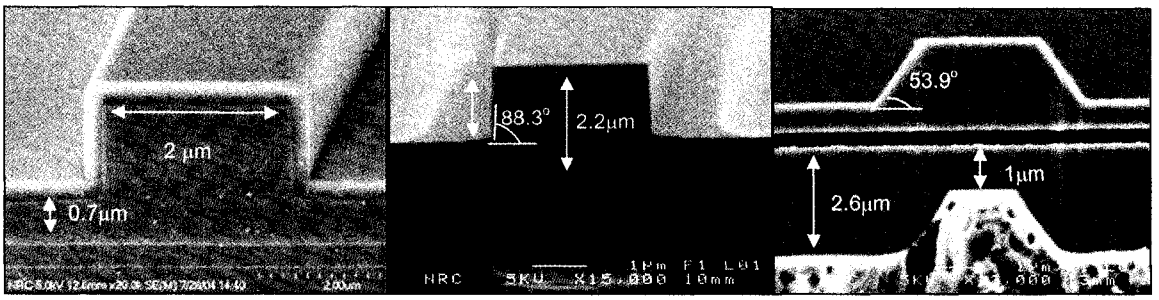
The trench-etch step was basically introduced to continue etching down the Si substrate to a depth of 70 μm. This trench-etch step also required a good directionality to minimize sidewall attack. This was achieved by a cryogenic ICP etching process. By reducing the substrate temperature down to −120°C, this cryogenic process used a mixture of 100 sccm $SF_6$ and 14 sccm $O_2$ to suppress lateral attack on the sidewalls with an oxide passivation layer [2.21], thus produced better verticality, higher etch rate (around 2 μm/min), and smoother sidewalls compared to a room-temperature etching process [2.22]. After the deep trench etch, the Al protection layer was completely removed, leaving PECVD $SiO_2$ capped waveguides and clean facets, as shown in Fig. 2.3(e) and Fig. 2.4(c).

The last step of the facet fabrication was to break the samples to separate the facets. In order to facilitate precise separation within the etched trenches, grooves that

were aligned to the trenches were cut on the backsides of the samples using a dicing saw. The thickness of remaining Si in the grooves was kept at approximately 100 μm from the wafer surface, so that they were sufficiently thin for a clean break, as shown in Fig. 2.3(f).

The physical quality of the fabricated optical facets was measured by their profile and texture, as well as their alignment accuracy. An optical microscope and a scanning electron microscope (SEM) were used to investigate and compare the physical quality of the etched facets with the conventional polished facets. Fig. 2.5(a) shows the SEM image of the cross-section of a dry-etched SOI ridge waveguide with the facet prepared by conventional polishing method; the facet surface is free of any defect of 100 nm length scale. On the other hand, Fig. 2.5(b) shows the SEM image of a similar dry-etched waveguide with an etched facet; the waveguide surface also appears to be defect-free. The slab region of the facet, however, is damaged during dry etching. This damage originates from the lower corners of the ridge and extends into the Si substrate underneath the BOX layer. Nevertheless, this etching induced damage has minimum impact on the coupling loss because the damaged region overlaps less than 5% of the mode field. The cause of this damage is from insufficient Al protection along the waveguide sidewalls during the facet etch, as a result of poor step coverage of the sputtered Al over PECVD $SiO_2$ layer. Deposition of the $SiO_2$ layer over sharp vertical edges by PECVD is known to create a bulge profile that prevents the uniform coverage of metal along the edges. The lack of sufficient Al protection from this non-uniform

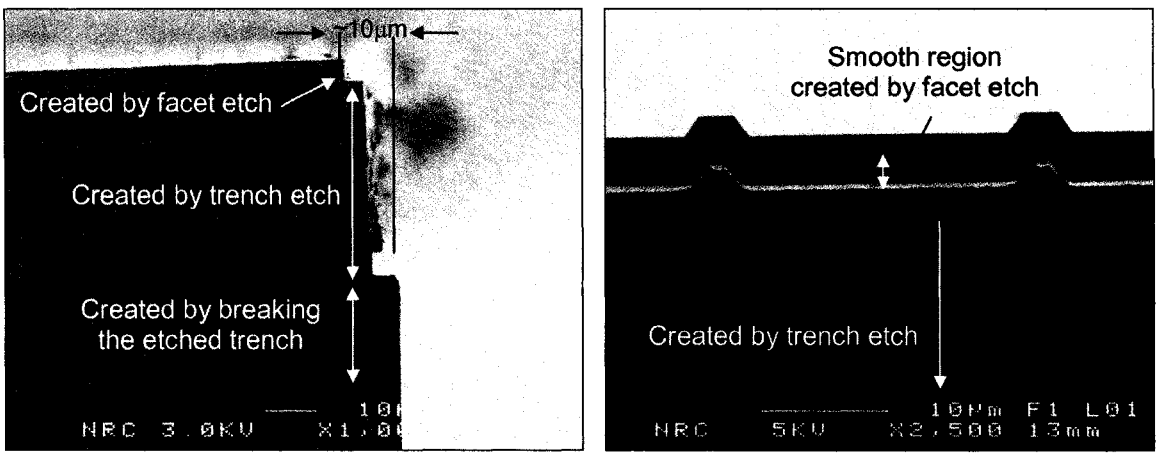
coverage thus results in the lower corners of the ridge vulnerable to plasma attack during etching. This problem, however, can be solved by either replacing the PECVD $SiO_2$ layer with spin-on-glass (SOG) or the Al sputtering with Al evaporation that uses a rocking motion to enhance coverage, or by sloping the sidewalls of the ridge waveguide to avoid sharp corners. The sidewalls sloping approach is proven effective from the SEM image of the wet-etched SOI ridge waveguide with identical etched facet (Fig. 2.5(c)), where no damage is observed because of the uniform Al coverage that protects the trapezoidal-shape waveguide sidewalls during facet etching.




(a) (b) (c)

Fig. 2.5. Cross-section of (a) a dry etched waveguide with the facet prepared by polishing, (b) a dry etched waveguide with the facet prepared by etching and breaking, and (c) a wet etched waveguide with the facet prepared by etching and breaking [2.20].

Fig. 2.6(a) shows the side view of an etched facet after breaking, where three distinct regions separated by the steps along the horizontal direction are seen. The first region is created by the shallow facet etch, starting from the waveguide end faces down to Si substrate underneath the BOX layer. Since the facet surface is well protected by the evaporated Al, this first region is characterized by a uniform smooth surface, as shown in Fig. 2.6(b).




(a) (b)

Fig. 2.6. (a) Side view of an etched facet showing the small step from the sidewall protection by Al before trench etch and the location of cleavage, and (b) front view of the etched facet revealing the smooth waveguide surfaces and the step created by Al sidewall protection [2.20].

The second region is located below the first region to a depth of 70 μm and has a relatively rough texture. The third region is flat and clean as a result of a good cleavage. Fig. 2.6(a) shows that the distance from the cleavage plane to the waveguide edge is around 10 μm; a safe gap which ensures no significant beam divergence when a single-mode fiber is coupled to the waveguide at the facet.

The facet angle should be as vertical as possible given the limited numerical aperture of the SOI waveguide, while the surface roughness must be low to ensure low scattering loss. High-resolution SEM images show that our process produces a facet angle of $89 \pm 1^{\circ}$, and an average peak-to-peak roughness value of 30 nm.

The optical insertion loss of the etched facets was determined by coupling light at 1550 nm wavelength from a tunable laser, via a tapered fiber into the on-chip SOI waveguides through the input facet, and detecting the output light power from the output

facet using a 20× objective lens and an optical power meter, as shown in Fig. 2.7.

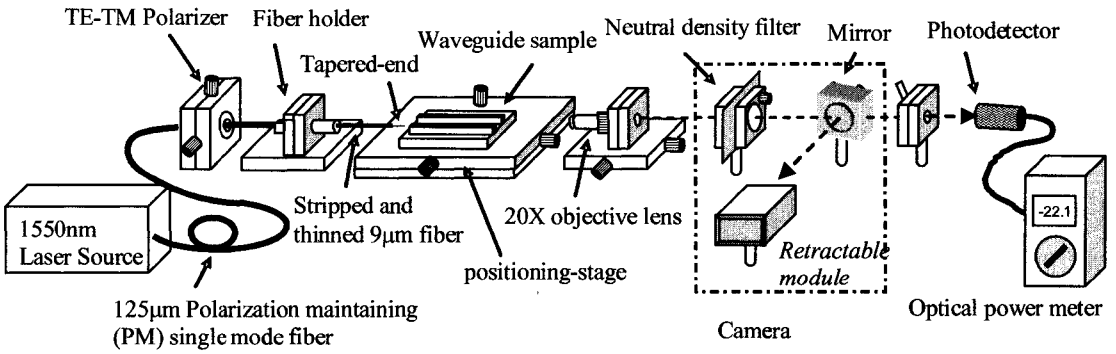



Fig. 2.7. Optical measurement setup for the testing of SOI ridge waveguides with facets fabricated by both etch-and-snap and conventional dice-and-polish techniques [2.20].

The measured insertion loss of TE polarization of the dry-etched waveguides with etched-and-snapped facets (22 ± 4 dB) is comparable to the diced-and-polished facets (22 ± 5 dB). These loss values are collected on two separate sets of samples, each with seven straight waveguides of a nominal width of 2 μm. The measured insertion losses are a sum of the losses from the measurement setup (around 3 dB) and the device under-test, including the estimated 6.5 dB coupling loss due to modal mismatch between taper fiber and SOI waveguides, the Fresnel reflection loss of about 3 dB, the scattering loss by the texture and angle of the facet, and the waveguide propagation loss. Since other losses remain unchanged, the comparison provides a relative measurement of the facet quality in terms of roughness and facet angle.

## 2.3. CONCLUSION

In this research, an etch-and-break method has been successfully developed to create facets with good optical quality and vertical sidewalls at designated locations on SOI wafers. The facets are prepared using lithography and ICP etching techniques. The optical insertion loss measurement results show that the facets prepared by this method are as good as the facets prepared by conventional dice-and-polish method. This observation is in good agreement with the physical results from SEM analysis, which show smooth waveguide end faces and vertical sidewalls on the facets prepared by ICP etching. This method is an important step towards wafer-scale manufacturing of silicon photonic chips because it essentially simplifies and improves the efficiency of optical facets fabrication by eliminating the need for labor-intensive mechanical lapping and polishing, therefore saving production time and cost significantly.

# CHAPTER 3

# WAVEGUIDE SCATTERING LOSS

Light can be scattered or absorbed when it propagates through a silicon waveguide, resulting in a reduction in total transmitted power. When the light is absorbed, the photons are annihilated by giving up their energy to the electrons of the absorbing material. On the contrary, when the light is scattered, the photons retain their energy but change their direction of travel. Regardless, attenuation or loss of transmitted power occurs and the attenuation can be described by:

$$I = I_o e^{-\alpha_o L} \tag{3.1}$$

where $I$ is the attenuated intensity, $I_o$ is the initial intensity, $\alpha_o$ is the exponential attenuation coefficient in $cm^{-1}$ and $L$ is the length of the waveguide. The attenuation loss per unit length, $\alpha$, in dB/cm, is given by:

$$\alpha = 4.34\alpha_o = 10 \cdot \log\left(\frac{I}{I_o}\right)\Big/L \tag{3.2}$$

In a silicon or silicon-on-insulator (SOI) waveguide with a width larger than ~300 nm, a strong electric field of the guided light exists in the core, because of the strong confinement introduced by the large refractive index step between the core and cladding layer. As a result, the scattering loss of the guided light is strongly dependent on the

interaction of the electric field with any imperfections present at the interfaces between the core and cladding, such as the roughness of waveguide sidewalls. These imperfections serve as the primary scattering centers for the light, resulting in considerable attenuation loss up to 30 dB/cm [3.1-3.5].

The scattering loss caused by sidewall roughness is sensitive to the waveguide width [3.1, 3.6-3.9]. For waveguides with smaller cross-sections and therefore larger electric field strength, the effect of scattering by the roughness at the interfaces becomes more prominent because of the stronger interaction of the mode field with the roughness.

As mentioned in Chapter 1, because of the large difference in the effective index and profile of the guided modes in the silicon waveguides, scattering loss also varies greatly with polarization state. This variation in scattering loss for different polarization results in a measurable polarization dependent loss (PDL), which is undesirable when the guided light in the waveguide comes from an optical fiber with an unknown state of polarization.

Roughness can be qualitatively characterized by a root-mean-square roughness $\sigma$, a measure of the typical height of the asperity present at the interface, and the correlation length $L_c$, which is a measure of the width of the asperity [3.1, 3.7]. Various studies intended to model the effect of roughness on scattering loss have been reported in the literature [3.3, 3.5, 3.7, 3.10]. Payne and Lacey have proposed a closed-form analytical expression to describe the scattering loss in two-dimensional planar waveguides as a function of surface roughness, waveguide width, core and cladding index, and correlation

length [3.4, 3.7]. In the Payne-Lacey analysis, the theoretical treatment of the waveguide scattering problem is based on the direct computation of the far field radiation loss caused by the asperities at the waveguide surface. They derived the exponential radiation loss coefficient for scattering by surface roughness in a symmetrical planar (slab) waveguide, and assumed that scattering occurred independently at both surfaces of the slab waveguide, where the roughness is identically distributed but uncorrelated [3.7]. The surface roughness of the waveguide was described by the spectral density function, $\mathfrak{R}(\Omega)$, which is related to the autocorrelation function $R(u)$ of the roughness through the Fourier transform:

$$\mathfrak{R}(\Omega) = \int_{-\infty}^{\infty} R(u)\exp(i\Omega u)du \tag{3.3}$$

where $u$ is the coordinate along the axial direction of the waveguide. Using previously reported measurement results of various waveguides [3.6], Payne and Lacey have classified autocorrelation functions into two major types, the Exponential function and the Gaussian function [3.7]:

$$\textit{Exponential:} \quad R(u) = \sigma^2 \exp\left(-\frac{|u|}{L_c}\right) \tag{3.4}$$

$$\textit{Gaussian:} \quad R(u) = \sigma^2 \exp\left(-\frac{u^2}{L_c{}^2}\right) \tag{3.5}$$

In either case, the surface roughness of a waveguide is described by the autocorrelation function, which includes two critical parameters: correlation length $L_c$, and mean square deviation $\sigma^2$ from an unperturbed, flat surface. The parameter $\sigma^2$ is related to the autocorrelation function $R(u)$ by:

$$\sigma^2 = R(0) \tag{3.6}$$

Payne and Lacey have further evaluated the dependence of the scattering loss on the surface roughness characteristics of the waveguide using both autocorrelation functions, and have arrived at a closed-form analytical expression:

$$\alpha = 4.34 \frac{\sigma^2}{\sqrt{2} k_o d^4 n_1} g \cdot f \tag{3.7}$$

where $\alpha$ is the scattering loss, $k_o$, $d$ and $n_1$ are the free-space wave number, the waveguide half width, and the core index, respectively. $g$ is determined purely by the waveguide geometry, whilst $f$ is determined by the correlation length and index step of the waveguide [3.7]. The detailed equations for $g$ and $f$ are given in Appendix A.

The importance of this Payne-Lacey expression is that scattering loss $\alpha$, can be expressed in term of various normalized parameters of waveguide geometry and surface roughness. This expression predicts that the scattering loss increases with the mean square deviation of the surface roughness, $\sigma^2$, and for any given roughness, the scattering loss increases rapidly as waveguide dimensions are reduced.

The limitation of the Payne-Lacey expression is the assumption that the roughness characteristics can be described simply by an exponential or Gaussian profile, while in reality the profile is highly random and difficult to describe mathematically. Also, the expression is derived for slab waveguides, therefore corrections have to be made in calculating the scattering loss of any practical waveguides that usually resume a channel or rib configuration. Nevertheless, the expression is a closed-form solution to the

waveguide roughness-induced scattering loss problem and represents a useful guideline for determining various factors contributing to the loss.

With a high index contrast ($\Delta n$ = 2) and small cross-section, SOI waveguide devices with considerable sidewall roughness are prone to high scattering loss. Reducing scattering loss is one of the major challenges to overcome in developing high performance SOI photonic devices. The objective of this work is therefore to improve fabrication process conditions in the aim to produce optimum waveguide geometry and smooth sidewalls that can result in low scattering loss and polarization dependent loss.

In order to reduce scattering loss we need to establish an effective waveguide loss measurement technique that gathers accurate optical loss data to correlate with physical data such as roughness and sidewall profile, allowing us to control process parameters that affect the optical loss. The existing loss measurement techniques such as the cut-back method and Fabry-Perot resonance method [3.9] collect loss data from individual waveguides and only measure one waveguide loss in each measurement step [3.11]. To measure scattering losses of SOI waveguides with different widths, multiple measurements must be taken. In the cut-back method, the insertion loss of a waveguide is measured at a constant input power, every time the waveguide is cut back in length. The waveguide scattering loss can be calculated from the variation of insertion loss ln($I$), with waveguide length $L$, obtained directly from the slope of ln($I$) with respect to $L$:

$$\alpha_o = \frac{\Delta \ln I}{\Delta L} \tag{3.8}$$

The major assumption of cut-back method is that the input power and coupling, which depend on the quality of waveguide end surface at the optical facet, remain unchanged. Variations in facet quality and coupling often limit the accuracy of this method [3.9]. Another major disadvantage is the destructive nature of this method.

On the other hand, the Fabry-Perot resonance method draws on the fact that a waveguide with polished facets forms an optical resonant cavity. Light traveling in the waveguide undergoes multiple reflections at the two interfaces bounding the waveguide. The amplitude of the maximum and minimum intensity is related to the reflectivity $R$ of the air-waveguide interface and the exponential loss coefficient $\alpha_o$ in the waveguide by:

$$T_{\max} = \frac{(1-R)^2 e^{-\alpha_o L}}{(1-Re^{-\alpha_o L})^2},\ T_{\min} = \frac{(1-R)^2 e^{-\alpha_o L}}{(1+Re^{-\alpha_o L})^2} \tag{3.9}$$

It is common to evaluate the ratio of the maximum intensity to the minimum intensity as:

$$\kappa = \frac{T_{\max}}{T_{\min}} = \frac{(1+Re^{-\alpha_o L})^2}{(1-Re^{-\alpha_o L})^2} \tag{3.10}$$

For the large single mode SOI ridge waveguide, the Fresnel reflectivity $R$ of the facet can be determined from the index of Si core ($n$) and air ($n_{air}$ =1).

$$R = \frac{(n-1)^2}{(n+1)^2} \tag{3.11}$$

The scattering loss in a straight waveguide of length $L$ can thus be calculated:

$$\alpha = 4.34\frac{1}{L}\ln\left(\frac{1}{R}\frac{\sqrt{\kappa}-1}{\sqrt{\kappa}+1}\right) \tag{3.12}$$

The integrity of the waveguide sample can be preserved in Fabry-Perot (F-P) test method

since it is unnecessary to cut back the sample and the technique is nondestructive. However, the accuracy of Fabry-Perot method is limited by the need for a precise value of the facet reflectivity to calculate the scattering loss, while the actual reflectivity is often difficult to determine [3.11, 3.12]. The optical facets defining the cavity may have rough texture and profile, introducing unpredictable reflection losses. Furthermore, the facet reflectivity for small waveguides differs from Equation (3.11), which is based on a single plane wave calculation. For instance, the calculated facet reflectivity of the III-V cavity laser can vary from 20% to 40% depending on waveguide thickness, index contrast and optical polarization [3.13]. Apart from the uncertainty in the reflectivity value, interference from leaky modes and stray light in a multimode waveguide could causes variations in the peak heights of the Fabry-Perot fringes and imposes difficulty in determining an accurate fringe contrast [3.14], which is essential to the calculation of scattering loss.

To overcome these limitations, a non-destructive technique using SOI star couplers to measure the sidewall roughness induced scattering loss has been devised in this research [3.11, 3.15]. The accuracy of this technique is independent of the input coupling efficiency and facet reflectivity. It simplifies the measurement of scattering losses at various waveguide widths to a single step. By measuring these losses on various SOI star couplers fabricated from different processes, this technique provides a reliable feedback to the process development and optimization.

## 3.1. OPTICAL STAR COUPLER SCATTERING LOSS MEASUREMENT

### *3.1.1 Operating Principle*

The star coupler used for scattering loss measurement has an input array of five waveguides and an output array of seventeen waveguides, connected by a free-space slab region (FPR), as shown in Fig. 3.1.

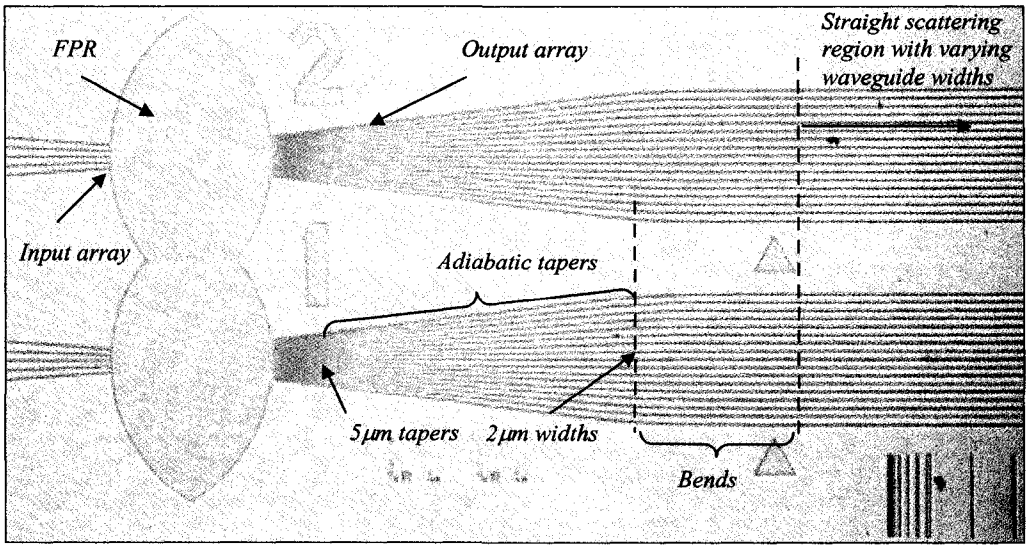



Fig. 3.1. Optical image of two fabricated star couplers for waveguide scattering loss measurement.

In this star coupler, a traveling Gaussian wave from any input waveguide will be diffracted at the input array-slab interface and project a Fraunhofer far-field profile to illuminate all output waveguides at the slab-output array interface. The Fraunhofer profile assumes an approximately Gaussian output pattern, when the input waveguide profile is approximately Gaussian. Each waveguide in the array will propagate light to the output facet. In the absence of optical loss, the intensity distribution across the output array at

the facet should have the same profile as was launched at the slab-output array interface. If extra scattering loss is introduced into any waveguide of the output array, a drop in the intensity of the corresponding waveguide output will be observed, as shown in Fig. 3.2. Since scattering loss increases rapidly with the reduction in waveguide width, the star coupler with an array of output waveguides appears to be an excellent device to study the loss at different widths.

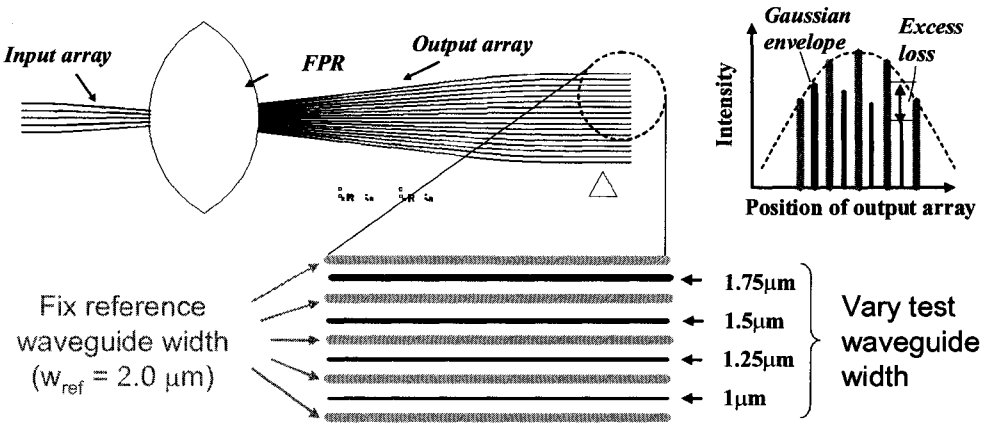



Fig. 3.2. Schematic illustration of waveguide scattering loss measurement using a star coupler. The odd waveguides are reference waveguides with fixed width of 2 μm, while even waveguides are test waveguides of varying width. The output intensity at the far field contains multiple peaks with a Gaussian envelope, as shown in the upper right corner.

The input waveguides of our star coupler have identical width of 3 μm but output waveguides have varying widths. The width of all odd output waveguides is fixed at 2 μm, while the width of even waveguides varies from 0.2, 0.4, 0.6, 0.8, 1, 1.25, 1.5 to 1.75 μm. By fixing the width of every odd waveguide in the array to be 2 μm while varying the width of remaining even waveguides, lower peak intensities will be seen for the even waveguides as a result of the increased scattering due to width reduction. Using the odd

waveguides as reference waveguides with intensities following the symmetric far-field envelope, as illustrated in Fig. 3.2, the extra scattering loss of any even waveguide can then be calculated from the ratio of its measured output intensity to the average intensity of the two adjacent reference waveguides. This excess loss represents the relative scattering loss of the even waveguides with respect to the reference waveguide:

$$\alpha = \log_{10}\left(\frac{I_n}{0.5(I_{n-1} + I_{n+1})}\right), n = 2,4,6,\ldots,16 \qquad (3.13)$$

where $I_n$ is the measured intensity of the $n^{th}$ waveguide ($n$ is an even number).

The measurement of this excess loss can be done relatively easily using an infra-red (IR) camera to capture the near field optical image of all output waveguides in the array. Output intensity of each waveguide can be measured from the image, from which the excess loss can be determined. Since one image contains the intensity information of all waveguides, the excess loss of all waveguides can thus be measured in a single step.

### *3.1.2 Design of the Star Coupler*

A 10 μm-wide gap between the input waveguides at the input array-slab interface is designed to avoid mode coupling. The radius of curvature of both array-slab interfaces is 400 μm, so that the curvature at the output array-slab interface matches the wavefront of the diffracted light from any input waveguide, after propagating through the slab region. At the output array-slab interface, the width of output waveguides is tapered to 5 μm to receive maximum power and to minimize back reflection from the curved wall of the interface to the FPR, as shown in Fig. 3.3(a) and (b).

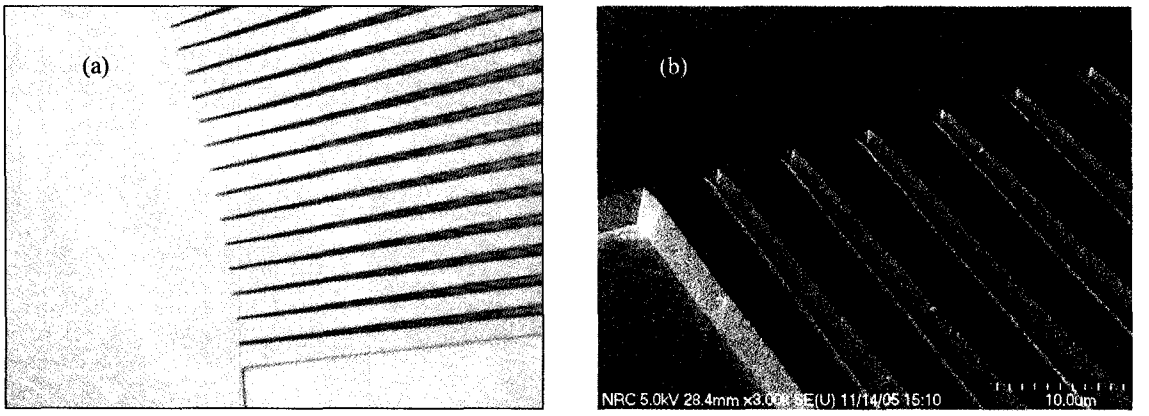



Fig. 3.3. (a) Top-view optical image of the slab-output array interface of our fabricated star coupler, (b) Side-view SEM image showing the tapering of output waveguides at the same interface.

This leaves a minimum gap of 1 μm in between adjacent output waveguides. The output waveguides are adiabatically tapered down to their respective widths over a length of 350 μm and converge to form a straight and parallel array region towards the output facet. This 7 mm-long straight array region is where the effect of scattering is measured as a function of waveguide width, as shown in Fig. 3.1. Since the length of the tapered region is much less than the length of the straight array region, the total waveguide loss is dominated by the scattering at the straight region.

## 3.2. SOI WAVEGUIDE FABRICATION PROCESS DEVELOPMENT

Waveguide sidewall roughness may originate from the line edge corrugations of photoresist that is transferred to the waveguides during the subsequent etching, or from the etching process itself [3.8, 3.9]. Choosing the right combination of lithography, photoresist and dry etching process is therefore crucial in minimizing roughness. In this

study, we have chosen to compare three processes using two different lithography tools commonly used to pattern SOI waveguides: a contact aligner and an e-beam direct writer. For the e-beam direct writing, we have studied both positive and negative resist for roughness comparison. An inductively coupled plasma (ICP) etcher has been used to etch the SOI waveguides given the excellent Si etch rate and good control of plasma energy. The three different fabrication processes to study waveguide roughness are shown in Fig. 3.4. These processes mainly differ by pattern transfer techniques and resist chemistry:

(i) Process I: Contact lithography with a positive photoresist

(ii) Process II: E-beam lithography with a positive e-beam resist and lift-off process

(iii)Process III: E-beam lithography with a negative e-beam resist on a Cr hardmask layer

The starting substrate was a (100) p-type SOI wafer (background doping concentration of $10^{15}/cm^2$) with a 2.5 μm top Si layer on a 0.4 μm buried $SiO_2$. As illustrated in Fig. 3.4(a), one set of samples was patterned using contact lithography and dry etching in an inductively coupled plasma (ICP) etcher with $SF_6$: $C_4F_8$ chemistry. UV light at $\lambda = 365$ nm was used to expose the SPR510 photoresist by contact lithography to achieve fine patterning of both input and output waveguide arrays. In order to minimize bend loss and polarization dependent coupling loss of the star coupler [3.9, 3.16], etch depth of the ridge waveguides was targeted at 1.8 μm.

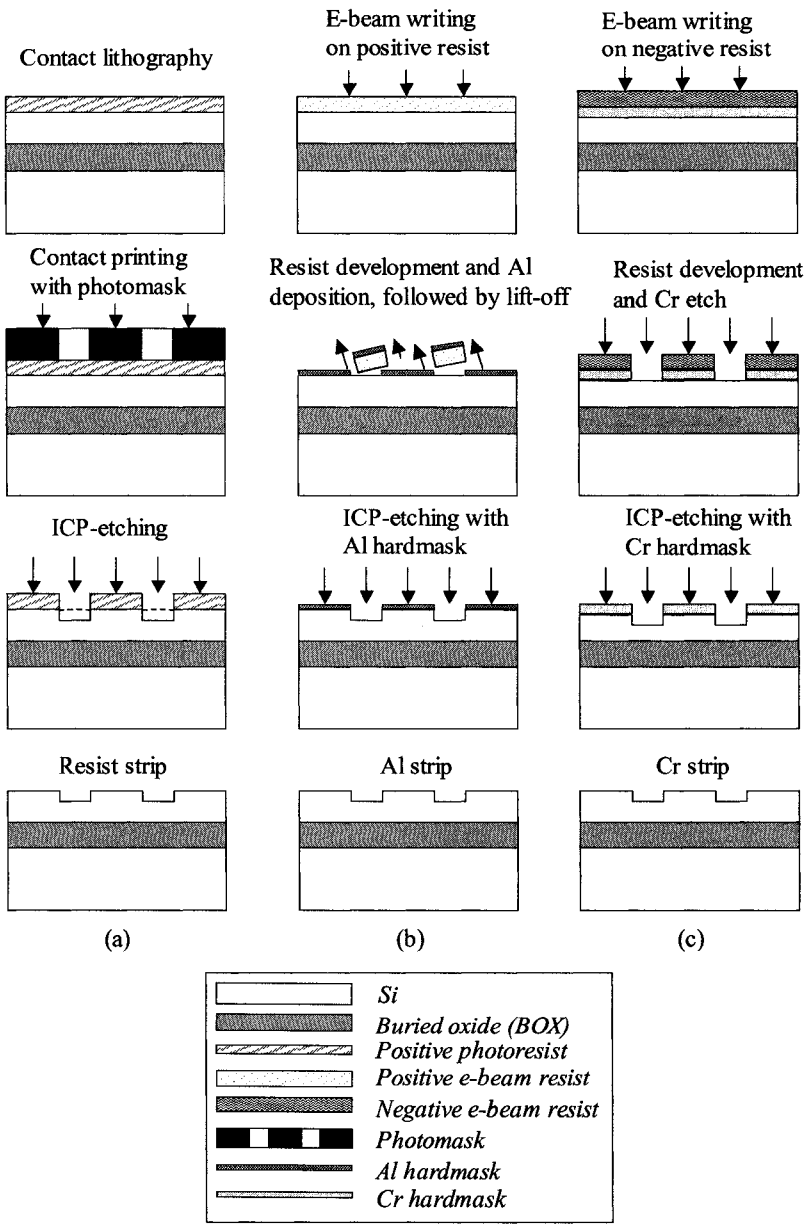



Fig. 3.4. Schematics of three different processes to fabricate SOI star couplers and waveguides with different sidewall roughness, (a) Process I: contact lithography, (b) Process II: e-beam lithography and lift-off, (c) Process III: e-beam lithography and Cr hardmask.

Two other sets of samples using resists of opposite polarity were patterned by electron-beam direct writing. One set was patterned using a positive e-beam resist

ZEP520, as shown in Fig. 3.4(b). After resist development, a 50 nm-thick Al layer was evaporated on this set of samples and the samples were then subjected to a lift-off treatment. Using the remaining Al layer as a hardmask, the samples were then dry etched in ICP etcher with the same $SF_6$: $C_4F_8$ recipe. The final set of samples was patterned using NEB22, a negative e-beam resist. A 50 nm-thick Cr layer was previously sputtered onto the samples serving as the hardmask for the dry etching of SOI waveguides in ICP, as shown in Fig. 3.4(c). The Cr hardmask was etched in a $Cl_2$:$O_2$ plasma at room temperature with a chamber pressure of 30 mTorr to give an optimum etch rate of 15 nm/min. After the Cr etch, the samples were subsequently etched in $SF_6$: $C_4F_8$ plasma to form the ridge waveguides. The high selectivity of Cr to Si (> 200:1) gave an excellent process window for this etching step. The remaining Cr hardmask was then removed in a solution containing perchloric acid and ammonium cerium nitride, a standard wet etch agent for Cr. A 0.5 μm-thick $SiO_2$ film was subsequently deposited on all samples by plasma-enhanced chemical vapor deposition (PECVD) to protect their structural integrity during facet polishing.

Since all three sets of samples were patterned with different resists and lithography techniques, the resulting sidewall roughness of the dry-etched SOI ridge waveguides of each sample set is different, depending mainly on the initial sidewall roughness and profiles of the patterned hardmask or resist. This provides a comparison for the investigation of scattering loss caused by different sidewall roughness.

In order to obtain low loss waveguides other structural imperfections besides

roughness that will influence the measured loss should also be eliminated. These imperfections include micro trenches (localized recess at the bottom of the sidewalls), footings (tails at the foot of the sidewalls), undercuts (slanted sidewalls with narrower bottom), overcuts (slanted sidewalls with wider bottom) and micro-masking (particles or residues on Si surface that act as tiny masks during etching) defects [3.2], whose formation depends on the etching chemistry, plasma properties and the passivation mechanisms. In general, the final profile has to be optimized to achieve a flat top, vertical waveguide with uniform and accurate dimensions (with respect to the design). This waveguide profile is strongly affected by both lithography and etching processes.

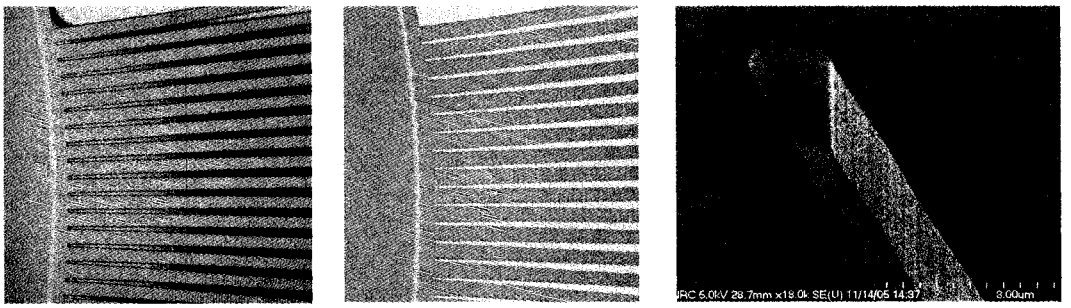
In the contact lithography fabrication process, since the optical mask and photoresist are brought into contact, particles and defects are inadvertently present and the fabricated waveguides usually have rougher sidewalls. On the other hand, the profile and roughness of waveguides patterned by e-beam lithography and lift-off process depend greatly on the degree of undercut in the exposed resist and the coverage of Al during deposition. For a successful lift-off, sufficient amount of undercut is required for the chemical (lifting agent) to penetrate under the resist to enhance the lift-off mechanism. In the case of insufficient undercut, Al will be deposited along the sidewalls and prevent the penetration of the chemical. The remaining Al at the sidewalls after the lift-off step, which can be non-continuous along the waveguides, acts as flakes that cause micromasking or non-uniform sidewalls during subsequent Si etching in ICP.

We have worked on minimizing the micromasking defects associated with the Al flakes but are limited by the capacity of our Al evaporation tool to produce highly

directional deposition for a clean lift-off. In an effort to improve the process, we have been successful in producing defect-free waveguides with optimum profile using the negative resist in the final set of samples. The followings are the improvement steps taken to optimize the process:

(i) *E-beam dose control and the use of Cr hardmask*: in e-beam lithography, low dose exposure produces rounded top profile and ragged sidewalls on negative resists due to insufficient cross-linking, while high dose exposure results in the formation of footings [3.15]. Therefore there is a narrow dose range to produce flat top waveguide profile without footings, however, the results are significantly affected by unique features such as tapers. In order to effectively eliminate the footings in Si waveguides we have introduced a Cr layer underneath the negative resist. Since this is a very thin hardmask layer, any small footings in the resist do not transfer to the Cr layer during the short Cr etching step. The use of hardmask significantly improves the process window for dose control.

(ii) *Short-interval oxygen ashing treatment*: Despite the elimination of footings by the introduction of Cr hardmask and optimization of isolated waveguide profile by dose control, finding the right dosage for both the isolated and dense patterns on the same SOI sample is still difficult, especially when trying to create gaps of decreasing width such as in Fig. 3.5.



(a) (b) (c)

Fig. 3.5. Optical images of the dense pattern area (output waveguide array of the star coupler) (a) before oxygen ashing showing the presence of residues in the gaps; (b) and (c) after oxygen ashing showing no residue in the gaps [3.15].

A proximity correction scheme has been used to correct for variations in pattern density over the sample [3.15]. In this case, four doses have been used where narrow isolated features receive the higher dose and narrow gaps in densely packed features receive the lowest dose. Also, a 50 nm wide outline of all the features has been exposed with a dose 30 % larger than the minimal dose to better define the sidewalls. Still, a thin layer of exposed resist was left in the narrow gaps, as shown in Fig. 3.5(a), due to the relatively low contrast of the resist. These residue patterns would be transferred to the etched waveguides and result in loss and detrimental crosstalk between the waveguides. The problem has been solved by introducing a short interval oxygen ashing step after the resist development to remove the residues in the gap while leaving the resist on the waveguides intact. This treatment requires highly directional oxygen plasma with moderate energy, and is best implemented in the reactive-ion etching (RIE) mode with a short interval of 25 to 30 s at 10 sccm $O_2$ plasma. As shown in Fig. 3.5(b) and 3.5(c), the residues were effectively removed after the treatment while the resist remained intact.

(iii) *Etching of Cr hardmask and SOI waveguides*: Once the optimum patterns of the star couplers have been established in the resist layer, the next challenge is to transfer these patterns into the Cr hardmask. The 50nm Cr hardmask etch recipe has to give a good selectivity to the e-beam resist, reasonable etch rate and also needs to be repeatable. The conditions of the chamber prior to Cr etching play a critical role in determining the repeatability of the etch result. We have observed the fluctuation of Cr etch rate if the chamber has not been properly conditioned prior to the actual etching. One possible explanation is the presence of carbon residues in the chamber that favor the formation of $Cr(CO)_6$ rather than the formation of lower boiling point $CrO_2Cl_2$ compounds during the subsequent Cr etch [3.17, 3.18]. At room temperature, it is harder and slower to remove these by-products by sputter etching. As a result, we have implemented a conditioning step prior to every Cr dry etching process, by incorporating He gas in the $Cl_2$:$O_2$ plasma to foster more directional sputter cleaning of the chamber. This conditioning recipe has successfully improved the repeatability of our Cr etch rate. After patterning the Cr hardmask, the samples were then subjected to $SF_6$:$C_4F_8$ plasma in the same ICP etcher to form SOI ridge waveguides. The selectivity of Cr to Si (> 200:1) gives an excellent process window for this etching step.

## 3.3. ROUGHNESS AND SCATTERING LOSS MEASUREMENTS

### *3.3.1. Roughness and Correlation Length Measurement*

SEM analysis was employed to extract roughness characteristics of waveguides fabricated by all three processes. A series of continuous high-resolution top view SEM

images of the waveguide edges at high magnification (at least 80k×) were collected. These collected images were stitched for digitization, as shown in Fig. 3.6.

The gray-scale intensity of the stitched SEM images was digitized into numerical scale, so that the intensity of any point on the SEM image, sampled at a high pixel resolution of approximately 1.2 nm, could be represented by a numerical value. Using an edge finding algorithm [3.11], one could determine the shift in the waveguide edge with respect to a reference edge position, as shown in Fig. 3.6. The waveguide sidewall roughness could be determined from the root-mean-square deviation of these shifts. The autocorrelation length could also be extracted from the autocorrelation function.

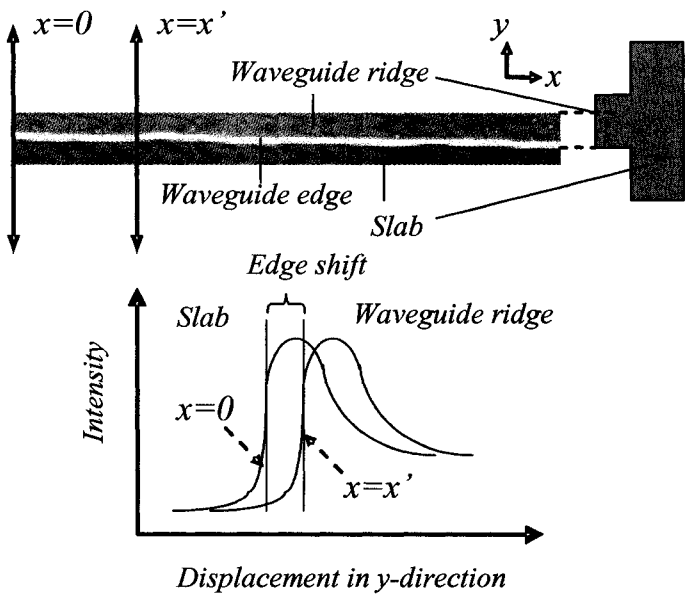



Fig. 3.6. An illustration of the sidewall roughness analysis by SEM. The graph shows the intensity profiles taken at $x = 0$ and at $x = x'$.

To extract the autocorrelation length, we have evaluated both exponential and Gaussian autocorrelation function, described by Equations (3.4) and (3.5). The

correlation length could be found from the best fit to the inverse Fourier transform given in Equation (3.3) using either the exponential or Gaussian autocorrelation function.

### *3.3.2. Optical Scattering Loss Measurement*

Loss measurements on star coupler were performed using the setup shown in Fig. 3.7. Broadband light (1530-1560 nm) from an Erbium-doped fiber source was coupled into the input waveguides of the SOI star coupler and the near field image of the full output waveguide array was captured by an IR camera.

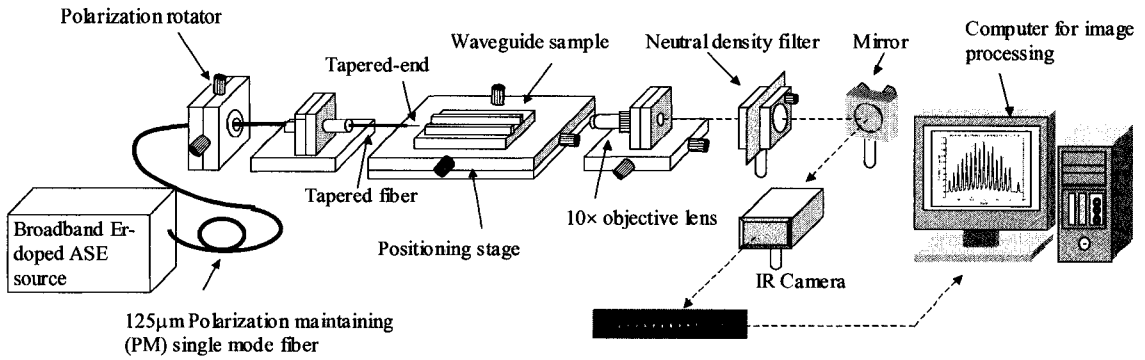



Fig. 3.7. Schematic of the optical scattering loss measurement using star coupler structures.

The IR camera was characterized to give a linear pixel response to the optical output intensity. A neutral density filter was inserted to attenuate the output intensity to avoid pixel saturation. The captured image was then converted to a normalized intensity profile by taking the area integral of the pixels, as shown in Fig. 3.7, and the relative scattering loss of each even waveguide was extracted from the ratio of its output intensity to the average intensity of its two adjacent reference waveguides using Equation (3.13).

A polarization rotator was used so that the loss measurement of both transverse-electric (TE) and transverse-magnetic (TM) polarization could be performed, separately.

## 3.4. LOSS MEASUREMENT RESULTS AND DISCUSSION

The r.m.s (root-mean-square) roughness and autocorrelation length extracted from SEM analysis are summarized in Table 3.1. The waveguides fabricated by e-beam lithography and Cr hardmask process yield the smoothest r.m.s sidewall roughness of approximately 3.6 nm. The sidewall roughness of waveguides patterned by e-beam lithography and lift-off process is 20% larger. Among all, contact lithography process gives the largest sidewall roughness of 7.7 nm, approximately twice the roughness of the Cr hardmask process. In addition, the correlation length from contact lithography is the smallest among all, and the autocorrelation function is approximately Gaussian.

Table 3.1. Measured r.m.s sidewall roughness and autocorrelation length of SOI waveguides fabricated by three different processes.

| *Fabrication Process* | *r.m.s roughness (nm)* | *Autocorrelation length (nm)* | *Autocorrelation function* |
|---|---|---|---|
| Process I (Contact lithography) | 7.7 ± 1.0 | 160 ± 25 | Gaussian |
| Process II (E-beam lithography with positive resist) | 4.3 ± 0.2 | 180 ± 14 | Exponential |
| Process III (E-beam lithography with negative resist) | 3.6 ± 0.2 | 225 ± 30 | Exponential |

To verify the accuracy of the SEM analysis, sidewall roughness of an SOI waveguide patterned by e-beam lithography with negative resist was also characterized by Boris Lamontagne at NRC using atomic force microscopy (AFM).

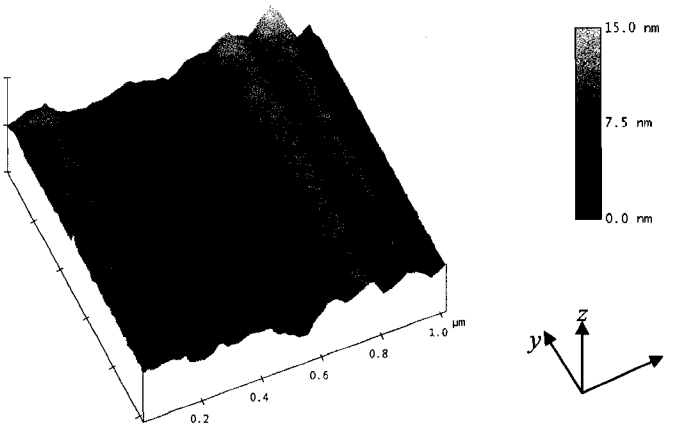



Fig. 3.8. A scanned AFM image of the waveguide sidewall of a sample fabricated using e-beam lithography with negative resist and Cr hardmask. The image clearly shows the size of the corrugations and the uniformity of the corrugations along the waveguide height (y-axis) [3.15].

For this measurement, the sample was cleaved in close proximity to a waveguide sidewall and then inserted into the AFM sideways, (i.e. with the sidewall facing up) to be scanned with a standard tip from above. One of the scanned AFM images of a waveguide sample fabricated using Process III is shown in Fig. 3.8. From the scanned images, we found an r.m.s roughness of 2.8 nm on the waveguide, reasonably close to the value measured using SEM.

Fig. 3.9(a) and 3.9(b) show the near-field IR image and the measured output intensity distibution of an output waveguide array in TE and TM polarization respectively, from a sample patterned by e-beam and dry etched with a Cr hardmask. Similar intensity distributions were obtained for waveguides fabricated by the other two processes. The intensity profile of the reference waveguides follows a far-field radiation pattern that can be approximated by a symmetric Gaussian envelope, as expected.

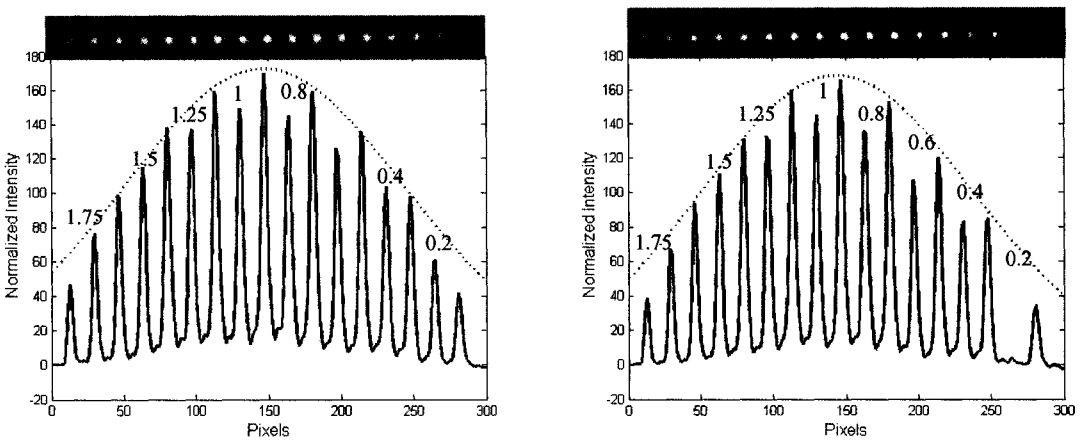



Fig. 3.9. Measured output intensity of waveguide array fabricated using Process III (e-beam, Cr hardmask) with the input light polarized along (a) TE direction and (b) TM direction. The horizontal axis represents the locations of the waveguides, while the vertical axis shows the measured output intensity of each waveguide. From left to right, the width of even waveguide is 1.75, 1.5, 1.25, 1, 0.8, 0.6, 0.4 and 0.2 μm, respectively. Intensities of odd waveguides follow a Gaussian envelope.

Fig. 3.10 is the plot of the measured TE and TM excess loss of the waveguides fabricated by the three different processes versus different waveguide width. The data points represent the measured experimental losses, where each data point is an average of the measured losses of three samples from the same process. The spread in the measured losses is shown by the error bars. The solid lines in Fig. 3.10 are the theoretical losses calculated using a modification of the Payne-Lacey model to account for varying ridge heights, as explained below. The correlation length $L_c$ and roughness $\sigma$ used to calculate these curves were obtained by fitting the modified Payne and Lacey equation to the TM loss data in Fig. 3.10(b).

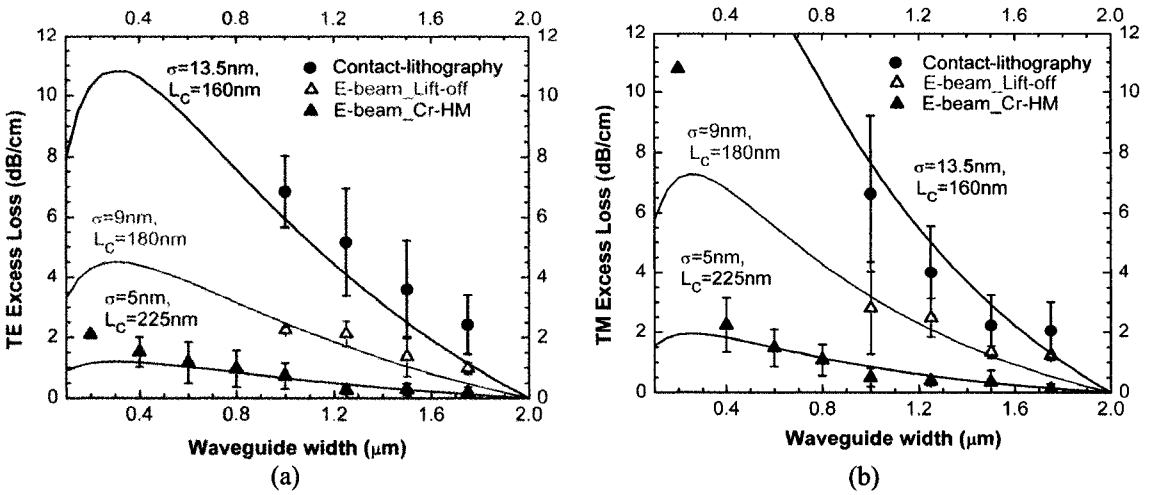



Fig. 3.10. Excess loss versus width of waveguides fabricated by three different processes for (a) TE and (b) TM polarization. Data points represent experimental loss while solid lines show theoretical loss. The theoretical loss is calculated by multiplying Payne-Lacey model with a scaling factor, to estimate the root-mean-square roughness.

The excess loss from all three processes increases monotonically with decreasing width for waveguides above 1 μm. There isn't any result for waveguides smaller than 1 μm for the first two processes because our contact lithography has a resolution limit of 1 μm, and the e-beam lift-off process did not produce reproducible results at waveguide widths less than 1 μm. When the width reduces to below 1 μm, the guided mode extends into the underlying slab of the ridge waveguide, and the loss becomes affected not only by scattering from the sidewalls but also from the surface roughness of the slab and leakage to the substrate [3.9]. We will first discuss excess losses for waveguide widths larger than 1 μm.

Samples patterned by contact lithography exhibit the highest excess losses among the three processes. Losses measured from e-beam patterned, lift-off processed waveguides

are from 1 to 4 dB/cm lower than the contact lithography, and the difference becomes increasingly significant with reducing width because the effect of roughness induced scattering increases rapidly with decreasing waveguide width [3.7]. The Cr hardmask process with the smoothest sidewall produces the lowest excess losses among all, ranging from 0.1 to 0.5 dB/cm. The trend in the measured scattering losses from our star couplers shows very good correlation with the trend of measured roughness by SEM.

To assess the usefulness of our SOI star couplers for measuring waveguide loss, we have correlated the roughness with the measured loss. We have adapted the Payne-Lacey model [3.7] for loss calculation, but have introduced modifications to acquire a more accurate roughness-loss correlation. The original Payne-Lacey roughness-loss expression applies only for two-dimensional slab waveguides and the scattering loss is calculated using the core index (refractive index of the slab).

Replacing the core index with an effective index will account for the change in modal propagation constant [3.19] in going from a slab to channel or ridge waveguide. Furthermore, since the Payne-Lacy model was developed using a simple three-layer slab waveguide model, it should overestimate the scattering loss from etched sidewalls of a ridge waveguide. To apply the model to our SOI ridge waveguides, we develop a correction to modify the Payne-Lacey expression to take into account varying ridge etch depths. The loss $\alpha$ due to scattering depends on the modulus square of the mode electric field $EE^*$ at the location of the scattering defect, *i.e.* at the rough sidewall [3.7, 3.20]. Assume that there is a hypothetical local refractive index perturbation $\Delta n$ at the

waveguide surface in question. The variational theory for waveguides [3.21] (which will be explained in detail in Section *5.4*) predicts that the change in effective index $\delta N_{eff}$ induced by a $\Delta n$ will also vary with the overlap integral of $EE^*$ with $\Delta n$ at the perturbed surface, as illustrated in Equation (3.14):

$$\delta N_{eff} = \frac{\iint (n \cdot \Delta n) EE^* \cdot dxdy}{N_{eff} \iint EE^* \cdot dxdy} \tag{3.14}$$

This suggests that $\delta N_{eff}$ and the scattering loss $\alpha$ should both scale identically with local mode intensity $EE^*$ overlap integral at the surface. A relative measure of the mode overlap with the ridge sidewall can therefore be obtained by using a mode solver [3.22] to calculate the differential change in effective index $\delta N_{eff}$ induced by a very small change in waveguide ridge width $\delta d$. A scaling factor can thus be obtained by taking the ratio of $\delta N_{eff}$ between a ridge waveguide and a channel waveguide (*i.e.* the sidewalls are completely etched down to the buried oxide layer):

$$s = \left( \frac{\delta N_{effr} / \delta d}{\delta N_{effc} / \delta d} \right) \tag{3.15}$$

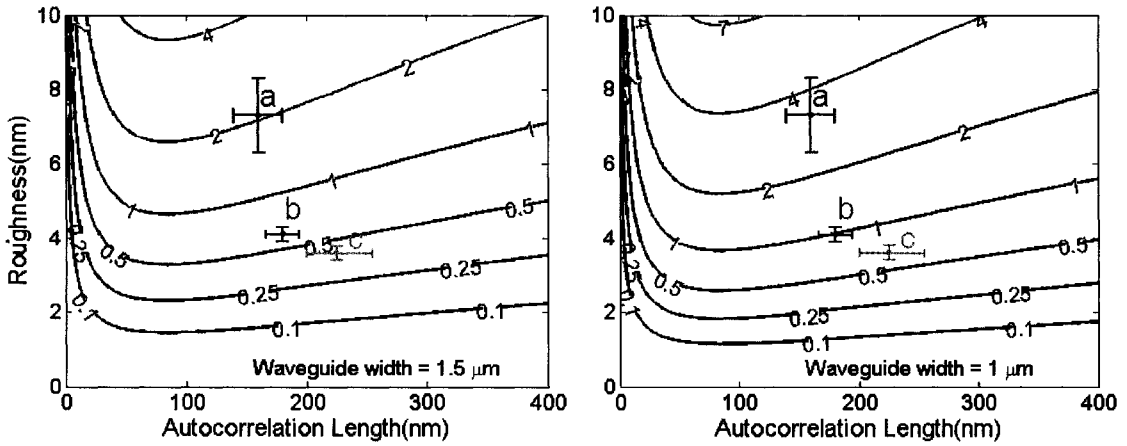
where $\delta N_{effr}$ is the change in the effective index in a ridge waveguide, and $\delta N_{effc}$ is the change in effective index in a channel waveguide of the same width. This ratio should give an accurate estimate of the relative strength of the waveguide mode coupling to the waveguide ridge sidewalls for different etch depths. Applying these corrections to the basic Payne-Lacey expression from Equation (3.7), an expression for the sidewall scattering loss $\alpha$ in a ridge waveguide is obtained:

$$\alpha = 4.34 \frac{\sigma^2}{\sqrt{2} k_o d^4 N_{eff}} g \cdot f \cdot s \tag{3.16}$$

where $s$ is the scaling factor of Equation (3.15) and $N_{eff}$ is the calculated effective index of the fundamental waveguide mode. As the etch depth is increased, the ridge waveguide will approach a channel waveguide geometry and the scaling factor $s$ will approach unity. Conversely as the ridge etch becomes shallower, $s$ approaches zero and sidewall scattering vanishes. The scaling factors of the TE and TM polarization have a slightly different dependence on waveguide width, because of the difference in the rate of change of mode index in both polarizations.

A series of excess loss contour maps with respect to roughness and autocorrelation length have been generated using the modified Payne and Lacey model of Equation (3.15). The calculated loss is in TM polarization, because light is assumed to be polarized with the electric field parallel to the scattering surface in the original Payne-Lacey model [3.7]. The excess loss contour map of our 1.5 μm and 1 μm-wide SOI waveguides is plotted in Fig. 3.11(a) and 3.11(b), respectively.

The excess scattering losses on the contour maps are relative to the scattering loss of the 2 μm nominal waveguides. For any given correlation length $L_c$ larger than 75 nm, the loss increases monotonically with roughness. As $L_c$ increases, the dependence of loss on roughness $d\alpha/d\sigma$ reduces, as shown by the widening gap between two contour lines. However, at the vicinity of 75 nm, loss increases more rapidly with the change in roughness. When $L_c$ decreases below 75 nm, loss decreases rapidly with decreasing $L_c$, and the $d\alpha/d\sigma$ again reduces.




(a) (b)

Fig. 3.11. Contour map of the relative TM scattering loss (in dB/cm) as a function of roughness $\sigma$ and correlation length $L_c$ for waveguides of (a) 1.5 μm and (b) 1 μm width. Each solid line represents a contour of constant loss. The indicators on the map mark the measured roughness and correlation lengths with error bars obtained from the SEM analysis, for the three processes, *a*: Process I: contact lithography, *b*: Process II: e-beam lithography with positive resist and lift off, and *c*: Process III: e-beam lithography with negative resist.

Keeping the correlation length away from the high loss-increment region (*i.e.* around 75 nm for our waveguide configuration) has therefore a more prominent effect on loss reduction than merely reducing roughness. This general trend is also observed and reported in the literature [3.8, 3.19]. This indicates that loss reduction is viable through optimization of the patterning process that changes the characteristics of correlation length. In particular, we have shown that it is important to choose an optimal combination of lithography technique and resist chemistry. For instance, it has been noticed that the contact lithography produces smaller $L_c$ (~ 160 nm) with the characteristic of a Gaussian autocorrelation function, while e-beam lithography produces larger $L_c$ (~ 180 to 225 nm)

with the characteristic of an exponential autocorrelation function.

In order to compare the measured loss with the measured $\sigma$ and $L_c$, we have marked the measured $\sigma$ and $L_c$ from SEM with the error bars, for all three processes on the loss contour maps, as indicated by marker *a*, *b*, and *c* in Fig. 3.11(a) and 3.11(b). From the locations of the markers, we can derive the approximate values of the losses using the loss contour lines. For example, for a 1.5 μm waveguide fabricated by contact lithography process, the measured loss is around 2.24 dB/cm (TM), while the derived loss centers around 2.08 dB/cm on the contour map. Similar comparisons have been made on waveguides with 1.75, 1.5, and 1.25 μm for all three processes using the contour maps. The results of all comparisons are summarized in Table 3.2.

Table 3.2. Measured scattering loss versus derived loss from the contour maps (both in TM polarization).

| *Fabrication Process* | *Waveguide Width (μm)* | *Measured Loss (dB/cm)* | *Derived Loss (dB/cm)* |
|---|---|---|---|
| Process I (Contact lithography) | 1 | 6.63 ± 2.59 | 3.33 ± 1.26 |
| | 1.25 | 4.01 ± 1.54 | 2.79 ± 1.06 |
| | 1.5 | 2.24 ± 1.01 | 2.08 ± 0.79 |
| | 1.75 | 2.05 ± 0.96 | 1.16± 0.44 |
| Process II (E-beam lithography with positive resist) | 1 | 2.82 ± 1.54 | 0.99± 0.14 |
| | 1.25 | 2.48 ± 0.68 | 0.83± 0.12 |
| | 1.5 | 1.35 ± 0.20 | 0.61 ± 0.09 |
| | 1.75 | 1.24 ± 0.05 | 0.34 ± 0.06 |
| Process III (E-beam lithography with negative resist) | 1 | 0.50 ± 0.30 | 0.66 ± 0.13 |
| | 1.25 | 0.39 ± 0.15 | 0.53 ± 0.13 |
| | 1.5 | 0.35 ± 0.39 | 0.41 ± 0.08 |
| | 1.75 | 0.11 ± 0.17 | 0.23 ± 0.05 |

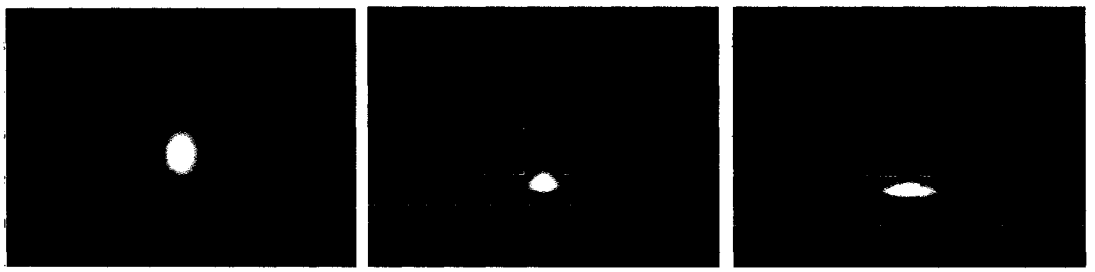
In Table 3.2, the losses calculated from the measured roughness profiles are consistently smaller than the measured waveguide losses by a factor of two or less. Similarly, the roughness values obtained by simply fitting the Payne and Lacey model to

the measured loss in Fig. 3.10 are correspondingly larger than the measured roughness data of Fig. 3.11. These differences are to be expected, since the model includes only loss from the etched sidewalls and neglects scattering at other waveguide surfaces. Nevertheless, the results are in good qualitative agreement given the experimental uncertainties. This comparison shows the functionality of our star couplers in collecting loss data that are verifiable by process monitoring tool such as SEM and AFM. The star coupler measurement technique therefore provides useful process optimization feedback.

The measured losses reported so far are excess loss relative to the 2 μm reference waveguides. To determine the absolute scattering losses, we can use the Fabry-Perot method [3.9] to measure the loss of a 2 μm wide reference waveguide. By this method, we obtain losses of 7.01 dB/cm and 1.02 dB/cm for reference waveguides fabricated by contact lithography (Process I) and e-beam lithography (Process III), respectively. The absolute losses of all other smaller waveguides can then be calculated readily by adding their own excess loss to the respective 2 μm reference waveguide loss.

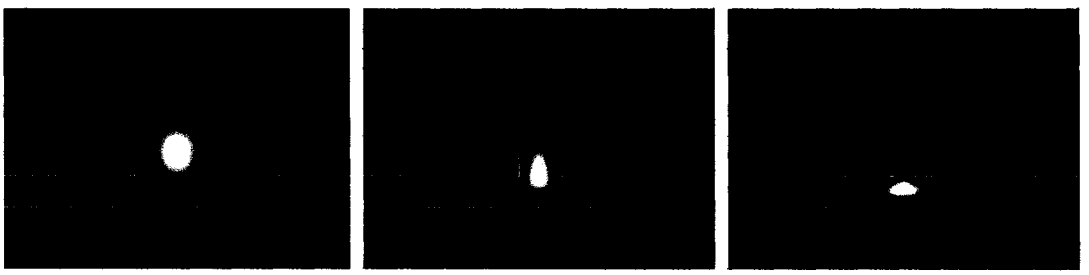
The excess loss of waveguides with a width of 1 μm and below will be discussed next. In a micron-size or sub-micron size SOI ridge waveguide, the major loss mechanisms include scattering not only from sidewall roughness, but also from slab surface roughness and the ridge lower corners. The mechanisms responsible for the scattering loss depend on the profile and confinement of the guided mode in the waveguide. Using mode matching method [3.22] to simulate the profile of the fundamental TE and TM modes in our waveguides, changes in mode confinement and the

mode extension into the underlying slab have been observed, as the waveguide width is reduced below 1 μm.



(a) 2 μm (b) 0.8 μm (c) 0.4 μm

Fig. 3.12. TE mode profile of our SOI ridge waveguides of different widths.



(a) 2 μm (b) 0.8 μm (c) 0.4 μm

Fig. 3.13. TM mode profile of our SOI ridge waveguides of different widths.

As shown in Fig. 3.12 and 3.13, for wider ridges, the scattering loss of our waveguides (etch depth of 1.8 μm) is caused primarily by the interaction of the mode with the sidewall roughness. However, with narrowing ridge width the mode is forced into the underlying slab, the sidewall scattering decreases and loss becomes more dependent on slab surface roughness and the properties of the ridge lower corners (texture, stress distribution etc.).

The theoretical excess losses of our waveguides can be calculated from Equation (3.16). In this calculation, the correlation lengths are fixed at their measured mean values

as given in Table 3.1 (since the change in loss is relatively insensitive to the correlation lengths within the measured range), therefore scattering losses vary only with waveguide width and roughness. Various loss curves were generated using r.m.s roughness as an adjustable parameter, and the best fit to the measured loss data is shown in Fig. 3.10. The generated loss curves are shown by the solid lines, while the results of the fitting are summarized in Table 3.3.

Table 3.3. R.m.s. roughness measured from SEM versus roughness derived from fitting the measured loss.

| *Fabrication Process* | *Measured roughness (nm)* | *Fitted roughness (nm)* |
|---|---|---|
| Process I (Contact lithography) | 7.7 ± 1.0 | 13.5 ± 1.5 |
| Process II (E-beam lithography with positive resist) | 4.3 ± 0.2 | 9.0 ± 1.5 |
| Process III (E-beam lithography with negative resist) | 3.6 ± 0.2 | 5.0 ± 1.0 |

The fitted roughness agrees with the measured roughness from SEM, within a factor of 2. The remaining discrepancy may have several possible origins. The effect of surface roughness of the slab on the scattering loss of our small-dimension ridge waveguides is not accounted in the theoretical loss calculation. Therefore our theoretical loss calculated from the modified Payne-Lacey expression is underestimated, and result in a corresponding overestimate in the roughness extracted by fitting to the Payne and Lacey model. In addition, the roughness in the theoretical model is described by either an exponential or Gaussian autocorrelation function, which is at best an oversimplified approximation of the real roughness profile.

The polarization dependent losses (PDL = $\alpha_{TE}$ - $\alpha_{TM}$) of the SOI samples with the roughest and smoothest sidewalls are plotted in Fig. 3.14. For waveguides with rough sidewalls, such as those processed by contact lithography, when the waveguide width is large (*i.e.* 1.5 μm and above), the TE modes experience more loss than the TM modes, giving rise to a positive PDL. This is because the TE mode field vector is polarized normal to the sidewalls; therefore the optical field has a higher sensitivity to sidewall roughness induced scattering [3.23]. The TM mode field vector, on the other hand, is polarized parallel to the sidewall, therefore is more susceptible to scattering by the slab surface roughness. As expected, the polarization dependence at large waveguide width is more prominent in samples with rough sidewalls, and less significant in the e-beam patterned waveguides with smoother sidewalls.

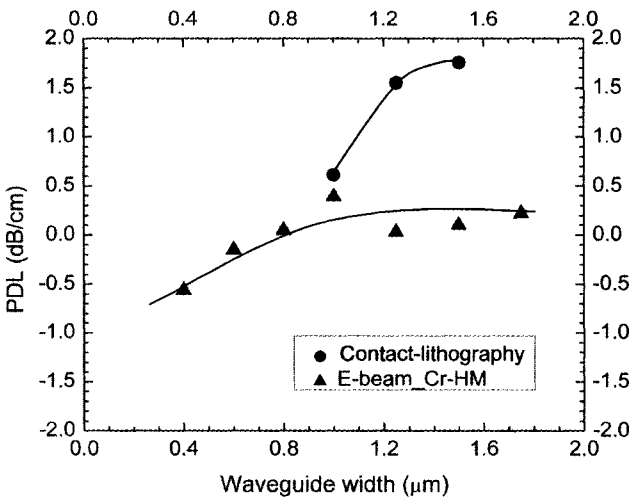



Fig. 3.14. Polarization dependence loss (PDL) of the waveguides as a function of decreasing width [3.11].

With decreasing waveguide width, the mode extends into the underlying slab, resulting in a change in the intensity of field overlap with the sidewall. As shown in Fig. 3.12 and 3.13, TE modes extend faster into the slab than TM modes as the waveguide width reduces. The overlapping optical field of the TE mode at the sidewall thus becomes smaller than the TM mode at the same waveguide width, for instance, at 0.8 μm. As a result, the TM mode experiences more scattering than TE mode and the PDL decreases rapidly towards negative values. The further extension of the mode profile into the underlying slab causes a change in the loss mechanism, from strongly sidewall roughness dependent to slab surface roughness dependent. This further reduces the PDL because TM modes which are more sensitive to surface scattering, will continue to experience higher loss than TE modes.

The star coupler loss measurement technique allows determination of PDL at various SOI waveguides width for a given set of roughness statistics, therefore provides useful feedback to the waveguide design and fabrication processes to minimize PDL.

## 3.5. DISCUSSION OF PROCESS SCHEMES FOR LOSS REDUCTION

After describing the techniques to measure sidewall roughness and scattering loss of SOI waveguides, it is worthwhile to continue to explore some processing schemes for roughness and loss improvement. There are several suggested processing schemes in the literature, such as using thermal oxidation [3.19] or thermal annealing in hydrogen [3.24] to smoothen the waveguide sidewalls after fabrication. These are post-process treatments that have demonstrated successful roughness reduction, but would require holding the

fabricated waveguide samples at elevated temperature above 1000°C in a properly controlled ambient. This requirement may not be met in some applications where thermal budget is a concern, especially involving the integration with CMOS transistors and diodes. Thermal oxidation scheme [3.19] has been shown to be effective in smoothing waveguide sidewalls, but this scheme requires more careful design considerations and the choice of a suitable SOI platform to accommodate the necessary Si consumption from the formation of sacrificial oxides. In the design of complex structures such as star couplers or AWGs, it may be challenging to predict the dimensional changes of tapers and variable gaps in the waveguide arrays during subsequent sacrificial oxidation step. Another interesting process scheme has been proposed and demonstrated by N. G. Tarr *et al.* [3.25], which employs local oxidation of silicon (LOCOS) technique to fabricate waveguide devices, such as unbalanced Mach-Zehnder Interferometers (MZIs). This process scheme eliminates the need for post-process oxidation smoothing, but is subjected to similar design challenges in predicting dimensional changes of taper structures introduced during LOCOS process. In this regard, other roughness improvement schemes such as the wet chemical oxidation treatment proposed by D. K. Sparacin *et al.* [3.26] appears attractive, because it preserves dimensional integrity and allows for a good control in the reaction kinetics with great smoothing efficiency.

While most post-processing treatments require elaborate processing steps after the device fabrication, there have also been several reported schemes on reducing sidewall roughness during the patterning steps by modifying the exposure process, either using resist with lower molecular weights or smaller aggregates [3.2, 3.27, 3.28]. More

importantly, some authors have reported successful experiments on optimizing masking schemes [3.2, 3.28, 3.29, 3.30], mainly on III-V waveguides to improve roughness. The results from these experiments, may be leveraged onto SOI systems, suggest that incorporating masking layers (such as hardmasks) to the patterning stacks generally improve process window for smoothening sidewall roughness.

## 3.6. CONCLUSION

We successfully demonstrate the effectiveness of star couplers as a test structure for assessing optical scattering loss induced by sidewall roughness. A large number of optical loss data can be obtained rapidly, since the relative loss of many waveguides can be collected in a single measurement. This provides a powerful tool for process engineers to assess various waveguide fabrication processes.

Relating the scattering loss and roughness analysis, we show that the process utilizing e-beam lithography with negative resist and a Cr hardmask for ICP dry etching produces the smoothest waveguide sidewalls and lowest scattering loss. We have modeled the measured ridge waveguide losses at various widths and demonstrated that the fitted sidewall roughness is in reasonable agreement with the measured roughness from SEM. In conclusion, this star coupler technique is capable of studying roughness induced scattering loss and will enable optimization of process parameters that critically affect waveguide sidewall roughness.

# CHAPTER 4

# THERMO-OPTIC MODULATION I: DEVICE DESIGN AND MATERIALS

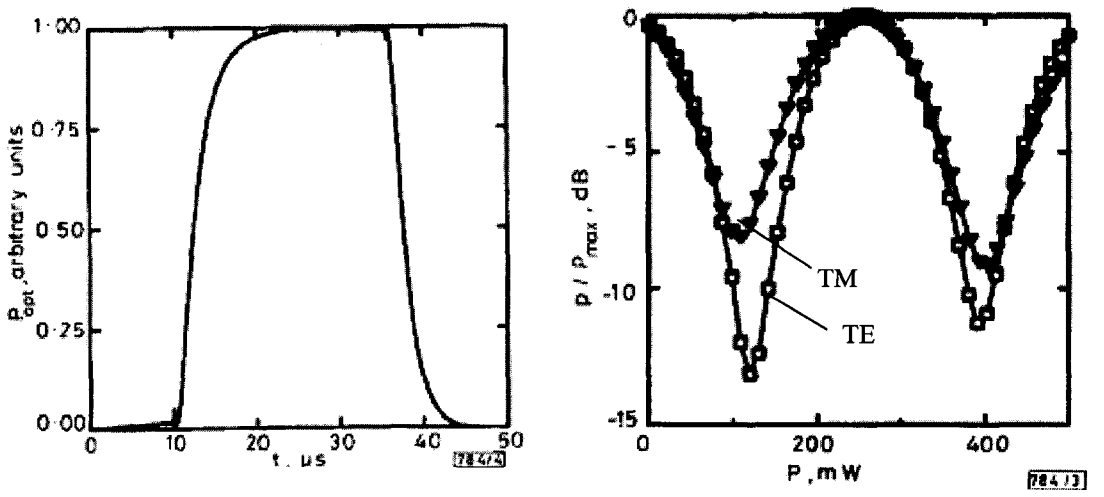
The objective of the research described in this chapter is to improve understanding of parameters that determine thermo-optic modulation in a SOI platform, therefore allowing optimization of the design of SOI thermo-optic switches and modulators employing a Mach-Zehnder Interferometer (MZI) configuration.

## 4.1. OPTICAL SWITCHES AND MODULATORS

Low power consumption and low cost optical switches built on planar lightwave circuits (PLCs) have been receiving increasing interest from the telecommunication industry, especially in the applications of optical cross-connect (OXC) and optical add-drop multiplexing (OADM). Various designs that differ in the choice of materials, device configuration or modulation mechanism, have been demonstrated experimentally and reported in the literature. Several reports on the optical switches exploiting thermo-optic effect based on a MZI configuration have been published. These switches are made with $SiO_2$ [4.1], SiON [4.2], $Si_3N_4$ [4.3], polymers [4.4, 4.5], and Si [4.6-4.13] waveguides. $SiO_2$ and $Si_3N_4$ switches typically require 100-300 mW of power and switch in 100 μs to

10 ms, while polymer and Si switches require less power (10-100 mW) and Si switches have faster speed ranging from 1 to 100 μs. The lower power of polymer and Si switches is a result of a higher refractive index change with temperature, as determined by the thermo-optic coefficient, $dn/dT$. This thermo-optic coefficient is approximately $dn/dT \sim -10^{-4}$ for polymer and $dn/dT = 1.86 \times 10^{-4}$ for Si, compared to around $dn/dT \sim 10^{-5}$ for $SiO_2$ and $Si_3N_4$. The improved switching speed of Si switches is mainly due to their higher thermal conductivity and smaller dimensions as a result of the miniaturization from a high index contrast system.

The current research focuses on the study of Si MZI thermo-optic switches built on an SOI substrate. Among recent publications, Fischer *et al.* [4.6] first demonstrated an SOI MZI thermo-optic switch with large waveguide cross-section. The SOI waveguides were fabricated on a substrate with a 1 μm-thick buried oxide layer. The total core Si layer thickness was 4 μm and the ridge waveguide had an etch depth of 2 μm. The nominal width of the ridge waveguide was 3 μm and the waveguide was covered by a 0.5 μm $SiO_2$ cladding layer. The heater was made of 0.5 μm Ti layer with a width of 10 μm. As a result of large waveguide cross-section and heater width, the device length was very large, with a length of 15 mm (15,000 μm). The switch had a fast response of 5 μs, with a switching power of 150 mW, as shown in Fig. 4.1.




(a) (b)

Fig. 4.1. (a) Rise time and (b) power consumption of Fischer's SOI thermo-optic switch [4.6]. The square data points in (b) represent the measured output power of TE polarization while the inverse triangular data points represent TM polarization.

The low power was a marked improvement over many polymer, SiON and $SiO_2$ switches [4.1, 4.2, 4.4, 4.5]. Another important achievement in this research was the derivation of a theoretical expression to estimate the switching speed and power requirement of an SOI MZI thermo-optic switch. Using this expression, Fischer *et al.* were able to calculate the values for the switching time and power in their switch, which showed a good agreement with their experimental results. However, the operating wavelength of this switch was at 1.3 μm instead of 1.55 μm and there were two major drawbacks for this switch. The extinction ratio was rather low (~9 dB for TM) and the switch was slightly polarization dependent, as shown in Fig. 4.1(b).

Y. Li *et al.* [4.9, 4.10, 4.11, 4.12] proposed an SOI thermo-optic switch integrated with a spot size mode converter [4.9, 4.10], as shown in Fig. 4.2.

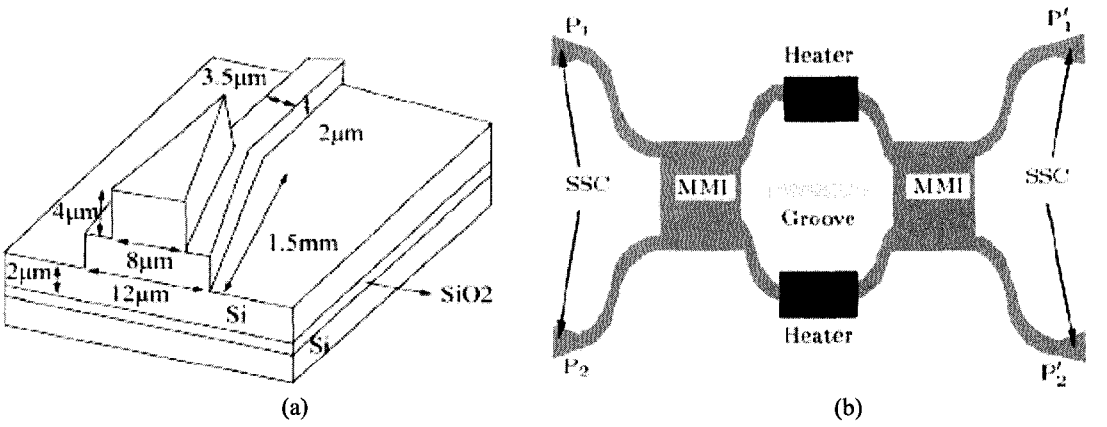



Fig. 4.2. (a) A spot size mode converter integrated with the SOI switch made by Y. Li *et al.*, and (b) schematic of this MMI-MZI thermo-optic switch [4.9, 4.10].

Their SOI switch adapted a MZI configuration based on ridge waveguides with a width of 3.5 μm, height of 4 μm and an etch depth of 2 μm. A mode converter (or coupler) was incorporated at the end of the input and output port to expand the waveguide mode in order to match the fiber mode. In addition, MMI splitters were used instead of y-splitters to improve fabrication tolerance, reduce radiation losses from splitting and to minimize uneven splitting that will deteriorate the extinction ratio. The upper cladding layer thickness was reduced to 70 nm to improve heat conduction. The extra design efforts paid off as the switching was able to achieve a high extinction ratio of 20 dB, and a rise time of 4.6 μs with less than 200 mW input power. The insertion loss was reduced to 10 dB and the polarization dependence loss was as low as 0.8 dB. The device size was also greatly reduced compared to Fischer's switch to an area of 1,000 × 20 $\mu m^2$ (length × width).

The current state-of-the-art silicon photonic technology revolves around the

research in devices that can be fabricated on a silicon photonic wire platform. A more compact, faster SOI switch based on photonic wire waveguides was proposed by Espinola *et al.* in 2003 [4.8], as shown in Fig. 4.3.

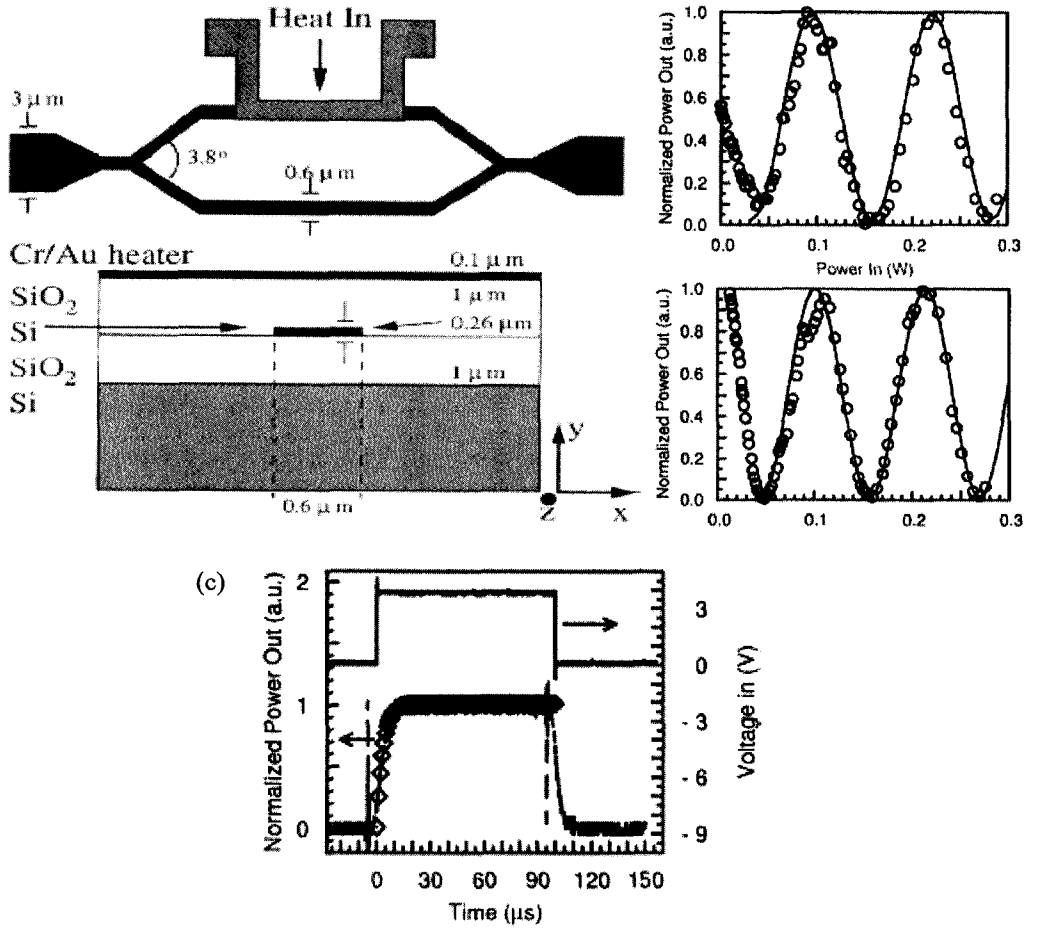


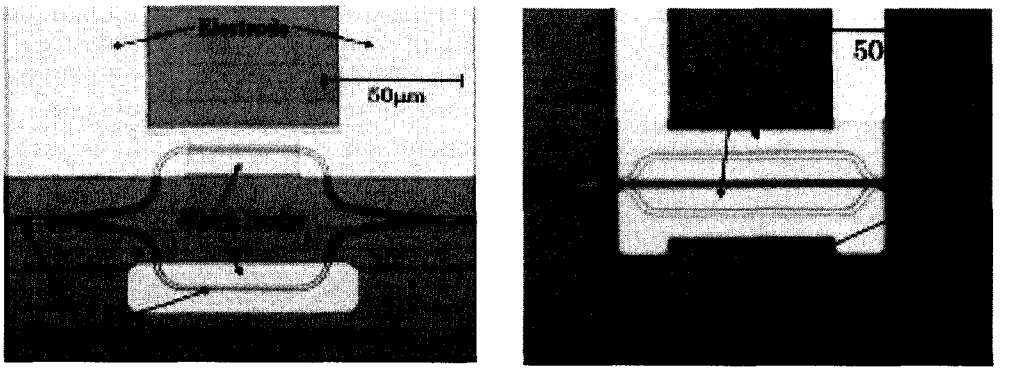

Fig. 4.3. (a) Schematic diagram, (b) power consumption and (c) switching speed of the SOI thermo-optic switch made by Espinola *et al.* [4.8].

The device was built on a thin SOI substrate, consisting of a 0.26 μm-thick Si core layer on a 1 μm-thick BOX layer. The heater was made of Cr/Au bilayer defined also by liftoff process to a width of 10 μm. Using a channel waveguide configuration and

an e-beam lithography for patterning, the waveguide cross-section was reduced to 0.6 μm × 0.26 μm (width × height), as shown in Fig. 4.3. As a result, the total size of this switch was only 1,500 × 200 $\mu m^2$ (length × width), which is several orders of magnitude smaller than Fischer's switch. This switch was designed to operate at a waveguide of $\lambda$ = 1.55 μm.

Benefiting from the smaller device size, the power consumption was at 50 mW and the rise time of this SOI thermo-optic switch was less than 3.5 μs, as shown in Fig. 4.3(b) and (c). The extinction ratio had been improved to more than 15 dB compared to Fischer's switch, but the polarization dependence loss of the switch was unavoidable because of the asymmetry in the cross-section of the channel waveguides. The major drawback of this switch was the substantial insertion loss of 32 dB due to modal mismatch and a considerable scattering from the sidewall roughness. This highlights the importance of our research efforts in reducing both coupling loss and scattering loss.

Apart from research groups, many telecom companies are also trying to develop commercially available ultra-small OXC switches on an SOI chip. Another example of thermo-optic switch built on Si photonic-wire waveguides was developed by T. Chu *et al.* from NEC [4.13]. Building the switch with photonic-wire waveguides of dimensions of 0.3 μm × 0.3 μm (weight × height), the device occupied only 85 × 40 $\mu m^2$ (length × width), as shown in Fig. 4.4. This is the smallest size reported in the literature to date.




(a) 1 x 1 optical switch (b) 1 x 2 optical switch

Fig. 4.4. A (a) 1×1 and (b) 1×2 thermo-optic switch based on Si photonic wire waveguides that are made by T. Chu *et al.* from NEC [4.13].

However, because the mode expands considerably into the cladding layer as the waveguide width reduces to around 200 nm [4.14, 4.15], the thickness of both cladding layers has to be increased to 1 μm, to isolate the delocalized mode from the metal heater and prevent significant propagation loss. This design limitation obviously sacrifices the switching speed because the heater has to be placed far from the waveguide core by the thick cladding. This explains the slow switching speed of 100 μs obtained by the NEC's switch, which is more than one order of magnitude slower than the speed achievable by ordinary SOI thermo-optic switches consisting of ridge waveguides. However, the power consumption of NEC's switch was reasonably low, at 90 mW, and the extinction ratio was as high as 19 dB for TE and 27 dB for TM mode. Again, without a proper mode converter or coupler, the insertion loss was as high as 15-22 dB due to modal mismatch. Clearly, design of the reported photonic-wire SOI thermo-optic switches has not been optimized and the study to improve their switching performance is an interesting research

direction.

Other researchers have proposed different designs or methods to increase the switching speed and reduce power. Spector *et al.* have proposed a sub-μs, sub-mW SOI thermo-optic switch operated by direct heating of waveguides [4.16]. In their research, the waveguides were implanted with $B^+$ ions at a dose of $2.5\times10^{13}$ /cm$^2$, and a current was conducted through the waveguides to generate heat. This direct heating method could achieve a rise time of 0.6 μs and a low power of 6 mW for an SOI switch on a 200 × 60 μm$^2$ area. However, the implantation and annealing steps will load up the thermal budget especially when electronic circuits are integrated on the same chip, and raise the complexity of the fabrication process.

Another method to obtain sub-microsecond response time in SOI MZI thermo-optic switches by using a differential modulation technique has been proposed by T. Aalto *et al.* [4.17, 4.18]. As shown in Fig. 4.5, this technique could markedly improve the speed to less than 0.7 μs but would require additional electronic control circuits to generate the differential heating pulses. Moreover, the power consumption increases greatly with the complexity of heating pulses. For instance, in the 'off' stage of switches with differential heating, the static power is continuously consumed. As opposed to normal thermo-optic switches, this static power consumption will surge to a very high level when several switches are cascaded into a matrix.

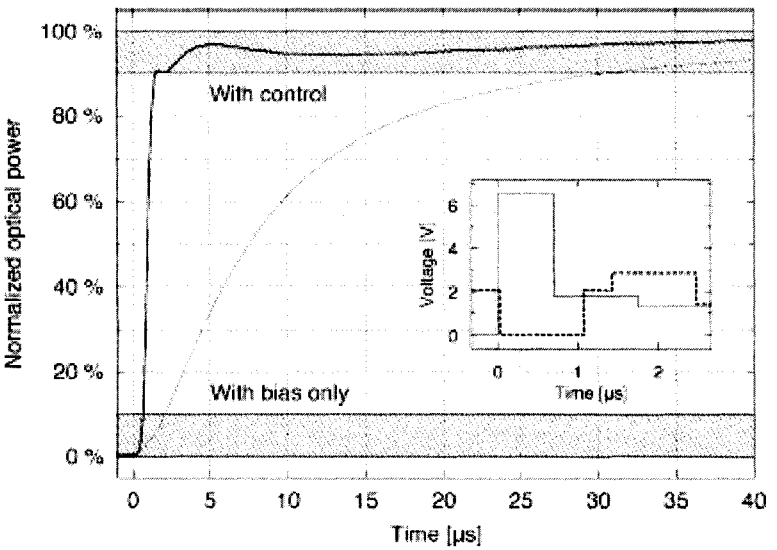



Fig. 4.5. The differential modulation technique proposed by T. Aalto *et al.* to achieve fast switching in SOI MZI thermo-optic switch [4.17].

In conclusion, a number of reports on SOI MZI thermo-optic switches capable of achieving a speed of several microseconds and a power consumption of hundreds of milliwatt or less have been published over the last 15 years. However, no systematic work has been done on the impact of device parameters such as cladding material, MZI arm spacing and heater geometry, which are essential to the optimization of switching speed and power requirement.

The objective of this research is to establish a comprehensive understanding of the fundamental parameters that affect the performance of thermo-optic switches. By systematically applying the design rules developed in this work, designers should be able to create a switch that will surpass the performance of existing devices.

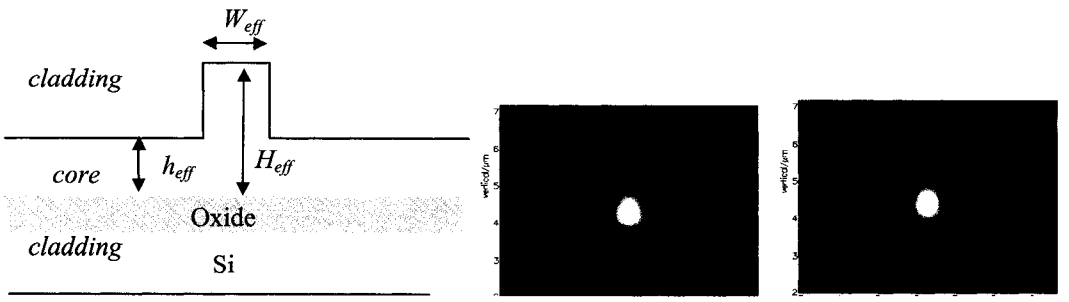
## 4.2. DESIGN OF SOI MACH-ZEHNDER INTERFEROMETER SWITCHES

### *4.2.1. Basic Building Blocks: SOI Waveguides and MZI*

SOI waveguides used in modulators and switches must operate in single mode. In a multimode waveguide modulator, modes having different phase velocity and propagation constant will respond differently to the thermo-optic actuation, causing interference and distortion of the resultant output signal. The phase shift in the signal induced by the thermo-optic modulation will become unpredictable in the presence of multimode interference. As a result, the output intensity of the modulator will not vary systematically with the input signals.

Soref *et al.* [4.19] has proposed an empirical formula as a guideline for the single-mode design. Given the geometry of a SOI ridge waveguide shown in Fig. 4.6(a), the proposed single-mode criterion is [4.19]:

$$t < 0.3 + \frac{r}{\sqrt{1-r^2}} \quad where \quad t = \frac{W_{eff}}{H_{eff}}, r = \frac{h_{eff}}{H_{eff}} \tag{4.1}$$




(a) (b) (c)

Fig. 4.6. (a) Design of SOI ridge waveguide for single-mode operation, (b) TE and (c) TM fundamental mode profile in a 1.5 μm single-mode SOI ridge waveguide with an etch depth of 1.3 μm, simulated using FIMMWAVE mode solver.

We have chosen the SOI ridge waveguides forming our MZI arms to have a nominal width of 1.5 μm and a core layer thickness ($H_{eff}$) of 2.2 μm. The maximum etch depth corresponding to a single mode operation as derived from Soref's formula is therefore 1.42 μm. Shallow etch depth causes high bend loss especially for SOI waveguides with branches, splitters and curves. Thus, in our design we selected etch depth of 1.3 μm for our 1.5 μm waveguides. The mode profile and effective index of the fundamental modes (in both TE and TM polarization) in the designed waveguide are determined using FIMMWAVE. The simulated mode profiles are shown in Fig. 4.6, and the simulation result from FIMMWAVE further confirms the designed waveguide is single mode.

In the design of a thermo-optic switch, the aim is to first design a single-mode SOI waveguide of negligible absorption loss by the heater layer. Minimum thickness of the cladding layer required to prevent this absorption loss is estimated using a mode solver "MENU", developed by André Delâge at NRC. To calculate the absorption loss, instead of using a complicated three-dimensional ridge configuration that requires a full vectorial solution to the Maxwell equations, the waveguide can be modeled using a two-dimensional slab waveguide. The effective indices, the extinction coefficients (imaginary part of the effective index) $k$, and the propagation constants of the guide fundamental modes in the slab waveguide can then be calculated in MENU using the transfer matrix method. The fundamental TE mode profile of our slab waveguide is shown in Fig. 4.7(a).

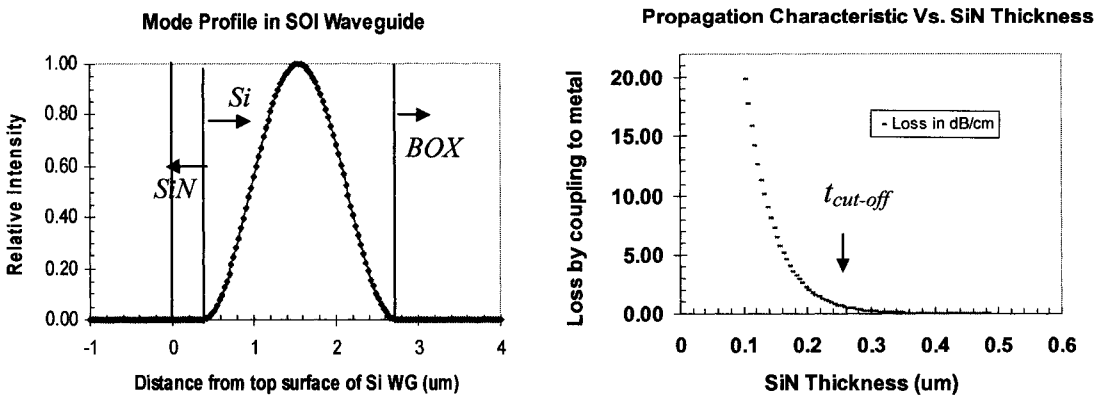



Fig. 4.7. (a) Profile of the fundamental TE mode in a two dimensional SOI slab waveguide with a 0.4 μm thick SiN upper cladding; (b) absorption loss as a function of the SiN cladding thickness.

When the SiN upper cladding layer is sufficiently thick, the mode is confined within the Si waveguide layer and isolated from the top metal. As the thickness of SiN decreases, the mode leaks into the metal and absorption loss increases accordingly. The absorption loss could be calculated using Beer-Lambert's law of absorption [4.20]:

$$\alpha = -4.34 \times 10^{-2} \frac{4\pi k}{\lambda} \quad (dB/cm) \tag{4.2}$$

where λ is the operating wavelength in meter and $k$ is the extinction coefficient of the mode. The cut-off thickness corresponding to an absorption loss of less than 0.1 dB for the entire device (0.1 dB/mm for an MZI length of 1 mm) is shown in Fig. 4.7(b). At a thickness of 0.3 μm, the absorption loss is slightly less than 1 dB/cm, but the loss increases exponentially with reducing thickness below this value. This cutoff thickness of 0.3 μm is calculated using the optical properties of an e-beam evaporated Cr layer and a hydrogenated PECVD SiN layer, which are obtained from various sources listed in the

footnotes. The optical and material properties of the claddings, core and metal layers are summarized in Table 4.1[1]. In our simulation models and the fabricated samples, we actually doubled the hydrogenated SiN thickness to 0.6 μm to eliminate any metal absorption loss.

Table 4.1 Material properties of Si, $SiO_2$, SiN and Cr.

| *Material* | *Refractive index, n @1.55μm* | *Extinction coefficient, k @1.55μm* | *Thermal conductivity, σ (W/μm·K)* | *Specific heat, c (J/kg·K)* | *Density, ρ (kg/μm³)* |
|---|---|---|---|---|---|
| Si | 3.476 | - | $1.48\times10^{-4}$ | 710 | $2.33\times10^{-15}$ |
| $SiO_2$ | 1.445 | - | $1.1\times10^{-6}$ | 745 | $2.3\times10^{-15}$ |
| SiN | 1.910 | $4.9\times10^{-6}$ | $3\times10^{-5}$ | 170 | $2.5\times10^{-15}$ |
| Cr | 3.674 | 4.19 | $9.37\times10^{-5}$ | 450 | $7.14\times10^{-15}$ |

### *4.2.2. Heat Conduction Equations*

Prior to the discussion on the design of MZI thermo-optic switches, an introduction to fundamental heat transfer equations would be useful for the understanding of the kinetics and thermo-dynamics of heat conduction in the thermo-optic switches.

Heat conduction is the transfer of thermal energy between neighboring molecules in a medium or substance in the presence of a temperature gradient. The law of heat conduction, also known as Fourier's law, states that the flow rate of heat energy through a medium is proportional to the negative temperature gradient and to the area at right angles, to that gradient, through which the heat is flowing [4.21-4.23]. The Fourier's law is most commonly stated in its differential form [4.21, 4.22]:

---

[1] Data from source:
(i) www.standnes.no/chemix/preiodictable/thermal-conductivity-table.htm
(ii) www.standnes.no/chemix/preiodictable/specific-heat-capacity.htm
(iii) www.standnes.no/chemix/preiodictable/density-chart-elements.htm
(iv) www.engineeringtoolbox.com/air-properties-d_156.html

$$\Phi_q = -\sigma \cdot \nabla T \tag{4.3}$$

where $\Phi_q$ is the local heat flux or the amount of energy in W/μm$^2$, flowing through a surface area of $A$ per unit time. The thermal conductivity $\sigma$ of the medium has units of W/(μm·K) and $\nabla T$ is the temperature gradient with units of K/μm. The negative sign indicates that the heat flux is always flowing from high to low temperature. For a steady-state unidirectional heat flow in an isotropic medium, the thermal gradient $\nabla T$ in the equation can simply be replaced by $\partial$T/$\partial$x [4.21, 4.22]. Note that the thermal conductivity of a material could vary with temperature, but generally the variation is small over a significant range of temperatures for most common materials.

In addition to the rate of heat flow, it is also important to determine the rate of temperature rise in the conducting medium during heating. The equation describing the variation in the temperature with time $t$ is given by [4.21, 4.22]:

$$\frac{\partial T}{\partial t} = \alpha \cdot \nabla^2 T + q = \frac{\sigma}{\rho c} \cdot \left( \frac{\partial^2 T}{\partial x^2} \right) + q \tag{4.4}$$

where $\alpha$ is the thermal diffusivity which has a unit of μm$^2$/s, $\nabla^2$T is the divergence of the temperature gradient, and $q$ is a constant heat source. For unidirectional heat flow in an isotropic medium, $\nabla^2 T$ can be replaced by $\partial^2$T/$\partial$x$^2$ [4.21-4.23]. The thermal diffusivity $\alpha$ can be represented by the ratio of the thermal conductivity $\sigma$ to the heat capacity of the medium. The heat capacity is the product of the density $\rho$ (in kg/μm$^3$) and specific heat $c$ (in J/kg·K), and has a unit of J/μm$^3$·K. The thermal diffusivity $\alpha$ measures the ability of a

material to conduct thermal energy relative to its ability to store thermal energy. Using the values for the thermal conductivity $\sigma$, density $\rho$ and specific heat $c$ in Table 4.1, thermal diffusivity of Si, SiN and $SiO_2$ is calculated to be $\alpha_{Si} = 8.95\times10^7$ J/μm$^3$·K, $\alpha_{SiN} = 7.06\times10^7$ J/μm$^3$·K and $\alpha_{SiO2} = 6.42\times10^5$ J/μm$^3$·K, respectively. This explains in part the increase in speed observed in Si thermo-optic switches compared to oxide switches. The larger $\alpha$ of SiN also implies that the rate of temperature rise in a SiN cladding will be faster than in a $SiO_2$ cladding layer.

### *4.2.3. Thermo-optic Switch Based on MZI Configuration*

Table 4.2 summarizes the material properties and geometrical parameters of our SOI MZI thermo-optic switch design. In this table, the architecture of the thermo-optic switch is described in terms of its various constituents, namely the waveguide core and cladding layers, the heater strip and the MZI module. There are many critical material and geometrical parameters that affect the switching performance, but in this research only selective parameters are studied using a finite-difference thermal simulator. The selected simulation parameters are:

(i) MZI arm spacing (or separation), $d_{MZI}$

(ii) Heater position offset, $d_h$

(iii) Heater width, $w_h$

(iv) Cladding material

(v) Cladding thickness, $t_{SiN}$

Table 4.2. Summary of the design architecture of the SOI MZI thermo-optic switches.

| Component | Attribute/Material | Critical Parameter | Simulation Parameter |
|---|---|---|---|
| **SOI waveguide** | | | |
| • nominal width, $w$ | 1.5 μm | Yes | |
| • ridge height, $t$ | 1.3 μm | Yes | |
| • slab thickness, $h$ | 0.9 μm | Yes | |
| • buried oxide thickness, $t_{SiO2}$ | 0.4 μm | Yes | |
| **Cladding layer** | PECVD SiN | | |
| • thickness, $t_{SiN}$ | 0.1, 0.4, **0.6** μm | Yes | Yes |
| **Heater strip** | Cr | | |
| • thickness, $t_h$ | 50 nm | Yes | |
| • width, $w_h$ | 0.5, 1.5, **4** μm | Yes | Yes |
| • offset or distance from MZI arm, $d_h$ | −4,..., −1,0, 1, ..., 3, 4 μm | Yes | Yes |
| • length, $l_h$ | 800 μm | Yes | |
| **MZI** | | | |
| • arm length, $L$ | 800 μm | Yes | |
| • arm separation, $d_{MZI}$ | 5, **10**, 20, 40, 100 μm | Yes | Yes |
| • branching angle, $\theta = \tan^{-1}(Y/X)$ | **0.32**, 0.37, 0.39° | Yes | |

+ The values in **bold** denote the default values in our standard simulation models. We vary the values of the selected parameters to study their effects on the switching performance.

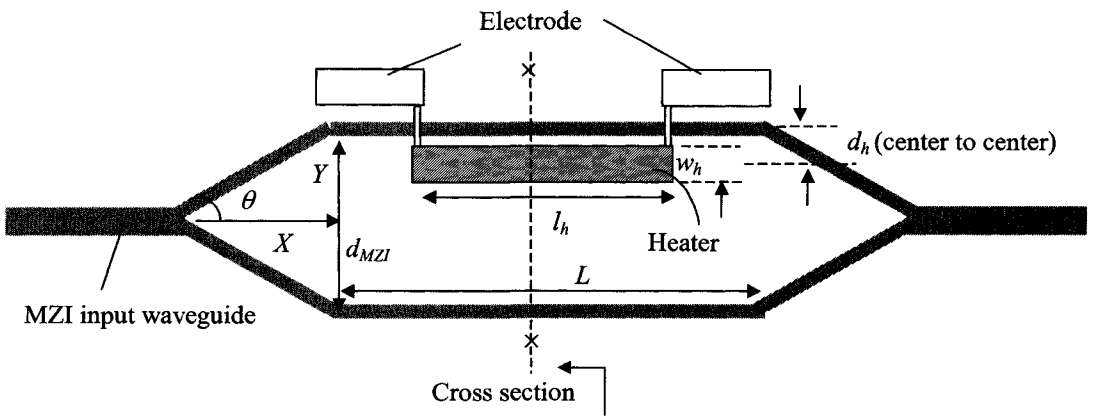



Fig. 4.8. Design of a 1×1 thermo-optic switch based on a y-branch MZI configuration.

Fig 4.8 shows a typical 1×1 MZI thermo-optic switch made of two y-branches and two parallel straight waveguides. A metallic heater is added on top of one waveguide, hereafter referred to as the "heated" (or "active") arm to introduce a phase shift. The unheated waveguide serves as a "reference" (or "passive") arm" with a zero phase. The cross-section of this 1×1 MZI thermo-optic switch is illustrated in Fig. 4.9(a), showing the definition of heater position offset, with respect to the center of the ridge waveguide.

The primary consideration in the design is how the output intensity and extinction ratio vary in the presence of thermal stimulant. Referring to Fig. 4.9(b) of the 1×1 y-branch MZI switch, assume that the input power $I_{in}$ splits into both arms at the y-branch, giving $I_1$ power to the upper arm and $I_2$ power to the lower arm.

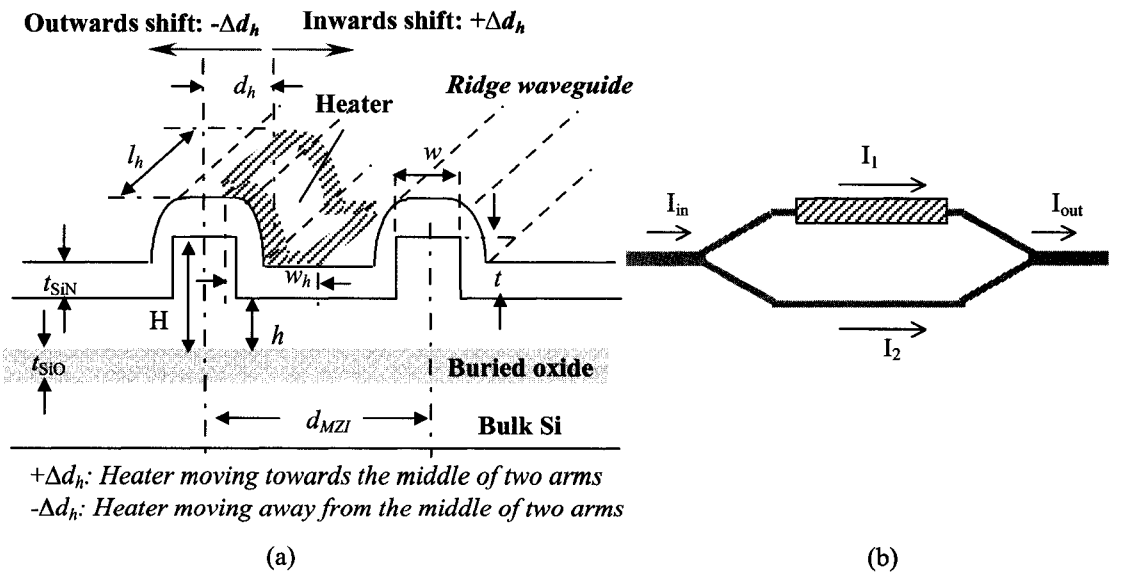



Fig. 4.9. (a) Cross-section of our 1×1 y-branch MZI thermo-optic switch, (b) Intensity and phase of the guided power in different segments of the MZI switch.

Upon heating, assuming that the phase of the optical mode in the upper arm is shifted by $\Delta\phi = \Delta\beta \cdot L$, while the phase shift of the mode in the lower arm is zero. The electric field of the mode in the lower arm is given by:

$$\mathbf{E_2} = |E_2| e^{i(\beta L - \omega t)} \tag{4.5}$$

while the electric field of the mode in the upper arm is given by:

$$\mathbf{E_1} = |E_1| e^{i[(\beta L + \Delta\phi) - \omega t]} = |E_1| e^{i[(\beta + \Delta\beta)L - \omega t]} \tag{4.6}$$

The output intensity is proportional to the square modulus of the total field. Therefore, the combined output power at the second y-branch is:

$$I_{out} \sim |\mathbf{E_1} + \mathbf{E_2}|^2 = E_1^2 + E_2^2 + 2E_1E_2\cos(\Delta\phi) \tag{4.7}$$

The maximum output power $I_{out,max}$ and minimum output power $I_{out,min}$ are thus given by:

$$I_{out,\max} = E_1^2 + E_2^2 + 2E_1E_2 = (E_1 + E_2)^2 \tag{4.8}$$

$$I_{out,\min} = E_1^2 + E_2^2 - 2E_1E_2 = (E_1 - E_2)^2 \tag{4.9}$$

The maximum extinction ratio of the 1×1 thermo-optic MZI switch is given by:

$$ER = -10\log\left(\frac{I_{out,\max}}{I_{out,\min}}\right) \tag{4.10}$$

Fig. 4.10 shows the plotted extinction ratio with respect to the ratio of the power split. In order to maximize this extinction ratio, the power splitting ratio between two arms has to be as even as possible.

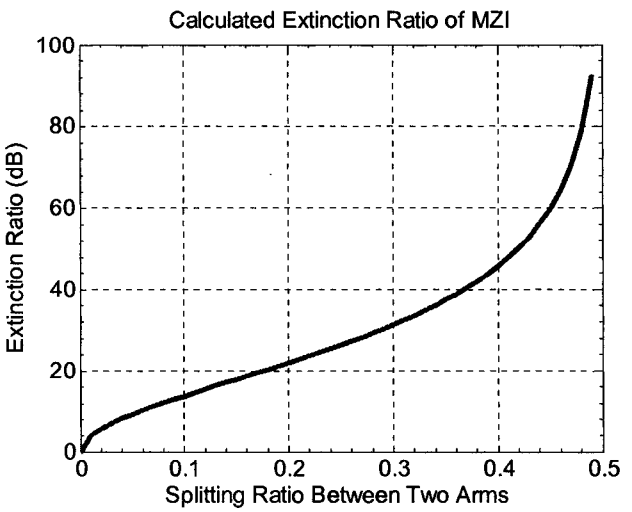



Fig. 4.10. Calculated extinction ratio in a 1×1 y-branch MZI thermo-optic switch as a function of power split between the two arms.

The total phase shift introduced by a heater with a length $L$ is given by:

$$\Delta\phi = \Delta\beta \cdot L = \Delta T\left(\frac{\partial N_{eff}}{\partial T}\right)\cdot\left(\frac{2\pi}{\lambda}\right)L \tag{4.11}$$

In a Si or SOI waveguide, the change in effective index $\partial N_{eff}$ with respect to temperature is approximately equal to the change in the refractive index of Si. The desired temperature change to introduce $\pi$-phase shift for switching is therefore:

$$\Delta T = \left(\frac{\partial n}{\partial T}\right)_{Si}^{-1}\cdot\frac{\lambda}{2L} \tag{4.12}$$

For an 800 μm-long Si ridge waveguide with a thermo-optic coefficient of $1.86\times10^{-4}/K$, operating at 1550 nm wavelength, the temperature change that gives rise to a $\pi$-phase shift (complete switching) can be calculated using Equation (4.12):

$$\Delta T = \frac{1}{1.86\times10^{-4}} \cdot \frac{1.55}{2(800)} = 5.2K \approx 6K$$

A temperature rise of at least 6 K (after rounding the value) is required to cause a π-phase shift.

Fig. 4.11(a) shows the switching characteristics of a y-branch MZI thermo-optic switch with respect to the change in temperature. The corresponding change in the effective index for the π-phase shift is determined to be $\Delta N_{eff} = 9.7\times10^{-4}$.

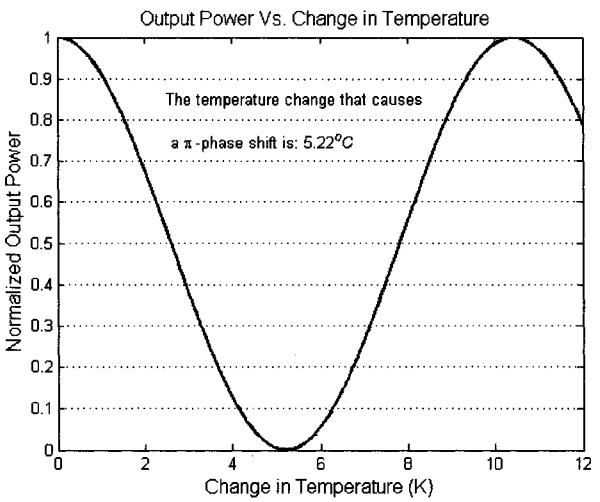



Fig. 4.11. A plot of output power vs. temperature change for a 1×1 MZI thermo-optic switch.

From the design perspectives, the most critical parameter to consider is the total power required to generate the required temperature change. A simple theoretical estimation of the power and switching speed of an SOI MZI thermo-optic switch based on prior work by Fischer *et al.* [4.6] is presented below.

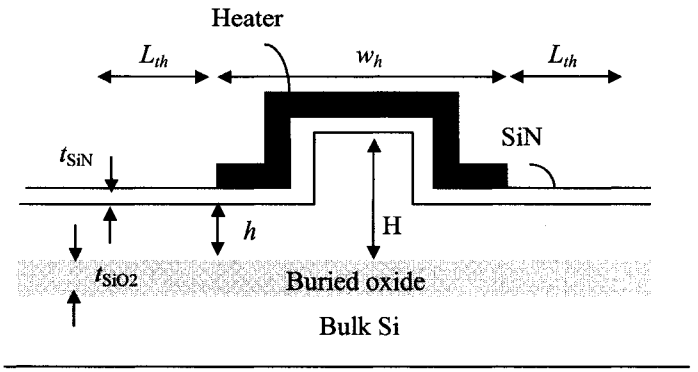



Fig. 4.12. Illustration of various geometrical parameters used in the derivation of the switching characteristics of an SOI MZI thermo-optic switch.

Imagine that an SOI ridge waveguide with a thin metallic heater covering its SiN upper cladding layer has all the geometrical parameters given in Fig. 4.12. The heat energy required to heat up a volume $V$ to a temperature change of $\Delta T$ is given by [4.23]:

$$Q = c \cdot \rho \cdot V \cdot \Delta T \tag{4.13}$$

where $\rho$ is the density of the heat conduction medium. The power required to induce a temperature gradient $\Delta T/\Delta x$ can be derived from Equation (4.3):

$$P = -\Phi_q \cdot A = A \cdot \frac{\sigma}{\Delta x} \Delta T \tag{4.14}$$

where $A$ is the heated area, $\Delta x$ is the thickness of the waveguide and cladding layers. The time taken to generate the require heat energy $Q$ at the given power $P$ is:

$$\tau_g = \frac{Q}{P} \tag{4.15}$$

The desired change in temperature to introduce a $\pi$-phase shift for switching has been given in Equation (4.12):

$$\Delta T = \left(\frac{\partial n}{\partial T}\right)_{Si}^{-1} \cdot \frac{\lambda}{2L}$$

Using Equation (4.12), the π-phase shift power can be written as:

$$P = \frac{\sigma A}{\Delta x}\left(\frac{\partial n}{\partial T}\right)_{Si}^{-1} \cdot \frac{\lambda}{2L}$$

In the multilayer stack consisting of SiN, Si and $SiO_2$ layers, the composite thermal resistance $\Delta x/\sigma$ is the sum of the thermal resistance of individual layer [4.22]:

$$\frac{1}{\sigma/\Delta x} = \frac{1}{\sigma_{SiN}/t_{SiN}} + \frac{1}{\sigma_{Si}/t_{Si}} + \frac{1}{\sigma_{SiO2}/t_{SiO2}} \tag{4.16}$$

Since the thermal conductivity of the buried $SiO_2$ layer is 100 times slower than Si and 10 times slower than SiN, the heat generated by the metal heater will be contained within the Si core layer after flowing through the SiN cladding layer, and will spread laterally onto the two wings of the ridge waveguide. The lateral diffusion length of this heat can be estimated by [4.6]:

$$L_{th} = \sqrt{t_{SiO_2} h}\sqrt{\frac{\sigma_{Si}}{\sigma_{SiO_2}}} \tag{4.17}$$

The heated area $A$ can be represented by $L \cdot w_{th}$, where $L$ is the length of the heater, $w_{th}$ is the sum of the lateral thermal diffusion lengths $L_{th}$ and the heater width $w_h$, such that $w_{th} = w_h + 2L_{th}$. Therefore, the π-phase shift power can now be rewritten as:

$$P_\pi = \frac{\sigma \cdot w_{th}}{\Delta x} \cdot \frac{\lambda}{2}\left(\frac{\partial n}{\partial T}\right)_{Si}^{-1} \tag{4.18}$$

Using Equation (4.16), this π-phase shift power can be further simplified into [4.6]:

$$P_\pi = \frac{w_{th}}{\frac{t_{SiN}}{\sigma_{SiN}} + \frac{t_{Si}}{\sigma_{Si}} + \frac{t_{SiO_2}}{\sigma_{SiO_2}}} \cdot \frac{\lambda}{2}\left(\frac{\partial n}{\partial T}\right)_{Si}^{-1}$$

$$P_\pi \approx \sigma_{SiO_2} \cdot \frac{w_h + 2L_{th}}{t_{SiO_2}} \cdot \frac{\lambda}{2}\left(\frac{\partial n}{\partial T}\right)_{Si}^{-1} \tag{4.19}$$

The denominator in Equation (4.18) is dominated by the relatively small thermal conductivity of $SiO_2$.

Assuming that the speed of the switch is characterized by $\tau_g$, which is the time taken to heat up a stack of waveguide and cladding of volume $V$ and thickness of $\Delta x$, from turning on the heat source to the point where steady state is reached. From Equation (4.13) and (4.14), the time to reach steady state $\tau_g$, is given by:

$$\tau_g = \frac{c\rho V \cdot \Delta T}{\sigma A\left(\frac{\Delta T}{\Delta x}\right)} = \frac{c\rho V \cdot \Delta x}{\sigma A}$$

since $V = A \cdot \Delta x$, $\tau_g$ can be rewritten as :

$$\tau_g = \frac{c\rho \cdot \Delta x^2}{\sigma} \tag{4.20}$$

The cut off frequency (or bandwidth) of the switch $f_g$ is therefore given by:

$$f_g = \frac{1}{2\pi\tau_g} = \frac{\sigma}{2\pi c\rho \Delta x^2} \tag{4.21}$$

Combining Equation (4.18) and (4.21), the relation between cutoff frequency and power

can then be expressed by:

$$f_g = \frac{P_\pi}{\pi \rho c \lambda w_{th} \cdot \Delta x} \left( \frac{\partial n}{\partial T} \right)_{Si}$$

Let $a = w_{th} \cdot \Delta x$ be the cross-sectional area, the above expression can be rewritten as [4.6]:

$$f_g = \frac{P_\pi}{\pi \rho c \lambda a} \left( \frac{\partial n}{\partial T} \right)_{Si} \tag{4.22}$$

In the multilayer stack consisting of SiN, Si and $SiO_2$ layers, the reciprocal of the composite thermal capacitance $1/\rho ca$ is the sum of the reciprocal of thermal capacitance in individual layer:

$$\frac{1}{\rho ca} = \frac{1}{w_{th}} \left( \frac{1}{\rho_{SiN} c_{SiN} t_{SiN}} + \frac{1}{\rho_{Si} c_{Si} t_{Si}} + \frac{1}{\rho_{SiO_2} c_{SiO_2} t_{SiO_2}} \right) \tag{4.23}$$

Since the specific heat capacity of SiN is much smaller than Si and $SiO_2$, the denominator in Equation (4.23) is dominated by the thermal capacitance of SiN, such that the cutoff frequency is determined by:

$$f_g = \frac{P_\pi}{\pi \rho_{SiN} c_{SiN} \lambda \cdot w_{th} \cdot t_{SiN}} \left( \frac{\partial n}{\partial T} \right)_{Si} \tag{4.24}$$

The power consumption and cutoff frequency of our SOI-MZI thermo-optic switch can be calculated using the set of equations from (4.13) to (4.24). Our switch contains ridge waveguides of the following geometries: top Si thickness of 2.2 μm, buried oxide thickness of 0.4 μm, etch depth of 1.3 μm, ridge width of 1.5 μm, SiN thickness of 0.6 μm, and a 4 μm-wide Cr heater of 50 nm thickness. From the material

properties of Si, $SiO_2$ and SiN given in Table 4.1, the power required to introduce a $\pi$-phase shift in our switch can be calculated using Equations (4.17) and (4.19), so that $L_{th}$= 6.96 μm and $P_\pi$ = 250 mW. Given that $w_{th} \cdot t_{SiN}$ = 10.75 $\mu m^2$, the cutoff frequency of $f_g$ = 494 kHz is calculated using Equation (4.24). The corresponding rise time [4.24] of our switch (approximated to a one stage low pass RC network) is approximately 1μs.

It is important to note that the derived theoretical equations for power and switching speed calculation are based on the steady state heat flow in a single ridge waveguide with a heater on top. This model will only describe the thermal response in a MZI arm of a thermo-optic switch where heat flow is confined within one lateral diffusion length of the heater. The theoretical estimation ignores the heat flow beyond the lateral diffusion length and the time required for the temperature to be stabilized in the unheated (passive) arm. It therefore does not provide a good estimate of the power and speed of any MZI switches where the reference arms are affected by the applied heat. The theoretical analysis predicts that the maximum switching speed for our 1.5 μm-wide ridge waveguide MZI thermo-optic switch with minimum arm spacing is around 1 μs and the $\pi$-phase shift power is approximately 200 mW.

The significance of these theoretical equations is to address the relation between switching speed and power consumption, as well as the key parameters that affect their values. In particular, Equation (4.18) explains the lower power consumption in SOI switches compared to silica switches by the larger thermo-optic coefficient of Si compared to $SiO_2$. Equation (4.21) predicts a switching speed gain with the use of a SiN

cladding layer because of its lower specific heat capacity compared to $SiO_2$ cladding layer. Equation (4.22) highlights the tradeoff relation between switching speed and power consumption, and also attributes the faster switching speed of SOI switches to its larger thermo-optic coefficient compared to $SiO_2$. In addition, according to Equation (4.19), power consumption of an SOI thermo-optic switch can be improved without sacrificing speed by:

(i) increasing the buried oxide thickness $t_{SiO_2}$

(ii) reducing the slab thickness $h$ (increasing etch depth or reducing Si core layer thickness), which decreases lateral diffusion length $L_{th}$

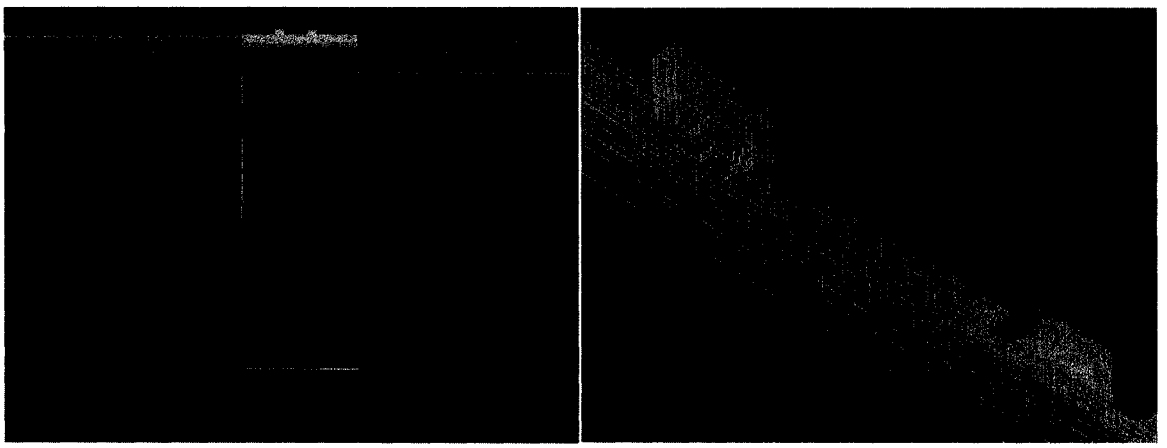
(iii) reducing the heater width $w_h$.

## 4.3. THERMAL SIMULATION USING A FINITE-DIFFERENCE SIMULATOR

Power consumption and switching speed of the switches can be calculated from thermal simulation using a finite-difference simulator "ATAR" [4.25]. The basis of power and speed calculation from the thermal simulation in ATAR is established from the heat conduction equations presented in Section *4.2.2*. The power can be derived from the steady-state heat transfer described by Equation (4.3), while the speed can be determined from the transient state heat flow described by $\partial T/\partial t$ given in Equation (4.4).

In ATAR, each simulation model is created by taking a thin slice of the MZI switch along its cross-section. To improve simulation speed, each model is built with a graded grid system which varies from a coarse grid at the boundaries of the simulation

window to a fine grid in the active regions, as shown in Fig. 4.13.



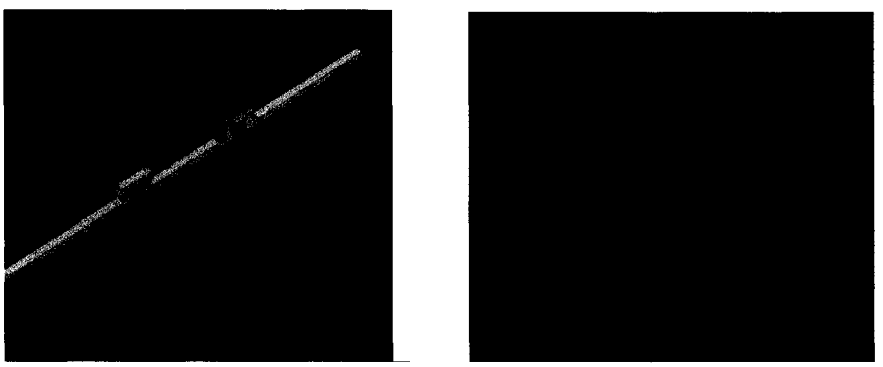
(a) (b)

Fig. 4.13. (a) Variable grid size of the model, (b) Dense and fine grids surrounding the heated ridge waveguide are essential in generating the details of heat distribution in that area.

The thermal simulation algorithm in ATAR is based on the Transmission Line Matrix (TLM) method, which models heat flow as a sequence of voltage pulses traveling through a matrix network of transmission lines [4.25]. The simulation assumes a linear heat flow in the model according to the linear heat conduction equations given in Section *4.4.2*, with the bulk Si substrate as a heat sink satisfying the boundary condition of constant substrate temperature of 300K at a substrate depth of 600 μm. The rise in substrate temperature due to heating should have minimal effect on thermal simulation results since the switching speed and power of the MZI switches are determined by the differential temperature between the two MZI arms (will be described in detail later) instead of their absolute temperatures. The substrate-temperature-induced change in optical and thermal properties of the waveguide core and cladding is negligible over the

range of 30°C. For instance, the change in the effective index of the guided mode due to thermo-optic effect is in the order of $10^{-3}$, which is negligible compared to the effective index itself ($N_{eff} \sim 3.4$). The thermal conductivity of $SiO_2$ changes by approximately 2% and thermal conductivity of Si changes by around 10% [4.26] over a range of 30°C, indicating that the simulation results will change by less than 10%.

Fig. 4.14 show the MZI switch model built in ATAR and the simulated temperature distribution of the model.



(a) (b)

Fig. 4.14. (a) Structural model of SOI thermo-optic switches in ATAR thermal simulation, (b) Simulated temperature distribution of the model.

The rise time of the MZI thermo-optic switch is defined as the time taken for the differential temperature between the two MZI arms to reach an approximate steady state. In order to determine the rise time of the switch using ATAR, the analysis of rise time can be approximated by counting the time taken for the differential temperature to reach 6°K at the input power of $P_{\pi}$.

The outputs from ATAR simulation are:

(i) The $\pi$–phase shift power required to achieve the 6°K temperature difference between the heated and reference arms.

(ii) The time taken for the differential temperature to reach 6°K (rise time for a $\pi$–phase shift) at the given input power of $P_{\pi}$.

(iii) The thermal gradient along any MZI cross section at any time after a heating pulse is applied.

(iv) The 2D temperature contours of the MZI cross-sections at any given time, including after the 6°K temperature difference has been established.

### *4.3.1. MZI arm spacing*

Fig. 4.15 is a plot of simulated differential temperature as a function of the time after the heating power is switched on, for the MZI switches with different arm spacing. From the plot, the effect of MZI arm spacing on the rise time can be determined. The simulated arm spacing varies from 5, 10, 20, 40 to 100 μm. Reducing arm spacing has a prominent effect on the rise time of the switches. For example, as shown in the inset in Fig. 4.15, decreasing arm spacing from 100 μm to 5 μm reduces the rise time drastically from 100 μs to 1.5 μs, which is a two-order of magnitude improvement.

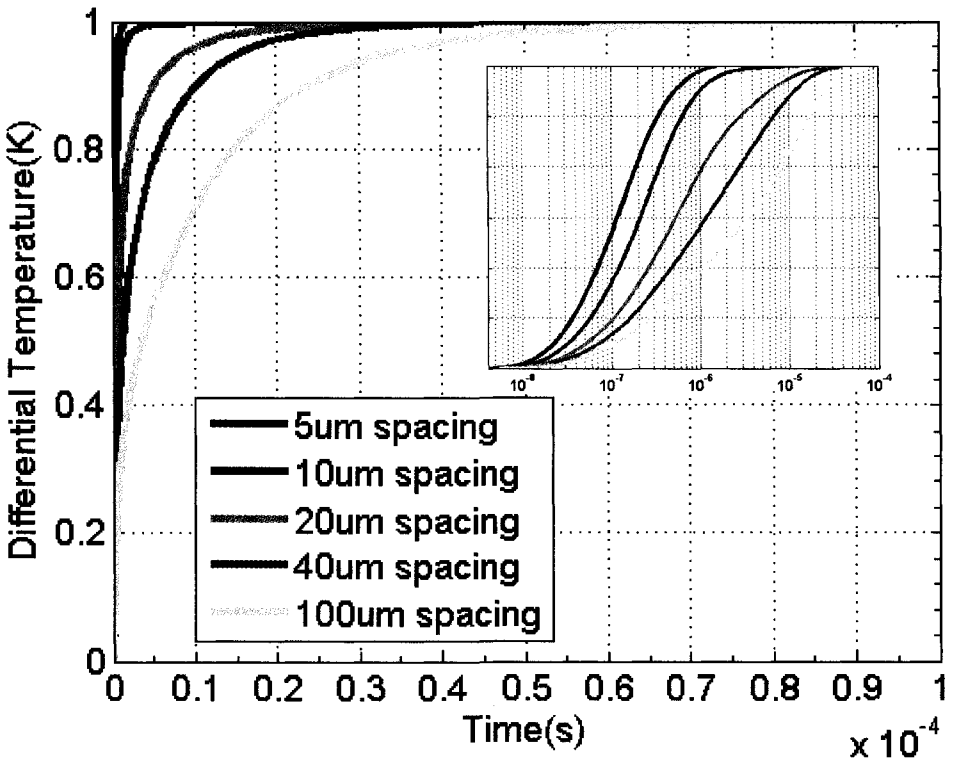



Fig. 4.15. The plot of differential temperature versus the time after heating power is switched on, for MZI switches with arm spacing of 5, 10, 20, 40 and 100 μm.

The strong dependence of rise time on the arm spacing can be explained by the heat flow mechanism in MZI. The rise time is determined in two major steps: (i) how fast heat is generated by the heater to increase the local temperature of the heated arm, and (ii) how fast heat is conducted to the unheated arm to stabilize the temperature such that the *relative temperature* or *temperature difference between the two arms* no longer changes. These steps are illustrated in Fig. 4.16, which is a plot of the temperature distribution at different time interval, along the cross-section of a 10 μm-spaced MZI with a heater placed on top of its right arm.

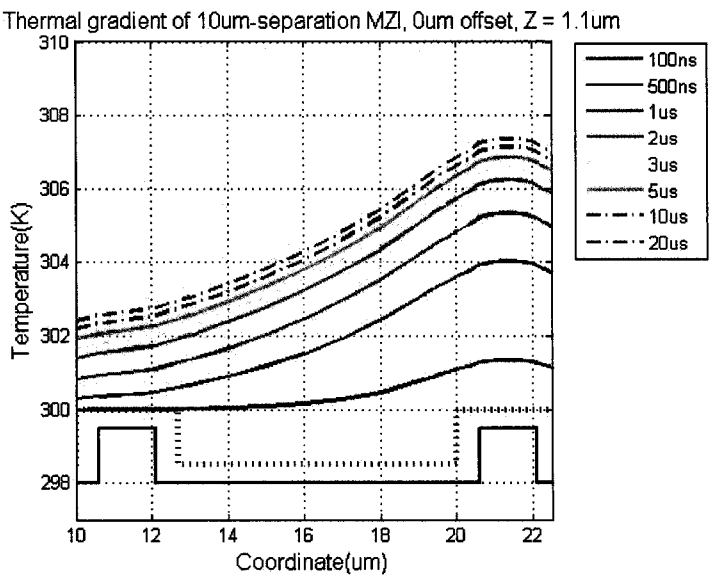
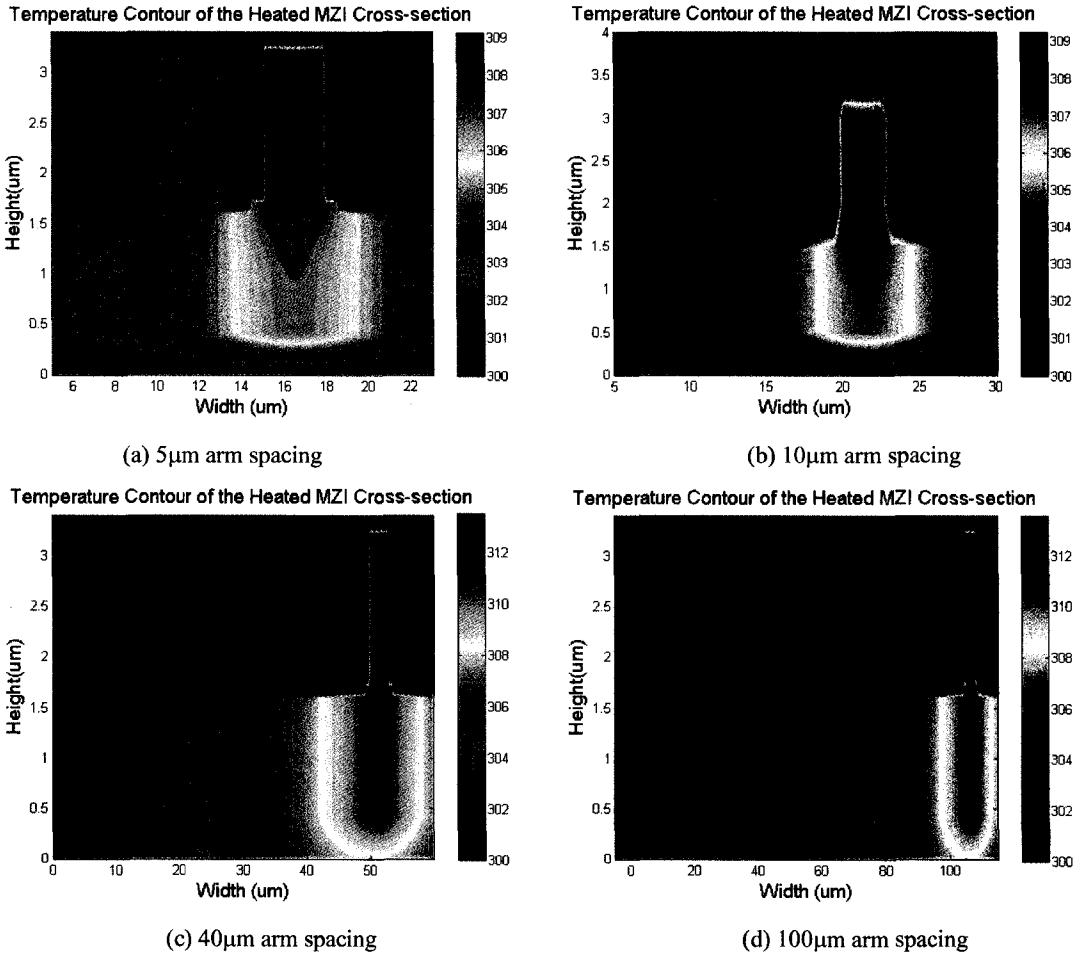



Fig. 4.16. Temperature profile along the cross-section of a 10 μm-spaced MZI thermo-optic switch at different sampling time intervals.

As shown in Fig. 4.16, within 100 ns after turning on the heater, the right arm is heated up by more than 1 °K, while the left arm's temperature remains unchanged. This means that a thermal gradient has been established across the arms. In the next 400 ns, this thermal gradient grows steeper as the heat continues to build up rapidly and locally in the right arm, while only small amount of heat is conducted to the left arm to increase its temperature. From 500 ns to 1 μs, more heat has been generated in the right arm but the rate of heat conduction to the left arm is still slower, resulting again a steeper thermal gradient. This thermal kinetic continues until approximately 5 μs, when the rate of heat generation and heat conduction become equal. At this point, the switching cycle is complete because the *temperature difference between the two arms* has stabilized, although their absolute temperatures continue to rise.

The explanation for the observed speed improvement with reducing MZI arm spacing is illustrated in Fig. 4.17. These are the temperature contours obtained from simulation in the transient stage after heating for 20 μs.




(a) 5μm arm spacing

(b) 10μm arm spacing

(c) 40μm arm spacing

(d) 100μm arm spacing

Fig. 4.17. (a) Temperature contour of various MZI switches with different arm spacing: 5, 10, 40 and 100 μm, after heating for 20 μs.

As the arm spacing increases, the heat distribution is localized in the heated arm rather than reaching out to the reference arm. It is simply due to the longer heat conduction path across larger arm spacing that the rise time to a steady temperature

difference becomes longer. In other words, the speed of a MZI thermo-optic switch is critically determined by its arm spacing and the time required for the local thermal gradient to reach a steady state.

Another important attribute of the MZI switch is the power required to achieve a $\pi$–phase shift. The $\pi$–power of our switch is determined using the steady-state simulation engine of ATAR. For any given power, the temperature difference between the cores of heated and reference waveguides can be extracted from the simulation. Given that heat flow equations are linear, the power required to achieve a 6°K temperature difference can therefore be extrapolated.

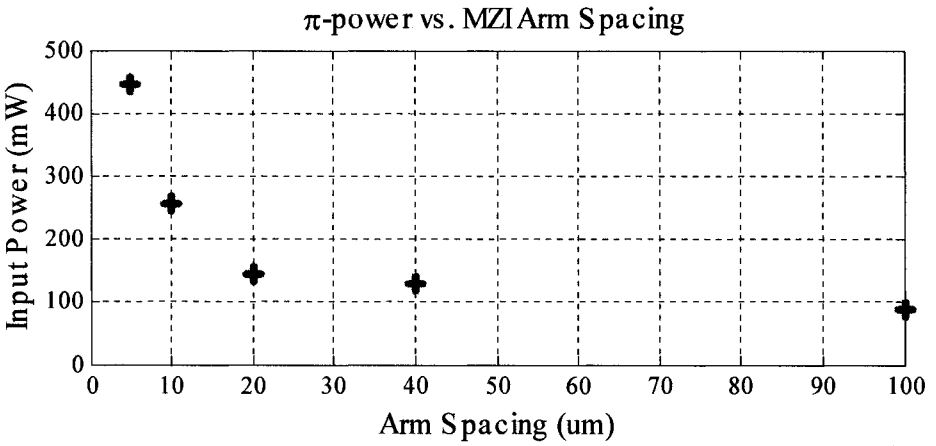



Fig. 4.18. The π-phase shift power of MZI switches with the arm spacing of 5, 10, 20, 40 and 100 μm.

As shown in Fig. 4.18, the $\pi$–phase shift power $P_\pi$, obtained from ATAR simulation of a 10 μm-spaced MZI switch is approximately 250 mW. This value is in approximate agreement with the 200 mW power calculated from the theoretical

estimation in Section *4.2.2*. Less power is required to achieve the $\pi$–phase shift as the arm spacing increases, an observation that is readily explained in Fig. 4.17. Adversely, by reducing arm spacing from 100 μm to 5 μm, the power requirement increases by a factor of 4.5× to a total of 450 mW.

In conclusion, reducing arm spacing improves switching speed significantly, but at the expense of power consumption.

### *4.3.2. Heater position offset*

Given that the temperature gradient plays a major role in switching speed and power consumption, an experiment is designed to investigate the thermal gradient effect by varying the position of the heat source (or heater) with respect to the two MZI arms. The position of the heater is gradually displaced from directly on top of the heated arm to the middle of both arms. In our design, this displacement is chosen to be at 0, 1, 2, 3 or 4 μm offset from the top of the heated arm, in a 10 μm-spaced MZI. The schematic of their layouts is shown in Fig. 4.19. The conventional design is the layout with 0 μm offset, where the heater is placed right on top of the ridge waveguide, therefore the distance from the reference arm to the center of the heater is the furthest. By shifting the heater towards the middle, the distance between the reference arm and the heater is reduced, therefore the thermal gradient and heat flow pattern is altered.

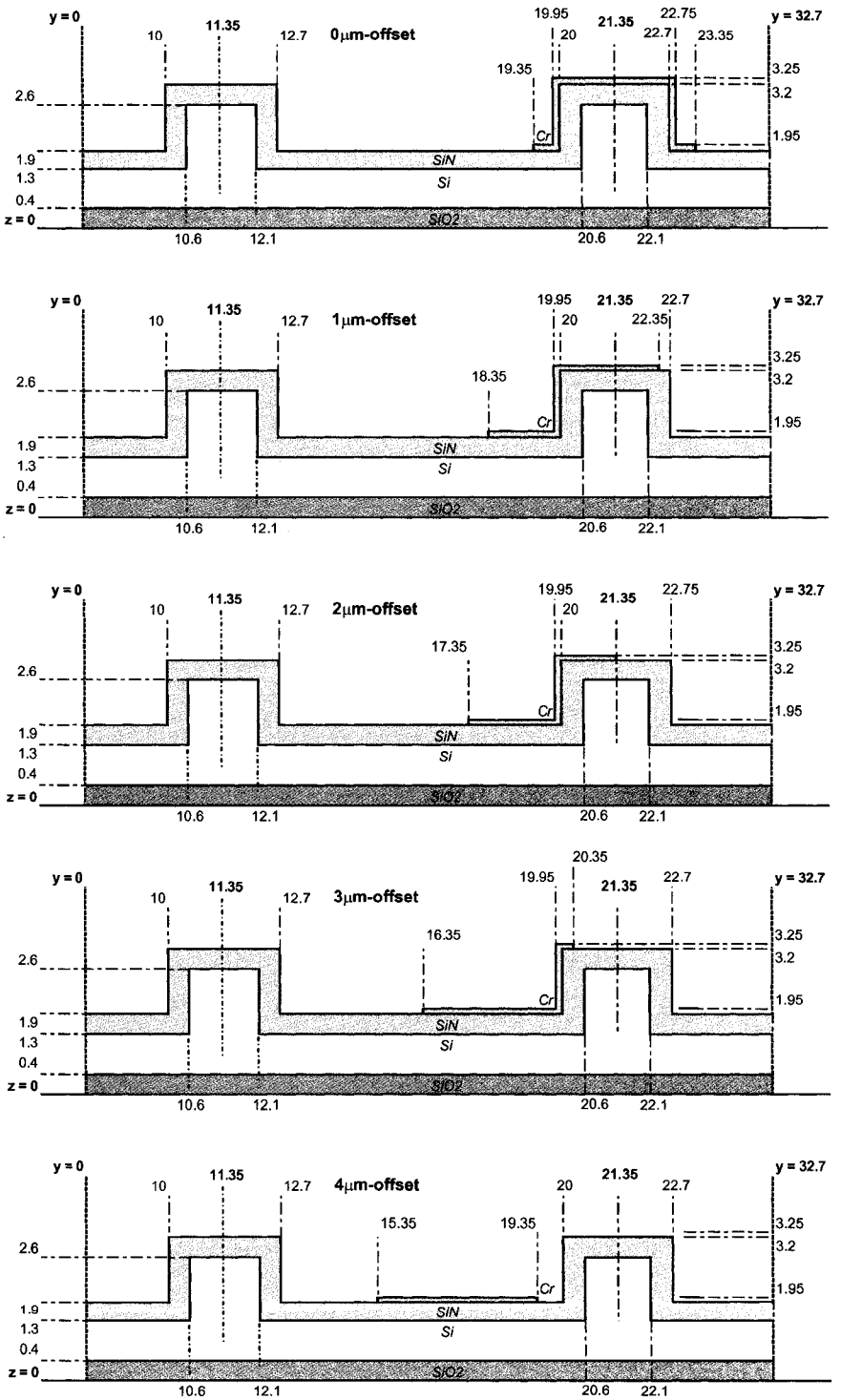



Fig. 4.19. Schematic layouts of 10 μm-spaced MZI switches with the heater offset of 0, 1, 2, 3 and 4 μm.

Fig. 4.20 shows the temperature contours of various 10 μm-spaced MZIs with a heater offset of 0, 1, 2, 3, 4 and 5 μm, after heating up for 20 μs. A gradual left-shift in the peak temperature is clearly observed, together with an increase in the temperature of the reference waveguide core. 5 μm offset is included in the simulation only to verify the accuracy of the heat flow.

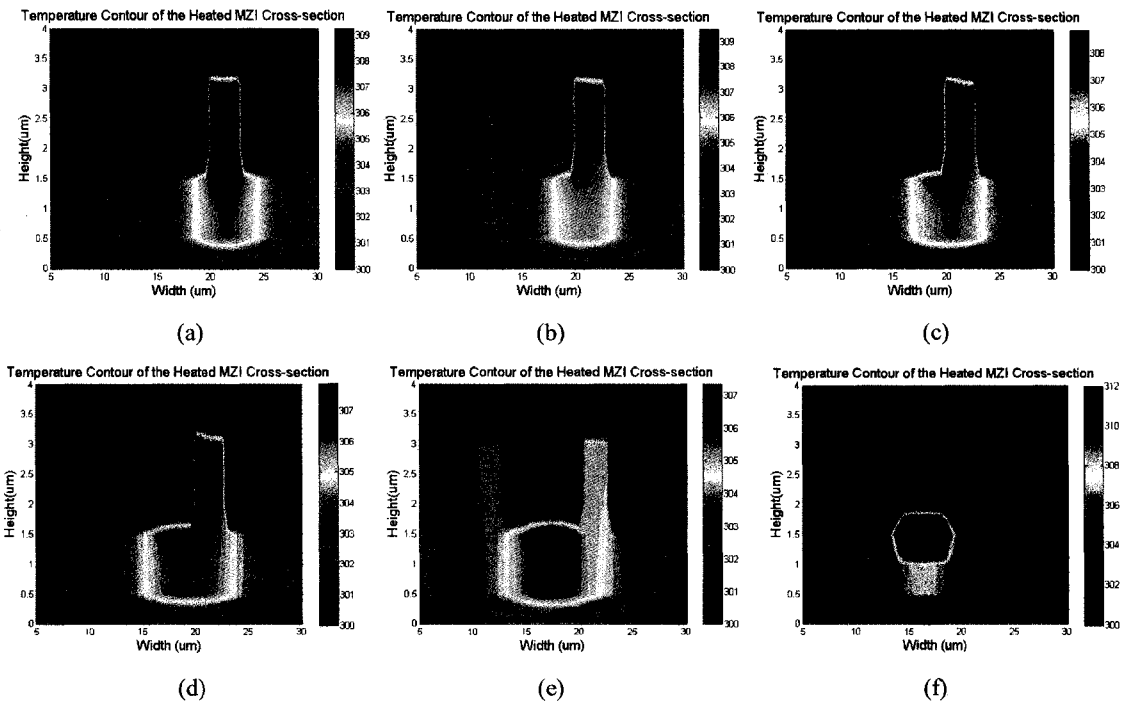



Fig. 4.20. Temperature contour of MZI switches with a heater position of (a) 0 μm, (b) 1 μm, (c) 2 μm, (d) 3 μm, (e) 4 μm and (f) 5 μm offset, after heating for 20 μs.

The rise time of these switches is plotted in Fig. 4.21. Almost no improvement in the rise time is observed when the heater is gradually displaced towards the middle of the two arms.

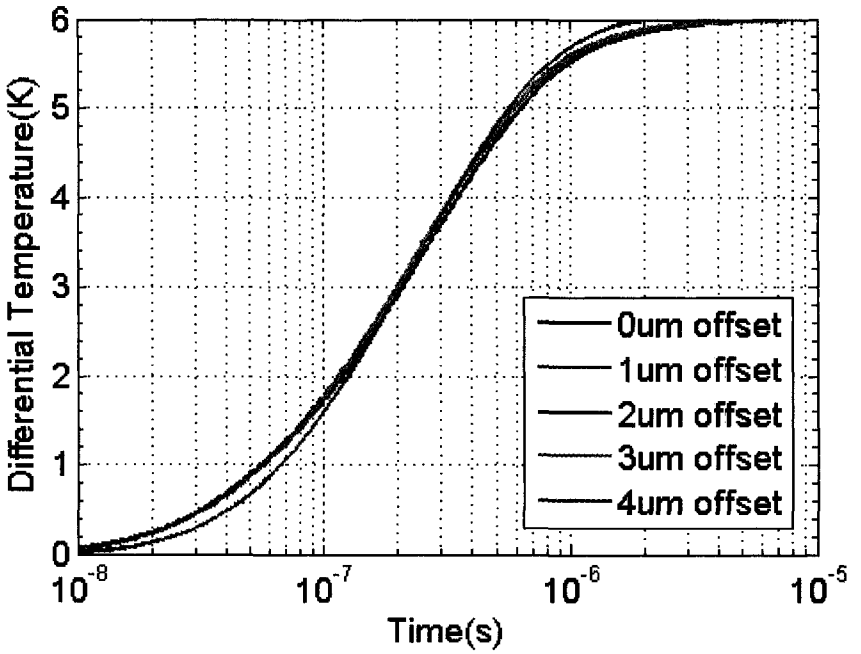



Fig. 4.21. The differential temperature versus time for MZI switches with different heater offset of 0, 1, 2, 3 and 4 μm.

However, a considerable increase in power consumption is observed when the heater position is shifted toward the middle of the arms, as shown in Fig. 4.22.

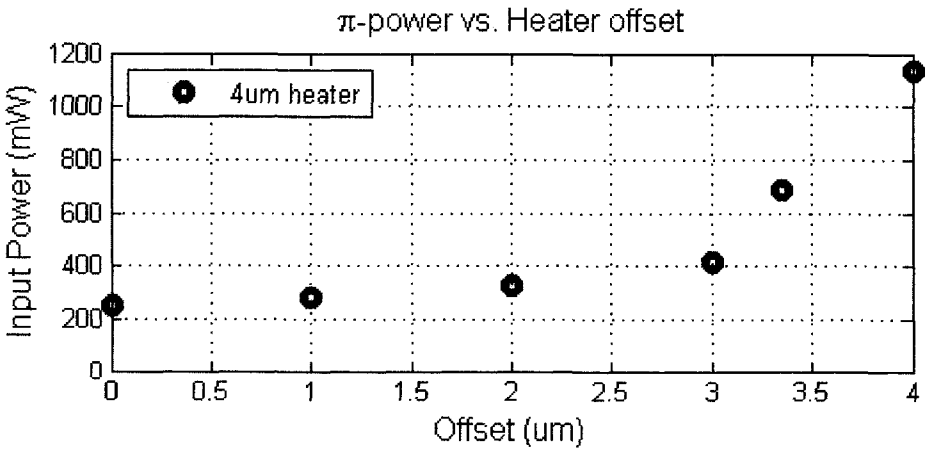



Fig. 4.22. The π-phase shift power of MZI switches with different heater offset.

When the heater is placed directly on top of one arm, the heat distribution is localized in the heated arm, therefore the temperature difference between the two arms rises significantly. When the heater is shifted toward the middle of the two arms, the heat is divided to both arms rather than localizing at the heated arm, resulting in a drop in the temperature difference between the two arms. As a result, more power is required to achieve the same temperature difference when the heater is displaced toward the middle. A total of 1140 mW power is required to switch a MZI with a 4 μm heater offset compared to 250 mW (4.5× less) for a MZI with 0 μm offset, as shown in Fig. 4.22.

### *4.3.3. Heater width*

The effect of heater width on rise time is studied by simulating the temperature rise introduced by 4 μm (default), 1.5 μm and 0.5μm wide heaters, as shown in Fig. 4.23.

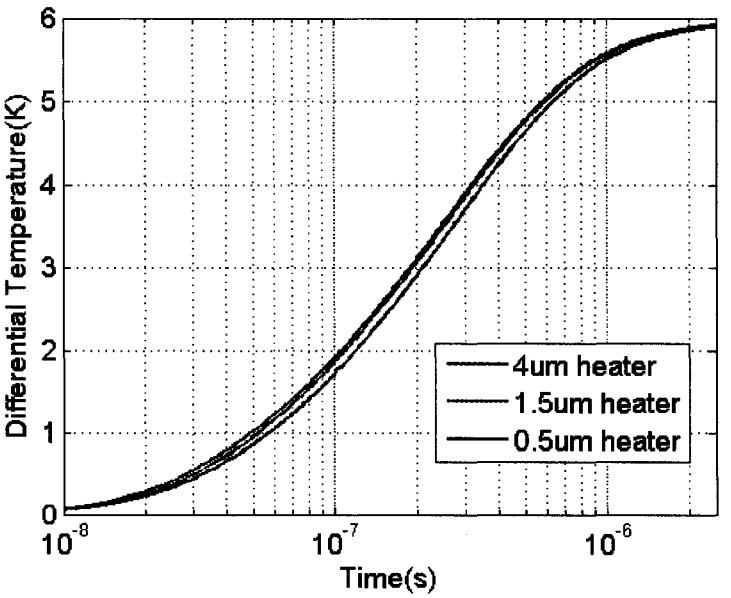



Fig. 4.23. The plot of differential temperature versus time for MZI switches with the heater width of 4, 1.5 and 0.5 μm.

There is a very small change in the rise time when the heater is reduced from 4μm to 1.5μm (the nominal width of our ridge waveguides). The small change is probably caused by the reduction in lateral heat diffusion in the SiN cladding layer, as the heater is no longer in contact with the ridge sidewalls and their adjacent slab regions. As a result, more heat is directed towards the underlying Si layer to heat up the entire ridge in shorter time, rather than dissipated through the SiN cladding, which has a thermal conductivity one order of magnitude lower than Si.

The effect of heater width on the power requirement is also small, as illustrated in Fig. 4.24.

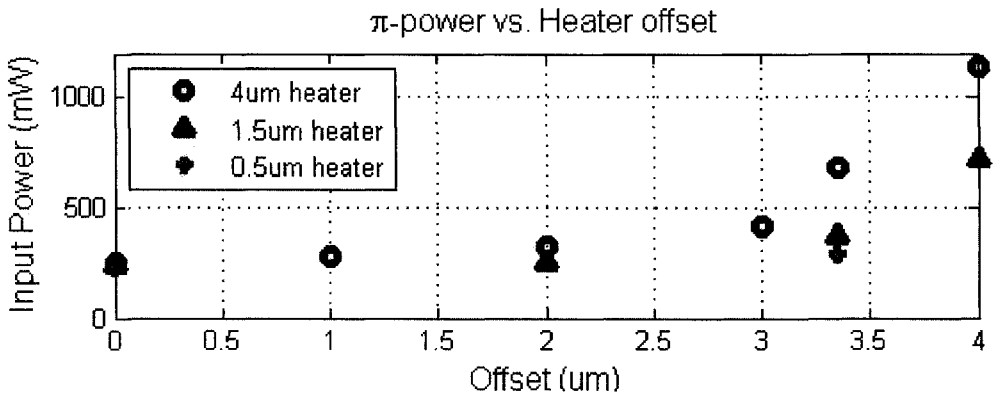



Fig. 4.24. The π-power of MZI switches with heater width of 4, 1.5 and 0.5 μm.

At the default heater offset of 0 μm, when the heater width is reduced from 4 μm to 1.5 μm, the required power for $\pi$–phase shift drops only mildly from 255 mW to 239 mW. Power saving with reducing heater width becomes more prominent in the MZI switches where the differential temperature between two arms is smaller. Reduction in heater width in this case results in higher power density (per unit area at a given input

power), which translates into higher amount of generated heat and heating efficiency. This explains an obvious 1.5× reduction in power by decreasing the heater width from 4 μm to 1.5 μm for a MZI switch design that has a heater offset of 4 μm, as shown in Fig. 4.24.

### *4.3.4. Cladding material*

Existing SOI MZI thermo-optic switches use $SiO_2$ as the upper cladding layer. However, the higher thermal conductivity and lower specific heat of SiN make it a superior cladding material than $SiO_2$ for high speed thermo-optic switching. Therefore, all simulation models discussed so far are based on SiN upper cladding layer. To illustrate the effect of using SiN cladding on switching speed improvement, similar SOI MZI switches with a $SiO_2$ upper cladding layer are simulated. The comparison in simulated rise time of the switches employing these two different cladding materials is shown in Fig. 4.25. The solid lines in the graph represent the rise time of switches with SiN cladding, while the dash lines represent $SiO_2$ cladding. Given identical arm spacing, heater width and cladding thickness, a thermo-optic MZI switch with SiN cladding is at least 3× faster than a conventional switch with $SiO_2$ cladding.

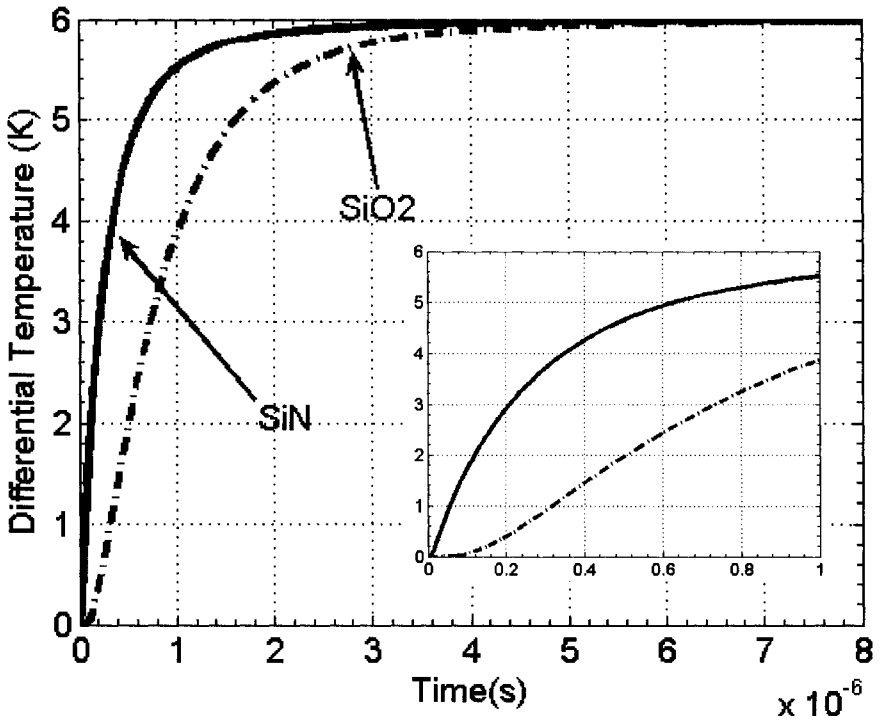



Fig. 4.25. The plot of differential temperature versus time for MZI switches consisting of SiN and $SiO_2$ cladding layers.

One important observation is the initial delay in the rise time of the switches with $SiO_2$ cladding as opposed to the sharp rise in the switches with SiN cladding, as illustrated in the inset in Fig. 4.25. This delay is related to the ability of $SiO_2$ cladding to store thermal energy compared to SiN. As mentioned in Section *4.2.2*, the ability of $SiO_2$ to store energy can be quantified by the product of two intrinsic material properties, density $\rho$ and heat capacity $c$. As illustrated in Table 4.1, while the density of $SiO_2$ is comparable to SiN, the specific heat of $SiO_2$ (740 J/kg·k) is approximately 4× of the specific heat of SiN (170 J/kg·k). Therefore, compared to SiN cladding under the same input power, a delay in the temperature rise is observed in the $SiO_2$ cladding due to heat

storage. Another important note is the effect of thermal diffusivity. As illustrated in the inset in Fig. 4.25, even after the initial delay, the slope $\partial T/\partial t$ of the SiN curve is steeper than the $SiO_2$ curve, indicating temperature rises much more rapidly in SiN than in $SiO_2$. This increase in the steepness of the slope is accounted by the higher thermal diffusivity $\alpha$ of the SiN compared to $SiO_2$ as mentioned in Section *4.2.2*.

Nevertheless, more heat is dissipated laterally in SiN cladding because of the higher thermal conductivity, and higher power is required to achieve the same temperature than when an $SiO_2$ cladding is used. For example, $P_\pi$ of a 10 μm-spaced MZI switch with SiN cladding is 255 mW compared to 225 mW for a similar switch with $SiO_2$ cladding. This result is in good correlation with Equation (4.22), which predicts the tradeoff relation between switching speed and power requirement when changing parameters such as specific heat, density and thermo-optic coefficient.

### *4.3.5. Cladding thickness*

The thickness of the cladding layer, in this case, a PECVD SiN film, also influences the heat conduction dynamics. To study the effect of this thickness, thermal models of 10 μm-spaced MZI switches with cladding thickness of 0.6, 0.4 and 0.1 μm were built in ATAR. All models consist of a 4 μm wide heater located symmetrically across the waveguide ridge of the heated MZI arm.

The simulated rise time of these switches is summarized in Fig. 4.26. In the range of our investigation, there is virtually no difference in the rise time of the switches as the SiN cladding thickness is reduced. A subtle difference, however, exists at the early stage

of the heating. Thinner cladding permits faster heat conduction from the heater to the ridge waveguide at this initial stage, as depicted by the solid lines of the inset in Fig. 4.26. Subsequent spreading of heat from the waveguide to its surroundings is dominated by transport through the Si and buried oxide, so there is no change in overall switching time. The effect of cladding thickness will become more prominent when it reaches the same order as the waveguide core layer thickness, because at that dimension, the rise time is affected equally by the heat flow within waveguide core layer and across the upper cladding from the heater on top. This aspect of study will be addressed in the next chapter when we discuss the effect of device scaling on the switching speed and power.

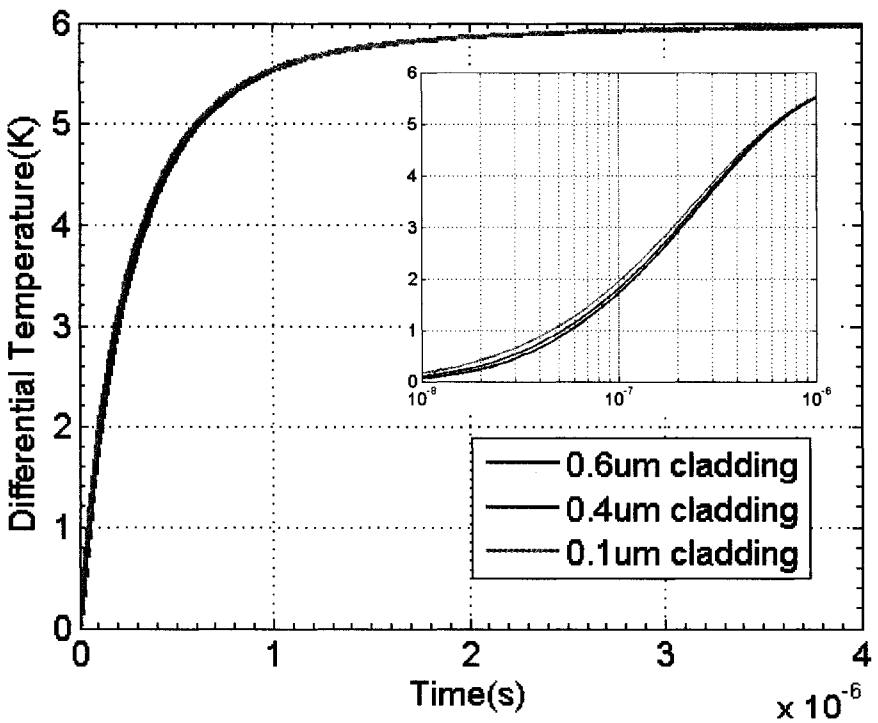



Fig. 4.26. The plot of differential temperature versus time for MZI switches with cladding thickness of 0.6, 0.4 and 0.1 μm.

Reducing cladding thickness has an effect on the power consumption. The change in $\pi$–phase shift power for 10 μm-spaced MZI switches with SiN cladding thickness of 0.6, 0.4 and 0.1 μm is 255, 248 and 180 mW, respectively. In other words, reducing the SiN cladding thickness from 0.6 μm to 0.1 μm results in approximately a 30% saving in the $\pi$–phase shift power. This power saving is attributed to the reduction in heat loss through the transverse heat conduction path from the heater to the waveguide core as the cladding thickness is reduced. Conversely, power consumption can also be reduced by increasing the thickness of the lower cladding (buried oxide). The reason for the power saving in this case is heat insulation instead of heat conduction. As mentioned in section *4.2.2*, heat is trapped within the Si waveguide core layer since the thick lower cladding BOX layer has a much lower thermal conductivity.

### *4.3.6. Conclusion of the effects of various parameters*

The following short statements summarize the effects of the various parameters studied in this section:

(i) Reducing the MZI arm spacing increases the speed significantly with a tradeoff in power

(ii) Reducing the heater width has little effect on speed but results in power saving for MZIs with the heater displaced towards the middle of two arms.

(iii) Substituting the $SiO_2$ cladding with SiN cladding increases the switching speed markedly (by a factor of 3×), with little power tradeoff

(iv) Reducing the upper cladding layer thickness has little effect on speed gain, but

allows power saving

These conclusions give the designer important guidelines on how to optimize the performance of SOI MZI thermo-optic switches. For instance, in an application where switching speed is the most critical factor while power is relatively less important, the design options to achieve high speed are to use SiN cladding and to decrease the arm spacing. On the other hand, in the application where low power and moderate speed is desired, the design options are to reduce the upper cladding thickness, increase buried oxide thickness, reduce the heater width and increase MZI arm spacing.

## 4.4. FABRICATION PROCESS AND TEST RESULTS

The schematic of the fabrication process for our thermo-optic switches is shown in Fig. 4.27. A *p*-type SOI wafer with a 0.4 μm-thick BOX layer and a 2.2 μm-thick Si overlayer was used as a substrate. Ridge waveguides with the design described in Section *4.2* were patterned by contact lithography on the SOI wafer using an SPR510 photoresist, and etched in an ICP chamber containing $SF_6$:$C_4F_8$ plasma. The etch depth was chosen to be 1.3 μm to obtain single mode. An upper cladding layer of 0.6 μm SiN was deposited on top of the etched waveguides by using PECVD.

The subsequent step was to form the heaters using a lift-off process. A bilayer resist consisting of a 1.3 μm LOR10A layer and a 1.3 μm SPR1813 layer, was spun coated over the SiN cladding. A short oxygen ashing treatment and a vapor prime step were introduced prior to the photoresist coating to render the SiN surface relatively hydrophilic for a better adhesion. The LOR10A resist was used primarily for a clean lift-

off while the SPR1813 layer was used as the imaging layer. Upon exposure to *uv* light, the inverted images of the heaters were stored in the imaging layer. During the photoresist development in *n-methyl pyrrolidone* (NMP) developer, the inverted images remained attached to the wafer while other areas dissolved away. A 50 nm thin Cr layer was subsequently evaporated by e-beam onto the wafer. The wafer was then treated by a lift-off treatment in the *LDD26* solution to create the heaters, as shown in Fig. 4.27.

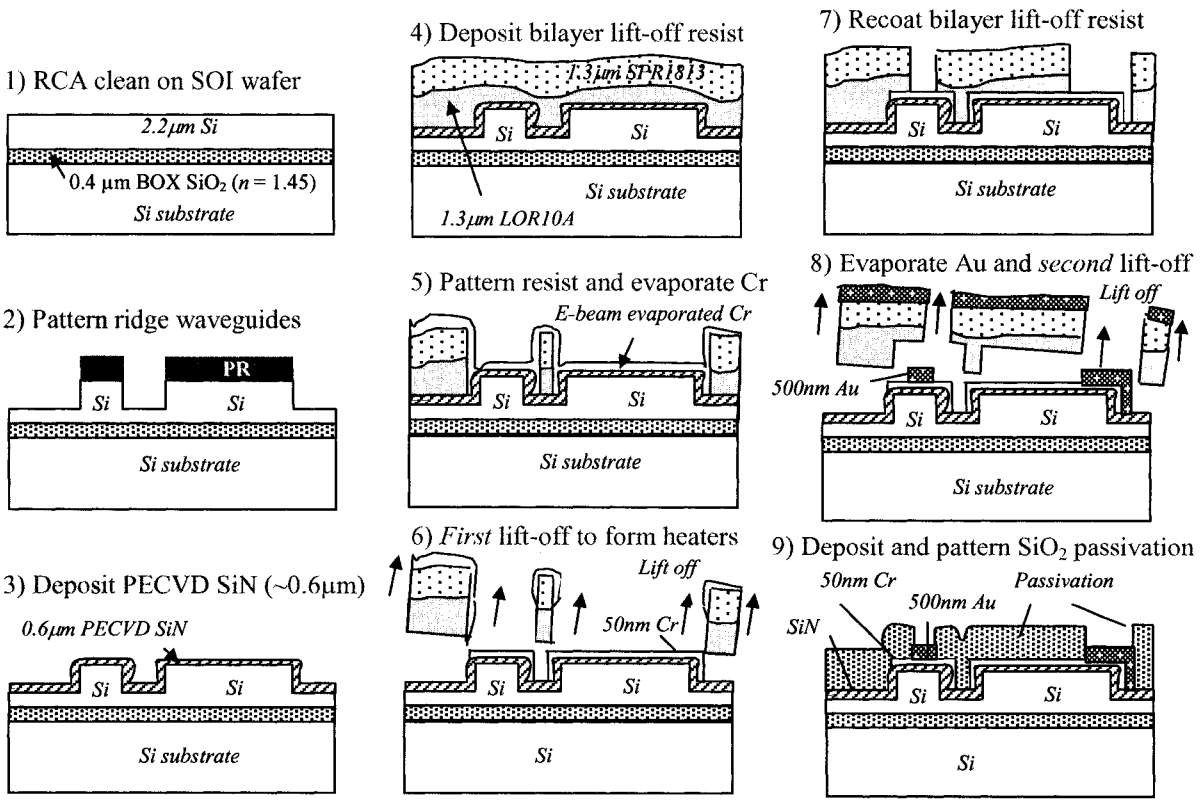



Fig. 4.27. Schematic of the fabrication process of our SOI MZI thermo-optic switches.

After the creation of heaters, another identical stack of bilayer resist was again coated onto the wafer to pattern the electrode layer. A 500 nm layer of Au was

evaporated by the same e-beam technique onto the wafer after the resist development. The second lift-off step was carried out to define the electrodes. The final process was to deposit and pattern a thick $SiO_2$ passivation layer over the electrodes for mechanical protection.

Fig. 4.28 shows a block of fabricated thermo-optic switches with the Cr heaters and Au electrodes.

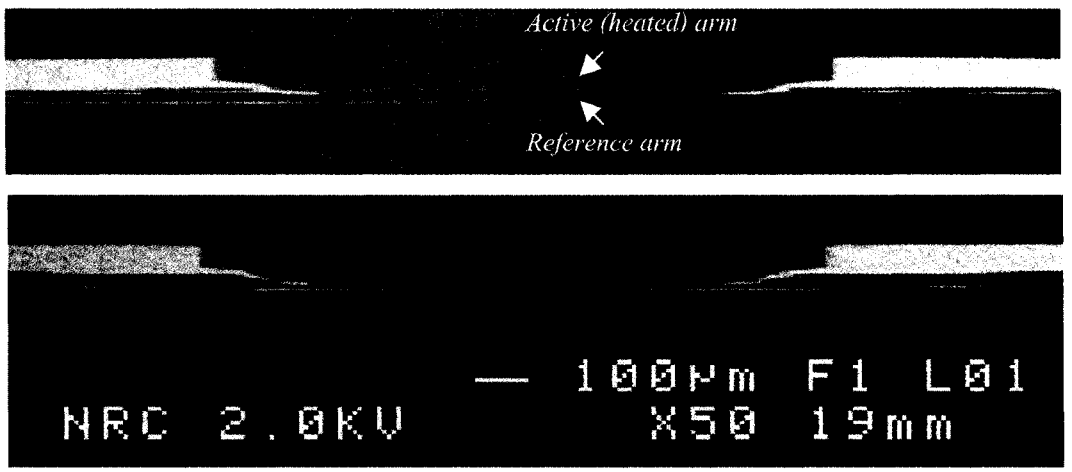



Fig. 4.28. SEM images of the fabricated 1×1 SOI MZI switches with Au electrodes and Cr heaters, showing the Cr heater is located (a) on top of the active arm, and (b) 4 μm away from the active arm.

The switches in this block have common MZI arm spacing of 10 μm. From the top image (Fig. 4.28(a)) to the bottom image (Fig. 4.28(b)), the heater position is displaced from the top of the active (heated) arm toward the middle of both arms. The fabrication tolerance of theses switches was assessed by inspection under a scanning electron microscope. As shown in Fig. 4.29(a), (b) and (c), the design gap of our y-branch was 1μm but the actual gap of the fabricated y-branch was 1.3 μm. The design width of

the nominal waveguide was 1.5 μm while the actual width of the etched waveguides was around 1.15 μm. This 23% shrinkage in width, from the mask layout to fabrication, accounts for the observed larger gap at the y-branch.

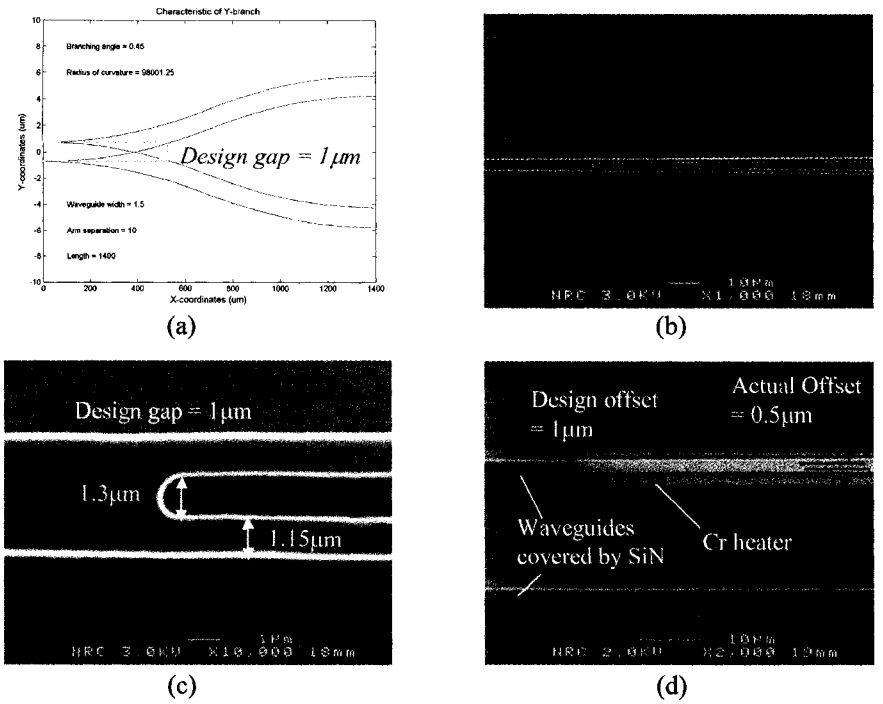



Fig. 4.29. (a) Mask layout of a y-branch in one of the MZI switches. (b) The fabricated y-branch inspected by SEM. (c) The actual gap of the fabricated y-branch inspected under high magnification SEM. (d) The fabricated Cr heater on top of an SOI waveguide.

A larger gap is undesired because of a higher loss associated with radiation and reflection resulted from power splitting at the y-branch. This eventually translates into a higher insertion loss and a decrease in extinction ratio. Also, in the vertical scale, cross-sectional SEM inspection revealed that the ridge waveguides were slightly over-etched to 1.5 μm instead of the designed height of 1.3 μm. The over-etched samples would probably experience a multimode effect but the insertion loss was expected to be lower.

Fig 4.29(d) shows a Cr heater fabricated with the lift-off process covering an SOI waveguide in one of the 10 μm-spaced MZI switches. There is an alignment offset of approximately 0.5 μm from the center of the heater to the center of the waveguide. This offset is common in the contact aligner where the alignment tolerance is around ±1 μm. However, this inevitable alignment offset due to equipment, material and operator's limitation could mislead the experimental results of the study on the effect of heater position offset on the switching speed and power consumption, which is very sensitive to the variation in alignment within the order of submicron. To provide such alignment accuracy, e-beam lithography or a high-precision deep *uv* stepper is required.

The fabricated SOI thermo-optic switches were tested using a combined optical and electrical test setup. First, the switches were tested in a "DC" mode to examine the π–phase shift power. In this DC test, an optical measurement setup similar to Fig. 2.7 was used to align the waveguides to the input fibers and output focusing optics. Once the TE-polarized light was coupled into the waveguides and transmitted to the output facet to be detected successfully by the photodetector, a dc voltage was applied across the two Au electrodes that connected the Cr heater. The current that flowed through the close loop would heat up the Cr heater and introduce a phase shift. This voltage was swept from -50 V to 50 V linearly with a 0.2 V interval to introduce a nonlinear phase shift. This phase shift would attenuate the output optical signal of the 1×1 MZI switches or modulators, and produce a periodic response curve, as indicated by Equation (4.7). By measuring the current flowing through the heater, the electrical input power could be calculated and

plotted against the detected optical output power, as shown in Fig. 4.30.

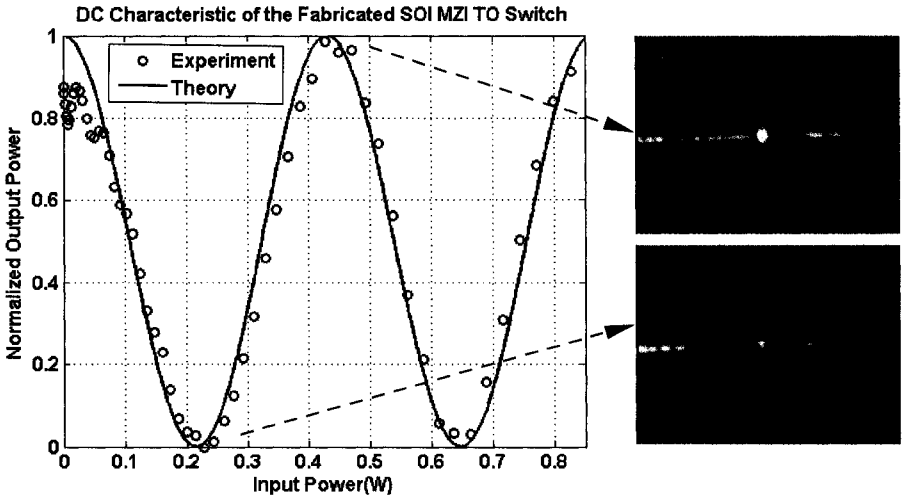



Fig. 4.30. DC response curve of a 20 μm-spaced SOI MZI thermo-optic switch illustrating the change in detected optical output power (normalized) as a result of phase shift introduced by the applied electrical power.

In Fig. 4.30, the data points are the measured optical output power when different electrical power is applied on a 20 μm-spaced MZI thermo-optic switch. The measured optical output power is normalized by dividing with the peak output power, which is detected at the 'off' stage without any applied heat or electrical power. When the splitting of power is even, the detected output intensity of the mode guided in the output waveguide is at maximum. This is illustrated by the bright spot in the top right IR image shown in Fig. 4.30. When a $\pi$–phase shift is introduced to the heated MZI arm by flowing current through the heater, the resultant recombined power in the output waveguide drops to minimum, as shown in the bottom right IR image. As expected, when the phase shift introduced by the applied electrical power falls between the multiples of $\pi$ and $2\pi$, the

output power fluctuates between its minimum and maximum value.

The solid curve in Fig. 4.30 is a theoretical fit to the measured data. The output power of this theoretical curve, $P_{out}$, is derived from Equation (4.7) by assuming even power splitting at the Y-splitter ($I_1 = I_2 = 0.5P_{in}$):

$$P_{out} = \left(\frac{\sqrt{I_1}}{\sqrt{2}}\right)^2 + \left(\frac{\sqrt{I_2}}{\sqrt{2}}\right)^2 + 2\left(\frac{\sqrt{I_1 I_2}}{2}\right)\cos(\Delta\phi)$$

$$= 0.5(1 + \cos(\Delta\phi))P_{in} \qquad (4.22)$$

where $\Delta\phi$ is the resultant phase shift. The measured data can be fitted very well with the theory, indicating the validity of our DC measurement.

As mentioned in Section *4.2.2*, to maximize the extinction ratio of a MZI switch (the ratio between the maximum and minimum detected power), the power split between the two arms has to be as even as possible. Due to fabrication variation, the Y-splitters and arms of MZI switches are rarely perfectly symmetrical. Therefore the power splitting between arms is not even, and the extinction ratio is not 100%. Small arm length differences can cause an initial phase shift to the output power even in the absence of applied electrical current. Also, the insertion loss of our fabricated devices is relatively high. The average insertion loss of our fabricated 10 and 20 μm-spaced MZI switches is around -22 dB. The insertion loss of straight waveguides, with or without heater, is around -12 dB, including the reflection loss from the two facets, coupling loss from modal mismatch and scattering loss from the sidewalls. The excess -10 dB loss in the MZI devices is attributed mainly to radiation loss at the junctions and the *S*-curves of the

two Y-splitters. The best extinction ratio achieved is approximately 8 dB. The extinction ratio can be improved by a better process control and the implementation of selective process improvement schemes, such as those proposed in the previous chapters.

In order to confirm the thermal gradient effect observed from our simulation, we have measured the DC characteristics of a set of 10 μm-spaced MZI switches with a heat offset of 0, 1, 2, 3 and 4 μm, and another set of 20 μm-spaced MZI switches with an offset of 0, 1, 2, 3, 4, 5, 6, 7, 8 and 9 μm. Again, the power plots of some of these measured switches are shown in Fig. 4.31.

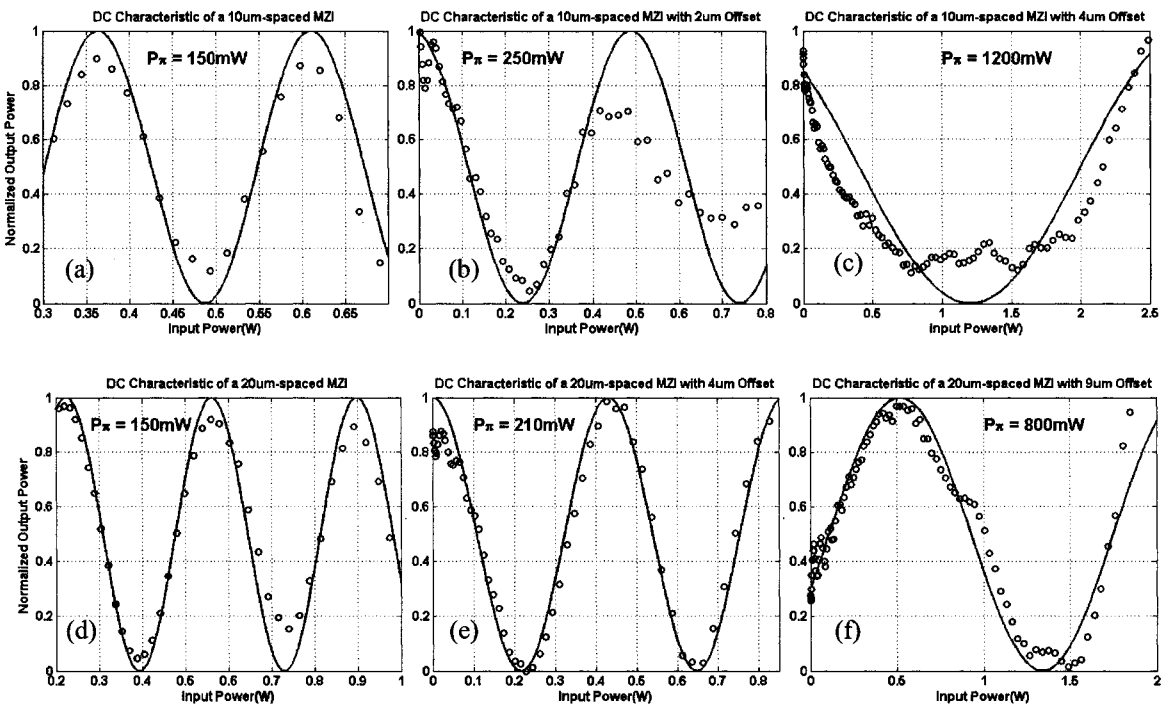



Fig. 4.31. Input-output power characteristics of the fabricated MZI thermo-optic switches with a 10 μm arm spacing and a (a) 0 μm, (b) 2 μm, and (c) 4 μm heater offset. Same power characteristics of switches with a 20 μm arm spacing and a (d) 0 μm, (e) 4 μm, and (f) 9 μm heater offset.

Fig. 4.31 (a), (b) and (c) corresponds to the input-output power characteristic of 10 μm-spaced MZI switches with a heater offset of 0, 2 and 4 μm, respectively. In all three switches, periodic fringes of output power are observed over the entire range of the input power, spanning over from 0 to 2.5 W. The half-period (peak-to-valley distance) of any fringes represents a π–phase shift power of that particular switch. In Fig. 4.31 (b), there is a secondary beating in the background of the fringes, which results from multimode interference. The multimode effect is an unfortunate consequence of the overetching of the measured switches to 1.5 μm instead of 1.3 μm. Nonetheless, the multimode interference should not affect the measured π–phase shift power because the response of MZI depends only on the change in effective index with temperature $dN_{eff}/dT$, which does not change much for different modes in large waveguides.

In order to measure the π–phase shift power, the horizontal axes of all three plots are set in the range that best reveal the corresponding half-periods. Using these half-periods, the π–phase shift power of the switches with a heater offset of 0, 2 and 4 μm is determined to be approximately 150, 250 and 1200 mW, respectively. The observed trend of increased in power is in excellent agreement with the simulated power shown in Fig. 4.22, except the measured power for the switch with 0 μm offset is slightly lower than its simulated value. The same trend of the increase in the π–phase shift power of switches having 20 μm arm spacing with a heater position offset of 0, 4 and 9 μm is also observed from the measurement, as demonstrated in Fig. 4.31 (d), (e) and (f). These switches have significantly less multimode interference and are showing identical trend in power

consumption in response to the thermal gradient effect. Therefore this measurement result is a solid evidence of the good agreement between experiment and simulation.

Pulse response experiments were performed on the switches to examine their rise time. The optical test setup used for the DC test was shared by the pulsed measurementt, but pulse generators were used to introduce square pulses from Hz to MHz frequencies. The test setup is capable of measuring nanosecond rise time. The rise time of any switch was calculated from the minimum to the maximum output power after complete switching had been accomplished. A typical pulse response plot of the measured switches is shown in Fig. 4.32. The input square pulse has a period of 4 ms and a holding time of 2 ms (50% duty cycle). The rise time of this 20 μm-spaced MZI switch is approximately 1.8 ms, which is significantly slower than the 6 μs rise time calculated from the simulation. The best result of our pulsed measurements on a 10 μm-spaced MZI gives a rise time of around 400 μs.

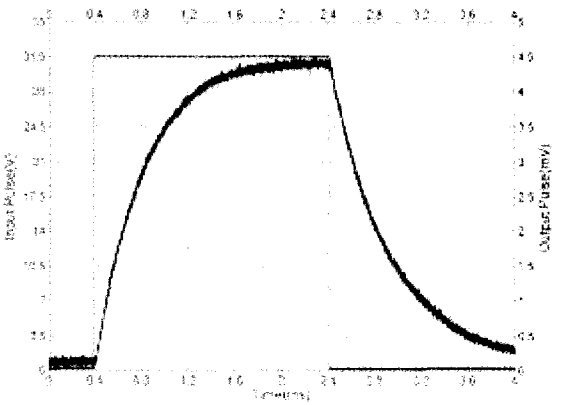


Fig. 4.32. Measured rise time of a 20 μm-spaced MZI thermo-optic switch with a 0.25 kHz square input pulse.

In the DC test, the Cr heater resistance was calculated to be in between 3 kΩ to 5 kΩ. A further *I-V* measurement on the Van Der Pauw's structures on the same chip confirmed that the sheet resistance was about 17.7 Ω/□, corresponding to approximately 4 kΩ for a heater strip of 200□ (length of 800 μm and width of 4 μm). This measured resistance is one order of magnitude larger than the theoretical resistance of a 50 nm Cr film (electrical resistivity of 12.9 μΩcm or sheet resistance of 2.58 Ω/□). It is believed that this large resistance increases the RC delay of the heater and manifests itself into a slow heating response (rise time of the thermo-optic switches). The origin for this large resistance could have several possibilities, one of which is the residual bilayer photoresist remain in between the Cr heater and Au electrodes during the two successive lift-off processes. Another possible cause of high resistance is the oxidization of Cr metal strip after long exposure in air. The evidence of Cr oxide is a significant drop in measured sheet resistance on the Cr pads using four-point probe and on Van Der Pauw's structures at a probe station after recurring testing. Scratching by the probe needles and repeated passing of current through the Cr pads gradually breaks down the Cr oxide and eventually brings the resistance down from 5 kΩ to 3.5 kΩ. To verify the effect of large heater resistance on the RC delay of the pulse response, an additional 100 nm of Pt layer was selectively deposited using focus ion beam (FIB) on top of the Cr heater to top up the metal thickness and reduce the overall electrical resistance. The resultant resistance was reduced to 500 Ω and the measured rise time dropped from 400 to 200 μs. This result

indicates that the experimental rise time can be further reduced to tens of micro-seconds, if the resistance can be further reduced to 50 Ω by depositing Cr/Au bilayer metal and optimizing the fabrication process.

## 4.5. CONCLUSION

In this chapter, a design and optimization package of an SOI 1×1 y-branch MZI thermo-optic switch has been presented. As part of the optimization package, a detailed simulation study on the effects of various switch parameters on the switching speed and power, using a finite-difference thermal simulator, has also been provided. The simulated rise time of our designed switches is in the order of 1 μs, which is in good accordance with the experimental rise time of many recently published reports studying this type of SOI switch. Our switches were fabricated using a double lift-off process and were tested for both power consumption and rise time. The measured power consumption agrees very well with the simulation, but the measured rise time is about two orders of magnitude longer than the simulated rise time. The cause of this discrepancy between simulation and experiment is likely associated with the RC delay resulted from the high series resistance of the heater. Photoresist residue remains in between Au electrode and Cr heater, as well as oxidation of Cr are believed to have increased the contact resistance and responsible for the increase in RC delay. Nevertheless, the agreement in the experimental and theoretical power consumption validates our simulation procedures.

# CHAPTER 5

# THERMO-OPTIC MODULATION II: DEVICE SCALING

The basic building block of the SOI thermo-optic switches discussed in the previous chapter takes the form of ridge waveguides with a nominal width of 1.5 μm. Ridge waveguide of this dimension cannot be bent to a small curvature because the bending loss surges drastically when the bending radius is reduced to less than several hundred micrometers [5.1]. This hinders the development of compact photonic chips with large-scale integration, since device size is limited by the minimum allowable radius of curvature [5.2]. To address this issue, compact photonic devices are often fabricated using SOI channel waveguides that consist of a Si core with extremely small cross-section. In some occasions, these channel waveguides with submicron core dimensions, also known as "photonic wire waveguides", have to be fabricated with accuracy in the range of 1-10 nm [5.2]. In recent years, many functional optical devices of compact size have been demonstrated in the literature using these Si photonic wire waveguides, such as channel-drop filters with small ring resonators [5.3-5.5], optical switches [5.6-5.7], directional couplers [5.8], array waveguide gratings [5.9], optical add-drop multiplexers (OADM) [5.10] and evanescent field biosensors [5.11] etc.

## 5.1. PROPERTIES OF SILICON PHOTONIC WIRE WAVEGUIDES

A Si photonic wire waveguide is basically a high index contrast channel waveguide consisting of a submicron Si core with a surrounding dielectric cladding material [5.1, 5.2]. With such tiny cross-section, the core of Si photonic wire waveguides can be approximated to a circular wire that resembles the structure of an optical fiber with a diameter equivalent to the channel waveguide width. Following this approximation, wave guiding properties and single-mode condition of these photonic wire waveguides can be solved using mathematical models established for conventional optical fibers. Based on Maxwell's equations, the eigen-value solution can be expressed in Bessel functions and the single mode condition of the photonic wire waveguide is given by the following equation [5.12]:

$$2\pi \cdot \frac{a}{\lambda}\sqrt{n_{core}^{\ 2} - n_{clad}^{\ 2}} \leq 2.405 \qquad (5.1)$$

where $a$ is the wire radius, $\lambda$ is the operating wavelength, $n_{core}$ is the refractive index of the core, and $n_{clad}$ is the refractive index of the cladding. For example, the diameter or width ($2a$) of a Si square photonic wire waveguide with a $SiO_2$ cladding should be less than 375 nm, in order to be operating in single mode at the wavelength of 1.55 μm. Alternatively, if the $SiO_2$ cladding ($n_{clad}$ = 1.44409) is replaced by SiN ($n_{clad}$ = 1.91), the maximum waveguide width for single mode operation can be increased to 408 nm.

In the literature, Si photonic wire waveguides are normally made as small as 300 × 300 $nm^2$ to achieve single mode operation [5.1, 5.8, 5.10]. Apart from square channel

waveguides, rectangular SOI photonic wire waveguides can also be used to construct integrated optical components for telecommunication [5.2] and sensor [5.11] applications. For instance, a widely used configuration of Si photonic wire waveguide reported by IMEC, LETI and NRC contains a thinner core of 220 nm and a width of 450 nm [5.2, 5.11]. The single mode condition for the rectangular waveguide differs from Equation (5.1) as the mode field in this case cannot be solved readily with analytic approach, but instead requires a more sophisticated semi-vectorial or full vectorial mode solver, such as FIMMWAVE [5.13]. The optical devices are usually designed to operate in either TE (electric field parallel to the substrate plane) [5.2] or TM (electric field perpendicular to the substrate plane) polarization only [5.11]. In this study, we have chosen to evaluate the performance of the SOI thermo-optic switches that are constructed with both $300 \times 300$ nm$^2$ and $220 \times 450$ nm$^2$ configurations.

The mode field profile of photonic wire waveguides is important in determining the performance of thermo-optic switches and modulators. Compared to micron-size ridge waveguides, photonic wire waveguides are less effective in confining light tightly within the core, especially when the core size becomes smaller than the effective wavelength ($\lambda/n$, $\lambda$: free space wavelength, $n$: refractive index of the medium) of the light propagating in the core. When light no longer remains tightly confined within the core, its evanescent field expands further into the cladding. Field expansion into the oxide cladding as the SOI waveguide shrinks from large dimension ridge waveguide to small size photonic wire waveguide is illustrated in Fig. 5.1 [5.14].

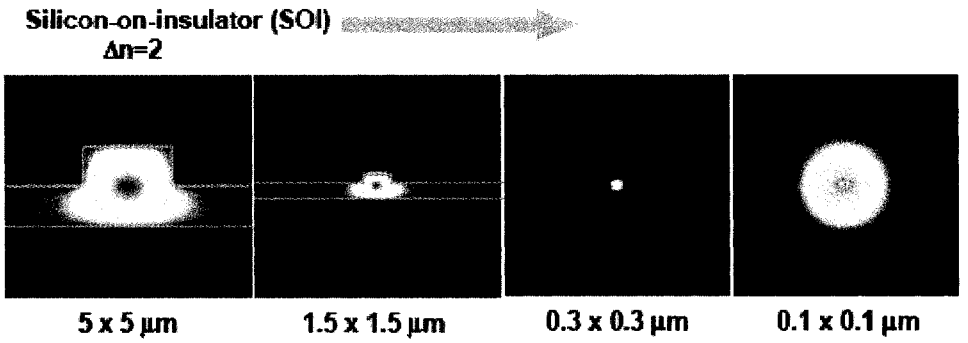



Fig. 5.1. Evolution of mode profile as the optical waveguide shrinks from large dimension ridge configuration to small size photonic wire configuration [5.14].

In Fig. 5.1, it is clear that the size of the optical mode field increases significantly when the core size of the photonic wire waveguide decreases to less than 0.3 μm. For an SOI thermo-optic switch or modulator made of photonic wire waveguides, its power consumption and response time are greatly affected by this mode expansion, as the field is redistributed across the core and claddings. The performance of the switch or modulator has essentially become dependent not only on the properties of the core, but also the cladding. Investigating and understanding the effect of device scaling and mode field distribution on the performance of SOI MZI thermo-optic switches of various dimensions is the main objective of this chapter. The following waveguide configurations have been chosen for this study:

(i) a *ridge* waveguide with a Si core layer thickness of *10 μm*, with a 5 μm width and an etch depth of 5 μm (aspect ratio of 1:1, etch ratio of 0.5:1). The waveguide is denoted hereafter as 10 μm ridge waveguide.

(ii) a *ridge* waveguide with a Si core layer thickness of *3 μm*, with a 1.5 μm

width and an etch depth of 1.5 μm (aspect ratio of 1:1, etch ratio of 0.5:1). The waveguide is denoted hereafter as 3 μm ridge waveguide.

(iii) a *ridge* waveguide with a Si core layer thickness of *1.5 μm*, with a 0.7 μm width and an etch depth of 0.7 μm (aspect ratio of 1:1, etch ratio of ~0.5:1). The waveguide is denoted hereafter as 1.5 μm ridge waveguide.

(iv) a *ridge* waveguide with a Si core layer thickness of *0.7 μm*, with a 0.3 μm width and an etch depth of 0.3 μm (aspect ratio of 1:1, etch ratio of ~0.5:1). The waveguide is denoted hereafter as 0.7 μm ridge waveguide.

(v) a *channel* waveguide with a Si core layer thickness of *0.3* μm and a 0.3 μm-width (aspect ratio of 1:1). This symmetrical photonic wire waveguide is denoted hereafter as 0.3 × 0.3 $\mu m^2$ channel waveguide.

(vi) a *channel* waveguide with a Si core layer thickness of *0.22* μm and a 0.45 μm width (aspect ratio of 1:2.045). This asymmetrical photonic wire waveguide is denoted hereafter as 0.22 × 0.45 $\mu m^2$ channel waveguide.

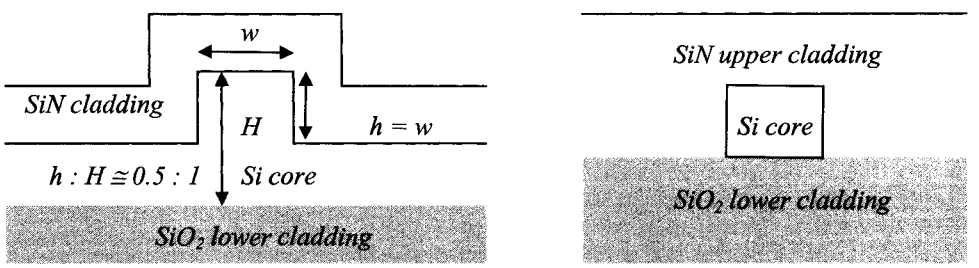



Fig. 5.2. Configuration of (a) ridge waveguide, and (b) channel waveguide designated to the study of device scaling.

As illustrated in Fig. 5.2, all ridge waveguides are composed of a SiN upper cladding, a Si core and a buried oxide layer as lower cladding, while all channel waveguides consist of a bottom oxide cladding layer and a Si core that is covered by SiN on all other sides. When the waveguide core layer thickness is scaled from 10 μm to 0.22 μm, the effect of mode expansion on the thermo-optic response of the MZI switches will become apparent.

## 5.2. OPTICAL SIMULATION AND MODE PROFILES

The first step of the study of device scaling is to simulate the mode field profile of both TE and TM polarization for all six waveguides mentioned above. There are two solutions in obtaining accurate mode field distribution for the waveguides using our optical simulation software FIMMWAVE [5.13], namely the "film-mode matching" (FMM) mode solver and the "finite-difference" mode (FDM) solver. The FMM solver models an arbitrary waveguide by a set of vertical slices, each uniform laterally, but composed vertically of a number of layers. For the case of a ridge waveguide, each slice is essentially a slab waveguide, with no refractive index variation in the lateral direction, as shown in Fig. 5.3. Because of this restriction, the arbitrary field profile of the waveguide can be acquired from a sufficient number of slab (1D) modes of all the slices. These slab modes are the modes corresponding to the assumption that the slices are infinitely wide.

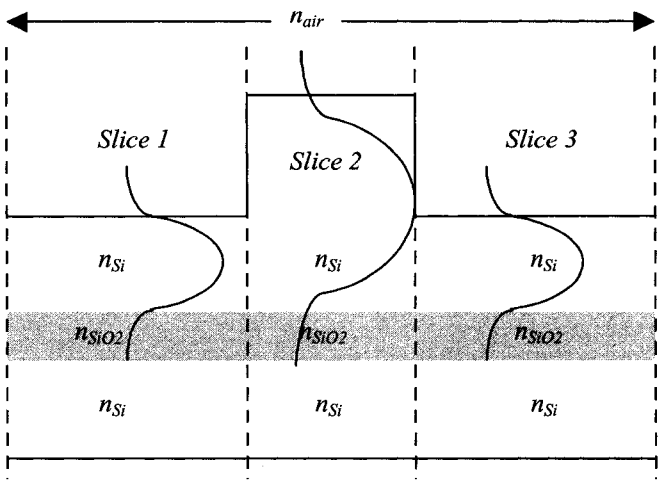



Fig. 5.3. Illustration of the film-mode-matching (FMM) solving method to obtain the mode field profile in a ridge waveguide. The slab (1D) modes of each slice are used to acquire the valid guided mode in the ridge.

From the slab modes of each slice, a vectorial solution of the guided "ridge mode" (2D mode) can be obtained by generating matrices of overlap integrals between the slab modes of the $n^{th}$ slice and $(n+1)^{th}$ slice. For example, as illustrated in Fig. 5.3, since there are three slices forming a complete ridge waveguide, the overlap integrals of *slice 1* and *slice 2*, as well as *slice 2* and *slice 3* are generated. The mode solver will then attempt to find a set of coefficients or propagation constants of the 1D slab modes in each slice that will give a field profile obeying Maxwell's equations everywhere including the boundaries of the slices. A solution based on any propagation constant can be matched across *slice 1*, *slice 2* and *slice 3*, using the overlap matrices. Any arbitrary propagation constant in *slice 1* usually will not produce a solution that can meet the boundary conditions in *slice 3*. Only unique propagation constant that produces meaningful overlap

integrals and satisfies boundary conditions at all interfaces will constitute a valid guided mode. By scanning propagation constant over a range of values, a set of valid solutions will eventually be found, which correspond to a set of valid guided modes. This method is powerful in extracting ridge waveguide modes with high accuracy and short computation time. For this reason, all optical modes of the ridge waveguides mentioned in previous chapters were obtained using FMM solver. However, when the ridge waveguide dimension becomes as large as 10 μm, each slice of the waveguide will contain a thick slab where a substantial number of 1D modes exist. In order to acquire the valid guided ridge mode, FMM solver will need to generate a large matrix of overlap integrals across all slices based on a considerable number of 1D modes. Depending on the size of the simulation window defining the geometry of the ridge waveguide, the computation task may be too intensive for the FMM solver to manage. This is certainly the case for our simulation, as the FMM solver could not generate any meaningful output for the 10 μm thick ridge waveguide.

An alternative method known as finite-difference method (FDM) solver is used to acquire the mode profile of all waveguides. This method approximates the solutions to the Maxwell's equations by replacing derivative expressions with approximately equivalent algebraic formulae [5.15, 5.16, 5.17]. In other words, FDM solver discretizes the electromagnetic differential equations by using algebraic formula to approximate the original derivatives with an infinitesimally small interval [5.15]. This is a numerical method seeking for numerical solutions to the differential equations within the simulation

boundaries over a set of points called "*nodes*". In solving the waveguide mode, the FDM solver places adequate number of nodes around the core and its interfaces with the cladding, while leaving other regions with sparsely-spaced nodes. This enables the collection of meaningful information on the solution of the mode. The process of placing the nodes in a given region is called "*grid generation*" and the placement of the nodes is known as "*grid density*".

### *5.2.1. Mode Field Simulation Settings*

The accuracy of the optical simulation result from FDM solver greatly depends on two factors, (i) the distance of the simulation boundary from the mode, or the size of the simulation window, and (ii) the grid density. If the window size is too small, the boundaries may interact with the solution and affect the accuracy of the results, such as the effective index and profile of the mode. For instance, the left and right boundaries in our optical simulation are set to the perfect electric wall condition where $E_{//} = 0$ (electric field component that is parallel to the wall is zero). This means that the electric field of the simulated mode will be reflected at the left and right boundaries, if these boundaries are sitting too close to the mode. This field reflection will increase the electric field at the boundary such that the simulated mode never decays to zero at the boundary. The accuracy of the simulated propagation constant or effective index of the mode will therefore be affected. The use of perfect electric wall boundary condition basically allows users to judge whether the boundaries are sufficiently distanced from the simulated modes.

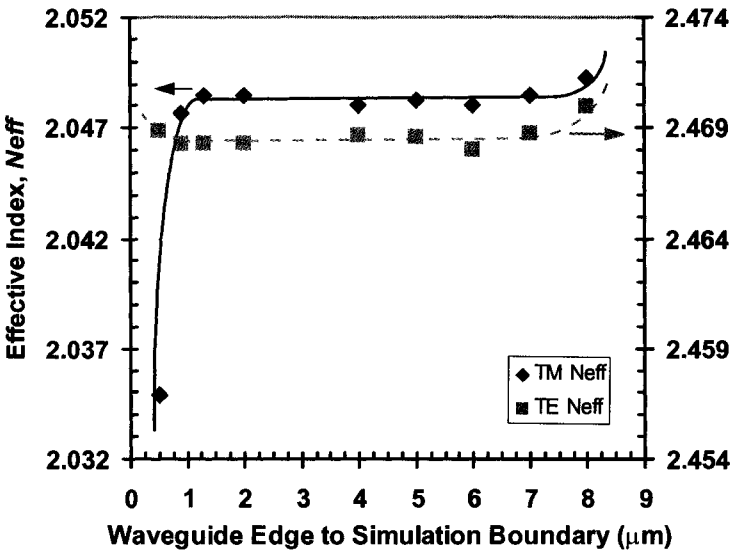



Fig. 5.4. Effective indices of fundamental TE and TM modes of a 0.22 × 0.45 $\mu m^2$ channel waveguide, determined at different simulation window size using finite-difference (FDM) mode solver.

Fig. 5.4 illustrates such an interaction for a channel waveguide of 0.22 × 0.45 $\mu m^2$, as the distance from the waveguide edge to the simulation boundary is reduced to less than 1 μm. The resultant effective index of TM mode falls off dramatically while the index of TE mode starts to increase. In the range of 1.2 to 6 μm, where the boundary is at a safe distance from the active mode, the effective indices of both TE and TM modes remain constant regardless of the change in the window size. This is a stable region where one can be confident with the accuracy of the effective index and mode profile as they do not vary with the window size. When the distance between the boundary and active mode is increased beyond 6 μm, the larger window size will translate into a lower density grid if the number of grid points remains unchanged. The drop in grid density

will result in a deterioration of spatial resolution, in that the calculated mode no longer reflects the true waveguide geometry. If the number of grid points is increased to maintain the same grid density, the number of points becomes too large and the computational time is too long. Selecting a suitable window size and grid density is thus critical for obtaining accurate simulation results. To confirm the accuracy of our simulation, plots similar to Fig. 5.4 were generated for all other waveguides and appropriate window sizes were chosen.

The accuracy of our simulation was verified by comparing the effective indices of TE and TM modes acquired from the FDM solver with those obtained using the FMM solver. By selecting a narrow range of valid window size ranging from 1.2 to 2 μm, we ran the simulation with FDM and FMM solver separately to obtain the effective indices and profiles of TE and TM modes of the waveguide. As shown in Fig. 5.5, the effective indices obtained from these two solvers agree within an error of 0.25%, and demonstrate consistency over the range of valid window size.

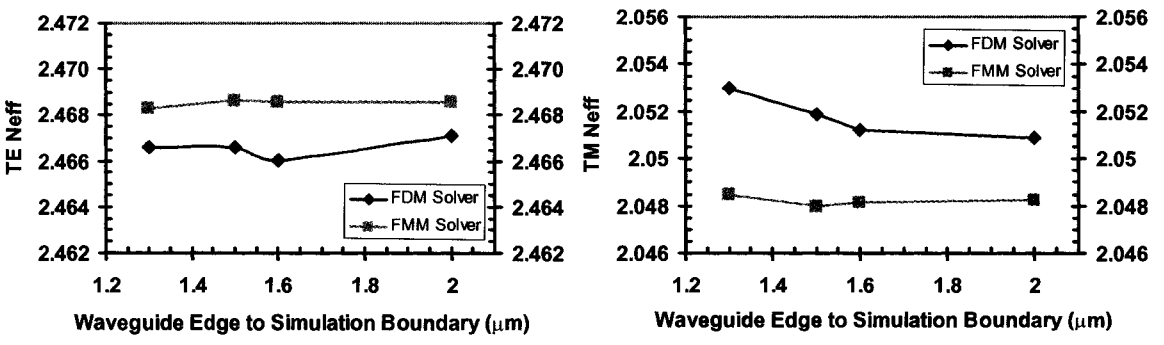


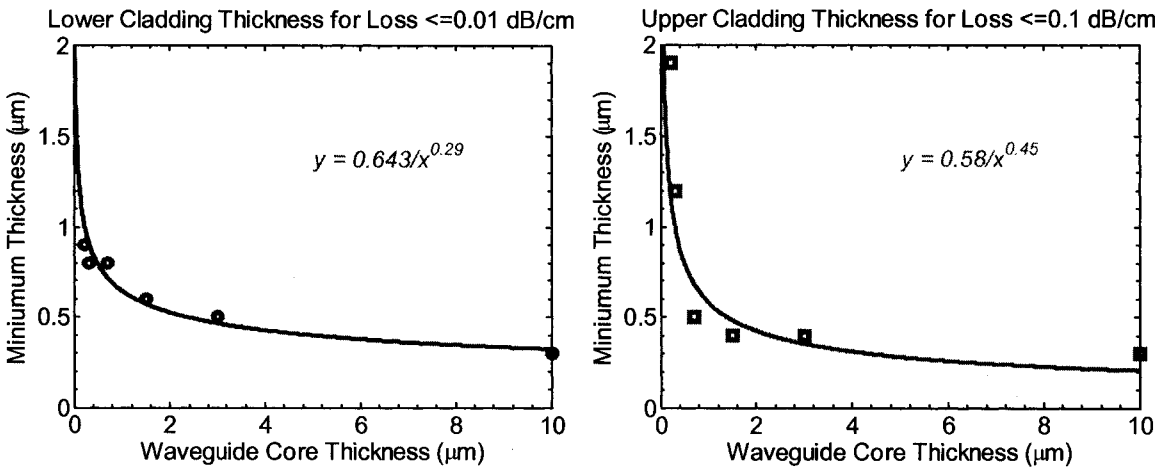

Fig. 5.5. Comparison of the effective index of fundamental (a) TE and (b) TM modes of 0.22 μm channel waveguide determined from film-mode-matching (FMM) mode solver and finite-difference mode (FDM) solver.

This comparison shows the validity of FDM solver in simulating mode profile and acquiring accurate effective index for our analysis.

### *5.2.2. Optical Loss Criteria and Cladding Thickness*

As mentioned in Chapter 4, optical loss can be caused by the absorption of the metal heater stripe or the coupling to the bulk Si substrate. In the study of device scaling where the waveguide thickness varies from 10 to 0.22 μm, the minimum thickness of the buried oxide layer required to keep the coupling loss to the Si substrate (in TE polarization) below 0.01 dB/cm also varies accordingly. This lower cladding thickness can be determined in a 2D slab waveguide model using MENU mode solver, which utilizes the transfer matrix method to calculate the loss. Calculating the coupling loss in FIMMWAVE by constructing a 3D ridge waveguide model will otherwise require an appropriate thickness of Si substrate to start with, which is difficult to determine because either insufficient or additional substrate thickness will result in the loss of accuracy and efficiency in the optical loss calculation. This problem can be avoided in MENU solver by using the slab model, where the six waveguides of interest mentioned in *Section 5.1* can be simplified to a three-layer slab waveguide model consisting of a Si core layer, a buried oxide layer and a bulk Si substrate. In these simplified waveguide models, the thickness of the slab waveguide is set equal to the thickness of Si core layer, which is 10, 3, 1.5, 0.7, 0.3 and 0.22 μm, respectively. The solution of the effective index and extinction coefficient of any slab mode is relatively insensitive to the bulk Si substrate. Using MENU solver, the increase in optical loss in the slab waveguide models with

decreasing lower cladding thickness could be estimated, as the guided mode couples to the substrate. From the loss-cladding thickness relation, the minimum thickness of oxide cladding required to maintain a coupling loss limit of ≤ 0.01 dB/cm could thus be determined. The calculated minimum lower cladding layer thickness as a function of the waveguide core thickness is plotted in Fig. 5.6(a). The calculated data can be fitted with a power law equation (stated in the figure), as shown by the solid curve.




(a) (b)

Fig. 5.6. The minimum thickness of (a) buried oxide layer required to keep the coupling loss to the Si substrate below 0.01 dB/cm, and (b) SiN upper cladding layer required to keep the absorption loss by the metal heater below 0.1 dB/cm, for SOI waveguides with thickness ranging from 10 to 0.22 μm. The calculated cladding thickness can be fitted using power law equations as shown by the solid curves.

The minimum thickness of the buried oxide increases rapidly with the scaling of waveguide core thickness. At the extreme of our scaling spectrum, the 0.22 μm thin photonic wire waveguide requires around 1 μm thick buried oxide layer to isolate the mode from coupling to the substrate.

Another possible loss component in SOI waveguides of a thermo-optic switch or modulator is the absorption loss caused by insufficient isolation between the waveguide core and metal heater on top of the upper cladding. The extinction coefficient depends on the evanescent field penetration into the metal layer, and therefore on the SiN upper cladding thickness. In this work, the SiN thickness of each waveguide is chosen to give ≤ 0.1 dB/cm of absorption loss, in both TE and TM polarizations. This is a relaxed loss criterion as compared to the 0.01 dB/cm for the substrate coupling loss, because the substrate loss will affect the total propagation length of the devices, while the metal absorption loss affects only the heater length. For our designed heater length of ~1 mm, the absorption loss will not exceed 0.01 dB as long as the SiN cladding thickness is chosen to meet the loss criterion of ≤ 0.1 dB/cm. Loss simulation with 3D waveguide model in FIMMWAVE can provide detailed information on the requirement of SiN upper cladding thickness. Unlike in MENU solver, realistic 3D waveguide models consist of ridges or channels are analyzed using a FDM solver, to calculate the extinction coefficient $k$, and effective index $N_{eff}$ of their guided modes. From the extinction coefficient of the mode, one can determine the absorption loss using Equation (4.2). In the calculation of this minimum SiN thickness, SiN is assumed to be lossless and the buried oxide layer thickness is set by the corresponding value shown in Fig. 5.6(a).

The calculated SiN thickness is plotted with respect to the waveguide core thickness in Fig. 5.6(b). The thickness also increases with decreasing waveguide dimension following a power law. For the thinnest photonic wire waveguide of 0.22 μm,

a 1.9 μm thick SiN upper layer is required to keep the optical loss below 0.1 dB/cm. This thickness is around 4× larger than the cladding thickness of a 0.7 μm ridge waveguide.

### *5.2.3. Simulated TE and TM Modes*

The next step is to simulate the TE and TM fundamental modes guided in each of the six waveguides. Using the cladding thickness found in Fig. 5.6 and the appropriate simulation setting for window size and grid density described in the previous section, all six SOI waveguide models with well-defined width and height are constructed in FIMMWAVE so that their fundamental TE and TM modes can be simulated with the FDM solver. The simulated TE modes of all the waveguides are shown in Fig. 5.7, while the TM modes are shown in Fig. 5.8.

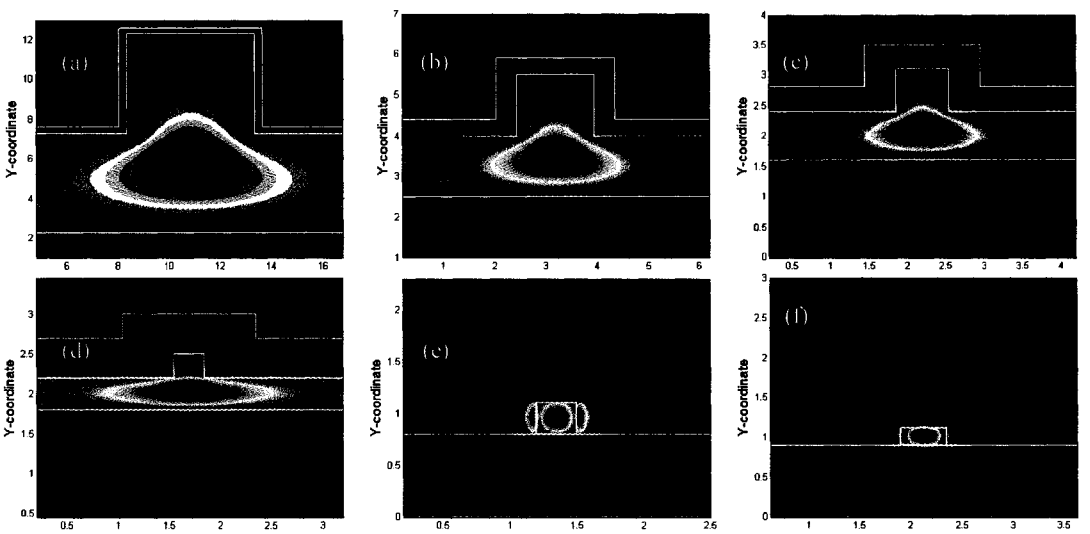



Fig. 5.7. The fundamental TE mode of a (a) 10, (b) 3, (c) 1.5, (d) 0.7 μm ridge waveguide, (e) 0.3 × 0.3 and (f) 0.22 × 0.45 $\mu m^2$ channel waveguide.

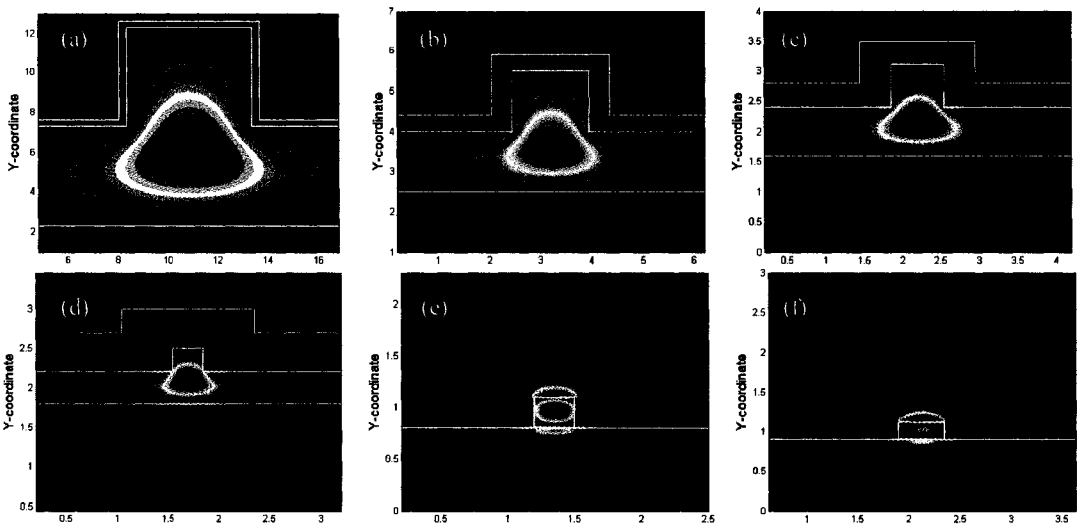



Fig. 5.8. The fundamental TM mode of a (a) 10, (b) 3, (c) 1.5, (d) 0.7 μm ridge waveguide, (e) 0.3 × 0.3 and (f) 0.22 × 0.45 $\mu m^2$ channel waveguide.

For the ridge waveguides, although both TE and TM modes appear to be tightly confined within the Si core, it is interesting to note that TE modes expand more laterally into the wings of the ridges than TM modes. As the waveguide shrinks, the field in the ridge is *compressed* and pushed downward into the slab. Nevertheless, the mode is overall confined within the Si core layer that includes both ridge and slab.

On the other hand, in a 0.3 μm wide channel waveguide, both TE and TM modes are no longer confined tightly within the core. The mode field expands noticeably into the cladding. Due to a smaller index step between SiN and Si, the expansion of mode field into the upper cladding layer is deeper than the lower oxide cladding. As the waveguide dimension shrinks further to 0.22 μm, the TM mode of the channel waveguide delocalizes and its field extends considerably into the cladding. The peak intensity of the field is no longer located within the core, but has shifted instead to the core-cladding

interfaces.

## 5.3. REFRACTIVE INDEX AND THERMO-OPTIC COEFFICIENT CONTOURS

Contour plots of refractive index and thermo-optic coefficient distribution in the waveguides are needed to quantify the thermo-optic response of SOI switches and modulators. As an example, the refractive index contour of a 1.5 μm wide ridge waveguide is shown in Fig. 5.9(a), while the thermo-optic coefficient contour of the same waveguide is shown in Fig. 5.9(b).

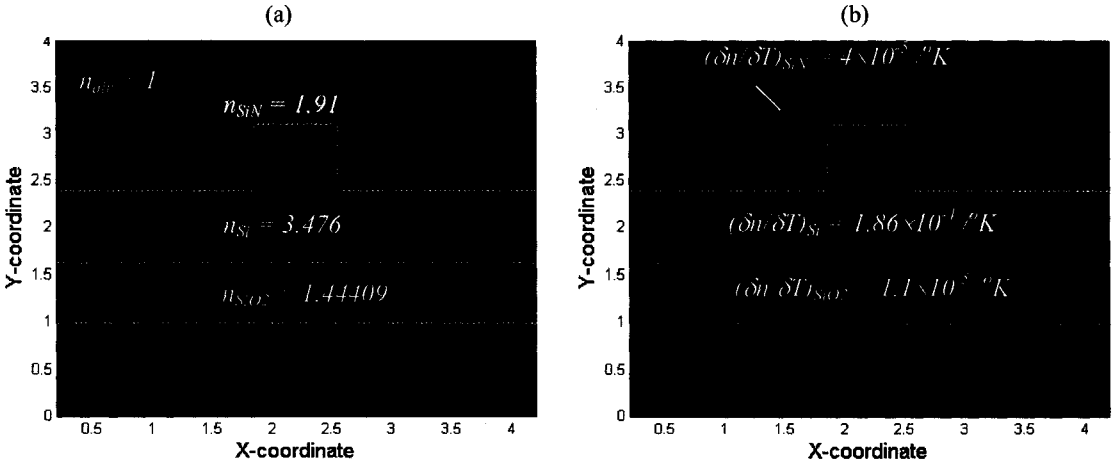



Fig. 5.9. Contour plots of (a) refractive index and (b) thermo-optic coefficient of a 1.5 μm ridge waveguide.

As the device scales, the region of high refractive index ($n_{si}$ = 3.476) decreases with the decreasing core size while the region of moderate refractive index ($n_{siN}$ = 1.91) and low refractive index ($n_{siO2}$ = 1.44409) increases with the increasing cladding thickness to maintain waveguide loss at acceptable levels as outlined in Section *5.2.2.*

## 5.4. PERTURBATION THEORY

The primary goal in the study of device scaling is to evaluate the impact of the change in mode field profiles on the power and speed of SOI MZI thermo-optic switches. The method used in Chapter 4 of extracting the differential temperature between the cores of the heated and reference waveguides to derive the $\pi$-phase shift power is a good approximation only when the mode is strictly confined within the core. When the analysis involves photonic wire waveguides, this simplification can no longer provide accurate results (this aspect will be discussed in greater detail in Section *5.6.1*). A numerical method based on perturbation theory of optical waveguides offers a rigorous solution to this problem [5.18].

Perturbation theory allows one to use the known solutions for unperturbed optical waveguides to determine the effect of small changes that occur to the refractive indices of optical waveguides, which are caused by changes in environment, such as temperature, electric field, magnetic field, and mechanical stress etc [5.19]. In this study, the perturbation theory is applied to quantify the changes in the effective index of the guided modes induced by small temperature changes.

Consider the various SOI waveguides with mode profiles described in the previous section. The exact solutions of these mode profiles are known and will change only slightly under the perturbation by the thermo-optic effect. By taking advantage of the smallness of perturbation, one can use approximation technique to derive accurate expressions for the modes of the perturbed waveguides in terms of the known modes of

the unperturbed waveguides. Assuming the perturbation does not vary in the propagation direction $z$ along the waveguide, and the perturbed waveguide is characterized by a refractive index profile $\bar{n}(x,y)$ relative to the Cartesian axes in the cross-section, the unknown electric field of the perturbed mode can be expressed as [5.19]:

$$\bar{E}(x,y,z) = \bar{\psi}(x,y) \cdot e^{i\bar{\beta}z} \tag{5.1}$$

where $\bar{\beta}$ is the propagation constant and $\bar{\psi}(x,y)$ is the electric field determined by the refractive index profile $\bar{n}(x,y)$. The corresponding mode on the unperturbed waveguide is characterized similarly by the refractive index profile $n(x,y)$ and known electric field $\psi$ with the propagation constant of $\beta$, where

$$E(x,y,z) = \psi(x,y) \cdot e^{i\beta z} \tag{5.2}$$

The exact solution to the Maxwell's equation for the perturbed waveguide will then satisfy:

$$\left\{\nabla^2 + k^2\bar{n}^2(x,y) - \bar{\beta}^2\right\}\bar{E} = 0 \tag{5.3}$$

while the known solution for the unperturbed waveguide satisfies:

$$\left\{\nabla^2 + k^2 n^2(x,y) - \beta^2\right\}E = 0 \tag{5.4}$$

where $\nabla^2$ is the transverse Laplace operator, $k = 2\pi/\lambda$ is the wave number, and $\lambda$ is the free-space wavelength. In order to express the characteristics of perturbed waveguides, namely $\bar{\beta}$ and $\bar{E}$, in terms of $\beta$ and $E$, one can use a reciprocal relationship between the two solutions [5.19]:

$$\beta^2 - \overline{\beta}^2 = \frac{k^2 \iint (n^2 - \overline{n}^2) E \cdot E^* \cdot dxdy}{\iint E \cdot E^* \cdot dxdy} \tag{5.4}$$

When the magnitude of the perturbation is very small, the transverse dependence of the mode fields on the perturbed and unperturbed waveguides is similar, *i.e.* $\overline{\psi} \cong \psi$ and consequently $E \cong \overline{E}$ [5.19]. Given that $\overline{n} - n = \Delta n$, and $\overline{\beta} - \beta = \Delta\beta$, Equation (5.4) can then be simplified to:

$$\Delta\beta = \frac{k \iint (n\Delta n)|E|^2 \cdot dxdy}{N_{eff} \iint |E|^2 \cdot dxdy} \tag{5.5}$$

The resultant change in the effective index of the mode is given by:

$$\Delta N_{eff} = \frac{\iint \left[ n \cdot \left( \frac{\partial n}{\partial T} \cdot \Delta T \right) \right] |E|^2 \cdot dxdy}{N_{eff} \iint |E|^2 \cdot dxdy} \tag{5.6}$$

The perturbation mainly occurs in the regions of high field concentration, high refractive index and high thermo-optic coefficient. In the case of SOI ridge waveguides where the mode is strongly confined within the Si core, which possesses high refractive index ($n_{si}$ = 3.476) and high thermo-optic coefficient ($1.86 \times 10^{-4}$ /°K) compared to SiN or $SiO_2$ cladding, the equation predicts that index perturbation will originate mainly from heating the Si core. However, for photonic wire waveguides where the mode expands into the cladding, an effective index perturbation will also result from temperature changes in the cladding.

## 5.5. POWER ANALYSIS : STEADY STATE THERMAL SIMULATION

Perturbation theory will be used to calculate the heater power required to induce a π-phase shift in a thermo-optic switch, using Equation (5.6).

### *5.5.1. Temperature Distribution*

The simulated temperature distribution for all six MZI switches constructed from the six different waveguide configurations is shown in Fig. 5.10. These switches have a common arm separation of 10 μm and the power applied to the heaters is 200 mW. Fig. 5.10(a) shows the temperature distribution in a 10 μm wide ridge waveguide thermo-optic switch. From left to right, the first image in the Fig. 5.10(a) shows the temperature distribution in the reference arm of the switch, while the last two images correspond to the temperature distribution in the heated (or active) arm. The isothermal lines in the last image have an interval 0.25°C, while the arrows indicate the direction of heat flow. Figure 5.10(b), (c) and (d) shows the same temperature distribution in a 3, 1.5 and 0.7 μm ridge waveguide thermo-optic switch, respectively.

Because of the higher thermal conductivity of Si, the temperature is much more uniform in Si than in the $SiO_2$ buried layer. The major drop in temperature occurs mainly across the $SiO_2$ layer instead of Si. This means that heat is insulated by the buried oxide from diffusing into the bulk Si substrate from Si core layer. As the buried oxide thickness increase, the temperature in the Si core layer increases accordingly, even if the power remains constant. This is shown in Fig. 5.10 from (a) to (d). As the buried oxide thickness

increases from 0.3 to 0.8 μm with the decreasing waveguide core thickness, the peak temperature in the waveguide core increases from 307 K to 315 K.

When the waveguide core thickness decreases from 10, 3, 1,5, to 0.7 μm, at a fixed heater width of 4 μm, the heater coverage changes from covering the ridge partially to folding over the entire ridge and its wings. The heat flow pattern varies significantly with this change in the coverage. In the 10 μm ridge waveguide, heat flux is flowing unidirectionally downwards before reaching the slab layer. When the heat reaches the slab layer, the flow eventually curves toward lateral directions, as indicated by the arrows in Fig. 5.10(a). When the waveguide thickness shrinks to 3 μm, as shown by the arrows in Fig. 5.10(b), the heater is large enough to fold over the ridge and heat is supplied not only from the top of the ridge but also through the sidewalls of the ridge.

Comparing Fig. 5.10(b) and 5.10(a), it is clear that the center of the 3 μm ridge in the active arm is heated to a higher temperature than the 10 μm ridge, at the same applied power to the same heater width. Similar conclusions can be drawn by comparing Fig. 5.10(c) and 5.10(d) to Fig. 5.10(a). In summary, as the ridge waveguide shrinks in width and thickness under the same applied power, the temperature at the center of the heated (or active) ridge increases because:

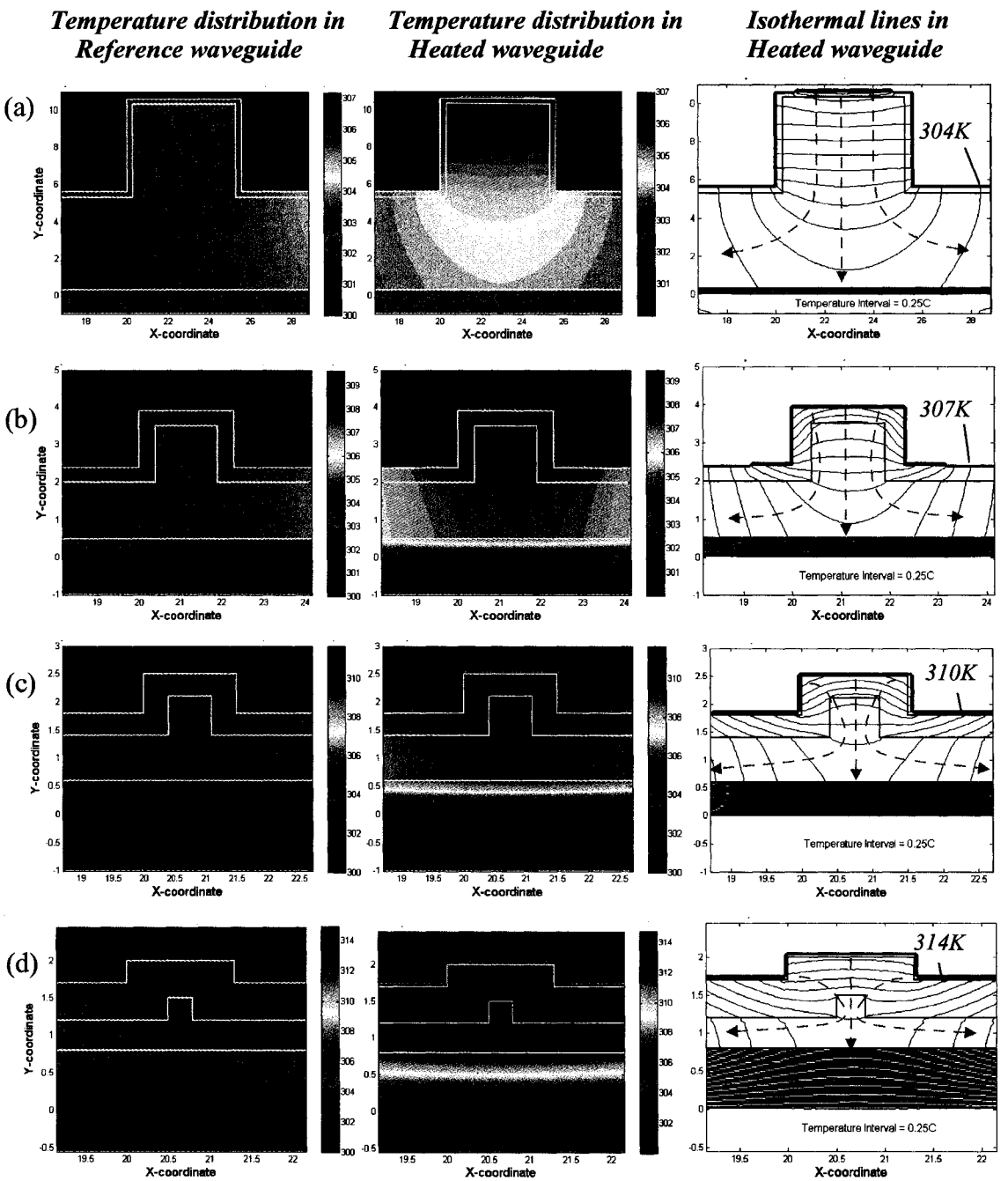



Fig. 5.10. Temperature distribution in the reference waveguides and heated waveguides of 10 μm-spaced ridge waveguide MZI switches with a core thickness of (a) 10 (b) 3, (c) 1.5 and (d) 0.7 μm. The switches are heated at 200 mW power. The isothermal lines have a fixed interval of 0.25°C.

(i) the cross-section of the Si ridge is reduced therefore more heat per unit volume is received in the ridge (refer to Equation (4.3) for the definition of $\Phi_q$).

(ii) the heater folds over the ridge thus increasing heating efficiency.

(iii) the buried oxide layer is thicker and therefore more effective in insulating heat within the Si core layer.

(iv) the Si slab layer is thinner thus reducing lateral spreading of heat.

The temperature distribution in the reference arms is equally essential to the thermo-optic responses of the MZI switches. As shown in Fig. 5.10(a), (b), (c) and (d), the temperature at the center of the reference waveguide core increases as the waveguide shrinks.

The temperature distributions of the reference and heated photonic wire waveguides are shown in Fig. 5.11. For a 0.3 × 0.3 $\mu m^2$ photonic wire waveguide, the heater is separated from the waveguide core by a 1.2 μm thick SiN upper cladding. Because of this thick cladding, less heat from the heater will be able to reach the core because of the lower thermal conductivity of SiN. In addition, since the heater is much wider than the waveguide core, heat generated close to the edges of the heater is conducted away from the channel waveguide core, as illustrated by the red arrows in Fig. 5.11. This results in the loss of energy. The heating efficiency in a 0.3 μm photonic wire waveguide will therefore be lower than in a 0.7 μm ridge waveguide. When the channel waveguide shrinks further to 0.22 μm, the SiN cladding thickness is further increased to 1.9 μm, so that more heat is lost through lateral diffusion, and the temperature in the 0.22

μm core is lower than the temperature in 0.3 μm core.

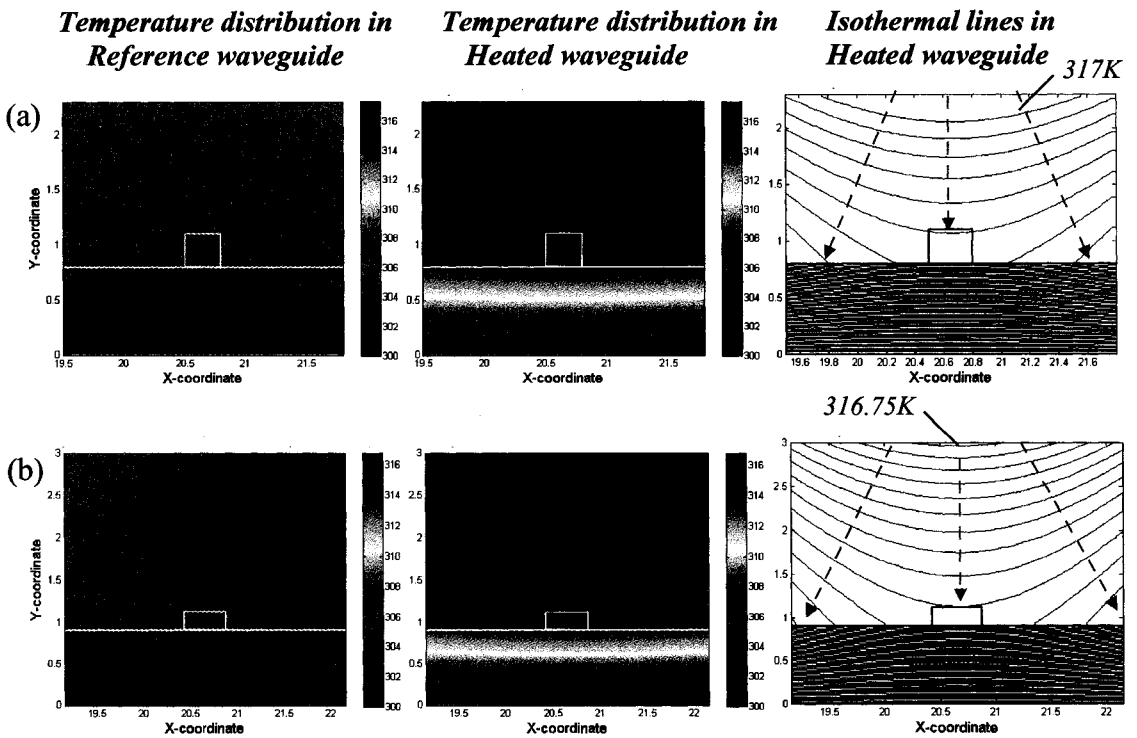



Fig. 5.11. Temperature distribution in the reference waveguides and heated waveguides of 10 μm-spaced photonic wire waveguide MZI switches with a core thickness of (a) 0.3 and (b) 0.22 μm. The switches are heated at 200 mW power. The isothermal lines have a fixed interval of 0.25°C.

Another difference in heat flow in the channel waveguides is the thermal isolation between the two waveguide cores. Without the connecting Si slab, heat no longer flows from the heated waveguide to the reference waveguide through Si. Instead, heat is only conducted through SiN and $SiO_2$ cladding from the heat source to the reference core. This change in heat conduction path has a significant effect on both power consumption and speed of the thermo-optic switches and modulators. The temperature distribution of the 0.3 and 0.22 μm reference channel waveguides is plotted in Fig. 5.11(a) and (b),

respectively. While the two temperature contours appear to be similar to each other, they differ from the contours of reference ridge waveguides in that the temperature in the photonic wire reference core is primarily determined by the heat flow and distribution in the SiN upper cladding.

### *5.5.2. Perturbation of TE and TM modes*

By using perturbation theory, the change in the effective index of the waveguide mode $\Delta N_{eff}$ as a result of thermo-optic modulation, can be calculated from the temperature induced change in waveguide refractive index $\Delta n = \Delta T \cdot (\partial n / \partial T)$. Using the mode profile, refractive index profile, thermo-optic coefficients and temperature distribution in the waveguides, one can apply Equation (5.6) to calculate the change in the effective index of the mode. The magnitude of perturbation due to thermo-optic modulation scales as the product $n \cdot \Delta n \cdot |E|^2$, which provides an analytical insight into how and where the waveguide mode is perturbed. This product for TE and TM mode of a 10 μm ridge waveguide is plotted in Fig. 5.12(a) and 5.13(a), respectively.

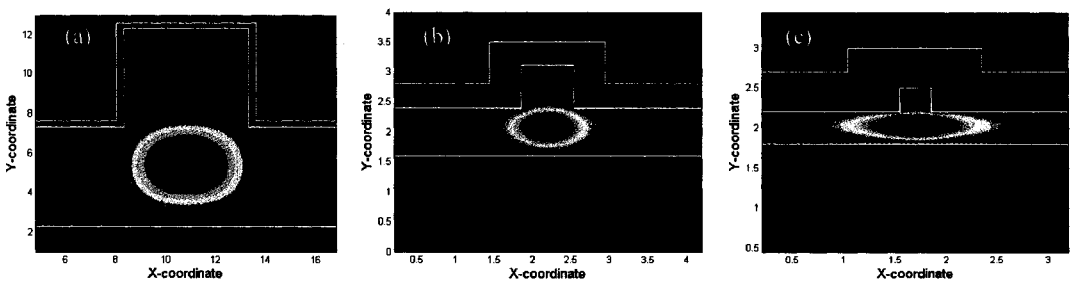



Fig. 5.12. The effect of thermo-optic perturbation $n \cdot \Delta n \cdot |E|^2$ on TE mode of a (a) 10, (b) 1.5, and (c) 0.7 μm ridge waveguide.

As shown in Fig. 5.12(a), perturbation of TE mode of a large 10 μm ridge waveguide occurs solely in the core and roughly resembles the original profile of the guided mode. However, the effect of perturbation appears to be more rounded and contracted in the core than the original mode profile. This is caused by the curved wavefront of the heat flux as it diffuses from top to bottom and spreads in the lateral direction.

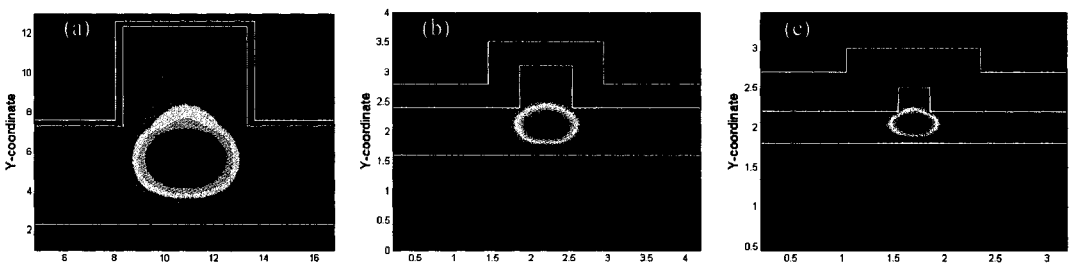



Fig. 5.13. The effect of thermo-optic perturbation $n \cdot \Delta n \cdot |E|^2$ on TM mode of a (a) 10, (b) 1.5, and (c) 0.7 μm ridge waveguide.

The effect of heating is prevalent in TM perturbation as the profile not only contracts into a more circular shape, as shown in Fig. 5.13, but also shifts closer towards the heat source. Apparently, the effect of perturbation is more dominant in the hotter core region. Similar "rounding" effect is observed for the perturbation of the guided modes in smaller ridge waveguides with the core thickness of 1.5 and 0.7 μm, as shown in Fig. 5.12 and 5.13(b) and (c). Again, in these smaller waveguides, the perturbation occurs solely in the ridge and slab of the Si core layer, but not in the cladding layer.

Surprisingly, the perturbation in photonic wire waveguides is still dominated by the Si core, despite the expansion of the mode into the cladding, as shown in Fig. 5.14

and 5.15. The magnitude of perturbation in the cladding of the photonic wire waveguides is ≤ 10% for TE mode and ≤ 20% for TM mode. The peak of TM perturbation shifts from the center of the core to the cladding-core interface when the thickness of the photonic wire waveguide is reduced from 0.3 to 0.22 μm. Also, as shown in Fig 5.15, although the perturbation of TM mode in the SiN upper cladding grows in response to the mode expansion, the contribution of the cladding to $\Delta N_{eff}$ remains small. As expected, the perturbation is weighted more strongly in the upper cladding than in the oxide lower cladding simply because of the much smaller thermo-optic coefficient and refractive index of oxide.

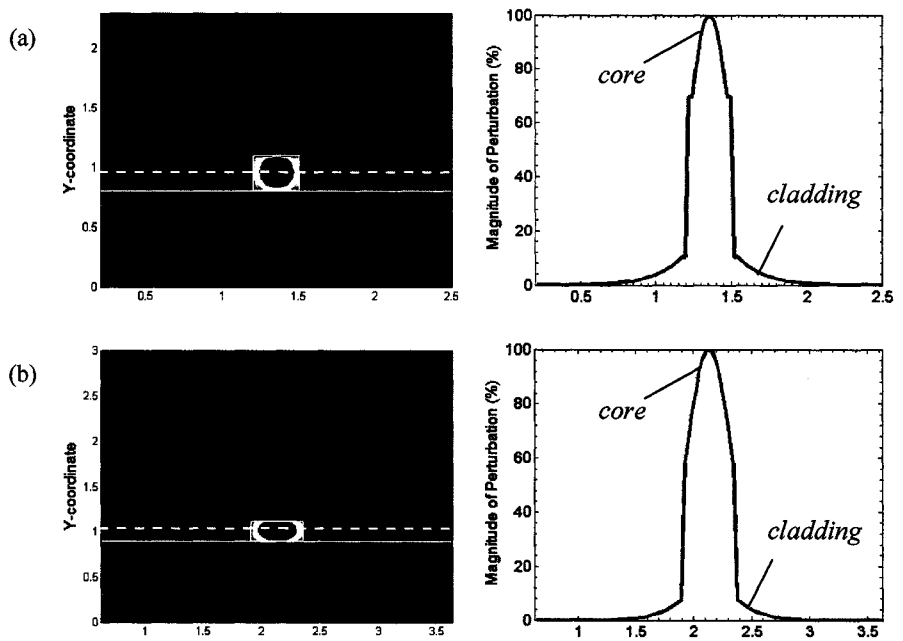



Fig. 5.14. *Left*: The effect of thermo-optic perturbation $n \cdot \Delta n \cdot |E|^2$ on TE mode of a (a) 0.3 × 0.3 and (b) 0.22 × 0.45 μm$^2$ channel waveguide. *Right*: The magnitude of TE perturbation along the dotted vertical lines, which run through the center of the cores of the two different channel waveguides.

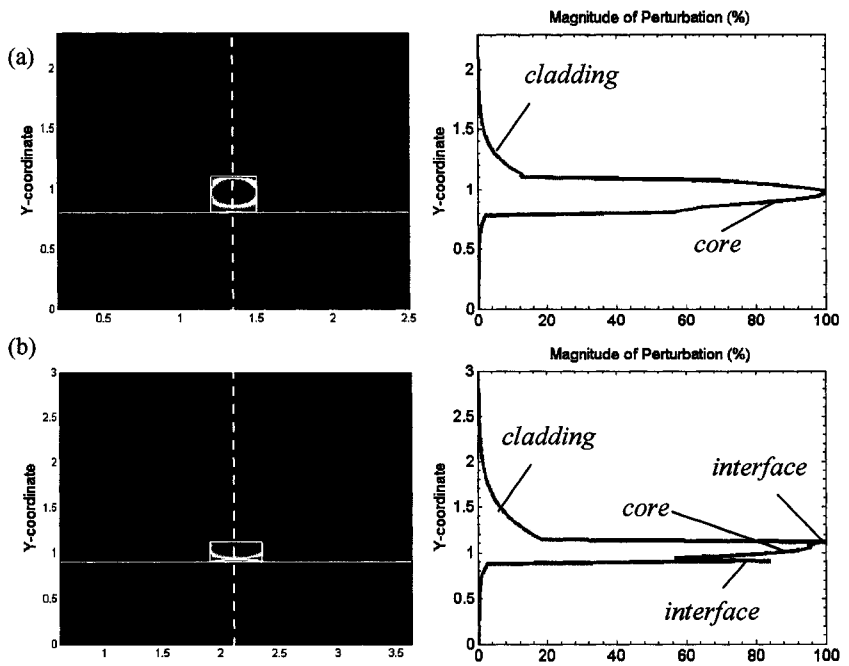



Fig. 5.15. *Left*: The effect of thermo-optic perturbation $n \cdot \Delta n \cdot |E|^2$ on TM mode of a (a) 0.3 × 0.3 and (b) 0.22 × 0.45 μm$^2$ channel waveguide. *Right*: The magnitude of TM perturbation along the dotted vertical lines, which run through the center of the cores of the two different channel waveguides.

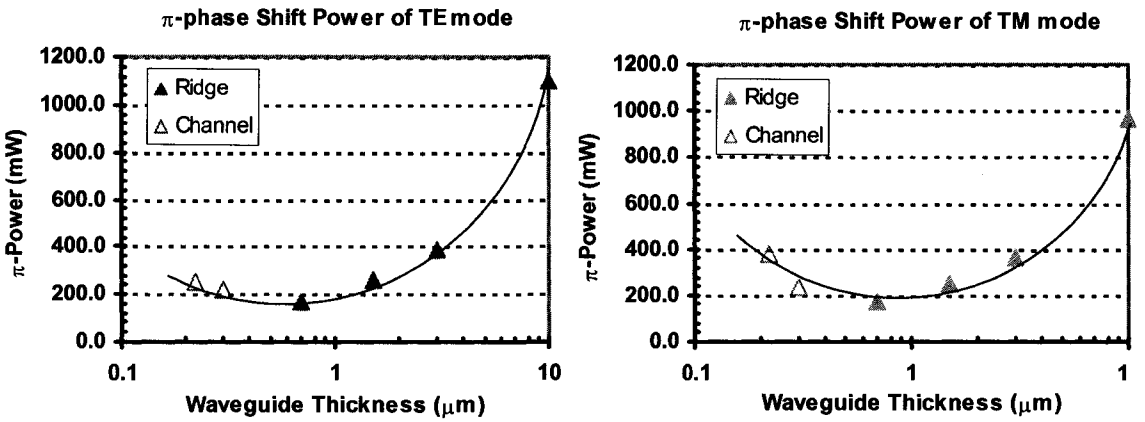
### *5.5.3. Effect of Device Scaling and Mode Expansion on Power*

By taking the overlap integral of the calculated perturbation and normalizing the integral by the unperturbed mode field as described in Equation (5.6), the change in the effective index of the guided modes as a result of heating can be determined. Table 5.1 summarizes the calculated effective index change of both TE and TM modes of six MZI thermo-optic switches with a common 10 μm arm separation at a given input power of 200 mW. These switches consist of different waveguides that were described previously.

Table 5.1 The change in effective index $\Delta N_{eff}$ at 200mW heating power and π-phase shift power $P_\pi$ for the TE and TM modes of MZI thermo-optic switches with the arm spacing of 10 μm.

| *Waveguide configuration* | *Thickness (μm)* | *Width (μm)* | *ΔNeff of TE mode* | *ΔNeff of TM mode* | *π-Power of TE mode (mW)* | *π-Power of TM mode (mW)* |
|---|---|---|---|---|---|---|
| *Ridge* | 10 | 5 | 0.0001759 | 0.000200 | 1103.1 | 971.2 |
| *Ridge* | 3 | 1.5 | 0.0005034 | 0.000540 | 385.3 | 359.1 |
| *Ridge* | 1.5 | 0.7 | 0.0007518 | 0.000769 | 258.0 | 252.4 |
| *Ridge* | 0.7 | 0.3 | 0.0011536 | 0.001149 | 168.2 | 168.8 |
| *Channel* | 0.3 | 0.3 | 0.0008852 | 0.000835 | 219.2 | 232.4 |
| *Channel* | 0.22 | 0.45 | 0.0007643 | 0.000512 | 253.8 | 378.8 |

From the calculated effective index change $\Delta N_{eff}$, the π-phase shift power $P_\pi$ that is required to introduce a $\Delta N_{eff}$ of $9.7\times10^{-4}$ can be derived from extrapolation. Variation in π-phase shift power with respect to the waveguide thickness of the TE mode and TM mode is plotted in Fig. 5.16(a) and (b), respectively.




(a) (b)

Fig. 5.16. Variation of π-phase shift power of (a) TE and (b) TM mode as a function of the thickness of waveguide core layer for ridge and channel waveguides in 10 μm–spaced SOI MZI switches.

In each figure, a trend line is inserted as a guide to the eye. The largest thermo-optic switch with 10 μm ridge waveguides has the highest switching power of more than 1000 mW. When the waveguide core layer thickness is reduced, the π-power drops significantly. A more than 6× (around 85%) power saving in response to the scaling of ridge waveguide thickness from 10 to 0.7 μm is observed. This power saving is mainly due to the *mode compression* (smaller mode field size therefore less area to be heated) as explained in Section *5.2.3* and increase in heating efficiency as explained in Section *5.5.1*.

Interestingly, if the waveguide configuration is altered from ridge to channel waveguide to the thickness of 0.3 μm, the π-power actually increases by 30% to 220 mW for TE and by 27% to 230 mW for TM. This undesired increase in power is a combined result of the increase in upper cladding thickness, the expansion of the mode field into the cladding and the reduction in heating efficiency because of the lack of side heating from the heater that would otherwise fold around a ridge waveguide.

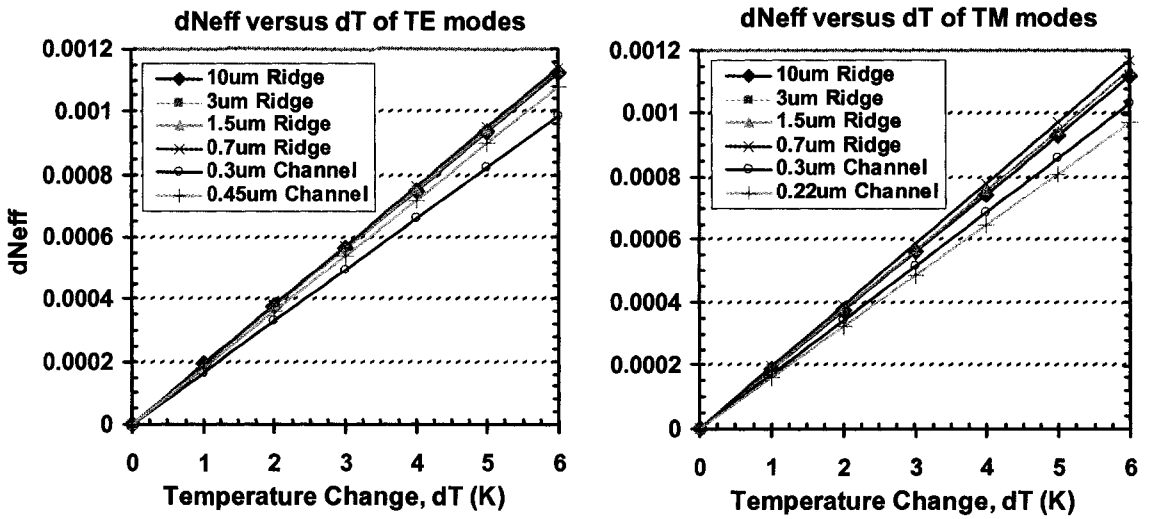
The π-power of TM mode rises from around 230 to 380 mW, when the channel waveguide thickness is reduced from 0.3 to 0.22 μm. The rise in power will continue with the continuing scaling of channel waveguide thickness and essentially reverses the trend of power consumption observed for the micron-size ridge waveguides in which shrinking of device promotes power saving. Eventually, the power-scaling plot produces a parabolic curve with a minima corresponding to the optimum operating point where the power consumption is minimum. The power consumption of a MZI switch with 0.7 μm

ridge waveguide is the minimum among all waveguide configurations.

Further scaling of photonic wire waveguide will only increase power consumption as the mode expands further and forces a thicker cladding. Contrary to what many would have expected, smaller switches do not necessarily consume less power. Therefore, designing low-power SOI MZI switches in the context of device scaling actually requires much careful and thorough consideration of multiple factors, including mode field profile, properties of core and cladding materials, as well as geometries of waveguides and heater, which eventually affect the heat flow pattern.

At this point, it is worth de-convoluting the effect of mode expansion from cladding and heat flow pattern on the power increment in the photonic wire waveguides. The effect of mode expansion in both TE and TM polarizations can best be quantified by the rate of change in the effective index of the mode with respect to a uniform change in temperature $dN_{eff}/dT$, at all waveguide dimensions. $dN_{eff}/dT$ can be calculated from the optical simulation in FIMMWAVE, by assuming a uniform temperature distribution over the waveguide cross-section. When the temperature of the waveguide cross-section is changed uniformly, the change in the effective index of the mode in the waveguide is determined by the change in the refractive indices of the waveguide materials, including Si, SiN upper cladding and $SiO_2$ lower cladding, which are in turn determined by their thermo-optic coefficients. By comparing $N_{eff}$ calculated at two different temperatures (e.g. $T_o$ and $T_o+\Delta T$, where $\Delta T = 1^{\circ}C$), $dN_{eff}/dT$ can be calculated. The plot of $dN_{eff}$ for TE and TM modes of all six waveguides with increasing temperature is shown in Fig. 5.17(a)

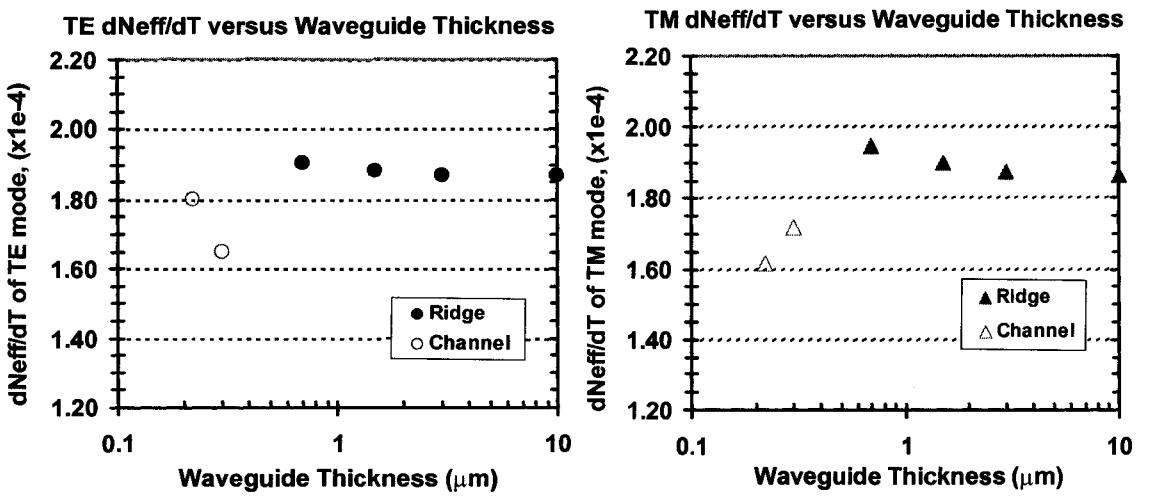
and (b), respectively.




(a) (b)

Fig. 5.17. Change in the effective indices $dN_{eff}$ of (a) TE and (b) TM modes as a function of temperature for the ridge and channel waveguides, simulated in FIMMWAVE.

Since the $dN_{eff}$ varies linearly with temperature $dT$ in both TE and TM polarizations, the slopes $dN_{eff}/dT$ can be extracted and plotted with respect to the waveguide thickness, as shown in Fig. 5.18. A special case in the plot is the asymmetrical $0.22 \times 0.45$ $\mu m^2$ photonic wire waveguide. Because of the direction of polarizing vector, the change in the effective index of the TE modes is actually sensitive to the waveguide width rather than thickness. Therefore, although it appears in Fig. 5.18(a) that the $dN_{eff}/dT$ of the TE modes of the photonic wire waveguides increases with the decreasing waveguide thickness from 0.3 to 0.22 μm, in reality it is actually increasing with the increasing waveguide width from 0.3 μm to 0.45 μm, so that the trend is consistent with the $dN_{eff}/dT$ of TM modes.




(a) (b)

Fig. 5.18. Change in the effective indices of (a) TE and (b) TM modes with respect to temperature change $dN_{eff}/dT$, as a function of the dimensions of the ridge and channel waveguides.

As shown in Figure 5.18, when the waveguide thickness is large, *i.e.* more than 1 μm, the rate of change in the effective index of the mode with temperature $dN_{eff}/dT$ is completely dominated by the thermo-optic coefficient of Si ($dN_{eff}/dT = \partial n/\partial T = 1.86\times10^{-4}$ /K). This is because the mode is tightly confined within the core and the refractive index of Si is significantly larger than SiN or Si, therefore perturbation mainly occurs in the Si. This means that the thermo-optic coefficients of the SiN and $SiO_2$ cladding do not play a role in the thermal perturbation of the mode, and therefore have no impact on the change in power consumption, when the ridge waveguide thickness is reduced from 10 to 1.5 μm. As the waveguide thickness is reduced to 0.7 μm, there is a slight change in the $dN_{eff}/dT$, but the major change occurs when waveguide configuration is switched from ridge to channel waveguide at the thickness of 0.3 μm. The decrease in $dN_{eff}/dT$ indicates

the delocalization of mode and its expansion into the cladding. From the waveguide thickness of 0.7 to 0.3 μm (the waveguide width remains unchanged at 0.3 μm), there is a 13% decrease in $dN_{eff}/dT$ for TE and a 12% decrease for TM polarization. Compared to the 30% increase in π-power for TE mode (from ~168 mW to ~220 mW) and the 37% increase for TM mode (from ~168 mW to ~232 mW) in the same thickness range, as shown in Fig. 5.16(b), the effect of mode expansion accounts for approximately 1/3 of the total power change. This would imply that the increase in the upper cladding thickness and the change in heat flow pattern in the waveguide are the dominant factors accounting for the increase in the π-power.

### *5.5.4. Effect of Polarization*

TE modes of the large dimension ridge waveguides of the thermo-optic switches require more switching power than the TM modes. This is illustrated by the plot of the difference in π-power between TE and TM modes ($\Delta P_\pi = P_{\pi(TE)} - P_{\pi(TM)}$) with respect to the waveguide thickness, as shown in Fig. 5.19. This polarization dependent power difference $\Delta P_\pi$, is at a large positive value of 140 mW when the ridge waveguide thickness is at 10 μm. Refer to Fig. 5.10, it is obvious that the temperature at the top of the ridge is the hottest. Since the TM mode distribution sits higher in the ridge than the TE mode, as shown in Fig. 5.8(a), the TM mode is more effectively heated. The change in effective index of the TM mode is therefore larger than in the TE mode, under the same power. Hence, for large ridge waveguides, $\Delta P_\pi$ is large. As the waveguide shrinks, the effect of temperature gradients on $P_\pi$ for the two polarizations diminishes in

accordance with the decreasing mode size. This explains the drop in the value of $\Delta P_\pi$ toward zero, as the ridge waveguide thickness reduces to 0.7 μm.

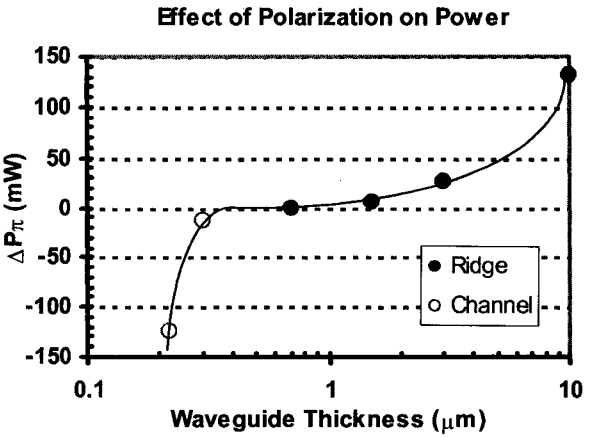



Fig. 5.19. Polarization dependent π-phase shift power as a function of waveguide thickness in SOI MZI switches with an arm separation of 10 μm.

Even when the waveguide configuration is switched over from ridge to photonic wire, $\Delta P_\pi$ will be approximately zero as long as the geometrical symmetry of the waveguide is preserved (width to height ratio of unity). This is the case for our 0.3 × 0.3 $\mu m^2$ photonic wire waveguide. The thermo-optic switch adapting this waveguide configuration is basically polarization independent, as shown in Fig. 5.19. Conversely, π-power of a thermo-optic switch made of 0.22 × 0.45 $\mu m^2$ (height × width) asymmetrical photonic wire waveguides is strongly sensitive to polarization. In this waveguide where the thickness is only half of the width, TM mode field expands extensively into the cladding but TE mode field is still confined within the core. Significantly more power is needed to perturb the TM mode than TE mode, leading to a

drastic drop of $\Delta P_\pi$ value towards negative. This underscores the importance of either maintaining geometrical symmetry or not making the photonic wire waveguide too thin, in the design to achieve polarization independent signal processing.

### *5.5.5. Effect of Arm Spacing*

In Chapter 4, thermal gradient between the two arms has been demonstrated to have a profound effect on the power and speed of the MZI switches. It has been shown that by increasing the arm spacing, the $\pi$-power requirement of an MZI switch can be improved. In the study of device scaling, arm spacing is still a critical device parameter. For this reason, models of MZI switches with a common arm spacing of 40 μm were built and simulated in ATAR to obtain the temperature contours that would allow the calculation of the change in effective index of guided TE and TM modes. Table 5.2 summarizes the change in effective index of the switches with arm spacing of 40 μm.

Table 5.2 The change in effective index $\Delta N_{eff}$ at 200mW heating power and $\pi$-phase shift power $P_\pi$ for the TE and TM modes of MZI thermo-optic switches with the arm spacing of 40 μm.

| *.Waveguide configuration* | *Thickness (μm)* | *Width (μm)* | *ΔNeff of TE mode* | *ΔNeff of TM mode* | *π-Power of TE mode (mW)* | *π-Power of TM mode (mW)* |
|---|---|---|---|---|---|---|
| *Ridge* | 5 | 5 | 0.0004500 | 0.000473 | 431.1 | 410.2 |
| *Ridge* | 1.5 | 1.5 | 0.0009658 | 0.001004 | 200.9 | 193.3 |
| *Ridge* | 0.7 | 0.7 | 0.0012536 | 0.001269 | 154.8 | 152.9 |
| *Ridge* | 0.3 | 0.3 | 0.0017746 | 0.001732 | 109.3 | 112.0 |
| *Channel* | 0.3 | 0.3 | 0.0012063 | 0.001137 | 160.8 | 170.6 |
| *Channel* | 0.22 | 0.45 | 0.0011795 | 0.000789 | 164.5 | 245.8 |

Another interesting MZI thermo-optic switch model is the one that has infinite arm spacing. This model is identical to a thermally isolated MZI switch with a heated arm

and a completely remote reference arm. Imagine that heat flow between the arms is absolutely shut off, the temperature distribution in the reference are will remain at 300K uniformly, while the temperature in the heated arm is unaffected by the presence of the reference arm. The analysis of this MZI switch can be readily accomplished by considering only the temperature contour in the heated arm and assume a uniform 300K temperature profile of the reference arm even in the presence of a connecting slab layer. Using the absolute temperature contour of the heated arm of a MZI with an arm spacing of 10 μm, instead of the differential temperature contour between the two arms, the change in effective index and π-power of an infinitely-spaced MZI thermo-optic switch can be approximated. The calculated results of such switches of different waveguide thickness are summarized in Table 5.3.

Table 5.3 The change in effective index $\Delta N_{eff}$ at 200mW heating power and π-phase shift power $P_{\pi}$ for the TE and TM modes of MZI thermo-optic switches with infinite arm spacing.

| *Waveguide configuration* | *Thickness (μm)* | *Width (μm)* | *ΔNeff of TE mode* | *ΔNeff of TM mode* | *π-Power of TE mode (mW)* | *π-Power of TM mode (mW)* |
|---|---|---|---|---|---|---|
| *Ridge* | 10 | 5 | 0.000779 | 0.0008007 | 248.9 | 242.3 |
| *Ridge* | 3 | 1.5 | 0.001290 | 0.0013299 | 150.3 | 145.9 |
| *Ridge* | 1.5 | 0.7 | 0.001541 | 0.0015562 | 125.9 | 124.7 |
| *Ridge* | 0.7 | 0.3 | 0.002052 | 0.0020218 | 94.5 | 96.0 |
| *Channel* | 0.3 | 0.3 | 0.001356 | 0.0012780 | 143.1 | 151.8 |
| *Channel* | 0.22 | 0.45 | 0.001348 | 0.0009018 | 143.9 | 215.1 |

A plot of π-power with respect to waveguide thickness at different MZI arm spacing can be constructed by consolidating the data in Table 5.1, 5.2 and 5.3. The π-power plot for TE mode and TM mode is shown in Fig. 5.20 and Fig. 5.21, respectively.

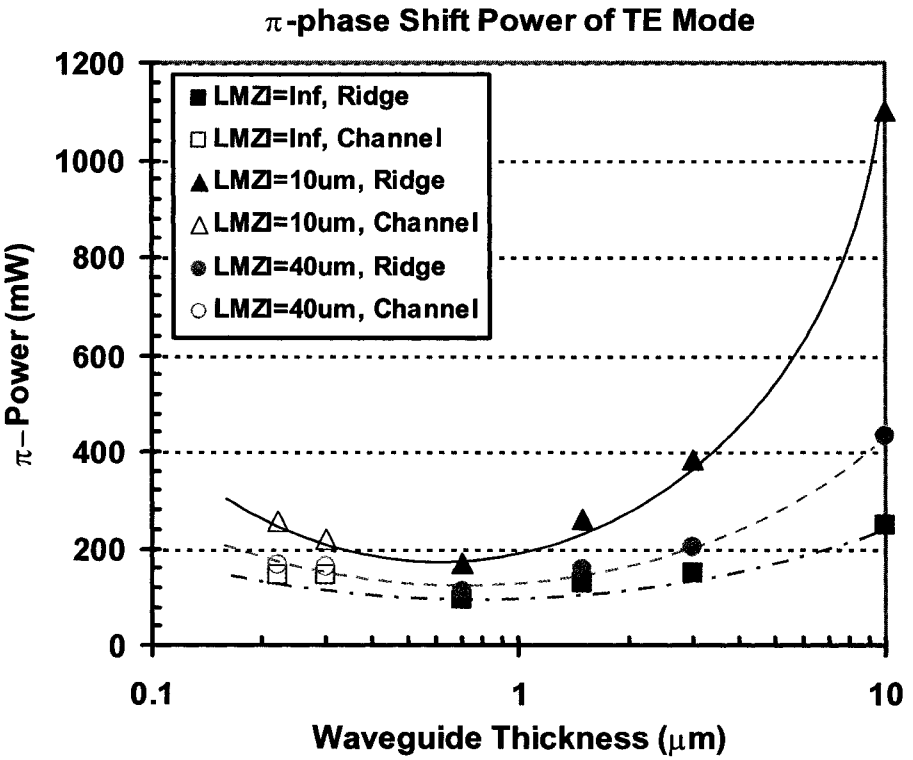



Fig. 5.20. π-power of TE modes as a function of waveguide thickness in various SOI MZI switches with different arm separation. The red solid trend line, pink dotted trend line and blue dash dotted trend line represents MZI with 10 μm, 40 μm and infinite arm spacing, respectively. (*LMZI* denotes arm spacing, *Ridge* denotes ridge waveguides, *Channel* denotes channel waveguides).

From the figures, it is clear that the MZI switches with 10 μm arm spacing consume the most power, while the thermally isolated MZI consumes minimum power. This result confirms that the power consumption of MZI thermo-optic switches reduces with increasing arm spacing. The π-power of a thermally isolated switch technically represents the lower limit of the power requirement.

Although the trend of power-consumption in response to device scaling is consistent for all switches with different arm spacing, the amplitude of power saving with

the reduction in device size varies with the arm spacing. As shown in Fig. 5.20 and 5.21, an 85% saving in power is attainable by reducing the ridge waveguide thickness from 10 to 0.7 μm in a 10 μm-spaced MZI switch. In comparison, 72% of power saving is achieved in the 40 μm-spaced MZI switch and only 60% in a thermally isolated switch. In other words, the difference in π-power due to different arm spacing actually becomes smaller when the ridge waveguide thickness reaches submicron dimension.

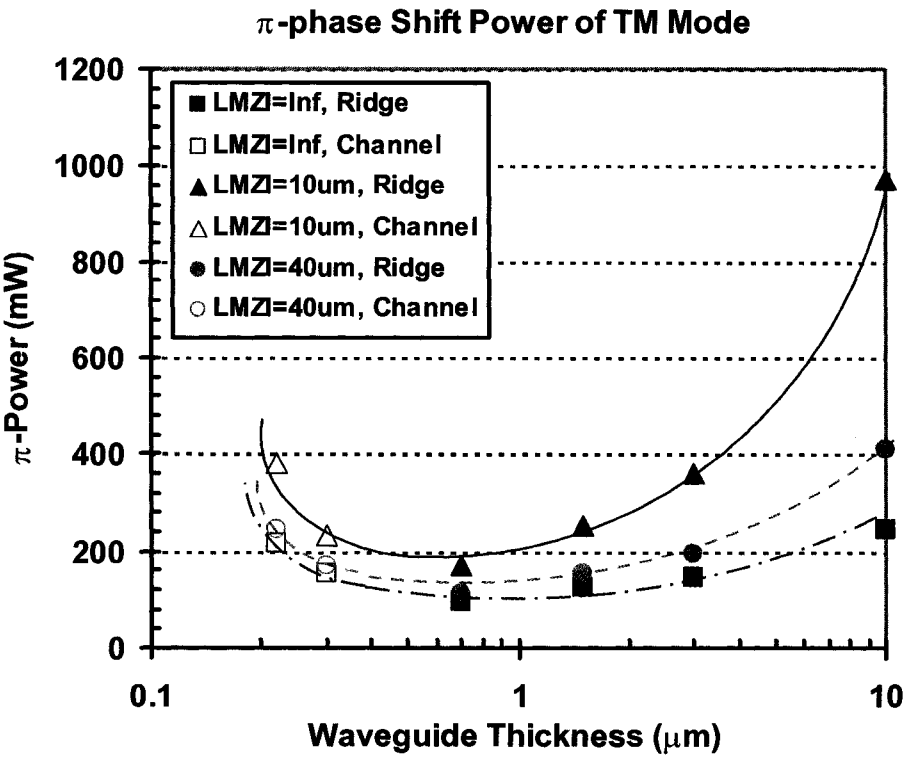



Fig. 5.21. π-power of TM modes as a function of waveguide thickness in various SOI MZI switches with different arm separation. The red solid trend line, pink dotted trend line and blue dash dotted trend line represents MZI with 10 μm, 40 μm and infinite arm spacing, respectively. (*LMZI* denotes arm spacing, *Ridge* denotes ridge waveguides, *Channel* denotes channel waveguides).

Interestingly, while more power saving is achievable by scaling down the size of ridge waveguides in a MZI switch with smaller arm spacing, more power is consumed by scaling down the size of photonic wire waveguides in a similar switch. As shown in Fig. 5.21, the $\pi$-power increases by 63% when the photonic wire waveguide height is reduced from 0.3 to 0.22 μm in a 10 μm-spaced MZI switch, while only 44% increase is observed in a 40 μm-spaced and 42% in a thermally isolated MZI switch.

The temperature distribution of a 0.3 μm photonic wire waveguide of the 40 μm-spaced MZI switch is shown in Fig. 5.22. The temperature distribution in the heated waveguide is identical to the heated waveguide of a 10 μm-spaced MZI switch shown in Fig. 5.11(a). The major difference between the switches is in the temperature distribution in the reference waveguide. The temperature in the reference waveguide of a 40 μm-spaced MZI only increases by less than 2°C, while the peak temperature in a 10 μm-spaced MZI is up by 6°C. This means that when the arms are separated further, the differential temperature between the two arms is larger, leading to a larger phase shift and lower power consumption. The same observation holds for 0.22 μm photonic wire waveguides of a 40 μm-spaced MZI, as shown in Fig. 5.23, and for the larger ridge waveguides.

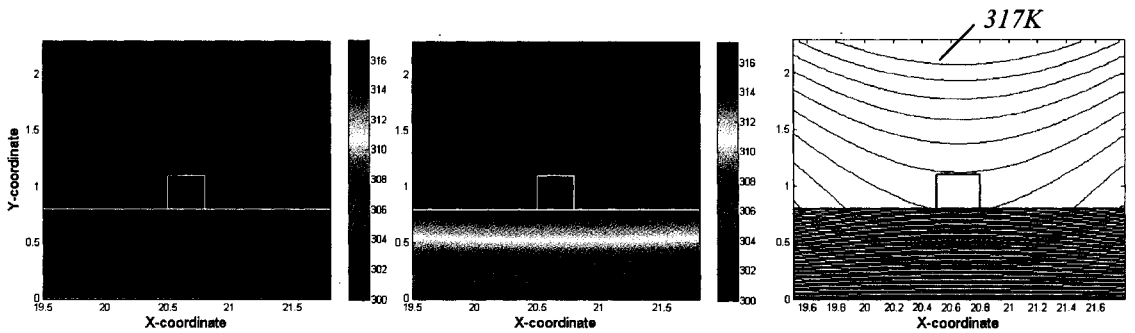



Fig. 5.22. Temperature distribution in a 0.3 μm (a) reference and (b) heated channel waveguide of a 40 μm-spaced MZI heated at 200 mW. (c) A plot of the same heated waveguide showing isothermal lines with an interval of 0.25°C.

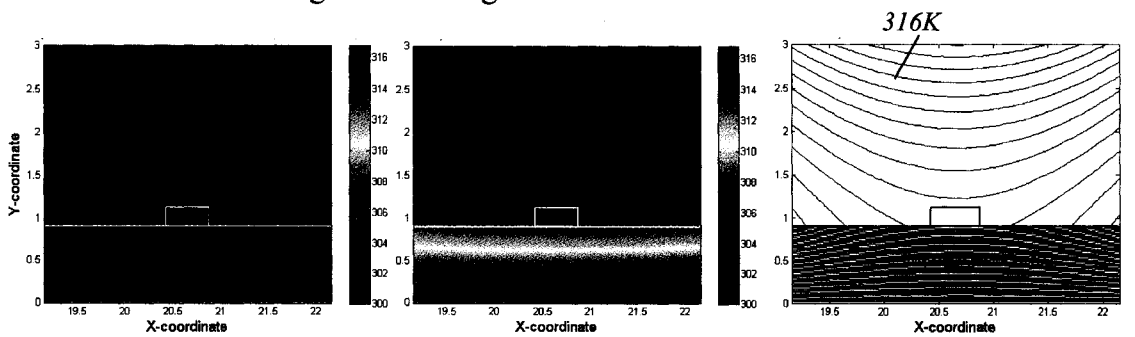



Fig. 5.23. Temperature distribution in a 0.22 μm (a) reference and (b) heated channel waveguide of a 40 μm-spaced MZI heated at 200 mW. (c) A plot of the same heated waveguide showing isothermal lines with an interval of 0.25°C.

The result of these calculations is that arm spacing is another important dimension of device scaling, which has a profound effect on the power of a MZI thermo-optic switch. This gives the designer an additional degree of flexibility in optimizing the performance of the miniaturized devices.

### *5.5.6. Effect of Heater Width*

Heater width is another device parameter to be evaluated in the study of device scaling. The effect of heater width is studied on the 0.22 μm photonic wire waveguide

switches by varying the heater width from 4 to 2 to 1 μm. The simulated temperature contour of a 0.22 μm waveguide having a 4, 2 and 1 μm heater under constant heating power of 200 mW is shown in Fig. 5.24 (a), (b) and (c), respectively. Their corresponding temperature contour line plots are shown in Fig. 5.24(d), (e) and (f).

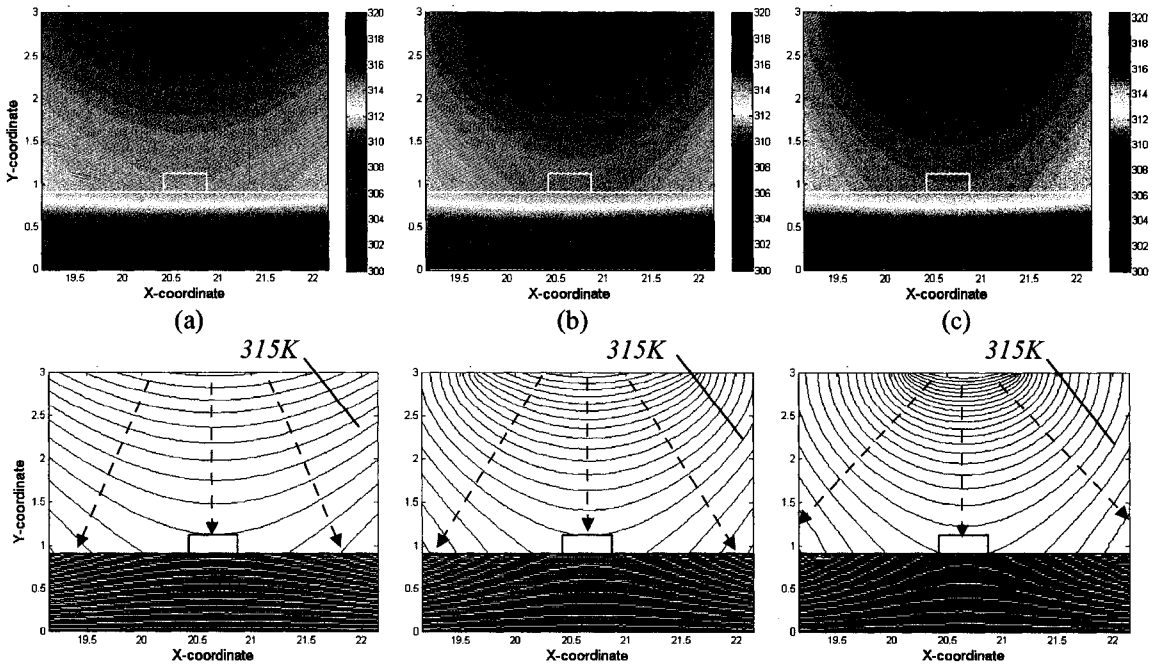
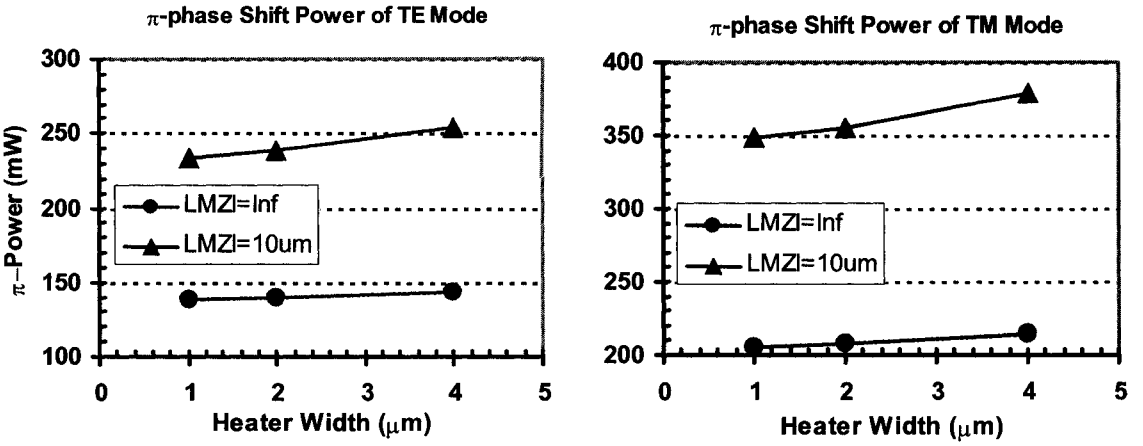



Fig. 5.24. Temperature distribution in a 0.22 μm channel waveguide with a (a) 4, (b) 2 and (c) 1 μm wide heater at an applied power of 200 mW. Their corresponding temperature contour line plots are shown in (d), (e) and (f).

The peak temperature in the cladding increases as the heater width is reduced. At a fixed total input power, a smaller heater will generate more heat per area, yielding an increase in heating efficiency. This results in an increase in the cladding temperature. However, the heat flow pattern also varies with decreasing heater width. As illustrated by the red arrows in Fig. 5.24(f), a small heater radiates heat in the lateral directions in the

same manner as a point source emits light into all directions. The lateral heat increases power consumption as it diffuses away from the waveguide core. Variation in π-power as a function of heater width is shown in Fig. 5.25.




(a) (b)

Fig. 5.25. Variation of π-phase shift power of (a) TE and (b) TM mode as a function of heater width in SOI MZI switches with 0.22 μm photonic wire waveguides. The red triangular data belong to the MZI with 10 μm arm spacing and blue circular data belong to the MZI with infinite arm spacing. (*'LMZI=Inf'* denotes infinite arm spacing, *'LMZI=10um'* denotes arm spacing of 10 μm).

Reducing the heater width from 4 to 1 μm yields only a 10 % power saving for the 10 μm-spaced MZI switches made of 0.22 μm photonic wire waveguides, and does not seem to have any significant impact on the power consumption of a thermally isolated MZI switch. A possible explanation for this observation is the upper cladding may be too thick, thus vertical heating is reduced and more heat is spread laterally, such that the waveguide does not benefit from the improved heating efficiency of the narrower heater. In summary, heater width reduction does not bring significant power saving to photonic wire waveguide switches with thick cladding.

### 5.5.7. *Effect of Cladding Thickness*

In order to quantify the effect of the upper cladding thickness on the rate of increase in π-power, the SiN cladding thickness in the 0.7 μm ridge waveguide is increased from 0.5 to 1.2 and 1.8 μm, while the cladding thickness in the 0.3 μm photonic wire waveguide is increased from 1.2 to 1.8 and 2.4 μm. These two waveguides were chosen since they consumed less power than the other four waveguides.

Figure 5.26 shows the temperature distribution in the 0.7 μm ridge waveguide with 1.2 μm thick SiN cladding, for a 10 μm-spaced MZI switch heated at 200 mW.

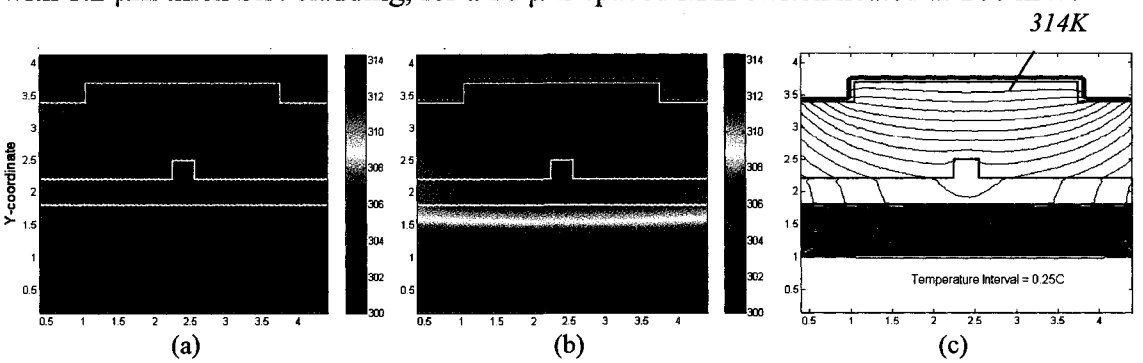



Fig. 5.26. Temperature distribution in the 0.7 μm (a) reference and (b) heated ridge waveguide with 1.2 μm thick SiN cladding of a 10 μm-spaced MZI heated at 200 mW. (c) A plot of the same heated waveguide showing isothermal lines with an interval of 0.25°C.

Table 5.4 π-phase shift power $P_\pi$ of the 10 μm-spaced MZI switches with different SiN cladding thickness.

| *.Waveguide configuration* | *Thickness (μm)* | *Width (μm)* | *Cladding thickness (μm)* | *π-Power of TE mode (mW)* | *π-Power of TM mode (mW)* |
|---|---|---|---|---|---|
| *Ridge* | 0.7 | 0.3 | 0.5 | 168.2 | 168.8 |
| *Ridge* | 0.7 | 0.3 | 1.2 | 207.8 | 205.1 |
| *Ridge* | 0.7 | 0.3 | 1.8 | 247.2 | 245.6 |
| *Channel* | 0.3 | 0.3 | 1.2 | 219.2 | 232.4 |
| *Channel* | 0.3 | 0.3 | 1.8 | 280.9 | 297.9 |
| *Channel* | 0.3 | 0.3 | 2.4 | 346.2 | 367.1 |

As the cladding thickness is increased, so is the width of the cladding on the ridge sidewalls. This causes a two-fold reduction in heating efficiency: a longer distance between the heater and waveguide core which results in the vanishing of sidewall heating, and more heat flow away from the waveguide. The result of increasing cladding thickness from 0.5 to 1.2 μm for the 0.7 μm ridge waveguide is a 24% π-power increment in the TE polarization and a 22% in the TM polarization, for a 10 μm-spaced MZI switch, as summarized in Table 5.4. Further increase in the cladding thickness to 1.8 μm results in a 47% increase in π-power (from the original 0.5 μm thickness), so that the rate of increase of power is linearly proportional to the increase in cladding thickness.

The change in π-power with cladding thickness $dP_\pi/dt_{SiN}$, is shown in Fig. 5.27. Increasing the upper cladding thickness of a 0.3 μm photonic wire waveguide switch results in a linear increase in the π-power of both TE and TM modes. However, compared to the 0.7 μm ridge waveguide, the rate of increase of the π-power with the cladding thickness in the 0.3 μm photonic wire waveguide is approximately 1.8× faster, as indicated by the steeper slopes of the red lines in Fig. 5.27(a) and (b).

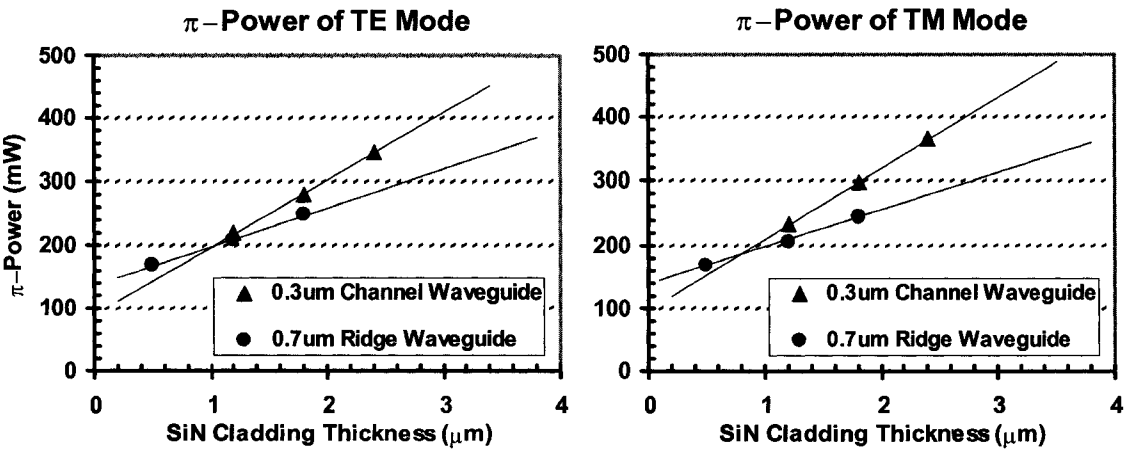



Fig. 5.27. The change in π-power for (a) TE and (b) TM mode as a function of the SiN upper cladding thickness, for a 0.7 μm ridge waveguide and a 0.3 μm channel waveguide.

In order to better characterize the role of cladding thickness as the device scales, it is useful to break down the total change in the π-power with respect to all contributing factors, as summarized in Table 5.5.

Table 5.5 The percentage change in the π-power of the thermo-optic switch as the waveguide is scaled from the 0.7 μm ridge to the 0.3 μm channel waveguide.

| *Contributing Factor* | *Percentage change in π-power of TE mode* | *Percentage change in π-power of TM mode* |
|---|---|---|
| *Cladding Thickness* | 23.5% | 21.5% |
| *Mode size and profile* | 5.5% | 13.5% |
| *Overall Device Scaling* | ~30% | ~37% |

The factors contributing to an increase in the π-power as the MZI switch scales from a 0.7 μm ridge waveguide to a 0.3 μm channel waveguide, are (i) the increase in cladding thickness and the associated change in heat flow pattern, and (ii) the change in mode profile or mode expansion. The change in π-power with simply increasing the

cladding thickness from 0.5 to 1.2 μm in a 0.7 μm ridge waveguide, as mentioned, is 24% for TE mode and 22% for TM mode. With the same cladding thickness, if the waveguide is changed from the 0.7 μm ridge to the 0.3 μm channel, the change of π-power is 5.5% for TE mode and 13.3% for TM mode. When adding up the change in π-power due to these two separate factors, the sum is approximately equal to the calculated overall change. The result indicates that effect of cladding thickness and the associated heat flow accounts for approximately 2/3 of the total increase in power, while the change of mode size and profile accounts for less than or equal to 1/3 of the total increase in power. This conclusion is in good agreement with the result of the analysis of $dN_{eff}/dT$ which is presented in Section *5.5.3*.

### *5.5.8. Optimization of Power from Device Scaling*

In conclusion, photonic device designers have the option to adjust several device parameters in order to achieve low power thermo-optic switching or modulation, as the device size reduces to submicron regime. These important parameters are:

(i) Arm spacing of the MZI switch

(ii) Upper cladding thickness

(iii) Waveguide configuration (ridge versus channel)

(iv) Polarization or waveguide geometrical symmetry

## 5.6. SPEED ANALYSIS : TRANSIENT STATE THERMAL SIMULATION

The π-power of an SOI MZI thermo-optic switch is calculated using the *full mode*

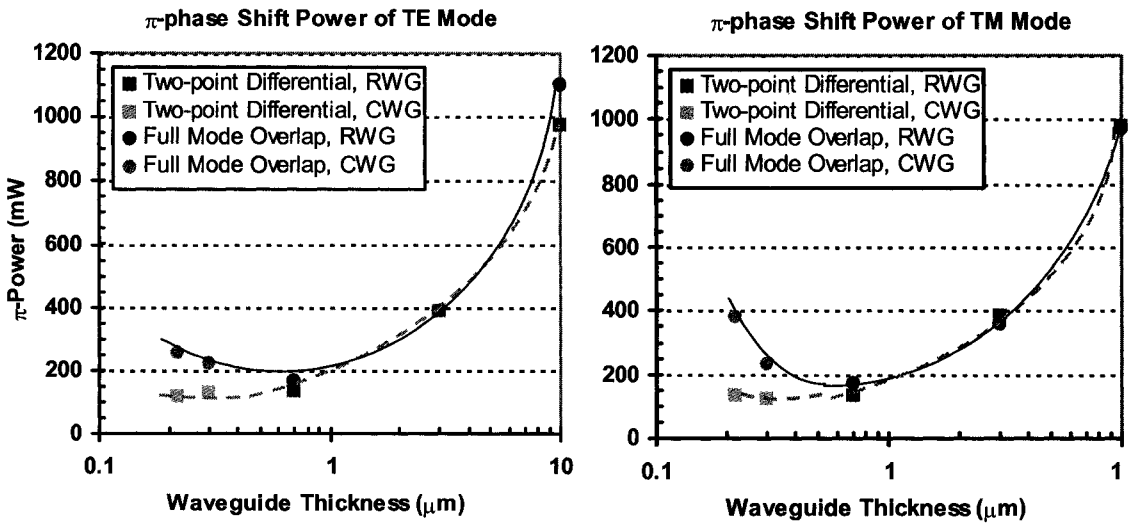
*overlap* method, which requires detailed temperature distribution of the two arms of the MZI switch from steady-state thermal simulation. In the speed analysis, a set of temperature contours of the two MZI arms at different time points has to be collected, so that *full mode overlap* method could be used to determine at which exact time point the change in effective index across the two arms reaches $9.7\times10^{-4}$. This is a rigorous but time consuming method given the vast amount of computational power needed to iterate the calculation over a large number of time points to guarantee calculation accuracy. Simplifying the calculation and reducing computational time are the main objectives in the speed analysis.

### *5.6.1. Comparison of Full Mode Overlap Method with Two-point Differential Method*

A simpler method to replace *full mode overlap* is by calculating the temperature difference between the centre of the heated waveguide core and the reference waveguide core, instead of determining the effective index change. This method, denoted as "*Two-point Differential*" method, has been used extensively in Chapter 4 to derive the $\pi$-phase shift power and to calculate the rise time of the MZI thermo-optic switches containing 1.5 μm wide ridge waveguides. In the derivation of $\pi$-power, we have assumed a uniform temperature distribution across the cores and claddings of the 1.5 μm wide ridge waveguides. Based on this assumption, the change in effective index is simply a function of the change in temperature in the waveguide core, regardless of the mode profile. The phase shift in the switch is also simply a function of the differential temperature across the two waveguide cores. From the phase shift, the $\pi$-power can be easily derived. This

assumption is valid for most ridge waveguides where the guided modes are confined tightly within the core, and in which the core temperature is relatively uniform across the waveguide cross-section. However, when the modes begin to expand into the cladding and a temperature drop is experienced across the cladding layer, this assumption is no longer valid and the accuracy of the calculated power using the *two-point differential* method degrades dramatically.

The variation in TE and TM π-power with respect to decreasing waveguide dimension, derived using the *two-point differential* method, is shown in Fig. 5.28. The π-power is calculated for the 10 μm-spaced MZI switches. For comparison, π-power calculated using the more rigorous *full mode overlap* method is also included in the figure.




(a) (b)

Fig. 5.28. Comparison of (a) TE and (b) TM π-power as a function of waveguide thickness in 10 μm-spaced SOI MZI switches, calculated using *full mode overlap* (black solid line) and *two-point differential* (dotted gray line) method. (*RWG*: Ridge waveguide, *CWG*: Channel waveguide).

As expected, significant discrepancies exist between the results obtained from the two different methods, particularly for the photonic wire waveguides. The *two-point differential* method clearly underestimates the power requirement for the two photonic wire waveguide switches having waveguide height of 0.3 and 0.22 μm, as shown in Fig. 5.28. This underestimation changes the trend of the power-waveguide dimension plot entirely and leads to erroneous conclusion. Comparison on the thermally isolated MZI switches shows exactly the same underestimation. This explains why *full mode overlap* method has to be used to determine π-power accurately in the study of device scaling.

While the *two-point differential* method does not provide a precise measure to the power analysis of the thermo-optic switch, we have found its accuracy and usefulness in the speed analysis. The explanation is based on a simple fact that time taken for the differential effective index of two MZI arms to stabilize, should equal the time taken for any two points in the two arms to reach thermal equilibrium. The two points are for example, the center of the core of the heated arm and the center of the core of the reference arm. The time taken to reach the thermal equilibrium is basically the rise time of the thermo-optic switch.

To verify this theory, we calculate the rise time of our switches containing large ridge waveguides as well as small channel waveguides using these two methods. The two methods give exactly identical results. For example, the rise time of a switch containing 3 μm thick ridge waveguides is plotted in Fig. 5.29.

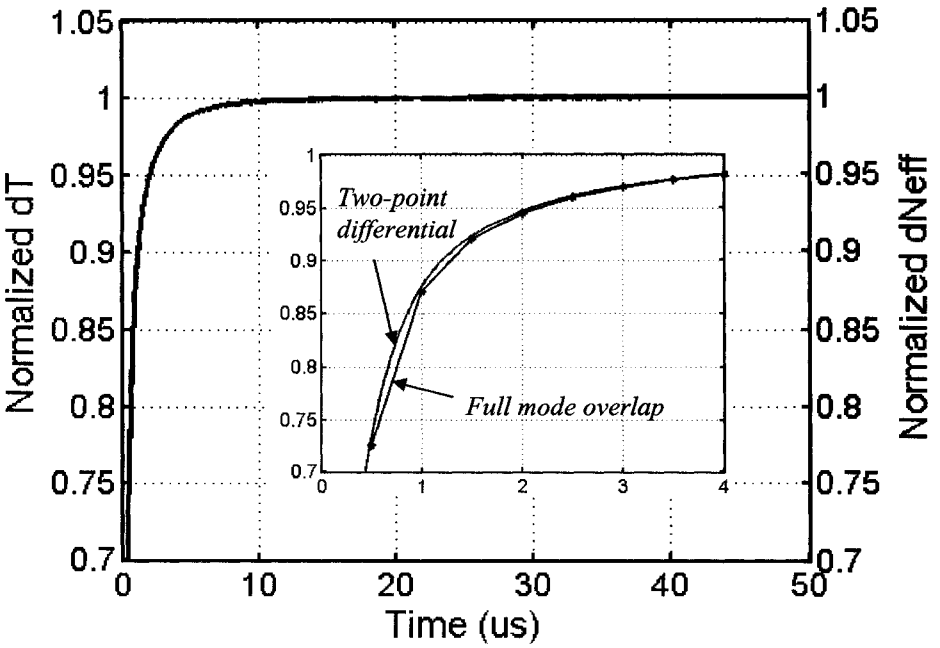



Fig. 5.29. Comparison of the rise time of a 3 μm ridge waveguide MZI switch, calculated using *two-point differential* (red line) and *full mode overlap* (black line) method. The inset shows the expanded view of the two curves at the initial time interval of 4 μs.

In Fig. 5.29, red line represents the normalized differential temperature *dT*, between two MZI arms of the switch, while the black line represents the normalized differential effective index, $dN_{eff}$. The differential temperature is calculated by the *two-point differential* method while the differential effective index is calculated by the *full mode overlap* method. Both quantities are plotted with respect to the turn-on time of the heating pulse. The two lines overlay each other perfectly.

### *5.6.2. Effect of Device Scaling and Mode Expansion on Rise Time*

The rise time of all six switches is determined from the plots of differential temperature versus heating time, as shown in Fig. 5.30 (a) and (b).

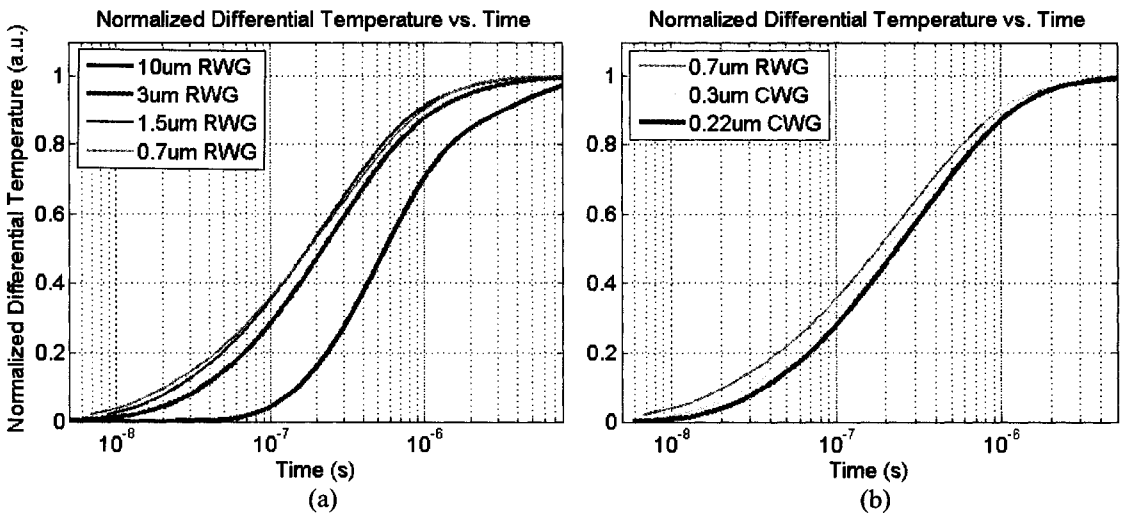



Fig. 5.30. The plot of the differential temperature versus the time after heater power is switched on, for the 10 μm-spaced MZI switches that consist of (a) ridge waveguides and (b) channel waveguides. (*RWG* denotes ridge waveguides, *CWG* denotes channel waveguides).

In these figures, the differential temperature between the two cores is normalized by its peak value and plotted in semi-log scale. The $x$-axis is the turn-on time of the heating pulse. The pulse is assumed to be turned on at $t = 0$, and have a step function response. Two specifications are adopted to determine the rise time of each switch. The time taken for the differential temperature to reach 99% of its maximum value is known as the "full rise time", while the duration for the differential temperature to rise to 90% of its maximum value is known as "90% rise time". Depending on the specification, the calculated rise time can differ greatly, but the overall trend with respect to the reduction in waveguide dimension remains in agreement. In our analysis, we adopt the full rise time specification because it represents a complete phase of switching.

Table 5.6 summarizes the calculated rise time of six MZI thermo-optic switches

with a common arm spacing of 10 μm, when heated at their corresponding π-power.

Table 5.6 Rise time of the SOI MZI switches with arm spacing of 10 μm.

| *Waveguide configuration* | *Thickness (μm)* | *Power (mW)* | *Full Rise Time (μs)* | *90% Rise Time (μs)* |
|---|---|---|---|---|
| *Ridge* | 10 | 1103.1 | 25 | 3 |
| *Ridge* | 3 | 385.3 | 7 | 1.2 |
| *Ridge* | 1.5 | 258 | 4 | 0.9 |
| *Ridge* | 0.7 | 168.2 | 3 | 0.9 |
| *Channel* | 0.3 | 219.2 | 4 | 1 |
| *Channel* | 0.22 | 253.8 | 5 | 1.2 |

The full rise time summarized in Table 5.6 can be plotted with respect to the waveguide thickness to illustrate the effect of device scaling on the speed of the thermo-optic switches, as shown in Fig. 5.31.

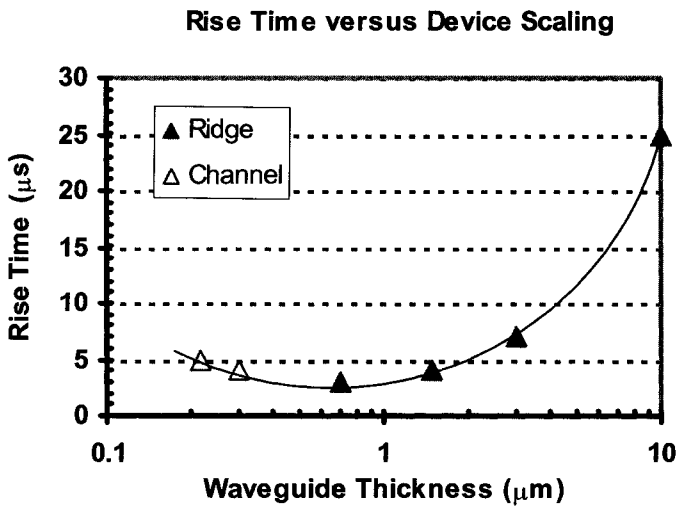



Fig. 5.31. The variation in full rise time of the 10 μm-spaced MZI switches as a function of the waveguide thickness. (*Ridge* denotes ridge waveguides, *Channel* denotes channel waveguides).

It is clear that the switch with the largest ridge waveguide has the slowest speed, requiring the longest rise time of 25 μs. Scaling the waveguide thickness down to 3 μm

improves the rise time to 7 μs. Further reduction in the waveguide dimension to 0.7 μm brings the rise time down to 3 μs, which is equivalent to a speed gain of more than 8× from the 10 μm ridge waveguide.

When the waveguide configuration changes from ridge to channel waveguide of 0.3 μm, the rise time of the MZI switch is increased to 4 μs. As shown in Fig. 5.30(b), at the initial phase of heating (within the first 100 ns), the differential temperature in the channel waveguide actually rises slower than in the ridge waveguide. This may be attributed to the lack of Si slab layer to facilitate heat flow, and the thicker SiN cladding thickness in the channel waveguide (1.2 μm compared to 0.5 μm in the ridge waveguide), which translates into a longer heat conduction path. As the waveguide core layer thickness is reduced further to 0.22 μm, the upper cladding thickness is increased to 1.9 μm and the rise time increases accordingly to 5 μs.

In conclusion, the variation in switching speed with respect to device scaling follows a similar trend as the variation in power. Reduction in the thickness of ridge waveguides results in mode compression and speed gain, while reduction in the width and height of photonic wire waveguides results in mode expansion and thickening of upper cladding thickness, leading to a speed reduction.

### *5.6.3. Effect of Arm Spacing*

A longer heat conduction path due to a larger MZI arm spacing will decrease the differential temperature between the arms and increase the rise time of a thermo-optic

switch. Compared to the 10 μm-spaced MZI, the rise time of 40 μm-spaced MZI switches is significantly larger, as illustrated in Table 5.7 and Fig. 5.32.

Table 5.7 Rise time of the SOI MZI switches with arm spacing of 40 μm.

| *Waveguide configuration* | *Thickness (μm)* | *Power (mW)* | *Full Rise Time (μs)* | *90% Rise Time (μs)* |
|---|---|---|---|---|
| *Ridge* | 10 | 431.1 | 50 | 9.5 |
| *Ridge* | 3 | 200.9 | 34 | 4 |
| *Ridge* | 1.5 | 152.9 | 25 | 2.5 |
| *Ridge* | 0.7 | 112.0 | 18 | 2.1 |
| *Channel* | 0.3 | 170.6 | 19 | 1.8 |
| *Channel* | 0.22 | 245.8 | 23 | 2.7 |

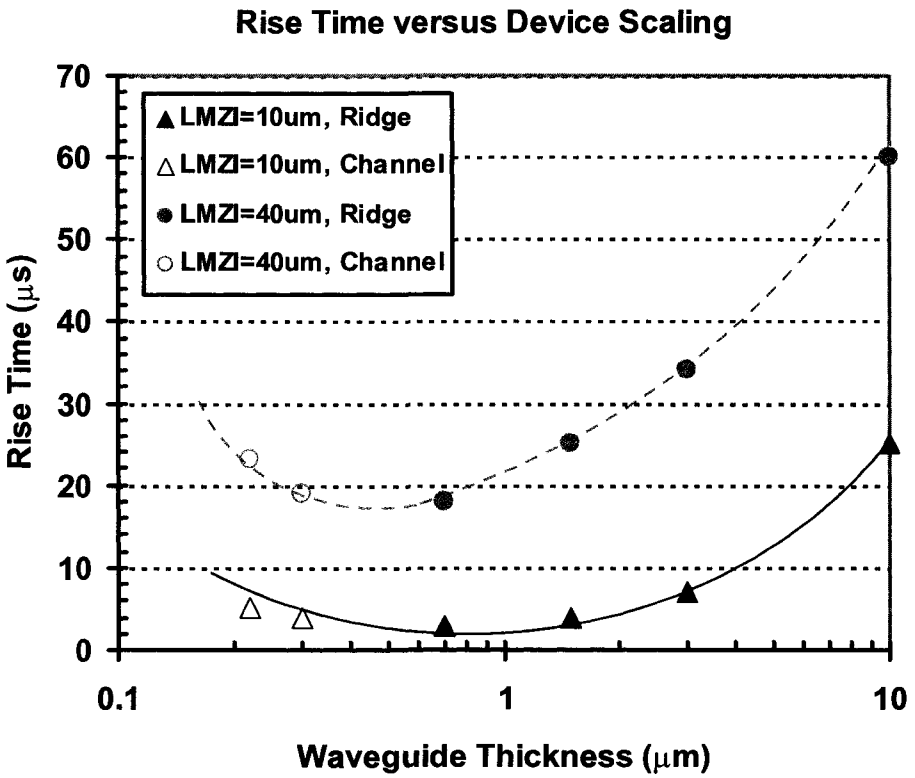



Fig. 5.32. The variation in rise time as a function of waveguide thickness in various SOI MZI switches with different arm separation. The triangles represent the data for switches with 10 μm arm spacing, while the circular dots represent the data for switches with 40 μm arm spacing. (*LMZI* denotes arm spacing, *Ridge* denotes ridge waveguides, *Channel* denotes channel waveguides).

As shown in Fig. 5.32, the full rise time of a 40 μm-spaced MZI switch made of the 10 μm ridge waveguides is calculated to be 50 μs, which is twice the rise time of an equivalent 10 μm-spaced MZI switch. Although the rise time decreases with decreasing ridge waveguide dimension, the minimum rise time achievable at the width of 0.7 μm is at best 18 μs. Compared to the 3 μs rise time achieved by the switch with 10 μm arm spacing, this 4× increase in arm spacing actually results in a 6× speed reduction. Thermo-optic switch designers will have to be aware of this speed tradeoff when attempting to reduce the power consumption by increasing the MZI arm spacing.

On the other hand, the rise time of a 0.3 μm photonic wire waveguide switch is again slightly longer than the 0.7 μm ridge waveguide, calculated to be 19 μs. As the photonic wire waveguide dimension is reduced further to 0.22 μm, the rise time increases to 23 μs. This is in agreement with the trend in rise time observed on the 10 μm-spaced MZI switches. The effect of the change in cladding thickness is expected to diminish as the arm spacing increases to several orders of magnitude larger than the upper cladding thickness. At that geometry, the limiting step in the rise time of the thermo-optic switch will be the heat conduction rate from one arm to the other, instead of the vertical heat conduction rate from the heater to the waveguide core.

### *5.6.4. Effect of Heater Width*

The effect of heater width on the speed is studied on the 0.22 μm photonic wire waveguides by varying the width from 4, 2 to 1 μm. Fig. 5.33 shows the rise time of the

10 μm-spaced MZI switches with varying heater width. As illustrated in Fig. 5.24 in Section *5.5.6*, reducing the heater width in a channel waveguide will enhance the heating efficiency by increasing the amount of generated heat per unit area. This expedites the rate of heating in the heated MZI arm. Meanwhile, a smaller heater radiates more lateral heat, which in turns expedites the heat conduction to the reference arm. These two effects combine to give a small speed improvement to the switch with narrower heater.

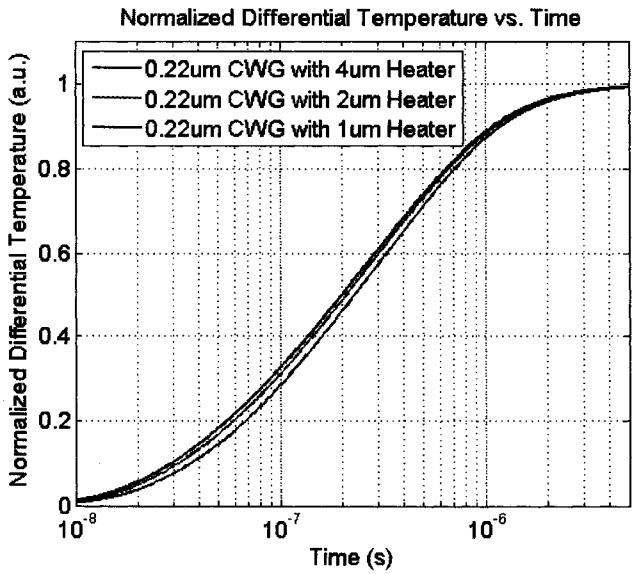



Fig. 5.33. The plot of differential temperature versus the time after heater power is switched on, for the MZI switches that consist of 0.22 μm channel waveguides with varying heater width. (*CWG*: channel waveguide).

As shown in Fig. 5.33, although there is an improvement in the rise time of the switch, the heater width effect is relatively weak compared to the effect of arm spacing reduction. To enhance this effect, both arm spacing and heater width will have to be at a comparable dimensional scale. This condition is difficult to achieve in reality because mode coupling will occur when the arm spacing is reduced to less than a micron.

### *5.6.5. Effect of Cladding Thickness*

In order to study the effect of cladding thickness on the speed of the miniaturized thermo-optic switch, the SiN thickness in a 0.7 μm ridge waveguide has been varied from 0.5 to 1.2 μm. The simulated rise time of the switches with the varying SiN thickness is shown in Fig. 5.34.

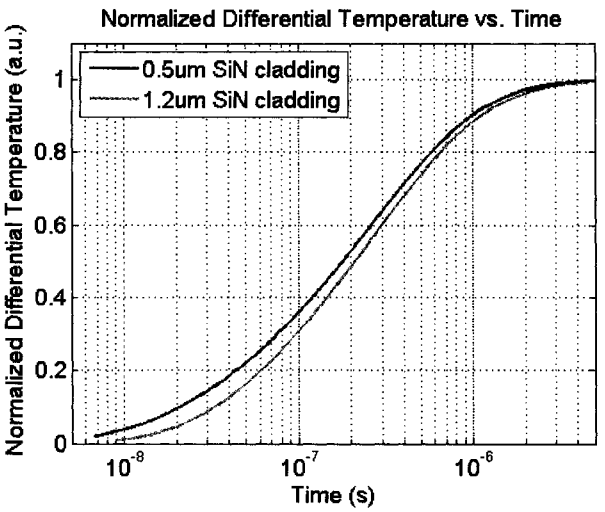



Fig. 5.34. The plot of the differential temperature versus the time after heater power is switched on, for the MZI switches that consist of 0.7 μm ridge waveguides with varying SiN cladding thickness.

There is clearly an additional initial delay in the rise of differential temperature when the cladding thickness is increased from 0.5 to 1.2 μm. However, this delay only translates to a 1 μs increment in rise time, suggesting the effect of SiN cladding thickness on switching speed is secondary to the effect of core size or arm spacing reduction.

### *5.6.6. Optimization of Speed from Device Scaling*

The critical device parameters which affect the speed of the SOI MZI thermo-optic switches in submicron regime are those that will cause significant changes to the mode size, mode field distribution and local thermal gradient. By adjusting these parameters, optimization of the speed can be achieved:

(i) Waveguide core: compressing the mode size by shrinking waveguide core will improve speed (as $f_g$ increases with decreasing $\Delta x^2$, given by Equation (4.21))

(ii) Waveguide configuration: minimizing mode expansion into cladding by forming ridge waveguide will reduce cladding thickness and improve heat flow, therefore will improve speed (as $f_g$ increases with decreasing $\Delta x^2$ and increasing $\sigma$)

(iii) Arm spacing: reducing heat conduction path by reducing arm spacing will improve speed

(iv) Upper cladding thickness: reducing heat conduction path by thinning the upper cladding layer will improve speed (again $f_g$ increases with decreasing $\Delta x^2$)

## 5.7. SUMMARY

In this chapter, a number of original findings regarding the effect of device scaling on the power and speed of SOI MZI thermo-optic switches are presented. The need for photonic wire waveguides to realize compact photonic devices is addressed and the important properties of photonic wire waveguides are elaborated. In order to study the effect of scaling, six different waveguides, starting with the largest 10 μm ridge

waveguides to the smallest 0.22 μm photonic wire waveguides are investigated. The optical mode field profiles and temperature contours of all six waveguides were simulated and were used to determine the π-power and rise time of the MZI switches.

Power consumption of a MZI thermo-optic switch can be reduced by compressing the mode through shrinking the size of ridge waveguides, while power can be increased as a result of mode expansion through shrinking the size of photonic wire waveguides. A list of key parameters that will allow for optimization of power, including arm spacing, cladding thickness, waveguide configuration and polarization is provided, and their respective effects are explained.

The trend of switching speed with respect to device scaling is also presented and mode expansion is shown to have an adverse effect on the speed by causing an increase in the upper cladding thickness. Finally, some options to improve the speed of miniaturized thermo-optic switches that are made of photonic wire waveguides are suggested.

# CHAPTER 6

# CONCLUSIONS AND RECOMMENDATIONS

The result of this research will contribute to the understanding of several critical technical challenges, in the development of a silicon photonic integrated chip and their solutions. These challenges include coupling light in and out of the photonic chip, guiding and propagating light in SOI waveguides with low roughness and scattering loss, as well as modulating light with an effective actuation mechanism that is well understood and reliable. In the course of understanding and addressing these challenges, a number of passive and active devices and test structures have been designed, fabricated, and characterized. These SOI devices not only are the test vehicles in the study of coupling loss, scattering loss and thermo-optic effect, but are also elements of an expandable photonic chip that can be further integrated with microelectronic circuits.

The primary contributions of this research are:

1. A successful development of a lithographically-defined facet fabrication technique employing ICP etching process to fabricate the required facets with optical quality on an SOI photonic chip. This technique eliminates the need of polishing while offering a placement accuracy of ±1 μm for the facets at any location within the chip. This facilitates the incorporation of specialized low-loss couplers and mode converters on

chip, that are needed to couple light in and out of the chip effectively.

2. The experimental demonstration of a novel non-destructive technique to measure the sidewall roughness induced scattering losses of SOI ridge waveguides using integrated optical star couplers. To the best knowledge of the author, this is the first demonstration of a measurement technique capable of determining losses of multiple waveguides of different width in a single measurement step. The measurement technique using star couplers overcomes the drawbacks of the conventional cutback method and Fabry-Perot method because its accuracy is independent of the coupling efficiency and consistency in the quality of the input facets. This technique allows the collection of sufficient loss data to provide useful feedback for improving fabrication process to reduce scattering loss.
3. The development of a robust low-loss SOI waveguide fabrication process, utilizing a Cr hardmask layer to reduce waveguide sidewall roughness, which is produced during patterning and etching steps. By optimizing the Cr etch recipe, a smooth sidewall profile is transferred from the Cr hardmask to the SOI waveguides. The final roughness on the sidewalls of SOI waveguides achieved by the optimized Cr hardmask process is around 3 nm.
4. A comprehensive simulation study on the critical parameters that affect the performance of MZI-based SOI thermo-optic switches, including cladding material, cladding layer thickness, MZI arm spacing and heater width. The simulation gives a quantitative measure of the effect of each parameter in terms of the switching speed and power, which can guide the optimization of SOI MZI thermo-optic switch design.

It is shown that by reducing MZI arm spacing from 100 μm to 10 μm, a switching speed improvement of at least an order of magnitude can be achieved. The author is also the first to propose the use of SiN as the upper cladding layer of the SOI waveguides to improve the speed of thermo-optic switches.

5. The effects of device scaling on the performance of SOI MZI thermo-optic switches are studied through optical and thermal simulation. Mode compression and mode expansion as a result of device scaling are shown to have significant impact on the power consumption and speed of various SOI thermo-optic switches based on ridge waveguides and photonic-wire waveguides. A significant power saving is achieved by shrinking the ridge waveguide width of the MZI thermo-optic switch, especially when the MZI arms are closely spaced. However, an increase in power of the switch is observed when the waveguide configuration is changed from ridge to channel waveguide and the waveguide thickness is reduced to 0.3 μm or below. This increase in power is due to the required increase in cladding thickness as a result of mode expansion. Similarly, an increase in the speed of a thermo-optic switch is achieved by scaling the waveguides, especially when the MZI arms are far apart. The change in waveguide configuration from a ridge to a channel waveguide results in a decrease in speed. The results from this study give the designers an insight to the tradeoffs in power and speed when various device parameters are adjusted, as the device is scaled down to submicron dimensions. This understanding will allow the designers to optimize the performance of more compact devices for larger scale integration.

These research results contribute toward the development and manufacturability of an integrated SOI photonic chip, by improving the input and output interfaces for coupling, straight and curved waveguides with low scattering loss, as well as a fully functional thermo-optic module that comes with a set of design and optimization guidelines.

In the future, it would be useful to extend this research in the following directions:

1. Circuit level implementation of low-power SOI thermo-optic switch matrices or optical add-drop multiplexers. The design of these switch matrices or multiplexers can benefit from the power and speed analysis of an individual switch at the component level.
2. Development of new fabrication schemes for low-loss SOI waveguides in compact photonic chips. As the scale of integration increases, optical loss requirement becomes increasingly more stringent. Development of processes that can produce smooth waveguide sidewalls (with roughness $\leq$ 1 nm) and low scattering loss is essential. In particular, improving the pattern transfer process of projection lithography which is capable of producing large scale integration appears to be an important aspect for future research. In the evaluation of new fabrication schemes, the star coupler loss measurement technique can be an effective approach to collect loss data quickly. One example would be using the star couplers to evaluate *LOCOS* waveguide fabrication scheme proposed by G. Tarr *et al.* [3.25].

# Appendix A

# Payne-Lacey Scattering Loss Equation

Payne and Lacey have evaluated the dependence of the scattering loss on the surface roughness characteristics of the waveguide using both autocorrelation functions, and have arrived at a closed-form analytical expression [3.7]:

$$\alpha = 4.34 \frac{\sigma^2}{\sqrt{2} k_o d^4 n_1} g \cdot f \tag{A.1}$$

where $\alpha$ is the scattering loss, $k_o$, $d$ and $n_1$ are the free-space wave number, the waveguide half width, and the core index, respectively. $g$ is determined purely by the waveguide geometry:

$$g = \frac{U^2 V^2}{(1+W)} \tag{A.2}$$

$U$, $V$ and $W$ are given by:

$$U = d\sqrt{n_1^2 k_o^2 - \beta^2} \tag{A.3}$$

$$V = k_o d\sqrt{n_1^2 - n_2^2} \tag{A.4}$$

$$W = d\sqrt{\beta^2 - n_2^2 k_o^2} \tag{A.5}$$

$\beta$ is the propagation constant and $n_2$ is the refractive index of the cladding layer. $f$ is determined by the autocorrelation length and function, as well as the index step of the

waveguide. For the exponential autocorrelation function,

$$f = \frac{x\left\{\left[(1+x^2)^2 + 2x^2\gamma^2\right]^{1/2} + 1 - x^2\right\}^{1/2}}{\left\{(1+x^2)^2 + 2x^2\gamma^2\right\}^{1/2}} \tag{A.6}$$

where

$$x = W\frac{L_c}{d} \tag{A.7}$$

$$\gamma = \frac{n_2 V}{n_1 W\sqrt{\Delta}} \tag{A.8}$$

$$\Delta = \frac{n_1^2 - n_2^2}{2n_1^2} \tag{A.9}$$

For the Gaussian autocorrelation function,

$$f = \frac{x}{\sqrt{2\pi}}\int_0^{\pi} \exp\left\{-\frac{x^2}{4}\left[(1+\frac{\gamma^2}{2})^{1/2} - \frac{\gamma}{\sqrt{2}}\cos\theta\right]^2\right\} d\theta \tag{A.10}$$

where $\theta$ is the scattering angle.

# References


1.1. B. E. A. Saleh, M. C. Teich, *Fundamental of Photonics*, Wiley, New York (1991).

1.2. L. Pavesi and D. J. Lockwood, *Silicon Photonics*, Springer-Verlag, Berlin (2004).

1.3. G. T. Reed, A. P. Knights, *Silicon Photonics*, John Wiley & Sons Ltd., England (2004).

1.4. Mario Paniccia (Intel, presentation), "The future of photonics -- is silicon the answer?" *Nature Photonics Techn. Conf. on Opt. Comm.*, October 23-25, Tokyo, Japan, 2007.

1.5. R. Soref, "The past, present, and future of silicon photonics," *IEEE J. Sel. Top. Quant. Elec.*, vol. 12, no. 6, pp. 1678-1687 (2006).

1.6. B. Jalali and S. Fartpour, "Silicon photonics," *IEEE J. Light. Tech.*, vol. 24, no. 12, pp. 4600-4615 (2006).

1.7. Optoelectronics Industry Development Association, "OIDA releases new green photonics market data", Washington, DC, February 2009. *http://www.oida.org/news/oida-news/2009/377.*

1.8. Merging Optics and Nanotechnologies (MONA), "A European roadmap for photonics and nanotechnologies," *http://www.ist-mona.org.*

1.9. Thomas L. Friedman, *The World Is Flat: a Brief History of the Twenty-first Century*, Douglas and McIntyre Ltd., Canada (2007).

1.10. R. Baets *et al.*, "Silicon photonics," *IEEE Int. Sym. VLSI-TSA 2007*, pp. 1-3, April 2007.

1.11. Konstantin K. Svidzinskiy, "Silicon-based optical integrated circuits for terabit-rate optical networks," *Microelec. Eng.*, vol. 69, pp. 221-227 (2003).

1.12. S. Janz, P. Cheben, A. Delâge, A. Densmore, B. Lamontagne, E. Post, J. Schmid, P. Waldron, D.-X. Xu, K. P. Yap, and W. N. Ye, "Silicon Microphotonic waveguide technology for sensing, spectroscopy and communication," *ECS transaction: Science and Technology of Dielectrics for Active and Passive Photonic Devices*, vol. 3, no.11, pp. 61-78 (2006).

1.13. B. Jalali, S. Yegnanarayanan, T. Yoon, T. Yosuimoto, I. Rendina, and F. Coppinger, "Advances in silicon-on-insulator optoelectronics," *IEEE J. Sel. Top. Quant. Elec.*, vol. 4, no. 6, pp. 938-947 (1998).

1.14. S. Janz *et al.*, "Microphotonic elements for integration on the silicon-on-insulator waveguide platform," *IEEE J. Sel. Top. Quant. Elec.*, vol. 12, no. 6, pp. 1402-1415 (2008).

1.15. S. Janz, "Photonics and food: food and water safety," Photonics Spectra, issue March, pp. 55-57 (2008).

1.16. S. O. Kasap, *Optoelectronics and Photonics*, Prentice-Hall Inc., United States (2001).

1.17. L. M. Giovane, L. Liao, D. R. Lim, A. M. Agarwal, E. A. Fitzgerald, and L. C. Kimerling, "$Si_{0.5}Ge_{0.5}$ relaxed buffer photodetectors and low-loss polycrystalline silicon waveguides for integrated optical interconnects at $\lambda = 1.3$ μm," in *Proc. of SPIE, San Jose, 1997,* vol. 3007, pp. 74-78 (1997).

1.18. F. Y. Huang, K. Sakamoto, K. L. Wang, and B. Jalali, "Epitaxial SiGeC waveguide photodetector grown on Si substrate with response in the 1.3-1.55 μm wavelength range," *IEEE Photon. Tech. Lett.,* vol. 9, pp. 229-231 (1997).

1.19. A. Liu, R. Jones, L. Liao, D. Samara Rubio, D. Rubin, O. Cohen, R. Nicolaescu, and M. Paniccia, "A high-speed silicon optical modulator based on a metal-oxide-semiconductor capacitor," *Nature*, vol. 427, pp. 615-618 (2004).

1.20. C. Gunn, "CMOs photonics—SOI learns a new trick," *Proc. of IEEE. Int. Silicon-on-Insulator (SOI) Conf.*, Oct. 3–6, 2005, pp. 7–13 (2005).

1.21. G. P. Agrawal, *Lightwave Technology: Components and Devices*, John Wiley & Sons Ltd., United States of America (2004).

1.22. K. P. Yap, A. Delâge, B. Lamontagne, S. Janz, D.-X. Xu, J. Lapointe, P. Waldron, J. Schmid, P. Chow-Chong, E. Post, B. Syrett, "Scattering loss measurement of SOI waveguides using 5×17 integrated optical star coupler," in *Proc. of SPIE Photonics West 2007*, vol. 6477, pp. 64770J1-11 (2007).

1.23. D. -X. Xu, P. Cheben, D. Dalacu, A. Delâge, S. Janz, B. Lamontagne, M. –J. Picard, and W. N. Ye, "Eliminating the birefringence in silicon-on-insulator ridge waveguides by use of cladding stress," *Opt. Lett.*, vol. 29, no. 20, pp. 2384-2386 (2004).

1.24. W. N. Ye, D. -X. Xu, S. Janz, P. Cheben, M. –J. Picard, B. Lamontagne, and N. G. Tarr, "Birefringence control using stress engineering in silicon-on-insulator (SOI) waveguides," *IEEE J. Lightwave Tech.*, vol. 23, no. 3, pp. 1308-1318 (2005).

2.1. G. T. Reed, A. P. Knights, *Silicon Photonics*, John Wiley & Sons Ltd., England (2004).

2.2. L. Pavesi and D. J. Lockwood, *Silicon Photonics*, Springer-Verlag, Berlin (2004).

2.3. K. K. Lee, D. R. Lim, D. Pan, C. Hoepfner, W. Oh, K. Wada, L. C. Kimerling, K. P. Yap, and M. T. Doan, "Mode transformer for miniaturized optical circuits," *Opt. Lett.*, vol. 30, no. 5, pp. 498-500 (2005).

2.4. T. Tsuchizawa, T. Watanabe, E. Tamechika, T. Shoji, K. Yamada, J. Takahashi, S. Uchiyama, S. Itabashi, and H. Morita, "Fabrication and evaluation of submicron-square Si wire waveguides with spot size converters," in *Proc. of the 15th Annual Meeting of the IEEE Lasers and Electro-Optics Society,* pp. 287-288, Piscataway, N.J. 2002.

2.5. T. Shoji, T. Tsuchizawa, T. Watanabe, K. Yamada, and H. Morita, "Spot-size converter for low-loss coupling between 0.3μm-square Si wire waveguides and single-mode fibers," in *Proc. of the 15th Annual Meeting of the IEEE Lasers and Electro-Optics Society,* pp. 289-290, Piscataway, N.J. 2002.

2.6. V. R. Almeida, R. R. Panepucci, and M. Lipson, "Nanotaper for compact mode conversion," *Opt. Lett.*, vol. 28, no. 15, pp. 1302-1304 (2003).

2.7. G. Z. Masanovic, V. M. N. Passaro, and G. T. Reed, "Dual grating-assisted directional coupling between fibers and thin semiconductor waveguides," *IEEE Photon. Technol. Lett.*, vol. 15, pp. 1395-1397 (2003).

2.8. A. Sure, T. Dilton, J. Murakowski, C. Lin, D. Pustai, and D. Prather, "Fabrication and characterization of three-dimensional silicon tapers," *Opt. Express*, vol. 11, pp. 3555-3561 (2003).

2.9. C. Manolatou, and H. A. Haus, *Passive components for Dense Optical Integration*, Kluwar Academic Publishers, Boston (2002).

2.10. K. Shiraishi, C. S. Tsai, H. Yoda, and K. Minagawa, "A micro-GRIN slab tip for integrating coupling between superfine-core waveguides and single mode fibers," in *Proc. of CLEO/Pacific RIM 2003*, CD-ROM (Institute of Electrical and Electronics Engineers, Piscataway, NJ, 2003).

2.11. K. Shiraishi and C. S. Tsai, "A micro light-beam spot-size converter using a hemicylindrical GRIN-slab tip with high-index contrast," *IEEE J. Light. Tech.*, vol. 23, no. 11, pp. 3821-3826 (2005).

2.12. A. Delâge, S. Janz, B. Lamontagne, A. Bogdanov, D. Dalacu, D. –X. Xu, K. P. Yap, "Monolithically integrated asymmetric graded and step-index couplers for microphotonic waveguides," *Opt. Express*, vol. 14, no. 1, pp. 148-161 (2006).

2.13. A. Delâge, S. Janz, D. –X. Xu, D. Dalacu, B. Lamontagne, and A. Bogdanov, "Graded-index coupler for microphotonic SOI waveguides," in *Proc. of SPIE Photonics North 2004*, vol. 5577, pp. 204-212 (2004).

2.14. B. Jalali, S. Yegnanarayanan, T. Yoon, T. Yosuimoto, I. Rendina, and F. Coppinger, "Advances in silicon-on-insulator optoelectronics," *IEEE J. Sel. Top. Quant. Elec.*, vol. 4, no. 6, pp. 938-947 (1998).

2.15. S. Janz, A. Bogdanov, P. Cheben, A. Delâge, B. Lamontagne, M.-J. Picard, D.-X. Xu, K. P. Yap, and W. N. Ye, "Silicon-based integrated optics: waveguide technology to microphotonics," in *Proc. of MRS Symposium F on Group-IV Semiconductor Nanostructures*, vol. 832, pp. F1.1 (2004).

2.16. S. J. McNab, N. Moll, and Y. A. Vlasov, "Ultra-low loss photonic integrated circuit with membrane-type photonic crystal waveguides," *Optics Express*, vol. 11, no. 22, pp. 2927-2939 (2003).

2.17. H. Ou, "Trenches for building blocks of advanced planar components," *IEEE Phot. Tech. Lett.*, vol. 16, no. 5, pp. 1334-1336 (2004).

2.18. M. Ukechi, T. Miyashita, Y. Komine, T. Masa, A. Takahashi, T. Nishimura, R. Kaku, S. Hirayama, N. Uehara, and K. Ito, "A new concept for the WDM module using a waveguide equipped with filter," in *Proc. of Opt. Fiber Comm.*, vol. 2, pp. 97-99 (2000).

2.19. M. Makihara, M. Sato, F. Shimokawa, and Y. Nishida, "Micromechanical optical switches based on thermocapillary integrated in waveguide substrate," *IEEE J. Light. Tech.*, vol. 17, no. 1, pp. 14-18 (1999).

2.20. K. P. Yap, B. Lamontagne, A. Delâge, S. Janz, A. Bogdanov, M. Picard, E. Post, P. Chow-Chong, M. Malloy, D. Roth, P. Marshall, and K. Y. Liu, "Fabrication of lithographically defined optical coupling facets for silicon-on-insulator waveguides by inductively coupled plasma etching," *JVSTA*, vol. 24, no. 3, pp. 812-816 (2006).

2.21. G. Craciun, M. A. Blauw, E. van der Drift, P. M. Sarro, and P. J. French, "Temperature influence on etching deep holes with $SF_6/O_2$ cryogenic plasma," *J. Micromech. Microeng.*, vol. 12, no. 4, pp. 390-394 (2002).

2.22. A. Tserepi, E. Gogolides, C. Cardinaud, L. Rolland, and G. Turban, "Highly anisotropic silicon and polysilicon room-temperature etching using fluorine-based high density plasmas," *Microelec. Eng.*, vol. 41-42, pp. 411 (1998).

3.1. L. Pavesi and D. J. Lockwood, *Silicon Photonics*, Springer-Verlag, Berlin (2004).

3.2. M. L. Calvo, V. Lakshminarayanan, *Optical Waveguides: From Theory to Applied Technologies*, CRC Press, Taylor and Francis group, Florida, 2007.

3.3. D. Marcuse, "Radiation losses of dielectric waveguides in terms of the power spectrum of the wall distortion function," *Bell Sys. Tech. J.*, vol. 48, pp. 3233-3242 (1969).

3.4. J. P. R. Lacey and F. P. Payne, "Radiation loss from planar waveguide with random wall imperfections," *IEEE J. Optoelectronics*, vol. 137, no. 4, pp. 282-288 (1990).

3.5. A. W. Synder and J. D. Love, *Optical Waveguide Theory*, Chapman and Hall, London, 1983.

3.6. F. Ladouceur, J. D. Love, and T. J. Senden, "Measurements of surface roughness in buried channel waveguides," *IEEE Electon. Lett.*, vol. 28, no. 3, pp. 1321-1322 (1992).

3.7. F. P. Payne, J. P. R. Lacey, "A theoretical analysis of scattering loss from planar optical waveguides," *Opt. and Quantum Elec.*, vol. 26, pp. 977-986 (1994).

3.8. K. K. Lee, D. R. Lim, H. Luan, A. Agarwal, J. Foresi, and L. C. Kimerling, "Effect of size and roughness on light transmission in a $Si/SiO_2$ waveguide: experiments and model," *Appl. Phys. Lett.*, vol. 77, no. 11, pp. 1617-1619 (2000).

3.9. G. T. Reed, A. P. Knights, *Silicon Photonics*, John Wiley & Sons Ltd., England (2004).

3.10. T. Barwicz and H. A. Haus, "Three-dimensional analysis of scattering losses due to sidewall roughness in microphotonic waveguides," *IEEE J. Lightwave Tech.*, vol. 23, no. 9, pp. 2719– 2732 (2005).

3.11. K. P. Yap, A. Delâge, B. Lamontagne, S. Janz, D.-X. Xu, J. Lapointe, P. Waldron, J. Schmid, P. Chow-Chong, E. Post, B. Syrett, "Scattering loss measurement of SOI waveguides using 5×17 integrated optical star coupler," in *Proc. of SPIE Photonics West 2007*, vol. 6477, pp. 64770J1-11 (2007).

3.12. S. Chen, Q. Yan, Q. Xu, Z. Fan, and J. Liu, "Optical waveguide propagation loss measurement using multiple reflections method," *Opt. Comm.,* vol. 256, no. 1-3, pp. 68-72 (2005).

3.13. T. Ikegami, "Reflectivity of mode at facet and oscillation mode in double-heterostructure injection lasers," *IEEE J. Quantum Elec.*, vol. QE-8, no. 6, pp. 470-476 (1972).

3.14. G. Tittelbach, B Richter, and W Karthe, "Comparison of three transmission methods for integrated optical waveguide propagation loss measurement," *Pure Appl. Opt.*, vol. 2, no. 6, pp. 683-706 (1993).

3.15. K. P. Yap, J. Lapointe, B. Lamontagne, A. Delâge, A. Bogdanov, S. Janz, and B. Syrett, "SOI waveguide fabrication process development using star coupler scattering loss measurements," in *Proc. of SPIE Microelectronics, MEMS, Photonics and Nanotechnology 2007*, Australia, vol. 6800, no. 680014, pp.1-12 (2008).

3.16. B. Jalali, S. Yegnanarayanan, T. Yoon, T. Yosuimoto, I. Rendina, and F. Coppinger, "Advances in silicon-on-insulator optoelectronics," *IEEE J. Sel. Top. Quant. Elec.*, vol. 4, no. 6, pp. 938-947 (1998).

3.17. A. P. Milenin, C. Jamois, R. B. Wehrspohn, M. Reiche, "The SOI planar photonic Crystal fabrication: patterning of Cr using $Cl_2/O_2$ plasma etching", *Microelectronic Engineering*, vol. 77, pp.139-143 (2005).

3.18. H. Nakata, K. Nishioka, and H. Abe, "Plasma etching characteristics of chromium film and its novel etching mode", *J. Vac. Sci. Tech.*, vol. 17, no. 6, 1351-1357 (1980).

3.19. K. K. Lee, D. R. Lim, L. C. Kimerling, J. Shin, and F. Cerrina, "Fabrication of ultralow-loss $Si/SiO_2$ waveguides by roughness reduction," *Opt. Lett.*, vol. 26, no. 23, pp.1888-1890 (2001).

3.20. J. H. Schmid, A. Delage, B. Lamontagne, J. Lapointe, S. Janz, P. Cheben, A. Densmore, P. Waldron, D. –X. Xu and K. P. Yap, "Interference effect in scattering loss of high-index-contrast planar waveguides caused by boundary reflections," *Opt. Lett.*, vol. 33, no. 13, pp. 1479-1481 (2008).

3.21. H. Kogelnik, "Theory of optical waveguides" in *Guided Wave Optoelectronics*, T. Tamir, Ed., Second edition, Berlin: Springer-Verlag, 1990, pp.7-87.

3.22. FIMMWAVE, Photon Design, Oxford, UK. Available: www.photond.com.

3.23. D. K. Sparacin, R. Sun, A. M. Agarwal, M. A. Beals, J. Michel, L. C. Kimerling, T. J. Conway, A. T. Pomerene, D. N. Carothers, M. J. Grove, D. M. Gill, M. S. Rasras, S. S. Patel, and A. E. White, "Low loss amorphous silicon channel waveguides for integrated photonics," *IEEE 3rd Int. Conf. on Group IV Photonics*, paper FD2, pp. 1-3 (2006).

3.24. M. -C. M. Lee and M. C. Wu, "Thermal annealing in hydrogen for 3-D profile transformation on silicon-on-insulator and sidewall roughness reduction", *J. Microelectromec. Sys.*, vol. 15, no. 2, pp. 338-343 (2006).

3.25. L. Rowe, M. Elsey, E. Post, N. G. Tarr, and A. P. Knights, "A CMOS-compatible rib waveguide with local oxidation of silicon isolation", *Proc. SPIE Photonics West: Silicon Photonics II*, San Jose, vol. 6477, pp. 64770L1-12 (2007).

3.26. D. K. Sparacin, S. J. Spector, and L. C. Kimerling, "Silicon waveguide sidewall smoothing by wet chemical oxidation," *IEEE J. Lightwave Tech.*, vol. 23, no. 8, pp. 2455– 2461 (2005).

3.27. H. Namatsu, M. Nagase, T. Yamaguchi, K. Yamazaki, and K. Kurihara, "Influence of edge roughness in resist patterns on etched patterns", *J. Vac. Sci. Tech. B*, vol. 16, no. 6, pp. 3315-3321 (1998).

3.28. J. W. Bae, W. Zhao, J. H. Jang, and I. Adesida, "Characterization of sidewall roughness of InP/InGaAsP etched using inductively coupled plasma for low loss optical waveguide applications", *J. Vac. Sci. Tech. B*, vol. 21, no. 6, pp. 2888-2891 (2003).

3.29. J. H. Jang, W. Zhao, J. W. Bae, and I. Adesida, "Study of the evolution of nanoscale roughness from the line edge of exposed resist to the sidewall of deep-etched InP/InGaAsP heterostructures", *J. Vac. Sci. Tech. B*, vol. 22, no. 5, pp. 2538-2541 (2004).

3.30. B. Docter, E. J. Geluk, M. J. H. Sander-Jochem, F. Karouta, and M. K. Smit, "Deep etching of DBR gratings in InP using $Cl_2$ based ICP process", *Proc. IEEE/LEOS Symposium, Benelux Chapter, Eindhoven*, pp. 97-100 (2006).

4.1. R. Kasahara, M. Yanagisawa, A. Sugitia, T. Goh, M. Yasu, A. Himeno, and S. Matsui, "Low-power consumption silica-based 2×2 thermooptic switch using trenched silicon substrate," *IEEE Photon. Tech. Lett.*, vol. 11, no. 9, pp. 1132-1134 (1999).

4.2. B. J. Offrein, D. Jubin, T. Koster, T. Brunschwiler, F. Horst, D. Wiesmann, I. Meijer, M. Sousa Petit, D. Webb, R. Germann, and G. L. Bona, "Polarization-independent thermooptic phase shifters in silicon-oxynitride waveguides," *IEEE Photon. Tech. Lett.*, vol. 16, no. 6, pp. 1483-1485 (2004).

4.3. Q. Lai, W. Hunziker, and H. Melchjior, "Low-power compact 2×2 thermooptic silica-on-silicon waveguides switch with fast response," *IEEE Photon. Tech. Lett.*, vol. 10, no. 5, pp. 681-683 (1998).

4.4. H. Min-Cheol, H. –J. Lee, M. –H. Lee, J. –H. Ahn, and S. G. Han, "Asymmetric X-junction thermo-optic switches based on fluorinated polymer waveguides," *IEEE Photon. Tech. Lett.*, vol. 10, no. 6, pp. 813-815 (1998).

4.5. Y. Hida, H. Onose, and S. Imamura, "Polymer waveguide thermooptic switch with low electric power consumption at 1.3μm," *IEEE Photon. Tech. Lett.*, vol. 5, no. 7, pp. 782-784 (1993).

4.6. U. Fischer, T. Zinke, B. Schuppert, and K. Petermann, "Singlemode optical switches based on SOI waveguide with large cross-section," *Electron Lett.*, vol. 30, no. 5, pp. 406-408 (1994).

4.7. A. House, R. Whiteman, L. Kling, S. Day, A. Knights, D. Hogan, F. Hopper, and M. Asghari, "Silicon waveguide integrated optical switching with microsecond switching speed," *Proc. of Opt. Fiber Comm.*, vol. 2, pp. 449-450 (2003).

4.8. R. L. Espinola, M. –C. Tsai, J. T. Yardley, and R. M. Osgood, Jr., "Fast and low-power thermo-optic switch on thin silicon-on-insulator," *IEEE Photon. Tech. Lett.*, vol. 15, no. 10, pp. 1366-1368 (2003).

4.9. Y. Li, J. Yu, and S. Chen, "A silicon-on-insulator-based thermo-optic waveguide switch with low insertion loss and fast response," *Chinese Phys. Lett.*, vol. 22, no. 6, pp. 1449-1451 (2005).

4.10. Y. Li, J. Yu, and S. Chen, "Rearrangeable nonblocking SOI waveguide thermooptic 4×4 switch matrix with low insertion loss and fast response," *IEEE Photon. Tech. Lett.*, vol. 17, no. 8, pp. 1641-1643 (2005).

4.11. Y. Li, Y. Chen, S. Chen, and J. Yu, "Silicon-on-insulator thermo-optic variable attenuator module with fast response," *Opt. Eng.*, vol. 44, no. 6, paper 064602, pp.1-3 (2005).

4.12. Y. Li, J. Yu, S. Chen, Y. Li, and Y. Chen, "Submicrosecond rearrangeable nonblocking silicon-on-insulator thermo-optic 4×4 switch matrix," *Opt. Lett.*, vol. 32, no. 6, pp. 603-604 (2007).

4.13. T. Chu, H. Yamada, S. Ishida, and Y. Arakawa, "Compact 1×N thermo-optic switches based on silicon photonic wire waveguides," *Opt. Express*, vol. 13, no. 25, pp. 10109-10114 (2005).

4.14. L. Tong, J. Lou, and E. Mazur, "Single-mode guiding properties of subwavelength-diameter silica and silicon wire waveguides," *Opt. Express*, vol. 12, no. 6, pp. 1025-1035 (2004).

4.15. S. Janz, P. Cheben, A. Delâge, A. Densmore, B. Lamontagne, E. Post, J. Schmid, P. Waldron, D.-X. Xu, K. P. Yap, and W. N. Ye, "Silicon Microphotonic waveguide technology for sensing, spectroscopy and communication," *ECS transaction: Science and Technology of Dielectrics for Active and Passive Photonic Devices*, vol. 3, no.11, pp. 61-78 (2006).

4.16. M. W. Geis, S. J. Spector, R. C. Williamson, and T. M. Lyszczarz, "Submicrosecond submilliwatt silicon-on-insulator thermooptic switch," *IEEE Photon. Tech. Lett.*, vol. 16, no. 11, pp. 2514-2516 (2004).

4.17. M. Harjanne, M. Kapulainen, T. Aalto, and P. Heimala, "Sub-μs switching time in silicon-on-insulator Mach-Zehnder thermooptic switch," *IEEE Photon. Tech. Lett.*, vol. 16, no. 9, pp. 2039-2041 (2004).

4.18. T. Aalto, M. Kapulainen, S. Yliniemi, P. Heimala, and M. Leppihalme, "Fast thermo-optical switch based on SOI waveguides," *Proc. of SPIE Integrated Optics 2003*, vol. 4987, pp. 149-159 (2003).

4.19. R. A. Soref, J. Schmidtchen, and K. Petermann, "Large single-mode rib waveguides in GeSi-Si and Si-on-SiO2," *IEEE J. Quantum Electron.*, vol. 27, no. 8, pp. 1971-1974 (1991).

4.20. Wikipedia, "Beer-Lambert Law," http://en.wikipedia.org/wiki/Beer-Lambert_law.

4.21. Y. S. Touloukian, R. W. Powell, C. Y. Ho, and M. C. Nicolaou, "Thermal Diffusivity" in vol. 10 of *Thermophysical Properties of Matter*, IFI/Plenum Data Corporation, New York (1973).

4.22. Wikipedia, "Heat Conduction," http://en.wikipedia.org/wiki/Heat_conduction

4.23. F. P. Incropera, D. P. Dewitt, *Introduction To Heat Transfer*, John Wiley & Sons, New York (1990).

4.24. Wikipedia, "Rise Time," http://en.wikipedia.org/wiki/Rise_time

4.25. T. Smy, D. Walkey, and S. K. Dew, "A 3D thermal simulation tool for integrated devices- ATAR," *IEEE Transactions on Computer-Aided Des.*, vol. 20, no.1, pp. 105-115 (2001).

4.26. R. C. Weast, *Handbook of Chemistry and Physics*, 64th Edition, CRC Press Inc., Florida (1984).

5.1. H. Yamada, T. Chu, S. Ishida, and Y. Arakawa, "Si photonic wire waveguide devices," *IEEE J. Sel. Topics in Quan. Elec.*, vol. 12, no. 6, pp. 1371-1379 (2006).

5.2. W. Bogaerts, P. Dumon, D. V. Thourhout, D. Taillaert, P. Jaenen, J. Wouters, S. Beckx, V. Wiaux, and R. G. Baets, "Compact wavelength-selective functions in silicon-on-insulator photonic wires," *IEEE J. Sel. Topics in Quan. Elec.*, vol. 12, no. 6, pp. 1394-1401 (2006).

5.3. P. Dumon, W. Bogaerts, V. Wiaux, J. Wouters, S. Beckx, J. V. Campenhout, D. Taillaert, B. Luyssaert, P. Bienstman, D. V. Thourhout, and R. G. Baets, "Low-loss SOI photonic wires and ring resonators fabricated with deep UV lithography," *IEEE Photon. Tech. Lett.*, vol. 16, no. 5, pp. 1328-1330 (2004).

5.4. T. Tsuchizawa, K. Yamada, H. Fukuda, T. Watanabe, J. Takahashi, M. Takahashi, T. Shoji, E. Tamachika, S. Itabashi, and H. Morita, "Microphotonics devices based on silicon microfabrication technology," *IEEE J. Sel. Topics in Quan. Elec.*, vol. 11, no. 1, pp. 232-240 (2005).

5.5. B. E. Little, J. S. Ferosi, G. Steinmeyer, E. R. Thoen, S. T. Chu, H. A. Haus, E. P. Ippen, L. C. Kimerling, and W. Greene, "Ultra-compact Si-$SiO_2$ microring resonator optical channel dropping filters," *IEEE Photon. Tech. Lett.*, vol. 10, no. 4, pp. 549-551 (1989).

5.6. R. L. Espinola, M. –C. Tsai, J. T. Yardley, and R. M. Osgood, Jr., "Fast and low-power thermo-optic switch on thin silicon-on-insulator," *IEEE Photon. Tech. Lett.*, vol. 15, no. 10, pp. 1366-1368 (2003).

5.7. M. W. Geis, S. J. Spector, R. C. Williamson, and T. M. Lyszczarz, "Submicrosecond submilliwatt silicon-on-insulator thermooptic switch," *IEEE Photon. Tech. Lett.*, vol. 16, no. 11, pp. 2514-2516 (2004).

5.8. H. Yamada, T. Chu, S. Ishida, and Y. Arakawa, "Optical directional coupler based on Si-wire waveguides," *IEEE Photon. Tech. Lett.*, vol. 17, no. 3, pp. 585-587 (2005).

5.9. T. Fukuzawa, F. Ohno, and T. Baba, "Very compact arrayed-waveguide-grating demultiplexer using Si photonic wire waveguides," *Jpn. J. Appl. Phys.*, vol. 43, pp. L673-L675 (2004).

5.10. H. Yamada, T. Chu, S. Ishida, and Y. Arakawa, "Optical add-drop multiplexers based on Si-wire waveguides," *Appl. Phys. Lett.*, vol. 86, pp. 191107 (2005).

5.11. A. Densmore, D.-X. Xu, P. Waldron, S. Janz, A. Delâge, P. Cheben, and J. Lapointe, "Thin silicon waveguides for biological and chemical sensing," *Proc. SPIE Photonics West: Silicon Photonics II*, San Jose, vol. 6477, pp. 647718-1 to 647718-10 (2007).

5.12. L. Tong, J. Lou and E. Mazur, "Single mode guiding properties of subwavelength-dimension silica and silicon wire waveguides," *Opt. Express*, vol. 12, no. 6, pp. 1025-1035 (2004).

5.13. FIMMWAVE, Photon Design, Oxford, UK. Available: www.photond.com.

5.14. S. Janz, P. Cheben, A. Delâge, A. Densmore, B. Lamontagne, E. Post, J. Schmid, P. Waldron, D.-X. Xu, K. P. Yap, and W. N. Ye, "Silicon Microphotonic waveguide technology for sensing, spectroscopy and communication," *ECS transaction: Science and Technology of Dielectrics for Active and Passive Photonic Devices*, vol. 3, no.11, pp. 61-78 (2006).

5.15. Wikipedia, "Finite Difference Method," http://en.wikipedia.org/wiki/Finite_difference_method

5.16. Y. –C. Chiang, Y. –P. Chiou, and H. –C. Chang, "Improved full-vectorial finite-difference mode solver for optical waveguides with step-index profiles," *IEEE J. Lightwave Tech.*, vol. 20, no. 8, pp. 1609– 1618 (2002).

5.17. M. S. Stern, "Semivectorial polarised finite difference method for optical waveguides with arbitrary index profiles," *IEE Proc.*, vol. 135, pt. J, no. 1, pp. 56-63 (1988).

5.18. S. G. Johnson, M. Ibanescu, M. A. Skorobogatiy, O. Weisberg, J. D. Joannopoulos, and Y. Fink, "Perturbation theory for Maxwell's equations with shifting material boundaries," *Phys. Rev. E*, vol. 65, no. 6, pp. 066611-1 to 066611-7 (2002).

5.19. A. W. Snyder and J. D. Love, *Optical Waveguide Theory*, Chapman and Hall, New York (1983).