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Investigation of Low Phase Noise Microwave Oscillators with LTCC Integration

by

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ABSTRACT

Low phase noise oscillators are important for modern wireless communications. System-in-package design approaches are increasingly being sought for miniaturization and cost reduction. This thesis addresses both issues by investigating low phase noise oscillator designs using the device-line technique along with LTCC-based resonators. Two basic oscillator designs are pursued at S-band and C-band, demonstrating the validity and legitimacy of the device-line technique for achieving low phase noise and the ability to realize compact, high-Q resonators in an LTCC environment. At 6.09GHz , the proposed oscillator produced 8.17 dBm of power and -125 dBc/Hz at 1 MHz offset for phase noise with a 260 mm^2 resonator having a Q of 125. The performance of this circuit is comparable to the best C-band published oscillators in recent literature.

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LIST OF ACRONYMS

AC	Alternating Current
AM	Amplitude Modulation
BJT	Bipolar Junction Transistor
BW	Bandwidth
CAD	Computer Aided Design
CPW	Coplanar Wave Guide
DC	Direct Current
DR	Dielectric Resonator
F	Noise Factor
FET	Field Effect Transistor
GaAs	Gallium Arsenide
HFSS	High Frequency Structure Simulator
IC	Integrated Circuits
IF	Intermediate Frequency
ISF	Impulse Sensitivity Function
LC	Inductor Capacitor
LHP	Left Hand Plane
LTCC	Low Temperature Cofired Ceramic
LTI	Line Time Invariant
LTV	Linear Time Variant
MESFET	MEtal Semiconductor Field Effect Transistor
NF	Noise Figure
pHEMT	Pseudo High Electron Mobility Transistor
PM	Phase Modulation
RF	Radio Frequency
RHP	Right Hand Plane

RLC	Resistor Inductor Capacitor
RMS	Root Mean Square
Rx	Receive
SMA	Sub Miniature – Type A
SMD	Surface Mount Device
SNR	Signal-to-Noise Ratio
SSB	Single Side Band
TEM	Transverse ElectroMagnetic
TL	Transmission Line
Tx	Transmit
VSWR	Voltage Standing Wave Ratio
YIG	Yittrium Iron Garnet

LIST OF SYMBOLS

$B(t)$	Amplitude oscillatory variations
Ceq	Equivalent resonator tank capacitance
f_c	Amplifier corner frequency
f_m	Noise modulating frequency
$G(j\omega)$	Frequency-dependent forward loop gain
$h_\Phi(t)$	Unit impulse response for excess phase
$H(j\omega)$	Frequency-dependent feedback network
$H_{resonator}(\omega_m)$	Resonator transfer function
k	Boltzmann's constant
$L(f_m)$	Ratio of noise power in a 1-Hz BW at f_m offset from carrier signal power
NF_{min}	Minimum noise figure
P_{1dB}	1-dB compression point
P_{avs}	Power available from the source
P_{DC}	DC input power
P_{diss}	DC Dissipated power
P_{in}	Input power
P_{out}	Output power
P_{osc}	Oscillator power
P_S	Power in carrier signal
P_{SBC}	Power in sidebands relative to carrier
P_{SSB}	Power in SSB signal at f_m offset in 1-Hz BW
PM	Phase modulation
q_{max}	Maximum charge displacement across the node capacitor where voltage is measured
Q	Resonator quality factor

Q_L	Resonator loaded quality factor
Q_U	Resonator unloaded quality factor
R_c	Passive circuit's real resistance
R_d	Active device's real resistance
s	Pole pair composed of real, σ, and complex, $j\omega$, frequencies
$S_{\Delta\theta}(f_m)$	Spectral density of phase fluctuation
T	Ambient temperature in Kelvin
$T(j\omega)$	Closed-loop transfer function
t_{cond}	Conductor thickness
$tan\delta$	Dielectric loss tangent
$u(t)$	Unit impulse function
$V_n(t)$	Noise input signal at oscillator power-up
$V_{n,rms}$	Noise voltage in 1-Hz BW
ω_0	Angular frequency
Z_c	Circuit impedance
Z_d	Impedance looking into a specific terminal of the active device
Z_L	Oscillator load network
Z_o	Characterisitc Impedance
Z_T	Oscillator terminating network
σ	Real frequency in complex pole
$\theta(t)$	Phase oscillatory variations
Γ_c	Passive circuit reflection coefficient
Γ_d	Active circuit reflection coefficient
Γ_{IN}	Input reflection coefficient
Γ_L	Load reflection coefficient
$\Gamma(x)$	Impulse sensitivity function
$\Delta\Phi(t)$	Random phase fluctuations due to noise
$\Delta\theta^2_{rms}$	RMS power function of $\Delta\theta_{peak}$
$\Delta\theta_{peak}$	Phase modulation index

CHAPTER 1

INTRODUCTION

1.1 – Background and Motivation

Taking a stroll down Tokyo's main boulevard, one notices what a revolution the wireless industry has spun together in the recent past. To a consumer's content nowadays, it is hardly inconceivable anymore to imagine a world in the future without any wires or cables. Even before the burst of the wireless devices prevalent in our daily life, one's imagination was not far from reality with classic Hollywood movies such as *"Star Wars"* and *"Star Trek"*, which not only mainstreamed wireless communications, but also made inter-galactic radio an imaginable concept.

The use and sometimes abuse of wireless devices has exploded onto the scene in an unprecedented manner at the turn of the century. It's not only people that are communicating more than ever before, but we also have found a way to allow the seamless information exchange between autonomous elements. Everything from cellular phones, wireless internet, instant messaging, and on-demand voice/video/data, to broadband satellite, to biomedical devices and medical instrumentation, to electronic warfare and a host of military applications are all behind the technical evolution of the

wireless boom. Figure 1.1 below illustrates the convergence and multi-use wireless systems and devices:

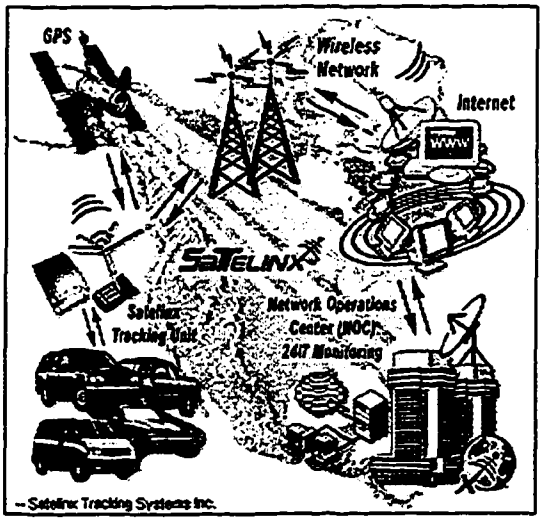


Figure 1.1: Wireless communication system [1.1]

At the core of the plethora of wireless communication systems are a multitude of electronic devices that operate independently. These devices, generally assembled of several integrated components, form the mechanism by which electromagnetic energy waves are transmitted and received. These combined electronic components constitute to form the basis of a wireless radio, illustrated in Figure 1.2 below:

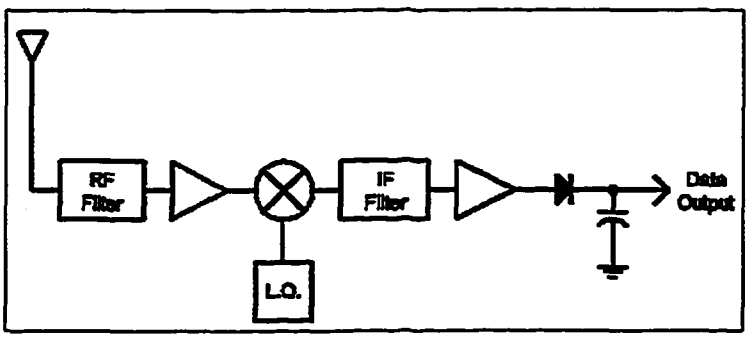


Figure 1.2: A simple single-conversion superheterodyne receiver

Of the components presented in the figure above, the local oscillator plays a key role in the operation of the transmitter and receiver apparatus. Its main function is to upconvert the IF to proper RF in the Tx path, while it downconverts the RF into the suitable IF in the Rx path. Below is a historical timeline of the oscillator:

- ***1893*** – First tunable oscillator by scientist American Michael Pupin [1.2]
- ***1906*** – Canadian Reginald A. Fessenden, inventor of the 1st sonar oscillator, successfully demonstrated the first voice broadcast over long distances from Brant Rock, Massachusetts laboratory. It was the first time anyone has transmitted anything other than dot-dash Morse Code developed by Marconi. Mr. Fessenden is credited in some circles as the father of AM modulation. [1.3]
- ***1912*** –Edwin Armstrong, the father of FM radio, discovers oscillation-enducing "regeneration", which gave birth to the superheterodyne radio. At the same time, Rocket pioneer Robert Goddard was first to employ positive feedback principles to demonstrate vacuum tube oscillators [1.4], shown in Figure 1.3:

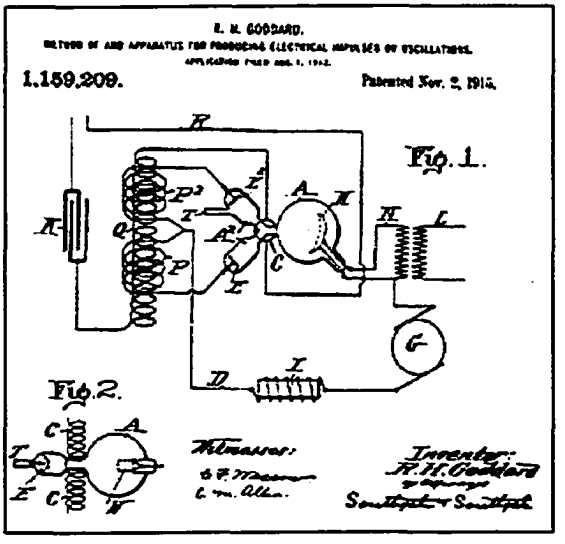


Figure 1.3: Oscillator demonstrated by Goddard [1.5]

- ***1913*** – Alexander Meissner was able to successfully induce oscillations in vacuum tube amplifiers by utilizing a regenerative (positive feedback) network based on Goddard's work
- ***1915*** – While at Western Electric Ralph V. L. Hartley and Canadian Edwin Colpitts invent what will be forever known as the "Colpitts" and "Hartley" oscillators.
- ***1920*** – Heinrich Georg Barkhausen, along with Karl Kurz, discovered the Barkhausen-Kurz oscillator for UHF, which led to the understanding of the principle of velocity modulation [1.6]. Shortly after, Heinrich Barkhausen established the Stability Criterion for oscillators, later to be known as the Barksausen Criterion.
- ***1950-1960*** – First schism in oscillator design. In the 1950, the first semiconductor transistor was made available, which transformed oscillators from vaccum-tube to semiconductor based circuits. In 1960, the first varactor diode was also introduced, which also enhanced oscillator circuit even further [1.7].
- ***1980*** – Second schism in oscillator design. Due to the vast improvement of planar technologies, the oscillator was designed using discrete or monolithic components.

However, the eruption of wireless applications has slowly led to a gradual crowding of the spectrum channel. The number of available free bands in the frequency spectrum is dwindling, and carriers are trying to squeeze out every bit of bandwidth from the allocated channels. Thus, in order to accommodate the number of wireless services,

carriers are operating their systems on assigned frequencies that are extremely close to each other, introducing interference and overlap quandaries. Therefore, stricter specifications are being applied for adjacent channels that operate within a close proximity of each other, where oscillator phase noise contributes to channel noisiness. As well, the desire for the combination of most wireless communications services into a single product has driven the creation of system-on-chip and system-in-package solutions. This has naturally led to an increasing level of integration of components, where the resulting low Q's and the effects of noise more seriously degrade today's wireless devices. Thus, a great need exists to make these components as low noise as possible, forming an important topic of research in the semiconductor industry. Of these components, microwave oscillators are among the most critical in terms of noise performance.

The subject of low phase noise oscillator design is quite vast and has been extremely well and thoroughly researched over the last 10 years. With the advancement of CAD tools, researchers and designers are able to comprehend the operation of oscillators and their phase noise performance in an improved way. In addition, the parameters affecting phase noise are also better understood, hence leading to structured and almost systematic design approach for low phase noise designs. The designer has an arsenal of techniques with which to achieve low phase noise: high-Q resonant elements, low noise transistor, optimized circuit topologies, injection locking, and PLLs. As will be seen later in this work, a basic circuit technique for minimizing oscillator noise, the "device-line technique", has not been sufficiently explored.

1.2 - Thesis Objectives

The thesis objectives for this work are as follows:

- To review the microwave oscillator design techniques, with particular emphasis on the phase noise concept;
- To outline a low-noise design methodology based on the device-line technique, and investigate numerous circuit using various parameters and their effect on phase noise;
- To design, build, and test various S/C-band oscillator circuits verifying the effects of the circuit parameters, and to demonstrate the amenability of these circuits to LTCC packaging environment;
- To compare designs, validate methodology, and confirm the accuracy simulation tools.

1.3 - Thesis Organization

There are a total of 5 parts in this thesis. The first part is the introductory chapter outlining the thesis motivation along with its proposed objectives.

The second part is the theory chapter. It contains background information regarding oscillators and the parameters that are to be evaluated. As well, the two methods that are most commonly used when analyzing oscillators are included. Mathematical derivations are carried out in this chapter with regards to oscillator design approach. Along with that, it also incorporates a part regarding phase noise and possible recommendations for improvement.

The third part is the application chapter. The main focus is the outline of the design methodology geared towards low-phase noise oscillators. In addition, the chapter describes the design of several oscillator circuits based on the design plan. Their simulation results are also presented in support of the design methodology. Since this work also emphasizes the use of high-Q resonators in the design process, a section is included discussing the LTCC resonators as well as their measured results. Finally, the implementation of several chosen oscillator designs in microstrip technology is shown, along with their respective simulation results.

The fourth part is the performance chapter. It contains the outcome of the measurements taken from the realized oscillators. Comparison between the acquired results and the simulation results are also discussed.

The fifth part is the concluding chapter. It summarizes the work presented in this thesis, along with recommendations for future improvements and research in this area of study.

CHAPTER 2

OVERVIEW OF OSCILLATOR THEORY AND FUNDAMENTALS

An electronic oscillator is a device that is able to efficiently convert DC power into an AC signal. There are various types of AC signals: Periodic, where the oscillator has a spectrum consisting of a fundamental frequency plus an certain number of harmonics; Pseudo-periodic, where the spectrum consists of more than one frequency all unrelated to each other; Chaotic, where the spectrum is flat and contains frequency components of all frequencies. As well, there are various forms of oscillator implementations: ring oscillators, LC tuned oscillators, crystal oscillators, relaxation oscillators, bandpass filter based oscillators, YIG oscillators, and DR oscillators. Our discussion will strictly be concentrated on LC-type tuned oscillators with a periodic sinusoidal output signal. Therefore, the fundamentals of oscillator theory are outlined in this chapter. As well, several methods of oscillator analysis are presented and examined, in order to establish several key design decisions for subsequent chapters. A detailed discussion about phase noise is also included along with its effects for this work.

2.1 – Feedback Oscillator Theory

Classic oscillator feedback theory has been instituted in student manuals since the early days of engineering. Although it has now been well-known and extremely thoroughly developed, it nonetheless establishes important concepts when studying oscillator behavior. However, although similar to the models that are to be studied here, the reader is welcomed to refer to oscillator feedback theory in Appendix A.1.

2.2 – Negative Resistance Oscillator Theory

2.2.1 – Why Negative Resistance?

As aforementioned in this chapter, an oscillator is mainly composed of an active device and a feedback network that allows part of the output signal to be fed back into the input of the active device, and hence create oscillations. An oscillator can also be analysed as an active device with a resonator, as shown in Figure 2.1.

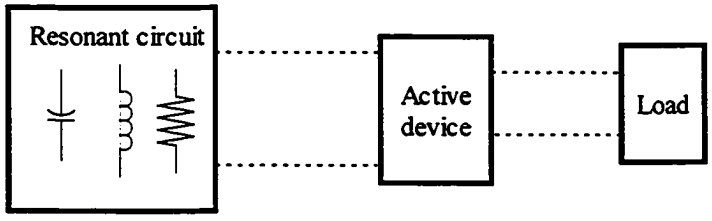


Figure 2.1: Oscillator with resonator

When spiked with a burst of energy, a resonator circuit is capable of transferring that energy back and forth between its charge and discharge elements. The reactive elements

store the energy for one half cycle, while releasing it in the next half cycle. This continuous energy transfer back and forth between components composes a sinusoidal signal trace. Hence, energy storage capability is a requirement for resonance and oscillation. There are numerous different types of resonators available for oscillators, some of which are:

- Lumped elements
- Dielectric puck;
- Distributed transmission line (TEM microstrip or coaxial line);
- Waveguide/Cavity;
- YIG sphere resonators;

As shown in Figure 2.1, almost all microwave resonators can be represented by a series/parallel lumped equivalent model, i.e. capacitors and inductors. Therefore, as with all lumped components, losses exist due to hysteresis, eddy currents, and imperfect inductors, while dielectric hysteresis, leakage in dielectric and finite conductivity for capacitors. As a result, a resistor always accompanies the equivalent circuit model representing losses in the actual circuit. Therefore, the energy transfer between lumped components will inherently experience loss in each cycle, leading to damped oscillations. Now, in order to experience undamped oscillations, a mechanism has to be introduced to counteract the resonator losses and hence eliminate the positive resistance through the introduction of negative resistance. If the manufactured negative resistance is able to exactly cancel out the resonator losses, then we obtain steady-state oscillations:

$$Z_d(\omega, P, V_{dc}, I_{dc}, T, ...) + Z_c(\omega) = 0 \quad \textbf{for} \quad Z = R + jX \tag{2.1}$$

Where Z_d is the device impedance dependent on bias point, frequency, and power, while Z_c is the circuit (resonator) impedance, dependent only on frequency. Negative impedance can be generated in a variety of ways, some of which involve 1-port active devices such as Gunn diodes or 2-port active devices such as transistors, which will be utilized in this work.

2.2.2 – Oscillation Conditions Using Impedances

A general schematic diagram for the one-port negative resistance oscillator is show in Figure 2.2:

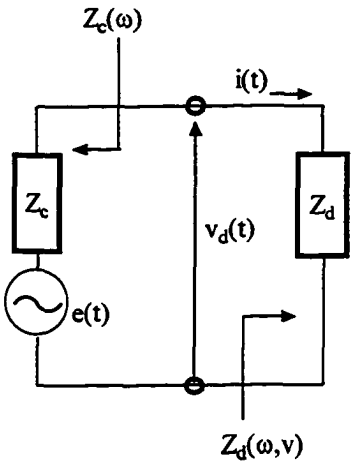


Figure 2.2: Impedance oscillator schematic at device reference plane

The oscillator is a closed loop system, thus any analysis requires the selection of a break point within the loop to gain insight into its operation. A loop opening would be at the device terminals reference plane, since it marks the physical connection between the resonator and the active device. Therefore we shall use this point as the start for the 1-port device oscillator analysis, to be expanded to 2-port devices. This analysis is aimed at obtaining the oscillation conditions at the fundamental frequency, in terms of the device and circuit impedance at the device reference plane.

As mentioned earlier, power supplies are the main initiators of oscillations in free-running oscillators. In Figure 2.2, *e(t)* is a representation of DC bias supply transients and/or noise. Therefore, as described in [2.6], the current circulating through the circuit is given by the following :

$$i(t) = \mathrm{Re}\{I(t)\} = B(t)\cos(\omega t + \theta(t)) \qquad \text{where } I(t) = B(t)e^{j(\omega t+\theta(t))} \tag{2.2}$$

B(t) and *θ(t)* are unknown amplitude and phase variables of the circuit, where *B(t)* is directly related to the oscillator RF power level and *θ(t)* is directly related to the oscillator frequency. For simplification, we will assume that the device impedance is only a function of amplitude (power) *B(t)*, while circuit impedance is only a function of angular frequency, *ω*. Now, applying Kirchoff's voltage law for the above circuit, we obtain the following:

$$e(t) = v_d(t, B) + \mathrm{Re}[I(t)Z_c(\omega)] \tag{2.3}$$

Equations (2.2) and (2.3) comprise the main components for solving for *B(t)* and *θ(t)* in terms of circuit and device impedances. *B(t)* and *θ(t)* are assumed to be slowly varying variables in time and can be interpreted as noise modulations in amplitude and phase of the signal at frequency *ω*. Examining the RHS of equation (2.3), an expression for $v_d(t)$, being the voltage drop across the device impedance, can be obtained. Using Ohm's Law, we have:

$$\begin{aligned} v_d(t) &= Z_d(\omega)\,\mathrm{Re}\{I(t)\} = i(t)(R_d(\omega) + jX_d(\omega)) \\ &= R_d(\omega)B(t)\cos(\omega t + \theta(t)) - X_d(\omega)B(t)\sin(\omega t + \theta(t)) \end{aligned} \tag{2.4}$$

Where $R_d < 0$ represents the device negative resistance. Turning our attention to the second term in (2.3), the voltage drop across the circuit impedance, with $Z_c(\omega)$ being frequency dependent, is expanded through first-order approximation using perturbation analysis[2.7]. The following derivation is taken from [3.28]:

$$\frac{dI(t)}{dt} = I(t)\left[j\left(\omega + \frac{d\theta(t)}{dt} \right) + \frac{1}{B(t)} \frac{dB(t)}{dt} \right] \tag{2.5}$$

However, we also know that $dI(t)/dt = j\omega I(t)$. Therefore, from (2.5), we can say that:

$$\omega = \omega_0 + \frac{d\theta(t)}{dt} - j \frac{1}{B(t)} \frac{dB(t)}{dt} \tag{2.6}$$

Now, if we introduce perturbation, where $\omega' = \omega + \Delta\omega$, and compare it to (2.6), we have the following result:

$$\Delta\omega = \frac{d\theta(t)}{dt} - j \frac{1}{B(t)} \frac{dB(t)}{dt} \tag{2.7}$$

Assuming that the perturbation $|\Delta\omega| << \omega$, then expanding $Z_c(\omega')$ in a Taylor series about $\omega' = \omega$ produces:

$$\begin{aligned} Z_c(\omega') &\approx Z_c(\omega) + \frac{dZ_c(\omega)}{d\omega} \Delta\omega \\ &= R_c(\omega) + jX_c(\omega) + \left[\frac{dR_c(\omega)}{d\omega} + j \frac{dX_c(\omega)}{d\omega} \right] \left[\frac{d\theta(t)}{dt} - j \frac{1}{B(t)} \frac{dB(t)}{dt} \right] \end{aligned} \tag{2.8}$$

Re-examining the voltage across the circuit impedance, while including the perturbation, we obtain the following:

$$\begin{aligned} \Re e[Z_c(\omega')I(t)] = &\left[R_c(\omega) + \frac{dR_c(\omega)}{d\omega} \frac{d\theta}{dt} + \frac{dX_c(\omega)}{d\omega} \frac{1}{B} \frac{dB}{dt} \right] B(t) \cos(\omega t + \theta(t)) \\ &- \left[X_c(\omega) + \frac{dX_c(\omega)}{d\omega} \frac{d\theta}{dt} - \frac{dR_c(\omega)}{d\omega} \frac{1}{B} \frac{dB}{dt} \right] B(t) \sin(\omega t + \theta(t)) \end{aligned} \tag{2.9}$$

If equation (2.4) and equation (2.9) are substituted back into the loop equation (2.3), the following is obtained:

$$e(t)=\left[R_c(\omega)+R_d(\omega)+\frac{dR_c(\omega)}{d\omega}\frac{d\theta}{dt}+\frac{dX_c(\omega)}{d\omega}\frac{1}{B}\frac{dB}{dt}\right]B(t)\cos(\omega t+\theta(t))$$
$$-\left[X_c(\omega)+X_d(\omega)+\frac{dX_c(\omega)}{d\omega}\frac{d\theta}{dt}-\frac{dR_c(\omega)}{d\omega}\frac{1}{B}\frac{dB}{dt}\right]B(t)\sin(\omega t+\theta(t)) \qquad \textbf{(2.10)}$$

After multiplying equation (2.10) with $cos(\omega t+\theta)$ first and then $sin(\omega t+\theta)$ and integrating over one period of oscillation T_0, in each case the following is obtained:

$$\frac{1}{B}e_c(t)=R_c(\omega)+R_d(\omega)+\frac{dR_c(\omega)}{d\omega}\frac{d\theta}{dt}+\frac{dX_c(\omega)}{d\omega}\frac{1}{B}\frac{dB}{dt} \qquad \textbf{(2.11)}$$

$$\frac{1}{B}e_s(t)=-X_c(\omega)-X_d(\omega)-\frac{dX_c(\omega)}{d\omega}\frac{d\theta}{dt}+\frac{dR_c(\omega)}{d\omega}\frac{1}{B}\frac{dB}{dt} \qquad \textbf{(2.12)}$$

$$\textit{where}\quad e_c(t)=\frac{2}{T_0}\int_{t-T_0}^{t}e(t)\cos(\omega t+\theta)dt \qquad \textbf{(2.13)}$$

$$\textit{and}\quad e_s(t)=\frac{2}{T_0}\int_{t-T_0}^{t}e(t)\sin(\omega t+\theta)dt \qquad \textbf{(2.14)}$$

Equations (2.11) and (2.12) are termed as the general oscillation conditions that enable the determination of the current amplitude and phase within the oscillating circuit at the fundamental frequency. Therefore, under steady-state conditions and during free-running oscillations, we can obtain the final oscillation equations from the above equations:

$$R_c(\omega)+R_d(B)+j\left[X_c(\omega)+X_d(B)\right]=0 \qquad \textbf{(2.15)}$$

For the case of $e(t) = 0$, $dB/dt = 0$ and $d\theta/dt = 0$, from which the amplitude $B = B_0$ and $\omega = \omega_0$ are to be determined. Therefore, we have arrived at an applicable form of equation (2.15), in terms of impedances, where the oscillator has to be designed for the following conditions:

$$R_c + R_d = 0 \Rightarrow R_c = -R_d \quad where\ R_d < 0\ \textbf{since}\ R_c > 0 \tag{2.16}$$

$$X_c + X_d = 0 \Rightarrow X_c = -X_d \tag{2.17}$$

Start-up conditions

The equations above represent the steady-state conditions for oscillator operations. For start-up conditions, a rule of thumb can be employed [2.8]:

$$R_c = -\frac{R_d}{3} \tag{2.18}$$

This condition allows the oscillator to be supplied with enough negative resistance to guarantee initial oscillations, and to also make sure that the condition $R_c(\omega)+R_d(\omega,B)>0$ is never satisfied, which would cause oscillations to cease. If $R_d(\omega,B)$ varies linearly with amplitude, then equation (2.18) is also a practical small-signal assumption for maximum output power [2.8].

Stability

If equation (2.15) is satisfied, then oscillations are achievable. However, if any slight disturbance occurs within the circuit's electrical characteristics (bias point, terminating impedances), then oscillations might gradually cease or the device might fail due to increased amplitude. Stability is a measure of how well the oscillator is able to adjust to various disturbances by returning to a steady-state operating point. Kurokawa [2.7] determined a measure of stability, *S*, that is identifiable, and it will only be stated here as:

$$S = \frac{\partial R_d}{\partial B}\frac{dX_c(\omega_0)}{d\omega} - \frac{\partial X_d}{dB}\frac{dR_c(\omega_0)}{d\omega}$$
$$= \frac{dR_c(\omega_0)}{d\omega}\frac{\partial R_d}{\partial B}\left[\tan\theta_c - \tan\theta_d\right] > 0 \qquad (2.19)$$

$$where\ \tan\theta_c = \frac{dX_c(\omega_0)/d\omega}{dR_c(\omega_0)/d\omega}\ \ and\ \ \tan\theta_c = \frac{dX_d(B)/dB}{dR_d(B)/dB}$$

2.2.3 – Oscillation Conditions Using Reflection Coefficients

In the above section, the oscillation conditions in terms of impedances using voltages and currents were described. However, at microwave frequencies, impedances determined through voltages and currents are extremely difficult to measure. Therefore, reflection coefficients are more suitable for oscillator analysis since they are easily manipulated on network analyzers, while being more applicable to Smith Charts. In this section, analysis for oscillation, stability, and noise criteria will be shown, similar to the analysis performed in section 2.2.2.

Let us then take a look at Figure 2.3:

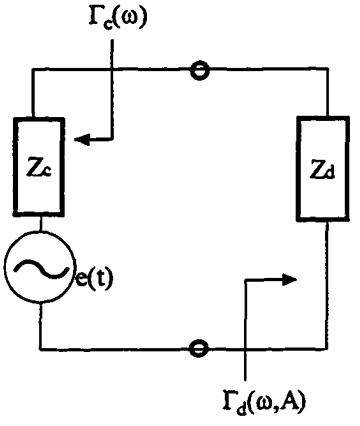


Figure 2.3: Reflection coefficient oscillator schematic at device reference plane

The oscillator equation from (2.15) stated that $Z_c+Z_d = 0$. If we translate this to reflection coefficients of Figure 2.3, we have the following:

$$Z = Z_0 \frac{1+\Gamma}{1-\Gamma}, \quad for \quad \Gamma = \frac{Z-Z_0}{Z+Z_0} \tag{2.20}$$

Where Z_0 represents the characteristic impedance of the system, and Γ and Z apply for both device and circuit components. Due to equation (2.20), equation (2.15) can now be rewritten as the following:

$$\frac{1+\Gamma_d}{1-\Gamma_d}+\frac{1+\Gamma_c}{1-\Gamma_c} = 0, \quad for \quad \Gamma_d = \frac{Z_d-Z_0}{Z_d+Z_0} \quad and \quad \Gamma_c = \frac{Z_c-Z_0}{Z_c+Z_0} \tag{2.21}$$

With simplification, we arrive at oscillation condition using reflection coefficients:

$$\Gamma_d\Gamma_c = 1 \quad or \quad \Gamma_c = \frac{1}{\Gamma_d} \tag{2.22}$$

Therefore, since almost all resonator circuits are passive, we have $0 \leq |\Gamma_c| \leq 1$, which leads to $|\Gamma_d| > 1$. This latter criterion implies that the device is inherently unstable, since for unconditional amplifier stability, $|\Gamma_{IN}| < 1$, where Γ_{IN} (equivalent to Γ_d) represents the amplifier's (oscillator's) input reflection coefficient [2.8], which is synonymous to section 2.1. While omitting derivation, we can also conclude from [2.8] that for $|\Gamma_{IN}| > 1$ we obtain $R_{IN} < 0$. Thus, having $|\Gamma_d| > 1$ also implies $R_d < 0$, that is, in order to induce negative resistance from the device, it suffices to render it unstable at the desired port.

Stability and Noise

Stability and noise are not easily derivable using reflection coefficients. Using [2.6], Esdale and Howes obtained expressions for both stability and noise utilizing an approach similar to Kurokawa [2.7]. Again, assuming that the device reflection coefficient is a function of the RF current amplitude *B(t)* only, and that the circuit reflection coefficient is a function of the frequency ω only, we have the following expression of oscillator stability:

$$S = \left|\frac{d\Gamma_c}{d\omega}\right|\left|\frac{d\Gamma_d^{-1}}{dB}\right|\sin\theta > 0, \tag{2.23}$$

$$where \quad \Gamma_c(\omega) = \gamma_c(\omega)e^{j\psi_c(\omega)} \quad and \quad \Gamma_d(B) = \gamma_d(B)e^{j\psi_d(B)}$$

Several things were remarked when examining (2.23) [2.9]:

- An oscillator is clearly stable when the angle θ is between 0° and 180°;
- For noise analysis, the following expressions were derived by Esdale and Howes [2.6], expanded from Kurokawa [2.7]:

$$\left|\delta B(\omega_m)\right|^2 = \frac{\frac{1}{\gamma_c^2}\left|\frac{d\Gamma_c}{d\omega}\right|^2 2|b_n|^2}{|B_0|^2\frac{1}{\gamma_c^2}S^2 + \frac{1}{\gamma_c^4}\omega_m^2} \tag{2.24}$$

$$\left|\delta\theta(\omega_m)\right|^2 = \frac{2|b_n|^2}{\omega_m^2|B_0|^2}\frac{\frac{1}{\gamma_c^2}\left|\frac{d\Gamma_d^{-1}}{dB}\right|B_0|^2 + \frac{1}{\gamma_c^2}\left|\frac{d\Gamma_c}{d\omega}\right|^2\omega_m^2}{|B_0|^2\frac{1}{\gamma_c^2}S^2 + \frac{1}{\gamma_c^4}\left|\frac{d\Gamma_c}{d\omega}\right|^4\omega_m^2} \tag{2.25}$$

$$where \quad b_n = e^2|1-\Gamma_d|^2/4Z_0|\Gamma_d|^2 \tag{2.26}$$

From the noise expressions, an optimum noise performance, given the circuit's limitations, can be achieved through the following:

- Since the stability term of (2.23) appears in the AM and PM noise expressions, it is important to maximize that expression in order to minimize noise. The maximum value for stability is achieved when $\sin\theta = 1$, or $\theta = 90°$. Plotted on the Smith Chart shown in Figure 2.4, the circuit and inverse device reflection coefficient loci intersect in an orthogonal manner for minimum phase noise performance;

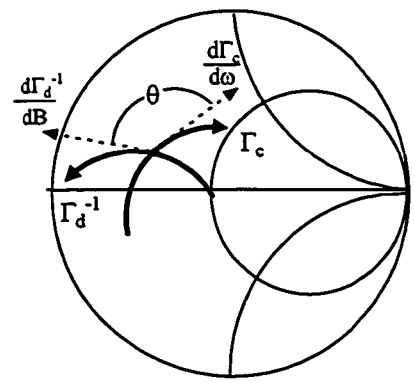


Figure 2.4: Loci of Γ_c and Γ_d^{-1} on Smith Chart

- In addition, $\left|\frac{1}{\gamma_c}\frac{d\Gamma_c}{d\omega}\right|$ takes on a maximum value. This implies that the slope of the circuit's reflection coefficient needs to be maximized, which is achieved through a high-Q resonator;
- Finally, $\left|\frac{1}{\gamma_c}\frac{d\Gamma_d^{-1}}{dB}\right|$ takes on a minimum value.

2.2.4 – 2-Port Negative Resistance Model

In order to achieve the negative resistance component, a transistor is used as an active device, with the 2-port S-parameters defined at microwave frequencies. This is an important step in gaining the required components of equation (2.15) and hence (2.22). The reader is referred to Appendix A.2 for more details.

2.3 – Oscillator Design Criteria

In this section, we will examine the most essential design criteria for oscillators in general, as well as the particular ones relating to this thesis. We will also define several design methodologies that will be adapted in the later sections.

2.3.1 – Small-Signal vs Large-Signal

With small-signal (linear) operation, frequency is taken as the main factor influencing circuit behavior, where for large-signal (nonlinear) operation, frequency and amplitude (power) are both considered to affect circuit behavior. As previously mentioned, the steady-state operation of the oscillator is under large-signal conditions, while its start-up operation is under small-signal conditions. For the first few cycles after being turned on, the start-up oscillator condition is being satisfied, where $Z_d(B)+Z_c(\omega) < 0$. As the signal amplitude grows, the device undergoes changes in its input and output impedances, in both magnitude and phase. This change brings forth a shift in oscillation frequency in order to satisfy the steady-state oscillation condition of $Z_d(B)+Z_c(\omega) = 0$. In the large-signal state, we are also able to predict oscillator stability, power, and harmonic content, which cannot be done by small-signal parameters [2.10]. Figure 2.5 (a)

illustrates the concept of operating point shift from small-signal to large-signal along with the parameters affected. Figure 2.5 (b) [2.7] shows the shift in device impedance with respect to amplitude in order to satisfy the oscillation condition at B_o, ω_o.

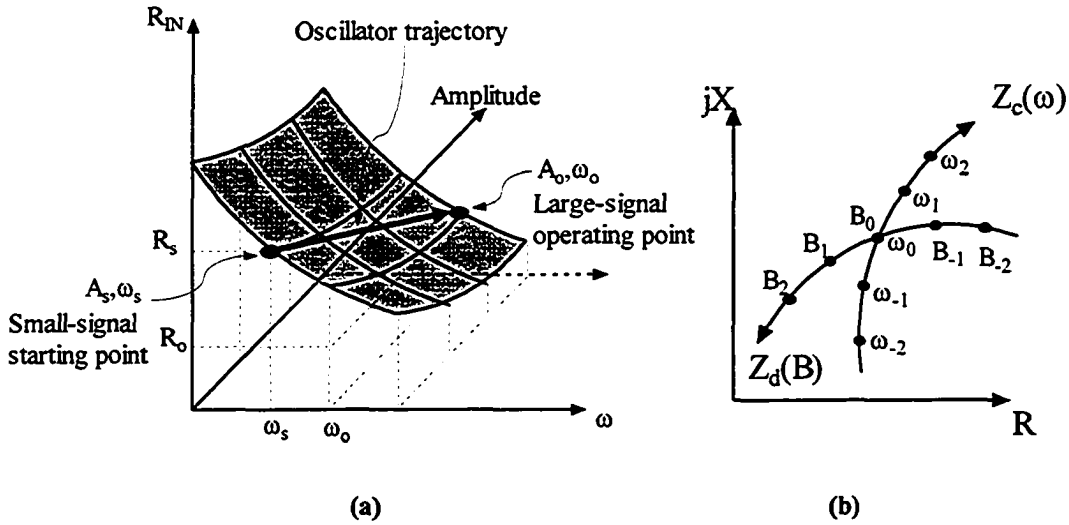


Figure 2.5: Operation point shift of oscillator (a) from small-signal to large-signal [2.10] (b) with respect to frequency and power [2.7]

2.3.2 – Phase Noise

Noise is inherently present in all electronic devices, whether active or passive. In an oscillator, composed mainly of an amplifier and a resonator, this amplified noise shows up at the output signal. From circuit theory, we know that a sinusoidal signal is composed of a linearly growing phase component, along side a randomly fluctuating phase component:

$$v(t) = v_s \cos[2\pi f_0 t + \Delta\phi(t)] \qquad (2.27)$$

Where $2\pi f_o t$ represents the phase component, and $\Delta\Phi(t)$ is the random phase noise. In the time domain, this can be observed as fluctuations of the zero crossings of the original signal, shown in Figure 2.6:

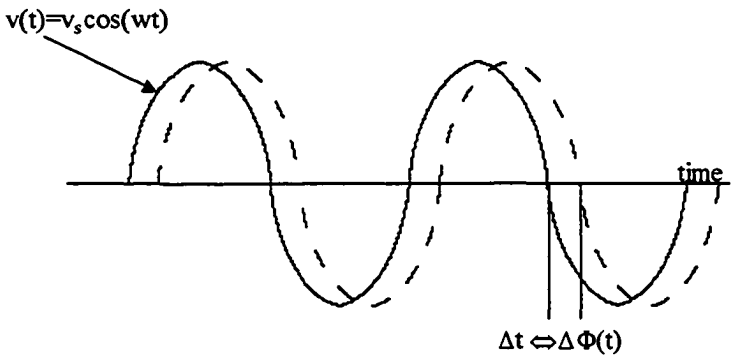


Figure 2.6: Signal fluctuations due to phase noise

As well, we also know that frequency and phase are related through the following:

$$f(t) = \frac{1}{2\pi}\frac{d\phi(t)}{dt} \tag{2.28}$$

Thus, any phase fluctuations, with respect to time, i.e. phase noise, are equivalent to frequency fluctuations with respect to time. In the frequency domain, the power spectrum is a common way to characterize the oscillator phase noise. This is accomplished through the measurement of RMS power versus frequency on a spectrum analyzer, provided that AM noise is insignificant in an amplitude-limiting active device.

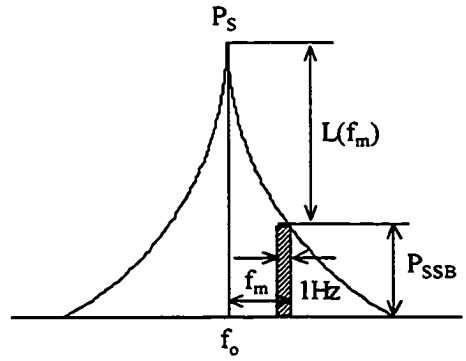


Figure 2.7: Power spectrum of a carrier signal

Thus, phase noise is single sideband (SSB) ratio of noise power in a 1-Hz bandwidth at f_m offset from carrier to carrier signal power, i.e. ,

$$L(f_m) = \frac{P_{SSB}(1Hz - BW)}{P_S} \quad dBc/Hz\ @ f_m Hz \qquad \textbf{(2.29)}$$

There are two ways of analyzing phase noise: the first one uses the age old Lesson's method along with its recommendations, while the second one most recent one, using Lee and Hajimiri's method along with its recommendations. For a detailed examination of Leeson's method, the reader is referred to Appendix A.3.

Leeson's Phase Noise Analysis [2.11] [2.12] [2.13]

For a total phase noise, the following expression is given:

$$L(f_m) = \frac{1}{2}\left[1 + \frac{1}{f_m^2}\left(\frac{f_0}{2Q_L}\right)^2\right]\frac{FkT}{P_{avs}}\left(1 + \frac{f_c}{f_m}\right)$$

$$= \frac{FkT}{2P_{avs}}\left[\frac{1}{f_m^3}\frac{f_0^2 f_c}{4Q_L^2} + \frac{1}{f_m^2}\left(\frac{f_0}{2Q_L}\right)^2 + \frac{f_c}{f_m} + 1\right] \quad (dBc/Hz) \qquad \textbf{(2.30)}$$

From the equation (2.30), we can see that there are two cases of interest with respect to phase noise response: for low-Q resonators, and for high-Q resonators. For the low-Q case, the phase noise will have a $1/f^3$ and a $1/f^2$ response from the above equation. For the high-Q case, the phase noise will now have a $1/f^3$ and a $1/f$ response near the carrier. This is illustrated in the following diagrams:

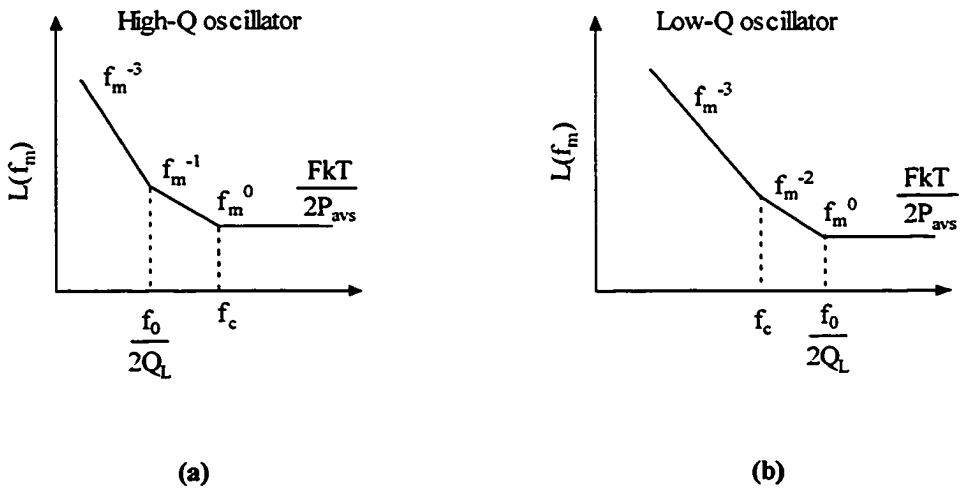


Figure 2.8: Oscillator phase noise (a) High-Q resonators (b) Low-Q resonators

If we closely examine each contributing noise term in the phase noise expression, we will notice several phase noise design rules:

1. $FkT/2P_{avs}$: This is the thermal noise floor and phase perturbation term, otherwise referred to as white PM noise. In order to minimize this term, we need to choose an active device with the lowest noise figure. As well, phase perturbations can be lessened by choosing high-impedance devices such as FETs, which exhibit a high SNR.

2. f_c/f_m : This is the flicker noise term, or flicker PM noise. This is device dependent, therefore it is recommended to choose a device with low flicker noise, i.e. low corner frequency.

3. $f_0^2 f_c/4Q_L^2$, $(f_0/2Q_L)^2$: This is the upconverted $1/f$ noise or flicker FM noise, and the thermal FM noise or white FM noise respectively. In order to reduce phase noise through this term, it is recommended that the unloaded Q of the resonator be maximized. As well, the resonator should be directly connected to the active device so that the resonator's energy is directly coupled. Attention should be paid to the loading effect of the resonator to the rest of the circuit.

Ali Hajimiri's and Tom Lee's LTV PN model [2.14] [2.15]

Another phase noise model has been recently put forth by Ali Hajimiri and Tom Lee. Although this model targets LC-tank type resonators implemented in IC technologies, several new and interesting points are worth exploring.

The theory is based on an impulse response model for phase noise. The oscillator is modeled as a system with n inputs for each noise source, while having 2 outputs: $A(t)$ representing the amplitude impulse response, and $\Phi(t)$ representing the phase impulse

response. Noise inputs can be current sources in parallel with circuit nodes, or series voltage sources in series with circuit branches. Let us consider the following circuit shown in Figure 2.9:

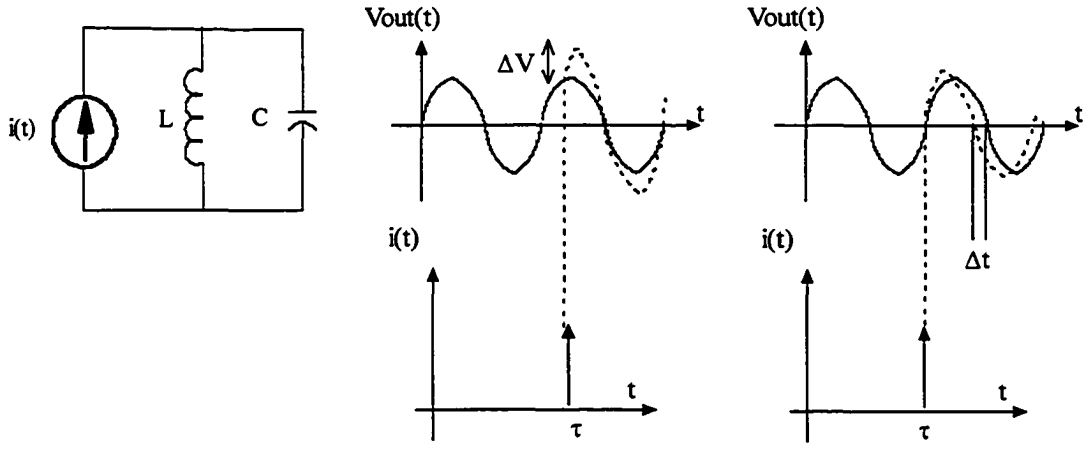


Figure 2.9: Circuit response due to an impluse input

Hajimiri and Lee noticed that if *i(t)* is applied at the peak of the tank voltage, then the phase noise is null and only the amplitude changes. However, if *i(t)* is applied at the zero crossing of the tank voltage, then phase noise is maximum. Due to amplitude limitations in the oscillator, any amplitude perturbation fades in time producing stable oscillation. On the other hand, phase perturbation results in a frequency step change as shown in the above Figure 2.9. This lead to the conclusion that this system is time dependent, and that its governing theory is based on that of an LTV (Linear-Time-Variant) system response. The model introduces the unit impulse response for excess phase as described by the following:

$$h_{\phi}(t,\tau) = \frac{\Gamma(\omega_0 \tau)}{q_{\max}} u(t-\tau) \qquad (2.31)$$

Where q_{max} = maximum charge displacement across the node capacitor where voltage changes are measured;

$u(t)$ = unit step function arising from the phase change due to an impulse input;

$\Gamma(x)$ = Impulse Sensitivity Function (ISF). It describes the sensitivity of the oscillator to a unit impulse with phase $\omega_o\tau$. It is a measured function ($\Gamma(x) = h_\Phi(t)C_{eq}V_{out}(t)$) that is proportional to $V_{out}(t)$

The following is given for the output excess phase term:

$$\phi(t) = \int_{-\infty}^{t} h_\phi(t,\tau)i(\tau)d\tau = \frac{1}{q_{\max}}\int_{-\infty}^{t}\Gamma(\omega_0\tau)i(\tau)d\tau \qquad (2.32)$$

Where $i(t)$ represents the injected noise current.

Since ISF is periodic, it can be expanded in a Fourier series:

$$\Gamma(\omega_0\tau)i = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos(n\omega_0\tau + \theta_n) \qquad (2.33)$$

Therefore, phase noise can be expanded into:

$$\phi(t) = \frac{1}{q_{\max}}\left[\frac{c_0}{2}\int_{-\infty}^{t} i(\tau)d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^{t} i(\tau)\cos(n\omega_0\tau)d\tau\right] \qquad (2.34)$$

The equation for the phase noise contains a harmonic generating expression, $\cos(n\omega_0 t)$, which also acts as a phase modulator turning excess phase into voltage. As an example, if we sequentially inject two separate sinusoidal signals $i(t)$ into the oscillator so that $i_0(t) = I_0\cos(\Delta\omega t)$ for n = 0 and $i_1(t) = I_1\cos[(\omega_0 + \Delta\omega)t]$ for n = 1 , where I is the maximum amplitude of $i(t)$ and $i_1(\omega) = \pm(\omega_o + \Delta\omega)$. Then, from the phase noise equation (2.34), we obtain the following corresponding output:

$$\phi_0(t) = \frac{I_0 c_0 \sin(\Delta\omega t)}{2q_{max}\Delta\omega} \quad (2.35)$$

$$\phi_1(t) = \frac{I_1 c_1 \sin(\Delta\omega t)}{2q_{max}\Delta\omega} \quad (2.36)$$

Where $\Delta\omega << \omega_o$.

For both (2.35) and (2.36), the resultant power spectral density function of $\Phi(t)$ will contain two impulses at $\pm \Delta\omega$. Thus, Hajimiri and Lee noticed that applying $i(t)=I_n cos[(n\omega_0+\Delta\omega)t]$ close to any integer multiple of the oscillation frequency will result in two equal sidebands at $\pm\Delta\omega$ in $S_\Phi(\omega)$. In order to measure phase noise however, the PSD of the output voltage, $S_{Vout}(\omega)$, is needed. From (2.27), it can be assumed that phase-to-voltage conversion occurs through phase modulation. Thus, if the conclusion of (2.35) and (2.36) are to be used, it can be shown that an injected current at $(n\omega_o + \Delta\omega)$ results in a pair of equal sidebands at $(\omega_o + \Delta\omega)$ in $S_{Vout}(\omega)$, with sideband power relative to the carrier given by:

$$P_{SBC} = 10\log\left(\frac{I_n c_n}{4q_{max}\Delta\omega}\right)^2 \quad (2.37)$$

The deductions of this theory indicate that time variancy in $i(t)$ and linearity in P_{SBC} (with respect to I_n) lead to better prediction of phase noise. LTI models and systems are limited in their analysis because they can only produce outputs at frequencies equal to the input frequencies and the system's poles. Therefore, they cannot explain the appearance of sidebands at $\Delta\omega$ close to the carrier from signals far off from the carrier, i.e. $n\omega_0+\Delta\omega$. This can only be justified by the LTV theory proposed above. As well, the prediction of amplitude sideband levels and their equality is different from the nonlinear mixing

phenomenon that appears in the conventional intermodulation of the active device's nonlinear voltage or current. Lee and Hajimiri's theory can be summarized in the following diagram Figure 2.10 :

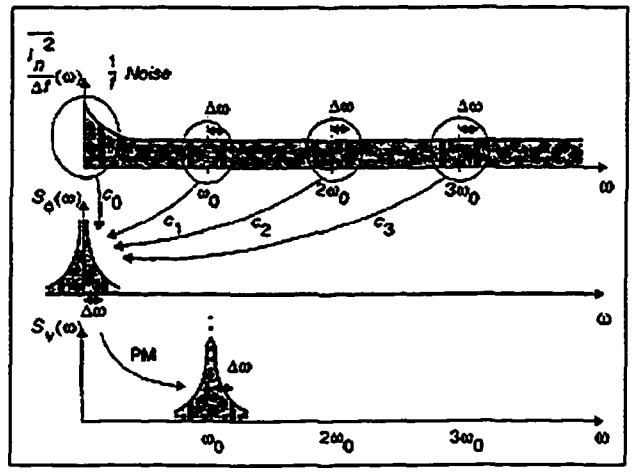


Figure 2.10: Harmonic noise translated to phase noise[2.15]

Finally, based on their assessment of phase noise, several proposals sprouted in order to reduce the effect of phase noise contributors:

1. From P_{SBC}, replacing q_{max} with $C_{eq}V_{swing}$, increasing the voltage swing at the resonator input will reduce sideband levels, and thus reduce phase noise degradation by a given noise source. This can be accomplished by evading supply-voltage or breakdown constraints through a tapped resonator to decouple the resonator voltage swings from device voltage limitations. Use of Clapp-oscillator, external AGC circuits, or differential oscillators is recommended.
2. Also from P_{SBC}, spurious interference in the vicinity of $n\omega_0$ should be minimized since this noise is downconverted to $\omega_0+\Delta\omega$. Power around integer multiples of

the oscillation frequency, i.e. $n\omega_0+\Delta\omega$, contributes significantly to close-in phase noise, more than any other frequency component.

3. Having a symmetrical waveform, with equal rise times and fall times along with a 50% duty cycle, will reduce the phase noise in the upconverted flicker noise region, i.e. $1/f^3$.
4. Signal power and resonator Q should be maximized. The energy returned by the active element should be delivered all at once, where the ISF has its minimum value, i.e. at the peak of resonator waveform. Consequenctly the transistor will act as an impulse current generator, waking up only on resonator voltage peaks.
5. Reducing the various coefficients c_n will reduce the overall noise contribution at all frequencies. This can be done by reducing the ISF, which is inherent to circuit configuration and performance.

The discussion on phase noise will be concluded by indicating that a study of low-phase noise design guidelines was undertaken concerning the integration of the recommendations from Leeson's phase noise theory with the ones from Lee and Hajimiri's theory along with the ones described by (2.33). A maximum signal power present at the resonator input along with a high-Q resonator is common to both Leeson and Lee *et al.* Furthermore, a high signal power is beneficial to phase noise in both theories, which might be accomplished by the "device-line" approach using the transistor's maximum P_{add} point. Obregon *et al.*[2.16] [2.17] were successful in implementing a low phase noise oscillator with the aid of a sapphire resonator, satisfying the high-Q condition, while operating the transistor at its maximum P_{add} point, satisfying

the signal power condition. However, their set-up involved a feedback, closed-loop, on-table oscillator with input and output tuners along with phase shifters. This allowed no power extraction, where phase noise was degraded once the loop was opened.

2.3.3 – Output Power

Output power is extremely difficult to predict, since the oscillator is a closed-loop circuit, as shown in Figure 2.11:

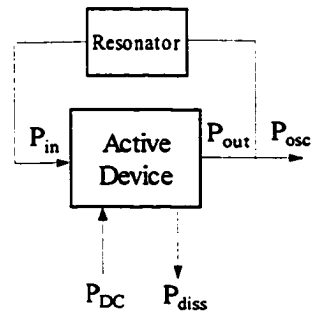


Figure 2.11: Power in oscillators

The closed-loop system predicts, as mentioned earlier, that the oscillator is a DC-to-RF power converter, where we have $P_{osc} = P_{DC} - P_{diss}$ when the energy conservation law is applied, emphasizing once again that oscillations are brought forth from the DC supply. However, output power may be determined by the power saturation properties of the amplifier and its compression characteristics. The difference in gain of the amplifier at startup and the amplifier in steady-state defines the amount of compression of the amplifier. The amount of compression will be an indicator of the output power the amplifier is able to produce. Thus, for a maximum output power oscillator, it suffices to operate the amplifier at the point of maximum efficiency, where $(P_{out} - P_{in})$ is maximum, i.e. just before compression.

2.3.4 – Oscillator Figure of Merit

Since oscillator design is widely varied in terms of design criteria and parameters, it is difficult to assess their performance in a comparative manner. Tiebout [2.18] compiled a figure of merit to quantitavely describe a circuit's operation:

$$FOM = 10\log\left[S_{SSB}(linear)\left(\Delta f / f_o\right)^2 P_{vco}(mW)\right] \qquad \textbf{(2.38)}$$

This generated a comparable value system where oscillators can be evaluated within theiir own design criteria. However, this quantity is geared towards monolithic CMOS designs where power consumption is minimized. For other devices, such as GaAs, output power should be factored into the expression.

2.4 – Conclusion

This chapter has reviewed fundamental oscillator principles starting from circuit feedback theory and ending at microwave negative resistance theory. The device-line technique has been mathematically presented. Based on this formulation, the basis for orthogonal intersection between device-line and resonator locus on the Smith Chart was established. Finally, two phase noise models have been examined and their resulting design guidelines highlighted. This partially fulfills the first thesis objective.

CHAPTER 3

DESIGN AND IMPLEMENTATION OF OSCILLATOR CIRCUITS

In this chapter, we will review the literature regarding several methods of oscillator design. As well, the parameters influencing the various oscillator design specifications will be examined. This will pave the way for discussions about design approaches adopted for microwave oscillators. A section on the design of the employed resonator is also included, with a brief description of the material (LTCC) used for its implementation. Finally, the design procedure is presented and outlined for the given resonators. It is approached in a methodical way, and each step is simulated using the CAD tool of choice, ADS™ by Agilent Technologies. The procedural design steps are presented, and based on the simulation results, several designs are duly chosen to be fabricated for verification.

3.1 – Oscillator Design Approaches

3.1.1 – Literature Review

We will begin our look at various oscillator design approaches with a broad literature review. Since oscillator design has been undertaken for some time, there are numerous papers on such design and implementation. We will highlight the most influential ones in general, and for this work in particular.

In the days of yore, oscillators used to follow mythical design procedures based on "black magic",. Since then, there has been great advancement in the area of systematic approach to the design process. A multitude of design methods have been implemented with a highly successful "first-time" rate, based on various criteria. These approaches are either classified as small-signal (linear) S-parameters emphasizing start-up conditions, or large-signal (nonlinear) S-parameters emphasizing steady-state conditions. Despite their implementation simplicity due to the readily available S-parameters from device manufacturers, small-signal linear designs remain nonetheless rough approximations. Their inaccuracy stems from the large-signal operation of the oscillator at steady-state which results in frequency shifts from the originally targeted frequency. As well, linear design procedures are incapable of predicting oscillator power and phase noise. However, their quick turnaround time and their relative simplicity usually compensates for their imprecision. The following Table 3.1 highlights some of the most noted oscillator design procedures examined for this thesis [3.1]:

Table 3.1: Literature review for microwave oscillators

Design Methodology	Author(s)	Year published	Reference
Small signal	Wilson *et al.*	1989	[3.1]
	Boyles	1986	[3.2]
	Esdale *et al.*	1981	[2.6]
	Golio *et al.*	1989	[2.10]
	Basawapatna *et. al*	1979	[3.3]
	Randal and Hock	2001	[3.4]
Large signal	Pucel *et al.*	1975	[3.5]
	Abe	1986	[3.6]
	Johnson	1979	[3.7]
	Wagner	1979	[3.8]
	Rauscher	1980	[3.9]
	Kotzebue	1984	[3.10]
CAD	Gonzalez	1998	[3.11]
	Liu *et al.*	1999	[3.12]
	El-Tager *et al.*	2000	[3.13]

Small signal design approach

As mentioned above, almost all small-signal design procedures rely on active device S-parameters in order to obtain the conditions for oscillation. This involves turning the 3-port stable active device inherently into a 2-port device, then into a 1-port de-stabilized device presented to the resonator. The de-stabilization usually occurs via either series or parallel feedback of the active device. Once de-stabilized, the negative impedance oscillatory model or the reflection model outlined in section 2.2.4 is then employed by most of the above design procedures in order to ensure oscillation start-up. In Wilson *et. al* and Boyles, the procedures are accurate enough to predict correct

frequency oscillations within 5%, along with frequency stability and low noise. Randal and Hock obtained quantitative expressions that characterized oscillator performance in terms of open-loop linear S-parameters, along with an oscillator stability equation. Basawpatna outlines a wideband microwave oscillator design procedure utilizing small signal analysis. As well, a load-pull setup is employed in their procedure to predict viable "real-world" impedance loads that can be attached to the circuit. Similarly, Golio *et al.* also used a combinational method, where a design procedure which used aspects of both small and large signal analysis techniques was adopted. In both cases, the use of a combinational small-signal and large-signal design methodology resulted in better design results. Nevertheless, small-signal design procedures suffer from the inability to accurately estimate oscillator performance, such as oscillation frequency, output power, and phase noise.

Large signal design approach

There are a number of different large signal design approaches for oscillator design based on its nonlinear behavior and various device simplifications. Mostly all design approaches are mainly geared for predicting the correct power levels and frequency of oscillation.

Pucel *et al.* devised an "***Output Power vs Input Power***" design approach where the active device in the oscillator circuit, namely the amplifier, was characterized in terms of its power performance. P_{in} vs P_{out} of the amplifier was measured well into the nonlinear region, and based on the feedback topology of the oscillator, they concluded that $P_{osc} = P_{out} - P_{in}$, while the maximum oscillator power is evaluated by dP_{osc}/dP_{in}.

Johnson outlined the "*Gain Saturation Approximation*" method, where it is assumed that the device's S_{21} is the only parameter that undergoes any significant change under large signal conditions. Thus, a model of the device is built around small-signal S-parameters except for S_{21}, where an approximate large signal equivalent is chosen, and hence the oscillator is designed based on power prediction. The difficulty in this approach is the approximation of the large signal behavior, where it is assumed that the device power is exponential.

Abe provides a similar method to Johnson, except that the entire device's S-parameters undergo changes at large signal. Thus, he used the small-signal parameters to model the large signal behavior of the device to gain insight into the transistor's large signal operation. Based on that, the resulting voltages and currents are used to synthesize the feedback network and complete the oscillator. This procedure is also difficult to undertake due to the derivation of a parameter-specific device model and its nonlinear operation.

Wagner uses a "*Device Line*" technique also utilizing the large signal device saturation approach, where the device's input impedance is measured versus input power as the device saturates. The device's impedance that corresponds to the maximum output power is used to satisfy the oscillation condition outlined in section 2.2.4. This method experiences problems in terms of oscillation start-up since most often the device's impedance at small-signal differs from its equivalent at large-signal.

Rauscher and Kotzebue wrote two classic papers about using large signal S-parameters for oscillator synthesis. Rauscher used Johnson's exponential saturation approximate model in order to devise equations for device voltages at maximum output power. With

the device voltages and currents known, a load line can be obtained, and thus a feedback network can be synthesized. Kotzebue also used Johnson's analysis as a base for his approach, where the transistor's port voltages and currents are found to maximize the amplifier's added power. Thus, it is assumed that these voltages and currents remain intact when the amplifier is transformed into an oscillator, is the latter synthesized with maximum output power.

CAD approach

With the recent advancement of available CAD tools to the engineering community, oscillator design has taken on a more systematic and focused approach since 20 years ago. The myriad of CAD tools are often used to produce "first-time" accurate designs ready for fabrication. The tools are able to simulate a variety of measurable results such as power, frequency, phase noise, harmonic distortion, and stability. However, the CAD tools are only as accurate as the models used in the simulation process. From Table 3.1, Gonzalez presented a CAD design procedure for appropriate series-feedback network selection to produce required negative resistance. This method can be conveniently used with small-signal for large-signal device models in order visualize the feedback effects. Liu *et al.* presented a graphical determination for the startup of oscillations by examining the stability criterion of the active device on the Smith Chart. This ensued a design geared towards small-signal, but it could also be extended to large-signal in order to ensure that the oscillation condition remains satisfied. Finally, El-Tager described three CAD-based methods for designing microwave

oscillators (linear, quasi-linear, and nonlinear) with a simulation results comparison of the three methods. The author concluded that the harmonic balance approach based on nonlinear simulations was the most accurate design resulting in a 0.4% deviation only.

3.1.2 – Active Device Selection

Having examined Leeson's phase noise formula in section 2.3.2, we will restate the factors that influence phase noise in oscillators, as well as expand the analysis to include surrounding circuit parameters. These factors will be taken into consideration when applying the design methodology.

In Leeson's formula, we learned there are a number of sources influencing the behavior of phase noise. It was concluded that maximizing the resonator's unloaded Q, while making sure that its coupling loss is minimized is an important requirement. Thus, a high-Q resonator, to be discussed in section 3.2.1 below, was implemented and used in this thesis as part of the low noise design requirement. Furthermore, the choice of the active device is another important requirement. Here, a device exhibiting a low noise figure as well as a low corner frequency is highly recommended to further reduce the phase noise.

There has been a multitude of studies done on the corner frequency of various active devices. Most of the results have shown that bipolar transistors have lower corner frequencies than most FET devices, with silicon being the best performer. This is due to the single crystalline structure composition of silicon, allowing for the lowest flicker frequency [3.14]. As well, with the improvement of SiGe processes today, corner

frequencies have reached enough low levels for high f_t BJT devices available for RF frequencies. On the other hand, FET devices have a higher f_t , and thus are preferred for microwave and millimeter-wave frequencies. But, FETs, mostly GaAs and HEMTs contain higher impurities, and thus exhibit a higher corner frequency. Thus, from an initial analysis, a Si BJT device would be a preferred active element for low-noise. However, also from Leeson's formula, a device that demonstrates high impedance at the resonator port and in turn a low noise figure is also preferable in order to make the SNR (Signal-to-Noise Ratio) as high as possible, reducing the phase perturbation. FETs, due to the absence of shot noise, possess such characteristics and are ideal for this scenario. A high SNR, i.e. low NF, is critical when the device operates in compression as the oscillator does, because the noise figure is increased by the same amount of compression the amplifier is in. Thus, the SNR of an oscillator is reduced by the amount indicated by the noise figure [3.14].

Consequently, taking all of the above factors in consideration, along with the availability of complete device models set for simulation at the frequency of choice, three different transistors from Agilent technologies were considered [3.15]: ATF-33143, ATF-34143, and ATF-35143. The ATF-3x series is a dual supply PHEMT FET device with gate width of 1600μm, 800μm, and 400μm respectively. Table 3.2 below illustrates a comparison between the transistors in question:

Table 3.2: Comparison between Agilent transistors

Transistor / Parameter	ATF-33143 @V_{ds}=4V, I_{ds}=80mA	ATF-34143 @V_{ds}=4V, I_{ds}=60mA	ATF-35143 @V_{ds}=2V, I_{ds}=15mA
Model	Spice +S-parameters	Spice +S-parameters	Spice + S-parameters
Noise	Yes	Yes	Yes
G_a [dB] @ 2GHz	15 dB	17.5	18 dB
gm[mS]= I_{dss}/V_p	440	230	180
F_{min}[dB] @ 6GHz	0.9 dB	0.8	0.7 dB
G_a [dB] @ F_{min}	10 dB	11.5	13 dB
P_{1dB}[dBm]	25	20	10

Considering all the above criteria as well as the available transistor data, it was decided that the ATF-35143 PHEMT transistor offers the best compromise between low noise figure, available gain, and output power. The remainder of the simulations and measurements will be carried forward utilizing this transistor. The nonlinear Statz model supplied by Agilent Technologies stipulates 6 GHz as the maximum frequency for simulation. However, with the availability of the transistor's measured data beyond this frequency, the model was modified in order to operate it up to 10 GHz. The datasheets and model are in Appendix B.

3.1.3 – Common Oscillator Topologies

The most common oscillator topologies available for circuit designers are either the common emitter/source (*CS*) or the common base/gate *(CG)* topologies, shown in

Figure 3.1. The common collector oscillator uses capacitive series feedback through C_f to create a negative resistance looking into the base of the transistor, while the common base oscillator uses an inductor, L_f, in the base of the transistor to create a negative resistance looking into the emitter of the transistor.

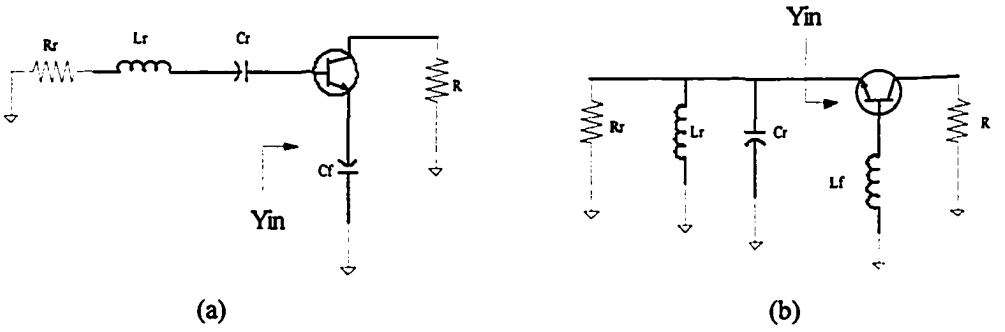


Figure 3.1: Common oscillator topologies (a) Common-emitter/source (b) Common-base/gate

There are several advantages and disadvantages for each configuration, which contribute to the choice of topology. According to [3.16], the negative impedance bandwidth of a *CS* transistor. with a capacitive loading at the source (C_f) extends from $f_{min} = 0$ Hz up to

$$f_{\max} = \frac{1}{2\pi C_d}\sqrt{\frac{C_d g_m + (1+R_o g_d)(g_m C_f - g_d C_g)}{C_g R_o}}Hz \qquad (3.1)$$

On the other hand, the negative impedance bandwidth of a *CG* transistor, with an inductive loading at the gate (L_f) extends from the following frequency ranges:

$$f_{\min} = \frac{1}{2\pi\sqrt{L_f C_g}}Hz \qquad (3.2)$$

$$f_{\max} = \frac{1}{2\pi}\sqrt{\frac{-\beta_G + \sqrt{\beta_G^2 - 4\alpha_G\varepsilon_G}}{2\alpha_G}}Hz, \qquad (3.3)$$

Where

Where the $\alpha_G = C_d^2 C_g R_o L_f, \beta_G = L_f C_g g_d(1+R_o g_d) - C_d^2 R_o, \varepsilon_G = (1+R_o g_d)(g_m g_d)$ variables in (3.1)-(3.3) represent device-specific model components.

Thus, both bandwidths depend on the choice of feedback element as well as the device parameters. From this standpoint, an advantage of the CG topology is its wider negative resistance bandwidth when compared to the CS topology. As well, with the CS topology having high input impedance, it is much preferable to use the CG topology to generate stronger negative resistances at the source. Thus, strong negative resistance can be easily achieved with minimal series feedback, improving the power performance of the oscillator. Finally, inductively loading the gate of the pHEMT also allows for an easier gate DC bias integration. On the other hand, a disadvantage of the CG topology is its inferior frequency stability due to the poor isolation between gate and drain, which might lead to undesired frequency hopping [3.21].

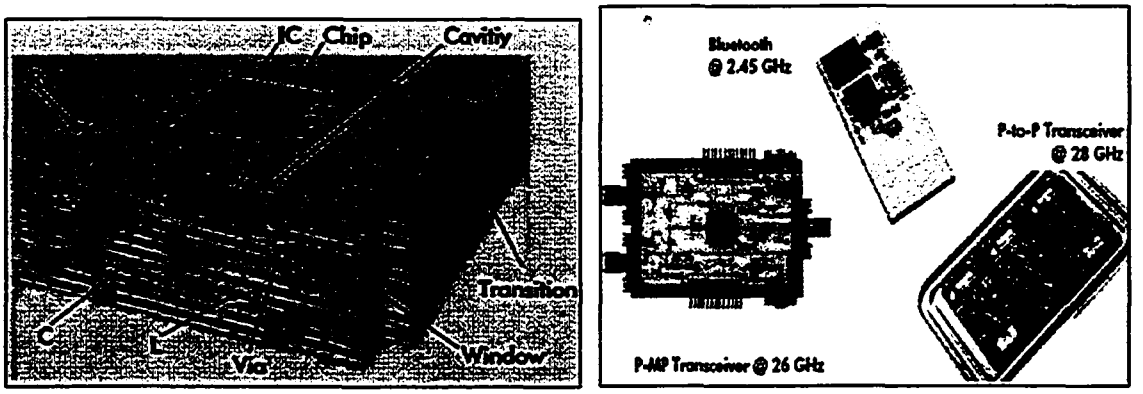
3.2 – LTCC : Low Temperature Cofired Ceramic

3.2.1 – What Is It?

The resonator included in this thesis is an integral part of the hybrid oscillator, and thus it will be described in this section. However, a concise discussion about LTCC will first be given before the oscillator description.

LTCC(Low Temperature Cofired Ceramic) was first introduced to the electronics world in 1999. Its high performance technology along with its low-loss characteristic as well as its minimal size made it extremely attractive not only to circuit designers but to layout engineers as well. Conventional RF and microwave circuits have been using the available 2-D layout space of the material of choice. Spiral inductors and interdigitated capacitors are not attractive at either end of the frequency spectrum either due to their

very large or very small size. LTCC offers a compact and cost-effective manufacturing option utilizing the z-dimension (typically used are 10-12 layers between 1-1.5 mm) as a third dimension, resulting in 3-D layout space offering flexibility and performance compared to designs restricted to 2-D. LTCC offers smaller area improvements for not only planar designs, but, it also permits the embedding of passives (resistors, capacitors, inductors) while interconnecting the multilayers through vias. The unique feature of LTCC is its ability to miniaturize bulky microwave circuits, i.e. conventional waveguides, into 3-D equivalents with horizontal conducting surfaces as printed metallization, and vertical conducting surfaces realized as via fences. As well, LTCC is very well suited to incorporate several different modules (ICs, flip chips, etc..) onto one package in order to complete a Multi-Chip-Module (MCM). This method also eliminates the need to complement circuits with off-chip components thus improving performance [3.17]. Beside its size advantage and highly dense integration capability, LTCC is also robust against mechanical stress/shock and temperature fluctuations, making it ideal for space-type applications. Figure 3.2 (a) below illustrates the multi-dimensional facet of an LTCC module, while Figure 3.2 (b) provides several LTCC type circuit examples.



(a) (b)

Figure 3.2: LTCC circuits (a) Core composition (b) Examples [3.19]

LTCC has become part of a circuit packaging revolution that is geared towards a System-on-Package (SOP) conversion, where it is expected to lead to microminiaturized and convergent systems with RF/microwave (including integrated antennas), photonics, MEMS, and even digital modules, all being included in a single component system [3.18].

The LTCC manufacturing process is outlined in Figure 3.3. As can be seen, the automated process is composed of several steps, mainly involved in the manufacturing of the circuit. The core element of the LTCC process is the "green" dielectric tape, which is very malleable and flexible. The tape is cut into blanks to the appropriate size of the designed module. The vias, along with any cavities, are then punched accordingly, and filled with conductive material (silver or gold paste). The following step involves the circuit printing of the conductors on all the proper layers, which are then assembled to be laminated accordingly under specified pressure.

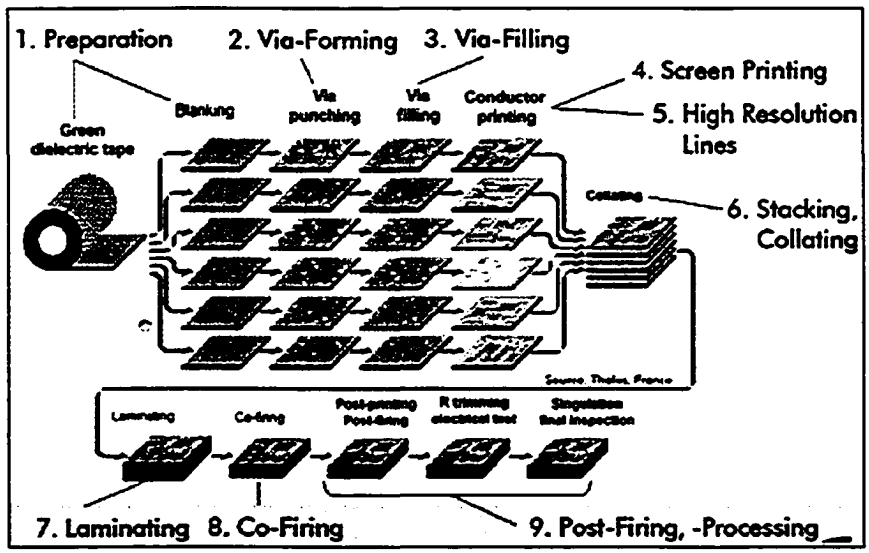


Figure 3.3: LTCC manufacturing process [3.19]

The final step involves co-firing the laminates at a temperature of about 850°C, for post-examination of any inadequacies. Lastly, SMTs are soldered or bonded, while chips are then placed inside cavities and interconnected to the rest of the module.

On the other hand, LTCC suffers from several disadvantages worthy of mentioning. One major deficiency is the shrinkage that occurs in the x, y, and z directions upon firing, where up to 15% shrinkage can be seen in the z-direction, and up to 13% in the x-,y-direction. The shrinkage in the x-direction can lead to defects such as misalignment of via posts, while shrinkage in the z-direction may lead to "posting", where the via hole shrinks while the paste filler remains of the same height causing uneven surfaces As well, LTCC packages are poor conductors of heat, and thus require a transfer mechanism to a core heat sink on the top of the package [3.20].

3.2.2 – LTCC Resonator

The resonator used in this thesis as part of the low-noise oscillator investigation was realized in LTCC, following the design guidelines and procedures outlined in previous work at Carleton University [3.21]. One of the main goals of that research was the investigation of several LTCC-based resonators, in order to establish a high-Q best design case for Ka-band applications. A cylindrical resonator shape was adopted due to an almost 50% size reduction when compared to rectangular resonators, offering a substantial saving in manufacturing cost. It was also found that a cylindrical resonator containing a rectangular air cavity, with various proportions of air and dielectric fillings, produced very good results. Figure 3.4 shows the basic geometry of the cylindrical resonator operating in the TM_{010} mode:

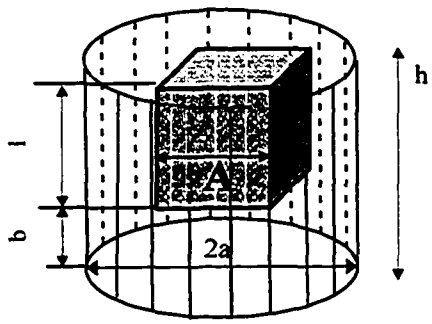


Figure 3.4: Illustration of resonator structure

Where: h = height of cylindrical resonator;

$2a$ = Cylindrical resonator diameter;

A = Length, width, and height of air-filled cavity;

l = height of air-filled cavity;

The air cavity is centered in the horizontal dimension of the resonator. The cavity extends vertically a distance l from the top of the resonator. All outside cylindrical surfaces are metallized, and except for the air cavity, the structure is dielectric-filled. Thus, we have:

$b = t * n_{diel}$, where t represents layer thickness and n_{diel} represents the number of dielectric layers;

$l = t * n_{air}$, where n_{air} represents the number of air layers;

$h = t * (n_{air} + n_{diel})$.

An LTCC implementation of the described resonator is depicted in Figure 3.5. The details of the feeding mechanism and the excited TM_{010} mode are given in [3.21].

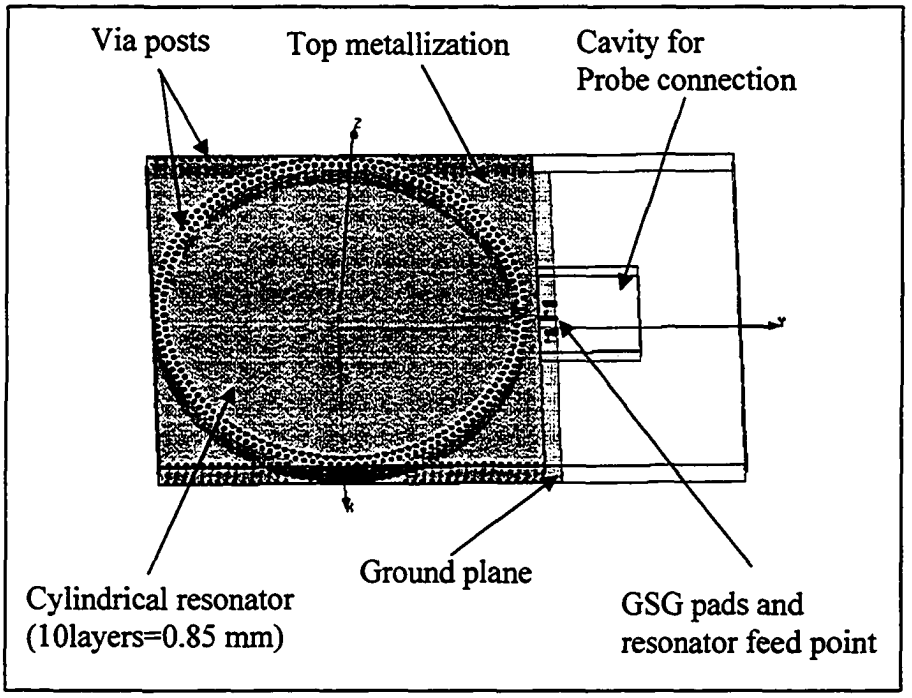


Figure 3.5: LTCC resonator structure for simulation and fabrication

Several conclusions were drawn from the work mentioned previously [3.21] with regard to achieving high Q's, and they are summarized as:

- Use of LTCC materials with the lowest possible material loss;
- Staggered double via walls, instead of single in order to contain more fields inside the resonator and minimize radiation loss;
- Use of the largest possible air-filling to decrease dielectric losses dramatically;
- Use of all possible layers to build the resonator to maximum height, while allowing only one layer for the excitation mechanism.

Table 3.3 lists the main results achieved at Ka-band from [3.21]:

Table 3.3: Summary of best LTCC resonator results from [3.21]

Resonator Type*	Size and Dimensions (mm x mm)	f_0 [GHz]	Q_0
Rectangular (dielectric-filled)	3 x 5	21.27	335
Rectangular (air-filled cavity)	9 x 11	19.81	1206
Cylindrical (air-filled)	Diameter = 7	23.96	840

* LTCC ceramic layers having $\varepsilon_r = 6$

For C-band operation, one can easily deduce through scaling that the required dimensions in $\varepsilon_r = 6$ material system would be increased by a factor of about 6, representing a significant additional cost. Hence, reported in this thesis for the first time are results of LTCC resonator structures realized in a very high dielectric constant material in order to achieve further size and cost reductions.

The dielectric material used for the resonator employed in this work were $\varepsilon_r = 68$ and $tan\delta = 0.00173$, while the conductor of choice was silver paste with conductivity $S = 61$ **MSiemens/m**. These are new (pre-commercial) materials employed in a research-based LTCC fabrication process which may become available in industrial processes in the future. A first principle approach was adopted in developing the resonators in use here, based on the design recommendations outlined in [3.21]. Accordingly, the 1st mode of resonance (TM_{010}) frequency of a cylindrical resonator is given by:

$$f_o = \frac{2.405}{2\pi a\sqrt{\mu\varepsilon}} \tag{3.4}$$

Where a represents the radius of the cylinder, ε is the permittivity of air and μ is the permeability. We also deduced that the frequency and material differences are related by the following:

$$f_{02} = \frac{a_1}{a_2}\frac{f_{01}}{\sqrt{11}} \tag{3.5}$$

Where f_{01} and a_1 represent the target frequency and corresponding cylindrical radius in [3.21], while f_{02} and a_2 represent the target frequency and corresponding cylindrical radius for this work. From here, aided by the design in [3.21] with f_{01} = 23 GHz and a_1 = 3.5 mm, a baseline structure having f_{02} = 4 GHz and a_2 = 6.1 mm was utilized as a first design.

3.2.3 – Experimental Results

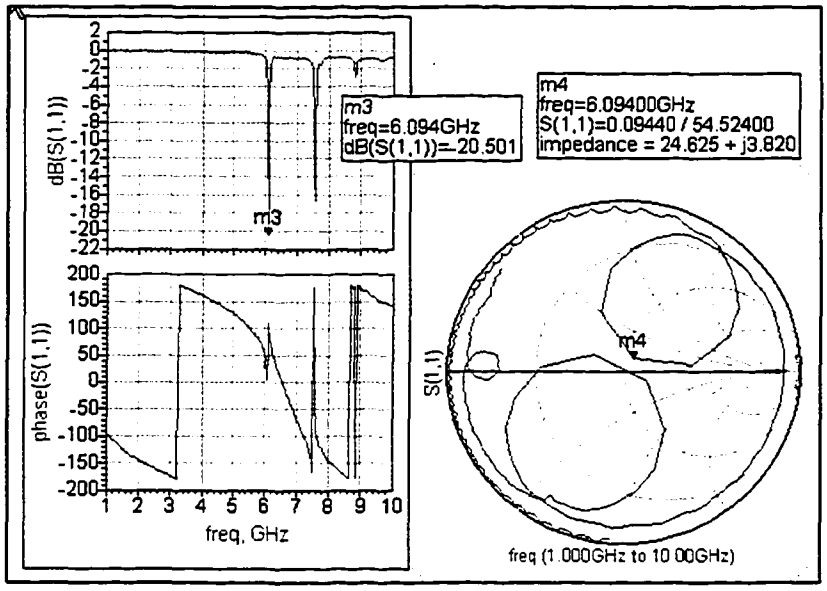
Thus, several resonators were designed, simulated, and built, with Table 3.4 summarizing the results of the highest Q structures. Of note, the excitation scheme used in the resonators consists of a center strip of Coplanar Waveguide (CPW) line terminated with a loop via extending all the way to the top metal layer of the resonator, as shown in Figure 3.5. This is a new excitation scheme that combines the TEM wave excitation method of a CPW with the resonator loop coupling mechanism.

Table 3.4: Summary of LTCC resonator designs

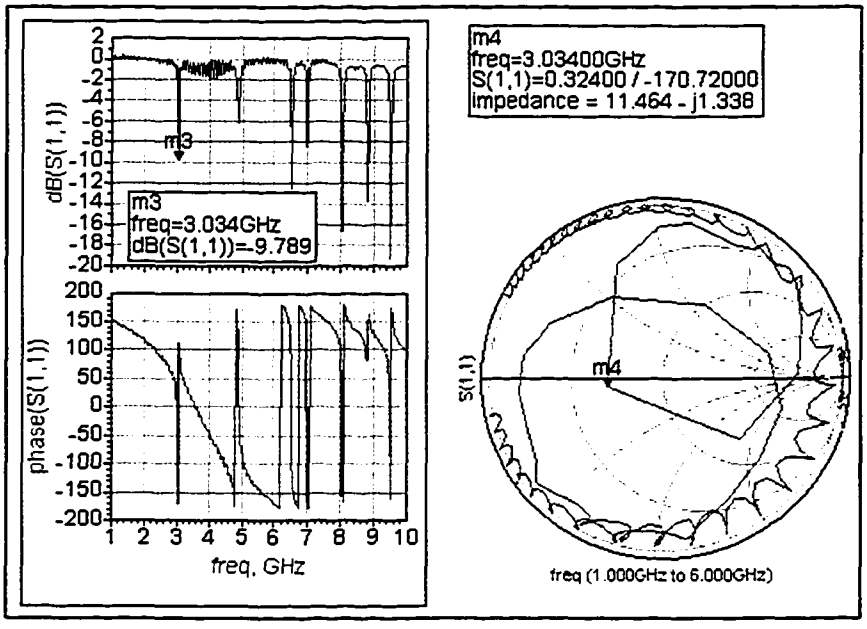
Parameter / Design		Diameter (mm)	Predicted f_o [GHz]	Predicted Q_o	Measured f_o [GHz]	Measured Q_o
No air cavity	**Design #2**	10.23	4.0	305	3.034	166(O)
With air cavity 5.8x5.8 [mm^2]	**Design #4**	11.64	4.0	285	6.094	127(U)

O = Overcoupled
U = Undercoupled

Using HFSS© by Ansoft Technologies, the simulated resonant frequency and unloaded *Q*-factor values were obtained using an eigen-mode analysis, omitting the excitation mechanism's influence. On the other hand, the measured resonant frequency and unloaded *Q*-factor values were obtained from the measured *S*-parameters, shown in Figure 3.6 below, using the techniques described in [3.22], [3.23].



(a)



(b)

Figure 3.6: S-parameter measurements of resonator #2 and #4 in Table 3.4

Comparing the measured results to the predicted values, several discrepancies were noticed. The most significant difference is in the Q-factor value for most of the

resonators. This can be attributed to the coupling approach employed by the resonators studied here, compared to [3.21]. As mentioned before, the mechanism used here is a combination of CPW along with loop excitation. Along with its advantages, this method also offers several disadvantages including the significant loss of a microwave signal due to the vertical transition between a CPW and a via [3.24]. As well, due the CPW feed, the probe's position was not necessarily optimal for Q performance [3.25]. From Table 3.4, we can reinforce the conclusions in [3.21], that the introduction of an air cavity in a cylindrical resonator resulted in a shift of the target frequency, confirming the existence of ε_{eff} and $f_{o,eff}$, the effective dielectric constant and the effective frequency due to the insertion of an air cavity.

Several other structures were characterized with their S-parameter response, but resonators #4 and #2 were chosen as the most promising resonators that will be able to fulfill the design strategy of high-Q chosen for this work. The oscillators in the next sections are designed based on their resonant properties. Hence, Figure 3.6 represents the measured corresponding S-parameters, while Figure 3.7 shows a photograph of the fabricated modules. A lumped element equivalent circuit was needed, able to reproduce the resonator's behavior to include it in the nonlinear oscillator simulation.

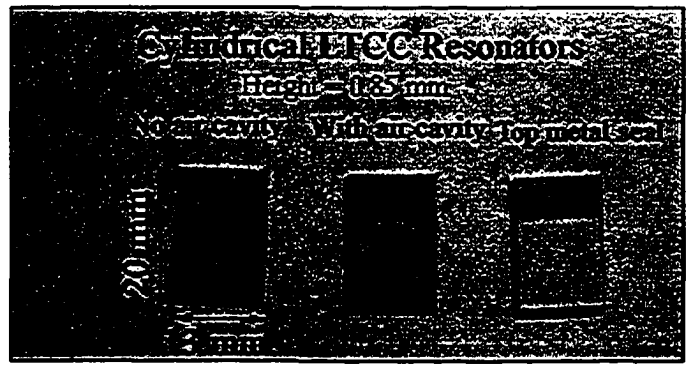


Figure 3.7: LTCC fabricated resonators

3.2.4 – Resonator Lumped Element Model

Resonators often exhibit a predictable response when measuring their *S*-parameter values near resonance. Also, since waveguide and cavity resonators are 1-port devices, it is valuable and simple to create an equivalent lumped element circuit that models the resonator's behavior near resonance, in order to better apply them in circuit simulations. It is well known that all resonators can be represented by either a lumped element series or parallel RLC circuit in the vicinity of their resonant frequency. The representation of a resonator with lumped elements is shown in Figure 3.8:

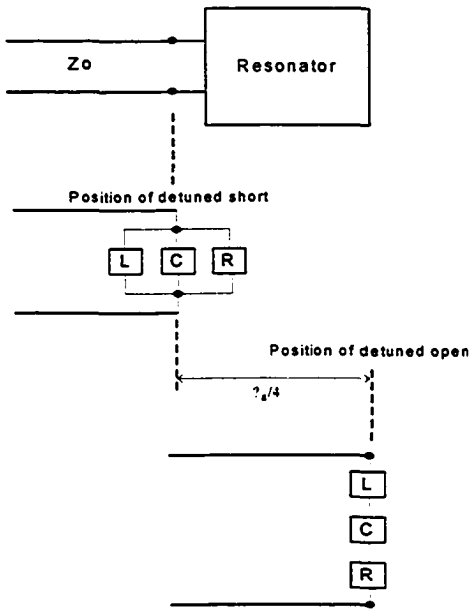


Figure 3.8: Equivalent lumped element circuit model for resonators

As can be seen from the Figure 3.8, the resonator needs to be firstly characterized at its ports in terms of detuned short (DS) or detuned open (DO) to determine the type of circuit that accurately models it. In this exercise, special attention must be paid to the resonator's reference plane, ensuring its exclusivity of any feed network. If the reference plane of the resonator is taken to be at the detuned short, then a parallel RLC-circuit is the

appropriate choice. On the other hand, a series RLC-circuit should be used if the detuned open position is chosen as the reference plane. The relationship between both reference planes is nothing more than a λ/4 revolution on a Smith Chart. Several ways are available to determine the appropriate reference plane of the resonator, and the simplest one is illustrated in Figure3.9 below:

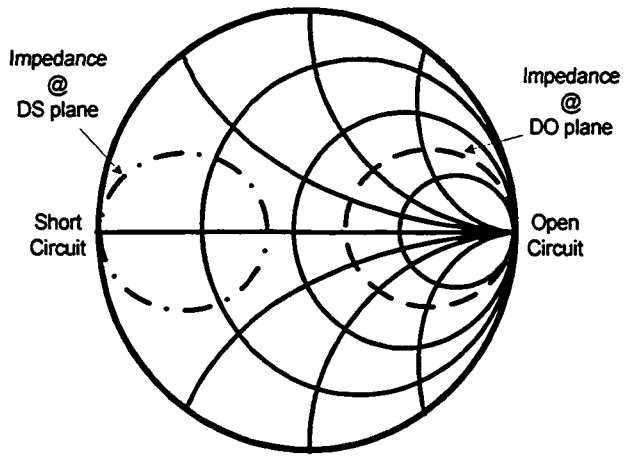


Figure 3.9: Impedance contours of DS and DO resonators

The Smith Chart (SC) above contains two impedance contours, one referring to the DO plane at the right hand side of the SC near the open circuit point, while the other referring to the DS plane at the left hand side of the SC near the short circuit point. The impedance contours are obtained by de-embedding the resonator cavity from any feed mechanism. The de-embedding process involves shifting the reference plane of the measurement apparatus from the lead of the feed network, i.e. CPW in this case, to the edge of the excitation edge, where we have:

$$\Gamma_{in}(d) = \Gamma_0 e^{-j2\beta d} \qquad \textbf{(3.6)}$$

Where β is phase constant, d is the length of the feed network to be de-embedded, and βd is the feed's electrical length.

Thus, once a reference plane is chosen and hence an equivalent circuit type is determined, the circuit values can be obtained by another resonator characteristic. The coupling mechanism's effect on the resonator is classified into three categories:

(1) **under-coupled**, when the resonator's Γ locus excludes the origin of a SC;

(2) **over-coupled**, when the resonator's Γ locus includes the origin of a SC;

(3) **critically coupled**, when the resonator's Γ locus passes through the origin of a SC.

Once the condition of coupling is known, the normalized resistance R can be calculated from the VSWR [3.26]:

R = VSWR ≥ 1 @ resonance for over-coupling;

R = 1/VSWR ≤ 1 @ resonance for under-coupling;

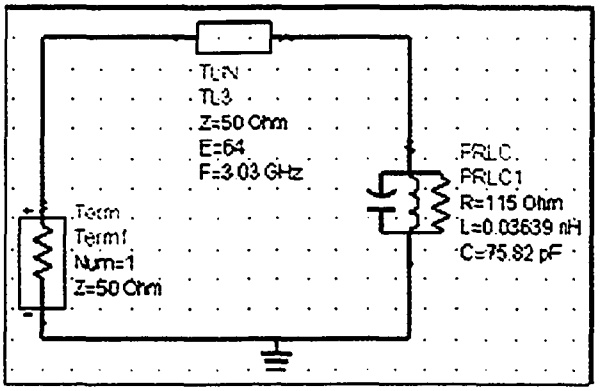
R = VSWR = 1 @ resonance for critical-coupling.

Consequently, for a series-RLC circuit, we have the following [3.27]:

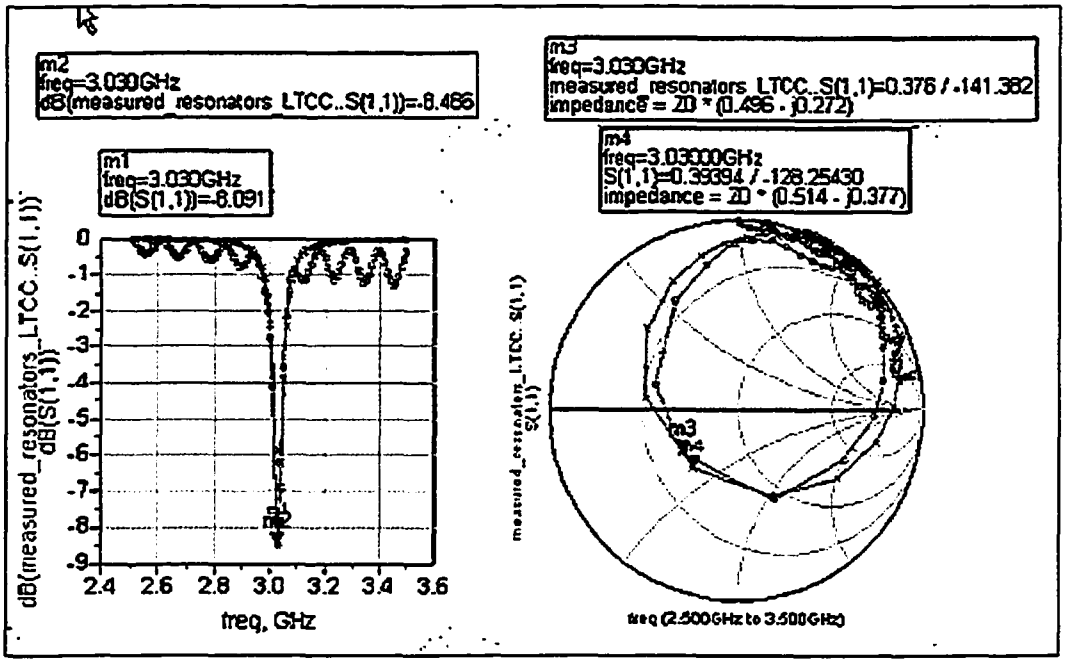
$$L = \frac{Q_u R}{\omega_0} \quad and \quad C = \frac{1}{\omega_0^2 L} \quad for\ series \tag{3.7}$$

$$L = \frac{R}{\omega_0 Q} \quad and \quad C = \frac{1}{\omega_0^2 L} \quad for\ parallel \tag{3.8}$$

As a result, the chosen resonators for this work, i.e. design #4 and design #2 in Table 3.4, have been modeled and verified against experimental results. For resonator #2, we have a parallel-RLC type equivalent circuit shown below in Figure 3.10:



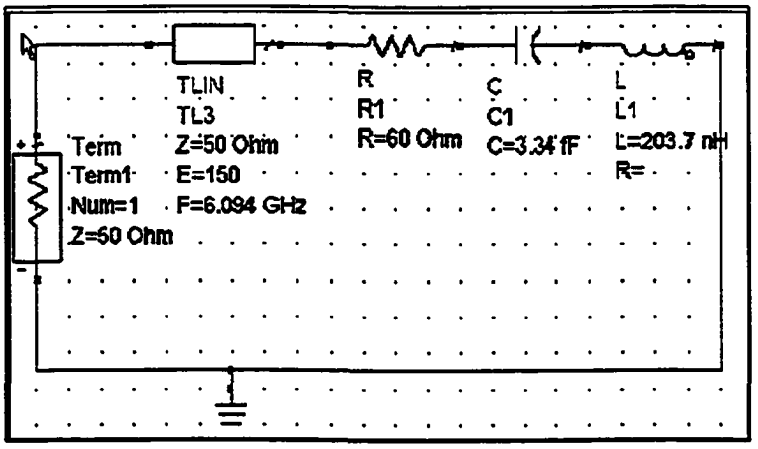
(a)



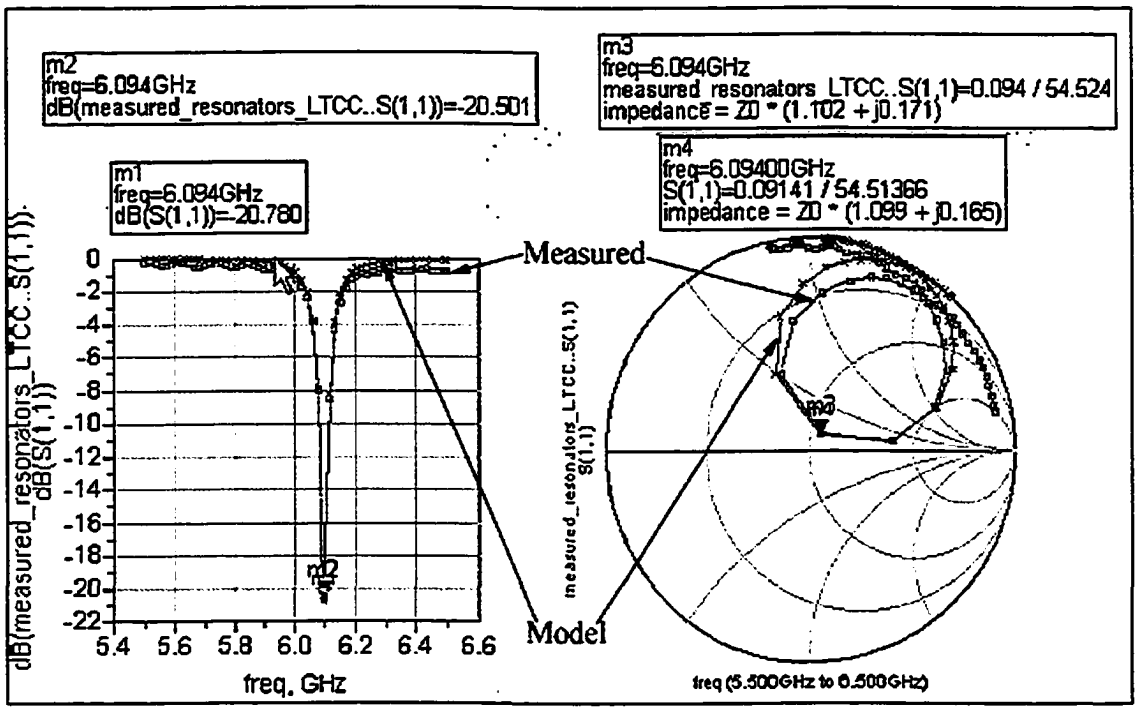
(b)

Figure 3.10: Resonator #2 model (a) Equivalent circuit (b) Simulation results

For resonator #4, we have a reverse mode of circuitry where a series-RLC type equivalent circuit is shown in Figure 3.11:



(a)



(b)

Figure 3.11: Resonator #4 model (a) Equivalent circuit (b) Simulation results

There are two observations that are to be noted in the circuit diagrams above. The first is the addition of an ideal transmission line (TL) in both circuits. The TLs were needed in order to add the appropriate phase shift supplied by the CPW feed network, in order to

mimic the resonator's response as closely as possible at the plane of the probe pads (for subsequent use in oscillator design). The second observation is the de-normalization of the component values in the circuit model. The characteristic impedance of the CPW feed network in both designs was $\mathbf{Z_0 = 22.345\ \Omega}$, while the measurements were done in a 50 Ω system. Thus, the de-normalization factor was taken to be 22.345/50 = 0.447.

3.3 – Low Noise Design Strategy and Procedure

3.3.1 – Device-Line Approach

There are several ways to obtain a low-noise design for oscillators, and most of the techniques mentioned in section 2.3.2 should be applied regardless of the designer's goals. However, Kurokawa [3.28] outlined a method, based on mathematical expressions for noise voltages, that allows the designer to reach the lowest possible phase noise tolerable by the circuit at hand. This method is called the "device-line approach", and it will be next discussed in general, before discussing its implementation in this work.

The "*device-line approach*" has been the subject of research in many previous works [3.29] [3.30] [3.8]. However, in most of these projects, the technique was used to design oscillators with the highest possible output power as a goal. In this work, the same process will be applied, with low noise being the main goal. Surprisingly, to the best knowledge of the author, this technique has not been widely applied specifically for obtaining low phase noise designs. As previously stated, the operation of negative resistance one-port oscillators is directly related to the load and terminating impedance presented to the active device, along with their amplitude dependence. The amplitude dependence will be re-introduced as a major component for noise, as it was always

ignored from any analysis for simplification purposes. In general, this relationship can be described graphically as the intersection of a load line and a device line in an impedance plane from which operating frequency, output power and associated load impedance and locking characteristics can be obtained. Inherently, the active device is turned into a negative-resistance monoport, whence the device-line technique is used to measure its properties in a non-oscillating mode of operation similar to the large signal mode of operation that occurs during oscillation. As it was mentioned in section 2.2.3 that when plotting the inverse of the amplitude-dependent device line along with the frequency-dependent load line, the AM-to-PM phase noise performance is determined by their intersecting angle, with orthogonal intersection being the optimum [3.28] [2.6] [3.2]. Figure 3.12 illustrates the device line measurement method:

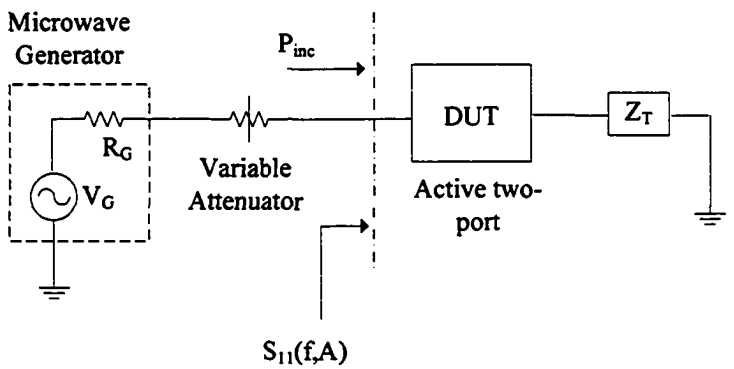


Figure 3.12: Setup for device-line characterization

This technique is very successful when applied in a measurement environment, since it involves the large-signal characterization of the transistor. However, in this work, we will take advantage of the powerful CAD tools to mimic the behavior of the measurement apparatus shown above. Figure 3.13 shows the device-line approach as described above:

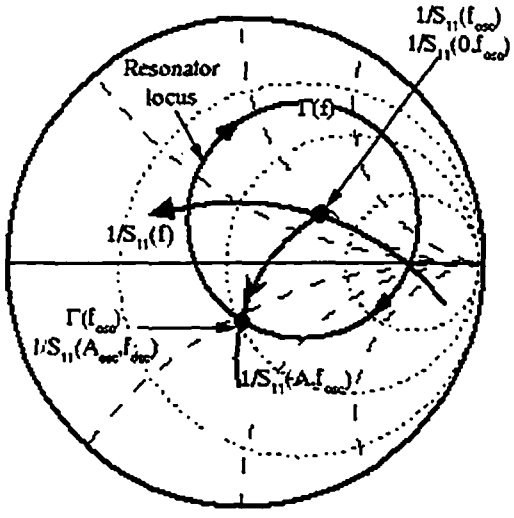


Figure 3.13: Smith chart illustration of device-line approach

Having outlined the basic road map that will be followed in this section, we will now describe a general procedure that will allow for the implementation of the device-line scheme:

1. Determine a proper bias point for the active device used in the circuit. Attention should be paid to the noise figure contribution at the chosen bias point.
2. Choose a transistor configuration along with a circuit topology to determine the oscillator's load and termination segments.
3. If needed, determine the feedback element to be included with the active device in order to create instability at the oscillator monoport. In design methodology, the feedback element is characterized to provide the largest negative impedance.

4. With the transistor and the feedback element combined into a single entity, determine the terminating impedance, Z_T, that will also result in maximum $|S_{11}|$ or minimum $|1/S_{11}|$ as shown in Figure 3.14:

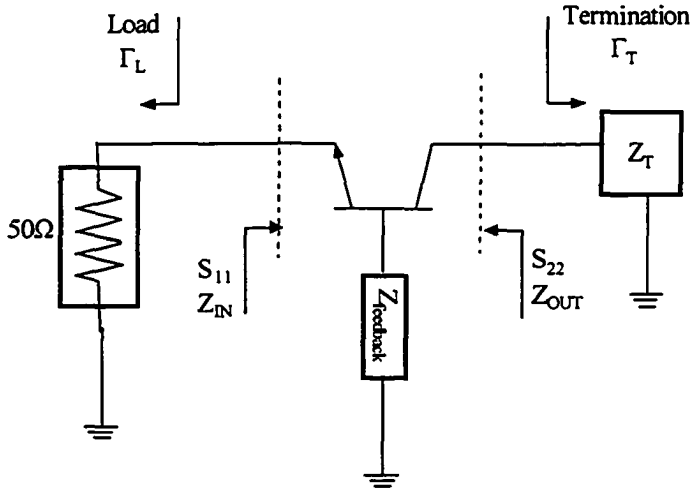


Figure 3.14: Feedback configuration showing various circuit parameters

As mentioned in section 2.2.4, in order to satisfy the first oscillation condition, the following conditions need to be satisfied:

$$\left|\frac{1}{S_{11}}\right| < |\Gamma_L| \quad and \quad \angle(1/S_{11}) = \angle\Gamma_L \tag{3.9}$$

Thus, attention should be paid to making sure that Z_T generates frequency-dependent (*F-D*) device-lines, $1/S_{11}(f)$ curves, that are mostly inside the Γ_L circle, where Γ_L is the load impedance, in this case the load being the resonator.

5. The second oscillation condition is that equation (3.9) has to be satisfied at only one frequency in order to have stable oscillations. This can be qualified on a Smith chart by confirming that the $1/S_{11}(f)$ locus and the $\Gamma_L(f)$ locus vary in opposite directions, as shown in Figure 3.13.

6. Generate power-dependent (*P-D*) device-lines, i.e. $1/S_{11}(A,f)$ curves. For lowest noise criterion, $1/S_{11}(A,f)$ at $f = f_{osc}$ must cross the locus $\Gamma_L(f)$ also at $f = f_{osc}$ perpendicularly, i.e., the angle between the device-line tangent, as it varies with amplitude, and the load-line tangent, as it varies with frequency, must be 90°, as shown in Figure 3.13.
7. Iterate from step 4 in order to accomplish steps 5 and 6.

Having outlined the design procedure, the implementation as it applies to this work will be discussed in the next few sections.

3.3.2 – Device-Line Implementation

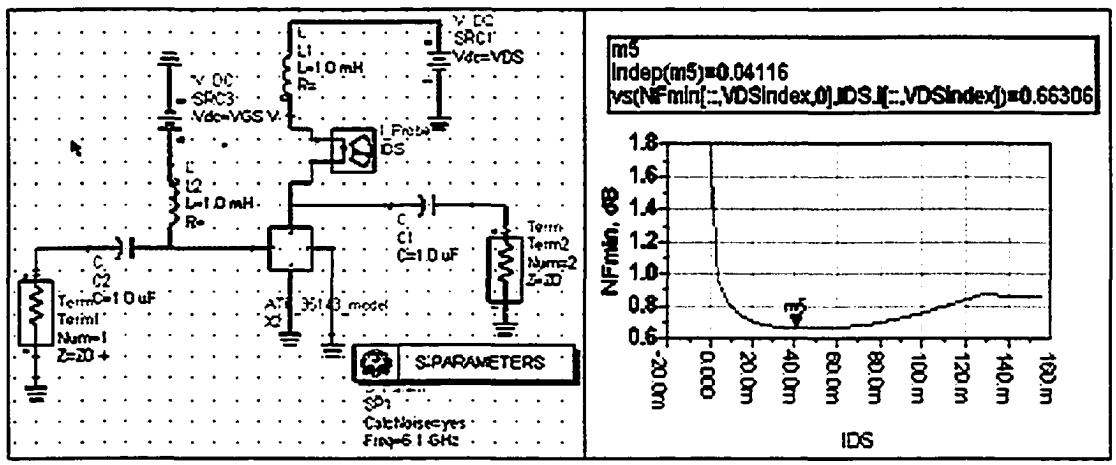
The device-line approach was to be incorporated with the built LTCC resonators. However, before embarking on this task, the target specifications are given as follows:

Table 3.5: Specifications for oscillator designs

Oscillator Specifications	Oscillator #1	Oscillator #2
Frequency of Oscillation	6.094 GHz	3.03 GHz
Output Power	6 dBm	6 dBm
Phase Noise	-100 dBc/Hz at 100 kHz or -120 dBc/Hz at 1 MHz	-100 dBc/Hz at 100 kHz or -120 dBc/Hz at 1 MHz
Maximum Harmonic Levels	-20 dBc	-20 dBc
Power Supply	< 5 V	< 5 V

As indicated in section 3.2.3, resonator #4 was identified as a suitable element for oscillator #1, and thus the next several sections describe the procedure's application using Agilent ADS™ as the industry-standard CAD tool.

The first step is to determine an appropriate bias point for the active device. Keeping in mind the recommendation regarding phase noise from Leeson's formula, it was determined that an active device with a low NF is best suited for such a design. Therefore, a bias point was chosen to potentially offer the lowest noise figure. This was done in the following Figure 3.15:



(a) **(b)**

Figure 3.15: Bias circuitry (a) configuration (b) noise figure results

While sweeping V_{DS} and V_{GS} and probing I_{DS}, it was determined that NF_{min} occurs at the following bias operating point: V_{DS} **= 3.0 V,** V_{GS} **= -0.3 V,** I_{DS} **= 41.16 mA where** NF_{min} **= 0.663 dB.** Although the chosen bias point does not represent a global NF_{min}, it was chosen for other secondary reasons. It is well known that if a waveform is compressed at its peak or trough due to low ceiling or high floor voltage levels, harmonics tend to

appear in the spectrum, which leads to unnecessary noise. Thus, the target bias point was modeled after a Class-A power amplifier biasing scheme, where a full voltage swing is allowed to occur with minimal cutoff. As well, as it was determined in [3.31] that a relationship existed between bias points of a GaAs MESFET with power and phase noise. On the DC curves of [3.31], 19 bias points were examined covering almost all areas of the *I-V* curves, subsequently revealing that the best PN and best output power occurred at Class-A bias point. It is noteworthy to mention here that the bias point for NF_{min} in the *CS* configuration also revealed a similar local NF_{min} for the *CG* configuration.

Referring to the procedure outlined above, step 2 was determined from section 3.1.3, where the *CG* configuration was chosen as an optimum circuit topology. In the *CG* configuration, it was determined that the circuit, in a 50 Ω system, was desirably unstable at the frequency of choice, without the addition of any feedback element. However, it was decided that an inductive feedback element would be added to the gate in order to increase instability while providing one more element of flexibility to carry out the design. The inductor, along with the termination impedance, allows two separate entities of variations in order to meet the device-line goals. Thus, the inductance value was not set, but left as a variable parameter for the subsequent steps. However, since the feedback element affects instability, a range of values was determined that would allow for the greatest number of termination impedance combinations, which represent valid loads causing instability. The idea is to expand the stability circle as wide as possible to include the greatest number of impedances inside the unstable region of the circle, as illustrated in Figure 3.16:

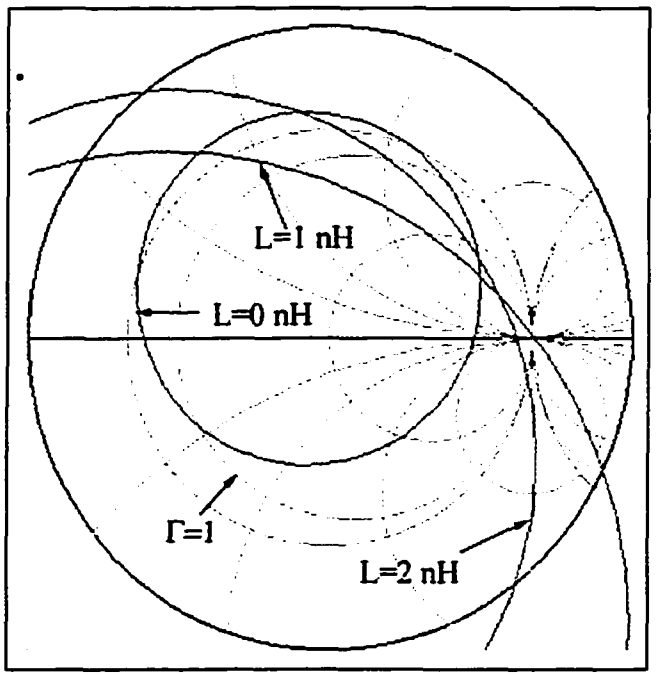
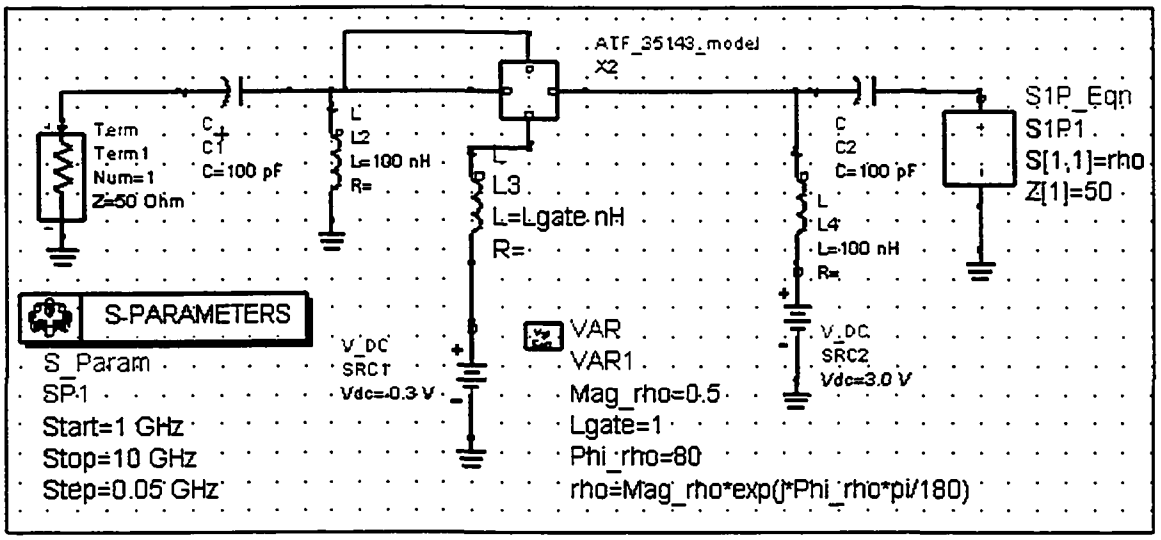


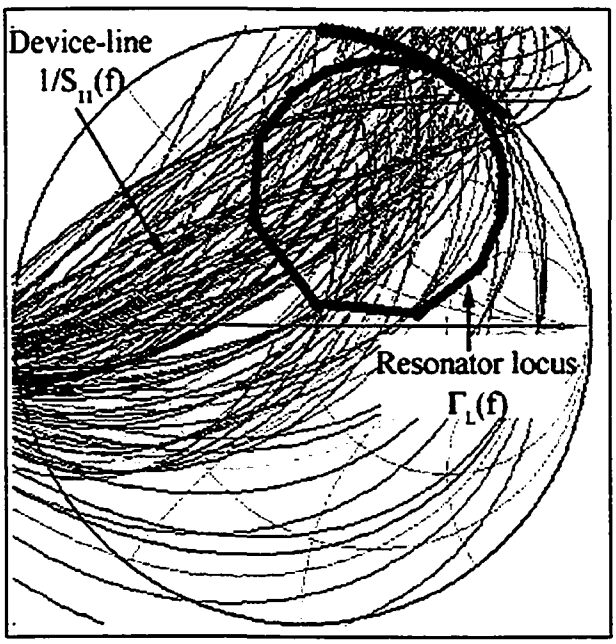
Figure 3.16: Stability contours for a given inductance range

Thus, for the inductance in the gate, an appropriate range was specified encompassing values from 0 nH to 2 nH.

The fourth and fifth steps of the design procedure are examined next. The aim is to forecast the type of response obtained from the examination of S_{11}, otherwise known as the device-line. This exploration will be done in order to quantify the extent of satisfaction of both oscillation conditions, mentioned in the design procedure, with respect to the variable parameters, the gate inductance and the termination impedance. Figure 3.17 shows the circuit configurations and the results obtained respectively:



(a)



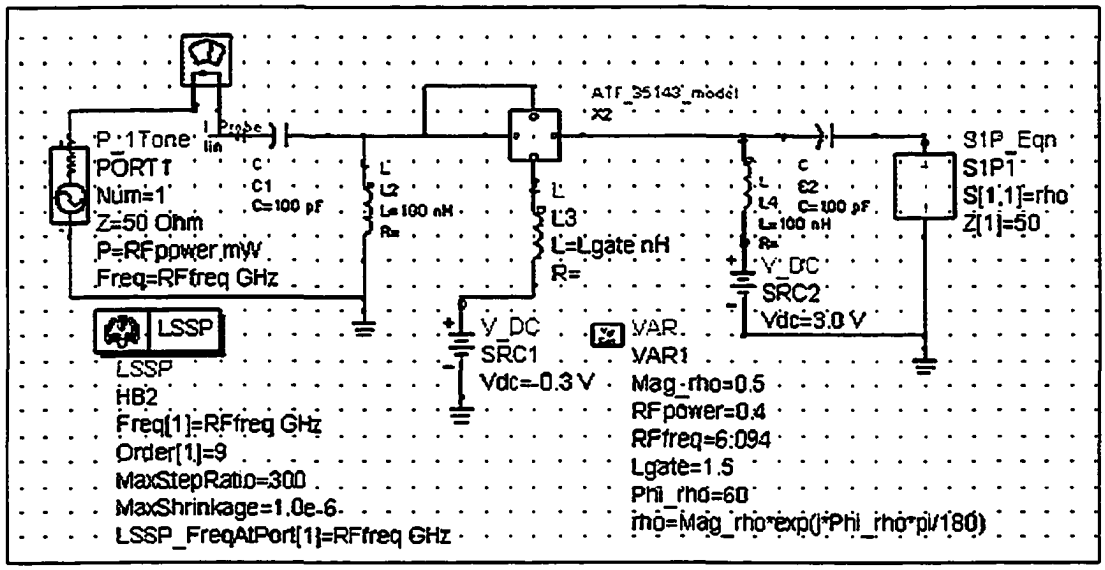
(b)

Figure 3.17: F-D device-line (a) CAD "measurement" setup (b) Results

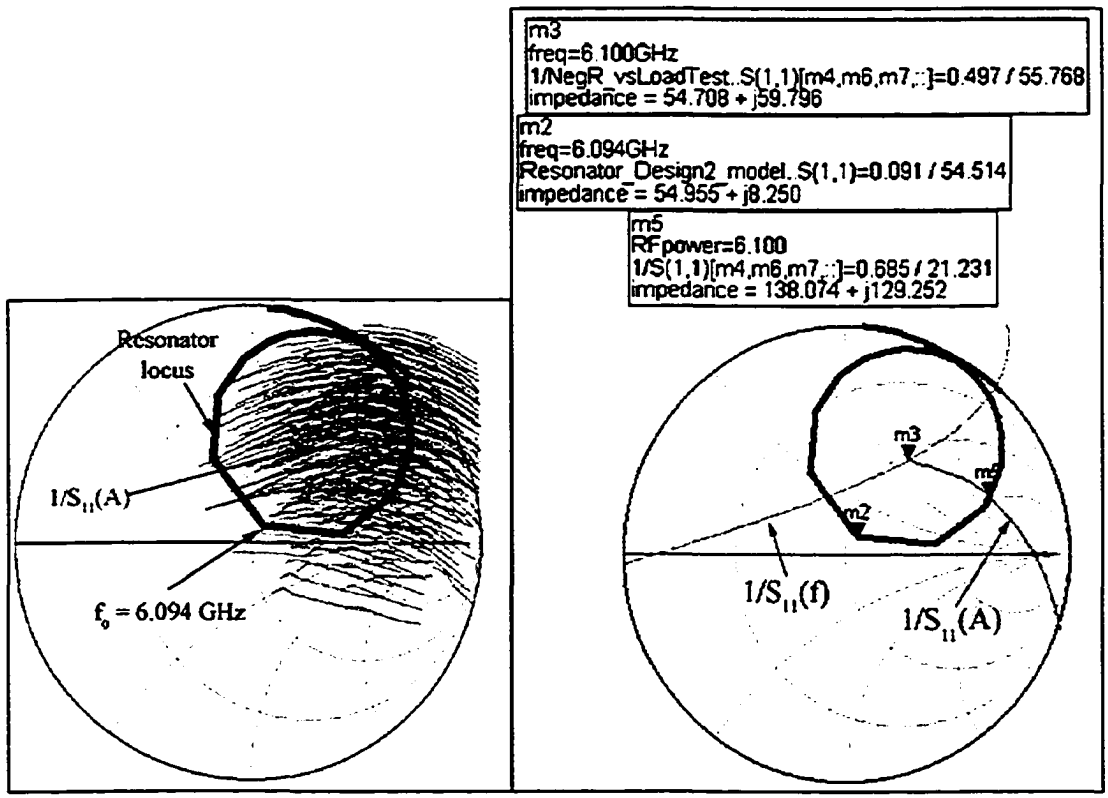
As shown in Figure 3.17 (a), the terminating impedance is represented by its reflection coefficient, Γ_T, through its magnitude and angle. Similar to a load tuner used in load-pull simulations, Γ_T was swept to cover the entire space of the Smith Chart, representing all

available termination impedances. Included with the Γ_T sweep space was the gate inductance, which was also swept in tandem with Γ_T. Figure 3.17 (b) shows the result of all three swept variables, where the resonator model locus is shown in bold representing Γ_L and the device-lines are shown as $1/S_{11}(f)$. From the results, it is shown that the device-line locus is included within the load circle, as it was also noticed that the resonator locus varied in a clockwise direction, while the device-lines varied in a counterclockwise direction. Thus, it was concluded that steps 4 and 5 have both been satisfied.

Having confirmed that stable oscillations are possible with a vast array of termination impedances, the next step called for the generation of power-dependent device-lines that satisfy the low-noise criterion. Thus, the same circuit used in Figure 3.17(a) was utilized with an input power port and a 50 Ω impedance for oscillations prevention. The power port injects a linearly increasing power signal at the input of the device, simulating its large-signal behavior at the frequency of oscillation. This will generate the power-dependent device-lines, or $1/S_{11}(A,f_{osc})$ curves, needed to satisfy the low-noise criterion. Figure 3.18 illustrates the setup used and the results obtained respectively:



(a)



(b) (c)

Figure 3.18: P-D device-line (a) CAD "measurement" setup (b) Results

As can be seen from Figure 3.18 (a), the setup used is the same as in Figure 3.17 (a), except the power port was substituted in order to simulate the amplitude response of the device. The sweep space adopted in Figure 3.18 is the same for the one Figure 3.17. For example, Figure 3.18 (c) shows the result of a single sweep entity with power, where *Lgate* = 1.25 nH, $|\Gamma|$ = 0.4, and $\angle\Gamma$ = 60°, for $1/S_{11}(f)$ and $1/S_{11}(A)$. It is concluded that for each frequency-dependent device-line, there exists a corresponding P-D device-line at f_0. Thus, Figure 3.18 (b) shows the results of $1/S_{11}(A)$ for an extended sweep space, defined in Figure 3.18 (a), without the inclusion of their corresponding $1/S_{11}(f)$ lines for clarity. It became apparent that the $1/S_{11}(A,f_{osc})$ lines could not intersect the resonator locus at f_0, nor could that intersection be orthogonal, as illustrated in the figure. Thus, it was concluded that the low-noise criterion is not met as stipulated in step 6 of the procedure, given the current circuit configuration. Therefore, another method was implemented in order to possibly transform the power-dependent device-lines in a direction that might be conducive to orthogonality. Figure 3.19 illustrates the components added to the original circuit:

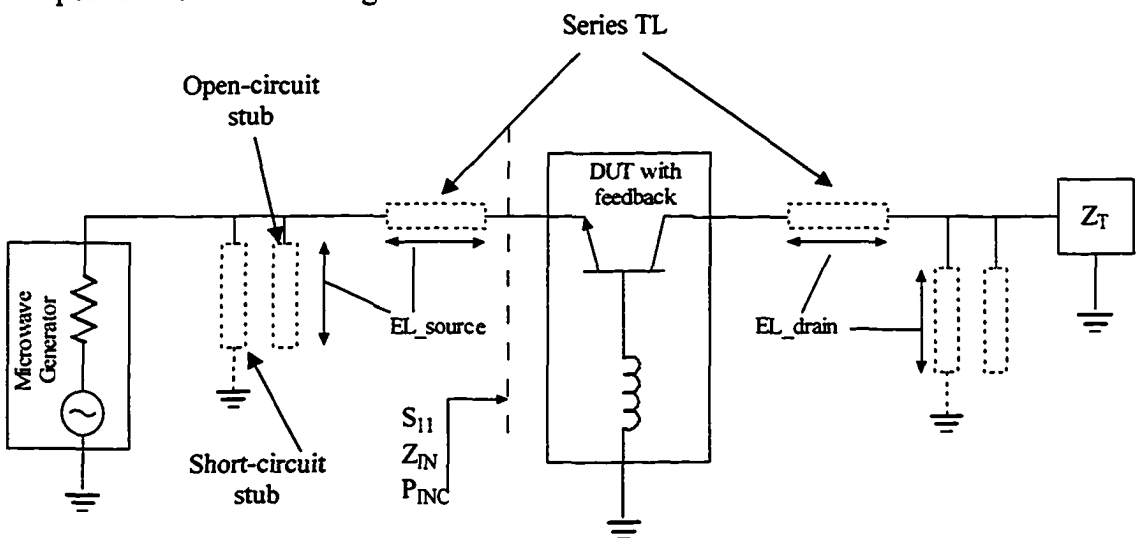


Figure 3.19: P-D device-line configuration with additional circuit elements

EL_source and *EL_drain* represent the electrical length of ideal transmission lines (TLs) that were added either in series or in parallel with the signal path. The purpose of the transmission lines is to effectively shift the P-D device lines around the Smith Chart, comparable to impedance transformation, so as to land near the resonator's oscillation frequency. Following various test simulations of TLs in the source and the drain, a pattern was observed where it appeared that the drain TLs shifted the P-D device-lines in a vertical manner, while the source TLs shifted the device-lines in an anti-clockwise manner. From there, the following result was obtained from the inclusion of the TLs in series with the signal path:

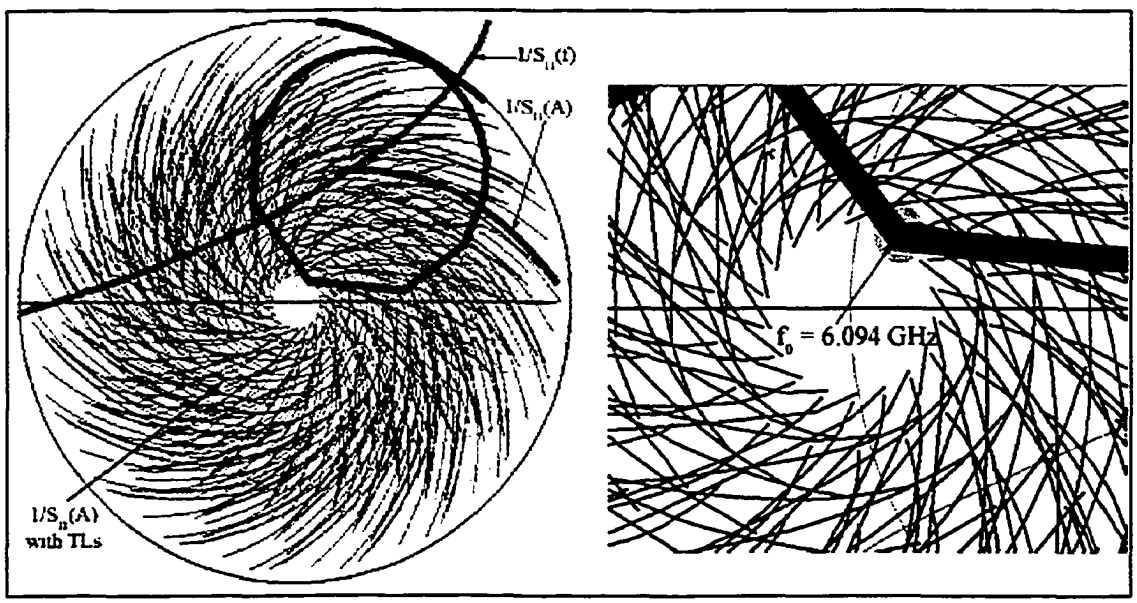


Figure 3.20: Results of P-D device-line with additional circuit elements

The component values that were used to generate those results are ***Lgate* = 1.5 nH, $|\Gamma|$ = 0.3, and $\angle\Gamma = 90°$**, where *EL_drain* and *EL_source* were swept from 0° to 180°. Thus, as shown in Figure 3.19, the addition of the TLs in the drain and source did manage to actually shift the P-D device-lines as predicted. Similar to Figure 3.18, the corresponding F-D device-lines have been omitted for clarity. However, it can also be seen that no orthogonal intersection occurred around f_0 = 6.094 GHz. As a result, having observed the behavior of the additional TLs, a myriad of combinations were attempted in order to generate orthogonality, with the same approach:

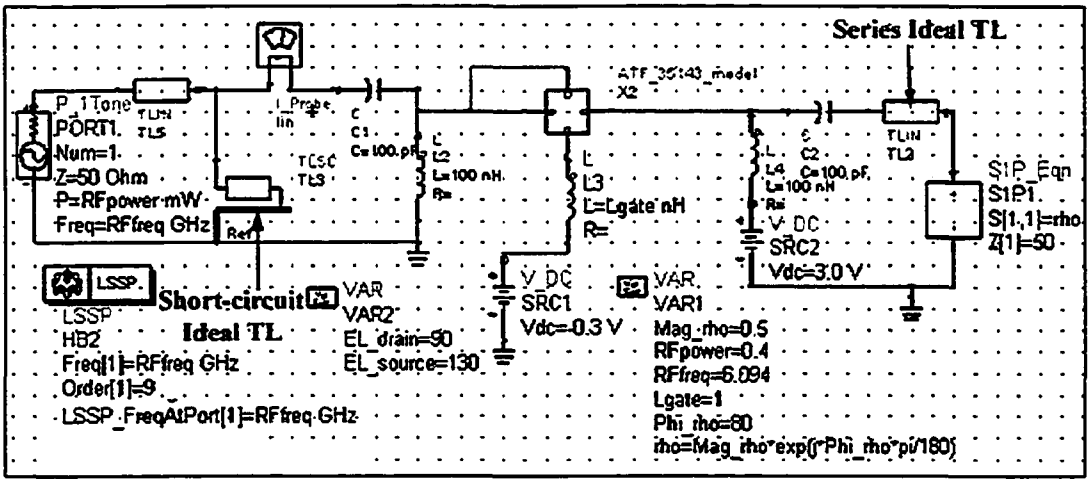
a. Choose an appropriate termination impedance, Z_T;
b. Check that the chosen termination impedance satisfies both oscillation criteria;
c. Insert either series or parallel TLs in the signal path;
d. Sweep the length of the TLs to satisfy the phase noise requirement;
e. Repeat steps c and d, while including step a if necessary.

This systematic approach can be combined with the procedure outlined earlier as an extension to the device-line methodology. Thus, the TLs are identified as new variable components, expanding the sweep space to include the feedback element and the termination impedance. As shown in [3.32], the drain voltage can also be included in that sweep space, however that would lead to a frequency shift and it was avoided here.

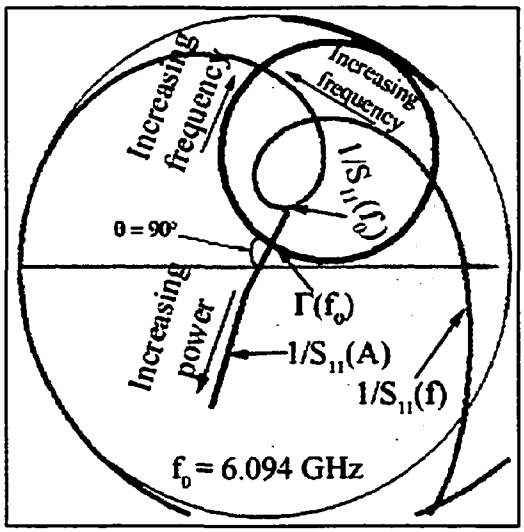
3.3.3 – Harmonic Balance Circuit Simulation Results

Having outlined the steps of approach, we will now examine the results of the various simulations that were attempted for low-noise. Considering the size of the sweep space, the most promising results will be presented, beginning with the most optimum.

Figure 3.21 (a) presents the circuit used to satisfy the low-noise criterion. It shows the addition of the TLs in the source and the drain, where an additional short-circuited stub was added only in the source.



(a)

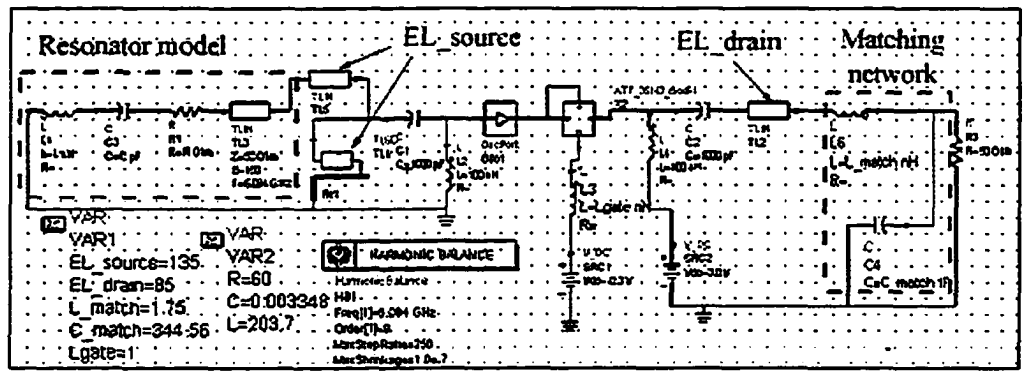


(b)

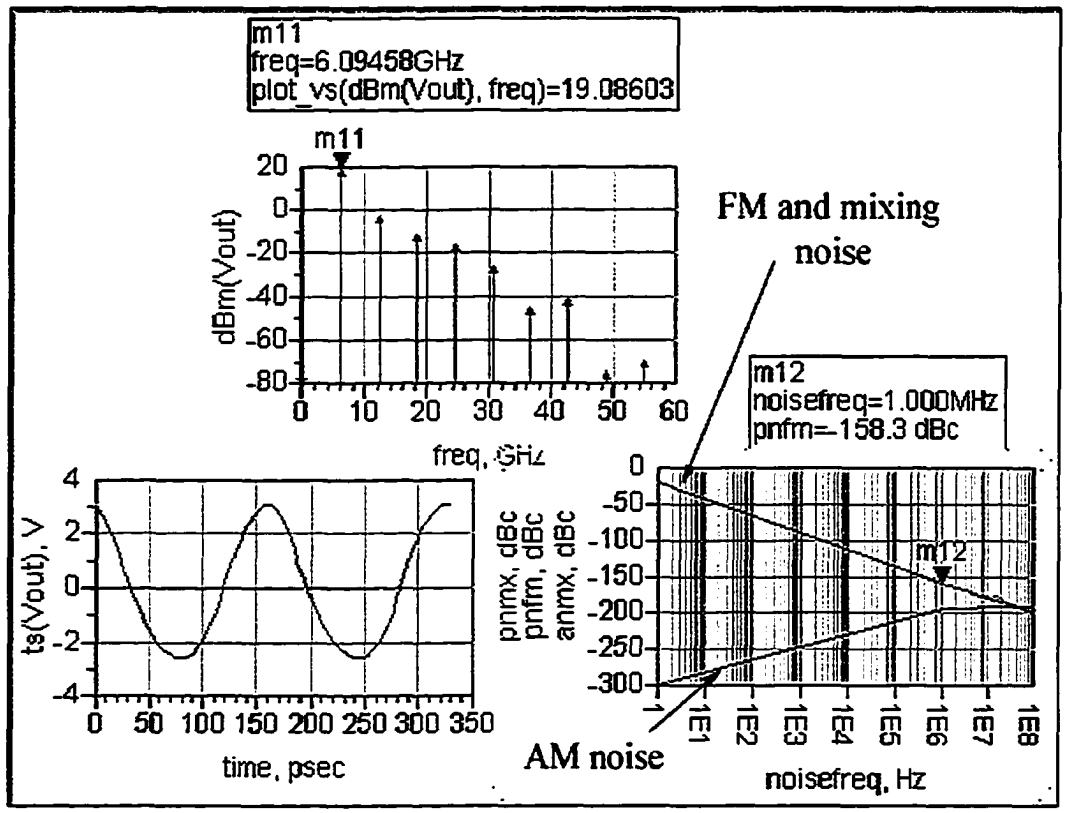
Figure 3.21: Optimal low-noise criterion (a) Circuit configuration (b) Smith chart result

As can be seen from Figure 3.21 (a), the component values that were used are the following: ***EL_source*** **= 130°** and ***EL_drain*** **= 90°;** $|\Gamma| = 0.5$, $\angle\Gamma = 80°$, and ***Lgate*** **= 1 nH.** Figure 3.21 (b) shows the result of the above shown circuit with the components values just mentioned. Both device-lines are also shown with the resonator locus, which has been extrapolated for more accuracy, along with the angle of tangential intersection. The enclosure of the F-D device-line locus as well as its frequency direction with respect to the resonator locus indicates the satisfaction of both oscillation criteria. Examining the P-D device-line, it is noticed that it is a perpendicular bisector of the resonator locus, i.e. the load line, hence satisfying the low-noise criterion. Of note in Figure 3.21 (b) is the presence of a loop in the F-D device-line. As mentioned in [3.2] and [3.28], a loop present in the frequency-dependent device-line may indicate a lock-up mode, where the oscillator "locks up" at some frequency either higher or lower than the resonant frequency. It was concluded that the loop was introduced by the addition of the transmission lines, due to their phase shift characteristic. Since there was no other way to currently avoid the present loop in the F-D device-line while meeting the low-noise criterion, it was decided that it would be recognized as a potential problem while carrying out the circuit design.

From here, a lumped-element oscillator was created for simulation given the above parameters. The termination's reflection coefficient was converted to an impedance load, and a Harmonic Balance simulation was carried out to test the above mentioned circuit. Figure 3.22 below shows the circuit used in the simulation along with the observed results:



(a)



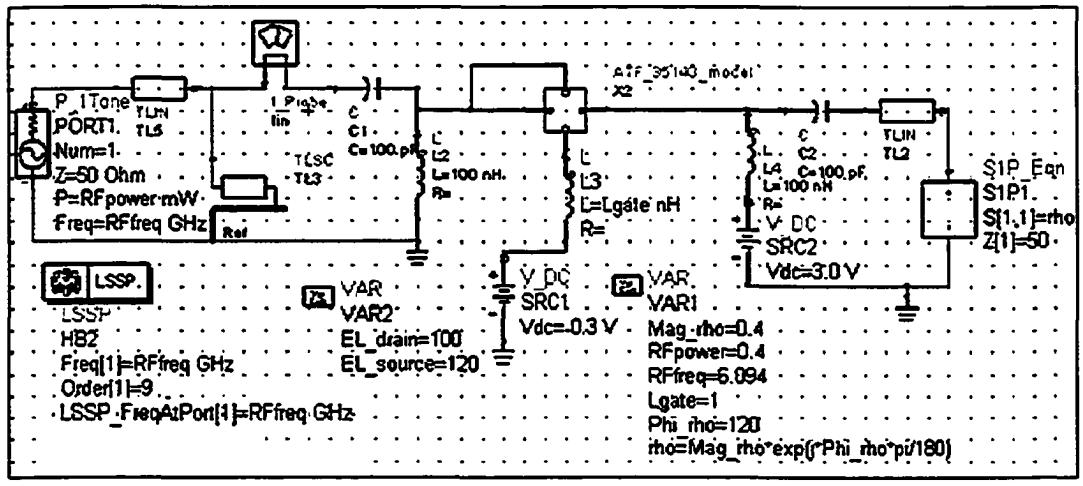
(b)

Figure 3.22: Equivalent lumped element oscillator for 90° intersection
(a) Circuit configuration (b) HB results

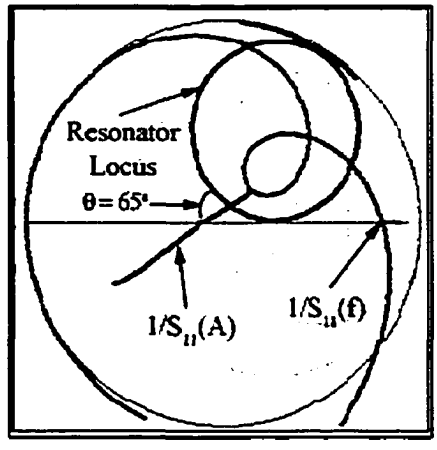
From Figure 3.22 (a), we can see the resonator model used for resonator #4, along with the additional TLs and a matching network. The matching network is used to match the terminating impedance (Z_T) to 50 Ω, where $Z_T = 34.84 + j*45.75$ Ω for $|\Gamma| = 0.5$ and $\angle\Gamma =$

80°. Examining the results in Figure 3.22 (b), we can see that the spectrum reveals a good output power at f_0 = 6.094 GHz, with a 2nd harmonic difference of -20 dB, revealing a clean sinusoidal time signal. As it is also shown, the phase noise displayed encouraging preliminary results for FM, AM, and mixing noise.

With the apparent success of the first design, a second design was initiated with the same resonator. However, for this design, the angle of intersection between the P-D device line and the load line was made sub-optimal, i. e. different than 90°. Figure 3.23 presents the circuit configuration used along with the results obtained:



(a)

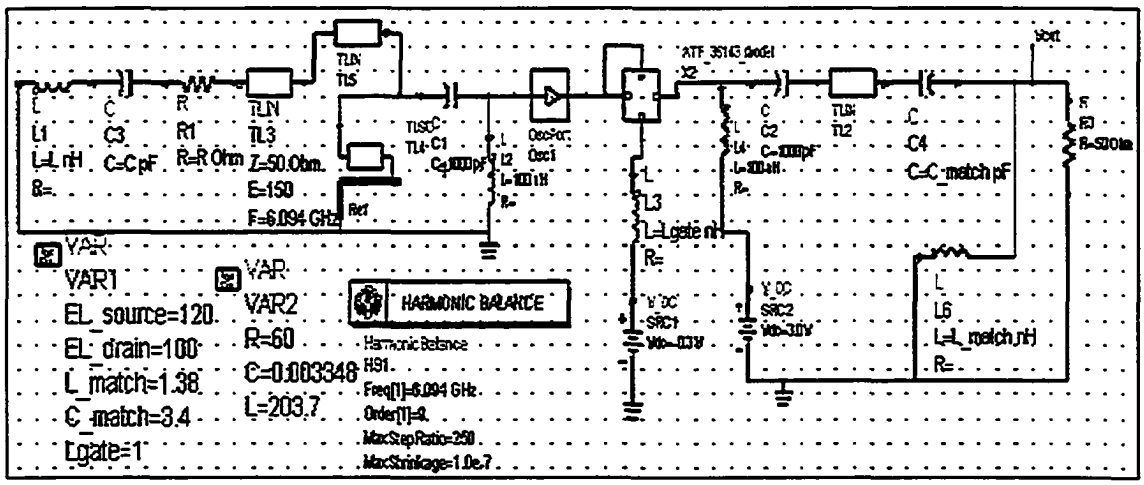


(b)

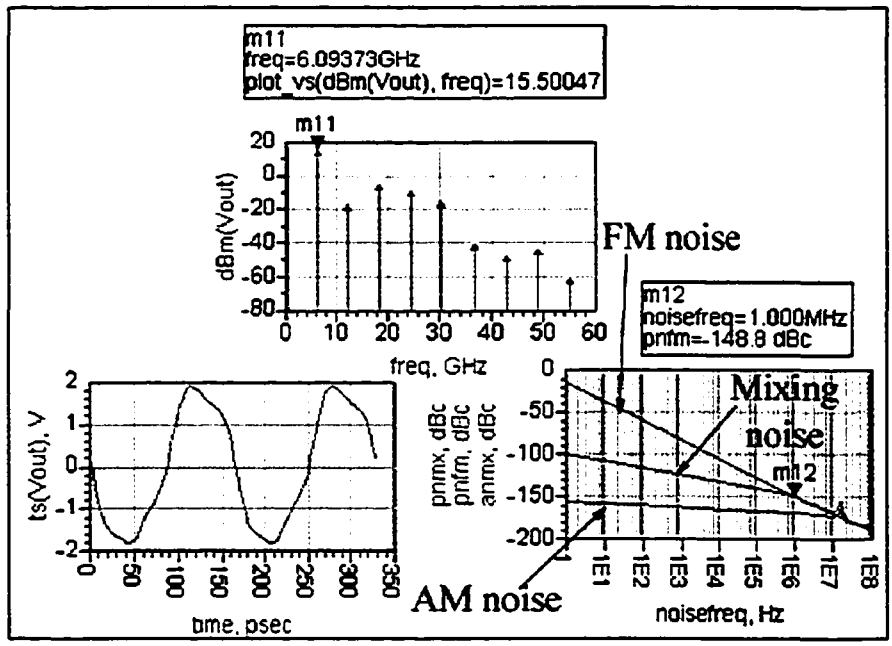
Figure 3.23: Sub-optimal low-noise criterion (a) Circuit configuration (b) Smith chart result

As can be seen from Figure 3.23 (a), the used component values are the following: ***EL_source*** = **120°** and ***EL_drain*** = **100°**; $|\Gamma| = 0.4$, $\angle\Gamma = 120°$, and ***Lgate*** = **1 nH**

Figure 3.23 (b) shows the result of the above shown circuit with the component values just mentioned. As well, the device-lines are similar to the previous circuit, except the difference is manifested in the angle of tangential intersection, due to the combinations of the terminating impedance along with the TLs. In the same way, a lumped-element oscillator was created, and its performance was measured through simulation, as shown in Figure 3.24:



(a)



(b)

Figure 3.24: Equivalent lumped element oscillator for sub-optimal intersection (a) Circuit configuration (b) HB results

Shown in Figure 3.24 (a) are the source and drain TLs along with the matching network to match Z_T = 26.92 +j*22.2 Ω, for $|\Gamma|$ = 0.4 and $\angle\Gamma$ = 120°, to 50Ω. The results in Figure 3.24 (b) show that the intersection of the P-D device-line with the resonator locus occurs at the frequency of oscillation, with good 2nd harmonic levels. As well, the degradation in phase noise reflects the shift from orthogonality between the two loci.

Several other combinatorial circuits were attempted and their simulation output were recorded in order to obtain a bigger pool of results. Table 3.6 summarizes that study:

Table 3.6: Summary of lumped element oscillator designs

Circuit Topology			Oscillation Frequency [GHz]	Intersection Angle [°]	Phase Noise [dBc/Hz] @ 1MHz	Output Power [dBm]
$\lvert\Gamma\rvert\angle\Gamma^{\circ}$ Z_T [Ω] Lgate[nH]	TL electrical length[°]					
	source	drain				
#2 0.5∠40° 77.5 + j*66.41 1.5	No TLs used		6.057	75	-146.5	10.3
#3 0.5∠80° 34.84 + j*45.75 1	130 S+P_sc	90 S	6.094	90	-158.3	19
#4 0.4∠120° 26.92 + j*22.2 1	120 S+P_sc	100 S	6.094	65	-148.8	15.5
#5 0.5∠60° 21.43 + j*24.74 1	174 S	105 P_sc+S	6.0984	55	-141.7	17
#6 0.5∠80° 34.84 + j*45.75 1	162 P_oc+S	120 S	6.104	32	-135.2	14

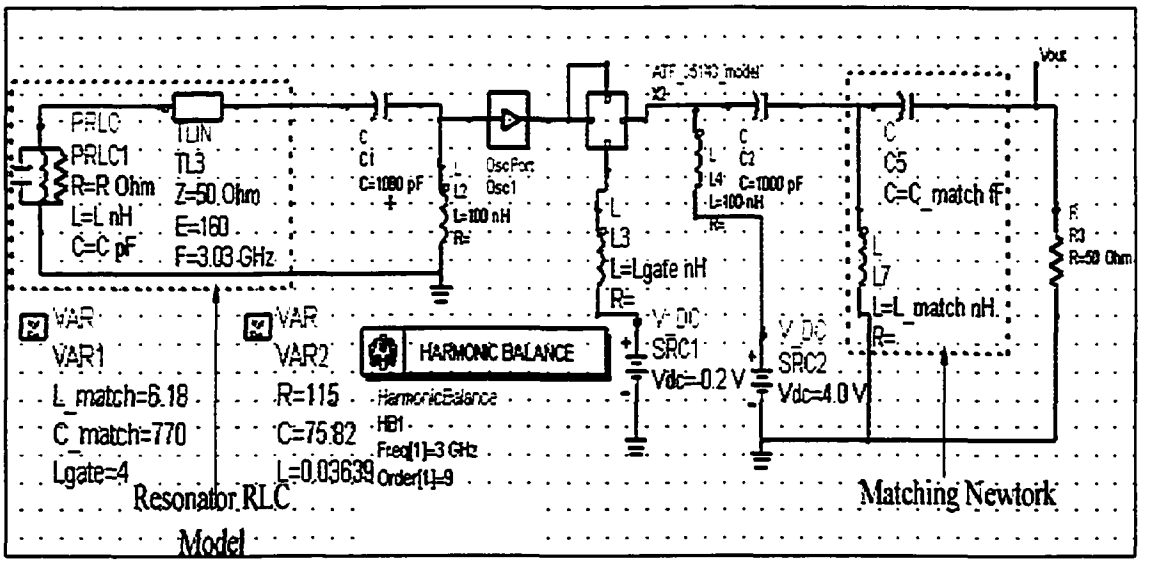
Note: S = Series TL
S+P_sc = Series TL followed by parallel short-circuit stub
P_ oc+S = Parallel open-circuit TL followed by series stub

Thus, it is noticeable, from the results presented in Table 3.6 that the device-line approach holds, where better phase noise is obtained with a perpendicular bisector.

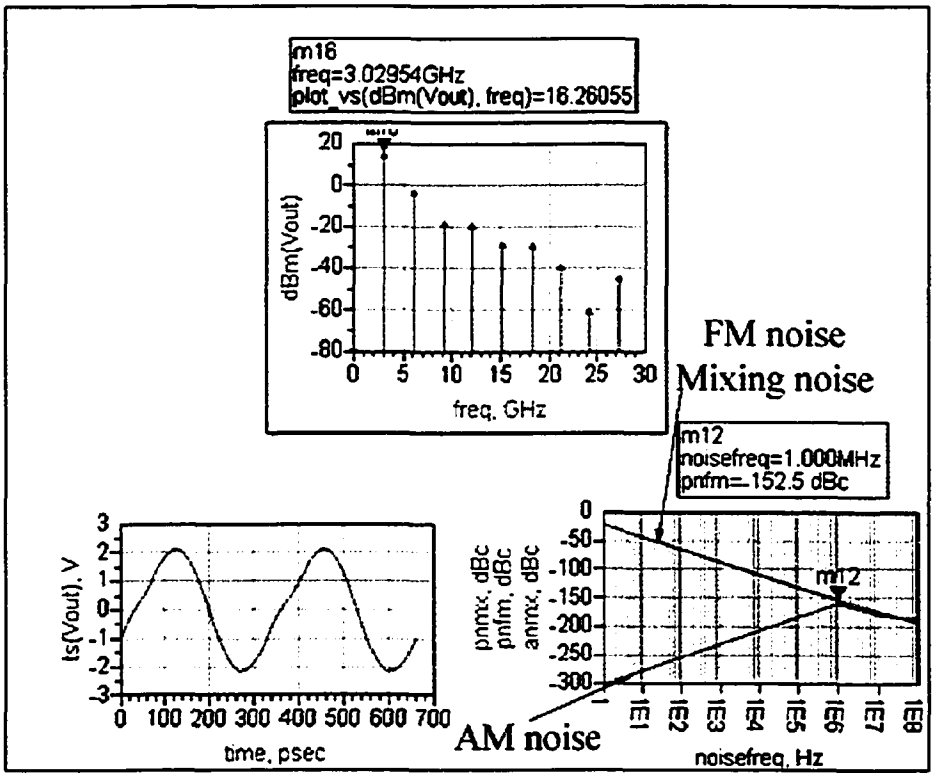
3.3.4 – Resonator #2 Circuit Simulation

A similar approach was adopted for the design of a low-noise oscillator circuit using resonator #2 mentioned in section 3.2.3. Utilizing the parallel-RLC lumped element model for this resonator, all of the design steps outlined in the previous sections were performed, in order to obtain a best design at 3.03 GHz. For clarity, only the results of this process will be described below.

Due to the position and shape of this resonator's locus on the SC, it was clear from the beginning that fulfilling the low-noise criterion would be a challenging task. Thus, several iterations of the design steps were undertaken before a comprehensive design approach was adopted. From here, the bias point of the circuit was chosen as follows: V_{DS} = 4 V; V_{GS} = -0.2 V; I_{DS} = 55.5 mA. The change in bias point was necessary in order to alter the device-line space, without greatly affecting the noise figure. Likewise, the inductive feedback element in the gate was also altered. Figure 3.25 below illustrates the oscillator circuit used for simulation along with the results obtained:



(a)



(b)

Figure 3.25: Resonator #2 equivalent lumped element oscillator for optimal intersection (a) Circuit configuration (b) HB results

The terminating load used in the above circuit is Z_T = 139 –j*20.89 Ω for $|\Gamma|$= 0.45 and $\angle\Gamma$ = 345°. The resulting P-D device-line intersection with the resonator locus occurred at 85°, reflected in the promising phase noise displayed in the results. Of note in this circuit topology is the absence of TLs to satisfy the noise criterion, due to the shape of the resonator locus and its resonance frequency. This will be labeled circuit #7.

3.4 – Oscillator Circuit Implementation in Microstrip

3.4.1 – From Lumped-Element to Distributed-Element Circuits

From the above section, several oscillator circuits were chosen to be implemented in order to verify the proposed concept. From Table 3.6, oscillator circuits #2 and #3 were chosen employing resonator #4, along with circuit #7 employing resonator #2 for implementation. Circuit #3 was chosen for its excellent phase noise response, while circuit #2 was chosen for its sub-optimal phase noise along with its non-locking mode potential. Circuit #7 was chosen for its varied frequency response. However, before implementation, the lumped-element oscillators had to be converted and simulated with their equivalent distributed element circuits. This work uses LTCC-based resonators incorporated onto low-cost Duroid circuit boards as a proof of concept for full LTCC integration in succeeding design completion. Hence, the circuits were implemented using copper microstrip technology, with the following parameters: ε_r = **2.33,** ***tanδ*** = **0.0012,** ***height*** = **0.787 mm, with** $thickness_{cond}$ = **17.5 µm.** Thus, the lumped-element oscillator circuits were converted to their equivalent microstrip counterparts, while keeping in mind

the inclusion of surrounding TLs and the henceforth necessary compensation. Consequently, the inductive feedback elements in the gate were converted to their equivalents in microstrip using a narrow TL while allowing the length to control the inductance value. Similarly, the drain and source TLs were also converted to microstrip, transforming their electrical length into their corresponding realizable physical lengths. Finally, the terminating impedances were also implemented in microstrip, taking into consideration essential adjustments due to the many interconnects. The main goal in the transition from lumped-element to microstrip is to keep the phase noise for each circuit as constant as possible, without much degradation in performance. As well, since the objective of this work is the investigation of phase noise performance relating to circuit parameters, it was important to study the effects of various circuits employing the same resonator. Therefore, the connection of the resonators with the rest of the surrounding circuit elements had to be achieved in a repeatable manner, realzing that the resonators are made from LTCC while the rest of the circuit is from microstrip. Thus, aided by [3.33] and [3.34], the resonator was mounted on a metal plate, where it was attached to the rest of the microstrip circuitry through bondwires. A square gap, slightly larger in size than the resonator, was inserted in the board to allow the resonator CPW to be flush with the top of the board, minimizing the length of the bondwire reducing its effect on the oscillator circuitry. Figure 3.26 illustrates the mounting technique:

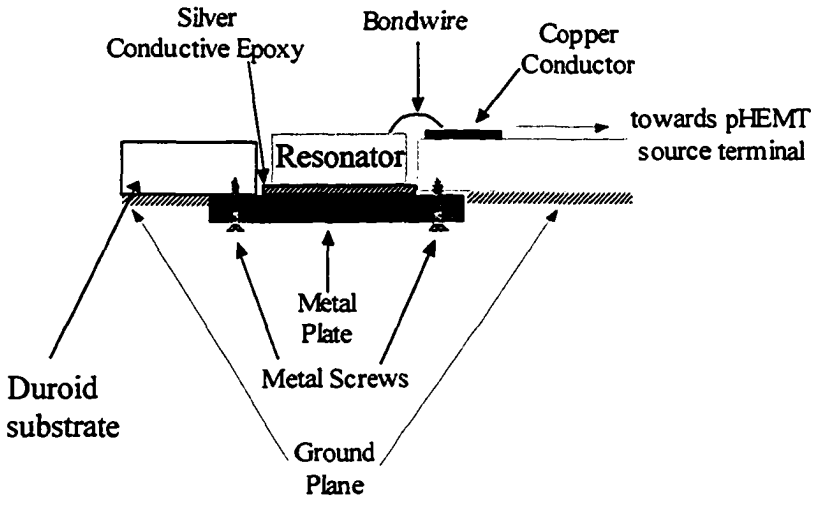


Figure 3.26: LTCC resonator to microstrip mounting technique

The resonator structure needs to be grounded properly in order to operate correctly and hence the importance of the metal plate attachment to the circuit ground plane.

While efforts were made to reduce the length of the anticipated bondwire, its introduction caused an additional inductance to be added to the signal path. Thus, a further compensation factor was to be accounted for in the simulation of the microstrip TL. Since the bondwires are made of gold, their inductance is relatively known to be 0.8 nH/mm. Thus, it was predicted that the length of the bondwire would be anywhere from 0.75 mm to 1 mm, hence introducing about 0.6 nH to 0.8 nH. Hence, the additional bondwire inductance was needed to be assessed in terms of TL length. Thus, for a TL with characteristic impedance $Z_0 = 50\ \Omega$, we have the following:

$$Z_0 = \sqrt{L/C}$$
$$(Z_0)^2 = \frac{L}{C} \qquad (3.10)$$
$$2500 = \frac{L}{C}$$

We also know for a TL at f_O = 6.094 GHz, we have the following:

$$\beta = 2\pi / \lambda_g$$
$$\beta = 179\, rads/m \qquad \textbf{(3.11)}$$

However, we also know the following:

$$\beta = \omega\sqrt{LC} = 179$$
$$LC = \left(\frac{179}{\omega}\right)^2 = \left(\frac{179}{2\pi(6.094x10^9)}\right)$$
$$LC = 2.185x10^{-17} \qquad \textbf{(3.12)}$$

Therefore, solving equation (3.10) along with equation (3.12), we obtain the following lumped-element equivalent model of a distributed TL, as shown in Figure 3.27:

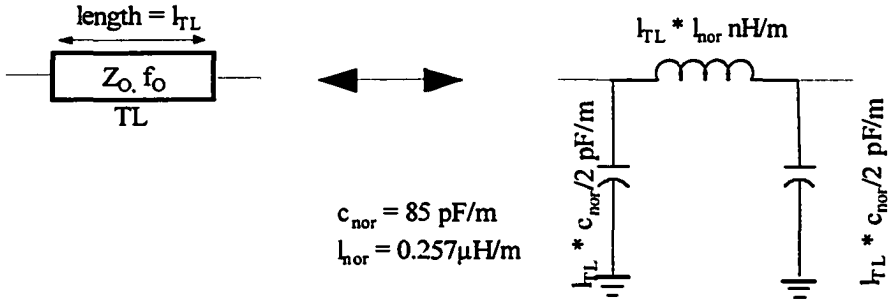


Figure 3.27: Lumped element equivalent of microstrip TL

Therefore, the addition of a bondwire of 1 mm in length with an equivalent inductance value of 0.8 nH is similar to the addition of a TL 3.11 mm in length, for the given dielectric parameters. Thus, in order to compensate for the bondwire, i.e. the extra TL length, the same length (3.11 mm) has to be subtracted from the connecting TL. However, the subtraction of a specific length of TL not only eliminates the effect of the corresponding inductive bondwire, but it also removes a comparable amount of

capacitance as well, due to the distributed nature of a TL. Thus, inserting an open-circuited TL of equal length to the bondwire's equivalent TL, i.e. 3.11 mm, is needed to guarantee the restoration of the original circuitry, before the addition of the bondwire. Figure 3.28 illustrates that concept:

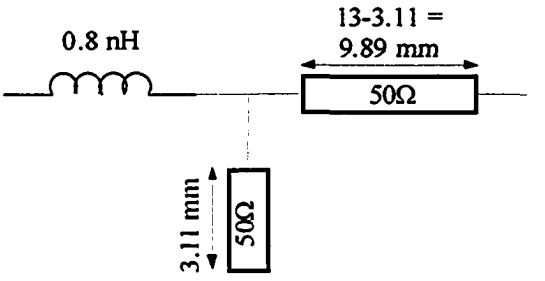


Figure 3.28: Bondwire inductance compensation method

3.4.2 – Final Circuit Implementation Based on Sensitivity Analysis

Several other challenging issues presented themselves during the conversion process. One of the more important ones was the sensitivity of the oscillator response of circuit #3 due to minute circuit tolerances. This was problematic because phase noise improvement alterations rendered the oscillator non-functional. Initial investigation of the oscillator's small-signal response revealed an unstable operating point for oscillation, under the Barkhausen criteria. Figure 3.29 illustrates a polar plot of the small-signal gain of circuit #3 of Table 3.6:

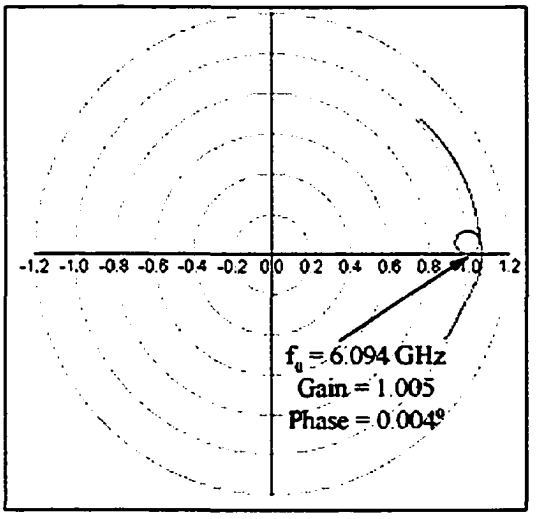


Figure 3.29: Polar plot showing sensitive Barkhausen Criteria for circuit #3 in Table 3.6

As can be seen from Figure 3.29, the peculiar small-signal response of the oscillator around the point (1,0°) at f_0 = 6.094 GHz caused extremely delicate fluctuations in the gain anywhere between 0.95 and 1.1 in the polar plot diagram. It became apparent that for values less than 1, the oscillator ceased to operate. The next step involved varying the circuit topology in order to decrease the volatility of the loop gain due to minor circuit modifications, i.e. to obtain a more continuous small-signal response around the point (1,0°). Again, the measure of performance gauged was the unvarying phase noise. From this analysis, the same circuit as #3 in Table 3.6, with different TL lengths, revealed an optimum phase noise result, while being insensitive to circuit variations. Thus, circuit #3 from Table 3.6 was replaced with circuit #3a with the following dimensions in Table 3.7 :

Table 3.7: New parameter dimensions for circuit #3 from Table 3.6

Circuit Topology			Oscillation Frequency [GHz]	Intersection Angle [°]	Phase Noise [dBc/Hz] @ 1MHz	Output Power [dBm]
$\lvert\Gamma\rvert\angle\Gamma^{\circ}$ Z_T [Ω] Lgate[nH]	TL electrical length[°]					
	source	drain				
#3a $0.5\angle 80^{\circ}$ $34.84 + j*45.75$ 1	74 S+P_sc	113 S	6.094	90	-153	14.57

The circuit was double-checked using the F-D and P-D device-lines, and the result revealed a 90° intersection as stated above, justifying the simulated phase noise performance. An ADS-generated layout of circuit #3a is given in Figure 3.30:

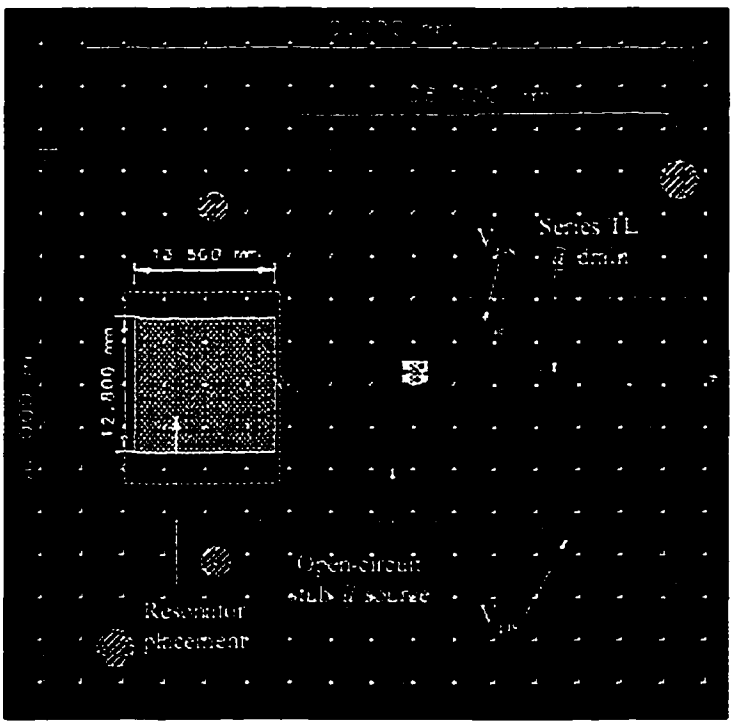
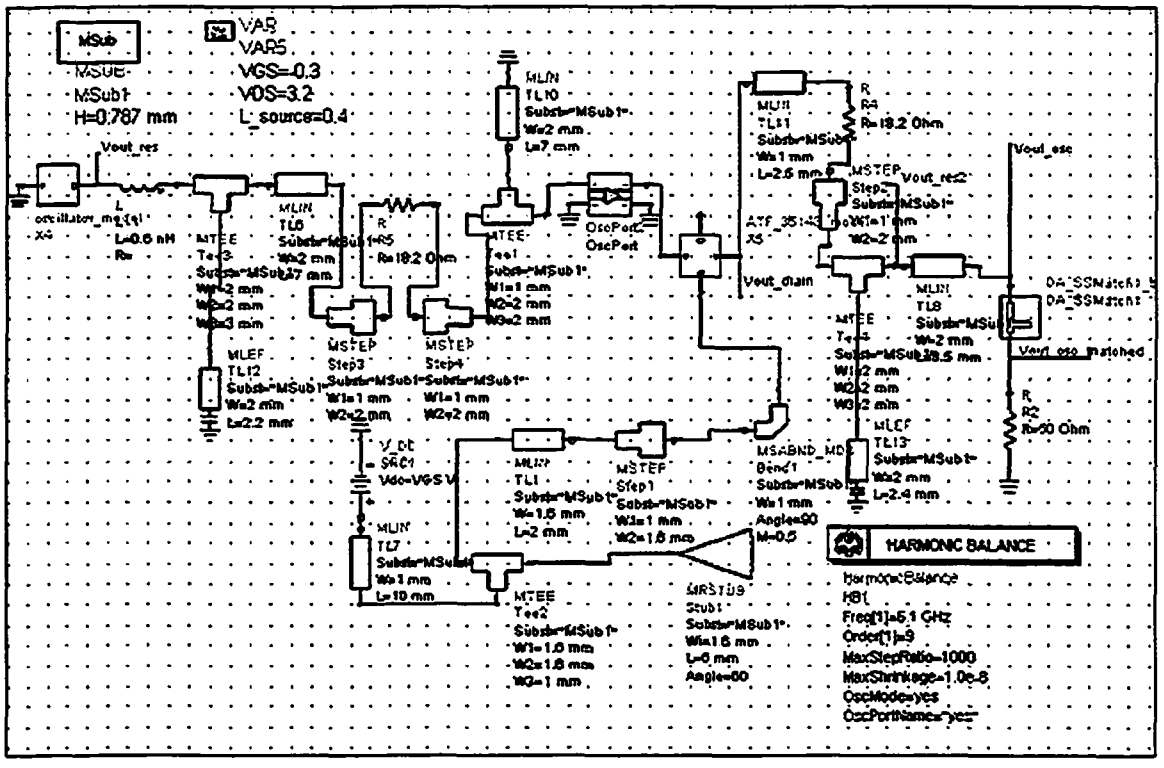
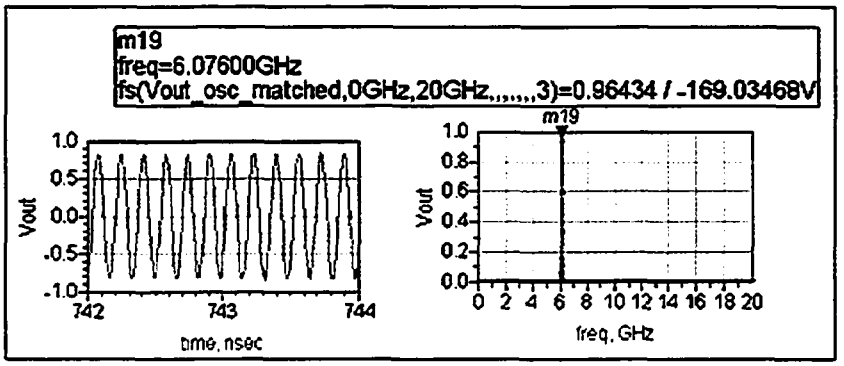


Figure 3.30: Layout of circuit #3a

Based on the above analysis in the previous paragraph, it was also determined, from simulation results of circuit #3a, that the oscillation condition was satisfied at an additional frequency to the oscillation frequency f_o = 6.094 GHz. This additional frequency, f_o = 5.314 GHz, was spotted from the polar plot of circuit #3a, and was verified with a transient analysis simulation, where the revealed oscillation frequency was not 6.094 GHz, but 5.314 GHz. Transient simulations, accompanied by FFT simulations, are used to obtain the components of the full frequency spectrum. Thus, from the simulation results, it was decided that a modification to circuit #3a would be needed in order to damp out the second oscillatory frequency. The approach adopted here is the one used for amplifier stability analysis. In simple terms, since oscillation is the result of instability at a particular frequency, the circuit can be rendered stable by the addition of either input or output resistors, or even both. Care was also taken to minimize the resistor values, since their noise voltage is directly proportional to their values. From this point of view, several iterations were attempted to make the circuit stable at f_o = 5.314 GHz, while maintining instablity at f_o = 6.094 GHz. Consequently, the employed resistive values were 18.2 Ω in the source and the drain. Figure 3.31 below illustrates the final circuit, circuit #3b, along with its simulation results:



(a)



(b)

Figure 3.31: Final circuit #3b for optimal low-phase noise design
(a) Circuit diagram (b) Transient analysis

The simulated phase noise resulting from circuit #3b in Figure 3.31 also revealed a respectable -148dBc/Hz @ 1MHz offset, comparable to the phase noise in Table 3.6. The layout for circuit #3b (with resistive frequency suppression) is given in Figure 3.32:

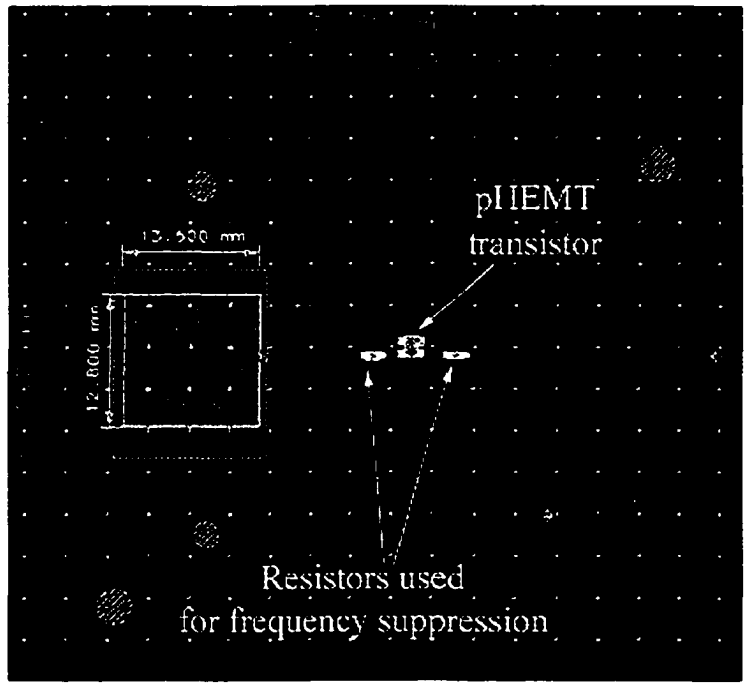
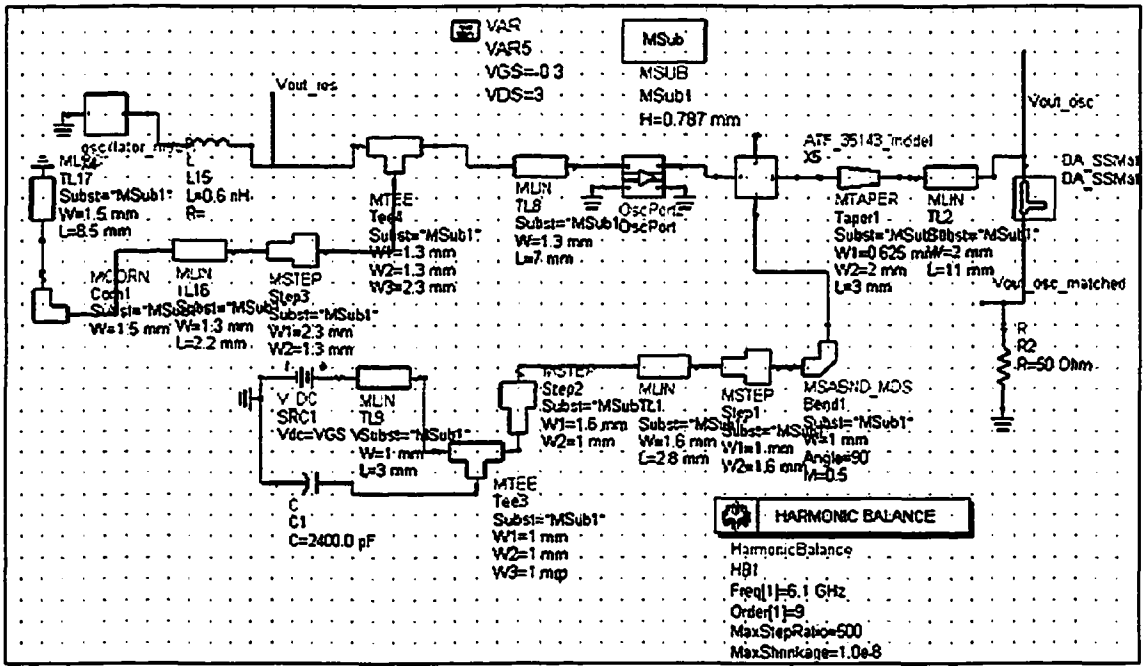
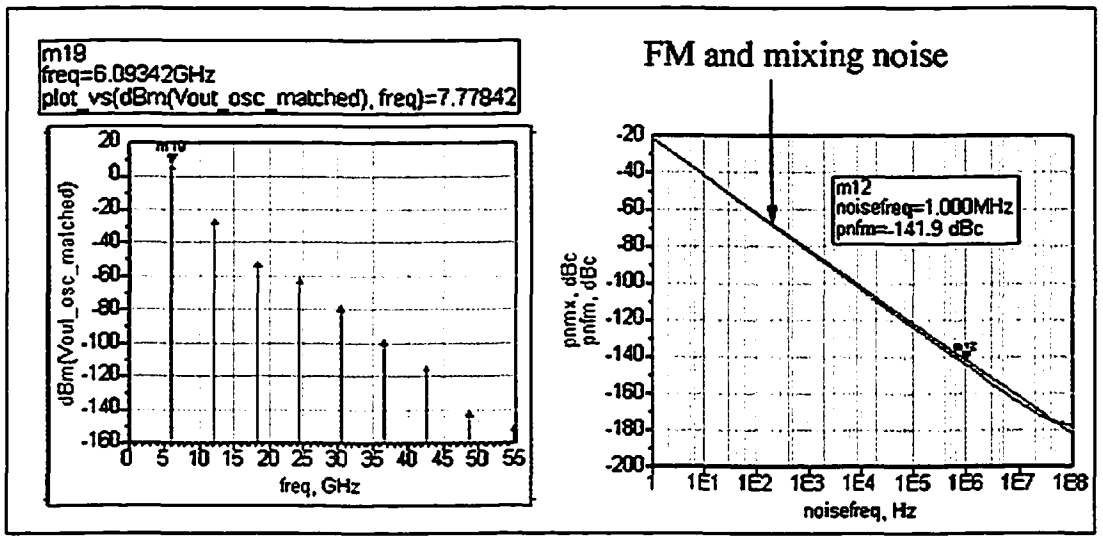


Figure 3.32: Layout of circuit #3b

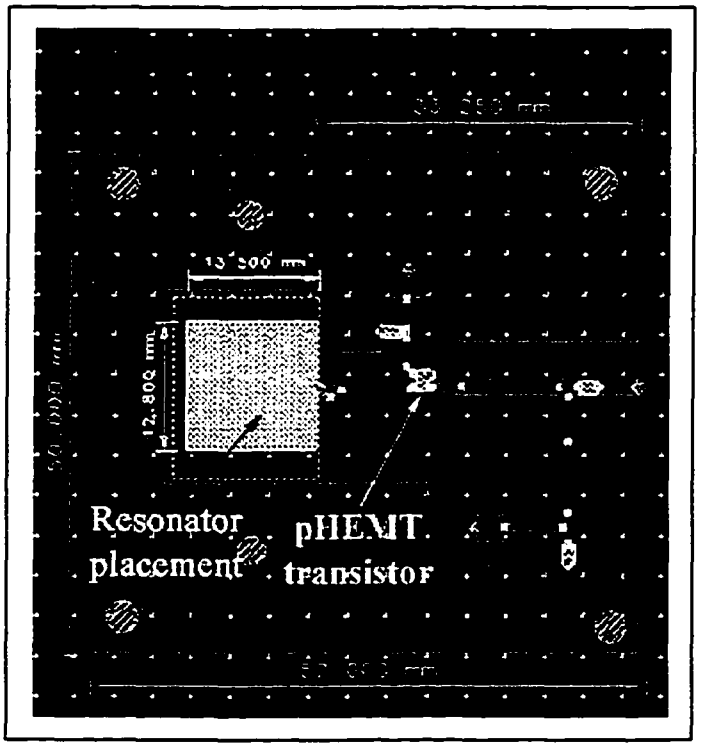
As mentioned in the beginning of this section, the third circuit that was implemented in microstrip was circuit #2 from Table 3.6. The lumped-element oscillator circuit was converted into microstrip equivalent circuit parameters. Figure 3.33 illustrates the final circuit for fabrication, along with final results and the layout:



(a)



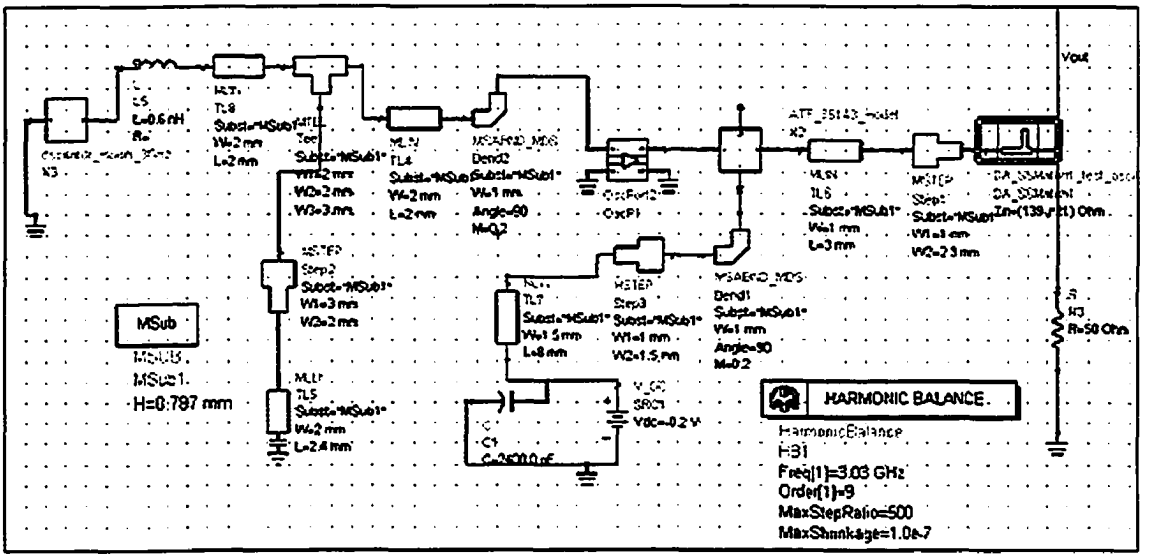
(b)



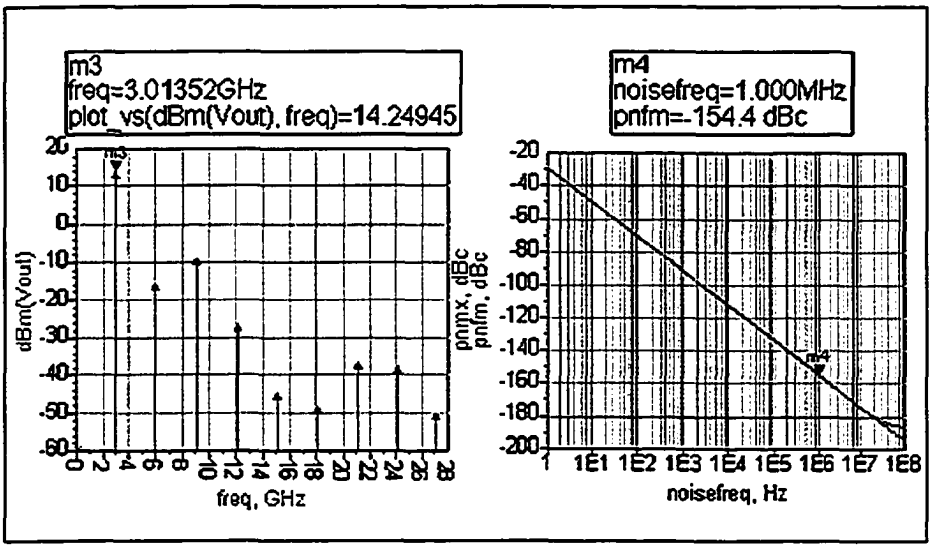
(c)

Figure 3.33: Final circuit #2 for non-optimal low-phase noise design (a) Circuit diagram (b) Harmonic Balance analysis (c) layout

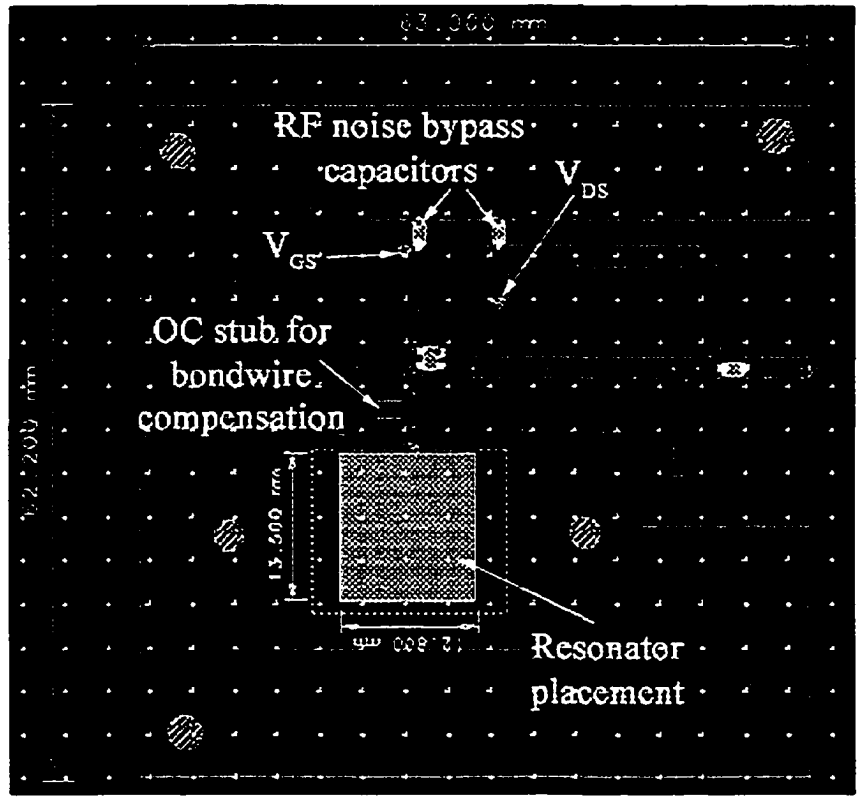
The final circuit to be fabricated in microstrip was circuit #7, which employed resonator #2. Similarly to the two previous circuits, the lumped-element oscillator circuit was converted to microstrip using distributed transmission lines, while being adjusted to meet the specifications. Figure 3.34 illustrates the circuit used for fabrication along with simulation results biased at V_{GS} = -0.2 V, V_{DS} = 4 V, and I_{DS} = 55 mA:



(a)



(b)



(c)

Figure 3.34: Final circuit #7 for optimal low-phase noise design
(a) Circuit diagram (b) Harmonic Balance analysis (c) Layout

3.5 – Conclusion

The work presented in this chapter gives the reader a detailed account of the strategy and design methodology adopted for designing low-phase noise oscillators using the *"device-line technique"*. The chapter commenced with a literature review of various oscillator design approached used over the years. A description of LTCC and its multi-purpose use followed, along with a presentation of the LTCC-based resonators using the high dielectric constant. The resonators are the first kind to report high ε_r results.

The device-line technique was clearly outlined in sequential number of steps to be carried out by circuit designers. Based on this method and the measurements of the LTCC resonators, the procedure was implemented utilizing the various circuit configurations as applicable tools. Based on the preliminary results, ideal transmission lines, mainly used as phase shifters, were needed to be added in order to fully execute the design methodology. Simulation results revealed excellent noise performance, solidifying the application of the aforementioned technique. Hence, several optimum performing circuits were chosen for conversion from lumped elements to microstrip technology.

Finally, a circuit sensitivity analysis was undertaken in order to remedy certain design issues that were unaccounted. This lead to the selection of the final design circuits to be fabricated. This completes the first and second thesis objectives.

CHAPTER 4

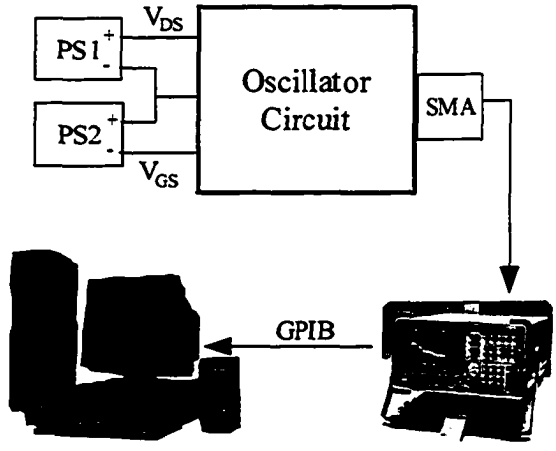
MEASUREMENT RESULTS AND DISCUSSION

This chapter will outline the various measurement results that were obtained while characterizing low phase noise oscillator designs. From the successive design approaches, the respective circuits that were fabricated are presented in this chapter. Thus circuit #3b, circuit #2, and circuit #7 all needed to be characterized. Phase noise was the most important performance feature considered throughout the measurements. However, power and frequency were also closely examined. The iterative process adopted for resolving unaccounted fabrication problems is presented here. As well, the measurement results are compared with the simulation results from Chapter 3, while being analyzed for performance qualification. Finally, the validity and applicability of the low-phase noise methodology is thus inspected.

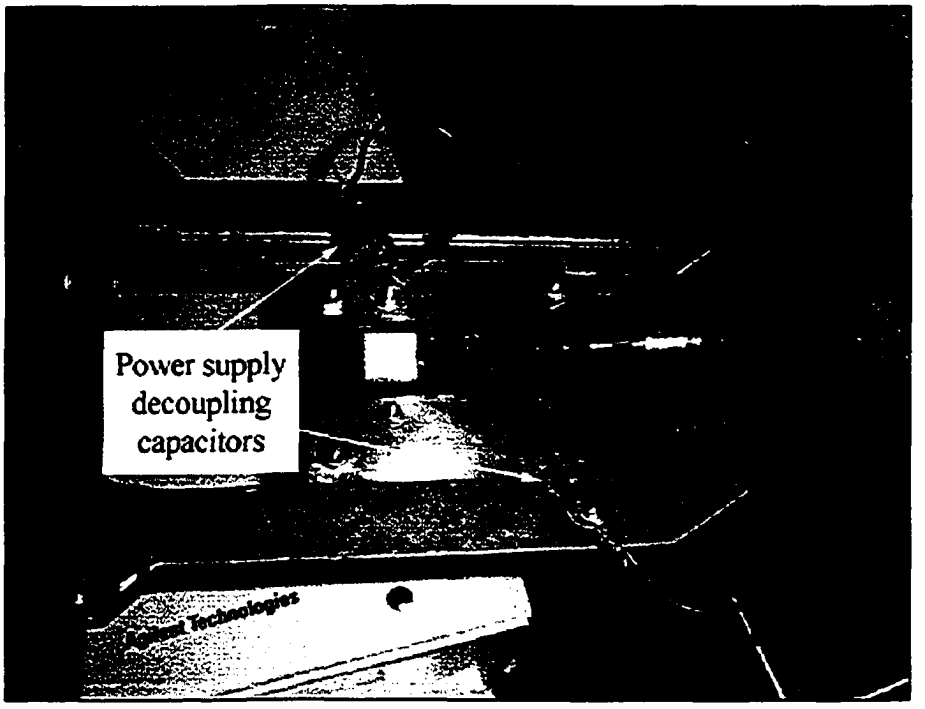
4.1 – Circuit Fabrication and Measurement Setup

As mentioned in Chapter 3, the circuits were manufactured in a hybrid manner, where the resonator, made from LTCC, was attached onto a metal plate using conductive silver epoxy. The plate was then attached to the rest of the circuit using metal screws and bolts in order to fasten it in place. Since copper is not a good bondable surface, a section of the TL was gold-plated in order to maintain a reliable bond. As well, due to the unevenness of the resonator and TL planes, the bondwires had to be arched in order to create a flexible connection. The LTCC resonator was then linked to the copper TL using gold ribbon-style bondwires, with a diameter of 75μm, and variable lengths around 0.75 mm, equivalent to the modeled inductance used in the design process. This technique allowed a single LTCC resonator to be separately integrated with multiple circuits. An illustration of the fabricated final circuits will be shown in the subsequent sections.

The measurement process was a simple procedure. Since the oscillator is a 1-port device, a spectrum analyzer (SA), Agilent 8564E, was used to measure the frequency, power, and phase noise. Figure 4.1 illustrates the setup along with circuit's external components:



(a)



(b)

Figure 4.1: Oscillator Measurement (a) Setup (b) external components

The type of measurement results is discussed next, since it is requires a mention in this work. It became apparent that the log plot measurement result of phase noise (PN) was not viable, where the $1/f^n$ response was either not distinguishable or severely distorted with discontinuities. Examining the documentation of Agilent's SA [4.1], it was noticed that in order to make measurements at offsets beyond 1MHz, the analyzer requires that input attenuation be set to 0 dB. The input attenuation helps protect the SA input from being damaged by too much power from the DUT, and its use should be minimized. The SA's input circuitry that is being protected is a downconversion IF mixer, with maximum input power of 0 dBm. Thus, it was concluded that for the oscillators of this work,

setting RF attenuation to 0 dB was not an option due to their high power performance. This was reflected in extreme bias point fluctuations when the SA's input mixer was driven into compression by high power levels. Thus, it was decided that PN measurements would be shown using the conventional manner described by (2.45).

4.2 – Initial Experimental Results

Figure 4.2 shows the completed circuit #3b as it was fabricated to be measured:

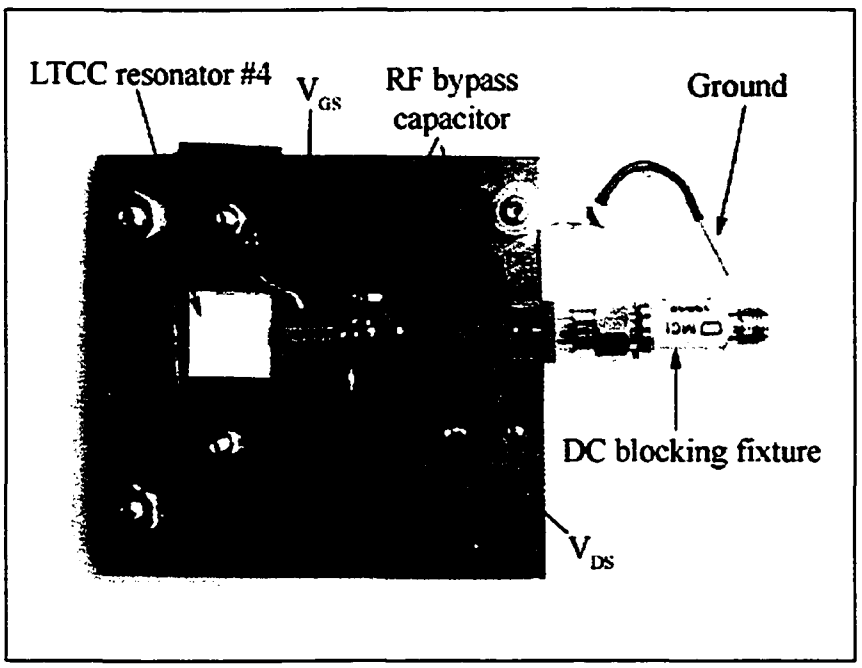
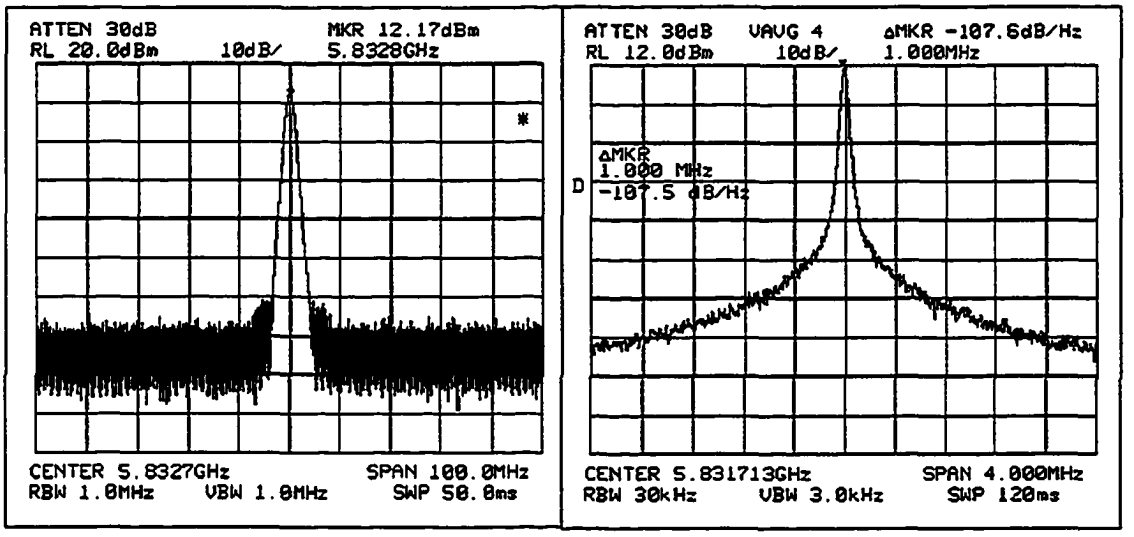


Figure 4.2: Picture of fabricated circuit #3b

The output signal results were measured and are shown in Figure 4.3, biased at V_{GS} = -0.32V, V_{DS} = 3.76V, and I_{DS} = 41mA:



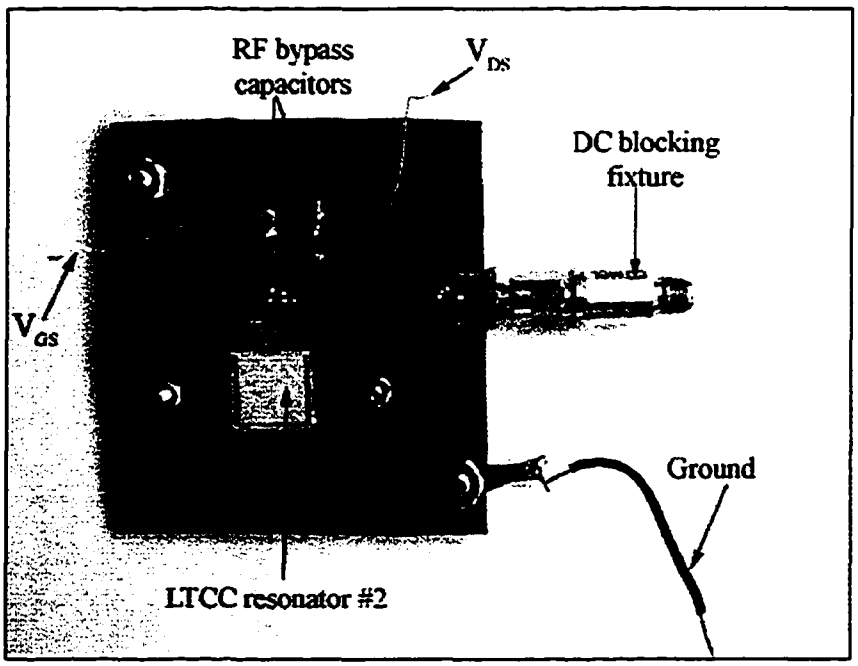
(a) (b)

Figure 4.3: Measured results for circuit #3b (a) Carrier frequency (b) Phase noise

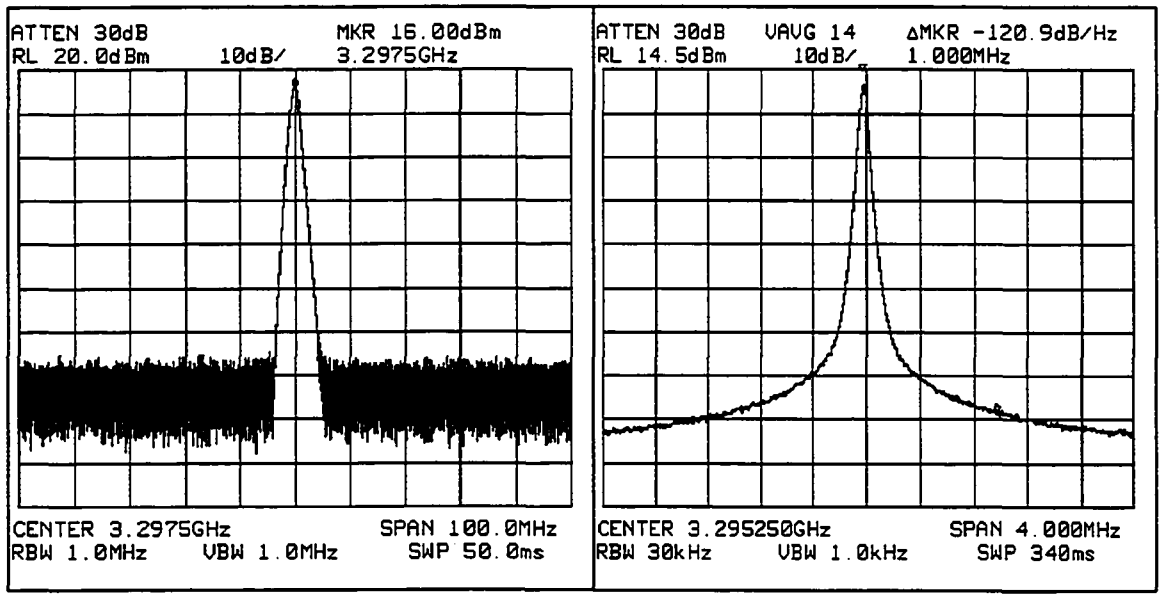
As can be seen, the oscillator produced large output power of 12 dBm at 5.83 GHz, with an average spot phase noise of -108 dBc/Hz @ 1MHz, and -90dBc/Hz @ 100 kHz. When compared to the results obtained from simulation shown in Table 3.6, it was quite clear that the targeted results were not attained. Thus, circuit #3b was re-simulated in ADS in order to establish the basis for such discrepancies. From small-signal analysis, it was concluded that the addition of the 2400 pF SMD capacitors shown in Figure 4.2 contributed to the birth of an oscillation condition at 5.95 GHz, where the results of Table 3.6 did not include the capacitor effects. Although their broadband response was characterized as low-loss, as shown in Appendix C, their addition as decoupling capacitors to filter out intrinsic noise elements heavily impacted the bias circuit's impedance.

Thus, it was decided that post-fabrication circuit tuning was necessary in order to eliminate the newly acquired oscillation frequency in order to truly characterize the phase noise response of circuit #3b.

Similarly, circuit #7 was also fabricated and measured. Figure 4.4 shows a photo of the fabricated circuit, along with its frequency response biased at V_{DS} = 4 V, V_{GS} = -0.23 V, I_{DS} = 51 mA:



(a)



(b) **(c)**

Figure 4.4: Measured results for circuit #2 (a) Picture of fabricated circuit #7

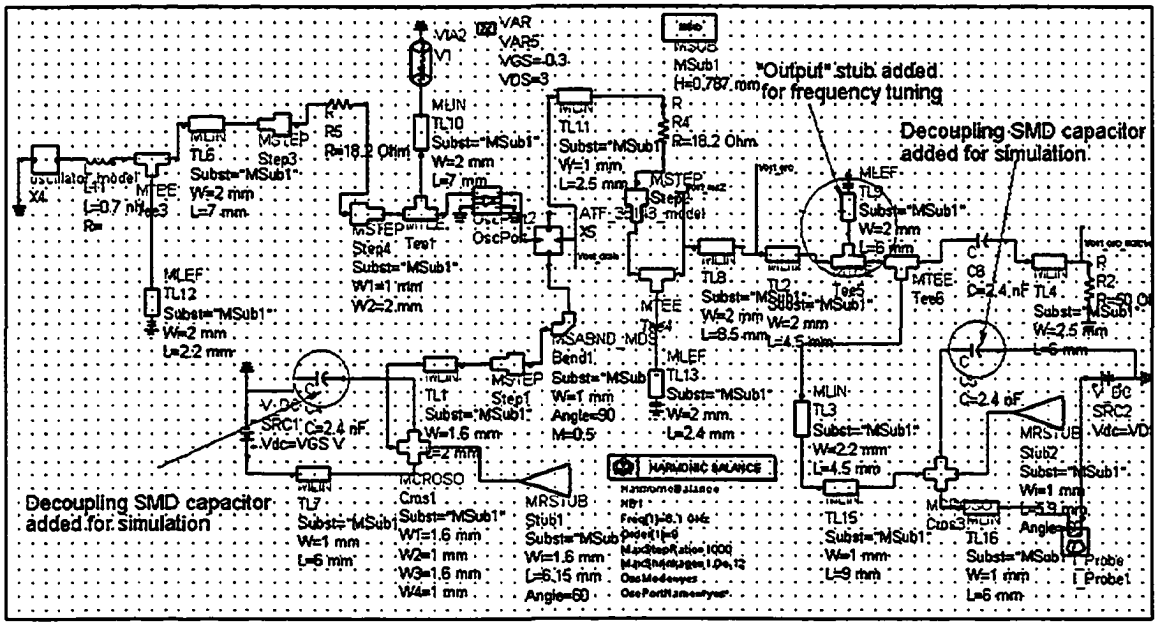
(b) Carrier frequency (b) Phase noise

Again, the oscillator showed high power output of 16 dBm at 3.3 GHz, as well as low phase noise at -121 dBc/Hz @ 1MHz and -85 dBc/Hz @ 100 kHz. Comparing the measured results with simulation, we can see that that output power exceeded expectations, with a significant difference in phase noise, and a mismatched oscillation frequency. The discrepancy in frequency is also attributed to the presence of a secondary oscillation condition at 3.4 GHz (similar to circuit #3a), which was noted in simulation but not presented in the previous chapter. Another iterative step to "stabilize" the circuit at its intended frequency of 3.03 GHz would lead to better phase noise results due to the theory of the device-line technique and the higher Q factor value of resonator #2.

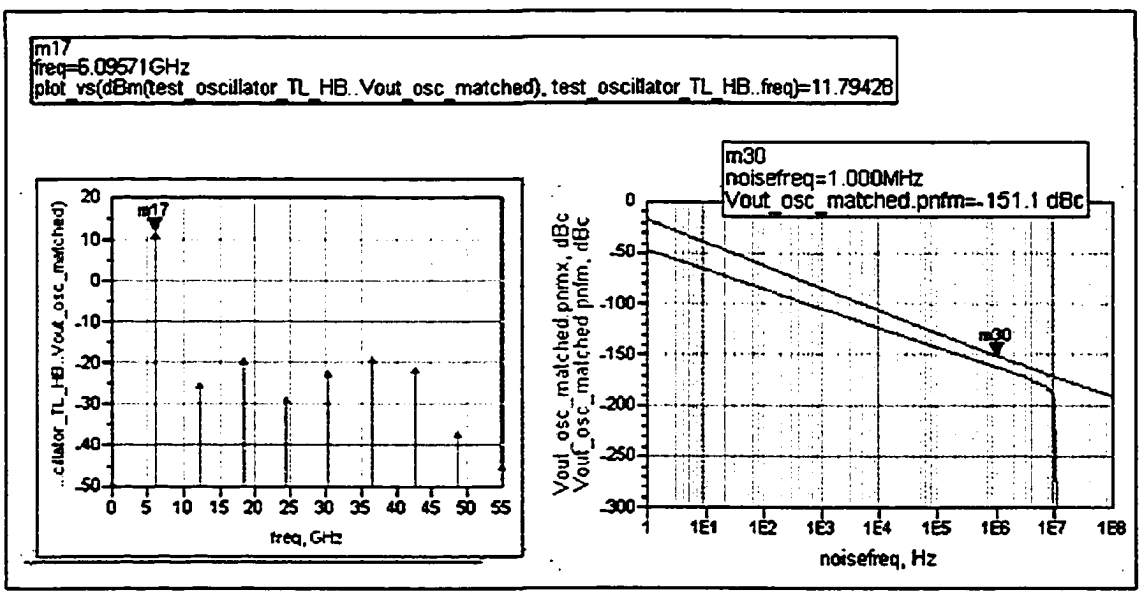
4.3 – Refined Circuit Simulations and Final Measurements

4.3.1 – Post-Fabrication Results – Simulated and Measured

As mentioned in the above section, circuit #3b required post-fabrication tuning to isolate the intended oscillation frequency as the sole operational one. Thus, several attempts were made to modify the circuit shown in Figure 4.2 to counteract the effects introduced by the decoupling SMD capacitors. The first attempt discussed for implementation was the actual removal of the decoupling caps. However, that choice was not beneficial since the capacitors do play an important role in noise filtering. The second attempt was the addition of a variable length open-circuited "input" stub at the source port of the transistor close to resonator. However, this resulted in degraded noise performance without any improvement in frequency. The third attempt was the addition of another variable length open-circuited stub at the drain of the transistor close to the termination network. This method revealed some promising results and it was immediately followed by simulation steps to identify the behavior of the "output" stub on the circuit's performance. Utilizing the same circuit as in Figure 3.31 with additional modifications, circuit #3b is shown in Figure 4.5 along with simulation results. As noted, the oscillation frequency is seen to be 6.096 GHz, very close to the targeted 6.094 GHz:.



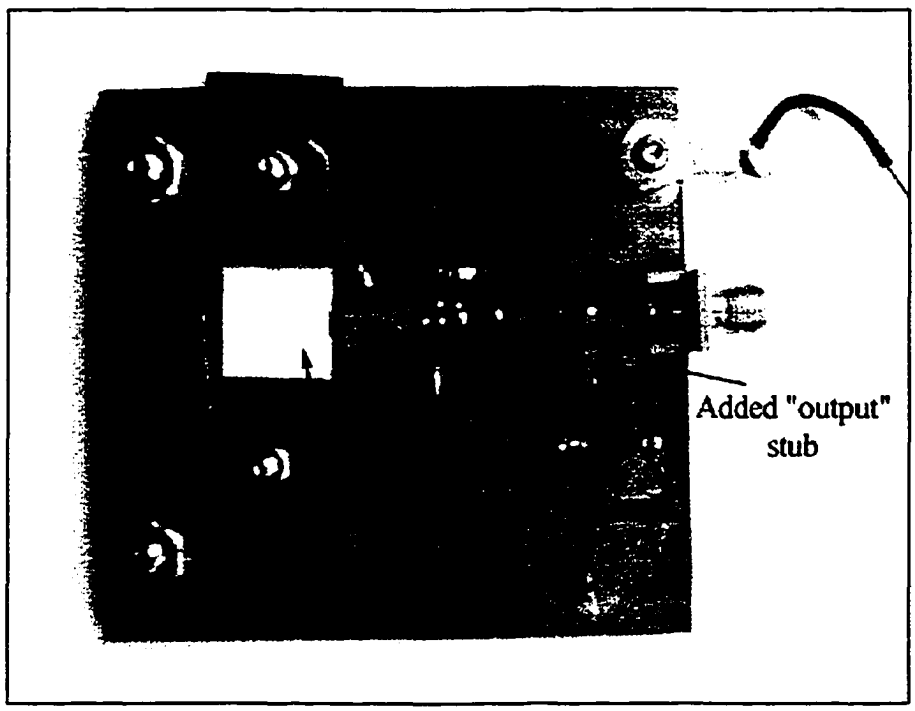
(a)



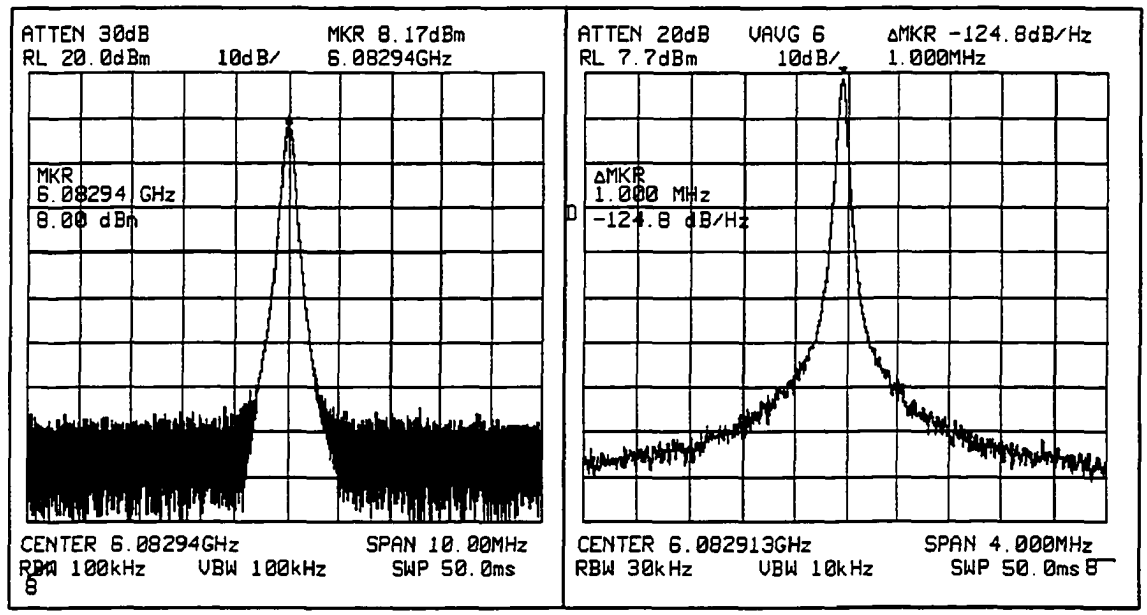
(b)

Figure 4.5: Post-fabrication tuning of circuit #3b (a) Circuit schematic (b) Simulation result

A stub placed at the "output" of the oscillator circuit having a length of 6 mm thus produces low phase noise results, eradicating the secondary oscillation frequency at 5.96 GHz. It was then decided that the "output" stub would be added to the fabricated circuit of Figure 4.2, i.e. circuit #3b, through the use of copper tape as shown in Figure 4.6 along with measurement results biased at V_{GS} = -0.33 V, V_{DS} = 3 V, and I_{DS} = 35 mA :



(a)



(b) (c)

Figure 4.6: Post-fabrication modification of circuit #3b (now circuit #3c)
(a) Photo of the modified circuit (b) Carrier measurement (c) Phase noise measurement

Comparing results in Figure 4.6 to Figure 4.3, it is apparent that the "output" stub accomplished its stated goal of frequency and phase noise improvements. Although the measured results do not exactly match with simulations of Figure 4.5 (b), their proximity reveals a good design case for circuit #3b with its adopted modifications, thus yielding circuit #3c. In order to illustrate that point, the circuit was investigated from a device-line's perspective in order to examine the intersection of the P-D line with the resonator locus. The simulation setup, applied to circuit #3c is similar to the one shown in Figure 3.18 (a), with results shown in Figure 4.7 below:

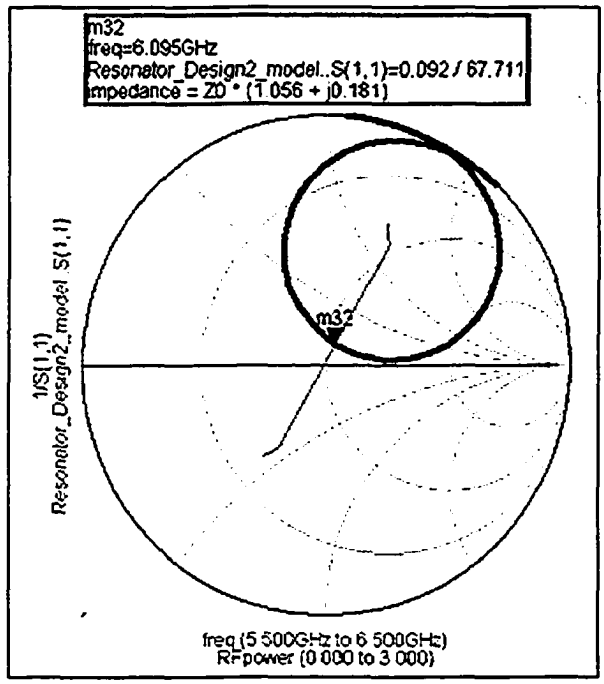


Figure 4.7: Device-line illustration of nominal circuit #3c

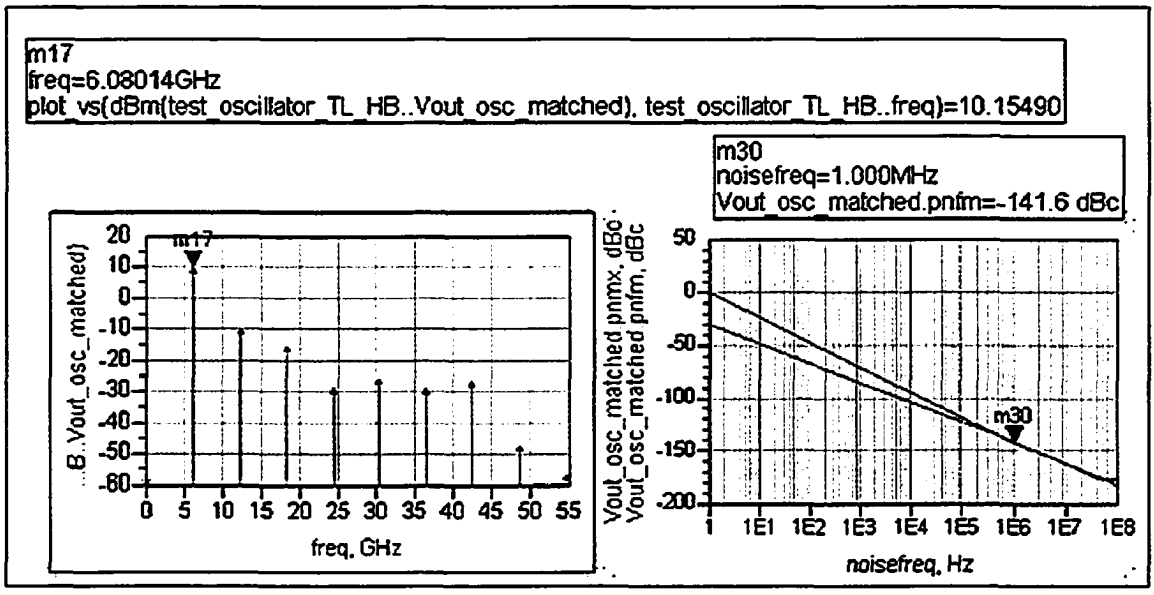
As can be seen, the P-D device line at the input of the oscillator circuit from the resonator side intersects the resonator locus in an orthogonal manner. As per the design methodology outlined in Chapter 3, this is a condition that must be satisfied for lowest phase noise, which is supported by the simulation results in Figure 4.5 (b). Thus, we can intuitively conclude that circuit #3c is also an optimally designed circuit for phase noise performance, and will therefore be labeled as "nominal design".

4.3.2 – Study of Phase Noise Performance

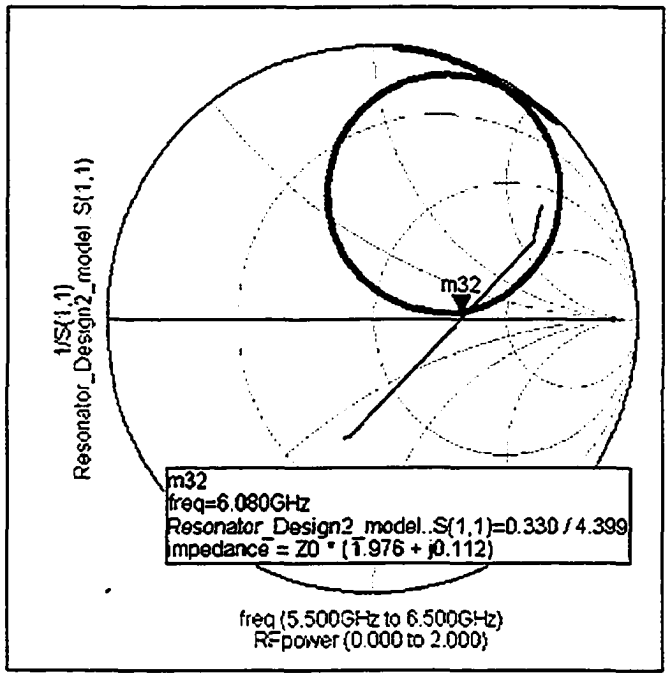
We will now commence the task of studying phase noise performance comparatively to the nominal design case. As mentioned in Chapter 3, several designs were simulated showing non-orthogonal device-line intersections in order to perform

phase noise measurements for evaluation. However, in light of the various problems encountered in the fabrication and measurement of the optimal design circuit, it was decided that the non-orthogonal designs would not be fabricated, and instead phase noise analysis would be accomplished through another set of modifications applied to circuit #3c. The goal is to disturb the orthogonality of the device-lines by circuit tuning procedures in order to examine the phase noise performance response. Thus, two easily implemented changes have been chosen: a modification of the "output" stub length, and a modification of the bias point, both applicable to circuit #3c.

We will begin by investigating the change applied to the stub length first through simulation, and then through measurement. From simulation, the goal was to obtain a P-D device-line that exhibits a non-orthogonal intersection with the resonator locus. The simulation results are thus shown in Figure 4.8:



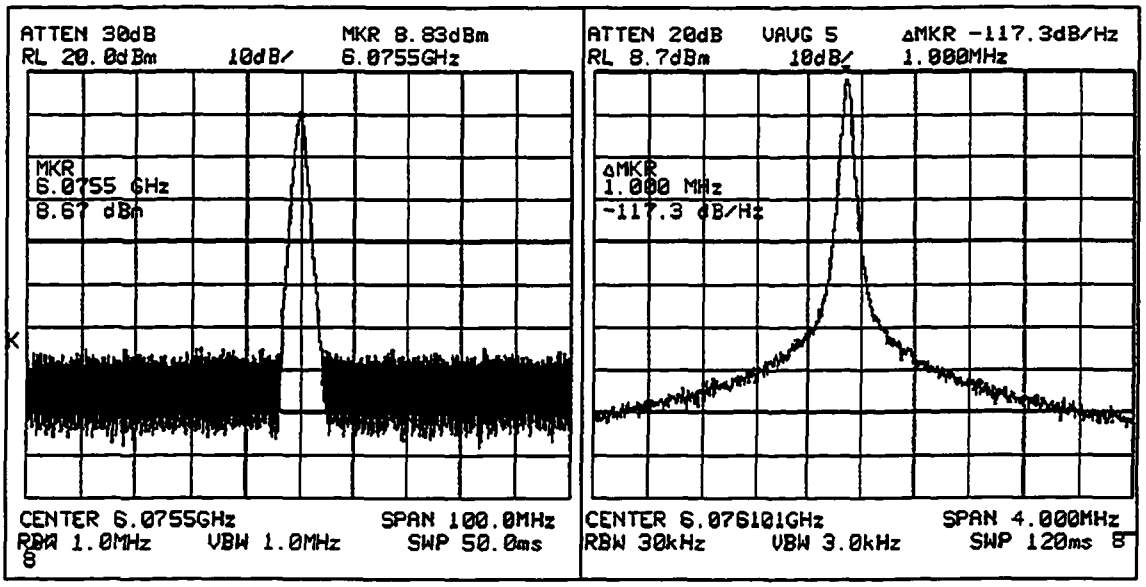
(a) (b)



(c)

Figure 4.8: Circuit #3c with stub modification simulation results
(a) Carrier frequency (b) Phase noise (c) Device-line intersection

The "output" stub length was shortened to 4 mm from 6 mm. As the results show in Figure 4.8 (c), a non-orthogonal intersection between the P-D device-line and the F-D resonator locus at 6.080 GHz was successfully generated. When simulated using HB, the phase noise expectantly worsened, compared to Figure 4.5(b). Thus, the listed modifications were applied to circuit #3b, and the resulting circuit was measured, as shown in Figure 4.9:

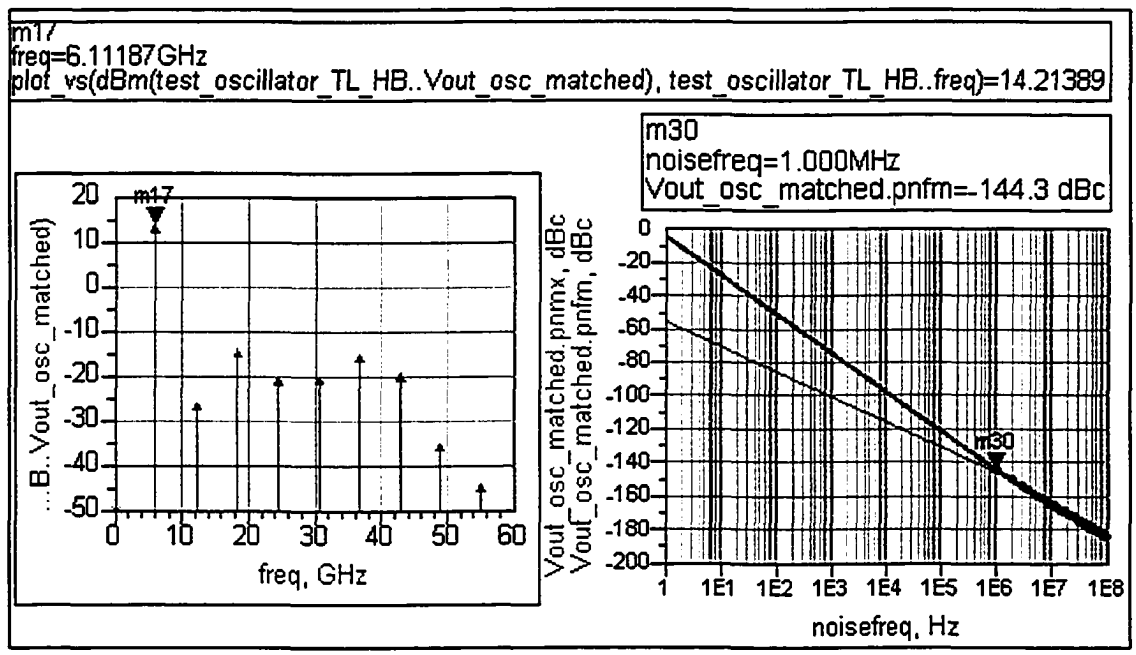


(a) (b)

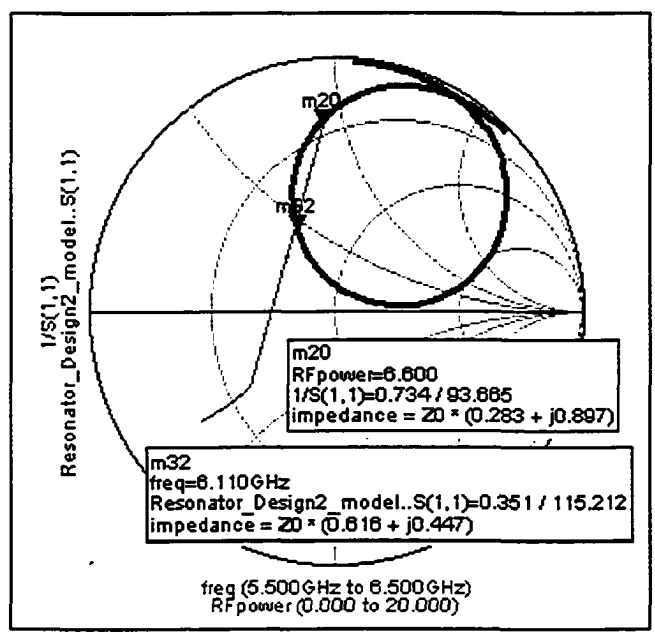
Figure 4.9: Measurement results of circuit #3c with output stub modification
(a) Carrier measurement (b) Phase noise measurement

Examining the results of Figure 4.9, it can be seen that the measured oscillation frequency (6.075 GHz) and power (8.83 dBm) compared well to the simulated results in Figure 4.8 (6.080 GHz and 10.15 dBm respectively). As well, the deterioration in measured phase noise (8 dB) was also relatively comparable to the results in Figure 4.8 (10 dB), reinforcing the effect of a non-orthogonal intersection for sub-optimal design.

The change in bias was investigated as the next step. Bias modification originated from [3.31], where the authors were able to shift the P-D device-line by manipulating the drain voltage of the active device. This step could also be included in the design methodology outlined in 3.3.1, however it was omitted to minimize the available variable parameters. Again, taking the nominal design of circuit #3c, and adjusting its bias point, this behavior was achievable in simulation. Figure 4.10 reveals the results of the simulations with a bias point of V_{GS}=-0.32 V, V_{DS} = 5.5 V, I_{DS} = 52 mA:



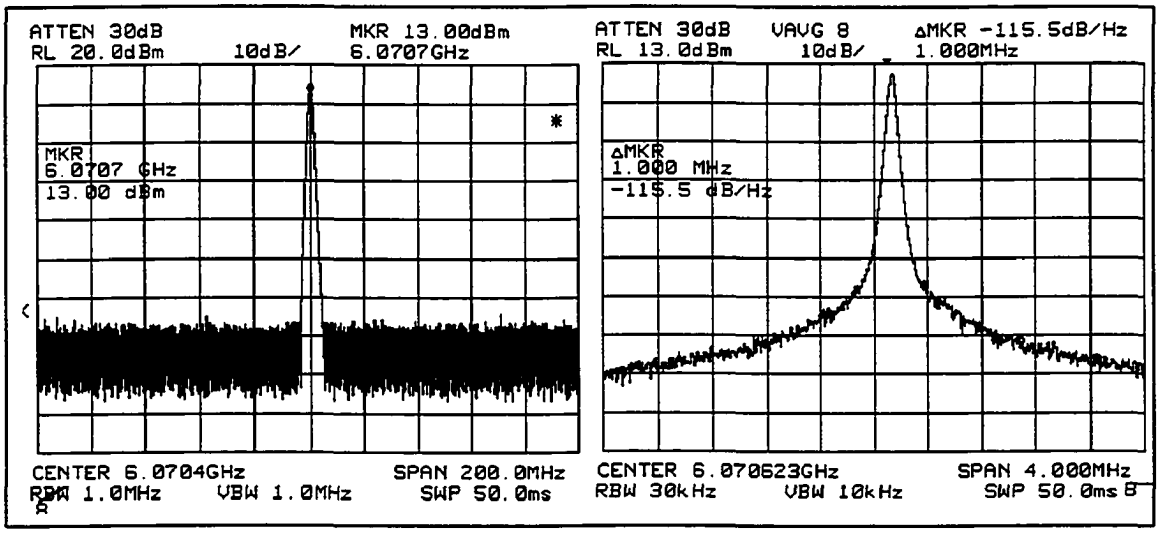
(a) (b)



(c)

Figure 4.10: Circuit #3c simulation results with bias point modification (a) Carrier frequency (b) Phase noise (b) Device-line intersection

Although the above simulation results indicated a degradation in phase noise, a more significant effect was required in order to notice a difference in phase noise levels. Thus, when measured, the circuit bias point was driven to its maximum limits, something that the model fails to replicate. At a bias point of V_{GS}=-0.32 V, V_{DS} = 6.5 V, I_{DS} = 65 mA, the following results in Figure 4.11 were obtained:



(a) **(b)**

Figure 4.11: Results of circuit #3c with bias point modification
(a) Carrier measurement (b) Phase noise measurement

Of note here is that as the bias was linearly increased in measurement, the oscillation frequency also linearly increased until it reached a threshold level, where it began to decrease. Thus, it was determined that the high bias point of operation lead to device compression, which might have contributed to the degradation of phase noise. Therefore, although the bias point delta simulations did not accurately resemble the measurement results, an illustration was made to indicate that varying the bias point does shift the P-D device-line, which leads to a worsening of the phase noise. Of note again is the

deficiency of the transistor model for simulation, where it became apparent the breakdown of the model occurred at high V_{DS} bias point.

4.3.3 – Summary, Comparisons, and Discussion

In the previous section, we have clearly demonstrated the performance of the designed oscillators using the LTCC resonators built with the newly introduced high ε_r material. The resonators revealed respectable Q factor numbers, and contributed to the phase noise performance of the measured oscillators. Table 4.1 below summarizes the main characteristics of the oscillator performances:

Table 4.1: Summary of measured oscillators

Oscillator Specification	3.03 GHz Oscillator			6.094 GHz Oscillator		
	Predicted	Measured	Error	Predicted	Measured	Error
Frequency of Oscillation [GHz]	3.014	3.3	9.5%	6.096	6.083	-0.21%
Output Power [dBm]	14.25	16	2.2 dB	11.8	8.17	-3.6 dB
Phase Noise [dBc/Hz @ 1MHz]	-154	-121	21.4	-150	-125	-16.7
DC-RF Efficiency[%]	12.2	16.1	4 %	12.3	6.25	-6%
Max.[d] Harmonic Levels [dBc]	-24	-20	4 dB	-19	-19	0 dB
Tuning Range [MHz]	-----	25	----	-----	30	----

As is generally found with CAD tools, the absolute value of predicted phase noise is significantly underestimated. However, the relative shift in predicted phase noise levels between the nominal and modified cases agree very well with the measured results.

The application of the device-line technique to design low phase noise oscillators has also been verified by the results mentioned in the above section. From circuit #3c's measurement results, it was concluded that this optimally designed oscillator produced the lowest possible phase noise value for this particular case. This was confirmed by the device-line simulation results of circuit #3c, where an orthogonal intersection of the P-D device line with the F-D resonator locus was observed. As well, two counter examples were given in order to supplement the device-line theory, where non-optimal designs were considered by varying various circuit parameters. This was also verified through simulation by the resulting non-orthogonal intersection of the curves. Table 4.2 contains a summary of the results:

Table 4.2: Summary of device-line phase noise study

Circuit Type	Circuit #3c	Circuit #3c with stub modification	Circuit #3c with bias point modification
Oscillation Frequency [GHz]	6.082	6.076	6.071
Phase Noise [dBc/Hz @1 MHz]	-125	-117	-115.5
Simulated Angle of Intersection*	90°	40°	165°
Output Power [dBm]	8.17	8.67	13

* All results measured, except this one

As can be seen from Table 4.2, phase noise is the most indicative mark of the validity and applicability of the device-line technique for oscillator design. Thus, it can be safely

concluded that to design an oscillator exhibiting the lowest phase noise possible, it suffices to have the device line and resonator locus intersect orthogonally. On the other hand, phase noise can be made manageable by controlling the intersection angle. However, more studies would have to be undertaken in order to determine the nature of that relationship. As for the power performance of the oscillators in Table 4.2, it can also be seen that good power output was produced by the designs, which is uncommon with low phase noise designs. The output power can also be predicted by the device-line technique, similar to Figure 2.11 (b), where the intersection point on the P-D device-line with the resonator locus reveals the output power level of the oscillator. In the case of this work, the output power is not extracted from the plane where the device-line is applied, but from the terminating impedance plane. By transferring the power measurement to the terminating port, i.e. output port for this work, the output power can be characterized very accurately using the device-line method. Although, not mentioned in the above section, the output power predictions using the device-line technique did correspond to the power output levels predicted by HB simulations. Thus, examining the power of circuit #3c with the stub modification, it is not surprising that the frequency and output power shifted, due to the total movement of the device-line in terms of frequency and power, as illustrated in Figure 3.13. This is another advantage of the technique, where as mentioned above, not only are phase noise levels controllable, but output power levels are also manageable.

It is interesting to compare the results of this work with recently published C-band oscillatiors. Table 4.3 cites the results of eight other authors along with this work:

Table 4.3: Summary of published performance results

Reference Year	Active Device	Circuit Type	Oscillation Frequency [GHz]	Phase Noise [dBc/Hz]		FOM	Expanded FOM
				100 kHz	1 MHz		
[4.2] 2001	GaAs MESFEST	MMIC Cross-Coupled Differential	6.44	-92	-111	----	----
[4.3] 2001	GaN FET	Ceramic Substrate	6	-90	-120	-152	-166.3
[4.4] 2002	SiGe HBT	Monolithic Coupled VCO	6.3	-104	-125	-185	---
			5.9	-106	-124	-184.2	---
[4.5] 2004	GaN HEMT	Monolithic BST	5.3	-105.9	-125	----	-----
[4.6] 2001	GaAs MESFET	MMIC Push-Push VCO	6.448	-92	-112	----	-----
			6.689	-98	-120		
[4.7] 2005	0.18 µm CMOS	Monolithic Differential Colpitts	5	----	-120	189.6	-191.4
[4.8] 2003	0.18 µm CMOS	FR-4	5.8	-85	-110	-176.2	-172.2
[4.9] 2002	0.24 µm CMOS	Monolithic	5.8	----	-112	-176.3	177.2
[This Work]	**GaAs pHEMT**	**Hybrid**	**6.082**	**-92**	**-125**	**-180.5**	**-189**
			3.3	**-85**	**-121**	**-168.3**	**-184.3**

In Table 4.3, FOM refers to the oscillator figure-of-merit [2.18] stated in equation (2.66). Since FOM does not take into account the output power of the oscillator, an expanded FOM was incorporated based on (2.66):

$$FOM = 10\log\left[\frac{S_{SSB}(linear)\left(\Delta f / f_o\right)^2 P_{DC}(mW)}{P_o(mW)}\right] \qquad \textbf{(4.1)}$$

Where P_0 is the output power of the circuit. Other performance values can also be incorporated in the FOM such as tunability, efficiency, stability, etc. The benefit of the newly proposed FOM can be seen when examining the 3.3 GHz oscillator, where power consumption was high, however offset by high output power to reveal a good FOM. Consequently, for the C-band of the oscillator presented in this work, it can be seen that its low phase noise performance measures extremely well against the best published circuits, which validates the adopted design strategy as a legitimate phase noise reduction technique for circuit designers.

4.4 – Conclusion

In this chapter, high performance microwave oscillators utilizing new LTCC-based resonators have been characterized and demonstrated. For the first time, oscillator circuits employing pre-commercial high dielectric-constant resonators along with an easily integrated phase noise reducing technique demonstrated good quality results in terms of phase noise and power. It is believed that this technique has been under-utilized by the microwave community, and can be widely available for general use in circuit

design. Agreement with predicted results using available CAD tools and models was found to be very good. This, along with the proof of concept of compact low phase noise oscillator in LTCC using very high ε_r materials, fulfills the last two objectives of this thesis.

CHAPTER 5

CONCLUSIONS, CONTRIBUTION, AND FUTURE WORK

5.1 – Conclusions

The fundamental oscillator principles starting from circuit feedback theory and ending at microwave negative resistance theory have been reviewed. The device-line technique has been mathematically presented. Based on this formulation, the basis for orthogonal intersection between device-line and resonator locus on the Smith Chart was established. Finally, two phase noise models have been examined and their resulting design guidelines highlighted. This partially fulfills the first thesis objective.

A detailed account of the strategy and design methodology adopted for designing low-phase noise oscillators using the *"device-line technique"* was stated. A description of LTCC and its multi-purpose use was also outlined, along with a presentation on the design of LTCC-based resonators using the high dielectric constant. The resonators are the first kind to report high-ε_r results.

The device-line technique was clearly outlined in sequential number of steps to be carried out by circuit designers. Ideal transmission lines, mainly used as phase shifters, were used as "device-line technique" enhancers in order to fully implement the methodology. Simulation results revealed excellent noise performance, solidifying the application of the aforementioned technique. Hence, several optimum performing circuits were chosen for conversion from lumped elements to microstrip technology. Finally, a circuit sensitivity analysis was undertaken in order to remedy certain design issues that were unaccounted. This lead to the selection of the final design circuits to be fabricated. This completed the first and second thesis objectives.

High performance microwave oscillators utilizing new LTCC-based resonators have been characterized and demonstrated. For the first time, oscillator circuits employing pre-commercial high dielectric-constant resonators along with an easily realizable phase noise reducing technique demonstrated good quality results in terms of phase noise and power. It is believed that this technique has been under-utilized by the microwave community, and can be widely available for general use in circuit design. Agreement with predicted results using available CAD tools and models was found to be very good. This, along with the proof of concept of compact low phase noise oscillator in LTCC using very high ε_r materials, fulfills the last two objectives of this thesis.

5.2 – Contributions

The following contributions were recorded in this work in S/C microwave band:

- LTCC resonator useful for system-on-package;
- $\varepsilon_r = 68$ LTCC material for miniaturization of high-Q resonators;

- Investigation of noise reduction techniques through circuit parameters;
- Enhanced low phase noise design technique adaptable to any technology, device, an resonator.

5.3 – Future Work

In terms of future work to complement this thesis, a few things can be discussed. Since LTCC-based resonators are a major part of this work and the main contributors to phase noise reduction, further research would be needed in order to improve the Q of the C-band resonators. Since Qs in the thousands were reported, it is of major benefit to further the resonator design process.

As well, an added advantage would be gained by integrating the high-Q resonators and the oscillator circuit onto one LTCC module making a seamless connection between the resonators and the surrounding circuitry. This would minimize the extrinsic losses associated with a hybrid design. All the mean while, the device-line technique can also be implemented to complement the high-ε_r module for even further phase noise reduction. As well, the ability to add low-loss tunability to the LTCC oscillator would enhance its application.

A study of the relationship between the intersection angle from the device-line technique and phase noise should be explored. The ability to leverage phase noise in lieu of other design parameters is an attractive feature for a circuit designer. Moreover, a more detailed characterization of the effect of this noise-reducing technique on close-in phase noise is also advantageous.

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APPENDIX A

Appendix A1 - Feedback Oscillator Theory

A1.1 – Barkhausen Criteria

In its most basic form, an oscillator can be described as an unstable amplifier having a frequency-selective network in the feedback path. Therefore, an oscillator circuit consists of three main components: an active device that acts as an amplifier, a feedback network to provide positive feedback in the system, and a nonlinear control mechanism to stabilize the amplitude. Figure A1.1 shows, in block form, the necessary components of an oscillator. It contains an amplifier with a frequency-dependent forward loop gain $G(j\omega)$ and a frequency-dependent feedback network $H(j\omega)$.

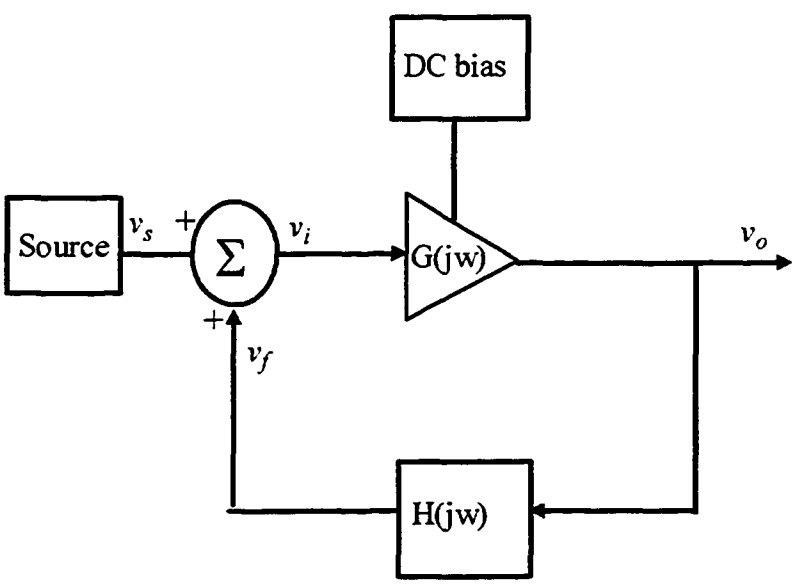


Figure A1.1: Block diagram of oscillator circuits

The illustration indicates the use of regenerative (positive) feedback for sustained oscillations. To maintain oscillations without external input, we will first have to examine the loop equations and their frequency interactions. To begin, we have:

$$T(j\omega) \equiv \frac{v_o(j\omega)}{v_s(j\omega)} = \frac{G(j\omega)}{1 - G(j\omega)H(j\omega)} \tag{A1.1}$$

Where $T(j\omega)$ represents the closed-loop transfer function. Thus, the loop gain $G(j\omega)H(j\omega)$ is a complex number that can be represented by the following:

$$L(j\omega) \equiv G(j\omega)H(j\omega) = |G(j\omega)H(j\omega)|e^{j\phi(w)} \tag{A1.2}$$

Where $L(j\omega)$ is the loop gain composed of magnitude and phase. Without turning on the system, if it is possible that, at a specific frequency ω_0, $L(j\omega) = 1$, then $T(j\omega)$ will be infinite. This indicates that at this particular angular frequency, the circuit will have a finite output signal while having a zero input signal. Hence, the following is the definition of oscillations:

$$\begin{aligned} &T(j\omega) = \infty \quad \text{iff} \quad G(j\omega) = \infty, \text{ or} \\ &1 - L(j\omega) = 0 \end{aligned} \tag{A1.3}$$

Since the gain of an amplifier, $G(j\omega)$, cannot be infinite, we are left with the oscillation condition:

$$L(j\omega_0) = |G(j\omega_0)H(j\omega_0)|e^{\phi(w)} = 1 \quad or \quad |G(j\omega_0)H(j\omega_0)| = 1 \tag{A1.4}$$

and

$$\phi(\omega_0) = \angle G(j\omega_0)H(j\omega_0) = 2n\pi \quad for\ n = 0,1,2,\ldots \tag{A1.5}$$

In other words, the Barkhausen Criteria states that if the loop gain $L(j\omega) = 1$ and $\angle L(j\omega) = 0^{\circ}$ at ω_o, then oscillations will occur at ω_o. Since the amplitude of oscillation is associated to the gain of the active device, equation (A1.4), known as the open-loop gain or simply loop gain, sets the oscillation amplitude. On the other hand, equation (A1.5), known as the loop phase, sets the oscillation frequency.

In order to visualize how the feedback network maintains oscillations, let us examine the mechanism for sustainable oscillations. With noise being ever present in any active circuit, an oscillator can also be called a noise amplifier. When DC bias power is applied to the circuit, it will generate a disturbance in the network while introducing a signal $V_n(t)$ at the input of the amplifier, consisting mainly of noise frequencies. As a result, with the presence of the active device acting as an amplifier, the energy transferred to the noise frequencies will be augmented. With this process continuously flowing through the closed-loop, noise amplification is repeated, and hence sustained oscillations take form within the loop. As the newly amplified noise signal is subjected to the passive network, all frequencies will be filtered out due to the latter's selectivity, allowing only the desired components to circulate. After a certain period of time, the amplified RF signal flowing in the loop will have reached a large enough amplitude to drive the device into nonlinearity, thus becoming saturated while self-regulating the signal amplitude [2.1]. This will be discussed in a later section, however, we will now mention the start-up conditions related to the Barkhausen Criteria:

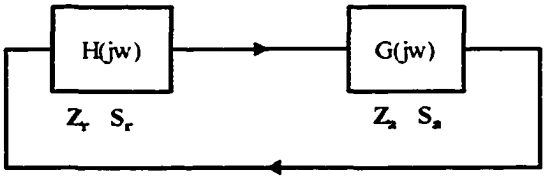
$$|G(j\omega_0)H(j\omega_0)| > 1 \qquad \textbf{(A1.6)}$$

$$\angle G(j\omega_0)H(j\omega_0) = 2n\pi \quad for\ n = 0,1,2,... \qquad \textbf{(A1.7)}$$

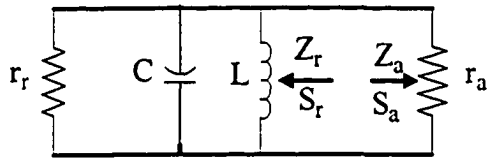
In order to commence oscillations, the start-up conditions indicate that the loop gain must be larger than one, while having a loop phase of zero. This is compared to (A1.4) and (A1.5) which designate the steady-state conditions.

A1.2 – Root-Locus Diagram: Poles and Zeros

When examining the ability of a circuit to oscillate, the underlying question of oscillation quickly revolves around the operating point's stability. The start-up conditions are one of the more widespread techniques for testing oscillator stability: "When the phase of the transfer function is zero and the magnitude, at the same frequency, is larger than one, then the system is unstable". Odyniec [2.2] states that the criteria are not necessarily true and should be replaced with the Nyquist plot and pole location analysis. Figure A1.2 illustrates a linearized oscillator that fails to demonstrate instability with $|S_a S_r| > 1$ and $\arg(S_a) = -\arg(S_r)$, equivalent to the start-up conditions of (A1.6) and (A1.7). Furthermore, Odyniec states that the steady-state Barkhausen Criteria can be correctly applied only when circuit analysis is done under large-signal conditions. So, what is the Nyquist plot stability test?



(a)



(b)

Figure A1.2: (a) A reflection-type oscillator using feedback representation
(b) Equivalent simple linearized circuit [2.2]

Let us first examine the poles of the closed-loop feedback system. In order to determine the location of these poles, we need to analyze equation (A1.1) in the *s*-plane:

$$T(s) = \frac{G(s)}{1 - G(s)H(s)} = \frac{G(s)}{1 - L(s)} \qquad \textbf{(A1.8)}$$

When the denominator becomes zero, the poles can be found at complex frequencies, *s*:

$$1 - L(s) = 0 \quad \text{or} \quad L(s) = 1 \qquad \textbf{(A1.9)}$$

When equation (A1.9) is solved, it reveals the roots of this characteristic equation for particular *s* values. The mapping of these *s* complex pair values is represented in the *s*-plane, otherwise known as the root-locus diagram. Let us then consider an amplifier with a pole pair at $s = \sigma_o \pm j\omega_o$. In the presence of an electrical disturbance, the output transient response of the amplifier will be of the form:

$$v(t) = e^{\sigma_0 t}\left[e^{+j\omega_n t} + e^{-j\omega_n t}\right] = 2e^{\sigma_0 t}\cos(\omega_n t) \qquad \textbf{(A1.10)}$$

This indicates a sinusoidal signal with an exponential envelope. If the complex poles are in the left-hand-plane, then σ_o is negative and the envelope will be exponentially

decaying, i.e. diminishing oscillations toward zero indicate a stable system. Now, if the complex poles are in the right-hand-plane, then σ_o is positive and the envelope will be exponentially increasing, i.e. growing oscillations toward infinity indicate an unstable system. Finally, if the poles lie directly on the $j\omega$ axis, then σ_o is zero, and oscillations will be sustained [2.3].

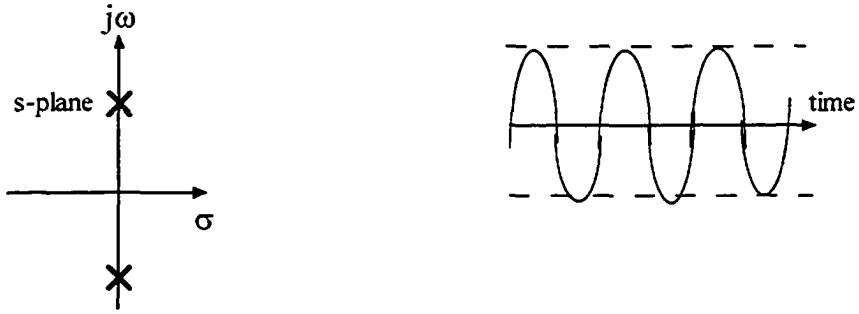


Figure A1.3: Transient response and pole location under steady-state [2.3]

A1.3 – Nyquist Plots and Pole Locations

Determining the pole location of the characteristic equations might not be a trivial procedure for complex circuits. The Nyquist plot is a useful graphical method that allows us to study the location of the poles, based on the root-locus diagram.

The Nyquist plot shown in Figure A1.4 is a polar plot of the loop gain's magnitude and phase versus frequency. It represents the mapping of the right-half plane of the root-locus diagram onto the L(s)-plane. The defining test is to determine whether any value in the RHP of the s-plane satisfies equation (A1.9). This is done by plotting values of $s = 0+j\omega$, for all values of ω, since this represents the boundary between RHP and LHP.

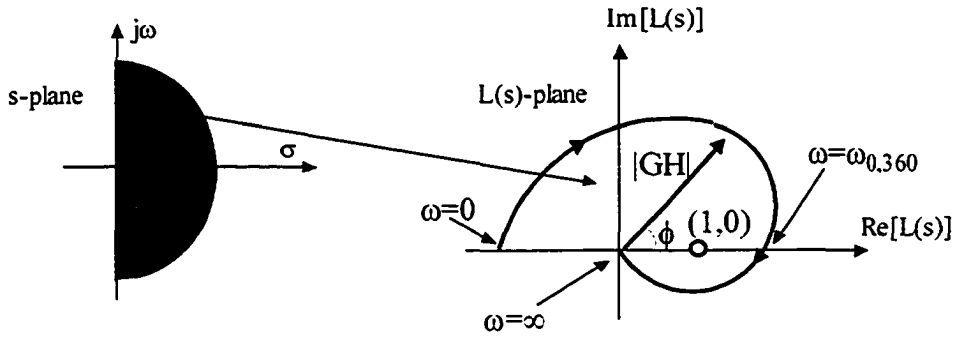


Figure A1.4: Nyquist plot for unstable feedback amplifier

While tracking the contour, we can readily identify the frequency point with magnitude of 1 and phase of 0°: if this critical point (1,j0) is encircled by the Nyquist plot, then it is concluded that there indeed exits a pole that satisfies equation (A1.9) in the RHP, rendering the feedback amplifier unstable. If, however, the intersection occurs to the left of the point (1,j0), then all the poles occur in the LHP, and therefore the amplifier is stable. As a result, it follows that if the Nyquist plot encloses the point (1,j0) in a clockwise manner, then the amplifier is determined to be unstable, and hence the loop gain magnitude is greater than unity. The number of clockwise encirclements of the Nyquist plot indicates the number of complex conjugate pole pairs in the RHP of a root-locus diagram of the closed-loop system [2.4].

Let us now examine the mechanism behind nonlinear amplitude control. We have stated that in order for a feedback system to be unstable and hence produce oscillations, the initial pair of complex poles must be in the RHP. This is usually accomplished via the active device's DC bias point as well as the surrounding circuit elements, where we are then guaranteed an initial sinusoidal signal that continuously grows in amplitude. As

mentioned above, amplitude keeps increasing in the feedback system until the active device reaches saturation levels. Here, the active device operates in a nonlinear mode under large signal condition, reducing the gain to unity, and thus curbing signal amplification. This is the steady-state ceiling amplitude for a particular device's bias point, represented from a root-locus diagram point of view, in Figure A1.5:

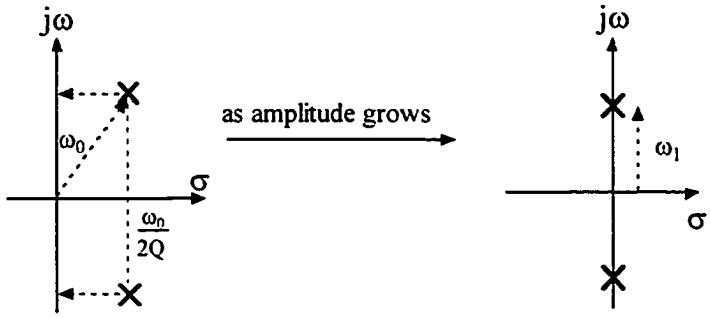


Figure A1.5: Pole location at (a) small-signal (b) large-signal

As the amplitude steadily increases, the poles have been pulled back onto the $j\omega$-axis, indicating unity gain and sustained oscillations under large-signal device operation.

The feedback mechanism of the oscillator circuit also allows for the detection of changes in the loop gain. Thus, if the loop gain happens to drop below unity at any time, the amplitude of the sinusoidal signal inherently gets reduced. This effect will be felt by the nonlinear active device, which will, in its turn, increase the amplitude to reach unity gain once again. This point is presented in [2.5], where Lindberg argues that it is nearly an impossible act of balance to maintain poles on the $j\omega$-axis ($s = \pm j\omega_o$) for sustained oscillations. Lindberg provides insight into the mechanisms behind oscillator behavior by means of *the "frozen eigenvalues approach"*, where steady-state oscillations are

described by complex pole pairs moving between the RHP and the LHP, instead of being simply on the $j\omega$-axis. By piece-wise linear modeling of the amplifier gain, i.e. large gain for small signals and small gain for large signals, it can be shown that when the system is in start-up mode (small-signal), the poles are in the RHP with large gain and increasing amplitudes, while in transient mode (large-signal) the poles are in the LHP with small gain and decreasing amplitudes. Steady-state is the movement of the poles between the RHP and the LHP so that a balance is achieved between the energy obtained from the power supply when the poles are in the RHP and the energy lost in the system when the poles are in the LHP. Note that in Figure A1.5, $\omega_o \neq \omega_1$ due to power dependency of the active device operating in large-signal, which has been temporarily omitted to simplify analysis. This mechanism is one of the most popular automatic gain control (AGC) mechanisms utilized in oscillator circuit design.

Appendix A2 – 2-Port Negative Resistance Model

In order to achieve the negative resistance component, a transistor is used as an active device, with the 2-port S-parameters defined at microwave frequencies.

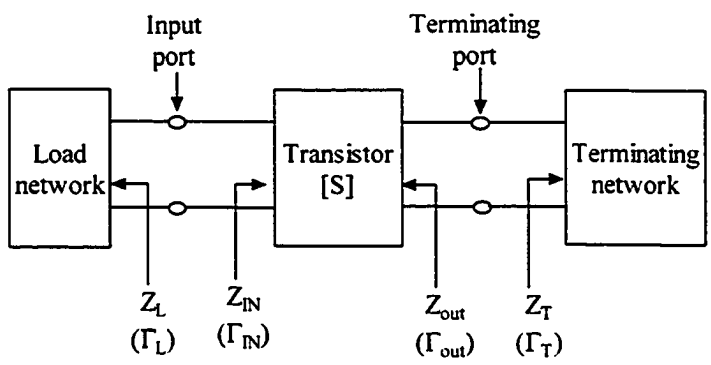


Figure A2.1: 2-port oscillator model [2.8]

In order to determine the oscillation conditions, it is imperative to separate the load network plane from the terminating network plane through the transistor plane. Figure A2.1 shows a two-port network configured as an oscillator. Z_T represents the terminating network and Z_L represents the load network, while the transistor is characterized by its S-parameters. Although the terminating and load networks are shown as in the Figure A2.1, they could also be interchanged for one another while maintaining the same oscillation conditions. Thus, by choosing a proper terminating network, the active device is made unstable at a specific frequency of oscillation. The load network on the other port is then designed in a manner described in the above section, according to (2.15). We will begin our analysis by showing that if one port satisfies the oscillation condition of (2.22), then the other port will also automatically satisfy that condition, and hence both ports are made to oscillate.

The input port is oscillating when:

$$\Gamma_{IN}\Gamma_L = 1 \tag{A2.1}$$

For a 2-port network, the input reflection coefficient is given as [2.8]:

$$\Gamma_{IN} = S_{11} + \frac{S_{12}S_{21}\Gamma_T}{1 - S_{22}\Gamma_T} \tag{A2.2}$$

and from (2.22), we now have:

$$\Gamma_L = \frac{1}{\Gamma_{IN}} = \frac{1 - S_{22}\Gamma_T}{S_{11} - \Delta\Gamma_T} \quad \textit{where} \quad \Delta = S_{11}S_{22} - S_{12}S_{21} \tag{A2.3}$$

or solving for Γ_T:

$$\Gamma_T = \frac{1 - S_{11}\Gamma_L}{S_{22} - \Delta\Gamma_L} \tag{A2.4}$$

Also, for a 2-port network, the output reflection coefficient is given as [2.8]:

$$\Gamma_{OUT} = S_{22} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} = \frac{S_{22} - \Delta\Gamma_L}{1\text{-}S_{11}\Gamma_L} \tag{A2.5}$$

Comparing (A2.5) with (A2.4), we can say that:

$$\Gamma_{OUT} = \frac{1}{\Gamma_T} \quad or \quad \Gamma_{OUT}\Gamma_T = 1 \tag{A2.6}$$

indicating that the terminating port is also oscillating.

Appendix A3 – Leeson's Phase Noise Model Explained

The spectral density of phase fluctuations, due to phase modulation of the carrier signal, is represented by the following:

$$S_{\Delta\theta}(f_m) = \Delta\theta^2_{rms} \tag{A3.1}$$

$$where \quad \Delta\theta_{rms} = \frac{1}{\sqrt{2}}\Delta\theta_{peak} = 2\frac{P_{SSB}}{P_S}$$

As well, from (2.29), we have $L(f_m) = \frac{1}{2}\Delta\theta^2_{rms}$ or $L(f_m) = \frac{1}{2}S_{\Delta\theta}(f_m)$. Thus, the power spectral density will be determined in order to obtain an expression for phase noise.

The main active device in an oscillator is an amplifier with feedback. The amplifier, with a noise figure F, will contribute to the phase noise of the oscillator through additive noise. Let us assume that the white noise added to a signal is nothing more than the sum

of contiguous 1-Hz bands. Each of these bands has an available noise power *FkT*. In order to represent these bands with a discrete signal, a noise voltage will be allocated:

$$V_{n,rms} = \sqrt{FkT \over R} \tag{A3.2}$$

Thus, as a result of (A3.2), the phase perturbations on the carrier signal can be represented by the following phasor diagram:

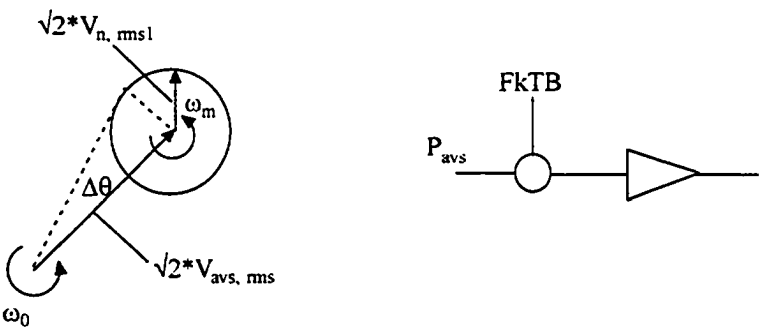


Figure A3.1: Phasor diagram for phase noise effect on carrier signal

Thus, the peak and RMS phase disturbance will occur when an orthogonal intersection occurs between the modulation and the signal component in Figure A3.1, i.e.:

$$\Delta\theta_{peak} = \frac{V_{n,rms1}}{V_{avs,rms}} = \frac{\sqrt{\frac{FkT}{R}}}{\sqrt{\frac{P_{avs}}{R}}} = \sqrt{\frac{FkT}{P_{avs}}} \tag{A3.3}$$

$$\Delta\theta_{rms1} = \frac{1}{\sqrt{2}}\Delta\theta_{peak} \tag{A3.4}$$

Where $\Delta\theta_{rms1}$ represents only a single sideband f_m Hz away from the carrier. Hence, the total phase disturbance is given by:

$$\Delta\theta_{rms,total} = \sqrt{2*\left(\frac{1}{\sqrt{2}}\Delta\theta_{peak}\right)^2} = \sqrt{\frac{FkT}{P_{avs}}} \tag{A3.5}$$

Finally, the spectral density, along with the phase noise are given by:

$$S_{\Delta\theta}(f_m) = \Delta\theta^2_{rms,total} = \frac{FkT}{P_{avs}} \tag{A3.6}$$

$$L(f_m) = \frac{1}{2}\frac{FkT}{P_{avs}} \quad for f_m > f_o \tag{A3.7}$$

When the modulating frequency, f_m, is close to the carrier signal, the phase noise experiences flicker noise, or *1/f* noise, which is a by-product of the amplifier's corner frequency, f_c. The corner frequency is device dependent, and it is caused by low-frequency devices noise modulating the input signal's phase. At frequencies below f_c, the noise spectral density decreases with slope f_m. Therefore, the total phase noise of the amplifier can be modeled as a phase modulator along with a noise-free amplifier:

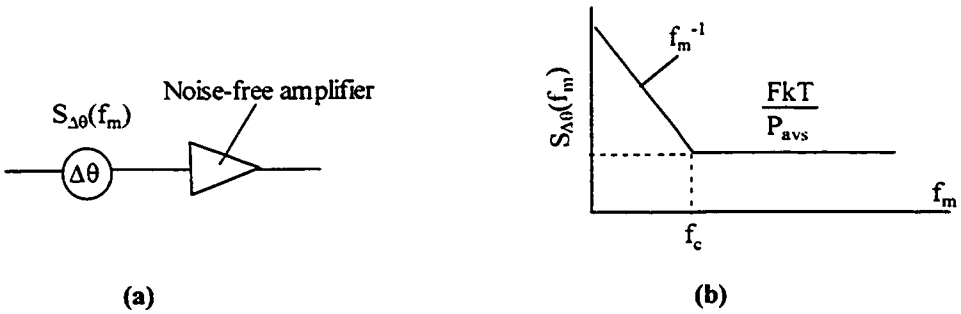


Figure A3.2: (a) Phase noise circuit representation (b) Flicker noise effect on phase noise

Thus, the additional corner frequency adds to the spectral phase noise of (A3.6) :

$$S_{\Delta\theta}(f_m) = \frac{FkT}{P_{avs}}\left(1 + \frac{f_c}{f_m}\right) \tag{A3.8}$$

Looking at phase noise from the complete oscillator's point of view, we have an amplifier along with a resonator in a feedback configuration:

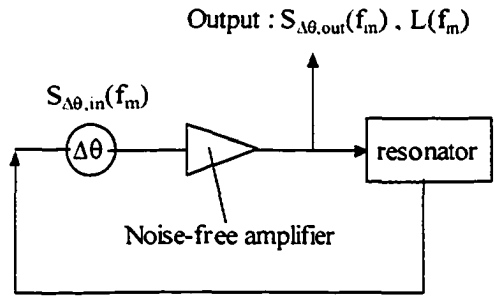


Figure A3.3: Phase noise within an oscillator

The bandpass resonator in the circuit affects the contribution of the input phase noise. Examining the equivalent low-pass function of the bandpass resonator, we have:

$$H_{resonator}(\omega_m) = \frac{1}{1 + j*\left(2Q_L \frac{\omega_m}{\omega_o}\right)} \tag{A3.9}$$

Where $\omega_o/2Q_L$ is the resonator's half-bandwidth. Due to the input phase modulation, the phase loop response is given by:

$$\begin{aligned} \Delta\theta_{out}(f_m) &= H_{resonator} * \Delta\theta_{in}(f_m) \\ &= \frac{1}{1 + j*\left(2Q_L \frac{\omega_m}{\omega_o}\right)} * \Delta\theta_{in}(f_m) \end{aligned} \tag{A3.10}$$

From (A3.1) and (A3.10), the output spectral density and phase noise functions are given as:

$$S_{\Delta\theta,out}(f_m) = \left[1 + \frac{1}{f_m^2}\left(\frac{f_o}{2Q_L}\right)^2\right] S_{\Delta\theta,in}(f_m) \tag{A3.11}$$

$$L(f_m) = \frac{1}{2}\left[1 + \frac{1}{f_m^2}\left(\frac{f_o}{2Q_L}\right)^2\right] S_{\Delta\theta,in}(f_m) \tag{A3.12}$$

where $S_{\Delta\theta.in}$ represents the amplifier's noise contribution of (A3.8).

The above equation illustrates the behavior of the input phase noise at the output of the amplifier. The appearance of the bandpass resonator's half-bandwidth, $\omega_o/2Q_L$, in (A3.12) implies that the perturbation is enhanced by the positive phase feedback.

Appendix B : pHEMT Transistor Data Sheet (Agilent)

Agilent Technologies

Low Noise Pseudomorphic HEMT in a Surface Mount Plastic Package

Technical Data

ATF-35143

Features

- **Lead-free Option Available**
- **Low Noise Figure**
- **Excellent Uniformity in Product Specifications**
- **Low Cost Surface Mount Small Plastic Package SOT-343 (4 lead SC-70)**
- **Tape-and-Reel Packaging Option Available**

Specifications

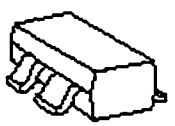
1.9 GHz; 2V, 15 mA (Typ.)

- **0.4 dB Noise Figure**
- **18 dB Associated Gain**
- **11 dBm Output Power at 1 dB Gain Compression**
- **21 dBm Output 3rd Order Intercept**

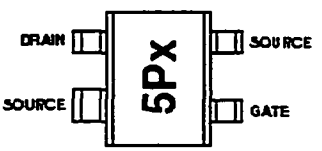
Applications

- **Low Noise Amplifier for Cellular/PCS Handsets**
- **LNA for WLAN, WLL/RLL, LEO, and MMDS Applications**
- **General Purpose Discrete PHEMT for Other Ultra Low Noise Applications**

Surface Mount Package SOT-343



Pin Connections and Package Marking



Note: Top View. Package marking provides orientation and identification.
"5P" = Device code
"x" = Date code character. A new character is assigned for each month, year.

Description

Agilent's ATF-35143 is a high dynamic range, low noise, PHEMT housed in a 4-lead SC-70 (SOT-343) surface mount plastic package.

Based on its featured performance, ATF-35143 is suitable for applications in cellular and PCS base stations, LEO systems, MMDS, and other systems requiring super low noise figure with good intercept in the 450 MHz to 10 GHz frequency range.

Other PHEMT devices in this family are the ATF-34143 and the ATF-33143. The typical specifications for these devices at 2 GHz are shown in the table below:

Part No.	Gate Width	Bias Point	NF (dB)	Ga (dB)	OIP3 (dBm)
ATF-33143	1600 µ	1V, 80 mA	0.5	15.0	33.5
ATF-34143	800µ	1V, 60 mA	0.5	17.5	31.5
ATF-35143	400µ	2V, 15 mA	0.4	18.0	21.0

Attention:
Observe precautions for handling electrostatic sensitive devices.

ESD Machine Model (Class A)

ESD Human Body Model (Class 1)

Refer to Agilent Application Note A004R: Electrostatic Discharge Damage and Control

ATF-35143 Electrical Specifications

T_A = 25°C, RF parameters measured in a test circuit for a typical device

Symbol	Parameters and Test Conditions			Units	Min.	Typ.[3]	Max.
I_{dss}[1]	Saturated Drain Current		V_{DS} = 1.5 V, V_{GS} = 0 V	mA	40	65	80
V_P[1]	Pinchoff Voltage		V_{DS} = 1.5 V, I_{DS} = 10% of I_{dss}	V	-0.65	-0.5	-0.35
I_d	Quiescent Bias Current		V_{GS} = 0.45 V, V_{DS} = 2 V	mA	—	15	—
g_m[1]	Transconductance		V_{DS} = 1.5 V, $g_m = I_{dss}/V_P$	mmho	90	120	—
I_{GDO}	Gate to Drain Leakage Current		V_{GD} = 5 V	µA			250
I_{gss}	Gate Leakage Current		$V_{GD} = V_{GS}$ = -4 V	µA	—	10	150
NF	Noise Figure[3]	f = 2 GHz	V_{DS} = 2 V, I_{DS} = 15 mA	dB		0.4	0.7
			V_{DS} = 2 V, I_{DS} = 5 mA			0.5	0.9
		f = 900 MHz	V_{DS} = 2 V, I_{DS} = 15 mA	dB		0.3	
			V_{DS} = 2 V, I_{DS} = 5 mA			0.4	
G_a	Associated Gain[3]	f = 2 GHz	V_{DS} = 2 V, I_{DS} = 15 mA	dB	16.5	18	19.5
			V_{DS} = 2 V, I_{DS} = 5 mA		14	16	18
		f = 900 MHz	V_{DS} = 2 V, I_{DS} = 15 mA	dB		20	
			V_{DS} = 2 V, I_{DS} = 5 mA			18	
OIP3	Output 3rd Order Intercept Point[4, 5]	f = 2 GHz	V_{DS} = 2 V, I_{DS} = 15 mA	dBm	19	21	
			V_{DS} = 2 V, I_{DS} = 5 mA			14	
		f = 900 MHz	V_{DS} = 2 V, I_{DS} = 15 mA	dBm		19	
			V_{DS} = 2 V, I_{DS} = 5 mA			14	
P_{1dB}	1 dB Compressed Intercept Point[4]	f = 2 GHz	V_{DS} = 2 V, I_{DSQ} = 15 mA	dBm		10	
			V_{DS} = 2 V, I_{DSQ} = 5 mA			8	
		f = 900 MHz	V_{DS} = 2 V, I_{DSQ} = 15 mA	dBm		9	
			V_{DS} = 2 V, I_{DSQ} = 5 mA			9	

Notes:

1. Guaranteed at wafer probe level
2. Typical value determined from a sample size of 450 parts from 9 wafers.
3. 2 V 5 mA min/max data guaranteed via the 2 V 15 mA production test.
4. Measurements obtained using production test board described in Figure 5.
5. P_{out} = -10 dBm per tone

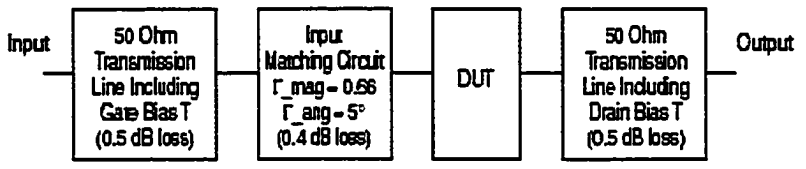


Figure 5. Block diagram of 2 GHz production test board used for Noise Figure, Associated Gain, P_{1dB}, and OIP3 measurements. This circuit represents a trade-off between an optimal noise match and a realizable match based on production test requirements. Circuit losses have been de-embedded from actual measurements.

ATF-35143 Absolute Maximum Ratings[1]

Symbol	Parameter	Units	Absolute Maximum
V_{DS}	Drain - Source Voltage[2]	V	5.5
V_{GS}	Gate - Source Voltage[2]	V	-5
V_{GD}	Gate Drain Voltage[2]	V	-5
I_{DS}	Drain Current[2]	mA	I_{dss}[3]
P_{diss}	Total Power Dissipation[4]	mW	300
$P_{in\ max}$	RF Input Power	dBm	14
T_{CH}	Channel Temperature	°C	160
T_{STG}	Storage Temperature	°C	-65 to 160
θ_{jc}	Thermal Resistance[5]	°C/W	310

Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. Assumes DC quiescent conditions.
3. V_{DS} = 0 V
4. Source lead temperature is 25°C. Derate 3.2 mW/°C for T_L > 67°C.
5. Thermal resistance measured using 150°C Liquid Crystal Measurement method.

Product Consistency Distribution Charts[7,8]

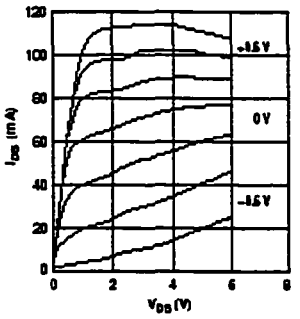


Figure 1. Typical Pulsed I-V Curves[6]. (V_{GS} = 0.27 V per step)

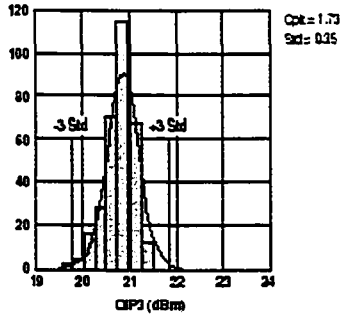


Figure 2. OIP3 @ 2 GHz, 2 V, 15 mA. LSL=19.0, Nominal=20.9, USL=22.0

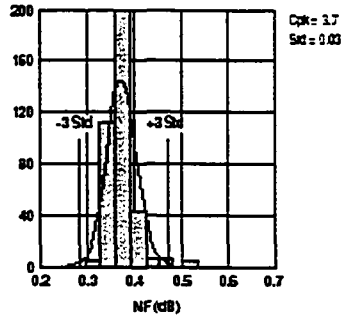


Figure 3. NF @ 2 GHz, 2 V, 15 mA. LSL=0.2, Nominal=0.27, USL=0.7

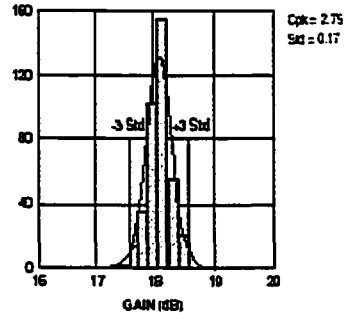


Figure 4. Gain @ 2 GHz, 2 V, 15 mA. LSL= 16.5, Nominal=18.0, USL=19.5

Notes:
6. Under large signal conditions, V_{GS} may swing positive and the drain current may exceed I_{dss}. These conditions are acceptable as long as the maximum P_{diss} and $P_{in\ max}$ ratings are not exceeded.
7. Distribution data sample size is 420 samples taken from 9 different wafers. Future wafers allocated to this product may have nominal values anywhere within the upper and lower spec limits.
8. Measurements made on production test board. This circuit represents a trade-off between an optimal noise match and a realizable match based on production test requirements. Circuit losses have been de-embedded from actual measurements.

ATF-35143 Typical Performance Curves, continued

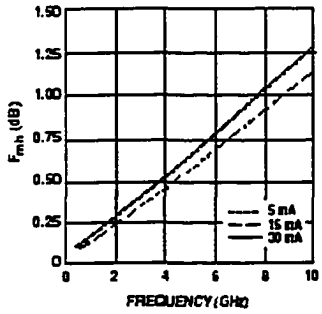


Figure 12. F_{min} vs. Frequency and Current at 2V.

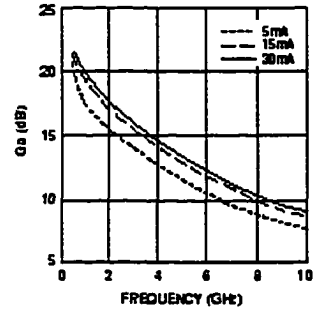


Figure 13. Associated Gain vs. Frequency and Current at 2V.

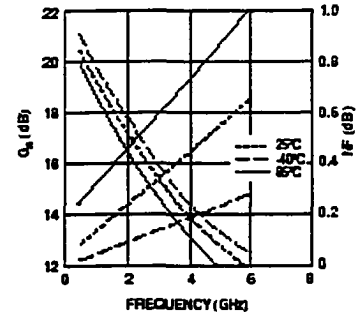


Figure 14. F_{min} and G_a vs. Frequency and Temperature, V_{DS}=2V, I_{DS}=15 mA.

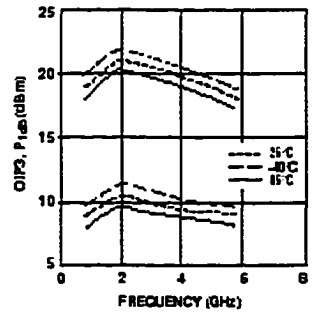


Figure 15. OIP3 and P_{1dB} vs. Frequency and Temperature[1,2], V_{DS}=2V, I_{DS}=15 mA.

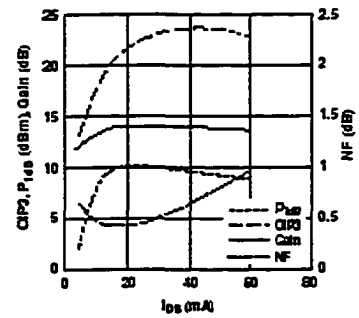


Figure 16. OIP3, P_{1dB}, NF and Gain vs. Bias[1] (Active Bias, 2V, 2.9 GHz).

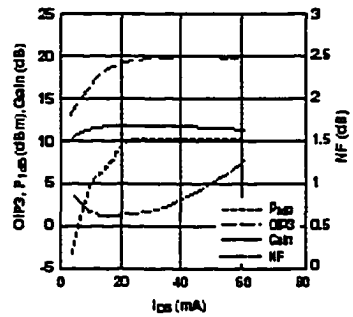


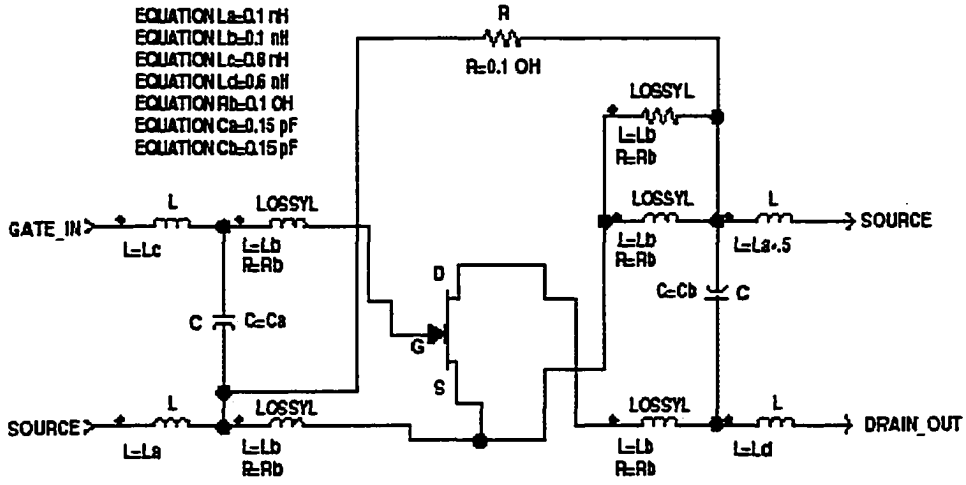
Figure 17. OIP3, P_{1dB}, NF and Gain vs. Bias[1] (Active Bias, 2V, 5.8 GHz).

Notes:

1. Measurements made on a fixed tuned test fixture that was tuned for noise figure at 2V 15mA bias. This circuit represents a trade-off between optimal noise match, maximum gain match and a realizable match based on production test requirements. Circuit losses have been de-embedded from actual measurements.
2. P_{1dB} measurements are performed with passive biasing. Quiescent drain current, I_{DSQ}, is set with zero RF drive applied. As P_{1dB} is approached, the drain current may increase or decrease depending on frequency and dc bias point. At lower values of I_{dsq} the device is running closer to class B as power output approaches P_{1dB}. This results in higher P_{1dB} and higher PAE (power added efficiency) when compared to a device that is driven by a constant current source as is typically done with active biasing. As an example, at a V_{DS} = 4V and I_{DSQ} = 5 mA, I_d increases to 30 mA as a P_{1dB} of +25 dBm is approached.

ATF-35143 SC-70 4 Lead, High Frequency Model

Optimized for 0.1 – 6.0 GHz



This model can be used as a design tool. It has been tested on MDS for various specifications. However, for more precise and accurate design, please refer to the measured data in this data sheet. For future improvements Agilent reserves the right to change these models without prior notice.

ATF-35143 Die Model

```
* STATZ MESFET MODEL *
MODEL = FET
IDS model          Gate model      Parasitics      Breakdown       Noise
NFET=yes           DELTA=.2        RG=1            GSFWD=1         FNC=81e+6
PFET=              GSCAP=3         RD=Rd           GSREV=0         R=.17
IDSMOD=3           CGS=cgs pF      RS=Rs           GDFWD=1         P=.65
VTO=-0.95          GDCAP=3         LG=Lg nH        GDREV=0         C=.2
BETA=Beta          GCD=Cgd pF      LD=Ld nH        VJR=1
LAMBDA=0.09                        LS=Ls nH        IS=1 nA
ALPHA=4.0                          CDS=Cds pF      IR=1 nA
B=0.3                              CRF=.1          MAX=.1
TNOM=27                            RC=Rc           XTI=
IDSTC=                                             N=
VBI=.7                                             EG=
```

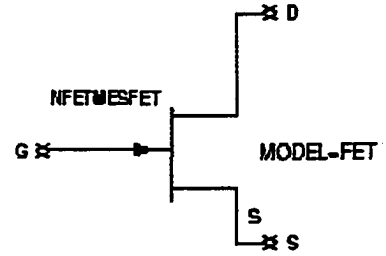
Model scal factors (W=FET width in microns)

```
EQUATION Cds=0.01*W/200
EQUATION Beta=0.06*W/200
EQUATION Rd=200/W

EQUATION Rs=.5*200/W
EQUATION Cgs=0.2*W/200

EQUATION Cgd=0.04*W/200
EQUATION Lg=0.03*200/W

EQUATION Ld=0.03*200/W
EQUATION Ls=0.01*200/W
EQUATION Rc=500*200/W
```



W=400 µm

Appendix C : DLI Broadband Capacitors C06/C08

C06/C08
BROADBAND DC BLOCKS

Low loss resonance free performance

Performance