Jitter Transfer and Jitter Tolerance Analysis of Bang-Bang Clock and Data Recovery Circuits

By

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Abstract

The clock and data recovery (CDR) circuit is a key enabling block in modern high speed serial communication systems with applications covering a wide range from wireline long-haul networks to chip-to-chip and backplane communications. Most high-speed CDR circuits employ bang-bang phase detectors for their simple structure and high speed of operation, unlike linear phase detectors. The bang-bang phase detector has two outputs indicating the sign of the phase detector. The two outputs cause the behaviour of the loop to be nonlinear resulting in a difficult analysis.

As the bang-bang CDR circuit became the most popular choice for designers, there was a need for accurate modeling of the loop relating jitter characteristics to design parameters. While there are many methods presented recently for analyzing bang-bang CDR circuits, in our analysis we will focus on two major methods and use them throughout the thesis. Jitter transfer, as one of the figure of merits of a CDR, is defined and analyzed, followed by the derivation of a more accurate expression that complies with the definition. A second figure of merit, jitter tolerance, is investigated in considerable depth using mathematical tools to simplify the analysis. A simpler expression for jitter tolerance is proposed and compared with existing expressions by means of behavioural simulations. Novel analysis explains the behaviour of the loop in different regions of the jitter tolerance curve.

Intellectual Property

The information used in this thesis comes in part from the research program of Dr. Tad A. Kwasniewski. The research results appearing in this thesis represent an integral part of the ongoing research program. All research results in this thesis including tables, graphs, and figures but excluding the narrative portions of the thesis are effectively incorporated into the research program and can be used by Dr. Kwasniewski for educational and research purposes, including publication in open literature with the appropriate credits. Matters of intellectual property may be pursued cooperatively with Carleton University and Dr. Kwasniewski where and as applicable.

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I am heartily thankful to my supervisor, Prof. Tad Kwasniewski, whose encouragement, guidance and support from the initial to the final level enabled me to develop an understanding of the subject. I will always be grateful for the time I spent working with him.

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Last but not least, I would like express my gratitude to my wife for her love, moral support and patience during my studies. This would not be possible without her understanding and help in managing a good balance between the family and school.

I dedicate this thesis to my mother and father.

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List of Abbreviations

BB	Bang-bang
BER	Bit Error Rate
BPF	Band-pass filter
CDR	Clock and Data Recovery
CP	Charge pump
DCD	Duty cycle distortion
DDJ	Data dependant jitter
DFF	D Flip-flop
DJ	Deterministic jitter
DLL	Delay locked loop
DM	Delta modulator
DPLL	Digital phase locked loop
DUT	Device under test
FOM	Figure of merit
IL	Injection locking
ISI	Inter symbol interference
LF	Loop filter
LFSR	Linear feedback shift register

NRZ	Non-return-to-zero
PD	Phase detector
PI	Phase interpolator
PJ	Periodic Jitter
PLL	Phase locked loop
PRBS	Pseudo-random bit sequence
PWD	Pulse width distortion
RJ	Random jitter
RMS	Root-mean-square
RZ	Return-to-zero
SDM	Sigma-delta modulator
SJ	Sinusoidal jitter
SONET	Synchronous optical network
UI	Unit interval
VCO	Voltage controlled oscillator

List of Symbols

A_{in}	Input jitter amplitude
A_{out}	Output jitter amplitude
C	Loop filter capacitance
I	Charge pump current
JG	Jitter generation function
$Jtol$	Jitter tolerance function
$Jtol_1$	Lee et al.'s Jitter tolerance function for region I
$Jtol_2$	Lee et al.'s Jitter tolerance function for region II
$Jtol_W$	Walker's Jitter tolerance function
$Jtrans$	Jitter transfer function
K_v	VCO gain in rad/sec/volt
r	Data rate
R	Loop filter resistance
t_{delay}	Delay in a PLL loop
T_J	Input jitter period
t_n	Sampling period
α	Integration path gain
β	Proportional path gain in Volts

δ	Arbitrary Phase Offset
ΔV_{bb}	Proportional path control voltage
ΔV_{in}	VCO control voltage
ΔV_{int}	Integral path control voltage
$\Delta\theta$	Proportional path phase step
$\Delta\theta_{integral}$	Integral path phase step
$\Delta\theta_{max}$	Maximum phase error
$\Delta\theta_{proportional}$	Proportional path phase step
$\delta\omega$	Input jitter frequency variation component
$\Delta\omega$	Integral path frequency step
ε	±1
ζ	Stability factor
$\theta'_{in}(t)$	Slope of the input phase signal
$\theta'_{out}(t)$	Slope of the output phase signal
θ_{bb}	Bang-bang phase step
θ_{err}	Phase error
θ_{in}	Input phase
θ_{out}	Output phase
$\Phi(t)$	Input jitter phase variation component
ω_{-3dB}	Jitter transfer -3dB bandwidth
ω_{bb}	Bang-bang radian frequency step
ω_C	VCO center frequency

ω_{in}	Input data frequency
ω_J	Input jitter radian frequency
ω_L	Lee et al.'s corner frequency for jitter transfer
ω_o	Output frequency
ω_{VCO}	VCO frequency
ω_W	Walker's corner frequency for jitter transfer

Chapter 1: Introduction

The continued increase in the speed of the internet has created a pressing need for high-speed communication systems. Serial communication is well suited for long distances, because fewer wires are used as compared to parallel communication. Serial communication systems require clock generation, multiplexing, clock recovery, demultiplexing and loss of signal detection. A clock and data recovery circuit (CDR) is an essential block used as part of the receiver of high-speed serial communication system and synchronous optical network (SONET). With the increasing interest in multi-gigabit per second links, CDR circuits have to meet strict jitter and stability requirements.

CDR circuits can be categorized into two groups according to their phase detector type: the linear CDR and the binary (bang-bang) CDR. While linear phase detector-based CDR circuits have proven to be suitable for meeting system requirements, the performance of this group of phase detectors descends as the data rates reach the speed limits of existing technology. More specifically, the linear phase detector produces narrow pulses proportional to the phase error between the incoming data and the clock. These narrow pulses require technology process speed much higher than the sampling frequency.

Bang-bang phase detector-based CDR circuits are becoming the common design choice for state-of-the CDR designs for three reasons. First, they are very simple in structure and can operate at much higher speeds than their linear counterparts. Secondly, they experience no static phase error due to the inherent sampling phase alignment. Finally, they adapt to multi-phase sampling structures, which allows for operation at frequencies at a fraction of the data rate. As a result of these advantages of the bang-bang CDRs, there is a marked increase in designs employing them. A survey of CDR designs at the *International Solid State Circuits Conference* showed that as the design data rate approach the speed limitation of the technology, it is more likely to implement a bang-bang CDR [1].

Despite its increasing popularity, the bang-bang CDR's nonlinear behaviour makes it difficult to analyze. Lack of complete analysis of the bang-bang CDR circuit adds complexity to the design. More simulations and prototypes are required in order to meet required specifications. As a result more resources and time are wasted. Some effort has been made in the last decade to develop models to characterize the CDR's nonlinear behaviour more accurately. Different models were introduced and the analysis methodologies are quite different resulting in a need to compare and validate the different models.

In this work we provide a more detailed analysis on second order bang-bang CDR circuits. We will present a detailed analysis of jitter transfer and jitter tolerance using existing models. In the case of jitter transfer analysis, a more accurate expression is derived and verified by behavioural simulation. The proposed expression complies with

the definition. As for the jitter tolerance analysis, simulation test benches are developed and used to verify the validity of existing models. A simplified expression for jitter tolerance is proposed based on method 1. Limitations of existing models in different regions of the jitter tolerance curve are explained and illustrated by simulation results.

Background information on linear and bang-bang CDR circuits from both the architectural and circuit level is presented in chapter 2. Next, figure of merits (FOM) used to measure the performance of CDR circuits are presented. Finally, different models for bang-bang CDR circuits are illustrated and expressions are derived. Analysis for jitter transfer based on the two major methods is introduced in chapter 3 where a more accurate expression for jitter transfer is derived and verified by behavioural simulation. Chapter 4 introduces the jitter tolerance analysis for a second order bang-bang CDR circuit in which time-domain and phase-domain test benches are developed and used to explain the loop dynamics in different regions of the jitter tolerance curve. Finally, chapter 5 summarizes the thesis, clarifies the major contributions and points to potential future work.

Chapter 2: Overview of Clock and Data Recovery Architectures

2.1 Introduction

The CDR circuit is a key element in high-speed serial links and as a result there have been a tremendous research going on designing different architectures of CDR circuits to enhance speed, accuracy, chip area, power and jitter characteristics. In this chapter, a background on CDR architectures and their main operation principles are reviewed. CDR architectures can be classified into three main categories, according to the relationship between the input phase signal and the output. In order to compare between CDR circuits, there are FOMs to characterize the performance of different CDR circuits, such as jitter tolerance, jitter transfer and jitter generation. After presenting a review on the jitter characteristics, different methods for modeling and analyzing the bang-bang CDR circuit are investigated. Two main methods for modeling and analyzing the bang-bang CDR circuit are discussed in more details with an overview on previous work done.

2.2 Data modulation

In communication systems, transmitted data is usually modulated or encoded in order to make it easier to receive the data, or in order to enable error correction. While modulation is more commonly associated with wireless data communication, it is merely

a description of data in the electrical domain. Modulation, in the context of wireline data communication, is also known as line coding. While there are several different line codes, we will only discuss two examples, non-return-to-zero (NRZ) and return-to-zero (RZ) as shown in figure 2.1.

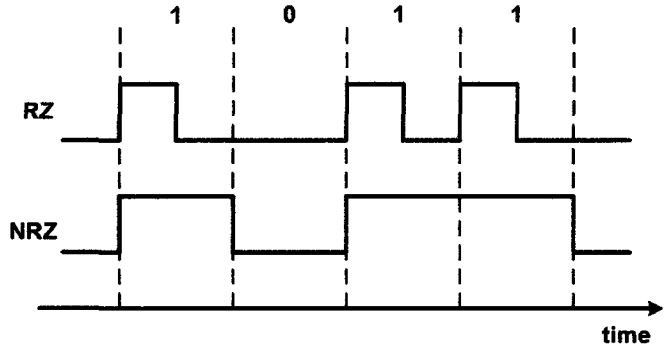


Figure 2.1 Time-domain representation of unipolar RZ and NRZ line codes

NRZ line code is the most frequently used line code in wireline data transmission. In a NRZ line code, there are two possible values for the input signal, '1' and '0', which correspond to the value of the input data bit for the full bit period (T). For example, for a 10Gb/s data stream, the highest frequency content will occur for a data of 101010. However, this data stream is equivalent to a 5GHz clock. While this is an advantage since the bandwidth requirements are halved, the absence of frequency content at the data rate cause a need for clock recovery, creating a disadvantage for NRZ line code. Another disadvantage is that for a long binary sequence with very few transitions, it will create a constant output, or a DC output. A DC output makes synchronization more difficult and therefore long runs of '0' and '1' need to be controlled.

In RZ line code, the data bit is represented in the first half of the bit period (T). In the second half, the output signal returns to its neutral level (where the neutral level is at zero voltage). Thus, a data bit of '1' is represented by a positive voltage, while a data bit of '0' is represented by a zero voltage, in unipolar RZ or a negative voltage in bipolar RZ. This makes data synchronization much easier as the signal has spectral power at the frequency equal to the data rate. Another benefit of the RZ code is that there are always transitions, indicating that the data signal will never be blocked by high-pass filtering with long runs of '1' or '0'. However, the main drawback of this line code is that it requires twice the bandwidth of NRZ.

Transmitted binary data are often encoded in wireline systems to overcome some issues. One such issue results when the lack of transitions during a long run causes the oscillator to drift and generate jitter. Encoding avoids this issue by limiting the number of consecutive '1's or '0's. For example, 8B/10B coding converts a sequence of 8 bits to 10 bits while guaranteeing a maximum run length of 5 bits. In addition, encoding the data allows the new data signal to maintain DC balance by guaranteeing that there are an equal number of `1's and `0's [2]. The 8B/10B code provides the benefits of guaranteed transitions and DC balance described above and hence is employed in a number of standards. A more efficient version, called 64B/66B coding is also used in other standards to lower the overhead to 3% as opposed to 25% overhead in 8B/10B coding.

2.3 CDR Basics

A random data stream has a unique interpretation only if a time reference is provided for synchronization. In serial data communications, the incoming data is first synchronized

to an internal clock and then retimed in order to remove jitter accumulation. CDR circuit is responsible to recover the clock from the incoming data stream and then use this clock to retime the data, as shown in figure 2.2 [2]. The retimed data, with no errors, is logically the same as the input data stream but with less jitter.

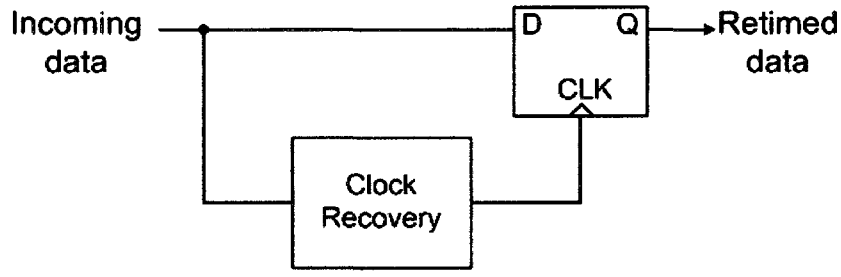


Figure 2.2 Clock and data recovery

We have seen in the last section that the data spectrum for NRZ line code does not contain any energy at the data rate. In order to allow recovery of the clock information contained in the data stream, energy must be created by a nonlinear operation, like edge detection, at the input of the CDR [2]. Edge detection is a combination of differentiation and rectification. Several phase detector circuit topologies for phase-locked loops (PLL) operating on random data streams have been developed. These structures, performing implicit edge detection at the input of the PLL, are discussed in more detail in [2].

There are many different architectures for CDR circuits, including closed-loop CDR architecture and open-loop CDR architecture. The closed-loop architecture is sometimes referred to as phase-locking CDR circuit [3]. In this thesis any reference to a CDR circuit implies the closed-loop architecture. A general architecture of closed-loop, or a PLL based CDR circuit, is given in figure 2.3. The phase detector detects phase errors

between the incoming data signal and the internal clock signal and supplies correction information to the charge pump. The charge pump takes the correction information and adds charge to or subtracts charge from the loop filter. The loop filter plays an important role in defining the frequency response of the system. The voltage on the loop filter controls the VCO, and the output of the VCO is sent to both the phase detector and also to the retiming circuit. More details on CDR circuit architectures are given in the following section.

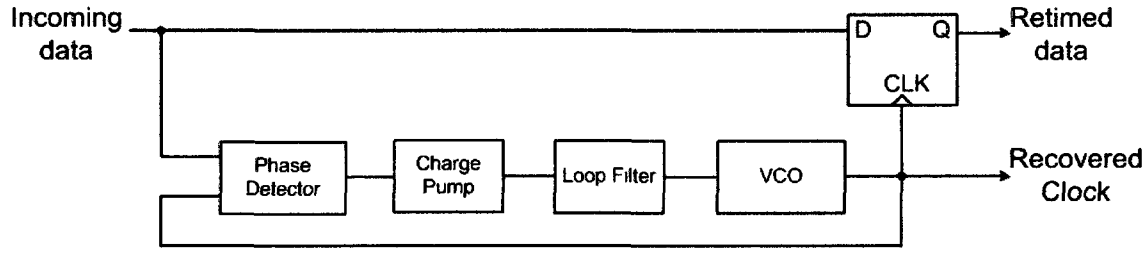


Figure 2.3 PLL based CDR circuit

2.4 CDR Architectures

There is a wide variety of CDR architectures have been proposed for high speed data transmission applications, such as CDR architectures based on analog PLL, digital PLL (DPLL), delay locked loop (DLL), phase interpolator (PI), injection locking (IL), oversampling, gate oscillator, and high-Q bandpass filter [4-11]. CDR architectures can be classified into three main types, the analog, semi-analog, and the all digital CDR architectures. Another classification is according to the phase relationship between the input data and the local clock at the receiver [12]. We can divide them into three categories:

1. Feedback phase tracking architectures such as PLL, DLL, PI, and IL.

2. Oversampling based CDR architecture.
3. Phase alignment without feedback phase tracking architecture such as gated oscillator and high-Q band pass filtering.

In each of the above categories, the CDR architectures can be further divided into subgroups. For more details, the reader is advised to refer to [12].

2.5 Phase detector in CDR circuits

In this section we will classify CDR circuits according to the phase detector type. CDR circuits employ two types of phase detectors, linear phase detectors and binary phase detectors. A linear phase detector (PD) compares the phase of the incoming data with the phase of the clock generated from the VCO. The linear PD generates an output that is proportional to the magnitude of the phase difference, hence the name linear. The linear phase detector characteristic is shown in figure 2.4. On the other hand, the binary phase detector, or bang-bang phase detector, gives the sign of the phase error and discards the magnitude. The binary phase detector characteristic is illustrated in figure 2.5 [13]. In the following sub sections we will review the characteristics of each phase detector in more details.

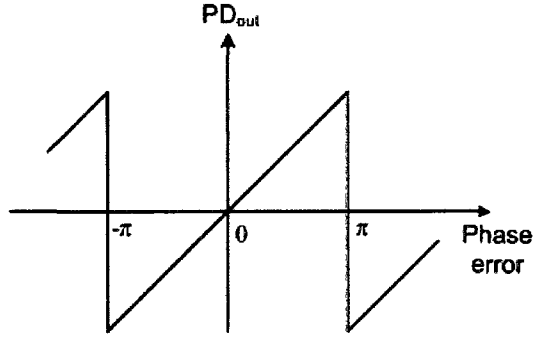


Figure 2.4 Linear phase detector characteristic

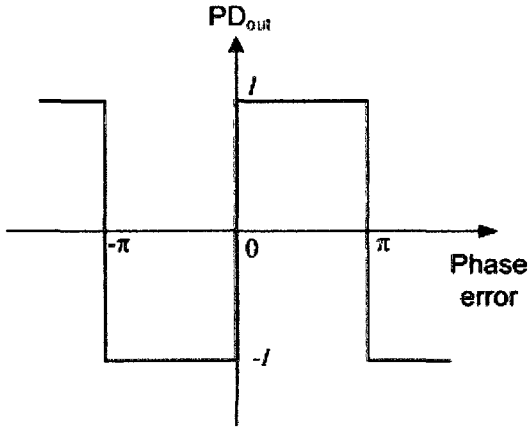


Figure 2.5 Binary phase detector characteristic

2.5.1 Linear phase detector

A linear phase detector is also known as a proportional phase detector, as the width of the output pulses varies linearly with the phase error. The proportional nature of the phase detector gain leads to low activity on the VCO control voltage when the CDR circuit is in the locked condition, which in turn leads to good jitter performance [3]. The linear response of this circuit allows for simple formulation of loop equations, which is very helpful for system analysis.

The Hogge phase detector is a common architecture for linear phase detectors [14]. As shown in figure 2.6, the Hogge phase detector has two outputs. The first output, *X*, is a variable width pulse, which is proportional to the phase difference between the incoming data and the clock. The second output, *Y*, is a reference signal with a pulse width of half the clock pulse. Both outputs are then integrated and compared to generate the phase error signal. Under lock conditions, *X* and *Y* produce equal pulse widths with a phase difference of π radians. A timing diagram for an arbitrary incoming data with all the output signals from the Hogge phase detector is shown in figure 2.7.

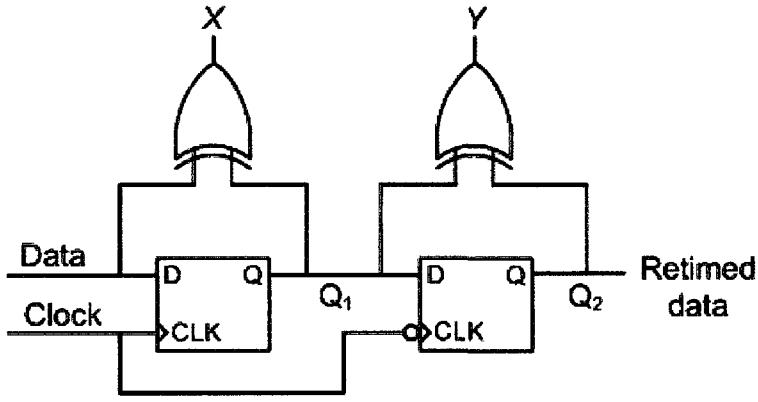


Figure 2.6 Hogge phase detector

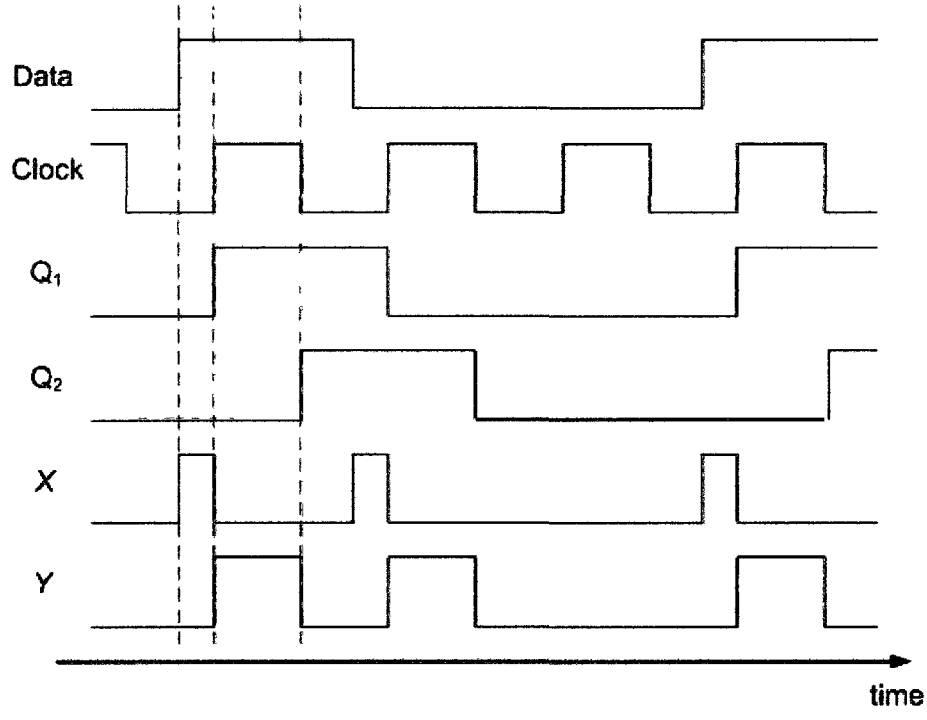


Figure 2.7 Waveforms of a Hogge phase detector

The limitations of Hogge phase detector arises when considering finite delays in the flipflops. Hogge addressed this problem by considering a delay line to compensate for the propagation delay of the flip flop. It is very difficult to implement a delay line with

process, voltage and temperature variations in modern high speed processes. Several papers [15,16] have improved the Hogge phase detector to overcome this limitation. Although they show some performance improvements, they still have limitations in high speed processes.

A common drawback of using linear phase detectors with setup times that are different from retiming flip-flops is that the recovered clock will not be intrinsically aligned in the optimum sampling point in the data eye. Another drawback is that the linear phase detector produces narrow pulses proportional to the phase error. These narrow pulses are very difficult to generate at high data rates. Both the setup/hold times and narrow pulses are the limiting factors to realize high speed CDR using a linear phase detector. Alternative techniques for utilizing a high speed CDR using a linear phase detector are reported in [17-20].

2.5.2 Bang-bang phase detector

The binary phase detector, or bang-bang phase detector, has two output states as shown in figure 2.5. Unlike the linear phase detector, the output of the bang-bang phase detector gives information on the polarity of the phase error rather than the magnitude. The bang-bang phase detector is usually used in many CDR circuit designs due to its ability to work at a much higher speed than the linear phase detector [1]. In our discussion we will present the simplest bang-bang phase detector, D-flipflop (DFF), and the most common binary PD, the Alexander phase detector.

The simplest binary phase detector is a DFF where the incoming data samples the clock generated by the VCO, as illustrated in Figure 2.8 [21]. The output of the phase

detector is used to drive the VCO frequency towards the input data bit rate. A second DFF, usually called decision circuit, is clocked by the VCO frequency and is used to retime the incoming data. While the phase detector circuit is very simple in structure and robust, it has several drawbacks.

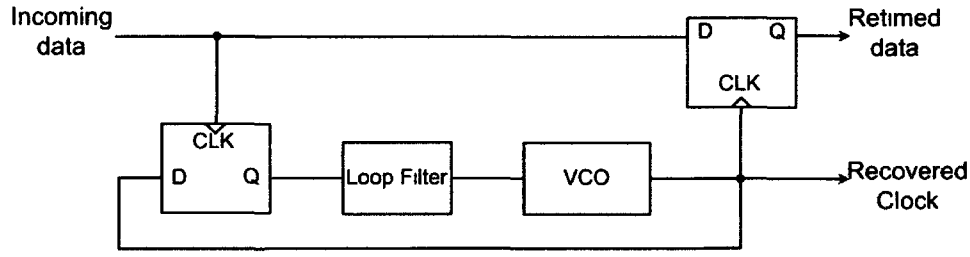


Figure 2.8 A CDR circuit with a DFF as the phase detector

The main problem with the above architecture is it's the lack of integrated retiming, unlike both the Hogge and Alexander phase detectors, which is discussed next, where they have integrated retiming. Integrated retiming means that the phase detector detects the phase error and retimes the data at the same time. In figure 2.8, the decision circuit samples the incoming data by the clock, while the phase detector samples the clock by the incoming data. Since the CLK-to-Q and D-to-Q delays are not equal, there is a substantial phase offset in the retimed data. A second problem with the DFF phase detector is that in the absence of data transitions, it still generates output pulses driving the VCO frequency. The change in the VCO frequency creates jitter at the output. Thus for long runs of '1's or '0's, the CDR circuit continues to lose lock. Many binary phase detectors have a third state during which no information is sent to the charge pump. These phase detectors are known as tri-state or ternary phase detectors. In many data communication systems the data is encoded such that there are a guaranteed minimum

number of transitions, in which case there would be a limited number of repeated `1's or `0's and the absence of a tri-state phase detector would not limit the performance.

The Alexander phase detector is another binary architecture and is commonly used in high speed CDR circuits, as shown in figure 2.9 [22]. As mentioned above, the Alexander phase detector inherits data retiming. The Alexander phase detector uses three samples to detect a data transition and weather the clock is leading or lagging. There are a total of four DFFs that determine the three samples and two XOR gates determine the direction of the phase error. The main difference between the Alexander phase detector and the DFF as a phase detector is the tri-state nature of the Alexander phase detector. In other words, the Alexander phase detector has three output states instead of two. The three output states are: Clock leading, clock lagging, and no transition. The tri-state nature of the Alexander phase detector means that the output is not driving the VCO frequency when there is no transition. This ensures the CDR circuit stays locked in a long strings of '1's or '0's.

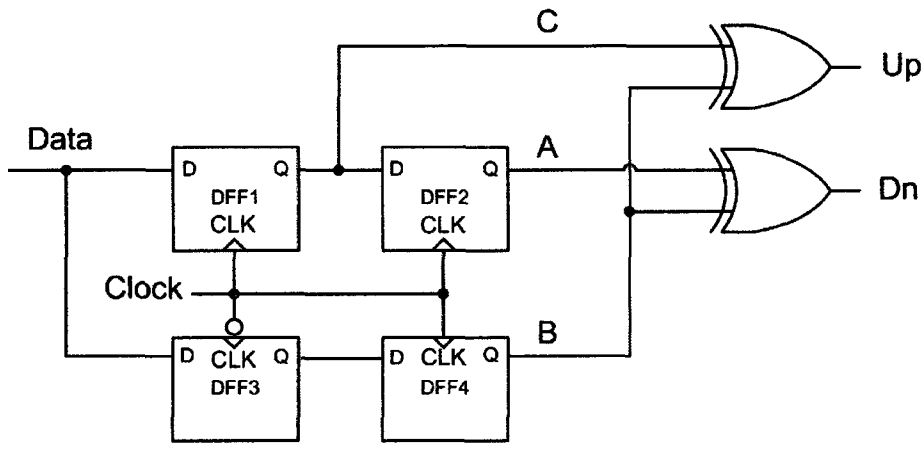


Figure 2.9 Architecture of Alexander Phase detector circuit

Figure 2.10 illustrates the operation of the Alexander phase detector. When the last sample, *C*, is different from the first two samples, *A* and *B*, then the clock is lagging "late", as shown in figure 2.10 (a). On the other hand, when the first sample, *A*, is different from the last two samples, *B* and *C*, then the clock is leading "early" as in figure 2.10 (b). The first two samples, *A* and *B*, are XORed to give the DOWN signal, while last two samples, *B* and *C*, are XORed to give the UP signal. Table 2.1 is a truth table that presents the binary logic of the UP and DOWN signals. Note that both Up and DOWN signals cannot be high at the same time.

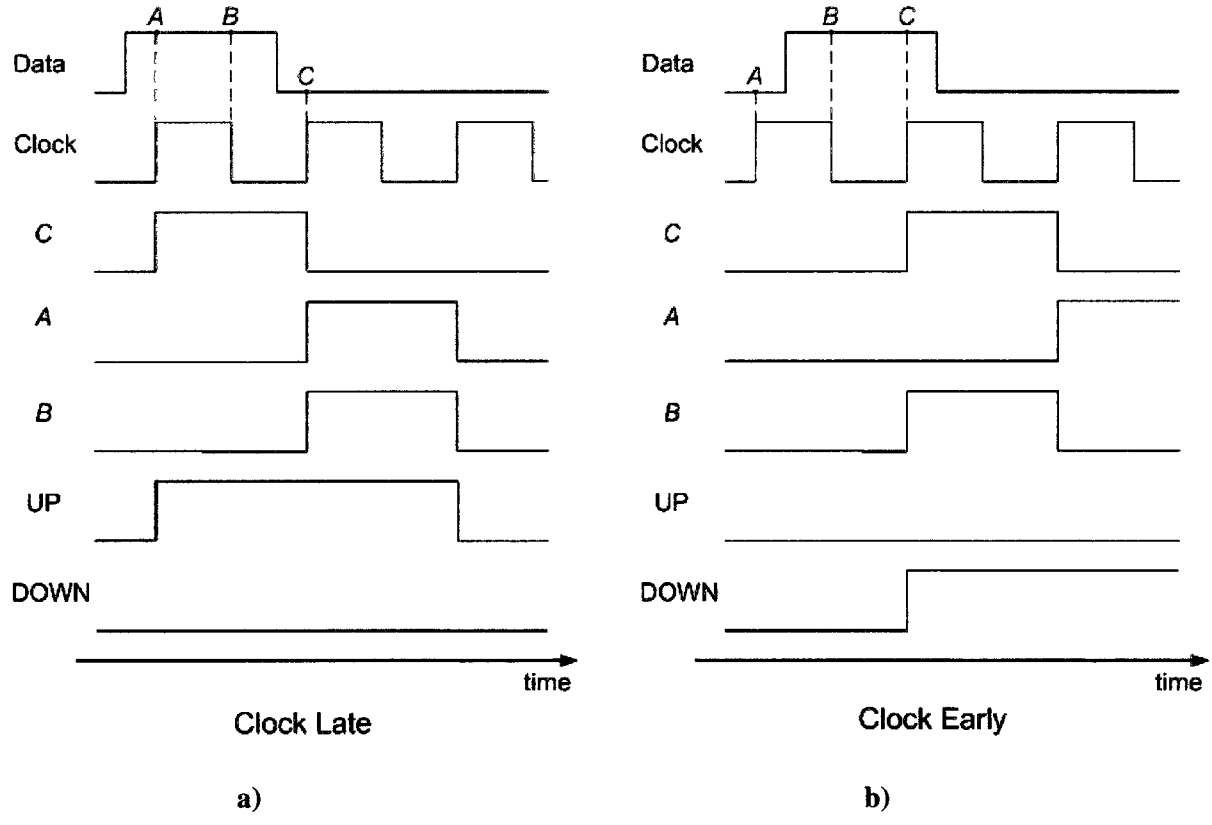


Figure 2.10 Waveforms of an Alexander phase detector

Table 2.1 Truth table of the bang-bang phase detector

Data State	A	B	C	UP	DOWN	Meaning
No data	0	0	0	0	0	Hold
Transition 0 to 1	0	0	1	0	1	Early
Not valid	0	1	0	0	0	Hold
Transition 0 to 1	0	1	1	1	0	Late
Transition 1 to 0	1	0	0	1	0	Late
Not valid	1	0	1	0	0	Hold
Transition 1 to 0	1	1	0	0	1	Early
No Edge	1	1	1	0	0	Hold

2.6 Classification of jitter

Jitter refers to the deviations of timing events from its ideal positions, as illustrated in figure 2.11. In a CDR circuit the events of interest are the optimum sampling instant of an NRZ encoded waveform. There are many definitions for the jitter, but there is a fundamental similarity that lies in the time difference between the ideal and actual occurrence of an event. Jitter is usually expressed in Unit interval (UI), where UI is the reciprocal of the average data rate. The definition of instantaneous jitter can be written mathematically as [23]

$$j[n] = t_E[n]_{Ideal} - t_E[n]_{Actual}$$

where j[n] is the instantaneous jitter at the n_{th} occurrence of the event and t_E[n] is the time of the n_{th} event.

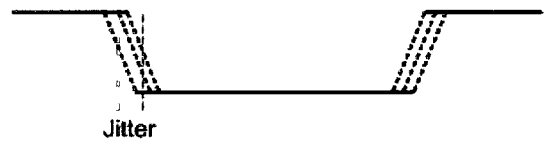


Figure 2.11 Jitter definition

An eye diagram is used to visualize how jitter can lead to errors when detecting binary bits, as shown in figure 2.12. An eye-diagram folds all the bit periods on each other relative to a bit clock. The eye diagram functions as a timing analysis tool providing the user with a good visual of timing and level errors. Jitter is very difficult to quantify since it changes from cycle to cycle, making an eye diagram a very good tool for finding the maximum jitter as well as voltage level errors. The open area within the eye is referred to as the eye opening, which decreases as errors increase. The eye diagram mask specifies a minimum eye opening for a CDR circuit.

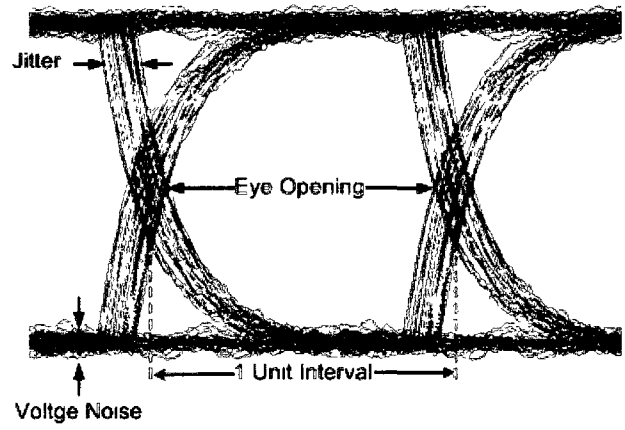


Figure 2.12 Eye diagram

While jitter is technically the non-ideality of a singular event, it is most often treated in a statistical manner. The difference in the zero-crossing points of the clock and data signals of a CDR circuit are measured over a period of time, and calculations are made with respect to both the magnitude and the phase [24].

While the exact nature of jitter can at times be difficult to determine, jitter is broadly divided into two fundamental types, called Random jitter (RJ) and Deterministic jitter

(DJ), as shown in figure 2.13. To add Random jitter (RJ) and Deterministic jitter (DJ) together, they have to have the same units. While random jitter is usually computed as rms value, deterministic jitter is computed as peak-to-peak value. Converting rms jitter to peak-to-peak jitter can be done by defining arbitrary limits on the Gaussian PDF that is characteristic of RJ. Limits are determined based on the bit error rate (BER) required by the system as in table 2.2 [25]. A value corresponding to an appropriate BER is then multiplied by the rms jitter to calculate the peak-to-peak jitter [23].

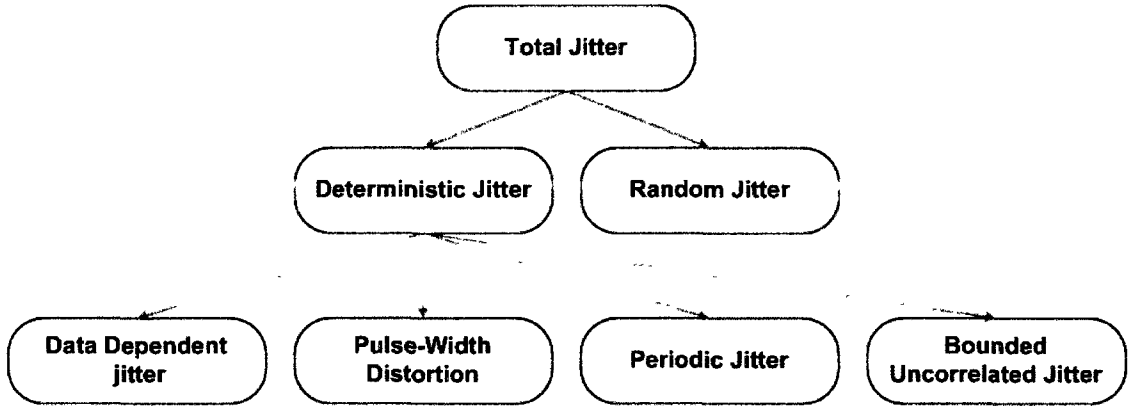


Figure 2.13 Jitter subcomponents

Table 2.2 Scaling Factors (α) Corresponding to System BER

BER	α	BER	α
10^{-5}	8.530	10^{-11}	13.412
10^{-6}	9.507	10^{-12}	14.069
10^{-7}	10.399	10^{-13}	14.698
10^{-8}	11.224	10^{-14}	15.301
10^{-9}	11.996	10^{-15}	15.883
10^{-10}	12.723	10^{-16}	16.444

2.6.1 Random jitter

Random jitter (RJ) is unpredictable and has a Gaussian probability density function. The causes of RJ are generally due to device noise sources such as shot noise [24,26]. Shot noise is related to the fluctuation in current flow in a transistor. Thermal noise is another component of device noise. Electron scattering causes thermal noise when electrons move through a conducting medium and collide with silicon atoms or impurities in the lattice. Higher temperatures results in greater atoms vibrations and increases chances of collisions. Another component of device noise is flicker noise, or 1/frequency noise. It is caused by the random capture and emission of carriers from oxide interface traps affecting carrier density in a transistor.

As random jitter is statistical in nature and has a Gaussian PDF. A Gaussian distribution is unbounded by definition and is characterized by its mean and rms values. As a result, random jitter measurements for separate system components cannot be directly added, but may be combined by taking the square-root of the sum of the squares.

2.6.2 Deterministic jitter

Deterministic jitter describes timing variations that have identifiable causes and bounded in amplitude. The sources of deterministic jitter include limited bandwidth, signal reflection, duty-cycle distortion, cross talk, and power-supply noise. Deterministic jitter can be divided into four categories: Data Dependent Jitter (DDJ), Pulse Width Distortion (PWD), Periodic Jitter (PJ) and Bounded Uncorrelated Jitter [23].

2.6.2.1. Data dependent jitter (DDJ)

Data Dependent Jitter (DDJ) and Intersymbol Interference (ISI) are two different names for the same type of jitter, viewed from the perspective of time and frequency, respectively. DDJ refers to jitter from a time-domain perspective. DDJ is the timing jitter that is correlated with the bit sequence in a data stream. In other words, the response of the current bit is affected by the response of the previous bits. DDJ is caused by limited bandwidth.

ISI refers to jitter from a frequency-domain perspective. It is defined as pulse spreading due to limitation in the system bandwidth. When the system bandwidth is approximately the same as the bandwidth required by the pulse, then the pulse are spread into adjacent bit times, causing errors in interpretation of binary bits.

2.6.2.2. Pulse Width Distortion (PWD)

Pulse Width Distortion (PWD) or Duty Cycle Distortion (DCD) is the difference between the pulse width of a high output and low output. PWD causes a distortion in the eye diagram where the eye crossings are offset up or down from the vertical midpoint of the eye. Figure 2.14 shows an eye diagram that is distorted by PWD. The most common causes of PWD are voltage offsets between the differential inputs and differences between the rise and fall times in the system.

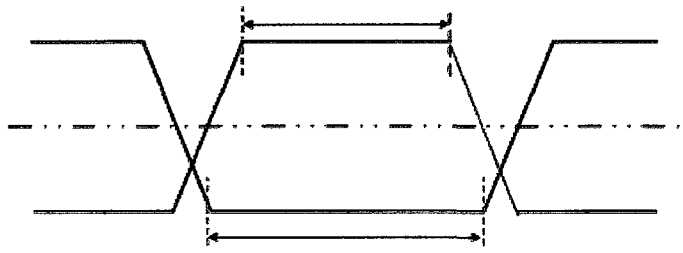


Figure 2.14 PWD illustration

2.6.2.3. Periodic Jitter (PJ)

Periodic jitter (PJ) or Sinusoidal Jitter (SJ) refers to the periodic variations of the rising and falling edges of the signal in time. The periodic variations follow a sinusoidal pattern and the is defined mathematically by,

$$j[n] = A_{in} \sin(\frac{\omega_j n}{r} + \delta)$$

where j[n] represents the instantaneous jitter at edge n, A_{in} is the jitter amplitude, ω_j is the jitter frequency, r is the data rate, and δ represents an arbitrary phase offset. Sinusoidal jitter is seldom encountered in real systems, but it is widely used in jitter testing.

2.6.2.4. Bounded Uncorrelated Jitter

Uncorrelated and Bounded Jitter is any deterministic jitter that is bounded but do not fit in any of the three sub groups mentioned above. Examples of this type of jitter are cross talk and power supply noise.

2.7 CDR figures of merit (FOM)

Jitter Generation, Jitter Transfer and Jitter Tolerance are the main figures of merit used to estimate the performance of the CDR circuits in the specified applications. Other

common FOM are BER, power consumption, chip area and operating frequency. In this section we only focus on Jitter Generation, Jitter Transfer and Jitter Tolerance.

2.7.1 Jitter Generation

Jitter generation, or sometimes called intrinsic jitter, is the jitter generated by a device or component when no jitter is applied to its input. This parameter is primarily used to measure the performance of transmitting components. Jitter generation in a CDR circuit is caused by a number of sources such as clock thermal noise, drift in clock oscillators and cross talk [27]. It is measured by applying an ideal signal, with no jitter, to the input of the Device Under Test (DUT), and measuring its output jitter. For OC-192, the jitter generation is specified not to exceed 100mUI peak-to-peak or 10mUI RMS when measured using a high-pass filter with a 50 kHz cut-off frequency. Figure 2.15 shows the jitter generation mask for OC-192 [28].

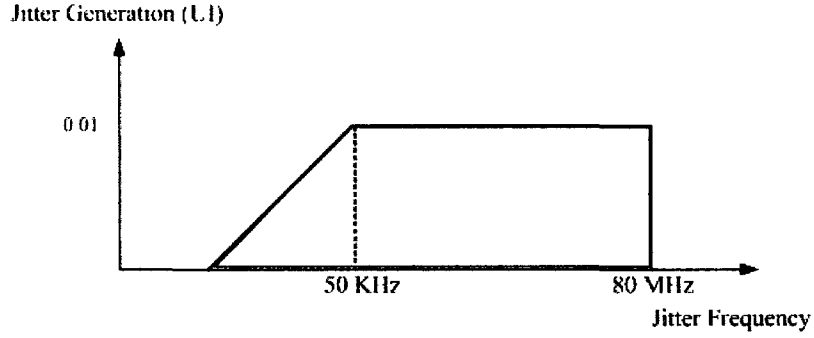


Figure 2.15 Jitter generation for OC-192

2.7.2 Jitter Transfer

Jitter transfer is defined as the relationship between the applied input jitter and the resulting output jitter as a function of frequency. In other words, it's a measure of how

much a CDR can attenuate its input jitter. It is represented mathematically as $\theta_{out} / \theta_{in}$. Jitter transfer is very important in optical communication systems where a signal goes through many repeaters. If jitter at a particular frequency is amplified at each repeater, the magnitude of the jitter will eventually cause the system to fail. For an OC-192 system the maximum jitter amplification which is acceptable is 0.1dB, and the jitter transfer function has a -3dB frequency of 8MHz. The OC-192 jitter transfer mask is shown in Figure 2.16.

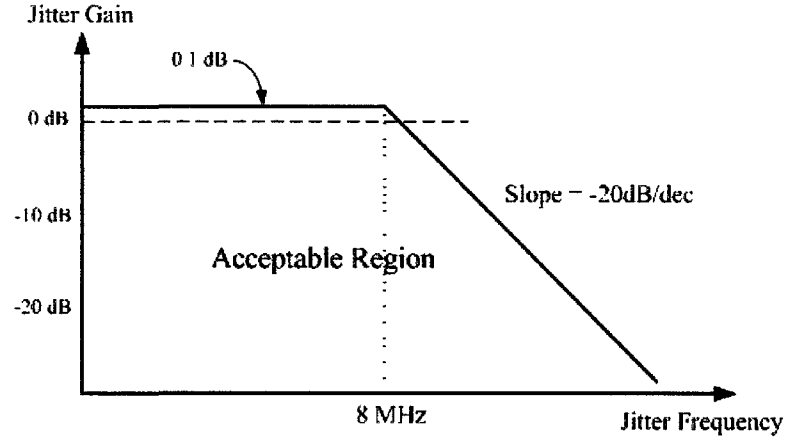


Figure 2.16 Jitter transfer mask for OC-192

2.7.3 Jitter Tolerance

Jitter tolerance is the maximum input jitter a CDR can tolerate while recovering data with specified BER. The jitter tolerance mask for SONET OC-192 is shown in Figure 2.17. This figure shows that the CDR circuit must be able to track jitter frequencies under 2.4kHz with a magnitude up to 15UI. The data rate for OC-192 is 10Gb/s, therefore the unit interval is 100ps. This means an OC-192 compliant CDR circuit must be able to track a data stream with up to 1.5ns of peak-to-peak jitter at 2.4kHz. At frequencies

higher than 2.4kHz, the mask drops by two orders of magnitude in two discrete steps. At jitter frequencies greater than 4MHz the CDR circuit must track only as long as the jitter magnitude is less than 0.15UI, or 15ps peak-to-peak.

The maximum phase error which can be tolerated in any situation is equal to half the period, or 0.5UI. This is expressed mathematically as

$$\theta_{in} - \theta_{out} < 0.5UI$$

Using the mathematical representation of jitter transfer, we can rewrite the above equation as,

$$\theta_{in}(1 - \frac{\theta_{out}}{\theta_{in}}) < 0.5UI$$

$$\theta_{in}(1 - Jtrans(s)) < 0.5UI$$

$$\theta_{in} < \frac{0.5UI}{1-Jtrans(s)} \quad 2.1$$

Equation 2.1 describes a relationship where the input jitter θ_{in} must be less than the expression on the right hand side. Since the maximum magnitude of input jitter is the jitter tolerance, an expression for jitter tolerance can be written as,

$$Jtol(s) = \frac{0.5UI}{1-Jtrans(s)} \quad 2.2$$

Jitter tolerance and jitter transfer create some obvious design constraints for a CDR circuit. The OC-192 jitter tolerance mask shows that the system must track jitter of reasonably large magnitudes less than 4MHz. As a PLL tracks jitter at frequencies less than its loop bandwidth, the loop bandwidth of an OC-192 CDR circuit must be greater than 4MHz. The jitter transfer mask shows that the input jitter with magnitude greater than 8MHz must be significantly attenuated. As a CDR circuit attenuates jitter at

frequencies greater than its loop bandwidth, the bandwidth must be less than 8MHz. For this reason most CDR circuits for OC-192 application have a system bandwidth of approximately 6MHz.

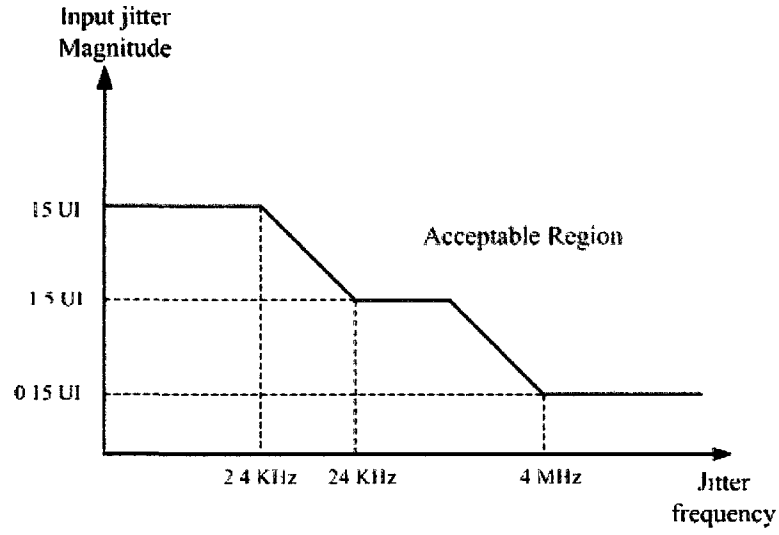


Figure 2.17 Jitter tolerance mask for OC-192

2.8 Modelling

One of the advantages of a linear phase detector is the ease of analysis. The analysis is based on the classical loop theory of PLL and is therefore used for the derivation of jitter transfer and jitter tolerance. On the other hand, a bang-bang phase detector is very challenging to analyze because of its non linear behaviour. While the output of a linear phase detector is proportional to the phase error, the output of a bang-bang phase detector is either UP or DOWN, regardless of the magnitude of the phase error.

In recent years, a number of papers have been published describing models for the analysis of the nonlinear behaviour of the bang-bang phase detector. Reviewing most of the papers, there are two main methods for analyzing the bang-bang PLL loop. The first

method was introduced by Walker [1] and the second method was illustrated by Lee et al. [29]. In sections 2.8.1 and 2.8.2 we will discuss each method into more details.

Other methods have been utilized to analyze the nonlinear loop dynamics [30-34]. In [30, 31] analysis of first and second order bang-bang PLL loops were analyzed using a discrete-time iterative method. The work was focused on studying the loop stability by investigating limit cycles. A continuation of this work was presented in [32] for third order bang-bang CDR circuits using discrete-time and continuous-time analysis. Equations were derived to describe the steady-state solutions and stability of the loop was illustrated.

Statistical analysis of first order bang-bang CDR circuit was used in [33] to analyze the steady-state timing jitter. An analogy was made between first order delta modulator and bang-bang CDR circuit in order to relate hunting jitter and slew rate limiting in bang-bang PLL loop to granular noise and slope overload in a delta modulator. However, jitter transfer and jitter tolerance analyses were not discussed in this paper.

Describing functions method was used in [34] for jitter tolerance analysis. However, the analysis is not accurate and there was no closed form solution for the jitter tolerance expression.

2.8.1 Analysis of bang-bang PLL loop: method 1

Walker was the first one to explain the influence of the non linear behaviour on the loop dynamics for the first and second order bang-bang CDR circuits [4]. Walker analyzed the first order loop by modelling the bang-bang phase detector with a binary quantizer as shown in figure 2.18. The binary quantizer limits the phase error of the loop at each

sampling time, t_n. The phase error, θ_{err}, of the loop is defined as the phase difference between the incoming data phase, θ_{in} and the output of the VCO phase, θ_{out}. The sign of the phase error then drives a frequency step to the VCO center frequency. The frequency step, or bang-bang frequency step, is defined as $\omega_{bb} = \beta K_v$, where β is an attenuator and K_v is the VCO gain. Then he derived a set of difference equations to describe the loop dynamics as

$$\theta_{in}(t_n) = \theta_{in}(0) + \delta\omega t_n + \varphi(t_n) \quad 2.3$$

$$\theta_{out}(t_n + 1) = \theta_{out}(t_n) + \varepsilon_n \theta_{bb} \quad 2.4$$

$$\varepsilon_n = sign[\theta_{in}(t_n) - \theta_{out}(t_n)] \quad 2.5$$

where θ_{bb} is the bang-bang phase step and is defined as

$$\theta_{bb} = \frac{\omega_{bb}}{\omega_c} \quad 2.6$$

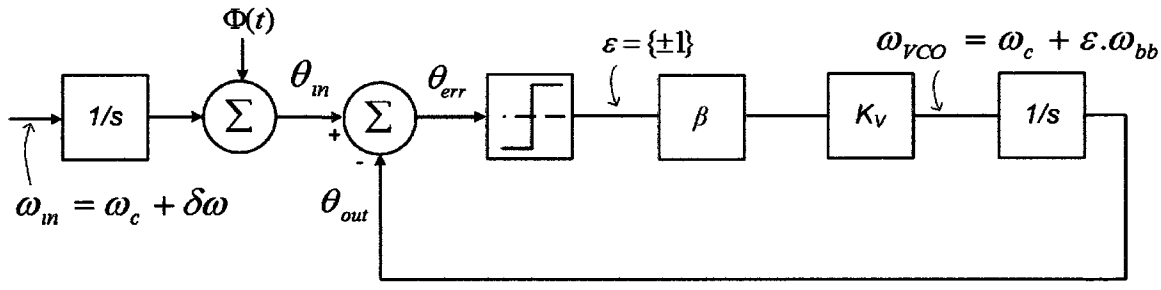


Figure 2.18 Model for first order bang-bang PLL loop

Walker then modeled the second order loop by introducing an integrator between the phase detector and the VCO to account for the capacitor in the first order loop filter. As shown in figure 2.19, the model consists of two paths, proportional path, or bang-bang path, and integral path. Modelling the loop filter as two non-interacting paths is valid as long as the proportional phase step is greater than the integral phase step. The ratio

between the phase steps of the two paths is defined as the stability factor, ζ, which has to be greater than one. An expression for the stability factor is given by equation 2.8

$$Stability\ factor = \frac{\Delta\theta_{proportional}}{\Delta\theta_{integral}} = \frac{\beta K_v t_n}{K_v \alpha {t_n}^2 / 2} \quad 2.7$$

$$Stability\ factor = \frac{2\beta}{\alpha t_n} \quad 2.8$$

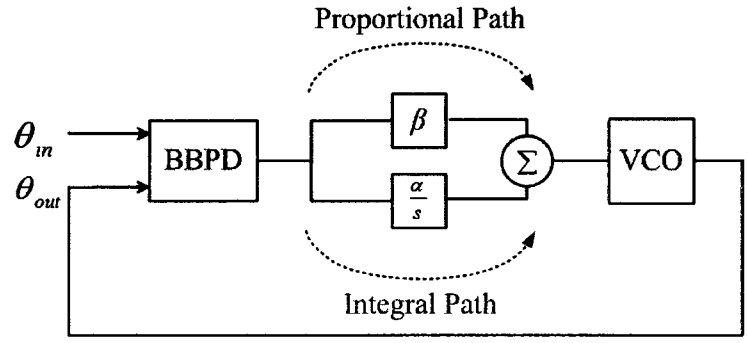


Figure 2.19 Model of second order bang-bang PLL loop

Jitter generation is usually not discussed in detail since it is difficult to formulate an equation which precisely describes it. In [35], Greshishchev et al. showed that loop delay, t_{delay}, and bang-bang frequency step, ω_{bb}, are proportional to jitter generation, as will be shown later. In contrast, Walker formulates an equation for jitter generation by describing the phase detector as a noise source and calculating the output noise. The analysis is quite detailed and deals with several regions of operation which depend on the magnitude of the input jitter and the bang-bang phase step. The resulting equation is given in equation 2.9

$$JG \approx 0.79\sqrt{\theta_{bb} \cdot A_{in}} \quad 2.9$$

In chapters 3 and 4 we will discuss Walker's analysis for jitter transfer and jitter tolerance respectively.

Ramezani et al. had valuable contributions to the Walker's model by further analyzing the loop in the time domain [36, 37] . They developed an equivalent circuit for the second order bang-bang that relates the proportional path and integral path to the charge pump and loop filter of the circuit, as shown in figure 2.20. The VCO control voltage, ΔV_{in}, is defined as the sum of the control voltage from the proportional and integral paths and is given by equation 2.10.

$$\Delta V_{in} = \Delta V_{bb} + \Delta V_{int}, \tag{2.10}$$

where

$$\Delta V_{bb} = IR = \beta \tag{2.11}$$

$$\Delta V_{int} = \frac{1}{C}\int_0^T I\, dt = \alpha T \tag{2.12}$$

The resulted phase and frequency steps at the output of the proportional and integral paths respectively during a time period t_n are

$$\Delta\theta = \Delta V_{bb} K_v \frac{T}{2} \tag{2.13}$$

$$\Delta\omega = \Delta V_{int} K_v \tag{2.14}$$

A timing model was used to explain the lock in frequency range and the lock in phase range for a second order bang-bang PLL loop. An expression was derived for the locking behaviour and is given in equation 2.15. The expression suggests the condition for the loop to converge to a small phase error. This condition calls for the phase step from the proportional path to be larger than the phase step from the integral path

$$2\Delta\theta > \Delta\omega . T \tag{2.15}$$

Looking at equations 2.11, 2.12, 2.13 and 2.14, it becomes evident that equation 2.15 is the same expression as the stability factor that Walker introduced and is shown in equation 2.8.

$$\beta > \alpha T \tag{2.16}$$

Although Ramezani et al. discussed in more details the loop dynamics of second order bang-bang CDR circuit, they did not analyze jitter transfer and jitter tolerance.

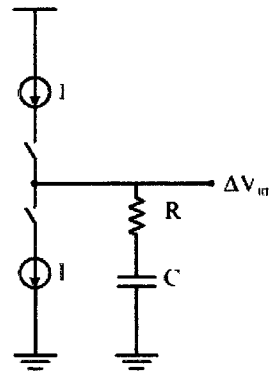


Figure 2.20 Charge pump and loop filter equivalent circuit

Greshishev et al. used Walker's model for the second order circuit to design a 10Gb/s bang-bang receiver [35]. He used the model to make an analogy with the behaviour of a double integration delta modulator with prediction [38] to approximate the bang-bang frequency step, ω_{bb}. Based on the delta modulator, he showed a relationship between the jitter transfer bandwidth, ω_j, and the bang-bang frequency step, ω_{bb}, as in equation 2.17.

$$\omega_j \propto \frac{\omega_{bb}}{A_{in}} \tag{2.17}$$

where ω_j is the jitter transfer bandwidth, A_{in} is the jitter amplitude, ω_{bb} is the bang-bang frequency step. Then he examines the effect of the bang-bang frequency step, ω_{bb}, on the jitter tolerance curve, as plotted in figure 2.21. Finally, he derived an empirical formula

for the relationship between jitter generation and the bang-bang frequency step, ω_{bb}, as in equation 2.18 and figure 2.22.

$$JG \propto t_{delay} \cdot \omega_{bb} \qquad 2.18$$

where JG is the jitter generation, and t_{delay} is delay in the PLL loop.

An optimum value for the bang-bang frequency step, ω_{bb}, was derived based on figures 2.21 and 2.22. Although the simulation results agree with measured results, there were no general equations shown for the three jitter characteristics.

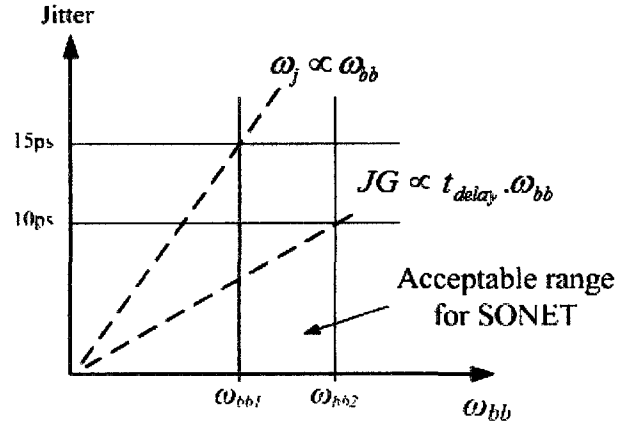


Figure 2.21 Trade off in the frequency step, ω_{bb}, for bang-bang PLL loop

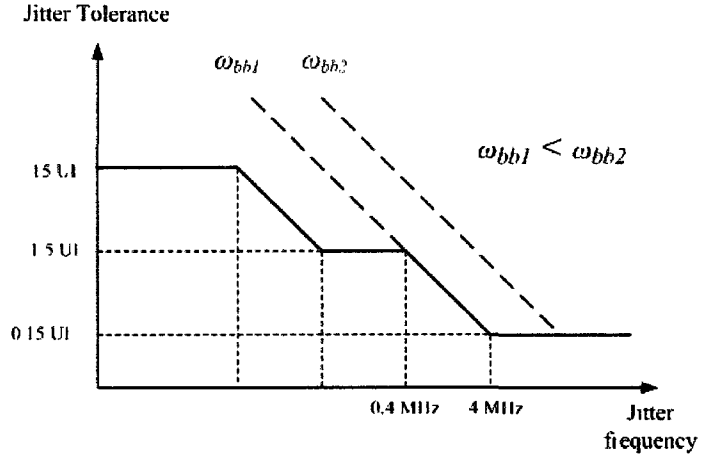


Figure 2.22 Jitter tolerance curve for two different bang-bang frequency steps

Wang et al. was the first to investigate the loop dynamics of a third order bang-bang PLL loop [39]. A second capacitor was added to the loop filter, as shown in figure 2.23, and equations derived by Walker were modified to account for the extra capacitor. Jitter tolerance performance was examined against different parameters such as Baud rate, loop filter resistor, and loop filter capacitance. The analysis showed that there is a trade-off between these parameters.

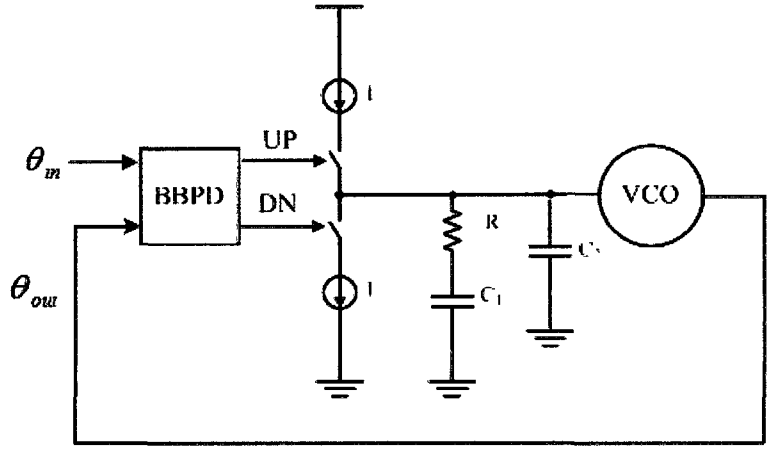


Figure 2.23 Third order bang-bang PLL loop

Other efforts include Chan et al. who analyzed the first and second order bang-bang PLL loops based on Walker models using transient analysis. In his work he discussed the cycle slipping and the far from lock regions [40, 41].

Sonntag and Stonick analyzed a digital bang-bang PLL loop by using a linearized small-signal model [6]. Unlike Walker, they modeled the bang-bang phase detector response as non-ideal.

2.8.2 Analysis of bang-bang PLL loop: method 2

The second method for analyzing the bang-bang PLL loop was presented by Lee et al. [29]. While all authors assumed an ideal response of the bang-bang phase detector, Lee et al. suggested that the response of the bang-bang phase detector should not be ideal. The presence of metastability and jitter resulted in a smoothed bang-bang phase detector response as illustrated by Lee et al. In the analysis, the circuit for bang-bang PLL loop was used instead of the model with two paths that was introduced by Walker, as shown in figure 2.24. A large-signal piecewise-linear model was utilized in describing the behaviour of the second order bang-bang PLL loop.

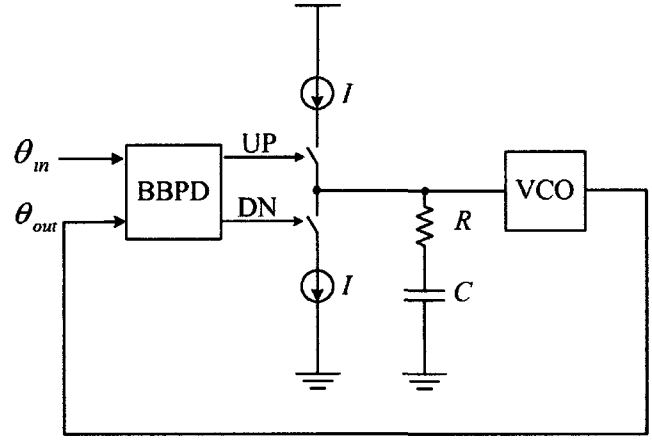


Figure 2.24 Second order bang-bang PLL loop

The analysis depends on the observation of the output jitter at different regions then deriving equations for each region. An expression is derived for jitter transfer by observing the output when the input jitter amplitude is high, as shown in figure 2.25. More details on jitter transfer analysis will be discussed in chapter 3.

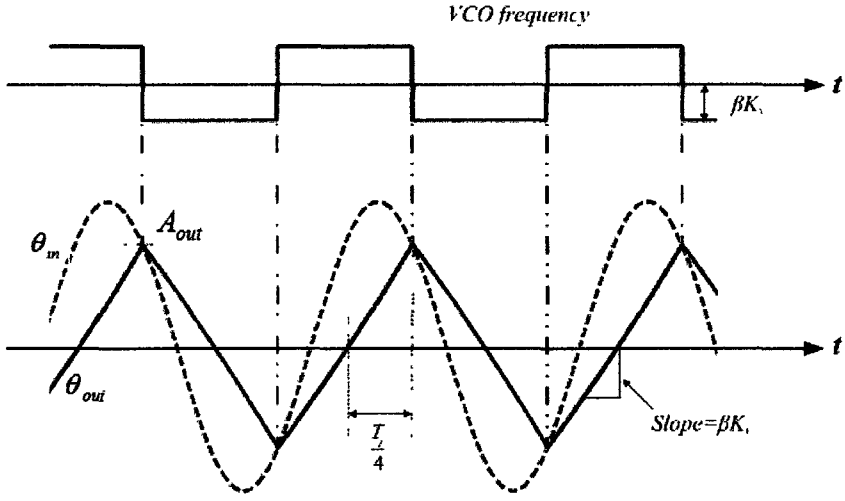


Figure 2.25 Waveform used to determine the jitter transfer response

An expression for jitter tolerance is then derived by finding the maximum input jitter that will cause a phase error of less than 0.5UI, where phase error is the difference between the input and output phase. The jitter tolerance curve is then divided into two regions according to the frequency range as shown in figure 2.26. Jitter tolerance analysis will be discussed in more details in chapter 4.

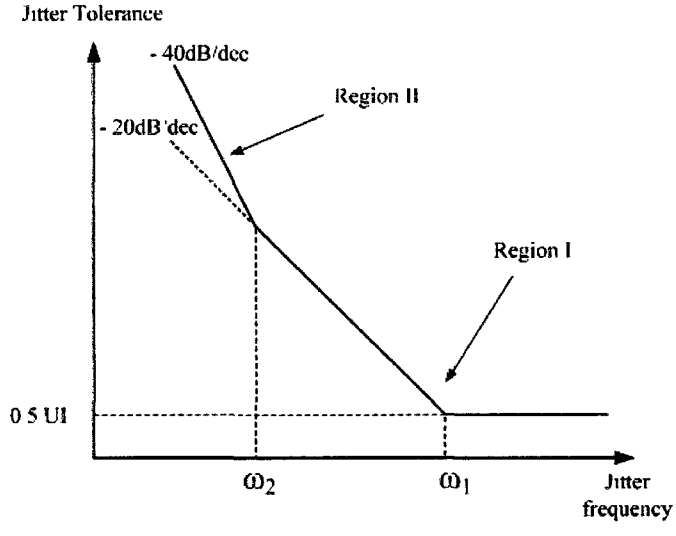


Figure 2.26 Jitter tolerance curve divided into two regions for analysis

Kundert continued Lee et al.'s work by using the developed phase model to estimate the BER of the circuit in presence of both deterministic and random jitter [42]. He discussed the non-ideal response of bang-bang phase detector in a phase domain model. Figure 2.27 illustrates the statistical averaged transfer function of a bang-bang phase detector due to jitter. Equations were derived for the jitter tolerance curve and BER in presence of both deterministic and random jitter. However, the study of random jitter is out of the scope of this thesis.

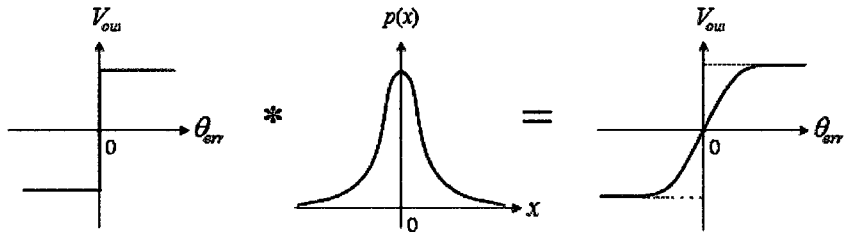


Figure 2.27 Statistically averaged transfer function of bang-bang phase detector

Another effort was put forth by Hong and Cheng where they investigated the effect of including random jitter on jitter transfer analysis [43]. Figure 2.28 shows simulation of jitter transfer when random jitter was included. The simulated results (dotted lines) exhibit smaller jitter bandwidth and steeper slopes. An empirical formula for the slope based on behavioural simulation using Matlab as in equation 2.19 was found.

$$Slope = \begin{cases} -14.5\left(\frac{\sigma_{PJ}}{\sigma_{PJ}+\sigma_{RJ}}\right) - 5.5 + 0.5\log_2\left(\frac{0\,1}{\sigma_{RJ}}\right) & ,if\ slope > -18.5 \\ -18.5 & ,otherwise \end{cases} \qquad 2.19$$

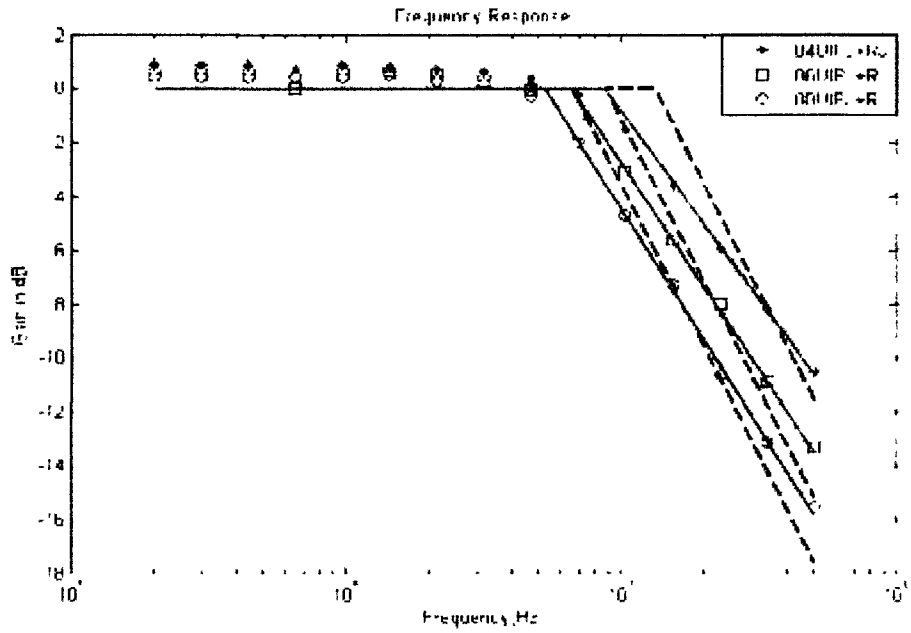


Figure 2.28 Variations in jitter transfer curve due to RJ [43]

Hong and Cheng then proposed a method for estimating the BER of the bang-bang PLL loop. The random jitter parameters were included in the jitter transfer and jitter tolerance expressions derived by Lee et al. However, only the equation for region I was used ignoring region II. In addition, he is comparing his simulation results with equations from [29] that did not include random jitter, as shown in figure 2.29.

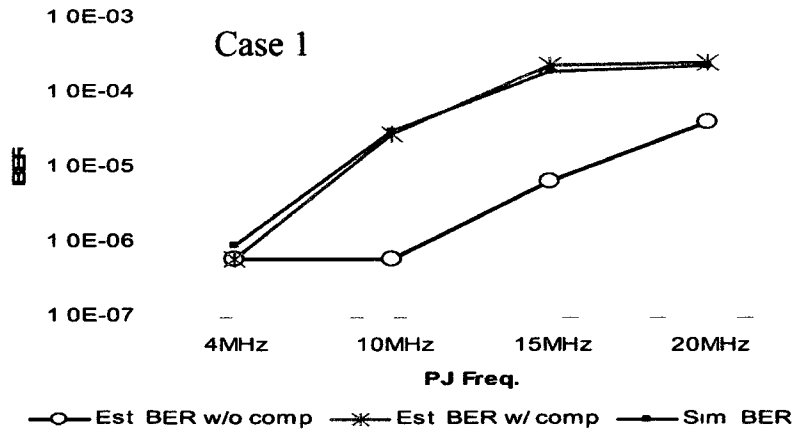


Figure 2.29 BER simulation results [43]

2.9 Summary

This chapter presented two popular formats of data modulation followed by presenting the basics of CDR circuits. CDR circuits employing both linear and bang-bang phase detectors were investigated showing the architecture of each one. Various FOM are used to characterize the performance of CDR circuits, and jitter generation, jitter transfer, and jitter tolerance were illustrated. Finally, we presented recent efforts to analyze the non-linear behaviour of bang-bang PLL loops. The methods used in the analysis were categorized into two main ones. Several papers in each category were presented.

Chapter 3: Jitter Transfer analysis

3.1 Introduction

Jitter transfer function is referred to as the ratio of the output jitter to the jitter applied at the input versus frequency. In long haul transmission systems where repeaters exist, it is very important to ensure that the CDR circuit meets the jitter transfer mask requirements. Several methods have been proposed for analyzing the nonlinear behaviour of BBPDs [1,29,37,44]. We have shown in section 2.8 that there are two main methods for analyzing second order bang-bang PLL loop. In this chapter we will use both methods to analyze the jitter transfer characteristics for the second order bang-bang PLL loop. A more accurate expression is proposed and verified by simulation [45].

3.2 Jitter Transfer Characteristics

As defined in section 2.7.2, Jitter transfer is the relationship between the applied input jitter and the resulting output jitter as a function of frequency. It is a measure of how much jitter is attenuated or amplified from the input to the output of a network equipment. If the jitter transfer mask is met, then there is no amplification of jitter by the network equipment as that jitter traverses multiple repeaters.

To measure jitter transfer, the amplitude of the output jitter is compared to the amplitude of the input jitter, as shown in figure 3.1 [46]. According to the jitter transfer

definition, only the amplitude of the fundamental frequency component of the output jitter is compared to the amplitude of the input jitter. As a result, the fundamental frequency component is extracted from the output jitter by employing a very narrow-band tracking filter in the test measurement process [27]. This process is illustrated in figure 3.1, where the narrow band-pass filter is centered at ω_{in}, same frequency as the sinusoidal input test signal.

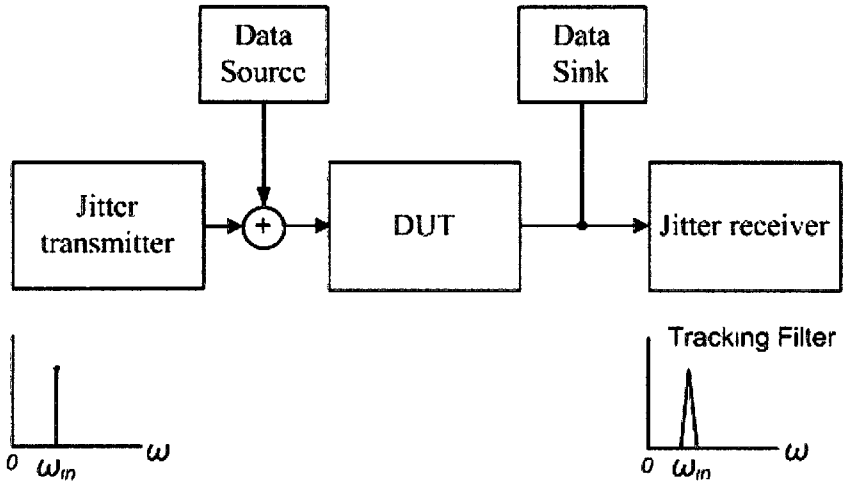


Figure 3.1 Jitter transfer measurement process where f_i denotes the jitter transfer test sinusoidal frequency

3.3 Jitter Transfer Analysis

We will limit our analysis to the two methods introduced in chapter 2. The first method models the CP and LF components as two separate paths, as shown in figure 3.2. One path is called the proportional path (or BB path) and it models the resistor in the LF, while the other path is called the integral path and it models the capacitor in the LF. Thus the VCO input control voltage, ΔV_{in}, is the sum of the BB voltage step, ΔV_{bb}, and the integral voltage step, ΔV_{int}, as were shown in equations 2.10, 2.11 and 2.12.

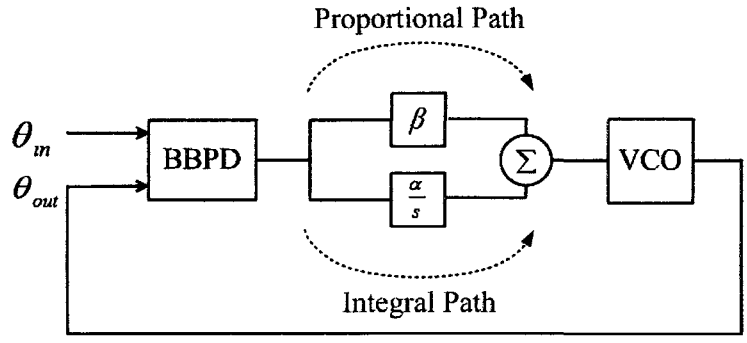


Figure 3.2 Bang-bang CDR circuit block diagram with two paths.

The second method used the block diagram of bang-bang PLL loop and has a conventional *RC* loop filter, as shown in figure 3.3. Even though this block diagram is a more straightforward illustration of the physical circuit, Walker's model is easier to comprehend making the operation of the loop more understandable. In the analysis, the effect of the capacitor, *C*, can be neglected at high jitter frequencies. This assumption is valid for large capacitor values.

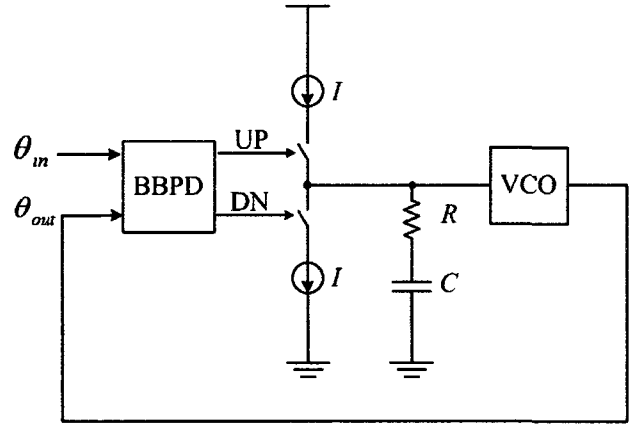


Figure 3.3 Bang-bang PLL loop block diagram with analog filter.

Jitter transfer is measured by applying a sinusoidal jitter at the input, $\theta_{in}(t) = A_{in}\sin(\omega_j t)$, and measuring the output jitter at the same frequency. The input jitter

amplitude is specified according to the jitter tolerance mask. At low frequencies the bang-bang loop can track the input jitter, and the gain is close to zero dB. As the jitter frequency increases, the loop cannot track the input and the phase error ($\theta_{err} = \theta_{in} - \theta_{out}$) increases. The region where the loop tracks is represented by the horizontal line on the jitter transfer curve in figure 2.16. The –20dB/dec slope is where the loop is slewing resulting in large errors. The corner frequency, which differentiates these two regions, is called the –3dB bandwidth (corner frequency) of the jitter transfer, ω_{-3dB}.

We will start presenting the analysis for Walker first in section 3.3.1, following the analysis by Lee et al. in section 3.3.2. However, in the analysis of both representations, the jitter transfer definition was disregarded leading to inaccurate results. Consequently, we had to apply the jitter transfer definition to derive a more accurate expression.

3.3.1 Method 1

Walker made a useful analogy between the bang-bang PLL loop and the Delta Modulator (DM) that allowed a valid explanation of the loop using existing theory on DM. In the DM, two types of distortion exist: quantization distortion (granular noise) and slope overload distortion. If the DM output is able to track the sinusoidal input signal, there is no error and the quantizer output frequently changes its sign. This tracking behaviour can be seen in figure 3.4 (a). If, on the other hand, the DM output is unable to follow the sinusoidal input signal shape, errors start to occur and the loop is said to experience slope overload [38], as shown in figure 3.4(b).

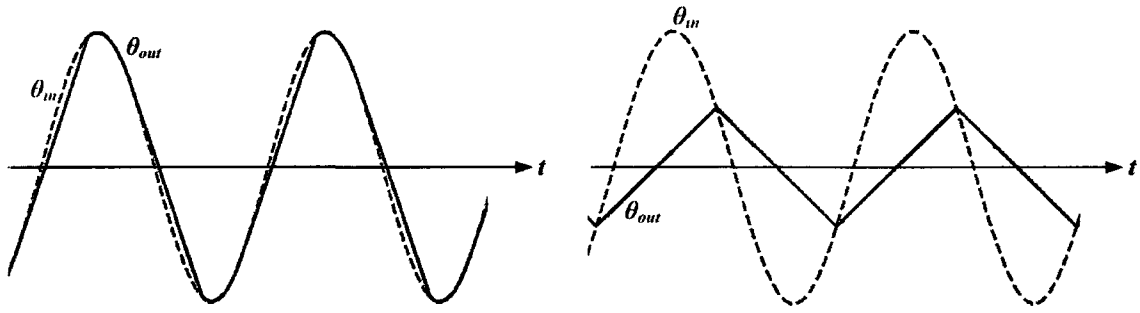


Figure 3.4 Slewing mechanism in PLL loop: (a) Onset of slewing. (b) Heavy slewing: loop cannot track the input sinusoidal shape.

Slewing, which occurs on the jitter transfer curve, is the same phenomena as slope overload in DM. This analogy enables us to derive an expression for the slewing condition based on DM theory.

For a sinusoidal input signal with amplitude A_{in} and frequency ω_j, the slope of the input signal is

$$\theta'_{in}(t) = A_{in}.\omega_j.cos\ (\omega_j t). \qquad 3.1$$

As mentioned earlier, the integral path is neglected reducing the loop to a first order loop. The maximum rate of increase of θ_{out}(t) is equal to the proportional path gain. Thus,

$$\theta'_{out}(t) = \beta K_v, \qquad 3.2$$

where K_v is the VCO gain in rad/V.s. Slope overload is avoided if $\theta'_{in} \leq \theta'_{out}$, and therefore from 3.1 and 3.2:

$$A_{in}\omega_j \leq \beta K_v. \qquad 3.3$$

The amplitude-frequency product defines the condition, so as to avoid slope overload. The loop starts to overload when either the amplitude or the frequency increases. Thus,

the maximum input jitter frequency where the loop can track the input jitter can be expressed as:

$$\omega_W = \frac{\beta K_v}{A_{in}}. \tag{3.4}$$

In this expression, the maximum input jitter frequency is inversely proportional to the jitter amplitude. ω_W can be thought of as the corner frequency for the CDR circuit as in a linear model. In other words, using this bandwidth will ensure that the CDR circuit never slews.

3.3.2 Method 2

Sinusoidal jitter with specified amplitude is applied to the block diagram in figure 3.3, and the frequency is increased until slewing occurs. To analyze the jitter transfer we use figure 3.5 as an extreme case where the bang-bang PLL loop is slewing. The output jitter is a triangular waveform with amplitude A_{out} and frequency ω_J. We can find the output jitter's peak amplitude by a simple integration of the slope for a duration of $T_J/2$ ($T_J = 2\pi/\omega_J$), that is,

$$A_{out} = \frac{\beta K_v T_J}{4}. \tag{3.5}$$

Therefore, the jitter transfer function can be represented as

$$\left|\frac{A_{out}}{A_{in}}\right| = \frac{\pi \beta K_v}{2 A_{in} \omega_J}. \tag{3.6}$$

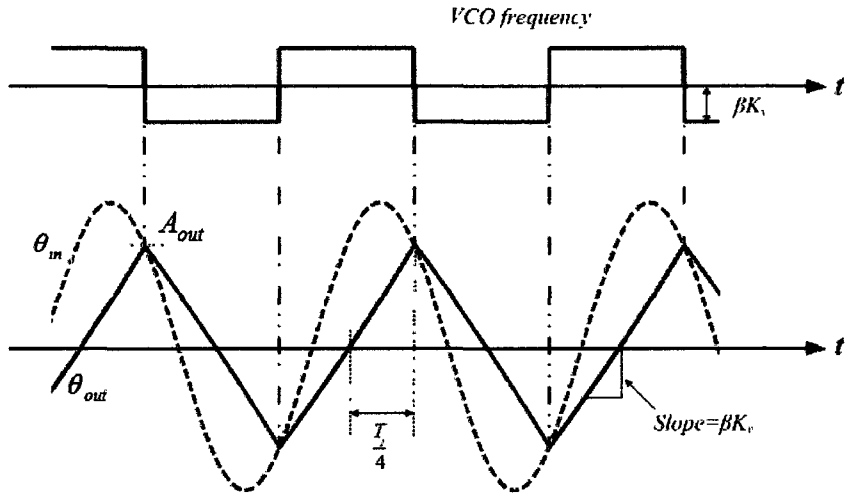


Figure 3.5 CDR loop is slewing.

This expression shows the dependency of the jitter transfer on the input jitter amplitude A_{in}. This dependency explains why the loop bandwidth of bang-bang PLL loops cannot be defined in a strict sense. An approximate value for the maximum frequency of the triangular waveform when $A_{out} = A_{in}$ can be found as:

$$\omega_L = \frac{\pi \beta K_v}{2A_{in}}. \qquad 3.7$$

3.3.3 Proposed expression

In order to comply with the definition, the output jitter must be measured at the same frequency as the input jitter. Consequently, we expand the output waveform into its Fourier series and measure the peak amplitude of the fundamental frequency component only. Taking only the fundamental frequency component corresponds to the describing function method used to analyze non linear systems [47]. For a triangle waveform the Fourier expansion is as follows:

$$f(t) = \frac{8}{\pi^2}(sin\omega t - \frac{1}{9}sin3\omega t + \frac{1}{25}sin5\omega t - \quad)$$

Thus, the jitter transfer function in equation 3.7 can be modified to be

$$\omega_{-3dB} = \frac{4\beta K_v}{\pi A_{in}}. \tag{3.8}$$

Equation 3.8 gives the -3dB bandwidth of the jitter transfer curve when both input and output jitter amplitudes are measured at the same frequency. In our analysis we use the physical output waveforms from simulation results to derive the jitter transfer expression.

Table 3.1 summarizes the jitter transfer expressions by Walker, Lee et al. and our proposed expression. The difference in the expressions for ω_w and ω_L is due to the phase error definition by each method. Walker used the slope overload analogy where the loop slews when the phase error, $\theta_{err} = \theta_{in} - \theta_{out}$, is greater than zero. On the other hand, Lee et al. suggested that the maximum phase error that will not degrade the BER is π. This explains why the maximum jitter transfer frequency is greater than the one derived by Walker.

Table 3.1 Jitter Transfer expressions

Jitter transfer, ω_w	$\frac{\beta K_v}{A_{in}}$
Jitter transfer, ω_L	$\mathbf{1.57}\frac{\boldsymbol{\beta K_v}}{\boldsymbol{A_{in}}}$
Jitter transfer, ω_{-3dB}	$\mathbf{1.27}\frac{\boldsymbol{\beta K_v}}{\boldsymbol{A_{in}}}$

3.4 Jitter transfer Simulation

In order to validate the jitter transfer analysis, a phase domain model for the second order bang-bang PLL loop was constructed in Matlab Simulink as shown in figure 3.6. A phase-domain model simulates the phase of the CDR signals. Details of each cycle are averaged and as a result faster simulations are achieved. The model is assumed to operate at 4Gb/s and a sinusoidal jitter signal is fed to the BBPD. The model uses the design parameters outlined in table 3.1. A very narrow band-pass filter is used at the output jitter signal.

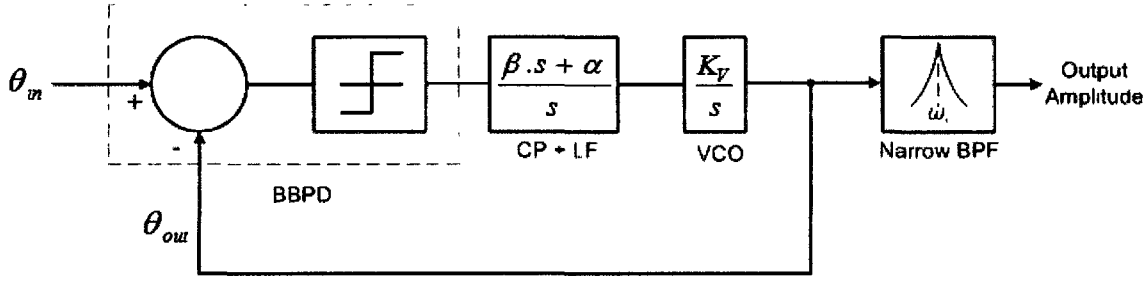


Figure 3.6 Phase-domain testbench for second order bang-bang PLL loop

Table 3.2 Design parameters for CDR circuit [48]

VCO gain, K_V (rad/V.s)	1.26×10^9
Charge Pump Current, I (μA)	40
Loop filter resistance, R (Ω)	500
Loop Filter Capacitor, C (nF)	5

Jitter transfer was simulated by sweeping the jitter frequency between 1 Mrad/sec and 1 Grad/sec using input jitter amplitude of 0.15 UI. At each frequency, the input and the resulting jitter amplitudes are recorded. Jitter transfer is then calculated as the ratio between the input and output jitter amplitudes at a given frequency. The bang-bang PLL

loop bandwidth can be estimated from its cutoff frequency. Simulation results are then compared with the theoretical analysis. From equations 3.4, 3.7 and 3.8 the entire jitter transfer curve can be approximated as a single pole curve:

$$Jtrans = \frac{\omega_{-3dB}}{\omega_{-3dB} + s}. \qquad 3.9$$

Figure 3.7 shows the predicted and simulated jitter transfer curves. Jitter curves show a –20dB/decade slope when the loop is in the slewing region. Equation 3.8 is the best fit for the simulated jitter transfer curve, as illustrated in figure 3.7.

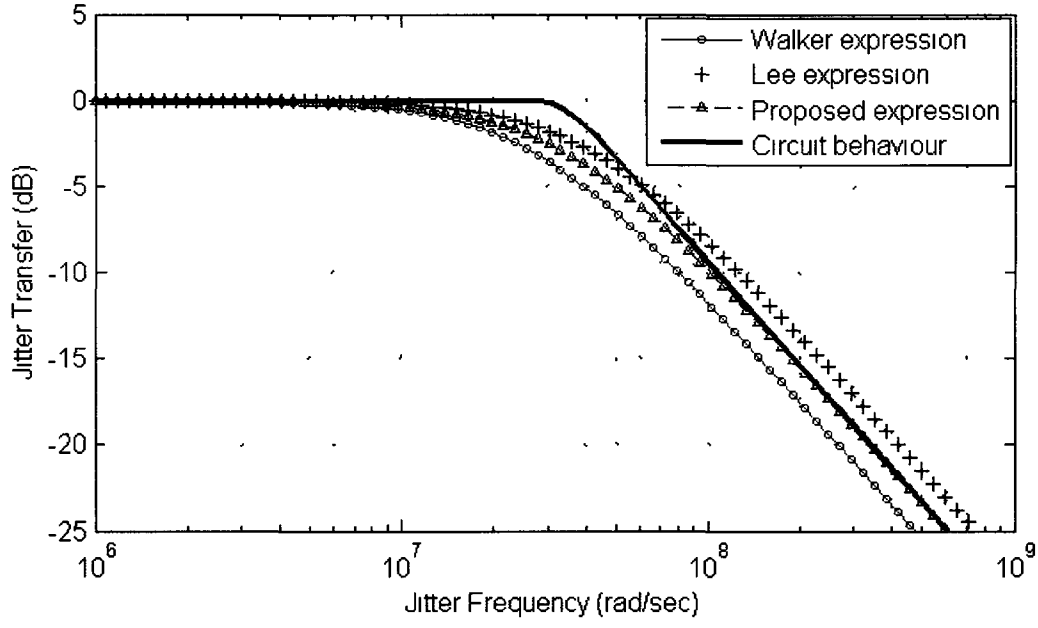


Figure 3.7 Predicted and simulated jitter transfer.

Different input jitter amplitudes were simulated, as shown in figure 3.8. Input jitter amplitudes of 0.15UI, 0.25UI and 0.5UI were simulated and compared with equation 3.8.

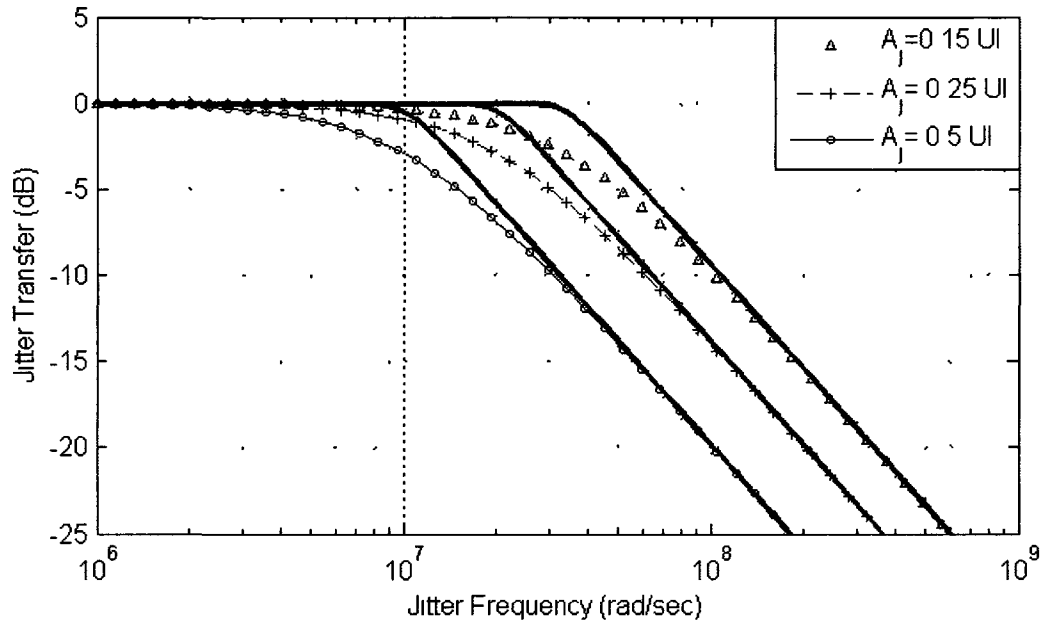


Figure 3.8 Predicted (dotted) and simulated (solid) jitter transfer curves for different input amplitudes.

3.5 Summary

In this chapter, we analyzed the jitter transfer characteristics of the second order bang-bang PLL loops using the two main methods introduced in chapter 2. The difference in the two representations was addressed and a more accurate expression was derived. Simulation results using a Simulink phase-domain model show the accuracy of our proposed expression.

Chapter 4: Jitter Tolerance analysis

4.1 Introduction

Jitter tolerance is defined as the peak amplitude of a sinusoidal jitter applied on the input of a CDR circuit that meets a given BER. In order to pass this requirement, a CDR circuit must exceed the limits in a jitter tolerance mask. Therefore an accurate design is required for meeting strict jitter tolerance masks. While there have been several papers investigating the jitter tolerance analysis, we will strict our analysis to the two main methods introduced in chapter 2. Then, verification of the accuracy of the models by behavioural simulation will be presented.

4.2 Jitter Tolerance Characteristics

Jitter tolerance measurements are required to confirm that in the presence of jitter, CDR circuits in a transmission system can operate with a desired BER. These tests can simply confirm that the minimum requirements are met or they can be more comprehensive where the additional margin and maximum tolerable jitter are measured. For convenience in testing, sinusoidal jitter is applied to the input of the DUT to simulate the phase variations. In practice, the jitter in transmission systems carrying real traffic is more like random noise [46].

A standard jitter tolerance mask is used as a reference during the test. A Sinusoidal jitter, $\theta_{in}(t) = A_{in}\sin(\omega_j t)$, is applied at the input of the DUT at a given frequency point. At the receiver's end, a check for transmission errors is carried out and input jitter amplitude is incremented or decremented until maximum tolerable jitter is determined. The process is repeated for each frequency point until the jitter tolerance mask frequency range is covered, as shown in figure 4.1. At low frequencies the bang-bang PLL loop can tolerate more jitter and as a result the input jitter amplitude is expected to be large. As the jitter frequency increases, the loop cannot tolerate much jitter and as a result there is a limitation on the maximum tolerable input jitter. Jitter tolerance mask for OC-192 was shown in chapter 2 and is presented here again for convenience.

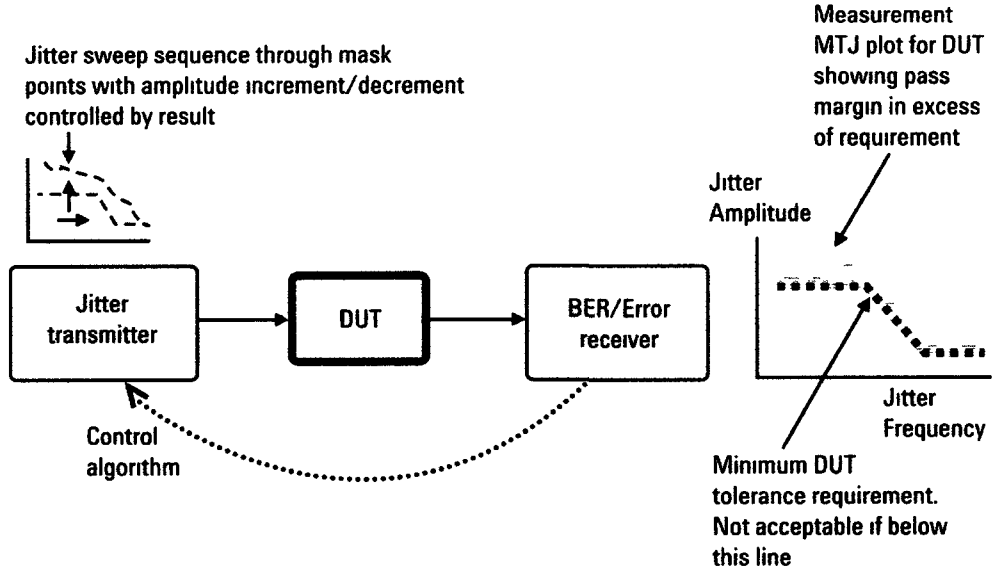


Figure 4.1 Maximum tolerable jitter Test [46]

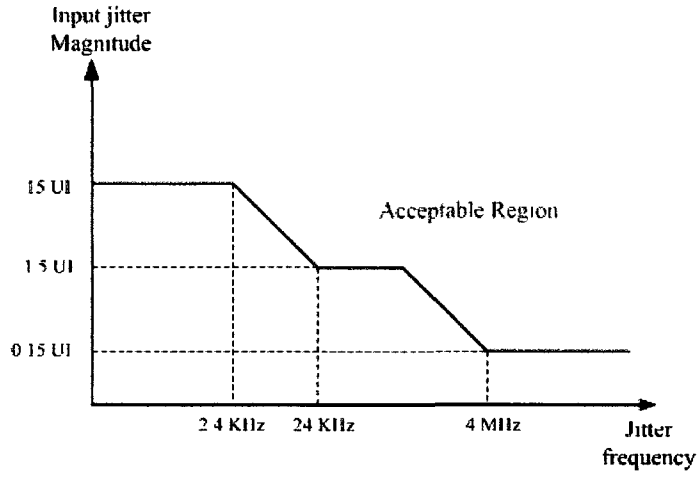


Figure 4.2 Jitter tolerance mask

4.3 Jitter Tolerance Analysis

Several methods have presented analysis for jitter tolerance of bang-bang CDR circuits [1,29,34,42]. We will focus our analysis on Walker and Lee et al.'s methods only. In the following sections we will examine in detail the jitter tolerance derivation for the second order bang-bang PLL loop.

4.3.1 Method 1

As mentioned in chapter 3, Walker made a useful analogy with Delta modulator to model the second order bang-bang PLL loop. A straight forward modelling of second order bang-bang PLL loop is illustrated in figure 4.3. We note that the model used is based on second order Delta-Sigma Modulator with prediction, where Delta-Sigma Modulator is a Delta Modulator with an integrator placed at the input. The transfer function for the loop from the quantizer output back to the quantizer input is:

$$\theta_{tI} = \left(\omega_{in} - V_{\theta}.\left(\beta + \frac{\alpha}{s}\right).K_v\right).\frac{1}{s} \qquad 4.1$$

$$\theta_{tI} = \frac{\omega_{in}}{s} - V_{\theta} \cdot \left(\beta + \frac{\alpha}{s}\right) \cdot \frac{K_v}{s} \tag{4.2}$$

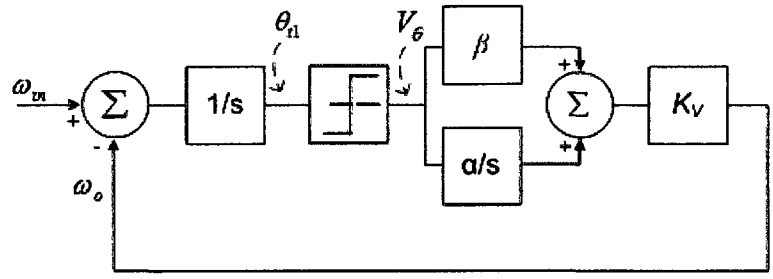


Figure 4.3 Second order bang-bang block diagram I

We can write another transfer function, H_I, for the loop from the input, ω_{in}, to the output, ω_o, as

$$H_I(s) = \frac{\omega_o}{\omega_{in}} = \frac{\frac{1}{s}\left(\beta+\frac{\alpha}{s}\right)K_v}{1+\frac{1}{s}\left(\beta+\frac{\alpha}{s}\right)K_v} \tag{4.3}$$

$$H_I(s) = \frac{\beta K_v + \frac{\alpha K_v}{s}}{s+\beta K_v + \frac{\alpha K_v}{s}} \tag{4.4}$$

$$H_I(s) = \frac{s\beta K_v + \alpha K_v}{s^2 + s\beta K_v + \alpha K_v} \tag{4.5}$$

$$H_I(s) = \frac{s\beta K_v}{s^2 + s\beta K_v + \alpha K_v} + \frac{\alpha K_v}{s^2 + s\beta K_v + \alpha K_v} \tag{4.6}$$

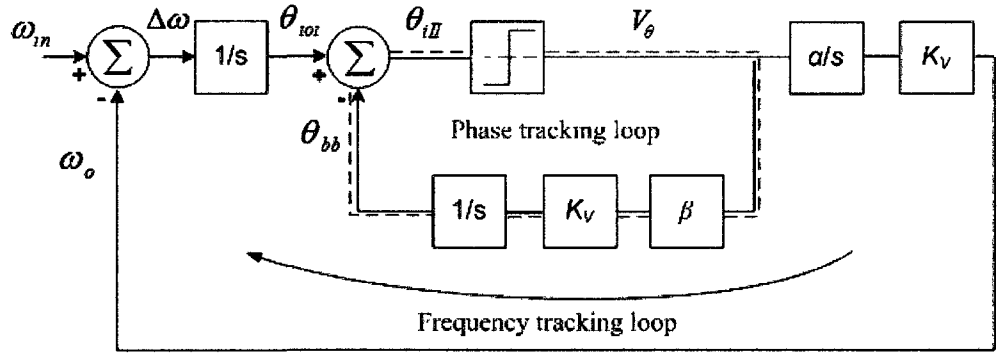
We note that the transfer function consists of two rational functions since we have two paths. The first rational function refers to the proportional path while the second rational function refers to the integral path. The output frequency, ω_o, is the summation of the proportional and the integral frequency steps, therefore:

$$\omega_o = \omega_{bb} + \omega_{int} = \beta K_v + \frac{\alpha K_v}{s} \tag{4.7}$$

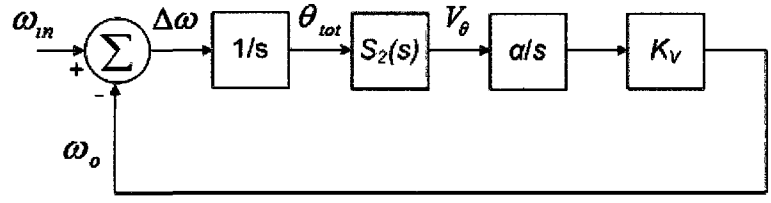
Walker rearranged figure 4.3 to establish a better understanding of the loop by creating an inner phase tracking loop and an outer frequency tracking loop, as shown in figure 4.4 (a). Although some signals do not represent actual physical signals, the arrangement is still useful in understanding the operation of the bang-bang loop. To verify the equivalence of the block diagram in figure 4.4 and the block diagram in figure 4.3, we write the transfer function. The transfer function for the loop in figure 4.4(a) from the output of the quantizer block back to the input of the quantizer is

$$\theta_{tII} = \left(\omega_{in} - V_\theta . \frac{\alpha K_v}{s}\right) . \frac{1}{s} - V_\theta \frac{\beta K_v}{s} \qquad 4.8$$

$$\theta_{tII} = \frac{\omega_{in}}{s} - V_\theta . \left(\frac{\alpha}{s} + \beta\right) . \frac{K_v}{s} \qquad 4.9$$



(a)



(b)

Figure 4.4 (a) Block diagram II (a) Simplified block diagram II

Both transfer functions in equations 4.2 and 4.9 are the same, making both block diagrams equivalent. The inner loop in block diagram II is a first order Delta Modulator (DM) where the input to the loop is a phase signal. By linearizing the quantizer we can write the transfer function for the first order DM as in equation 4.10.

$$H_{inner} = \frac{V_\theta}{\theta_{tot}} = \frac{1}{1+{}^{\beta K_v}/_{s}} \tag{4.10}$$

From the simplified block diagram II in figure 4.4 (b) we can write the transfer function for the outer frequency tracking loop from the input, ω_i, to the output, ω_{int}, as

$$H_{int}(s) = \frac{\omega_{int}}{\omega_{in}} = \frac{H_{inner}\,{}^{\alpha K_v}/_{s}}{s+H_{inner}\,{}^{\alpha K_v}/_{s}} \tag{4.11}$$

Substituting the expression of H_{inner} from equation 4.10 into the transfer function in 4.11 and simplifying gives us

$$H_{int}(s) = \frac{\omega_{int}}{\omega_{in}} = \frac{\alpha K_v}{s^2+s\beta K_v+\alpha K_v} \tag{4.12}$$

This is the same expression for the integral path as in equation 4.6. We can write an expression for the proportional path as well from the input to the phase step, θ_{bb}, as

$$\theta_{bb} = \left(\omega_{in} - \theta_{bb}\cdot\frac{s}{\beta K_v}\cdot\frac{\alpha K_v}{s}\right)\cdot\frac{1}{s} - \theta_{bb}\frac{s}{\beta K_v} \tag{4.13}$$

$$\theta_{bb} = \frac{{}^{\omega_{in}}/_{s}}{(1+\frac{\alpha}{s\beta}+\frac{s}{\beta K_v})} \tag{4.14}$$

$$\frac{\theta_{bb}}{\omega_{in}} = \frac{1}{(s+\frac{\alpha}{\beta}+\frac{s^2}{\beta K_v})} \tag{4.15}$$

$$\frac{\theta_{bb}}{\omega_{in}} = \frac{\beta K_v}{s\beta K_v+\alpha K_v+s^2} \tag{4.16}$$

$$H_{bb}(s) = \frac{\omega_{bb}}{\omega_{in}} = \frac{\theta_{bb}\,s}{\omega_{in}} = \frac{s\beta K_v}{s^2+s\beta K_v+\alpha K_v} \tag{4.17}$$

Since the total frequency step consists of the proportional and integral steps, we can add the two steps together in block diagram II to get the total step by adding 4.12 and 4.17 we get:

$$H_{II}(s) = H_{bb}(s) + H_{int}(s) \tag{4.18}$$

$$H_{II}(s) = \frac{\omega_o}{\omega_{in}} = \frac{s\beta K_v}{s^2+s\beta K_v+\alpha K_v} + \frac{\alpha K_v}{s^2+s\beta K_v+\alpha K_v} \tag{4.19}$$

Comparing the transfer functions H_I in equation 4.6 and H_{II} from equation 4.19, we conclude that both block diagrams I and II are equivalent.

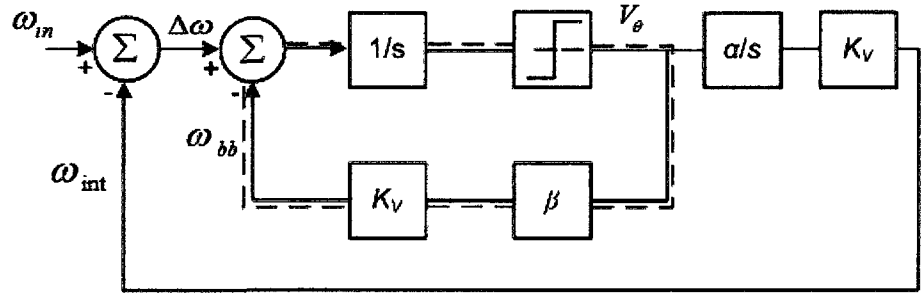


Figure 4.5 Second order bang-bang block diagram III

A third block diagram was introduced by Walker by pulling two integrators through the last summation node before the quantizer, as shown in figure 4.5. The inner loop with dotted line shows a first order delta-sigma modulator with a frequency signal as an input. Writing the transfer function for the loop as before, we can show that block diagram III is equivalent to the first two blocks. The transfer function for the loop from the input to the output, ω_{int}, is

$$H_{int}(s) = \frac{\omega_{int}}{\omega_{in}} = \frac{(\frac{1/s}{1/s+\beta K_v})\alpha K_v/s}{1+(\frac{1/s}{1/s+\beta K_v})\alpha K_v/s} \tag{4.20}$$

$$H_{int}(s) = \frac{\alpha K_v}{s^2+s\beta K_v+\alpha K_v} \tag{4.21}$$

This is the same expression for the integral path as in 4.12. We can write an expression for the proportional path as well from the input to the frequency step, ω_{bb}, as

$$\omega_{bb} = \left(\omega_{in} - \omega_{bb}.\frac{1}{\beta K_v}.\frac{\alpha K_v}{s}\right) - \omega_{bb}\frac{s}{\beta K_v} \quad 4.22$$

$$\omega_{bb} = \frac{\omega_{in}}{\left(1+\frac{\alpha K_v}{s\beta K_v}+\frac{s}{\beta K_v}\right)} \quad 4.23$$

$$H_{bb}(s) = \frac{\omega_{bb}}{\omega_{in}} = \frac{s\beta K_v}{s^2+s\beta K_v+\alpha K_v} \quad 4.24$$

Again, this is the same expression for the proportional path as in 4.17. We will use block diagram III to derive an expression for the jitter tolerance. In Walker analysis the loop quantizer is replaced by a unity gain element. This remains valid as long as there is no slew rate limiting. The analysis is based on slope overload condition from the DM theory. The system slope overloads when $|\Delta\omega| > \omega_{bb}$. Assuming the input signal is equal to the input frequency plus jitter, where $\omega(s) = \omega_{in} + s*\theta(t)$, then writing a transfer function for block diagram III, we get:

$$\Delta\omega = \frac{\omega(s)}{1+\left(\frac{\alpha K_v}{s}\right)\left(\frac{1}{s+\beta K_v}\right)} \quad 4.25$$

To get the maximum input phase as a function of frequency, we solve for $\omega(s)/s$ and substitute $\Delta\omega = \omega_{bb}$.

$$JTol_w(s) = \frac{\omega(s)}{s} = \frac{\beta K_v}{s} + \frac{\alpha\beta {K_v}^2}{s^2(s+\beta K_v)} \quad 4.26$$

$$JTol_w(s) = \frac{\beta K_v s^2+\beta^2 {K_v}^2 s+\alpha\beta {K_v}^2}{s^2(s+\beta K_v)} \quad 4.27$$

Equation 4.27 is identical to Walker's expression for jitter tolerance. However, in the next section we will further simplify this expression.

4.3.2 Proposed expression for jitter tolerance

In this section a simplified expression for jitter tolerance is derived. First we analyze equation 4.27 by partial fractions,

$$JTol_w(s) = \frac{\beta K_v - \alpha/\beta}{s} + \frac{\alpha K_v}{s^2} + \frac{\alpha/\beta}{(s+\beta K_v)} \quad 4.28$$

The third rational polynomial can be ignored since we know that:

$$\frac{\beta K_v}{2\pi} \gg \frac{\alpha}{\beta} \quad 4.29$$

The left-hand side represents the (small-signal) –3dB bandwidth of the loop (for a relatively large damping factor) while the right-hand side is equal to the closed-loop zero. Since the loop bandwidth is typically much greater than the closed-loop zero, the above assumption is valid [2]. We use this approximation to simplify the jitter tolerance expression in 4.28 to yield:

$$JTol = \frac{\beta K_v}{s} + \frac{\alpha K_v}{s^2} \quad 4.30$$

A plot of the exact and simplified jitter tolerance expressions is shown in figure 4.6. Table 3.2 was used to calculate the values for β and α and plot figure 4.6. It is clear that our approximation is valid under the condition we mentioned in equation 4.29.

It is interesting to show that if we remove the integral path, which means α tends to zero, the block diagram tends to a first order DM and the jitter tolerance expression becomes:

$$JTol_{1st\ order} = \frac{\beta K_v}{s} \quad 4.31$$

Equation 4.31 is the slope overload condition for a first order DM [38].

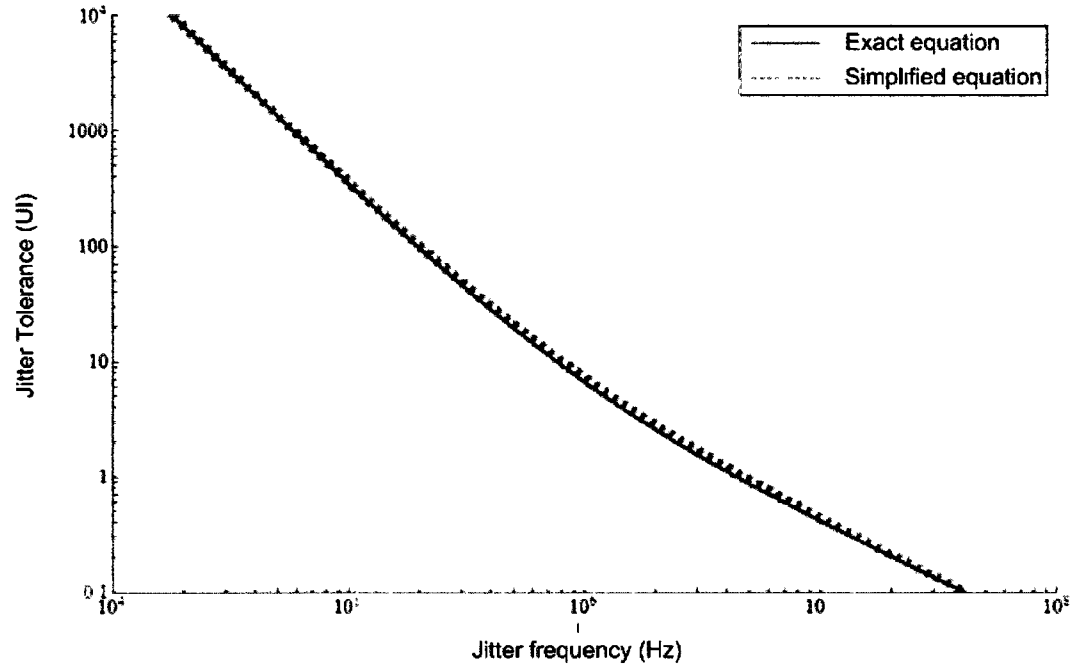


Figure 4.6 Jitter tolerance curve for Walker equation

We can rewrite the expression in 4.30 as in equation 4.32. The maximum tolerable sinusoidal input jitter in 4.32 has the characteristic of a single integrator which falls off at –20dB/decade, followed by an integrator with phase lead prediction, as shown in figure 4.7. The frequency between the two slopes can be found as in 4.33

$$JTol = \beta K_v \left[\frac{{}^{\alpha}/_{\beta} + s}{s^2}\right] \qquad 4.32$$

$$\omega_2 = \frac{\alpha}{\beta} \qquad 4.33$$

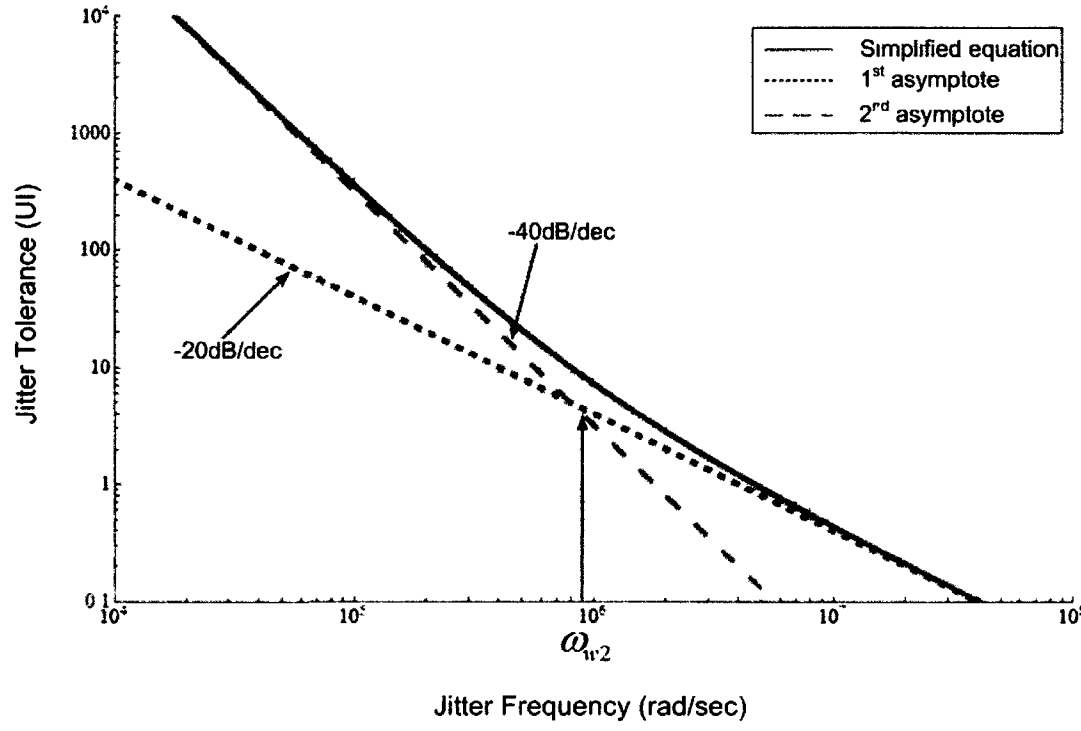


Figure 4.7 Jitter tolerance curve showing two regions

4.3.3 Method 2

An expression for jitter tolerance describes the maximum input jitter magnitude that a CDR circuit can tolerate with a low BER usually of order 10^{-12}. BER increases rapidly when the phase error is larger than π. In other words, when the clock and data are 90 degrees out of phase, which can be expressed as $\theta_{in} - \theta_{out} = \pi$.

In this analysis, the jitter tolerance curve is divided into two regions, as shown in figure 4.8. Region I represents the high frequency part of the jitter tolerance curve and it is assumed the voltage drop on the loop filter is mainly due to the resistor, leading to an output phase waveform of a triangular shape. At very high frequencies, the maximum allowable input jitter is 0.5UI, resulting in a flat region in the jitter tolerance curve. As the jitter frequency decreases, the CDR circuit can tolerate more jitter resulting in a jitter

tolerance curve with a slope of –20dB/dec. As the frequency continuous to decrease, we move to region II where the voltage drop on the capacitor gets larger in comparison to the resistor resulting in a parabolic shaped output phase.

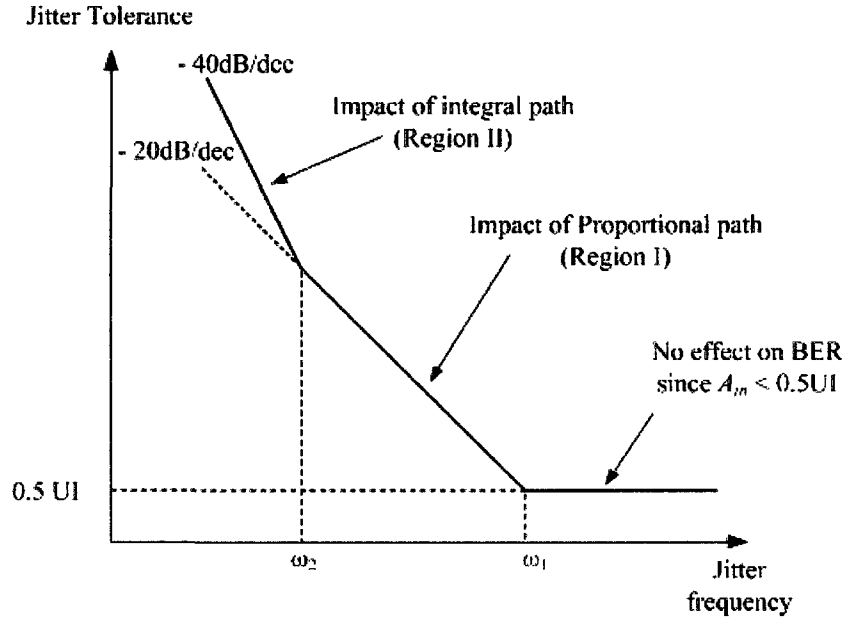


Figure 4.8 Jitter tolerance curve

Figure 4.9 illustrates an extreme case of jitter tolerance in region I. In this case the input jitter is defined as $\theta_{in} = A_{in}\ cos(\omega_j+\delta)$, where the input is offset by an angle δ. Angle δ is an arbitrary angle that makes the maximum amplitude of the output phase signal occurs at time $t = 0$. An expression for the output amplitude at time $t = 0$ is given by Equation 4.34.

$$A_{out} = \beta K_v . \frac{T_J}{4} = A_{in} . \cos(\delta) \qquad 4.34$$

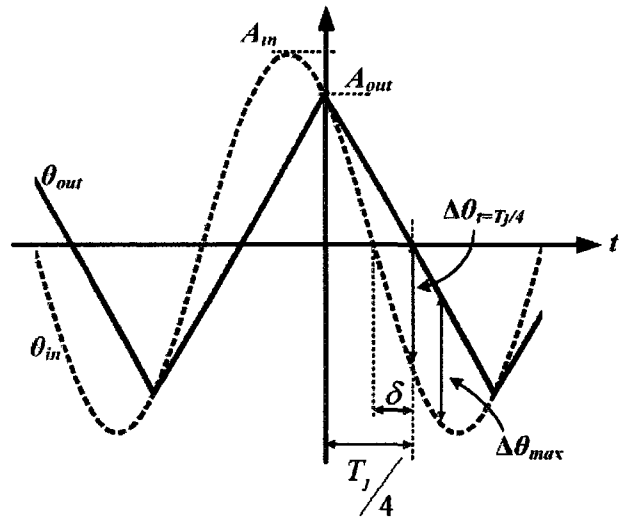


Figure 4.9 Waveforms used to determine the jitter tolerance response

Equation 4.34 can be reworked as in Equations 4.35, 4.36 and 4.37.

$$\cos(\delta) = \frac{\pi\beta K_v}{2\omega_J A_{in}} \tag{4.35}$$

$$\sin(\delta) = \sqrt{\frac{A_{in}^2 - \left(\frac{\pi\beta K_v}{2\omega_J}\right)^2}{A_{in}^2}} \tag{4.36}$$

$$\sin(\delta) = \sqrt{\frac{4\omega_J^2 A_{in}^2 - \pi^2\beta^2 K_v^2}{4\omega_J^2 A_{in}^2}} \tag{4.37}$$

Dividing Equation 4.37 by Equation 4.35 results in an expression for *tan*(δ), which is given by Equation 4.38.

$$\tan(\delta) = \frac{\sqrt{4\omega_J^2 A_{in}^2 - \pi^2\beta^2 K_v^2}}{\pi\beta K_v} \tag{4.38}$$

It is difficult to find an exact expression for the maximum phase error ($\Delta\theta_{max}$) shown in figure 4.9. We can approximate $\Delta\theta_{max} \approx \Delta\theta_{t=Tj/4}$ as it almost leads to the same result but it is easier to derive $\Delta\theta_{t=Tj/4}$ mathematically [29]. The jitter tolerance is defined

where $\Delta\theta_{max} = \pi$, and as such Equation 4.39 provides an expression when the maximum phase error is equation to π.

$$\Delta\theta_{max} \approx \Delta\varphi_{t=\frac{T_J}{4}} = \left|A_{in}.\cos\left(\frac{\pi}{2}+\delta\right)\right| = |A_{in}.\sin(\delta)| = \pi \tag{4.39}$$

We can eliminate the angle δ by substituting equation 4.37 into equation 4.39.

$$\Delta\theta_{max} = A_{in}.\sqrt{\frac{4\omega_J{}^2A_{in}{}^2-\pi^2\beta^2K_v{}^2}{4\omega_J{}^2A_{in}{}^2}} = \pi \tag{4.40}$$

With some manipulation an expression for the jitter tolerance, for region I, in terms of the input jitter frequency and βK_v is given in Equation 4.42.

$$A_{in} = \sqrt{\frac{(2\pi\omega_J)^2+\pi^2\beta^2K_v{}^2}{4\omega_J{}^2}} \tag{4.41}$$

$$Jtol_1 = A_{in} = \pi\sqrt{1+\frac{\beta^2K_v{}^2}{4\omega_J{}^2}} \tag{4.42}$$

Writing the jitter tolerance in terms of UI instead of radians gives us,

$$Jtol_1 = 0.5\sqrt{1+\frac{\beta^2K_v{}^2}{4\omega_J{}^2}} \tag{4.43}$$

Equation 4.43 again illustrates the response of the loop at high frequencies. For very high input jitter frequencies the maximum magnitude of input jitter is equal to 0.5UI. However as the input jitter frequency decreases the loop gains the ability to handle large magnitudes, increasing at a rate of 20dB/dec. This is the same response as a first order loop. The corner frequency will occur when Equation 4.42 is equated to $\sqrt{2}\pi$. This in turn allows the calculation of the corner frequency, as shown in Equation 4.45.

$$Jtol_1 = \sqrt{2}\pi = \pi\sqrt{1+\frac{\beta^2K_v{}^2}{4\omega_J{}^2}} \tag{4.44}$$

$$\omega_1 = \frac{\beta K_v}{2} \qquad 4.45$$

Figure 4.10 illustrates the frequency response of the simple first order binary phase detector. By changing the value of βK_v a designer can alter the system response in order to achieve the desired performance.

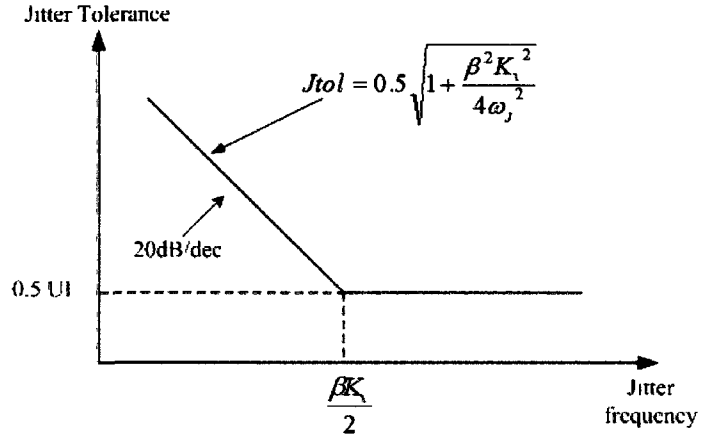


Figure 4.10 The jitter tolerance response of the first order loop

So far we have presented the analysis for the jitter tolerance curve in region I. The analysis has followed the same assumption we mentioned in figure 4.9, that is the change in the control voltage is due to the proportional path and the voltage from the integral path is negligible. As the jitter frequency decreases below $(\beta/\alpha)^{-1}$, the voltage from the integral path becomes comparable to the proportional path resulting in a nonlinear slewing at the output. A parabolic shape for the output phase is observed at very low jitter frequencies, as shown in figure 4.11.

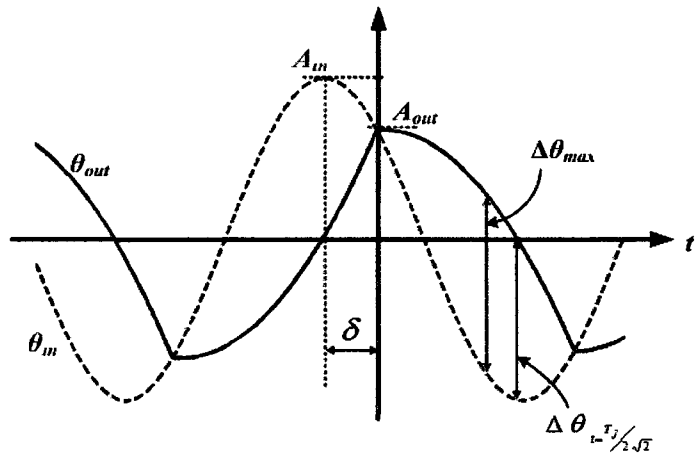


Figure 4.11 Waveforms showing the integral response provided by the capacitor

The input jitter is defined as $\theta_{in} = A_{in}\, cos(\omega_J+\delta)$, where the input is offset by angle δ so that the maximum amplitude of the output phase signal would occur at time $t = 0$. An expression for the output amplitude at time $t = 0$ is given by Equation 4.46.

$$A_{out} = \frac{\pi^2 K_v \alpha}{4\omega_J{}^2} = A_J.\cos(\delta) \qquad 4.46$$

Equation 4.46 can be reworked as in Equations 4.47, 4.48 and 4.49.

$$\cos(\delta) = \frac{\pi^2 K_v \alpha}{4\omega_J{}^2 A_J} \qquad 4.47$$

$$\sin(\delta) = \sqrt{\frac{A_J{}^2 - \left(\frac{\pi^2 K_v \alpha}{4\omega_J{}^2}\right)^2}{A_J{}^2}} \qquad 4.48$$

$$\sin(\delta) = \sqrt{\frac{16\omega_J{}^4 A_J{}^2 - \pi^2 K_v{}^2 \alpha^2}{16\omega_J{}^4 A_J{}^2}} \qquad 4.49$$

It is difficult to find an exact expression for the maximum phase error ($\Delta\theta_{max}$) shown in figure 4.11. We can approximate $\Delta\theta_{max} \approx \Delta\theta_{t\,=\,T_J/2\sqrt{2}}$ as it almost leads to the same result but it is easier to derive $\Delta\theta_{t\,=\,T_J/2\sqrt{2}}$ mathematically [29]. The jitter tolerance is

defined where $\Delta\theta_{max} = \pi$, and as such Equation 4.50 provides an expression when the maximum phase error is equation to π.

$$\Delta\theta_{max} \approx \Delta\theta_{t=\frac{T_J}{2\sqrt{2}}} = \left|A_j.\cos\left(\omega_J \frac{T_J}{2\sqrt{2}} + \delta\right)\right| \quad 4.50$$

$$\Delta\theta_{max} \approx -A_j.\cos\left(\frac{\pi}{\sqrt{2}}\right)\cos(\delta) + A_j.\sin\left(\frac{\pi}{\sqrt{2}}\right)\sin(\delta) \quad 4.51$$

We can eliminate the angle δ by substituting equations 4.47 and 4.49 into equation 4.51.

$$\Delta\theta_{max} = 0.61\frac{\pi^2 K_v \alpha}{4{\omega_J}^2} + 0.8\sqrt{\frac{16{\omega_J}^4 {A_J}^2 - \pi^4 {K_v}^2 \alpha^2}{16{\omega_J}^4}} = \pi \quad 4.52$$

With some manipulation an expression for the jitter tolerance, for region II, in terms of the input jitter frequency and the $K_v\alpha$ is given in Equation 4.53.

$$Jtol_2 = A_J = \sqrt{\frac{\left(\pi - 0\,61\frac{\pi^2 K_v \alpha}{4{\omega_J}^2}\right)^2}{0\,64} + \frac{\pi^4 {K_v}^2 \alpha^2}{16{\omega_J}^4}} \quad 4.53$$

Since at very low frequencies we have,

$$\pi \ll 0.61\frac{\pi^2 K_v \alpha}{4{\omega_J}^2} \quad 4.54$$

Expression 4.53 can be simplified to give the jitter tolerance equation for region II as

$$Jtol_2 = 1.26\frac{\pi^2 K_v \alpha}{4{\omega_J}^2} \quad 4.55$$

Equation 4.55 again illustrates the response of the loop at low frequencies. The jitter tolerance amplitude decreases at a rate of –40dB/dec with increasing frequencies until it intersects with region I. The corner frequency can be found between the two regions by equating equations 4.42 and 4.55 as shown in Equation 4.57.

$$\pi\sqrt{1+\frac{\beta^2 {K_v}^2}{4{\omega_J}^2}} = 1.26\frac{\pi^2 K_v \alpha}{4{\omega_J}^2} \quad 4.56$$

$$\omega_2 = 0.63\pi\frac{\alpha}{\beta} \quad 4.57$$

4.4 Jitter Tolerance Simulation

We have presented the theoretical analysis so far and derived expressions for jitter tolerance. In this section we will simulate the jitter tolerance to verify the expressions we presented. An efficient test bench will be presented based on Simulink. Behavioural simulation is being increasingly used in order to verify design at a system level.

Two test benches are used, transient and phase-domain simulations. While transient simulation imitates a real CDR circuit, it is very slow when the CDR circuit speeds are in Gb/s range. Transient simulation will be used for relatively high frequency (above 10KHz), as below that the simulation becomes extremely slow. For example, to achieve a BER below 10^{-12}, typically simulation is required to run to gather hundred of errors. Therefore it is required to run the simulation for 10^{14} cycles. With a simulation rate of 10Mcycles/sec, approximately 115 days would still be needed to accumulate the required number of errors [42]. On the other hand, phase domain models are formulated in terms of the phase of the signals. The Phase of a signal is determined by a process of averaging. Therefore, phase domain models are used to achieve faster simulations.

We will discuss the transient simulations in section 4.4.1, then we will present phase domain simulation in section 4.4.2.

4.4.1 Transient Simulation

The jitter tolerance test bench for transient simulation is shown in figure 4.12. The test bench was based on the work presented by Ahmed et al. [49]. However, we implemented the simulation using Simulink for faster simulation.

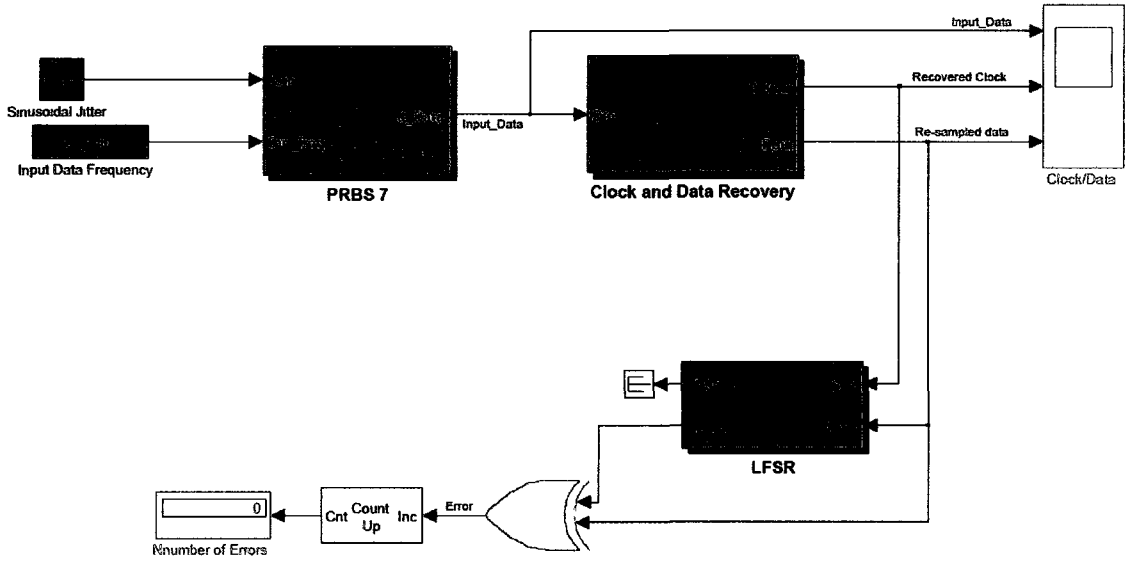


Figure 4.12 Test bench for Jitter tolerance simulation

A sinusoidal jitter signal with a known amplitude, A_m, and frequency, ω_j, is used to phase modulate a clock that drives the PRBS (Pseudo-Random Bit Sequence), as shown in figure 4.13. A phase modulator is implemented to phase modulate the clock signal with the input jitter. The phase modulator is a direct implementation of a jittered clock, as in equation 4.58.

$$x(t) = \sin(\omega t + A_j sin(\omega_j t)) \qquad 4.58$$

The Linear Feedback Shift Register (LFSR) implemented has two inputs, CLK and Data, and two outputs, LFSRout and XNORout. The XNORout is connected to the input

Data and our output is taken from LFSRout. The LFSR is designed using 7 D flip-flops and one XNOR gate, as shown in figure 4.14. Initially all the output from the flip-flops are zero and as a result if we use XOR gate then the LFSR never starts and will be stuck in the zero state.

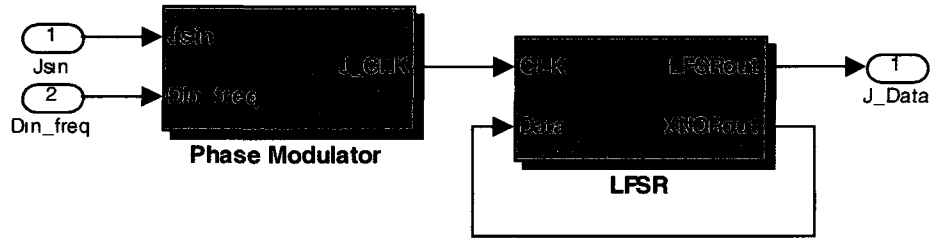


Figure 4.13 PRBS7 with sinusoidal input jitter

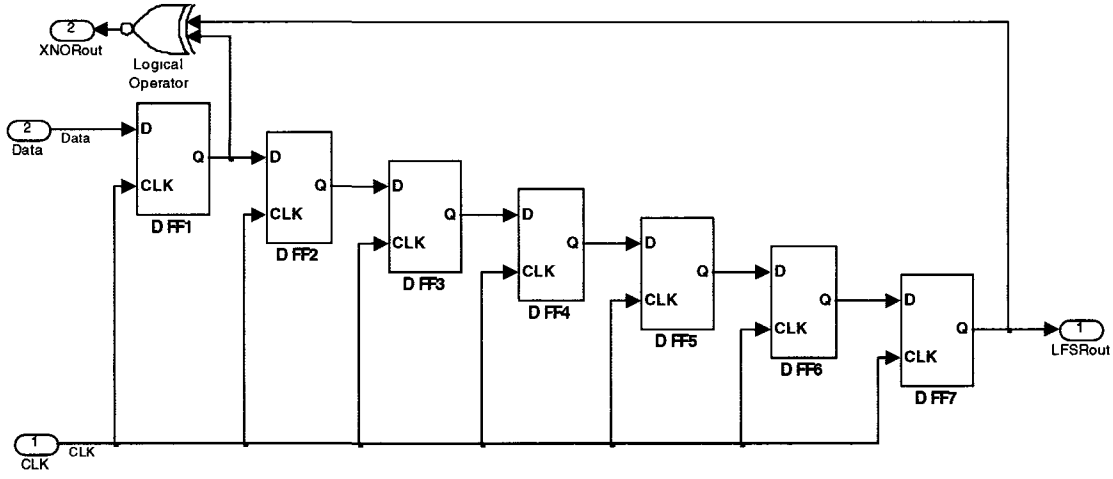


Figure 4.14 Linear Feedback Shift Register

The jittered data is transferred to the CDR model shown in figure 4.15. This is a typical second order bang-bang CDR circuit which we used in our analysis. The phase detector is an implementation of Alexander PD shown in figure 2.8.

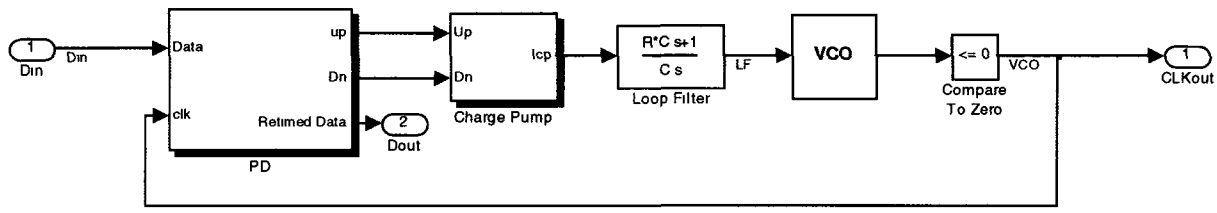


Figure 4.15 Second order bang-bang CDR circuit used in Simulation

The recovered data, which is usually delayed by 0.5UI, is compared with the original data to detect errors. We use the same method of Bit Error Rate Testers (BERTs) that involves setting up a replica-LFSR at the recovered data output. The recovered data (DOUT) is connected at its input as shown in Fig. 4.16. As the recovered bits arrive, the two LFSRs acquire the same state if correct bits are being received. In case of an erroneous bit entering the replica-LFSR, its output becomes different from that of the input-LFSR. The XOR gate at the output detects this error and runs a counter to count the bit errors. The amplitude of the JSIN signal has to be reduced until there are no errors at a particular jitter frequency during several cycles of the jitter sinusoid. The design parameters used in the simulation are summarized in table 4.1.

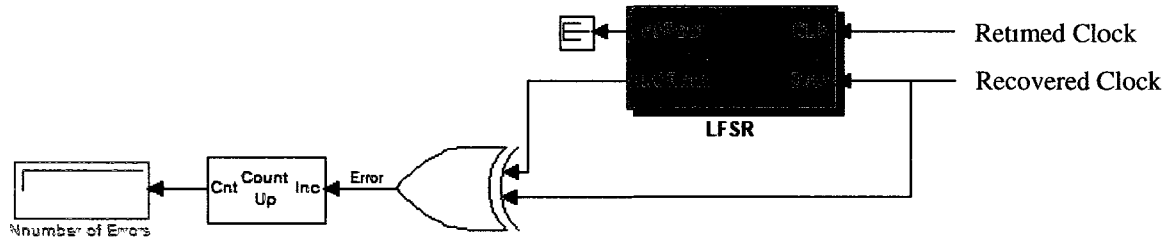


Figure 4.16 BER error detection.

Table 4.1 Design parameters for CDR circuit

Bit rate (GHz)	4
VCO gain, K_V (rad/V.s)	1.26×10^9
Charge Pump Current, I (μA)	40
Loop filter resistance, R (Ω)	500
Loop Filter Capacitor, C (nF)	0.5
$\beta = IR$ (V)	0.02
$\alpha = I / C$ (V/sec)	8×10^4

Figure 4.17 shows the jitter tolerance simulation along with theoretical results from Walker and Lee et al. As was explained in chapter 3, the main difference between Walker and Lee et al.'s methods lies in the phase error. In slope overload analysis, the phase error is assumed zero, while in Lee et al.'s method the maximum phase error is 0.5UI. As a result, there is a shift in Walker's curve to the right.

Two interesting points are worth mentioning from the simulation results. First, the amplitudes of the jitter in the simulation results are slightly smaller than the amplitudes of the jitter from the theoretical results as jitter tolerance expressions did not take into account transition density. In other words, since we are using PRBS7 in our simulations, we should expect more errors because there are fewer edges. This can be seen clearly in the flat region of the curve where the simulated jitter tolerance amplitude is 0.4UI. Second, there is a gap between the simulation and theoretical results in region II. In order to explain this gap, we need to look in more details at what is happening in this region by using phase simulation to observe the input and output jitter phases.

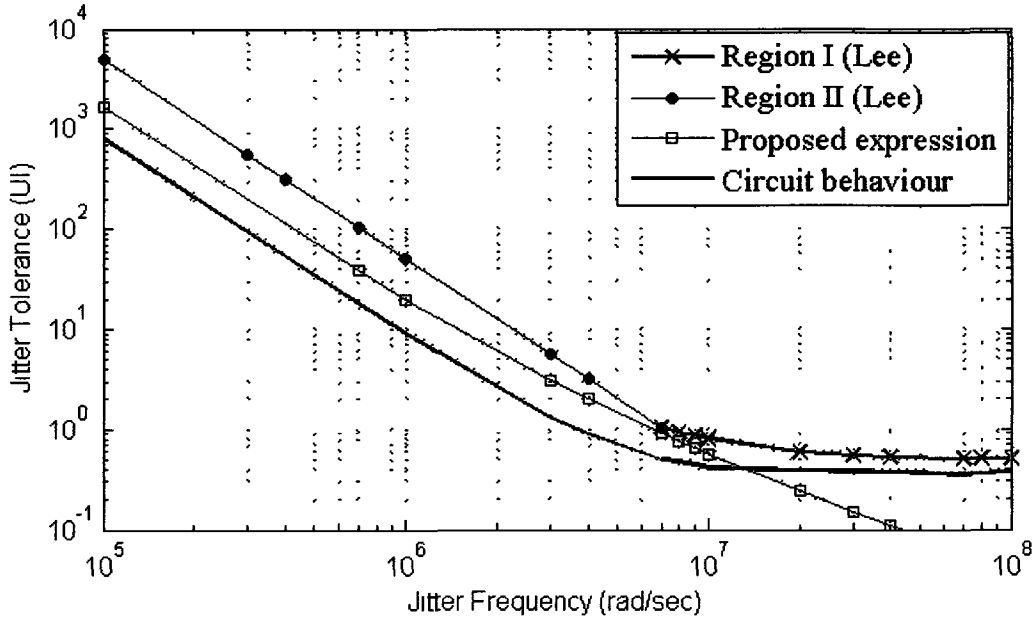


Figure 4.17 Simulated and derived jitter tolerance curve

4.4.2 Phase domain Simulation

We used the same test bench we used for jitter transfer simulation, shown in figure 4.18. The input is a sinusoidal jitter signal with frequency ω_j and amplitude A_{in}. At a given frequency, ω_j, the amplitude of the input jitter is increased until a phase error of 0.5UI is achieved.

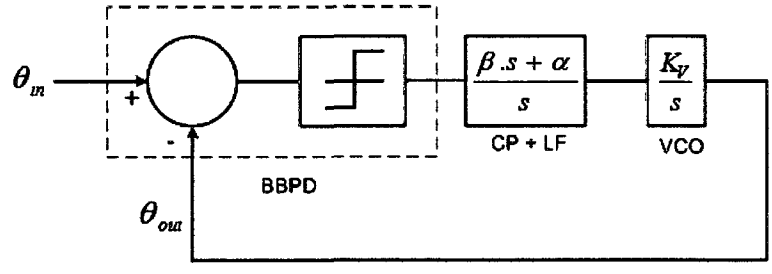


Figure 4.18 Phase domain model testbench

Figure 4.19 shows the phase-domain behavioural simulation for jitter tolerance. The lower curve represents the circuit behaviour, while the upper curves represent equations

4.30, 4.43 and 4.55 for our proposed expression, region I, and region II respectively. Unlike the time-domain simulations, the phase-domain simulation matches the expression 4.43 in the flat region of the curve. As explained before the matched results were expected since there is no PRBS implemented in the phase-domain testbench. Next we will explain the gap between circuit behaviour and theory by looking at the input and output phase signals at the three specified frequencies shown in figure 4.19.

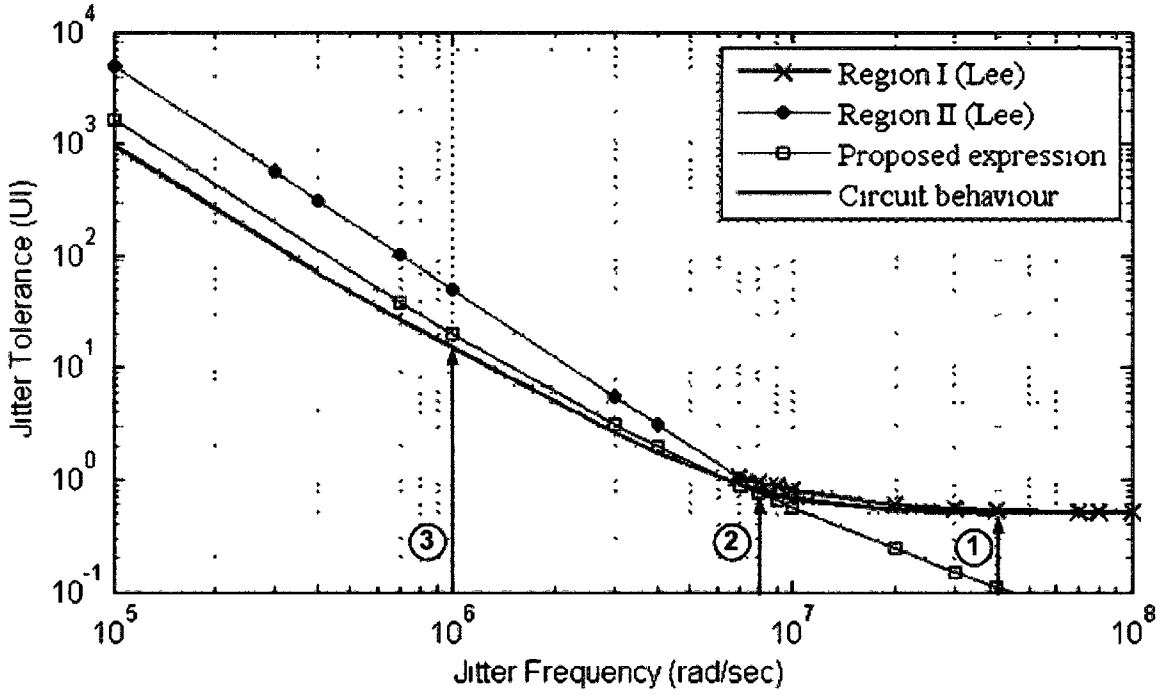


Figure 4.19 Jitter tolerance curve from phase-domain simulation

The first frequency point shown in figure 4.19 is ω_j=4x10^7 rad/sec and it lies in the flat portion of region I. The amplitude is increased until a phase error of 0.5UI occurs. The maximum amplitude that will cause an error of less than 0.5UI is 0.5UI, as expected. Figure 4.20 shows the simulation results for the input and output jitter. We notice that

the voltage drop on the loop filter is mainly from the proportional path, as mentioned before. The capacitor has very little effect in this region.

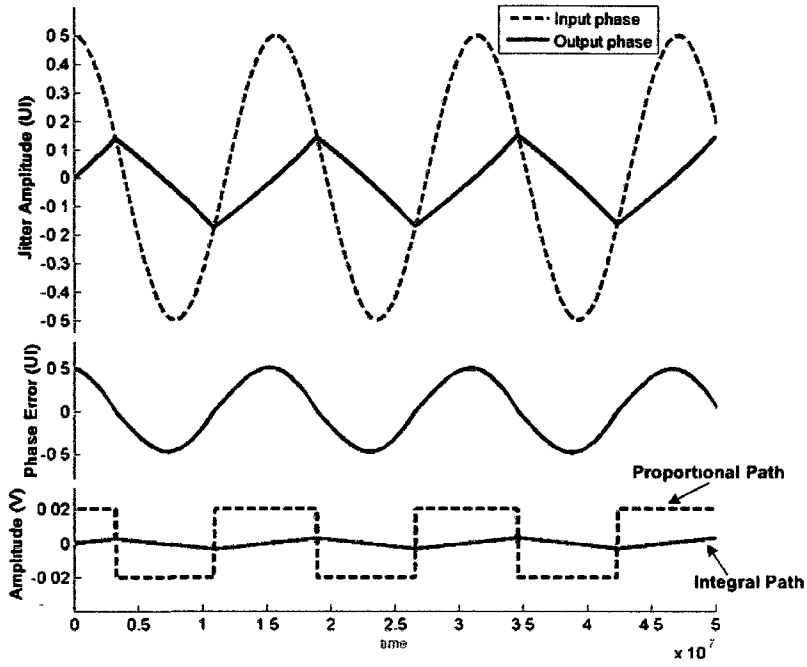


Figure 4.20 Simulation results for an input signal of 0.5UI at high frequencies

Next, we decrease the jitter frequency to ω_j=8x10^6 rad/sec to test the linear part of region I. As shown in figure 4.21, the maximum amplitude that will cause an error of less than 0.5UI is 0.79UI. Unlike the theoretical results, which assumed a triangular output phase, we are seeing a parabolic output. The parabolic shape is a result of the increased effect the capacitor has.

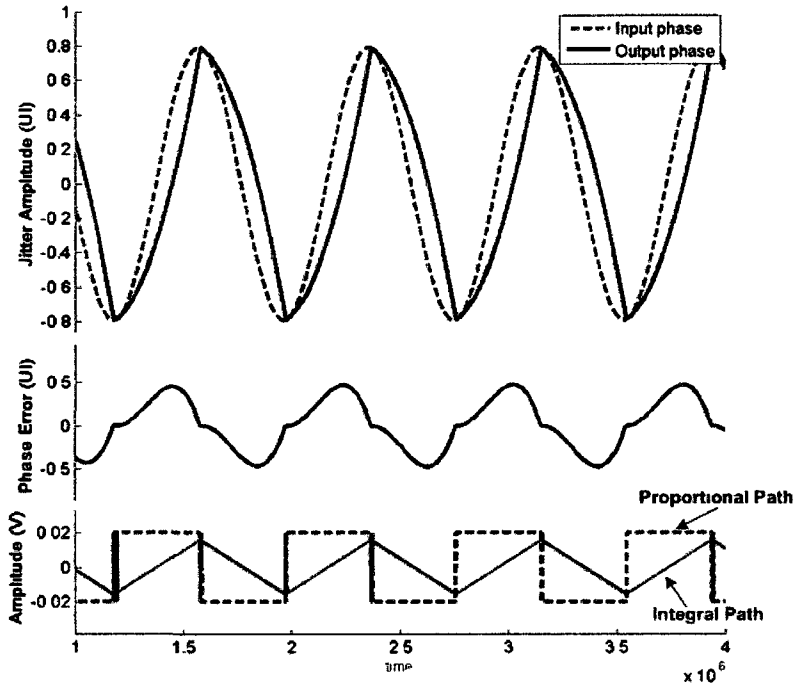


Figure 4.21 Simulation results for an input signal of 0.79UI in Region I

Finally, we decrease the jitter frequency to ω_j=1x10^6 rad/sec to test the output at region II. As shown in figure 4.22, the maximum amplitude that will cause an error of less than 0.5UI is 9.93UI. It is clear that the output phase is not parabolic anymore. The loop takes time to lock before the phase error becomes almost zero. As we slightly increase the input jitter amplitude to 9.94UI we observe that the loop is out of lock, as shown in figure 4.23.

It is obvious from the simulation results in region II that the assumption that the output jitter has a parabolic shape is invalid. In other words, we cannot assume that the VCO control voltage is mainly due to the loop filter capacitor. Although in figures 4.22 and 4.23, the integral path gain is larger than the proportional path gain, we cannot ignore the effect of the proportional path as it is required for loop stability.

In addition, as the jitter amplitude increases, as in region II, the condition stating that the maximum phase error is less than 0.5UI cannot be applied. In this region, the loop either tracks with a very small phase error, or does not track at all and has a very large phase error. Therefore, our proposed expression gives more accurate results in this region in comparison with simulation results because it is based on the slope overload condition.

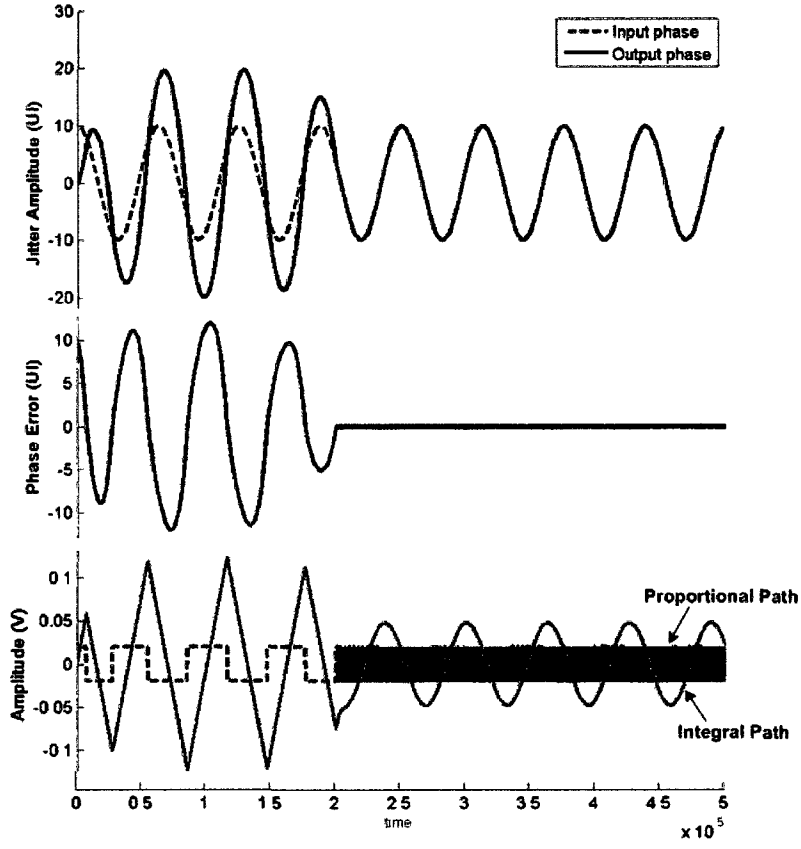


Figure 4.22 Simulation results for an input signal of 9.93UI in Region II

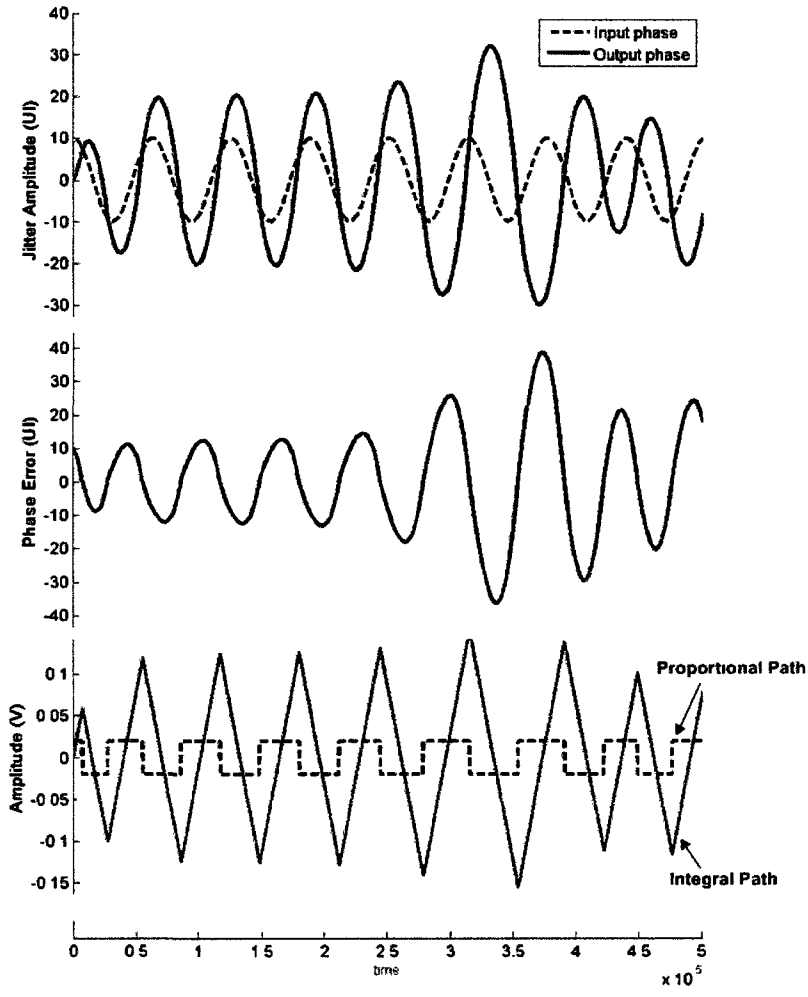


Figure 4.23 Simulation results for an input signal of 9.94UI in Region II

4.5 Summary

We presented the jitter tolerance analysis for second order bang-bang PLL loop. First we presented a detailed analysis of Walker model with manipulation of block diagrams. Based on Walker analysis, a simplified expression for jitter tolerance was proposed. Secondly, we discussed jitter tolerance analysis by Lee et al. Finally, we displayed our results based on phase-domain and time-domain simulation and how they are different from theoretical results.

Chapter 5: Conclusion

5.1 Conclusion

A detailed analysis of jitter transfer and jitter tolerance characteristics of second order bang-bang PLL loop was presented throughout the thesis. Literature review has shown that bang-bang phase detectors are widely used in CDR circuits for high speed serial communications for its superior performance.

A selected number of previous papers modeling and analyzing bang-bang PLL loops for jitter performance were presented. While there has been a number of methods developed to model the loop, no attempt has been made to unify different methods and investigate the variations of the proposed analysis. In chapter two we briefly presented most of the methods used and our analysis was restricted to two main methods, namely Walker's and Lee et al.'s.

Chapter three revolves around the discussion of Walker and Lee et al.'s methods for jitter transfer analysis. Throughout the chapter, the definition of jitter transfer was given according to the standards resulting in a modified expression that complies with the definition. In addition, a phase domain testbench was developed for jitter transfer simulation using Simulink and the simulation results showed favorable agreement with our derived expression.

In chapter 4 we investigated the jitter tolerance analysis presented by Walker and Lee et al. Different block diagrams developed by Walker were accurately analyzed and verified by means of transfer functions. This analysis gave us a better understanding of the dynamics of the loop. Next we presented the jitter tolerance expression derived by Walker and using mathematical tools this expression was simplified further. Walker' analysis was based on Delta Modulator conventional theory while Lee et al.'s method was based on large-signal piecewise-linear model. Lee et al. divided the jitter tolerance curve into two regions depending on the effect of the loop filter capacitor. Jitter tolerance expressions for each region were rederived and verified.

Finally, novel analysis for jitter tolerance was verified using time-domain and phase-domain simulations. Based on simulation results we were able to explain the loop behaviour in each region of the jitter tolerance curve. Although, simulation results showed good agreement with Lee et al.'s theoretical results in region I, in region II the simulation results did not match the theoretical work. On the other hand, a simplified expression based on Walker's method showed close agreement with simulation results in region II.

5.2 Contributions

The understanding of bang-bang PLL loop and related jitter transfer and jitter tolerance characteristics have been enhanced through the following contributions:

- A detailed jitter transfer analysis for Walker and Lee et al.'s work in considerable depth. An expression was proposed that complies with the

definition of jitter transfer. A paper was successfully published in an IEEE conference on this work [45],

- An indepth investigation of the manipulation of Walker's block diagram for second order bang-bang PLL loop. Transfer functions of the block diagrams were used as a tool to show the equivalence of the developed block diagrams,
- The development of a simplified expression for jitter tolerance based on Walker's work, as in equation 4.30,
- A novel analysis explaining the behaviour of the loop in each region of the jitter tolerance curve by means of behavioural simulations. Simulation results showed the shortcomings of Lee et al.'s expression in region II due to invalid assumptions.

5.3 Future Work

There are several ways in which the research presented in this thesis can be further pursued:

- In our analysis we assumed only deterministic jitter; random jitter can be included in the analysis as a practical case,
- The effect of metastability and jitter on bang-bang phase detector response can be further examined,
- The analysis can be extended to include jitter generation and BER as well. Jitter generation and BER are not fully investigated in the literature yet.

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