24 GHz Integrated Differential Antennas in Digital Bulk Silicon

by

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Abstract

In this thesis integrated antennas are investigated with an aim towards balanced-mode receiver front-end implementations in the 24 GHz ISM band. These antennas are realized on a silicon chip with a standard fabrication process, thus making them compact and low cost.

The goal of this thesis is to study the conditions under which standard Si technology can yield efficient ISM band antennas for air transmission. In order to test these differential dipole antennas, integrated balun structures have been implemented and completely characterized. A simple de-embedding technique is developed and verified to extract differential antenna impedance from single ended S-parameters of the dipole plus balun structure. A gain calibration technique is devised to estimate antenna gain on lossy Si substrate.

Measurements of various dipole dimensions on different substrates have been performed to establish the trade-offs between these parameters and achievable antenna performance in terms of impedance and gain. Also, based on the simulation and experimental results, some design guidelines are established along with a methodology and CAD strategy to predict antenna performance on various resistivity substrates. The antenna impedance in the range of 25-100 Ω and gain values from -11 dBi to -2 dBi have been achieved for different antenna geometries, indicating great design flexibility and potential to integrate these antennas into current VLSI technology for wireless communication.

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List of Acronyms and Abbreviations

AUT	antenna under test
BCB	Benzo Cyclo Butene
CAD	computer aided design
CPS	coplanar strips
CPW	coplanar wave-guide
CMOS	complimentary metal oxide semi conductor
DUT	device under test
EMI	electromagnetic interference
FET	field effect transistor
GSG	ground signal ground
GaAs	Gallium arsenide
GHz	giga hertz
HFET	heterojunction field-effect transistor
IC	integrated circuit
ISM	Industrial scientific medical
ISS	Impedance standard substrate
Ka-band	a frequency range of 26.5-40 GHz
LEO	low earth orbiting
LMDS	local multipoint distribution system
LRM	line reflect match
LRRM	line reflect reflect match
MESFET	metal semiconductor field- effect transistor
MMIC	monolithic microwave integrated circuit
NF	noise figure
PCB	printed circuit board
PCS	personal communications systems
PIFA	planar inverted F antennas
RF	radio frequency
SAIS	stand-alone integrated systems
SAT	stand alone transceiver
Si	silicon
SIMMWIC	silicon monolithic millimeter-wave integrated-circuit
SOI	silicon on insulator
SOLR	short open load reciprocal device
SOLT	short open load through
SOS	silicon on sapphire
SWR	standing wave ratio
VCO	voltage-controlled oscillators
VSWR	voltage standing wave ratio
WLAN	wireless local area networks
X-band	the frequency range of 8-12 GHz

Glossary

A	area
γ	propagation constant
λ	any wavelength in general
λ_o	wavelength in free space
λ_g	wavelength in dielectric medium (guided wavelength)
Ω	ohm
α	attenuation constant
β	phase constant
ρ	resistivity
δ	skin depth
σ	conductivity
π	pi
ω	radian frequency
c	speed of light
C_{in}	input capacitance
D	distance between transmit and receive antennas
dB	decibel
dBm	decibel with reference to milli-watt
ϵ	permittivity
ϵ_r	relative permittivity (dielectric constant)
ϵ_o	permittivity of free space
$\epsilon_{r,eff}$	effective dielectric constant of dielectric material
f_c	carrier frequency
f_T	frequency where the short circuit current gain of the transistor is equal to 1
G	gain
G_{ant}	antenna gain
G_{st}	gain of standard antenna
G_{aut}	gain of antenna under test
G_t	transmitter gain
G_r	receiver gain
g_m	transconductance
H	height
K	Boltzman constant
T	temperature
B	bandwidth
L	length
L_s	source inductance
P	power
P_{st}	received power level by standard antenna
P_t	transmitted power
P_r	received power
P_{aut}	received power level by antenna under test

R	resistance
R_{dc}	dc resistance
S	spacing between coplanar strips
S_{21}	transmission gain
S_{11}	input return loss
t	thickness
T	temperature
$\text{Tan } \delta$	loss tangent
T_m	measured transmission parameters
T_p	extracted parameters
μ	permeability
μ_o	permeability of free space
μ_r	relative permeability
V_{DD}	supply voltage
V_{on}	minimum on-voltage for the transistor
W	width
X	reactance
Y	admittance
Z	impedance
Z_L	load impedance
Z_{in}	input impedance
Z_r	receive antenna impedance
Z_s	source impedance
Z_{ant}	antenna impedance
Z_o	characteristic impedance

Chapter 1 Introduction

1.1 Introduction and Motivation

Over the last two decades, the development of printed and other planar antenna components technology has fundamentally changed microwave /millimeter wave communications. Planar antennas, often referred to as integrated antennas, can be printed on substrates with minimal cost and processing. In many new applications, these compact and low profile antennas, which can also be integrated with active devices, offer a practical and inexpensive solution to previously used configurations of waveguide or reflector based antenna systems.

Integrated antennas are highly advantageous for a number of reasons. Firstly, they can be manufactured at a much lower cost than waveguide based antenna technology and are considerably more compact and lightweight. These characteristics are essential for the many commercial applications that planar antennas are increasingly used in, such as base stations for LMDS (local multipoint distribution system), handset antennas, LEO (low earth orbiting) satellite applications and other PCS (personal communications systems) applications. Secondly, the planar nature of these antennas makes them ideal for the large arrays and simplifies the interaction of additional electronics such as amplifiers and phase shifters in applications like electronic warfare, vehicular radar, satellite communication or millimeter wave imaging. Their conformability to a given surface and ease of hybrid and monolithic integration is another important consideration that makes these antennas desirable.

However, many advantages of these antennas are often counterbalanced by low element gain, low efficiency, narrow bandwidth and limited power. Power maybe limited by the thermal

capacity of the substrate materials and efficiency may be lowered by surface waves. However, many antenna characteristics such as radiation, efficiency, bandwidth, input impedance, and radiation pattern can be optimized by a judicious choice of substrate thickness and relative permittivity value.

The 24 GHz ISM (industrial scientific medicine) band is presently attracting considerable attention for applications such as low cost vehicular radar [1], stand-alone integrated systems and system-on-chip (SAIS) [2], wireless local area networks (WLAN) and data communication in industrial environments [3]. This band and the nearby millimeter wave range are very advantageous for the realization of short haul communication systems. The small free space wavelength of a few millimeters allows circuits and components to be realized on semiconductor substrates. Moreover, the use of lower millimeter wave frequency bands (20-40GHz) for wireless point-to-point data links exhibits interesting and unique features, e.g. high available bandwidth and high directivity with small sized antennas. Despite these advantages, this frequency range still suffers from the problem of high design and production cost. Therefore, if the low cost requirement is to be fulfilled it is necessary to minimize the component count of the microwave front end. Integration of the complete transceiver on one single chip of smallest possible dimensions, and the use of Si IC technology, is a possible first step. Such miniaturization is best met through adoption of the integrated antenna concept. Having the antenna integrated on-chip provides several design advantages, including tailoring of the antenna's impedance to avoid matching networks, and eliminating the need for off-chip components.

Monolithic Si integrated antennas have been previously demonstrated, and full integration of antennas with transceivers has been reported in CMOS technology for intra-chip clock distribution [4-6] and air transmission [7]. On the other hand, fully integrated K/Ka band

vehicular radar antenna arrays [1] and 24 GHz transceivers have been demonstrated in printed circuit board format [8] [9]. However, as will be discussed in greater detail in Chapter 2, all of the monolithic antennas either suffer from large physical dimensions, digital CMOS incompatible material, non-standard processing, high transmission loss or limited range.

In addition, the hybrid technology antenna implementations still remain too bulky and expensive to meet emerging ISM application needs. Therefore, further research into standard Si technology-based antenna and transceivers is needed.

1.2 Thesis Objectives

The main goal of this thesis is to investigate conditions under which standard Si technology can yield efficient ISM band antennas for air transmission. The focus is on system-on-chip applications, where antenna structures suitable for balanced-mode receiver front end implementations are desired. The specific thesis objectives are therefore as follows:

Due to the experimental testing requirements of differential mode 24 GHz integrated antennas, a first objective is to develop and characterize appropriate integrated balun structures on Si.

Since the Si antennas to be studied are combined with a balun, a second objective is to develop an appropriate analysis (including CAD) strategy for the integrated antenna and balun structures. A third goal is to devise a suitable de-embedding technique to extract the antenna impedance and gain from the simulated and measured results of the combined antenna/balun structure.

The final objective of this work is to study the effects of key antenna dimensions and material parameters (substrate resistivity) for a candidate radiating element at 24 GHz.

1.3 Thesis Organization

The thesis is divided into five additional chapters. Second chapter provides some background on integrated antennas and the systems based on this concept. It also highlights the growing trends and related applications of this technology.

The third chapter describes the analytical procedure as well as the experimental process of on-chip balun design. It also explains the technique to extract CPS balun characteristic impedance from the measured results.

The fourth chapter discusses the effects of geometry and material properties on the input impedance of integrated dipole. Various trade offs between the design parameters and antenna input impedance have been explained. It also covers the de-embedding technique to extract antenna impedance from simulated and measured S-parameters.

The fifth chapter is a study of the gain of on-chip dipole. A gain calibration technique for on-chip antennas on lossy substrates has been presented.

The sixth chapter concludes the thesis. Some recommendations regarding the future work have been included in this chapter.

Chapter 2 Integrated Antenna Systems and Applications

2.1 Introduction

There has been rapid growth in printed antenna theory and technology during the last two decades. Most of this work has been for antennas operating in the UHF to lower microwave frequency band (300 MHz to 10 GHz), and the characteristics of printed antennas such as low cost, low profile, conformability, and ease of manufacture were found to outweigh the electrical disadvantages such as narrow bandwidth and low power capacity for many applications.

Some of the initial work on a printed antennas has given good guide lines for millimeter wave antenna design and has provided valuable information about general antenna characteristics, resonant frequency, resonant resistance, bandwidth, power loss to surface waves, dielectric losses and antenna efficiency [10]. Furthermore, the effects of substrate thickness, permittivity and power loss to surface waves on printed circuit dipole properties have been investigated in [11][12].

In the recent past a lot of work has been done on millimeter wave systems and applications such as aircraft-to-satellite communications, imaging array antennas and completely monolithic designs which combine antenna elements or arrays on the same substrate as the integrated RF/IF front and detector and amplifier circuits. Currently, integrated antennas are being employed in applications like stand alone integrated systems (SAIS)[2], vehicular radar [1] and intra-chip clock distribution [13].

2.2 Integrated Antennas

With the recent proliferation of wireless technology, the antenna is considered to be one of the key enabling elements. New research areas and applications have emerged. In traditional RF systems and even in modern wireless systems, the antenna is considered as a completely separate entity from the rest of the system. The antenna and RF front end are designed as different components and are connected with each other through a 50 Ω transmission line.

Unlike the conventional approach, the antenna and other components of the RF system may be combined as a single entity in the integrated antenna concept. In addition, the antenna may not only be used as a radiating element but also to provide some passive circuit functions, such as resonator, filter or diplexer.

Several attempts to integrate the antenna with the front-end circuit have been reported, and only a few representative examples are discussed here. In terms of passive circuit integration with antennas, a number of designs have been previously presented. A broadband printed dipole-radiating element with an integrated microstrip balun has been investigated in [14]. A tapered-slot antenna element, designed to be integrated with the active RF beam former units, has been exhibited in [15]. A CPW-fed CPS dipole antenna, which operates at dual frequencies, is presented in [16].

2.2.1 Wireless Clock Distribution through Integrated Antenna

The increase in operating frequency and reduction in die size for CMOS circuits has led to the concept of wireless communications within and between IC's using microwaves. A potential application is wireless clock distribution, proposed as an alternative to distribute high

frequency clock. Wireless interconnects can be used for both data and clock signals. A modulation scheme is, however, required for wireless data whereas the wireless clock only needs a single tone. Therefore, wireless clock distribution has been attempted first for evaluating the potential of wireless interconnects and for developing the key components of this system. It may consist of a clock transmitter, located on or off chip, broadcasting a microwave global clock signal at frequencies around 20 GHz or higher and a grid of integrated clock receivers as shown in Figure 2.1a [13]. The signal picked up by a receiving antenna (R) is divided down to the system clock frequency (~ 2.5 GHz) and locally distributed using a conventional clock tree, as shown in Figure 2.1b. For such systems, development of compact antennas, which can deliver sufficient power to a clock receiver circuit, is essential.

Figure 2.1 (a) Schematic diagram of wireless clock distribution system and (b) clock receiver [13].

Integrated antennas for wireless clock distribution have been investigated for low resistivity silicon substrates (5,10 and 20 $\Omega\text{-cm}$) [5] [13]. Different antenna topologies realized for wireless interconnects system are shown in Figure 2.2 [13]. These antennas have been characterized for transmission through the substrate and the study illustrates that meander dipole exhibits lower transmission loss as compared to the other configurations. A 2mm long and 10 μm wide zigzag dipole antenna pair, separated by a distance of 1 cm, has 56 dB of transmission loss at 18 GHz.

Analysis of different structures of integrated antennas implemented on silicon wafers for intra-chip communication confirms that the primary medium for electromagnetic wave transmission is the silicon substrate [17]. This is verified by computing the speed of electromagnetic waves through phase delay measurements.

Figure 2.2 Microphotographs of (a) linear (b) meander (c) zigzag (d) loop antennas [13].

Similar integrated antennas, designed for wireless interconnect systems, have been compared in performance from 10 to 18 GHz on different Si substrates, such as bulk, SOI and SOS [18]. The study reveals a transmission loss of 65 dB between a 2mm long antenna pair, separated by a distance of 4 mm, on bulk Si substrate, which reduces to 40 dB for SOS substrate.

Improved results in terms of interconnection distance for intra-chip communication at 15 GHz have been presented in [5], where separation of 3.2 mm was achieved between a 2mm long dipole pair. Due to the large losses, it appears that on-chip wireless interconnection will only be practical on high resistivity substrates.

2.2.2 Integrated Antennas on High Resistivity Silicon Substrate

One of the challenges for on-chip antennas is the large loss due to low resistivity (10 ohm-cm) silicon substrate. This is a fundamental limitation of Si and this issue becomes more serious as the frequency increases. In order to overcome this problem, experiments with high resistivity silicon have been done. Integrated antennas realized on $10^6 \Omega\text{-cm}$ silicon substrate have been presented in [19]. Both meander line and PIFA (planar inverted F antennas) configurations have been investigated, as shown in Figure 2.3. These antennas have been compared in performance with similar antennas on bulk silicon at 5, 10 and 20 GHz. The study confirms improved antenna performance on proton-implanted silicon with broad radiation patterns, low return loss and sharp well defined resonance. Furthermore, no mention of antenna gain has been made in this work, indicating probable low values. In contrast, poor antenna resonance is found on conventional oxide isolated silicon because of the lossy nature of the substrate. Moreover, air transmission has been attempted for low resistivity Si substrate without success. However, proton-implantation requires a number of extra steps, which make the process complex and expensive.

Similar work shows transmission loss of 36.5 dB for a 2 mm long and 10um wide dipole antenna pair on proton implanted Si substrate as compared to 56 dB for standard Si substrate [20]. The measurement setup requires off-chip baluns and the antennas have only been

characterized for substrate transmission. The measured results show considerable shift in the resonant frequency from the designed value and the antennas show poor return loss at the frequency of interest. The proton implantation process increases the resistivity of Si substrate from 10 Ω -cm to 0.1 M Ω -cm but a number of extra processing steps are required. The results prove that the transmission gain can be maximized for a given resistivity by optimizing the silicon substrate thickness or by inserting a low k dielectric layer below the substrate.

Figure 2.3 The structure of (a) meander antenna at 10 GHz, (b) PIFA at 10 GHz and (c) PIFA at 5.7 GHz [19].

The functionality of integrated antennas on silicon up to a frequency of 100 GHz is presented in [7]. Standard Si wafers with 10 ohm-cm resistivity are customized through low energy proton implantation to overcome the large RF loss. A G-S-G (ground signal ground) probe-fed monopole antenna design is shown in Figure 2.4. Its first and second resonance operating frequencies are well defined at 50 GHz and 103 GHz, respectively. Near its first

resonance the antenna exhibited a gain of 4 dBi and a narrow half power beam width of approximately 30 degrees. The design is efficient in terms of occupying space on the wafer but employs single ended feed, which is not suitable for integration with differential circuits. As with previous research, similar antennas fabricated on the standard Si illustrate a less sharp resonance with large loss over a wide frequency range.

Figure 2.4 On-chip monopole antenna [7].

2.2.3 Integrated antennas with baluns

An important aspect of this thesis will be the incorporation of balun structures with the integrated antennas. It is therefore appropriate to assess relevant work conducted in this area.

A broadband 10 GHz to 17 GHz printed dipole radiating element with an integrated microstrip balun has been investigated on fused silica substrate [14]. This combination exhibits an SWR of less than 2 over bandwidths in excess of 40 percent. The dipole-radiating element is integrated with the balun structure by forming the arms of the dipole as extension of the balanced line conductors, as depicted in Figure 2.5. By varying the balun parameters, the dipole

impedance can be double tuned to that of the system, resulting in a wide bandwidth impedance match. For a center frequency of 13 GHz, this balun structure requires approximately one wavelength long microstrip line. Moreover, it requires very broad ground structure and patterning on two metal layers.

Figure 2.5 Printed circuit realization of balun structure with integrated dipole [14].

Another wide band tapered slot antenna element has been realized on Duroid for 1 GHz to 5 GHz operation [15]. The design is shown in Figure 2.6, in which a Marchand balun is employed. The input microstrip line couples to an underlying slot line through four-quarter wave impedance matching sections. A VSWR of 2:1 is achieved over an octave bandwidth. In addition to requiring metal patterning on both sides of the substrate, the balun transition is electrically long in two dimensions.

Figure 2.6 Marchand Balun [15].

A 2.4 GHz microstrip via balun integrated with a dipole antenna on FR-4 PCB substrate is presented in [21]. Layout of the balun and dipole with a via-hole for WLAN and wireless communication application is shown in Figure 2.7. This design features a broad bandwidth and is ideally suited for applications like active phased arrays where monolithic microstrip circuitry is incorporated with each array radiating element. However, the balun design requires patterning on two-sided metallization and a via to connect both the metal layers. Furthermore, it incorporates a wide ground plane to realize the microstrip balun structure.

Figure 2.7 Microstrip via balun [21].

A different balun design using CPW (coplanar wave guide) to CPS (coplanar strips) transition, as shown in Figure 2.8, has been demonstrated in [16]. This design utilizes a circular stub to achieve a broad bandwidth of 2- 8 GHz on Duroid substrate. Only a single metallization layer is needed, however bond wires are required which is a limitation in this design. For a center frequency of 2 GHz, balun is quarter wavelength long and incorporates a broad CPW ground. Dual frequency operation of the CPS dipole is realized by introducing a small gap in the length of dipole and inserting varactor devices. The varactors provide various capacitive loadings, which correspond to various electrical lengths of the dipole antenna and thus different resonant frequencies.

Figure 2.8 CPW to CPS Balun [16].

Isolated CPS and CPW balun structures on high resistivity silicon substrate have been presented in [22]. These designs can be utilized for integration with differential antennas. As seen in the previous research, these structures incorporate vias and air bridges, which requires extra fabrication steps.

2.3 Integrated Antenna Systems/Applications

The previous sections dealt with the design and implementation of antennas alone. Considerable work has also been done on integrating antennas with active microwave circuitry on Si.

2.3.1 MMIC Oscillator with Integrated Antenna

Wafer level integration of antennas with a SiGe MMIC oscillator has been demonstrated at 24 GHz and 34 GHz using a Si host substrate [8]. A full wave loop antenna suspended on a thin dielectric (BCB) membrane is employed. The complete assembly is shown in Figure 2.9. The antenna is driven differentially and has a 2.4 mm diameter. Its gain is estimated to be 1.8 dBi at 24 GHz and the overall transmitter radiated power is 3.7 dBm. Radiated power has been estimated for the antennas by measuring the signal with a pyramidal horn antenna. While the work is interesting for its use of differential mode Si-based technology, the thin film processing and chip assembly steps required are far from standard.

Figure 2.9 wafer level integration of loop antenna with an oscillator [8].

2.3.2 Automotive Applications

As wireless applications move to higher frequencies, the integrated antenna technique becomes increasingly powerful alternative to conventional design approaches. In recent past, an

active silicon monolithic millimeter-wave integrated-circuit (SIMMWIC) antenna for vehicular sensor application at 76.5 GHz has been reported [23]. As shown in Figure 2.10, this design features a patch antenna integrated with an IMPATT diode, as well as a traveling-wave rat-race coupler as the synchronizing network. Due to the self-mixing properties of the integrated front end, IF is generated automatically and no additional mixer components are required. The whole structure is monolithically integrated on 125 μm thick high-resistivity silicon substrate, resulting in a very small chip size of 3.2x2.6 mm². This one chip front end features a high millimeter-wave output power up to 5 dBm. The measured gain of the active antenna is approximately -3 dB. Such novel integrated antennas are promising in realizing low-cost millimeter-wave sensor systems for automotive applications.

Figure 2.10 76.5GHz active SIMMWIC antenna for automotive applications [23].

2.3.3 Integrated Antennas in Other Technologies

Considerable work has been done in integrating the antennas with the active circuitry in technologies other than Si. Some examples from this work will be discussed in this section.

The integration of antenna with an up converter on Teflon-fiberglass substrate has been presented in [9]. The layout of the complete transmitter circuitry is shown in Figure 2.11. The incoming signal is 5GHz and the outgoing signal is 24GHz with a single GaAs Schottkey barrier diode doing the converter action. The signal is amplified in the MMIC power block. The transmitting antenna is realized using balanced (symmetrical) microstrip line technique with four broadband pentagonal dipoles, where one half of the dipoles are printed on one side and other half on the opposite side of the substrate. A balun has been incorporated between the antenna and the rest of the circuit through exponential tapering. The array gain is estimated to be about 10dB and the measured radiated power at 1 dB compression point is about 30 dB.

Figure 2.11 5 GHz to 24 GHz up-converter with integrated antennas [9].

Integrated antennas, which operate as both, a radiating element and a frequency dependent output load in the circuit, provide various circuit functionalities such as filtering and harmonic tuning [24-26]. Based on the integrated antenna design concept, the measured passive antenna impedance is directly transformed to the optimum load impedance for maximum efficiency. A high efficiency and compact AlGaN/GaN heterojunction field-effect transistor (HFET) power amplifier integrated with a microstrip antenna at 7.25 GHz for RF front-end circuit applications is shown in Figure 2.12 [27]. A microstrip circular sector antenna is employed as both a radiator and frequency dependent output load. Higher order harmonics from the HFET in nonlinear operation are reactively terminated because of the harmonic termination characteristic of the antenna.

Figure 2.12 Power amplifier integrated with a microstrip antenna [27].

The integrated antenna is an ideal candidate for designing compact transceivers for wireless applications because of the possibility of building the whole RF subsystem, including oscillator, amplifier, antenna, and mixer onto a single dielectric substrate. In one of the earlier designs [28], an X-band quasi-optical transceiver element has been realized by using the FET with an integrated microstrip patch array. The FET has been utilized as both signal source and self-oscillating mixer for down-conversion of the received signal. Since this arrangement provides the IF signal which corresponds to the Doppler-frequency shift, a simple, compact, and lightweight motion sensor is obtained. Similar concept has been applied to a two element microstrip patch array, which uses the injection-locking beam-switching technique to function as a Doppler radar with azimuth-tracking capability [29]. This transceiver module uses two MESFET's as both transmitting oscillators and self-oscillating mixers to obtain the IF (Doppler shift frequency) signals. The patch antenna is used as the radiating element as well as the resonator for the oscillator.

The use of integrated antenna based small low-cost microwave “tag” transponders for non-contact identification such as entry system, toll collection, and inventory control has attracted much interest in recent years. The photograph of a 6-GHz non-contact ID card based on a sub harmonically pumped quasi-optical mixer using a broadband bowtie antenna is shown in Figure 2.13 [30]. When illuminated by a 6-GHz interrogating signal, it transmits a unique digital identification code at the response frequency near 12 GHz.

Figure 2.13 Photograph of a non-contact RF ID card [30].

Another important objective of integrated antennas is to realize power-combining arrays with built-in beam-steering capabilities. An array of inter-injection-locked oscillators causing a progressive inter-element phase shift was demonstrated in [31], leading to the possibility of realizing beam-steering arrays without phase-shifters. This novel approach is especially attractive at millimeter wave frequencies where ferrite-based phase shifters and related feeding network can be lossy, bulky and extremely costly. A X-band prototype of a ten-element power combining and beam-scanning array using coupled voltage-controlled oscillators (VCO's) is shown in Figure 2.14 [32]. A medium power GaAs MESFET was employed on Duroid substrate for this work. By controlling the free running frequencies of oscillators a progressive phase shift is achieved.

Figure 2.14 Photograph of a power-combining and beam-scanning array [32].

Recent progress in semiconductor laser sources, fiber optics and photonic devices has made it possible to have applications like antenna remoting in cellular and micro cellular radio systems using analog fiber links, distribution of cable-television signals and beam forming for phased-array antennas. One technique commonly adapted for microwave-optical interaction is the optical control of active devices by direct illumination. The photograph of a two-element beam-scanning array based on unilateral injection locking and optical control of free running frequencies is shown in Figure 2.15 [33]. In order to achieve beam- steering, the free running frequency of the oscillating MESFETs is controlled by directly illuminating it with light. To prevent the illumination source from disrupting the microstrip antenna patterns, the MESFETs are mounted through the substrate and illuminated from the rear of the circuit.

Figure 2.15 Optically controlled two-element beam-scanning array [33].

2.4 Microwave measurement /calibration and de-embedding issues

Since one of the objectives of this work is to devise a suitable de-embedding technique for the extraction of antenna parameters, therefore it is necessary to have an insight into the issues related to microwave measurements, calibration fixtures and de-embedding techniques. On-wafer high frequency microwave measurements are very challenging because of many issues related to the low resistivity Si substrates and low-conductance metallization. Numerous problems include probing reliability, contact resistance issues, leakage effects, substrate coupling, and calibration/de-embedding accuracy. The probe tip discontinuities also have a large effect on the extracted parameters of the measured structures. Precise measurements at the component level are essential to obtain designs operating within their target specifications.

Typical probing configurations are shown in Figure 2.16 [34]. The fixture in Figure 2.16a allows very large devices to be measured and Figure 2.16b shows a fixture customized for a specific device. The general fixture shown in Figure 2.16c is common for 2 ports on wafer transistor measurements. A similar fixture that employs 45 degrees angles is shown in Figure 2.16d.

Probing pads constitute considerable parasitics. Most of the loss is associated with the coupling from signal pad to ground pads that originate from the pad substrate capacitance and the semi-conductor nature of the silicon substrate. Although the loss is reduced for very small pads, the degradation is still significant. For practical reasons, pad dimensions smaller than 45um are typically not feasible [35]. However, the test fixture should still be characterized by a few and dominating effects/parasitics for lowest de-embedding complexity and highest accuracy, so a trade off is required. Low substrate resistivity can also cause detrimental leakage effects, which can significantly distort the measurements. To avoid this phenomenon, an extensive grounding of the substrate surface is necessary. However a potential drawback of using extensive substrate grounding is that in some cases the behavior of the device under test may be affected. Another concern is the oxidation of metallization, which often happens instantaneously if the measurements are done outside a specified chamber. In that case it is difficult to obtain probing consistency.

An accurate ‘on-wafer’ fabrication of calibration standards is difficult with non-precision processing techniques. Many practical measurements therefore rely on an off-wafer calibration using a calibration substrate from an external manufacturer. Usually both the contact geometry and the substrate differ between the calibration structure and the device under test (DUT). The difference becomes especially important when measurements are performed on lossy-substrates.

However, on-wafer silicon calibration is still viewed as being less applicable because mostly the high forward coupling of on-wafer two port standards is not addressed by common calibration approaches.

Figure 2.16 Microwave probe fixture examples [34].

Moreover, calibration techniques are not as flexible as de-embedding techniques to address devices of various geometry and shapes [34]. Hence, several custom-made calibration kits are required on each test wafer. One reliable approach is to use a ceramic ISS (impedance standard substrate) in combination with calibration devices fabricated in the particular technology. By this approach, measurement pads and external interconnects may be included in the calibration and thereby de-embedded. Hence, the reference plane may be established close to the intrinsic boundary of the device as desired.

On-wafer microstrip calibration structures for microwave measurements up to 50 GHz have been presented in [36], but are not applicable to the coplanar regime in this work. Special contact structures for coplanar microwave probes have been utilized to determine the characteristic impedance of on-chip lossy lines through high frequency S-parameter measurements [37], but are limited to CPW (coplanar waveguide) lines rather than CPS (coplanar strips) lines of this thesis.

The sensitivity of different on-wafer calibration techniques to probe positioning is investigated in [38]. Common calibration techniques like SOLT (short, open, load, through), SOLR (short, open, load, reciprocal device), LRM (line, reflect, match), and LRRM (line, reflect, reflect, match) have been compared in terms of repeatability, reproducibility, load standard overlap, short standard overlap and open standard change. Analysis confirms the accuracy of LRRM calibration techniques over the others, however all the above methods are considered acceptable.

2.4.1 De-embedding Techniques

De-embedding is an important aspect of the microwave measurements in which the effects of the test fixture are removed. In certain cases this could be as simple as a shift of reference plane by a certain distance away or towards the DUT. Depending on the fixture used and the available calibration standards, various mathematical approaches for de-embedding measurements can be applied. Some of the widely used techniques are listed below and shown in Figure 2.17 as well [34] [39]. In all cases the goal is to obtain the DUT S-parameters based on measurements performed at the external terminals shown.

a. Open pad De-embedding (OPD)

The method is based on an assumption that the parasitics leading to the DUT can be described by a parallel admittance, y_p , as shown in Figure 2.17a. The admittance is determined as the measured input admittance of an open standard; that is $y_p = y_{i,o}$. To de-embed the fixture, the estimated admittance is simply subtracted from the measured input/output admittance of the DUT including pads and interconnects (y_{11} and y_{22}).

b. Open/short De-embedding (OSD)

Interconnects in CMOS technology are typically realized using aluminum traces. Since the ISS uses gold for metallization, this means that the contact impedance increases when the probes are lifted from the ISS onto the CMOS chip. This additional series loss can be determined by adding a short standard to the set as shown in Figure 2.17b.

c. Open/short/thru De-embedding (OSTD)

By adding a thru standard, the transmission line from the pad to the DUT can be de-embedded as well. This parasitic is denoted as Z_1 as illustrated in Figure 2.17c.

d. Two-port De-embedding (2 PD)

Another simple representation is to assume that a two-port network can describe the network from the probe tips to the DUT. This method only requires a thru standard as illustrated in Figure 2.17d. To extract the two-port parameters from reflection and transmission measurements on the thru, it is assumed that the input and output interconnects are identical, although mirrored, and, hence, reciprocal. The de-embedding is performed by converting the S-parameters into a wave-amplitude transmission matrix and then performs matrix division as

$$T_{dut} = T_p^{-1} \cdot T_m \cdot T_p^{-1}$$

where T_m are the measured transmission parameters and T_p are the extracted parameters.

e. 3-step De-embedding (3 SD)

The previous methods have neglected the possible coupling between the input and output. One method that offers a more complicated model topology for the test-fixture is the 3-step method. The fixture topology is shown in Figure 2.17e and four standards are required. The de-embedding procedure employs subtraction in Y and Z parameter domains.

Figure 2.17 De-embedding techniques [34].

Measurements incorporating these de-embedding techniques reveal that 3SD and 2PD methods are less accurate, while OSTD method is simple and reliable. The OPD method is useful

for small interconnect lengths, whereas OSD can give improved performance by adding a short standard to it.

2.5 Summary and conclusions

This chapter has reviewed previous work in integrated antennas and applications, as well as related balun structures and measurement issues, with a primary focus on Si-based implementations suitable for 24 GHz operation.

Nearly all of the on-chip antennas discussed have been characterized for transmission through the substrate. The only successful antenna design for air transmission was a monopole antenna, which is single ended and hence not suitable for integration with the differential circuitry. In general these antennas either suffer from large physical dimensions, digital CMOS incompatible material, extra processing, high transmission loss or limited range. The need therefore remains for further work on standard Si integrated antenna realization. All the integrated balun structures presented suffered from limitations in terms of size and fabrication complexity justifying new attempts to obtain useful baluns in a simple Si process.

In general, microwave measurements for on-chip differential antennas are performed through off-chip balun structures. Moreover, no de-embedding methods exist for integrated baluns in Si technology. Furthermore, existing microwave fixture designs for testing are complicated and large in size. Also, the de-embedding techniques employed to extract the DUT parameters from the measurements involve tedious mathematical analysis, which is time consuming and can cause errors in the final results. The remaining chapters of this thesis pursue each of these issues in detail.

Chapter 3 Development of On-chip Balun for IC Dipole Antenna

3.1 Introduction

A balun (balanced-unbalanced) is used to adapt a balanced device to an unbalanced one. The balanced device has an equal and opposite voltage on both the terminals with respect to ground, unlike an unbalanced device. Baluns are key components in balanced circuit topologies such as double balanced mixers, push-pull amplifiers, and frequency doublers. Various balun configurations have been reported for applications in microwave integrated circuits (MICs) and microwave monolithic integrated circuits (MMICs), and were discussed in chapter 2. In this chapter, an on-chip balun design adapted for Si integration is presented, analyzed and experimentally validated.

3.2 Balun Design and CAD Simulation Strategy

In order to obtain a compact, easily fabricated, planar Si balun, the simple structure shown in Figure 3.1 is proposed. Coplanar strips (CPS) are used to convert from the unbalanced GSG pad terminals to a balanced (non-grounded) resistive load. The CPS section is $\lambda/4$ long and the standard GSG probe pad configuration is modified by connecting the ground pads through a ground bar. This arrangement also provides an RF short to the balun structure. This balun design is different from and superior to previous reported configurations, as it is a simple planar structure with no vias, air bridges or bond wires. Moreover, it is a compact and low cost design because the structure is on-chip and realized using a standard IC fabrication process. The theoretical model of the balun, as shown in Figure 3.2 [40], transforms the load impedance (Z_L) to a source impedance (Z_{in}) through the simple quarter wave transmission line relationship as

given by equation (3-1). Z_0 represents the characteristic impedance of the transmission line. Z_L will later represent the differential-mode antenna impedance Z_{ant} .

$$Z_{in} = \frac{Z_0^2}{Z_L} \quad (3-1)$$

Figure 3.1 Proposed balun.

Figure 3.2 Balun theoretical model [40].

The theoretical balun model must be implemented in an EM analysis tool to feed the on-chip differential antenna and obtain single ended S-parameters along with the antenna radiation pattern. Certain issues must be resolved before realizing the balun structure in the chosen EM

simulator (Ansoft Ensemble). Conventional $50\ \Omega$ microstrip excitation of the balun is employed in the simulator in order to model the unbalanced feed test setup. On the other hand, the grounded CPS conductor and the load impedance are not connected through the substrate to the underlying ground. Thus, S-parameter “black boxes” are incorporated as shown in Figure 3.3 to represent Z_L and the grounded CPS terminal. In addition, since Ensemble cannot simulate structures with finite ground plane, a slot in the infinite ground plane is inserted to realize the CPS section. Using routinely achievable conductor spacing ‘S’ and width ‘W’ of $50\ \mu\text{m}$ and $200\ \mu\text{m}$ respectively, expressions for coplanar strip design [41] yielded Z_o of $88\ \Omega$. The length ‘L’ of the quarter wavelength CPS section was calculated to be $1.34\ \text{mm}$.

Figure 3.3 Realization of balun structure in Ansoft Ensemble.

The Ensemble setup for the substrate/ metallization layers is shown in Figure 3.4. As would be found in a standard Si process, the substrate has an insulating oxide on top of it.

Copper is employed for metallization. This analysis is done for a lossless substrate process ($\text{Tan}\delta = 0$) in order to verify the basic behavior of the balun. The overall dimensions are listed in Table 3.1. Further details of the fabrication will be provided in section 3.4.3.

Table 3.1: Substrate and metallization arrangement in Ensemble

Silicon substrate	300 μm
Insulating substrate (silicon dioxide)	3 μm
Metallization (copper)	1.9 μm
$\text{Tan}\delta$	0

Figure 3.4 Substrate/metallization setup in Ensemble.

3.3 Validation of CPS Balun Design

The goal is to first verify that the proposed balun design functions correctly and then to extract its attenuation constant (α), phase constant (β), and characteristic impedance (Z_0) for subsequent de-embedding operations. A microwave circuit simulator (Agilent ADS) is employed in this process.

The balun design in Ensemble incorporates “black boxes” for the load impedance and the grounded CPS terminal. The transition from a microstrip feed to the CPS section is another complexity of the Ensemble analysis. It is therefore important to compare the theoretical balun performance of Figure 3.2 using ADS (as shown in Figure 3.5) with the simulated performance of Figure 3.3 using Ensemble. The transmission line representing the balun is connected to a 50-ohm termination at the input and a load resistor Z_L at the output. Similarly, the balun in Ensemble is connected to a 50-ohm microstrip line at the input and a “black box” representing load resistor at the output. The verification is done by comparing the two sets of results over the frequency range 23 GHz to 25 GHz for a variety of identical load impedances, both real and complex. The resultant smith charts for two sample cases ($Z_L = 100 \, \Omega$ and $Z_L = 20 + j 68 \, \Omega$) are shown in Figure 3.6–3.7.

Figure 3.5 ADS Schematic for balun simulation setup.

(a)

(b)

Figure 3.6 (a) ADS result for $Z_L = 100\text{ohm}$ (note that m2 marker covers the curve),

(b) Ensemble result for $Z_L = 100\text{ohm}$.

(a)

(b)

Figure 3.7 (a) ADS result for $Z_L = 20 + j68ohm$, (b) Ensemble result for $Z_L = 20 + j68ohm$

Comparison of Ensemble and ADS results shows that both the models transform the load impedance in a similar fashion. Given the simplicity of the model used to represent the actual balun, perfect agreement is not expected. Very good correlation is nonetheless obtained. The inductive Z_L is transformed into capacitive Z_{in} and vice versa, as expected from a $\lambda/4$ transformer. This means that the balun design in Ensemble is satisfactory and reliable enough to map the simulated Z_{in} values to Z_{ant} (or Z_L) values.

3.4 Realization of balun structures on lossy Si substrate

Having confirmed that the basic balun design is sound in a lossless dielectric medium, we now proceed to develop a practical balun on standard silicon. Since the final goal of this work is to investigate integrated antennas (and not the baluns, which are simply included for testing purposes) the remaining steps are carried out experimentally. There are two major issues to be resolved before the balun can be realized on Si substrate with a single metallization layer process.

- a. To provide an RF short to the balun without incorporating a via hole.
- b. To test a GS (ground signal) balun structure with a GSG (ground signal ground) wafer probe.

These issues are discussed in detail in the next section, followed by the selection of the test structures and circuit fabrication considerations.

3.4.1 Probe pad configuration

The standard pad configuration for a GSG wafer probe is shown in Figure 3.8(a). The pad

size is $100\text{ }\mu\text{m} \times 100\text{ }\mu\text{m}$, while the pad-pad separation is $150\text{ }\mu\text{m}$ center to center. In order to feed/test the balun, this pad structure is modified as shown in Figure 3.8(b).

Figure 3.8(a) Wafer probe pad configuration, (b) Modified Wafer probe pad configuration.

The ground pads are connected with each other through a ground bar to make one ground structure. The ground bar is designed to achieve minimum coupling with the signal pad and it is wide enough to ensure good ground connection. It will also provide RF short to the grounded CPS terminal as shown in Figure 3.1. There are tapered sections between the pads and balun arms to gradually adjust for the difference in width between the two structures.

3.4.2 Selection of test structures

Two identical baluns having distinct termination resistors are realized in order to allow extraction of the characteristic impedance of the CPS section. Nichrome is used to realize the load resistors because it has high sheet resistance and therefore small size resistors are feasible. The length of the nichrome resistor is kept constant in both the cases as they extend from the

outer edges of the balun arms. The dimensions of these resistors are calculated using the expressions below.

$$R = \rho \frac{L}{A} \quad (3-2)$$

$$R = \rho \frac{L}{W \times t} \quad (3-3)$$

Where ρ = resistivity, L = length, W = width and t = thickness. Since L , ρ and t are constant in this case, therefore varying W varies the resistance value. Keeping this factor in mind, two Nichrome load resistors with different widths are designed for the balun structures as shown in Figure 3. 9. The exact values of resistance thus obtained are not important at this stage. The layout of baluns was created in LEDIT, which is routinely used in the Department of Electronics.

Figure 3.9 LEDIT Layout of balun structures with different load resistors.

3.4.3 Fabrication

Balun structures were fabricated on silicon wafers in the micro fabrication lab of Carleton university. The 2-inch wafers had a nominal thickness of 300 μm and resistivity of 10 $\Omega\text{-cm}$. At the first step of the device processing, the NiCr resistors were fabricated. A NiCr film (200 nm thickness) was deposited by sputtering and defined through a lift-off process. At the second step, the Cu balun structures were fabricated. Immediately prior to Cu deposition, the NiCr resistors contact surface was cleaned off the oxide by sputter etching. A stack of titanium (20nm thickness) and Cu (1.9 μm thickness) was deposited by sputtering and defined through the lift-off process. The titanium layer was used to improve adhesion. The fabrication sequence was as follows:

- a. Oxide is deposited on bulk silicon (10 $\Omega\text{-cm}$) through low temperature deposition.
- b. Photo resist is applied on the wafer and patterned through Nichrome mask.
- c. 0.2 micron NiCr is deposited through sputtering process.
- d. Lift off process is carried out to remove the unwanted NiCr.
- e. Photo resist is again applied and patterned through the Cu mask.
- f. 1.9-micron thick Cu is deposited using sputtering.
- g. Lift off is performed to remove unwanted Cu.

Appendix B contains the detailed fabrication process sheet. A microphotograph of the Cu balun with NiCr resistor is shown in Figure 3.10.

Figure 3.10 Microphotograph of Copper balun and Nichrome resistor on Si.

3.5 Experimental validation

In order to characterize the balun experimentally, the following steps must be performed.

- a. Measure the dc resistance of NiCr resistors and correct it for skin depth effect at 24 GHz.
- b. Measure the S-parameter of the baluns with a network analyzer. This is done with certain Si on-chip calibration structures.
- c. Extract the characteristic impedance (Z_0) from the measured results.

In step (a), a direct measurement of the resistors would not be useful due to several dissimilarities between possible test structures and the resistor plus-balun implementation.

3.5.1 Nichrome resistors measurement

The dc resistance for the Nichrome resistors (R_{L1} and R_{L2} in Figure 3.9) is measured using the four-probe method as shown in Figure 3.11. The four-point resistance measurement method eliminates lead resistance. Instruments based on the four-point measurement work on the following principle: (a) two current leads, C1 and C2, compromise a two-wire current source that circulates through the resistance under test. (b) Two potential leads, P1 and P2, provide a two-wire voltage measurement circuit that measures the voltage drop across the resistance under test.

(c) The instrument (HP 4155 Semi-conductor Parameter Analyzer, in our case) computes the value of resistance from the measured values of current and voltage.

The measured resistance values are $R_{L1} = 9.16 \text{ ohm}$ and $R_{L2} = 5.30 \text{ ohm}$. This is the dc resistance of Nichrome resistors, which has to be corrected for skin depth effect at 24 GHz.

Figure 3.11 Four probe resistance measurement setup.

Let us denote the dc value of the NiCr resistance as R_{dc} and the resistance value at 24 GHz as R_{24GHz} , where the latter was calculated by equation (3-4) [42].

$$R_{24GHz} = \frac{\rho \times l}{w \times \delta} \quad (3-4)$$

where ρ = Resistivity, l = Length and w = Width. Skin depth denoted as δ was calculated using equation (3-5).

$$\delta = \frac{1}{\sqrt{\pi \times f \times \mu \times \sigma}} \quad (3-5)$$

where f = frequency, μ = permeability and σ = conductivity.

$$\delta = 0.132 \mu m$$

Considerable change occurred in the NiCr resistance values due to the skin depth effect. Corrected values at 24 GHz were found to be $R_{L1} = 15.9 \Omega$ and $R_{L2} = 7.95 \Omega$.

3.5.2 Microwave Measurement

The original balun design was intended to provide a simple de-embedding relationship (quarter wave transformer) between load (or antenna) impedance and input impedance, in the form of equation (3-1) repeated here for convenience:

$$Z_{in} = \frac{Z_0^2}{Z_L}$$

The test setup consists of an Agilent 8722ES S-parameter network analyzer (0-40 GHz), probe station, GSG wafer probes (150 micron pitch) and an ISS (impedance standard substrate) calibration substrate. All the measurements were performed in a low interference chamber, where the walls are lined with absorbing material. SOL (short, open load) calibration was done on the ISS substrate. After establishing the reference plane at the tips of coplanar probes, the Si calibration and balun structures were measured. It is important to experimentally obtain the characteristic impedance and verify that the balun is indeed $\lambda/4$ long.

$\lambda/4$ Transformer verification

To verify that the CPS section of the realized balun is quarter wavelength long at 24 GHz, the open circuit pad and open circuit balun structures are tested as shown in Figure 3.12 and 3.13. The idea is to measure the difference in electrical length between the two. For the open circuit pad structure, the measured input impedance at 24 GHz is $Z_{ina} = 42.55 - j50.35$ which, when plotted on the smith chart gives 0.155λ on the wavelength towards the load scale.

For the Open circuit balun structure, the measured input impedance is $Z_{inb} = 35.32 + j15.53$. Plotting this point on the smith chart gives 0.42λ on the wavelength towards the load scale, but if the balun length were $\lambda/4$ long than it should have been located at 0.405λ . This means that the realized balun length on lossy Si is 0.015λ longer than $\lambda/4$, which is nonetheless close to the value calculated from approximate equations. Therefore equation (3-1) cannot be used to calculate the characteristic impedance from the measured results. Instead, the general transmission line equation will be employed.

Figure 3.12 Open cct pad structure.

Figure 3.13 Open cct balun structure.

Characteristic Impedance Calculation

The two balun structures with different load resistors are measured. Input impedances Z_{in1} and Z_{in2} for R_{L1} and R_{L2} respectively are shown in Figure 3.14(a) and 3.14(b). Since the quarter wave transformer equation is no longer valid, the standard lossy transmission line equation [41] is used to calculate Z_{o1} and Z_{o2} for both the cases.

$$Z_{in} = Z_0 \frac{(Z_L + Z_0 \tan \gamma \ell)}{(Z_0 + Z_L \tan \gamma \ell)} \quad (3-6)$$

where propagation constant denoted as γ is given by, $\gamma = \alpha + j \beta$.

$$\alpha = \sqrt{\frac{\mu \varepsilon}{2} \left(\sqrt{1.0 + \frac{\sigma^2}{\omega^2 \varepsilon^2}} + 1.0 \right)} \quad (3-7)$$

Using equation (3-7), we estimate $\alpha = 523$ Np/m, whereas $\beta = 1250$ rad/m is obtained from the measured results, hence $\gamma = 523 + j1250$. Equation (3-6) can now be solved for Z_0 , given that all the other quantities are known. Using (Z_{in1} and R_{L1}) yields $Z_{o1} = 42.36 + j21.66 \Omega$. Repeating for (Z_{in2} and R_{L2}) yields $Z_{o2} = 44.97 + j9.88 \Omega$, which is close to Z_{o1} . Convergence of the measured results for two different load resistors confirms that the characteristic impedance of the realized balun structure is $Z_o = 44 + j 15 \Omega$, which is the average value. The above line parameters will be employed in the de-embedding of integrated antenna impedance in Chapter 4.

(a)

(b)

Figure 3.14 Measurement results for balun (a) with R_{L1} (b) with R_{L2}

3.6 Conclusion

The analytical and experimental verification of the CPS balun on lossy Si substrate has been carried out. A modified wafer probe pad topology has been demonstrated to test the on-chip balun with standard GSG probe measurement setup. The balun is realized on a lossy silicon substrate and its Z_0 is extracted from measured results. Analysis also confirms that the electrical length of the realized balun is slightly longer than $\lambda/4$ at 24 GHz, requiring the use of more general transmission line equation. Through experimental investigation of two different cases of balun loading, the necessary line parameters have been extracted for subsequent de-embedding purposes. This balun design is superior to previous configurations, as it is simple planar structure with no vias, air bridges or bond wires. Moreover, it is a compact and low cost design because the structure is on-chip and realized using a standard IC fabrication process.

Chapter 4 Study of On-chip Dipole Antenna Impedance

4.1 Introduction

The on chip antenna concept represents a possible solution for wireless communication system having no external components. These single chip RF systems are useful in applications such as biomedical technology where space is at premium and transmission range can be short. A simple dipole is a natural choice for integration into a balanced mode transceiver front end, since it is differential in nature. Obviously, more complicated antenna geometries could be investigated, but the dipole provides a useful starting point. For an antenna with reasonable efficiency for air transmission, an arm length of approximately $\lambda/4$ in air (or approximately $\lambda/2$ on a Si chip) is required. In that case, for lower carrier frequencies such as the 2.4 and 5 GHz bands, the size of the antenna exceeds 10 mm (Table 1), which is too large to fit on a chip without bending. At 24 GHz, the antenna only needs to be 3 mm long, which can fit easily on the chip edges.

Table 4.1: Carrier frequency and antenna size

f_c [GHz]	Band	$\lambda/4$ [mm]
2.4	ISM	30
5	UNII	15
24	ISM	3

This chapter is devoted to the development of 24 GHz Si dipole integrated antennas and their characterization in terms of impedance. Building on the balun results of Chapter 3, de-embedding considerations will be presented. Finally, the effect of geometry and material properties on antenna impedance will be studied. Si substrate (300 Ω -cm) has been investigated

because it is considered as an industry standard for high resistivity Si applications. Antenna gain properties will be assessed in Chapter 5.

4.2 Antenna and Front-end Interface

Integrating the antenna on-chip eliminates the matching networks that transform between the system impedance and $50\ \Omega$ off-chip components. Antenna impedance becomes one of the design parameters, which provides design flexibility to the interfacing circuits. Furthermore, the integrated antenna is frequency selective that can be designed, as a band pass filter to remove unwanted interference. It is informative to briefly review the properties of integrated transceiver circuitry so as to appreciate the range of impedance values required of the co-located antenna.

Figure 4.1 Antenna interface to the (a) transmitter power amplifier and (b) receiver low-noise amplifier [2].

This section presents the analysis of the desired impedance of the antenna for two interface circuits: the power amplifier (PA) for the transmitter, and the low-noise amplifier (LNA) for the receiver [2]. For the transmit antenna (Figure 4.1a), the impedance $\text{Re}\{Z_t\}$ is determined by the required output power level of the PA. For a given supply voltage V_{DD} , the impedance $\text{Re}\{Z_t\}$ is inversely proportional to the output power P , given by

$$\text{Re}\{Z_t\} = \frac{(V_{DD} - V_{on})^2}{2P} \quad (4-1)$$

where v_{on} is the minimum on-voltage for the transistor to operate in the saturation region (CMOS), and a tuned load is assumed. If an output power of 10mW (10 dBm) is required and a 1.2-V CMOS technology is used, assuming minimum v_{on} is 0.2 V, $\text{Re}\{Z_t\}$ has to be less than 50 Ω single-ended, or 100 Ω differential.

For the receive antenna, the impedance Z_r is designed to optimize input matching and maximize the gain of the LNA. In modern integrated LNA design, inductive degeneration using L_s as shown in Figure 4.1b is often used to achieve the required input matching and gain. The input impedance Z_{in} is given by

$$Z_{in} = \frac{g_m L_s}{C_{in}} + j\left(\omega L_s - \frac{1}{\omega C_{in}}\right) \quad (4-2)$$

where g_m is the transconductance and C_{in} is the input capacitance. The condition for maximum power transfer between the antenna and the LNA is given by

$$Z_r = Z_{in}^* \quad (4-3)$$

where (*) denotes conjugation. From equation (4-2), L_s can be used to achieve the required small-signal matching by setting $g_m L_s / C_{in}$ to the reference impedance (such as 50 Ω). This results

in a simple one-component matching network (usually an inductor) at the input to resonate the $\text{Im}(Z_{\text{in}})$. This simple matching method is favorable at higher frequencies such as 24 GHz because matching components at these frequencies are very small and parasitic impedance is significant. However, the use of degeneration L_s , has a direct impact on gain G because

$$G = \frac{Z_l}{Z_s} \quad (4-4)$$

where Z_l is the load impedance and Z_s is the degeneration impedance. At 24 GHz, assuming a tuned load is used for the LNA, Z_l is relatively small due to limited Q at this frequency. Therefore, Z_s and hence L_s have to be small in order to achieve a reasonable gain. From equation (4-2), this implies a small $\text{Re}\{Z_{\text{in}}\}$ because g_m/C_{in} is given by technology dependent parameter f_T . Therefore, it is preferable to have small impedance for Z_r .

4.3 Antenna Implementation

The dipole antenna topology is shown in Figure 4.2. It consists of two metallic arms, with a separation of 50 microns, consistent with the strip spacing of the baluns previously developed.

Figure 4.2 On-chip antenna with integrated balun structure.

Each dipole arm has width 'W' and length 'L', resulting in an antenna length of 2L. The copper metal thickness is 1.9 μm , with 3 μm of silicon dioxide between the metal and the substrate. Every antenna structure has a $\lambda/4$ balun associated with it. The balun was used to convert the differential terminals of the antenna to single ended for simulation and measurement purposes. Though it is not part of the final on-chip antenna, it is still required for experimental validation. Several antenna structures were designed on three different substrates, 10 ohm-cm for digital silicon, 300 ohm-cm for low loss silicon, and >10,000 ohm-cm high resistivity quartz substrate. Since quartz is considered to be a lossless substrate, it will serve as the reference design for comparison. L-Edit is utilized to create the layout from the schematic as shown in Figure 4.3, which displays a single antenna structure layout.

Figure 4.3 24 GHz Dipole Antenna and Balun Layout.

The layout of a block of antennas and de-embedding structures is shown in Figure 4.4. Three antenna geometries have been selected to become part of the final layout. The original size of the $\lambda/2$ antenna on Si (0.1 mm x 1.5 mm) is varied in terms of width (0.5 mm x 1.5 mm) and length (0.1 mm x 1.6 mm) to observe the effects of some geometry variations on the antenna performance. The balun structures with different load resistors are included in the layout. A few on-chip calibration structures (open, short, load) are fabricated to make a comparison between the off-chip and on-chip calibration standards. These structures were also utilized to determine the electrical length of the realized CPS section of the balun in Chapter 3. The alignment structures are needed to align the copper and nichrome masks during fabrication.

Figure 4.4 Layout of Antenna/De-embedding Structures.

The layout of the complete wafer is shown in Figure 4.5, which includes 12 identical blocks of antennas and de-embedding structures.

Figure 4.5 Layout of the Complete Wafer.

This layout was utilized to generate photo-masks in order to realize copper antennas and nichrome resistors on silicon and quartz substrates. The details of the fabrication process are listed in the process sheets of Appendix 'B'. A microphotograph of the realized copper antennas and de-embedding structures is shown in Figure 4.6.

Figure 4.6 Microphotograph of antennas and de-embedding structures on silicon.

4.4 Dipole Input Impedance through De-embedding

Antenna impedance (Z_{ant}) is one of the most important antenna design features, especially in the case of on-chip antennas. The on-chip differential antenna is fed/tested through an integrated balun structure (Figure 4.7) and Z_{ant} cannot be simply calculated from the simulated or measured S-parameters. It is, therefore, required to extract Z_{ant} from the feed point impedance Z_{in} , as shown in Figure 4.8. It can be obtained by de-embedding the balun S-parameters from the simulated or measured S-parameters.

Figure 4.7 Input Impedance through balun

Figure 4.8 Antenna Input Impedance.

4.4.1 De-embedding Technique

Extraction of the differential mode antenna impedance Z_{ant} from the single ended simulated or measured S-parameters is achieved through the de-embedding operation. This is done in three steps.

1. Simulate the balun structure terminated with 50Ω system impedance in ADS and obtain the 2 port S-parameters for the balun. These S-Parameters are denoted as $[S_{\text{balun}}]_{2 \times 2}$.
2. Perform the inverse function to the balun S-parameters using the ADS de-embedding tool. The result is denoted as $[S_{\text{balun}}]^{-1}_{2 \times 2}$.
3. Using the one port S-parameter of the complete structure (antenna and balun), denoted as $[S_{\text{ant+ balun}}]_{1 \times 1}$, carry out the following symbolic operation in ADS.

$$[S_{\text{balun}}]^{-1}_{2 \times 2} [S_{\text{ant+ balun}}]_{1 \times 1} = [S_{\text{ant}}]_{1 \times 1},$$

This will yield the one port S-parameter of the antenna structure denoted as $[S_{\text{ant}}]_{1 \times 1}$. The desired antenna impedance Z_{ant} can be calculated from these S-parameters. A limitation of this technique is that ADS can only simulate real characteristic impedance (Z_0) for the CPS balun, whereas the measured Z_0 is complex. Nonetheless, the imaginary part of the complex Z_0 is deemed small enough ($j10 \Omega$) to be neglected in this particular case. The balun structure in ADS is therefore imparted the real Z_0 value only for simulation purpose.

4.4.2 Validation of De-embedding Technique

Before de-embedding unknown antenna impedances, the procedure is first validated using a known resistive load as follows.

- a. An isolated balun is simulated in ADS as shown in Figure 4.9. The transmission line representing the balun is assigned the extracted characteristic impedance and propagation

constant. It is simulated from 20 GHz to 30 GHz and the resultant S-parameters are denoted as $[S_{\text{balun}}]_{2 \times 2}$.

Figure 4.9 Balun simulation setup in ADS.

b. The balun is simulated with a 100 Ω resistor as shown in Figure 4.10. It is represented by a S-parameter box containing $[S_{\text{balun}}]_{2 \times 2}$. The result is denoted as $[S_{\text{balun} + 100 \text{ ohm}}]_{1 \times 1}$.

c. The simulation setup for balun de-embedding is shown in Figure 4.11. The ADS de-embedding tool is used to transform the balun S-parameter into $[S_{\text{balun}}]^{-1}_{2 \times 2}$. These inverse balun S-parameters along with the results from step 1 yield the 100 Ω S-parameters $[S_{100 \text{ ohm}}]_{1 \times 1}$, as shown in Table 4.2, where $S_{11} = (100 - Z_0) / (100 + Z_0) = 0.333$. The operation can be expressed as:

$$[S_{\text{balun}}]^{-1}_{2 \times 2} [S_{\text{balun} + 100 \text{ ohm}}]_{1 \times 1} = [S_{100 \text{ ohm}}]_{1 \times 1}$$

Figure 4.10 ADS simulation setup for balun with 100ohm.

Figure 4.11 Balun de-embedding setup.

This result verifies the de-embedding procedure and provides a platform for the antenna impedance to be extracted from subsequent simulated and measured S-parameters. The antennas with integrated balun structures provide feed point impedance Z_{in} that are now processed through the de-embedding procedure to extract Z_{ant} . Either simulated or measured S-parameters will replace $[S_{balun + 100\ ohm}]_{1 \times 1}$ in Figure 4.11.

Table 4.2: S-parameters for $Z_L = 100\ ohm$ after de-embedding operation.

Frequency	S_{11} (mag< angle)
20.00 GHz	0.333/-1.297E-7
20.50 GHz	0.333/-5.612E-9
21.00 GHz	0.333/-2.164E-8
21.50 GHz	0.333/4.022E-7
22.00 GHz	0.333/1.390E-7
22.50 GHz	0.333/-3.494E-8
23.00 GHz	0.333/-7.961 E-7
23.50 GHz	0.333/-2.613 E-7
24.00 GHz	0.333/2.057 E-7
24.50 GHz	0.333/1.154 E-7
25.00 GHz	0.333/-5.099 E-7
25.50 GHz	0.333/-5.234 E-7
26.00 GHz	0.333/1.930 E-7
26.50 GHz	0.333/9.115 E-8
27.00 GHz	0.333/3.337 E-7
27.50 GHz	0.333/4.542 E-7
28.00 GHz	0.333/-8.866 E-7
28.50 GHz	0.333/5.046 E-7
29.00 GHz	0.333/-4.527 E-7
29.50 GHz	0.333/3.478 E-7
30.00 GHz	0.333/-1.687 E-7

4.5 Effect of Geometry/material properties on Z_{ant}

In pursuit of the main thesis objective, different lengths and widths of the on-chip dipoles were analyzed through simulation and experimentation for various resistivity substrates to assess the effects of these parameters on Z_{ant} . Standard “lossy Si”, “lossless” quartz and “low loss” Si substrate will be considered.

4.5.1 Lossy Si substrate ($\rho = 10 \text{ ohm-cm}$)

Here, standard digital bulk Si with 10 ohm-cm resistivity is employed as the substrate. The substrate losses must be incorporated in the Ensemble model to establish a reliable simulation setup. The conductivity of the substrate is related to the resistivity by $\sigma = \frac{1}{\rho}$. The loss tangent ($\tan \delta$) can be calculated through a simple equation in terms of conductivity [43].

$$\tan \delta = \frac{\sigma}{\omega \epsilon} \quad (4-5)$$

At 24 GHz, equation (4-5) yields $\tan \delta = 0.624$. The accuracy of this result has been verified by comparing the calculated loss tangents of different resistivity substrates with the measured loss tangents. These substrates were measured at CRC (Communication Research Center) labs for ϵ_r and $\tan \delta$ using a 30 GHz free space (quasi-optical) setup [44]. Table A.1 in Appendix ‘A’ shows an acceptable agreement between the calculated and measured loss tangent, thus verifying the accurate representation of substrate losses by equation (4-5) in the Ensemble model.

a. 0.1 mm x 1.5 mm on-chip dipole antenna

The antenna plus balun structure with a width of 0.1 mm and length of 1.5 mm was simulated in Ensemble from 20-30 GHz. The simulation predicts a return loss of more than 25

dB at 24 GHz, as shown in Figure 4.12. The realized antenna was measured using the setup discussed in section 3.5.3 of Chapter 3 and the measured return loss is shown in Figure 4.13. A sharp notch is observed at 24.9 GHz. Returning to the simulated antenna, its impedance (Z_{ant}) after the de-embedding conversion from Z_{in} is shown in Figure 4.14. The simulator predicts a Z_{ant} magnitude of 36.8 ohm at 24 GHz, whereas measured results show Z_{ant} magnitude to be 30.2 ohm. The measured antenna impedance after the de-embedding operation is shown in Figure 4.15.

A comparison of simulated and measured return loss is shown in Figure 4.16a. There is slight deviation between the simulated and measured resonant frequency and a deeper null is observed in the measured results. This difference is thought to be attributable to the presence of the metal chuck beneath the wafer, which acts as a ground plane during the measurement. Moreover, the simulation model employs a black box to provide an ideal short circuit to the CPS terminal, whereas the ground pins of the wafer probes provide the short circuit to the realized balun. Nonetheless, simulation provides a fairly accurate estimate of the return loss. Figure 4.16b shows the simulated and measured antenna impedance after the de-embedding operation. In general, agreement between the two sets of curves is good. The deviation between the predicted and measured Real $\{Z_{\text{ant}}\}$ is within 5 Ω . The imaginary $\{Z_{\text{ant}}\}$ has a deviation of about 10 Ω (approximately 0.6 pF or 0.07 nH) at 24 GHz. This is thought to be due to the simplified substrate loss assumption in the antenna model for simulation and the transformer de-embedding using standard low-loss transmission line equations. Nevertheless, the agreement between the simulation and measurement is acceptable.

Figure 4.12 Simulated return loss for 0.1x1.5 antenna on 10 ohm-cm Silicon.

Figure 4.13 Measured return loss for 0.1x1.5 antenna on 10 ohm-cm Silicon.

Figure 4.14 Simulated antenna impedance for 0.1x1.5 antenna on 10 ohm-cm Si.

Figure 4.15 Measured antenna impedance for 0.1x1.5 antenna on 10 ohm-cm Si.

Figure 4.16 Comparison of simulated and measured (a) return loss (b) antenna impedance.

b. 0.5 mm x 1.5 mm on-chip dipole antenna

The width of the antenna structure is increased from 0.1 mm to 0.5 mm in this case with the same arm length as that of the first case. The simulated and measured return loss, as shown in Figures 4.17 and 4.18, has not changed much but the antenna impedance has decreased. Figures 4.19 and 4.20 shows the simulated and measured Z_{ant} . At 24 GHz the simulation predicts a Z_{ant} magnitude of 29.4 ohm whereas measurement shows it to be around 26 ohm, which is excellent agreement.

Figure 4.17 Simulated return loss for 0.5-1.5antenna on 10 ohm-cm Si.

Figure 4.18 Measured return loss for 0.5-1.5antenna on 10 ohm-cm Si.

Figure 4.19 Simulated antenna impedance for 0.5-1.5 antenna on 10 ohm-cm Si

Figure 4.20 Measured antenna impedance for 0.5-1.5 antenna on 10 ohm-cm Si.

Thus, increasing the width of the dipole arm on this substrate tends to decrease the antenna impedance, but this lower impedance is achieved at the cost of the antenna acquiring more space on the chip.

c. 0.1 mm x 1.6mm on-chip dipole antenna

In this configuration, the arm length of the dipole is increased from 1.5 mm to 1.6 mm whereas the width is 0.1mm. The simulated and measured return loss is shown in Figures 4.21 and 4.22. As expected, the resonant frequency has decreased because of the increased arm length. Moreover, a weaker resonance is observed in this case. Figures 4.23 and 4.24 show the simulated and measured Z_{ant} . Agreement at 24 GHz is somewhat poorer than before with the simulation predicting a Z_{ant} magnitude of 38 ohm and measured results showing it to be 46 ohm. One of the probable reasons can be the inconsistency during the microwave measurements caused by the rotation of the chuck in order to measure this particular antenna. The location of this antenna (0.1 mm x 1.6 mm) on the wafer is orthogonal to that of the other two antennas (0.1 mm x 1.5 mm and 0.5 mm x 1.5 mm), therefore the wafer has to be rotated in order to measure it after measuring the other two antennas. Nonetheless, this means that increasing the length of the dipole arm can cause the Z_{ant} to increase.

Figure 4.21 Simulated return loss for 0.1-1.6 antenna on 10 ohm-cm Si.

Figure 4.22 Measured return loss for 0.1-1.6 antenna on 10 ohm-cm Si.

Figure 4.23 Simulated antenna impedance for 0.1-1.6 antenna on 10 ohm-cm Si

Figure 4.24 Measured antenna impedance for 0.1-1.6 antenna on 10 ohm-cm Si.

4.5.2 Loss less quartz substrate

The same antenna and de-embedding structures are realized on quartz to observe the effect of lossless substrate on antenna parameters. Since this is near enough a lossless case, $\tan\delta$ is set to zero in the Ensemble model. The simulation, measurement and de-embedding set up is the same as for the lossy silicon case. The NiCr resistors are measured and corrected for skin depth effect in a similar fashion as well, yielding $R_{L1} = 25.885 \text{ ohm}$, $R_{L2} = 14.885$. Also, analysis of the measured results yields the following values for the balun CPS line:

$$\alpha = 0, \quad \beta = 978 \text{ rad/m},$$

$$Z_o = 70 \Omega$$

a. 0.1 mm x 1.5 mm on-chip dipole antenna

The antenna structure with a width of 0.1 mm and length of 1.5 mm on quartz substrate is simulated for a frequency range of 20-30 GHz. The simulated and measured return loss for this geometry is shown in Figure 4.25 and 4.26. It is evident from the return loss plots that the antenna shows no resonance in the entire frequency range. It is because this particular antenna configuration is designed to resonate at 24 GHz on lossy silicon substrate, which has a different relative permittivity ($\epsilon_r = 11.9$) than quartz ($\epsilon_r = 3.78$). The resonance frequencies of antennas on these substrates, therefore, will be different. Figures 4.27 and 4.28 show the simulated and measured Z_{ant} after the de-embedding operation.

Figure 4.25 Simulated return loss of 0.1-1.5 antenna on quartz.

Figure 4.26 Measured return loss of 0.1-1.5 antenna on quartz.

Figure 4.27 Simulated Antenna impedance of 0.1-1.5 antenna on quartz.

Figure 4.28 Measured Antenna impedance of 0.1-1.5 antenna on quartz.

The real part of Z_{ant} is very small and almost flat, whereas the imaginary part of Z_{ant} varies uniformly in the entire frequency range. The simulation predicts a Z_{ant} (mag) of 58.1 Ω and the measured results show it to be 65.4 Ω . There is relatively good agreement between the simulated and measured results. The deviation between predicted and achieved results can be attributed to the simulation, which neglects several small losses associated with the measurement setup.

b. 0.5 mm x 1.5 mm on-chip dipole antenna

The width of the dipole arms is increased from 0.1 mm to 0.5 mm in this case keeping the arm length constant. The simulated and measured return loss is shown in Figures 4.29 and 4.30, whereas Figures 4.31 and 4.32 show the simulated and measured antenna impedance. The antenna impedance follows the same pattern as in the previous case, except that the Z_{ant} (Mag) has decreased from 65.4 Ω to 43.2 Ω . The trend of lower impedance for wider dipole arms was also observed for antennas on lossy Si substrate.

c. 0.1 mm x 1.6 mm on-chip dipole antenna

The arm length of the dipole is increased from 1.5 mm to 1.6 mm whereas the width is 0.1 mm in this case. The simulated and measured return loss is shown in Figures 4.33 and 4.34, whereas Figures 4.35 and 4.36 show the simulated and measured antenna impedance. It can be seen that the measured Z_{ant} (Mag) has increased to 105 ohm. The longer dipole arms displayed higher impedance in the case of lossy Si substrate as well. It means that the variation pattern of antenna impedance with geometry is consistent for both quartz and lossy Si substrates.

Figure 4.29 Simulated return loss of 0.5-1.5 antenna on quartz.

Figure 4.30 Measured return loss of 0.5-1.5 antenna on quartz.

Figure 4.31 Simulated antenna impedance of 0.5-1.5 antenna on quartz.

Figure 4.32 Measured antenna impedance of 0.5-1.5 antenna on quartz.

Figure 4.33 Simulated return loss for 0.1-1.6 antenna on quartz.

Figure 4.34 Measured return loss for 0.1-1.6 antenna on quartz.

Figure 4.35 Simulated antenna impedance for 0.1-1.6 antenna on quartz.

Figure 4.36 Measured antenna impedance for 0.1-1.6 antenna on quartz.

4.5.3 Low Loss Silicon substrate (Resistivity = 300 ohm-cm)

This section consists of simulation results only because of the unavailability of low loss Si substrates. Since the previous simulated and measured results for antennas on lossy and lossless substrates were in good agreement, the simulation results can be considered reliable enough to predict the antenna performance on low loss substrate. The calculation of loss tangent using equation (4-5) yields $\text{Tan}\delta = 0.02$ at 24 GHz.

a. 0.1 mm x 1.5 mm dipole antenna

The antennas on low loss substrate show a more distinct resonance than the lossless case, as indicated by the sharp dip at 28 GHz in Figure 4.37. The simulated antenna impedance, shown in Figure 4.38, predicts a Z_{ant} (Mag) of 43.1Ω at 24 GHz.

Figure 4.37 Simulated return loss for 0.1-1.5 antenna on low loss substrate.

Figure 4.38 Antenna impedance for 0.1-1.5 on low loss substrate.

b. 0.5 mm x 1.5 mm dipole antenna

The return loss for this geometry is shown in Figure 4.39, whereas antenna impedance is shown in Figure 4.40. The simulator predicts a Z_{ant} (Mag) of 39.29 ohm at 24 GHz. As in the lossy substrate case, widening the dipole arms slightly reduces both the resonance frequency and the antenna impedance.

Figure 4.39 Simulated return loss for 0.5-1.5 antenna on low loss substrate.

Figure 4.40 Antenna impedance for 0.5-1.5 antenna on low loss substrate.

c. 0.1 mm x 1.6 mm dipole antenna

The return loss for this geometry is shown in Figure 4.41. Consistent with the previous results, resonant frequency is lower and Z_{ant} is higher for the longer dipole arms. The simulator predicts the Z_{ant} (Mag) to be 54.1 ohm, as shown in Figure 4.42.

Figure 4.41 Simulated return loss for 0.1-1.6 antenna on low loss substrate.

The simulation results for antennas on low loss Si substrate show that the resonance frequency is higher as compared to that of the antennas on lossy Si but the variation of antenna impedance with respect to the geometry varies in similar fashion to the previous two cases.

Figure 4.42 Antenna impedance for 0.1-1.6 antenna on low loss substrate.

4.6 Discussion and conclusion

Table 4.3 and Table 4.4 show the antenna impedance variation with respect to antenna geometry and material properties for the simulated and measured cases respectively. From the results, the antenna impedance (25-100 ohm range) is suitable for direct integration to the interfacing circuits as described in Section 4.2. Furthermore, the impedance can be modified by adjusting the length and width of the antenna arms. The longer dipole arms display higher Z_{ant} , whereas increasing the width of the dipole arm causes the Z_{ant} to decrease. It is also evident that the impedance sensitivity to antenna dimensions is greater in the low loss and lossless substrates, providing better design flexibility.

Table 4.3: Simulated antenna impedance for varying geometry on different resistivity substrates

Substrate Resistivity ohm-cm	Width *Length mm	Antenna Impedance (Mag) ohm
10 (Lossy)	0.1 *1.5	36.79
	0.1*1.6	37.64
	0.5*1.5	29.41
300 (Low Loss)	0.1 *1.5	43.17
	0.1*1.6	54.1
	0.5*1.5	39.29
Quartz (Loss less)	0.1 *1.5	58.13
	0.1*1.6	70.1
	0.5*1.5	25.17

Table 4.4: Measured Antenna impedance for varying antenna geometry on different resistivity substrates

Substrate Resistivity ohm-cm	Width *Length mm	Antenna Impedance (Mag) ohm
10 (Lossy)	0.1 *1.5	30.23
	0.1*1.6	48.32
	0.5*1.5	25.49
Quartz (Loss less)	0.1 *1.5	65.4
	0.1*1.6	105
	0.5*1.5	43.28

Chapter 5 Study of Gain of On-chip Dipole Antennas

5.1 Introduction

The final quantity needed to characterize Si integrated antennas for air transmission is antenna gain. The antenna gain G_{ant} is defined with respect to the intensity of an isotropic source radiating in free space by

$$G_{\text{ant}} = \frac{\text{(antenna radiation intensity)}}{\text{(isotropic source intensity)}} \quad (5-1)$$

for identical input powers and is generally evaluated at the peak of the radiation pattern. The goal of this chapter is to determine the gain of the 24 GHz on-chip dipole antennas under consideration, and observe the effects of relative permittivity, conductivity of substrate and geometry variation on the gain. This will be done by first establishing an appropriate measurement and gain calibration technique. Based on the results obtained the air transmission range for various Si antennas will be assessed.

5.2 On-chip Dipole Gain

5.2.1 Standard Antenna Gain Measurement Procedure

The most common method to measure the radiation pattern/gain of an antenna is to use a far-field test range. The range consists of transmit and receive towers, separated by a known distance R , such that the antennas are in the far field regions of each other. The towers can be set up outdoors in an open field, or indoors in an anechoic chamber, whose walls are aligned with absorber material to prevent unwanted scattered signals from interfering with the measurement.

The antenna under test (AUT) is usually mounted as the receive antenna and the source antenna is transmitting. The AUT is mounted on a tower, which typically contains positioners for varying the azimuth and elevation angles of the antenna. To characterize the performance of most antennas, pattern cuts are usually taken in the two principle planes (the E-plane and the H-plane).

The technique described above can be used to measure the relative power pattern of the AUT, from which many useful parameters can be obtained such as the beam width, maximum relative side lobe levels, and the directivity of the antenna. This technique produces the antenna's radiation patterns, it however, does not measure the absolute gain of the antenna. In other words, it does not account for any ohmic, dielectric and impedance mismatch losses in the antenna. In order to obtain the gain of the antenna, the gain-transfer method is generally adopted.

The gain-transfer method requires an antenna gain standard, i.e. an antenna whose gain has already been determined. In this method, the antenna gain standard (with a gain of G_{st}) is first mounted on the receive tower and the received power level (P_{st}) is recorded at the position where the antenna's beam peak is aligned with the source antenna [45]. The AUT is then mounted so that its beam peak is aligned to the source antenna and the received power level (P_{aut}) is recorded. The difference in received power levels between the gain standard and the AUT represents the difference in gain between the two antennas:

$$G_{aut} [\text{dB}] = G_{st} [\text{dB}] + (P_{aut} [\text{dBm}] - P_{st} [\text{dBm}]) \quad (5-2)$$

5.2.2 Challenges in on-chip dipole gain measurement

There are multiple problems in executing the standard gain measurement procedure for the 24 GHz on-chip dipoles of this work.

- a. On-chip dipoles are fed using wafer probes, unlike other antennas with co-axial or other standard connectors. The probe tips are very sensitive and may get damaged during the AUT movement.
- b. The Si wafers are fragile unlike other common antenna substrates. There is a higher probability that a silicon wafer may be scratched or broken during measurement.
- c. A microscope is essential to accurately contact the miniature on-chip antenna structures with the probes. In general, a microscope is not part of the standard equipment in an anechoic chamber. Furthermore, the presence of a microscope may affect the antenna radiation pattern or block the movement of AUT.
- d. A special test fixture must be designed and fabricated in order to mount the on-chip dipole in the anechoic chamber and measure its radiation pattern and gain.

Due to these complexities, most of the on-chip antennas are characterized for forward transmission gain only, which is just the S_{21} between two on-chip antennas [5]. It is only a measure of transmission through the substrate and does not provide any information regarding the transmission through air. Very little work has been done thus far to characterize the on-chip antennas for air transmission.

5.2.3 On-chip dipole gain calibration technique

In order to alleviate the above problems, a simple air transmission gain estimation technique has been developed, based on the 24 GHz measurement set up shown in Figure 5.1. Here, the on-chip antenna is placed on a probe station and fed from port 1 of the network analyzer. The radiated signal is received (at bore sight) by a horn antenna placed 40 cm above

the on-chip dipole and connected to port 2 of the analyzer. GSG wafer probes having a 150 μm pitch are employed, with accurate placement provided by means of a moveable microscope. Measurement is done in a low interference chamber, where the walls are lined with absorbing material.

The dipole antennas to be measured are realized on both low loss quartz substrates and lossy silicon substrates. Since the quartz based antenna EM simulations were previously found to agree well with measurements (in terms of their input impedance) as shown in Figures 4.27 and 4.28 of Chapter 4, the simulated gain values of these same antennas were considered to be accurate. They are therefore taken as the reference for subsequent lossy Si antenna gain measurements. The transmission (S_{21}) between the AUT and the horn antenna is first measured for antennas on low loss quartz. Then the S_{21} between AUT and the horn is measured for the dipole on lossy Si substrate. For system impedance matched antennas, the difference in transmission levels between the two cases represents the difference in their gain values. Given that the gain of the antenna on low loss material is known, the gain of the AUT on lossy material is easily found. However, an important correction factor must be applied for typical on-chip antennas that are not matched to the system impedance. In essence, the reflected powers need to be taken into account.

Figure 5.1 Gain measurement setup.

5.3 Effect of geometry/material properties on antenna gain

5.3.1 Lossless quartz substrate

The 0.1 mm x1.5mm antenna on quartz will be used as the reference antenna for gain estimation. The simulated radiation pattern and the gain at 24 GHz are shown in Figure 5.2. Simulation predicts a single lobe radiation pattern at boresight, as expected. The gain for dipole on quartz is -3.5 dBi from the simulator whereas the measured S_{21} between this antenna and the horn antenna is -15.3 dB as shown in Figure 5.3. Incidentally, the dipole gain is expected to be low even though a nearly lossless substrate is employed. The antenna is in close proximity to the underlying ground plane and its radiation is comparable to that of an open-circuited microstrip line.

Figure 5.2 Simulated radiation pattern for 0.1x1.5 dipole on quartz.

Figure 5.3 Measured S_{21} for 0.1-1.5 antenna on quartz.

The measured S_{21} is corrected for the mismatch loss ($S_{11} = -1.81$ dB) at 24 GHz. The difference between the corrected S_{21} and the simulated gain value is 7.3 dB. This factor can now be utilized to estimate the gain of dipoles on lossy silicon.

5.3.2 Lossy silicon substrate ($\rho = 10\text{ohm-cm}$)

a. 0.1 mm x 1.5 mm on-chip dipole antenna

The measured S_{21} between the dipole on lossy silicon and the horn antenna is -20.6 dB as shown in Figure 5.4. Since there is negligible mismatch loss ($S_{11} < -20$ dB), the measured S_{21} is not corrected in this case. However, the measured S_{21} is compensated by the 7 dB factor obtained from the lossless case. The resulting gain of dipole and the integrated balun structure is -13 dBi. Finally, the loss in the balun structure must be subtracted from the total gain in order to obtain the on-chip dipole gain. Losses in the balun structure ($S_{21} = -3.5$ dB) were estimated through the isolated balun structure of Figure 4.9 of Chapter 4. Thus, the gain of on-chip dipole is found to be $(-13 + 3.5) = -9.5$ dBi.

b. 0.1 mm x 1.6 mm on-chip dipole antenna

The measured S_{21} between this dipole configuration and the horn antenna at 24 GHz is -22.16 dB, as shown in Figure 5.5. Again, the measured S_{21} is compensated by the 7 dB factor obtained from the lossless case. The resultant gain of dipole and the integrated balun structure is -15 dB. Finally, the loss in the balun structure ($S_{21} = -3.5$ dB) must be subtracted from the total gain in order to obtain the on-chip dipole gain. Thus, the gain of on-chip dipole is found to be -11.5 dBi.

Figure 5.4 Measured S_{21} of 0.1-1.5 antenna on lossy Si

Figure 5.5 Measured S_{21} of 0.1-1.6 on dipole on lossy Si.

c. 0.5 mm x 1.5 mm on-chip dipole antenna

The measured S_{21} between this dipole configuration and the horn antenna at 24 GHz is -18.18 dB, as shown in Figure 5.6. Going through similar analysis as that of the previous two cases, the resultant gain of dipole and the integrated balun structure is found to be -11.8 dB. Finally, the loss in the balun structure ($S_{21} = -3.5$ dB) is subtracted from the total gain in order to obtain the on-chip dipole gain. Thus, the gain of on-chip dipole is found to be -8 dBi.

Figure 5.6 Measured S_{21} of 0.5-1.5 antenna on lossy Si.

From the results, it is observed that the wider antenna exhibits the maximum gain out of the three antennas. The ripples in the measured results can be attributed to reflections in the free space measurement setup.

5.3.3 Low Loss silicon substrate ($\rho = 300\text{ohm-cm}$)

After establishing the simulator reliability for lossless conditions and devising the procedure for on-chip gain calculations, we can extrapolate gain numbers for low loss substrate conditions from the simulated results. Losses in the balun structure ($S_{21} = -0.5\text{ dB}$) were estimated through the isolated circuit of Figure 4.9 of Chapter 4, with a different $\text{Tan}\delta$ in this case. Going through similar analysis for the $0.1\text{ mm} \times 1.5\text{ mm}$ antenna, the gain from simulator (antenna + balun) = -5.2 dBi and thus the gain of the on-chip dipole ($-5.2 + 0.5$) = -4.7 dBi . For the $0.1\text{ mm} \times 1.6\text{ mm}$ cases, the dipole gains are -4.8 dBi and -4.6 dBi , respectively.

5.3.4 Discussion

All the antenna gain results of this section are summarized in table 5.1. Although small geometry changes can have a significant effect on antenna impedance (as seen in Chapter 4), one expects only minimal variations of the antenna gain with the minor geometrical changes done here. This is observed in the simulations for low loss and lossless substrate antennas. The gain values vary by less than 0.3 dB , except for the last table entry (0.5×1.5 quartz antenna), which is considered to be an anomaly.

Compared to the lossless substrate case, the antennas on low loss Si exhibit approximately 1 dB lower gain. This is consistent with the fact that the substrate losses cannot be considered negligible.

The gain results of the antennas on lossy silicon are the only ones to have been determined experimentally. It is therefore acceptable to observe a greater variation in these values, especially given the simple nature of the measurement apparatus. It would be necessary to measure the radiation patterns of the antennas to fully verify their behavior. However, it may be stated that increased antenna gain is achievable by widening the dipole arms.

From the measured data, a designer may choose between an area efficient (0.1x 1.5 mm) antenna or one that provides greater gain (0.5x1.5 mm) antenna. At 24 GHz, increasing the substrate resistivity from 10 to 300 Ω -cm improves antenna gain by approximately 5 dB. By investigating the same antennas on extremely high resistivity substrate (quartz), the improvement in gain is only a further 1 dB, suggesting that the 300 Ω -cm substrate is a better compromise between performance, level of integration and cost.

Table 5.1: Antenna gain for varying geometry on different resistivity substrates

Substrate Resistivity (Ohm-cm)	w x l mm	Antenna Gain (dBi)
Lossy Si 10ohm-cm	0.1x1.5	-9.5
	0.1x1.6	-11.5
	0.5x1.5	-8
Low loss Si 300ohm-cm	0.1x1.5	-4.7
	0.1x1.6	-4.8
	0.5x1.5	-4.6
Lossless >10000ohm-cm Quartz	0.1x1.5	-3.5
	0.1x1.6	-3.8
	0.5x1.5	-2.3

5.4 Air Transmission Range

It is now possible to assess the system implications of the thesis results [2]. Consider the system as shown in Figure 5.7 where the stand-alone transceiver (SAT) with on-chip antenna (on 10 Ω -cm substrate) is to be linked with the “base-station”. First the receive path is considered. Using Friis’ transmission equation, the receive power P_r is given by

$$P_r = P_t G_t G_r \left(\frac{\lambda}{4\pi D} \right)^2 \quad (5-3)$$

where P_t is the transmitter power, G_t and G_r are the antenna gain of the transmitter and the receiver respectively, and D is the distance between the transmitter and the receiver. Assume the system requires a dynamic range of 50 dB and a bandwidth B of 1 MHz for both receive and transmit operations. The receiver thermal noise is kTB , where k is the Boltzman constant and T is the temperature. At T of 290 K, kT is -174 dBm/Hz, and the system thermal noise floor is -114 dBm. Assume the receiver has NF of 8dB and the base-station has P_t of 20 dBm and G_t of 10 dBi. This results in a maximum receive range of 6 m. For the transmitter, assume the SAT is able to deliver 10dBm, and the base station has NF of 5 dB and G_r of 10 dBi. This results in maximum transmit range of 2.7 m. Finally, using an antenna on a 300 Ω -cm substrate can result in at least 2 times improvement in transmission range compared to a 10 Ω -cm substrate.

Figure 5.7 Transceiver system: transmit and receive path [2].

5.5 Conclusion

A novel gain calibration technique has been developed for on-chip antennas on lossy substrates. The effects on gain of a number of geometrical and substrate parameters have been studied for 24 GHz on-chip antennas. The results show that a gain improvement of approximately 5 dB is possible by increasing the Si substrate resistivity from 10 Ω -cm to 300 Ω -cm.

Chapter 6 Thesis Conclusions, Contributions and Future Work

6.1 Conclusions

In this thesis, the conditions have been investigated under which standard digital bulk Si technology can yield efficient on-chip antennas for fully differential transceiver implementations. The effects of the IC material properties and the antenna geometry on radiation and impedance characteristics have been studied. 24GHz on-chip antennas on lossy Si have been successfully demonstrated, using a standard IC fabrication compatible Cu process.

Some background on the integrated antenna concepts was first presented for a better understanding of their nature. This review highlighted the areas, which have to be improved upon. An insight into integrated antenna systems helped in establishing the design considerations and objectives for this thesis. A number of calibration, measurements and de-embedding techniques were also investigated in order to devise simple and accurate methods for microwave measurement and analysis.

Since the differential dipole must be integrated into a balanced mode transceiver, an appropriate balun structure was designed to feed the dipole differentially and still obtain single ended S-parameters. This balun design was realized in Ansoft Ensemble (EM Simulator) through S-parameter black boxes and coplanar strips (CPS). Validation of the balun design in Ensemble was carried out by simulating the same structure in a circuit based simulator ADS. The Cu balun and NiCr resistors were realized on lossy Si substrate using standard IC fabrication process. The

standard wafer probe pad configuration was modified to measure a GS (ground signal) balun structure with a GSG (ground signal ground) probe. The characteristic impedance and propagation constant for the balun structure were extracted from the experimental results.

Various antenna geometries and calibration/de-embedding structures were realized on lossy Si and lossless and quartz substrates. The feed point impedance for the on-chip antenna and the integrated balun structure was obtained through the measured results. A simple de-embedding technique was developed to de-embed the balun S-parameters from the measured results and extract Z_{ant} . Analysis of the results revealed that the wider the dipole arms, the lower is the antenna impedance and likewise, the longer the antennas, the higher is the antenna impedance. A good agreement between the simulated and measured results established the reliability of the simulation setup in order to predict the antenna performance on 300 Ω -cm resistivity Si substrate. The antenna impedance (25-100 Ω) range is suitable for direct integration to the interfacing circuits. Z_{ant} can be modified by adjusting the length and width of the antenna arms. Impedance sensitivity to antenna dimensions is greater for the high resistivity substrates, providing better design flexibility.

Standard antenna radiation pattern/gain measurement technique could not be adapted for the on-chip antenna because of the limitations in the measurement setup and unavailability of a special test fixture. Nevertheless, a simple gain calibration technique for air transmission was employed utilizing the antenna on lossless quartz as the reference antenna. The S_{21} between the on-chip antennas and a 24 GHz horn antenna was measured and the result was corrected for the balun losses and the error factor from the lossless case. The on-chip antennas were successfully characterized for air transmission gain.

The radiation characteristics from the simulator predicted single lobe pattern at bore sight. Wider antenna displayed the maximum gain out of the three realized antennas. From the measured data, a designer may choose between an area efficient ($l = 1.5\text{mm}$, $w = 0.1\text{mm}$) or one that provides greater gain ($l = 1.5\text{mm}$, $w = 0.5\text{mm}$). At 24 GHz, increasing the substrate resistivity from $10\ \Omega\text{-cm}$ to $300\ \Omega\text{-cm}$ improves the gain by about 5 dB. The air transmission range is almost double in case of $300\ \Omega\text{-cm}$ substrate. By further increasing the resistivity, the improvement in gain is only marginal, suggesting that the 300ohm-cm substrate is a better compromise between performance, level of integration and cost. The study of performance trade-offs versus on-chip dipole parameters in this thesis indicates the great potential to integrate these antennas into current VLSI technology for wireless communication and wireless interconnects.

6.2 Thesis contributions

A simple on-chip planar balun structure has been designed and experimentally verified to test 24 GHz balanced mode integrated antennas. The design is superior to previous configurations, as it contains no vias, air bridges or bond wires, and is fabricated in a single metallization process.

Silicon integrated differential dipole antennas have been characterized for different substrates and geometries. The results quantify for the first time the tradeoffs between the design parameters, antenna impedance and achievable antenna gain for air transmission.

A suitable de-embedding technique has been developed using a standard microwave circuit simulator to obtain antenna impedance from the single ended S-parameters. In addition, a gain calibration technique has been devised for on-chip antennas on lossy substrates.

6.3 Future Work

The main goals and objectives of this thesis have been achieved; however other experimental issues regarding on-chip antennas on Si substrate still need to be addressed. For instance, the antennas must be physically realized on the 300 Ω -cm substrate to verify the accuracy of simulated results. The de-embedding technique has limitations because of the inability of the ADS simulator to incorporate complex characteristic impedance of the balun structure. A more accurate de-embedding technique, which can handle complex characteristic impedance issues for lossy substrates should be developed. The radiation pattern of the on-chip antennas should also be measured. A suitable test fixture should be designed for radiation pattern/ gain measurement of on-chip antennas in the anechoic chamber. Finally, the technique to realize NiCr resistors on Cu structures must be improved for accurate resistor values.

Further investigations can be to realize these antennas on HR (high resistivity) and SOI substrates and gauge the improvement in antenna performance. These antennas can be used for simple chip RF systems in biomedical applications such as radiotherapy to treat cancer. In such case Cu metallization is a wrong choice because it can be hazardous to human organs. Furthermore, if the SAIS (stand alone integrated systems) is used for environmental monitoring or detecting high-energy radiation, even then Cu is not a good choice because it corrodes very fast. Therefore, future on-chip antenna work should investigate other metals like silver and compare their performance in terms of efficiency, gain and durability with Cu antennas. Finally, to take maximum advantage out of wafer space, multiple antennas can be designed on top and back of the wafer, depending on the application. Integrated antennas is a fast growing field and

future developments in this technology can fundamentally change microwave/millimeter wave communications.

APPENDIX A Loss Tangent verification

Measured loss tangent values of different resistivity Si substrates have been obtained at 30 GHz from [44], whereas the calculated values have resulted from equation (4-6). The error between measured and calculated values is within 10 percent.

Table A.1: Comparison of calculated and measured loss tangents for different substrates

Resistivity ohm-cm	Measured Loss Tangent	Calculated Loss Tangent	Percentage Error
18	0.303	0.279	7.9
37	0.145	0.136	6.2
300	0.017	0.0167	1.76
620	0.0088	0.0081	7.95

APPENDIX B Antenna Fabrication Process Sheet

Run #6:

Table B.1: Masks

#	Lable
1	CU-233-02 NiCr resistors
2	CU-233-01 Copper antennas

Table B.2: Wafers

#	Scribed as	Resistivity, Ωcm	Type	Oxide, μm	Polyimide, μm
1	Quartz wafer				
2		1-10	P	3	-
3		1-10	P	3	-

Table B.3: Process flow

#		Notes
1	PR processing Wafers pre-bake (30 min at 250 °C) HMDS (1 krpm; 15 sec; 1k rpm; 30 sec) Soft bake (102 °C; 1 min) LOR 10B (ramp up to 1 krpm; 15 sec; 1k rpm; 30 sec) Wait (5 min) Bake (185 °C; 5 min) S1811 (1 krpm; 10 sec; 4k rpm; 30 sec) Soft bake (102 °C; 1 min) Mask #1 (no aligning) Expose (27 sec) Develop (60 sec; MF321) Rinse (DI; 1 min) No Postbake Descum (1 min; 100 W; 0.3 Torr; oxygen plasma)	
2	NiCr sputtering : NiCr - 2000 A	

#		Notes
3	Lift-off In 1165 at 60°C in Ultrasonic (30 min) Rinse (10 min)	
4	PR processing Wafers pre-bake (30 min at 250 °C ????) HMDS (1 krpm; 15 sec; 1k rpm; 30 sec) Soft bake (102 °C; 1 min) LOR 10B (ramp up to 1 krpm; 15 sec; 1k rpm; 30 sec) Wait (5 min) Bake (185 °C; 5 min) S1811 (1 krpm; 10 sec; 4k rpm; 30 sec) Soft bake (102 °C; 1 min) Mask #2 alignment Expose (27 sec) Develop (60 sec; MF321) Rinse (DI; 1 min) No Postbake Descum (1 min; 100 W; 0.3 Torr; oxygen plasma)	
5	Cu sputtering : Ti - 200 Å Cu – 1.9 µm	
6	Lift-off In 1165 at 60°C in Ultrasonic (30 min) Rinse (10 min)	

APPENDIX C Matlab codes

C.1 Matlab code for antenna impedance

```
real_a = [  
0.49447895  
0.443245451  
0.436858256  
0.416539361  
0.398010681  
0.388568327  
0.350343897  
0.338339325  
0.317775263  
0.270187368  
0.265519391  
0.258066069  
0.223803956  
0.186733902  
0.115252655  
0.05491155  
-0.01036261  
-0.079850067  
-0.155486424  
-0.23734885  
-0.323577959];
```

```
img_a= [  
-0.71161371  
-0.721740453  
-0.733423477  
-0.748914971  
-0.757425219  
-0.776366727  
-0.80585215  
-0.81161371  
-0.821740453  
-0.833423477  
-0.848914971  
-0.857425219
```

```

-0.876366727
-0.895852158
-0.94610391
-0.947863706
-0.945401079
-0.93770106
-0.92312045
-0.899747422
-0.865840086];

```

```

x = [20000000000
20500000000
21000000000
21500000000
22000000000
22500000000
23000000000
23500000000
24000000000
24500000000
25000000000
25500000000
26000000000
26500000000
27000000000
27500000000
28000000000
28500000000
29000000000
29500000000
30000000000 ]/(1*10^9);

```

```

Sant=[];
for b=1:21
    Sant = [Sant ;real_a(b)+ j*img_a(b)];
end
Sant

```

```

Zant = 50 * ((1+Sant)./(1-Sant))

```

```

plot(x,real(Zant),'k');grid on;
hold on
plot(x,imag(Zant),'b-.');

```

hold off

```
XMIN = 20;  
XMAX = 30;  
YMIN=-100;  
YMAX =40;
```

```
AXIS([XMIN XMAX YMIN YMAX])
```

```
title('Quartz');  
xlabel('Frequency (GHz)');  
ylabel('Antenna Impedance(ohm)');  
Legend('Real','Imaginary');  
hold off
```


C.2 Matlab code for CPS balun dimensions

```
a= 50 *10^(-6);
b= 432*10^(-6);
h=0.3*10^(-3);
l=1.34*10^(-3);
Epsr=11.9;

resistivity = 0.1;
lambda_0=12.5*10^(-3);

Eps=Epsr *8.85*10^(-12);
omega = 2*pi *24 *10^9;
sigma= 1/resistivity ;
tandelta=sigma/(Eps * omega)
k=a/b;
kp=sqrt(1-(k^2));

k1 = sinh (pi *a/(4*h))/sinh(pi *b/(4*h));
k1p=sqrt(1-k1^2);
Ellip1 = 2 *pi /log(2*(sqrt(1+kp)+(4*kp)^(1/4))/(sqrt(1+kp)-(4*kp)^(1/4)));

Ellip1inv= 1/Ellip1;

Ellip2=2 *pi /log(2 * (sqrt(1+k1p)+(4*k1p)^(1/4))/(sqrt(1+k1p)-(4*k1p)^(1/4)));

q=0.5*Ellip1inv* Ellip2;
Epsef = 1 + (Epsr-1)/2 *q
Zo= 120*pi /sqrt(Epsef) * Ellip1
```

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