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The undersigned recommends to the Faculty of Graduate Studies
and Research, acceptance of the thesis

A NOVEL DYNAMIC AMPLIFIER FOR SWITCHED CAPACITOR FILTERS

as partial fulfillment of the requirements for the degree of
Master of Engineering.

Ma Copeland

Thesis Supervisor

Boothby

Professor and Chairman
Department of Electronics

Department of Electronics.

Carleton University

September 30 1983

A NOVEL DYNAMIC AMPLIFIER FOR SWITCHED CAPACITOR FILTERS

by

①

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Submitted to the
Faculty of Graduate Studies and Research
in partial fulfillment of the requirements
for the degree of
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Department of Electronics
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TABLE OF CONTENTS

ABSTRACT	i
ACKNOWLEDGEMENTS	ii
LIST OF SYMBOLS AND ABBREVIATIONS	iii
LIST OF TABLES	v
LIST OF FIGURES	vi
 CHAPTER 1 INTRODUCTION	 1
1.1 Factors Contributing to Chip Area and Power Consumption	2
1.1.1 Switches	2
1.1.2 Amplifiers	3
1.2 Parallel Switched Capacitor Integrator	5
1.3 Static Amplifier	8
1.4 Introduction to Dynamic Amplifiers	10
1.4.1 Principle of Operation	10
 CHAPTER 2 COMPARISON OF PREVIOUS WORKS	 14
2.1 Dynamic Amplifiers Proposed by Copeland and Rabey	14
2.1.1 Circuit Operation	14
2.1.1.1 Assumptions	14
2.1.1.2 Description	16
2.2 A CMOS Dynamic Amplifier	18
2.2.1 Circuit Operation	18
2.3 Sampled Data Filters Using MOS Current Multipliers	19
2.3.1 Circuit Operation	21
2.4 A Comparison of the Circuits	23

CHAPTER 3	INTRODUCTION TO THE MODIFIED DYNAMIC AMPLIFIER	25
3.1	Circuit Operation	27
3.2	Voltage Gain of Dynamic Amplifier	39
3.3	Second Order Effects in the Dynamic Amplifier	45
3.3.1	Output Offset Voltage	45
3.3.2	Negative Feedback Due to Gate Capacitance	47
3.3.3	Channel Length Modulation	51
3.4	Tetrode Transistor - The Solution for Second Order Effects	52
3.4.1	Miller Effect	55
3.4.2	Channel Length Modulation	55
3.4.3	Output Resistance	57
3.5	Computer Simulation of the Proposed Circuit	58
3.5.1	Results of Computer Simulation	59
3.6	Bread Board Experiments With the Dynamic Amplifier	61
3.6.1	The Necessity of the Experiments	61
3.6.2	Bread Board Construction	61
3.6.2.1	Voltage Monitoring Circuit	62
3.6.3	Experiment	64
3.6.3.1	Open Loop Gain	66
CHAPTER 4	SC INTEGRATED CIRCUIT USING DYNAMPS EXPERIMENTAL RESULTS	67
4.1	Introduction	67
4.2	Filter Specifications	68
4.3	Description of the Test Vehicle	70
4.4	Experiments on the Dynamp Integrated Circuit As An Integrator	75
4.4.1	Open Loop Gain of the Amplifier	75
4.4.4.1	Details of Test Set Up	75
4.4.4.2	Clock Frequency	77
4.4.4.3	Measurements	77
4.4.2	Analysis of the Results	77

4.4.2.1	Positive Saturation Region	80
4.4.2.2	Transition Region	80
4.4.2.3	The Negative Saturation Region	84
4.4.3	Offset Voltage	85
4.5	Measurement of Frequency Response of the Notch Filter	86
4.5.1	Preliminary Set Up	86
4.5.2	Sampling Clock	88
4.5.3	Instrumentation	91
4.6	Experiments and Analysis	91
4.7	Frequency Response of the IC as a Low Pass Filter	93
4.7.1	Analysis of Experimental Results	94
4.8	Frequency Response as a High Pass Filter	96
4.9	Conclusions	98
CHAPTER 5	EFFECT OF FINITE GAIN AND ANALYSIS OF POWER SUPPLY NOISE REJECTION	99
5.1	Introduction	99
5.2	High Pass Filter - Effect of Finite Gain	100
5.3	Effect of Power Supply Noise	101
5.3.1	V _{DD} Noise	102
5.4	Analysis of the Effect of V _{SS} Noise	104
5.5	Measurements	111
5.6	Results	113
CHAPTER 6	CONCLUSIONS	117
6.1	Summary	117
6.2	Conclusion	118
6.3	Suggestions for Future Work	119
REFERENCES		121
APPENDIX 1	Transfer Function With Finite Gain Amplifier	122
APPENDIX 2	Transfer Function For V_{SS} Noise Analysis	125
APPENDIX 3	Transfer Function for Notch Filter	129
APPENDIX 4	Gain Calculation Using SPICE Simulation	

ABSTRACT

Switched capacitor filters have become a standard choice for realizing active filters as monolithic integrated circuits. Conventionally these ICs employ op amps which draw continuous current from the power supplies and take a relatively large amount of silicon area. This thesis presents a new dynamic amplifier which is capable of replacing the conventional op amps in SC filters. The dynamp is based on the principle of dynamic logic devices and hence consumes less power and occupies smaller area than op amps. Details of the characterization of a monolithic SC filter IC which uses the new dynamp also are presented. An attempt is also made to analyze the power supply noise rejection of the circuit.

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LIST OF SYMBOLS AND ABBREVIATIONS

A	Amplifier gain
α	Capacitor ratio in switched capacitor filters
BW	Bandwidth
CMOS	Complementary Metal Oxide Semiconductor
CMOST	CMOS Transistor
C_{ox}	Oxide capacitance of MOST
dynamap	Dynamic amplifier
f	Frequency in Hertz
g_m	Transconductance of MOST
g_o	Output conductance of MOST
r_o	Output resistance of MOST
Hz	Hertz, cycles per second
$H(z)$	Transfer function in the Z domain
IC	Integrated circuit
I_D, I_d	MOST drain current
I/P	Input
K	Gain factor of MOST
L	MOST channel length
MOS	Metal Oxide Semiconductor
MOST	MOS Transistor
O/P, OUT	Output
Op Amp	Operational amplifier
PMOS	P channel MOS
PSR	Power Supply Rejection
Q	Quality factor of filter
SC	Switched capacitor

τ	Time constant
μ	Mobility of charge carriers
V_d, V_D	Drain voltage of MOST
V_{dd}, V_{DD}	Most positive power supply voltage
V_{ds}, V_{DS}	Drain-source voltage of MOST
V_{SS}	Most negative power supply voltage
V_T, V_{TH}	MOST threshold voltage
W	MOST channel width
π	3.14159
ω	$2 \pi f$
Z	Z operator in discrete systems, equal to $e^{j\omega}$

LIST OF TABLES

Table 3.1	Table showing the decay of dynamp's output during the charge transfer phase of the clock	37
Table 3.2	Table showing consecutive output samples of the dynamp for evaluating the gain	44

LIST OF FIGURES

Figure No.	Page
1.1 (a) Parallel Switched Capacitor Integrator	6
(b) 2 Phase Non-Overlapping Clock Wave Form	6
1.2 (a) Circuit Diagram of a Common Source Amplifier	9
(b) Small Signal Model of Common Source Amplifier	9
1.3 (a) Circuit Diagram of Basic Dynamp	12
(b) Waveforms of the Two Phase Non-Overlapping Clock and the Output Signal	12
	12
2.1 (a) Dynamp Proposed by Copeland and Rabey	15
(b) Four Phase Clock Waveform for Copeland's Dynamp	15
2.2 (a) CMOS Dynamp by Hostica	19
(b) Two Phase Clock for Hostica's Dynamp	19
2.3 (a) Model of a Typical Sampled Data Filter	22
(b) Realization of Sampled Data Filter Using Current Multipliers	22
3.1 (a) Copeland's Dynamp Modified to Reduce Threshold Voltage Limitations	26
(b) Timing Diagram of the Required Four Phase Clock	26
(c) Equivalent Circuit of the Modified Dynamp During Charge Transfer Phase	31
3.2 Output and Gate Voltage Waveforms of the Dynamp During ϕ_4 Phase	38
3.3 (a) A NMOS Static Amplifier	40
(b) Small Signal Model for the Static Amplifier	40
3.4 (a) Output Voltage Waveform of Modified Dynamp	42
(b) Gate Voltage Waveform of Modified Dynamp	42
(c) Waveform of the Voltage at the Effective Input of the Modified Dynamp	42
3.5 Output Waveforms Emphasizing the Effect of Offset Voltage	48
3.6 Dynamp Showing the Parasitic Gate Drain Capacitance	49

3.7	(a) Dynamp Output Waveform Showing the Effect of dc Input Voltage	53
	(b) Corresponding Gate Waveform	53
	(c) Corresponding Gate Waveform Showing the Effect of Channel Length Modulation	53
3.8	Circuit Diagram of a Cascode Amplifier	56
3.9	Circuit Diagram of Dynamp, Modified as a Cascode Amplifier	56
3.10	SPICE Simulation Output of Modified Cascode Dynamp	60
3.11	Circuit Schematic for Monitoring the Nodes of Breadboard Model of Modified Dynamp	63
4.1	Circuit Diagram of Active RC Notch Filter	69
4.2	SC Equivalent of Active RC Notch Filter	69
4.3	Circuit Schematic of the SC Integrator Circuit Employing Dynamps	71
4.4	Photomicrograph of the Integrated Circuit	72
4.5	Schematic of a Circuit for Monitoring the Node Voltages of Dynamp ICs	76
4.6	(a) and (b) Dynamp Integrator Input vs Output Characteristics	78, 79
4.7	(a) and (b) Figure 4.6 Expanded Along the X Axis Around 0 Volt Input	81, 82
4.8	Output Voltage vs Tetrode Bias Characteristics of the Modified Dynamp	87
4.9	(a) Schematic Diagram of Test Set Up for Frequency Response Measurements	89
	(b) Timing Diagram of the Four Phase Clock Used After IC Testing	90
4.10	Frequency Response of Dynamp Notch Filter	92
4.11	Frequency Response of Dynamp Low Pass Filter	95
4.12	Frequency Response of Dynamp High Pass Filter	97
5.1	(a) Second Stage of Dynamp IC, Showing Parasitic Capacitors	106
	(b) Typical Output Waveform Showing Sampling Instants	107

5.2	Circuit Model for V_{SS} Noise Analysis	109
5.3	V_{SS} Noise-Frequency Response: Analytical Results	110
5.4	Block Diagram of Test Set Up for Measurement of V_{SS} Noise Rejection	112
5.5	Experimental Results of V_{SS} Noise Rejection Measurements	114
5.6	V_{SS} Noise-Frequency Response: Analytical and Experimental Results Plotted Together	115
A1.1	Second Stage of the Dynamp IC, Showing Finite Gain Amplifier	122
Plate 1. Oscilloscopes of Bread Board Circuit Waveforms		65

Chapter 1

INTRODUCTION

Metal oxide semiconductor (MOS) amplifiers are key elements of the well known sampled analog signal processing circuits called switched capacitor filters. The fact that the general tendency in the industry is to fabricate the switched capacitor filters as monolithic integrated circuits using MOS technology, points out the significance of better understanding of various types of MOS amplifiers which can be used to realize such filters. In general, the work reported in this thesis deals with new MOS amplifiers which are specially meant for switched capacitor filter applications. In particular, this thesis explores the use of so-called dynamic amplifiers in SC filters. A dynamic amplifier is defined here as an amplifier which does not draw continuous current from the power supplies.

The switched capacitor filter was first introduced in 1977 in its present day form [1,2]. The concept raised a lot of research interest among industry and universities around the world, due to the following attractive features of such filters:

1. The filter characteristics depend only on the ratios of capacitor values and not on the absolute capacitances and resistances of the circuit elements. This is contrary to what is seen in active RC circuits.
2. Filter tuning, or modifying the frequency response of

the filter along the frequency axis is easily accomplished by simply varying the switching frequency.

3. Fabrication of the SC filters as monolithic ICs is simpler than that of an active RC filter because of the well known fact that capacitor ratios can be more accurately realized in MOS technology than resistors.

The above factors led to the marriage between SC filters and MOS technology resulting in the availability of SC filter ICs even in the commercial market. However extensive research is still being carried out for widening the area of application and for overcoming any remaining drawbacks of such filters, as can be seen in the literature. This is not surprising because such filters have gained a stable place in the telecommunications industry where filtering in the voice frequency range has many applications. The number of filter circuits employed is so great that a reduction in the power consumption of the circuit, or an increase in the circuit density of the chip will be greatly welcomed.

1.1 Factors Contributing to Chip Area and Power Consumption

1.1.1 Switches

Switched capacitor filters operate on the principle of charging and discharging of various capacitors to different voltages during different time periods, following a preset sequence. These switching sequences are controlled by analog switches belonging to PMOS, NMOS or CMOS technology. Since,

neither these switches nor the waveforms of the voltage pulses driving these switches are ideal, some power dissipation is unavoidable. However, power dissipation, owing to the non ideal characteristics of the switches becomes significant only when the sampling frequency is high enough to make the sampling interval comparable to the charging time constants due to the finite ON resistances of the switches. Besides, today's high speed MOS technologies such as HMOS, ISOCMOS, DMOS etc. offer feasible solutions to this problem to a great extent.

1.1.2 Amplifiers

Switched capacitor filters are built around amplifiers with a high gain and very high input impedance and a settling time high enough for the highest sampling frequency used. For example, the switched capacitor implementation of a commonly used second order filter section known as 'biquad' uses two op amps when SC filters are integrated. These op amps are realized in MOS technology along with the switches and capacitors. The general trend in the industry is to use standard MOS amplifier circuits which are static amplifiers, that is, amplifiers which draw a finite continuous current from the power supplies. This results in considerable power dissipation as high as 13 mW*. Besides, these static amplifiers take a considerable area on the chip, as the number of NMOS transistors in a typical amplifier may vary

* NMOS, Al gate technology, 10 μm minimum feature size, 2.5 μm minimum alignment tolerance, 700 $\text{\AA}$ gate oxide thickness.

from 9 to 18, the actual number being dependent on the specific characteristics of the amplifiers [2,3]. Typical chip area occupied by such amplifiers can be as high as 784 square mils, using a 10 μ m minimum feature size process.

The problem of power dissipation and chip area becomes more severe when it becomes necessary to integrate many filters in one monolithic IC. A solution for reducing the chip area in such applications is to apply the principle of time division multiplexing. This means that the capacitors of different filters will use the same op amp on a time shared basis. However, this solution has a drawback that such a multiplexed amplifier should have a high slew rate in order to satisfy the requirements of the increased switching speed. Obviously, amplifiers with high slew rates draw more current from the power supplies compared to those with lower slew rates.

The goal of the work reported here was to study some of the special dynamic amplifier circuits for SC filters which have been reported in the literature and then to explore the possibility of developing or improving a circuit which would be small in terms of chip area and with as low a power consumption as possible. It was also intended to utilize the fact that the amplifier can be disconnected from the rest of the circuit elements, during part of the clock period, yet not affecting the operation of a switched capacitor circuit. It will become evident from the following description of a parallel SC filter that the high gain and input impedance of

the amplifier are made use of only during a part of the sampling period, in the process of transferring the charge from one capacitor to another.

1.2 Parallel Switched Capacitor Integrator

Figures 1.1(a) and 1.1(b) show the circuit diagram of a parallel switched capacitor integrator and the corresponding switching waveforms respectively. Let us assume that the switches are realized by NMOS transistors M1 and M2 and also that the op amp is ideal. Let us also assume that the voltages are sampled and considered valid at the end of phase ϕ_2 . The input capacitor C_i is charged to the present input voltage sample $V_i(n)$, through the switch M1 when the clock phase ϕ_1 is high. The op amp OA is inactive during ϕ_1 and any charge in the feedback capacitor C remains unchanged. The output voltage sample remains as $V_o(n)$.

During the following phase (when ϕ_2 is high) switch M2 is closed. The input capacitor C_i is now connected to the virtual ground. The charge in C_i is transferred to the feedback capacitor C. The completeness of this charge transfer depends on the amplifier properties which we have assumed to be ideal. The resulting output voltage at the end of ϕ_2 is given by

$$\begin{aligned} V_o(n+1) &= V_o(n) - \frac{V_i(n) C_i}{C} \\ &= V_o(n) - \alpha_1 V_i(n) \end{aligned} \quad (1.1)$$

where $\alpha_1 = C_i/C$.

FIG 1.1(a) PARALLEL SWITCHED CAPACITOR INTEGRATOR

FIG 1.1(b) TWO PHASE CLOCK WAVE FORMS

FIG 1.3 (a) CIRCUIT DIAGRAM OF A BASIC DYNAMIC AMPLIFIER

FIG 1.3 (b) & (c) NON OVERLAPPING, TWO PHASE CLOCK WAVEFORMS

FIG 1.3 (d) OUTPUT (V_o) WAVEFORM FOR THREE DIFFERENT INPUT VOLTAGES

1.3 Static Amplifier

Figure 1.2(a) shows the circuit diagram of a common source amplifier which can be considered as a typical static amplifier. The active element is an NMOS transistor and therefore, the input impedance is capacitive. The voltage gain A_v of the circuit is given by

$$A_v = \frac{-g_m R_L r_o}{(R_L + r_o)} \quad (1.2)$$

where $g_m = \frac{dI_d}{dV_g}$; the transconductance of the active element

and $r_o = \frac{dV_{ds}}{dI_d}$; the output resistance of the active element

The amplifier should have a high gain in order to simulate an op amp. The gain of the common source amplifier can be increased by increasing R_L or r_o . However, there are practical fabrication limitations in realizing very high values of resistances. The second solution for increasing the gain is to increase g_m which is proportional to the channel width to channel length ratio. Hence a high g_m means a wider transistor or a short channel MOST, which either increases the final chip area required or introduces fabrication limitations owing to the small geometries involved.

Another solution to increase the gain is to replace R with an active device such as another NMOS device, with a suitable gate bias. However, in such circuits, the gain is

FIG 1.2 (a) CIRCUIT DIAGRAM OF A COMMON SOURCE AMPLIFIER

FIG 1.2(b) SIMPLIFIED SMALL SIGNAL EQUIVALENT CIRCUIT OF THE ABOVE CIRCUIT.

shown to be proportional to the ratio of width to length ratio of the load transistor, to the width to length (W/L) ratio of the driver transistor. Hence the maximum gain attainable is limited even in this case due to fabrication limitations. Let us now look at the basic principle of the dynamic amplifiers to see how they compare to the above factors in static amplifiers.

1.4, Introduction to Dynamic Amplifiers

As mentioned earlier, the principle of operation of a typical dynamic amplifier is very similar to that of dynamic logic circuits. Figures 1.3(a), and 1.3(b) show the circuit diagram and the non overlapping clock waveforms ϕ_1 and ϕ_2 respectively of a basic dynamic amplifier (dynamp hereafter) [4]. Note that this circuit is intended to show only the basic principle of working of the dynamp and does not represent the actual scheme.

1.4.1 Principle of Operation

Let us assume that NMOS transistors, M1, M2, M4 and M5 are ideal switches. M3 is the active transistor which takes part in the amplification. C_N represents the capacitance present at the output node (Node 5). C_i is the input capacitor.

Switches M1 and M5 are closed during clock phase ϕ_1 (when ϕ_1 is high). The input voltage sample is stored in

capacitor C_i . Also the output node is precharged to V_{DD} . When ϕ_2 is high, switches M2 and M4 are closed, thereby connecting the input voltage to the gate of M3 and opening a discharge path for C_N through M4 and M3. The bottom waveform of Figure 1.3(b) shows the possible voltage waveforms of the output node, indicating the dependence of output waveforms, on the input voltages. Since the duration of ϕ_2 is finite the output voltage V_o also would be higher than the desired value by a small but finite quantity, at the end of every ϕ_2 . The voltage V_R shown in Figure 1.3 may be defined as a voltage which would produce an output of zero volts at the end of ϕ_2 , when it is applied at the input node.

In practice, we shall see that the output voltage will occupy only one of the two values, either V_{DD} or V_{SS} because of the very high gain of the circuit during ϕ_2 . This allows for the use of a similar circuit for the dynamic logic using minimum size NMOS transistors and using their gate capacitances as memory elements.

Some circuits based on the principle of dynamic amplifiers, i.e. circuits having a precharge phase followed by discharge phase as a common feature had been reported in the recent past [4,5,6]. These circuits were intended to replace the static op amps found in SC integrators.

A new dynamic integrator is proposed in this thesis. The proposed circuit has many advantages compared to the circuits which have been reported so far. The circuit was simulated by SPICE and was found to perform satisfactorily.

FIG 1.3 (a) CIRCUIT DIAGRAM OF A BASIC DYNAMIC AMPLIFIER

FIG 1.3 (b) & (c) NON OVERLAPPING, TWO PHASE CLOCK WAVEFORMS

FIG 1.3 (d) OUTPUT (\$V_O\$) WAVEFORM FOR THREE DIFFERENT INPUT VOLTAGES

The simulation results were substantiated by breadboard experiments. Later an integrated circuit was fabricated which was configured as a switched capacitor second order filter employing the proposed dynamp. The IC was fabricated with facilities to modify the circuit as a notch, low pass or a high pass filter. The IC was characterized and the performance was found to agree with theoretical predictions. Work related to this IC characterization is described in detail here. The thesis format is as follows.

Chapter 2 presents a review of the dynamic amplifiers which are already reported. In Chapter 3 the proposed dynamp is introduced. The detailed circuit operation, computer simulation and results of experiments on a bread board model are also explained in this chapter.

In Chapter 4, the characterization of the integrated circuit is discussed. The filter performance as a notch, low pass and high pass filter is analyzed. Second order effects of the IC, such as effects of finite gain and power supply noise on the performance of the filter circuits are discussed in Chapter 5. Chapter 6 concludes the thesis by summarizing the work done. Some suggestions for improving the performance of the circuit also are given in Chapter 6.

Chapter 2

COMPARISON OF PREVIOUS WORKS

2.1 Dynamic Amplifiers Proposed By Copeland and Rabey

The concept of using a dynamic amplifier for switched capacitor filters was originally presented by M.A. Copeland and J.M. Rabey [4] in 1979. The circuit diagram and the corresponding clock waveforms of their circuit are given in Figures 2.1(a) and 2.1(b) respectively.

2.1.1 Circuit Operation

2.1.1.1 Assumptions

The circuit operation is described below under the following assumptions.

1. The voltages at various nodes are considered valid only at the end of clock phase ϕ_1 since the circuit is a sampled analog system.
2. All switches in Figure 2.1(a) are considered ideal, i.e., they have zero ON resistance, zero switching time and zero offset voltage. These assumptions, though not true in practice, help to understand the circuit operation without much difficulty.
3. The sub threshold current of all NMOS transistors are assumed to be zero so that the transistor would not conduct if its gate to source voltage is less than its threshold voltage.

FIG 2.1(a) DYNAMIC AMPLIFIER PROPOSED BY COPELAND

FIG 2.1(b) CLOCK WAVEFORMS FOR THE ABOVE CIRCUIT

4. The threshold voltage (V_{TH}) of transistor M1, i.e., the gate to source voltage above which M1 conducts, is the same as the difference between signal reference voltage and the negative power supply (V_{SS}). In other words, $V_{TH} = V_{REF} - V_{SS}$ where V_{REF} is zero volts in Figure 2.1(a).

2.1.1.2 Description

Switches S_1 and S_6 are closed when clock phase ϕ_1 high. The input voltage sample $V_i(n)$ is stored in the input capacitor C_i . Simultaneously, the output voltage sample $V_o(n)$ from capacitor C_o is transferred to the next stage through S_6 . Let us assume that the voltage at node 3 is at signal reference voltage during ϕ_1 so that M1 would not conduct according to the third assumption mentioned above. In the next phase ϕ_2 the output node (node 4) is precharged to V_{DD} , the positive power supply, through S_3 which is closed. The voltage rise of node 4 is capacitively coupled to node 3 through the feedback capacitor C_o . Switches S_2 , S_3 , and S_5 are also closed during ϕ_2 . As a result the voltage at node 3 rises to V_3^* at the end of ϕ_2 . V_3^* is given by

$$V_3^* = \frac{V_i(n) \times C_i}{C_i + C_o} + \frac{(V_{DD} - V_o(n)) \times C_o}{C_i + C_o} \quad (2.1)$$

In the next clock phase ϕ_4 , switch S_4 is closed and switch S_3 is opened. Capacitors C_i and C_o discharge through S_4 and M1. The output voltage at node 4 decreases, thereby coupling

a negative voltage to node 3. Since node 3 is the gate of M1 the discharge current is reduced, as a result of which, the rate of reduction of the output voltage is diminished. The process continues until the voltage at node 3 reduces to that of the signal reference voltage V_{REF} when M1 stops conducting (Note 1). Hence by the end of ϕ_4 all the charge in C_1 would be transferred to the feedback capacitor C_0 . The resulting voltage at the output node (node 4) can be expressed as

$$V_o(n+1) = V_o(n) - \frac{V_i(n) \times C_i}{C_o} \quad (2.2)$$

$$V_o(n+1) = V_o(n) - \alpha_i V_i(n) \quad (2.3)$$

where $\alpha_i = C_i/C_o$, the ratio of the input capacitor to the feedback capacitor. Obviously (2.3) is the difference equation describing the conventional parallel switched capacitor integrator which uses static op amps. However, a special requirement here is that the threshold voltage (V_{TH}) of the NMOS transistor M1, has to be much higher than the normal industrial standard which is about one volt. For example, if the power supply voltages are + and - 7.5 volts and the signal voltage swing is symmetric about the signal reference voltage (here zero volts), then, the threshold voltage of M1 should be 7.5 volts in order to ensure the proper operation of the circuit. Such a restriction on the

Note 1: Note that, theoretically it would take infinite time to reach such a state. However, in practice, the current would become negligible within a short and finite time.

threshold voltage is a drawback in terms of fabrication of the devices. However, the simplicity of the circuit (two switches and a transistor) to achieve results comparable to those with complex op amps motivates further investigation, resulting in this thesis.

2.2 A CMOS Dynamic Amplifier

A CMOS dynamic amplifier was reported by Hostica a shortwhile after Copeland's proposal [5]. Hostica's circuit is a CMOS differential amplifier in which the conventional constant current source is replaced by a switching arrangement of two switches and a capacitor. The circuit and its clock waveforms are shown in Figures 2.2(a) and 2.2(b) respectively.

2.2.1 Circuit Operation

Let us assume that the signal samples are considered valid at the end of ϕ_1 . Let the input capacitor C_i be charged to the present input voltage sample $V_i(n)$ during ϕ_1 . The capacitor C_B is discharged at the same time. Also let the corresponding output voltage at node 3 be $V_o(n)$.

During the following clock phase ($\bar{\phi}_1$) C_i is connected to node 2 which serves as the virtual ground of the amplifier. C_i discharges through C , $M3$ and C_B . The initial current through the circuit is high, thus giving the amplifier a high slew rate, due to the charging current of C_B . However the

current through M3 diminishes as the voltage at node 6 rises. Hence towards the end of the decay the amplifier operates in a subthreshold mode. Hence, towards the end of the charge transfer from C_i to C , the gain of the amplifier increases due due to the subthreshold operation [5]. The resulting high gain aids in the complete discharge of C_i .

The advantage of this circuit compared to the former one is that it is threshold voltage independent. However, its positive and negative output voltage swings are not symmetric. Its negative swing is small compared to the magnitude of the negative power supply.

Later, this problem was minimized by replacing the capacitive current source by extra circuitry involving capacitors and NMOS transistors.

2.3 Sampled Data Filters Using MOS Current Multipliers

A different scheme for realizing SC filters without using continuous power has been proposed by Arreola et al [6]. Their scheme uses MOST current multipliers for transferring charges between capacitors. Figures 2.3(a) and 2.3(b) show the scheme and circuit realization respectively of such a filter.

FIG 2-2(a) A CMOS DYNAMIC AMPLIFIER

FIG 2-2(b) CLOCK WAVEFORMS FOR THE ABOVE CIRCUIT

2.3.1 Circuit Operation

The input capacitor C_1 and C_2 are charged to the input voltages during ϕ_1 and then are discharged through NMOS transistor $M1$ of the current multiplier A_1 during the following ϕ_3 . Capacitor C which is precharged to V_{DD} during ϕ_2 also discharges through $M2$ while C_1 and C_2 are discharging. However, the charge lost by C during ϕ_3 is proportional to the input charges because the gates of $M1$ and $M2$ are connected together and due to the fact that $M1$ and $M2$ are fabricated in the same monolithic chip. The remaining charge in C is discharged through $M3$ during the following ϕ_1 phase. Now, C_O after being precharged to V_{DD} during ϕ_4 , discharges through $M4$, while C is discharging through $M3$. The loss of charge for C_O is proportional to the charge lost by C during ϕ_1 . As a result, the output voltage V_O at the end of ϕ_4 will be equal to a linear combination of the input voltages provided the capacitor ratios and the current multiplier constants are related as shown below.

The capacitor ratios are

$$\frac{C}{C_O} = \frac{1}{A_O} \text{ and } \frac{C_1 + C_2}{C} = \frac{1}{A_1}$$

where A_O and A_1 are the current multiplier constants which are proportional to the W/L ratios of the transistors. The coefficients α_1 and α_2 of Figure 2.3(a) are given by

$$\alpha_1 = \frac{A_1 A_O C_1}{C_O} \quad \alpha_2 = \frac{A_1 A_O C_2}{C_O}$$

FIG 2.3 (a) A TYPICAL SAMPLED DATA FILTER

FIG 2.3(b) A CURRENT MULTIPLIER REALIZATION OF THE FILTER IN FIG 2.3 (a) .

2.4 A Comparison of the Circuits

The circuit descriptions given above indicate that the last circuit is the most complex among the three. It uses more components than the other two. The technique of precharging to V_{DD} in different phases can lead to stronger coupling of high frequency noise to the power supply, which could further couple this noise to the output signal. In addition, it depends on geometrical matching of, not only capacitors, but transistors also.

Hostica's circuit has advantage over Copeland's in terms of threshold voltage independence. The differential input nature of the circuit offers better common mode rejection ratio. The power supply noise rejection is also higher for Hostica's circuit. However, the open loop gain of this circuit is much lower than Copeland's dynamp. Besides the capacitor C_B may become very large if better overall performance is required for the CMOS dynamp.

Referring to Copeland's dynamp, its most serious disadvantage is that the threshold voltage of the active MOST has to be equal to difference between circuit reference voltage and the source voltage of the order of a few volts. The circuit is simplest of all the three we have discussed. Its power consumption and chip area are the smallest among the three.

The simplicity of Copeland's circuit demanded more attention and consequently necessary modifications were added to make the circuit free from threshold voltage

dependency and also to have higher open loop gain. A detailed analysis of the modified circuit and a description of the various stages of its development are given in the next chapter.

Chapter 3

INTRODUCTION TO THE MODIFIED DYNAMIC AMPLIFIER

The circuit of the dynamic amplifier which Copeland proposed originally, is modified here. The modified circuit is shown in Figure 3.1. In the original circuit, if the output signal were to swing symmetrically about a signal reference voltage, then the threshold voltage V_{TH} of transistor M1 had to be such that

$$V_{SS} + V_{TH} = V_{REF}$$

In this case, the output signal swing would be limited to V_{DD} , the positive power supply and V_{SS} , the negative power supply, if V_{REF} is equal to zero volts.

The above constraint on the threshold voltage of M1 is removed by storing a voltage equal to $V_{SS} - V_{TH}$ in the capacitor C_{OS} of Figure 3.1 at the beginning of every sampling cycle. The gate potential of M1 is then raised by this voltage during the phase ϕ_3 , so as to simulate the effect of having a high threshold voltage as in the original circuit.

FIG 3-1(a) DYNAMIC AMPLIFIER MODIFIED TO REDUCE THRESHOLD VOLTAGE LIMITATION

FIG 3-1(b) TIMING DIAGRAM OF CLOCKS ϕ_1 , ϕ_2 , ϕ_3 AND ϕ_4

3.1 Circuit Operation

The operation of the circuit of Figure 3.1 during each of the 4 phases of the clock is described below, separately, by considering the voltage variations of different nodes, under the following assumptions:

- The switches, though fabricated by minimum geometry NMOS transistors are assumed to be ideal.
- The transistor M1 has infinite output impedance in the saturation region of its I_d vs V_{DS} characteristics.
- Effects of parasitic elements are not considered.
- The switches are labelled with the same names as those of the clock phases, which drive them, i.e. a switch ϕ_i will be closed when clock phase ϕ_i is high.

Clock Phase ϕ_1

Node 1

The present input sample $V_i(n)$ is connected to node 1. $V_i(n)$ is a sampled analog signal and not a continuous one.

Node 2

Node 2 is connected to node 1. The input capacitor C_{in} is charged to the input sample $V_i(n)$. Let C_{in} be equal to $\alpha_1 C$ where α_1 is a constant and C is the feed back capacitor.

Node 3

Node 3 is floating during ϕ_1 . The voltage at node 3 is very close to the signal reference voltage V_{REF} . It has

decayed to its present level, during the preceding ϕ_3 phase as a result of the circuit operation. Let the node 3 voltage be $V_3(n)$. It may also be noted that node 3 is the effective input node of the dynamic amplifier.

Node 4

Node 4 is connected to the signal reference voltage V_{REF} , through a switch which is closed by ϕ_1 . The value of V_{REF} is normally 0 volt dc (the analog ground) and can be adjusted to control the output offset voltage of the amplifier.

Nodes 5 and 6

Node 5 is the actual input node of the amplifier. The gate and drain of M1 are connected together during ϕ_1 . Any residual charge at node 6 (the drain of M1) is discharged through M1 until the node 6 voltage falls to the threshold voltage V_{TH} at which time M1 stops conducting. Thus the capacitor C_{OS} is charged to a voltage equal to $V_{REF} - (V_{SS} + V_{TH})$ across its plates. Storing of this voltage across C_{OS} is the first step in eliminating dependency of the original dynamp on the threshold voltage.

Node 7

Node 7 is the output node of the dynamp and floats during ϕ_1 . Let its voltage be $V_O(n)$.

Node 8

This is the node to which the input capacitors of any following filter stages are connected. Voltage at node 8 would start with a value $V_O(n)$, at the beginning of ϕ_1 .

Its final value, at the end of ϕ_1 , would depend on the absolute value of the capacitor C_0 and the nature of the following circuit. However, in the circuit of Figure 3.1, node 8 voltage will be equal to $V_0(n)$ at the end of ϕ_1 .

Clock Phase ϕ_2

All switches labelled as ϕ_2 and ϕ_3 are closed during ϕ_2 . Switches labelled as ϕ_1 and ϕ_4 are open.

Node 1

A new input sample $V_i(n+1)$ is being presented to node 1. Note that the corresponding sampling switch and hold capacitor are not shown in Figure 3.1.

Nodes 2, 3, 4, 7 and 8

Nodes 2, 3 and 4 are connected together during ϕ_2 . Nodes 7 and 8 are precharged to V_{DD} , the positive power supply voltage. The voltage at node 3 is changed from $V_3(n)$ to a new value, which is a function of the input voltage $V_i(n)$ and the rise in voltage at node 7. V_3^* , the new voltage at nodes 2, 3 and 4 at the end of ϕ_2 , can be expressed as

$$\begin{aligned} V_3^* &= V_3(n) + V_i(n) \frac{C_{IN}}{C_{IN} + C} + (V_{DD} - V_0(n)) \times \frac{C}{C_{IN} + C} \\ &= V_3(n) + \frac{V_i(n) \alpha_i + V_{DD} - V_0(n)}{1 + \alpha_i} \end{aligned} \quad (3.1)$$

where $\alpha_i = C_{IN}/C$

Node 5

The change in voltage at node 3 is capacitively coupled to node 5 which is the gate of M1. This node which was at V_{TH} at the end of the preceding ϕ_1 phase, rises to a new voltage V_g^* which is given by

$$V_g^* = V_{SS} + V_{TH} + \frac{V_i(n) \alpha_i + V_{DD} - V_o(n)}{1 + \alpha_i} \quad (3.2)$$

It must be noted that the oxide capacitance of M1 is ignored in (3.2).

Node 6

Node 6, the drain of M1 is floating during ϕ_2 as it is not connected to any other node. Any charge remaining at node 6, will be discharged and the node voltage will fall towards V_{SS} since the gate of M1 will be at a high positive potential, during ϕ_2 .

Thus the ϕ_2 phase is the precharge phase in which the circuit draws power from the power supply. Power is consumed in charging the capacitances at nodes 7 and 8.

Clock Phase ϕ_4

All switches labelled as ϕ_3 and ϕ_4 are closed during ϕ_4 phase. It is during this phase that the charge transfer from the input capacitor C_{IN} to the feedback capacitor C is taking place. Capacitor C_{IN} discharges through C and transistor M1. The load capacitor C_O also discharges through

M1. The voltage at nodes 7 and 8 starts decaying towards V_{SS} from the precharge voltage V_{DD} . The gate voltage of M1 also decreases from its initial value as it is coupled to node 3. As the gate voltage decreases from the value given by (3.2), the current through M1 also decreases, thereby reducing the rate of decay of the output voltage at nodes 7 and 8. A closed form expression can be derived for this voltage transient at node 7, as a function of

- a) the voltages at the different nodes with respect to V_{REF} , at the end of ϕ_2 .
- b) the gain factor $\mu C_{ox} \frac{W}{L}$ of the transistor M1.
- c) capacitances.
- d) time.

The expression for node 7 voltage during ϕ_4 is derived as shown below. The equivalent circuit of the dynamic amplifier in Figure 3.1(a) during the charge transfer phase ϕ_4 can be shown in Figure 3.1(c) if the switches are assumed to be ideal, i.e., to have zero ON resistance and zero voltage drop across them.

Figure 3.1(c) Equivalent Circuit of the Modified Dynamp.

During ϕ_4

The current i , through the transistor M1 during ϕ_4 can be expressed as a function of V_g , its gate potential, with reference to the signal reference voltage (0 volts), as well as a function of time, as

$$i(t) = \frac{K}{2} [V_g - V_{SS} - V_{TH}]^2 \quad (3.3)$$

where $K = \mu C_{ox} \frac{W}{L}$

Since $i(t)$ is the sum of i_1 and i_2 , (3.3) can be expressed as

$$-\frac{d(V_o - V_1)C}{dt} - \frac{dV_o}{dt} \alpha_o C = \frac{K}{2} [V_g - V_{SS} - V_{TH}]^2 \quad (3.4)$$

(3.4) assumes the gate current of M1 to be zero.

$$\frac{dV_1}{dt} = \frac{dV_o}{dt} \frac{1}{(1 + \alpha_1)} \quad (3.5)$$

since V_{in} is constant during ϕ_4 .

From (3.4) and (3.5)

$$-\left[\frac{dV_o}{dt} - \frac{dV_o}{dt} \frac{1}{(1 + \alpha_1)}\right] - \frac{dV_o}{dt} \alpha_o C = \frac{K}{2} (V_g - V_{SS} - V_{TH})^2$$

$$\frac{dV_o}{dt} \left[\frac{\alpha_1}{(1 + \alpha_1)} + \alpha_o\right] C = -\frac{K}{2} (V_g - V_{SS} - V_{TH})^2 \quad (3.6)$$

Relationship between V_o and V_g :

The incremental change in V_1 is the same as the

incremental change in the gate voltage V_g , since the gate capacitance of M_1 is assumed to be zero.

$$\therefore \frac{dV_1}{dt} = \frac{dV_g}{dt} \quad (3.7)$$

From (3.6) and (3.7)

$$V_g(t) = \frac{V_o(t) + \text{constant}}{1 + \alpha_1} \quad (3.8)$$

Applying the initial conditions for V_g from (3.2) and initial value of $V_o(t)$ as

$$V_o(0) = V_{DD} \quad (3.9)$$

The gate voltage $V_g(t)$ is expressed as

$$V_g(t) = [V_o(t) + (V_{SS} + V_{TH})(1 + \alpha_1) - V_o(n) + V_{in}(n)\alpha_1] \quad (3.10)$$

Substituting (3.10) in (3.6)

$$\frac{dV_o}{dt} \left(\frac{\alpha_1}{1 + \alpha_1} + \alpha_o \right) C = - \frac{K}{2(1 + \alpha_1)^2} [V_o(t) - V_o(n) + \alpha_1 V_{in}(n)]^2 \quad (3.11)$$

(3.11) is of the form

$$K_1 \frac{dy}{dx} = K_2 \left(\frac{y}{K_3} - K_4 \right)^2 \quad (3.12)$$

where

$$K_1 = \left(\frac{\alpha_1}{1 + \alpha_1} + \alpha_o \right) C$$

$$K_2 = - \frac{K}{2(1 + \alpha_1)^2}$$

$$K_3 = 1$$

$$K_4 = V_0(n) - \alpha_i V_{in}(n)$$

Solution of (3.12) is of the form

$$\frac{-K_3^2}{y - K_3 K_4} = \frac{K_2}{K_1} + \frac{K_3^2}{y(0) - K_3 K_4} \quad (3.13)$$

where $y(0) = V_{DD}$, the precharge voltage.

From (3.13)

$$\frac{1}{V_0(t) - (V_0(n) - \alpha_i V_{in}(n))} = - \frac{K t}{2(1+\alpha_i)^2 C(\frac{1}{1+\alpha_i} + \alpha_o)} - \frac{1}{V_{DD} - (V_0(n) - \alpha_i V_{in}(n))} \quad (3.14)$$

Rearranging (3.14) and renaming $V_0(t)$ as $V_7(t)$ (Figure 3.1(a)) we get

$$V_7(t) = V_0(n) - V_{in}(n) \alpha_i + \frac{1}{\frac{C_{ox} \mu(W/L) t}{(1+\alpha_i) 2C(\alpha_i + \alpha_o(1+\alpha_i))} + \frac{1}{V_{DD} - (V_0(n) - \alpha_i V_{in}(n))}} \quad (3.15)$$

Equation (3.15) is valid for $0 < t < T_4$ where T_4 is the duration of ϕ_4 high level. Similarly, an expression for the gate voltage of M1 also can be derived from (3.10) as $V_g(t)$, as is given in (3.16) below

$$V_g(t) = \frac{V_7(t) + (V_{SS} + V_{TH}) (1+\alpha_i) - (V_0(n) - V_{in}(n) \alpha_i)}{1 + \alpha_i} \quad (3.16)$$

The expressions (3.15) and (3.16) are derived using the simple model of the NMOS transistor in the saturation region, in which the drain current I_D is given by

$$I_D = \frac{K}{2} (V_{gs} - V_{TH})^2 \quad (3.17)$$

where $K = \mu C_{ox} \frac{W}{L}$

V_{gs} = gate to source voltage

V_{TH} = threshold voltage with 0 substrate bias

The following are evident from (3.15)

- The initial value of the output voltage V_7 is the precharge voltage which would be V_{DD} if the switches are ideal.
- $V_7(t)$ decays towards a final value which is equal to $V_0(n) - \alpha_i(n)$.
- The slope of this decay is very high initially and becomes very small towards the end of ϕ_4 .

Now, $V_0(n+1)$ can be defined as the value of $V_7(t)$ at the end of ϕ_4 .

A plot of the voltage decays of $V_7(t)$ and $V_g(t)$ are shown in Figure 3.2, using expressions (3.15) and (3.16). The instantaneous values of $V_7(t)$ and $V_g(t)$ are evaluated by assuming the following parameters

$$V_0(n) = 0 \text{ V}$$

$$V_1(n) = 1.0 \text{ V}$$

$$\alpha_i = 0.1$$

$$\alpha_o = 0.1$$

$$C = 20 \text{ pF}$$

$$V_{DD} = 7.5 \text{ V}$$

$$V_{SS} = -7.5 \text{ V}$$

$$V_{TH} = 0.5 \text{ V}$$

The calculated values of $V_7(t)$ and $V_8(t)$ are also shown in Table 3.1 for quick analysis of the voltage decay. Table 3.1 shows that the output voltage approaches -0.1 volt asymptotically. V_{out} is 96 mV at the end of 3.5 microseconds. The difference of 4 mV (from the final value of -100 mV) may be considered as the amplifier's effective offset voltage which will be discussed in detail in a later section. If this difference is ignored, then the final output voltage, at the end of ϕ_4 can be expressed as

$$V_0(n+1) = V_0(n) - \alpha_i V_1(n) \quad (3.18)$$

Equation (3.18) together with the foregoing description of the circuit operation shows that the parallel switched capacitor integrator employing a dynamp (Figure 3.1(a)) is functionally equivalent to the parallel switched capacitor integrator realized by static operational amplifiers (Figure 1.1(a)). However, the second order effects which were ignored in the circuit description given above, are more significant in a dynamic amplifier than in a static amplifier and therefore, deserve more attention.

Time (μ Seconds)	$V_7(t)$ (Volts)	$V_g(t)$ (Volts)
0.0	7.5	0.0909
0.1	0.0375	-6.8750
0.2	-0.0306	-6.9369
0.3	-0.0536	-6.9578
0.4	-0.0652	-6.9683
0.5	-0.0721	-6.9746
0.6	-0.0767	-6.9789
0.7	-0.0801	-6.9819
0.8	-0.0825	-6.9841
0.9	-0.0845	-6.9859
1.0	-0.0860	-6.9873
1.5	-0.0907	-6.9915
2.0	-0.0930	-6.9936
2.5	-0.0944	-6.9949
3.0	-0.0953	-6.9958
3.5	-0.0960	-6.9964

Table 3.1 Instantaneous Values of Output and Gate Voltages,
During a Typical ϕ_4 Phase. $V_o(n) = 0V$; $V_{in}(n) = 1.0V$.

Fig. 3.2 OUTPUT AND GATE VOLTAGES VS TIME DURING Φ_4 PHASE. PLOT CORRESPONDING TO TABLE 3.1.

3.2 Voltage Gain of Dynamic Amplifier

The small signal voltage gain A_v of an amplifier is defined as

$$A_v = \frac{dV_o}{dV_{in}} \quad (3.19)$$

where dV_o is a very small change in the output voltage, as a result of a corresponding change dV_{in} in the input voltage.

Small signal gain is evaluated around a specified dc operating point (quiescent point). Hence (3.19) is quite valid for a static NMOS amplifier. However, (3.19) cannot be directly applied for evaluating the gain of a dynamic integrator. This should be evident from the following explanation.

Consider the equivalent circuit of a first order model of an NMOS transistor which is configured as a common source amplifier (Figures 3.3(a) and 3.3(b)). The gain A_v of such an amplifier is given by (3.19) as

$$A_v = - \frac{g_m R_L}{1 + g_o R_L} \quad (3.20)$$

where g_m is the transconductance which is proportional to the square root of the quiescent drain current, and g_o is the output conductance (i.e. $\frac{dI_d}{dV_{ds}}$) of the transistor, in its saturation region.

FIG 3.3 (a) A SIMPLE NMOS AMPLIFIER

FIG 3.3(b) A SIMPLIFIED LOW FREQUENCY EQUIVALENT
CIRCUIT OF THE AMPLIFIER IN FIG 3.3(a).

The amplifying property of the dynamp circuit becomes effective only during ϕ_4 , when the load resistance R_L in the expression (3.20) becomes the OFF resistance of the switch ϕ_2 . Hence the effective gain of the dynamp becomes

$$A_v = -g_m/g_o \quad (3.21)$$

Hence, in the absence of parasitic elements, A_v is limited by the finite output conductance g_o of the transistor M1 of Figure 3.1. Hypothetically, the gain can be even infinity, if the transistor has ideal characteristics which would imply zero output conductance. However, the standard technique of defining the gain of static amplifiers, as the ratio of a small change in output voltage to corresponding change in input voltage, cannot be applied directly for the dynamp. The reason is that for a static amplifier, the gain can be evaluated for any specific operating point but for the dynamp, such a specific operating point cannot be defined in a simple way, during the period of ϕ_4 . Instead, the operating point around which the gain can be calculated, is considered valid by the end of ϕ_4 , after assuming the input to be zero volt. The dynamp gain is evaluated as explained below.

Typical voltage waveforms of the output node, the gate of M1, and node 3 which is the effective input node are shown in Figures 3.4(a), (b) and (c) respectively. With reference to Figure 3.4, the dc open loop gain A_e of the dynamp is given as

$$A_e = \Delta V_o / \Delta V^*$$

where ΔV_O is the difference in two consecutive output voltage samples and ΔV^* is the difference in the corresponding gate voltages, all voltages being considered valid, at the end of ϕ_4 .

The gain computed in this way is very high, of the order of 30,000 to 200,000 because of the ideal conditions assumed for the computations. It is evident that the finite duration of the ϕ_4 phase, will limit the maximum gain attainable from the circuit.

An interesting fact which emerges by examining (3.16) is that a finite output offset voltage is unavoidable for the dynamic amplifier. That is, even if the input voltage is zero, the output voltage sample at the end of ϕ_4 will be a few millivolts more positive than the ideal output. The reason for this output offset is the finite duration of ϕ_4 . The voltage decays to the desired value asymptotically during ϕ_4 and so, the desired value will be attained only if the duration of ϕ_4 is infinitely long.

The output voltage $V_O(n)$ and the gate to source voltage $V_{gs}(n)$ are tabulated (Table 3.2) against n , for three different values of dc input voltages. Four consecutive samples are evaluated for each of the input voltages. The component values, transistor parameters and voltage levels, assumed for the calculations are also given in Table 3.2, along with the calculated gains using (3.15) and (3.16). However, the actual gain practically obtainable from the dynamic circuit is much less than what one would see in Table 3.2. The lower gain is due to the second order effects such

V_{in} Volt	n	$V_{g_s}(n)$	$V_o(n)$	Gain = $\frac{V_o(n+1)-V_o(n)}{V_{g_s}(n+1)-V_{g_s}(n)}$
0	0	-7	0	
	1	-6.983971	0.0200356	-32315
	2	-6.98397162	0.04007109	
	3	-6.983971735	0.06010642	-174220
	4	-6.983971851	0.08014161	-172717
	5	-6.983971967	0.10017665	-172715
V^*	0	-7	0	
	1	-6.983971391	0.0000003845	
	2	-6.983971391	0.0000007691	
	3	-6.983971391	0.0000011536	
	4	-6.983971391	0.0000015381	
1	0	-7	0	
	1	-6.983970124	-0.2299626544	-192453
	2	-6.983968929	-0.4599238158	-203865
	3	-6.983967801	-0.689883576	-215720
	4	-6.983966735	-0.9198419865	-227680
	5	-6.983965725	-1.149799143	
-1	0	-7	0	
	1	-6.983972981	0.2700337734	157597
	2	-6.983974694	0.5400654054	145880
	3	-6.983976545	0.8100947241	134653
	4	-6.98397855	1.0801215360	123830
	5	-6.983980731	1.350145623	113516
	6	-6.98398311	1.620166736	

$V^* = 0.0801415V$
Table 3.2

$K = 400 \mu A/V^2$; $\alpha_1 = 0.25$; $V_T = 0.5V$; $T_D = 3.5 \mu sec.$
 $V_o(o) = 0V$; $V_{g_s}(o) = -7V$; $V_{DD} = 7.5V$; $V_{SS} = -7.5V$

as gate overlap capacitances, finite slope of I_d vs V_{ds} characteristics in the saturation region, dependence of threshold voltage on V_{ds} (drain to source voltage) etc. Hence it is appropriate now to discuss the second order effects of the dynamp and the necessary modification to the circuit of Figure 3.1(a) for reducing such effects.

3.3 Second Order Effects in the Dynamic Amplifier

3.3.1 Output Offset Voltage

The output offset voltage in a dynamic amplifier integrator is generated in a different way compared to the offset voltage in a static op amp integrator. In a static amplifier, the output offset voltage is developed by the accumulation of voltage or current mismatches, over the various stages of the amplifier. That is, the generation of offset voltage can be avoided in a static amplifier, at least hypothetically, if perfect matching of the devices can be obtained. However, in the dynamic amplifier, the offset voltage is the result of the duration of ϕ_4 being finite. The dependence of offset voltage on ϕ_4 duration can be seen in Figure 3.5.

In addition, the output voltage buildup in the dynamp integrator and the static integrator also takes place in different ways. In the static case, build up will take place for zero input voltage, only if the input bias current is not zero. Charge is stored in the feedback capacitor due to the

finite input bias current flowing through the capacitor, thereby developing an output voltage, which eventually would clamp at one of the power supply voltages. Now, in the case of dynamp integrator, if an output offset voltage is developed with zero input voltage, in any sample period, then the output voltage will start building up in the following periods. The reason is as follows.

Once an offset voltage exists, the voltage difference $V_{DD}-V_O(n)$ differs from V_{DD} . The voltage coupled to the gate of M1 (Figure 3.1) also varies in the next sample period. As a result, the discharge current will be different in the second sample period, though the input voltage would still be at zero. As the discharge currents are different in consecutive clock phases and as duration of ϕ_4 and level of precharge voltage remain the same, the voltages at the end of consecutive ϕ_4 phases would be different. Hence the net result is similar to that of a static integrator having a finite input bias current.

The compensation for this offset voltage build up is carried out in a similar manner as in the static amplifier. A compensating input current solves the voltage build up problem for the static amplifier. Similarly, a compensating dc voltage, added to the actual input signal solves the problem, for the dynamp integrator. For example, in Table 3.2, we see that an input voltage of 0.0801415 volts reduces the output offset voltage from 20 mV to 0.38 microvolts.

The offset voltage can also be controlled by the addition of another cascode NMOS transistor with suitable biasing in series with the main active transistor M_1 of Figure 3.1. A detailed discussion of this technique is given in a later section.

3.3.2 Negative Feedback Due to Gate Capacitance

It is needless to say that the frequency dependent voltage gain of an inverting amplifier is reduced when its input and out nodes are capacitively coupled. In other words, when such a capacitor is present as a parasitic element, the effective input capacitance of the amplifier is increased by an amount equal to the parasitic capacitance multiplied by the gain of the amplifier. This is the well known Miller effect associated with amplifiers. The Miller effect is applicable to the dynamp as well, in which case the parasitic capacitance is formed by the gate drain capacitance of the transistor M_1 in Figure 3.1(a). The dynamp of Figure 3.1 is redrawn in Figure 3.6, in which the gate drain capacitance is shown as C_{gd} .

Referring to Figure 3.6, one can see that the voltage variations at the effective input node V^* and the gate of M_1 are not the same, in the presence of C_{gd} . As such, the effective open loop gain evaluated with respect to V^* , reduces to the ratio of C_{os} to C_{gd} if the open loop gain with respect to the gate of M_1 is much greater than C_{os} C_{gd} . The effective gain, A_{eff} can be expressed as

FIG 3.5 OUTPUT TRANSIENT WAVEFORM WITH EMPHASIS ON OFFSET VOLTAGE

FIG. 3.6 DYNAMIC AMPLIFIER SHOWING THE GATE DRAIN PARASITIC CAPACITANCE

$$A_{\text{eff}} = - \frac{C_{\text{os}}}{(1+1/A) C_{\text{gd}} + C_{\text{os}}/A} \quad (3.22)$$

where A is the open loop gain, evaluated w.r.t. equations (3.15), (3.16) and Table 3.2. The expression (3.22) is used to compute $V_o(n)$ for successive values of n so the gain can be evaluated as

$$A = \frac{V_o(n+1) - V_o(n)}{V^*(n+1) - V^*(n)}$$

Equation (3.22) can be approximated as

$$A_{\text{eff}} = - \frac{C_{\text{os}}}{C_{\text{gd}}}$$

as A is very high, of the order of few thousands according to Table 3.2.

Hence, the effective gain of the dynamp is limited due to the finite values of C_{os} and C_{gd} . A very low gate drain capacitance as well as a high C_{os} are required for the gain to be high. However, the dynamp circuit is to be integrated eventually, and so the capacitor values have to be chosen considering the limitations of IC fabrication. Therefore, the maximum value of C_{os} will be limited as the silicon area required by C_{os} in the IC, is proportional to its value. Besides, if C_{os} is too large, then C_{os} may not discharge to the threshold voltage limit during the ϕ_1 phase in which case the voltage stored across C_{os} at the end of ϕ_1 will be higher than the desired voltage of $V_{\text{SS}} + V_{\text{TH}}$.

Similarly, the minimum value of C_{gd} also is finite despite the fact that fabrication techniques which yield self

aligned polysilicon gates can reduce the gate overlap capacitances significantly. This is so because C_{gd} is constituted by an intrinsic capacitance proportional to the gate oxide capacitance in addition to the gate overlap capacitance.

Hence one can conclude that, in practice, the circuit of Figure 3.6 can have only a lower gain than predicted by (3.15) and (3.16). For example, a gain of only 500 can be expected if C_{os} and C_{gd} are assumed to be typically 5 PF and 0.01 PF respectively.

3.3.3 Channel Length Modulation

In the previous sections, it was assumed that the threshold voltage of M1 (Figure 3.6) is independent of V_{ds} . However, in practice, this assumption is not quite valid [7]. The threshold voltage of a MOS transistor is affected by the charges in its substrate and the channel region. The depletion width of the drain junction is proportional to the square root (or cube root depending on the gradient of doping concentration at the junction) of the drain voltage. In other words, the effective channel length of the MOS transistor will be shorter for a higher V_{ds} . It is also known that the threshold voltage of the device is affected by the substrate charge near the channel region. Hence, the effective substrate charge becomes smaller which in turn, lowers the threshold voltage, when the drain source

(substrate) voltage (V_{ds}) becomes higher.

The above argument can be illustrated by the following example, (referring to Figure 3.7) in which all second order effects except channel length modulation are ignored. Let two consecutive output voltage samples be $V_o(1)$ and $V_o(2)$ in which $V_o(1)$ is greater than $V_o(2)$. Let the corresponding gate voltages $V_g(1)$ and $V_g(2)$, at the end of ϕ_4 be equal to the threshold voltages $V_{TH}(1)$ and $V_{TH}(2)$. In the absence of channel length modulation, $V_{TH}(1)$ is the same as $V_{TH}(2)$, in which case the gain is limited only due to the finite duration of ϕ_4 . However, due to channel length modulation, $V_{TH}(1)$ should be less than $V_{TH}(2)$ so that ΔV_{g2} is greater than ΔV_{g1} in Figure 3.7, thereby further reducing the gain which is the ratio of ΔV_o to ΔV_g . It can also be stated that channel length modulation manifests the finite slope in the drain characteristics of a MOS device. The finite slope, in turn results in a finite value for g_o in (3.21) the effect of which is to reduce the dynamp's open loop gain.

3.4 Tetrode Transistor - The Solution for Second Order Effects

As mentioned earlier the gate drain capacitance C_{gd} reduces the small signal gain of the dynamp due to Miller effect. In fact, the reduction of the voltage gain is caused by the negative feedback from the output node to the input node, through the parasitic capacitor C_{gd} . The Miller effect can be minimized by reducing the amount of negative feedback,

FIG 3.7(a) TYPICAL OUTPUT VOLTAGE WAVEFORM FOR DC INPUT VOLTAGES

FIG 3.7(b) CORRESPONDING GATE VOLTAGE WAVEFORM WITH NEGLIGIBLE CHANNEL LENGTH MODULATION

FIG. 3.7(c) GATE VOLTAGE WAVEFORM WHEN CHANNEL LENGTH MODULATION IS SIGNIFICANT, RELATIVE TO CHANNEL LENGTH. NOTE THE INCREASE IN ΔV_g

without affecting the output voltage swing. This implies that only a fraction (ideally 0) of the output voltage should be allowed to couple to the input.

Therefore, the principle of the well known cascode amplifier is adopted for modification of the dynamp as well. The circuit diagram of a typical cascode amplifier is shown in Figure 3.8, in which the presence of transistor T2 prevents the output voltage from being directly coupled to the base of T1 through the parasitic capacitor C_{bc} . Though the dynamic range of V_{OUT} in Figure 3.8 can be from $2V_{CESat}$ to V^+ the variation of collector voltage of T1 can be only from V_{CESat} to $(V_{BIAS} - V_{BE2})$ where V_{BE2} is the base emitter voltage of T2. So, most of the output voltage swing is absorbed across T2's collector and emitter and what is coupled to input of T1 is only nominal. (Since V_{BE2} does not vary appreciably, say from 0.6 to 0.7 volt). Besides, the output conductance g_o of the cascode amplifier is much less than that of the common emitter amplifier.

The dynamp of Figure 3.6 is modified to convert it to a cascode amplifier by adding a second NMOS transistor M2. The modified circuit is shown in Figure 3.9. The effect of the addition of M2, on the performance of the dynamp is discussed below.

3.4.1 Miller Effect

Miller effect is very much reduced in the modified dynamp circuit of Figure 3.9. However, the degree of cancellation of the effect is not as great as in the cascode amplifier of Figure 3.8, because the negative feedback is almost negligible in the case of the bipolar transistor amplifier. The voltage variation of the drain of M1 in Figure 3.9 is, not negligible, though small. The drain of M1 may vary from $V_{SS} + V_{TH1}$ to $V_{BIAS} - V_{TH2}$ where V_{TH1} and V_{TH2} are the threshold voltages of M1 and M2 respectively. Hence the fraction of the output voltage variation, coupled to the input through C_{gd} can be controlled by adjusting V_{BIAS} . This implies that the actual gain of the dynamp can be controlled by V_{BIAS} , the voltage applied to the gate of M2.

3.4.2 Channel Length Modulation

The adverse effect of channel length modulation is reduced in the cascode dynamic amplifier (Figure 3.9) because the channel length modulation itself is very much reduced owing to the limited swing of M1's drain voltage.

FIG. 3.8 CIRCUIT DIAGRAM OF A CASCODE AMPLIFIER

FIG 3.9 CIRCUIT DIAGRAM OF THE DYNAMIC AMPLIFIER
MODIFIED AS A CASCODE AMPLIFIER

3.4.3 Output Resistance

The gain of a static amplifier as given in (1.2) is

$$\text{gain} = \frac{g_m r_o R_L}{r_o + R_L}$$

where R_L is the load resistance, g_m is the transconductance and r_o the output resistance.

For a dynamp, the equivalent value of R_L is that of an open switch. So, the gain is limited by the output resistance, which is evaluated from the I_D vs V_{DS} characteristics. The output resistance r_o is finite for the dynamp of Figure 3.6. However, for the modified circuit of Figure 3.9 (cascade type), the slope of the drain current vs output voltage characteristics, in the operating voltage range is much smaller than the corresponding slope of Figure 3.6. This is so because, the current in the circuit is mostly decided by the gate voltage of M_1 and the effect of output voltage on the drain current is very small. Because of M_2 , only a fraction of the output voltage appears across the source and drain of M_1 and hence the effect of its drain voltage on the drain current is suppressed to a great extent.

In short, the cascode amplifier of Figure 3.9, has a much higher output resistance than the common source type dynamp, which in turn would imply a higher gain.

3.5 Computer Simulation of the Proposed Circuit

The proposed dynamic amplifier circuit, as shown in Figure 3.9 was simulated in a computer using the circuit simulation program SPICE2.F. The computer simulation was carried out in order to substantiate the circuit analysis which was done qualitatively in the previous sections. Simulation was necessary also because the derivation of a closed form expression similar to (3.15) and (3.16) was very tedious in the case of a cascode amplifier, and besides, such a task does not provide results which are useful enough for the effort required. The use of a circuit simulation program is a more practical way to take the second order effects into account while analyzing the circuit.

The circuit was analyzed to study the transient behaviour under the following conditions:

- All switches are realized by NMOS transistors of 4x4 micron geometry.
- Transistors M1 and M2 are 80 micron (channel width) x 7 micron (channel length) geometry.
- The input signal is a pulse of 1 volt amplitude and of 1 millisecond duration.
- DC bias on the gate of M2 is 1.5 V above the signal reference.
- Power supplies are ± 7.5 volts.

The voltages at the output, input and M1 gate nodes were computed and plotted for 4 consecutive clock cycles, at a clock frequency of 100 KHz.

3.5.1 Results of Computer Simulation

The results of the simulation are very encouraging (i.e., supporting the qualitative analysis) as can be observed in the plots of the transient analysis, shown in Figure 3.10. The net gain w.r.t. the input node is found to be varying between 1000 and 3000, the actual value being dependent on the output voltage at which the gain is evaluated as $\Delta V_o / \Delta V_{in}$. (See Appendix 4 for gain calculations). As expected, it is also observed that the open loop gain w.r.t. to M1's gate is greater than 25,000.

The simulation also reveals how body effect relates to the performance of the circuit. The maximum positive output voltage or the precharge voltage is about 3 V below V_{DD} , the positive power supply. This is because the threshold voltage of a NMOS transistor increases due to body effect when the source to substrate voltage V_{SB} becomes more positive. The increase in threshold voltage is approximately proportional to $\sqrt{V_{SB}}$. Hence, threshold voltage of the precharge switch (ϕ_2) increases when its source rises towards V_{DD} during the clock phase ϕ_2 because the substrates of all NMOS transistors are connected to V_{SS} , the negative power supply.

For any NMOS transistor switch which^o is closed, the maximum drain or source voltage of the switch is limited to its gate voltage minus the threshold voltage. Now, V_{SB} is approximately 12 volts during ϕ_2 , and so a threshold voltage of about 3 V is comparable to the previous approximations. And since clocks are assumed to have an amplitude equal to

DYNAMIC AMPLIFIER (5 PICOSEC)

FIG. 3.10 TRANSIENT RESPONSE OF DYNAMIC AMPLIFIER (SPICE SIMULATION)

the positive power supply, a precharge voltage which is roughly 3 V less than V_{DD} , also is justifiable.

In short, we can summarize that the computer simulation supports the qualitative analysis presented in the previous sections of this chapter. It also reveals the influence of body effect in reducing the maximum swing of the circuit's output voltage.

3.6 Bread Board Experiments With the Dynamic Amplifier

3.6.1 The Necessity of the Experiments

Though the computer simulation of the circuit was very useful, it could not be used for an extensive analysis because running the simulation program was expensive owing to the complexity of the circuit. Hence, in order to justify the fabrication of the circuit as a monolithic IC, it was decided to build a bread board model of the dynamp and study the characteristics.

3.6.2 Bread Board Construction

The circuit diagram for the bread board experiments is the same as that of Figure 3.9. The switches were realized by CMOS analog switches (type CD4066). CMOS analog switches were selected because they have better switching properties compared to NMOS switches such as constant ON resistance and

freedom from body effect. The transistors M1 and M2 of Figure 3.9, were realized by the NMOS transistors in the CMOS IC package CD4007.

Capacitor values were selected to be ten times greater than those used for the computer simulation. The switching frequency was, on the other hand, reduced by ten times. This scaling was done for suppressing the effects of stray capacitances of the bread board, used in the experiment. The capacitor values selected are given below:

Feedback capacitor C	= 200 pF
Input capacitor C_i	= 33 pF
Output capacitor C_o	= 68 pF
Capacitor for compensating the threshold voltage dependence	= 56 pF

3.6.2.1 Voltage Monitoring Circuit

The dynamp nodes were to be observed with sufficient precaution since all the nodes are capacitive. The circuit schematic for monitoring the nodes is given in Figure 3.10(b). It is basically a voltage follower followed by sample and hold circuit. The effective input impedance as seen by the dynamp node is very much increased by the source follower SF1. Source follower SF2 should be closely matched with SF1 so that output of op amp OA1 will be the same as dynamp node voltage. OA1 can be a bipolar op amp with very high slew rate. It may be noted that voltage monitoring scheme was adopted for the dynamp integrated circuit also, in

FIG 3.11 CIRCUIT SCHEMATIC FOR SOURCE FOLLOWER AND SAMPLE AND HOLD FOR OBSERVING DYNAMIC SIGNALS.

which source follower MOSFETS SF1 and SF2 are fabricated within the same substrate.

The four phase non-overlapping clock was generated by means of a 1MHz master oscillator and a set of dividers and decoders. The clock edges were separated by 1 sec to provide non-overlapping. Some discussion of the test results is presented in this section, but in order to avoid repetition a detailed analysis will be presented in the discussion of the integrated circuit version having dynamic amplifiers done in the next chapter.

3.6.3 Experiment

The dynamic amplifier integrator was tested, first by applying a 2 V peak to peak square wave signal as the input. The input frequency was chosen to be 1/10th of the sample frequency so that the output signal could be observed, as synchronized with the clock frequency.

Plate 1 shows the waveforms of the input signal, four phase clock (ϕ_1 , ϕ_2 , ϕ_3 , ϕ_4) gate voltage of M1, and the dynamic output. The amplitudes of the signal are not shown to scale. The similarity of the output and gate voltage waveforms of the bread boarded and simulated versions of the circuit can easily be noticed.

- ① INPUT
- ② ϕ_1
- ③ ϕ_2
- ④ ϕ_3
- ⑤ ϕ_4
- ⑥ GATE
- ⑦ OUTPUT

FIG. 3.11. OSCILLOGRAMS OF BREAD BOARD CIRCUIT
WAVEFORMS (NOT TO SCALE)

3.6.3.1 Open Loop Gain

The output and gate voltage waveforms of Plate 1 were used to find the open loop gain of the dynamp as defined in section 3.2. As predicted earlier, the open loop gain was found to vary depending on the actual value of the output voltage. However, there is one major difference between theory and practice. The absolute value of gain is very low varying from 100 to 1000 depending on the output voltage level at which the gain is evaluated. Such a low value of gain is in contradiction to the predicted values of gain which is of the order to tens of thousands. The large reduction in gain can be attributed to the following.

The dc bias applied to the gate of M2 also controls the Miller effect if the bias is too high, M2 may represent a closed switch with a finite ON resistance. If the bias is too low, the absolute magnitude of the current flowing through M1 and M2 will be reduced, resulting in a reduction of gain. Such gain reduction occurs inspite of the fact that a low bias on the gate of M2 would limit the voltage swing on the drain of M1; a fact due to which the Miller effect is reduced. The important thing to remember in this context is that the gain would have been lower if M2 were absent due to C_{gd} .

It has also been proven that the output offset voltage could be controlled by the dc bias applied to the gate of M2. The complete analysis of the dependence of gain and offset voltage on the dc bias on gate M2 is given in the next chapter.

Chapter 4

SC INTEGRATED CIRCUIT USING DYNAMPS EXPERIMENTAL RESULTS

4.1 Introduction

A detailed analysis of a second order switched capacitor notch filter circuit which is fabricated as a monolithic integrated circuit, is presented in this chapter. The filter was first designed as a second order active RC section (biquad). The continuous filter was then transformed into a switched capacitor filter by replacing the resistances with switched capacitors, according to the relationship

$$C = T/R$$

where T is the sampling period. The IC was fabricated as a test vehicle so as to evaluate the performance of the dynamic amplifier which replaced the conventional static op amps. There were provisions in the IC for electrically isolating the two stages of the filter so that the individual integrators could be tested separately.

The integrated circuit was fabricated using NMOS Technology, at the facilities of General Electric Co., Schenectady, New York. The main driver and the tetrode transistors (M1 and M2 of Figure 3.9) of each section were fabricated with 10 micron channel length and 80 micron channel width. The switches were made of 7.5 microns square channel devices.

4.2 Filter Specifications

The frequency specifications of the notch filter are the following:

Notch frequency (fz) (transmission zero)	= 2918.7 Hz
Transmission pole (fp)	= 2600 Hz
Q at pole (Qp)	= 4
DC gain	= 0 dB
High frequency gain	= -2.5 dB

Figure 4.1 shows the circuit diagram of the active RC circuit which meets the above filter characteristics. The transfer function $H(s)$ of the filter w.r.t. Figure 4.1 is given by

$$H(s) = \frac{\frac{C_5}{C_1} (s^2 + \frac{1}{R_1 R_5 C_2 C_5})}{s^2 + \frac{1}{R_3 C_1} s + \frac{1}{R_1 R_2 C_1 C_2}} \quad (4.1)$$

where $S = j\omega$

From equation (4.1) we get

$$\begin{aligned} f_p &= \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}} & \text{DC gain} &= \frac{R_2}{R_5} \\ f_z &= \frac{1}{2\pi\sqrt{R_1 R_5 C_2 C_5}} & \text{High frequency gain} &= \frac{C_5}{C_1} \\ Q_p &= 2\pi f_p R_3 C_1 \end{aligned}$$

The circuit diagram of the switched capacitor filter equivalent to the active RC filter of Figure 4.1 is shown in Figure 4.2 in which static op amps and two phase clocks are employed.

$$R_1 = R_2 = R_5 = \frac{10}{1.04\pi} \text{ M}\Omega$$

$$R_3 = 12.2426 \text{ M}\Omega$$

$$C_1 = C_2 = 20 \text{ PF}$$

$$C_5 = 15.87 \text{ PF}$$

FIG. 4.1 CIRCUIT DIAGRAM OF THE ACTIVE RC FILTER

$$CR_1 = CR_2 = CR_5 = 1.04\pi \text{ PF}$$

$$CR_3 = 0.26\pi \text{ PF}$$

$$C_1 = C_2 = 20 \text{ PF}$$

$$C_5 = 15.87 \text{ PF}$$

FIG. 4.2 EQUIVALENT SC FILTER WITH 2 PHASE CLOCK AND STATIC AMPLIFIERS.

4.3 Description of the Test Vehicle

The complete circuit diagram of the integrated circuit filter employing dynamic amplifiers and having four phase clocks is shown in Figure 4.3. A photomicrograph of the IC is shown in Figure 4.4.

In Figure 4.3, the circuit shown within the dotted box is external to the IC and is intended to observe any node voltage without loading the node considerably. The node under observation is connected to the gate of an in built NMOS transistor (SF3) which functions as a source follower. The V_{gs} drop of SF3 (Figure 4.3) is cancelled by the V_{gs} drop of SF4, by virtue of the particular configuration of the circuit within the dotted box (assuming SF3 and SF4 are identical), and so, the output of static op amp OA1 would represent the actual voltage of the node under observation. The only load for the node besides the filter circuit would be due to the gate capacitance of SF3. The op amp used for this voltage follower is of high slew rate (LM118, 50V/microsecond).

Provisions for observing the input and output of both dynamp integrators are made in the IC. The two sections of the filter can be electrically disconnected by applying $-V_{SS}$ to the nodes marked as XX and YY. Node XX will be tied to V_{DD} and node YY will be connected to clock phase ϕ_3 , for the normal operation of the filter.

FIG 4-4 PHOTOMICROGRAPH OF THE DYNAMIC
AMPLIFIER SWITCHED CAPACITOR FILTER
(COURTESY GENERAL ELECTRIC)

It should also be noted that the two transistors M1 and M2 (similarly M3 and M4) are not physically separated within the IC, but fabricated in such a way that the source of M2 and drain of M1 share the same 'N' diffusion. Hence M1 and M2 together form a single transistor having two gate terminals and therefore is referred as tetrode in later sections.

The IC package is provided with two pairs of pins named as V_{dc1} , V_{ref1} and V_{dc2} , V_{ref2} . V_{dc1} and V_{dc2} are connected to the gates of tetrodes (M2 and M4) so that the effects of tetrode bias on the performance of the dynamp can be studied. The pins referred as V_{ref1} and V_{ref2} are equivalents of the non-inverting inputs of static op amps. The output offset voltages can be adjusted by the voltage biases applied to these two pins.

Yet another point worth mentioning about the IC, is on the realization of the equivalent of switched capacitor resistor CR1 of Figure 4.2. In Figure 4.2, the capacitor CR1 is charged to the output of OA1 during ϕ_1 . The switches are activated in such a sequence that CR1 discharges into the virtual ground of OA2 in the opposite direction, thereby effectively forming a negative resistance. However, such a switching sequence using a single capacitor is not possible in the dynamp filter because of the necessity of a precharging phase. The dynamp, by itself, cannot charge a capacitor directly without losing the voltage it has attained in the previous clock cycle. Therefore, the negative resistance is realized by two equal valued capacitors, each

having twice the capacitance of CR_1 , arranged in a series parallel switching mode. Its operation is as follows.

During any ϕ_3 phase, the capacitance $2CR_{11}$ of Figure 4.3 charges to V_0 , the output voltage of the first stage. This charge which is equal to $2 \times CR_1 \times V_0$ is shared by the second capacitor $2CR_{12}$ (equals $2 \times CR_1$) during the following ϕ_1 phase, with a negative polarity. Hence the net charge in $2CR_{12}$ would be $-CR_1 \times V_0$ which would be discharged into the feedback capacitor of the second stage, during the next ϕ_3 phase. Thus, the charge transfer requirement of the two phase SC filter (Figure 4.2) is met in four phase dynamp filter circuit of Figure 4.3 also. However, the capacitor values of $2CR_{11}$ and $2CR_{12}$ have to be precisely controlled to take account of the stray capacitances associated with the switches, owing to the presence of floating nodes during ϕ_1 , when these capacitors share charges.

We have discussed the circuit details of the IC package so far. The results of the measurements taken on the first stage of the filter are presented in the following sections. Experiments with DC input, could be conducted only on the first stage because the second stage input was capacitively coupled.

4.4 Experiments on the Dynamp Integrated Circuit As An Integrator

4.4.1 Open Loop Gain of the Amplifier

The dynamp is configured as a switched capacitor integrator and as such it cannot be viewed separately as an amplifier alone. So, only the DC open loop gain is meant, when one refers to the open loop gain of the dynamp. The dc open loop gain of the dynamp is measured by evaluating the slope of the 'output voltage vs input dc voltage' characteristics in which the output voltage sample is considered valid, at the end of ϕ_4 .

4.4.1.1 Details of Test Set Up

A variable dc voltage was sampled during ϕ_1 in a 0.1 μF capacitor in order to simulate a sampled analog input for the circuit under test (see Figure 4.5). A sample and hold circuit was added to the op amp assisted source follower circuit of Figure 4.3 so that the node voltage under observation could be viewed as a continuous signal. This additional circuit can be seen in Figure 4.5, in which OA1 is a high slew rate op amp (LM318) and OA2 and OA3 are high input impedance type amplifiers (CA3240). The high input impedance of OA2 and OA3 keeps the voltage decay of sample and hold capacitors to a minimum.

FIG 4.5 CIRCUIT SCHEMATIC FOR SOURCE FOLLOWER AND SAMPLE AND HOLD FOR OBSERVING DYNAMIC SIGNALS.

4.4.1.2 Clock Frequency

The four phase clock had a frequency of 103.956 KHz. The clock was generated by means of a master oscillator and a set of monostable multivibrators so as to ensure non overlapped clocking.

4.4.1.3 Measurements

The continuous output voltage was measured against the dc input voltage, with the tetrode bias as a parameter. The results are plotted in Figures 4.6 and 4.7. Figure 4.6 shows the curves for a full range of input voltage, that is, -7.5V to +7.5V. Figure 4.7 shows the same characteristics in more detail for input voltages around 0 volts, for which the slope of the characteristics is maximum.

4.4.2 Analysis of the Results

The output vs input voltage characteristics can be divided into three sections:

1. A positive saturation region
2. A transition (high gain) region
3. A negative saturation region

Fig. 4-6(a) INPUT V_B OUTPUT CHARACTERISTICS
FOR POSITIVE TETRODE BIAS (V_B)

Fig. 4-6(b) INPUT VS OUTPUT CHARACTERISTICS
FOR NEGATIVE TETRODE BIAS

4.4.2.1 Positive Saturation Region

The output voltage remains at a high positive level for input voltages from -7.5V to -0.5V . However, the output voltage level varies from $+3.7\text{V}$ to $+4.7\text{V}$, in this +ve saturation region, the actual value being a function of the tetrode bias, which varies from -6 volt to $+7$ volt. The output voltage is minimum when the tetrode bias is most positive.

The dependence of the positive maximum value of the dynamic's output voltage, on the tetrode bias can be explained as follows. Consider that the dc input voltage is held constant at a negative value such that the output is at a positive maximum. The output node which is precharged to a voltage of about 5 volt, discharges through M1 and M2 (Figure 4.3) during ϕ_4 . However, the discharge takes place only due to the subthreshold current of M1, as M1 gate would be below threshold. As M2 is in series with M1, the bias on M2 also decides the discharge current. Hence, a more positive bias on the gate of M1 will cause more decay of the output node, thereby reducing the output voltage, at the end of ϕ_4 phase.

4.4.2.2 Transition Region

The open loop gain of the dynamic amplifier is evaluated from this portion of the characteristics. Figures 4.7 (a) and (b) show this portion of the characteristics, expanded

FIG. 4.7(a) FIG 4-6 MAGNIFIED ALONG INPUT VOLTAGE
AXIS, AROUND ZERO INPUT VOLTS.

FIG. 4.7(b)

FIG. 4.6 MAGNIFIED ALONG INPUT AXIS
(TETROD BIAS : POSITIVE)

22
OF / DE

along the input voltage axis. They reveal that the dc open loop gain varies from as low as -30 to as high as -10000, as a function of the tetrode bias. When the tetrode is biased in its threshold region, it offers a very high effective load resistance to the amplifier. Most of the output voltage variations appear, across the drain and source of M2. As explained in Chapter 3, we are now seeing the effect of tetrode bias, on controlling the negative feedback through the parasitic gate-drain capacitance, and thereby, on the net gain of the amplifier. We can expect the gain to increase as the bias on tetrode decreases.

Another interesting point about the gain is that the slope of the characteristics in this region is not constant though it is fairly high, when each curve is considered separately. The slope is higher for positive output voltages than for negative voltages. In addition, the output voltage range for which the gain is high also varies as a function of tetrode bias. This high gain range is proportional (refer to Figure 4.7) to the magnitude of the negative bias on the tetrode gate. A simple explanation for this behaviour can be given as follows.

The tetrode passes through its saturation and triode regions as the output voltage decays during ϕ_4 . When tetrode is in saturation, it offers a very high effective output impedance. In the triode region, the tetrode behaves like a voltage controlled resistor, whose value is controlled by the tetrode bias. Hence, we can expect that, if the output voltage at the end of ϕ_4 is low enough to bring the

tetrode to its triode region, the amplifier gain would be reduced. In other words, if the input voltage and tetrode bias are such that the final output level is high enough to keep the tetrode in its saturation region [where $V_{ds} > V_{gs} - V_{TH}$], then, the gain of the amplifier would be high. This gives rise to the variable slope of the output characteristics, in the transition region.

4.4.2.3 The Negative Saturation Region

The output voltage saturates to its negative maximum value, when the input voltage is greater than zero volt. For the dynamp IC, this minimum value is found to be only $\sim 6.5V$ which is one volt above V_{SS} , the negative power supply. This reduction in the negative maximum level can be explained as follows, with respect to Figure 4.3.

The circuit works on the basis of storing a voltage equal to $V_{SS} + V_{TH}$, across the capacitor Cos . This is done by short circuiting the drain and gate of $M1$ during ϕ_1 and allowing the capacitor Cos to discharge through $M1$, until the voltage at the combined node reaches the threshold voltage, when the transistor $M1$ enters the subthreshold region. However, for this to take place effectively, the voltage of $M1$'s drain just before ϕ_1 , should be greater than its threshold voltage. Now, if we assume that $M1$'s drain has fallen below its threshold voltage, at the end of any ϕ_4 then Cos will not have $V_{SS} + V_{TH}$ across its plates at the end

of the following ϕ_1 . The net result is that a fraction of the input voltage will be used up to cover this loss of voltage across C_{os} , in the following charge transfer phase (ϕ_3). Indirectly, this assumption would suggest the presence of a fictitious negative voltage at the input, the tendency of which would be to keep the output voltage more positive than negative.

The circuit can be looked at, in another way also. The circuit path on either side of the output node becomes of a high impedance state towards the end of every ϕ_4 , because switch ϕ_2 would be OFF and M_1 is near threshold. Besides, the drain current through M_1 will be decided by both its drain and gate voltages when the voltage levels are low enough. Hence, the ideal charge transfer may not take place, thereby making it impossible for the output voltage to reach the lowest limit which is V_{SS} . The steady state output voltage at the intersection of two high impedance devices connected to V_{DD} and V_{SS} , and carrying only leakage current, can only be between V_{DD} and V_{SS} .

4.4.3 Offset Voltage

A simple way of evaluating the output offset voltage is by applying zero volts to the input and then to measure the output voltage. However, this technique is not adequate for the dynamic amplifier, because it is configured as an integrator. The offset voltage gets integrated, during every cycle and eventually the output saturates to its maximum

positive value as can be seen in Figure 4.8.

Although the high output offset voltage of the dynamp is a disadvantage, the integrated dynamp circuit can still be effectively used as a building block in switched capacitor filters. The offset voltage can be cancelled by applying a suitable dc bias on the terminals marked as V_{ref1} and V_{ref2} which are shown in Figure 4.3.

So far, we have been discussing the results of experiments conducted on the individual dynamp integrator. We shall now discuss the results of the frequency response measurements carried out on the IC, when configured as a switched capacitor notch filter.

4.5 Measurement of Frequency Response of the Notch Filter

4.5.1 Preliminary Set Up

The IC was configured to be a notch filter by making the following connections:

1. The node marked as XX in Figure 4.3 was connected to V_{DD} so that the feed back path to the first stage from the second stage could be established.

2. The node marked YY was connected to clock phase ϕ_3 in order to complete the forward path. The schematic of the test set up is shown in Figure 4.9(a).

The input voltage was sampled and stored in a $0.1 \mu F$ capacitor, external to the IC, during ϕ_1 . This capacitor is

FIG. 4-8 OUTPUT OFFSET VOLTAGE VS TETRODE BIAS
 CHARACTERISTICS OF THE DYNAMP INTEGRATOR

then connected to the input terminals marked as $V_i(n)$ in Figure 4.3, during ϕ_3 . A separate sample and hold amplifier was not necessary after the 0.1 μF because the largest capacitor within the IC is only 20 pF which is 5000 times smaller than 0.1 μF capacitor. The charge lost from the sampling capacitor was therefore negligible. The output of the filter is obtained as a continuous signal $V_o(t)$ by means of the circuit shown in Figure 4.5.

In order to optimize the frequency response of the filter so as to match the predicted response, the biases on the tetrode gates and the dynamic reference inputs (V_{REF1} and V_{REF2}) were to be precisely adjusted. The dc biases, thus optimized experimentally are given below.

First stage:	Integrator without resistive feedback
Tetrode bias	-3.476 V
V_{REF1}	-0.388 V
Second stage:	Integrator with resistive feedback
Tetrode bias	1.515 V
V_{REF2}	1.581 V

4.5.2 Sampling Clock

A sampling frequency of 103 KHz was used for the frequency response measurements. The timing diagram of the four phase clock is shown in Figure 4.9(b). The clock was generated by means of a master oscillator, a chain of monostable multivibrators and D flip flops, all belonging to CMOS logic family.

FIG 4-9(a) CIRCUIT SCHEMATICS USED FOR FREQUENCY RESPONSE MEASUREMENTS

FIG 4.9(b) FOUR PHASE CLOCK WAVEFORMS FOR THE DYNAMP FILTER UNDER TEST

4.5.3 Instrumentation

A programmable signal generator (HP3722) was used as the signal source for the continuous input voltage. The output was observed using a Tektronix 475 oscilloscope. The frequency response was observed using a spectrum analyzer also.

4.6 Experiments and Analysis

A sine wave of variable frequency and constant amplitude (2V peak to peak) was used as $V_i(t)$ in the circuit of Figure 4.9(a). The measured amplitude response is compared with the predicted response in Figure 4.10 in which the solid curve and the dotted curve represent the former and latter responses respectively. The predicted (theoretical) response is evaluated on the basis of the Z domain transfer function $H(z)$ of the sample data filter. The transfer function which is derived in Appendix 3, is given below as

$$H(z) = \frac{C_5}{(C_1 + C_3)} \times \frac{z^2 - (2 - \frac{C_{R1} C_{R5}}{C_2 C_5}) z + 1}{z^2 - (2C_1 + C_3 - \frac{C_{R1} C_{R2}}{C_2}) z + \frac{C_1}{(C_1 + C_3)}} \quad (4.2)$$

where

$$z = e^{j\omega T}$$

ω = signal frequency in radians/sec.

and the capacitors are w.r.t. Figure 4.9(a).

FIG 4.10. DYNAMIC AMPLIFIER NOTCH FILTER RESPONSE.
 THE THEORETICAL CURVE IS OBTAINED BY
 ANALYZING THE FILTER IN THE Z-DOMAIN.

The experimental results obtained for the notch filter show very good agreement with the theoretically predicted results, as one can see in Figure 4.10. The low frequency attenuation differs by 0.2 dB from the predicted value, whereas, the high frequency attenuation differs by 0.5 dB. The notch frequency is obtained as 3.014 KHz instead of 3.0172 KHz which is the theoretical notch frequency for a sampling frequency of 103 KHz. The attenuation at the notch frequency is greater than 60 dB.

4.7 Frequency Response of the IC as a Low Pass Filter

Referring to Figure 4.9(a) the integrated circuit can be configured as a low pass filter by:

1. By floating the input terminal which is connected to the capacitor C_5 or
2. By connecting the above input terminal to the signal reference such that C_5 would be connected between the signal ground and the dynamic's virtual ground.

The first method is not advisable because a floating pin can pick up high frequency noise and cause error in the output. However, if the IC is meant to be used only as a LPF, then capacitor C_5 need not be realized within the IC at all.

The second method was adopted to realize the LPF (low pass filter) in the experiment. The technique of connecting C_5 to ground has the same effect of not having C_5 at all, if the gain of the second stage is high enough to consider the

input node of the dynamp as a virtual ground. However, in reality, the second stage gain is small and as such, the low pass response is affected by the dynamp's finite gain.

4.7.1 Analysis of Experimental Results

The theoretical and experimental responses are in good agreement in the pass band of 0 to 4 KHz (3 dB pass band) as can be seen in Figure 4.11. The error is less than 0.5 dB. However, the error increases up to 4 dB in the high frequency end of the response curve in which the measured high frequency attenuation is greater than expected. The reasons for this higher attenuation are given below.

1. The second stage of the filter has a tetrode bias 1.515 V, which is high enough to lower the open loop gain to about 200. The capacitors (C_1 , C_{R3} and $2C_{R1}$) connected to the input of the amplifier would not discharge completely by the end of t_4 , because of the low gain of the dynamp.

2. The capacitor C_5 which is grounded would reduce the effective input impedance of the amplifier, again due to its finite gain. This effect of C_5 is more prominent at higher frequencies.

A more detailed discussion on the performance of a switched capacitor filter, having a finite gain amplifier is presented in the next chapter.

Fig. 4.11. AMPLITUDE RESPONSE OF THE INTEGRATED CIRCUIT WHEN CONNECTED AS A LOW PASS FILTER.

4.8 Frequency Response as a High Pass Filter

A first order, high pass filter can be realized from the IC by making the following connections.

1. Separate the two stages of the filter by applying V_{SS} (≈ 7.5 V) to gates of switches XX and YY in Figure 4.9(a).

2. Apply the input voltage samples to capacitor C_5 .

Now, the second stage, consisting of capacitors C_5 , C_1 switched capacitor C_{R3} and the dynamp, becomes a high pass filter. The Z domain transfer function $H(z)$ of this switched capacitor HPF is given by

$$H(z) = \frac{V_0(z)}{V_1(z)} = - \frac{(1-z^{-1}) \times C_5}{(1-z^{-1}) \times C_1 + C_{R3}} \quad (4.3)$$

Such a high pass filter was built and the frequency response was measured. The results are plotted as the solid curve in Figure 4.12. The dotted curve in the same figure represents the theoretical response, based on (4.3).

The measured response matches the predicted response within 0.5 dB, when the signal frequency is greater than 1000 Hz. This difference of 0.5 dB can be accounted by the low open loop gain of the second stage. The stray capacitances at the input of the amplifier also will have a degrading effect when the amplifier's gain is low.

FIG 4.12 FREQUENCY RESPONSE OF HIGH PASS FILTER

4.9 Conclusion

Results of the frequency response experiments on the integrated dynamic amplifier filter circuit have been presented and analyzed. The measured responses of the IC when it was configured as a low pass and a notch filter were in good agreement with theory. The error was less than 0.5 dB. The high pass filter response of the second stage was in good agreement, only in the pass band. Its response in the stop band differed from theory by as much as 2 dB. This discrepancy may be attributed to the second stage having a lower gain, due the relatively high positive bias applied to its tetrode gate.

The next chapter discusses the effect of finite gain on the frequency response of the filter. The effect of power supply noise also is analyzed in the same chapter.

EFFECT OF FINITE GAIN AND ANALYSIS OF POWER SUPPLY NOISE REJECTION

5.1 Introduction

We have seen in Chapter 4 that measured and ideal frequency responses of the various filter circuits derived from the integrated circuit, are in good agreement. Any significant difference between the predicted and experimental responses was observed only in the high frequency end of the pass band, and even this difference is less than 0.5 dB. This mismatch can be accounted for by the following factors:

1. The low gain of the second stage.
2. Stray capacitance of the virtual ground node of the second stage.
3. Stray capacitances of switches associated with the switched capacitor resistors, labelled as CR11 and CR12 in Figure 4.9(a).
4. A slight error contributed by the attenuation of high frequency signals due to the $\sin X/X$ factor associated with the spectrum of a sampled analog signal. X in this case stands for $\pi \times \text{Signal Frequency/Clock Frequency}$. This error is too small to be considered for signal frequencies which are much below the Nyquist limit.

The above factors are discussed in more detail below.

FIG 5.1(a) CIRCUIT DIAGRAM OF THE SECOND STAGE
MODELLED FOR V_{SS} NOISE ANALYSIS

the filter, by considering the finite gain of the second stage and is given in (5.1). Equation (5.1) takes care of the effects of stray capacitance at the input node of the amplifier.

$$\frac{V_0(z)}{V_1(z)} = \frac{C_5 (1 - Z^{-1})}{\left(\frac{1}{A} (C_{R3} + C_S + C_5) - C_1 \left(1 - \frac{1}{A} \right) \right) (1 - Z^{-1}) + C_{R3} \left(\frac{1}{A} - 1 \right) + \frac{C_{R3}}{2A}} \quad (5.1)$$

where A is the gain and

C_S is the stray capacitance.

Equation (5.1) predicts an error of 0.3 dB when A is 100. The remaining error of 0.2 dB may be attributed to the clock feedthrough in the sample and hold switches and any other imperfection which are signal to the IC. It is interesting to note that the effect of low amplifier gain is to increase the effective values of feedback capacitor C_1 and the damping (SC) resistor C_{R3} . Hence one can expect a corresponding decrease in the notch frequency, from the predicted value. The previous experiments have proven this point by the fact that the measured notch frequency was 3.014 KHz instead of the predicted 3.017 KHz.

5.3 Effect of Power Supply Noise

Rejection of power supply noise is an important requirement for most types of amplifiers, including the dynamic amplifier. For switched capacitor filters, especially the switching transients can induce more noise

into the power supply. In telecommunications systems, where banks of such filters are used, the problem of power supply noise become more severe. Because of its significance, an analysis of the effect of power supply noise on the circuit performance is presented here.

5.3.1 V_{DD} Noise

The effect of noise on the V_{DD} line (positive power supply) can be analyzed considering V_{DD} as a signal represented by

$$V_{DD}(t) = V_d + V_n(t) \quad (5.2)$$

where V_d is a noise free dc voltage and V_n(t) is the noise on the dc supply voltage.

Consider the decay of the output voltage V_o(t) of the dynamp ignoring the parasitic elements during ϕ_4 . V_o(t) is then given by (refer to equation (3.15))

$$V_o(t) = V_o(n) - V_i(n) \alpha_1 + \frac{1}{\frac{k t}{2C[\alpha_1 + \frac{1}{\alpha_1}]} + \frac{1}{V_p - V_o(n) + \alpha_1 V_i(n)}} \quad (5.3)$$

where V_p is the precharge voltage and is given by

$$V_p = V_{DD} - V_{TH}$$

where V_{TH} is the threshold voltage of switch ϕ_2 (ref Figure 4.3). Equation (5.3) is the same as equation (3.15) with the exception that we precharge voltage is V_p , instead of V_{DD} .

It is clear from (5.3) that, for ideal conditions in which the open loop gain is very high, small variations in V_p due to noise do not have significant effect on the output. Equation (5.3) can be expressed, by replacing the variables by typical values, as

$$V_0(n+1) = V_0(n) - \alpha_i V_i(n) + \frac{0.51 \times 10^{-3} [V_p(n) - V_0(n) + \alpha_i V_i(n)]}{V_p(n) - V_0(n) + \alpha_i V_i(n) + 0.51 \times 10^{-3}} \quad (5.4)$$

In (5.4) V_p is replaced by $V_p(n)$ just to suggest that it could be a time dependent value. In any case, (5.4), indicates that small variations in V_p (or V_{DD}) due to noise, do not have significant effect on the output voltage. The only way for V_{DD} noise to be present in the output signal is through stray capacitances associated with the precharge switch. The small portion of the noise which gets into the output signal will experience the loop gain of the filter and will show a specific response as a function of frequency. This response is derived in the next section which deals with the effect of V_{SS} noise.

5.4 Analysis of the Effect of V_{SS} Noise

The noise on the negative power supply (V_{SS}) directly affects the output voltage of the dynamp since V_{SS} is directly tied to the substrate and source of the active transistor. The noise voltage on the V_{SS} line can affect the output transient significantly, during ϕ_4 .

The second stage of the filter is redrawn in Figure 5.1(a) showing the parasitic capacitances which also contributes to the V_{SS} noise. Figure 5.1(b) shows the output transient as well as the important sampling instants. Since V_{SS} is a continuous signal, it is not quite valid to consider it as sampled data. However for the purpose of simple analysis, the noise voltage V_N also is considered sampled, with fractional sampling period. Valid output samples are taken at the end of ϕ_1 . How V_{SS} affects the output voltage can be explained in the following manner. In the absence of V_{SS} noise, the output voltage $V_0(n+1)$ of the circuit in Figure 5.1(a), ignoring the stray capacitances $\alpha_d C$ and $\alpha_s C$ is given by

$$V_0(n+1) = \frac{V_0(n) - \alpha_1 V_1(n)}{(1+\alpha_3)}$$

The above expression is valid because, the circuit brings down the value of the gate voltage to be equal to $V_{SS} + V_{TH}$ at the end of every ϕ_4 . Hence the reference is actually to V_{SS} and not to the signal reference voltage or analog ground as in the case of a static op amp. Therefore, any noise in the V_{SS} line, would cause the output voltage (at the end of

ϕ_4) to adjust itself such that V_g , the gate voltage is equal to $V_{SS} + V_{TH}$. The deviations from this assumptions are due to (1) finite time duration of ϕ_4 , (2) V_N being continuous, (3) stray capacitances associated with the devices, which become significant at higher noise frequencies, and (4) body effect applied to the tetrode.

The output voltage sample $V_o(n)$ of the circuit in Figure 5.1(a) and with reference to the sampling instants of timing diagram in Figure 5.1(b) can be derived in terms of $V_N(n)$, the noise voltage sample and $V_i(n)$, the input sample, based on the assumptions given above. The corresponding difference equation is

$$\begin{aligned} & \frac{V_o(n+1) - V_o(n) + V_i(n)\alpha_i + V_o(n+1)\alpha_3}{K1} \\ & + \frac{[V_o(n+1) - V_N(n)]\alpha_d}{K2} + \frac{[V_N(n+0.65) - V_N(n)]\alpha_s}{K2} \\ & - [V_N(n+0.65) - V_N(n)] = 0 \end{aligned} \quad (5.5)$$

$$\text{where } K1 = \frac{1}{2\alpha_i + \alpha_3 + \alpha_4 + 1 + \frac{\alpha_{os}(\alpha_s + \alpha_d)}{\alpha_{os} + \alpha_s + \alpha_d}} \times \frac{\alpha_{os}}{(\alpha_{os} + \alpha_d + \alpha_s)}$$

$$\text{and } K2 = \frac{1}{\alpha_s + \alpha_d + \frac{\alpha_{os}(2\alpha_i + \alpha_3 + \alpha_4 + 1)}{\alpha_{os} + 2\alpha_i + \alpha_3 + \alpha_4 + 1}}$$

The coefficients ' α 's are the capacitor ratios in the circuit. It may be noted that (5.5) is a general expression and can be applied to the first stage of the filter also.

FIG 5.1(b) TYPICAL OUTPUT VOLTAGE WAVEFORM
SHOWING THE SAMPLING INSTANTS USED FOR
VSS NOISE ANALYSIS

For the first stage, (a) $\alpha_3=0$; (b) $2\alpha_i$ becomes α_i , and (c) $\alpha_4=0$. Also, α_d can be neglected because the high gain effect of tetrode is very significant in the first stage.

The effect of V_{SS} on the filter is analyzed with the aid of equation (5.5). Each stage is considered separately, as having noise in the V_{SS} line. The noise transfer functions of the filter, when noise is applied separately to each stage are found and then vectorially added together to get the total V_{SS} noise response. The circuit model for V_{SS} noise analysis is given in Figure 5.2, in which the noise source is modelled to be a signal source applied to the non inverting input of a hypothetical op amp. The individual transfer functions in the Z domain for V_{N1} and V_{N2} are derived in Appendix 2. The transfer functions, assume that the noise is considered valid only during the interval of beginning of ϕ_2 phase to the end of ϕ_4 phase. Thus the effect of noise is only for a period of 0.65 times the sampling period.

The transfer functions are

$$\frac{\dot{V}_0(z)}{V_{N1}(z)} = \frac{(Z^{0.65}-1) \left(\frac{K_{21}-\alpha_s}{1+\alpha_1+\alpha_{os}} \right) \alpha_{os} \alpha_1}{((1+\alpha_3 + \frac{\alpha_d \alpha_{os}}{\alpha_T}) Z - 1) (Z-1) + \alpha_1^2 Z}$$

$$\text{where } K_{21} = \frac{1}{\alpha_s + \frac{\alpha_{os} (1+\alpha_1)}{\alpha_{os} + 1 + \alpha_1}} \quad \text{and} \quad \alpha_T = \alpha_{os} + 2\alpha_1 + \alpha_3 + \alpha_4 + 1 \quad (5.6)$$

and

$$\frac{V_0(z)}{V_{N2}(z)} = \frac{(Z-1) ((K_2-\alpha_s) (Z^{0.65}-1) + \alpha_d)}{(((1+\alpha_3) \frac{\alpha_T}{\alpha_{os}} + 2\alpha_d) (Z-1) + \alpha_1^2 \frac{\alpha_T}{\alpha_{os}}) Z - (\frac{\alpha_T}{\alpha_{os}} + \alpha_d) (Z-1)} \quad (5.7)$$

FIG 5.2 CIRCUIT MODEL FOR V_{SS} NOISE ANALYSIS

FIG. 5.3 VSS NOISE VS OUTPUT - FREQUENCY RESPONSE (THEORETICAL)

The frequency responses based on (5.6) and (5.7,3) and their sum are evaluated and plotted in Figure 5.3. The coefficient values for the plots are the design values used in the integrated circuit and are taken from section 4.2.

Figure 5.3 shows that the overall V_{SS} noise response of the filter would be relatively poor. Noise frequencies below the transmission pole (2.6 KHz) of the Notch filter are contributed, significantly by the first stage. The closed loop response of the first stage noise (considered alone) is that of a bandpass filter. The second stage noise finds itself in a high pass filter and contributes significantly to the filter output, for noise frequencies above the transmission pole. The absolute value of the peak level in the noise response is determined by the Q of the filter, which is controlled by the value of the capacitor C_3 .

5.5 Measurements

The analysis of the effect of power supply noise has been verified by measurements. The circuit schematic for the measurements is shown in Figure 5.4. The spectrum analyzer (Model HP3580) is set up in the network analyzer mode, in which a sweep frequency sine wave is generated and can be applied to the network under test. The sinewave signal is added to the appropriate dc supply voltage and the resulting signal is applied to the appropriate power supply pin of the dynamp IC. The IC is configured as a notch filter with its input grounded. The filter output is converted as a output

FIG 5.4 BLOCK DIAGRAM OF TEST SET UP FOR POWER SUPPLY NOISE RESPONSE ANALYSIS

as a continuous time signal using the circuit of Figure 3.11. The continuous time output signal is fed to the input of the network analyzer, for frequency response measurements. It may also be noted that, a normal frequency response measurement of the notch filter, also was taken, and plotted along with the noise response curves. The results as plotted by the spectrum analyzer are shown in Figure 5.5.

5.6 Results

Figure 5.5 shows three calibration levels also, in addition to noise responses. It is seen that both V_{DD} and V_{SS} noise responses peak at the transmission pole of the filter. However, the level of V_{DD} noise in the output is very low, as predicted earlier. Yet, the level of -38 dB at the peak is much higher than one would expect. The main culprit for this behaviour is the stray capacitances, associated with the ϕ_4 switches.

The V_{SS} noise response, obtained experimentally is shown in Figures 5.5 and 5.6. In Figure 5.6, the theoretically predicted noise response also is shown for the purpose of comparison.

The V_{SS} noise performance is, on an average worse than predicted, with the exception that the level at the pole frequency is less than the predicted value. The reasons for this error may be attributed to the following:

FIG 5.5 SPECTRUM ANALYZER PLOTS OF THE OUTPUT SIGNAL LEVEL OF THE NOTCH FILTER AS A FUNCTION OF FREQUENCY WHEN THE INPUT SIGNAL IS APPLIED TO:
 CURVE ① IN SERIES WITH THE POSITIVE POWER SUPPLY (V_{DD})
 CURVE ② IN SERIES WITH THE NEGATIVE POWER SUPPLY (V_{SS})
 CURVE ③ THE NOTCH FILTER INPUT

FIG. 5.6. NOTCH FILTER OUTPUT VS V_{SS} NOISE
AS A FUNCTION OF FREQUENCY

1. Errors in assuming the V_{SS} noise as continuous. A more realistic analysis may be applied, rather than considering noise as a sampled signal.

2. The analysis was done basically from the point of view of a switched capacitor circuit, rather than as a continuous analog circuit. Since V_{SS} noise, sees the circuit as a common gate amplifier, the predicted low frequency gain may be too much underestimated, since it was decided mainly by capacitors.

3. The assumption that V_{TH} as stored in the capacitor $a_{OS}C$ will be constant also, cannot be quite valid. Since V_{TH} is dependent on the voltage between the drain and source. These factors were not considered in the earlier analysis and may be accounted for the increased gain for the V_{SS} noise.

4. The tetrode also contributes to the V_{SS} noise, due to body effect. The substrate potential of the tetrode follows the noise, resulting in unsteady threshold voltage. As the tetrode has tremendous control over the gain, a noisy substrate potential would introduce noise in the output significantly.

The notch filter response seen in Figure 5.5 is in good agreement with expected values, and has already been discussed in detail in Chapter 4.

Chapter 6

CONCLUSIONS

6.1 Summary

A study of a novel NMOS dynamic amplifier and its applications as a building block for switched capacitor filter ICs was described in this thesis. The few dynamic amplifier circuits which are already reported in the literature were considered and the simplest among them was chosen for further development. The selected circuit which was originally reported by Copeland and Rabey required an NMOS transistor with very high threshold voltage and had relatively low gain.

The original dynamp was modified by adding 3 switches, a capacitor and by converting the common source amplifier into a cascode amplifier. A qualitative analysis of the operation and performance of the circuit was presented. The qualitative analysis was then supported by computer simulation (SPICE analysis) of the circuit.

A bread board model of the new dynamp was built and characterized in order to supplement the computer simulation. Following the satisfactory performance of the bread board model and computer simulation, a switched capacitor filter integrated circuit was fabricated, in which the static op amps were replaced by the new dynamps. The IC was of NMOS technology and was fabricated at the facilities of General Electric, Schenectady, New York.

The integrated circuit chip measured approximately 650 microns x 850 microns at the bonding pad edges. It drew a power supply current of 68 A from ± 7.5 volt powersupplies at a clock rate of 100 KHz. The IC was fabricated as a test vehicle and therefore had provisions to configure the circuit as a notch, low pass or high pass filter.

Details of the IC characterization were presented and it was shown that the measured frequency responses of the various filter configurations agreed very well with the predicted responses. The dynamic range of the dynamp output was greater than 50 dB.

The disadvantages of the circuit also were pointed out which are mainly asymmetry in the maximum output signal swing and poor rejection of the negative power supply noise. An analysis of the power supply noise rejection of the IC also was presented.

6.2 Conclusion

The work reported in this thesis has demonstrated the feasibility of realizing SC filters using simple dynamic amplifiers which use only a dual gate NMOS transistor (cascode stage), a small capacitor and five NMOS switches of minimum size geometry. The chip area and power consumption specifications of the dynamp are small compared to other circuits reported, and therefore it has potential for large scale use in SC filter integrated circuits. The main deterrents against its general acceptance are (1) the output

voltage swing asymmetry and (ii) low V_{SS} noise rejection.

6.3 Suggestions For Future Work

The two main drawbacks of the dynamp can be minimized by carrying out the following suggestions.

The problem of output voltage asymmetry, i.e., the positive maximum level being more than 3V below V_{DD} due to body effect in switch $\#2$, can be solved by replacing that switch by a PMOS switch. Obviously, this proposal suggests the use of CMOS technology. However, in the light of the recently increased interest in CMOS technology, the above suggestion may not be out of place. Use of a PMOS switch having its N well tied to V_{DD} , avoids the body effect, thereby allowing the precharge voltage at the output node to reach the positive supply rail.

Solutions for improving the V_{SS} noise rejection are not that simple. However a modification of the conventional power supply decoupling scheme may improve the situation, as suggested below.

Usually, the negative as well as positive power supply voltages are fed to the power supply pins of the IC, through a LC or RC filter which functions as a decoupling filter. One may recall that it is the noise which exists in the V_{SS} line during the clock phase ϕ_4 that contributes most to the output noise. Hence, if the V_{SS} line can be held fairly constant during the clock phase ϕ_4 or even ϕ_3 , then the

noise will not appear at the output. This can be achieved by replacing the conventional decoupling filter by a sample and hold circuit. The negative power rail should be sampled during clock phase ϕ_1 and held during ϕ_3 in a capacitor (around 25 μF) which should be external to the IC. The sampling switch can be part of the IC itself.

Once the above problems are solved to a satisfactory level, work can be carried out to reduce the number of clock phases from four to two or three.

In conclusion, it can be stated that though the dynamp IC in its present form may not be suitable for industrial production due to its disadvantages, the suggestions given above are worth investigating, because the interest in switched capacitor filters is still growing within the semiconductor industry, as can be seen in current literature.

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APPENDIX 1

Transfer function of the second stage, with finite gain amplifier. (Ref.: Section 5.2, Equation (5.1)).

The circuit diagram of the second stage of the integrated circuit is shown in Figure A1.1, in which the dynamp is represented by the conventional symbol of the op amp. Switches are shown as ideal.

Figure A1.1. Second Stage (High Pass Filter Section) of the IC With Finite Gain Amplifier

The following are assumed for the purpose of deriving the transfer function of the second stage which has a gain of the order of only -100.

1. C_5 is the stray capacitance, present at the amplifier input denoted by *.

2. The voltage $V^*(n)$ is the voltage sample at the end of 4 phase and would be negligible if the gain A is very high.

3. $C_{R1} = C_{R2}$

By definition of the gain of the dynamp, we get

$$V_o(n) - V_o(n-1) = A(V^*(n) - V^*(n-1)) \quad (A.1)$$

where the voltage samples are taken at the end of 4 phase. Equating the charge transferred through capacitor C_5 to the charges flown through the other capacitors, between two consecutive sample periods, we get

$$\begin{aligned} & ((V_i(n) - V^*(n)) - (V_i(n-1) - V^*(n-1))) C_5 \\ & = (V^*(n) - V^*(n-1)/2) C_{R1} + (V^*(n) - V^*(n-1)) C_5 \\ & + (V^*(n) - V_o(n) - (V^*(n-1) - V_o(n-1))) C_1 \\ & + (V^*(n) - V_o(n)) C_{R3} \end{aligned} \quad (A.2)$$

Taking Z transform of (A.2) and rearranging, we get

$$\begin{aligned} V_i(z)(1-Z^{-1}) C_5 & = V^*(z)(1-Z^{-1}) C_5 + V^*(z)(1-Z^{-1}/2) C_{R1} \\ & + V^*(z)(1-Z^{-1}) C_5 + V^*(z)(1-Z^{-1}) C_1 \\ & - V_o(z)(1-Z^{-1}) C_1 + V^*(z) C_{R3} - V_o(z) C_{R3} \end{aligned} \quad (A.3)$$

Taking the Z transform of (A.1), $V^*(z)$ can be expressed as

$$V^*(z) - V^*(z)Z^{-1} = 1/A V_o(z) - V_o(z) Z^{-1}$$

$$V^*(z) = V_o(z)/A \quad (A.4)$$

Substituting (A.4) in (A.3) we get

$$V_1(z) C_5 = V_0(z) \left(\frac{1}{A} (C_5 + C_{R1} + C_5 + C_1) - C_4 + \frac{C_{R1} z^{-1}}{2A(1-z^{-1})} + \frac{C \left(\frac{1}{A} - 1 \right)}{1 - z^{-1}} \right) \quad (A.5)$$

From (A.5) the transfer function $H(z)$ is given by

$$H(z) = \frac{V_0(z)}{V_1(z)} = \frac{C_5 (1 - z^{-1})}{\left(\left(\frac{1}{A} (C_5 + C_{R1} + C_5) - C_1 \left(1 - \frac{1}{A} \right) \right) (1 - z^{-1}) + C_{R3} \left(\frac{1}{A} - 1 \right) + \frac{C_{R1} z^{-1}}{2A} \right)} \quad (A.6)$$

APPENDIX 2

Derivation of transfer function for V_{SS} noise vs output.

Refer to Figures 5.1(a), 5.1(b) and 5.2.

Case 1 V_{N2} is considered zero.

With reference to equation (5.5) which expresses the output voltage sample in terms of noise and input samples, we can write

$$\begin{aligned} \frac{V_{01}(n+1) - V_{01}(n)}{K_{11}} - (V_{N1}(n+0.65) - V_N(n)) \left(1 - \frac{1}{K_{21}}\right) \\ + \frac{\alpha_1}{K_{11}} V_0(n+1) = 0 \end{aligned} \quad (A2.1)$$

(A2.1) assumes that the Miller capacitance α_d of the first stage is negligible.

In (A2.1),

$$K_{11} = \frac{1}{1 + \alpha_1 + \frac{\alpha_{os} \alpha_s}{(\alpha_{os} + \alpha_s)}} \cdot \frac{\alpha_{os}}{(\alpha_{os} + \alpha_s)}$$

$$K_{21} = \frac{1}{\alpha_s + \frac{\alpha_{os}(1 + \alpha_1)}{\alpha_{os} + 1 + \alpha_1}}$$

K_{11} and K_{21} are the capacitive voltage divider ratios, for the different voltages appearing at the gate of M1 in Figure 5.1(a) or the inverting input terminal of A1 in Figure 5.2.

Let

$$\alpha_{T1} = 1 + \alpha_{os} + \alpha_1$$

Then

$$\frac{K_{11}}{K_{21}} = \frac{\alpha_{os}}{\alpha_{T1}}$$

Rearranging (A2.1) we get

$$V_{01}(n+1) - V_{01}(n) = -\alpha_i V_0(n+1) + (V_{N1}(n+0.65) - V_N(n)) \\ \times (K_{21} - \alpha_s) \frac{K_{11}}{K_{21}}$$

Taking Z transform of the above

$$V_{01}(Z) (Z-1) = -V_0(Z) (\alpha_i Z) + V_{N1}(Z) (Z^{0.65}-1) (K_{21} - \alpha_s) \frac{\alpha_{os}}{\alpha_{T1}} \\ (A2.2)$$

In order to eliminate V_{01} from (A2.2), V_{01} can be expressed in terms of V_0 as

$$\frac{(V_0(n+1) - V_0(n)) + V_0(n) \alpha_3}{K_1} + \frac{V_0(n+1) \alpha_d}{K_2} - \frac{V_{01}(n) \alpha_i}{K_1} = 0 \\ (A2.3)$$

Taking Z transform of (A2.3) and rearranging

$$V_0(Z) \left(\left((1 + \alpha_3 + \frac{\alpha_d \alpha_{os}}{\alpha_T}) Z - 1 \right) \frac{(Z-1)}{\alpha_i} + \alpha_i Z \right) \\ = V_{N1} (Z^{0.65}-1) (K_{21} - \alpha_s) \frac{\alpha_{os}}{\alpha_{T1}}$$

$$\text{where } \alpha_T = 1 + 2\alpha_i + \alpha_3 + \alpha_4 + \alpha_{os} \quad (A2.4)$$

From (A2.4), the required transfer function is

$$\frac{V_0(z)}{V_{N1}(z)} = \frac{\frac{K_{21} - \alpha_s}{\alpha_{T1}} \alpha_{os} \alpha_i (Z^{0.65}-1)}{\left((1 + \alpha_3 + \frac{\alpha_d \alpha_{os}}{\alpha_T}) Z - 1 \right) (Z-1) + \alpha_i^2 Z} \\ (A2.5)$$

Case 2 $V_{N1} = 0$, V_{N2} active

The output sample of the second stage, V_0 is obtained from the difference equation

$$\frac{V_0(n+1) - V_0(n) + V_{01}(n) \alpha_1 + V_0(n+1) \alpha_3}{K_1} + \frac{(V_0(n+1) - V_{N2}(n)) \alpha_d}{K_2} - (V_{N2}(n+0.65) - V_N(n)) + (V_{N2}(n+0.65) - V_{N2}(n)) \frac{\alpha_s}{K_2} = 0 \quad (A2.6)$$

where K_1 and K_2 are already defined in (5.1) and

$$\frac{K_1}{K_2} = \frac{\alpha_{os}}{\alpha_T}$$

Taking Z transform of (A2.6) and rearranging

$$V_0(z) \left(\frac{(1+\alpha_3)}{K_1} z + \frac{\alpha_d}{K_2} z - \frac{1}{K_1} \right) = -V_{01} \frac{(z) \alpha_1}{K_1} + V_{N2}(z) (z^{0.65} - 1) \left(\frac{K_2 - \alpha_s}{K_2} \right) + \frac{V_N(z) \alpha_d}{K_2} \quad (A2.7)$$

Multiplying both sides of (A2.7) by K_2 and substituting for

$$V_0(z) \left[((1 + \alpha_3) \frac{\alpha_T}{\alpha_{os}} + \alpha_d) z + (z-1) \alpha_d - \frac{\alpha_T}{\alpha_{os}} \right] = \frac{\alpha_1 \alpha_T}{\alpha_{os}} V_{01}(z) + V_{N2}(z) ((K_2 - \alpha_s) (z^{0.65} - 1) + \alpha_d) \quad (A2.8)$$

To eliminate V_{01} from (A2.8), it is first obtained in terms of V_0 . We get, for the first stage

$$\frac{V_{01}(n+1) - V_{01}(n) + V_0(n+1) \alpha_1}{K_{11}} = 0$$

$$\therefore V_{01}(z) (z-1) = -V_0(z) \alpha_1 z, \quad V_{01}(z) = -V_0(z) \frac{\alpha_1 z}{z-1} \quad (A2.9)$$

Substituting (A2.9) in (A2.8) and rearranging

$$\begin{aligned} V_0(z) & \left\{ \left((1 + \alpha_3) \frac{\alpha_T}{\alpha_{os}} + 2ad + \frac{\alpha_1^2 T}{\alpha_{os}(z-1)} z - \left(\frac{\alpha_T}{\alpha_{os}} + ad \right) \right) \right. \\ & \left. = V_{N2}(z) \left((K_2 - \alpha_s) (z^{0.65} - 1) + ad \right) \right\} \end{aligned}$$

(A2.10)

From (A2.10) we get the second transfer function

$$\frac{V_0(z)}{V_{N2}(z)} = \frac{(z-1) \left((K_2 - \alpha_s) (z^{0.65} - 1) + ad \right)}{\left[\left((1 + \alpha_3) \frac{\alpha_T}{\alpha_{os}} + 2ad \right) (z-1) + \frac{\alpha_1^2 \alpha_T}{\alpha_{os}} \right] z - \left(\frac{\alpha_T}{\alpha_{os}} + 2d \right) (z-1)}$$

(A2.11)

APPENDIX 3

Derivation of the transfer function of the switched capacitor notch filter, in z domain.

Refer to Figure 4.9(a) and Section 4.6.

In Figure 4.9(a) the output of the first stage of the filter is denoted as V^* and the second stage output (filter output) is marked as V_o .

The difference equation of the first age is given by

$$(V^*(n) - V^*(n-1)) C_2 = -V_i(n) C_{R5} - V_o(n) C_{R2} \quad (A3.1)$$

Taking the z transform of (A3.1) gives

$$V^*(z) (1 - z^{-1}) C_2 = -V_i(z) C_{R5} - V_o(z) C_{R2} \quad (A3.2)$$

From (A3.2)

$$V^*(z) = - \frac{V_i(z) C_{R5}}{(1 - z^{-1}) C_2} - V_o(z) \frac{C_{R2}}{(1 - z^{-1}) C_2} \quad (A3.3)$$

Similarly taking the difference equation of the second stage we get

$$(V_o(n) - V_o(n-1)) C_1 = -V_o(n) C_{R3} + V^*(n-1) C_{R1} - (V_i(n) - V_i(n-1)) C_5$$

Corresponding z transform is

$$V_o(z) (1 - z^{-1}) C_1 = -V_o(z) C_{R3} + V^* z^{-1} C_{R1} - V_i(z) (1 - z^{-1}) C_5 \quad (A3.4)$$

Substituting for $V^*(z)$ in (A3.4),

$$V_o(z) (1 - z^{-1}) C_1 = -V_o(z) C_{R3} - V_i(z) \frac{C_{R5} C_{R1} z^{-1}}{(1 - z^{-1}) C_2} - V_o(z) \frac{C_{R2} C_{R1} z^{-1}}{(1 - z^{-1}) C_2} - V_i(z) (1 - z^{-1}) C_5$$

Separating $V_o(Z)$ and $V_i(Z)$ on either side of the equation yields

$$\begin{aligned} V_o(Z) [(1-Z^{-1})^2 C_1 C_2 + (1-Z^{-1}) C_2 C_{R3} + C_{R1} C_{R2} Z^{-1}] \\ = -V_i(Z) [(1-Z^{-1})^2 C_2 C_5 + C_{R1} C_{R5} Z^{-1}] \end{aligned}$$

Hence the transfer $H(Z)$ is given by

$$H(z) = \frac{V_o(z)}{V_i(z)} = \frac{C_2 C_5 + (C_{R1} C_{R5} - 2C_2 C_5) z^{-1} + C_2 C_5 z^{-2}}{C_1 C_2 + C_2 C_{R3} + (C_{R1} C_{R2} - C_2 C_{R3} - 2C_1 C_2) z^{-1} + C_1 C_2 z^{-2}} \quad (A3.5)$$

i.e.,

$$\frac{V_o(Z)}{V_i(Z)} = - \frac{C_5}{(C_1 + C_{R3})} \frac{1 + (\frac{C_{R1} C_{R5}}{C_2 C_5} - 2) z^{-1} + z^{-2}}{1 + [\frac{C_{R1} C_{R2} - C_2 (C_{R3} + 2C_1)}{C_2 (C_{R3} + C_1)}] z^{-1} + \frac{C_1}{C_1 + C_{R3}} z^{-2}}$$

or

$$H(Z) = - \frac{C_5}{(C_1 + C_{R3})} \frac{z^2 + (\frac{C_{R1} C_{R5}}{C_2 C_5} - 2) z + 1}{z^2 + (\frac{C_{R1} C_{R2}}{(C_1 + C_{R3}) C_2} - \frac{2C_1 + C_{R3}}{C_1 + C_{R3}}) z + \frac{C_1}{C_1 + C_{R3}}} \quad (A3.6)$$

APPENDIX 4

CALCULATION OF GAIN FROM SIMULATION

Refer to Section 3.5.1.

The table below shows the voltage levels at the output, gate of M1 and the virtual ground input (node V*) of Figure 3.9, as obtained from a transient analysis run of the dynamp. Voltage samples at the end of four consecutive ϕ_4 phases are shown in table. The simulation used 5 micron, minimum feature NMOS process, with Cgd assumed to be 0.01 pF.

Sample No. (n)	Virtual Ground Volts $V_I(n)$	Gate of M ₁ Volts $V_g(n)$	Output Volts $V_O(n)$	Gain wrt gate $\frac{V_O(n)-V_O(n-1)}{V_g(n)-V_g(n-1)}$	Gain wrt Virtual Ground $\frac{V_O(n)-V_O(n-1)}{V_I(n)-V_I(n-1)}$
1	-0.02425132	-6.958972	0.1221259		
2	-0.02438097	-6.958978	0.2677239	-22000	-1120
3	-0.02446100	-6.958984	0.4133705	-24270	-1820
4	-0.02452540	-6.958990	0.5680383	-25100	-2400

END

3 1 1 0 8 8 4

FIN