1 of/de 1

PM-1 3½"x4" PHOTOGRAPHIC MICROCOPY TARGET
NBS 1010a ANSI/ISO #2 EQUIVALENT

National Library
of Canada

Bibliothèque nationale
du Canada

Canadian Theses Service Service des thèses canadiennes

Ottawa, Canada
K1A 0N4

NOTICE

The quality of this microform is heavily dependent upon the quality of the original thesis submitted for microfilming. Every effort has been made to ensure the highest quality of reproduction possible.

If pages are missing, contact the university which granted the degree.

Some pages may have indistinct print especially if the original pages were typed with a poor typewriter ribbon or if the university sent us an inferior photocopy.

Reproduction in full or in part of this microform is governed by the Canadian Copyright Act, R.S.C. 1970, c. C-30, and subsequent amendments.

AVIS

La qualité de cette microforme dépend grandement de la qualité de la thèse soumise au microfilmage. Nous avons tout fait pour assurer une qualité supérieure de reproduction.

S'il manque des pages, veuillez communiquer avec l'université qui a conféré le grade.

La qualité d'impression de certaines pages peut laisser à désirer, surtout si les pages originales ont été dactylographiées à l'aide d'un ruban usé ou si l'université nous a fait parvenir une photocopie de qualité inférieure.

La reproduction, même partielle, de cette microforme est soumise à la Loi canadienne sur le droit d'auteur, SRC 1970, c. C-30, et ses amendements subséquents.

**INCORPORATION OF DIGITAL ANGLE-MODULATION INTO
A FRACTIONAL DIVISION SYNTHESIZER**

by

Adam Xuesi Dong

**A thesis submitted to the Faculty of Graduate Studies and Research
in partial fulfillment of the requirements for the degree of**

Master of Engineering

Ottawa-Carleton Institute for Electrical Engineering

Department of Electronics

Faculty of Engineering

Carleton University

Ottawa, Canada

April 1992

© copyright 1992, Adam X. Dong

National Library
of Canada

Bibliothèque nationale
du Canada

Canadian Theses Service Service des thèses canadiennes

Ottawa, Canada
K1A 0N4

The author has granted an irrevocable non-exclusive licence allowing the National Library of Canada to reproduce, loan, distribute or sell copies of his/her thesis by any means and in any form or format, making this thesis available to interested persons.

The author retains ownership of the copyright in his/her thesis. Neither the thesis nor substantial extracts from it may be printed or otherwise reproduced without his/her permission.

L'auteur a accordé une licence irrévocable et non exclusive permettant à la Bibliothèque nationale du Canada de reproduire, prêter, distribuer ou vendre des copies de sa thèse de quelque manière et sous quelque forme que ce soit pour mettre des exemplaires de cette thèse à la disposition des personnes intéressées.

L'auteur conserve la propriété du droit d'auteur qui protège sa thèse. Ni la thèse ni des extraits substantiels de celle-ci ne doivent être imprimés ou autrement reproduits sans son autorisation.

ISBN 0-315-75980-1

Canada

The undersigned recommend to the Faculty of Graduate Studies and
Research the acceptance of the thesis:

**"INCORPORATION OF DIGITAL-ANGLE MODULATION
INTO A FRACTIONAL DIVISION SYNTHESIZER"**

submitted by Adam Xuesi Dong in partial fulfillment of the requirements
for the degree of Master of Engineering.

Ted Kwasniewski

Prof. T. A. Kwasniewski

Thesis Supervisor

J. S. Wight

Prof. J. S. Wight

Chairman,

Department of Electronics

Carleton University

April 1992

ABSTRACT

This thesis studies the incorporation of digital angle modulation via high order Σ - Δ modulation into single loop indirect synthesis, which offers advantages over direct digital synthesis method in terms of compactness, power consumption, cost and compatibility for monolithic integration. The proposed scheme is validated by theoretical analysis and computer simulation. Further, a prototype system is designed and set up to demonstrate the feasibility. Experimental results including modulated signal spectra in frequency domain and eye diagrams in time domain are presented. The low-pass characteristic of the loop that affects the modulating signal is analytically predicted and experimentally verified.

ACKNOWLEDGEMENTS

I would like to extend my profound gratitude and appreciation to Dr. T. A. Kwasniewski for his patient supervision and invaluable encouragement. Also I would like to acknowledge the financial support of Carleton University and the equipment provision of the Telecommunications Research Institute of Ontario (TRIO). Finally, special thanks are due to T. Riley, T. Kenny and R. Shum for their kind help throughout the course of this work.

CONTENTS

1	Introduction.....	1
1.1	Thesis Motivation and Objectives	1
1.2	Thesis Outline	2
2	Frequency Synthesis and Digital Modulation	4
2.1	Introduction.....	4
2.2	Direct Analog Synthesis	4
2.3	Direct Digital Synthesis and Digital Modulation	5
2.3.1	Direct Digital Synthesis	5
2.3.2	Digital Modulation with Direct Digital Synthesis	7
2.4	Indirect Synthesis and Digital Modulation	8
2.4.1	Indirect Synthesis.....	8
2.4.2	Fractional Division Synthesis	10
2.4.3	Digital Modulation with Fractional Division Synthesis	13
2.5	Discussion	13
3	Σ-Δ Modulation - Generation of the Modulus Control Signal for Fractional Division Synthesis	16
3.1	Introduction.....	16
3.2	Principle	16

3.3 Higher Order Modulator Structures and Their Simulation	21
4 Digital FM and the Proposed Generation Scheme.....	30
4.1 Modulation Principle and Simulation	30
4.2 Modulator Structure.....	36
4.2.1 Indirect FM	36
4.2.2 Direct FM.....	38
4.2.2.1 Proposed FM Scheme	39
4.2.2.2 Low-Pass Characteristic of the PLL for the Modulating Signal in the Proposed Scheme.....	41
5 Experimental Verification of Incorporating Digital FM into a Fractional Division Synthesizer.....	46
5.1 Block Diagram.....	46
5.2 Detailed Description	46
5.2.1 ROM	46
5.2.2 Σ - Δ Modulator	48
5.2.3 Interfacing between Software and Hardware.....	51
5.2.4 PLL	51
5.3 System Integration and Results.....	57
5.3.1 Obtaining Single Tone by Bit-Stream Switching.....	57
5.3.2 FM by Bit-Stream Switching.....	58
5.3.3 Low-Pass Characteristic of the PLL for the Modulating Signal as Reflected in the Experiment.....	61

6	Conclusions.....	64
6.1	Summary	64
6.2	Suggestions for Future Research	65

LIST OF FIGURES

1.1	Block Diagram of a Digital Portable Transceiver	2
2.1	Example of a Direct Analog Synthesizer (DAS)	5
2.2	Basic Structure of a Direct Digital Synthesizer (DDS)	6
2.3	Digital Modulation with Direct Digital Synthesis	7
2.4	Basic Phase Locked Loop (PLL)	9
2.5	Divide-By-N Synthesizer	10
2.6	Fractional Division PLL Synthesizer	11
2.7	Bit Stream Generator	11
2.8	Digital Phase Accumulator (DPA) as the Bit Stream Generator	12
2.9	Digital Modulation with a Fractional Division Synthesizer	14
3.1	Discrete Model of a First Order Σ - Δ Modulator	17
3.2	Time Domain Simulation Result of the First Order Σ - Δ Modulator	17
3.3	Frequency Domain Simulation Result of the First Order Σ - Δ Modulator	18
3.4	Linearized Discrete Model of the First Order Σ - Δ Modulator	18
3.5	Δ Modulator	19
3.6	Modified Δ Modulator	20
3.7	First Order Σ - Δ Modulator	20
3.8	Nth Order Σ - Δ Modulator of the Ritchie Structure	23
3.9	Nth Order Σ - Δ Modulator of the Lee-Sodini Structure	23
3.10	A Second Order Ritchie Structure	24
3.11	A Third Order Ritchie Structure	24
3.12	A Third Order Lee-Sodini Structure	24

3.13	A Fourth Order Ritchie Structure	25
3.14	Simulation Result of the Second-Order Ritchie Structure	26
3.15	Simulation Result of the Third-Order Ritchie Structure	26
3.16	Simulation Result of the Third-Order Lee-Sodini Structure	27
3.17	Simulation Result of the Fourth-Order Ritchie Structure	27
3.18	Transfer Functions of the Third Order Lee-Sodini Structure	28
3.19	Output Spectrum within the Low Frequency Range When Input is 0.25	28
3.20	Output Spectrum within the Low Frequency Range When Input is 0	29
4.1	Baseband Waveform $b(t)$	32
4.2	Eye Diagram	32
4.3	Baseband Waveform Spectrum	33
4.4	A Segment of the Modulating Wave	34
4.5	Power Spectrum of the Modulating Wave $m(t)$	34
4.6	Frequency Modulated Signal Power Spectrum	35
4.7	Indirect Method of Generating an FM Signal	36
4.8	Narrow-Band Phase Modulator	37
4.9	A PLL Feedback Scheme for the Frequency Stabilization of a Direct Frequency Modulator	38
4.10	An Unconventional Direct FM Scheme	39
4.11	Equivalent of Figure 4.10	41
4.12	Equivalent of Figure 4.11	43
4.13	System Model for the Time-Variant Input only	
	(a) Time Domain Model	43
	(b) S-Domain Model	44
5.1	Block Diagram of a Synthesizer and Modulator Combined into one	47
5.2	Generation of the Modulating Waveform by ROM	48

5.3	The Third-Order Digital Σ - Δ Modulator	49
5.4	Simulated Spectrum of the Information Bearing Bit Stream	50
5.5	Interfacing between Software and Hardware	51
5.6	PLL Circuit Diagram	52
5.7	PLL Output Spectrum when the Divider is not Switched between its two Moduli	55
5.8	PLL Output Spectrum when the Divider is Switched (by Square Wave of Frequency $f_r/2$) Evenly between its two Moduli	56
5.9	PLL Output Spectrum when the Divider is Switched by the Bit-Stream Generated by the Σ - Δ Modulator of a DC Input of 0	58
5.10	PLL Output Spectrum when the Divider is Switched by the Bit-Stream Bearing Modulating Signal	59
5.11	A Measured Segment of the Modulating Wave	60
5.12	Measured Eye Diagram	60
5.13	PLL Output Spectrum when the Divider is Switched by the Bit-Stream Bearing Modulating Signal (Narrow Loop Bandwidth)	61
5.14	A Measured Segment of the Modulating Wave (Narrow Loop Bandwidth)	62
5.15	Measured Eye Diagram (Narrow Loop Bandwidth)	62

CHAPTER 1

INTRODUCTION

1.1 Thesis Motivation and Objectives

The purpose of any communication system is to convey a message from one point to another. Conventional static communication with designated source and sink locations is not suitable to the extensive mobility inherent in almost every aspect of modern life. In recent years, the availability of high quality mobile communication systems has proven to be invaluable in many facets of business and social life.

The use of mobile radios was originally confined to specialized users such as police departments, taxis and couriers. Now it is reaching the general public. Future integrated services digital networks (ISDN) will make possible immediate person-to-person communication and information resource access for anybody carrying a handheld terminal.

The successful deployment of mobile radio services to the general public depends on the availability of compact, inexpensive, low power consumption, integrated circuit devices. This thesis presents an effort to combine two modules of a cordless terminal into one for the above requirements.

An example block diagram of a digital portable transceiver [1] is shown in Figure 1.1. The transceiver provides duplexed communication of speech and data. It consists of two major functional units: a radio unit and a digital processing unit. The radio unit consists of a transmitter, receiver and frequency synthesizer. The digital processing unit consists of a speech codec, multiplexer/demultiplexer, scrambler/descrambler circuits and

Figure 1.1 Block Diagram of a Digital Portable Transceiver

microprocessor with memories.

This thesis is concerned with the frequency synthesizer and modulator (shaded boxes in Figure 1.1) in the digital portable transceiver radio unit. The focus of the research is to verify the idea of incorporating digital angle modulation into the frequency control of a single loop indirect synthesizer via a Σ - Δ modulator.

1.2 Thesis Outline

Chapter 2 reviews three types of frequency synthesizers and their extended ability for direct digital modulation. The idea of incorporating digital angle modulation into

fractional division synthesizer frequency control is developed at the end. Chapter 3 discusses Σ - Δ modulation which is to be utilized for generating a division control signal. Extensive simulation is performed to give some insight into the mechanism of this technique. An all-digital structure is selected for experimental investigation. Chapter 4 provides a theoretical foundation for the proposed scheme. The simulation and derivation serve as guidelines for the experiments presented in Chapter 5. A prototype system is designed and set up for feasibility study. The proposed scheme is successfully verified through the measurement results given in Chapter 5. Chapter 6 makes conclusions followed by suggestions for future research.

CHAPTER 2

FREQUENCY SYNTHESIS & DIGITAL MODULATION

2.1 Introduction

A frequency synthesizer is a device that generates useful frequencies from a stable reference source. Probably the greatest impetus to frequency synthesizer development has been the demand for communication capability within a limited spectrum. By providing accurate frequency control at reasonable costs, frequency synthesizers provide the maximum number of channels for an available total bandwidth and modulation technique.

In the past two decades, frequency synthesis has progressed from relatively crude “crystal bank” synthesizers to modern multiloop phase-locked systems. Contemporary frequency synthesis techniques can be broadly divided into three groups: direct analog synthesis (DAS), direct digital synthesis (DDS), and indirect synthesis (IS). This thesis is concerned with a type of IS which provides carrier frequencies for a mobile transceiver, and enables direct digital angle modulation. Here direct digital modulation means synthesized digital modulation, i.e., incorporating modulation into synthesizer frequency control.

2.2 Direct Analog Synthesis

In direct analog synthesis (DAS), the desired frequency is generated directly from the reference frequency using analog techniques such as mixing, filtering, division and switching. A typical direct analog synthesizer is shown in Figure 2.1 where

Figure 2.1 Example of a Direct Analog Synthesizer

$$f_{out} = f_3 \pm \frac{f_2}{N_2} \pm \frac{f_1}{N_1 \cdot N_2} .$$

High performance, in terms of acquisition time, resolution and operating speed can be achieved with DAS methods, but it could result in unreasonably high complexity circuits for frequency division, mixing, multiplication, switching and filtering. Another disadvantage of DAS is that spurious sidebands can be introduced by the use of non-linear elements [2]. While DAS can provide carrier frequency, it is irrelevant for direct digital modulation purposes.

2.3 Direct Digital Synthesis & Digital Modulation

2.3.1 Direct Digital Synthesis

In direct digital synthesis (DDS), the output waveform is directly synthesized digitally from the reference oscillator which is used as a clock for the digital operation.

Figure 2.2 Basic Structure of a Direct Digital Synthesizer

The basic structure of DDS is shown in Figure 2.2, although many variations exist [2]. At each clock cycle, the frequency control word that represents a phase increment is added to an accumulator whose content is proportional to the phase of the signal, and the accumulator value is passed to a read-only sine lookup table (ROM) whose output goes to a digital-to-analog converter (DAC). The phase accumulator is sometimes referred to as a numerically controlled oscillator (NCO) [3][4][5]. The ROM is actually a digital phase-to-amplitude converter. Its output drives the DAC to generate an analog representation of the sine waveform. In Figure 2.2, $f_{out} = \frac{P}{2^L} \cdot f_{clock}$. This basic structure suffers from the finite wordlength effect due to the truncation of the phase accumulator output.

DDS has the advantages of fast switching speed, fine frequency resolution ($\frac{f_{clock}}{2^L}$ in Figure 2.2) and phase continuous frequency hop. But one common feature of all DDS's is the requirement for a clock operating at a higher frequency than the synthesized frequency. Theoretically, this limitation is $f_{out} \leq 0.5f_{clock}$ according to Nyquist's theorem (in practice, $f_{out} \leq 0.4f_{clock}$) [6]. Another major concern for DDS is its spurious frequency performance [3][7].

2.3.2 Digital Modulation with Direct Digital Synthesis

With a modified NCO as the system core, digital modulation can be realized in Figure 2.3 as proposed by Digital RF Solution Corp [4][5]. The NCO allows easy

Figure 2.3 Digital Modulation with DDS

implementation of frequency, phase, and/or amplitude modulations. Combinations of these modulation techniques allow synthesis of nearly every kind of waveform because

AM can be simultaneously combined with FM and/or PM. All the parameters (amplitude, phase and frequency) of the generated signal are defined by digital numbers.

2.4 Indirect Synthesis and Digital Modulation

2.4.1. Indirect Synthesis

In indirect synthesis, typically a voltage-controlled oscillator (VCO), which is phase locked to the reference oscillator, is the source of the synthesizer output frequency.

Ideally, by controlling the input voltage of the VCO, any frequency within the VCO range can be obtained. However, due to the analog nature of the VCO, there is no certainty that the output frequency will not drift from the required value. To compensate for this potential drift, the VCO is usually controlled via a feedback loop system, i.e., phase-locked loop (PLL). So, an indirect synthesizer is also called a PLL synthesizer. Strictly speaking, such a system does not “synthesize” frequency, but derives the output frequency from a secondary oscillator that is phase-locked to the primary frequency reference.

A basic PLL as shown in Figure 2.4 consists of a phase detector, a low-pass filter and a VCO. The phase detector compares the VCO output to the reference signal, and generates a voltage proportional to the phase difference (phase error voltage). In addition, the phase comparator provides a frequency-tuning voltage. These voltages are passed through the low-pass filter for noise and high frequency component suppression, and then applied to the VCO. The polarity of the phase-error voltage is such that it will pull the VCO frequency in a direction to phase-track the reference frequency.

However, in this basic phase-locked loop the frequency range is limited by that of the reference source: to change the output frequency, the reference signal's frequency

Figure 2.4 Basic PLL

must be changed.

If a frequency divider is placed in the feedback path as in Figure 2.5, then $f_{VCO} = N \cdot f_{ref}$ when the loop is in lock. Thus, the use of a programmable divider allows a large number of frequencies, all multiples of f_{ref} , to be synthesized by changing the division ratio N .

However, the smallest achievable frequency step is limited to f_{ref} since N is assumed an integer here. In order to obtain fine frequency resolution, the reference frequency must be small. But small reference frequency results in many problems, among

Figure 2.5 Divide-By-N Synthesizer

which is the loop settling time. The loop settling time is inversely proportional to the reference frequency. The decrease of reference frequency means an increase of settling time. The switching speed of the synthesizer is therefore sacrificed. A frequently used rule

of thumb is that switching time $t_s = \frac{50}{f_{ref}}$ [8].

To resolve this contradiction, attention is turned to the division ratio N . If N could be assumed a fractional number, then fine frequency resolution could be achieved without lowering f_{ref} and sacrificing switching speed.

2.4.2 Fractional Division Synthesis

A variable modulus divider can be used for fractional division. In Figure 2.6, a

Figure 2.6 Fractional Division PLL Synthesizer

dual modulus divider replaces the programmable divider. It divides by N when the control input $b(t)$ is logic 0, divides by $N+1$ when $b(t)$ is logic 1¹. Now the problem is how to switch the dual modulus divider between the two division ratios N and $N+1$ in order to obtain an average division ratio $N.F$, where $0 \leq F = \overline{b(t)} \leq 1$ and $b(t) = 0, 1$. $\overline{(\cdot)}$ stands for the mean. The switching scheme is indeed a bit stream $b(t)$ generating scheme. The basic requirement of the bit stream generator is that its output density $\overline{b(t)}$ should reflect its

Figure 2.7 Bit Stream Generator

1. Just the opposite for some commercial dual modulus dividers. It is herein assumed only for the convenience of discussion.

input magnitude K as shown in Figure 2.7, where K is analog or multibit whereas $b(t)$ is one-bit.

The least sophisticated scheme is to use a digital phase accumulator (DPA), as in the basic structure of the direct digital synthesizer in Figure 2.2. But here $b(t)$ is the overflow signal rather than the phase register output itself. In Figure 2.8, $\overline{b(t)} = \frac{K}{2^L}$, i.e., the average overflow rate. When $b(t)$ is used to control the dual modulus divider, the average division ratio will be $N + \frac{K}{2^L}$. Here $F = \frac{K}{2^L}$. Thus, $f_{VCO} = (N.F)f_{ref}$ will be controlled by the number K .

However, things are never that easy. The bit stream $b(t)$ contains spurious components as well as the desired dc component for $\frac{K}{2^L}$ [9]. In fact, we can never have the

Figure 2.8 Digital Phase Accumulator (DPA) as a Bit Stream Generator

luxury of eliminating all the undesired spurs in the $b(t)$ spectrum. What we can do is one of the following: (1) to compensate at later stage - phase detector output, as in digiphase principle [10], but analog circuits have to be introduced; (2) to convert the spurs in $b(t)$ spectrum into white noise by adding random number to the input of DPA, as in Wheatley jitter injection scheme [11], but the noise floor is raised; (3) to randomize the spurs and push them to higher frequencies by using high order sigma-delta modulator instead of a DPA (a first order Σ - Δ modulator by itself) as the bit stream generator, as explicitly proposed in [12].

Comparatively, the last method is the most elegant solution which achieves good noise performance without resorting to analog circuits. Thus, it is suitable for digital implementation. The shaped noise in $b(t)$ will be greatly attenuated by the loop. It will be discussed later in more detail.

2.4.3 Digital Modulation with Fractional Division Synthesis

Since the bit stream generator input K decides the division ratio via $b(t)$, and hence controls the synthesizer output frequency $f_{VCO} = (N + \frac{K}{2^L})f_{ref}$, frequency modulation can be achieved as shown in Figure 2.9 by conveying a message through K . Then the closed-loop bandwidth has to be designed to let through the $K(t)$ spectrum within the low frequency range and not to let through the quantization noise in the higher frequency range. The principle expounded in this section will be the focus of the thesis.

2.5 Discussion

Three basic types of frequency synthesizers and some extensions have been reviewed above. In some instances, a hybrid produces a more favorable result, i.e., a

Figure 2.9 Digital Modulation with a Fractional Division Synthesizer

mixed system using two or more of the basic approaches, or a design adding circuits for more than basic frequency control. For example, a DDS-driven PLL is a powerful technique for the combination of the advantages of both types [13].

Quite often however, all requirements on performance and cost can be satisfied by one of the basic approaches and a monolithic design. For application in portable digital transceivers, a fractional division PLL synthesizer is a good choice. It allows monolithic design, small size and low power consumption, as well as high frequency and fine resolution.

For channelized communications, the main function of the frequency synthesizer

is to provide carrier frequencies. But with the recent advances in synthesizer techniques, the ability to fulfill modulation is also being considered in the synthesizer design. As briefly described in this chapter, direct digital synthesizers and PLL synthesizers are capable of direct digital modulation. But a direct digital synthesizer can only output frequencies lower than the operating clock frequency, and therefore is not suitable for GHz range application.

The succeeding chapters will concentrate on how to incorporate digital angle modulation into the frequency control of a PLL fractional division synthesizer which employs a high order $\Sigma\text{-}\Delta$ modulator as its bit stream generator.

Chapter 3

Σ - Δ Modulation - Generation of the Modulus Control Signal for Fractional Division Synthesis

3.1 Introduction

In section 2.4.2, a high order Σ - Δ modulator is chosen to generate a bit stream for divider modulus control in a PLL fractional division synthesizer. In retrospect, this is quite natural. As with its conventional application in oversampling A/D, a Σ - Δ modulator's output pulse density reflects its input amplitude. When used in a divider modulus control, that density corresponds to the average division ratio. So the input to the Σ - Δ modulator can control the average division ratio. That is exactly the job of the bit stream generator mentioned in section 2.4.2. Further a high order Σ - Δ modulator can shape the quantization noise, and the loop behaves very much like the decimation filter for oversampling A/D to greatly reduce the shaped noise. Thus the overall noise performance is enhanced without analog compensation.

3.2 Principle

A discrete model of first order Σ - Δ modulator is shown in Figure 3.1. The time domain result of simulation based on the model is shown in Figure 3.2. It can be seen that the binary output (± 1) density (output average value) corresponds to the input (sine wave)

Figure 3.1 Discrete Model of a First Order Σ - Δ Modulator

amplitude. The Σ - Δ modulator can also be viewed as pulse density modulation (PDM). This is an intuitive observation in time domain.

When a FFT is performed on the output, its spectrum in the frequency domain is obtained, as shown in Figure 3.3. The dominant spike is located at the sine wave input frequency. It is confirmed that the input (analog or multi-bit) spectrum is passed through the Σ - Δ modulator to the output (1-bit) spectrum. Also, it can be seen that quantization noise is introduced and shaped during the process.

Figure 3.2 Time Domain Simulation Result of the First Order Σ - Δ Modulator

Figure 3.3 Frequency Domain Simulation Result of the First Order Σ - Δ Modulator

A commonly used, although in some cases inaccurate, analysis is to assume that the nonlinear quantizer only introduces additive white noise which is uncorrelated to the input signal. Thus the discrete model in Figure 3.1 is modified as in Figure 3.4. This allows linear analysis to be used. The transfer functions for both the signal and noise can

Figure 3.4 Linearized Discrete Model of the First Order Σ - Δ Modulator

be derived:

$$H_{signal}(z) = \frac{\frac{1}{1-z^{-1}}}{1 + \frac{z^{-1}}{1-z^{-1}}} = 1 \quad (3.1)$$

and

$$H_{noise}(z) = \frac{1}{1 + \frac{z^{-1}}{1-z^{-1}}} = 1 - z^{-1} \quad (3.2)$$

For input signal, the first order Σ - Δ modulator is an all pass filter; For noise, it is a high pass filter. Thus, the modulator discriminates noise from signal. The noise contribution in the signal band is reduced. This effect is called noise shaping (shifting).

First order Σ - Δ modulation can also be appreciated from its origin. It is derived from two-level DPCM, or Δ modulation, as shown in Figure 3.5. The output of the integrator approximates the input signal. The 1-bit output of the quantizer reflects the differentiation (slope) of the input signal. By digitally integrating this one-bit output, the input signal can be reconstructed.

Although simpler than PCM, a Δ modulator is incapable of transmitting the dc component, its dynamic range and SNR are inversely proportional to the signal frequency

Figure 3.5 Δ Modulator

Figure 3.6 Modified Δ Modulator

and the inevitable integration at the receiving end causes an accumulative error when the system is subject to transmission disturbances.

Modification is made by adding a signal integration process at the input of the original Δ modulator as is shown in Figure 3.6. The structure can be further modified as in Figure 3.7. This results in the first order Σ - Δ modulator or modulator (the term modulator is preferred later on in this thesis because it is less misleading). The output pulse density corresponds to the input signal amplitude rather than slope due to the added integration.

The integrator in the forward path is not necessarily a single integrator but may be a double integrator or, more generally, any signal processing networks favorable to the

Figure 3.7 First Order Σ - Δ Modulator

system performance. This guideline leads to high order $\Sigma\Delta$ modulator structures with more favorable noise performance.

3.3 Higher Order Modulator Structures and Their Simulation

Higher order $\Sigma\Delta$ modulators provide high precision conversion not by decreasing error between the analog (or multi-bit) input and the 1-bit (or low-bit) digital output, but by making the error occur more often. In this way the error spectrum extends beyond the pass-band of interest. Although the output total noise power is high, the in-band noise power is low.

For a 1-bit $\Sigma\Delta$ modulator, there are the Ritchie structure and the Lee-Sodini structure [14], as shown in Figure 3.8 and Figure 3.9, respectively. Several particular 1-bit $\Sigma\Delta$ modulators are examined here, including a second order Ritchie structure shown in Figure 3.10, a third order Ritchie structure [15] in Figure 3.11, a third order Lee-Sodini structure [12] in Figure 3.12 and a fourth order Ritchie structure [16] in Figure 3.13.

Simulation is performed with MATLAB. The input is a sine wave of frequency $\frac{5}{2^{11}}f_s$ (f_s is sampling frequency) and amplitude of half full scale. A 2^{14} points FFT is performed, and in the computation, a Blackman window is used. Simulation results of the above structures under the same conditions are shown in Figure 3.14-17 (compare with Figure 3.3).

The third order Lee-Sodini structure is selected for the work of this thesis, because it gives good noise shaping and at the same time is suitable for digital implementation.

Using quasi-linear analysis, as mentioned in Section 3.2, one can derive its transfer functions:

$$H_{signal}(z) = \frac{8z^{-2} - 12z^{-3} + 5z^{-4}}{1 - 3z^{-1} + 11z^{-2} - 13z^{-3} + 5z^{-4}} \quad (3.3)$$

and

$$H_{noise}(z) = \frac{z^{-1} - 3z^{-2} + 3z^{-3} - z^{-4}}{1 - 3z^{-1} + 11z^{-2} - 13z^{-3} + 5z^{-4}} \quad (3.4)$$

They are plotted in Figure 3.18 to show the all pass characteristics for input signal and the high pass characteristics for quantization noise with a slope of 60dB per decade in the low frequency range.

Now let the input signal be a constant, dc or 0, and perform the simulation. Figure 3.19 and 3.20 show the results when the inputs are 1/4 and 0, respectively. The FFT point is 2^{17} for getting more detail of low frequency range near dc. Those little periodic spurs result from the finite sequence length effect.

Figure 3.8 Nth Order $\Sigma\text{-}\Delta$ Modulator of the Ritchie Structure

Figure 3.9 Nth Order $\Sigma\text{-}\Delta$ Modulator of the Lee-Sodini Structure

Figure 3.10 A Second Order Ritchie Structure

Figure 3.11 A Third Order Ritchie Structure

Figure 3.12 A Third Order Lee-Sodini Structure

Figure 3.13 A Fourth Order Ritchie Structure

Figure 3.14 Simulation Result of the Second-Order Ritchie Structure

Figure 3.15 Simulation Result of the Third-Order Ritchie Structure

Figure 3.16 Simulation Result of the Third-Order Lee-Sodini Structure

Figure 3.17 Simulation Result of the Fourth-Order Ritchie Structure

Figure 3.18 Transfer Functions of the Third Order Lee-Sodini Structure

Figure 3.19 Output Spectrum within the Low Frequency Range when Input is 0.25

Figure 3.20 Output Spectrum within the Low Frequency Range when Input is 0

CHAPTER 4

DIGITAL FM AND THE PROPOSED GENERATION SCHEME

4.1 Modulation Principle and Simulation

The basic expression of a digital frequency modulated signal is:

$$\begin{aligned} s(t) &= \cos(\omega_c t + \varphi(t)) \\ &= \cos\left(2\pi f_c t + 2\pi f_d \int_{-\infty}^t m(\tau) d\tau\right) \\ &= \cos\left(2\pi f_c t + 2\pi f_d \int_{-\infty}^t \sum_i a_i b(\tau - iT) d\tau\right) \end{aligned} \quad (4.1)$$

where f_c is the carrier frequency;

$\varphi(t)$ is the continuous phase function bearing the transmitted information;

f_d is the peak frequency deviation;

a_i represents a series of binary symbols bearing information, here $a_i = \pm 1$ is assumed

and each symbol being transmitted during T , bit rate $R = \frac{1}{T}$;

$b(t)$ is the baseband waveform;

$m(t) = \sum_i a_i b(t - iT)$ is the baseband modulating signal (wave);

$f_s(t) = f_c + f_d m(t) = f_c + f_d \sum_i a_i b(t - iT)$ is the instantaneous frequency.

$b(t)$ and f_d together determine both the spectrum of $s(t)$ in frequency domain and the eye diagram¹ of $f_s(t)$ in time domain.

The spectrum of $s(t)$ is of more interest on the transmitting side, and it should be narrow enough so that most of its power is confined in the designated channel. In other words, the bandwidth of $s(t) < \text{channel spacing}$. According to the generalized Carson's rule, $B_s \approx 2(B_b + f_d)$, where B_s stands for the bandwidth of $s(t)$ and B_b for the one-sided bandwidth of the baseband waveform $b(t)$. Note that the bandwidth of $s(t)$ is not just its instantaneous frequency deviation peak-to-peak value $2f_d$, but also is dependent on the baseband waveform bandwidth B_b . Usually, $\beta = \frac{f_d}{B_b}$ is referred to as the modulation index (or, deviation ratio). Thus, $B_s \approx 2B_b(1 + \beta)$.

The eye pattern of $f_s(t)$ is of more interest on the receiver side. It should be open enough for binary sign detection, and its zero crossing dispersion should be small enough for bit synchronization. In some cases, equalization is employed to counter intersymbol interference (ISI) and to achieve a better eye diagram.

For the feasibility study of the modulator configuration proposed in this thesis, a baseband waveform without introducing intersymbol interference at center and zero crossing is chosen (see Figure 4.1 and 4.2):

$$b(t) = \begin{cases} \frac{\sin \frac{\pi}{T}(t-0.5T)}{\frac{\pi}{T}(t-0.5T)} \cdot \frac{1 + \cos \frac{2\pi}{3T}(t-0.5T)}{2} & , -T \leq t \leq 2T \\ 0 & , \text{others} \end{cases} \quad (4.2)$$

1. In practice, an eye diagram is obtained by visualizing through an oscilloscope the demodulated binary message, with the horizontal sweep synchronized by bit rate.

Figure 4.1 Baseband Waveform $b(t)$

Figure 4.2 Eye Diagram

It is a 3-bit period raised-cosine function weighted by a $\sin(x)/x$ function. Later on it will be called WRC3. Or, to look at it in another way, it is a $\sin(x)/x$ function truncated by a 3-bit period raised-cosine function. Ideally, to make the spectrum compact, only a $\sin(x)/x$ function should be used to get a square shape spectrum. But a $\sin(x)/x$ function has a slow decaying tail, introducing too much ISI at zero crossing, not to mention the physical implementation problems. Consequently, it is here truncated by a 3-bit period raised-cosine function.

Once the proposed modulator has been proved to work well with WRC3, it will then work well with other baseband waveforms to produce any kind of digital FM signal including TFM and GMSK [17][18][19][20] signals, due to its unique configuration that is detailed in the next chapter.

Figure 4.3 Baseband Waveform Spectrum

Figure 4.4 A Segment of the Modulating Wave

The power spectrum of $b(t)$, obtained by performing a FFT, is shown in Figure 4.3.

Suppose binary message series a_i 's are uncorrelated to each other. A 2^{11} -bit pseudo-

Figure 4.5 Power Spectrum of the Modulating Wave $m(t)$

random series produced by a "rand" function in MATLAB is used for a_i 's. Next, a 2^{11} -bit period message wave $m(t) = \sum_i a_i b(t - iT)$ is generated, a segment of which is shown in Figure 4.4. Its power spectrum, obtained by performing a FFT, is shown in Figure 4.5. This spectrum is essentially the baseband waveform spectrum, imposed by $\frac{\sin(\pi f 3T)}{\pi f 3T}$, heritable from $b(t)$, and by $\frac{\sin(\pi f T)}{\pi f T}$, for a_i 's. This graph will be useful later in Section 5.2.2 of the next chapter.

Insert the above $m(t)$ into the expression of $s(t)$, and let $f_d = 6\text{KHz}$, then $s(t)$ can be simulated and its power spectrum calculated and plotted as shown in Figure 4.6. This

Figure 4.6 Frequency Modulated Signal Power Spectrum

graph is important in that it predicts the RF signal spectrum shape and serves as the reference for experimental results.

4.2 Modulator Structure

There are two basic methods of generating frequency modulated signals, namely, indirect FM and direct FM. In the indirect method of producing frequency modulation, the modulating wave is first used to produce a narrow-band FM, and frequency multiplication is next used to increase the frequency deviation to the desired level. On the other hand, in the direct method of producing frequency modulation the carrier frequency is directly varied in accordance with the input baseband signal.

4.2.1 Indirect FM

A simple block diagram of an indirect FM system is shown in Figure 4.7. The baseband modulating wave $m(t)$ is first integrated and then used to phase-modulate a

Figure 4.7 Indirect Method of Generating an FM Signal

Figure 4.8 Narrow-Band Phase Modulator

crystal-controlled oscillator. In order to minimize the distortion inherent in the phase modulator, the maximum phase deviation is kept small, i.e., $|\phi(t)|_{\max} \ll 1$ radian, thereby resulting in a narrow-band FM wave. This signal is then multiplied in frequency by means of a frequency multiplier in order to produce the desired wide-band FM wave. Limitations to frequency multiplication include the fact that losses incurred in the harmonic generation require additional amplification and small phase instabilities in the multiplication process accumulate and appear as noise in the output. For the implementation of the narrow-band phase modulator, see Figure 4.8. The structure is based on the following derivation:

$$s(t) = \cos(\omega_c t + \phi(t)) = \cos(\omega_c t) \cos(\phi(t)) - \sin(\omega_c t) \sin(\phi(t)) \quad (4.3)$$

For narrow-band phase modulation, $|\phi(t)|_{\max} \ll 1$ radian, $\cos(\phi(t)) \approx 1$, and $\sin(\phi(t)) \approx \phi(t)$. The above equation can be simplified as:

$$s(t) \approx \cos(\omega_c t) - \phi(t) \sin(\omega_c t) \quad (4.4)$$

This equation is the basis of the block diagram in Figure 4.8. The (indirect) FM system was first introduced by E. H. Armstrong in 1936 and recognized as the crucial technology

breakthrough for mobile radio transmission because of its much better noise and fading immunity in comparison to the AM system.

4.2.2 Direct FM

In a direct FM system, the instantaneous frequency of the carrier wave is varied directly in accordance with the baseband modulating signal, typically by means of a VCO. An attempt is usually made to generate as wide a frequency deviation as possible and thus these systems often require a lower frequency multiplication factor, if any, than those using the indirect method. On the other hand, because the frequency is not obtained from a highly stable oscillator and is controlled by the modulating voltage, the long-term frequency stability is not as good as the crystal-stabilized oscillators generally used in the indirect method. Thus the direct FM methods usually employ some auxiliary methods for frequency stabilization.

A PLL, as shown in Figure 4.9, is considered for this purpose [21]. However, the problem of this scheme is that the loop acts like a high-pass filter on the modulating signal

Figure 4.9 A PLL Feedback Scheme for the Frequency Stabilization of a Direct Frequency Modulator

which is applied to the control input of the VCO. Therefore the modulating signal in low-frequency range cannot be adequately transmitted.

4.2.2.1 Proposed FM Scheme

The scheme that is being studied in this thesis (first mentioned in Section 2.4.3) is aimed at circumventing this problem. It is shown in Figure 4.10. In this structure, the loop acts like a low pass filter on the modulating signal (detailed in the next section). The Σ - Δ modulator is employed to convert the analog or multibit modulating signal $m(t)$ into a one-bit signal $d(t)$ with a certain oversampling ratio. The one-bit signal $d(t)$ that bears the $m(t)$ spectrum is to switch the dual modulus divider in the PLL and hence modulate the output frequency. Therefore, a stabilized FM is elegantly achieved through its incorporation into

Figure 4.10 An Unconventional Direct FM Scheme

fractional division synthesizer frequency control.

The scheme also has several other important potentials and advantages:

1. By employing a ROM to store the baseband waveform (preceding the Σ - Δ modulator) instead of utilizing a dedicated digital or analog filter to generate the baseband waveform (and maybe another filter for anti-aliasing), this digital frequency modulator (ready to become a binary phase modulator) can flexibly produce any kind of FM signal with one baseband waveform or another easily changed and stored in the ROM.
2. By inputting another quantity, C_s , to the Σ - Δ modulator for channel selection (see Figure 4.10), this FM modulator can switch between channels within a certain frequency range (theoretically, $Nf_r \sim (N+1)f_r$. For example, if $f_r=20\text{MHz}$ and $N=40$, then the range is $800\text{MHz} \sim 820\text{MHz}$). Furthermore, it is a promising candidate for a direct sequence or frequency hopped spread spectrum signal generator of compact size and low power consumption. Settling time will be a big concern in that application.
3. This frequency modulator is designed not to be followed by a frequency multiplier. The experiment to be presented in the next chapter verifies that with the 3rd order Σ - Δ modulator and a reference frequency of 3.2768MHz , the scheme works quite well for a 16kbps data rate which is *ISDN* D channel standard. It is anticipated that with a higher reference frequency and/or higher order Σ - Δ modulator, the system could well accept an *ISDN* B channel data rate 64kbps .
4. This frequency modulator is designed not to require frequency up-conversion because the PLL operating frequency can be in the GHz range, although in the following experiment of feasibility, the PLL operates in the VHF band. But without IF filtering, spurious performance might be a concern.

Another quite different way of generating direct FM is already introduced in Section 2.3.2 - the totally digital method. Wideband FM can be generated this way. But the

digitally synthesized frequency is surely lower than the operation clock frequency. That is the weakness of this method if up-conversion is not to be used.

4.2.2.2 Low-Pass Characteristic of the PLL for the Modulating Signal in the Proposed Scheme

Figure 4.10 can be redrawn as Figure 4.11. When $d(t)=0$, the divider divides by N . When $d(t)=1$, the divider divides by $N+1$. Therefore, during each sampling (reference) period the division ratio is indeed $N+d(t)$. $d(t)$ can be dissolved into two terms: d_0 for its dc component and $\tilde{d}(t)$ for its ac component, i.e.,

$$d(t)=d_0+\tilde{d}(t) \quad (4.5)$$

d_0 corresponds to the channel selection word C_s , $d_0 \propto C_s$, and $\tilde{d}(t)$ reflects the modulating signal $m(t)$ plus shaped quantization noise $q(t)$, $\tilde{d}(t) \propto m(t) + q(t)$. If the PLL behaves like a low-pass filter to $\tilde{d}(t)$, then equivalently it behaves like a low-pass filter to the modulating signal $m(t)$ and quantization noise $q(t)$.

Figure 4.11 Equivalent of Figure 4.10

The division ratio can be written as

$$N + d(t) = N + d_o + \bar{d}(t) = (N + d_o) \left(1 + \frac{\bar{d}(t)}{N + d_o} \right) \quad (4.6)$$

Let

$$x(t) = \frac{\bar{d}(t)}{N + d_o} \quad (4.7)$$

then

$$\frac{1}{N + d(t)} = \frac{1}{N + d_o} \frac{1}{1 + x(t)} \quad (4.8)$$

Because $d(t)$ can only be 0 or 1,

$$0 < d_o < 1 \text{ and } |\bar{d}(t)| = \frac{1}{2} \quad (4.9)$$

It follows that

$$|x(t)| = \left| \frac{\bar{d}(t)}{N + d_o} \right| < \frac{1}{2N} \ll 1 \quad (4.10)$$

For example, in the experiment described in the next chapter, $N=20$, $|x(t)| < 0.025 \ll 1$.

Furthermore,

$$\frac{1}{1 + x(t)} = 1 - x(t) + x^2(t) - x^3(t) + \dots = 1 - y(t) \quad (4.11)$$

It is defined that

$$y(t) = x(t) - x^2(t) + x^3(t) - x^4(t) + \dots \quad (4.12)$$

Therefore,

$$\frac{1}{N + d(t)} = \frac{1}{N + d_o} (1 - y(t)) = \frac{1}{N + d_o} - \frac{y(t)}{N + d_o} \quad (4.13)$$

Now Figure 4.11 can be redrawn accordingly as Figure 4.12. The divider block becomes two.

Figure 4.12 Equivalent of Figure 4.11

At this stage, another approximation is to be made: regard the input to the lower block of the divider as though only the upper block exists. Then this input is constant $(N+d_o)f_r$. This approximation is reasonable because it only disregards second and higher order nonlinear effects of the small valued, time variant $x(t)$ (note that $x(t) < \frac{1}{2N} \ll 1$ as reasoned above).

Now the system models for only $y(t)$ as input are given in Figure 4.13(a) and (b) where K_ϕ is phase detector gain factor, $L(s)$ is loop filter transfer function, and K_v is VCO gain factor. The transfer function for $y(t)$ can be derived as

$$\frac{F_o(s)}{Y(s)} = \frac{K_\phi L(s) K_v}{s(N+d_o) + K_\phi L(s) K_v} (N+d_o) f_r \quad (4.14)$$

Since $y(t) = x(t) - x^2(t) + x^3(t) - x^4(t) + \dots \approx x(t) = \frac{\tilde{d}(t)}{N+d_o} \propto m(t) + q(t)$, the conclusion follows that for the divider modulus control input, i.e., the modulating signal plus the quantization noise, the PLL is equivalent to a low-pass filter of the same transfer

(a) Time Domain Model

(b) S-Domain Model

Figure 4.13 System Model for the Time-Variant Input only

function as the conventional close-loop transfer function for reference input, but with second order approximation. Further, the approximation condition suggests that the bigger

the basic division ratio is, the more the PLL acts like a linear low-pass filter on the modulating signal, as well as on the quantization noise. With respect to the modulating signal, the loop bandwidth should be as wide as possible to pass the low frequency range signal without significantly affecting it. But for the high-pass shaped (by the Σ - Δ modulator) quantization noise, the loop should have a narrow bandwidth to cut off the noise as much as possible. In the implementation of the system, a compromise has to be made. A higher reference frequency and/or higher order Σ - Δ modulator can ease the contradiction with the quantization noise being pushed even further away from the signal pass-band.

CHAPTER 5

EXPERIMENTAL VERIFICATION OF INCORPORATING DIGITAL FM INTO A FRACTIONAL DIVISION SYNTHESIZER

5.1 Block Diagram

To verify the idea of incorporating digital angle modulation into the frequency control of a fractional division synthesizer, a prototype system is built for a feasibility study. Its block diagram is shown in Figure 5.1. The system has three inputs: binary data in, channel selection command and reference frequency; and one output: angle modulated RF signal. For the purpose of this thesis, the PLL part is realized in hardware, and the information-bearing bit-stream generation part is realized in software.

5.2 Detailed Description

5.2.1 ROM

In the case of binary digital modulation where the incoming message consists of a series of binary symbols, pulse shaping (i.e., embodying each bit into certain base-band waveform) is necessary before modulation. Conventionally, this is done with an actual filter. But in the proposed system, ROM is used instead to store the baseband waveform, resulting in more flexibility for the implementation of various FM schemes.

Figure 5.1 Block Diagram of a Synthesizer and Modulator Combined into One

In fact, the ROM in the above block diagram needs some peripheral logic circuits for addressing. A more detailed diagram for this is shown in Figure 5.2.

Because the chosen baseband waveform extends for 3 bit-periods, a 3-stage serial-to-parallel shift register is necessary. Accordingly, $2^3 = 8$ modulation law waveforms as shown in Figure 4.2 eye diagram are stored in the ROM. Less storage may be achieved

Figure 5.2 Generation of the Modulating Waveform by ROM

through intelligent design due to the symmetric characteristics of modulation law waveforms. The sampling frequency is the reference frequency f_r , as used in the PLL. The oversampling ratio is $\frac{f_r}{R}$, where R is the bit rate of binary data. If $2^{k-1} < \frac{f_r}{R} \leq 2^k$, then ROM is addressed by $k+3$ bits. The r -bit output of the ROM goes to the Σ - Δ modulator input. In the software implementation of this building block, floating-point numbers are used.

Thus, this building block accepts a binary data at bit rate R and outputs a r -bit digital signal at the sampling frequency f_r . The information-bearing output will go through the Σ - Δ modulator to the PLL to modulate the RF signal frequency.

5.2.2 Σ - Δ Modulator

The third order digital Σ - Δ modulator shown in Figure 3.12 has been selected for our system, and its transfer function has been plotted in Figure 3.18. In our system, the input to the Σ - Δ modulator comes from the r -bit output of the ROM, and the output of the

Figure 5.3 The Third-Order Digital Σ - Δ Modulator

Σ - Δ modulator is a binary signal which reflects the input, but with shaped quantization noise. The modulator is redrawn in Figure 5.3, where $M < 2^r$. Again, in the software implementation of this block, floating-point numbers are used.

Now a simulation is performed by feeding the modulating wave shown in Figure 4.4 into the Σ - Δ modulator. The purpose of this simulation is to see if the output spectrum has the same shape within the signal pass-band as the input spectrum. First the amplitude of the input for real operation have to be determined. Ideally (i.e., disregarding the PLL filter effect and quantization noise), VCO output frequency is

$$f_o(t) = (N + \overline{d(t)})f_r = \left(N + \frac{1 + \overline{out(t)}}{2}\right)f_r = \left(N + \frac{1 + \frac{in(t)}{M}}{2}\right)f_r \quad (5.1)$$

where $\overline{(\cdot)}$ stands for the useful signal contained in the low frequency range, and $in(t) = C_s + i\tilde{n}(t)$ (i.e., channel selection word (dc component) + modulation term (ac component)), which are the quantities to be determined in terms of the modulation requirement. Now $f_o(t)$ can be further expressed as

$$f_o(t) = (N + \frac{1}{2} + \frac{C_s}{2M})f_r + \frac{i\tilde{n}(t)}{2M}f_r \quad (5.2)$$

But in Section 4.1, it is required that

$$f_o(t) = f_c + f_d m(t) \quad (5.3)$$

Apparently, the carrier frequency

$$f_c = (N + \frac{1}{2} + \frac{C_s}{2M})f_r \quad (5.4)$$

and

$$f_d m(t) = \frac{i\tilde{n}(t)}{2M}f_r \quad (5.5)$$

Now the actual input of the Σ - Δ modulator can be determined by stating that

$$in(t) = C_s + i\tilde{n}(t) \quad (5.6)$$

with

$$C_s = 2M \left(\frac{f_c}{f_r} - N - \frac{1}{2} \right) \quad (5.7)$$

and

$$i\tilde{n}(t) = 2M \frac{f_d}{f_r} m(t) \quad (5.8)$$

Figure 5.4 Simulated Spectrum of the Information Bearing Bit Stream

If $C_s = 0$, i.e., $f_c = (N + \frac{1}{2})f_r$, and $f_d = 6kHz$, and oversampling ratio $\frac{f_r}{R} = 204.8$, then the output spectrum can be obtained by simulation as shown in Figure 5.4. The input spectrum is shown in Figure 4.5 of the last chapter. Comparing the input spectrum with the output spectrum, one can observe that the main lobe, within the frequency of about one bit-rate, is relatively uncontaminated by the quantization noise.

5.2.3 Interfacing between Software and Hardware

The above two building blocks are realized in software. A program written in Turbo Pascal simulates the ROM and the Σ - Δ modulator, storing the binary output in a data file. A second program downloads the contents of the data file to a PC plug-in card¹. The card can store 2^{20} bits and output them as desired to the hardware. When outputting, the card is clocked by the divider output. The outputted bit-stream will control the hardware divider division ratio. This is shown in Figure 5.5.

Figure 5.5 Interfacing between Software and Hardware

5.2.4 PLL

A PLL hardware is built with commercially available components. Its circuit

1. The card is made in ETC room in Carleton University under the order of TRIO group of Electronics Department.

diagram is shown in Figure 5.6.

The high performance Z-COMM VCO L-100 has a tuning voltage range 0 - 12V, tuning frequency range 50 - 95 MHz, tuning sensitivity 3 - 5 MHz/V (measured value is $K_v \approx 6.5 \text{ MHz/V}$ for 60 - 70 MHz output), and phase noise -110 dBc/Hz at 10 KHz offset according to its specifications. The 10 dB resistive pad and the buffer amplifier MAV-11 followed by the power splitter are for VCO output matching.

The control input and the output of the 225 MHz $\div 20/21$ two modulus divider are both CMOS/TTL compatible. While the control input is low, the division ratio is 21. While the control input high, the division ratio is 20. In practice, set up time and release time of the control input relative to the clock input should be checked to ensure correct operation.

Here, only phase detector #1 in the well known phase/frequency detector 4044 is used. This sequential phase detector may phase-lock within a relatively wide phase window of -2π to $+2\pi$. It accepts TTL waveforms at its inputs. With a +5V power supply voltage, its output levels are low of 0V and high of +4V. Consequently, the phase detector gain factor is $K_\phi = \frac{4}{2\pi} \text{ V/rad}$.

Fundamental loop characteristics such as loop bandwidth and transient response are controlled primarily by the loop filter. As seen in the circuit diagram, an active lead-lag filter is employed as the loop filter. It essentially consists of R_1 , R_2 , C , and OP37. Its transfer function is

$$L(s) = \frac{1 + sR_2C}{sR_1C} \quad (5.9)$$

If we let $\tau_1 = R_1C$ and $\tau_2 = R_2C$, then

$$L(s) = \frac{1 + s\tau_2}{s\tau_1} \quad (5.10)$$

The capacitor C_c 's in Figure 5.6 are for flattening pulses and suppressing higher frequency transient overshoot, but at the same time the pole introduced by C_c should not

Figure 5.6 PLL Circuit Diagram

be too close to the loop natural frequency ω_n (loop bandwidth) in order to avoid further overshoot of lower frequencies around ω_n . Taking C_c into account, one can obtain

$$L(s) = \frac{1 + sR_2C}{sR_1C(1 + s\frac{R_1C_c}{4})} \quad (5.11)$$

If the added pole is five times ω_n , then $\frac{4}{R_1C_c} = 5\omega_n$, or,

$$C_c = \frac{0.8}{R_1C} \quad (5.12)$$

The other branch at the inverting input of the op amp is for phase offset adjustment in order to avoid the dead zone of the phase detector.

Ignoring C_c , one can get the close loop transfer function (of the output phase or frequency vs. the reference input phase or frequency)

$$H(s) = \frac{K_\phi K_L L(s) \frac{K_V}{s}}{1 + K_\phi K_L L(s) \frac{K_V}{sN}} \quad (5.13)$$

K_L is for the variable resistor R_L (see Figure 5.6). Division ratio N is assumed. Now let

$K = K_\phi K_L K_V$ and insert $L(s) = \frac{1 + s\tau_2}{s\tau_1}$, one can get

$$H(s) = \frac{N(1 + s\tau_2)}{\frac{s^2}{\omega_n^2} + \frac{2\zeta s}{\omega_n} + 1} \quad (5.14)$$

So this second order PLL has a loop bandwidth or natural frequency being

$$\omega_n = \sqrt{\frac{K}{N\tau_1}} \quad (5.15)$$

and damping factor being

$$\zeta = \frac{\tau_2}{2}\omega_n = \frac{\tau_2}{2}\sqrt{\frac{K}{N\tau_1}} \quad (5.16)$$

Figure 5.7 PLL Output Spectrum when the Divider is not Switched between its two Moduli

and DC gain being N as expected ($f_o = Nf_r$).

Figure 5.7 gives the measured PLL output spectrum as shown on a Network/Spectrum Analyzer HP4195A when the divider division ratio is fixed at 20, reference frequency f_r is 3.2768 MHz provided by a Synthesized Signal Generator HP8663A, and approximate loop parameters are $f_n = \frac{\omega_n}{2\pi} \approx 20\text{KHz}$ and $\zeta \approx 0.81$ ($R_1 = R_2 = 4.7\text{K}\Omega$, $C = 2.7\text{nF}$, $K_L = 0.16$). The output frequency is $20f_r$. At 80KHz (5 times 16 KHz which is the bit rate to be used later) away from the carrier, the noise floor is about -85dB lower with the resolution bandwidth of 100Hz.

Figure 5.8 PLL Output Spectrum when the Divider is Switched (by Square Wave of Frequency $f_r/2$) Evenly between its two Moduli

Figure 5.8 shows the measured PLL output spectrum when the divider is switched between its two modulus by a square wave of half reference frequency. The measurement conditions are about the same as above (henceforth, they are always the same unless otherwise stated). The output frequency is $20.5f_r$. Later, modulation will be done around this frequency. The noise floor in Figure 5.8 is about the same as in Figure 5.7.

Noise mainly emanates from the noise within the VCO itself and the reference frequency's spurious component feedthrough. The PLL acts like a high-pass filter on VCO noise. The transfer function can be derived as $H_e(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$. On the other

hand, the PLL acts like a low pass filter on reference input noise. The transfer function has

been derived above as $H(s) = \frac{N\omega_n^2(1+s\tau_2)}{s^2 + 2\zeta\omega_n s + \omega_n^2}$. Thus, there is trade-off for the choice

of natural frequency. To complicate matters further in the next section, the quantization noise contained in the modulus-control bit-stream will make another contribution to the output noise. The PLL acts like a low-pass filter on this quantization noise, as explained in Section 4.2.2.2.

Improving the PLL quality and raising its operation frequency are not the main tasks of this experiment. Rather, this experiment is aimed at an in-depth investigation on how to incorporate digital FM into the PLL synthesizer frequency control process by means of a digital Σ - Δ modulator.

5.3 System Integration and Results

Now the software sector and the hardware sector are connected together via the card that is mentioned in Section 5.2.3, after it has been verified that each sector is working satisfactorily.

5.3.1 Obtaining Single Tone by Bit-Stream Switching

This time the dual modulus divider is controlled by the bit-stream generated by the software Σ - Δ modulator. But for now the input to the Σ - Δ modulator is constant (channel selection word). Therefore, a single tone output (carrier) is expected. However, the quantization noise, which is first high-pass shaped by the Σ - Δ modulator and then low-pass filtered by the PLL, will be present at the output spectrum beside the VCO noise and reference input noise.

Figure 5.9 PLL Output Spectrum when the Divider is Switched by the Bit-Stream Generated by the Σ - Δ Modulator of a DC Input of 0

Figure 5.9 gives the PLL output power spectrum when the Σ - Δ modulator input is 0 (those little spurs in the graph could be traced back to Figure 3.20). It can be seen that the noise floor over 20KHz away from the carrier frequency ($20.5f_r$) is raised by the quantization noise to -70dB (with the resolution bandwidth of 100Hz) relative to the carrier in comparison to Figure 5.8 where quantization noise is not present. This demonstrates that the idea of using a Σ - Δ modulator to generate the modulus-control bit-stream for the PLL synthesizer is successful. However, if further noise suppression is desired, then a higher reference frequency and/or a Σ - Δ modulator of higher order should be used.

5.3.2 FM by Bit-Stream Switching

Finally, the modulation term is added to the input of the Σ - Δ modulator. Thus, the generated bit-stream bears the modulating signal. When the dual modulus divider is controlled (switched) by this bit-stream, the PLL output is expected to be a frequency modulated signal. The measured output power spectrum is shown in Figure 5.10.

Comparing this experimentally obtained power spectrum with the simulated power spectrum shown in Figure 4.6, one can observe their close resemblance. But in the measured spectrum, there exists a noise floor that buries the theoretical spectrum tail. This noise floor results from reference input noise, VCO noise, other circuit component noise, power supply noise and most significantly, quantization noise, all of which are not

Figure 5.10 PLL Output Spectrum when the Divider is Switched by the Bit-Stream Bearing Modulating Signal

Figure 5.11 A Measured Segment of the Modulating Wave

Figure 5.12 Measured Eye Diagram

reflected in the simulated spectrum shown in Figure 4.6.

Another way of verifying the generated FM signal is to look at it in the time domain, but of course not directly. Within the small frequency range being used

($2f_d=12\text{KHz}$), the VCO can be regarded as linear. So its voltage-control input directly reflects its output instantaneous frequency. Figure 5.11 and 5.12 are the traces measured at the VCO control input through a first order filter and oscilloscope. Figure 5.11 gives a single trace on the oscilloscope. In fact, it shows a segment of modulating wave and can be compared to Figure 4.4. Figure 5.12 gives the eye diagram and has Figure 4.2 as its theoretical reference. Their agreement further proves that the whole system functions well.

5.3.2 Low-Pass Characteristic of the PLL for the Modulating Signal as Reflected in the Experiment

Figure 5.13 PLL Output Spectrum when the Divider is Switched by the Bit-Stream Bearing Modulating Signal (Narrow Loop Bandwidth)

Now the loop bandwidth is made narrower, $f_n = \frac{\omega_n}{2\pi} \approx 15\text{KHz}$ and $\zeta \approx 0.74$
 ($R_1 = 4.7\text{K}\Omega$, $R_2 = 3.3\text{K}\Omega$, $C = 4.7\text{nF}$). The effect on the modulating signal can be

Figure 5.14 A Measured Segment of the Modulating Wave
 (Narrow Loop Bandwidth)

Figure 5.15 Measured Eye Diagram
 (Narrow Loop Bandwidth)

observed. The measurements are shown in Figure 5.13 - 15. The second-order low-pass characteristic of the PLL for the modulating signal is vividly reflected in these graphs. The prediction made in Section 4.2.2.2 is thus confirmed experimentally.

CHAPTER 6 CONCLUSIONS

6.1 Summary

This thesis is believed to be the first to theoretically and experimentally study the incorporation of digital angle modulation into a single loop synthesizer frequency control process via Σ - Δ modulation. This study is motivated by the stringent requirements of compactness, low cost, low power consumption and compatibility with monolithic fabrication for digital portable transceiver modules.

The proposed scheme is derived from two directions: 1. For channelized communication, the main function of a frequency synthesizer is to provide carrier frequencies. With the recent advances in synthesizer techniques, however, the ability to fulfill modulation is also being considered in the synthesizer design. Digital modulation has previously been successfully incorporated into direct digital synthesizers. Is it possible to incorporate digital modulation into an indirect synthesizer which offers advantages of high frequency, compactness, low power consumption, low cost and compatibility for monolithic integration? The author's answer is yes, based on his research, the details of which are provided in this thesis. 2. For conventional direct angle modulation, it is difficult to achieve a stabilized output without significantly affecting the modulation signal. The proposed scheme offers an alternative to this plight and provides more potential for future development.

In the course of this thesis, much simulation and derivation was performed to validate the scheme. Finally, a prototype system was designed and set up for a feasibility

study. Many implementation details are provided that could be referenced for later fabrication. The experimental results, including modulated signal spectra in the frequency domain and eye diagrams in the time domain, verify that the proposed scheme works successfully with the oversampling ratio of 204.8. Further, the low-pass characteristic of the PLL for modulating signal is confirmed experimentally, as well as being predicted analytically.

6.2 Suggestions for Future Research

Given that the incorporation of digital angle modulation into a single loop synthesizer frequency control process via Σ - Δ modulation has been validated, there are many possibilities for future study.

By selecting a higher reference (sampling) frequency and/or a higher order Σ - Δ modulator, quantization noise will certainly be pushed even further away from low frequency signal pass-band and be cut off more easily by the loop as a low pass filter. A multi-modulus divider driven by multi-level Σ - Δ modulator could be employed to achieve better noise shaping and to reduce the finite sequence length effect.

Various baseband waveforms could be stored in ROM to realize different FM schemes. GMSK would be a good candidate. By adding a differentiation process which could be combined into the ROM-stored baseband waveform, PM could also be realized.

As pointed out in Section 4.2.2.1, the application of this system to generate a direct sequence or frequency hopped spread spectrum signal is promising. In this case, the reference frequency must be high to ensure switching speed.

The power amplifier which usually succeeds the modulator could be included

inside the loop for its nonlinearity suppression. Also, this nonlinearity could be equalized at ROM. Further, another mechanism could be added to control the power amplifier gain in order to achieve AM. Therefore, the modified version could be a versatile modulator capable of producing any kind of modulated wave, while at the same time remaining compact, inexpensive, low in power consumption, high in frequency and compatible for monolithic integration.

REFERENCES

- [1] H. Suzuki, K. Momma, and Y. Yamao, "Digital portable transceiver using GMSK modem and ADM codec," *IEEE Transactions on Vehicular Technology*, Vol. 33, No. 3, pp. 220-226, August 1984.
- [2] V. Reinhardt, et al., "A short survey of frequency synthesizer techniques," *40th Annual Frequency Control Symposium*, pp. 355-365, 1986.
- [3] E. C. Kisenwether and W. C. Troxell, "Performance analysis of the numerically Controlled Oscillator," *40th Annual Frequency Control Symposium*, pp. 373-378, 1986.
- [4] R. J. Zavrel, Jr., "Digital modulation using the NCMOTM," *RF Design*, pp. 27-32, March 1988.
- [5] E. W. McCune, Jr., "Digital communications using direct digital synthesis," *RF Design*, pp. 39-46, January 1990.
- [6] J. A. Gallant, "Devices refine the art of frequency synthesis," *EDN*, pp. 95-104, November 1989.
- [7] E. M. Mattison and L. M. Coyle, "Phase noise in direct digital synthesizers," *40th Annual Frequency Control Symposium*, pp. 352-356, 1988.
- [8] J. Gorski-Popiel, *Frequency Synthesis: Techniques and Applications*, IEEE Press, 1975.
- [9] I. Jaquet, "A comparison of phase noise control techniques used in high resolution high-speed frequency synthesizers for mobile radio transceivers," Master Thesis, Carleton, 1990.
- [10] G. C. Gillette, "Digiphase principle," *Frequency Technology*, August 1969.
- [11] C. E. Wheatley, "Digital frequency synthesizer with random jittering for reducing

discrete spectral spurs," *US Patent 4410954*, October 1983.

[12] T. A. D. Riley, M. A. Copeland and T. A. Kwasniewski, "Sigma-Delta modulation in Fractional-N frequency synthesis," to be published.

[13] R. Gilmore and R. Kornfeld, "Hybrid PLL/DDS frequency synthesizers," *RF Design*, pp. 41-45, July 1990.

[14] W. L. Lee and C. G. Sodini, "A topology for higher orders interpolative coders," *IEEE International Solid State Circuits Conference*, Digest of Technical Papers, pp. 459-462, February 1987.

[15] E. Keyes, et al., "Third order, switched capacitor, CMOS, noise shaping, sigma delta coder for oversampled A to D conversion," *Proceedings of the 1986 Canadian Conference on VLSI*, Montreal, pp. 251-264, October 1986.

[16] M. Lamkemeyer, et al., "Switched-capacitor noise-shaping coders of higher order for A/D conversion," *Electronics Letters*, Vol. 21, No. 22, pp. 1039-1040, October 1985.

[17] S. Pasupathy, "Minimum shift keying: a spectrally efficient modulation," *IEEE Communications Magazine*, pp. 14-22, July 1979.

[18] F. de Jager and C. B. Dekker, "Tamed frequency modulation, a novel method to achieve spectrum economy in digital transmission," *IEEE Transactions on Communications*, Vol. 26, No. 5, pp. 534-542, May 1978.

[19] K. S. Chung and L. E. Zegers, "Generalized tamed frequency modulation," *Philips Telecommunication Review*, Vol. 41, No. 1, pp. 82-91, April 1983.

[20] K. Murota and K. Hirade, "GMSK modulation for digital mobile radio telephony," *IEEE Transactions on Communications*, Vol. 29, No. 7, pp. 1044-1050, July 1981.

[21] S. Haykins, *Communication Systems*, John Wiley & Sons Inc., 1983.

[22] J. Molina, "Synthetiseur de frequence a division fractionnaire utilise pour une modulation numerique," *Revue THOMSON-CSF*, Vol. 17, No. 1, pp. 23-42, March 1988

END

2/3·12·92

FIN