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Fully-Integrated Fully-Differential Silicon RF CMOS Distributed Amplifier based on Multi-Tanh Linearization Principle

by

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Faculty of Graduate Studies and Research
in partial fulfillment of the requirements for the degree of
Master of Applied Science

Ottawa-Carleton Institute for Electrical Engineering
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Abstract

The amplification of high frequency signals can be corrupted by nonlinearities present in typical distributed amplifiers. Undesired intermodulation products and significant harmonic distortion may result.

In this thesis, a fully-integrated fully-differential linearized distributed amplifier with third order intermodulation distortion cancellation tuning capability based on silicon RF CMOS technology is designed, fabricated and measured. The design incorporates the principle of Multi-Tanh and Feedforward linearization techniques and employs integrated stacked inductors. The realized design had a total chip area of $2.2 \times 1.1 \text{ mm}^2$. Experimental and simulated results are found to be in good agreement.

A compact lumped-element equivalent broadband circuit model of two-layer integrated stacked spiral inductor on silicon RF CMOS substrate is discussed in this work as well.

Computer-aided-design (CAD) tools and techniques are proven to be useful in the design of the “artificial” gate and drain transmission lines. ASITIC, Agilent ADS Momentum and Cadence Inductor modeler programs are found to be valuable tools in the analysis and optimization of the proposed linearized CMOS distributed amplifier architecture.

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To My Dear Family & Friends

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List of Symbols

ω_c	Cut-off frequency
ε_r	Relative dielectric constant of substrate
A_d	Drain line attenuation per section
A_g	Gate line attenuation per section
A_v	Voltage gain
C_{gd}	Gate-drain capacitance
C_{gs}	Gate-source capacitance
C_{ox}	Capacitance of oxide
C_{si}	Capacitance of silicon substrate
f_{max}	Maximum frequency of oscillation
f_T	Unity current-gain frequency
g_m	Transconductance
I_d	Drain current
L_d	Output drain line inductance
L_g	Input gate line inductance
N_{opt}	Optimum number of gain stages

NF	Noise Figure
P_{1dB}	1 dB compression point
P_{out}	Output power
R_{si}	Resistance of silicon substrate
Z_I	Image impedance
Z_o	Transmission line characteristic impedance
DA	Distributed Amplifier
dB	Decibel
dBm	Decibel referenced to 1 mW
EM	Electro magnetic
GBW	Gain-bandwidth product
IM3	Third-order intermodulation level, in dB
IP3	Third-order intercept point
N	Number of gain stages
Q	Quality factor
RF	Radio Frequency
RoF	Radio-over-Fiber
SRF	Self-resonant frequency
THD	Total harmonic distortion
UWB	Ultra wideband
X-band	frequency band 8-12.4GHz

Chapter 1

Introduction

1.1 Thesis Motivation

Recently, there has been much interest in providing broadband wireless access to fixed networks via RF radio transmission such as “RF Over Fiber” links [1]. It refers to the installation and use of an optical fiber cable to links with the last mile being copper or wireless to the home and/or any business. One promising solution is to use the outdoor broadband wireless access system as the last hop from the fiber to the subscriber [2].

It is expected that “RF Over Fiber” services will benefit not only residential and business consumers but can also assist in fulfilling the telecommunications and information technology needs of intelligent transportation systems “ITS” [3], schools, health care, libraries and rural communities [4] [5].

Distributed circuits are becoming a workhorse component for a variety of wireless and high-data rate communication systems including Radio Over Fiber [6] and ultra wideband transceivers [7]. Such applications require a distributed amplifier topology that can overcome the classical amplifier gain-bandwidth tradeoff by combining the outputs from several active gain elements in an additive fashion [8].

All amplifiers have inherent nonlinearities which limit their usefulness and range of applications. In modern high-performance transceivers, distributed amplification is required to have large dynamic range in order to meet tight system specifications [6].

To date, the majority of distributed amplifiers have been designed using various high-end technologies such as GaAs, HBT, MESFET or HEMT due to higher f_T and better

quality of on-chip passive components. However, the scaling of silicon CMOS has resulted in a strong improvement in the RF performance of CMOS devices. Consequently, silicon CMOS has become a viable option for RF and microwave applications [9].

1.2 Overview of Previous Work

There have been several recently published reports of CMOS distributed amplifiers, which will be discussed briefly in this section.

A summary of the characteristics of various implementations of DA on CMOS technology is presented in Table 1.1.

Table 1.1: State of the art Silicon CMOS Distributed Amplifiers performance comparison.

Ref.	Process	Gain(dB)	BW(GHz)	NF(dB)	S11(dB)	Area(mm ²)	Power(mW)
[10]	0.8 μ m	5	4.7	5.1	-6	0.7x0.3	54
[11]	0.6 μ m	6.5	4	6.8	-7	0.79	83.4
[12]	0.6 μ m	5.5	7.5	8.7-13	-6	1.3x2.2	216
[13]	0.35 μ m	20	5	1.5-3	-15	0.95x1.8	100
[14]	0.18 μ m	8	10	4-8	n/a	1.8x1.3	n/a
[15]	0.18 μ m	10.6	14	3.4-5.4	-11	1x1.6	52
[16]	0.18 μ m	7.3	22	4.3-6.1	-8	0.9x1.5	52
[17]	0.18 μ m	6	27	6	-10	1.8x0.9	68
[18]	0.18 μ m	5	13	n/a	-13	0.3x1.5	n/a

The use of bond-wires replacing inductors was presented by Sullivan et al. in a 0.8 μ m CMOS DA [10]. Sullivan's 4.7GHz CMOS DA achieved a 5dB gain with a 5.1dB noise figure at 2GHz and -6dB S11 and a 15dBm IIP3.

An extra thick 2 μ m AlCu top metal layer and external termination resistors was used by Kleveland et al. [18] to implement a 5-stage Traveling wave amplifier using coplanar stripline as on-chip inductors. The nonstandard 0.18 μ m CMOS process TWA achieved unit-gain frequency of 13GHz.

A practical 0.6 μ m 4-stage CMOS distributed amplifier was implemented by Ballweber et al. [11]. He used on-chip spiral inductors, achieving 6.5dB gain from 0.5GHz to 4GHz when probed on-wafer. It had a noise figure between 5 and 8dB from 0.5 to 2GHz.

Based on the work of Ballweber et al., Ahn and Allstot [12] proposed a differential $0.6\mu\text{m}$ 4-stage CMOS DA which achieved a higher bandwidth and better noise immunity at the expense of reduced gain of 5.5dB, increased ripple by 0.2dB and twice the power dissipation and chip area with a noise figure increase of more than 3dB.

The first to use coplanar waveguides as inductors in $0.18\mu\text{m}$ CMOS TWA design was Frank et al. [16]. With a cascode Darlington TWA gain cell he was able to achieved a gain of 8dB and a bandwidth of 10GHz.

Liu et al. [19] designed a single-ended cascode $0.18\mu\text{m}$ 3-stage CMOS DA with a 7.3dB of gain and a bandwidth of 22GHz with lumped on-chip inductors. Liu et al. [15] also designed another single-ended cascode $0.18\mu\text{m}$ 3-stage CMOS DA with a 10.6dB of gain and a bandwidth of 14GHz.

Amaya and Plett [17] designed a single-ended CMOS distributed amplifier with 27GHz bandwidth using coplanar waveguides as transmission lines in $0.18\mu\text{m}$ CMOS process. Amaya et al. [13] also designed a cascode $0.35\mu\text{m}$ 4-stage CMOS DA with a 20dB of gain and a 5GHz bandwidth.

1.3 Thesis Objectives

The objective of this thesis is to investigate two novel linearized distribution amplification techniques that achieve both tunable linearity and reasonable gain in silicon RF CMOS. The specific thesis objectives in pursuit of this goal are as follows:

1. To perform an analytical and experimental study of IMD3 reduction in silicon RF CMOS distributed amplifiers. To investigate two proposed silicon RF CMOS distributed amplifier based on a Multi-Tanh and Feedforward gain cell topology with tunable IMD3 cancellation capability.
2. To explore the feasibility of the proposed Multi-Tanh DA design with the fabrication of a test chip in a $0.18\mu\text{m}$ standard digital CMOS process.
3. To model, characterize and measure area efficient on-chip multi-level spiral inductors on silicon RF CMOS substrate. Design silicon RF CMOS DA artificial transmission line using the modeled multi-level on-chip inductors.

1.4 Thesis Organization

This thesis will review challenges and limitations of silicon RF CMOS based technologies in Chapter 2 as the basis for circuit design and a quick overview on linearization techniques. Chapter 3 will deal with the principle and theory of CMOS Distributed Amplification. Passive silicon RF CMOS spiral stacked inductors will be studied in Chapter 4. Chapter 5 will explore the design of silicon RF CMOS distributed amplifier based on a Multi-Tanh and Feedforward gain cell topology. The circuit attains wide bandwidth operation with a tunable IMD3 cancellation capability. The aim of Chapter 5 will be to provide an understanding of the techniques of distortion cancelation in silicon RF CMOS based circuits. Design procedures for CMOS fully-differential distributed amplifiers will also be presented. Special emphasis will be given to tuning techniques used for IMD3 cancellation in distributed amplifiers using integrated circuits, broadband matching and layout optimization. Chapter 6 will deal with high frequency layout techniques used in the linearized CMOS DA design and Chapter 7 will deal with test bench setup and measurement results of the multi-Tanh DA. Finally, Chapter 8 draws conclusions and discusses possible future research work.

Chapter 2

Silicon RF CMOS Integrated Technology and RF Linearization Techniques

2.1 Introduction

The rapid growth of optical and wireless communication using wireless LANs, mobile phones and base stations have created a great demand for silicon RF CMOS based RFICs operating at RF and microwave bands [20]. The strong improvement in the RF performance of MOS devices has made CMOS technology a viable option for such applications [20].

In this chapter a brief overview of silicon RF CMOS technology will be presented.

2.2 Why Silicon RF CMOS?

The demand for silicon CMOS RF chips with improved RF performance continues to increase due to the aggressive device scaling. The available transition frequency f_T of MOS transistors increases with every new technology generation [21]. A silicon CMOS-based implementation is advantageous in that it has both lower cost and higher integration capability with baseband circuits [22] [23].

CMOS processes offer a higher yield than other processes such as GaAs, a significant financial incentive which makes it the most appropriate technology for the implementation of a single chip solution, which was the main motivation behind the choice of a CMOS process [22] [24].

2.2.1 Will Silicon RF CMOS Technology Catch the Millimeter Wave?

High-frequency circuits which operate at millimeter-wave bands have been designed using III-V semiconductor technologies, such as GaAs and InP, which have higher performance compared to CMOS technology due to their higher electron mobility and higher breakdown voltage [25] [26].

RF and microwave integrated circuits in silicon RF CMOS were improved by addressing some of the technology key limitations such as transistor low speed in silicon, low quality passives and low isolation due to the conductive silicon substrates [24] [27].

Since RF and mm-wave CMOS circuits directly benefit from the higher speed of the scaled technology, CMOS continues to be used at higher frequencies for optical and wireless communication applications [22] [20].

2.2.2 The Silicon RF 0.18 μm CMOS Process

Figure 2.1: Simplified illustration of silicon MOSFET model.

With the rapid development of competitive high-performance CMOS technology, RF designers need to stay updated on the properties and the limitations of the latest device models [22].

The high-performance and low-cost $0.18\mu\text{m}$ CMOS technology used in this thesis is based on a p-type substrate, with a relatively high substrate conductivity of about $10\Omega\text{cm}$. The core back end stack consist of 1 poly and 6 metal layers of aluminum. The process offers a $0.99\mu\text{m}$ thick top metal and has a dc sheet resistance of 10 mOhms/Sq [28].

2.2.3 Silicon RF CMOS Practical High-frequency Limitations

In short-channel silicon CMOS devices, the ratio of the transconductance to the current can be expressed as [29]

$$\frac{g_m}{I} = \frac{1}{V_{GS} - V_t} = \frac{1}{V_{ov}} \quad (2.2.1)$$

Typically, The overdrive voltage V_{ov} for MOSFET transistors is about several hundred millivolts. Whereas, this ratio is $1/V_T$ for bipolar devices, where the thermal voltage V_T is 26mV . Thus, the g_m per given current is much lower for CMOS transistors than for bipolar ones.

In CMOS transistors, an increase in either input signal amplitude or device size is required to compensate for the small g_m . However, this will result in higher power consumption and will degrade the linearity of the device.

Another limitation in CMOS devices is low-resistivity substrate. The low resistivity substrates in CMOS devices allows for creation of eddy currents, which reduce the effective magnetic field and in turn have a negative impact on the quality factor of the on-chip spiral inductors [30].

The gate material used for CMOS devices is polysilicon, which has a high sheet resistance. A higher gate resistance can reduce the transistor power gain and increase noise. Fortunately, simple layout techniques, such as multi-fingering, can be used to reduce the negative effects of the polysilicon gate [28].

2.2.4 High Frequency MOSFET Model

The physical MOS small-signal equivalent circuit lumped model is depicted in Figure 2.2. In addition to the main RF device, parasitic access resistors, R_s , R_g , R_d and series inductors, L_s , L_g , L_d are added to all terminals to accurately model the delay effects related to

interconnect wiring [28].

C_{gs} , C_{ds} , C_{gd} capacitors are classical MOSFET intrinsic channel and overlap capacitances. Drain resistance R_{ds} , gate resistance R_{gs} and transconductance g_m are classical MOSFET equivalent circuit elements as well.

Figure 2.2: The physical MOSFET small-signal equivalent circuit lumped model.

2.3 CMOS Devices Figures of Merit

The most relevant figure-of-merits for the high-frequency capabilities of a process are defined as follows:

2.3.1 CMOS Unity Current Gain

The figure of merit f_T represents the maximum fundamental frequency component a device can generate.

f_T can also be defined as the frequency at which the current gain of the device is unity. For a CMOS FET device, f_T is approximated by [23] [22]

$$f_T = \frac{g_m}{2\pi \cdot (C_{gs} + C_{gd})} \quad (2.3.1)$$

Where g_m is the device transconductance and C_{gs} and C_{gd} are the gate-source and gate-drain overlap capacitances, respectively.

Figure 2.3 show simulated f_T unity current gain testbench for CMOS RF MOSFET active device with a $5\mu\text{m}$ width and a finger number of 32.

Figure 2.3: Simulated f_T unity current gain CMOS RF MOSFET active device testbench.

With the parameters from foundry supplied BSIM3v3 model files for $0.18\mu\text{m}$ process and with transconductance bias V_{gs} at 1.1V and with device size of $160\mu\text{m}$ width and $0.18\mu\text{m}$ length, the f_T is characterized in Figure 2.4 to be 49.85GHz .

By proper biasing, the f_T of an NMOS transistor in a standard $0.18\mu\text{m}$ CMOS technology can easily surpass 50GHz , opening the possibility for mm-wave circuits [20].

2.3.2 CMOS Maximum Frequency of Oscillation

For a CMOS MOSFET device, the frequency at which the maximum power gain is unity is defined as f_{max} which is approximated by [23] [22]

Figure 2.4: Simulated f_T unity current gain at 49.85GHz for CMOS RF MOSFET $0.18\mu\text{m} \times 160\mu\text{m}$ active device biased at 1.1V gate bias.

$$f_{\max} = \frac{f_T}{2\sqrt{g_{ds}(R_g + R_s) + 2\pi f_T R_g C_{gd}}} \quad (2.3.2)$$

where R_g and R_s are the resistance at the gate and source, g_{ds} is output conductance, and C_{gd} is the parasitic gate to drain capacitance. Where the gate resistance R_g is critical in determining $f_{\max}$ [31] which makes it a layout dependant figure of merit.

2.3.3 CMOS Maximum Power Gain

The maximum power gain sets a limit to how much power gain a CMOS device can provide. For a CMOS device $G_{\max}$ can be defined by [23]

$$G_{\max} = \frac{f_T}{8\pi R_g C_{gd} f^2} \quad (2.3.3)$$

where R_g is the gate resistance and C_{gd} is the parasitic gate to drain capacitance and f is the frequency of operation of the device and f_T is the unity current gain of the device.

2.3.4 CMOS Minimum Noise Figure

At high-frequencies CMOS device's channel thermal noise is the main noise source. The minimum noise figure is given by [23] [22]

$$NF_{\min} = 1 + K \frac{f}{f_T} \sqrt{g_m (R_g + R_s)} \quad (2.3.4)$$

where K is a material dependent constant. Where R_g and R_s are the resistance at the gate and source and g_m is the device transconductance. f_T is the unity current gain of the device and f is the frequency of operation of the device.

As can be noticed in (2.3.4) $NF_{\min}$ is a function of the bias current and frequency of operation and is expected to decrease with scaling of future CMOS devices [23].

2.4 Signal Distortion and Dynamic Range Considerations

All radio receivers contain nonlinear RF signal processing components such as amplifiers and mixers. An important objective of radio transceivers in communication applications is to combine low distortion with low noise in order to achieve a high dynamic range [32].

2.4.1 Why is Linearity so Important?

One of the main requirements in radio systems is minimum possible interference to other radio users [33].

Consider a device with two closely spaced in frequency signals at its input, one at a frequency w_1 and the other at frequency w_2 . It is usually the IMD3 products, at frequencies $2w_1 - w_2$ and $2w_2 - w_1$, that are of most concern because they fall in band near the two frequencies of interest, w_1 and w_2 , as shown in Figure 2.5 and therefore will be the most difficult to filter out of the system [34].

Therefore, RF telecommunication circuits, such as distributed amplifiers, require devices that exhibit highly linear operating characteristics.

Figure 2.5: Inband IM3 distortion for two inband interferer. IM3 fall near frequencies of interest. When filtering is applied, IM3 are difficult to filter out.

2.4.2 Linearity Metrics and Measures of Distortion

The third-order input intercept point, IIP3 as depicted in Figure 2.6, is a widely used figure of merit to quantifying the effects of intermodulation products in communication systems [35].

Where as the 1dB compression point measures the gain compression for large input signal as depicted in Figure 2.6.

2.5 CMOS High-frequency Amplifiers Nonlinear Distortion

All amplifiers are inherently non-linear devices [36]. Nonlinear characteristics of transistors produce intermodulation (IM) distortion, that can adversely effect system performance [37]. Non-linearity of the circuit arises from the non-linear dependence of I_d upon v_{in} .

The nonlinear I-V characteristic of a CMOS transistor can be approximated as [34] [38] [39]

Figure 2.6: System linearity metrics and measures of distortion.

$$I_d(v_{GS}) = \frac{\beta}{2[1 + \theta(v_{GS} - V_T)]} (v_{GS} - V_T)^2 \quad (2.5.1)$$

where θ is a mobility degradation factor, β is the transconductance factor, v_{GS} small signal gate-to-source voltage and V_T is the threshold voltage.

Assuming second term in (2.5.2) is much smaller than one.

$$[\theta(v_{GS} - V_T)] \quad (2.5.2)$$

Then equation (2.5.1) can be rewritten as [39]

$$I_d(v_{GS}) = \frac{1}{2}\mu_o C_{ox} \left(\frac{W}{L}\right) (v_{GS} - V_T)^2 \quad (2.5.3)$$

Using Taylor series expansion, the drain current of a FET small-signal nonlinear distortion from transconductance g_m can be modeled by a Taylor series expansion of the nonlinearity around the bias point. The FET drain current I_{ds} can be expressed as [34] [37]

$$I_{ds}(v_{GS}) \approx I_{dc} + \frac{\partial I_d}{\partial v_{GS}} \delta v_{GS} + \frac{1}{2!} \frac{\partial^2 I_d}{\partial v_{GS}^2} \delta v_{GS}^2 + \frac{1}{3!} \frac{\partial^3 I_d}{\partial v_{GS}^3} \delta v_{GS}^3 \quad (2.5.4)$$

$$I_{ds}(v_{GS}) \approx I_{dc} + a_1 \delta v_{GS} + \frac{a_2}{2!} \delta v_{GS}^2 + \frac{a_3}{3!} \delta v_{GS}^3 \quad (2.5.5)$$

When the input is excited by two RF stimulus time harmonic signals of equal amplitude at frequencies ω_1 and ω_2 as in (2.5.6)

$$\delta v_{GS} = A [\sin(\omega_1 t) + \sin(\omega_2 t)] \quad (2.5.6)$$

It is well-known that v_{GS}^3 coefficient in (2.5.6) plays a vital role in determining the IMD3 of the CMOS RF amplifier [35]

$$\frac{a_3}{3!} \delta v_{GS}^3 = \frac{a_3}{6} \cdot \frac{A^3}{4} \{3 \sin[(\omega_1 - 2\omega_2)t] + 3 \sin[(2\omega_1 - \omega_2)t]\} + \dots \quad (2.5.7)$$

The IP3 is defined as the signal level at which the above sidebands in (2.5.7) have the same amplitude as the input signals amplified by the first order term

$$a_1 \cdot \delta v_{GS} \quad (2.5.8)$$

and can thus be calculated as:

$$a_1 \cdot A = \frac{a_3}{6} \cdot A^3 \frac{3}{4} \quad (2.5.9)$$

Therefore, solving the equation (2.5.9) gives

$$A = \sqrt{8 \left| \frac{a_1}{a_3} \right|} \quad (2.5.10)$$

By inserting the values of a_1 and a_3 calculated from equation (2.5.1) we get

$$A = \sqrt{\frac{4}{3}} \sqrt{\frac{v_{od} (1 + \theta v_{od})^2 (2 + \theta v_{od})}{\theta}} \quad (2.5.11)$$

Where v_{od} is the overdrive voltage defined as:

$$v_{od} = V_{GS} - V_t \quad (2.5.12)$$

and V_{GS} is the gate-source bias voltage. We see that the IIP3 is a function of v_{od} . The higher the overdrive voltage, the higher the IIP3. This analytical expression for the third-order intercept point as a function of DC-bias will be used in the design consideration of the linearized Multi-Tanh CMOS DA Chapter 5.

2.6 RF Linearization Techniques

The performance of radio transceivers continue to be limited by the presence of nonlinearities in CMOS RF amplifiers [34].

Undesired signals that block the reception of weak signals in receivers and undesired out-of-band radiation that can interfere with adjacent frequency bands in transmitters all have motivated the development of a variety of approaches to linearize CMOS devices [34].

Various linearization techniques has been proposed earlier which suffer many limitations in both complexity and performance.

Modern communication system RF linearization techniques can be classified into three main categories [40]: a) RF feedforward technique, b) RF feedback technique, c) RF pre-distortion technique d) Optimum gate biasing technique and e) Derivative superposition technique.

2.6.1 RF Feedforward Technique

Invented by Harold S. Black, in 1928 [41], the Feedforward technique is the most popular linearization technique for IMD correction. His basic idea for the Feedforward technique was to build two identical amplifiers and use one amplifier to subtract the distortion from the other.

Feedforward systems are unconditionally stable and ideally do not reduce amplifier gain [41] [40].

The feedforward method is preferred to other schemes because it does not decrease the gain of amplifier significantly [40].

2.6.2 RF Feedback Technique

The second major linearization method is the Feedback technique [40].

Harold S. Black also invented the negative Feedback technique [42] as a way as to solve the distortion problem of the positive feedback technique.

Feedback can include active and passive techniques [40]. The principle limitation of feedback is the inability to handle wideband signals [40]. Beyond several MHz the delay of the amplifier and associated signal processing components can cause instability.

2.6.3 RF Predistortion Technique

The third major linearization technique is predistortion [40]. Predistortion is based on the idea of placing a nonlinear device preceding the RF amplifier then cascading the two devices such that the total output transfer function of both devices has a linear transfer characteristic [43] resulting in a system that has little or no distortion.

Analog Predistortion linearization techniques function at RF frequencies. The main disadvantages of RF predistortion is its modest linearity improvement compared to other linearization techniques [40].

2.6.4 RF Optimum Gate Biasing Technique

Another simple linearization technique suitable for FET amplifiers is the optimum gate biasing linearization technique. It is based on biasing a FET transistor at the gate-source voltage at which the 3rd-order derivative of its dc transfer characteristic is zero. Such biasing causes an IMD3 nulling [44].

2.6.5 RF Derivative Superposition Technique

Derivative superposition linearization technique extends the bias voltage range in which a significant IIP3 improvement is achieved [45] [46].

Most of these linearization schemes are implemented at the board level, i.e. multiple chip solutions, and have not really been explored at the integrated single-chip level.

2.7 Chapter Summary

This chapter presented reasons why CMOS is being considered for high-frequency applications, with references to appropriate prior work. Both the concept of nonlinearity in MOSFET devices and the effects of nonlinearity on radio systems were discussed. Modern communication system RF linearization techniques were also presented.

Chapter 3

Silicon RF CMOS Distributed Amplification - Principle of Operation

3.1 Introduction

In this chapter, a brief DA historical perspective is presented. A theoretical analysis of the CMOS DA operation for both ideal and lossy constant-k transmission lines is discussed. Expressions for power gain, optimum number of stages and line attenuation, specific to CMOS technology, are presented for both cases.

3.2 Distributed Amplification - Historical Perspective

During the 1960s, using transistor devices instead of vacuum tubes in distributed amplifiers was still under research [47].

A detailed paper by Ginzton et al. [48] in 1948 turned Percival's patented concept [19] of distributed amplification into an actual implementation. Monolithic GaAs FET-based distributed amplifiers were successfully designed during early 1980s [49] [50]. The useful advantages of GaAs DAs, such as their wide bandwidth and gain flatness, were rapidly recognized leading to intense research and development [51] [52].

Distributed amplifier IC's are widely used as broadband gain blocks in many applications such as optical transceivers and high data rate communication systems [53].

3.3 CMOS Distributed Amplifier Theory

The concept of distributed amplification is based on the principle of utilizing the parasitic capacitances of FET transistors in a constructive manner so as to form the artificial transmission lines as depicted in Figure 3.1 [50].

These capacitors, in conjunction with inductors coupled by the transconductance of the FETs provide a propagating medium in which signal waves can travel [50].

If these artificial transmission lines are well designed, the maximum operating frequency of the amplifier would be limited by the cut-off frequency of these transmission lines not the FET device itself [6] [54].

Figure 3.1: (a) Simplified CMOS distributed amplifier with artificial transmission lines physical configuration. (b) CMOS DA with transmission lines circuit equivalent configuration.

An RF input signal applied at the gate line is depicted in Figure 3.1. As the RF input signal travels down the gate line, each FET transistor is excited by the traveling power wave and transfers the signals to the drain line through its transconductance [6] [54]. If the phase velocities on the gate and drain lines are equal, then the power signals on the drain line add in the forward direction and an RF output signal is generated. The waves traveling in the reverse direction are absorbed by the drain line termination [6] [54].

3.4 CMOS Distributed Amplifiers Basic Operation: Lossless Condition

To get a better understanding of the CMOS DA operation, it is useful to consider the wave propagation behavior along the lossless transmission line. Assuming ideal transistors with no parasitics, the output drain current is given by [29] [55]

$$i_d = g_m \cdot v_{gs} \quad (3.4.1)$$

The RF input signal is fed into the gate line, where it excites the FET transistors along the gate line as it propagates, until it reaches the gate line termination, where it is ideally dissipated without reflections [54].

Assuming gate and drain line have equal propagation velocity and zero loss, $\beta_g = \beta_d$ and $\alpha = 0$ for the lossless condition, where α is defined as attenuation factor and β is also known as phase constant [10] [56] [57].

An input wave v_g propagating on a lossless line can be expressed as in (3.4.2) [57] [50] [55], where v_g appears at the transistor inputs as v_{gs} and half of V_s being the amplitude of the input wave that flows into the terminating gate resistance.

$$v_g(z) = \frac{V_s}{2} \cdot e^{-j\beta z} \quad (3.4.2)$$

An input wave propagating along the gate line to the output on the drain line is depicted in Figure 3.2 and given by,

$$v_{gn} = \frac{V_s}{2} \cdot e^{-(n-1)j\beta_g \ell_g} \quad (3.4.3)$$

Figure 3.2: Simplified wave propagation in CMOS distributed amplifier.

where $n=1$ when it is the first stage, implies there is no delay. The output drain current and output voltage relationship is given in equation (3.4.4)

$$v_o = I_d \cdot Z_d \quad (3.4.4)$$

The output drain current across the n -th FET, I_d , can be expressed as [50] [58] [55]

$$I_d = \frac{1}{2} \sum_{n=1}^N i_{dn} (e^{-(N-n)})^{j\beta_d \ell_d} \quad (3.4.5)$$

where $n = N$ represents the last stage and knowing the transconductance relationship in equation (3.4.6)

$$i_{dn} = g_m \cdot v_{gs} \quad (3.4.6)$$

Substituting equation (3.4.3) and (3.4.5) into (3.4.6) we get [50] [58] [55]

$$I_d = -\frac{g_m}{4} \cdot V_s \cdot \sum_{n=1}^N (e^{-(n-1)})^{j\beta_g \ell_g} \cdot (e^{-(N-n)})^{j\beta_d \ell_d} \quad (3.4.7)$$

$$I_d = -\frac{g_m}{4} \cdot V_s \cdot e^{-Nj\beta_d\ell_d} \cdot e^{j\beta_g\ell_g} \cdot \sum_{n=1}^N (e^{-nj})^{(\beta_g\ell_g - \beta_d\ell_d)} \quad (3.4.8)$$

Each FET injects current into the output line as seen in Figure 3.2, if the phase constants of both lines are equal, these currents add constructively at the output, while out-of-phase signals are dissipated on the drain termination [50]. If under normal operating conditions, the waves in the gate and drain lines are near synchronism [49] [55]

$$\beta_g\ell_g = \beta_d\ell_d = \beta\ell \quad (3.4.9)$$

$$I_d = -\frac{g_m}{4} \cdot V_s \cdot e^{-Nj\beta\ell} \cdot e^{j\beta\ell} \cdot N \quad (3.4.10)$$

In the case of ideal lossless constant-k lines, the expression for the power gain of N section distributed amplifier is thus given by [50]

$$G = \frac{P_{out}}{P_{in}} = \frac{\frac{1}{2} |I_d|^2 Z_d}{|v_g|^2 / 4 Z_g} = \frac{g_m^2 Z_d Z_g N^2}{4} \quad (3.4.11)$$

For the ideal lossless transmission line case the gain increases relative to N^2 as can be seen from (3.4.11), and the bandwidth is infinite.

3.5 CMOS Distributed Amplifiers Basic Operation: Lossy Condition

The simplified CMOS equivalent circuits of the gate and drain lines of a DA, is shown in Figure 3.3, using N FET gain cells which are connected using transmission lines absorbing the capacitances of a FET into those of the transmission line.

The parasitic capacitances C_{gs} and C_{ds} of each FET device are separated using inductors, forming the artificial transmission lines. As depicted in Figure 3.3 the drain and gate artificial lines are terminated by their characteristic impedances.

The CMOS transistor equivalent small signal model with losses is depicted in Figure 3.4, where R_i is the intrinsic charge resistance.

Transistor will load the line and losses will increase transmission line losses which limits

Figure 3.3: Silicon CMOS DA equivalent small signal circuit.

Figure 3.4: Lossy equivalent small signal CMOS transistor model.

the distributed amplifier performance [50].

If we assume a unilateral MOSFET transistor device, we can set $C_{gd}=0$ [50]. We will enforce equal gate and drain phase velocities and matched image impedance terminations as well. Figure 3.5 shows an equivalent gate line circuit.

The gate resistance R_i in series with parasitic capacitance C_{gs} introduces a frequency dependent attenuation per line section [50].

The impedance of the gate line, shown in Figure 3.5, can be approximated as [49]

Figure 3.5: Gate Line equivalent distributed circuit representing loss per normalized gate unit cell.

$$Z = j\omega L_g \quad (3.5.1)$$

where L_g is the per-unit-length inductance of the gate line as shown in Figure 3.5.

$$Y = j\omega C_g + \frac{j\omega C_{gs}/l_g}{1 + j\omega R_i C_{gs}} \quad (3.5.2)$$

$$Z_g = \sqrt{\frac{Z}{Y}} \cong \sqrt{\frac{L_g}{C_g + C_{gs}/l_g}} \quad (3.5.3)$$

The propagation constant of the gate line, γ_g can be expressed as [56]

$$\gamma_g = \alpha_g + j\beta_g = \sqrt{Z \cdot Y} \quad (3.5.4)$$

Substituting (3.5.2) and (3.5.3) into (3.5.4) we get the propagation constant of the gate line as follows

$$\gamma_g = \sqrt{j\omega L_g \left(j\omega C_g + \frac{j\omega C_{gs}/l_g}{1 + j\omega R_i C_{gs}} \right)} \quad (3.5.5)$$

$$\gamma_g \cong \sqrt{-\omega^2 L_g \left(C_g + C_{gs} (1 - j\omega R_i C_{gs})/l_g \right)} \quad (3.5.6)$$

The equivalent drain line circuit is shown in Figure 3.6.

Figure 3.6: Drain line equivalent distributed circuit representing loss per normalized drain unit cell.

The impedance of the drain line, shown in Figure 3.5, can be approximated as [49]

$$Z = j\omega L_d \quad (3.5.7)$$

where L_d is the per-unit-length inductance of the drain line as shown in Figure 3.6.

$$Y = \frac{1}{R_{ds}l_d} + j\omega \left(C_d + C_{ds}/l_d \right) \quad (3.5.8)$$

where R_{ds} is the shunt resistance of the MOSFET and ω is the operating frequency [49]

$$Z_d = \sqrt{\frac{Z}{Y}} \cong \sqrt{\frac{L_d}{C_d + C_{ds}/l_d}} \quad (3.5.9)$$

The propagation constant of the drain line, γ_d can be expressed as [56]

$$\gamma_d = \alpha_d + j\beta_d = \sqrt{Z \cdot Y} \quad (3.5.10)$$

Substituting (3.5.8) and (3.5.9) into (3.5.10) we get the propagation constant of the drain line as follows

$$\gamma_d = \sqrt{j\omega L_d \left(\frac{1}{R_{ds}l_d} + j\omega (C_d + C_{ds})/l_d \right)} \quad (3.5.11)$$

Since $j\omega(C_d + C_{ds}/l_d)$ term dominates in (3.5.11)

$$\gamma_d \cong \frac{Z_d}{2R_{ds}l_d} + j\omega \sqrt{l_d (C_d + C_{ds}/l_d)} \quad (3.5.12)$$

The gain calculation with the lossy condition can be determined as follows [49]

$$v_{gsn} = \frac{V_s}{2} \cdot e^{-(n-1)j\gamma_g \ell_g} \left(\frac{1}{1 + j\omega R_i C_{gs}} \right) \quad (3.5.13)$$

$$\left(\frac{1}{1 + j\omega R_i C_{gs}} \right) \approx 1 \quad (3.5.14)$$

$$I_d = -\frac{g_m}{4} \cdot V_s \cdot e^{-N\gamma_d \ell_d} \cdot e^{\gamma_g \ell_g} \cdot \sum_{n=1}^N (e^{-n})^{(\gamma_g \ell_g - \gamma_d \ell_d)} \quad (3.5.15)$$

$$I_d = -\frac{g_m V_s}{4} \cdot \frac{e^{-N\gamma_g \ell_g} - e^{-N\gamma_d \ell_d}}{e^{-\gamma_g \ell_g} - e^{-\gamma_d \ell_d}} \quad (3.5.16)$$

When losses are incorporated in the analysis, the power gain can be determined as, assuming unilateral device [49]

$$G = \frac{g_m^2 \cdot Z_d \cdot Z_g}{4} \cdot \frac{(e^{-N\alpha_g \ell_g} - e^{-N\alpha_d \ell_d})^2}{(e^{-\alpha_g \ell_g} - e^{-\alpha_d \ell_d})^2} \quad (3.5.17)$$

$$e^{-\alpha_g \ell_g} - e^{-\alpha_d \ell_d} \approx \alpha_g \ell_g - \alpha_d \ell_d \quad (3.5.18)$$

As can be seen, the gain is no longer a monotonic function of N but peaks at a finite N.

In other words, adding an extra stage will only improve gain if the product of $\frac{g_m \cdot V_{gs}(N+1) \cdot Z_d}{2}$ is greater than $|e^{\gamma_d \ell_d}|$, where $\frac{g_m \cdot V_{gs}(N+1) \cdot Z_d}{2}$ is the extra gain and $e^{\gamma_d \ell_d}$ is the attenuation on the drain line. Therefore, the loss due to the extra transmission line exceeds the gain of the N FET. Eventually the polynomial additive increase in gain due to the extra stage will not outweigh the exponential loss.

By taking the derivative of the gain function in equation (3.5.17), we get the optimum number of MOSFET gain cells for maximum gain [50] [12]

$$N_{opt} = \frac{\ln(\alpha_g \ell_g / \alpha_d \ell_d)}{\alpha_g \ell_g - \alpha_d \ell_d} \quad (3.5.19)$$

where α_g and α_d are the attenuation per section in Nepers on the gate and drain line.

We also notice that the gain is not flat with frequency due to frequency dependence of α_g and α_d .

There are two advantages of maximizing the number of stages. The mid-band gain ripple is proportional to $1/N$ [47], where N is the number of sections. Also, the noise figure of a distributed amplifier improves with higher number of stages assuming no losses in the artificial transmission line [55].

3.6 Artificial Transmission Line Models

Artificial transmission lines are usually modeled by cascading T-sections as shown Figure 3.7. The structure is usually referred to as low-pass constant k filter.

In the case of a lossless lumped cascade of T-section, the image impedance and the propagation coefficient are respectively given by [56]

Figure 3.7: Lowpass constant-k filter constructed using a cascade of T-sections.

$$Z_i = \sqrt{L/C \left(1 - \left(\omega/\omega_c \right)^2 \right)} \quad (3.6.1)$$

$$e^\gamma = 1 - \frac{2\omega^2}{\omega_c^2} + \frac{2\omega}{\omega_c} \sqrt{\frac{2\omega^2}{\omega_c^2} - 1} \quad (3.6.2)$$

where ω_c is the line cut-off frequency of the transmission line given by [12] [50]

$$\omega_c = \frac{2}{\sqrt{LC}} \quad (3.6.3)$$

The characteristic impedance Z_o of the lossless artificial transmission line is given by [12] [50]

$$Z_o = \sqrt{\frac{L}{C}} \quad (3.6.4)$$

where L and C are the inductance and capacitance per unit length of the transmission line.

The artificial transmission line has a cut-off frequency f_c given by [50]

$$f_c = \frac{1}{\pi\sqrt{LC}} \quad (3.6.5)$$

The bandwidth is determined by the input capacitance of the transistor and the inductance of the transmission line yielding a wider bandwidth than that of lumped element circuits [50]. Artificial line uses lumped inductors and capacitors. C_{gs} and C_{ds} are absorbed into the T-line.

In the presence of attenuation, the gate signal decays as it propagates down the line. Hence, there will be a point at which the gain added by an additional device will not overcome the losses induced by the extra section in the gate and drain lines.

The reason for this is that the devices added are not driven sufficiently to overcome the losses in the drain line cause of high signal attenuation.

3.7 Conclusion

In this chapter, a theoretical analysis of CMOS DA operation for both lossless and lossy constant-k transmission lines is presented. The derivation for the power gain, optimum number of stages and line attenuation expressions, specific to MOSFET device, are presented in both cases. It is clear that for an ideal simple case, the gain is a monotonic function of number of stages. For a lossy constant-k transmission line however, the polynomial increase in gain due to extra stages will not outweigh the exponential loss. The power gain, optimum number of stages expressions presented in this chapter is intended to be used in analytical design procedure which will be a starting point for simulations.

Chapter 4

Integrated CMOS RF Passive Stacked Inductor Characterization and Modeling

4.1 Introduction

On-chip inductors play a crucial role in radio frequency integrated circuits. Several factors degrade the performance of on-chip passives at high frequencies such as skin effect, proximity effect, electric field penetration into substrate, and substrate eddy current losses [59].

This chapter discusses the design and optimization of multi-level on-chip inductor circuits. The major issues that must be considered in the development of accurate models of spiral stacked inductors on silicon CMOS substrates will be presented.

4.2 Overview

For gigahertz circuitry, on-chip inductors are usually designed using spirals, as shown in Figure 4.1, since they exhibit good matching and they permit a large range of inductances to be realized. However, they possess small Q values and are difficult to model [60].

The problem of producing high- Q inductors in silicon CMOS technologies presents a serious challenge to RF integration at widely used microwave frequencies [30]. Recent attempts to integrate inductors into conventional silicon CMOS technologies have yielded either inductor Q values of less than 10, or required additional processing steps to remove the lossy silicon substrate.

Figure 4.1: Square spiral inductor with 1.75 turns.

4.3 Silicon Integrated Inductor Characterization

The main parameters that characterize an inductor are its self-inductance value, L , its quality factor, Q , and its resonant frequency f_{res} [61].

While capacitors store electric energy, inductors store magnetic energy [62]. Hence, Q is proportional to the net magnetic energy stored which is equal to the difference between the peak magnetic and electric energies.

An inductor reaches self-resonance frequency when both the peak electric and magnetic energies are the same [63].

The performance of an inductor is best judged by the inductance value and its quality factor, Q , across a frequency spectrum of interest. A good inductor has a high Q .

Q can be defined as follows [62]

$$Q = 2\pi \cdot \frac{\text{energy stored}}{\text{energy loss in one oscillation cycle}} \quad (4.3.1)$$

4.4 High Frequency Loss Mechanisms in Silicon RF CMOS Inductors

A good understanding of loss mechanisms is essential in designing silicon RF CMOS on-chip inductors. Loss mechanisms include metal losses, substrate losses and high frequency

losses [59].

At lower frequencies, metal losses are mainly determined by the sheet resistance of the process layers used to create the device [57]. At higher frequencies, skin effect, proximity effects and current crowding have a major impact on loss mechanism [64] as illustrated in Figure 4.2.

Figure 4.2: Losses mechanisms that can affect integrated silicon inductors.

The skin effect drives the ac current toward the surface of the conductor [64]. Skin effect increases the ac resistance of the conductor leading to lower Q .

Proximity effect metal loss degrades the performance of on-chip inductor at high frequency due to the influence of the magnetic field created by a nearby conductor [65] and thereby increasing the effective series resistance in (4.4.1) [66],

$$Q = \frac{\omega L_s}{R_s} \times \frac{R_p}{R_p + [(\omega L_s / L_s)^2 + 1] \cdot R_s} \times \left(1 - \frac{R_s^2 C_o}{L_s} - \omega^2 L_s C_o \right) \quad (4.4.1)$$

where L_s represents the series inductance, R_s the series resistance, R_p represents the parallel resistance and C_o the sum of both C_s and C_p .

Eddy current substrate losses are caused by the magnetic field of the conductor inducing a current in the substrate parallel to the direction of the current flow in the conductor [64].

4.5 Why Do We Implement Stacked Inductors?

The multi-level spiral inductor was first proposed by H. J. Finlay in 1985 [67]. The first actual implementation and experimental results were presented by M. W. Geen [67]. Strong mutual coupling in multi-layer inductors allows the generation of the same inductance in less area as compared to planar inductors [68].

Figure 4.3: Silicon RF multi-level stacked inductor.

In distributed broadband amplifiers, a large number of inductors are necessary, leaving a small silicon area for each [12]. A good candidate for this purpose is the stacked structure shown in Figure 4.3, where two planar spirals are placed in series each on different metal layer.

4.6 How Do We Implement Stacked Inductors?

On-chip inductors can be designed using more than one level of metal. The increasing number of metal layers available in modern RF CMOS process technologies made the

multi-layer inductor design simpler [69] [62] [68].

Multi-level inductors can be implemented by connecting two or more layers in series [62]. This will let the same silicon area to be realized in an increased inductance value as shown in Figure 4.3.

Since the current flows through both metal layers in the same direction, the magnetic flux lines in the same direction result in higher mutual inductance [62]. The fluxes through the two windings will strengthen one another and the total inductance of a stacked spiral consists of the sum of the two planar spiral inductances plus their mutual inductance [62].

If perfect coupling is assumed and both inductors L are equal in size, then this gives approximately four times the inductance value L . Thus, this is a way to get larger inductance without using as much chip area [62].

One drawback with this approach is the lower self-resonant frequency resulting from the large feedthrough capacitance between the layers [70].

The layout of a stacked spiral inductor with 1.75 turns is depicted in Figure 4.3.

Once the spiral layout is chosen, the physical parameters have to be determined, including number of turns, conductor width and line separation.

4.7 Silicon CMOS Inductor Modeling in ASITIC

On-chip silicon CMOS inductor implementation involves a large number of trade-offs. In order to understand these trade-offs, we need to consider the geometry of the inductor layout [59] [71].

Square spirals are popular in circuit design because of the ease of their layout. Square inductors are generated easily with ASITIC [71]. ASITIC generates the inductor pi model parameters of spiral inductors through electromagnetic field solutions at a given frequency [71]. The layout is then imported to Cadence and ADS simulation environments.

The geometrical parameters of a spiral are specified as follows:

The number of turns, N , the metal width, W , the edge-to-edge spacing between adjacent turns, S , and the outer diameter, OD .

The geometrical parameters were chosen to realize optimum inductance value while minimizing parasitic capacitance and area.

Table 4.1 to Table 4.4 shows the on-chip inductor characterization Pi model results obtained by ASITIC simulations. In all cases, the dc series resistance predicted by ASITIC is less than 3.5Ω .

Three planar square inductors were designed using ASITIC. The first single layer inductor was implemented using the top metal layer with an outer diameter of $70\mu\text{m}$ and the second with outer diameter of $80\mu\text{m}$ and the third with outer diameter of $90\mu\text{m}$.

The outer diameter, OD, is increased from $70\mu\text{m}$ to $90\mu\text{m}$ as shown in Table 4.1. The inductance value increases from 227pH to 373pH with increasing outer diameter where as the self-resonant frequency is decreased from 95.6GHz to 62.8GHz. Since parasitic capacitance increase in proportion to the size of the inductor, the f_{res} decreases as the size of the inductor increases. The smaller inductor size results in an improved f_{res} . Also the Q value is increased from 7.36 to 8.35 and the series resistance value increases with increasing outer diameter from 1.5Ω to 2.07Ω .

Table 4.1: ASITIC simulation Pi model parameter extraction for single layer square spiral inductor, conductor spacing= $2\mu\text{m}$, $W=10\mu\text{m}$, number of turns=1.75 and varying outer diameter at 8GHz.

Outer Diameter	Inductance value	Quality factor	Series Resistance	f_{res}
70 μm	0.227 nH	7.36	1.5 Ω	95.6GHz
80 μm	0.297 nH	7.93	1.79 Ω	76GHz
90 μm	0.373 nH	8.35	2.07 Ω	62.8GHz

The inductor line spacing, S, is increased from $2\mu\text{m}$ to $5\mu\text{m}$ as depicted in Table 4.2. The inductance value decreases from 297pH to 248pH with increasing S and the self-resonant frequency is increased from 88.1GHz to 93.5GHz. The Q value is decreased from 6.9 to 6.62 and the series resistance value decreases from 1.99Ω to 1.85Ω .

The inductor width, W, is increased from $10\mu\text{m}$ to $16\mu\text{m}$ as depicted in Table 4.3. The inductance value decreases from 279pH to 144pH, since the loop area of the inner windings decreases with increasing width where as the self-resonant frequency increases from 88.1GHz to 118.4GHz. The Q quality factor decreases from 6.9 to 5.39 and the series resistance value decreases with increasing line width, W, from 1.99Ω to 1.33Ω .

Table 4.2: ASITIC simulation Pi model parameter extraction for single layer square spiral inductor, OD=80 μ m, W=10 μ m, number of turns=1.75 and varying conductor spacing at 8GHz.

Conductor Spacing	Inductance value	Quality factor	Series Resistance	f_{res}
2 μ m	0.297 nH	6.90	1.99 Ω	88.1GHz
3 μ m	0.268 nH	6.83	1.93 Ω	89.2GHz
4 μ m	0.258 nH	6.73	1.89 Ω	91.6GHz
5 μ m	0.248 nH	6.62	1.85 Ω	93.5GHz

Table 4.3: ASITIC simulation Pi model parameter extraction for single layer square spiral inductor, conductor Spacing=2 μ m, outer diameter=80 μ m, number of turns=1.75 and varying conductor Width at 8GHz.

Conductor Width	Inductance value	Quality factor	Series Resistance	f_{res}
10 μ m	0.279 nH	6.90	1.99 Ω	88.1GHz
14 μ m	0.184 nH	6.17	1.48 Ω	104.9GHz
16 μ m	0.144 nH	5.39	1.33 Ω	118.4GHz

The inductor number of turns, N , is increased from 1.25 to 2.75 as shown in Table 4.4. As expected, the inductance value increases from 204pH to 352pH when the spiral has more turns. The self-resonant frequency decreases from 118.5GHz to 79.7GHz because of the increased capacitive coupling between the windings and the increased capacitive coupling to the substrate. The peak Q also decreased from 7.09 to 5.62 with increasing N because of the increased metal loss and the resistance value increases with increasing number of turns, N , from 1.43Ω to 3.05Ω .

Table 4.4: ASITIC simulation Pi model parameter extraction for single layer square spiral inductor, conductor Spacing= $2\mu\text{m}$, outer diameter= $80\mu\text{m}$, Width= $10\mu\text{m}$ and varying number of turns at 8GHz.

Number of Turns	Inductance value	Quality factor	Series Resistance	f_{res}
1.25	0.204 nH	7.09	1.43Ω	118.5GHz
1.5	0.249 nH	7.18	1.7Ω	103.6GHz
1.75	0.279 nH	6.88	1.99Ω	94.3GHz
2.75	0.352 nH	5.62	3.05Ω	79.7GHz

4.8 Silicon Stacked Inductor Characterization in ADS Momentum

Accurate modeling at microwave frequencies require electromagnetic field simulations using ADS Momentum or HFSS EM engines [57] [13].

Layout implementation of single layer inductors designed in ASITIC was imported into Agilent's ADS Momentum using the GDSII format and a double layer inductor was designed in ADS Momentum based on the single. An EM simulation performed on the final layout views for the Stacked inductors including vias and metal interconnects.

ADS Momentum EM simulator was used to characterize the multi-level inductors in order to minimize losses at high frequencies. These results are then incorporated into circuit simulation for optimization purposes. Because EM simulation adds predictive nature to the design process, changes can be made more easily to optimize and fine-tune the layout of the spiral to get the desired inductance value and good Q and self-resonance frequency.

Figure 4.4: Silicon multi-layer on-chip inductor, top metal metal6 and metal5, in Momentum.

Figure 4.5: Characterization of Gate Line OD=80 μ m, W=10 μ m, S=2 μ m, n=1.75, CMOS 0.18 μ m stacked inductor in Momentum.

For accurate results, a fine mesh has to be constructed on the conductor planes of the multi-level inductor layout [72].

The simulated results of the on-chip inductor structure used on the drain transmission line is shown in Figure 4.5, it has 1.75 turns, the spiral inductor width is $10\mu\text{m}$, the spacing between spirals is $2\mu\text{m}$, and the spiral inductor outer diameter is $80\mu\text{m}$. Metal 6 and metal 5 are stacked and connected in series to form a double metal layer on-chip inductor. The two metal layers are connected using vias. The EM simulation takes into account the oxide, substrate, metal layer conductivity and thickness, as well as the spiral geometry.

At low frequencies, the inductance of the stacked inductor is relatively constant at 850pH as depicted in Figure 4.5. However, as the frequency increases, the impedance of the parasitic capacitance elements starts to become more considerable. At 32.7GHz frequency, the admittance of the parasitic elements will cancel that of the inductor and the inductor will self-resonate. Beyond, the self-resonant frequency the parasitic capacitance will dominate and the inductor will look capacitive.

The Q reaches a maximum of 9.6 at 15GHz. This low value Q indicates that the loss effects in the inductor metallization and in the silicon CMOS substrate, along with the parasitic capacitive-coupling effects, have seriously deteriorated the electrical behavior of the stacked on-chip spiral.

4.8.1 Silicon CMOS Substrate Definition in ADS Momentum

To obtain reliable results, EM-based simulation tools such as ADS Momentum or Ansoft HFSS, require an accurate setup of the process parameters, including substrate and metallization characteristics and dielectric information [13].

A $0.18\mu\text{m}$ CMOS silicon substrate was constructed in Momentum, based on the available data from process foundry, with six aluminum metal layers, the top-level metal has a dc sheet resistance of $0.010\Omega/\text{Sq}$ as shown in Figure 4.6 [73].

The on-chip spirals are fabricated on a $733\mu\text{m}$ substrate with a conductivity of 10 S/m [28].

In $0.18\mu\text{m}$ CMOS process, the top metal layer six has the largest thickness, thereby minimizing the DC series resistance of the inductor. The top metal layer is $0.99\mu\text{m}$ thick whereas the lower layers are about $0.53\mu\text{m}$. The intermediate level dielectric thickness is

approximately $1.2\mu\text{m}$ as summarized in Table 4.5.

Table 4.5: CMOS $0.18\mu\text{m}$ process parameters and technology profile.

Parameter	Value
Top Metal 6 resistivity	$0.036 \Omega\text{-}\mu\text{m}$
Metal 5 resistivity	$0.078 \Omega\text{-}\mu\text{m}$
Metal 6 thickness	$0.99\mu\text{m}$
Metal 6 spacing	$0.46\mu\text{m}$
Metal 5 thickness	$0.53\mu\text{m}$
Metal 5 spacing	$0.28\mu\text{m}$
Oxide thickness	$0.35\mu\text{m}$
Substrate resistivity	$10 \Omega\text{-cm}$
Silicon dielectric constant	11.9
Oxide dielectric constant	3.9

Table 4.5 shows three different types of layers, the dielectric layer, where the whole layer is dielectric of uniform dielectric constant, the metal layer, where part of the structure is metal surrounded by dielectric, and the ground plane, where the whole layer is a piece of metal as shown in Figure 4.6.

4.9 Influence of Layout Parameters on CMOS Stacked Inductor Performance

To illustrate the effects of varying different physical parameters on the performance of multi-level square spiral, several inductor parameter variations were made and their effects were studied using Momentum EM-based simulations.

Three CMOS stacked inductors were designed, the first using the top two metal layers with an outer diameter of $70\mu\text{m}$ and the second with outer diameter of $80\mu\text{m}$ and the third with outer diameter of $90\mu\text{m}$.

Figure 4.6: Scheme of cross-section of Silicon CMOS RF 0.18 μ m process substrate layer and interconnect structure definition in Momentum ADS.

The outer diameter, OD, is increased from $70\mu\text{m}$ to $90\mu\text{m}$ as shown in Figure 4.7. The inductance value increases with increasing outer diameter whereas the self-resonant frequency is decreased. Since the parasitic capacitance increases in proportion to the size of the inductor, the f_{res} decreases as the size of the inductor increases. Thus, the size of on-chip inductors that can be built is severely limited. The smaller inductor footprint results in an improved f_{res} .

Figure 4.7: Quality factor and inductance for OD= $70\mu\text{m}$, $80\mu\text{m}$ and $90\mu\text{m}$ ($W=10\mu\text{m}$, $S=2\mu\text{m}$, $n=1.75$) stacked inductor in Momentum. The arrow indicates increasing outer diameter, OD.

The series resistance value increases with increasing outer diameter, OD, from $70\mu\text{m}$ to $90\mu\text{m}$ is shown in Figure 4.8.

The inductor line spacing, S , is increased from $2\mu\text{m}$ to $5\mu\text{m}$ as depicted in Figure 4.9 on page 44. The inductance value decreases with increasing S whereas the self-resonant frequency is increased. Line Spacing could be increased in order to achieve a higher Q .

Figure 4.8: Series resistance for OD=70 μ m, 80 μ m and 90 μ m ($W=10\mu$ m, $S=2\mu$ m, $n=1.75$) stacked inductor in Momentum. The arrow indicates increasing outer diameter, OD.

The series resistance value decreases with increasing line spacing, S , from 2μ m to 5μ m as can be seen in Figure 4.10 on page 45.

The inductor width, W , is increased from 10μ m to 16μ m as depicted in Figure 4.11 on page 46. The inductance value decreases, since the loop area of the inner windings decreases with increasing width where as the self-resonant frequency increases. The peak quality factor decreases as well.

As can be seen in Figure 4.12 on page 47, the series resistance value decreases with increasing line width, W , from 10μ m to 16μ m.

The inductor number of turns, N , is increased from 1.25 to 2.75 as shown in Figure 4.13 on page 48. As expected, the inductance value increases when the spiral has more turns. However, the inductance value does not increase linearly with the number of windings. The self-resonant frequency decreases as N is increased because of the increased capacitive coupling between the windings and the increased capacitive coupling to the substrate. The peak Q also decreases significantly with increasing N because of the increased metal loss.

The series resistance value increases with increasing number of turns, N , from 1.25 to 2.75 as depicted in Figure 4.14 on page 49.

Figure 4.9: Quality factor and inductance for $S=2\mu\text{m}$, $3\mu\text{m}$ and $5\mu\text{m}$ ($W=10\mu\text{m}$, $OD=80\mu\text{m}$, $n=1.75$) stacked inductor in Momentum. The arrow indicates increasing Conductor Spacing, S .

Figure 4.10: Series resistance for $S=2\mu\text{m}$, $3\mu\text{m}$, $4\mu\text{m}$ and $5\mu\text{m}$ ($W=10\mu\text{m}$, $OD=80\mu\text{m}$, $n=1.75$) stacked inductor in Momentum. The arrow indicates increasing conductor spacing, S .

A summary of EM simulation results using Momentum for different inductor parameter variations and their effect on CMOS multi-level inductor performance is shown in Table 4.6.

Table 4.6: Study summary of parameter variation effects on integrated inductor using Momentum EM engine, $\nearrow$ indicates increasing trend and $\searrow$ indicates decreasing trend.

Parameter Effect	Inductance	Quality@peak	f_{res}	Series Resistance
Number of Turns $\nearrow$	$\nearrow$	$\searrow$	$\searrow$	$\nearrow$
Line Width $\nearrow$	$\searrow$	$\searrow$	$\nearrow$	$\searrow$
Outer Diameter $\nearrow$	$\nearrow$	$\searrow$	$\searrow$	$\nearrow$
Line Spacing $\nearrow$	$\searrow$	$\nearrow$	$\nearrow$	$\searrow$
Stacked $\nearrow$	$\nearrow$	$\searrow$	$\searrow$	$\nearrow$

Figure 4.11: Quality factor and inductance for $W=10\mu\text{m}$, $14\mu\text{m}$ and $16\mu\text{m}$ ($S=2\mu\text{m}$, $OD=80\mu\text{m}$, $n=1.75$) stacked inductor in Momentum. The arrow indicates increasing Conductor Width, W .

Figure 4.12: Series resistance for $W=10\mu\text{m}$, $12\mu\text{m}$, $14\mu\text{m}$ and $16\mu\text{m}$ ($S=2\mu\text{m}$, $OD=80\mu\text{m}$, $n=1.75$) stacked inductor in Momentum. The arrow indicates increasing conductor width, W .

4.10 Broadband Silicon RF CMOS Stacked Inductor Equivalent Circuit Model

Accurate on-chip inductor modeling is essential to successful high frequency circuit designs [74]. It is important that a model not only capture all relevant energy loss mechanisms but also accurately represent the equivalent parasitic capacitances such as one shown in Figure 4.15. Inaccurate capacitance modeling leads to poor prediction of the Q and the self-resonance frequency which have a great impact on RF CMOS DA performance [74].

A 2-port double pi broadband equivalent model, proposed by S. J. Pan, shown in Figure 4.16 was used for the CMOS $0.18\mu\text{m}$ stack inductor parameter extraction [61]. Where $L1$ and $L2$ are the self-inductances of the upper and lower spirals in stacked inductor, respectively, and M is the mutual inductance between the two. In our case, the upper and lower spirals are identical $L1 = L2 = L$, and the mutual inductance is $M=k(L1*L2)$, where k denotes the coupling coefficient $0 \leq k \leq 1$ [61]. So the total inductance for double-level cases is approximately $L = L1 + L2 + 2M$ [61].

The parameter extraction was performed for a $W=10\mu\text{m}$, $S=2\mu\text{m}$, $OD=80\mu\text{m}$ and $N=1.75$ stacked spiral inductor. Table 4.7 lists the extracted circuit parameters obtained.

Figure 4.13: Quality factor and inductance for $N=1.25$ and 2.75 ($S=2\mu\text{m}$, $OD=80\mu\text{m}$, $W=10\mu\text{m}$) stacked inductor in Momentum. The arrow indicates increasing number of turns, N .

Figure 4.14: Series resistance for $N=1.25$ and 2.75 ($S=2\mu\text{m}$, $OD=80\mu\text{m}$, $W=10\mu\text{m}$) stacked inductor in Momentum. The arrow indicates increasing number of turns, N .

Figure 4.15: Cross-section of stacked inductor structure with simple equivalent pi model circuit illustration.

Figure 4.16: Lumped-element broadband equivalent circuit model of two-layer spiral inductor on silicon CMOS 0.18 μm substrate.

Table 4.7: Extracted circuit parameters for a $W=10\mu\text{m}$, $S=2\mu\text{m}$, $OD=80\mu\text{m}$ and $N=1.75$ stacked inductor broadband lumped element equivalent model shown in Figure 4.16 implemented in CMOS 0.18 μm process.

Circuit Parameter	Parameter description	Extracted Value
Ls	Series Inductance	295pH
Rs	Series resistance	2.85k Ω
Mutual k	Coupling Coefficient	0.7
Csub1,2,3	Substrate capacitance	32fF
Rsub1,2,3	Substrate resistance	1k Ω
Cox1,2,3	Oxide capacitance	24fF
Cinter1	Interwind capacitance	5fF
Cinter2	Interwind capacitance	2fF

The S-parameter stacked inductor and the equivalent lumped element model were found to be in close agreement using ADS Momentum as shown in Figure 4.17. Markers m1, m24 and m9 show that a lumped element curve fitted quality factor of 6.1 at 6GHz, inductance of 1.1nH at 10GHz and self-resonance frequency at 32.6GHz.

Figure 4.17: Quality factor and inductance for broadband lumped-element stacked inductor Model curve-fitting performance in Momentum. Figure Markers m20 and m23 indicates the Q and L values respectively.

The Q factor of the Momentum simulation at 6Ghz is 6.1 which is quite reasonable for the $0.18\mu\text{m}$ CMOS process. However, since the on-chip inductor parasitics are distributed, the equivalent lumped-element model is not very accurate [73]. Also, it does not model high frequency effects such as substrate currents.

4.11 Stacked Inductor Current Crowding and Skin Effect

Stacked inductor surface current density at 8GHz is shown in Figure 4.18 using ADS Momentum.

Figure 4.18: Magnetic currents are plotted along with crowding current effect in corners of stacked square inductor at 8GHz.

Current crowding can be observed at higher frequencies in Figure 4.18, where current tends to increase on the edges of the inductor lines which in turn has a negative effect on both the spiral Q and the series resistance [75]. Note, that the current crowding appears to increase towards the center of the spiral coil.

4.12 Chapter Summary

In this chapter, the design and optimization of multi-level on-chip CMOS inductor was presented.

A study of the effects of varying different physical parameters on the performance of

multi-level CMOS square spiral was discussed. A lumped-element broadband equivalent circuit model of two-layer spiral inductor on silicon CMOS $0.18\mu\text{m}$ substrate was also presented.

Chapter 5

Silicon RF CMOS Linearized DA Design Considerations

5.1 Introduction

The role of distributed amplification in communication systems is not only in amplifying the weak RF signal without adding much noise but also maintaining linear operation when receiving weak signal in the presence of a strong interference [6].

Amplifiers must maintain ultra linear transfer functions to achieve spectrally efficient operation [76]. Feed-forward and Multi-Tanh CMOS distributed amplifier architectures capable of ultra linear operation are illustrated, compared and analyzed.

The linearization techniques described in this chapter have occasionally been utilized in complex, expensive RF and microwave systems, but they have not yet found their way into low-cost portable terminals [40] [77].

5.2 CMOS Distributed Amplifier Design Consideration

The design of two linearized CMOS distributed amplifiers will be discussed in detail. The first amplifier employs a Feedforward gain cell. The second distributed amplifier is based on the Multi-Tanh principle.

A distributed integrated circuit design is an effective approach for the design of optical communication ultra wideband circuits, particularly in CMOS technology [8] [20]. The

linearized distributed amplifiers were designed to meet the specifications shown in Table 5.1. All simulations were carried out using a $0.18\mu\text{m}$ CMOS process technology.

Table 5.1: Targeted DA design specifications

Technology	CMOS $0.18\mu\text{m}$
Frequency range	0.5 - 10GHz
S21 Power Gain $\pm$ Ripple	10dB $\pm$ 2
IIP3 Output power	10dBm
1dB Output power	0dBm
S11 and S22 return loss	< -10dB
S12 Isolation	< -25dB
IMD3 Intermodulation	< -40dB
Group Delay	< 50ps
NF at max. Gain	5dB
Power Consumption	100mW
Silicon area	2mm X 1mm

5.3 Fully-Differential CMOS DA Topology

The artificial transmission lines of the single-ended distributed amplifier have been replaced with a pair of transmission lines for each gate and drain line [12].

The topology of a fully-differential DA is depicted in Figure 5.1. It consists of four differential gain stages with a constant current source for each amplifier.

The usefulness of differential-pair stems from two key properties: (i) differential designs suppress substrate noise; (ii) the diff-pair is primarily sensitive to the difference between two input voltages, allowing a high degree of rejection of signals common to both inputs [12].

Figure 5.1: Fully-differential CMOS DA topology.

5.4 CMOS Transistor Selection

The next step is the choice of appropriate device size. Each multi-fingered device of the transconductance stage in the DA contains 32 fingers. Each finger has $0.18\mu\text{m}$ of channel length and $5\mu\text{m}$ of channel width for a total gate width of $160\mu\text{m}$.

The transistor size has been chosen for high-speed operation with relatively large current operation. A multiple-finger device structure has been used to reduce the input capacitance and the gate resistance [12].

A higher gain can be achieved by increasing the device size, that is increasing g_m . However, increasing device size increases capacitance which in turns lowers bandwidth as is depicted in Figure 5.2.

The width of all the CMOS DA gain cell transistors are chosen to be the same. Since a twice as large g_m will be required to produce the same gain as in the corresponding single-ended circuit, a $0.18\mu\text{m}$ length and a $160\mu\text{m}$ width was chosen as device size.

Figure 5.2: Simulated Gain S21 versus frequency performance for different CMOS device dimensions.

5.5 Cascode Configuration Design

The amplifier cell is based on a broadband cascode architecture. The cascode topology is widely used in DAs to obtain better reverse isolation [57].

The cascode eliminates the bandwidth degradation due to the Miller capacitance of the common-source stage's gate-drain capacitance. This degradation is particularly significant in CMOS circuits, where the gate-drain capacitance can be as high as one-third of the gate-source capacitance. The cascode also enhances the overall gain by increasing the stage's output impedance [57].

In many applications it is desirable to be able to produce a large output resistance and low output conductance at the drain of the MOSFET [33]. The cascode configuration is important mostly because it increases output resistance and reduces unwanted capacitive feedback in amplifiers, allowing operation at higher frequencies than otherwise possible [78].

5.6 M-derived Half Section Image Impedance

In order to improve the impedance match of the 50Ω termination resistor to the input artificial transmission line, an m-derived half section used as a buffer stage has been inserted as well. It has been shown through simulations that using m values near 0.66 provides near optimal results [56].

The values of the m-derived section L and C components, depicted in Figure 5.3, can be determined as follows [56]

$$L_1 = \frac{m}{2} L \quad (5.6.1)$$

$$L_{gp} = \frac{(1 - m^2)}{2m} L_g = 0.66 L_g \quad (5.6.2)$$

$$C_{gp} = \frac{m}{2} C_g = 0.33 C_g \quad (5.6.3)$$

Solving these equations gives $L_{gp}=600\text{pH}$ and $C_{gp}=150\text{fF}$.

Figure 5.3: M-Derived matching networks for differential CMOS DA matching of the resistive termination.

This technique also reduces a large undesirable peak in the gain response near the cutoff frequency and improves the gain-flatness of the amplifier [56] [33].

Table 5.2: M-derived matching networks component values.

M-derived components	drain network	gate network
L1	1.15nH	915pH
L2	687pH	608pH
C1	200fF	240fF

5.7 Voltage Headroom Performance Limitation in Silicon CMOS DA

The performance of CMOS distributed amplifiers is constrained by numerous effects. One main problem, is that the supply voltage places an upper bound on the number of the gain stages [57] [79] and hence the achievable voltage gain as illustrated in Figure 5.4.

The bias current of all of the stages flow through the same loads, the circuit suffers from a severe trade-off between voltage gain and voltage headroom [57] [79].

5.8 Analytical CMOS DA Design Approach

The CMOS DA transmission lines are formed using lumped inductors and are referred to as the gate and drain lines. The first step of the DA design of the input transmission line is to determine the L and C values.

The bandwidth of a distributed amplifier is limited by the cutoff frequency of the artificial transmission line formed for both the input and the output of the transistor [50].

The cut-off frequency f_c of a lossless transmission line is given by [50]

$$f_c = \frac{1}{\pi \sqrt{L_g C_g}} \quad (5.8.1)$$

Due to the differential nature of the complementary inputs, the line impedance of the

Figure 5.4: Voltage headroom performance limitation of Silicon CMOS DA.

differential circuit should be equal to half of the desired input impedance that is 50Ω and each of the gate line impedance has to be set to 25Ω [12].

The transmission line characteristic impedance, Z_o , of the gate and drain are designed for 25Ω in order to match the differential impedance of 50Ω :

$$Z_o = \sqrt{\frac{L_g}{C_g}} = 25\Omega \quad (5.8.2)$$

Setting a target for the line cutoff frequency to be 12GHz , the required inductance and capacitance values are:

$$f_c = 12\text{GHz} = \frac{1}{\pi\sqrt{L_g C_g}} \quad (5.8.3)$$

The inductance and capacitance values for the gate lines can be determined using the specified cutoff frequency and line characteristic impedance equation as:

$$L_g = (25\Omega)^2 C_g \quad (5.8.4)$$

We know that f_H is equal to 0.86 times the cutoff frequency f_c [50]

$$f_H = 0.86 \times f_c \quad (5.8.5)$$

$$f_H = 0.86 \left(\frac{1}{\pi \times Z_o \times C_g} \right) \quad (5.8.6)$$

$$C_g = 0.86 \left(\frac{1}{\pi \times 25 \times 12 \times 10^9} \right) \quad (5.8.7)$$

$$C_g \approx 1pF \quad (5.8.8)$$

For differential circuit C_{gs} is equal to twice of C_g capacitance:

$$C_{gs} \approx 2pF \quad (5.8.9)$$

$$Lg = Z_o^2 \times C_g = (25)^2 \times 1pF \approx 625pH \quad (5.8.10)$$

After adjusting the sizes of the transistors and passive components to meet the specification, the parameters obtained above are slightly modified due to circuit performance optimization.

Now, the gate area of the transistors is estimated using the above results.

The transistor width can be estimated using equation 5.8.11

$$C_{gs} = W \cdot L \cdot C_{ox} \quad (5.8.11)$$

Where C_{ox} is the oxide capacitance per unit area. W and L are the width and length of the MOSFET. C_{ox} is fixed for a given technology and L is fixed considering minimum length devices. Therefore, C_{gs} can be approximated by,

$$C_{gs} \cong \frac{2}{3} C_{ox} \cdot W \cdot L \quad (5.8.12)$$

Twice larger g_m will be required to produce the same gain as in the corresponding single-ended circuit [12].

The device transconductance can be approximated by equation 5.8.13,

$$g_m = \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{gs} - V_T) \quad (5.8.13)$$

The lossless power gain can be approximated as [12] [50],

$$G = \frac{N^2 g_m^2 Z_o^2}{4} \quad (5.8.14)$$

For target gain of 10dB, and a calculated g_m of 31mS the number of stages can be approximated by,

$$N^2 = \frac{4G}{gm^2 Z_o^2} \quad (5.8.15)$$

$$N = \frac{2\sqrt{10}}{(0.031)(50)} = 3.61 \quad (5.8.16)$$

Since we have to account for losses and parasitics, N is chosen to be:

$$N = 4 \quad (5.8.17)$$

L_g and L_d are chosen to be close to each other so that phase velocities can be equalized.

For a higher cutoff frequency of the DA, a lower effective inductance is desirable. The drain inductance line value L_d is given by [50]

$$L_d = Z_o^2 \times C_d \quad (5.8.18)$$

$$L_d = (25)^2 \times C_d \quad (5.8.19)$$

5.9 Optimum Number of Gain Stages

The number of distributed amplification stages is limited as the series parasitic resistance and shunt capacitance become large, and the more inductors needed will consume more chip area [50].

Circuit analysis and simulations led to the number of stages that brings the best gain-bandwidth performance to 4 which agrees with analytical calculation.

Figure 5.5: Simulated Gain S21 versus frequency performance for different number of CMOS DA gain stages.

The simulation results of increasing the number of gain cell stages in the amplifier and its effect is depicted in Figure 5.5. It can be seen that if we increase the number of gain cell stages, the S21 power gain increases in the lower frequency limit, but the bandwidth is simultaneously reduced.

By cascading more stages, the lost gain can be compensated. The loss of the transmission lines in CMOS limits the length of the line, the number of sections, and ultimately the gain that can be achieved [50].

5.10 Fully-Differential Feedforward CMOS Distributed Amplifier Design

In 1927, H.S. Black of Bell Telephone Laboratories invented the concept of feedforward as a method of linearizing amplifiers [41]. His idea for feedforward was simple: reduce the

amplifier output to the same level as the input and subtract one from the other to leave only the distortion generated by the amplifier. Amplify the distortion with a separate amplifier and then subtract it from the original amplifier output to leave only a linearly amplified version of the input signal. The feedforward configuration consists of two circuits, the signal cancellation circuit and the error cancellation circuit [36].

5.11 Feedforward “Cascomp” Gain Cell

In order to obtain an improved CMOS transconductor linearity, a Feedforward stage is used [80].

Feedforward distortion cancellation is a technique suitable for IC design. One of the most common structures for wideband feedforward compensation is the cascode compensator network [80]. A gain cell employing a Feedforward distortion cancellation scheme is shown in Figure 5.7. An example of Feedforward correction applied to a transconductor is an adaptation of Pat Quinn’s bipolar “cascomp” circuit [80] is depicted in Figure 5.7. As can be seen, this transconductor consist of a cascode differential pair plus cross-coupled differential pair to compensate for distortion.

The goal is to have a differential output current exactly proportional to the differential input voltage v_{in} . The name “cascomp” derived from the combination of a cascode and error compensation [80].

The additional cross-coupled differential pair, which can be linearized as well, measures the nonlinearity of the cascode pair and adds a canceling term to the output current [80].

For a linear circuit the output ΔI_{out} should be exactly proportional to the input voltage V_{in} . However for a differential pair with degenerated resistor, R , as shown in Figure 5.7:

$$\Delta I_{out} = \frac{V_R}{R} = \frac{\Delta V_{in} - (V_{gs1} - V_{gs2})}{R} = \frac{\Delta V_{in} - \Delta V_{gs}}{R} \quad (5.11.1)$$

where ΔI_{out} is not proportional to the input differential voltage V_{in} .

The output current of the cross-coupled differential pair injected into the drain of M3 and M4 is expressed as,

$$\Delta I_{gm} = G_m[(V_{BIAS} - V_{gs4}) - (V_{BIAS} - V_{gs3})] = G_m \Delta V_{gs} = \frac{\Delta V_{gs}}{R} \quad (5.11.2)$$

Figure 5.6: A fully-differential Linearized CMOS Feedforward distributed amplifier.

Figure 5.7: Feedforward “cascomp” gain cell topology

When the additional current ΔI_{gm} is taken into account, the new overall differential output current $\Delta I'_{out}$ becomes proportional to V_{in} ,

$$\Delta I'_{out} = \Delta I_{out} + \Delta I_{gm} = \frac{\Delta V_{in} - \Delta V_{gs}}{R} + \frac{\Delta V_{gs}}{R} = \frac{\Delta V_{in}}{R} \quad (5.11.3)$$

where $\Delta I_{out'}$ is proportional to the input differential voltage V_{in} .

A fully-differential Feedforward CMOS DA topology is shown in Figure 5.8. It consists of four differential gain stages with a constant current source for each amplifier [81].

A transconductance plot of the proposed linearized Feedforward CMOS distributed amplifier is depicted in Figure 5.9. The horizontal axis is the differential input voltage, and the vertical axis is the normalized transconductance. The g_m curves become flatter over a wider input range as can be seen in Figure 5.9 by tuning the Feedforward gain cell error amplifier bias tail current from 2.5mA to 0.5mA.

The transconductance first order derivative, IMD2, of the linearized Feedforward CMOS distributed amplifier is depicted in Figure 5.10. The horizontal axis is the differential input voltage, and the vertical axis is the normalized transconductance first derivative. The

Figure 5.8: Linearized CMOS DA based on Feedforward Gain Cell Topology.

IMD2 is tuned by decreasing the Feedforward gain cell error amplifier bias tail current from 2.5mA to 0.5mA as can be seen in Figure 5.10.

The second order derivative transconductance, IMD3, of the linearized CMOS Feedforward distributed amplifier is shown in Figure 5.11. The horizontal axis is the differential input voltage, and the vertical axis is the normalized transconductance second order derivative. The IMD3 decreases as can be seen in Figure 5.11 by tuning the Feedforward gain cell error amplifier bias tail current from 2.5mA to 0.5mA.

The linearized CMOS Feedforward DA simulated S21 forward gain peaks at 8dB with unity gain bandwidth of 10.8GHz is depicted in Figure 5.12. Using m-derived matching networks, S11 and S22 stay below -5dB up to 10.5GHz with reverse isolation is better than -23dB.

The output simulated frequency spectrum of the linearized Feedforward CMOS DA circuit with a two-tone test signal as input is shown in Figure 5.13. The innermost spectral lines are the fundamental tones of the two-tone test at frequencies f_1 and f_2 and the outermost spectral lines are third order distortion products.

Figure 5.9: Simulated Taylor coefficient g_m versus input voltage, the g_m curves become flatter over a wider input range by tuning the Feedforward gain cell error amplifier bias tail current from 2.5mA to 0.5mA.

Figure 5.10: Simulated Taylor coefficient, IMD2, g_m first order derivative, versus input voltage, the IMD2 is tuned by decreasing the Feedforward gain cell error amplifier bias tail current from 2.5mA to 0.5mA.

Figure 5.11: Simulated Taylor coefficient, IMD3, g_m second order derivative versus input voltage. The IMD3 decreases by tuning the Feedforward gain cell error amplifier bias tail current from 2.5mA to 0.5mA.

Figure 5.12: Simulated linearized Feedforward CMOS DA S-parameters, S21 forward gain peaks at 8dB with unity gain bandwidth of 10.8GHz, S11 and S22 stay below -5dB up to 10.5GHz with reverse isolation better than -23dB.

The difference ΔP equals $P_{out} - P_{IMD3}$. P_{out} is the output power level of the fundamental frequency, and P_{IMD3} is equal to the power level of the third order intermodulation product.

A practical approximation for calculation of IIP3 can be found with expression [35]:

$$IIP3_{dBm} = \frac{P_{OUT} - P_{IMD3}}{2} + P_{in} \quad (5.11.4)$$

Before IMD3 cancellation is applied, by tuning the Feedforward gain cell error amplifier bias tail current to 1.25mA, the simulated IMD3 is at -41.23dBm power level as shown in Figure 5.13. P_{in} was taken at -18.2dBm power level with fundamental component at 5.5GHz and 5.55GHz.

Figure 5.13: Simulated output frequency spectrum with fundamental component at 5.5GHz and 5.55GHz and with IMD3 at 5.45GHz and 5.6GHz with -41.23dBm power level and with $P_{in} = -18.2\text{dBm}$ before 3rd order distortion cancellation effect is applied by tuning the Feedforward gain cell error amplifier bias tail current to 1.25mA.

Before IMD3 cancellation is applied, by tuning the Feedforward gain cell error amplifier bias tail current to 1.25mA, the simulated IIP3 is 2.41dBm power level as shown in Figure 5.14. P_{in} was swept from -45dBm to 20dBm power level with fundamental frequency components at 5.5GHz and 5.55GHz.

By tuning the Feedforward gain cell error amplifier bias tail current to 0.25mA, with

Figure 5.14: Simulated IIP3 with power level 2.41dBm input referred third order intercept point at 5.5GHz and with Pin swept from -45dBm to 20dBm before 3rd order distortion cancellation effect is applied by tuning the Feedforward gain cell error amplifier bias tail current to 1.25mA.

fundamental component at 5.5GHz and 5.55GHz, the IMD3 is reduced to -53.52dBm power level as depicted in Figure 5.15. A comparison of Figure 5.13 and Figure 5.15 shows that IMD3 is improved by approximately 12.29dB, from -41.23dBm to -53.52dBm at 5.45GHz.

Figure 5.15: Simulated output frequency spectrum with fundamental component at 5.5GHz and 5.55GHz and with IMD3 at 5.45GHz and 5.6GHz with -53.52dBm power level and with $P_{in} = -18.2$ dBm after 3rd order distortion cancellation effect is applied by tuning the Feedforward gain cell error amplifier bias tail current to 0.25mA.

By tuning the Feedforward gain cell error amplifier bias tail current to 0.25mA, with fundamental component at 5.5GHz and 5.55GHz, the IIP3 have increased to -53.52dBm power level as depicted in Figure 5.16. A comparison of Figure 5.14 and Figure 5.16 shows that IIP3 is improved by approximately 6.15dB, from 2.41dBm to 8.56dBm.

Before IMD3 cancellation is applied, by tuning the Feedforward gain cell error amplifier bias tail current to 1.25mA, the simulated IMD3 is at -55.56dBm power level as shown in Figure 5.17. P_{in} was taken at -18.2dBm power level with fundamental frequency components at 1.5GHz and 1.55GHz.

Before IMD3 cancellation is applied, by tuning the Feedforward gain cell error amplifier bias tail current to 1.25mA, the simulated IIP3 is 9.58dBm power level as shown in Figure 5.18. P_{in} was swept from -45dBm to 20dBm power level with fundamental frequency components at 1.5GHz and 1.55GHz.

Figure 5.16: Simulated IIP3 with power level 8.56dBm input referred third order intercept point at 5.5GHz and with Pin swept from -45dBm to 20dBm after 3rd order distortion cancellation effect is applied by tuning the Feedforward gain cell error amplifier bias tail current to 0.25mA.

Figure 5.17: Simulated output frequency spectrum with fundamental component at 1.5GHz and 1.55GHz and with IMD3 at 1.45GHz and 1.6GHz with -55.56dBm power level and with Pin=-18.2dBm before 3rd order distortion cancellation effect is applied by tuning the Feedforward gain cell error amplifier bias tail current to 1.25mA.

Figure 5.18: Simulated IIP3 with power level 9.58dBm input referred third order intercept point at 1.5GHz and with Pin swept from -45dBm to 20dBm before 3rd order distortion cancellation effect is applied by tuning the Feedforward gain cell error amplifier bias tail current to 1.25mA.

By tuning the Feedforward gain cell error amplifier bias tail current to 0.25mA, with fundamental component at 1.5GHz and 1.55GHz, the IMD3 is reduced to -61.53dBm power level as depicted in Figure 5.19. A comparison of Figure 5.17 and Figure 5.19 shows that IMD3 is improved by approximately 5.97dB, from -55.56dBm to -61.53dBm at 1.45GHz.

By tuning the Feedforward gain cell error amplifier bias tail current to 0.25mA, with fundamental component at 1.5GHz and 1.55GHz, the IIP3 have increased to 12.56dBm power level as depicted in Figure 5.20. A comparison of Figure 5.18 and Figure 5.20 shows that IIP3 is improved by approximately 2.98dB, from 9.58dBm to 12.56dBm.

5.12 Proposed Linearized CMOS DA Based on Multi-Tanh Principle

Linearity can be improved using the Multi-Tanh technique pioneered by B. Gilbert [32]. It flattens the transconductance G_m of the gain stage. Thus, the linearity is greatly improved. It is based on biasing the FET differential pair at the gate-source voltage at which the 3rd-order derivative of its dc transfer characteristic is zero as shown in Figure 5.21. Such

Figure 5.19: Simulated output frequency spectrum with fundamental component at 1.5GHz and 1.55GHz and with IMD3 at 1.45GHz and 1.6GHz with -61.53dBm power level and with $P_{in} = -18.2 \text{ dBm}$ after 3rd order distortion cancellation effect is applied by tuning the Feedforward gain cell error amplifier bias tail current to 0.25mA.

Figure 5.20: Simulated IIP3 with power level 12.56dBm input referred third order intercept point at 1.5GHz and with P_{in} swept from -45dBm to 20dBm after 3rd order distortion cancellation effect is applied by tuning the Feedforward gain cell error amplifier bias tail current to 0.25mA.

biasing causes an IMD3 nulling.

Source degeneration is just one option for extending the linear range of the differential pair; there are however some other options [82]. The other approach is based on Multi-Tanh, multiple diff pairs, approach. It achieves reductions in distortion through the use of a multiplicity of tanh functions.

The distortion cancellation is achieved by connecting two devices, diff pairs, in parallel and biasing them in different regions of their transfer characteristics, in which the signs of the 3rd-order derivative are opposite [83]. With the proper device biasing, the composite 3rd-order derivative can be made zero for an extended range of biases as can be seen in Figure 5.21.

Figure 5.21: Multi-Tanh CMOS gain cell topology.

The proposed CMOS DA linearization method is illustrated in a simple architecture shown in Figure 5.22. The Multi-Tanh linearized CMOS distributed amplifier is comprised of two differential pairs connected in parallel.

The linearized CMOS DA gain cells invoke a well-developed concept known as the Multi-Tanh principle [32]. The main idea is that the individually nonlinear hyperbolic tangent

transconductance functions may be separated along the input-voltage axis to attain a much more linear overall function. The overall transconductance is the sum of the individual offset transconductances.

The technique proposed here to improve linearity is easily applied to traveling wave amplifier designs without sacrificing significant power, noise or gain performance. This technique makes use of the hyperbolic tangent characteristics of a current bias differential pair [32].

The major element is a couple of differential pairs connected in parallel scaled with gate voltage offset V_{off} . Each pair is given an appropriate input offset voltage value in such a way that the combined input-output characteristic of those pairs in parallel has a flatter slope [33].

Shown in Figure 5.22, the differential pair formed of M1 and M2 can be viewed as the main amplifier, whereas the pair formed of M3 and M4 is an auxiliary amplifier, whose purpose is to cancel IMD3 of the main amplifier.

Figure 5.22: Proposed Linearized CMOS DA Based on Multi-Tanh Gain Cell Topology.

This topology has three artificial transmission lines, drain, gate and auxiliary gate line.

The trade off is an increase in power dissipation and input capacitance, which in turn impacts the DA's bandwidth performance.

A detailed schematic of the CMOS DA linearization technique is depicted in Figure 5.23.

On-chip tuning is an important aspect of the proposed linearized CMOS DA design. IMD3 cancellation tuning can be achieved by changing the gate bias voltage of the gain cells, shown in Figure 5.23, proportionally.

5.13 Multi-Tanh CMOS DA Simulation Results

A number of simulations, results presented in this section, were conducted to investigate the behavior of the proposed CMOS DA topology.

The amplifier is designed in a $0.18\mu\text{m}$ CMOS technology and simulated using 2.3V supply. Higher supply voltage is used to increase the gain of each stage without being constrained by voltage headroom.

Simulated gain peaks at 11dB and using m-derived matching networks, S11 and S22 stay below -10dB up to 15GHz and reverse isolation better than -23dB is depicted in Figure 5.24.

Simulated noise figure of 3.8dB at 6GHz is shown in Figure 5.25. The noise figure grows monotonically out of the 15.5GHz unity gain bandwidth range when DA attenuation increases.

5.14 Multi-Tanh CMOS DA Layout-based Simulation Results

After the schematic simulation results meet the desired specifications, the next step is to perform a series of simulations based on the DA layout.

The parasitic effects of the layout geometry are crucial in the design of the high-speed distributed circuits. Thus, all simulations contain a complete set of parasitic elements extracted from the layout of the linearized DA.

Post-layout of simulated S21 gain peaks at 8dB using m-derived matching networks and Cadence on-chip passive component modeler as shown in Figure 5.26. The results

Figure 5.23: Schematic of Linearized CMOS DA Based on Multi-Tanh Gain Cell.

Figure 5.24: Simulated Multi-Tanh CMOS DA S-parameters.

Figure 5.25: Simulated Multi-Tanh CMOS DA Noise Figure.

show that S11 and S22 stay below -6dB up to 14GHz and the reverse isolation is better than -30dB.

Figure 5.26: Post-layout Multi-Tanh CMOS DA S-parameters using cadence on-chip passive component modeler.

Using both Cadence on-chip passive component modeler and Agilent ADS Momentum pi model, the Multi-Tanh CMOS DA simulated and post-layout S21 forward gain is depicted in Figure 5.27.

Post-layout simulated S21 forward gain is shown in Figure 5.28 for different drain bias voltage supply values. An increase in gain is observed with an increase in drain bias. This may be explained by the fact that the higher drain bias voltage causes higher output resistance R_{ds} of the MOSFET. Thus, the overall gain is increased through the reduction of the drain line losses.

Stability Rollet's factor K is shown in Figure 5.29. We see that K is always higher than unity over the bandwidth of operation up to 15GHz, assuring unconditional stability for the distributed amplifier [69].

Figure 5.27: Post-layout and simulated Multi-Tanh CMOS DA S21-parameters comparison using both cadence on-chip passive component modeler and ADS pi model.

Figure 5.28: Post-layout simulation of Multi-Tanh CMOS DA S21-parameters comparison applying different VDD voltage supply.

Figure 5.29: Post-layout simulation of Multi-Tanh CMOS DA K_f and B_{1f} stability performance.

5.15 Multi-Tanh CMOS DA Time Domain Simulation Results with Impulse Input

To assess the performance of the linearized Multi-Tanh CMOS DA and its suitability for UWB applications, post-layout simulation have been conducted in the time domain as well.

Multi-Tanh CMOS DA post-layout simulation with input step response of 100mV amplitude and 100ps rise time is depicted in Figure 5.30. The output mono-cycle pulse is distorted as expected due to the fact that the amplifier does not pass the low-frequency and DC components of the input impulse.

The full scale post-layout simulation of Multi-Tanh CMOS DA with input step response with 100mV amplitude and 100ps rise time is shown in Figure 5.31. The results show that the linearized CMOS DA is free from oscillations.

The Multi-Tanh CMOS DA post-layout simulation with input voltage swing applied with signal level of 400mV peak-peak at 5.5GHz is shown in Figure 5.32. Where as, the output voltage swing with signal level of 1.29V peak-peak resulting in 5.11dB output power

Figure 5.30: Post-layout simulation of Multi-Tanh CMOS DA with input step response with 100mV amplitude and 100ps rise time, zoomed in.

Figure 5.31: Post-layout simulation of Multi-Tanh CMOS DA with input step response with 100mV amplitude and 100ps rise time, zoomed out.

at 5.5GHz can be seen in Figure 5.33.

Figure 5.32: Post-layout simulation of Multi-Tanh CMOS DA with input voltage swing applied with signal level of 400mV peak-peak at 5.5GHz.

5.16 Multi-Tanh CMOS DA IMD3 Cancellation and Power Harmonics Simulation Results

The circuit was simulated with a two-tone test at closely spaced frequencies. The bias voltages at the gates of differential pair gain cells were changed by modifying the gate transmission line bias voltages.

Before IMD3 cancellation is applied, by tuning the Multi-Tanh gain cell auxiliary gate bias voltage to 1.3V, the simulated IMD3 is at -51.14dBm power level as shown in Figure 5.34. Pin was taken at -18.2dBm power level with fundamental component at 5.5GHz and 5.55GHz.

Before IMD3 cancellation is applied, by tuning the Multi-Tanh gain cell auxiliary gate bias voltage to 1.3V, the simulated IIP3 is 7.5dBm power level as depicted in Figure 5.35. Pin was swept from -45dBm to 20dBm power level with fundamental frequency components

Figure 5.33: Post-layout simulation of Multi-Tanh CMOS DA with output voltage swing with signal level of 1.29V peak-peak resulting in 5.11dB output power at 5.5GHz.

Figure 5.34: Simulated output frequency spectrum with fundamental component at 5.5GHz and 5.55GHz and with IMD3 at 5.45GHz and 5.6GHz with -51.14dBm power level and with $P_{in} = -18.2\text{dBm}$ before 3rd order distortion cancellation effect is applied by tuning the Multi-Tanh gain cell auxiliary gate bias voltage to 1.3V.

at 5.5GHz and 5.55GHz.

Figure 5.35: Simulated IIP3 with power level 7.5dBm input referred third order intercept point and with Pin swept from -45dBm to 20dBm before 3rd order distortion cancellation effect is applied by tuning the Multi-Tanh gain cell auxiliary gate bias voltage to 1.3V.

Before IMD3 cancellation is applied, by tuning the Multi-Tanh gain cell auxiliary gate bias voltage to 1.3V, the simulated 1dB compression point is 2.7dBm power level as depicted in Figure 5.36. Pin was swept from -45dBm to 20dBm power level with fundamental frequency components at 5.5GHz and 5.55GHz.

By tuning the Multi-Tanh gain cell auxiliary gate bias voltage to 0.6V, with fundamental component at 5.5GHz and 5.55GHz, the IMD3 is reduced to -58.74dBm power level as depicted in Figure 5.37. A comparison of Figure 5.34 and Figure 5.37 shows that IMD3 is improved by approximately 7.6dB, from -51.14dBm to -58.74dBm at 5.45GHz.

By tuning the Multi-Tanh gain cell auxiliary gate bias voltage to 0.6V, with fundamental component at 5.5GHz and 5.55GHz, the simulated IIP3 has increased to 11.17dBm power level as depicted in Figure 5.38. A comparison of Figure 5.35 and Figure 5.38 shows that IIP3 is improved by approximately 3.6dB, from 7.5dBm to 11.17dBm.

Figure 5.36: Simulated 1dB compression point with input power level -2.94dBm and with 1dB output power 2.7dBm before 3rd order distortion cancellation effect is applied by tuning the Multi-Tanh gain cell auxiliary gate bias voltage to 1.3V.

Figure 5.37: Simulated output frequency spectrum with fundamental component at 5.5GHz and 5.55GHz and with IMD3 at 5.45GHz and 5.6GHz with -58.74dBm power level and with $P_{in} = -18.2$ dBm after 3rd order distortion cancellation effect is applied by tuning the Multi-Tanh gain cell auxiliary gate bias voltage to 0.6V.

Figure 5.38: Simulated IIP3 with power level 11.17dBm input referred third order intercept point and with Pin swept from -45dBm to 20dBm after 3rd order distortion cancellation effect is applied by tuning the Multi-Tanh gain cell auxiliary gate bias voltage to 0.6V.

By tuning the Multi-Tanh gain cell auxiliary gate bias voltage to 0.6V, with fundamental component at 5.5GHz and 5.55GHz, the simulated 1dB compression point has increased to 1.5dBm power level as shown in Figure 5.39. A comparison of Figure 5.36 and Figure 5.39 shows that IIP3 is improved by approximately 4.4dB, from -2.94dBm to 1.5dBm.

Before IMD3 cancellation is applied, by tuning the Multi-Tanh gain cell auxiliary gate bias voltage to 1.3V, the simulated IMD3 is at -51.26dBm power level as shown in Figure 5.40. Pin was taken at -18.2dBm power level with fundamental component at 1.5GHz and 1.55GHz.

Before IMD3 cancellation is applied, by tuning the Multi-Tanh gain cell auxiliary gate bias voltage to 1.3V, the simulated IIP3 is 7.43dBm power level as depicted in Figure 5.41. Pin was swept from -45dBm to 20dBm power level with fundamental frequency components at 1.5GHz and 1.55GHz.

Before IMD3 cancellation is applied, by tuning the Multi-Tanh gain cell auxiliary gate

Figure 5.39: Simulated 1dB compression point with input power level 1.5dBm and with 1dB output power 6.7dBm after 3rd order distortion cancellation effect is applied by tuning the Multi-Tanh gain cell auxiliary gate bias voltage to 0.6V.

Figure 5.40: Simulated output frequency spectrum with fundamental component at 1.5GHz and 1.55GHz and with IMD3 at 1.45GHz and 1.6GHz with -51.26dBm power level and with $P_{in} = -18.2\text{dBm}$ before 3rd order distortion cancellation effect is applied by tuning the Multi-Tanh gain cell auxiliary gate bias voltage to 1.3V.

Figure 5.41: Simulated IIP3 with power level 7.43dBm input referred third order intercept point and with Pin swept from -45dBm to 20dBm before 3rd order distortion cancellation effect is applied by tuning the Multi-Tanh gain cell auxiliary gate bias voltage to 1.3V.

bias voltage to 1.3V, the simulated 1dB compression point is 3dBm power level as depicted in Figure 5.42. Pin was swept from -45dBm to 20dBm power level with fundamental frequency components at 1.5GHz and 1.55GHz.

By tuning the Multi-Tanh gain cell auxiliary gate bias voltage to 0.6V, with fundamental component at 1.5GHz and 1.55GHz, the simulated IMD3 is reduced to -55.69dBm power level as depicted in Figure 5.43. A comparison of Figure 5.40 and Figure 5.43 shows that IMD3 is improved by approximately 4.43dB, from -51.26dBm to -55.69dBm at 1.45GHz.

By tuning the Multi-Tanh gain cell auxiliary gate bias voltage to 0.6V, with fundamental component at 1.5GHz and 1.55GHz, the simulated IIP3 has increased to 9.64dBm power level as depicted in Figure 5.44. A comparison of Figure 5.41 and Figure 5.44 shows that IIP3 is improved by approximately 2.21dB, from 7.43dBm to 9.64dBm.

By tuning the Multi-Tanh gain cell auxiliary gate bias voltage to 0.6V, with fundamental component at 1.5GHz and 1.55GHz, the simulated 1dB compression point has increased to 6dBm power level as shown in Figure 5.45. A comparison of Figure 5.42 and Figure 5.45

Figure 5.42: Simulated 1dB compression point with input power level -2.5dBm and with 1dB output power 3dBm before 3rd order distortion cancellation effect is applied by tuning the Multi-Tanh gain cell auxiliary gate bias voltage to 1.3V.

Figure 5.43: Simulated output frequency spectrum with fundamental component at 1.5GHz and 1.55GHz and with IMD3 at 1.45GHz and 1.6GHz with -55.69dBm power level and with $P_{in} = -18.2\text{dBm}$ after 3rd order distortion cancellation effect is applied by tuning the Multi-Tanh gain cell auxiliary gate bias voltage to 0.6V.

Figure 5.44: Simulated IIP3 with power level 9.64dBm input referred third order intercept point and with Pin swept from -45dBm to 20dBm after 3rd order distortion cancellation effect is applied by tuning the Multi-Tanh gain cell auxiliary gate bias voltage to 0.6V.

Figure 5.45: Simulated 1dB compression point with input power level 0dBm and with 1dB output power 6dBm after 3rd order distortion cancellation effect is applied by tuning the Multi-Tanh gain cell auxiliary gate bias voltage to 0.6V.

shows that IIP3 is improved by approximately 2.5dB, from -2.5dBm to 0dBm.

5.17 Multi-Tanh CMOS DA Simulation Results Summary

Table 5.3 indicates IIP3 and IMD3 performance levels achieved in the linearized CMOS DA with both Feedforward and Multi-Tanh techniques. The described simulated results will be compared to future measured results in Chapter 7.

Table 5.3: Feedforward (FF) versus Multi-Tanh (MT) linearized CMOS DA IMD3 and IIP3 simulated performance result comparison.

Tuning Frequency	FF IMD3	FF IIP3	MT IMD3	MT IIP3
5.5GHz before Tuning	-41.23 dBm	2.41 dBm	-51.14 dBm	7.5 dBm
5.5GHz after Tuning	-53.52 dBm	8.56 dBm	-58.74 dBm	11.17 dBm
1.5GHz before Tuning	-55.56 dBm	9.58 dBm	-51.26 dBm	7.43 dBm
1.5GHz after Tuning	-61.53 dBm	12.53 dBm	-55.69 dBm	9.64 dBm

Table 5.4 Indicates S21 simulated performance result before and after tuning the linearized CMOS DA using Multi-Tanh linearization technique.

Table 5.4: Linearized Multi-Tanh CMOS DA S21 forward gain simulated performance result before and after tuning is applied.

Frequency	Multi-Tanh S21
1.5GHz before tuning	9 dB
1.5GHz before tuning	6.6 dB
5.5GHz before tuning	7 dB
5.5GHz before tuning	4.5 dB

5.18 Chapter Summary

In this chapter, an analytical study of linearized CMOS Feedforward DA and Multi-Tanh DA and their simulation results have been presented.

A systematic and simple approach of implementing a CMOS linearized DA with a wide linearity range, simple IMD3 distortion cancellation tuning and good frequency response, has been discussed in this chapter as well.

Chapter 6

Silicon RF CMOS Linearized DA Layout Considerations

6.1 Introduction

This chapter contains several practical layout aspects of the linearized CMOS Multi-Tanh distributed amplifier. The circuit elements forming the linearized DA are discussed in terms of their physical arrangement.

6.2 Linearized CMOS Multi-Tanh DA High Frequency Layout Technique

At high frequencies, the linearized CMOS Multi-Tanh DA layout cannot be ignored [12]. Matching accuracy and noise immunity was the concern during DA layout rather than minimizing area. The linearized CMOS DA was carefully laid out to minimize unwanted behaviors such as magnetic coupling, noise and crosstalk. An obvious feature of the linearized CMOS DA layout is the mirrored symmetry. The use of balanced modular layout design results in balanced current distribution, easing power supply routing.

Symmetrical layout in the linearized CMOS distributed amplifier is essential to ensure proper wave phase alignment between all the gain stages output. Otherwise, drain transmission line output waves will not be added constructively and gain will be attenuated.

Wide metal tracks were used to reduce the low-frequency resistance of the metal. The drain transmission line signal conductor dimensions are made $10\mu\text{m}$ wide in order to reduce

the resistivity on the drain transmission lines which greatly affects the high-frequency performance of the device.

6.3 Resistor Layout Guidelines

Substrate noise isolation was achieved by placing resistors over an N-well as shown in Figure 6.1. Dummy resistors were placed at the ends in order to minimize effects of boundary dependent etching. Guard rings were placed surrounding the resistor layout to reduce noise.

Figure 6.1: Expanded Cadence layout of silicon RF CMOS resistor with guard ring, dummy resistors and N-well.

6.4 Minimum Inductor Separation

Separation between on-chip spiral inductors should be large enough to minimize magnetic coupling effects between them [59].

It was decided early in the linearized CMOS DA layout design phase to ensure sufficient spacing between the spiral inductors. Typically on-chip separation between inductors involves spacings of the order of $80\mu\text{m}$ for high frequency applications [59].

6.5 Halo: a Metallization Ground Ring

Surrounding the inductor is a metallization ground shield rings, halo, as shown in Figure 6.2 which acts as the path for the return current in the structure and to reduce the substrate loss. The halo prevents eddy currents from being induced in the substrate [59].

Figure 6.2: Expanded Cadence layout of silicon RF CMOS stacked inductor with Halo.

6.6 Optimal Linearized CMOS Multi-Tanh DA Gain Cell Layout Guidelines

Critical layout techniques such as interdigitized transistor layouts, symmetry for transmission line differential paths, multiple finger transistor layout to minimize gate resistance and guard rings surrounding the layout to reduce noise were all adopted to enhance the linearized CMOS Multi-Tanh DA performance.

Figure 6.3: Silicon RF CMOS Multi-Tanh cascode full gain cell.

Another important consideration in the linearized CMOS DA layout is the series gate resistance of the MOS transistor because it reduces gain significantly at higher frequencies. To prevent this effect, the gate poly was split into 32 fingers as depicted in Figure 6.3 in order to keep the total resistance down [10].

Minimizing the MOSFET gate resistance was achieved by properly sizing the finger width used during the layout of the transistor to $W_{finger}=5\mu\text{m}$.

Figure 6.4: Silicon RF CMOS Multi-Tanh distributed amplifier gain cell module with stacked inductors.

6.7 Linearized CMOS Multi-Tanh DA Layout Guidelines

Most of the interconnections, such as a signal energy transmission traces, are done at the top metal six layer which has the highest conductivity. The first metal layer was used as a ground plane. The layouts of the gain cell blocks are done symmetrically as can be seen in Figure 6.4. The width of metal interconnections was chosen according to the amount of current flowing through them. The bends in the routing lines consist of 45 degree turns to decrease reflections.

To meet pattern density requirements for the layout, fill cells are placed in the blank space surrounding the gain cells as shown in Figure 6.5.

Figure 6.5: Silicon RF CMOS Multi-Tanh distributed amplifier layout without Inductors.

As shown in the layout in Figures 6.6, the chip area is dominated by the passive components, which is typical for RFICs. The chip size is approximately $2.1 \times 1.1 \text{ mm}^2$ including testing pads as shown in Figures 6.6. An on chip MIM capacitance of 10pF is used to provide supply de-coupling.

Figure 6.6: Fully-integrated fully-differential Multi-Tanh distributed amplifier in silicon CMOS RF $0.18\mu\text{m}$ process.

6.8 Chapter Summary

In this chapter, high frequency layout design techniques used in implementing fully-integrated fully-differential linearized CMOS distributed amplifier based on the Multi-Tanh principle have been discussed.

Chapter 7

Silicon RF CMOS Linearized DA Experimental Results

7.1 Introduction

This chapter presents experimental results of the fully-integrated fully-differential silicon RF CMOS distributed amplifier based on Multi-Tanh linearization principle.

First, the test setup used for small-signal s-parameters, harmonics power and noise figure measurements of the linearized distributed amplifier are described. Then plots of the results including S-parameters, noise figure, 1dB power gain compression point, IMD3 and IIP3 are presented. Finally, deviations between measured results and predicted values are explained. All RF measurements were made with on-wafer probing in the microwave lab.

7.2 High-Frequency Measurements: On-Wafer Probing

Carleton university is equipped with an advanced on-chip RF and mm-wave measurement testbench setups. Labs include automated network analyzers, high-speed wafer probes and programmable DC source/monitor units in conjunction with state-of-the-art calibration techniques to characterize mm-wave active and passive devices on lossy silicon CMOS substrate.

On-Wafer probing shown in Figure 7.1 was performed on an analytical probe station

eliminating all of the problems inherited in packaging, as well as removing any uncertainty about bond wire inductances.

Figure 7.1: Test setup for on-wafer probing S-parameters and harmonic power measurements.

7.3 S-parameter Measurement Setup

The S-parameter test setup is shown in Figure 7.2 and includes DC-supplies, device under test, 8-pin high frequency probes and a vector network analyzer.

The S-parameter measurements were carried out using the Agilent 8722ES Vector Network Analyzer and multi contact wedge 8-pin high frequency differential probes with 3 RF needles up to 40GHz. The network analyzer is capable of accurately extracting the S-parameters of the device up to 65GHz. The Agilent 8722ES was calibrated up to the probes with the Open-Short-Load-Through calibration method.

The network analyzer was set to provide -20dBm output power, this will ensure the amplifier is operating under small signal conditions.

A full 2-port calibration from a start frequency of 50MHz to a stop frequency of 14GHz was performed. The device was connected as shown in Figure 7.2.

Figure 7.2: Test setup for S-parameter measurements.

7.4 Harmonics Power Measurements Setup

The output power measurement setup is shown in Figure 7.3. Large signal IIP3 measurements test setup used two Rohde and Shwartz tone signal generators and a high frequency power combiner with a 40GHz 8975A spectrum analyzer.

An external 18GHz power combiner was used to combine the tones from signal generators. At the output stage, the differential RF signal was fed to a spectrum analyzer which provided a load resistance of 50Ω . On-wafer two-tone IMD3 measurements were performed. The 40GHz 8975A spectrum analyzer was used for single-tone compression measurements as well.

7.5 Noise Figure Measurement Setup

The noise figure test setup is shown in Figure and includes DC-supplies, device under test, 8-pin probes and a noise figure analyzer.

A noise figure, NF, measurement of the linearized CMOS DA was performed using a

Figure 7.3: Two-Tone high-dynamic range test setup for measuring power and intermodulation distortion.

Figure 7.4: Noise Figure Test Setup

noise source and an Agilent N8975A NF measurement system.

7.6 Measured S-parameter Results

The S-parameter measurements were carried out using the Agilent 8722ES Vector Network Analyzer on an analytical probe station. The complete set of s-parameter measurements of the DA is presented in Figure 7.5. The measured S21 differential power gain peaks at 7dB in the lower frequency band and then rolls-off to a unity gain bandwidth of 8GHz. The supply voltage could be lowered to 2V and still achieve reasonable gain. The measured input and output matching S11 and S22 are both below -10dB up to 10GHz bandwidth. The measured Isolation S12 performance is below -23dB. Single-ended S-parameter measurements can be found in Appendix A.

Figure 7.5: Measured S-parameters: differential S21 forward power gain and single-ended input and output return losses and single-ended reverse isolation. The measured S21 differential power gain peaks at 7dB in the lower frequency band and then rolls-off to a unity gain bandwidth of 8GHz. The S21 differential power gain is extrapolated 2dB higher than the measured S21 single-ended power gain as depicted in Figure A.5 in Appendix A.

Two possible causes of S21 forward gain slopes are the large input and output capacitance of the $160\mu\text{m}$ CMOS transistors [84]. Since C_{gs} in $0.18\mu\text{m}$ process is much larger than other III-V process FETs, it causes the forward gain slope and drastically reduces bandwidth.

The S21 forward gain of the CMOS distributed amplifier is fundamentally limited by the resistive losses associated with both spiral inductors, the gate series resistance of the MOSFETs, the metal layers comprising the transmission lines and parasitic capacitance of FET transistor.

7.7 Measured Power Results

A two-tone harmonic balance technique was used to measure third-order distortion IMD3. Then equation 7.7.1 was used to calculate the third-order intercept point [35].

$$IIP3 = P_{in} + \frac{1}{2}(P_{out} - P_{IMD3}) \quad (7.7.1)$$

Before IMD3 cancellation is applied, by tuning the Multi-Tanh gain cell auxiliary gate bias voltage to 1.3V, the measured IMD3 is at -33.33dBm power level as shown in Figure 7.6. P_{in} was taken at 1dBm power level with fundamental component at 1.5GHz and 1.55GHz.

By tuning the Multi-Tanh gain cell auxiliary gate bias voltage to 0.6V, with fundamental component at 1.5GHz and 1.55GHz, the measured IMD3 is reduced to -38.00dBm power level as depicted in Figure 7.7. A comparison of Figure 7.6 and Figure 7.7 shows the measured IMD3 is improved by approximately 4.67dB, from -33.33dBm to -38dBm at 1.6GHz.

A wider span of measured IMD3 level -36.33dBm, 2nd order harmonics and IMD2 at 1.5GHz is depicted in Figure 7.8.

Before IMD3 cancellation is applied, by tuning the Multi-Tanh gain cell auxiliary gate bias voltage to 1.3V, the measured IMD3 is at -48dBm power level as shown in Figure 7.9. P_{in} was taken at 1dBm power level with fundamental component at 5.5GHz and 5.55GHz.

By tuning the Multi-Tanh gain cell auxiliary gate bias voltage to 0.6V, with fundamental component at 5.5GHz and 5.55GHz, the measured IMD3 is reduced to -52.50dBm

Figure 7.6: Measured output frequency spectrum with fundamental component at 1.5GHz and 1.55GHz and with IMD3 at 1.45GHz and 1.6GHz with -33.33dBm power level and with $P_{in}=1\text{dBm}$ before 3rd order distortion cancellation effect by tuning the Multi-Tanh gain cell auxiliary gate bias voltage to 1.3V.

Figure 7.7: Measured output frequency spectrum with fundamental component at 1.5GHz and 1.55GHz and with IMD3 at 1.45GHz and 1.6GHz with -38.00dBm power level and with $P_{in}=1\text{dBm}$ after 3rd order distortion cancellation effect by tuning the Multi-Tanh gain cell auxiliary gate bias voltage to 0.6V.

Figure 7.8: Measured IMD3 -36.33dBm, 2nd order harmonics and IMD2 at 1.5GHz.

Figure 7.9: Measured output frequency spectrum with fundamental component at 5.5GHz and 5.55GHz and with IMD3 at 5.45GHz and 5.6GHz with -48dBm power level and with Pin=1dBm before 3rd order distortion cancellation effect is applied by tuning the Multi-Tanh gain cell auxiliary gate bias voltage to 1.3V.

power level as depicted in Figure 7.10. A comparison of Figure 7.9 and Figure 7.10 shows the measured IMD3 is improved by approximately 4.5dB, from -48dBm to -52.50dBm at 5.45GHz.

Figure 7.10: Measured output frequency spectrum with fundamental component at 5.5GHz and 5.55GHz and with IMD3 at 5.45GHz and 5.6GHz with -52.50dBm power level and with $P_{in}=1\text{dBm}$ after 3rd order distortion cancellation effect by tuning the Multi-Tanh gain cell auxiliary gate bias voltage to 0.6V.

Before IMD3 cancellation is applied, by tuning the Multi-Tanh gain cell auxiliary gate bias voltage to 1.3V, the measured IMD3 is at -51.50dBm power level as shown in Figure 7.11. P_{in} was taken at -1dBm power level with fundamental component at 5.5GHz and 5.55GHz.

By tuning the Multi-Tanh gain cell auxiliary gate bias voltage to 0.6V, with fundamental component at 5.5GHz and 5.55GHz, the measured IMD3 is reduced to -57.33dBm power level as depicted in Figure 7.12. A comparison of Figure 7.11 and Figure 7.12 shows the measured IMD3 is improved by approximately 5.83dB, from -51.5dBm to -57.33dBm at 5.45GHz.

Experimental results verified the effectiveness of the proposed Multi-Tanh linearized CMOS DA in improving both the IMD3 and IIP3. An average of about 5dB improvement in IMD3 cancellation was measured. IIP3 was improved from 16.5dBm to 19dBm as shown

Figure 7.11: Measured output frequency spectrum with fundamental component at 5.5GHz and 5.55GHz and with IMD3 at 5.45GHz and 5.6GHz with -51.50dBm power level and with $P_{in}=-1$ dBm before 3rd order distortion cancellation effect by tuning the Multi-Tanh gain cell auxiliary gate bias voltage to 1.3V.

Figure 7.12: Measured output frequency spectrum with fundamental component at 5.5GHz and 5.55GHz and with IMD3 at 5.45GHz and 5.6GHz with -57.33dBm power level and with $P_{in}=-1$ dBm after 3rd order distortion cancellation effect by tuning the Multi-Tanh gain cell auxiliary gate bias voltage to 0.6V.

in results.

The HP8564E spectrum analyzer was used for single-tone compression measurements as well. P1dB is measured at 1.5GHz shown in Figure 7.13 at 4dBm.

Figure 7.13: Measured P1dB compression point for Multi-Tanh linearized CMOS DA, linearity up to 4dBm is measured.

7.8 Group Delay Measurements

By measuring the transit time using a vector network analyzer (Agilent 8722ES), with respect to frequency, of a signal through the device under test, the group delay was characterized.

The measured linearized distributed amplifier group delay versus frequency is shown in Figure 7.14. A constant group delay indicates a linear phase response. A relatively flat profile is observed, with variations of ± 150 ps, demonstrating good phase linearity which is sufficient for broadband amplification at high data rates.

As can be seen in Figure 7.14, there is a noticeable distortion effect between 8GHz and 10GHz, before the DA linearization was tuned. After the 3rd order cancellation tuning is applied a much flatter group delay response is measured.

Figure 7.14: Measured Group Delay before and after 3rd order distortion cancellation effect by tuning the Multi-Tanh gain cell.

7.9 Measured Noise Figure Results

The measured linearized DA noise figure ranges from 5.4dB to 8.4dB over the desired bandwidth.

Minimum noise figure of 7.6dB at 2GHz occurs at maximum gain. Noise gets amplified and starts to increase monotonically out of bandwidth operation range beyond 8GHz.

Figure 7.15: Measured noise figure of the fully-differential CMOS DA.

7.10 Measured On-chip Stacked Inductor Results

As the passive components are a main source of uncertainty, incorporating measured results with simulation gives a good estimation of the expected performance. The ability to accurately design and model these components is central to successful design of a distributed amplifier.

The de-embedding structure was fabricated along with the DA on the same die so that the parasitic components of the distributed amplifier can be corrected. Figure 7.16 shows die photograph of a $W=10\mu\text{m}$, $S=2\mu\text{m}$, $OD=80\mu\text{m}$ and $N=1.75$ stacked spiral inductor.

Having not simulated in momentum the transmission lines connecting the inductors together had a major impact on DA performance.

Also having placed process fillings near the inductor de-embedding and not having enough spacing more than $50\mu\text{m}$ between the inductor and the pad structure effected the performance of the on-chip inductor under characterization.

The inductor is measured with an Agilent 8722ES VNA. The square inductor is laid

Figure 7.16: Measured on-chip stacked inductor characterization.

out for 2-port measurement.

The open and short de-embedding structure, depicted in Figure 7.19, does not reflect the full test structure for lack of silicon space. The measurements, as depicted in Figure A.1 in Appendix A, are tainted by the capacitance of the pad's, as a result inductor characterization shown did not reflect the true results without proper de-embedding.

The microphotograph of Silicon RF CMOS Multi-Tanh DA gain stage with gate and drain line stacked inductors is depicted in Figure 7.17.

Figure 7.18 shows the microphotograph of $0.18\mu\text{m} \times 160\mu\text{m}$ Silicon RF MOSFET.

The fully-integrated 4-stage silicon RF distributed amplifier based on Multi-Tanh linearization principle is shown in Figure 7.19. The chip area is $2.1 \times 1.1\text{mm}^2$.

Carleton University copper RF cage on-wafer Probe Analytical station Test Setup is depicted in Figure 7.20.

7.11 Linearized CMOS Multi-Tanh DA Measured Performance Result Summary

The measured data is used to confirm the simulation results.

Figure 7.17: Microphotograph of Silicon RF CMOS Multi-Tanh DA Gain Stage with Gate and Drain Line Stacked Inductors.

Figure 7.18: Microphotograph of $0.18\mu\text{m} \times 160\mu\text{m}$ Silicon RF MOSFET.

Figure 7.19: Microphotograph of Fully-Integrated 4-stage Silicon RF CMOS Distributed Amplifier based on Multi-Tanh linearization principle.

Figure 7.20: Carleton university copper RF cage on-wafer Probe Analytical station Test Setup 2006.

Table 7.1 shows measured versus simulated Multi-Tanh IMD3 performance result comparison.

Table 7.1: Measured versus simulated Multi-Tanh IMD3 performance result comparison.

Tuning Frequency	Simulated Multi-Tanh IMD3	Measured Multi-Tanh IMD3
5.5GHz before Tuning	-51.14 dBm	-48.00 dBm
5.5GHz after Tuning	-58.74 dBm	-52.50 dBm
1.5GHz before Tuning	-51.26 dBm	-33.33 dBm
1.5GHz after Tuning	-55.69 dBm	-38.00 dBm

Table 7.2 shows measured versus targeted DA design specifications..

The difference between the measured and the simulated values can be attributed to a number of factors such as:

- a) Although the BSIM3 model is fairly accurate, there are inaccuracies in the RF device transistor models.
- b) Fifth order nonlinear effects not included in the analysis.
- c) Unaccounted nonlinear parasitic capacitances.
- d) Measurement inaccuracies.

The simulation results do not include all the parasitics associated with the test setup.

The schematic would have to be simulated taking into account the bends in the layout at the input and output ports of the amplifier. Each of these discontinuities degrade the gain performance.

The performance degradation is due to many compounding factors. One obvious reason is that the large parasitic capacitances and series resistances associated with the monolithic inductors attenuate the signal that passes through, especially at higher frequencies.

The gain and bandwidth performance could be improved by optimizing the gain cell limiting its parasitic capacitance and by utilizing either microstrip line or low-loss coplanar waveguides as transmission lines [84].

Having explained possible ways to enhance future performance, adding distortion cancellation tuning to conventional DAs proved a useful practical design solution.

Table 7.2: Measured versus targeted linearized CMOS DA design specifications.

Performance measures	Target	Simulated	Measured
Technology	CMOS 0.18 μm	CMOS 0.18 μm	CMOS 0.18 μm
Unity Gain Bandwidth	10GHz	15.69GHz	8GHz
S21 Power Gain	10dB	10.56dB	7dB
IIP3	10dBm	11.43dBm	15dBm
1dB	0dBm	0.88dBm	+4dBm
S11 and S22	< -10dB	< -10dB	< -10dB
S12	< -25dB	-23dB	-23dB
IMD3	< -40dB	< -50.14dB	< -35dB
Group Delay	< $\pm 25\text{ps}$	na	< $\pm 150\text{ps}$
Min. NF	5dB	3.9dB	7.5dB
Power Consumption	100mW	110mW	158mW
Silicon area	2mm X 1mm	na	2.1mm X 1.1mm

Table 7.3 shows a comparison with measured published Differential CMOS distributed amplifiers.

Table 7.3: Comparison with measured published CMOS distributed amplifiers.

Design	Process	Gain(dB)	BW(GHz)	NF(dB)	IIP3(dBm)	Area(mm ²)	Power(mW)
[12]	0.6 μ m	5.5	7.5	8.7-13	4	1.3x2.2	216
[11]	0.6 μ m	6.5	4	6.8	14	na	83.4
[7]	0.18 μ m	7.8	25	4.8-7	4.6	1.0x1.29	54
[85]	0.18 μ m	7.5	25	4.8-7	4.7	1.0x0.9	100
[79]	0.18 μ m	15	22	na	na	na	190
[10]	0.8 μ m	5	4.7	5.1	15	0.7x0.3	54
[15]	0.18 μ m	10.6	14	3.4-5.4	9.4	1.0x0.9	52
[14]	0.18 μ m	8	10	6-6.9	9.3	0.7x0.7	122
[84]	0.18 μ m	4	39	na	na	1.1x3	140
[13]	0.35 μ m	20	5	1.5-3	-15	0.95x1.8	100
[17]	0.18 μ m	6	27	6	na	1.8x0.9	68
this work	0.18 μ m	7	8	8-10.5	15-19	2.1x1.1	158

Table 7.3 demonstrates that with the large input and output capacitance of the 160 μ m CMOS transistors used in Multi-Tanh DA design, the S-parameter of the linearized CMOS DA performance is comparable to [12], [11], [10] and [14].

A 4-stage single-ended linearized distributed amplifier operating between 0.8 and 2.2GHz is presented in [77]. The parallel diode linearization technique is applied to a distributed amplifier resulting in a 14dB gain with an average of 9.5dB reduction in spectral regrowth for the first sidelobe. Although, compared to this work, the diode linearized DA [77] achieved both higher gain and distortion reduction. However, [77] had a very limited bandwidth which is not suited for broadband applications.

Larger chip area and higher power dissipation was the main disadvantage of the Multi-Tanh differential CMOS DA.

7.12 Conclusions

In this chapter, a fully-integrated CMOS distributed amplifier employing double gate stacked on-chip inductor as transmission lines and a tunable linearity Multi-Tanh distortion cancellation networks differential cascode gain cells has been experimentally validated.

To the authors knowledge this is the first reported experimental verification of the use of Multi-Tanh measured CMOS DA circuit performance was presented.

Experimental results show that the Silicon CMOS DA provides a 7dB peak power gain then rolls off to 8GHz of unity gain bandwidth and less than negative -25dB of reverse isolation, while requiring no off-chip components. The experimental results are fairly good. Linearity is improved by at least 3.5dB using multi-tanh distortion cancellation networks as the DA gain cells. The 1dB compression point is 4dBm. IIP3 is adjustable from 16dBm to 19dBm. Using m-derived matching networks, S11 and S22 stay below -10dB up to 10GHz. The 0.4-8GHz DA dissipates 158.5mW of power.

Chapter 8

Conclusions And Recommendations

In this thesis, two major tasks have been explored. One is the construction of an architecture for tunable IMD3 distortion cancellation in CMOS distributed amplifiers for optical communication systems and ultra wide bandwidth applications. The other is the study of multi-level passive components in Silicon RF CMOS substrate. As a conclusion, the key contributions presented in previous chapters are summarized.

The fully integrated Multi-Tanh CMOS DA attains wide bandwidth operation with a tunable linearity capability, experimental results show 7dB peak power gain then rolls off to 8GHz of UGB. Linearity improved by at least 3.5dB using Multi-Tanh IMD3 cancellation networks as the DA gain cells. The 1dB compression is 4dBm and the IIP3 is adjustable from 16dBm to 19dBm.

Early in the design process, a Feedforward DA design topology was explored and designed but not fabricated. Then a Multi-Tanh DA configuration was investigated, designed, fabricated and measured. Biasing of the linearized CMOS DA was kept very simple, with gate and drain being biased directly which provided IMD3 distortion cancellation tuning capability.

The main disadvantage of the Multi-Tanh DA linearization technique is its large silicon area and high power consumption. The large silicon area is compensated by using multi-level on-chip inductors in the transmission lines.

Physics-based EM simulations of circuit structures, in particular stacked inductors, proved to be an important tool in performing investigative predictions of the device performance.

8.1 Summary

The proposed linearized CMOS DA solution is suitable for high frequency applications requiring a wide dynamic range (i.e. lower intermodulation distortion).

It should be apparent that the design idea is not limited to CMOS technology but can be used also for bipolar, GaAs, or other exotic technologies.

In this work we have shown that silicon RF CMOS based technologies have the potential to compete with GaAs and other III-V technologies for high-performance circuit applications. In Chapter 2, a silicon technology overview was presented to set the basis for silicon circuit design. At high frequencies, it is crucial for designers to have an understanding of the process limitations of silicon substrates, since it is a non-conventional microwave substrate. CMOS distributed amplification theory was presented in Chapter 3. Chapter 4 introduced silicon based stacked passive on-chip inductors, their design, limitations, and sources of loss. In Chapter 5, linearized CMOS DA designs implemented in silicon RF substrates with distortion cancellation techniques were presented. In Chapter 6, linearized CMOS DA high frequency layout techniques used in the design process are presented. In Chapter 7, experimental results of the fully-integrated, fully-differential silicon RF CMOS distributed amplifier based on Multi-Tanh linearization principle are presented. Finally, a thesis summary and a list of thesis contributions in this chapter is presented.

8.2 Thesis Contributions

In summary, this thesis has presented several contributions aimed at furthering the development of silicon RF CMOS ICs.

1. First reported experimental verification of the use of Multi-Tanh measured CMOS DA. The feasibility of the proposed design was evaluated with the fabrication of a test chip in a $0.18\mu\text{m}$ standard digital CMOS process. Experimental and analytical study of IMD3 distortion reduction in silicon RF CMOS distributed amplifiers.

A silicon RF CMOS distributed amplifiers based on a Multi Tanh and Feedforward gain cell topologies were proposed and designed. The circuit attains wide bandwidth operation with a tunable linearity capability and a reasonable gain and noise figure. It combines active analog techniques with a microwave distributed design approach done using silicon

RF CMOS technology.

2. Both proposed linearized CMOS DA solutions present an effective method for tuning circuit performance externally after chip fabrication.

3. Silicon RF CMOS DA artificial transmission lines were designed using multi-level on-chip spiral inductors. Stacked inductors were modeled using ASITIC, fullwave ADS Momentum and Cadence Inductor Modeler EM-simulator on silicon RF CMOS substrate.

8.3 Future Proposed Work

There are a few issues that await exploration in future studies. Techniques such as self adaptable DA IMD3 cancellation may be useful to pursue research on. A system controller circuitry can be designed to adaptively linearize CMOS DA performance.

Fabrication of the Feedforward CMOS DA topology comparing the measured results with the Multi-tanh CMOS DA topology can give valuable insight in exploring more efficient DA IMD3 distortion cancellation techniques at high frequency.

For future high frequency designs, it is highly recommended to fabricate and measure different on-chip inductors that span the desired range of operation with the same technology process ahead of designing the DA. To improve Linearized DA performance, I would rather research on-chip CPW in the Transmission lines instead of on-chip spirals.

Appendix A

De-embedding and Mixed-Mode S-parameters

A.1 On-chip Inductor S-parameter De-embedding and Extraction

After stack spiral on-chip inductor fabrication, 2-port S-parameters can be measured using an HP8722ES Network Analyzer and RF G-S-G 3-pin probes. Performance quantities such as inductance and Q value can be derived from the measured S-parameter data set [69].

To characterize the on-chip passive device performance, an open, short and passive device structure s-parameter is required for accurate de-embedding [69] [86].

First, de-embedding from measured SHORT and OPEN test structures 2-port Y-parameters is performed using the procedure outlined [86].

The 2-port Y-parameters were obtained from the S-parameters using a matrix transformation [69] [86].

$$\begin{aligned} Y_{DUT} &= Y_{Total} - Y_{Open} \\ Y_{Short/Open} &= Y_{Short} - Y_{Open} \end{aligned} \tag{A.1.1}$$

The next step is to convert Y-parameters data set to Z-parameters data set:

$$\begin{aligned} Z_{DUT/Open} &= Z(Y_{DUT/Open}) \\ Z_{DUT/Open} &= Z(Y_{DUT/Open}) \end{aligned} \tag{A.1.2}$$

Then de-embedding from Short is performed using the Z-parameters data set:

$$Z_{DUT} = Z_{DUT/Open} - Z_{Short/Open} \quad (A.1.3)$$

At this point, the Z-parameters data set is converted to S-parameters data set:

$$S_{DUT} = S(Z_{DUT}) \quad (A.1.4)$$

After de-embedding, the extracted inductor S-parameters is a 2-port S-parameters data set.

Now the 2-port S-parameters data set have to be transformed to 1-port S-parameters data set and then to Z-parameters.

Once the extracted inductor S-parameters, S11,S12,S21 and S22 are available.

Then convert the 2-port S-parameters to 1-port:

$$S_{11_1port} = \frac{S_{11} - (S_{12} \times S_{21})}{(1 + S_{22})} \quad (A.1.5)$$

Then convert S11 1-port to Z11 1-port:

$$Z_{11_1port} = 50 \times \frac{(1 + S_{11_1port})}{(1 - S_{11_1port})} \quad (A.1.6)$$

Finally, the inductance and Quality factor values can be calculated from:

$$L = \frac{imag(Z_{11_1port})}{(2 \times \pi \times frequency)} \quad (A.1.7)$$

$$Q = \frac{imag(Z_{11_1port})}{real(Z_{11_1port})} \quad (A.1.8)$$

Figure A.1: Multi-level on-chip inductor measurement result and de-embedding structure.

A.2 Differential Mixed-Mode S-parameters Characterization

One way of characterizing differential circuits in RF and microwave frequencies is measuring the mixed-mode S-parameters [87].

As the linearized differential CMOS DA itself is a four-port network dealing with differential and common-mode signals, a mixed-mode s-parameter measurement technique using a conventional two-port network analyzer is discussed.

A simple transformation matrix to operate on single-ended S-parameters to produce mixed-mode S-parameters is presented in [88].

The simple linear relationship between the parameters is given by [88]

$$S_{d2d1} = \frac{1}{2} (S_{31} - S_{41} - S_{32} + S_{42}) \quad (\text{A.2.1})$$

Where S_{d2d1} is the differential output from composite port 2, the previous ports 3 and 4,

ratioed against a differential drive into composite port 1, the previous ports 1 and 2 [88]. A complete set of mixed-mode S-parameter measurements of the linearized CMOS Multi-Tanh DA are carried out. Results are depicted in Figure A.2 to Figure A.17.

The single-ended measured forward gains S21, exhibit relatively lower S21 value over the entire frequency band as shown in Figure A.5. The mixed-mode return loss S11 and S22, show better than -10dB over the frequency of operation as shown in Figure A.2 and Figure A.3. The reverse isolation S12 is better than -23dB as depicted in Figure A.4. The linearized CMOS Multi-Tanh DA mixed-mode S-parameters results were obtained with performing calibration up to the VNA precision cable only without calibrating the 8-pin probe-tips and without performing de-embedding procedure to the 8-pin pads frame. Figure A.18 show the probe pad floorplan frame used in the measurements of the linearized CMOS DA.

Figure A.2: Measured mixed-mode[31] single-ended S-Parameter S11.

Figure A.3: Measured mixed-mode[31] single-ended S-Parameter S22.

Figure A.4: Measured mixed-mode[31] single-ended S-Parameter S12.

Figure A.5: Measured mixed-mode[31] single-ended S-Parameter S21.

Figure A.6: Measured mixed-mode[41] single-ended S-Parameter S11.

Figure A.7: Measured mixed-mode[41] single-ended S-Parameter S22.

Figure A.8: Measured mixed-mode[41] single-ended S-Parameter S21.

Figure A.9: Measured mixed-mode[41] single-ended S-Parameter S12.

Figure A.10: Measured mixed-mode[32] single-ended S-Parameter S21.

Figure A.11: Measured mixed-mode[32] single-ended S-Parameter S11.

Figure A.12: Measured mixed-mode[32] single-ended S-Parameter S22.

Figure A.13: Measured mixed-mode[32] single-ended S-Parameter S12.

Figure A.14: Measured mixed-mode[42] single-ended S-Parameter S21.

Figure A.15: Measured mixed-mode[42] single-ended S-Parameter S11.

Figure A.16: Measured mixed-mode[42] single-ended S-Parameter S22.

Figure A.17: Measured mixed-mode[42] single-ended S-Parameter S12.

A.3 Publications/Presentations

A.3.1 Conference Paper

"A 0.1-12 GHz fully differential CMOS distributed amplifier employing a Feedforward distortion cancellation technique." El-Khatib, Z.; MacEachern, L.; Mahmoud, S.A.; Proceedings of the 2004 International Symposium on Circuits and Systems, ISCAS '04. Volume 1, 23-26 May 2004 Page(s): 617-20.

ABSTRACT:

A fully differential CMOS distributed amplifier (DA) with a 10-dB pass band gain and 12-GHz bandwidth is described. The fully differential eight-stage DA employs a feedforward distortion cancellation topology. The circuit attains wide bandwidth operation with a high gain and minimal linearity degradation. Input and output are matched to 50 ohms using m-derived matching networks, with a worst-case return loss of -10-dB up to 8-GHz. The input-referred 1-dB compression point varies from 11.6-dBm at 1-GHz to 13.68-dBm at 10-GHz. The amplifier has an input-referred third-order intercept point of 4.73-dBm. A parasitic-aware simulation methodology was used to optimize the design in a standard

Probe Pad Frame Layout

**150um pitch (tip spacing)
configuration
DC-G-S-S-G-S-G-DC
tip footprints.
The probe would provide:
3 RF (40GHz) needles
and 5 DC needles.
note: ground needle
is also considered as
DC**

0.18- μm CMOS process using Agilent's ADS simulation environment. The eight-stage DA dissipates 145-mW from a single 1.8-V power supply.

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