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**A DIGITAL IMPLEMENTATION OF A
RADAR COHERENT-ON-RECEIVE SYSTEM**

by

M. C. Fernando B.Eng

A thesis submitted to the
Faculty of Graduate Studies and Research
in partial fulfillment of the requirements of

Master of Engineering

Faculty of Engineering
Department of Electronics
Carleton University

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The undersigned recommend to the faculty of
Graduate Studies and Research
the acceptance of the thesis:

**A DIGITAL IMPLEMENTATION OF A
COHERENT-ON-RECEIVE RADAR SYSTEM**

Submitted by M. C. Fernando
in partial fulfillment of the requirements for the
degree of Master of Engineering

Prof J.S.Wight

Thesis Supervisor

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Department of Electronics

ABSTRACT

A novel digital Coherent-On-Receive Subsystem has been designed, built and tested. Its purpose is to provide Coherent-On-Receive operation for pulsed radar systems employing incoherent magnetron transmitters. This design used two Finite Impulse Response (FIR) filters, which extracted the coherent phase from the return signal by performing a matched filter operation between the transmit and receive signals.

The phase locking characteristics of this subsystem were evaluated using a magnetron transmitter, and its performance was compared with that of a conventional coherent oscillator (COHO), which was tested in a similar fashion. Results indicate that in a nonchirped environment the performance of this digital technique is comparable to that obtained with the COHO, while the possibility exists of it displaying superior performance in a highly chirped scenario.

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LIST OF SYMBOLS

R	ground range
L	two way distance
L_λ	two way distance expressed in terms of transmitted wavelength
L_ϕ	distance expressed in terms of radian phase angle
λ	transmitted wavelength
v_r	velocity in the direction of the target
v	velocity of the vehicle
f_d	Doppler frequency
c	speed of light
Φ	grazing angle
P_r	received power
P_t	peak transmit power
G	gain of the antenna
D	slant range to target
σ_0	radar cross section/unit area
T	length of the transmit pulse
ω_{11}	transmit frequency
t_{01}	two way time to a target located at slant range of D_{01}
h	altitude of the aircraft
$P_r(t)$	return power as a function of time
θ_B	beamwidth of the antenna
σ	radar cross section of a target
ρ_r	minimum range resolution of a radar system
f_t	transmit frequency
ϕ_t	random transmit phase of the magnetron
$A_1(t)$	amplitude envelope of transmit pulse
A_2	peak amplitude of RF signal
$A_3(t)$	peak amplitude of IF pulse input to COHO
f_2	local oscillator frequency

ϕ_2	local oscillator phase
$A_4(t)$	amplitude of the received signal
ϕ_{TR}	phase angle from target
Δt	two way travel time to a target
$\Delta\phi$	phase run between magnetron chirp and COHO frequency
$h(t)$	frequency response of filter
$s_o(t)$	output signal from filter
$s_1(t)$	input signal to filter
$S_1(f)$	Fourier transform of $s_1(t)$
N_o	input noise power/unit bandwidth
N	output noise power
E	signal energy
$s_1^*(T-t)$	impulse response required to obtain the matched filter criteria
$y(t)$	output of matched filter
$Y(f)$	Fourier transform of $y(t)$
$A(t)$	amplitude of transmit signal
$B(t)$	amplitude of receive signal
d	distance to the target
$I_i(t), I_r(t)$	In-phase components of transmit/receive signal
$Q_i(t), Q_r(t)$	Quadrature component of transmit/receive signal
P_{av}	average output power from magnetron
f_p	pulse repetition frequency
T'	two way travel time to the maximum range (100 km)
σ	standard deviation
σ_{aw}	amplitude weight standard deviation

CHAPTER I INTRODUCTION

1.1 Introduction

Since its advent in the early twentieth century, the radar has undergone an exponential growth in sophistication. This growth has enabled radars to be employed in a wide variety of applications such as air traffic control, space surveillance and tracking, ship navigation, remote sensing and military reconnaissance [1].

Radar systems can be broadly categorized into two groups: CW and pulsed. The CW systems operate continuously, while the pulsed systems transmit short bursts of energy. These two types of radars are used for very different purposes: the CW radar for obtaining target Doppler information and the pulsed radar for target ranging.

The CW radar is limited by two main factors. First, the transmitted power, and hence the maximum range of the system, is limited by the amount of isolation achievable between the transmitter and receiver (the unwanted transmitted signal entering the receiver limits receiver sensitivity). The pulsed radar has no such limitation since the transmitter and receiver operate during different time intervals. Secondly, the CW radar (without any modulation) is unable to measure range to a target since it is operated on a

continuous basis with no timing information. A pulsed radar, on the other hand, can unambiguously detect any target which has a return time less than the time between two consecutive transmit pulses (the pulse repetition period).

Radar systems can also be broadly categorized into different groups depending upon the function they serve. Systems which detect moving targets in the presence of clutter are known as MTI (Moving Target Indicator) radars. The change of phase caused by moving targets is extracted by means of a circuit such as a delay line canceller. This device acts as a filter to eliminate the DC components of fixed targets while passing the AC components of moving targets. MTI radars can operate in a coherent or non-coherent fashion. A coherent system uses the phase variations in the echo signal to detect moving targets while the non-coherent system uses the amplitude fluctuations of this signal to recognize the target.

Pulse Doppler radars serve much the same function as the MTI systems, the principal difference being that they operate at a higher PRF (pulse repetition frequency). Pulse Doppler radars use fully coherent transmitters. Coherency on transmit is required, as multiple returns from different pulses return to the receiver simultaneously, and the only way to process all returns is to transmit with a continuous phase on a pulse to pulse basis.

Tracking radars differ from other radars in that they determine the azimuth and elevation position of a target in addition to range, and supply data which can be used to determine a target's future position. There are two main types of tracking radar systems: the track-while-scan radar and the continuous tracking radar. The former provides sampled data on one or more targets while the latter supplies continuous information on a single target.

Airborne imaging radars use the radar return information to create an image of the terrain. There are two main types of airborne radars used for imaging: the real-aperture-radar called Side Looking Airborne Radar (SLAR) and the Synthetic Aperture Radar (SAR) [2]. A SLAR is usually operated in a non-coherent fashion, with occasionally a coherent section to perform MTI. The SAR, on the other hand, requires either totally coherent operation or at least coherent-on-receive operation.

The type of radar of greatest interest to this body of work is the Synthetic Aperture Radar. The advantage of this radar over the SLAR is that it offers far better azimuthal resolution. If pulse compression is also employed, a large improvement in the cross-track resolution is also obtained.

The primary difference between SARs and SLARs is that the former

must use a coherent detection process whereas the latter need not. Another difference is that SLARs need only to correct for gross variations in altitude and along-track speed, while the SARs must correct for very small altitude and speed fluctuations.

Most systems which do not require coherent transmission use incoherent microwave oscillators. Presently, one of the most popular incoherent microwave oscillators is the coaxial magnetron. The use of a coaxial magnetron yields a cost effective system which can be operated in either an incoherent fashion, or can be converted into a coherent system on reception by means of a Coherent-On-Receive (COR) subsystem. The COR subsystem stores the randomly emitted phase of the magnetron during the transmit cycle, and uses this for phase detection in the receive cycle.

For COR operation, the transmit signal can be memorized in either an analogue or a digital manner. The analogue method uses a coherent oscillator (COHO) which is phase locked to the transmit RF pulse. In this manner the COHO provides a reference signal which is preserved for the entire pulse repetition interval.

A new digital technique uses a tapped delay line correlator which samples the transmit signal at discrete intervals, and uses these samples to

perform a matched filtering of the return signal, thereby extracting the phase information from each range cell.

1.2 Thesis Objectives

The primary objective of this thesis has been to design, build, test and evaluate a digital Matched COR subsystem, based on a Finite Impulse Response (FIR) filtering scheme implemented using several tapped delay line correlators. A one sample version of this system (called a One Coefficient Multiplier) has also been implemented and tested. Testing has been performed using both a coaxial magnetron transmitter and a signal generator. The phase locking characteristics of these two systems have also been compared with those of a commercial COHO which was also tested using the same transmitter.

As the locking performance of any COR system is dependent upon the phase characteristics of the transmitter, an intrapulse phase analysis has also been performed to determine the phase run out (chirp) and the stability of the coaxial magnetron.

1.3 Thesis Outline

Included in Chapter 2 is an introduction to coherent radar techniques, with emphasis placed on the matched filtering concepts. The basic concepts regarding a coaxial magnetron are introduced along with a discussion on the general operations of a COHO.

The magnetron intrapulse phase analysis is described in detail in Chapter 3. The data obtained from this test is discussed and interpreted in the latter part of the chapter.

In Chapter 4, the testing of the COHO with both the magnetron and the signal generator is described. The test results are also presented in this chapter.

The design and fabrication of the FIR FILTER subsystem and the One Coefficient Multiplier are described in Chapter 5. The testing of these two systems along with that of the COHO are presented. The performance characteristics for each system is then discussed and compared.

In Chapter 6, a synopsis of the experimental results is presented. Ways of improving the FIR FILTER performance are discussed. Also mentioned are suggestions for future work related to this project.

CHAPTER II   GENERAL RADAR CONCEPTS

2.1   Introduction

There are many aspects that must be addressed when designing a radar in general and a Coherent-On-Receive (COR) subsystem in particular. A good knowledge of the underlying theory and the performance characteristics of each radar subsystem is essential to this design process. The purpose of this chapter is to introduce the general concepts dealing with the coherent radar process and to present the basic theory pertaining to the coaxial magnetron. The performance characteristics and limitations of the COHO and FIR FILTER systems are also discussed.

2.2   Theory of Radar Detection

A radar is an electromagnetic system used for the detection and location of objects [1]. It emits electromagnetic radiation which illuminates the area encompassed by the antenna beamwidth. A target present in this area intercepts some of the transmitted signal, and reradiates it in all directions, thereby giving rise to a return signal. This return is gathered by the radar system and processed in order to extract the required information.

Figure 2.2.1 Target Doppler Information

Consider a vehicle moving past a target as illustrated in Figure 2.2.1. As the vehicle moves past the target, the instantaneous distance between the two objects changes. Thus, if the distance between the two objects is R , the two way distance is L where:

$$L = 2R$$

Now, in terms of wavelengths L is given by

$$L_{\lambda} = \frac{2R}{\lambda}$$

If this distance is represented in terms of an angular phase, the above expression becomes

$$L_{\phi} = \frac{2R}{\lambda} 2\pi = \frac{4\pi R}{\lambda}$$

The rate of change of distance to the target leads to a rate of change of phase which manifests itself as a Doppler frequency

$$\frac{dL_{\phi}}{dt} = \frac{4\pi}{\lambda} \frac{dR}{dt}$$

Now

$$\frac{dR}{dt} = v_r$$

which is the velocity in the direction of the target.

This velocity is related to v , the velocity of the vehicle, as follows:

$$v_r = v \sin \theta$$

where θ is shown in Figure 2.2.1.

Therefore

$$\frac{dL_{\phi}}{dt} = \frac{4\pi}{\lambda} v \sin \theta$$

The Doppler frequency, f_d equals

$$f_d = \frac{1}{2\pi} \frac{dL_{\phi}}{dt} = \frac{2}{\lambda} v \sin \theta$$

When a pulse is transmitted by a radar system, it travels across the coverage area (illuminated by the radar beam) sending return signals from all ranges. The illuminated area is directly proportional to the antenna beamwidth, and the transmit pulse length. Consider Figure 2.2.2 where a radar at point A is shown illuminating a swath of terrain.

Figure 2.2.2 Imaging Radar Geometry

For grazing angles less than 90 degrees, the dimensions of the illuminated area is given as $(cT/2) \sec \Phi$ in the cross track direction and $D\theta_B$ in the along track direction, as shown in Figure 2.2.2. For large range values the illuminated area is directly proportional to the range. The power received from a unit area in the illuminated swath is inversely proportional to the fourth power of the range and is given by the equation

$$P_r = \frac{P_t G^2 \sigma_0 \lambda^2}{(4\pi)^3 D^4}$$

where: P_r is the received power

P_t is the peak transmit power

G is the gain of the antenna

λ is the wavelength of the transmitted signal

D is the range to the target

σ_0 is the radar cross section/unit area

Mathematically, the return signal from any target can be expressed as the time convolution of the transmit signal, with a time function that represents the spatial extent of the target.

For a point target, the above time function is a delta function delayed by the two way travel time to the target. If the transmit signal can be represented as $\cos \omega_{11} t$ for $0 \leq t \leq T$, where T is the length of the pulse, then the return can be written as

$$s(t) = \cos \omega_{11} t * \delta(t - t_{01})$$

where

$$t_{01} = \frac{2D_{01}}{c}$$

and D_{01} is the slant range to the target.

Hence

$$\begin{aligned} s(t) &= \cos \omega_{11} (t - t_{01}) \\ &= \cos (\omega_{11} t - \phi_{01}) \quad t_{01} \leq t \leq t_{01} + T \end{aligned} \quad (2.2.1)$$

where

$$\phi_{01} = \omega_{11} t_{01}$$

The power of this return signal is given by

$$P_r = \frac{P_t G^2 \sigma_0 \lambda^2}{(4\pi)^3 D_{01}^4}$$

If ground clutter is approximated as a uniformly distributed target, the slant range D is given by the following equation:

$$D = \sqrt{h^2 + R^2}$$

where R is the ground range, and
 h is the altitude of the aircraft.

Now

$$D = \frac{ct}{2}$$

Therefore, the ground range to the illuminated area, expressed as a function of time, is given by

$$R = \sqrt{\left[\frac{(ct)^2}{4} - h^2 \right]} \quad \text{for } \frac{ct}{2} \geq h$$

The return signal $s(t)$ can be expressed as

$$s(t) = \left\{ \cos \omega_{11} t * \sqrt{\left[\frac{(ct)^2}{4} - h^2 \right]} \right\} P_r(t) \quad t \geq \frac{2h}{c} \quad (2.2.2)$$

where the two convolving functions are time limited.

This represents the return from any point in the antenna beam.

Therefore, to obtain the total return, 2.2.2 should be integrated over the entire beamwidth.

$$s(t) = \int_{-\frac{\theta_B}{2}}^{\frac{\theta_B}{2}} \left\{ \cos \omega_{11} t * \sqrt{\left[\frac{(ct)^2}{4} - h^2 \right]} \right\} P_r(t) d\theta$$

$$s(t) = \left\{ \cos \omega_{11} t * \sqrt{\left[\frac{(ct)^2}{4} - h^2 \right]} \right\} P_r(t) \theta_B \quad t \geq \frac{2h}{c} \quad (2.2.3)$$

This equation yields an expression which describes the return signal as a function of time.

If a strong point-like reflector, such as a vehicle, exists in the area illuminated by the antenna beamwidth, the return can be represented by equation 2.2.1 along with a term for the background clutter. The background clutter term can be thought of as being made up of returns from a large number of point scatterers having a return power much less than that from the target.

For a radar on board an aircraft, the point of observation moves. Hence,

the radar's aspect angle changes with respect to the swath being observed. This change in the aspect angle makes the phase return from the background clutter as well as from point targets vary on a pulse to pulse basis. When the return data is processed, the pulse to pulse coherence of the clutter and the point targets enables them to be Doppler binned and hence associated with a certain angular fraction of the radar beam. This Doppler binning in turn allows increased angular resolution to be achieved.

2.3 Transmitter

A radar transmitter consists of a microwave power generating tube and a modulator power supply. Several families of microwave tubes are commercially available. The type of device selected for a particular system is dependent upon several factors such as cost, function, output power, coherency and the mode of operation, either continuous or pulsed.

The microwave tube used in this study is a pulsed coaxial magnetron. The remainder of this section will be used to familiarize the reader with the basic concepts associated with this device.

A magnetron is an incoherent (random phase) microwave oscillator. It converts the potential energy of an electron into RF energy in a series of resonant cavities similar to the one shown in Figure 2.3.1.

Figure 2.3.1 Cut Section of a Conventional Magnetron

The outer wall of this structure can be considered to be the inductive portion while the vane tip region is the capacitive portion. Hence, the resonant frequency of this structure is determined by the physical dimensions of the resonant cavities [3, 4].

To sustain oscillations in a resonant cavity, energy has to be continuously supplied at the correct phase such that the instantaneous RF field retards the electrons travelling through it. When this occurs, the energy lost by the electrons is exactly offset by an increase in the RF field strength.

The coaxial magnetron differs from the conventional magnetron due to the presence of a built-in stabilizing cavity which supports a TE 101 mode. The cavity improves the frequency stability, spectrum quality and pulse-to-

pulse conformity of the device. Figure 2.3.2 illustrates a coaxial magnetron structure.

Figure 2.3.2 Coaxial Magnetron

The magnetron can be tuned by altering the physical dimensions of the cavity. This can be achieved by moving the end plate of the stabilizing cavity. The cavity resonators are coupled to the stabilizing cavity by means of a series of slots as shown in the illustration.

Certain fundamental characteristics of a transmitter such as the output power, transmit pulse width, Pulse Repetition Frequency (PRF), and intrapulse chirp play an important role in determining the overall system parameters. Each of these characteristics are briefly addressed in the following discussion.

The output power of a magnetron determines the strength of the radar return signal. The relationship between the received power and the peak transmitted power for a monostatic radar is given by the following equation:

$$P_r = \frac{P_t G^2 \lambda^2 \sigma}{(4\pi)^3 R^4}$$

where σ is the radar cross section of the target.

This equation shows that the transmitted power, P_t , is proportional to the return signal power, P_r . Thus, for a given P_r , a larger transmitted power indicates a larger maximum range.

The transmit pulse width, T , of the magnetron determines the range resolution of the system, ρ_r , which is given by the relationship

$$\rho_r = \frac{cT}{2}$$

In an imaging radar, high range resolution and hence a short pulse is needed to obtain good clarity in the images produced by the system. On the other hand, for Coherent-On-Receive (COR) operation, the use of a narrow transmit pulse implies that the coherent oscillator (COHO) has less time to lock on to the random phase of the transmit pulse. This places more stringent locking time requirements on the COR system. Therefore, if the transmit pulse width is controllable, both these conflicting factors should be taken into account when selecting an appropriate value for this quantity.

The Pulse Repetition Frequency (PRF) of the transmitter determines the unambiguous range of a system. Even though radars which operate at a low PRF usually suffer from ambiguous Doppler measurements, at low PRFs the time between consecutive pulses is large enough for these systems to provide unambiguous range measurements. The opposite is true for the high PRF systems, where the Doppler measurement is unambiguous, while ambiguities have to be resolved in the range measurement.

The intrapulse chirp refers to the carrier frequency change within the RF transmit pulse. The presence of a chirp adds an extra level of complexity to the COR system because the phase run through the pulse is a nonlinear function of time. When the COHO locks on to the transmit pulse, it retains the phase of only that point in the pulse. If the chirp is large and random on

a pulse-to-pulse basis, the phase corrected returns from different pulses would have varying phase runs for each pulse, thereby making it impossible to perform any form of pulse-to-pulse integration. One of the primary goals of magnetron design is to reduce the intrapulse chirp. Most practical magnetrons have some chirp at the beginning and end of each transmit pulse, but are relatively chirp free in the middle of the pulse.

As mentioned earlier, the transmitter contains another major unit known as the modulator. The modulator accepts several input signals, transforms these into appropriate voltages and currents, and applies them to the magnetron tube, causing it to fire at the pulse repetition rate.

The modulator also contains control and built-in test equipment (BITE) circuitry for the protection of the magnetron/modulator unit. This circuitry monitors various signals vital to the safe operation of the unit. If a fault occurs, it is detected by the control/BITE circuitry and appropriate action is taken to safeguard the unit.

2.4 Keyed COHO

An injection-locked COHO works as a free running oscillator that can be locked in phase with the carrier of an injected short duration pulse signal. It thus provides an on-going reference phase even after the disappearance of

the original pulse.

The COHO is usually housed in the receiver, as illustrated in Figure 2.4.1. A sample of the RF transmit signal is obtained by means of a coupler placed in the transmit path of the signal. This high frequency signal is then down-converted using several down-conversion chains and then injected into the COHO at an intermediate frequency close to its free running value. The COHO locks on to the phase of the input signal, and during the receive interval, acts as a reference local oscillator by downconverting the receive signal from the intermediate frequency to baseband.

The operation performed by the COHO can be mathematically expressed as follows. The signal transmitted by the magnetron is

$$s_1 = A_1(t) \cos(2\pi f_t t + \phi_t) \quad 0 \leq t \leq T$$

where: $A_1(t)$ is the amplitude of the pulse

f_t is the transmit frequency

ϕ_t is and the random phase of the transmitter

T is the transmit pulse width

The signal from the local oscillator is

$$s_2 = A_2 \cos(2\pi f_2 t + \phi_2)$$

where A_2 is a constant, and

f_2 is the local oscillator frequency

Figure 2.4.1 Receiver

When these two signals are mixed and low pass filtered, the following is obtained:

$$s_3 = A_3(t) \cos(2\pi(f_1 - f_2)t + \phi_1 - \phi_2) \quad 0 \leq t \leq T$$

where: $A_3(t) = \frac{A_1(t)A_2}{2}$

Here f_3 represents the input signal to the COHO.

The high frequency signal received from a point target can be represented as

$$s_4 = A_4(t) \cos(2\pi f_1 t + \phi_1 - \phi_{TR}) \quad t_{01} \leq t \leq t_{01} + T$$

where ϕ_{TR} is the two-way phase angle to the target.

After mixing f_2 and f_4 and low pass filtering, the IF signal becomes

$$s_5 = A_5(t) \cos(2\pi(f_1 - f_2)t + \phi_1 - \phi_2 - \phi_{TR}) \quad t_{01} \leq t \leq t_{01} + T$$

where $A_5(t) = \frac{A_4(t)A_2}{2}$

Now using the COHO as the final local oscillator, s_6 (which is equal to s_3) and s_5 are mixed and low pass filtered to yield a coherent baseband return signal.

$$s_7 = A_7(t) \cos(\phi_{TR}) \quad t_{01} \leq t \leq t_{01} + T$$

where: $A_7(t) = \frac{A_5(t)A_6}{2}$

Notice that this signal is not dependent on the random phase of the magnetron. Hence the COHO has eliminated the random phase component of the transmit pulse, thereby making the return signal coherent.

There are certain limitations placed on the type of signal that the COHO can lock on to. The locking signal should ideally be of constant frequency for a specified period of time as illustrated in Figure 2.4.2. By the

Figure 2.4.2 Theoretical COHO Lock Pulse

appropriate down-conversion process, it should be guaranteed that the IF of the transmit pulse be as close to the free running frequency of the COHO as possible. If this is not met, a phase lock would still occur as long as the input frequency is within the injection locking bandwidth of the COHO. A certain amount of phase run corresponding to the frequency difference between the two signals multiplied by the two way travel time will be superimposed on the coherent return.

If a chirp is present on the transmit pulse, the COHO will still phase lock to this signal as long as its frequency is within the injection locking limit. The coherent baseband return will have a phase offset associated with it, this offset being equal to the phase run between the COHO and magnetron chirp

multiplied by the two way time of travel, Δt , to the target. Mathematically, this can be expressed as

$$\Delta \phi(t) = (f(t) - f_{\text{COHO}}) \Delta t \quad 0 \leq t \leq T$$

Most magnetron pulses experience a chirp only at the beginning and end of each transmit pulse. This chirp is mainly due to the switching characteristics of the magnetron. To obtain good locking stability, it must be ensured that the COHO phase locks to a point located in the chirp free portion of the pulse and that the frequency of this portion is close to that of the free running COHO.

Apart from performing the aforementioned locking function, COHOs have several other features which vary from one system to another. These features usually aid in the testing of the COR unit. The keyed COHO is similar to a normal COHO, the difference being that the oscillator is quenched prior to the injection of the locking signal. The operation of a typical keyed COHO is described below.

When a signal reaches the COHO input, it is used to generate an injection locking signal which forces the oscillator to follow its frequency and phase. The duration of this injection locking is a function of the transmit pulse width and the amount of chirp on the pulse. The injection locking

signal is used to ensure that the COHO locks on to the chirp free portion of the pulse. Once the locking signal is removed the COHO reverts to its free running frequency while retaining the phase of the locking point. The COHO keeps oscillating in this fashion until it is quenched before the start of the next transmit pulse. The presence of quenching usually produces better locking performance as it forces the oscillator to start from rest. Figure 2.4.3 illustrates the timing signals associated with a keyed COHO.

Figure 2.4.3 Keyed COHO Timing

2.5 Matched Filter Correlator

A filter whose frequency response maximizes the output peak signal to mean noise power is known as a matched filter. The following derivation will illustrate the impulse response, $h(t)$, required to obtain the matched filter criteria.

The output voltage of a filter with a frequency response function $H(f)$ is:

$$|s_0(t)| = \left| \int_{-\infty}^{\infty} S_1(f) H(f) e^{j2\pi ft} df \right|$$

where $S_1(f)$ is the Fourier transform of the input signal $s_1(t)$. The output noise power is

$$N = \frac{N_0}{2} \int_{-\infty}^{\infty} |H(f)|^2 df$$

where N_0 is the input noise power per unit bandwidth.

Assume that

$$|s_0(t)|_{\max} = |s_0(t = T)|$$

The ratio that has to be maximized is

$$R_f = \frac{|s_0(t)|^2_{\max}}{N} = \frac{\left| \int_{-\infty}^{\infty} S_1(f) H(f) e^{j2\pi f T} df \right|^2}{\frac{N_0}{2} \int_{-\infty}^{\infty} |H(f)|^2 df}$$

Schwartz's inequality states that if P and Q are two complex functions, then

$$\left| \int P^* Q dx \right|^2 \leq \int P^* P dx \int Q^* Q dx \quad (2.5.1)$$

Let

$$P^* = S_1(f) e^{j2\pi f T}$$

and

$$Q = H(f)$$

now using the fact that

$$\int A^* A dx = \int |A|^2 dx$$

the following is obtained

$$\left| \int_{-\infty}^{\infty} S_1(f) H(f) e^{j2\pi f T} df \right|^2 \leq \int_{-\infty}^{\infty} |S_1(f)|^2 df \int_{-\infty}^{\infty} |H(f)|^2 df$$

Therefore

$$R_f \leq \frac{\int_{-\infty}^{\infty} |S_1(f)|^2 df \int_{-\infty}^{\infty} |H(f)|^2 df}{\frac{N_0}{2} \int_{-\infty}^{\infty} |H(f)|^2 df} = \frac{\int_{-\infty}^{\infty} |S_1(f)|^2 df}{\frac{N_0}{2}}$$

From Parseval's theorem, we have

$$\int_{-\infty}^{\infty} |S_1(f)|^2 df = \int_{-\infty}^{\infty} s_1^2(t) dt = E$$

where E is the signal energy.

Therefore we have

$$R_f \leq \frac{2E}{N_0}$$

The frequency response which maximizes R_f may be obtained by noting that the equality sign in equation 2.5.1 applies when

$$P = KQ \tag{2.5.2}$$

where K is a real constant.

Now if

$$P^* = S_1(f) e^{j 2 \pi f T}$$

then

$$P = S_1^*(f) e^{-j 2 \pi f T}$$

Also, letting $Q = H(f)$ and substituting for P and Q in equation 2.5.2, we have

$$S_1^*(f) e^{-j 2 \pi f T} = K H(f)$$

Therefore

$$H(f) = S_1^*(f) e^{-j 2 \pi f T}$$

where K has arbitrarily been set to 1.

Now

$$H(f) \xrightarrow{f} h(t)$$

where

$$\begin{aligned} h(t) &= \int_{-\infty}^{\infty} H(f) e^{j 2 \pi f t} df \\ &= \int_{-\infty}^{\infty} S_1^*(f) e^{-j 2 \pi f T} e^{j 2 \pi f t} df \\ &= \int_{-\infty}^{\infty} S_1^*(f) e^{j 2 \pi f (t - T)} df \\ &= \int_{-\infty}^{\infty} S_1^*(f) e^{-j 2 \pi f (T - t)} df \\ &= \left[\int_{-\infty}^{\infty} S_1(f) e^{j 2 \pi f (T - t)} df \right]^* = s_1^*(T - t) \end{aligned}$$

The impulse response $h(t)$ required to obtain the matched filter criteria is

$$h(t) = s_1^*(T - t)$$

The matched filter output is given as

$$Y(f) = S(f) H(f)$$

where $S(f)$ is the Fourier transform of the return signal. Hence

$$Y(f) = S(f) S_1^*(f) e^{-j2\pi fT}$$

In the time domain, this gives

$$y(t) = \int_{-\infty}^{\infty} s(\tau) h(t-\tau) d\tau = \int_{-\infty}^{\infty} s(t-\tau) h(\tau) d\tau = s(t) * h(t)$$

where the asterisk implies the convolution of the two signals.

As shown earlier

$$h(t) = s_1^*(T-t)$$

Hence

$$h(t-\tau) = s_1^*(T-t+\tau)$$

and

$$y(t) = \int_{-\infty}^{\infty} s(\tau) s_1^*(T-t+\tau) d\tau = s(t) * s_1^*(T-t)$$

but

$$s(t) * s_1^*(T-t) = s(t) \star s_1^*(t-T)$$

where $\star$ implies the cross correlation of the two signals

$$y(t) = s(t) \star s_1^*(t-T) \quad (2.5.3)$$

Equation 2.5.3 illustrates the fact that the matched filter output represents the cross correlation between the complex conjugate of the transmit signal and the receive signal [5, 6]. Substituting equation 2.2.3 into this equation, the following is obtained

$$y(t) = \left[\cos \omega_{11} t * \sqrt{\frac{(ct)^2}{4} - h^2} \right] P_r(t) \theta_B \cdot \left[\cos \omega_{11} (t - T) \right]^* \quad t \geq \frac{2h}{c}$$

The return signal is the time convolution of the transmit signal with the time function that represents the spatial extent of the target. The cross correlation of these two signals enables the coherent phase to be extracted from each range bin.

Now, the transmit signal is

$$s_1(t) = A(t) e^{j(\omega_t t + \phi_t)}$$

where ϕ_t is the random phase of the transmitter, and

ω_t is the downconverted IF of the transmit pulse.

The received signal from a point target can be represented as

$$s(t) = B(t) e^{j[\omega_t t - \phi_{TR} + \phi_t]}$$

where ϕ_{TR} is the phase given by

$$\frac{4\pi d}{\lambda}$$

where λ is the transmitted signal wavelength, and

d is the distance to the target.

Therefore

$$s_1^*(T - t + \tau) = A(T - t + \tau) e^{-j\omega_t(T - t + \tau) - j\phi_t}$$

and

$$s(\tau) = B(\tau) e^{+j[\omega_t\tau - \phi_{TR}] + j\phi_t} \quad 0 \leq \tau \leq T$$

Therefore

$$y(t) = \int_{-\infty}^{\infty} A(T - t + \tau) B(\tau) e^{-j\omega_t T + j\omega_t t - j\omega_t \tau - j\phi_t} e^{j\omega_t \tau - j\phi_{TR} + j\phi_t} d\tau$$

$$\int_{-\infty}^{\infty} A(T - t + \tau) B(\tau) e^{+j[\omega_t(t - T) - \phi_{TR}]} d\tau$$

Now, at $t = T$

$$y(T) = e^{-j\phi_{TR}} \int_0^T A(\tau) B(\tau) d\tau$$

Therefore the phase at this output point is

$$y_\phi(T) = -\phi_{TR} = -\omega_{11} t_{01}$$

If the transmit and receive signals are both downconverted to baseband before the matched filter operation is performed, then in the above derivation ω_t is equal to zero, and the following result is obtained

$$y(t) = e^{-j\phi_{TR}} \int_0^T A(T-t+\tau) B(\tau) d\tau$$

Therefore the phase of this signal is

$$y_\phi(t) = -\phi_{TR} = -\omega_{11} t_{01} \quad 0 \leq t \leq 2T$$

Therefore it is seen that if the matched filter operation is performed at baseband, the correct phase output is obtained not only for $t = T$, but for all time corresponding to the overlap of the two signals. This is due to the fact that at baseband there is no phase run across the transmit and receive pulses. Therefore the correlation operation yields COR performance for all instances during which the two signals are overlapped.

A matched filter is often approximated by using an implementation of a correlator such as a digital tapped delay line. This type of structure is illustrated in Figure 2.5.1.

Figure 2.5.1 Digital Tapped Delay Line Correlator

Here the transmit pulse is digitally sampled and stored in locations a_0 through a_N , where a_0 represents the first sample and a_N the last. These samples form the multiplying coefficients of the filter. The input enters the tapped delay line from the left and moves one position to the right with every clock cycle. During each clock cycle, the digital correlator multiplies each coefficient with its corresponding tapped delay line input and passes this result to the accumulator. The accumulator sums all individual results and passes them to the output.

A practical implementation of a coherent matched filter system requires that each signal sample be broken down to its in-phase and quadrature phase components as follows:

$$s(t) = I_r(t) + jQ_r(t)$$

$$s_1(T-t) = I_t(T-t) + jQ_t(T-t)$$

Therefore

$$s(t) \cdot s_1^*(T-t) = I_r(t) \cdot I_t(T-t) + Q_r(t) \cdot Q_t(T-t) + j[Q_r(t) \cdot I_t(T-t) - I_r(t) \cdot Q_t(T-t)] \quad (2.5.4)$$

$$\begin{aligned} &= \int_{-\infty}^{\infty} s(\tau) s_1^*(T-t+\tau) d\tau \\ &= \int_{-\infty}^{\infty} [(I_r(\tau) + j Q_r(\tau)) \{I_t(T-t+\tau) + j Q_t(T-t+\tau)\}^*] d\tau \\ &= \int_{-\infty}^{\infty} I_r(\tau) I_t(T-t+\tau) d\tau + \int_{-\infty}^{\infty} Q_r(\tau) Q_t(T-t+\tau) d\tau \\ &\quad + j \left[\int_{-\infty}^{\infty} Q_r(\tau) I_t(T-t+\tau) d\tau - \int_{-\infty}^{\infty} I_r(\tau) Q_t(T-t+\tau) d\tau \right] \quad (2.5.5) \\ &= I'(t) + j Q'(t) \end{aligned}$$

Therefore the phase ϕ equals

$$y_\phi(t) = \arctan \left[\frac{Q'(t)}{I'(t)} \right]$$

Equation 2.5.4 is made up of four components. The first two components form the in-phase value of the result, and the latter two form the quadrature value. A practical implementation of this equation would require four digital tapped delay line correlators, with the first two correlator outputs being fed into a summer while the latter two correlator outputs are fed into a subtractor. A conceptual block diagram of such a system is illustrated in Figure 2.5.2 [7].

It should be noted that if only one intrapulse sample of the transmit pulse is retained by the correlators, the matched filtering process reduces to the complex multiplication of the receive signal with the transmit pulse sample. Such a system can be implemented using a commercially available complex multiplier.

Figure 2.5.2 Conceptual Design of FIR FILTER System

CHAPTER III   TRANSMITTER INTRAPULSE PHASE ANALYSIS

3.1   Introduction

As mentioned in Section 2.3, the intrapulse phase characteristics of the transmitter are of great importance to a Coherent-On-Receive Subsystem, as this determines the complexity of the COR Subsystem required to achieve good locking stability. The primary objectives of an intrapulse phase analysis is to determine the intrapulse chirp (as a function of the position within the pulse), and to evaluate the phase stability of the transmitter. Once these two factors have been assessed, the characteristics of the transmitter can be matched to a suitable COR Subsystem.

This chapter presents the general characteristics of the coaxial magnetron used in this thesis, also a detailed description of the magnetron intrapulse phase analysis is provided.

3.2   General Characteristics of the Magnetron

The magnetron/modulator unit evaluated in this thesis was built by the Microwave Division of Varian Microwave Incorporated. Both the magnetron and modulator are housed and operated as a single unit. The general characteristics of this unit are given in Table 3.2.1.

Table 3.2.1 General Characteristics of the Magnetron (VMX1615/VMX 3410)**ELECTRICAL**

Warm up time	3 minutes
Filament voltage (standby)	13.75 V
Filament voltage (operating at 800 Hz)	12.00 V
Average magnetron current (at 800 pps)	4.75 mA min 5.62 mA max
Peak RF power	200 kW

TRIGGER

Amplitude	15 V $\pm$ 5 V
Duration	250 ns $\pm$ 50 ns
Rise time, 10 - 90%	20 ns max
Fall time, 10 - 90%	20 ns max

PULSE REPETITION FREQUENCY

Pulses per second(pps), nominal	800
Frequency range	8600 MHz to 9400 MHz

DETECTED PULSE WIDTH

Nanoseconds (max/min)	260/220 ns

ENVIRONMENTAL

Temperature(operating)	-15 to +55 °C
Temperature(non-operating)	+55 °C
Altitude	sea level to 20,000 ft

As the pulse width and peak output power of the transmitter play an important role in the parameters of the system (as mentioned in Section 2.3) these values were measured and compared with the manufacturer's specifications. It was observed that the transmit pulse was amplitude modulated and had a fast rise time and a slow fall time. Also, the entire pulse was measured to be 350 ns in length, with a 3 dB width of 226 ns. This compared favourably with values quoted by the manufacturer of 220 to 260 ns. Figure 3.2.1 shows the magnetron transmit pulse downconverted to an intermediate frequency of 30 MHz.

Figure 3.2.1 Magnetron IF Pulse Output

The peak transmitted power can also be obtained for comparison with the manufacturer's specifications by using the following equation:

$$P_t = \frac{P_{av}}{T f_p}$$

where P_t is the peak output power

T is the pulse width

P_{av} is the average output power

f_p is the PRF

With the test setup illustrated in Figure 3.2.2, the average power reading at the power meter was measured as -4.7 dBm. The average power from the magnetron can be then calculated as:

$$\begin{aligned} P_{av} &= -4.7 \text{ dBm} + 10 \text{ dB} + 40 \text{ dB} = 45.3 \text{ dBm} \\ &= 33.88 \text{ W} \end{aligned}$$

Using the 3 dB pulse width, T , of 226 ns and the pulse repetition frequency of 800 Hz, the peak transmit power of the magnetron is found as:

$$P_t = \frac{33.88}{226 \cdot 10^{-9} \cdot 800} = 82.73 \text{ dB} = 187.5 \text{ kW}$$

The peak power quoted by the manufacturer is 200 kW. The difference between these two values is probably due to the aging of the magnetron as well as errors associated with the measured quantities.

**Figure 3.2.2 Test Set -up for Measuring the Average Output Power
from the Magnetron**

3.3 Experimental Setup for the Magnetron Intrapulse Phase Analysis

To analyze the intrapulse characteristics of the magnetron, the test setup illustrated in Figure 3.3.1 was used. An attenuated sample of the magnetron output was first obtained by means of a 40 dB coupler placed between the magnetron output and the microwave load. This signal was then attenuated using two 20 dB attenuators and fed to an Aventek Mixer, where it was downconverted to baseband using a synthesized signal generator. The two 20 dB attenuators ensured that the signal level reaching

the mixer was within its linear operating range. The output of the mixer was then low pass filtered and sampled at a rate of 200 MHz using a Le Croy waveform digitizer. The signals required to operate the digitizer were generated by a Le Croy waveform generator.

The timing signals used in this setup are illustrated in Figure 3.3.2. The digitizer was operated in the burst mode so that it sampled the input data only when the STOP signal was high (+5 V). The signal fed to the High Level Input was 10 ns wide and had an amplitude of 10 V. Its function was to act as a marker, which when present, was superimposed on the data input channel. This signal was coincident with the STOP signal and due to its large amplitude, its presence had the effect of saturating the sampling A/D, thereby functioning as a marker between consecutive transmit samples. The STOP signal was set to a width of 400 ns, thereby enabling the digitizer to capture the entire transmit signal. A delay of 6.7 μ s was observed between the input of the magnetron trigger signal and its actual firing. Due to this delay the STOP and High Level Input signal were delayed by 6.7 μ s with respect to the magnetron trigger pulse.

Figure 3.3.1 Test Configuration for Magnetron Phase Analysis

Figure 3.3.2 Timing Signals for Magnetron Phase Analysis

A 200 ns pulse with an amplitude of 12 V was required for the trigger pulse to fire the magnetron. This signal had to be provided to the magnetron at the required pulse repetition frequency. Since the output from the Le Croy waveform generator was limited to 10 V, the START signal which triggered the magnetron was provided using a second, triggered signal generator (HP 214 A) which could provide the necessary drive.

The digitizer was run continuously until its 64 K memory was completely filled. Then, this data was transferred to a personal computer via an HPIB bus and stored on floppy disks. The digitizer and the Le Croy waveform generator were both operated from the same PC using the Catalyst/Easywave Software.

3.4 Data Processing and Results

The data gathered from the Le Croy digitizer was analyzed using a Fortran software program. This program analyzed all the data to obtain the envelope of the sample signal. This was done by taking the first 64 samples from each output signal and searching for the highest and lowest values among these samples. This search yields 64 low values which constituted the lower portion of the sample envelope and 64 high values which represented the upper portion of the envelope. Each set of values were placed in a one dimensional array that was 64 samples in length. Using these arrays the DC

offset and peak values for each of the 64 envelope sample points were calculated. The 64 amplitude values of each chirp output (397 pulses in all) was then normalized by dividing each sample by its corresponding peak value. Then the phase of each of these values was calculated by taking the inverse cosine function of each of the normalized amplitudes. This is illustrated in Figure 3.4.1. A constant phase term was removed from each chirp output leaving only the phase ripple. Then the mean and standard deviation of this phase ripple was calculated for each sample point. The mean represents the average phase run through the pulse while the standard deviation indicates the repeatability of the output pulse or in other words, the phase stability of the magnetron. The results are presented in Table 3.4.1 and illustrated in Figures 3.4.2, 3.4.3 and 3.4.4

$$\theta(t_1) = \text{Arccos} \frac{A_1}{A(t)}$$

Figure 3.4.1 Phase Analysis of Magnetron Output

Table 3.4.1 (Sheet 1) Peak Amplitude, Mean and Standard

Deviation Values for Magnetron Output

	A	B	C	D
1	TIME	AMPLITUDE	STD	MEAN
2	(NS)	A/D LEVELS	DEG	DEG
3	15	81	28.87	-3.37
4	20	109	4.51	2.2
5	25	109.5	3.84	0.82
6	30	106.5	3.16	-0.23
7	35	105	3.86	-0.49
8	40	105	3.14	0.08
9	45	106.5	2.92	-0.17
10	50	106.5	2.1	0.29
11	55	107.5	2.24	0.49
12	60	107	2.15	0.01
13	65	106.5	1.86	0.19
14	70	107.5	1.78	-0.08
15	75	107.5	1.91	-0.29
16	80	107	1.89	0.06
17	85	107.5	2.37	-0.41
18	90	107.5	2.16	0.16
19	95	107.5	2.39	-0.47
20	100	106.5	2.16	-0.3
21	105	106.5	1.87	-0.55
22	110	107	0	0
23	115	106	1.63	0.9
24	120	106	2.12	-0.54
25	125	105.5	2.12	-0.51
26	130	105	1.95	-0.79
27	135	104.5	2.33	-0.73
28	140	103.5	2.42	-0.89
29	145	103.5	3.03	-1.54
30	150	102.5	3.46	-1.44
31	155	101.5	4.21	-1
32	160	100.5	4.97	-1.49
33	165	98	5.8	-2.05
34	170	96.5	6.76	-2.57
35	175	94	7.65	-2.88
36	180	92	8.36	-3.66
37	185	89.5	9.31	-3.78
38	190	87.5	9.91	-3.91
39	195	84.5	10.64	-4.49
40	200	81.5	11.11	-5.07
41	205	78	11.56	-5.21
42	210	75	11.73	-5.84
43	215	71.5	11.82	-5.84
44	220	66.5	10.92	-7.08
45	225	62	10.4	-7.19
46	230	57.5	9.45	-7.36
47	235	52	9.04	-8.2
48	240	47.5	7.93	-8.06

**Table 3.4.1 (Sheet 2) Peak Amplitude, Mean and Standard
Deviation Values for Magnetron Output**

	A	B	C	D
4 9	245	43	9	-6.93
5 0	250	40.5	10.3	-6.81
5 1	255	37.5	13.73	-8.23
5 2	260	33	19.07	-5.73
5 3	265	30.5	24.74	-4.86
5 4	270	28.5	29.61	-5.06
5 5	275	25.5	36.3	-6.63
5 6	280	22.5	43.32	-6.43
5 7	285	20	49.34	-6.99
5 8	290	10	53	-8.54
5 9	295	16	59.68	-12.37
6 0	300	13.5	63.91	-13.8
6 1	305	12	65	-16.12
6 2	310	10.5	68.67	-13.01
6 3	315	8.5	73.14	-11.99
6 4	320	7.5	75.63	-12.87
6 5	325	6	82.56	-16.56
6 6	330	6	79.39	-21.32
6 7	335	5.5	78.02	-24.4

Figure 3.4.2 Magnetron Pulse Amplitude vs Time

Figure 3.4.3 Magnetron Mean Phase vs Time

Figure 3.4.4 Magnetron Phase Standard Deviation vs Time

3.5 Discussion

The presence of chirp can be detected by the variation of the mean phase with respect to time. From Figure 3.4.3 it is seen that the mean fluctuates significantly over the first 25 ns and the last 190 ns (i.e., $t = 140$ to $t = 330$), thus the output is seen to contain significant amounts of chirp in these regions.

The standard deviation indicates the phase stability of the output pulse. Figure 3.4.4 indicates that the output is within 4 degrees standard deviation for a 140 ns period beginning 25 ns from the start of the pulse. Therefore this region exhibits good phase stability on a pulse to pulse basis.

The peak pulse amplitude is presented in Figure 3.4.2. The amplitude of the pulse is large and very nearly constant for a 150 ns period commencing 25 ns from the start of the pulse. This indicates that a large portion of the output power is resident within this region of the pulse.

It should be noted that the accuracy of the above measurement and analysis is dependent upon the signal amplitude. The higher the peak amplitude, the more accurate is the normalized values and hence the phase. Thus the results obtained for the latter portion of the pulse where the amplitude is small (i.e. $t > 250$ ns) may be in error. This analysis shows that

the output signal contains a relatively chirp free, phase stable portion, 150 ns in length, commencing 25 ns after the start of the pulse. As the signal amplitude in this portion is large, it indicates that this chirp free portion has a substantial amount of power associated with it. Therefore the power return from this region of the pulse would also be relatively strong. The presence of this phase stable, chirp free region allows for the use of a COHO for Coherent-On-Receive purposes.

CHAPTER IV   COHERENT OSCILLATOR

4.1   Introduction

The analysis of the magnetron intrapulse chirp revealed the presence of a relatively chirp free, stable frequency region in the magnetron output pulse. This region was seen to be 140 ns long, beginning 25 ns after the start of the pulse.

The presence of this stable region enables the system designer to use a coherent oscillator (COHO) for Coherent-On-Receive (COR) purposes. In particular the phase stability in this region allows the COHO to accurately lock on to the random phase in this portion of the pulse, thereby acting as a reference signal which can be used to coherently down-convert the receive data.

This chapter introduces the general characteristics of the COHO evaluated in this thesis; it also presents a detailed discussion on the testing performed to evaluate the phase locking characteristics of the COHO using both the magnetron and a signal generator. These characteristics are later used for comparison purposes in the evaluation of the Finite Impulse Response Filter and the One Coefficient Multiplier in Chapter V.

4.2 General Characteristics of the COHO

The coherent oscillator (COHO) evaluated in this body of work was designed by Gould/3DBM. The general operating specifications for this device are given in Table 4.2.1 and are briefly described below.

A block diagram of the COHO is provided in Figure 4.2.1. The COHO input lock pulse at J5 should have a nominal frequency of 30 MHz and a nominal length of at least 200 ns. In addition the peak power of this signal should be between -6 and 0 dBm. The COHO output signal level at J2 is set at 0 dBm and has a nominal frequency of 30 MHz. The oscillator quench trigger input at J8 should be provided to the COHO at the pulse repetition rate. It should be a logic high pulse (i.e. +5 V) with a minimum duration of 150 ns. This pulse triggers a monostable which produces a 3 μ s quench pulse. For this reason the input trigger should precede the lock pulse by 3 μ s. The output J6 and J7 indicate the presence of the injection locking signal (RF PULSE), and the presence of the quenching signal (LOCK GATE) respectively. Both these signals are logic high TTL level signals. The output at J4 provides a series of input pulse replicas at 12.23 μ s intervals. These pulses are used in the testing of the COR system.

Table 4.2.1 Characteristics of the COHO

ELECTRICAL

Input frequency	30 MHz $\pm$ 1.5 MHz
Pulse to pulse frequency stability	20 kHz max
Input signal level	0 to -6 dBm
Input impedance	50 Ω
System range time	667 μ s max
Quench signal time	3 μ s
Trigger time	100 ns
Output signal level	0 dBm

DIMENSIONS

Length	7.81 inches
Height	4.66 inches
Depth	1.45 inches
Weight	2 lbs

ENVIRONMENTAL

Operating temperature	-15 to +40 $^{\circ}$ C
Storage temperature	-55 to +55 $^{\circ}$ C
Operating altitude	20,000 ft max

POWER REQUIREMENTS

Voltage supply lines	+5, +15, -15 V dc

The COHO lock pulse input at J5 is split by a 3-way splitter. The first output from this splitter is directed to the detection circuitry which acknowledges the presence of the input by applying an injection locking signal to the locking circuitry. A replica of this locking signal is provided at J6 (RF PULSE). The locking circuitry uses this signal to injection-lock the oscillator to the input signal (which it obtains from the second output of the 3-way splitter). Once the locking signal is removed the oscillator reverts to its free running frequency while retaining the phase of the locking point. The output of the oscillator is split and applied to J2 (OUTPUT1) and J3 (OUTPUT2).

The third output from the 3-way splitter is applied to an echo delay line which produces replicas of the input signal at $12.23\ \mu\text{s}$ intervals and applies these to J4. Figure 4.2.2 illustrates this output.

The oscillator is quenched $3\ \mu\text{s}$ prior to each transmit pulse by a trigger input at J8 (COHO GATE). Quenching ensures that the oscillator is started with the correct phase at each pulse repetition interval. In addition a replica of this input is applied to J6 (LOCK GATE). For the proper operation of the COHO it must be ensured that the lock gate signal (J6) ends within the RF pulse output (J7).

A more detailed description of the COHO is provided in Appendix A1.

Figure 4.2.1 Keyed COHO

Figure 4.2.2 COHO Delay Line Output

4.3 Testing the COHO

The performance of a COHO is dependent upon its phase locking accuracy and its phase stability while free running during the receive time interval.

Since the intrapulse frequency characteristic varies from one type of transmitter family to another, the phase locking accuracy of a COHO is dependent largely upon the transmitter employed. On the other hand, the phase stability of the COHO is dependent upon the single side band noise characteristics of its oscillator. Both of these characteristics have to be addressed when testing a COHO [8].

The phase locking accuracy of the Gould COHO was evaluated using both a simulated test pulse (generated by pulse modulating a 30 MHz carrier) and a magnetron signal (downconverted to an IF of 30 MHz).

Figure 4.3.1 (a) illustrates the test configuration used with the simulated test pulse, and Figure 4.3.1 (b) shows the timing signals required for the proper operation of this setup. The 30 MHz carrier from the signal generator was pulse modulated using a single pole double throw (SPDT) switch, the output of which was a 30 MHz pulse. The time extent of this

pulse was determined by the width of the CNT signal input to the SPDT switch. The switch output was split. One output used as a lock test sample for the COHO. The other signal was applied to one input of the I/Q generation circuit through a series of amplifiers and a $2.33\ \mu\text{s}$ delay line. This signal functioned as a return IF pulse. The other input to the I/Q circuit was an amplified version of the COHO output at J2. This signal was amplified to obtain the correct device level for the mixers in the I/Q generation circuit. The I/Q generation circuit shown in Figure 4.3.2 produced an inphase and quadrature phase component for each of the delayed IF pulses. These components were then filtered by two 10.7 MHz low pass filters and displayed on a 100 MHz oscilloscope operating in the x-y mode, thereby providing a Lissajou's figure. Figure 4.3.3 illustrates the Lissajou's figure obtained and Figure 4.3.4 illustrates the filtered inphase and quadrature phase components. The intensity of the oscilloscope was controlled by the z-axis output signal which allowed the screen to be illuminated only when this signal was low.

If the COHO locks on to the test pulse output without any error, the Lissajou's figure would resemble Figure 4.3.5 (a). Notice that in this perfect scenario, the Lissajou's figure is jitter free. If there were a phase run through the test pulse, then this would produce a finite trajectory angle as illustrated in Figure 4.3.5 (b).

Figure 4.3.1 (a) COHO/Simulated Test Pulse Configuration

Figure 4.3.1 (b) Timing Signals for the COHO/Simulated
Test Pulse Configuration

Figure 4.3.2 I/Q Generation Circuit

Figure 4.3.3 Lissajou's Figure from COHO/Simulated Test Pulse Configuration

Figure 4.3.4 I/Q Components from COHO/Simulated Test Pulse Configuration

Figure 4.3.5 (a) Theoretical Jitter-Free Lissajou's Figure

Figure 4.3.5 (b) Lissajou's Figure with a Finite Phase Run

In practice the Lissajou's figure will always have a finite angular extent due to the jitter caused by locking error and the phase run through the pulse. As both of these factors manifest themselves as an angular error, their coexistence makes it difficult to assess the error contributed by each factor. The combined peak to peak error from the two factors in the simulated test pulse case was measured to be equal to 11 deg. If Figure 4.3.3 is examined closely, two white hazy dots can be observed in the upper left hand quadrant. Their angular extent is smaller than the angle which separates them, indicating a small intrapulse phase run in the return pulse. This seems intuitively correct as the simulated test pulse was generated from a 30 MHz frequency stable source. The intensity of the two dots indicates the number of times the COHO locked on to the phase associated with each point. From Figure 4.3.3 it can be seen that the leftmost dot is of greater intensity than the one on the right. This indicates that the COHO usually locks on to the phase associated with the left dot but on occasion it locks to the phase associated with the right dot. The haze around each dot indicates the error associated with locking on to each point. A major portion of the locking error in this system is due to the COHO locking to two distinct phases. This locking error which was measured to be equal to 7.0 deg may have been caused by switching transients (introduced by the pulse modulating switch) corrupting the input signal. Also note that the COHO was designed for operation with a

magnetron pulse which starts from zero and builds up in amplitude, whereas the modulated pulse begins at any random amplitude (random phase) within the peak to peak limit of the signal.

Figure 4.3.6 (a) illustrates the test configuration used with the X-band magnetron, and Figure 4.3.6 (b) the timing associated with this setup. The X-band output of the magnetron was down-converted to a nominal IF of 30 MHz by using an X-band synthesized signal generator as a local oscillator. This signal was then low pass filtered to eliminate mixer harmonics. The signal was then manipulated in the same fashion as was described with the simulated test pulse. The COHO quench pulse and the trigger signal were offset by $6.75 \mu\text{s}$ to account for the firing delay associated with the magnetron. Figure 4.3.7 illustrates the Lissajou's figure obtained for this case, and Figure 4.3.8 illustrates the filtered in-phase and quadrature phase components for the baseband magnetron outputs. The combined locking error and intrapulse phase run was measured to equal to 9 deg.

Unlike the simulated test pulse, here it is very difficult to separate the locking error from the intrapulse phase run. To analyze these two factors more carefully, the setup illustrated in Figure 4.3.9(a) was configured. The timing requirements for this setup are illustrated in Figure 4.3.9(b). This test

Figure 4.3.6 (a) COHO/Magnetron Test Configuration

Figure 4.3.6 (b) Timing Signals for COHO/Magnetron Test Configuration

Figure 4.3.7 Lissajou's Figure from COHO/Magnetron Test

Figure 4.3.8 I/Q Components from COHO/Magnetron Test

set is very similar to that in Figure 4.3.6 (a), the significant difference being that the I/Q circuit outputs were low pass filtered, amplified, digitized and then sampled using a logic analyzer.

The clocks required for the two digitizers and the logic analyzer, along with the trigger required to synchronize the signal generators to the sampling clock, were generated by the timing card. Figure 4.3.10 illustrates the timing card in detail. The system clock was generated by a crystal clock oscillator which was buffered by a 74F244 octal line buffer to provide a greater drive current. The digitizer clocks were obtained from the output of the 74F244. The sample clock was a buffered version of the delayed crystal clock output. The delay could be varied from 4 ns to 74 ns. Two 74F269 8-bit binary counters were tied together to form a 16-bit binary counter which counted up from a preset value to zero. When the counter reached zero, output Q15 went low thereby resetting the device and also providing a 50 ns negative going trigger signal. The trigger signal was buffered using the 74F244 and then input to the TRIGGER INPUT of the pulse generator triggering the magnetron.

Each ECL digitizer was located on an evaluation board (EB101) consisting of an input buffer, 8-bit ECL A/D, clock generation circuit and an

4.3.9 (a) COHO/Magnetron Digitizing Configuration

Figure 4.3.9 (b) Timing Signals for the COHO/Magnetron Digitizing Configuration

Figure 4.3.10 Timing Card Block Diagram

8-bit ECL D/A. The TTL clock inputs to the evaluation boards were converted to an ECL level by the clock generation circuit. These clocks were then used to sample the input data.

The logic analyzer (Tektronics 1240) consisted of three 9-channel pods. Two of these pods were used to sample the A/D outputs, while the third pod was used to sample the system clock and the detected COHO quench pulse (J6), which acted as a trigger signal for the logic analyzer. The sampling clock was delayed such that valid data would be present at the A/D outputs on its falling edge.

Using this setup the inphase and quadrature phase channels were digitized at 50 ns sampling intervals (20 MHz clock). Data for 75 transmit pulses were gathered by photographing the relevant portions of state table outputs displayed on the logic analyzer. One transmit sample is illustrated in Figure 4.3.11. The data relating to the I/Q pulses on each photograph was manually converted from its hexadecimal to decimal equivalent. Then, using a fortran software program the data for each transmit pulse was entered into a separate file. Finally, each of these files were transferred to another program which calculated the phase at each sample point in the pulse, and produced the mean and standard deviation for each of these points over all 75

transmit samples. The results of this analysis are illustrated in Table 4.3.1

TIMING
DIAGRAM

CURSOR2 = 111
CURSOR = TRIG
CURSOR = 111

KNOB=

HIGHLIGHT:

ACTIVE MEM: ACQMEM

LOC TRIG CH01 CH02

104	0	03	FF
105	0	01	FF
106	0	03	FF
107	0	05	FF
108	0	04	FF
109	0	08	FF
110	0	08	FF
111	0	01	FF
112	0	08	FF
113	0	05	FF
114	0	07	FF
115	0	07	FF
116	0	06	FF
117	0	04	FF
118	0	08	09

NEXT
HIGHLIGHT

SWITCH
DISPLAY TO

ACQMEM
TO

Figure 4.3.11 COHO/Magnetron Sample Data

Table 4.3.1 COHO/Magnetron Phase Locking Results

BIN#	AMPLITUDE	MEAN VALUE DEG	STD DEG
1	43.8	230.0	1.64
2	75.0	224.9	1.37
3	82.0	224.2	1.35
4	78.0	225.2	2.17
5	64.9	226.0	2.63
6	32.5	205.3	5.56

The phase stability of the free running COHO was analyzed using the power spectral density (PSD) plot of its output, illustrated in Figure 4.3.12. Using this plot, the single side band (SSB) noise characteristic was obtained as a function of frequency, and approximated by three straight lines. This is represented by the solid curve in Figure 4.3.13. If the peak phase deviation is much less than 1 radian then the phase noise spectral density can be obtained by adding 3dB to the SSB noise plot. The phase noise curve is illustrated by

the dashed line in Figure 4.3.13. Similarly, this curve was approximated by three straight lines having the following equations:

$$y_1(f) = 7.95 \times 10^{-3} f^{-2.4} \quad 100 \text{ Hz} \leq f \leq 1000 \text{ Hz}$$

$$y_2(f) = 7.24 \times 10^{-8} f^{-0.72} \quad 1000 \text{ Hz} \leq f \leq 5000 \text{ Hz}$$

$$y_3(f) = 1.31 \times 10^{-4} f^{-1.6} \quad 5000 \text{ Hz} \leq f \leq \infty$$

The phase variance of the COHO (which develops over one receive interval of the radar) was calculated by integrating the phase noise plot from $\frac{1}{T'}$ to infinity; where T' is the two-way travel time to the maximum range (100 km).

Therefore

$$\begin{aligned} \sigma^2 &= \int_{1500}^{5000} y_2(f) df + \int_{5000}^{\infty} y_3(f) df \\ \sigma^2 &= \int_{1500}^{5000} 7.24 \times 10^{-8} f^{-0.72} df + \int_{5000}^{\infty} 1.31 \times 10^{-4} f^{-1.6} df \\ &= 8.03 \times 10^{-7} + 1.32 \times 10^{-6} = 2.12 \times 10^{-6} \text{ rad}^2 \end{aligned}$$

Hence the standard deviation of this error, σ , is found to be

$$\sigma = 0.0015 \text{ rad} \quad = 0.083 \text{ deg}$$

Figure 4.3.12 COHO Power Spectral Density

Figure 4.3.13 COHO SSB Noise Characteristic

From these results it is seen that the phase error of the COHO due to the SSB phase noise of the oscillator is extremely small and does not contribute appreciably to the total locking error.

4.4 Discussion

The mean locking phase of the COHO is seen to vary by less than 2 degrees in the central 150 ns portion of the pulse. The locking ability is seen to degrade in the first and last 50 ns of the output pulse: this can be attributed to the chirp present in these portions of the pulse. The standard deviation in the phase is also less than 5 degrees for the first 250 ns of the pulse, hence the locking characteristics of the COHO to the magnetron output is very good during the centre portion of the pulse. As the performance of the COHO with the transmitter cannot be any better than the frequency characteristics of the transmitter itself, the results obtained in Chapter 3 (Table 3.4.1) should compare favourably with those in Table 4.3.1. The results from these two sources seem to be in agreement for the first 130 ns of the magnetron output. Beyond this point, Table 4.3.1 seems to yield better results than those presented in Chapter 3. Intuitively, this does not seem correct. One possible reason for this discrepancy may be due to the way in which the data in Chapter 3 was analyzed. It was mentioned in Section 3.5 that the error associated with this analysis is inversely proportional to the pulse amplitude.

As the pulse amplitude does decrease quite sharply in the region where the discrepancy exists, this could be one possible source of error. Another reason may be due to the use of two different transmitters (same model but different units) to collect the data in these two chapters. Due to equipment constraints, the same transmitter could not be retained for the entire course of this thesis. If the intrapulse frequency characteristics of the two transmitters are different, then this could explain the discrepancy between the two sets of data.

The latter method of analyzing the COHO locking characteristics yields more accurate results than those obtained by examining the Lissajou's figure. Using this method, the intrapulse phase run in the high power region of the pulse (first 250 ns) was observed to be 5.8 deg, while the average phase locking error was calculated to be 1.8 deg. This yields a combined error of 7.6 deg, which is very close to the 9 deg observed using the Lissajou's figure.

CHAPTER V   FINITE IMPULSE RESPONSE (FIR) FILTER

5.1   Introduction

In the past, COR systems have almost always been built using a coherent oscillator (COHO). The digital matched filter scheme represents an emerging alternative implementation for the COR system. The matched filter stores a replica of the transmit pulse by collecting samples within the pulse and uses these to perform a correlation operation with the return signal. The matched filtering is carried out by using a digital Finite Impulse Response (FIR) filter (see Section 2.5).

5.2   Selection of a FIR Filter

The theory of matched filtering as it applies to a COR system is dependent on the proper correlation of the transmit and receive data. Therefore, the selection of a suitable correlator chip is of primary importance to the matched filter implementation. The criteria for selection are listed in terms of descending importance, as follows:

i)   Internal correlation implementation

The correlation process is implemented differently by different manufacturers of FIR filters. In practice, certain implementations are

easier to work with than others.

ii) Speed of devices

The clock determines the throughput of the device . For proper operation of the matched filter system, it is required that the input signals be sampled at the same clock rate as that applied to the device. The clock rate is decided by the number of intrapulse transmit/receive samples that are to be gathered in a given period of time. A larger number of intrapulse samples provides a better description of the input data which in turn leads to a more accurate characterization of the correlation output.

iii) Order of the filter

This indicates the number of filter cells (taps) in the FIR filter. In the coherent matched filter implementation, the number of data samples captured during the transmit cycle dictates the order of the filter implementation. It must be ensured that the order of the FIR filter is equal to or greater than the number of transmit coefficients. The filter cells whose coefficient registers are not loaded with a transmit sample should be set to zero to prevent them from latching noise which would lead to a corruption of the output data. The number of coefficients

captured by the system is governed by the sampling rate as well as the time extent of the magnetron output pulse. For a given sampling rate, a narrow output pulse implies a smaller number of coefficients while a wider pulse implies the converse.

iv) Number of devices required

The number of devices that are required for this implementation determines the total area required for these chips on any test structure (PC board).

Two commercially available FIR filter chips were considered for this design. They are the Zoran ZR33881 and the LSI Logic L64240-A.

The Zoran ZR33881 is a Digital Filter Processor (DFP) chip having a maximum clock rate of 20 MHz. Each filter chip has a length of 8 taps, but several of these devices can be cascaded to achieve higher tap lengths. The DFP provides for both signed and unsigned arithmetic, which are independently selectable for coefficients (transmit data) and return data. The coefficients have to be continuously circulated through the device so that they can be properly multiplied by the input data. Figure 5.2.1 (a) illustrates the conventional implementation of a 4 tap FIR FILTER correlator while Figure

5.2.1 (b) illustrates the Zoran implementation of this structure. In the direct form structure, the outputs from each filter cell are summed together and then latched by the output register of the device. The data moves one filter tap to the right with each clock cycle. The Z^{-1} indicates the one clock cycle delay that exists between the data at consecutive taps. Note that in this implementation the coefficients are stationary.

In the Zoran implementation the data is applied to all the filter taps simultaneously. The coefficients travel through the device by moving one filter tap to the right with each clock cycle. If decimation of the output data is required, then the additional delays indicated by the dashed boxes can be engaged. The output from each filter cell is passed to its associated accumulator which retains a dynamic sum of all its inputs. The multiplexer selects the appropriate accumulator output which is then cleared to make room for new data. Table 5.2.1 illustrates the sequence tables for the conventional and the Zoran implementations. Both implementations yield the same result, but in the conventional design only the return data is applied to the device (the coefficients are stored in the filter taps) while in the Zoran implementation both the coefficients and return data have to be constantly provided to the chip. The coefficients are normally read from a circulating memory buffer.

where n is the sampling time interval
 $n = 0, 1, 2, 3, \dots$

Figure 5.2.1 (a) Conventional Implementation of 4-Tap FIR FILTER

Figure 5.2.1 (b) ZR33881 DFP Implementation of 4-Tap Filter

Table 5.2.1 Sequence Tables for Zoran and Conventional Implementation

ZORAN IMPLEMENTATION						CONVENTIONAL IMPLEMENTATION
CLK 1	Cell 0	Cell 1	Cell 2	Cell 3	Sum/Clear	
0	$C_3 X_0$	$C_2 X_0$	$C_1 X_0$	$C_0 X_0$	Cell 0	$C_3 X_0$
1	$C_0 X_1$	$+C_3 X_1$	$+C_2 X_1$	$+C_1 X_1$	Cell 1	$C_3 X_1 + C_2 X_0$
2	$+C_1 X_2$	$C_0 X_2$	$+C_3 X_2$	$+C_2 X_2$	Cell 2	$C_3 X_2 + C_2 X_1 + C_1 X_0$
3	$+C_2 X_3$	$+C_1 X_3$	$C_0 X_3$	$+C_3 X_3$	Cell 3	$C_3 X_3 + C_2 X_2 + C_1 X_1 + C_0 X_0$
4	$+C_3 X_4$	$+C_2 X_4$	$+C_1 X_4$	$C_0 X_4$	Cell 0	$C_3 X_4 + C_2 X_3 + C_1 X_2 + C_0 X_1$
5	$C_0 X_5$	$+C_3 X_5$	$+C_2 X_5$	$C_1 X_5$	Cell 1	$C_3 X_5 + C_2 X_4 + C_1 X_3 + C_0 X_2$
6	$+C_1 X_6$	$C_0 X_6$	$+C_3 X_6$	$C_2 X_6$	Cell 2	$C_3 X_6 + C_2 X_5 + C_1 X_4 + C_0 X_3$
7	$+C_2 X_7$	$+C_1 X_7$	$C_0 X_7$	$C_3 X_7$	Cell 3	$C_3 X_7 + C_2 X_6 + C_1 X_5 + C_0 X_4$

Where $C_0 \dots C_3$ represents the filter coefficients (transmit data)

and $x_1 \dots x_7$ represents the receive data

The second commercial chip considered for the FIR FILTER design, the L64240-A built by LSI-Logic, is a 64 tap high speed transversal filter processor consisting of two 32 tap sections, with 8 bit wide coefficients and data. This chip has a maximum clock rate of 20 MHz. Each device can accept signed or unsigned data/coefficients. All control signals to the device are double

buffered. This allows the loading of a new set of control signals while processing continues with the current set. The correlation process is implemented using the conventional technique illustrated in Figure 5.2.1 (a). A block diagram of this device is illustrated in Figure 5.2.2. The control signals and filter coefficients enter the device through the C1.0 - C1.7 bus. The coefficients are loaded into the filter taps addressed by the REGADR0-5 inputs. The data enters through any/all of the 8 individual data input buses denoted by the symbols D10 to D17. The order of each filter dictates the number of input data buses accepted by the device. Table 5.2.2 summarizes the various filter lengths that are available and the data buses accepted by each configuration.

Table 5.2.2 Summary of Various Filter Lengths for the L64240-A

	FILTER ORDER	INPUT DATA BUSES
1	1 x 64	D10
2	2 x 32	D10,D14
3	4 x 16	D10,D12,D14,D16
4	8 x 8	ALL

This device has two phases of operation: the power-up initialization phase, and the correlation phase. During the initialization phase the device is loaded with the control/coefficient values. When the device is first powered up, it should always be initialized. Once initialization is complete, input data can be accepted and the correlation process can begin. This is known as the correlation phase. During the correlation process, the outputs of the first four 8 tap filters are summed together and latched in a pipeline register. The sum of the last four 8 tap filters are latched in another register as illustrated in Figure 5.2.2. The outputs of these registers are sign extended in the format control blocks and then may be scaled in the barrel shifter blocks. The outputs of the two barrel shifters are then summed together. This result is delayed by a variable delay of 0 to 8 clock cycles and then added to the partial result bits. The format of this sum may be adjusted by the format adjust block and then latched by the output register. Several of these devices can be cascaded to achieve higher order filters.

After carefully considering the two devices, the L64240-A was chosen for the Coherent-On-Receive design. This decision was mainly based on the internal correlation implementation. As mentioned earlier, the L64240-A uses a conventional form implementation while the ZR33881 uses a technique in which both the coefficients and data have to be simultaneously

applied to the device. As was apparent from Table 5.2.1, the correct synchronization between the return data and the coefficients was essential for proper operation of the Zoran chip. This synchronization requirement is an artifact of the Zoran design and is not required in the conventional implementation.

As mentioned in Section 2.5, the implementation of a coherent matched filter requires 4 FIR filters. Therefore, if the ZR33881 chips are used, four are required. On the other hand, as the L64240-A has two 32 tap FIR FILTERS in each chip, it takes only two of these to implement the design.

Figure 5.2.2 L64240-A Transversal Filter Processor, Block Diagram

5.3 Design Methodology

The first step in any design such as the FIR filter COR subsystem is to define the inputs/outputs to the circuit. Once this is established the circuit can be subdivided into several logical sections. Each of these can then be defined separately. The data flow circuitry should be established first, then the control and timing circuitry can be defined. Finally the user interfaces to the system can be established. Depending on the design, the control circuit may have to be enlarged to accommodate input signals to the user interface.

Once the entire circuit is defined, timing diagrams can be drawn for the system. These diagrams are used to ensure that the proper timing exists between all pertinent signals. Next, each circuit can be designed using the circuit definitions outlined above. Then these circuits can be integrated to form the complete system. The timing diagrams should be rechecked to ensure that no errors have been made during the integration process. Finally the design can be implemented in accordance with the electrical and mechanical constraints of the system [9, 10].

Using this design methodology the FIR FILTER subsystem was designed and implemented. A description of this process is provided in the following section.

5.4 FIR FILTER Design

The input circuitry associated with the FIR FILTER board is responsible for transforming the X-band magnetron output into baseband in-phase (I) and quadrature phase (Q) data, which can then be digitized and sent to the FIR FILTER board. This circuitry also produces a time delayed replica of the magnetron output, which can be used by the system to simulate the return signal. The output circuitry consists of a logic analyzer which captures the 17-bit output from the two correlators.

The input/output circuitry associated with the FIR FILTER subsystem is shown in Figure 5.4.1. The attenuated magnetron output is downconverted to 30 MHz and passed through a 50 MHz LPF. The 30 MHz signal is then split and one signal is sent directly to the I/Q generator circuit which separates the signal into its baseband in-phase (I) and quadrature phase (Q) components. The I/Q components are then filtered, amplified and digitized to ECL levels before being sent to the FIR FILTER board. This signal acts as the magnetron transmit sample. The signal input to the COHO is fed to an echo delay line, which produces attenuated replicas of the input signal at 12.23 μ s intervals. These replicas, which are output at J4, simulate the return signals. From this point onward, the return signals are treated in the same fashion as the transmit signal. The inputs to the FIR FILTER board are

Figure 5.4.1 FIR FILTER Subsystem I/O Circuitry

ECL level I/Q data, and the time interval between transmit and receive pulses is 12.23 μ s.

The data flow is presented in pages 1 through 4 of the FIR FILTER design schematic (contained in Appendix A2). The data (8 bit I/Q) enters the board through the input connectors and are applied to the ECL/TTL converters (U40, U44, U45 and U46) which level shifts the data to TTL values. Then, the data is latched by two octal latches (U31 and U37), the outputs of which are delivered to the random access memories (RAM) (U30, U38, U39, U47). When the I and Q values of the transmit pulse are applied to the system, the RAMs store this data in the locations indicated by the inputs on its address lines, SO-2. In all, eight transmit values are retained by the RAMs.

The correlators are configured in the 2 x 32 mode shown in Table 5.2.2. This allows two correlation processes to be performed simultaneously on one chip, thus only two chips are required to implement the matched filter process. Equation 2.5.4 presents the four correlation terms that need to be implemented.

$$I_r * I_t(T-t) + Q_r * Q_t(T-t) + j\{Q_r * I_t(T-t) - I_r * Q_t(T-t)\} \quad (2.5.4)$$

The first two terms give the I component of the output while the latter two terms form the Q component. The I and Q components are implemented using correlators U3 and U1 respectively. The two correlation processes involved with each I/Q component is performed in the 0th and 4th filter cell blocks of each chip. The Q component involves the subtraction of one correlation component from the other. To achieve this, the quadrature phase transmit data is negated before being applied to correlator U1. The values in the IRAMs (In-phase data storage RAM) are passed through the arithmetic logic units (ALU) and transferred to the 8 coefficient latches of the 0th filter cell block (i.e. FIR 0.0 to FIR 0.7). These filter cells are addressed by the inputs on the REGADR 0-5 pins. This process is repeated with the outputs of the QRAM (quadrature phase data storage RAMs), but in this case ALU U4 negates its input data. These values are stored in the eight coefficient latches of the 4th filter cell block (i.e. FIR 4.0 to FIR 4.7). Prior to the loading of transmit data the 64 coefficient latches of both correlators are loaded with zeros by the control circuit (this occurs during the power up/initialization sequence). This is done to prevent any non-zero values in other filter cells from corrupting the output data. The in-phase return data enters the correlators through DI0.0-7 and DI4.0-7 in U3 and U1 respectively, while the quadrature phase data enters through buses DI0.0-7 and DI4.0-7 in U1 and U3 respectively. Table 5.4.1 illustrates the correlations performed by each chip.

Table 5.4.1 Correlations Performed by DFP Chips

CHIP	FILTER CELL BLOCK	CORRELATION
U1	0	$Q_r * I_t (T-t)$
U1	4	$I_r * Q_t (T-t)$
U3	0	$I_r * I_t (T-t)$
U3	4	$Q_r * Q_t (T-t)$

The two octal latches U6 and U5 collect one I and one Q value respectively, which they transfer to the one complex coefficient multiplier, U2. This chip was added to the FIR FILTER design to compare its performance with that of the correlator chips. The 19 bit outputs from each correlator are transferred to one 64 pin DIN connector, J2, while the 34 bit output (17 I and 17 Q) from the complex multiplier are transferred to another 64 pin DIN connector, J1.

The control circuit illustrated on pages 5 and 6 of the schematic provides all the required signals for the operation of the FIR FILTER board. The control circuit on page 5 consists of two 8-bit counters tied together to form one 16-bit counter. Only the first 10 bits of this counter are used to address the EPROMs (Erasable Programmable Read Only Memories). Each

EPROM is 2K by 8 bits wide and is arranged in pairs. During the normal operation of the FIR FILTER board, only 1K of memory is used from either EPROM; therefore, each EPROM is divided into two 1K memory blocks. Either block can be selected by setting address pin A_{10} to the appropriate value by means of pin 1 on SW1. The position of pin 2 of SW1 determines which EPROM from each pair transfers data onto its common bus. Thus by controlling pins 1 and 2 of SW1, four separate timing patterns can be selected.

EPROMs U14 and U27 store the data required to initialize the two correlators. The initialization data consists of 6 eight bit wide control words followed by 64 zeros which are placed in the coefficient registers of all the filter cells. The output from these two EPROMs are latched by U15 and U28 which provides this data to the coefficient registers of U1 and U3 respectively. As more than one bus is tied to these coefficient registers, signal LT1 is used to ensure that only one device communicates with these registers at any one time. All other EPROM pairs provide control signal for the operation of the FIR FILTER board. Table 5.4.2 provides a brief description of each signal. The EPROMs were programmed using an Inlab 28 EPROM programmer.

The timing and user interface circuits are illustrated on page 6 of the schematic. The output of the crystal clock oscillator is applied to pins 2, 6, 11

and 13 of a line driver which buffers the signals to increase their fanout capabilities. The CLK output from this buffer is sent to the user interface circuitry and also delayed by 35 ns and sent to the two correlators. This delay enables the input data to meet the required setup and hold times of the correlators. The CLK1 output is used to operate the counter and EPROM circuitry while CLK2 is used to drive the input data latches, the complex multiplexer, and the ALUs. One output from the clock oscillator is applied to two variable length delay lines U48 and U49. The outputs of these are buffered by the line driver and sent to output connectors J3 and J5. These two signals act as clock inputs to the two A/Ds. The variable length delays ensure that the proper timing exists between the input data clock (CLK2) and the A/D outputs. Another buffered clock output is attached to output connector J4. This signal is used to drive a timing circuit which synchronizes all the signals required to operate the FIR FILTER board and its associated circuitry.

Table 5.4.2 (Sheet 1) Description of the Control Signals

Signal	Description
ADR0-5	These 6 control lines provide addresses to the correlator for the placement of coefficients and return data during the power up/initialization and correlation sequences. During the former sequence it provides addresses for the insertion of control bits into the control register and also directs the zero coefficients into all 64 coefficient latches. During the correlation sequence it directs the transmit I/Q data into the appropriate coefficient latches.
O0-7	During the power up/initialization sequence it provides the control bits and the 64 zero coefficient values to the correlators.
LT2	During the correlation sequence it latches an in-phase transmit value into U6.
LT3	During the correlation sequence it latches a quadrature phase transmit value into U5.

Table 5.4.2 (Sheet 2) Description of the Control Signals

Signal	Description
OE1-NOT	When this signal is Low it disables the outputs of the IRAMs (in-phase data RAMs). This signal controls the flow of in-phase transmit data to the ALUs.
OE2-NOT	When this signal is Low it disables the outputs of the QRAMs (Quadrature phase data RAMs). This signal controls the flow of quadrature phase transmit data to the ALUs.
LT1	When this signal is Low it allows the EPROMs (U14 and U27) to communicate with the coefficient/control inputs of the correlators. When it is High it allows the ALUs to communicate with the aforementioned inputs.
COEFF-NOT	Input to the COEFF pin of both correlators. When this signal is High the correlators assume the data on its coefficient/control inputs to be control bits, and when Low these inputs are assumed to be coefficients.

Table 5.4.2 (Sheet 3) Description of the Control Signals

Signal	Description
RESET	Input to the RESET pin of both correlators. It is set High during the power up/initialization sequence and Low during the correlation sequence.
BNKLD1	Input to the BNKLD1 pin of both correlators. It loads the coefficients in all filter cells from the Master to the Slave latches.
MR-NOT	Input to the MR-NOT pin of the programmable counter U32. When Low it resets the counter.
CP1-NOT	Input to AND gate U8. When Low, it causes the 16 bit counter to go into the HOLD mode.
ASR1	Input to ALU, U4. When Low, the output of the ALU is a time delayed replica of its input. When High, the output is equal to a time delayed version of the negated input.

Table 5.4.2 (Sheet 4) Description of the Control Signals

Signal	Description
PE1*-NOT	When Low, it causes the counter to reset to address 512.
PAL	This signal is 8 clock cycles in length. It is input to NAND gate U20 along with a delayed version of the CLK signal. The output of the NAND gate (WERAM-NOT) enables each set of RAMs to store 8 data values at their inputs.
WE-NOT	Input to the WE-NOT pin of both correlators, it enables the control bits to be latched into the coefficient registers and the loading of coefficients into the Master latches.
S0-2	Provides address locations to the RAMs in which the I/Q values are stored.

The user interface section consists of reset switch SW7 and trigger input J9. When SW7 is depressed, pin 3 of U33 is forced low, thereby causing P9 (the ninth preset bit of the 16-bit counter) to go low after another two clock cycles. A low on pin 1 of U34 causes its output (PE1-NOT) to go low two clock cycles after the output of SW7 has gone low. When PE1-NOT is low, it causes the counter to be reset to a value determined by P9 which in this case is zero as P9 is low. If P9 were high when PE1-NOT was low, the counter would be reset to 512. The trigger input to the magnetron is split and one signal is sent to J9. The diode CR3 and resistor R4 prevents the voltage of this pulse from exceeding 5 V. The NAND Schmitt trigger output goes low when the trigger pulse is present at its input. The purpose of this chip is to sharply define the edges of the input pulse. The output signal is passed through two flip-flops and sent to a programmable counter which is set to a delay of 6.7 μ s. This delay accounts for the finite time interval between triggering the magnetron and its actual firing. After the 6.7 μ s delay, the output of the counter goes low, thereby allowing the circuit to sample the magnetron output.

A brief description is now provided to illustrate the sequence of events that takes place during the normal operation of the system. On power up, the reset switch SW7 is depressed by the user. This causes the counter which addresses the EPROMs to be set to zero (this marks the beginning of the power

up/initialization sequence). During this sequence, 6 control words are sent to the two correlators. These configure the correlators to the required mode of operation. Next the 64 coefficient latches are loaded with zeros. Then the counter is disabled and the system waits for a transmit pulse trigger to arrive (this marks the beginning of the correlation sequence). The transmit pulse trigger enters the FIR FILTER board through connector J9, and is then delayed by $6.7\ \mu\text{s}$ to account for the latent delay associated with firing the magnetron. At this point the counter is enabled and the transmit I/Q values are stored in the RAMs. These values are then transferred to the filter blocks in each correlator. Finally the counter is disabled once again and the system waits for another transmit pulse trigger. During this period the FIR FILTER system correlates the transmit signal with the return data and delivers the result to connector J2. The complex multiplier which stores one I/Q transmit sample multiplies the stored value with the return data and delivers these values to connector J1. The FIR FILTER system normally operates in the correlation sequence; it only goes to the initialization sequence when SW7 is depressed.

A detailed description of the timing sequence is given in Appendix A2.

This design was implemented on a four layer PCB. The internal layers consisted of the power and ground planes while the horizontal and vertical

track layers were on the outside planes. Most signal/data tracks were 12 mil wide (0.0012") and the minimum spacing between tracks was 10 mil Figure 5.4.2 illustrates the component layout on the PCB.

The problems encountered during the debugging of the FIR FILTER system and the solutions implemented to rectify these difficulties are outlined in Appendix A3.

Figure 5.4.2
FIR FILTER
PCB LAYOUT

5.5 Testing the FIR FILTER Design and Comparison with COHO

The phase locking performance of all three subsystems (FIR FILTER, COHO, and One Coefficient Multiplier) was analyzed using a pulse modulated signal generator and the coaxial magnetron. The test configurations and the timing signals required for each analysis is described below.

TEST 1

The FIR FILTER was tested using a pulse modulated signal generator as shown in Figure 5.5.1(a). The timing signals required for this setup are illustrated in Figure 5.5.1(b). The pulse modulated output from the signal generator was sent to the I/Q generation circuit which divides the signal into its inphase and quadrature phase components. These components were then filtered, amplified and then digitized before being input to the FIR FILTER board. The FIR FILTER outputs were obtained at output connector J2. The HP1650A logic analyzer was used to observe the output of the FIR FILTER (34 channels) and the data input to the I/Q RAMs (8 channels for IRAM and 8 channels for QRAM). The PAL control signal was observed along with the trigger signal for the logic analyzer (pin 6 of chip U8). The logic analyzer samples the output data from this board, while the timing card provided the trigger signal required to synchronize all the pulse generator outputs. The FIR TRIG triggered the FIR FILTER board, while the MOD signal pulse modulated

Figure 5.5.1 (a) FIR FILTER/Signal Generator Set-up

Figure 5.5.1 (b) Timing Signals for FIR FILTER/Signal Generator Set-up

the signal generator to produce the transmit and receive pulses. Data for 70 transmit pulses were obtained, and the phase angle at the point corresponding to the peak output was analyzed (i.e point at which the transmit and receive data overlap completely) for its standard deviation values. When analyzing this data the error due to the finite A/D offsets had to be taken into consideration. Table 5.5.5 illustrates the obtained results.

TEST 2

Next, the FIR FILTER was tested using the magnetron circuit illustrated in Figure 5.4.1. The timing for this circuit is shown in Figure 5.5.2(a). As the transmit pulse window was much larger than the pulse length, the sampling window was positioned as shown in Figure 5.5.2(b). Data for 70 transmit pulses were obtained, and analyzed in the same manner as that done with the aforementioned signal generator pulse samples. Figure 5.5.3 illustrates the sample data obtained for one transmit pulse along with the calculations that were performed to take into account the A/D offset error. Table 5.5.5 illustrates the standard deviation that was obtained.

TEST 3

The COHO was tested using the signal generator setup presented in Figure 5.5.4(a). The timing signals required for this setup are illustrated in

Figure 5.5.2 (a) Timing Signals for FIR FILTER/Magnetron Set-up

Figure 5.5.2 (b) Positioning of Transmit Sample Window

Label Base	> >	POD 1 Hex	PE Hex	PAL Hex	POD3 Hex	(I') POD4 Dec	(Q') POD2 Dec
+0183		01	1	0	00	000438	000203
+0184		01	1	0	01	000405	000159
+0185		02	1	0	00	000425	000213
+0186		01	1	0	01	000437	000264
+0187		02	1	0	01	000355	000236
+0188		11	1	0	01	000317	000219
+0189		2C	1	0	09	000330	000099
+0190		41	1	0	15	000316	131046
+0191		46	1	0	1D	000391	130978
+0192		20	1	0	1C	000882	130598
+0193		24	1	0	0B	002540	130006
+0194		16	1	0	0D	006076	129356
+0195		0A	1	0	F8	010941	129537
+0196		03	1	0	F8	014214	130561
+0197		00	1	0	F9	014413	001137
+0198		DC	1	0	F9	011377	001574
+0199		FA	1	0	FB	007479	001096
+0200		FC	1	0	FD	005048	130654
+0201		FC	1	0	FD	002315	130347
+0202		FC	1	0	FD	130556	129490
+0203		FC	1	0	FD	128710	130591
+0204		FD	1	0	FE	127583	130711
+0205		FD	1	0	FE	127385	130984
+0206		FD	1	0	FE	129733	130638
+0207		FC	1	0	FE	129885	130736
+0208		FD	1	0	FE	129913	130790
+0209		FD	1	0	FE	130030	130787
+0210		FD	1	0	FE	130128	130847
+0211		FC	1	0	FE	130194	130899
+0212		FD	1	0	FF	130166	130920
+0213		FD	1	0	FF	130147	130912
+0214		FD	1	0	FF	130151	130919
+0215		FD	1	0	00	130205	130900
+0216		FD	1	0	F0	130185	130946
+0217		FE	1	0	FF	130195	130991
+0218		FE	1	0	FF	130227	131062

Figure 5.5.3 (Sheet 1) FIR FILTER/Magnetron Sample Data

Average offset error in I

$$\overline{I}_E = \frac{1}{6} \sum_{i=1}^6 I_i = \frac{1}{6} (438 + 405 + 425 + 437 + 355 + 317) = 396.2$$

Average offset error in Q

$$\overline{Q}_E = \frac{1}{6} \sum_{i=1}^6 Q_i = \frac{1}{6} (203 + 159 + 213 + 264 + 236 + 219) = 215.7$$

Therefore at location 197

$$I' = I_{197} - \overline{I}_E$$

$$I' = 14413 - 396.2 = 14016.8$$

$$Q' = Q_{197} - \overline{Q}_E$$

$$Q' = 1137 - 215.7 = 921.3$$

$$\phi_{195} = \arctan \left[\frac{Q'}{I'} \right] = \arctan \left[\frac{921.3}{14016.8} \right] = 3.76 \text{ deg}$$

Figure 5.5.3 (Sheet 2) FIR FILTER/Magnetron Sample Data

Figure 5.5.4(b). This analysis is similar to that performed in Chapter IV, except that a delay line with a longer delay was used. The signal generator was pulse modulated by the MOD signal which produced two 30 MHz pulses. The first acted as the COHO lock pulse, while the second acted as the return, which was sent to the I/Q generation circuit along with the COHO output, J2. The I/Q components formed by this circuit were filtered, amplified and digitized before being captured by the logic analyzer. The clock for the logic analyzer was provided by the FIR FILTER board. Six time bins corresponding to 333 ns of the baseband return were analyzed for 70 transmit pulses. The results are presented in Table 5.5.1. To compare these results with those obtained from the FIR FILTER, an amplitude weighted standard deviation, σ_{aw} , was calculated as follows:

The average amplitude $\bar{A}$ is

$$\bar{A} = \frac{1}{N} \sum_{i=1}^{N=6} A_i = 91.7$$

The amplitude weighted standard deviation, is

$$\sigma_{aw} = \frac{1}{AN} \sum_{i=1}^{N=6} \sigma_i A_i = 2.86 \text{ deg}$$

Figure 5.5.4 (a) COHO/Signal Generator Test Set

Figure 5.5.4 (b) Timing Signals for COHO/Signal Generator Test Set

Table 5.5.1 COHO/Signal Generator Results

BIN#	AMPLITUDE	MEAN VALUE DEG	STD DEG
1	102.6	52.8	2.91
2	93.4	53.0	2.83
3	90.8	53.3	2.77
4	89.4	53.5	2.77
5	88.8	53.9	2.85
6	85.2	53.8	3.02

TEST 4

The COHO was then tested using the magnetron setup illustrated in Figure 5.5.5(a). The timing signals for this setup are given in Figure 5.5.5(b). The magnetron output was attenuated and then downconverted to an intermediate frequency of 30 MHz. Then it was low pass filtered and applied to a two way splitter. One output of the splitter was used as a lock test sample for the COHO, while the other output was sent to the I/Q generation circuit through a SPDT switch. The purpose of this switch was to connect the I/Q

generation circuit to either the splitter or the COHO output, J4. The outputs from the I/Q generation circuit were low pass filtered, amplified and then digitized before being captured by the logic analyzer. The MAG TRIG was used to fire the magnetron, while the FIR TRIG triggered the FIR FILTER board. The CNT signal controlled the position of the SPDT switch. The clock from the FIR FILTER board was used by the A/Ds and the timing circuit board. The I/Q output of the A/Ds were observed using the logic analyzer which was triggered using the COHO QUENCH output at J6. Seventy transmit samples were analyzed in the same manner as that used when analyzing the COHO/Signal Generator data. The results are shown in Table 5.5.2. The amplitude weighted standard deviation for this data was calculated to be 3.52 degrees.

Figure 5.5.5 (a) COHO/Magnetron Test Configuration

Figure 5.5.5 (b) Timing Signals for COHO/Magnetron Test Configuration

Table 5.5.2 COHO/Magnetron Test Results

BIN#	AMPLITUDE	MEAN VALUE DEG	STD DEG
1	17.5	248.8	11.8
2	53.6	234.1	4.45
3	87.0	226.2	1.89
4	96.4	221.0	1.43
5	79.2	217.5	3.52
6	50.2	224.8	6.46

TESTS 5 and 6

The One Coefficient Multiplier was also tested with both the signal generator and the magnetron. The test setups used are similar to those used for analyzing the FIR FILTER. Figure 5.5.6 illustrates the sample data obtained for one magnetron pulse and also the calculations that were performed to account for the finite DC offset errors. The results obtained for this device when used with the signal generator and magnetron are given in Table 5.5.3 and 5.5.4 respectively. If the results for the multiplier/signal generator

Label Base	> >	POD 1 Hex	PE Hex	PAL Hex	POD3 Hex	(I') POD4 Dec	(Q') POD2 Dec
+0181		02	1	0	06	000952	130896
+0182		02	1	0	06	000952	130896
+0183		02	1	0	05	000952	130896
+0184		03	1	0	05	001048	131048
+0185		08	1	0	0D	000952	130896
+0186		12	1	0	29	001104	130800
+0187		21	1	0	48	000800	130992
+0188		33	1	0	59	000952	130896
+0189		3B	1	0	54	001104	130800
+0190		37	1	0	34	001104	130800
+0191		2A	1	0	15	000952	130896
+0192		1C	1	0	02	001048	131048
+0193		0E	1	0	01	002744	131040
+0194		05	1	0	F8	007960	129872
+0195		00	1	0	FA	014112	129176
+0196		FC	1	0	FD	018424	130280
+0197		FD	1	0	FC	018432	000904
+0198		FD	1	0	B8	013184	003368
+0199		FD	1	0	01	007224	004368
+0200		FE	1	0	01	002992	004064
+0201		FE	1	0	01	001496	002032
+0202		FE	1	0	01	130336	001528
+0203		FE	1	0	01	130160	000576
+0204		FF	1	0	01	130232	130752
+0205		FE	1	0	01	130176	131000
+0206		FE	1	0	02	119840	006456
+0207		FE	1	0	01	130936	130520
+0208		FF	1	0	02	131032	130672
+0209		FF	1	0	03	131032	130672
+0210		FF	1	0	02	131032	130672
+0211		FF	1	0	02	131032	130672
+0212		FF	1	0	02	000056	130824
+0213		FF	1	0	02	131032	130672
+0214		FF	1	0	02	000112	130576

Figure 5.5.6 (Sheet 1) One Coefficient Multiplier/Mage tron Sample Data

Average offset error in I

$$\bar{I}_E = \frac{1}{6} \sum_{i=1}^6 I_i = \frac{1}{6} (952 + 952 + 952 + 1048 + 952 + 1104) = 993.3$$

Average offset error in Q

$$\bar{Q}_E = \frac{1}{6} \sum_{i=1}^6 Q_i = \frac{1}{6} (130896 + 130896 + 130896 + 131048 + 130896 + 130800) = 130905.3$$

but

$$131072 = 0$$

Therefore

$$130905 = -166.7$$

At location 195

$$I' = I_{195} - \bar{I}_E = 14112 - 993.3 = 13118.7$$

and

$$Q' = Q_{195} - \bar{Q}_E = -1896 - (-166.7) = -1729.3$$

Therefore

$$\phi_{195} = \arctan \left[\frac{Q'}{I'} \right] = \arctan \left[\frac{-1729.3}{13118.7} \right] = -7.51 \text{ deg}$$

The phases at locations 195 through 200 were calculated in this way.

Figure 5.5.6 (Sheet 2) One Coefficient Multiplier/Magnetron Sample Data

(Table 5.5.3) are observed, it can be seen from the amplitude of the multiplier output that valid data is only present for the first 4 sample points. Therefore when analyzing this data only the first 4 samples should be considered. The σ_{aw} for these results was calculated to be 4.33 degrees. The amplitude weighted standard deviation was calculated to be 8.59 degrees when used with the magnetron.

All the above results are presented in Table 5.5.5.

Table 5.5.3 One Coefficient Multiplier/Signal Generator Test Results

BIN#	AMPLITUDE	MEAN VALUE DEG	STD DEG
1	17982	89.2	5.69
2	18873	88.4	3.83
3	18617	89.2	2.13
4	16844	89.3	4.03
5	1297	-38.9	80.3
6	1773	-86.1	28.8

Table 5.5.4 One Coefficient Multiplier/Magnetron Test Results

BIN#	AMPLITUDE	MEAN VALUE DEG	STD DEG
1	12815	100.6	6.04
2	17378	94.8	5.03
3	18306	87.4	7.64
4	14449	79.1	12.3
5	8842	56.6	12.5
6	5404	31.8	12.8

Table 5.5.5 Test Results for all Three Subsystems

	FIR FILTER	COHO	MULTIPLIER
	σ deg	σ_{aw} deg	σ_{aw} deg
SIGNAL GENERATOR	2.49	2.86	4.00
MAGNETRON	5.23	3.52	8.59

CHAPTER VI CONCLUSION

6.1 Conclusion

The magnetron intrapulse phase measurement and analysis undertaken in this thesis demonstrated the presence of a chirp free, phase stable region 25 ns from the start of the pulse for the magnetron employed. The existence of this stable region allows for the use of a Coherent-On-Receive subsystem in conjunction with the magnetron in coherent radar applications.

Three Coherent-On-Receive subsystems were then evaluated; a commercially available COHO, and two novel digital designs called the FIR FILTER, and the One Coefficient Multiplier. All gave good results during all or parts of the baseband output when used in association with the signal generator. The standard deviation of the amplitude weighted phase ($\sigma_{a\omega}$) for the COHO was 2.86 degrees. This small value resulted in good locking performance throughout the baseband return. The FIR FILTER achieved a standard deviation for its phase of 2.49 degrees, while the One Coefficient Multiplier had a $\sigma_{a\omega}$ of 4.00 degrees.

When used in association with the magnetron, the COHO yielded a $\sigma_{a\omega}$ of 3.52 degrees while the FIR FILTER had a phase locking standard deviation of 5.23 degrees, and the One Coefficient Multiplier a $\sigma_{a\omega}$ of 8.59 degrees. Hence, the locking performance of the FIR FILTER is seen to rival that of the COHO while retaining the flexibility to work in a more highly chirped situation.

The COHO does not provide this flexibility, as exhibited by its performance in the middle of the pulse, but degraded locking performance at the extremities where it suffers from chirp. Similarly, the locking performance of the One Coefficient Multiplier is reasonably good during the first part of the pulse but deteriorates towards the latter part where the signal chirp becomes more prominent

In summary, the COHO performed superbly with both the signal generator and the magnetron, while the FIR FILTER achieved excellent locking characteristics with the signal generator and acceptable performance with the magnetron. The One Coefficient Multiplier performed moderately well with the signal generator. With the magnetron, its locking performance was seen to degrade severely in the regions where chirp was present.

In conclusion, the phase errors for the COHO and the FIR FILTER were measured to be within 6 degrees, which is an acceptable value for Coherent-On-Receive systems. This shows that both of these devices can be successfully employed in a radar system which incorporates this class of coaxial magnetron as the transmitter.

6.2 Future Studies

As the transmit sample window used by the FIR FILTER is much longer than the transmit signal, the FIR FILTER captures the entire transmit pulse along with some noise due to the switching characteristics of the magnetron. It is conceivable that if the transmit sample window is shortened and the system is made to sample only the 3 dB region of the pulse, the results obtained would be better than those presented in Table 5.5.5. The locking performance of this subsystem could be evaluated at one sample decrements.

Also the COHO, FIR FILTER and the One Coefficient Multiplier should be evaluated with a waveform that contains a significant amount of chirp. It is expected that in such an analysis the locking performance of the FIR FILTER would surpass those of the other two devices. This hypothesis is based on the fact that the FIR FILTER retains several intrapulse samples of the

transmit signal. Hence it would be able to phase lock to the return more accurately than the COHO or the One Coefficient Multiplier which samples the transmit signal at only one point.

Appendix A1

OPERATION OF THE COHO

The internal circuitry of the COHO is illustrated in Figure A.1.1.

The COHO lock pulse at J5 is a 30 MHz IF sample of the magnetron output. This input is split by a 3-way splitter DC1. The first output from pin 2 of DC1 is input to the base of transistor Q6 where it is amplified and detected by the active detector Q7. This pulse can be seen at test point 3 (TP3).

Transistor Q7 saturates and allows transistor Q8 to turn off thereby allowing pin 2 of the monostable multivibrator U2A to go high. The rising edge of this input triggers U2A which remains in this state for the time period determined by R31, R32 and C46. In this case it was set to 100 ns. R31 can be adjusted to set the injection signal pulse width to the desired length which in turn is influenced by the magnetron intrapulse characteristics. When U2A is triggered, its Q output goes high thereby sending the output of the NAND gate U3C low. This enables transistor Q1 for the duration of injection signal generated by U2A. Q1 is also enabled by gates U3A and U3D and either signal will keep Q1 active. The NAND gate U4D is at a logic high while U2A is triggered. This output can be observed at J6 (RF PULSE).

Figure A.1.1

COHO Circuit

The second output from DC1, on pin 5, is applied to the delay line DL1. The signal passes through the delay line and is input to the base of Q1 which when enabled amplifies this signal and synchronizes the oscillator to the phase of the input pulse. The oscillator which consists of Q3 and its associated components will oscillate in phase with the input pulse until Q1 is turned off at which point it will revert to its natural oscillating frequency while still retaining a direct phase relationship with the original input signal. The oscillator can be adjusted using the coarse adjust C23 and the fine adjust C25. The emitter follower Q4 provides isolation between the oscillator and the amplifier Q5. Q5 amplifies the signal which is then passed through a filter consisting of C39-41 and L5. This signal is then split by DC2 which applies the two outputs to J2 and J3.

The oscillator is quenched 3 μ s before the start of the next RF pulse by the input at J8 (COHO GATE). Quenching ensures that the oscillator can be restarted at the correct phase at each pulse repetition interval. When the COHO GATE signal is present at the input to U2B, it triggers this gate thereby sending the Q output of this device high. The period of time for which it remains triggered is determined by R37, R38 and C47. For this device it was set at 3 μ s. The inputs to the NAND gate U3A are Q from U2B and Q-NOT from U2A. When either or both of these inputs are high, it sends the output

of this gate high, which keeps transistor Q2 turned off. When both inputs to U3A are high simultaneously, it sends U3A low which in turn turns on Q2. This causes Q2 to conduct thereby heavily loading the tuned circuit and quenching the oscillator. This occurs only during the 3 μ s when Q of U2A is high and Q-NOT of U2B is high. When an input pulse is present at J5, it triggers U2A which sends Q-NOT low and produces a high on the output of U3A thereby turning Q2 off. When Q2 is turned off, the oscillator begins to oscillate. It is important that the input lock pulse is present and properly aligned when the oscillator begins oscillating. The correct timing is achieved by adjusting DL1. The delay line compensates for the finite delay encountered in the U2A path.

The pulse width of U2A is adjusted such that it is less than that of the transmitted pulse. This is done so as to turn off Q1 before the end of the input pulse. As the magnetron turns on and off, its output experiences an undesirable phase run at the beginning and end of each transmit pulse. Therefore Q1 should be turned off in the middle of each pulse so that the oscillator locks on to a relatively chirp-free portion of the input signal.

The Q-NOT output from U2B is fed to the two inputs of the NAND gate U4C, the outputs of which go to J7 (LOCK GATE). For proper operation of the COHO, it must be ensured that the Lock Gate at J7 end within the RF

Pulse at J6. If this criterion is not met, the COHO will not correctly memorize the phase of the transmit pulse. If J7 ends before the rising edge of J6, then the oscillator is turned on before the lock pulse is present at its input. On the other hand, if J7 turns off after J6, then the oscillator will start with the correct phase but would be quenched during the time J6 is low and J7 is high. These effects are illustrated in Figure A.1.2.

The third output from DC1 is input to the base of transistor Q9. When this transistor is enabled by transistors Q11 and Q12, it amplifies this signal and applies it to the base of transistor Q10 and also to the echo delay line DL2. Q11 is enabled by gate U3B during the triggering of U2B and the time delay caused by capacitor C57. The delay line produces a series of pulses each separated from the next by 12.23 μ s time intervals. The amplitude of these pulses decreases with time as illustrated in Figure 4.2.2. The original pulse and those produced by the delay line are input to the base of transistor Q10 which amplifies and outputs them at J4 (LOCK TEST SAMPLE). Q12 controls Q9 and Q10 and is in turn controlled by the Lock Test Control located on the input connector. When this signal is left open, -15 V is applied to the base of Q12 which turns it off. When the lock test control is high Q12 is turned on thereby enabling Q9 and Q10. The outputs at J4 can be used to test the phase locking characteristics of a COHO/transmitter combination.

Figure A.1.2 Incorrect Positioning of Signals J6 and J7

Appendix A2

FIR FILTER TIMING

The circuit timing is explained to provide a better understanding of the sequence of events that takes place within the circuit during its normal operation. On power up, the reset switch SW7 is depressed. This causes the counter to be set to zero which in turn is applied to the EPROM address inputs. (This marks the beginning of the power up/initialization sequence.) On the next rising edge of the clock, this address is latched by the EPROMs and on the following clock cycle, valid data is present on all the EPROM outputs. After the second clock cycle in this sequence, the MR-NOT signal goes low for two clock periods, thereby resetting the programmable counter U32. Then, EPROMs U14 or U27 (depending on the selected chip) begin to output the control coefficients and one clock cycle later, EPROM U13 or U26 (depending on the selected chip) outputs the address locations into which the control coefficients are to be placed (i.e. inputs to REGADR 0-5 pins on the correlator chips). The one clock cycle delay between the control bits and their address values is due to the octal latches U15 and U28. This data is loaded into the correlators at a rate four times slower than the input clock rate. In all, 6 control bits are loaded into each device.

The WE-NOT pulse to the correlators are sent low at appropriate times, this loads the control bits into the appropriate master latches asynchronous to the clock. The COEFF signal is held high until the loading is complete. This signal is sent to the COEFF-NOT pins of the correlators. When this signal is high, it denotes that control bits are being loaded into the correlators. If it is low, it denotes the loading of data into the coefficient latches. The loading of the control bits is finalized by activating the BNKLD1 control signal which is held high for 4 clock cycles. This allows the synchronous transfer of data from the master to the slave latches. Next, the zero's are loaded into all 64 coefficient latches. As in the previous case, EPROM U13 or U26 provides the valid addresses while the coefficients are provided by EPROM U14 or U27. The loading takes place at one quarter of the input clock rate. Once all 64 values have been loaded, these values are simultaneously transferred from the master to the slave latches. This completes the power up/initialization sequence, under normal operation the circuit will perform this sequence only when the reset switch SW7 is depressed. At all other times, it will be cycling through the correlation sequence which will be explained below.

At the end of the power up/initialization sequence, the PE1-NOT* is set low for one clock cycle. This causes PE1-NOT to go low thereby resetting

the counter to location 512. After one clock cycle, the EPROM outputs the data at location 512. At location 512, the Control signal CP1-NOT goes high. This causes the CEP-NOT input of the 16-bit counter (U9 and U22) to go high thereby "freezing" the counter at location 513 (this marks the beginning of the correlation sequence). The counter remains in this state until the trigger input at J9 causes Q1 to go low. This enables the counter by setting CEP-NOT low. The PAL signal is set high as the counter resumes incrementing. This signal is input to a NAND gate (U20) along with a delayed version of the CLK output. The output of the NAND gate forms the write enable pulse (WERAM-NOT) to the RAMs. When this signal is low, the RAMs store the I/O transmit pulse samples at its inputs in locations specified by the control signals SO-2. The MR-NOT signal is once again held low for two clock cycles thereby resetting the counter and sending Q1 high. Then, the control signal LT1 is set high, this disconnects the coefficient/control inputs of the correlators from the EPROMs and connects them to the ALUs. The in-phase data in the RAMs are passed through the ALUs and sent to the master latches of the eight coefficient locations of the 0th filter cell block L64240-A chips. During the transfer of data, LT2 goes high, latching one of the in-phase components into U6. After the transfer of the I data, the ASR1 control signal goes high. When this signal is high, the ALU (U4) delivers the negated input signal. The quadrature phase data is passed through the ALUs and entered

into the master latches in locations 32 through 39. During this data transfer, LT3 goes high, thereby capturing the quadrature phase value corresponding to the in-phase value present at the output of U6. This value is stored in latch U5. Once all the coefficient values are entered into the correlators, they are transferred to the slave latches.

Finally, PE1-NOT* goes low for one clock cycle making the counter jump to location 512. Once again, the counter "freezes" at location 513 until a trigger input arrives at J9 during the next pulse repetition interval. Until then, the FIR FILTER system correlates the input coefficients with the return data and outputs these values to connector J2.

Figure A.2.1
FIR FILTER SCHEMATIC
 sheet 1

Figure A.2.1
FIR FILTER SCHEMATIC
 sheet 2

Figure A.2.1

FIR FILTER SCHEMATIC

sheet 3

Figure A.2.1

FIR FILTER SCHEMATIC

sheet 4

Figure A.2.1

FIR FILTER SCHEMATIC

sheet 4

Figure A.2.1

FIR FILTER SCHEMATIC

sheet 5

Figure A.2.1

FIR FILTER SCHEMATIC

sheet 6

Appendix A3

DEBUGGING OF THE FIR FILTER DESIGN

This design was debugged using a bottom-up debugging approach. The timing circuit which was used by all the other circuits was the first to be debugged. Then the user interface circuit which controls some of the vital functions of the control circuit was tested. Next, the functioning of the control circuitry was analyzed in association with the other two circuits. Finally, the data flow circuitry was tested with the rest of the circuitry.

The crystal clock oscillator and its associated circuitry was put in place and the delay lines were adjusted to give the required offsets. Then the user interface circuitry was installed and switch SW7 was tested along with control signal outputs P9 and PE1-NOT. A pulse was input at J9 and the output Q1 (chip U42) was observed. Initially, the desired output was not observed. This problem was traced to the programmable counter, U32. Contrary to what was stipulated in the data sheets for this device, the WE-NOT input signal (pin 12) must be taken low for at least one clock cycle after the chip is powered up. This enables the data on pins D0-16 to be latched into the device. To ensure a low on WE-NOT, it was tied to the output pin of the switch SW7. Then the control circuitry (16 bit counters and the EPROMs) was put in place. Only one

EPROM from each pair was inserted into the board (i.e. U10, U11, U12, U13 and U14). It was felt that both chips would not be required for debugging purposes. As the Inlab 28 EPROM programmer could not program the CY7C245A-18WC chips these were replaced by the CY7C245-25WC. These chips were pin to pin compatible with the CY7C245A-18WC, the only difference being that their address setup time was 7 ns greater than in the former chip. This 7 ns difference presented no problem with the timing requirements of the system.

Once the control/timing circuitry was in place each data flow arm of the FIR FILTER design was debugged separately. A constant amplitude pulse and having a time extent of 300 ns was provided by a pulse generator. This pulse was digitized and input to the I channel of the FIR FILTER board. Using a logic analyzer (HP1650A) the input and output of the ECL/TTL converters were observed to ensure the proper conversion of data from the ECL to TTL levels. Then the input latch (U31) was examined along with the outputs from the IRAMs (U30 and U39). The IRAM output consisted of eight separate values corresponding to the data previously observed at the input latch (U3). This indicated that the input data was being stored and delivered correctly from the IRAMs. Once this was established, the output of ALU U4 was observed. Initially, this output was seen to be incorrect. This problem was traced to two pin settings on the ALU. The first problem dealt with two

unconnected pins (L5 and K7). Pin L5 was an output enable pin for a register that was not used and pin K7 was a register clear pin which also was not used by the ALU when configured in the manner required for this design. Both pins were tied high as illustrated in the schematic. The second problem dealt with pin A5 which had been incorrectly tied to high when it should have been tied low. This pin enabled the clock to Register B which was an essential component in the ALU configuration. The absence of this clock was the reason for the incorrect data at the ALU output. The quadrature data arm was also debugged in a similar fashion. The setup used to test this portion of the circuit is illustrated in Figure A.3.1. When the circuit was powered up with the correlator chip U1 in place, this chip was seen to draw approximately 200 mA more than it should under normal operating conditions. Upon consulting an erratum distributed by the manufacturer it was discovered that the RESET pin input to the device should be held low when the circuit is powered up, and should remain low until the device has been initialized. Failure to comply with this requirement leads to an excessive current draw by the device. To meet this requirement the circuit shown in Figure A.3.2 was constructed.

Figure A.3.1 Test Set for Evaluating Correlator Performance

Figure A.3.2 RESET Circuitry for FIR FILTER Subsystem

When this circuit is powered up the RESET output is pulled low by the 10 k Ω resistor. Once the momentary contact switch is pressed it turns ON the LED, which, in turn, turns ON the transistor, thereby setting the RESET output high. The LED keeps the transistor ON, thereby maintaining a high level on the RESET output until the circuit is powered down. The RESET pins of the two correlators were disconnected from the EPROMs and connected to the RESET output of the optocoupler circuit.

The new power up/initialization sequence is as follows:

- 1) Power up circuit
- 2) Depress SW7 (This initializes the correlators)

- 3) Depress SWA (RESET goes high and remains in this state until the circuit is powered down)

The setup used to test the correlators is illustrated in Figure A.3.3. In this setup PULSE1 acts as the transmit pulse and PULSE2 acts as the receive pulse. Using this setup the outputs from each correlator were observed along with the input data to the circuit. The input data was correlated manually and compared with the correlator output data. The two sets of data were seen to agree with one another. Therefore the correlators were judged to be working correctly.

The outputs of the One Coefficient Multiplier were assessed to be incorrect. The problem was due to the data buses being connected to the wrong input pins. The One Coefficient Multiplier performs a 12 by 16 bit multiplication out of which it retains only the most significant 16 bits of the result. Therefore, by tying the data buses to the least significant 8 bits of each input, most of the desired result was lost. To rectify this matter, all data buses were tied to the most significant 8 bits of each input. The rest of the pins on each input were tied to ground. Once these corrections were made, the output from this device was correct.

Figure A.3.3 Test Set for Evaluating Performance of Both Correlators

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