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Hot Carrier Induced Degradation and Gamma Radiation Induced Degradation in SiGe HBTs and VCOs

by

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Abstract

Reverse-bias electrical stressing causes degradation of the base current and current gain of SiGe HBTs. Two types of hot carrier stressing were used in this study: open-collector (OC) stressing and forward-collector (FC) stressing. Gamma irradiation results in changes to the HBT collector current similar to the changes seen during electrical stressing. Reverse-bias electrical stressing causes damage in the base-emitter (BE) junction while irradiation causes damage in both the BE junction and the base-collector (BC) junction. Gamma irradiation of transistors also causes degradation in the phase noise of voltage controlled oscillators (VCOs) made from SiGe HBTs.

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Abbreviations

^{60}Co	Cobalt-60
α_R	Reverse Common Base Gain
$\Delta\omega$	Frequency Offset from VCO Carrier Frequency
ω_0	Frequency of Oscillation
Al	Aluminum
As	Arsenic
β	DC Current Gain
β/β_0	Normalized Current Gain
B	Boron
BBT	Band-to-Band Tunneling
BC	Base Collector
BE	Base Emitter
BED	Base-Emitter Diode
BiCMOS	Bipolar-Complementary Metal-Oxide Semiconductor
BJT	Bipolar Junction Transistor
CS	Collector and Substrate of HBT are connected
CVD	Chemical Vapour Deposition
ECL	Emitter Coupled Logic
E_g	Band-gap Energy
ES	Emitter and Substrate of HBT are connected
f	Frequency
F	Excess Noise
FC	Forward-Collector

FET	Field-Effect Transistor
FG	Forward Gummel
FIB	Focused Ion Beam
f_{max}	Maximum Oscillation Frequency
f_T	Unity Gain Cut-off Frequency
Ge	Germanium
GND	Ground
HBT	Heterojunction Bipolar Transistor
IC	Integrated Circuit
I_C	Collector Current
I_{CFC}	Collector Current for FC Stressing
I_{FC}	Forward Collector Stress Current
I_{OC}	Open Collector Stress Current
JFET	Junction Field Effect Transistor
k	Boltzman's Constant
MOS	Metal-Oxide Semiconductor
n	Ideality Factor
n_B	Base Current Ideality Factor
N_{IN}	Input Noise Power
N_{OUT}	Output Noise Power
OC	Open-Collector
PN	Phase Noise
P_{peak}	VCO Peak Power
P_s	Power in Oscillator Tone
P_{SSB}	Single Sideband Offset Power
RF	Radio-Frequency
RG	Reverse Gummel
RTS	Random Telegraph Signals
Si	Silicon
SiGe	Silicon Germanium

SIMS	Secondary Ion Mass Spectroscopy
SiO ₂	Silicon Dioxide
SRH	Shockley-Read-Hall Recombination
TAT	Trap-Assisted Tunneling
TTF	Time To Failure
TTL	Transistor-Transistor Logic
UHV	Ultra-High Vacuum
V_A	Early Voltage
V_{BC}	Base Collector Voltage
V_{BE}	Base Emitter Voltage
V_{bi}	Built-in Junction Voltage
V_{CC}	Supply Voltage (Input)
VCO	Voltage Controlled Oscillator
V_{osc}	Oscillation Voltage
V_{out}	VCO Single Sided RF Output Voltage
V_{tank}	VCO Tank Voltage (Input)
V_{tune}	VCO Tuning Voltage (Input)

Chapter 1

Introduction

1.1 Background

1.1.1 Silicon Germanium Technology

Germanium (Ge) can be added to the base of a silicon (Si) bipolar junction transistor (BJT) to form a heterojunction bipolar transistor (HBT). A heterojunction is a junction created between two semiconductors with different bandgaps. Heterojunctions are used in designing devices such as field-effect transistors (FETs), semiconductor lasers, and bipolar transistors [1]. While silicon (Si) integrated circuits (ICs) are highly effective in the design of high-density, low-speed, high-volume applications they are not effective for high-frequency radio frequency (RF) and microwave circuit applications. These applications usually use high-speed III-V semiconductor technologies that can be bandgap engineered for the required application. So while Si ICs are cheaper they cannot do the job of the more expensive III-V technologies alone. The addition of Ge to Si bipolar transistors was intended to allow bandgap engineering in Si and improve the performance of the Si transistors so as to make a technology competitive with the III-V semiconductors in the high-frequency and RF markets [2]. The attempt was successful and SiGe HBTs are now being marketed for wireless networks, RF applications, optical transmission applications, mobile networks, and high speed ICs [3].

The addition of SiGe to Si BJTs is used to improve the dc current gain (β), Early voltage (V_A) and unity gain cut-off frequency (f_T) as well as the maximum oscillation frequency (f_{max}) compared with Si BJTs [2]. In addition to increasing the previously mentioned characteristics, improvements in noise characteristics have also been noted. The improvements in SiGe HBTs over Si BJTs are a function of the transistor design as well as the Ge content and profile [4], [5].

Si BiCMOS, combining bipolar transistors with a CMOS process, was first developed in the mid 1980s [6]. This allowed the integration of high-density MOS logic with the current-driving capabilities of bipolar transistors. BiCMOS is especially useful for buffering and driving [7]. SiGe BiCMOS is the further improvement of Si BiCMOS through the integration of high-speed SiGe HBTs. SiGe HBTs, with their improved performance, can be more competitive price-wise than Si bipolar transistors when integrated into BiCMOS [8]. SiGe circuits are now cost effective compared with III-V circuits.

1.1.2 Reverse-Bias Electrical Stress

Reverse-bias electrical stressing occurs when the base-emitter (BE) junction of a bipolar transistor is reverse biased. Reverse-bias stress in polysilicon emitter BJTs causes degradation of the bipolar gain, due to an increase in the base current. The degradation has been studied since the early work of [9] and [10], and is generally understood to arise from damage by hot carriers of the Si/SiO₂ interface around the emitter perimeter. Work on SiGe devices [11] and references therein, and [12] has shown that the effects are very similar to results in Si BJTs [13], [14]. This is not surprising since the SiGe technology is based on Si BJT technology and the addition of the SiGe base layer is done with the aim of preserving most of the basic features of the underlying Si technology.

In bipolar circuits reverse-bias stressing is known to occur in emitter-coupled logic (ECL) circuits and transistor-transistor logic (TTL) circuits. In ECL circuits stressing occurs in the base-emitter (BE) junction of the multiple fan-in input transistors when the inputs are not in phase and the logic swing of the circuit is greater than $V_{be(on)}$. If the logic swing is less than $V_{be(on)}$ then reverse-bias stressing is not an issue in an ECL circuit. In TTL circuits one of the input transistors will experience stressing anytime the inputs to a gate are not in phase. In both cases the size of the reverse-bias experienced by the stressed device is the difference between the logic swing and $V_{be(on)}$ [15].

In BiCMOS circuits the bipolar transistors can experience transient reverse-bias stress when the gate switches from high to low. There is a delay between when the input (V_{IN}) of a bipolar transistor in the output section of a typical gate circuit switches from high to low and when the output (V_{OUT}) of the circuit also switches from high to low. During that delay the BE junction of the upstream bipolar transistor is reverse-biased [19]. This transient reverse-bias stress condition in BiCMOS gates cannot be removed by reducing the logic swing of the circuit [15] and the degradation caused by it helps to determine the lifetime of the BiCMOS circuit [19].

1.1.3 Reliability

Reliability is very important in telecommunications applications and it is important that SiGe maintain the level of reliability provided by Si technologies. Overall, SiGe provides better reliability and yield than III-V semiconductor technologies [2]. The effects of hot carriers is a reliability issue in Si and SiGe integrated circuit (IC) applications where such stressing can occur when the base-emitter junction is reverse biased, such as in BiCMOS and some ECL and TTL circuit designs. Reverse bias electrical stressing is used in time-to-failure (TTF) testing to determine failure rates and degradation mechanisms [2] and can be used to approximate radiation damage [20]. Conventionally time-to-failure (TTF) lifetimes are measured using high reverse-bias voltages in an open-collector (OC) configuration. Accelerated stressing techniques, such as forward-collector (FC) stressing which uses a high stress current caused by

forward-biasing the base-collector (BC) junction, are used to speed-up the reliability testing process by causing more damage in a shorter time [11].

1.1.4 Gamma Radiation

Gamma radiation is electromagnetic radiation produced by ionizing radiation sources such as cobalt-60 (^{60}Co). Ionizing radiation effects in semiconductor electronics are encountered in nuclear power, space, medical, and defense applications [2]. To avoid expensive experiments when evaluating the radiation immunity of bipolar technology hot carrier stressing can be used to approximate radiation effects [20] or, conversely, radiation effects could be used to approximate hot-carrier degradation.

Ionizing radiation causes damage in semiconductor circuits by generating electron-hole pairs in the insulator (SiO_2 in Si ICs), which results in excess charges being trapped in the semiconductor interface regions or in the interface region between the insulator and the semiconductor and damage to the interfaces. It is usually holes that are trapped in this manner. In CMOS transistors this radiation results in charge trapping in the field oxides. In bipolar transistors ionizing radiation results in a decrease in gain and an increase in leakage current [21].

1.2 Thesis Objectives

The main objective of this thesis is to examine the effects of open-collector (OC) and forward-collector (FC) reverse-bias stressing techniques on the dc device characteristics of SiGe self-aligned HBTs and the phase noise characteristics of SiGe voltage controlled oscillators (VCOs). The effects of two types of reverse-bias stressing techniques on SiGe HBTs are compared.

The examination of the hot-carrier damage due to reverse-bias stressing on the

SiGe HBTs including measurements of characteristics such as the forward Gummel (FG), current gain, base-emitter diode (BED), ideality factor, and comparisons between FC and OC stressing effects. Annealing is known to repair hot-carrier induced degradation in Si HBTs [22] and the effects of annealing on hot-carrier damaged SiGe HBTs is investigated here.

Gamma irradiation is known to increase the amount of low frequency noise ($1/f$) in a bipolar transistor. Low frequency noise can be upconverted into phase noise in a voltage controlled oscillator. Therefore, the phase noise degradation, and degradation of the transistor and circuit characteristics due to gamma irradiation is examined by exposing SiGe VCOs and HBTs to doses of gamma radiation and taking measurements after each dose. Both independent HBTs and HBTs isolated from the VCO by FIB were used. Single-sided phase noise measurements were used. Comparisons between gamma radiation effects and hot carrier stress effects on SiGe HBTs are made and the effect of HBT degradation on VCO circuit operation is examined.

1.3 Thesis Outline

This introductory chapter has outlined the background of reverse bias stressing in silicon and silicon-germanium technology, stated the objectives of the project and briefly mentioned the steps taken to accomplish them. Chapter 2 provides a description of the SiGe HBTs used and presents some nominal device measurements for them. Chapter 3 describes the two types of reverse-bias stressing and how the amount of stress current is calculated. Chapter 4 contains the forward collector and open collector reverse-bias stress measurements, the comparison between the two types of stress measurements, random telegraph signals recorded during stressing, and changes to HBT characteristics due to annealing. Chapter 5 examines the effect of gamma irradiation on SiGe HBTs while chapter 6 describes the VCO and the effects of gamma irradiation on oscillator phase noise. Conclusions and future work are presented in

chapter 7.

The devices used in the reverse-bias stressing experiments were designed and fabricated by SiGe Semiconductor Inc. The devices and circuits used in the gamma radiation experiments were designed by John Rogers and fabricated by SiGe Semiconductor Inc. The irradiation of the devices and circuits was done by John McCaffery at NRC's Institute for National Measurement Standards.

Chapter 2

Device Structure

2.1 SiGe HBT

The individual transistors described in chapters 2, 3, and 4 of this thesis were unpackaged SiGe HBTs fabricated in an adapted BiCMOS process and supplied by SiGe Semiconductor Inc. The epitaxial SiGe base was deposited by ultra-high vacuum (UHV) chemical vapour deposition (CVD) as a modified part of the process flow. The emitter was conventional polysilicon [23]. The voltage controlled oscillators (VCOs) and corresponding SiGe HBTs used in chapter 5 were also designed by John Rogers and fabricated by SiGe Semiconductor Inc. in a similar SiGe process.

The base-emitter junction in the devices is displaced from the polysilicon/silicon interface by the n^+ (As) emitter doping driven into the epitaxial Si, towards the highly doped (boron) base. The As in the emitter polysilicon diffuses more rapidly vertically than laterally into the Si [23]. The As emitter diffusion profile results in a large built-in electric field (0.5 to 1×10^6 V/cm) within a narrow region of the epitaxial Si layer around the emitter perimeter [12].

In our devices the boron-doped SiGe base layer had a ramped Ge concentration profile which increases linearly from the emitter to the collector. A thin, 30 to 60 nm, Si layer was grown on top of the SiGe layer [23], [12]. This type of Ge profile in

a SiGe HBT results in a substantial improvement in the Early voltage (V_A), cut-off frequency (f_T), and current gain (β) over a Si BJT [24].

The transistors each have two $0.8 \times 12 \mu m^2$ emitter strips and gains were typically 100. The unity gain cut-off frequency (f_T) was typically 30 GHz or larger [12]. A schematic cross-section of the SiGe HBT is shown in Figure 2.1 and a photo is shown in Figure 2.2 [23].

Figure 2.1: Schematic cross section of HBT used.

Two different configurations of the device were used in these experiments. The first configuration had the emitter and substrate shorted together (ES) as part of the fabrication design flow. The second configuration had the collector and substrate of the device shorted together (CS). Both device configurations were fabricated on the same wafer and were identical except for the substrate connection. The type of device, ES or CS, used in the experiments depended on the type of electrical stressing chosen, as will be explained later.

Figure 2.2: A photo of a SiGe HBT used in the stressing experiments.

2.2 Nominal HBT Measurements

The unstressed forward Gummel (FG) plots and forward gain characteristics of the typical SiGe HBTs used are shown in Figure 2.3. A Gummel plot is a current-voltage characteristic of a bipolar transistor in which the base and collector currents are plotted on a semi-log scale as a function of the base-emitter forward bias voltage [1].

Figure 2.3: Current gain and forward Gummel plots of an unstressed SiGe HBT.

The forward current gain (β) is ≈ 100 typically as determined from the FG characteristic shown in Figure 2.3. The individual gain values varied within the 80 to 120

range, as shown in Figure 2.4. The location of the device on the wafer affected the current gain with lower current gains found in the devices closest to the edge of the wafer. The non-ideal low-bias base current in the forward Gummel plot scales with emitter perimeter while the ideal region of both the base and collector currents scale with emitter area [12]. Reverse Gummel (RG) plots, as shown in Figure 2.5, were used to determine the reverse current gain. Typical reverse current gains of ≈ 10 or less are shown in Figure 2.5.

Figure 2.4: Variations in initial forward Gain characteristics for a series of different devices.

The ideality factor (n) is the measure of deviation of a p-n junction from the ideal diode equation, $I = I_0'(e^{\frac{qV}{nkT}} - 1)$. It reflects the generation and recombination effects which can cause a departure from the ideal diode characteristic ($n = 1$). The ideal region of a current in a Gummel plot occurs when the ideality factor of current is unity. If both the base and collector currents are ideal then this results in a constant current gain region [1]. The ideality factor usually varies between 1 and 2 although

Figure 2.5: Current gain and reverse Gummel plots of an unstressed SiGe HBT.

this is dependent on the semiconductor material, technology, and temperature [1]. The base ideality factor (n_B) is unity for bias voltages between approximately 0.45 and 0.80 volts, in our devices, and the current gain is constant in that region. For low forward bias voltages n_B is between approximately 2.5 and 3.0. This ideality factor cannot be accounted for using only Shockley-Read-Hall recombination effects, which typically produce $n_B \approx 2$. This non-ideal ideality factor is discussed further in Chapter 4.

The base-emitter diode (BED) characteristic was used to examine the BE junction when the device was not operating as a transistor. A typical unstressed base-emitter diode (BED) characteristic is shown in Figure 2.6. The forward biased region is

Figure 2.6: Base-emitter diode plot of an unstressed (0 seconds of stress) SiGe HBT.

similar to the base current in the forward Gummel plot. The reverse bias current is not ideal or just a leakage current, but has been interpreted as reflecting significant band-to-band tunneling (BBT) effects [25]. The band-to-band tunneling (BBT) rate is strongly dependent on the electric field which increases with the magnitude of the reverse base-emitter bias. The rate of BBT and the magnitude of the reverse base

current increase as the reverse base-emitter bias voltage increases [11], [12], [13], [14]. Band-to-band tunneling (BBT) dominates the reverse BED characteristic [12].

2.3 Simulations

The low forward bias region of the base-emitter diode (BED) exhibits a non-unity ideality factor as shown in Figure 2.6. Simulations using the SiGe HBT cross section profile shown in Figure 2.7 and the doping profile are shown in Figure 2.8. This structure was used to examine the effects of band-to-band tunneling (BBT), Shockley-Read-Hall recombination (SRH), and trap-assisted tunneling (TAT) on the BED characteristic. The Silvaco [16] Atlas simulation software was used for these simulations. The doping profile reflects corresponding data from a SIMS analysis of typical devices.

The devices have a high built-in electric field region due to the narrow BE junction. The simulations, as shown in Figure 2.9, shows this electric field region around the emitter perimeter as mentioned in previous sections.

Shockley-Read-Hall (SRH) recombination effects result in the generation current shown in Figure 2.10. Obviously SRH recombination is not the only effect being observed in these SiGe HBTs. The addition of trap-assisted tunneling (TAT) effects, as shown in Figure 2.11, approaches the effects observed but does not adequately explain them.

The reverse bias current contained significant band-to-band tunneling (BBT) effects [25]. This effect is simulated in Figure 2.12 for the reverse bias region of the BED characteristic. However the implementation of BBT effects in the Atlas simulator resulted in non-zero current at zero bias voltage, as shown in Figure 2.13 and Figure 2.14. This effect also occurred when using the Synopsis [17] MEDICI simulation software. Both the MEDICI and ATLAS simulation programs are derived from

Figure 2.7: Schematic of the HBT used in the Atlas simulations.

Figure 2.8: The SiGe HBT doping profile used in the Atlas simulations.

Figure 2.9: The electric field profile resulting from the SiGe HBT design used in the Atlas simulations.

Figure 2.10: Shockley-Read-Hall recombination effects on the Base Emitter Diode characteristic as a function of the electron and hole lifetime. Lifetime curves have steps of 10^{-10} , 10^{-9} , 10^{-8} , and 10^{-7} seconds.

the Stanford [18] PICSES simulation software. This feature is not a physical effect but arises from the approximations and equations used by the software to simulate the tunneling physics. Correction of this issue would require the implementation of a better tunneling model in the software.

Simulations can provide a useful description of the contributions to the base and stressing currents but since there were problems in the implementation of the tunneling processes it would be unwise to rely too heavily on them for quantitative conclusions.

Figure 2.11: Shockley-Read-Hall recombination and trap assisted tunneling effects on the Base Emitter Diode characteristic as a function of the effective mass. Effective mass curves have step sizes of 0.1, in units of the electron mass.

Figure 2.12: Band-to-Band Tunneling effects on the reverse bias region of the Base Emitter Diode characteristic. Effective mass curves have step sizes of 0.1, in units of the electron mass.

Figure 2.13: The simulation of the Base Emitter Diode characteristic which shows a non-zero current at zero bias due to band-to-band tunneling components in the simulation.

Figure 2.14: The simulation of the Base Emitter Diode characteristic which shows a non-zero current at zero bias due to the band-to-band tunneling contributions in the simulation. The effects of Shockley-Read-Hall recombination and trap-assisted tunneling are also shown. Effective mass curves have step sizes of 0.1, in units of the electron mass.

Chapter 3

Reverse Bias Electrical Stress

3.1 Types of Reverse Bias Electrical Stress

Two different reverse-bias stressing methods were used in these experiments. In the open-collector (OC) method of stressing the base-emitter (BE) junction was reverse-biased at a constant voltage, with the collector and substrate open and isolated from the probe chuck. The OC stressing is a constant voltage method. In the forward-collector (FC) method of stressing the BE junction is also reverse-biased at a constant voltage but the base-collector (BC) junction is forward-biased instead of leaving the collector open. In this method extra carriers (electrons) are injected into the base, and then emitter, from the collector. One aim of FC stressing is to increase the degradation rate especially at lower (negative) biases where it is low. The FC stressing can be a constant voltage or a constant current method. A constant current method was used in these experiments, to allow easy calculation of the stress charge. A circuit diagram of the two stressing methods is shown in Figure 3.1.

3.2 Carrier Movement During Stressing

The movement of the carriers during FC and OC stressing is shown schematically for the device geometry in Figure 3.2 while Figure 3.3 shows the carrier movement during both types of stressing for the energy bands of a generic Si BJT with no Ge

Figure 3.1: This circuit diagram shows configurations for OC and FC stressing a device.

profile in the base.

In OC stressing the reverse biasing of the BE junction increases the electric field in the BE junction, resulting in a reverse BE current which is dominated by band-to-band tunneling (BBT) effects, see Figure 2.6 [25]. Electrons tunnel across the narrow BE junction into the emitter leaving hot holes on the base side of the junction area, as shown in Figure 3.3. These holes are in a region of large electric field, Figure 2.9, and can impinge upon the Si/SiO_2 interface region creating damage and traps at the surface and in the oxide [26], as is shown in Figure 3.2.

In forward-collector (FC) stressing both hot electrons and hot holes cause damage. In this stressing method the device is biased in a manner similar to that used for a reverse Gummel plot. The electrons are injected from the forward-biased base-collector (BC) junction and are accelerated into the emitter by the field in the BE junction, as shown in Figure 3.3. This is in addition to the hot carriers from the reverse biased base-emitter junction. Since the hole contribution to the stress is determined by the BE bias alone, the BC junction can be biased so that the contribution from the electrons rather than the holes dominates the FC stress.

Figure 3.2: Carrier movement in Open Collector and Forward Collector stressing.

Figure 3.3: Carrier movement in the bandgap for Open Collector and Forward Collector stressing.

3.3 Methods Used

The transistors were all stressed and tested at 295 K (room temperature) using a HP4155 Semiconductor Parameter Analyzer and dc probes. The devices were mounted with glue on a thin alumina carrier that isolated the devices from the probe station chuck. The measurements were performed in the dark using a probe station within a shielded box. Annealing, as described in the section on recovery in Chapter 4, was done in a Thermolyne type 1400 Furnace that was heated to the desired temperature, and only opened to remove the devices for measurements. Reverse-biased stressing was performed as a function of time and interrupted at various times to make dc measurements. The probe positions on the device were not changed between the stressing and measurement steps. The devices were characterized using BE diode, forward Gummel (FG) with $V_{BC} = 0$ V, reverse Gummel (RG), and other measurements.

For OC stressing the damage to the devices increases as the stress time increases and as the magnitude of the reverse BE voltage increases. In FC stressing the damage increases as the stress time increases and the magnitude of the reverse BE voltage increases (as in the OC case), but also with increasing FC stress current. To compare stress methods the total stress charge (product of stress current and time) was used. At the same reverse BE stress voltage, the FC method should require less time to cause an equivalent amount of damage as the OC method, since a larger stress current is used. Since smaller BE stress voltages require a longer stress time to reach damage levels equal to those at higher BE stress voltages, the FC method enables the stressing to be accelerated, in time, compared with OC stressing. This is particularly important at low stress bias levels where the OC experiments might require long periods (greater than 10^5 seconds) of stressing before any significant changes can be observed.

The OC stress current was determined by the BE voltage during stressing. The FC method can be a constant current or a constant voltage method. In the constant voltage method of FC stressing the BE junction was reverse-biased, as in the OC

stressing, but the BC junction was forward biased at a constant voltage. For these experiments a constant current method was used for the FC stressing. To determine the required constant current the BE diode characteristic measurement was used to determine the OC emitter stress current, I_{OC} , at the required BE stress voltage. Then the desired total FC stressing current in the emitter, I_{FC} , was chosen. Usually this current was chosen to be 100 times the OC emitter stress current for the given BE stress voltage, $R = 100$. The current required from the forward biased BC junction, I_{CFC} , was determined from $I_{FC} = I_{CFC} + I_{OC}$. To examine any differences between the OC and FC stressing I_{CFC} needs to dominate the total stress current in the FC case, $I_{FC} = RI_{OC}$ with $R \gg 1$. The current into the collector contact, I_C , required to create the desired I_{CFC} , is determined from $I_{CFC} = \alpha_R I_C$, where α_R is the reverse common-base gain calculated from the reverse Gummel plot of the device. Thus the total constant current applied to the collector during constant current FC stressing was $I_C = I_{OC}(R - 1)/\alpha_R$. The average value for α_R was 0.89 ± 0.04 for the devices used. Figure 3.4 shows the emitter stress current as a function of BE voltage for OC stressing and at various base-collector voltages for FC stressing.

To determine the FC emitter stress current required at each BE voltage, the reverse Gummel and the BE diode characteristics of the device were initially measured. Since reverse Gummel and reverse BE diode measurements can cause inadvertent stress damage, due to reverse biasing of the base-emitter diode, care was taken to choose voltage levels that would not stress the devices during the initial or subsequent set-up measurements.

Figure 3.4: Emitter stress current as a function of BE voltage for OC stressing.

Chapter 4

HBT Reverse-Bias Stress Measurements

4.1 Tunneling Damage

During the normal operation of a BJT trap-assisted tunneling occurs when electrons from the conduction band in the emitter move, via quantum mechanical tunneling, into traps in the energy gap in the emitter-base space-charge region. Recombination occurs when a hole is captured at the trap to complete the process. This process may also occur with holes from the valence band moving into traps and capturing electrons [6].

Forward bias tunneling at low bias has been discussed earlier in Si devices in papers, such as [27] and [28], and known to be important in modern high performance Si-based BJTs. Since it depends strongly on the doping levels (and thus fields) at the BE junction it depends on the processing used during device fabrication. It is a sensitive measure of the quality of the BE junction.

The trap-assisted tunneling in the forward bias region is not the same as the BBT present in the reverse bias region. The unstressed base-emitter diode (BED) characteristic contained a significant reverse bias current dominated by band-to-band

tunneling effects [25]. These effects are phonon-mediated because of the indirect nature of the Si band gap. The BBT rate is strongly dependent on the electric field which, in the BE junction, increases with the magnitude of the reverse bias. Therefore, as the reverse BE bias increases, the rate of BBT and the magnitude of the reverse base current also increases [12], [11], [13], [14]. The electric field in the BE junction of the devices used in this experiment was large enough (0.5 to 1×10^6 V/cm) for BBT to dominate at all but the very small reverse BE biases [12].

During reverse bias stressing damage is caused by hot holes, created by band-to-band tunneling in the base-emitter junction, during OC stressing and by hot holes and electrons, injected from the collector into the base, in FC stressing. The reverse biasing of the BE junction increases the electric field in the junction, resulting in a reverse current dominated by band-to-band tunneling (BBT) [25]. Electrons tunnel across the narrow BE junction, where there is a large built-in field, leaving hot holes on the base side of the BE junction area. These hot holes can then penetrate the Si/SiO₂ interface region to create damage and traps at the surface and in the oxide [26].

4.2 Open-Collector Stress Damage

The BE junction was reverse-biased while the collector and substrate were left open during OC stressing. The BBT dominated emitter current is the OC stress current. When the device was stressed the BE current did not change at large reverse BE voltages and hence the stress current did not change significantly.

A significant increase in the base current is observed in the low forward bias region of the forward Gummel characteristic following reverse bias stress, as shown in Figure 4.1. This increase in base current results in a decrease in current gain as shown in Figure 4.2. As the base current increases, due to the stress damage, the ideality factor of the base current in the area in which the increase is noted ($V_{BE} < 0.6V$), changes

from ideal ($n_B=1$) to values > 2 ($n_B \approx 2.5$ to 3). The increase in the base current arises predominantly from damage caused by the stress, which creates traps in the Si/SiO_2 interface region. This gives rise to an increase in trap-assisted tunneling in the BE junction [26].

Figure 4.1: The degradation of the base current in forward Gummel plots at low BE biases as a result of OC stressing. Steps of 0, 1, 10, 100, and 1000 seconds are used.

At low reverse BE voltages there was a small increase in the reverse BE current with increasing stress time. This is shown in Figure 4.3 where the base-emitter diode measurements are shown for a device stressed for up to 1000 seconds of OC stressing at a BE stress voltage of -3.2 V. This increase in the stress current at low reverse bias may be due to an increase in trap-mediated tunneling rather than BBT.

Figure 4.2: Decrease in current gain as a result of OC stressing. Steps of 0, 1, 10, 100, and 1000 seconds are used.

Figure 4.3: Effects of OC stressing on the Base Emitter Diode (BED) characteristic. Steps of 0, 1, 10, 100, and 1000 seconds are used.

4.3 Forward-Collector Stress Damage

The hot carriers in the FC method of stressing (as well as in OC stressing) cause no change to the collector current in the forward Gummel plot in Figure 4.4 where the device was stressed at -2.7 V for between zero and 1000 seconds. V_{BC} in the Gummel measurements was always 0 volts. These results are typical for Si BJTs [26], and suggests that there is no degradation in the BC region. The base current increased as the devices were stressed for longer periods of time. Therefore the current gain of the devices, derived from Gummel plots, degraded with stressing, as shown in Figure 4.5. This figure shows the degradation in the current gain for a HBT FC stressed up to 1000 seconds at a BE stress voltage of -2.8 V and a constant stress current of 1.91 mA. The current gain degrades substantially due to stress at these voltages. Similar curves were found previously for OC stressing.

An increase in the base current was also observed in the reverse Gummel characteristic after FC stressing, as shown in Figure 4.6. This device was FC stressed for 1000 minutes at a base-emitter voltage of 1.8 volts and a stress current of 3.82 mA. This small increase in RG base current was not observed during OC stressing and may be a result of the additional current used damaging the BC junction.

4.4 Comparisons

The decrease in the current gain and charge-to-failure calculations were used to compare the effects of OC and FC stressing. The accumulated stress is the integrated stress charge calculated as the product of stress current and time. The failure point of a device was considered to be when a 10 percent degradation in gain was observed at a BE voltage of 0.75 volts. All the devices were measured and stressed at 295 K.

A decrease in the normalized gain due to FC and OC stressing as a function of stress charge is shown in Figure 4.7 for various BE voltages. In Figure 4.7 the gain

Figure 4.4: The degradation of the base current in forward Gummel plots at low BE biases as a result of FC stressing. Steps of 0, 1, 3, 10, 30, 100, 300, and 1000 seconds are used.

Figure 4.5: Decrease in current gain as a result of FC stressing. Steps of 0, 1, 3, 10, 30, 100, 300, and 1000 seconds are used.

Figure 4.6: An increase in the base current is observed in the reverse Gummel characteristic after 1000 minutes of FC stressing. Steps of 0, 1, 3, 10, 30, 100, 300, 1000, 3000, 10000, 30000, 40000, 50000, and 60000 seconds are used.

during FC and OC stressing at a BE stress voltage of -2.8 volts is compared. The FC emitter stress current chosen for the FC stressed device was 100 times that of the OC stressed device. The BE stress voltage of -2.8 V is the point where the FC and OC “charge to failure” curves cross in Figure 4.8. Figure 4.7 shows a slight difference between the rates at which the two stress methods decrease the gain of the device.

Figure 4.7: Decrease in normalized current gain due to FC and OC stressing as a function of stress charge.

The charge-to-failure is compared between FC and OC stressed devices for different reverse BE stress voltages in Figure 4.8. Each point in Figure 4.8 corresponds to a separate stressed device. The charge-to-failure (charge per area) was calculated using the emitter current. The emitter current gives the total number of carriers leaving the base and entering the emitter. The resulting curves for FC and OC stressing are different. The FC curve crosses the OC curve at approximately -2.8 volts. At voltages lower than this crossover point the FC stressing requires less charge to cause failure than OC stressing. This crossing of the two curves is not shown in the data

in [11] for SiGe devices, possibly due to experimental difficulties in performing the FC stressing at the higher biases where the charge-to-failure times can become very short and difficult to measure accurately.

Figure 4.8: Charge to failure comparison between OC and FC stressing. Shifted curves are explained in the text.

At the highest base-emitter voltage biases, the holes are so much more effective at causing damage that they begin to dominate the charge-to-failure in the FC measurements. The emitter current in the FC experiments is set to be a factor R times the current that would flow in the OC case. Thus, if electrons cause negligible damage compared to holes, the damage in the FC measurement is caused by the fraction $1/R$ of the current due to holes, and so the charge to failure in FC stressing should become R times the charge to failure at the same bias in the OC measurement. The curves labeled $\times 50$ and $\times 100$ in Figure 4.8 show the OC results shifted upward by a factor R , for comparison with the FC data. All but the three FC points at highest bias voltages in Figure 4.8 had $R = 100$ while those three points had $R = 50$. The last two FC points are so close to the shifted OC curve that the hole contribution

presumably dominates. To get information on the damage due to electrons at these high biases would require larger R , which would make the stress time unreasonably short.

The crossover is mainly due to two offsetting effects: kinetic energy of the carriers and current distribution in the device. At a given base-emitter bias, as discussed in [12] for SiGe HBTs and [26] for Si BJTs, electrons injected from the base into the emitter can gain a maximum kinetic energy of $e(V_{BE} + V_{bi})$, which is the full drop in energy in the conduction band from base to emitter. V_{bi} is the built-in voltage of the junction. However, holes created by tunneling can only gain a maximum kinetic energy of $e(V_{BE} + V_{bi}) - E_G \approx eV_{BE}$, since the band-gap energy E_G is used in creating the electron-hole pair. Thus at a given V_{BE} , holes in OC stressing have less energy available to cause damage than do electrons in FC stressing. Offsetting this effect is the current distribution: holes flow toward the base contact, and therefore are closer to the oxide interface than are electrons flowing from the collector to the emitter. The crossover suggests that the larger kinetic energy of the electrons dominates at low bias, but the closer proximity of holes to the oxide dominates at higher bias. References [12] and [26] suggest that the FC curve be shifted by V_{bi} (or E_G/e) for a comparison based on kinetic energy. When this is done, as shown in Figure 4.8, the curves no longer cross, indicating that at a given kinetic energy, holes cause more damage per unit charge than electrons do. These conclusions are consistent with the views expressed in [12] and [26], for SiGe and Si devices respectively.

4.5 Random Telegraph Signals

Random Telegraph Signals (RTS) are an intermittent form of burst noise found in submicron semiconductor devices such as MOSFETs, JFETs, and bipolar transistors. RTS are usually caused by the capture and emission of carriers from traps located in the Si, in the oxide, or at the interface between the Si and oxide [29], [30], [31]. They are usually found in the drain current of a MOSFET [32] rather than a bipolar

transistor. RTS behavior is normally associated with small Si MOSFETs.

During some Forward Gummel (FG) measurements the base current at low forward BE bias showed instabilities similar to RTS. This phenomena occurred after short amounts of high voltage and current stressing. These RTS-like results were observed after the device in Figure 4.9 had experienced a small amount of FC stressing at a -2.7 V bias voltage and 3.7×10^{-4} C (1.23 mA for 0.3 seconds). This effect was visible in the Gummel plots because the time scale of the sweep was similar to the time-scale of the random currents. We believe these instabilities in the base current are caused by the trapping and de-trapping of charge around the emitter corner which causes 'gating' of the current [12].

Figure 4.9: Example of random telegraph signals (RTS) in base current.

Further examination by McAlister confirmed the presence of RTS in the base current of the device in [12] and [23]. In the measurements made by McAlister on a SiGe HBT (Figure 4.10 : emitter area of $1 \times 3 \mu m^2$) the random signals were discovered in the base current after 2 to 5 seconds of OC stress at a BE stress voltage of -3.5 V. This device was examined at V_{BE} of 0.4 V after the OC stressing [12].

Figure 4.10: Example of random telegraph signals (RTS) as a function of time.

While an instance of RTS in a individual transistor may have little effect, averaging many RTS signals could lead to additional low frequency noise ($\propto 1/f$). Low frequency noise has effects on the phase noise of voltage controlled oscillators as is described in chapter 6.

4.6 Annealing

Thermal annealing can be used to repair interface traps caused by tunneling currents [33]. It is known that hot-carrier-induced damage in Si BJTs can be partially repaired using thermal annealing [34] so it can be expected that annealing will also result in recovery in reverse-bias electrically stressed SiGe HBTs.

In Figure 4.11 it is shown that both FC and OC damage, caused by 1000 seconds of stress, using either stressing method, recover when annealed at 150 C. As described in the previous sections FC stress causes more damage than OC stress for the same

stress time. The OC stressed device was stressed at a BE stress voltage of -2.7 volts. The FC stressed device was stressed at a BE stress voltage of -2.7 volts and a constant stress current of 1.72 mA ($R = 100$). The gain for the devices was determined for a BE voltage of 0.75 volts. The normalized current gain of the unstressed device remained essentially constant throughout the annealing phase while the OC stressed device recovered from a minimum normalized current gain of ≈ 0.97 to a maximum recovered gain of ≈ 0.99 , and the FC stressed device recovered from a minimum normalized current gain of ≈ 0.79 to a maximum recovered gain of ≈ 0.93 . The devices were annealed for a total of approximately 120 hours.

Figure 4.11: Example of samples annealed after 1000 seconds of stressing.

Two devices were then stressed to the same normalized current gain ($\beta/\beta_0 \approx 0.89$), as shown in Figure 4.12. The equivalent level of stressing was achieved using both FC and OC stressing methods. Annealing at 150 C resulted in the OC stressed device recovering to a normalized gain of approximately 0.976 in 74 hours of annealing. The

FC stressed device recovered to approximately 0.968 in 74 hours of annealing. The OC stress damage recovered faster than the FC stress damage.

Figure 4.12: Devices were annealed at 150 C after equivalent FC and OC stress charge. [12]

These results show that some of the current gain degradation caused by hot carriers during reverse-bias stressing can be reversed through low temperature (150 C) annealing of the damaged devices. The results also show that OC stress damage devices recover more quickly and fully than FC stress damaged devices. This suggests that annealing is more effective at repairing damage caused by holes than electrons.

4.7 Ideality Factor

The ideality factor (n) is the measure of deviation of a p-n junction from the ideal diode equation, $I = I_0'(e^{\frac{qV}{n k T}} - 1)$. The ideality factor usually varies between 1 and 2

although it is dependant on the diode material and temperature [1]. The HBTs used in this thesis typically exhibited ideality factors between 2.5 and 3 at low forward bias BE voltages. These low bias ideality values did not change significantly as the devices were stressed. Figure 4.13 shows the base and collector ideality factors for a device that was OC stressed at -2.8 V for up to 30,000 seconds. The ideality factors for the low BE voltage case were calculated between 0.2 and 0.4 volts. The ideality factors for the high BE voltage case were calculated between 0.7 and 0.8 volts. Initial ideality values for the device shown in Figure 4.13 were 0.99 for the base current at high BE voltages, 2.85 for the base current at low BE voltages, and 1.0 for the collector current at low BE voltages. The ideality factor of the collector remained at a constant value close to unity regardless of the applied stress. There is some slight increase in n_B at high BE voltages at long times as the non-ideal component increases.

Figure 4.13: HBT ideality factors after stressing.

As shown in the FC forward Gummel characteristic, Figure 4.4, the ideality factor changed from unity to the non-ideal value as the low bias base current increased due

to stress. The ideality factors > 2 cannot be explained using only Shockley-Read-Hall recombination effects, as mentioned in chapter 2, and is best understood by considering tunneling effects.

Chapter 5

HBT Radiation Damage Measurements

5.1 Rationale

Initially the effects of hot-carrier stressing on the circuit operation of a SiGe voltage controlled oscillator (VCO) was to be examined by isolating a single HBT using microsurgery, applying reverse-bias stressing to the device, reconnecting the device to the rest of the circuit, and comparing circuit operation before and after stressing. Reverse-bias stressing increases the low frequency noise ($1/f$) in a transistor [20]. SiGe VCOs operate at high frequencies but are sensitive to low frequency noise, which affects the phase causing phase noise [35]. Hence it is worthwhile to examine the effects of reverse-bias electrical stressing on the phase noise of a voltage controlled oscillator.

Some problems were encountered during the attempt to implement this plan. There was only a small number (seven) of VCOs available for experimentation. Initial measurements indicated that one device was of questionable quality. This was initially attributed to environmental interference but further investigation of the isolated HBT in this circuit determined that it was likely a processing issue. A small number of devices (four) were sent to be cut using a Focused Ion Beam (FIB) tool.

FIB uses a focused beam of accelerated gallium ions to sputter materials, deposit metals, or etch materials. Of these circuits two, including the previously mentioned device, were severely damaged due to faulty conductive paint during attempts to repair the microsurgery modifications. Reconnecting the devices isolated by the FIB process proved to be more difficult than planned. Further attempts to repair the cuts by evaporating aluminum (Al) into the cut were inadequate. The depth of the cut and the angle of the cut sidewalls meant that the thickness of the Al that could be evaporated was inadequate to provide good low resistance contact between the two sides of the metal layer, as shown in Figure 5.1. Due to these difficulties the experiment could not be completed as expected.

Figure 5.1: SEM image of two layers of aluminum evaporated onto a FIB cut isolating the collector of a VCO HBT.

When it became apparent that the electrical stressing experiment was not going to work it was decided that the effect of gamma radiation on VCO phase noise would be examined. The shift in focus from electrical stressing to irradiation was appropriate because hot carrier stressing can be used to approximate radiation effects and avoid expensive radiation experiments when evaluating the radiation immunity of bipolar

technology [20].

Irradiation will result in the entire circuit being exposed to gamma radiation, not just the transistors. This creates an isolation problem that could affect comparisons between gamma radiation effects and the effects of reverse-bias stressing.

5.2 Devices and Measurement Setups

The bipolar transistors used in this chapter were SiGe HBTs created in a similar process technology as those devices used in earlier chapters. Some of the HBTs were test structures located on the same chip as the voltage controlled oscillator (VCO) discussed in Chapter 6. These HBTs were isolated from the other circuits and test structures on the chip and each terminal was connected to its own pad. The remaining devices examined were SiGe HBTs from the VCO circuits themselves where a FIB had been used to cut the base and collector metal layers to isolate the devices from the rest of the circuit. A FIB at MuAnalysis Inc. was used to open $5\mu m \times 5\mu m$ probe windows, so that the dc probes could make contact with the base and collector metal layers. The emitter was connected to the ground pads of the circuit. A resistor, approximately 230Ω , was located between the emitter of the device and the pad. All devices were unpackaged.

The chips were exposed to gamma radiation in doses of approximately 1.9 kGy, which corresponds to approximately 15 hours of exposure time per dose. Neither the HBTs nor the VCOs were biased during irradiation. Each chip was irradiated for up to a total of four doses of gamma radiation. During irradiation the devices were mounted on the front of a 14.5 cm thick Lucite phantom with double-backed tape with an additional 4.75 mm thick piece of Lucite mounted on the front of the devices to provide full build-up (electron equilibrium). The devices were positioned at a distance of 42.2 cm from the ^{60}Co gamma (γ) radiation source. The top of the chips faced the radiation source. The dose rate to silicon was approximately 2.1 Grays/min. The

exposure area, $16\text{ cm} \times 16\text{ cm}$, was too large to limit exposure to individual transistors however multiple chips could be irradiated in a single run and it provided a flat field over the area. The unmodified circuits were used to determine the effects of radiation on the phase noise of the VCO while the isolated HBTs and the test HBTs on the chips were used to determine the effect of radiation on individual HBTs. After each dose the dc characteristics were measured, similar to the procedure for the electrical stressing experiments. John McCaffery at NRC's Institute for National Measurement Standards performed the irradiation.

5.3 Irradiation Effects

Gamma radiation resulted in degradation of the current gain of the devices as well as changes to the forward Gummel, reverse Gummel, and BE diode characteristics. These changes were similar, but not identical, to the changes caused by reverse bias electrical stressing as described in previous chapters.

As with the reverse-bias stressed devices, the irradiated SiGe HBTs exhibited an increase in the base current of the forward Gummel characteristic at low BE bias voltages with increased exposure to gamma radiation. Unlike the reverse-bias stressed devices, the irradiated devices also exhibited an increase in the collector current at very low BE bias voltages after radiation. The results of irradiation on the Gummel characteristic of two test HBTs are shown in Figure 5.2 and Figure 5.3, and for a HBT isolated from the VCO in Figure 5.4. Variations in both base and collector currents at high BE bias voltages were observed and can be attributed to variations in contact resistance due to repositioning of dc probes for each measurement. This effect was not observed in the reverse-biased stressed devices because the position of the dc probes remained unchange throughout stressing and measurements.

The forward current gain degraded with exposure to gamma radiation. Some devices, such as test HBT 6 in Figure 5.6, exhibited a slight increase in current gain

Figure 5.2: Forward Gummel plots for an irradiated test HBT (HBT3). The curves indicate 1.9 kGy steps.

Figure 5.3: Forward Gummel plots for an irradiated test HBT (HBT6). The curves indicate 1.9 kGy steps.

Figure 5.4: Forward Gummel plots for an irradiated HBT isolated from a VCO (VCO2). The curves indicate 1.9 kGy steps.

for the highest cumulative radiation amount. This may be due to differences in the degradation rates in the collector and base currents of the devices or this could be a problem with the probe contacts. As shown in Figure 5.5 and Figure 5.7 not all devices exhibited this slight increase in gain at high radiation amounts.

Figure 5.5: Current gain degradation in an irradiated test HBT (HBT3). The curves indicate 1.9 kGy steps.

In OC stressing the RG characteristics of the devices did not change. However after irradiation changes were noted in the RG characteristic. The effects of radiation on the RG characteristic of SiGe HBTs was explored by Sheng in [36] where it was observed that exposure to gamma radiation caused an increase in the base current and as a result a decrease in the reverse current gain. This suggests that irradiation causes changes to the BC junction [36].

Unlike the BE diode characteristics for the reverse-bias electrically stressed de-

Figure 5.6: Current gain degradation in an irradiated test HBT (HBT6). The curves indicate 1.9 kGy steps.

Figure 5.7: Current gain degradation in irradiated HBT isolated from a VCO (VCO2). The curves indicate 1.9 kGy steps.

vices gamma radiation causes no change in the current in the reverse bias region. The current increased at low forward bias voltages similar to the increase seen in the electrical stressing case. The ideality factor and current magnitude were altered by the radiation over most of the voltage range. This effect was not observed in reverse bias stressed devices. As for the forward Gummel characteristics, variations in the current at high BE bias voltages were observed. This can be attributed to variations in the probe contact resistance due to repositioning of dc probes for each measurement. Plots of the BE diode characteristics of an irradiated test HBT and an irradiated isolated VCO HBT are shown in Figure 5.8 and Figure 5.9 respectively.

Figure 5.8: Base emitter diode plots of an irradiated test HBT (HBT6). The curves indicate 1.9 kGy steps.

Irradiated SiGe HBTs exhibit similar current gain and base current (forward Gummel) degradation as was observed in the devices electrically stressed via hot-carrier stressing, although differences were observed in the low-bias collector current (forward

Figure 5.9: Base emitter diode plots of an irradiated HBT isolated from a VCO (VCO2).

Gummel), the reverse Gummel, and BE diode characteristics. These results suggest that the damage caused by the gamma radiation occurs not only in the BE junction but also in the BC junction.

Chapter 6

VCO Measurements

6.1 VCO Introduction

Phase noise is noise that causes changes in an oscillator signal's phase. This jitter can be observed in the skirts around the oscillation frequency in the frequency response, which reduces the spectral purity of the signal [37]. The phase noise of a VCO can be caused by the Q of the resonator, the Q of the varactor, active devices in the circuit, power supply noise, and tuning voltage supply noise. The measurement setup was designed to reduce supply and environmental noise as much as possible. Single sideband (SSB) phase noise is measured in dBc/Hz (dB offset from the carrier frequency for a 1 Hz bandwidth) for a specific offset frequency [38]. The waveform formula for a real VCO is $V_{OSC} = A\cos(\omega_0 t + \phi_n(t))$ where ϕ_n is the phase noise. Based on Leeson's formula for oscillator noise, $|N_{OUT}(s)/N_{IN}(s)|^2 = \omega_0^2/4Q^2(\Delta\omega)^2$ Rogers rewrote the phase noise equation for this VCO to be $PN = (\omega_0/(2Q\Delta\omega))^2(FkT/2P_S)$ where P_S was the power in the oscillator tone, k is Boltzmann's constant, ω_0 is the frequency of oscillation, $\Delta\omega$ is the frequency offset from the carrier, F is excess noise injected by noise sources other than the losses in the tank, and T is the temperature of the circuit [39].

6.2 VCO Design and Fabrication

The integrated SiGe VCO used for this experiment was designed by John Rogers [39] and is shown in Figure 6.1. A schematic of the VCO circuit is shown in Figure

Figure 6.1: Image of SiGe 5 GHz VCO with transformer-coupled feedback designed by John Rogers.

6.2. The circuit is a cross-coupled $-G_m$ design. It was fabricated using a 75 GHz SiGe bipolar process and was not packaged during testing. The VCO was designed to operate between 5.0 GHz and 5.6 GHz with a tuning ratio of approximately 12 percent. A 1.8 volt supply voltage was used [39]. Tuning voltages used during testing were in the 0.25 volt and 1.7 volt range. Experimental examination of the frequency range indicated that the circuits used in these experiments had a frequency range of 5.10 GHz to 5.55 GHz over the tuning range as shown in Figure 6.3. Transformer-

Figure 6.2: Schematic of SiGe 5 GHz VCO with transformer-coupled feedback designed by John Rogers [39].

coupled feedback (with a 2:1 circular transformer) was used to increase the voltage swing, diode clamps were used to prevent amplitude fluctuations, and resistive emitter degeneration was used to decrease noise. Roger's initial phase noise experimental measurements resulted in a phase noise of -115.8 dBc/Hz at a 1 MHz offset. The circuit had buffers on the RF outputs [39].

6.3 Measurement Setup

Initial measurements at Carleton University encountered problems, so a measurement setup was created at the NRC. Lack of a Faraday cage to work in proved to be a large stumbling block. Quite a few problems were encountered due to external interference from environmental sources. To reduce the effect of environmental interference the measurements were performed at night between 11 p.m. and 4 a.m. when the interference was found to be at its lowest. The chuck and optical table, where the chips were mounted, were grounded to the water main, as was the chassis of the spectrum analyzer. The dc supply was isolated from the 60 Hz ac power line to reduce noise

Figure 6.3: The measured oscillation frequency of a SiGe VCO (VCO1) as a function of tuning voltage before gamma irradiation.

signals being introduced through the supply. To prevent vibrations in the probe cards the cables to the probes were physically clamped and checked regularly to ensure that they remained stationary. Experiments were performed in the dark since a shift in the peak oscillation frequency occurred when the fluorescent lights were on.

The VCOs were initially measured at 295 K (room temperature) using a HP71209a spectrum analyzer. The DC inputs to the VCO were supplied by a HP 6253A dual DC power supply to provide the supply, tuning, and tank voltages. For the V_{CC} and V_{tune} input voltages Moodle bias tees were used to eliminate undesirable high frequency noise from the DC signal. The V_{tank} input used a Mini Circuit low pass filter (BLP-10.7) for the same purpose. The input to the spectrum analyzer was protected using a Pico-pulse DC Block on the RF output of the VCO. The supply and tank voltages were set to a constant 1.8 volts. The tuning voltage was varied using incremental steps between 0.25 and 1.7 volts. Measurements were made with a frequency span of 5.0 MHz, a band-width of 30.0 kHz, and video averaging of 25. Measurements were

remotely controlled via computer using the program in Appendix A.1 to make trace and delta measurements. Phase noise was calculated from the spectrum analyzer delta measurement using $PN \text{ in dB} = 10\log(P_{peak}/P_{ssb}) + 10\log(BW) = \Delta + 10\log(BW)$ [38]. For this experiment a single ended measurement was used.

6.4 Irradiation Effects

The circuits were irradiated overnight then measured the following night. There was a minimum of two nights between radiation doses and it was possible for up to five nights to elapse between exposures. The devices were transported between irradiation and measurement locations on the double-sided tape that was used to mount the chips at both locations. The elapsed time between irradiation and measurements, and between separate radiation exposures may have allowed some recovery.

The phase noise of the circuit increases from its initial value for all tuning voltages until 3.86 kGy of radiation is accumulated then the phase noise decreases again for 5.78 kGy of accumulated radiation. The final measurement, 7.70 kGy, results are inconsistent over the tuning voltage range. The single ended phase noise at 1 MHz offset as a function of cumulative radiation for various tuning voltages is shown in Figure 6.4.

The single ended phase noise at 1 MHz offset as a function of tuning voltages for various cumulative radiation levels is shown in Figure 6.5. Irradiation causes an increase in phase noise as shown in Figure 6.5 however this increase is not linear with radiation dose. The single ended phase noise results for the 7.70 kGy case and the high voltage 1.93 kGy case are inconsistent with the other cumulative radiation plots. It is not known why they are different.

For the most part the phase noise appeared to be fairly consistent across the tuning voltage range for each radiation plot although some change in phase noise with

Figure 6.4: Single ended phase noise at a 1 MHz offset verses cumulative radiation dose per tuning voltage for a SiGe VCO.

Figure 6.5: Single ended phase noise at a 1 MHz offset as a function of tuning voltage at each radiation step for a SiGe VCO.

tuning voltage was observed. Phase noise was consistently higher at 1 volt tuning voltage. As shown in Figure 6.4 the phase noise increased then decreased as radiation accumulated.

Figure 6.6: VCO signal at 0.75 volt tuning voltage for each radiation step.

As shown in Figure 6.6 and Figure 6.7 the frequency of oscillation (peak frequency) increases with the first dose of gamma radiation then decreases with each additional dose of gamma radiation. The irradiated devices all had frequencies of oscillation higher than the oscillation frequency of the initial non-irradiated device. However the magnitude of the frequency shift was not large and may not be significant.

6.5 Observations and Conclusions

It is not known why a linear degradation in the phase noise of the VCO is not observed. Instead the phase noise of the circuit degrades with initial gamma irradiation then improves (not universally) with additional radiation exposure. This could be caused by the effects of different parts of the circuit degrading or recovering at different rates.

Figure 6.7: VCO signal at 1.25 volt tuning voltage for each radiation step.

Most of the effects of the irradiation are likely to be seen in the transistors and where the increase in low frequency noise in the transistors causes voltage variations on the terminals of the varactor bank. The passive elements (resistors, capacitors, and inductor) of the VCO are unlikely to be significantly damaged by the gamma radiation [2].

Varactors, voltage controlled capacitors, were used instead of fixed capacitors for tuning in this VCO design. The varactors in this design were sets of SiGe HBTs with the collector connected to the base of each transistor which were in turn connected to the collectors of the other varactor transistors and the emitters of the varactor transistors connected together. Noise applied at the terminals of the varactors becomes frequency modulated around the carrier frequency [39].

As shown by the previous measurements on the irradiated SiGe HBTs used in the design of the VCO, the current gain degrades with exposure to gamma radiation. While it was shown in Chapter 5 that exposure to gamma radiation degrades the

gain of SiGe HBTs the extent of the effect on the circuit performance would depend on the biasing conditions of the transistor. In both electrical stressing and radiation experiments the lower BE bias regions experienced more degradation than the higher bias regions. Hence, transistors operating in the low BE bias region would exhibit a greater change in gain characteristics. Other researchers have found that irradiation increases the low frequency ($1/f$) noise of SiGe HBTs [2]. This increase in low frequency noise could affect the phase noise of the VCO especially if it was observed on the terminals of the varactor bank or in the transistors Q1 and Q2.

Some phase noise variations between measurements may have been due to fluctuations on the dc supply and environmental interference that varied between measurement nights. Variations in probe contacts between sessions may have also contributed to differences in measured values. Efforts were made to minimize these effects. As was suggested by [21] and shown by [36] gamma irradiation can experience partial recovery due to annealing. It is unknown whether any of the devices in this VCO experienced recovery due to room temperature annealing.

Chapter 7

Conclusions and Future Work

7.1 Summary and Conclusions

We have shown that both reverse-bias stress and gamma radiation causes current gain degradation in the SiGe HBTs. Reverse-bias stressing causes an increase in the base current while gamma irradiation causes an increase in both the base current and the low bias collector current of the devices. While hot-carrier stressing appears to cause damage in the BE junction gamma radiation appears to cause damage in both the BE and BC junctions.

In FC stressing the electrons may possibly damage the polysilicon-silicon interface as well as the polysilicon-oxide emitter perimeter which is damaged during OC stressing. This makes the situation with FC stressing even more complex. The effects of reverse-bias stress on SiGe HBTs are similar to reverse-bias stress induced changes observed by other researchers in Si bipolar devices. The addition of SiGe to Si bipolar devices does not significantly change the observed response of the devices to stress, which is not unexpected since the underlying designs are similar.

As demonstrated by the comparison of FC and OC charge to failure as a function of reverse base-emitter stress voltage the effects of FC and OC stressing are different. The crossover point observed in the comparison of FC and OC charge to failure

appears to be related to the distribution of current across the emitter, the predominance of hot holes or hot electrons as the primary damaging carrier, and the size of the electric field in the BE junction. The effects of hot carrier stressing are not very different from those observed in FETs which have similar Si, polysilicon and SiO_2 structures [41].

Also, exposure to short periods of large reverse-bias stressing was shown to result in random telegraph signals (RTS) in the base current occasionally being observed. Annealing was found to repair some of the current gain degradation caused by electrical stress damage while current gain degradation caused by OC stress damage recovered after annealing to a greater extent than that caused by FC stress damage. As the base current of the forward Gummel characteristic increased the low-bias region where the ideality factor was greater than unity also increased. This effect was also seen in the irradiated devices.

While similar in their effect on the base current, reverse-bias stressing and gamma irradiation differ in their effects on the collector current of the devices as seen in the low bias region of the forward Gummel plots. The increase in low bias collector current and the changes observed in the reverse Gummel plots were probably caused by damage to the BC junction region. Unlike reverse-bias electrical stressing gamma radiation affects the whole chip and is not constrained to a specific region.

Gamma radiation affects the phase noise of the SiGe VCOs in a complex manner. Radiation generally increased the phase noise of the system while degrading the current gain of the SiGe HBTs in the circuit. The phase noise increased with irradiation then decreased with further irradiation over all tuning voltages. Some anomalies were observed at the highest cumulative radiation dose. Irradiation also resulted in some small increases in oscillation frequency however these are small.

7.2 Future Work

Further examination of the effects of reverse-bias stressing circuits containing SiGe HBTs can be pursued either through stressing individual transistors isolated via microsurgery, or through designing a circuit that will allow for isolation of the transistors without microsurgery. Redesigning the circuit so that FIB isolation is unnecessary should eliminate many of the problems experienced during these experiments. The effects of stressing on the circuit performance could then be measured.

One potential problem with our experiment is that radiation was done on an area and not limited to a single transistor. To compare the effects of electrical stressing and gamma radiation on VCO phase noise characteristics the individual transistors being examined would have to be isolated from the rest of the circuit so that those transistors are irradiated separately. This could be done either through designing an appropriate circuit layout, masking the parts of the circuit that are not to be irradiated, or by using discrete devices that can be irradiated separated from the circuit. Screening gamma rays is almost impossible at this scale therefore the use of discrete devices in the design would allow for the easiest method of comparison. If the same circuit is then exposed to gamma radiation then the damage caused by reverse-bias stressing can be compared to that caused by irradiation.

Semiconductor circuits are exposed to damaging protons and electrons as well as gamma radiation in space applications. Shielding can protect circuits from most radiation except for high energy protons which produce displacement damage [21]. Therefore the effects of proton radiation could be investigated and compared to the effects of gamma radiation and hot-carrier stressing on VCO operation.

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Appendix A: Programs

A.1 VCO Trace and Delta Measurements

```
; ~~~~~  
; Author: Coralie Gill  
; Date: 14 May 2003  
; References:  
;  
; Purpose: Phase noise measurements of a VCO. Save to file.  
;  
; Notes: Equipment must be initialized manually and marker peaked.  
;  
; ~~~~~  
AddExtender("WWGPIBNI.DLL")           ; Include GPIB Extender Functions  
home=FilePath(IntControl(1004,0,0,0,0)) ; Get Path to this File.  
GoSub DefineUDFs                       ; Define UDFs at the end  
  
; ~~~~~  
; Include UDFs/UDS libraries for GPIB related tasks.  
; ~~~~~  
#Include "udf_gpib.wbt"  
  
; ~~~~~  
; Define variables for Instrument Control
```

```

;~~~~~
hp71209a=18 ;; GPIB Address initially then instrument handle

;~~~~~
; Prompt the user for the name of a data file to store the results.
; Create the output file and add the header information
;~~~~~
file_types="Text Files|*.txt|Data Files|*.dat;*.mnu|All Files|*.*|"
fn1=AskLine("Data File Name", "Enter a data FileName", StrCat(home, "A.txt"))

fh1=FileOpen(fn1, "WRITE") ; Open data file for writting
FileWrite(fh1, "Hp71209A Spectrum Analyzer Measurements - CRG")

FileWrite(fh1, TimeYmdHms() ) ; Add a time & date stamp
FileWrite(fh1, @CRLF) ; Add a blank line

;~~~~~
; Set-up the instrument.
;~~~~~
;; Initialize the instruments
hp71209a=udf_gpib_InstInit("hp71209a", hp71209a, T1s, "hp71209a")

;~~~~~
; Find parameters and save data to a file
;~~~~~

;; Start and Stop Frequencies
ibwrt(hp71209a, "FA?", 0) ;; Find start frequency
ibWait(hp71209a, TIMO) ;; Wait for instrument to time-out
start_freq = ibrd(hp71209a, 25) ;; Get start frequency

```

```
ibwrt(hp71209a, "FB?", 0) ;; Find stop frequency
ibWait(hp71209a, TIMO) ;; Wait for instrument to time-out
stop_freq = ibrd(hp71209a, 25) ;; Get stop frequency

FileWrite(fh1, StrCat("Amplitude vs. frequency (From ", start_freq,
" to ", stop_freq, " Hz)" ))

;; Frequency Span
ibwrt(hp71209a, "SP?", 0) ;; Find span
ibWait(hp71209a, TIMO) ;; Wait for instrument to time-out
sp_bw = ibrd(hp71209a, 25)
FileWrite(fh1, StrCat("Span(Hz) ", sp_bw))

;; Resolution Band-Width
ibwrt(hp71209a, "RB?", 0) ;; Find resolution band-width
ibWait(hp71209a, TIMO) ;; Wait for instrument to time-out
rb_bw = ibrd(hp71209a, 25)
FileWrite(fh1, StrCat("Resolution Band-width(Hz) ", rb_bw))

;; Scan Time
ibwrt(hp71209a, "ST?", 0) ;; Find scan time
ibWait(hp71209a, TIMO) ;; Wait for instrument time-out
st_s = ibrd(hp71209a, 25)
FileWrite(fh1, StrCat("Scan Time(sec) ", st_s))

;; Marker at max peak
ibwrt(hp71209a, "MKOFF", 0) ;; Turn off markers
ibwrt(hp71209a, "MKPK HI", 0) ;; Put marker on peak
ibwrt(hp71209a, "MKA?", 0) ;; Find resolution band-width
```

```

ibWait(hp71209a, TIMO) ;; Wait for instrument to time-out
mka_db = ibrd(hp71209a, 25)
ibwrt(hp71209a, "MKF?", 0) ;; Find resolution band-width
ibWait(hp71209a, TIMO) ;; Wait for instrument to time-out
mkf_hz = ibrd(hp71209a, 25)
FileWrite(fh1, StrCat("Peak Freq(Hz) ", mkf_hz, @TAB,
    "Peak Amp(dB) ", mka_db))
FileWrite(fh1, @CRLF) ;; Add a blank line

```

```

; ~~~~~
; Measure and save data to a file
; ~~~~~

```

```

;; Choose type of measurement (Delta or Trace)

```

```

response = AskYesNo("Choose Measurement Type","Delta(Yes)
or Trace(No)")

```

```

If response == @YES

```

```

;; Delta measurement section

```

```

FileWrite(fh1, StrCat("Amp(dB)", @TAB, "Freq(Hz)", @TAB,
    "Phase Noise(dB/Hz)") )

```

```

frequency = 0 ;; initialize delta frequency

```

```

delta_steps = 150 ;; Number of delta measurements

```

```

step_size = 10 ;; Size of delta step in KHZ

```

```

For ii=1 TO delta_steps

```

```
ibwrt(hp71209a, StrCat("MKD ", frequency, "KHZ"), 0) ;; Set delta freq
ibwrt(hp71209a, "MKA?", 0) ;; Find delta amplitude
ibWait(hp71209a, TIMO) ;; Wait for instrument to time-out
delta_amp = ibrd(hp71209a, 25) ;; Read delta amplitude
FileWrite(fh1, StrCat(delta_amp, @TAB, frequency) )
frequency = frequency + step_size ;; increment frequency

Next ii

Else

;; Trace measurement section

FileWrite(fh1, StrCat("Amp(dB)", @TAB, "Freq(GHz)") )

;; Set timeout length
T300s = 16 ;; Timeout code
ibtmo(hp71209a, T300s) ;; Set timeout

;; Collect Trace
ibwrt(hp71209a, "TS", 0) ;; Single sweep
ibwrt(hp71209a, "TRA?", 0) ;; Call Trace
ibWait(hp71209a, TIMO) ;; Wait for instrument to time-out
tra_temp = ibrd(hp71209a, 8000) ;; Get Trace

;; Save Data to file
For jj = 1 TO 8000
    tra_store = ItemExtract(jj, tra_temp, ",") ;; Get item
    FileWrite(fh1, tra_store ) ;; write to file
```

```
Next jj ;; itterate
```

```
Endif
```

```
;; Clean up
```

```
FileClose(fh1) ;; Close File
```

```
;; Display the text in a dialog box
```

```
A=AskFiletext("Hp4285a Measurment", fn1, @UNSORTED, @EXTENDED)
```

```
Exit
```

```
;~~~~~
```

```
:DefineUDFs
```

```
Return
```

```
;~~~~~
```