NOVEL MEMBRANE-BACKED DEFECTED GROUND PLANE TRANSMISSION LINE PHASE SHIFTER

By

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ABSTRACT

A reconfigurable defected ground plane utilizing a micromachined, corrugated membrane is proposed and investigated as a phase shifter for phased array applications. The concept is based on etching slotted defects in the ground plane of the existing transmission line feed network of the antenna. Operation is regulated via control of the membrane electrode voltage, and thus a digital, analog and/or hybrid phase shifter is possible.

A parametric study is performed with a transmission line whose ground plane is defected by a single slot. For minimum return loss of 10 dB, up to 18° of phase shift is attainable, independent of substrate properties, with long, narrow rectangular slots promoting greater phase. Paired defects provide increased phase, and minimize return loss when defect separation promotes an impedance match. Phase shift figure of merit (FOM) of 500°/dB is possible with paired elements associated with 25Ω lines. Adopting a dumbbell shape for the defect pushes the paired defect FOM close to 600°/dB. An equivalent circuit model for the defect is presented, and is in agreement with its full wave analysis.

Fabricated prototypes of defected loaded line phase shifters, based on criteria of minimum size, yield measured FOMs of 334°/dB and 455°/dB, providing the required phase with a return loss of less than 10 dB as desired, in agreement with simulation. These structures are applied within a 3-element patch array, with beam scan in the far field computed for different element separations and phase shift progressions. Phase shifter designs based on minimum return loss by cascaded matched element pairs, require inter-pair spacing larger than 3 mm, at 10 GHz.

A cavity constructed beneath a ground plane defect is shown to influence phase shift, from 0° with zero cavity depth, up to the full defect phase, when the depth is twice the defect width. An electrostatically controlled membrane is selected to produce the cavity effect. Measured FOMs of 133°/dB and 143°/dB for defected transmission lines with and without a membrane backing, respectively, indicate that loss attributed to the membrane is negligible. Techniques for reducing the membrane electrode voltage are also studied and established.

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NOMENCLATURE

a_n	Array element amplitude
A	Absolute plate area of a parallel plate capacitor
A_p	Dimensionless stiffness coefficient
AF	Array factor
B	Shunt susceptance
B_p	Dimensionless coefficent of non-linear tension
C	Capacitance
C_{air}	Parallel-plate capacitance with air dielectric
C_{cavity}	Parallel-plate capacitance of the membrane-electrode cavity
C_g	Parallel-plate capacitance with glass dielectric
d	Array antenna element separation
d_{slot}	Defect element separation
d-z	Distance between membrane and driving electrode
E	Young's modulus
$\boldsymbol{E}$	Electric field
f	Frequency
f_c	Cutoff frequency
f_o	Resonant frequency
F	Force
FOM	Figure of Merit
g_1	One-pole low-pass filter element prototype value
h	Substrate thickness
H	Corrugation depth
k	Free space wave number
k	Spring force constant
l	Transmission line length
l_g	Dumbbell gap length
l_{slot}	Defect slot length

L	Inductance
L	Corrugation period
L_D	Line or dissipation loss
L_I	Insertion loss
L_M	Mismatch loss
L'	Normalized inductance
P_T	Power delivered to the load of a 2-port network
P_o	Source power
P_1	Power delivered to port 1 of a 2-port network
q	Membrane quality or profile factor
R	Resistance
R	Membrane radius
s	MEMS bridge spacing for DMTL phase shifter
S	Corrugation arc length
t	Copper membrane thickness
t_{air}	Air-gap thickness between copper membrane and insulator
t_g	Insulator thickness
$tan\delta$	Loss tangent
T_o	Transition temperature
T_c	Curie temperature
V	Voltage potential difference
V_i	Signal input
V_o	Signal output
w	MEMS bridge width for DMTL phase shifter
w_g	Dumbbell gap width
w_{line}	Microstrip transmission line width
w_{slot}	Defect slot width
W	Strip conductor width
W_e	Electrostatic energy
X_L	Transformed series reactance
X_{LC}	Reactance of the LC circuit

X_L'	Normalized series reactance of the prototype Butterworth filter
y_{strip}	Strip length
z	Displacement or deflection
Z	Impedance
Z_o	Transmission line characteristic impedance
Z_b	Stub impedance
Z_{in}	Input impedance
Z_t	Transmission line impedance for stub mounted loaded line phase shifter
Z_{LC}	Impedance of the LC circuit
β	Propagation constant
$\Delta\phi$	Path length difference
$\Delta\phi_{21}$	Differential insertion phase between port 2 and port 1 of a 2-port network
$\Delta\psi$	Phase progression between two successive array elements
ε	Permittivity
ε_{air}	Permittivity of the membrane air-gap region
ε_{cavity}	Membrane cavity permittivity
ε_{eff}	Effective permittivity
ε_g	Insulator permittivity
ε_r	Relative permittivity
ϕ	Phase
Γ	Reflection coefficient
Γ_S	Source reflection coefficient
Γ_T	Load reflection coefficient
Γ_1	Input reflection coefficient at port 1 of a 2-port network
η	Efficiency of a two port system
λ	Wavelength
λ_d	Dielectric wavelength
λ_g	Guided wavelength
λ_o	Free-space wavelength

μ	Permeability
ν	Poisson's ratio
v_p	Propagation or phase velocity
θ	Electrical length
θ_a	Slot orientation angle
θ_b	Shunt stub electrical length
θ_o	Beam scan angle
ω	Angular frequency
ω_o	Angular resonant frequency
ω_c	Angular cutoff frequency
ω'	Normalized angular frequency
ψ	Phase progression or digital phase state
ψ_n	Array element phase progression

CHAPTER 1

INTRODUCTION

1.1 Motivation

The goal of this research is to establish technology based on adaptive ground planes for use in electronic components, in particular phase shifting for phased array applications. The application of a defected ground structure in conjunction with micro-electromechanical systems (MEMS) devices was used to realize a novel phase shifting device, having the added benefit of a compact and lightweight structure. This phase shifting device has the potential to provide cost effective design alternatives for phased array reconfigurable antennas and substrates.

Beam-steering capability is a critical component of aerospace, satellite, and wireless antenna systems, for both commercial and military applications. Electronic beam steering of phased array antennas is achieved using phase shifters, allowing the antenna beam to be steered without a physical repositioning of the antenna. When analyzing the performance of a phased array system, factors that must be considered include the additional loss and systematic errors incurred in the system due to phase shifters, as well as the added burden of the control circuitry necessary to achieve beam scanning. Consequently, the actual undertaking of the phased array is costly, limiting their commercial application. Minimizing the size of the phased array is a constant challenge and is a fundamental requirement for aerospace applications. With the increasing popularity of wireless handheld products, the expectation of the user and industry is towards an increasingly compact and portable multi-function device. With this expectation, the need to further reduce the size and layout of system components becomes a priority. An affordable, easily reproducible and reliable phase shifter device would allow phased array technology to be more widely implemented.

Electronic beam steering in conventional phased arrays is achieved using external ferrite or solid-state phase shifters, while the antenna geometry is itself invariant. Ferrite devices are commonly bulky and expensive, while a trade-off between affordability and loss exists with solid-state phase shifter solutions. Incorporating the beam steering mechanism into the ground plane of the antenna, either in combination with or eliminating external phase shifters altogether, would greatly reduce the cost and bulk of a phased array. A complimentary technology is necessary in order to fully achieve the phase shifting process. Thus, the area of MEMS research has moved to the forefront. New technologies of micro-electromechanical systems offer an alternative to solid-state phase shifters. MEMS devices are extremely small in size and weight. The actuation of a simple MEMS switch can be achieved under the influence of an applied electrostatic force. Their insertion losses are extremely low, as are their power requirements, given that current consumption is negligible at switching time. This provides the potential for minimizing the cost and the bulk of added circuitry, and to achieve necessary power requirements required by spacecraft and handheld device applications. As the capability to fabricate and implement MEMS devices improves, their use as an alternative technology to further miniaturize existing hardware applications becomes a legitimate reality.

Miniaturization of device structures can also be achieved through layout/circuit size, a more common alternative for rendering a microwave/antenna system more compact. When considering the microstrip and coplanar media, popular configurations in the design of monolithic microwave integrated circuits (MMICs) and of antennas, reduction in layout/circuit size can be achieved by implementing structures in the ground plane as well as the trace layer. As a consequence of the increasing popularity of MMIC, the demand has risen to optimize the performance of these conventional transmission line structures. Recently, an explosion of research has developed in the domain of artificial dielectric structures, which has spread rapidly to the areas of microwave microstrip and coplanar technology. While artificial dielectrics themselves are well established and have been demonstrated using a periodic array of cylinders, their use in a planar medium is currently popular to optimize circuit and antenna performance on a common substrate. These structures were recently "rediscovered" as a consequence of the popularity of so-

called photonic bandgap structures, originally proposed in the late 1980s and demonstrated in the early 1990s [1]. Their use in the optical spectrum, together with design scalability, have lent their application to the microwave and millimeter-wave domains. Common and easily fabricated structures have been implemented using microstrip and coplanar media, specifically for use with microwave and antenna applications. One and two-dimensional periodic structures have been etched into the conductive layers, or holes have been drilled into the substrate medium to create necessary bandgap structures as a means to minimize surface wave excitation. In turn, the radiation characteristics of antennas are enhanced and losses within microwave circuits are minimized. This has led to the informal establishment of the following complimentary branches of study in recent years: Electromagnetic bandgap (EBG) structures, metamaterials, artificial dielectrics, and defected ground structures. While EBG structures are focused on the creation of an electromagnetic bandgap over a specific frequency band, artificial dielectrics and metamaterials have the direct design goal to alter the dielectric constant in the former case, or both the permittivity and permeability in the latter case. Defected ground structures form a broad category, encompassing any structure that imposes a defect in the ground plane of a circuit. In all cases, no matter the stated design goal, the effected outcome is achieved by altering the propagation constant of the system in question.

1.2 Brief Evolution of Reconfigurable Antennas

The arrival of photonic crystals and photonic bandgap research in the field of microwave technology would ultimately lend speculation toward their application for use within controllable or reconfigurable antennas and substrates. It was demonstrated in [2] that placing discontinuities along the structure could modify the transmission properties of periodic structures. Diodes were proposed for electronic control of a two-dimensional periodic structure at centimetre-wavelengths. Due to increasing losses of metallic structures at higher frequencies, optical laser control offered a means to achieve control at higher frequencies that have millimetre-wave properties. MEMS switches have also been

incorporated for use within smart antennas to adjust the radiating output of the antenna [3]. Opening or closing a particular switch, varying the overall geometry of the radiating elements of the antenna and thus its radiation pattern, may realize "variable-spacing phased arrays". The success of this design depends on many factors; the packaging of each MEMS component within the antenna must be considered, as well as the voltage required to actuate each individual switch. It is also necessary to ensure that the antenna substrate does not contribute any perturbations or reflections to the system.

The above concepts were more vigorously investigated at the end of the 1990s in the United States, when the Defence Advanced Research Projects Agency (DARPA) opened a competition geared at the development of reconfigurable aperture antennas, which became known as the Reconfigurable Aperture (RECAP) Program. The stated goals of the project were to focus on the development and integration of technologies that offer the capability of rapid reconfiguration through embedded techniques, with specific emphasis on reconfigurable ground planes [4]. In addition, the focus is toward efficient antenna operation over a wide frequency band, and the cost effective fabrication of these wideband antennas.

With the goal to tailor the frequency of operation via the reconfigurability of an antenna aperture, this project resulted in the initiation of research programs at universities including UCLA, University of Colorado at Boulder, Georgia Tech Research Institute, the University of Michigan, and the University of Illinois at Urbana-Champaign, in conjunction with or independently from industrial partners such as Northrup Grumman Corp, HRL Laboratories, among others. Various projects combining so-called "hot" areas of research, including the analysis and feasibility of photonic bandgap structures, cavity structures, MEMS technology, frequency selective surfaces and broadband design elements, were explored as a means to achieve the project goal. As a result of this project, publications detailing research supported by DARPA began appearing at the beginning of 2000. An example of a proposed integration of MEMS switches by UCLA and HRL is discussed in [5], whereby a cantilever structure switch was applied to reconfigure printed circuit dipoles and slot elements. Dipoles were either lengthened or shortened by the switch, changing operational frequencies and the phase of the radiated field through changes in the reactive impedance, while slot resonances were adjusted by

the opening and closing of the switch. An additional proposal involved a reflectarray approach, placing MEMS switches along the coplanar transmission line that forms the flared notch reflective elements. The results of this proposal were presented in [6] with five cascaded sections to demonstrate wideband performance. A reconfigurable cross-slot array was presented in [7], designed for operation from 1 to 6 GHz. This reconfigurable antenna aperture consisted of a multi-layer frequency selective surface and volume. Switches were placed along the top layer cross-slot array, and when switched open, the slot lengths were equivalent to $\lambda/2$ at 1.7 GHz, activating lower band operation between 1 to 3 GHz. With the switches in the closed state, the slot lengths corresponded to $\lambda/2$ at 4 GHz, resulting in the higher frequency band of operation, between 3 to 6 GHz.

As data from the DARPA funded RECAP projects was being published, interest in reconfigurable antenna technology utilizing emerging areas such as MEMS and EBG structures, began to expand. Simons, Chun, and Katehi introduced an antenna-MEMS design for the reconfiguration of the operating frequency [8]. A metal overpass was balanced by two MEMS actuators located on a patch antenna fabricated on high resistivity silicon ($\varepsilon_r = 11.7$), with spin-on-glass as a support layer ($\varepsilon_r = 3.1$). When in the OFF position, the antenna operates at its nominal frequency. When the MEMS actuators pull down the metal overpass, the capacitance of the metal overpass, in shunt with the antenna impedance, lowers the operating frequency of the antenna by 400 MHz to 24.6 GHz. A more dramatic difference in frequency band operation was presented by Rebeiz *et al.* [9] with a dual L- (1-2 GHz), and X- (8-12.5 GHz) band antenna consisting of a planar 3×3 microstrip array on duroid material with $\varepsilon_r = 2.2$. The MEMS "switches" were simulated as ideal OPEN (X-band) and CLOSED (L-band) configurations on two separate fabricated prototypes. Increased bandwidths of 1.2% in L-band and 7% in X-band were achieved with this design.

The concept of a switchable reconfigurable leaky-wave antenna was detailed in [10], where leaky-wave apertures were segmented into smaller patch antenna apertures. Switching was proposed with conventional devices or MEMS elements to control the mode of operation of the antenna, allowing moderate gain, multi-band frequency coverage using the patch elements, and high-gain, moderate bandwidth through the leaky-wave apertures. A microstrip patch antenna with switchable slots (PASS) for the

reconfiguration of the antenna polarization was presented in [11]. Thin orthogonal slots were etched into the antenna, with pin diodes placed along the mid-point of each slot to achieve the switching. Either right hand circular polarization (RHCP) or left hand circular polarization (LHCP) may be achieved by switching the appropriate diode on or off, without altering the feeding probe located along the diagonal of the antenna. Two antennas were fabricated, consisting of vertical and horizontal slots, with metal tabs used to represent the ON switch along a slot. If the tab along the horizontal slot is present, or ON, a RHCP pattern results, while if the horizontal tab is OFF and the vertical tab is present, the polarization is LHCP.

A reconfigurable ground plane was proposed in [12] to achieve a variation in the radiation pattern of a microstrip antenna. Elamaran *et al.* reported the use of a reconfigurable PBG ground plane to satisfy the beam steering requirement of a phased array. The design consists of a simple PBG structure composed of a series of etched holes in the ground plane beneath the transmission line feeds of the patch elements, as shown in Figure 1.1 (a). The reconfiguration of the beam is achieved by varying the number of periods in the PBG structure. According to the authors, the insertion loss should be lower than that of solid-state phase shifters, since the reconfiguration is done in the ground plane. Covering the PBG holes by conductive tape altered the number of PBG periods, resulting in the reconfiguring of the beam. The phase shifts were found to be proportional to the number of periods. An 18 period design was implemented, similar to the smaller scaled version shown in Figure 1.1 (a). Their design obtained a maximum steering angle of 35° with the array steering at 6° increments. Frequency controlled scanning was also examined, since the electrical distance between periods is altered with frequency change. Therefore, for a fixed PBG lattice, a beam steering angle of 15° was achieved by changing the operating frequency from 5 to 6 GHz. It was the intent of the researchers to implement pin diode switches and MEMS switches to the reconfigurable PBG structure, in place of the conductive tape.

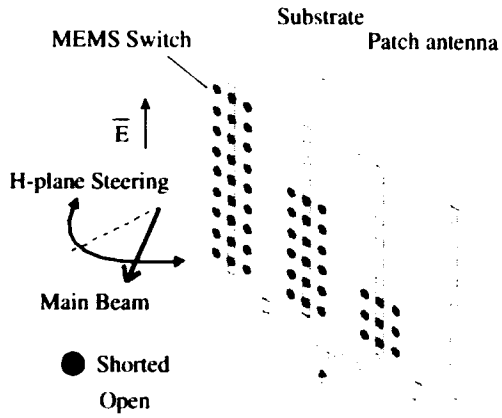


Figure 1.1: *4-element patch array with PBG ground plane [12], [13].*

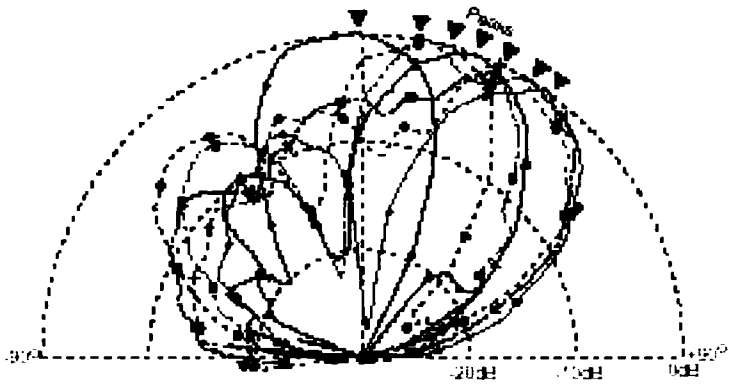


Figure 1.2: *Measured beam patterns for different ground plane configurations [12].*

Recently, a similar idea was also proposed and implemented by Hwang *et al.* [14], in which rectangular slot defects were imposed in the ground plane, in lieu of the circular shaped elements in [12]. Large number of identical and equidistant slots, of up to 56 elements, were placed under a microstrip transmission line. To achieve a continuous phase shift, a sliding conducting plate was used to progressively cover selected slots, as shown in Figure 1.3. However, the relationship between the slot geometry and slot separation with respect to the phase shift values were not presented.

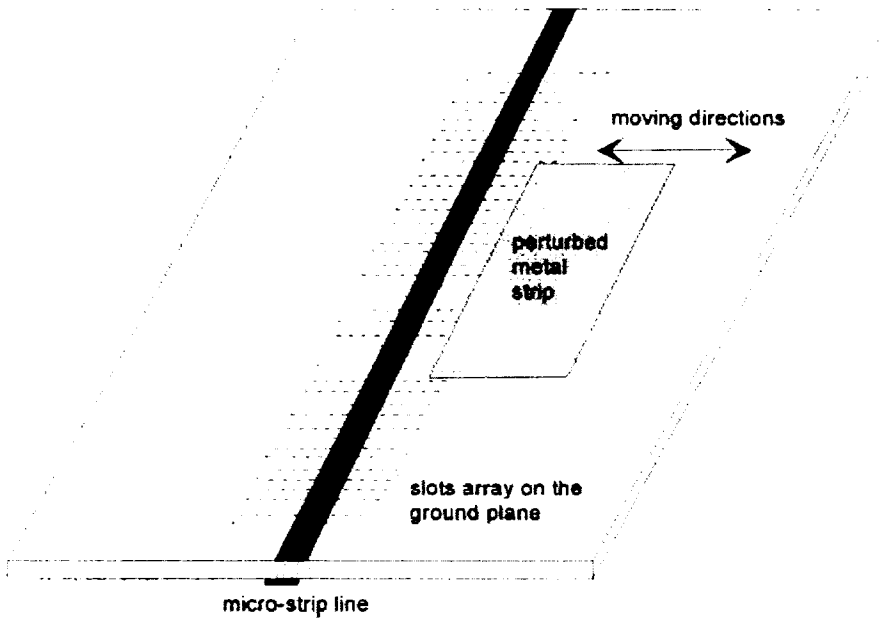


Figure 1.3: *Structural configuration of slotted microstrip line perturbed by a metal strip (top view) [14].*

1.3 Objective

In considering MEMS technology for phase shifters, the conventional approach dictates the use of circuit architectures similar to solid-state phase shifters. In such designs, a delay-line technique is commonly used to control the amount of phase shift, initiated by variable MEMS capacitors. However, adopting a design from solid-state switches may not provide optimum phase shifting by a MEMS device. It is therefore proposed to investigate the phase shifting capability of a defected ground plane for applications in phased array antennas. With this configuration alternative, there is no variation in the transmission line length to achieve the phase shifting. Rather, the concept is based on the simple alteration of the transmission line network of the phased array, by etching slotted defects in its ground plane. Its implementation therefore, does not require a separate technology or hardware. It can be fabricated within an existing phased array by integrating the design into that of the antenna feed network. Control of the phase shifter is provided by the actuation of a micromachined, corrugated, copper membrane, whose control circuitry is physically separated from the phased array signal path by a conducting ground plane.

Fundamentally, this architecture constitutes a loaded line phase shifter, as the defect impedance loads the transmission line, whose fabrication is compatible with present integrated circuit/antenna technology. The proposed phase shifters are ideal for antenna arrays utilizing microstrip technology, further complimenting microstrip advantages of low profile and lightweight conformable structures. There is, therefore, potential for the use of a membrane backed defected transmission line phase shifter with phased array antennas, for telecommunications and satellite applications.

1.4 Scope

Chapter 2 provides a review of conventional beam scanning technologies and discusses their salient features. It also summaries briefly the main emerging concepts compatible with planar microstrip antenna arrays using novel materials and fabrication

techniques. The fundamental research and contributions of this thesis with respect to defected ground structures are presented in Chapters 3 and 4. Chapter 3 provides a detailed study of uniform slots, and establishes their working principles. Chapter 4 extends the work presented in Chapter 3 to more efficient defect structures based on dumbbell shaped slots, and determines the figure of merit (FOM) of such defects for phase shifter design.

The application of the ground plane defect for loaded line phase shifters in phased array applications is discussed in Chapter 5. Two novel design methodologies are proposed, based on "minimum size" and "minimum return loss" criteria. Sample designs of defected transmission line phase shifters are provided, having high and superior figure of merits. Finally, Chapter 6 proposes and investigates a unique and novel concept for implementing reconfigurable ground plane defects based on micromachined membrane technology. An electrode actuated ground plane membrane was placed below the ground plane defect and used to alter its phase shift, thereby allowing control of its phase shift and thus the antenna beam scan. Also investigated in Chapter 6, are methods for minimizing the electrode control voltage. A unique property of the membrane architecture is the physical separation of the control signal of the electrode from the RF signal of the defected transmission line phase shifter, thus minimizing their interactions. Chapter 7 summarizes the contributions of this thesis and briefly lists some main areas for future research.

CHAPTER 2

LITERATURE REVIEW

Beam scanning in phased array antennas is normally achieved using a phase shifting network, which sets the array element phases, in accordance with a beam scan algorithm. The hardware technology for such a phase shifting network normally depends on the operating frequency and power, the beam switching speed and the insertion losses of the corresponding circuits. To appreciate the motivation for the proposed research, this chapter summarises the main conventional phase shifting technologies that have been used to date in phased arrays. The advantages and disadvantages of each technology are presented briefly, including discussion into research areas of emerging phase shifter technologies, such as ferroelectric thin films and micro-electromechanical systems.

2.1 Phase Shifting Technologies for Phased Arrays

The phase ϕ, of an electromagnetic wave along a transmission line is a function of the frequency f, propagation velocity v_p, and line length l, and may be expressed as [15]:

$$\phi = \frac{2\pi f l}{v_p} \tag{2.1}$$

where the propagation velocity is a function of the permeability μ, and the permittivity ε, of the medium,

$$v_p = \frac{1}{\sqrt{\mu\varepsilon}} \tag{2.2}$$

Thus, any variation of the above parameters will cause a change in the phase of an electromagnetic wave travelling along a transmission line. Early phase shifters involved so-called electromechanical devices that utilized mechanical means to physically alter the electrical length of transmission lines or the dimensions of a waveguide [15]. These

devices achieved switching speeds on the order of milliseconds and are no longer widely used. Conventional digital phase shifter technology has focused primarily on applying the properties of ferrimagnetic material or semiconductor devices to obtain a phase shift. More recent technologies have been devoted to implementing ferroelectric thin films and MEMS components as phase shifters. With ferrite phase shifters, a change in the permeability and thus the propagation velocity is achieved by the applications of an external bias voltage to manipulate the magnetic properties of the material. A similar process is attempted with ferroelectric materials to alter the material permittivity through the application of an external electric field. Semiconductor phase shifters utilize diode, field effect transistor (FET), or MEMS switching devices to switch in and out of transmission lines, affecting line lengths.

Phase shifters may be analog, implementing a continuous phase variation, or digital, where a discrete phase shift is realized using a set of predetermined values [16]. For example, the common four-bit design has phase bits of 0°, 22.5°, 45°, 90°, and 180°. While analog control devices possess distinct advantages when compared to their digital alternatives, *e.g.* no quantization errors, and no special foundry processes required for the device fabrication [17], they are not inherently compatible with the digital architecture and algorithms providing the electronic beam scanning of a phased array, as are their digital counterparts. The focus of the following sections will thus be on digital phase shifter implementations.

2.1.1 Characteristics

Operating frequency, power per phase shifter, as well as size and weight, are factors that contribute to the selection of a phase shifter for a particular application. Cost is inevitably increased by the desire to achieve good device performance. Ideally, a phase shifter for use in a phased array should posses the following characteristics [17]-[19]:

- **Beam switching speed**: It is desirable to realize the shortest possible switching time, at least on the order of microseconds.

- **Insertion loss**: Insertion losses result in a reduction in generated power during transmission, as well as in signal to noise ratios during reception. Additional power amplifiers are necessary to overcome loss at the expense of increased power consumption and cost. Increased insertion losses also raise the phase shifter temperature, and thus should be kept to a minimum.

- **Phase errors**: Quantization error should be kept low so that consistent phase reproduction is achieved between devices. Pattern and gain degradation will also be minimized.

- **Cost**: Phased arrays are, by and large, expensive undertakings due to the large number of radiators and control devices used to maintain power levels and phase. For this reason they have been almost exclusively developed by the military. In the interest of affordability therefore, it is desirable to minimize the overall cost of the application.

- **Weight and physical size**: Practically, weight and physical size must be kept as low as possible, simplifying the layout of the devices within the formation of the array system.

- **Power**: Issues concerning power include the handling ability of the device, as well as the stability of the device characteristics with temperature, particularly at high power levels. High power requirements would negatively influence the size and weight of the array system, and consequently the overall cost. Drive power is high with diode phase shifters, since they require both holding and switching power. Ferrite phase shifters can be latched and thus do not continuously consume

power. Transmitted power levels are dependent on radar range and data rate. Levels beyond peak values of 10 kW would traditionally necessitate a ferrite device.

- **Reproducibility**: Ease of construction and high manufacturing tolerance levels are advantageous to ensure the reproducibility of the device. If the performance of the device cannot be repeated due to construction limitations, additional control circuitry and expense are required to tune the system.

- **Thermal Stability:** Material properties are affected if temperature levels are variable, a phenomenon that is common with ferrite and ferroelectric applications, in particular with ferrites at low frequencies. For example, ferrite magnetization characteristics are temperature dependent, and in turn, phase shift is dependent on the magnetic permeability of the material.

2.2 Conventional Phase Shifting Techniques for Phased Array Antennas

2.2.1 Ferrite Phase Shifters

Ferrite phase shifters employ ferrimagnetic materials whose permeability may be controlled by an applied magnetic field. An external magnetic field is used to drive the ferrite into saturation to achieve the desired phase. Ferrimagnetic materials possess high permeability and hysteresis characteristics, but their atomic spins are unequal in magnitude and are anti-parallel, which gives rise to a net magnetic moment [20]. Their magnetic permeability is dependent on orientation and is thus anisotropic. Material selection for these devices derives from ferrimagnetic spinels and garnets, two basic metal oxides for which fabrication is quite costly. At higher microwave frequencies (above S-band, 2-4 GHz), waveguide ferrite phase shifters are preferred to solid-state devices, due to lower loss and more favourable power handling capabilities [18]. Ferrite devices, in general, easily satisfy bandwidth requirements [21]. They may involve a microstrip or waveguide structure, the waveguide being the more dominant configuration for its superior performance. These phase shifters may be reciprocal, or non-reciprocal devices. Reciprocity is a necessary condition to achieve an identical phase shift during transmission or reception [19], [22], irrespective of the direction of propagation of the electromagnetic wave. The most common types of ferrite phase shifters are:

- Reggia-Spencer
- Toroidal latching

2.2.1.1 Reggia-Spencer Phase Shifter

The reciprocal Reggia-Spencer ferrite phase shifter was first employed in a phased array in 1957 to provide continuous phase shift. An axial ferrite rod is placed in a rectangular or circular waveguide, with an external wire coiled about the waveguide

structure as a solenoid, as shown in Figure 2.1. The solenoid allows the application of a bias current to the structure producing a longitudinal magnetic field. A variation in the material permeability μ_r, and thus the associated propagation constant β, results from the applied magnetic field. Consequently, a phase shift occurs which can be manipulated by the applied current.

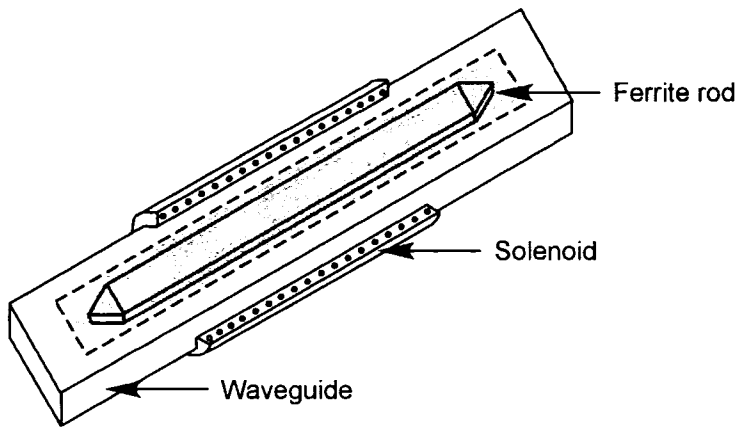


Figure 2.1: *Reggia-Spencer phase shifter [22].*

A disadvantage in the design of the Reggia-Spencer is the limited thermal dissipation of the device. Because the ferrite rod is located in the center of the waveguide, heat dissipation is radiated since the rod is not in contact with the waveguide walls. It is necessary for the thermal environment of the Reggia-Spencer to be strictly controlled, as any temperature variation may cause a change in phase, with ratios reported at 1:1 for degree of phase change per °C of variation. The power handling of the device is also negatively affected. A low-loss dielectric cooling liquid has been successfully used to cool the ferrite bar, also allowing for a high peak power [15]. With this implementation, a phase shifter volume of 2.4 × 2.1 × 8.2 inches and weight of 1.5 lbs had a reported maximum handling power of 100 kW and average power of 600 W. Switching speed and insertion loss were reported to be 125 μsec and 0.9 dB, respectively.

The possibility of shorted turns between the external solenoid and the waveguide also exists with the architecture of the Reggia-Spencer device. This would result in a reduction in the applied magnetic field and a time delay, and consequently an increase in switching time and power requirements to attain the desired phase. Also, in order to overcome hysteresis errors that alter permeability values, switching time is further increased, to allow an additional pulse to drive the ferrite to saturation prior to sending another phase shift setting to the solenoid [22].

2.2.1.2 Toroidal Latching Phase Shifter

While the Reggia-Spencer provides continuous phase shift, the toroidal latching phase shifter, a non-reciprocal device, has the capability to provide discrete phase shifting. The architecture involves a toroidal core placed symmetrically within a waveguide, as shown in Figure 2.2.

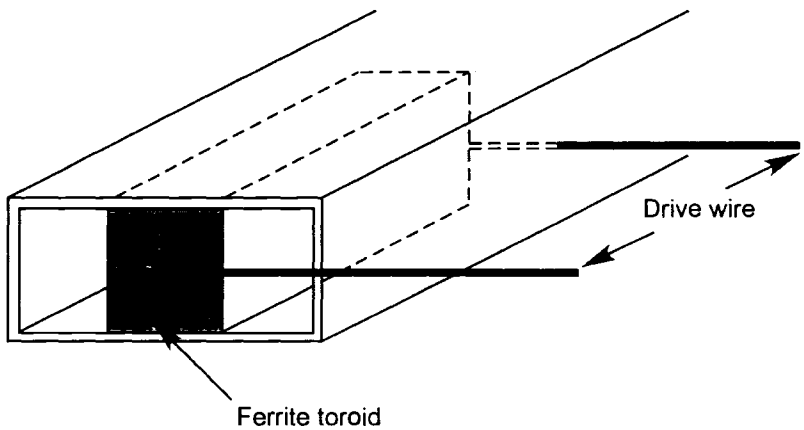


Figure 2.2: *Toroidal ferrite phase shifter [22].*

A drive wire excited by either a positive or negative current is passed through the center of the toroid. In this device, the bias current is not continuous, but rather pulsed, allowing for its release when the ferrite reaches saturation. When released, the material is then in a remanent condition of magnetization. This state is either positive or negative, depending on the polarity of the current pulse. A differential phase shift results between the two remanent states, a function of the electrical length of the toroid. The toroidal latching phase shifter utilizes the properties of the material hysteresis loop to achieve a non-continuous phase shift. This is in contrast to the Reggia-Spencer device where hysteresis was a hindrance to be overcome during operation. A four-bit digital phase shifter is achieved with this device by implementing several ferrite sections of decreasing lengths, to realize the necessary binary phase shifts of 180°, 90°, 45°, 22.5°, and 0°.

The toroidal ferrite phase shifter is also referred to as a latching phase shifter, since the ferrite is latched in one of two remanent states of magnetization, either positive or negative. The drive power applied to the toroidal phase shifter is therefore less than the Reggia-Spencer because of its current latching condition. The Reggia-Spencer requires that the bias current is held and not latched, a disadvantage in terms of necessary power levels as well as cost. Because the magnetic field is applied to the toroid within the waveguide, there is no danger of shorted turns and thus a greater switching speed may be realized. Peak power of 100 kW is attainable by the toroidal device with an average power of 1 kW. Switching time is generally between 2-10 μsec, with average insertion losses of 0.5 dB. The weight of the device may be approximately 1 oz at X-band (8-12.5 GHz) or greater at S- (2-4 GHz) or C-band (4-8 GHz). The device figure of merit, as the ratio of the phase shift in degrees per dB of loss, may be improved and required switching power decreased by filling the toroid slot with high dielectric material. This is at the expense of peak power capabilities [15], [21]. Peak power of 1-10 kW has been reported with dielectrics having a relative permittivity of 30 to 50 at S-band. This technique also has the advantage of decreased system cost, as this allows for a reduction in the necessary oxide material.

2.2.2 Semiconductor Phase Shifters

A disadvantage of ferrite phase shifters is their high cost and bulk. While ferrite devices cannot be miniaturized, solid-state phase shifters satisfy the size and weight constraints necessary for compact designs and can be easily incorporated within integrated circuit packages. Semiconductor device phase shifters are phasers that utilize diodes or FETs to switch in or out of different lengths of lines. They are commonly used when RF powers are low. At frequencies between 1-10 GHz, RF power on the order of milliwatts is generally handled by FETs, while PIN diodes have a higher handling ability, up to 1 kW [23]. Typically, PIN diode phase shifters are preferable at lower frequencies (e.g. < 2 GHz) due to lower insertion losses than ferrite devices. Below S-band (2-4 GHz), ferrite use is hampered by temperature sensitivity. The insertion loss of PIN diode phase shifters increase with increasing frequency, and thus ferrite devices acquire a competitive position above S-band. Both the ferrite and PIN diode devices are comparable within the frequency range of 2.5-3.5 GHz. Figures of merit for semiconductor phase shifters range from 200°/dB at 12 GHz and below, to 86°/dB at 18 GHz, 60°/dB at 60 GHz, and 41°/dB at 94 GHz [23].

Silicon PIN diodes have been the dominant solid-state switching device, possessing high breakdown voltages, a characteristic that sets the upper limit for its power handling capabilities. They are thus useful when high-power digital phase shifters are required and maintain stable characteristics over long periods of time when switched between forward or reverse bias. Much like unlatched ferrite phase shifters, semiconductor diode phase shifters require a continuous bias current [22]. Thus, power requirements for diode phase shifters are generally higher in comparison to a latched ferrite phaser. Gallium arsenide (GaAs) FETs have also acquired some popularity within the development of phase shifters for monolithic circuits, while PIN diodes are found more often in MIC phase shifters. In comparison to ferrite phase shifters with switching speeds of 1 to 50 μsec, diode phase shifters can provide very high-speed switching ranging from 10 nsec to 1 μsec. The GaAs FET, however, generally provides a greater switching speed than the PIN diode (≤ 1 nsec [24]), due to the very high mobility of the carriers in a GaAs FET device [25].

The most common types of semiconductor phase shifters can be classified as either transmission-type or reflection-type phase shifters. They include:

- switched-line
- loaded-line
- reflection-line

Reflection-type phase shifters are typically one-port devices that utilize the reflected signal at a terminated transmission line to obtain a phase shift. Switched-line and loaded-line transmission-type phase shifters are two-port networks in which phase shift occurs due to a change in the phase of the transmission coefficient through the device. In an ideal, lossless reflection-type phase shifter, the reflection coefficients are unity. Similarly, the magnitudes of the transmission coefficients are unity for lossless transmission-type phase shifters. These architectures may also be implemented with analog devices by replacing the diode or FET switching elements with a variable reactance device (e.g. a varactor diode), with continuous phase control provided by a variation in the DC bias. Details of the above listed semiconductor phase shifters are provided in the following sections, with focus on passive mode architectures.

2.2.2.1 Switched-Line Phase Shifter

The switched-line phase shifter is the simplest semiconductor configuration, and is also referred to as the switched-network phase shifter. The switched networks in this case are represented by two transmission line sections of different arbitrary lengths, l_1 and l_2, as illustrated in Figure 2.3.

A minimum of four devices (e.g. PIN diodes) per phase bit are used to represent a single pole double throw (SPDT) switch at both the input and the output of the phaser, routing the signal along either line l_1 or l_2. The losses of both switches and the two-transmission lines account for the losses associated with the phaser. The differential phase shift is simply a function of the propagation constant β and the path length

difference, i.e. $\Delta\phi = \beta(l_1 - l_2) = 2\pi f/v$ as in (2.1). Thus, this device provides true-time delay, as the phase shift is directly proportional to the operating frequency. High isolation losses may occur due to resonance in the OFF state, which result when the line lengths are multiples of a half-wavelength. Selecting line lengths other than half-wavelength multiples and compensating for the loss by designing a high isolation switch are techniques for minimizing isolation loss. A common variation of the switched-line configuration involves the replacement of the transmission lines with low-pass and high-pass filter networks.

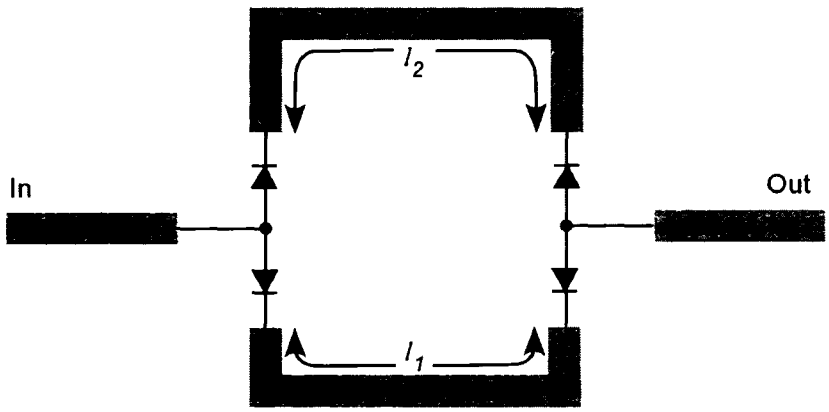


Figure 2.3: *Switched-line phase shifter [22].*

This device can provide broadband phase shift, but is dependent on frequency and the number of phase bits available. A minimum of phase bits is more desirable below 1 GHz, whereas at millimeter-wave frequencies, 5-bit implementations are possible [17]. Insertion loss of less than 2 dB in the ON state and isolation greater than 18 dB in the OFF state, between 42-46 GHz, was reported in [26], for a 4-bit GaAs MESFET device.

2.2.2.2 Loaded-Line Phase Shifter

The loaded-line phase shifter, also a transmission type device, is commonly employed for 22.5° or 45° phase bits, when smaller phase shift increments are desired. A transmission line is loaded at each end by shunt susceptances $Z_b = jB$, implemented by either lumped components or a stub of length θ_b. Single pole single throw (SPST) diode switches are either directly mounted on the main line or stub-mounted across the main line, respectively. The configuration of a stub-mounted loaded-line phase shifter is given in Figure 2.4, where θ and Z_t are the line length and impedance between the stubs.

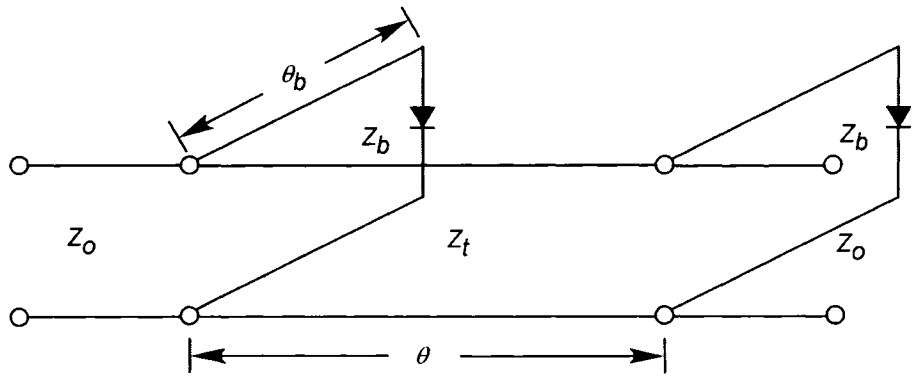


Figure 2.4: *Stub-mounted loaded-line phase shifter [16].*

Identical susceptances and an optimal line length of a quarter-wavelength will minimize the unavoidable reflections that occur with this design. Reflections for a line length of $\lambda/4$ are almost equal in magnitude and 180° out-of-phase, and thus are effectively eliminated [16], [22]. Phase shift increments are kept to a minimum to maintain acceptable return losses [17], as good impedance match is difficult with this configuration. Return loss degrades as the device deviates from its operating frequency, becoming narrowband with larger values of relative phase shift. With smaller phase shift increments, this phase shifter possesses a wide bandwidth, as well as a low SWR [24]. Larger susceptances are necessary to achieve a greater phase shift, but have adverse effects on bandwidth and SWR. This configuration is thus considered inefficient for larger phase shifts, e.g. 360°, as considerable layout area would be necessary.

2.2.2.3 Reflection-Line Phase Shifter

The reflection-line phase shifter involves a reflection-type architecture. A differential phase shift of $\Delta\phi = \phi_1 - \phi_2$ is achieved by switching between two reflection coefficients $\Gamma_1 = |\Gamma_1|\angle\phi_1$ and $\Gamma_2 = |\Gamma_2|\angle\phi_2$. A switchable-reactance reflection-type filter involves the use of a SPST switch to alter the reactance terminating the transmission line. In order to implement a two-port configuration, a 90° hybrid is commonly coupled to the network, as shown in Figure 2.5. The advantage of this architecture over the switched-line configuration is the number of switching devices per phase bit. With the hybrid, only two devices per bit are required, while four are necessary for the switched-line [25]. This device typically accommodates larger phase bit requirements, in excess of 45°. Insertion loss of 1-2 dB per phase bit is possible with this configuration [27]. However, low-loss phase shifting is increasingly difficult with hybrid couplers above 40 GHz.

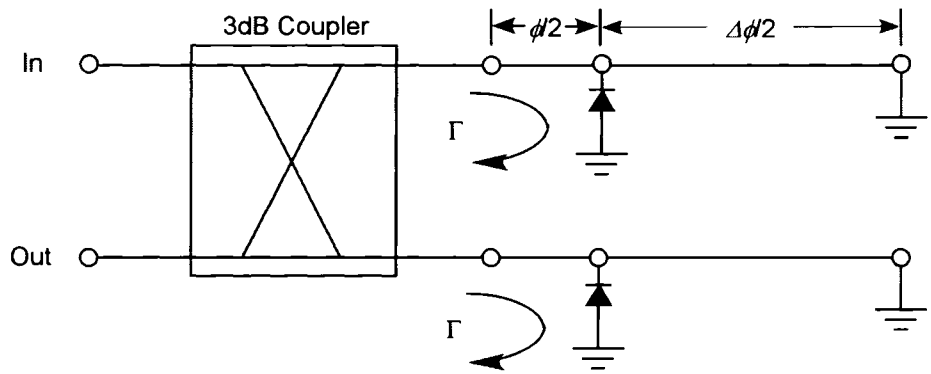


Figure 2.5: *Reflection-type phase shifter [22].*

Other 3 dB couplers may be substituted for the hybrid, e.g. the branch-line coupler or the Lange coupler. A switching time of 1.7 nsec was reported for a branch-line coupler phase shifter, with losses of 1.6 dB ± 0.2 dB at 12 GHz [28]. Power handling was verified to 800 mW, with further analysis indicating that the diode device can sustain 1100 mW. A return loss of at least 20 dB was achieved in the operating range of 11.7-12.2 GHz.

2.3 Emerging Phase Shifting Techniques for Phased Array Antennas

Phase shifters implemented using thin film ferroelectrics, optical techniques, ferrite substrates, low temperature cofired ceramics, and MEMS technology are among the emerging phase shifter technologies proposed for RF applications today. These areas are novel and interdisciplinary, integrating the fields of microwave and electronic devices, as well as material science. These applications borrow fabrication techniques from integrated circuit technology, an advantage in their implementation with printed circuits and substrates. However, research into these emerging areas is ongoing, with efforts focusing on the improvement of fabrication, reliability and performance.

2.3.1 Ferroelectric Thin Films

Ferroelectric materials have recently been applied for use in phased array antennas, as an alternative to ferrite and semiconductor based phase shifters. The application of an electric field to a ferroelectric produces a change in the permittivity of the material, allowing the control of the device phase. Ferroelectrics possess a high material permittivity, ranging from 50 to several thousand, which is largely dependent on material composition, as well as temperature. High permittivity, as well as the use of a bias electric field, allows for the advantage of smaller physical size and weight in comparison to a ferrite phase shifter, which is bulkier and necessitates a magnetic field bias [29].

By means of some deposition process, a thin film of the ferroelectric is grown on a planar substrate, a configuration that allows for compatibility with a planar circuit or antenna. Phase shift is obtained by a DC voltage-controlled lumped barium-strontium titanate capacitor in a coaxial line or microstrip arrangement [30]. The present level of DC potential applied to a ferroelectric can be as high as several thousand volts [29]. The use of thick film ferroelectrics at high frequencies was somewhat restricted in the past, due in part to the large bias voltage required to produce a significant change in the permittivity of the material [31], [32], but also due to their bulk and high unit cost. In

contrast, thin films are lightweight and require only a low or medium bias voltage to tune the device. Typically, a low voltage on the order of 0-40V may be applied [33]. The thin film may thus be used in tunable microwave devices, as well as beam steering and phased array applications. However, it is important to note that issues of low loss, low cost, and low bias voltage with ferroelectric thin film phase shifters have not been simultaneously addressed or achieved [34].

Efforts to improve material purity and device tunability has encouraged research towards fabrication and material issues, such as film thickness, doping, substrate choice, and temperature, and their effects on the electrical properties of the material. Design, control, and other documented data may be highly dependent on the composite and its fabrication. This application thus has interested researchers in the areas of material science, as well as electronics and microwave engineering.

2.3.1.1 Basic Material Properties

Ferroelectric materials are nonlinear dielectrics whose relative dielectric constant ε_r may be tuned by an applied DC electric field [31]. They are the dielectric analogue of ferrimagnetic materials whose magnetic permeability is a function of an applied magnetic field. Due to the spontaneous alignment of ions, permanent electric dipoles exist within a ferroelectric compound. This state is referred to as the ferroelectric phase, where the crystal is distinguished by a lack of ionic symmetry at its center. The relative alignment of the positive and negative ions within the crystal in the ferroelectric state is slightly deformed, forming an ionic dipole moment [35], [36]. Ferroelectric properties are destroyed by increased thermal collisions above a certain transition temperature T_o, which in most ferroelectrics is identical to the Curie temperature T_c. Under these conditions, the material is said to be in a paraelectric state. The transition from the ferroelectric to the paraelectric state is a solid-to-solid phase transition [29]. The crystal assumes a symmetric cubic structure when in the paraelectric phase.

Anticipating the effect of an applied electric field bias on the material dipoles is difficult, complicating phase shifting when operating in the ferroelectric state. The

operation temperature may also be difficult to select as the Curie point temperature can shift several degrees Celsius depending on the strength of the applied electric field bias [29]. Material quality suffers at the Curie point, as internal stresses break down the ferroelectric, and it is not prudent to repeatedly expose the ferroelectric to the transition temperature. The material is operated in its paraelectric region, at a temperature slightly above the Curie point (approximately 10°C), where hysteresis effects due to the applied E-field are also small [29]. The property of high permittivity must also be considered when using conventional microwave equations that have been derived for permittivities of $\varepsilon_r < 50$.

2.3.1.2 BSTO

Barium strontium titanium oxide, or BSTO, is the most commonly used ferroelectric thin film composite, having the chemical formula $Ba_{1-x}Sr_xTiO_3$. The transition temperature is closer to room temperature than most other ferroelectric materials that require cryogenics for their operation. A common molar ratio is $Ba_{0.6}Sr_{0.4}TiO_3$, with a transition temperature of 290K [37]. BSTO possesses attractive properties for high frequency applications, which include [33], [38]:

- **High dielectric constant**: This parameter typically has a magnitude of ε_r = 200-300. A high dielectric constant provides the advantage of smaller physical dimensions.

- **Field dependent permittivity**: Ratio of 4:1 variation. The DC biased electric field also offers negligible DC power consumption.

- **Rapid polarization response**: This property is suitable for rapid tuning and thus optimum phase shifting.

- **High breakdown field**: Electric field breakdown of the material is typically greater than 2×10^6 V/m, providing excellent power handling capability.

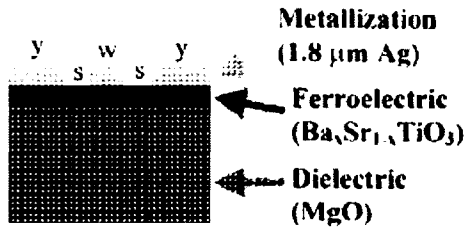
2.3.1.3 Tunability and Loss

A critical material parameter to be considered is the loss tangent ($\tan\delta$) of the ferroelectric. The loss tangent is an intrinsic material property and is a measure of the power loss in a particular medium [39]. It is thus desired to be as small as possible. A low loss tangent is advantageous for obtaining an optimum phase shifter figure of merit, i.e. degrees of phase shift per dB of loss. The permittivity of a ferroelectric is high and consequently, the loss tangent is intrinsically high in these materials. For this reason, their exploitation as phase shifters has perhaps not been fully realized. Prediction of the material permittivity and loss tangent with respect to the external electric field, as well as frequency, is critical for a characterization of potential material devices with some confidence. Various established analysis techniques have been proposed and compared, which include method of moments, finite element method, and conformal mapping [41], [42].

For strontium titanium oxide, $SrTiO_3$, phase shift increase has been shown to be linearly proportional to increasing film thickness, but similar linear results are not achieved with thin film BSTO [43]. For the coplanar waveguide structure in Figure 2.6 (a), the effect on the phase shift slope (at any given frequency) for BSTO samples of different thickness is shown in Figure 2.6 (b), with respect to increasing ε_r. A greater phase shift is achieved with thicker BSTO films [41]. A plot of the ε_r with respect to the applied electric field, determined by measurement and simulation from 13.6 GHz to 20 GHz, is also provided in Figure 2.6 (c). While an increase in phase is possible, increasing BSTO film thickness has been shown to increase tanδ [34]. Beyond approximately 0.5μm, film quality degrades and benefits are no longer observed. It should be noted that lowering ε_r while also increasing film thickness with the intent to reduce losses, would as a consequence increase the necessary dimensions of a microwave circuit. Hence,

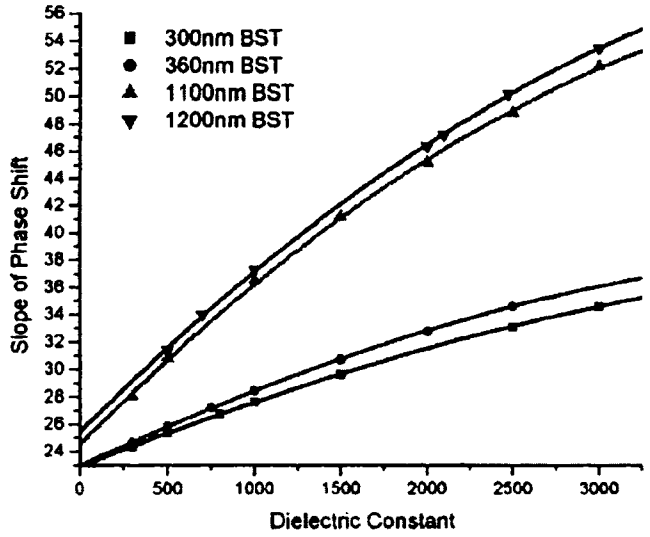
increased layout size and thickness may be a compromise for reduced loss [43]. The addition of dopants such as manganese and magnesium to BSTO composites [40], [43], [44] and the reduction of material imperfections through the application of an annealing process [33], [43], have been shown to reduce the losses in the thin film.

The loss tangent increases with increasing ε_r of the ferroelectric [40], as does the dielectric tunability, i.e. the variability of the ferroelectric permittivity by an applied electric field. Lower permittivity materials have lesser loss tangents and lower insertion loss. A high dielectric tunability is desired to maximize phase shift, ideally exhibiting a change in material permittivity with applied DC voltage of greater than 10%. Thus, a trade-off exists between the optimum tunability and lower loss tangent.

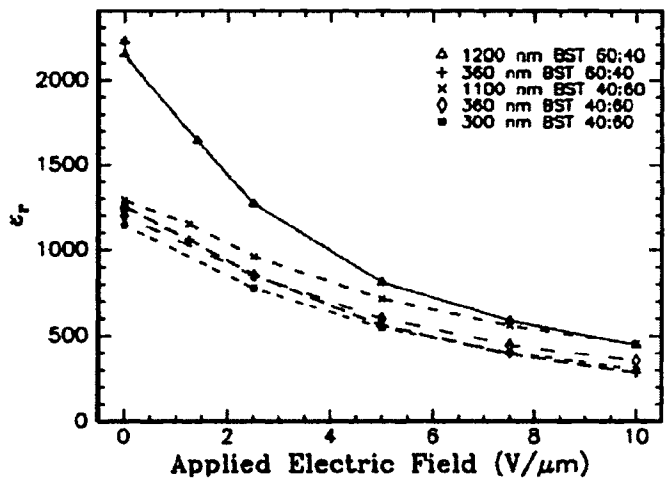


(a)

Figure 2.6: *(a) CPW structure with a magnesium oxide (MgO) substrate and silver (Ag) metallization, (b) simulated slope of total phase shift vs. ε_r for BSTO of different thickness, (c) dielectric constant of four BSTO films as determined by CPW measurements from 13.6 to 20 GHz and simulated calculations [41].*



(b)



(c)

***Figure 2.6** continued*

Lowering the barium content Ba_{1-x} is also useful in reducing the loss of BSTO. With increasing barium content, the material also becomes more paraelectric, as the Curie temperature is lowered. Experiments performed in [44] (at 1 kHz and E-field bias of 2.0 V/μm) using BSTO with barium content Ba_{1-x} ranging from $x = 0$ to $x = 1.0$, show that materials containing $Ba_{0.45}$ to $Ba_{0.6}$ possess the most attractive electrical parameters, i.e. ε_r, $\tan\delta$, and tunability. The tunability of BSTO with barium molar ratios from 0.0 to 0.40 was too low (less than 10%), while those with 70-100% barium content have loss tangents that are too high. In essence thus, each electrical parameter may be lowered by effectively lowering the content of barium in BSTO. Thus, while it is advantageous to reduce the barium in order to achieve a lower loss tangent, it is at the expense of the tunability of the compound, as well as a variation in the transition temperature.

2.3.1.4 Coupled Microstrip Line Phase Shifter (CMPS)

A recent implementation of a ferroelectric thin film phase shifter is the coupled microstrip line phase shifter (CMPS), which consists of series coupled sections of transmission lines [32], [43]. Each line is a single-pole filter structure that undergoes a phase shift in its passband when the ferroelectric layer undergoes a DC bias. Quarter-wave radial stubs in series with a high impedance transmission line are used to apply the DC bias to each microstrip line section. The eight section CMPS shown in Figure 2.7, was etched overtop a 750 nm layer of ferroelectric deposited on a lanthanum aluminate substrate ($LaAlO_3$), having an $\varepsilon_r = 25$ and a thickness of 254 μm. A maximum phase shift of 299° was achieved with a figure of merit of 43°/dB for a Ba:Sr ratio of 40:60 using 400V DC bias. Insertion loss at room temperature is thus 6.95 dB. The phase shift in degrees per dB of loss was improved using a 4 section CMPS structure over a 508 μm thick magnesium oxide (MgO) substrate of $\varepsilon_r = 9.8$, with a thin film thickness of 500 nm. A figure of merit of 54°/dB was achieved with Ba:Sr ratio of 60:40, and a dopant of 1% manganese (Mn) at 15 GHz, but a maximum phase shift of only 114° was attained. The larger dimensions of the MgO circuit, due to the lower dielectric constant and thicker substrate, accommodated a larger DC bias. Increased phase shift however would require

additional CMPS elements. Strontium titanium oxide ($SrTiO_3$) thin films of similar CMPS devices deposited on a $LaAlO_3$ substrate, achieved a maximum phase shift of 484° over 80°/dB insertion loss, to a maximum insertion loss of 6 dB at 16 GHz. These results were achieved under cryogenic conditions, well away from room temperature [43].

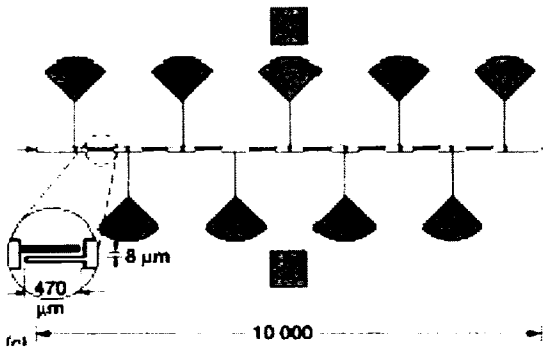


Figure 2.7: *Schematic of 8 element 50Ω CMPS [32].*

2.3.2 Optical Phase Shifters

Optical control has been put forth as an alternative technology for phase shifters as operating frequencies have been pushed beyond the 30 GHz mark [2]. At extremely high frequencies, use of light as a means of adaptive control will eliminate loss issues common to metallic structures at shorter wavelengths. Fabrication of microstrip lines becomes more difficult with increasing frequencies, and thus waveguides composed of dielectric, specifically high purity semiconductor materials, are generally implemented as an alternative to metal structures. Conventional phase shifters or switching devices require conducting lines to provide power or control signals, which in antenna applications can disturb the antenna properties. Thus, the elimination of these wires can be achieved by using an optical source of fibre optics to control the device. Early configurations used to tune a patch antenna involved optically illuminating a PIN diode connected between the patch and a short stub. When forward biased, both the patch and

the stub radiates, tuning the radiating area of the antenna. The direct light source is used to vary the impedance characteristics of the diode, but has the disadvantage of degrading the diode quality factor by varying the device resistance and capacitance. This simple technique was introduced in 1985 [45] and later patented [46].

A second technique involves the use of photoconductive silicon, where the silicon is directly illuminated [47]. Both GaAs and silicon are photoconductive materials that are commonly used for optical switches due to their low DC resistance when subject to an illuminated source, and a high DC resistance when the source is dark. The method to achieve a phase shift involves the introduction of plasma into the guiding medium [48]. That layer of the waveguide in which the plasma occupies, possesses an index of refraction greater than the remainder of the waveguide, perturbing the guiding structure. By optically illuminating the plasma layer with above-bandgap radiation, a phase shift may be detected by determining the propagation constant along the guide, and comparing it to the propagation constant determined in the absence of the plasma. Advantages of optical control include, fast response time, near perfect isolation and low insertion loss, and high power handling capability.

2.3.3 Ferrite Substrates

Research into the realm of ferrite substrates to aid in beam scanning has also emerged in recent years. Original research into this domain was motivated by a desire to utilize the higher dielectric constant of the ferrite to achieve reduced dimensions for patch antenna design at low frequencies through loading of the substrate. During the course of this research, it was discovered that ferrite substrates under the influence of a DC magnetic bias could be influential in aspects of polarization control and pattern shaping [49], tuning of the resonant frequency [50], and the reduction of the radar cross section [51], as well as beam steering [52]. A biased 3 cm long microstrip line was used to feed a simple four-element patch array in [52]. Significant changes in phase occurred for a correspondingly minor change in the bias field at 8 GHz. Little change in phase was recorded at the onset of the applied bias, with a beam scan of only 5° with an applied

field of 2000 Oe. However, beyond this threshold, the beam scan angle increased to 20° with only an increase of 100 Oe. A loss of 2 dB was obtained for a scan of 40°, with a substantial increase in loss above 2300 Oe. In this application, the array was printed directly on the ferrite substrate. A similar trend of large scan variation versus bias field is observed with measured and simulated data in [53] for a 4 × 1 microstrip patch array. The entire array structure was composed of 6 regions of varying permittivity, the ferrite region located beneath the patch element feed lines. The main beam is located at 19.2° for an applied field of 5020 Oe, and subsequently at –19.2°.

Alternative configurations have been recorded with the ferrite as an additional layer to the device substrate, or as a superstrate layer overtop the antenna. Bulk (mm thickness) and thin films (μm thickness) [49] have been explored for these purposes. Miniaturization of the magnetic device has not been addressed with these applications, thus research into the potential of ferrite substrates for beam steering has not grown quite as rapidly as the evolution of ferroelectric thin films. Ferrite films were investigated for use with planar microwave devices, but were found to be incompatible with the design dimensions of these structures.

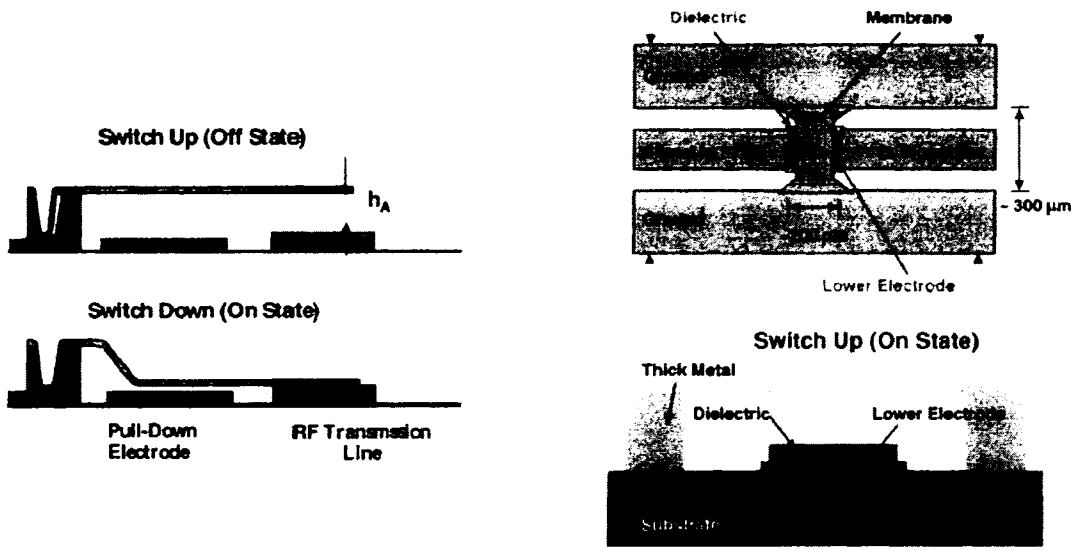
2.3.4 Low Temperature Cofired Ferrite Ceramic

An example of a new ferrite-filled rectangular waveguide phase shifter packaged within a low-temperature cofired ceramic is discussed in [54]. As discussed by the paper's authors, a decline in the popularity of ferrite phase shifters resulted due to the increasing implementation of planar-based technologies. A solution, according to the authors, is to integrate the ferrite at the package level, to render the ferrite dimensions more in-line with millimetre wavelengths. This phase shifter consists of a ferrite filled waveguide within an LTCC package based entirely of ferrite layers. Hughes developed LTCC in the early 1980s and its technology is originally based on thick-film materials [55], [56]. LTCC consists of a glass-ceramic composite that has been developed for firing temperatures below 1000°C. Typically high temperature cofired ceramics (HTCC) are fired at 1600°C and above, which restricts the use of high conductivity metallization

layers such as gold, silver, and copper whose melting points fall below the firing temperature. LTCC is thus compatible for use with these good conductor materials, which also ensure ease of soldering and wire bonding with the metallization layers. Typically, HTCC required the use of such metals as tungsten that possess low conductivity and higher losses than good conductors commonly desired and applied as the metallization layer. With a firing temperature below the melting points of good material conductors, low-loss metallizations are achieved in conjunction with a three-dimensional microwave interconnect substrate. In addition, while thick film technology requires repeated firing stages, LTCC necessitates only one firing step. An LTCC package offers a multilayer, hermetic and highly integrated architecture, incorporating buried microstrip, stripline, coplanar, or DC lines, thereby reducing necessary interconnections and increasing overall simplicity and reliability. Prototype measurements in [54] detail a phase shift of 52.8° at 36 GHz, with an insertion loss of 3.6 dB, for a bias current of 500 mA.

2.3.5 MEMS Phase Shifters

The most popular example of a MEMS phase shifter is the electrostatic actuator, a mechanical switch that necessitates an electrostatic force to complete the actuation process. Electrostatically controlled switches have been demonstrated for use over a wide frequency range, from 0.1 GHz to as high as 100 GHz, with high reliability [57]. The simplest designs consist of a basic cantilever beam or an air bridge, as shown in Figure 2.8, which are variations of a rigid parallel-plate capacitor. With the cantilever, one of the 4 sides of the top capacitor plate is anchored to form a beam. The air bridge in contrast to the cantilever is fixed at both ends, suspended over an electrical contact. When under the influence of an applied voltage, the air bridge and the unanchored side of the cantilever will deflect, eventually closing the switch when the necessary threshold voltage is achieved. Other common configurations include torsional actuators, which allow deflections in two directions, or comb-drive actuators that involve the actuation of interdigitated fingers.



(a) *(b)*

Figure 2.8: *(a) Cantilever, and (b) air bridge RF MEMS switch structures [3].*

A MEMS phase shifter has many application advantages for RF phase shifters [3], [57]-[59]:

- **Low insertion loss**: Typically a loss of 0.1 dB up to 40 GHz [57] exists during signal transmission in the ON state, which minimizes the dependency of the device on a power amplifier. High insertion losses, typical with solid-state phase shifters, necessitate additional power amplifiers for higher gain and power consumption.

- **High isolation**: Low signal leakage at the output in the OFF state. Thus, cross-talk effects are at a minimum, an attractive feature when comparing these devices to PIN diode phase shifters.

- **Low power dissipation**: Actuation of a MEMS switch requires very little power, since current consumption is negligible during the application of the electrostatic force.

- **Ultra small size and weight**: Issues of excessive weight to the phased array from the MEMS phaser, as well as the additional electronics, are non-existent and promote a low cost structure ideal for satellite communication systems.

- **Fabrication**: Processes are complimentary to existing IC fabrication techniques, resulting in ease of integration with existing RF technology. These include bulk and surface micromachining, fusion bonding, and LIGA, a process involving X-ray lithography, electrodeposition and molding.

- **Linearity**: No intermodulation occurs between differing frequencies, unlike PIN diodes that demonstrate non-linear device characteristics.

Mechanically, the actuator deflection is a function of the structural and material properties of the beam or bridge. More specifically, the deflection is a function of the moment of inertia of the beam and its Young's modulus, a constant of proportionality that relates a material's stress and strain. The Young's modulus is thus a measure of the material's stiffness; the higher the modulus, the stiffer the material and the less likely it is to bend. These devices still conform to the basic laws of mechanics and physics, but are extremely small, on the order of micrometers, with a mass of approximately 10^{-10} to 10^{-11} kg [57]. Because of their small physical parameters, acceleration/gravitational forces are negligible. There are thus multitudes of advantages with the application of a MEMS actuator within a phase shifter device. However, the disadvantages related to their use are largely due to the mechanical aspects of the device. These are:

- **Speed:** Its switching speed is slower in comparison to solid-state phase shifters, from 2-40 μsec, which may or may not be a concern depending on the intended application, e.g. in radar systems where switching speed affects the radar range. The limitation lies primarily in the release time of the switch, e.g. switching from the down to up state, and may be 10 times longer than its initial actuation, from the up to down position.

- **Long-term reliability:** MEMS device lifetime is a concern as its key components are subject to contact failure and stiction. However, they have been tested to failure, demonstrating switch lifetimes of 0.1 to 100 billion cycles [57]. As with switch speed, this may be a concern if the proposed system necessitates a greater number of cycles. They are, in general, satisfactory for wireless communication systems and most satellite communications systems implementing Butler matrices for reconfigurable antennas, or switching of multibeam satellite communication systems.

- **Packaging:** Success of a MEMS structure depends highly on the structural and electrical reliability of its delicate components. Successful packaging of a MEMS device is therefore critical to maintain its dependability. To ensure the device success, it is necessary to consider such factors as the device environment, handling, and EM coupling, discussed in following section.

2.3.5.1 Packaging

Packaging of a MEMS device is currently a popular area of research. However, while techniques developed by commercial institutions are not commonly divulged, current IC processing practices are all favourable techniques for patterning two-

dimensional MEMS layers. Three-dimensional components are generally achieved by stacking two-dimensional layers, etching selectively over a substrate, or by mechanically bending or securing a hinged structure [59]. Currently, it is possible to overcome environmental, handling and coupling issues, but at the expense of added financial burden. These issues include:

- **Environmental factors**: Humidity and surface contaminants around the switch promote *stiction*, a term that refers to the "sticking" of a component to adjacent elements or the circuit substrate [58]. For this reason, fabrication and packaging must be performed in a strict, low humidity environment and inert atmosphere to ensure the reliability of the device.

- **Handling:** To protect its small components during handling, a MEMS device is packaged first at the microscopic level (the device level), a process termed microriveting [60], using IC fabrication processes. It is a mechanical joining technique that allows two wafer pieces to be joined by rivets. Following this procedure, MEMS devices are thus protected and subsequent packaging on the IC wafer can be safely completed on a macroscopic level.

- **EM coupling:** It is necessary to electrically isolate MEMS components to protect them from the phenomena of electromagnetic coupling and moding, which contribute additional transmission line losses. Moding results from the resonant behaviour of the cavity that encloses the MEMS circuit. A technique termed self-packaging [61] integrates the cavity enclosing the circuit into the original design concept, rather than considering its addition during the packaging phase. Thus, the cavity is designed so that its resonant frequencies are well away from the operating frequency of the MEMS device.

2.3.5.2 Phase Shifters

MEMS switches, when incorporated within phase shifter circuits, usually replace a PIN diode or GaAs FET as the switching component. The phase shifter circuit architecture is otherwise the same. According to Rebeiz, Tan and Hayden [62], the reason for this is simply that these standard designs have been well documented. Their application with MEMS switches in place of diode or FET components is therefore straightforward, and results in satisfactory phase shifter performance.

A reflection-line phase shifter was fabricated on high resistivity silicon with a RF MEMS switch as detailed in [63] for X-band operation. A combination of two 2-bit reflection phase shifters using Lange couplers was combined to achieve a four-bit phase shifting device. Longer line sections of 45° electrical length were constructed to provide 90° phase shift by one of the 2-bit configurations, while shorter lines of 11.25° length provided the 22.5° increments. The overall circuit had a measured average insertion loss of 1.4 dB, with projected improvements set to achieve a projected insertion loss of 1.0 dB. Return loss greater than 11 dB was achieved at 8 GHz.

Switching through delay lines at Ka-band with shunt MEMS switches is reported in [64]. An average insertion loss of 2.25 dB over 337.5° is achieved for the four-bit phase shifter, close to the 2.2 dB predicted value at 34 GHz. A return loss of 15 dB is achieved over all phase states. A similar three-bit phase shifter was constructed achieving a return loss of 13 dB and an average insertion loss of 1.7 dB over 315°.

A novel approach to the use of MEMS switches in phase shifter design is the distributed MEMS transmission-line phase shifter (DMTL) [65]. A slow-wave structure was developed by periodically placing MEMS air bridge switches along a coplanar waveguide (CPW) transmission line, as shown in Figure 2.9. The line length, bridge size and periodic spacing of the switch are the parameters that control the propagation velocity of the wave down the line, and thus the phase change. A single analog control voltage is applied to the center of the CPW to actuate each air bridge, effectuating a true-time delay structure. The switch provides an additional design parameter in the form of a shunt capacitance with the transmission line structure that increases as the switch is deflected, decreasing the phase velocity of the transmission line. The achievable phase

change with 8, 16, and 32 air bridges having a width of 30 μm and a periodic spacing of 306 μm at 40 GHz is 12°, 36°, and 62°, with insertion losses of 0.5, 0.75, and 1.57 dB. The line impedance under zero bias conditions was 60Ω, and the switch control voltage was 21V. An increase in phase shift is recorded for 16, 60 μm wide air bridges spaced 400 μm apart, to a maximum of −74° with insertion loss of 1.4 dB at 40 GHz. Control voltage in this case was a mere 6V, with a line impedance of 43Ω at zero bias. Increasing the periodic spacing of the identical air bridges to 580 μm achieved a maximum phase shift of −82°, but was achieved with a control voltage of 23V.

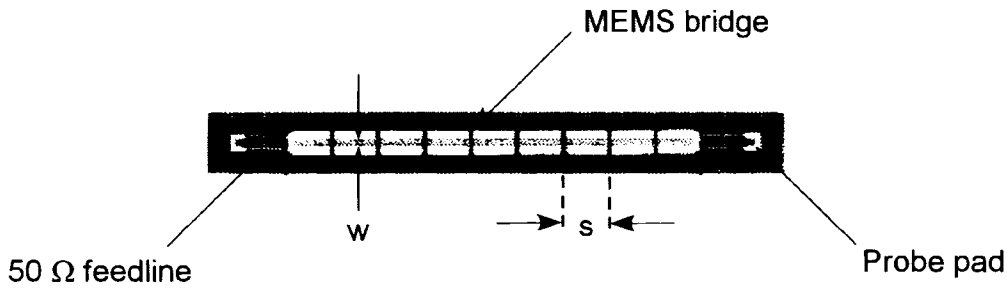


Figure 2.9: *DMTL phase shifter with MEMS bridges of width w, and spacing s, terminated by a 50Ω feedline and probe pads for testing [65].*

In a more recent publication by the same authors [23], DMTL phase shifters were designed for use at V-band (50-75 GHz) and W-band (75-110 GHz). Figures of merit of 70°/dB and 90°/dB were obtained at 40 GHz and 60 GHz, respectively, and 70°/dB over 75 GHz to 110 GHz, with less than 20% change in MEMS bridge capacitance. It was stated that the phase shifter performance could be greatly increased with a 30% to 50% increase in the bridge capacitance.

A similar design using two parallel-connected varactor diodes in place of the MEMS devices was investigated in [66], resulting in a continuous phase shifter. At 20 GHz, insertion loss of 4.2 dB over 360° phase shift (86°/dB) was achieved by 24 series connected cells (each cell defined by the spacing between diodes) for a total line length of 19.44 mm. While switching speed is increased with this design, the loss at frequencies of 40 GHz to 60 GHz, explored by its MEMS counterpart in [23], would be greater.

CHAPTER 3

TRANSMISSION LINE DEFECTED GROUND STRUCTURES

In this chapter, the phase scanning potential of a single slot defect element in the ground plane of a transmission line is investigated. A parametric study was performed, beginning with an examination of the influence of the slot width, length, and orientation on the defected transmission line phase performance, as well as the return loss and transmission loss of the structure. The scalability of these structures is also discussed with respect to the material permittivity and substrate thickness. The significance of the transmission line width and thus the line impedance on single and paired elements is presented, with some discussion on the associated performance of these configurations, with regards to their phase shift figures of merit. Results presented in this chapter were achieved through simulations using Ansoft's method of moments based software package Ensemble 8.0.

3.1 Microstrip

Microstrip is a popular lightweight medium for use within antenna and microwave circuit design due primarily for its low-profile, low cost, and relative ease of fabrication using established photolithography techniques [22]. The lightweight and conformal characteristics of microstrip render it an ideal medium to comply with the structural design requirements of costly satellite and aircraft applications. The geometry of a microstrip circuit consists of a dielectric material sandwiched by two metallization layers, the top conductor involved as the circuit trace, and the bottom conductor serving as the circuit ground plane, as shown in Figure 3.1 for a simple microstrip transmission line. The circuit metallization layer is commonly realized by the deposition of metal on a bare substrate, or by the removal of conductor using an etching process. The open-air

architecture of the microstrip conductor lends itself for use with microwave integrated circuits where lumped components can be easily mounted on a circuit substrate. Design adjustments are also possible following fabrication, as the microstrip structure is easily accessible, in contrast to a medium such as stripline where the conductor is embedded within a homogeneous dielectric medium.

Because a microstrip transmission line is bounded on one side by the dielectric and by air on the other, fields are supported in both the dielectric and free space. The microstrip medium is not homogenous, and thus does not support TEM propagation. For most practical purposes, a microstrip line is considered to support quasi-TEM fields, as the substrate thickness is considered negligible with respect to wavelength. Under this assumption, an effective dielectric constant is used to quantify the permittivity of the structure, and is expressed as a function of the strip conductor width w, and the substrate thickness h, as follows:

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1 + \frac{12h}{W}\right)^{1/2} \tag{3.1}$$

with ε_{eff} having a magnitude between the relative permittivity of free space and that of the substrate dielectric ε_r ,

$$i.e.\ \ 1 < \varepsilon_{eff} < \varepsilon_r$$

The propagation constant and phase velocity of the medium are expressed in terms of ε_{eff} as follows:

$$v_p = \frac{c}{\sqrt{\varepsilon_{eff}}} \tag{3.2}$$

$$\beta = \frac{\omega}{c}\sqrt{\varepsilon_{eff}} \tag{3.3}$$

The width of a microstrip transmission line is usually very small with respect to wavelength, and is used to characterize the transmission line characteristic impedance Z_o, for a particular substrate thickness and relative permittivity.

The substrate itself is a necessary component of the microstrip structure, providing mechanical support for the two conductive layers of the medium. However,

while it satisfies not only the mechanical needs of a microstrip circuit, it also influences the electrical characteristics of the structure. With regards to the choice of a particular substrate, there is no specific standard, rather selection is dependent upon a particular application and its design objectives. Four main material categories exist for substrate selection, and include [67]: inorganics (ceramics), plastics (e.g. Teflon) with ε_r around 2-3, semiconductors such as gallium arsenide or silicon (ε_r = 13.1, and 12, respectively), and ferrimagnetic materials such as yitrium-iron garnet (ε_r =9-16) employed in the design of non-reciprocal devices. For the specific case of microstrip patch antennas, low permittivity and thicker substrates are generally chosen for their higher radiation efficiency and bandwidth, but at the expense of larger element sizes. Higher permittivity (GaAs or Si) and thinner substrates are selected for microwave circuit applications to minimize radiation and achieve smaller dimensions. It is the relative permittivity of the material that is the main contributing factor to the miniaturization of the circuit.

The accuracy of the permittivity of the substrate and the thickness of the material are factors that can affect the operating frequency of a microstrip device. Of the two material parameters, the relative permittivity is generally considered to be the most sensitive as its overall accuracy is more difficult to guarantee. However, together with the material thickness, they are considered fundamental in their influence over the propagation constant, velocity, resonant antenna frequency, as well as the characteristic impedance of a microstrip structure. As a result of mechanical and chemical tolerances at play during the preparation of the substrate, ensuring the uniformity of the permittivity over the entire material, and the reproducibility of the thickness with each fabrication batch can become a costly requirement. Long-term environmental effects on the antenna substrate, such as weather exposure (moisture, temperature extremes), and the environmental effects unique to space (e.g radiation), can alter the substrate properties. Mechanical strength can also impair performance, but can be improved by reinforcing a substrate material by glass fibres or ceramic powders at the expense of loss and anisotropy, i.e. dependence of the material permittivity on the applied electric field orientation [67], [68].

While the photolithographic manufacturing process of the actual microstrip circuit is relatively inexpensive, the cost of a substrate material capable of satisfying and

maintaining the necessary electrical and mechanical requirements of a particular design over the long term can be prohibitively high for commercial applications. The cost of a microstrip antenna is directly related to the cost of its substrate and becomes increasingly relevant if the antenna is designed for mass-production. Therefore, while advances in substrate technology are slowly improving, in practice it is not uncommon with microstrip technology for an objectionable S_{11} to be considered at a level that is greater than a threshold of −10 dB. This limit may seem pessimistic in comparison to other technologies, such as reflector applications that can ensure greater manufacturing precision, but the low-profile, low-cost manufacturing, and compatibility of the medium with microwave circuits outweighs any manufacturing limitations. While a trade-off exists between cost and substrate performance, higher losses and variable levels of permittivity uniformity are acceptably tolerated by most applications.

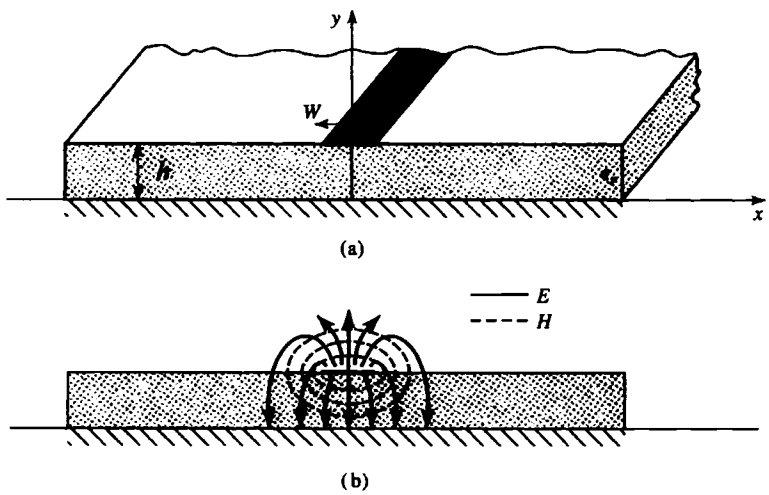


Figure 3.1: *Microstrip transmission line geometry; (a) geometry, and (b) electric and magnetic field lines [22].*

3.2 Ground Plane Defects

Ground plane defects in the form of slits in circuit boards have been investigated to better understand their effects on signal integrity and circuit line coupling [69], [70]. These slits have been introduced when separating the ground plane of multiple circuits to accommodate the increased density of printed circuit boards. Researchers Ahn *et al.* have recently published a series of letters and papers regarding their design and numerous implementations of a defected ground structure, the first of these appearing in April 2000 [71]. In each of these implementations, most commonly the unit cell applied to the periodic structure involved some sort of variation or mutation of a "dumbbell" like structure placed in the ground plane beneath a microstrip line. The characteristic of an increased effective inductance unique to their defect has been employed for the improvement of the chosen circuit structure. This structure is an evolution of the uniplanar compact PBG structure proposed by Itoh *et al.* [72], and has evolved from the philosophy that the unit defect cell provides a frequency stopband due to an increase in the effective inductance.

The equivalent circuit of the microstrip line defect has been compared to a parallel *LC* circuit, which is recognizable as a low-pass filter. The single defect element by itself produces an additional reactive component to the transmission line structure, by creating impedance discontinuities in removing portions of the ground plane [73]. This in turn produces a disruption in the current distribution in the ground plane of the microstrip line [74], [75]. Thus, the current on the ground plane below the line is forced to travel around the defect, which increases the current path, causing a delay and an associated phase shift. Additional filtering can be achieved by placing multiple elements beneath the microstrip line.

The defected ground structures investigated by Ahn, *et al.* were applied for use within a Wilkinson power divider for the implementation of unequal power division [76], and in the performance enhancement of a 10 dB, 90° branch line coupler [77]. The structure was also implemented to improve the design of a low-pass filter [73], and increase the stopband performance of a coupled-line bandpass filter [74]. The application of their defect was implemented within active circuit design to achieve a size-reduction

of over 50% for an amplifier circuit by adopting their unit cell within the matching network [78], as well as an improved power added efficiency of 1-5% for an amplifier circuit [79] with the defect placed at the amplifier output, and phase noise reduction of 10-15 dB for a microwave oscillator [80].

A vertically periodic defected ground structure (VPDGS), consisting of defects vertically cascaded beneath a transmission line, demonstrated a much higher slow-wave factor than a similar structures horizontally configured for a similar transmission line [81]. This architectural variation was adopted within the matching circuit of an amplifier to achieve a size reduction of 38.5% and 44.4% on the original lengths of two series microstrip lines located at the input and output matching circuits of the amplifier [82]. These improvements were all calculated in comparison to identical designs implemented with conventional microstrip lines.

Variations on the defect design have occurred, including a spiral shaped cell [83], [84], or fractal structures [85] as the ground plane defect. These structural variations nonetheless preserve the dumbbell shape, or the perimeter, of the unit cell. The conclusion that the resonant characteristics of the defect are defined by the structural perimeter of the defect and not its area was stated in [86], following a parametric study of similar but slightly different etched structures beneath a transmission line. While these defected structures have been extensively explored for use in conjunction with a variety of microwave circuits in the listed references [71]-[76], and their benefits acknowledged, the emphasis of these designs is placed on filter performance, specifically for the improvement of device performance and not on phase shifter design.

3.3 Single Defected Ground Structure

A study conducted in [69] for the model of a slit on the ground plane, focused on establishing a methodology to easily evaluate the effects of slits used to separate circuit boards sharing a common ground plane. It was stated by the authors that this defect caused a delay in the current flow, and consequently a delay in the insertion phase. Thus, as a starting point for examination, a simple two-dimensional slot was selected as the initial structure of interest, as shown in Figure 3.2.

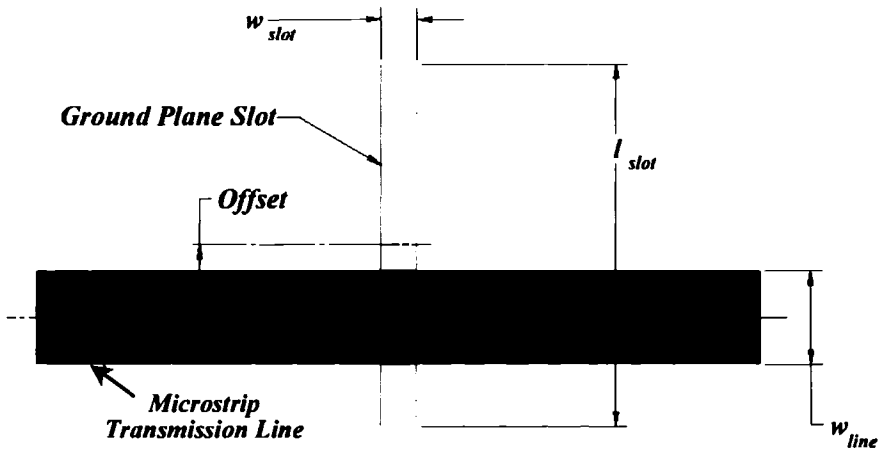


Figure 3.2: *Ground plane slot loaded transmission line.*

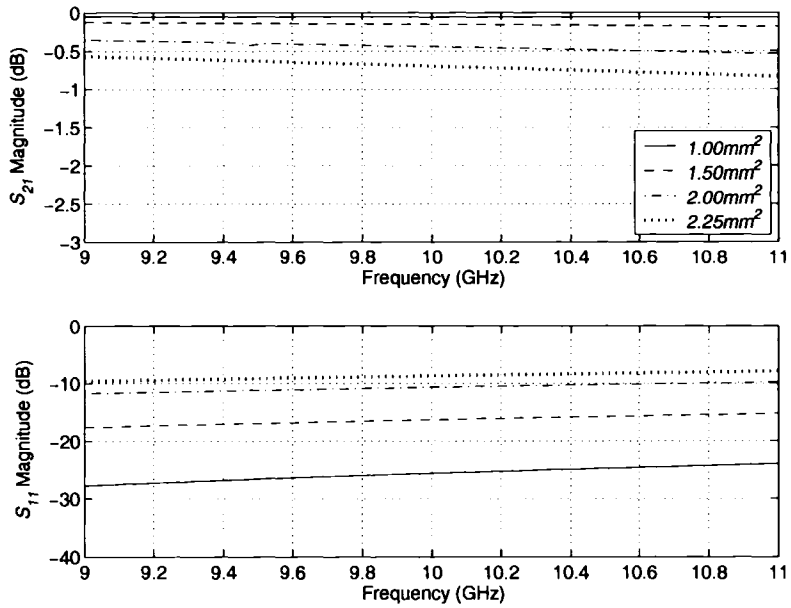
A single defected ground structure, was placed in the ground plane beneath a transmission line [87], [88], where w_{slot} and l_{slot} represent the width and length, respectively of the defect. Initial studies were attempted with a slot offset of 0 mm. The transmission line strip was placed on a substrate of permittivity ε_r = 3, loss tangent of $\tan\delta$ = 0.0013, and thickness of h = 20 mil. The line width corresponds to a characteristic impedance of 50Ω (1.279 mm), and had an arbitrary length of $\lambda_g/2$, at 10 GHz. These material parameters were imposed for purely practical purposes, motivated by the available fabrication materials at the time of study.

Because it is desired to apply this structure for use with an antenna, it is necessary that the phase scanning be operable in the passband of the structure. An upper limit of –10 dB was therefore selected as an acceptable S_{11}, for a design at 10 GHz. Design at this frequency results in physical dimensions conveniently fabricated by available etching processes, and falling within the frequency range of existing laboratory equipment. Slot dimensions are also limited to magnitudes less than $\lambda_g/2$ to avoid radiation. The differential insertion phase, $\Delta\phi_{21}$, of the structure was determined by comparing the insertion phase of an identical but unloaded transmission line, with that loaded with the defect ground structure.

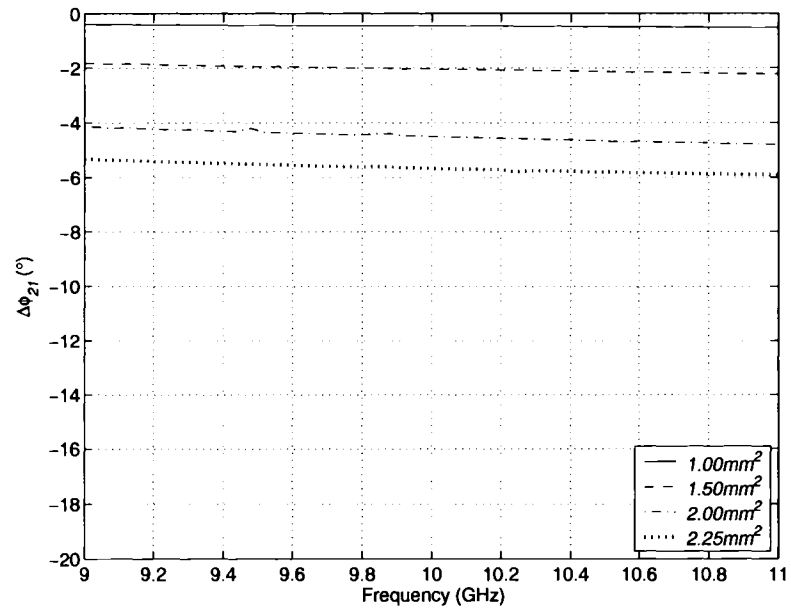
3.3.1 Defect Dimensions

Initial studies considered a simple square structure centred beneath a transmission line, with $w_{slot} = l_{slot}$. With the upper limit of 10 dB for an acceptable return loss, a differential insertion phase of between 4.50° and 5.66° was achieved for defects having a square area of 2.0 mm^2 and 2.25 mm^2, respectively. Greater differential insertion phase was achievable for larger square areas, but resulted in an S_{11} above the desired threshold of -10 dB. The S_{11}, S_{21}, and $\Delta\phi_{21}$, for the square defect are shown in Figure 3.3.

The observed results for the square geometry suggest that maintaining a constant 1:1 ratio between the defect dimensions may not be the optimum design with regards to phase. The length and width of the structure offer two degrees of freedom within the design, and thus their respective influences were explored. The influence of the slot length on the achievable insertion phase was examined, while the width dimension remained fixed. The results of four experiments are shown in Figures 3.4 to 3.7, for slot widths of w_{slot} = 0.25, 0.5, 1.0, and 2.0 mm, with the S_{11} and S_{21} magnitude for each respective case shown in part (a) and the differential insertion phase detailed in part (b) of each figure.

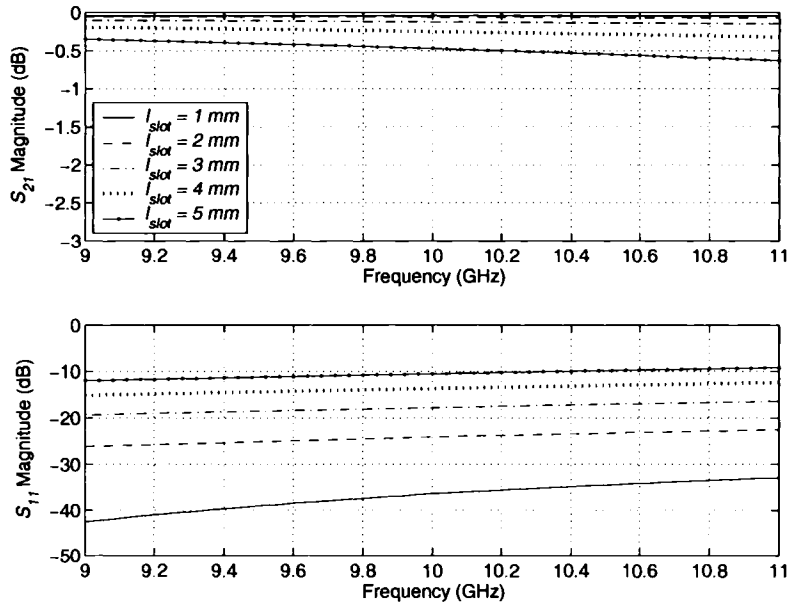


(a)



(b)

***Figure 3.3**: S-parameters and differential insertion phases of a 50Ω transmission line with a square defect of $w_{slot} = l_{slot}$; (a) S_{21}, S_{11}, and (b) $\Delta\phi_{21}$ with respect to frequency.*



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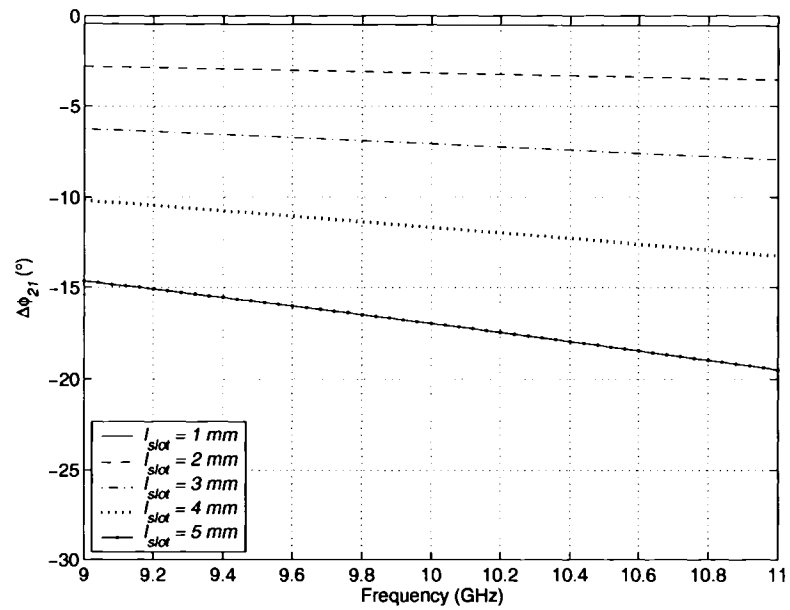
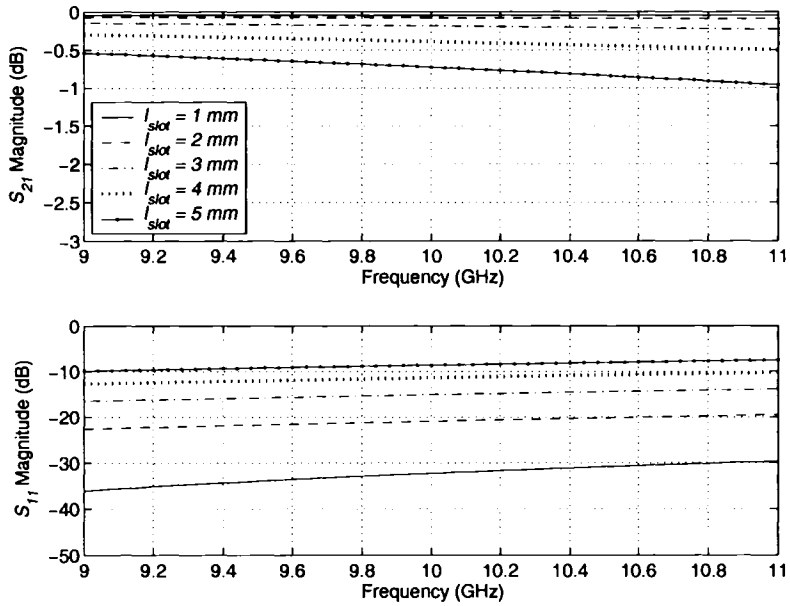
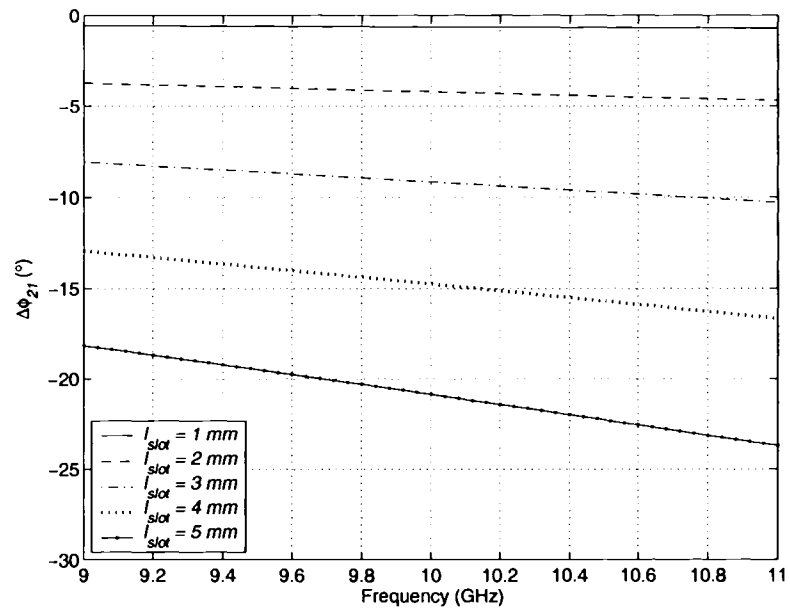


(b)

***Figure 3.4**: S-parameters and differential insertion phases of a 50Ω transmission line with a rectangular defect of w_{slot} = 0.25 mm, and l_{slot} as indicated; (a) S_{21}, S_{11}, and (b) $\Delta\phi_{21}$ with respect to frequency.*

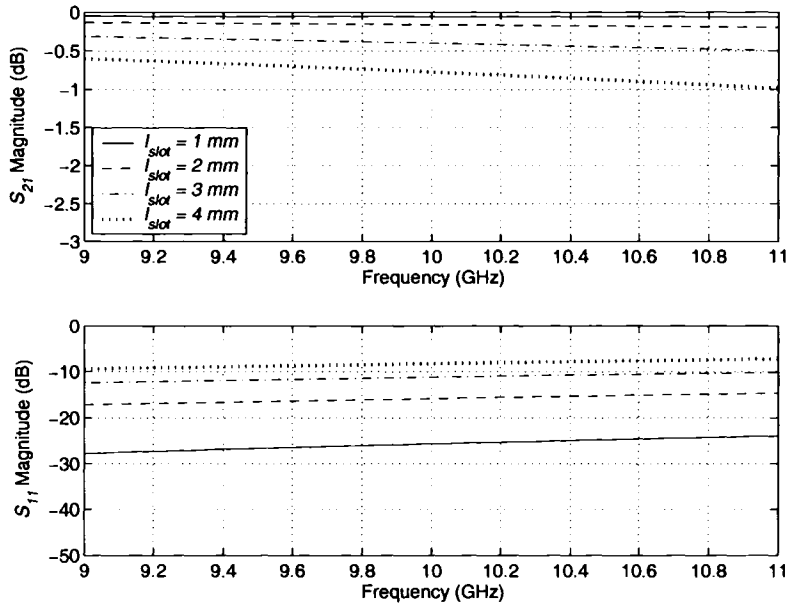


(a)

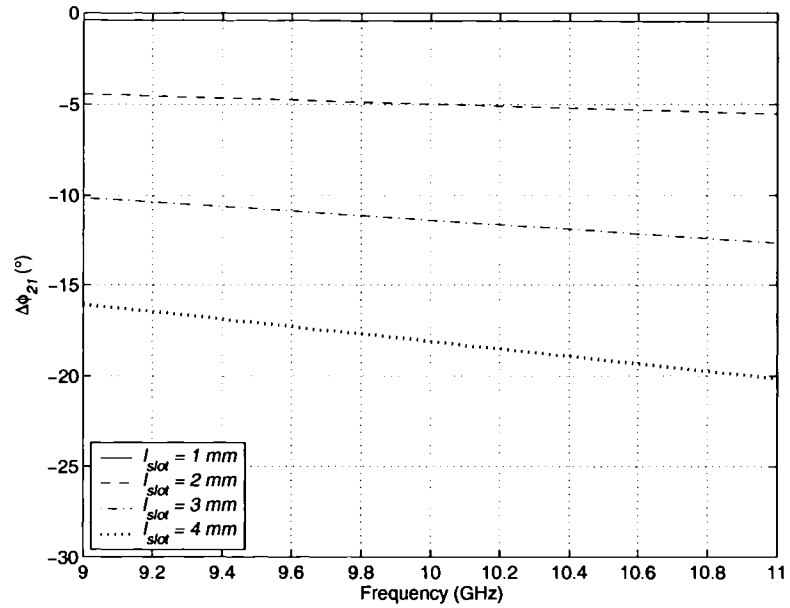


(b)

***Figure 3.5**: S-parameters and differential insertion phases of a 50Ω transmission line with a rectangular defect of w_{slot} = 0.5 mm, and l_{slot} as indicated; (a) S_{21}, S_{11}, and (b) $\Delta\phi_{21}$ with respect to frequency.*

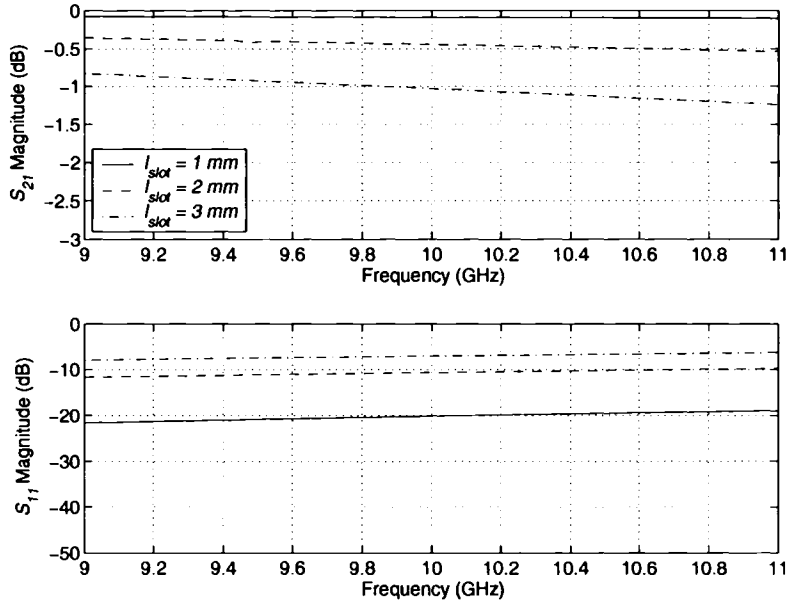


(a)

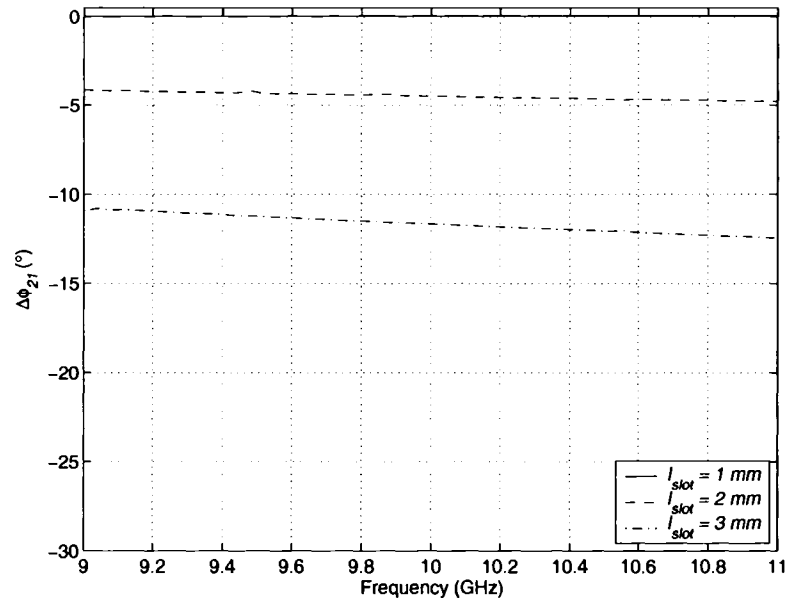


(b)

Figure 3.6: *S-parameters and differential insertion phases of a 50Ω transmission line with a rectangular defect of w_{slot} = 1.0 mm, and l_{slot} as indicated; (a) S_{21}, S_{11}, and (b) $\Delta\phi_{21}$ with respect to frequency.*



(a)



(b)

***Figure 3.7**: S-parameters and differential insertion phases of a 50Ω transmission line with a rectangular defect of w_{slot} = 2.0 mm, and l_{slot} as indicated; (a) S_{21}, S_{11}, and (b) $\Delta\phi_{21}$ with respect to frequency.*

The *S*-parameter data in Figures 3.4 to 3.7 demonstrates that, with an increase in the slot length for a constant slot width, an increase occurs in the reflection at the input port of the structure. Also, the differential insertion phase increased in magnitude as the slot length was made longer. These results are summarised in Table 3.1.

Table 3.1: *Simulated results for l_{slot}, and $\Delta\phi_{21}$, at $S_{11} = -10$ dB for select w_{slot} at 10 GHz, for a single defect below a 50Ω transmission line.*

Slot width w_{slot} (mm)	*Slot length l_{slot} (mm)*	$\lvert\Delta\phi_{21}\rvert$ (°)
0.25	5.2021	18.2181
0.50	4.4578	17.4836
0.75	3.8499	15.7826
1.00	3.3628	13.8143
2.00	2.1780	5.7731
3.00	1.8493	2.1033
4.00	1.6679	0.9462

A greater phase change is achieved for narrower slots, from less than 1° for the widest slot to over 18° for w_{slot} of 0.25 mm. For increased slot width, the possible achievable phase while maintaining a limit of −10 dB in the return loss gradually decreases. Thus, a narrower slot has performance benefits over one that is wider. However, the length of the slot is equally critical, achieving the phase results listed in Table 3.1 with longer lengths as the width is decreased. Regardless of whether the slot width is slim or fat, a rise in the differential phase as its length was increased still occurs. The width influenced the rate with which the differential phase grew with increasing perforation length. Increasing the slot width had little benefit on the return loss or the insertion phase. With shorter and wider defects, the larger dimension of the slot lies parallel to the transmission line and does not create a significant disturbance in the current path.

For coming experiments in this chapter, a slot was selected with dimensions of l_{slot} = 4.5 mm and w_{slot} = 0.5 mm, achieving a $|\Delta\phi_{21}|$ of 17.7°. While a narrower slot demonstrated a slightly higher potential $|\Delta\phi_{21}|$ of just over 18°, at the time of selection, the dimensions of the selected slot were deemed the most convenient for fabrication purposes.

3.3.2 Angled Slot

The slot was gradually rotated beneath the transmission line, positioned at an orientation of θ_a = 0° to 90° beneath the transmission line, with θ_a as indicated in Figure 3.8. As shown in Figure 3.9 (b), the greatest differential insertion phase occurs for a slot that is normal to the line, while a slot co-linear to the line illustrates essentially no change in phase. This is in agreement with the data in Table 3.1 pertaining to slots possessing a large w_{slot} in comparison to the l_{slot} dimension. The S_{11} and S_{21} magnitudes, shown in Figure 3.9 (a), for a slot orientation close to 0°, resemble that of a well-matched transmission line. A slot placed in the ground plane, normal to the transmission line in question, caused a greater disruption in the path length of the current with a "head-on" obstruction, rather than one that may have its dominant dimension parallel to the directional path of the current.

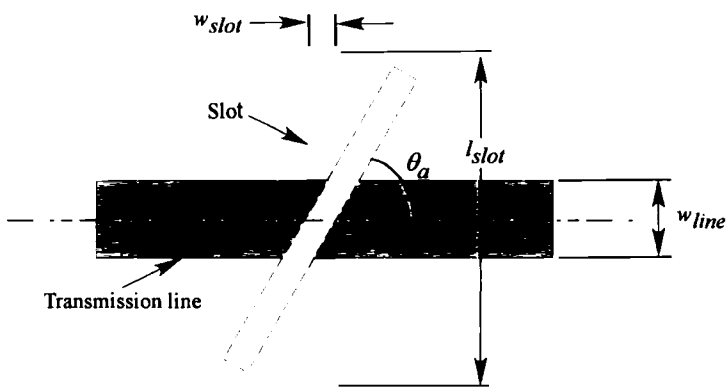
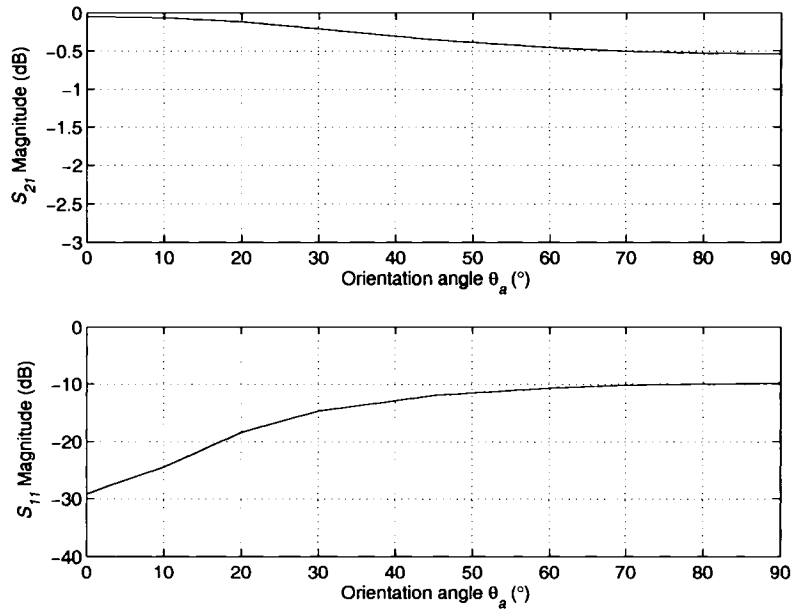
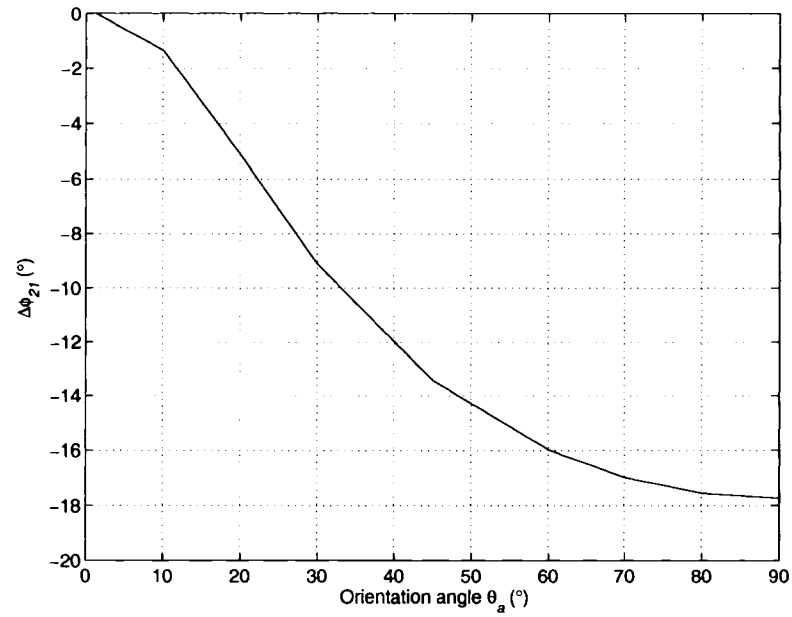


Figure 3.8: *Angled slot configuration.*



(a)



(b)

Figure 3.9: *S-parameters and differential insertion phase of a 50Ω transmission line with an angled defect slot of w_{slot} = 0.5 mm, and l_{slot} = 4.5 mm; (a) S_{21}, S_{11}, and (b) $\Delta\phi_{21}$ with respect to the orientation angle θ_a.*

A long, narrow slot placed transverse to the line provides the greatest insertion phase with respect to a wider, collinear slot. This trend is visually illustrated in Figure 3.10 for the seven optimised slots in Table 3.1. The vertical colour bar associates each slot with their optimum achievable phase for an S_{11} of –10 dB at 10 GHz.

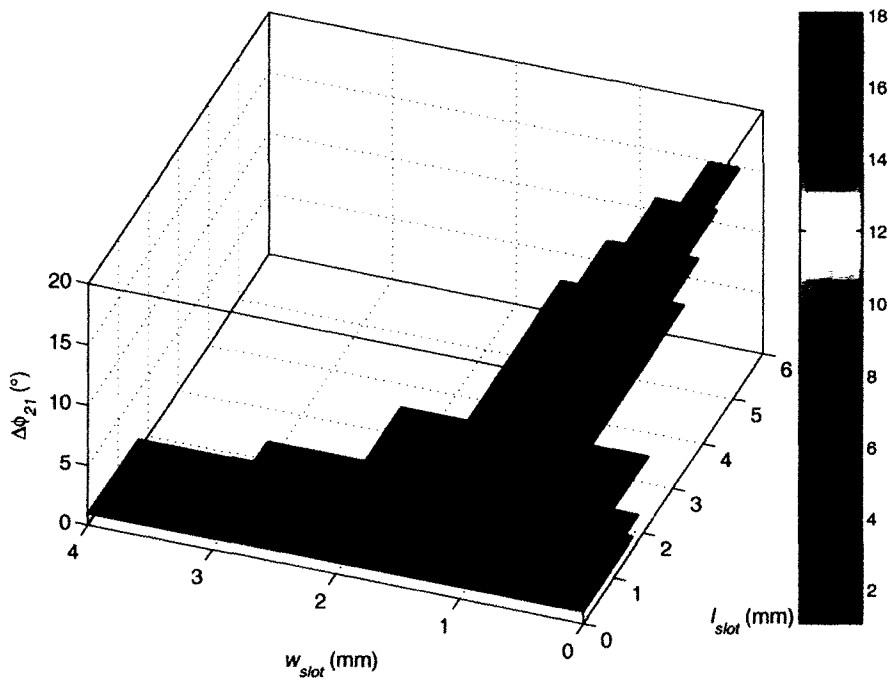


Figure 3.10: *Optimum $\Delta\phi_{21}$ for a single slot for w_{slot} and l_{slot}.*

3.3.3 Relative Permittivity

It is a known property of microstrip circuits that when all other parameters are kept equal, the size of a circuit is proportional to $1/(\varepsilon_{eff})^{1/2}$. The effective dielectric constant is established knowing the line width and the substrate height of the microstrip transmission line structure. When these parameters are unknown, the substrate relative dielectric constant can be used, as a first order approximation, to determine the line width and the substrate height. These results can be used to determine the effective permittivity and thus new and more accurate line parameters. As a means to confirm this statement with respect to the scalability of the defect dimensions, the candidate rectangular slot structure (w_{slot} = 0.5 mm, l_{slot} = 4.5 mm) having an ε_r = 3, was redesigned for a substrate with a relative dielectric constant of 10.2. Maintaining the design frequency at f = 10 GHz, the defect structure, as a first order of approximation, was scaled accordingly by the dielectric wavelength,

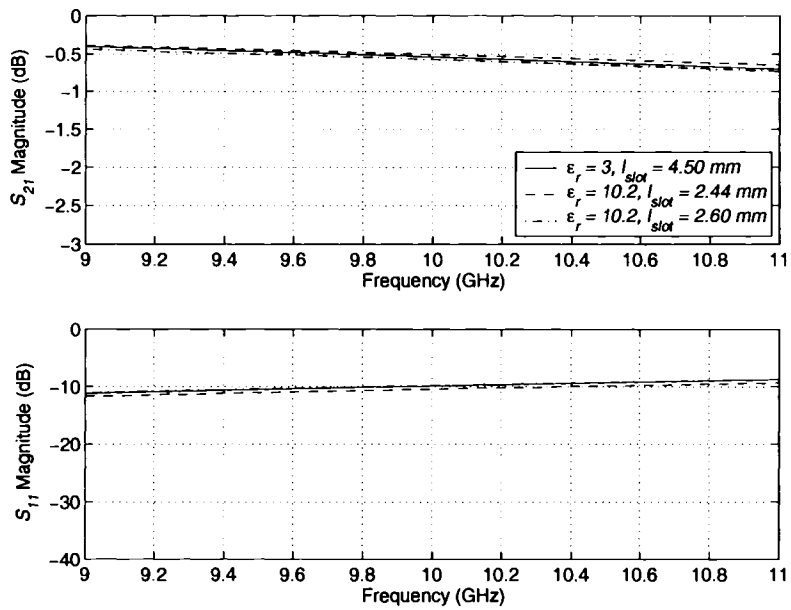
$$\lambda_d = \frac{c}{f\sqrt{\varepsilon_r}} \tag{3.4}$$

The scaled circuit parameters are listed in Table 3.2. With these slot and corresponding line and substrate parameters, the associated S_{11}, S_{21} and $\Delta\phi_{21}$ are provided in Figure 3.11, over a frequency range from 9 to 11 GHz. Scaling the line width and substrate thickness by λ_d resulted in a change in the characteristic impedance of the original transmission line. For ε_r = 10.2, the scaled line possesses a Z_o of 28Ω, and thus miniaturization of the slot structure occurs with the transfer of the circuit to a higher permittivity material. The influence of line impedance with respect to slot miniaturization will be discussed further in 3.3.5.

Note that scaling the slot length further, using the effective permittivity, provides a length of 2.6 mm, in lieu of 2.44 mm. The dimensions listed in Table 3.2, for the defect associated with the ε_r = 10.2 substrate, were applied to (3.1) to determine an effective permittivity of 7.52. The results in Figure 3.11 show clearly that a slot length of 2.6 mm provides differential phase that agrees very closely with the candidate rectangular slot designed with a relative permittivity of 3.

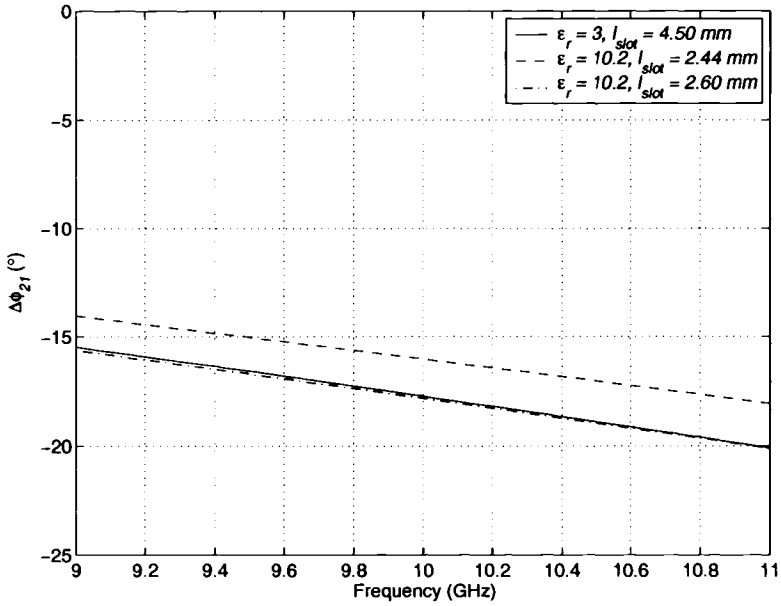
Table 3.2: *Scaled slot and substrate parameters for $\varepsilon_r = 3$ and $\varepsilon_r = 10.2$, in units of mm and λ_d.*

Defect parameters	*Dimensions in mm for $\varepsilon_r = 3$*	*Dimensions in mm for $\varepsilon_r = 10.2$*	*Dimensions in units of λ_d*
λ_d	17.321	9.393	1
h	0.508	0.276	0.0293
w_{line}	1.279 (Z_o = 50Ω)	0.694 (Z_o = 28Ω)	0.0738
l_{line}	10.00	5.423	0.5773
w_{slot}	0.500	0.271	0.0289
l_{slot}	4.500	2.440	0.2598



(a)

Figure 3.11: *Comparison of S-parameters and differential insertion phases for two lines having relative permittivities of $\varepsilon_r = 3$ and $\varepsilon_r = 10.2$; (a) S_{21}, S_{11}, and (b) $\Delta\phi_{21}$ with respect to frequency for $w_{slot} = 0.0289\lambda_d$ and l_{slot} as indicated.*



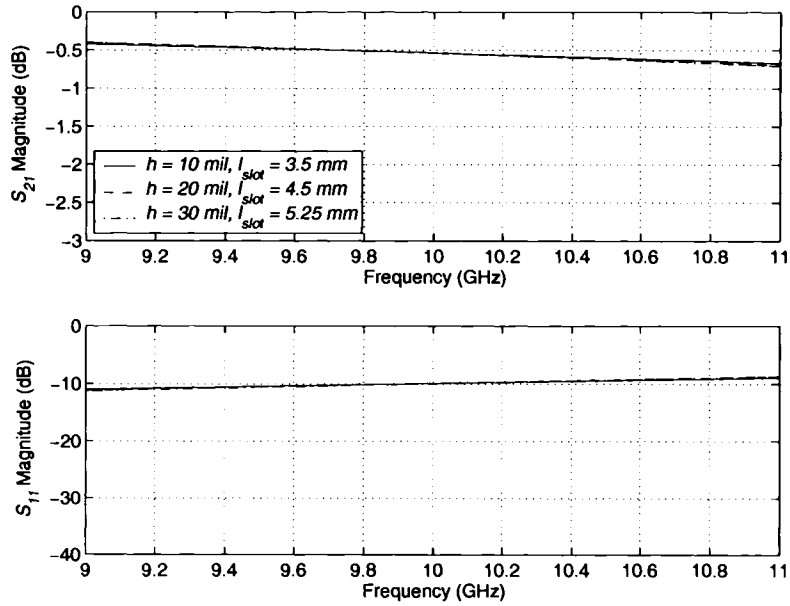
(b)

***Figure 3.11** continued*

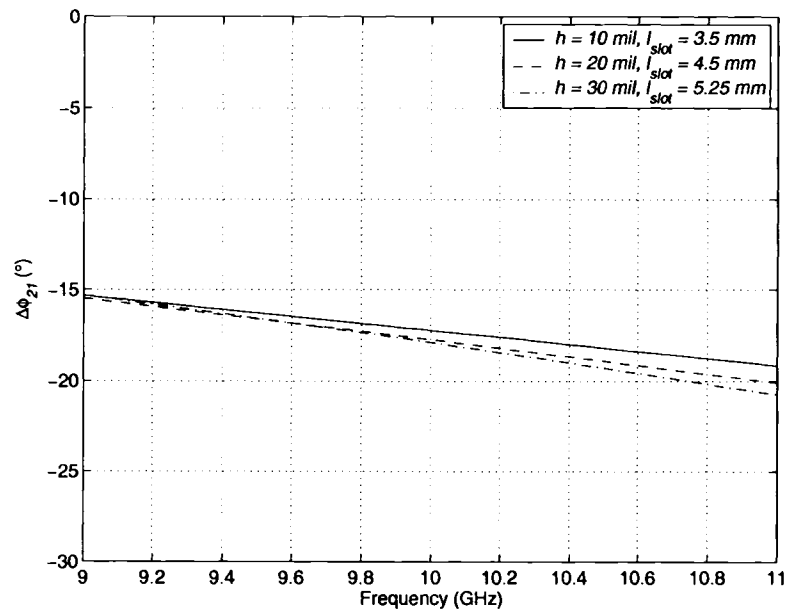
3.3.4 Substrate Thickness

The thickness of the substrate has an effect on the length of the slot implemented in the transmission line ground plane. As the substrate material is made thinner, the necessary length of the slot can be lessened to achieve a similar phase result in reference to a thicker material. Knowledge of this consequence is addressed further in Chapter 6.

Corresponding transmission lines having widths of 0.64 mm, 1.28 mm, and 1.92 mm were applied to h = 10 mil, 20 mil, and 30 mil substrates to maintain a Z_o of 50Ω. Substrate permittivity and slot width were unchanged, at ε_r = 3, and w_{slot} = 0.5 mm, respectively. The resulting S_{11}, S_{21}, and $\Delta\phi_{21}$ are shown in Figure 3.12. To achieve a similar phase result with frequency, the slot length was found by simulation to be 3.5 mm, 4.5 mm, and 5.25 mm, for h = 10 mil, 20 mil, and 30 mil, respectively.



(a)



(b)

Figure 3.12: *S-parameters and differential insertion phases for substrate thicknesses of h = 10 mil, 20 mil, and 30 mil; (a) S_{21}, S_{11}, and (b) $\Delta\phi_{21}$ with respect to frequency, for w_{slot} = 0.5 mm and l_{slot} as indicated.*

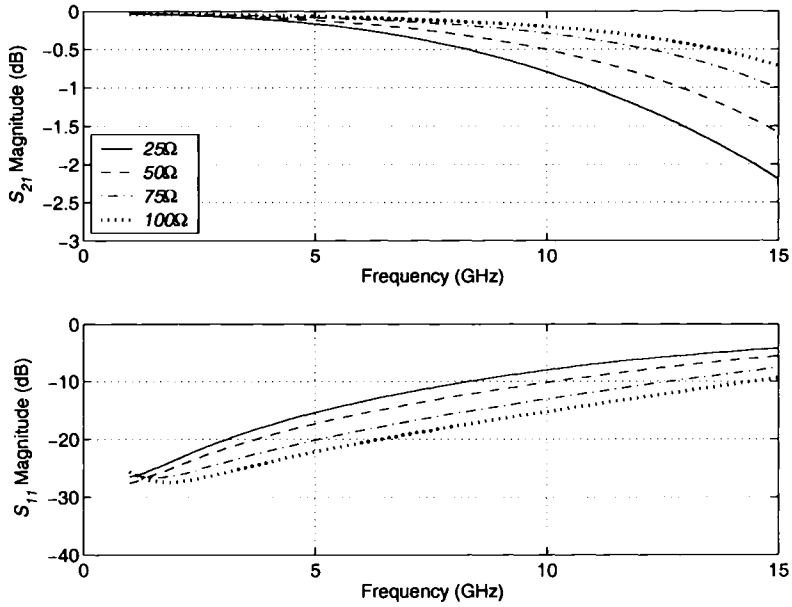
3.3.5 Line Impedance

The parametric studies concerning the slot width, length and orientation were applied to a transmission line designed for a 50Ω system. In the case of a system design of different impedance, the predicted phase in the case of 25Ω, 75Ω, and 100Ω lines was determined in order to establish if an advantage exists in selecting impedances that differ from the 50Ω convention. Identical slot dimensions were used for the line impedances, with the substrate parameters held constant. The candidate slot having w_{slot} = 0.5 mm and l_{slot} = 4.5 mm was placed at a 90° orientation beneath each line. The line widths were 3.329 mm, 0.635 mm, 0.341 mm, for the 25Ω, 75Ω, and 100Ω lines, respectively. The return loss and insertion losses are detailed in Figure 3.13 (a) for each system impedance, with their respective differential insertion phase given in Figure 3.13 (b) over frequencies from 1 GHz to 15 GHz.

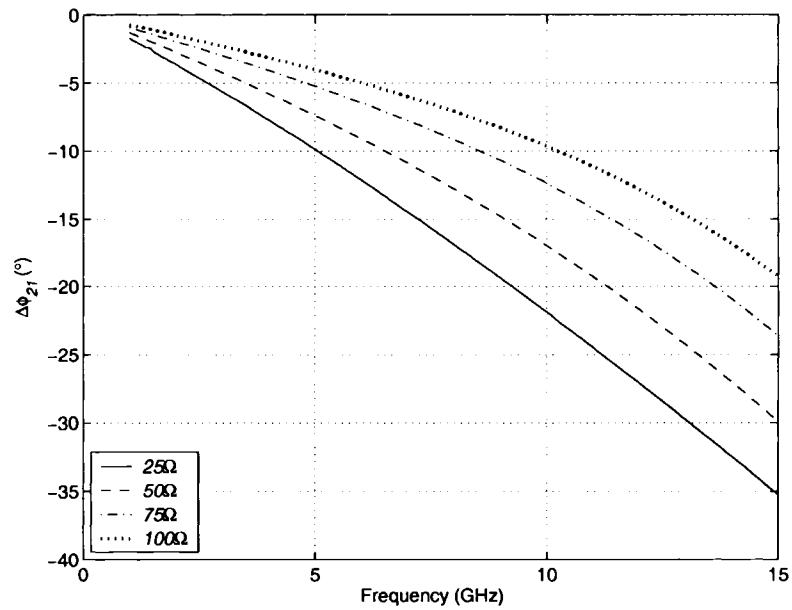
Recall that the differential insertion phase for the candidate slot was 17.7° when placed beneath a 50Ω line. The 50Ω slot structure was designed for optimum phase and maximum allowable return loss at 10 GHz, yet the results at this frequency for the 25Ω, 75Ω, and 100Ω systems appear less satisfactory. For an impedance above 50Ω, the match is improved, but the phase level is reduced (e.g. 9.6° for the 100Ω line). With an impedance below 50Ω, the phase level is increased (e.g. 22° for the 25Ω line), but at the expense of the S_{11}. In spite of this, when comparing the achievable phase levels of each system, it is interesting to note that at the return loss threshold of 10 dB, a differential insertion phase in and around a magnitude of 17.7° was observed for each of the 25Ω, 75Ω and 100Ω, but at frequencies other than 10 GHz. Thus, two comparison states are of interest:

- The return loss and phase levels at the design frequency of 10 GHz
- The frequency and phase levels at the return loss threshold

Table 3.3 summarizes the properties for each impedance instance for these two scenarios.



(a)



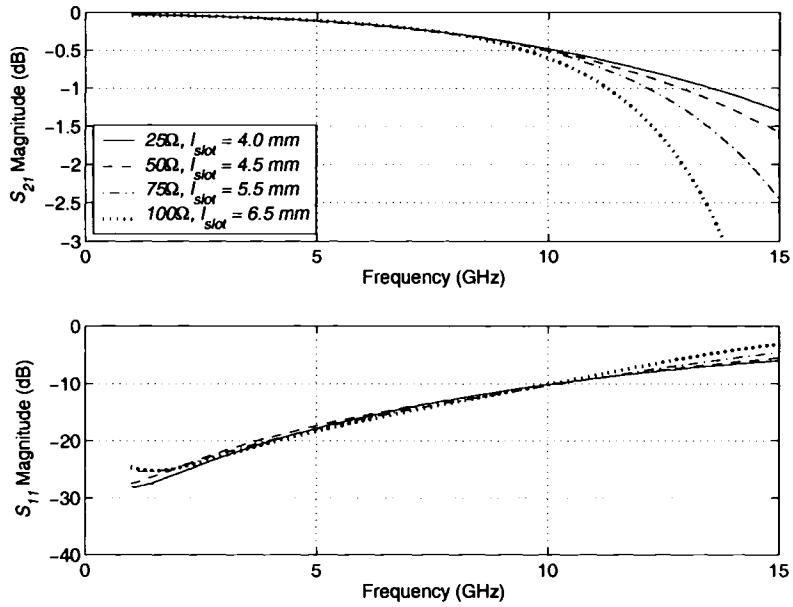
(b)

Figure 3.13: *S-parameters and differential insertion phases of a transmission line with line impedances of 25Ω, 50Ω, 75Ω, and 100Ω, over a defect with w_{slot} = 0.5 mm, and l_{slot} = 4.5 mm (a) S_{21}, S_{11}, and (b) $\Delta\phi_{21}$ with respect to frequency.*

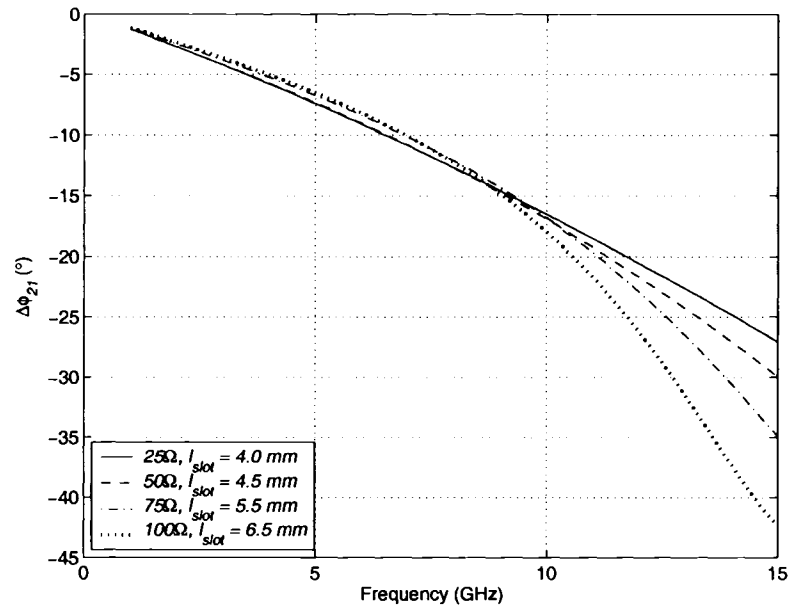
Table 3.3: *1) Return loss and $\Delta\phi_{21}$ at 10 GHz; 2) frequency and $\Delta\phi_{21}$ when S_{11} = –10 dB, for a 25Ω, 50Ω, 75Ω, and 100Ω system impedance, with l_{slot} = 4.5 mm and w_{slot} = 0.5 mm, respectively.*

Impedance (Ω)	*At 10 GHz*		*At S_{11} = -10 dB*	
	S_{11} (dB)	*$\Delta\phi_{21}$ (°)*	*Freq. (GHz)*	*$\Delta\phi_{21}$ (°)*
25	-8.02	-21.88	8.30	-17.62
50	-9.90	-17.74	10.00	-17.74
75	-13.06	-12.35	12.65	-17.62
100	-15.27	-9.63	14.40	-17.76

Data in Table 3.3, as well as Figure 3.13 (a), indicates that with slot dimensions constant within each impedance system, the lower the line characteristic impedance, the lower the frequency at which the return loss threshold will be attained. This suggests that a smaller slot is necessary for lesser impedance systems, while a longer slot is required by higher impedance systems to achieve the same phase result at the desired frequency. Thus, utilizing a lower impedance system may offer some advantages in terms of miniaturization of the ground plane slot elements. Approximate slot lengths were determined to be l_{slot} = 4.0 mm, 5.5 mm, and 6.5 mm, for the 25Ω, 75Ω, and 100Ω systems, respectively, to satisfy the S_{11} limit and $\Delta\phi_{21}$ at 10 GHz. The simulation results for these cases are detailed in Figure 3.14 over a frequency range from 1 to 15 GHz. Above 10 GHz, the higher impedance lines indicate greater loss and phase levels, while at frequencies below 10 GHz, insertion loss, return loss, and differential insertion phase levels are similar.



(a)



(b)

Figure 3.14: *S-parameters and differential insertion phases for line impedances of 25Ω, 50Ω, 75Ω, and 100Ω; (a) S_{21}, S_{11}, and (b) $\Delta\phi_{21}$ with respect to frequency, for w_{slot} = 0.5 mm and l_{slot} as indicated.*

3.4 Paired-Slot Combination

All previous investigations involved a single slot defect below a transmission line. The slot impedance loads the line and thus deteriorates its input impedance match. This problem can be overcome by considering pairs of slots, provided the reflection of one cancels that of the other, as investigated in this section. A paired defect combination was placed beneath the transmission line, with the element separation d_{slot} as the variable parameter, defined in Figure 3.15.

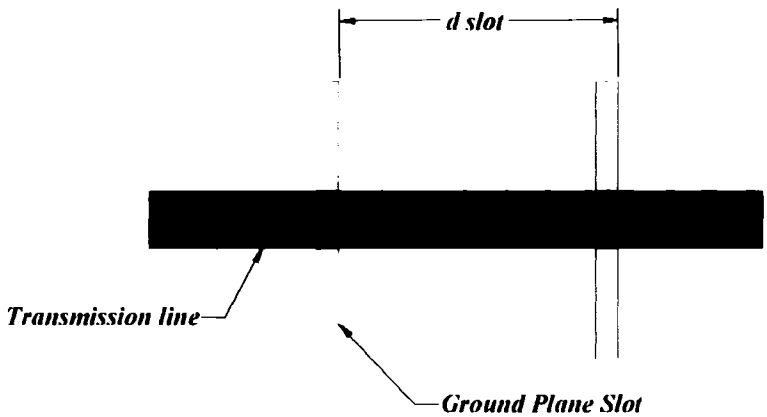
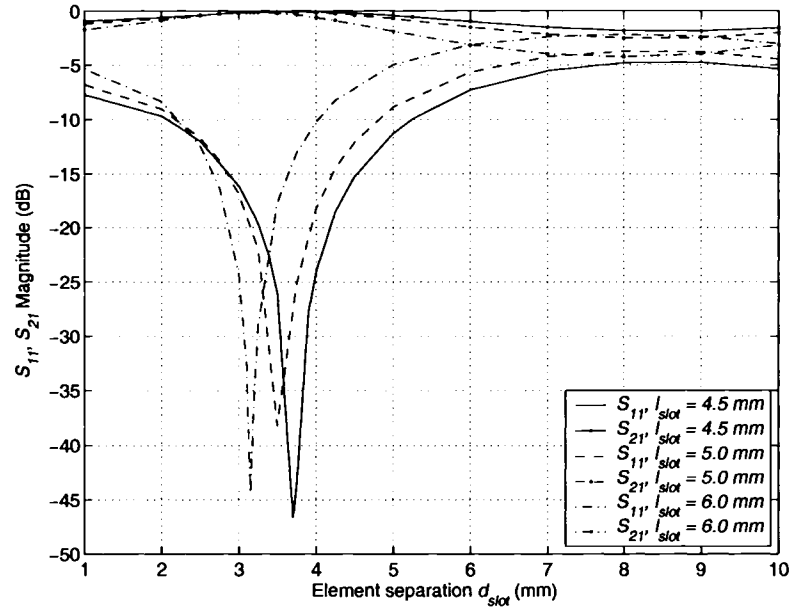
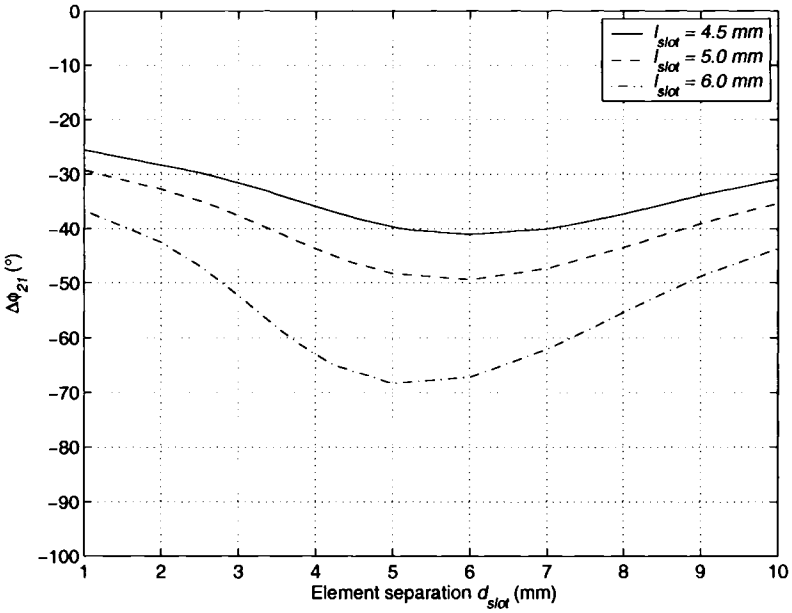


Figure 3.15: *Paired-slot combination,* $w_{slot} = 0.5$ *mm.*

Simulation results of the S_{11}, S_{21}, and $\Delta\phi_{21}$ are shown in Figure 3.16 for three slot lengths of 4.5, 5.0, and 6.0 mm, each with slot width of 0.5 mm. It is interesting to note from Figure 3.16(a) that for all these cases, there exists a small inter-slot separation, between 3 and 4 mm, where the input reflection is totally eliminated. Figure 3.16 (b) shows the differential phase shifts, which are larger than those of a single slot. For instance, the matched pair of 6 mm slots provides about 55° of phase shift at its optimum return loss slot separation. This separation provides more than three times the phase shift than that provided by a single slot, while also occurring at the optimum impedance match of the phase shifter. If higher reflection levels can be tolerated, phase shift values of about 62° are attainable with an S_{11} of −10 dB.



(a)



(b)

Figure 3.16: *S-parameters and differential insertion phases of a paired slot combination for different slot lengths with w_{slot} = 0.5 mm and Z_o = 50Ω; (a) S_{21}, S_{11}, and (b) $\Delta\phi_{21}$.*

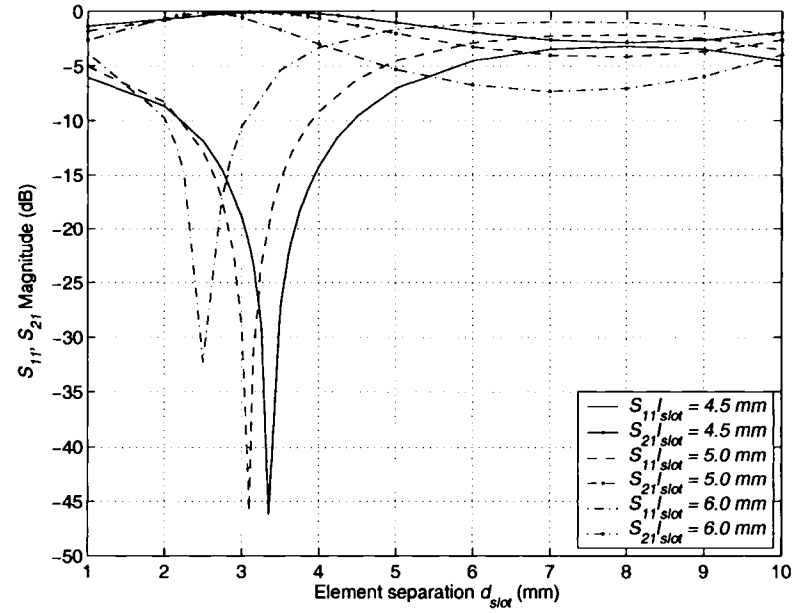
3.4.1 System Impedance

It was observed in section 3.2.5 that there was no additional benefit to the achieved phase by a single defect structure at the return loss threshold, if a system impedance other than 50Ω is selected. However, with a lower line impedance, the maximum phase shift achievable at the S_{11} limit occurred at a lower frequency. Thus, for a fixed slot length, it may be suggested that the implementation of a lower impedance system when utilizing a multiply-defected structure, would produce greater phase shift when compared to a similar structure designed with a higher impedance line. With this in mind, paired slot combinations with l_{slot} = 4.5, 5.0, and 6.0 mm were also implemented with 25Ω and 100Ω transmission lines. The S_{21}, S_{11}, and $\Delta\phi_{21}$, results are provided in Figures 3.17 and 3.18. As expected, $\Delta\phi_{21}$ in Figure 3.17 (b) for the 25Ω line is more significant than the phase levels observed in Figure 3.16 (b) with the 50Ω line, for all l_{slot} considered. A greater magnitude of $\Delta\phi_{21}$ was also achieved over reduced element separations.

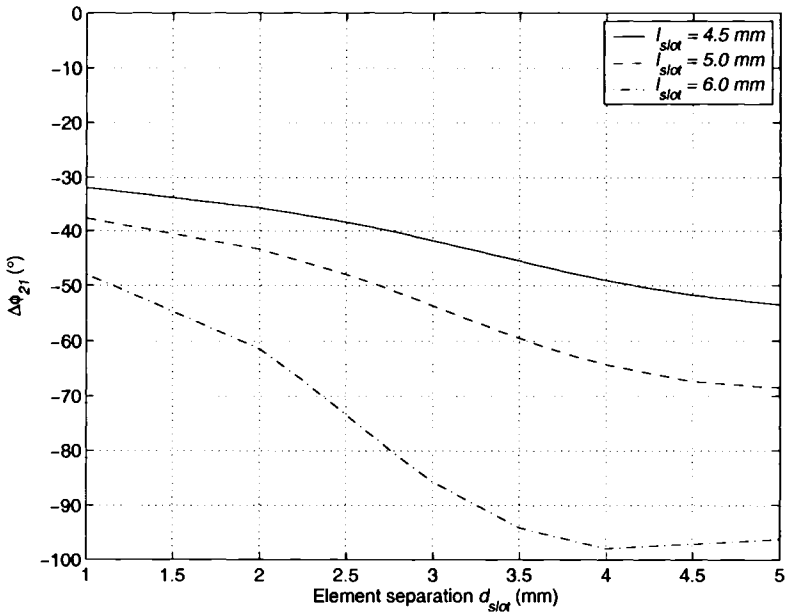
Figure 3.19 indicates an equivalent phase shift result for each of the system impedances under consideration, when utilizing shorter slot lengths as the line impedance drops from 100Ω to 25Ω. Slot lengths of 4.0, 4.5, and 6.5 mm illustrate impedance match and equivalent phase levels at a similar slot separation, in and around 3.7 mm. The values for l_{slot} considered in Figure 3.19 are identical to those determined for optimum phase and return loss in the single slot discussion of 3.3.5. The results at the impedance match points are summarized in Table 3.4, for the above three cases, with the 6.0 mm slot pairs.

Table 3.4: *Differential phase shifts at the match points for the three line impedances of 25Ω, 50Ω, and 100Ω, for paired slots of l_{slot} = 6.0 mm, and w_{slot} = 0.5 mm.*

Line impedance (Ω)	*d_{slot} separation (mm)*	*$\Delta\phi_{21}$ (°)*
25	*2.50*	*-73*
50	*3.15*	*-54*
100	*4.00*	*-32*

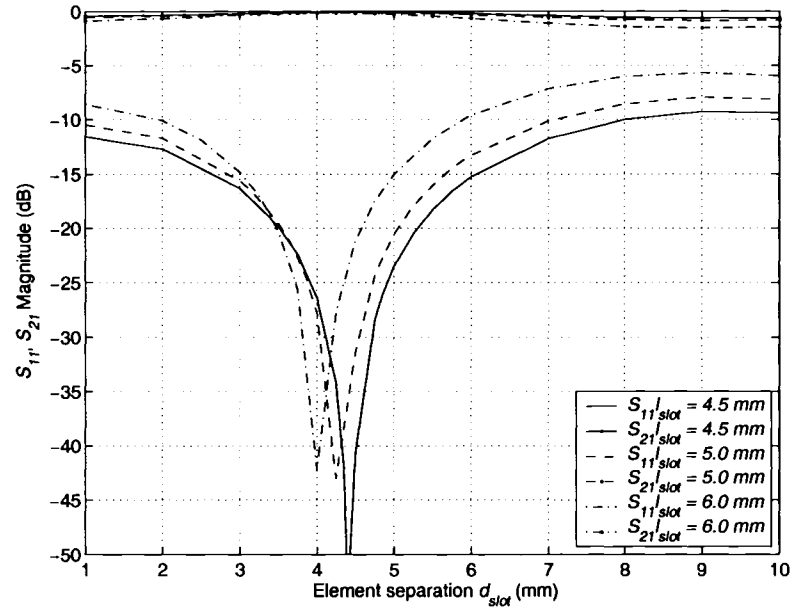


(a)

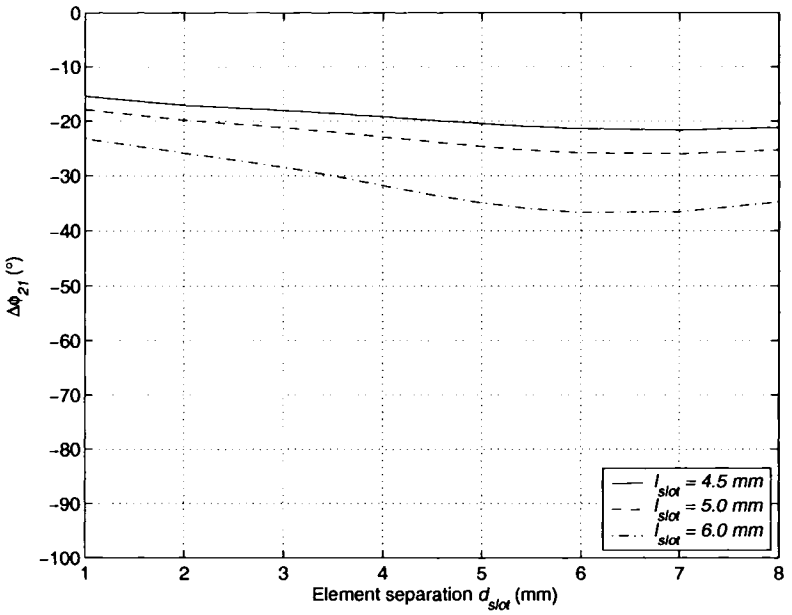


(b)

Figure 3.17: *25Ω line paired slot combination; (a) S_{11} and S_{21}, (b) $\Delta\phi_{21}$.*

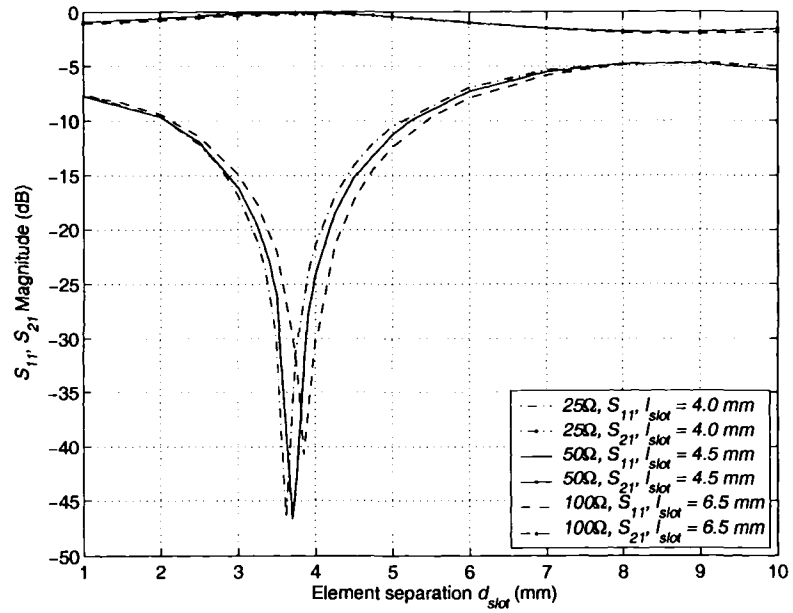


(a)

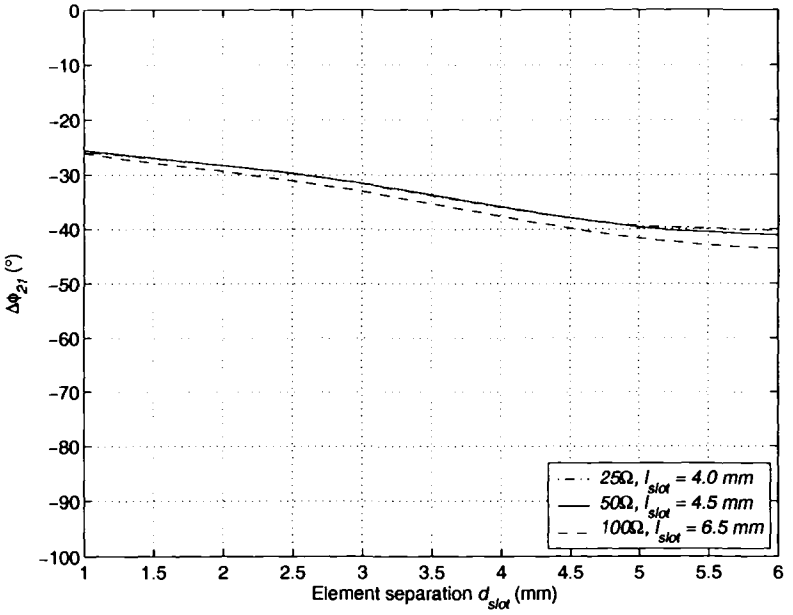


(b)

Figure 3.18: *100Ω line paired slot combination; (a) S_{11} and S_{21}, (b) $\Delta\phi_{21}$.*



(a)



(b)

Figure 3.19: *Paired combinations of l_{slot} = 4.0 mm for Z_o = 25Ω, l_{slot} = 4.5 mm for Z_o = 50Ω, and l_{slot} = 6.5 mm for Z_o = 100Ω; (a) S_{21}, S_{11}, and (b) $\Delta\phi_{21}$.*

3.5 Performance Comparison for Single and Paired Slots

3.5.1 Line Loss and Figure of Merit

The transmission line with a defected ground plane is a two-port microwave circuit. A general two-port network embedded between a source and a load is shown in Figure 3.20, where Γ_s and Γ_T are the source and load reflection coefficients. The following discussion assumes forward transmission from port 1 to port 2. For a physically symmetric two-port, such as the single and multiple defect structures presented to this point, the discussion also holds for transmission from port 2 to port 1.

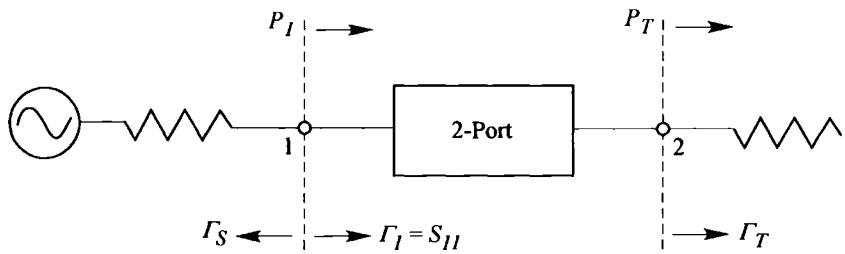


Figure 3.20: *Two-port system.*

In general terms, the insertion loss L_I, is defined as the ratio of the power delivered to the load of a two port system, with respect to a reference power delivered to the load when it is directly connected to the source [89]. This loss may be expressed as,

$$L_I = 20\log|S_{21}| \tag{3.5}$$

The insertion loss of a two-port system is a representation of two loss components, i.e. the mismatch loss, L_M, and the dissipation loss, L_D, or line loss, and is given by [89],

$$L_I = 10\log\left(\frac{P_1}{P_o}\right)\left(\frac{P_T}{P_1}\right) = L_M + L_D \tag{3.6}$$

where P_1 is the power delivered to port 1 of the defect structure, P_o is the power from the source or the Z_o-available power delivered to a load under matched conditions, and P_T is

the power delivered to the load. The mismatch loss, L_M, and the dissipation loss L_D are expressed in terms of P_o, P_1, and P_T, as,

$$L_M = 10\log\left(\frac{P_1}{P_o}\right) \tag{3.7}$$

$$L_D = 10\log\left(\frac{P_T}{P_1}\right) = 10\log\eta \tag{3.8}$$

where η is a measure of the efficiency of the two-port. The power P_1 is dependent on the incident power from the generator, P_o, and the reflection coefficient Γ_1,

$$i.e. P_1 = P_o\left(1-|\Gamma_1|^2\right) \tag{3.9}$$

Substituting (3.9) into (3.7), and knowing that the S_{11} magnitude of the two-port is equivalent to the magnitude of its input reflection coefficient Γ_1, the mismatch loss may be expressed as,

$$L_M = 10\log\left(1-|S_{11}|^2\right) \tag{3.10}$$

The expression in (3.10) indicates that the mismatch loss is a measure of the impedance mismatch between the defected transmission line structure and the source. For a lossless two-port, $\eta = 1$, and L_D is 0 dB. Thus,

$$L_1 = L_M = 10\log\left(1-|S_{11}|^2\right) \tag{3.11}$$

If the two-port is matched, $L_M = 0$ dB, and

$$L_1 = L_D = 20\log|S_{21}| \tag{3.12}$$

Thus, under matched conditions, the insertion loss and the line loss are identical and can be interchanged.

The expression in (3.12) holds for the matched two-port transmission line with no defects in its ground plane. Thus, when considering a transmission line without a ground plane defect, the mismatch loss of the structure is 0 dB, and $L_1 = L_D$. With defects present in the ground plane, the line loss can be calculated as follows,

$$L_D = L_1 - L_M = 20\log|S_{21}| - 10\log\left(1-|S_{11}|^2\right) \tag{3.13}$$

The line loss L_D, represents the minimum possible loss that is present in the two-port defected transmission line system, while the insertion loss provides a more realistic representation of loss, provided it is referenced for the design of the final two-port structure, in this case a defected transmission line phase shifter. The line loss of the system is a constant minimum loss level, while the possible mismatch is variable and dependent upon the frequency bandwidth of the user, the number of elements utilized in the system, and consequently the overall line length of the defect structure. Mismatch loss is neither a dissipative or resistive loss component, but is a loss due to reflections returning to the input generator. It is a representation of the amount of power that propagates through the input terminals of the transmission line. The mismatch loss is external to the transmission line, as this structure alone was designed as a matched two-port.

The figure of merit (FOM) of a phase shifter is an expression of the phase shift of the device per dB of loss,

$$FOM = \frac{\Delta\phi_{21}}{L_I} \quad [°/\text{dB}] \tag{3.14}$$

The insertion loss is the loss component of interest with the FOM. However, since the defect phase shifter device is not yet a completed design, i.e. the switching element is not integrated within the structure, the FOM with respect to the insertion loss would not be an accurate classification of the defected transmission line performance with regards to phase shift at this stage. As the line loss is constant through out each stage of the design process, and is the minimum possible insertion loss associated with a two-port, the FOM with respect to L_D shall also be presented with that of (3.14) in the coming sections,

$$FOM = \frac{\Delta\phi_{21}}{L_D} \quad [°/\text{dB}] \tag{3.15}$$

3.5.2 Figure of Merit of Single and Paired Slots

The figure of merit for single and paired slot configurations is presented in this section. For completeness, FOM calculations using (3.14) and (3.15), for the insertion loss and line loss, respectively, are provided in Table 3.5 for the single slot, and in Table 3.6 for the paired slots. For the single slot defects listed in Table 3.5, the maximum phase shifts occur at the assumed limit of the reflection coefficient of –10 dB. It is clear from the data listed in Table 3.5 for the single slot case that the two FOMs are significantly different as a result of the mismatch loss. However, these values are identical for the paired slot cases at the optimum return loss slot separations.

***Table 3.5**: The insertion loss L_I, line loss L_D, and respective FOM for single slot configurations, with w_{slot} = 0.5 mm.*

Z_o (Ω)	l_{slot} (mm)	L_I (dB)	FOM w.r.t. L_I (%/dB)	L_D (dB)	FOM w.r.t. L_D (%/dB)
25	4.0	0.51	34	0.04	403
50	4.5	0.54	33	0.07	258
100	6.5	0.62	29	0.16	114

***Table 3.6**: The insertion loss L_I, line loss L_D, and respective FOM for optimal return loss of paired slot configurations, with w_{slot} = 0.5 mm, and l_{slot} = 6.0 mm.*

Z_o (Ω)	d_{slot} (mm)	L_I (dB)	FOM w.r.t. L_I (%/dB)	L_D (dB)	FOM w.r.t. L_D (%/dB)
25	2.50	0.15	487	0.15	487
50	3.15	0.15	360	0.15	360
100	4.00	0.16	200	0.16	200

3.6 Conclusions

The phase shifting properties of a single rectangular slot defect below a microstrip transmission line was investigated in this chapter. It was shown that the phase shift magnitude increases with increasing slot length and decreasing slot width. Two factors limited the maximum achievable phase shift. The first is the slot length, which must be kept below its resonance length of one half wavelength in the substrate, to avoid radiation. The second limiting factor is the phase shifter return loss. Loading the transmission line by the slot increases its return loss. Assuming the return loss to be limited by 10 dB, it was established via a parametric study that regardless of the slot dimensional parameters or the substrate permittivity and height, the maximum achievable phase shift due to a single slot was between 17° to 18°.

To overcome the return loss limitation, a paired slot configuration was used, such that one slot eliminated the reflection of the other. With this configuration, it is possible to further increase the slot length beyond that determined at the return loss limit for a single slot, to maximize the paired slot phase shift. In this case, the inter-slot separation distance sets a size limit for the phase shifter. Since there is a loss due to the transmission line length defined by the inter-slot separation, a figure of merit was expressed for the phase shifter, as the ratio of its achieved phase shift with respect to the loss. A parametric study was also conducted for the paired slots. It was found that the phase shifter figure of merit increased with a reduction in the line impedance. For the paired slots in Table 3.6 associated with a 25Ω line impedance, a figure of merit of 487°/dB was attained, which is more than twice that achieved by the semiconductor techniques discussed in 2.2.2. The loss of the semiconductor phase shifters increases rapidly with frequency. However, the defected transmission line is a passive structure and its loss is due primarily to line loss, and the rate of loss with frequency is much smaller.

CHAPTER 4

OPTIMIZATION OF DEFECT ELEMENT

The slot defect structure introduced in Chapter 3 was optimized for phase and return loss. However, with a single defect element, the associated S_{21} appears unsatisfactory as the S_{11} pushes the limit of the desired return loss. This would therefore imply that using a single defect element would not provide the most attractive return loss characteristics. It was however determined that when incorporating the slot in a paired combination of defects, the optimization of the return loss of the individual structure will not be necessary when seeking maximum phase by a combination of ground plane defects. The reflection of one defect can be cancelled by the other, resulting in a small return loss for the system. Thus, if the initial stages of the defect design include prior knowledge of a multiple defect structure as a final design, selection of the unit defect element need not satisfy the earlier return loss threshold of 10 dB. Consequently, there is a possibility to further optimize the phase output by the unit element, if there is no longer a rigid restriction on the return loss produced by a single element.

This chapter presents data resulting from attempts to further optimize the uniform slot discussed in Chapter 3, by pursuing additional variables of dimensional and positional variation, while still respecting the selected width and length already determined to produce a respectable phase shift. The rectangular slot candidate having width and length of 0.5 mm and 4.5 mm, respectively, for $\varepsilon_r = 3$ and $Z_o = 50\Omega$ microstrip parameters, was selected as the initial base element for optimization. Preliminary attempts at simulating a short-circuit along the defect structure are presented, with conclusions from this study applied to the optimization of the structure. A circuit model for the optimized defect is presented, with lumped element values extracted via the full wave analysis of the defect structure. Data in this Chapter was compiled through simulation using Ansoft Ensemble 8.0 and Designer software packages.

4.1 Effects of Position and Metallization

4.1.1 Defect Positioning

The effect of a slot that is offset or located some distance from the line is expected to be less significant than an identical defect placed immediately in the path of the current in the ground plane. This behaviour was confirmed by gradually shifting the position of an individual slot beneath the transmission line, with the offset as defined in Figure 4.1.

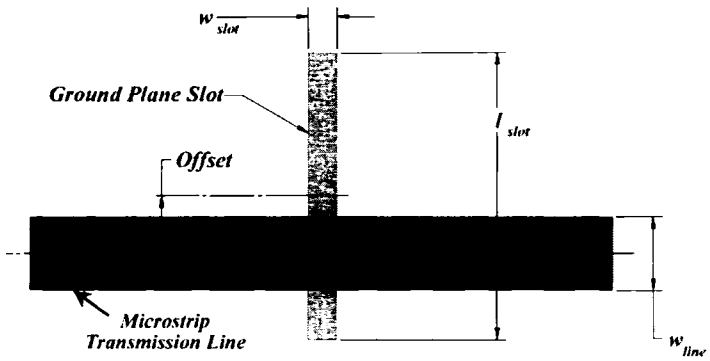
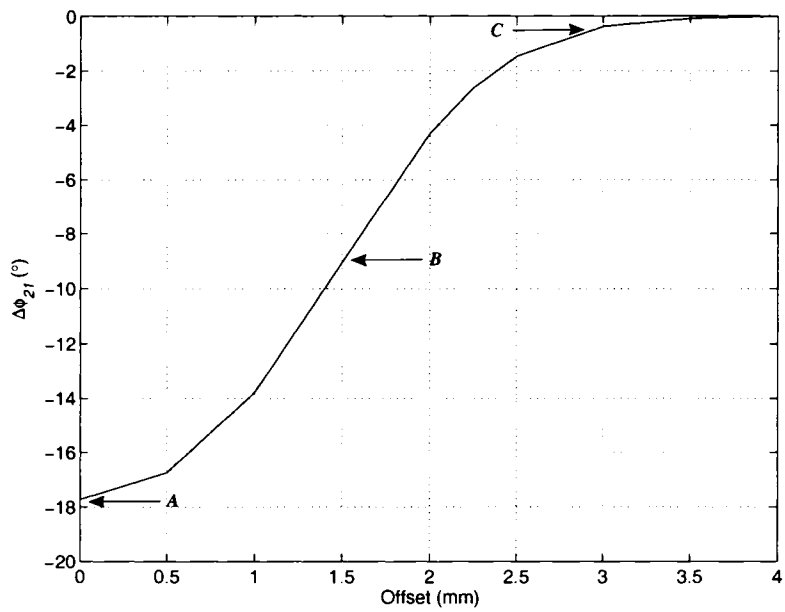
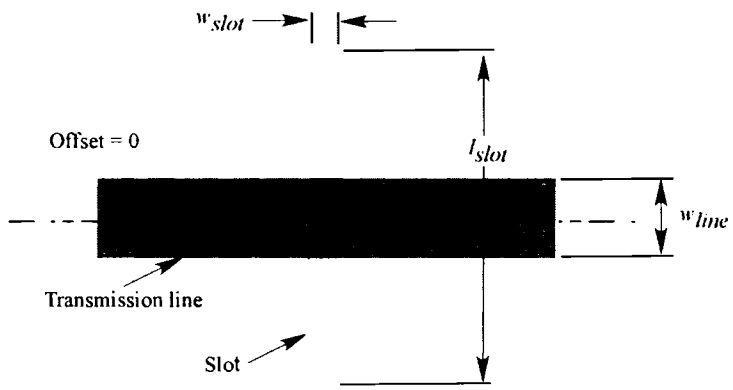


Figure 4.1: *Offset slot.*

The effect on the phase diminishes as the slot symmetry is disturbed, as shown in Figure 4.2 (a). An offset of 0 mm refers to a centred slot, shown in Figure 4.2 (b), symmetrically located directly below the transmission line, whose associated phase is highlighted in the figure by point *A*. The most rapid decline occurs when the offset position is between 1 and 2 mm. The mid-point in this phase level decline is just below 9°, designated by point *B*, does not occur when the slot has been shifted by half its length, i.e 2.25 mm, but at just over 1.5 mm. When the slot has been shifted upwards by ($l_{slot}/2 - w_{line}/2$) = 1.61 mm, the full region below the transmission line is still occupied by the slot, but no portion of it is visible in the region below the transmission line, identified in Figure 4.2 (b). When the entire slot is offset to one side of the line (Figure 4.2 (c)), above 2.89 mm ($l_{slot}/2 + w_{line}/2 > 2.89$ mm), its effect on the current distribution is no longer significant, and $\Delta\phi_{21}$ is virtually zero, indicated by point *C*.

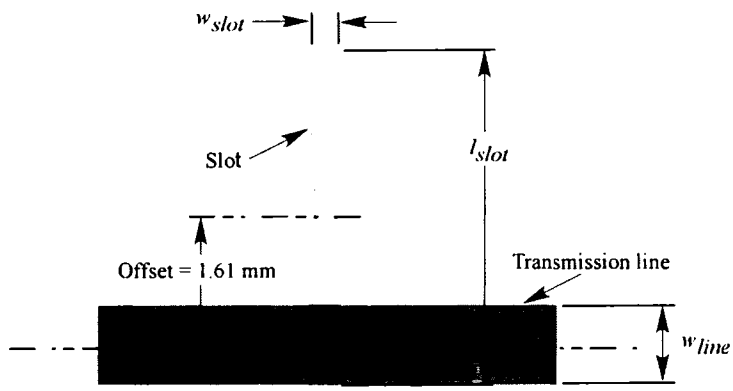


(a)

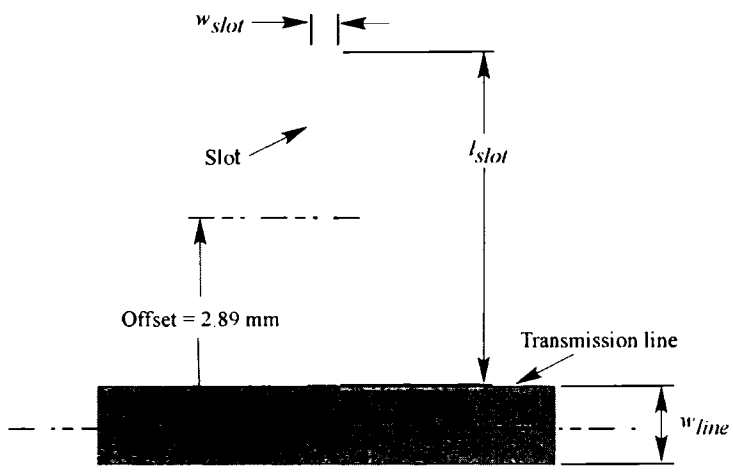


(b)

Figure 4.2: *(a) $\Delta\phi_{21}$ for offset positioning; offset configuration at points (b) A, (c) B, and (d) C.*



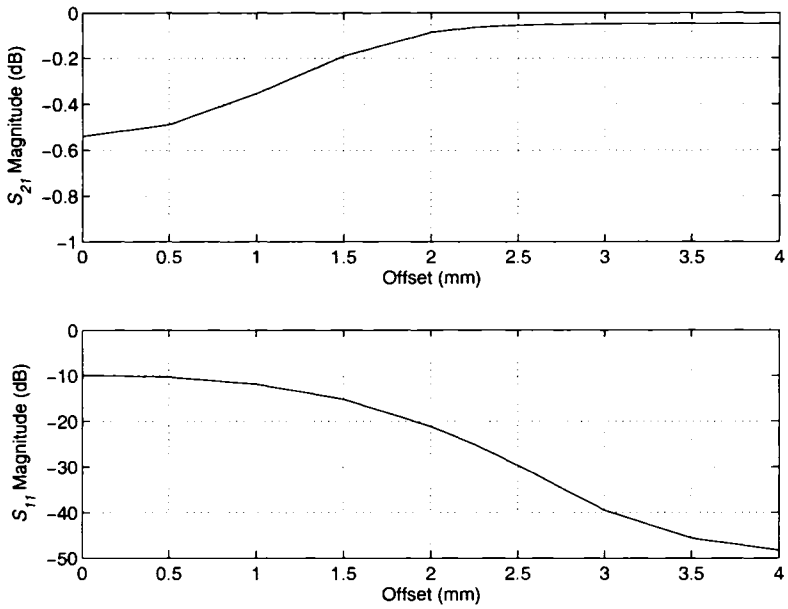
(c)



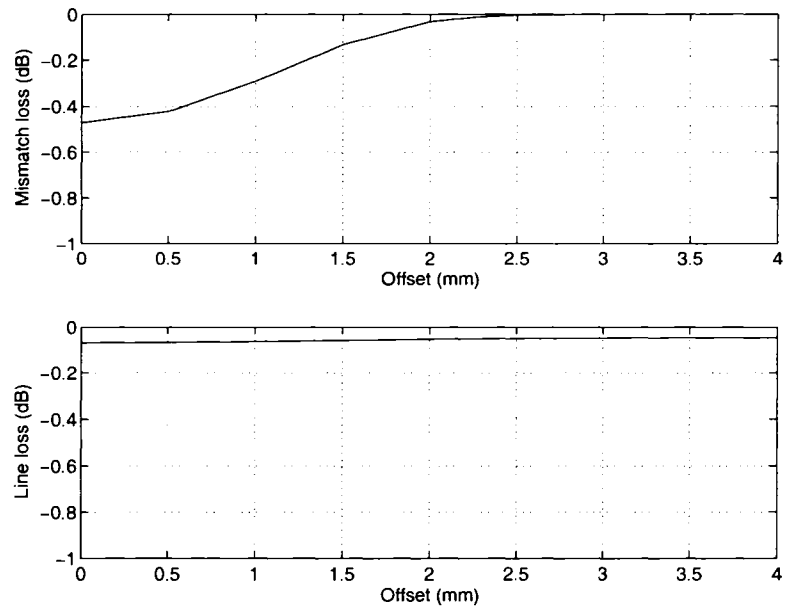
(d)

***Figure 4.2** continued*

The S_{11} and S_{21} levels at point C (offset = 2.89 mm) mirror the characteristics of a conventional transmission line, as shown in Figure 4.3 (a). Because the structure at this point, and for higher offset values, is well matched, the mismatch loss is non-existent, observed in Figure 4.3 (b), with the line loss of the structure over the entire offset range indicating a loss magnitude below 0.1 dB. In Figure 4.3 (c), the FOM calculated with respect to the total insertion loss indicates a peak at an offset of 2 mm, while the FOM shown due to the line loss follows the phase trend of Figure 4.2 (a), indicating greater FOM for a zero offset condition.

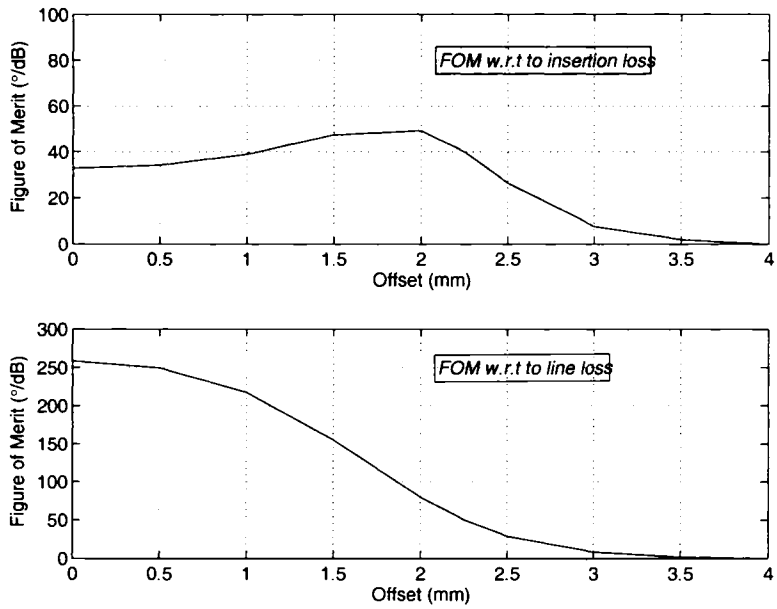


(a)



(b)

Figure 4.3: *Slot offset effect; (a) S_{11} and S_{21}, (b) mismatch loss and line loss, (c) figure of merit (FOM) with respect to (w.r.t.) insertion loss and line loss.*



(c)

***Figure 4.3** continued*

4.1.2 Short-Circuit via Metallization

While the study and application of the ground plane defect at this stage did not include a switching element, a preliminary investigation explored the potential effects caused by applying a short circuit to select locations along the slot. A simple metal strip was used to emulate a short circuit, by severing the slot at a specific location. The slot centre was referenced to 0 mm, with the initial placement of the strip located at this point, effectively dividing a symmetric slot into two separate offset slots. The strip was then moved towards an extremity of the slot and the effect observed. Two experiments were performed involving metal strips with dimensions of $w_{slot} \times y_{strip}$,

- w_{slot} = 0.50 mm × y_{strip} = 1.28 mm; w_{line}= 1.28 mm
- w_{slot} = 0.50 mm × y_{strip} = 0.50 mm; w_{line}= 1.28 mm

Figure 4.4 (a) and (b) show a 0.5 mm × 1.28 mm strip located at the initial position of 0 mm, and 1.28 mm, respectively. In the first experiment, dimensions of w_{slot} × w_{line} (0.5 mm × 1.28 mm) were used to emulate the short-circuit. The greatest effect on the phase occurred by placing the strip immediately beneath the transmission line at the centre of the slot, referenced to 0 mm and shown in Figure 4.4 (a). Two slots result, with neither having any slot portion positioned directly below the transmission line, i.e. $w_{line} - y_{strip} = 0$. In such a case, $\Delta\phi_{21}$ is at a minimum, observed in Figure 4.4 (c). A similar phase result was observed in Figure 4.2 (a) at point *C*, for an offset slot adjacent, but not immediately below the transmission line. As the strip is moved along one end of the slot, its effect is less pronounced.

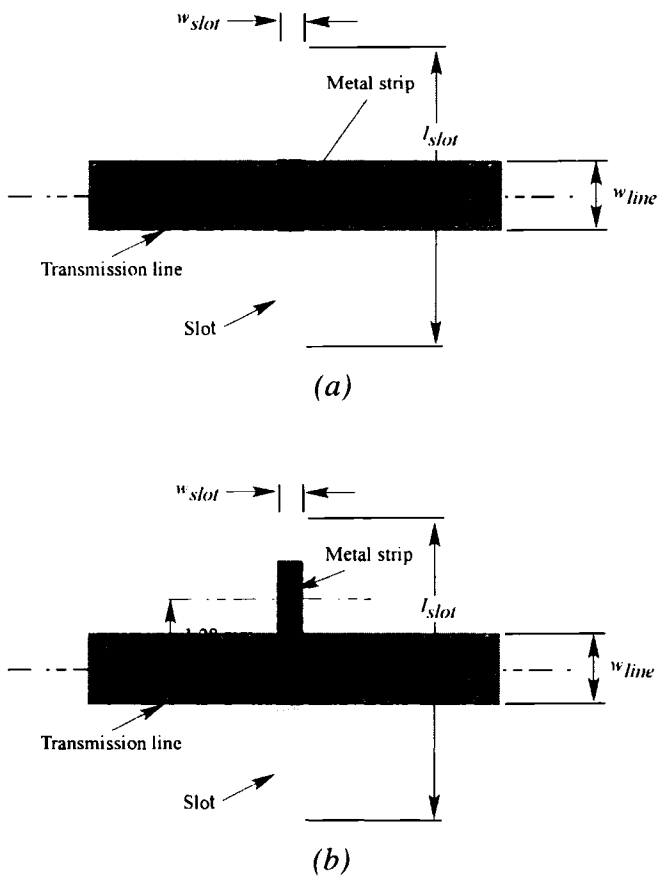
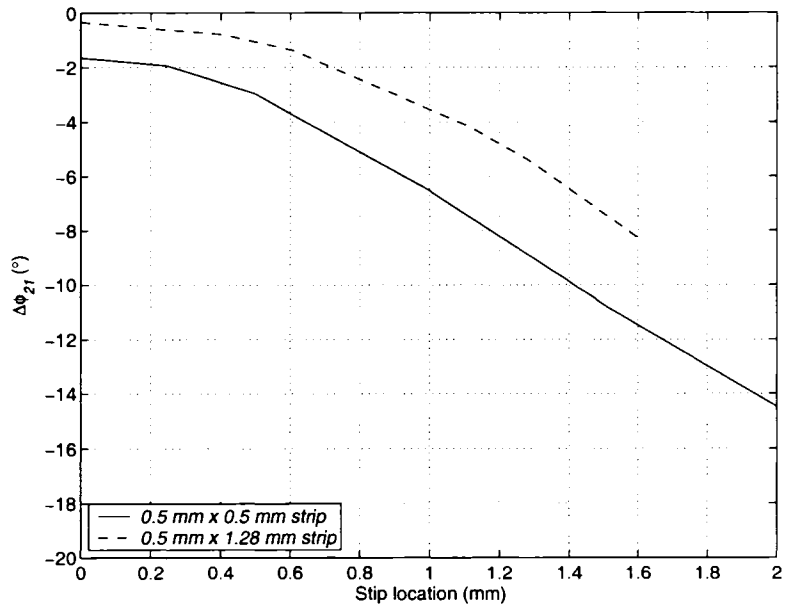


Figure 4.4: *0.5 mm × 1.28 mm metal strip at (a) 0 mm, (b) 1.28 mm, and (c) effect of metal strip on* $\Delta\phi_{21}$.



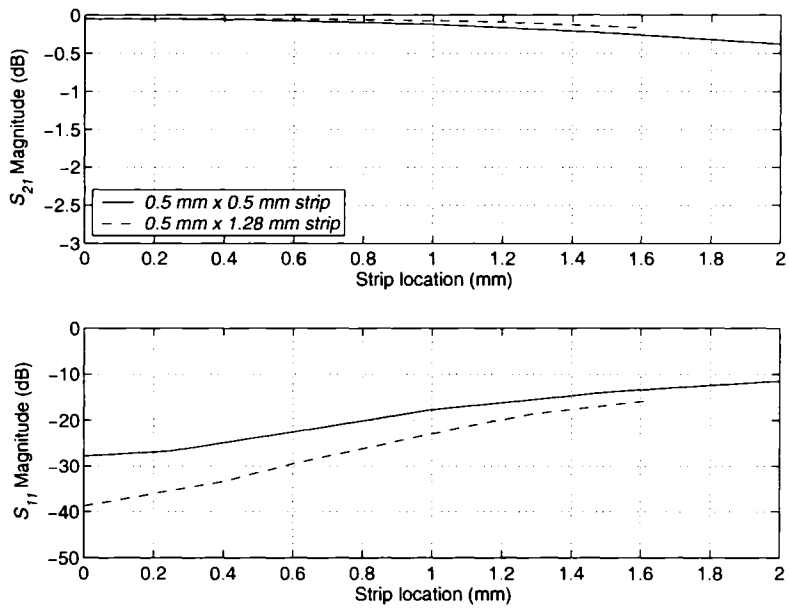
(c)

***Figure 4.4** continued*

This experiment was repeated for a strip of a smaller area, having a width identical to that of the slot defect, ie. $w_{slot} \times w_{slot}$ (0.5 mm × 0.5 mm). With the smaller strip positioned at the centre of a symmetric slot, almost 2° of phase is observed in Figure 4.4 (c). In this case, a portion of each of the two newly created offset slots remains positioned beneath the transmission line, since the smaller strip does not completely short out the region immediately below the transmission line, i.e. $(w_{line} - y_{strip})/2 = 0.39$ mm above and below the strip, or a total 0.78 mm of the slot remaining exposed. As observed in Figure 4.2 (a) with the offset slot, while a portion of the slot remains situated beneath the transmission line, the differential insertion phase value is reduced, but not negligible. An approximate comparison can be inferred between the phase result produced by the 0.5 mm × 0.5 mm strip at 0 mm and the phase of the offset slot in Figure 4.2 (a). With an offset of $l_{slot}/2 + (w_{line}/2 - y_{strip})$, or 2.39 mm, the slot is removed from the edge of the transmission line by 0.50 mm, leaving 0.78 mm of the slot beneath the line. This offset value corresponds to a phase shift magnitude of approximately 2°, just slightly higher

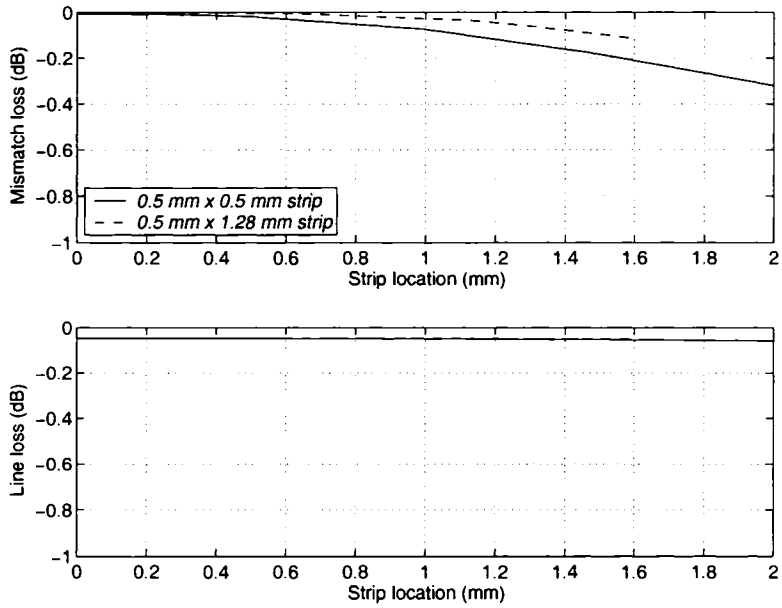
than the predicted phase level in Figure 4.4 (c), for the 0.5 mm × 0.5 mm strip. The greater phase level is slight, and may be attributed to a variety of factors, including the position of the offset slot, i.e. a portion of the slot lies directly below the transmission line center and not at the transmission line upper and lower edges as is the case with the strip metallization. The data observed in Figure 4.2 (a) as well as Figure 4.4 (c) strongly suggests that this region beneath the transmission line centre axis is highly significant in terms of phase. A slot positioned such that it lays below a portion of the transmission line, in particular its center axis, shall provide a significant measure of phase shift when compared to an identical and un-defected transmission line structure.

As the metal strip is moved away from the 0 mm reference, the mismatch loss observed in Figure 4.5 (b) increases with the diminishing short circuit effect of the strip. The FOM of Figure 4.5 (c) indicates maxima and minima similar to those observed in Figure 4.3 (c) with the offset slot. The S_{11} and S_{21} are provided in Figure 4.5 (a).

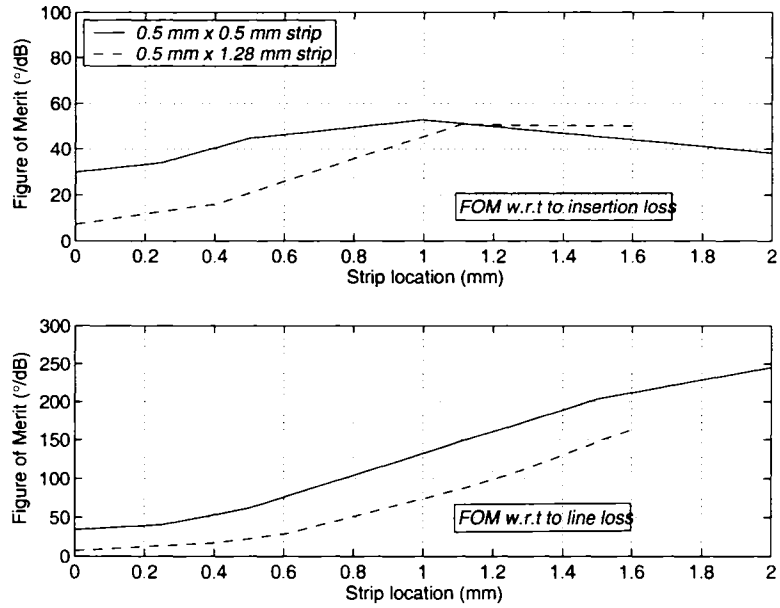


(a)

Figure 4.5: *(a) S_{11} and S_{21}, (b) mismatch loss and line loss, (c) figure of merit w.r.t to insertion loss and line loss, resulting from the placement of the metal strip.*



(b)



(c)

***Figure 4.5** continued*

4.2 Dumbbell Structure

The results for the offset and strip metallization effect on the slot in section 4.1 illustrate that a specific phase sensitivity exists within the 0.5 mm × 1.28 mm region in the ground plane. This region therefore holds a specific significance towards the placement of the shorting element, or of the defect itself, and must be considered when selecting a method to neutralize the phase shift effect of the slot when a phase shift is not desired. In addition, it is also possible that further optimization on the slot structure may be possible by focusing on this specific region.

In keeping with the conclusions that the slot should remain long, but also thin, and since the ground plane region beneath the transmission line has proven to be the most sensitive, some exploration was attempted to further optimize the unit defect element by altering the geometry of the slot lying in this region. Two additional variables were defined, identifying the width, w_g, and the length, l_g, of the slot region beneath the transmission line, as shown in Figure 4.6. For the purpose of discussion, the newly adjusted defect element shall be referred to as a "dumbbell" structure due to its similarity to that geometry.

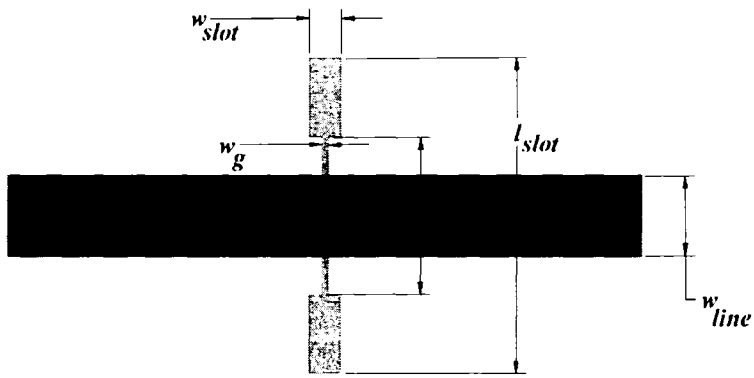
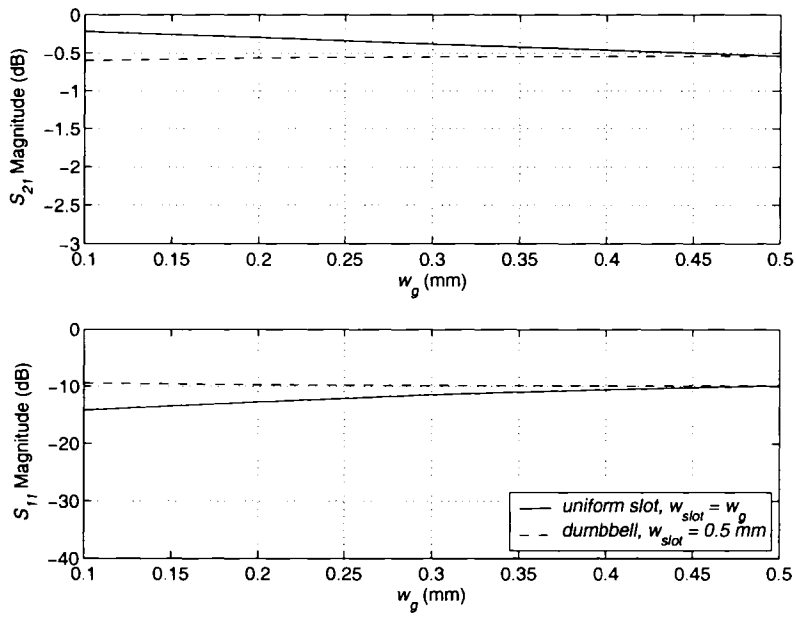


Figure 4.6: *Dumbbell loaded transmission line.*

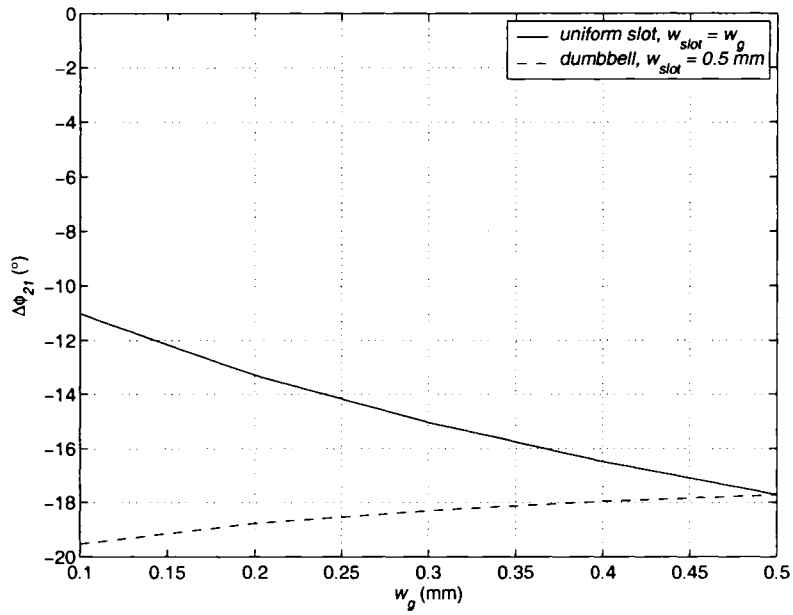
4.2.1 Gap Width

With w_{slot} and l_{slot} constant at 0.5 mm and 4.5 mm respectively, varying the magnitude of the variable w_g, from 0.1 mm to w_{slot}, results in the S-parameter data shown in Figure 4.7. In this study, the length of the gap was arbitrarily set to be equivalent to the dimensional width of the transmission line. The ensuing trend indicates that narrowing the slotted region beneath the transmission line provides a greater $\Delta\phi_{21}$ value. There is a very slight increase in the return loss, to just over –10 dB when w_g is at its minimum. The result is shown compared to a uniform rectangular slot with l_{slot} = 4.5 mm and $w_{slot} = w_g$. A uniform slot having a width of $w_{slot} = w_g$, does not receive the phase benefits observed while narrowing w_g with w_{slot} constant at 0.5 mm, as illustrated in Figure 4.7 (b).



(a)

Figure 4.7: *Variation of gap width, w_g; (a) S_{21}, S_{11}, and (b) $\Delta\phi_{21}$, for l_{slot} = 4.50 mm.*

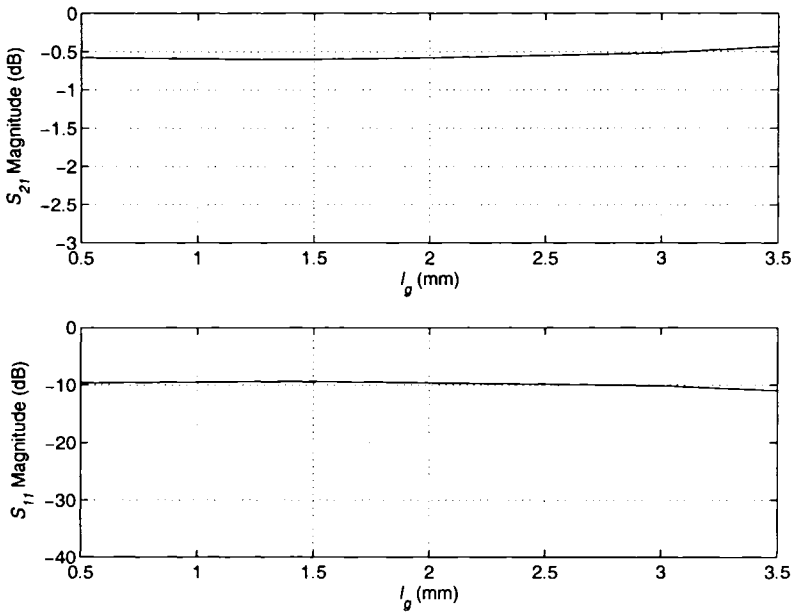


(b)

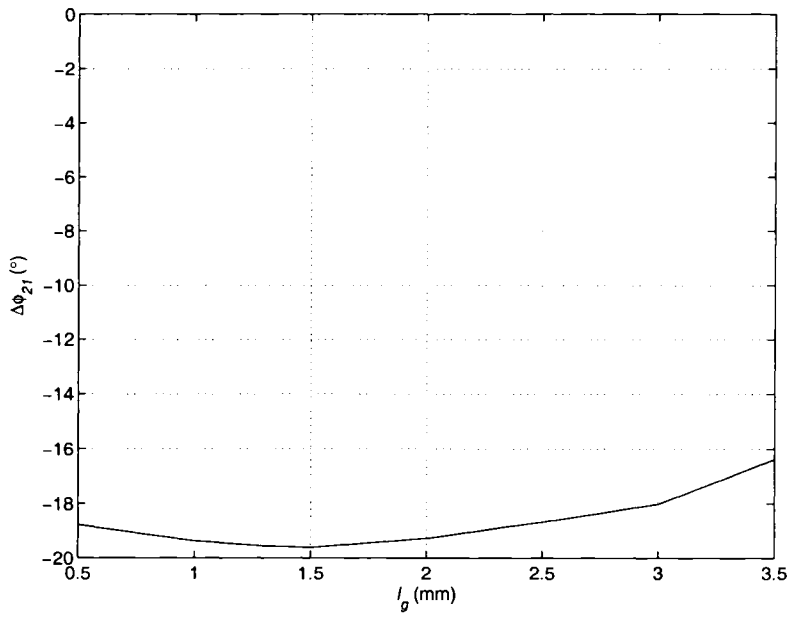
Figure 4.7 *continued*

4.2.2 Gap Length

The effect of altering the length of the gap, l_g, was also considered, while maintaining w_g constant to a width of 0.1 mm. From the *S*-parameter data illustrated in Figure 4.8, the optimal length was found to be in the region of l_g = 1.5 mm. Further, it appears from Figure 4.8 (b), that for $l_g < l_{slot}/2$ = 2.25 mm, there is an overall improvement in the differential insertion phase. An increase of almost 2° is achieved by the dumbbell geometry over the uniform slot for l_{slot} = 4.5 mm, when l_g and w_g are 1.5 mm and 0.1 mm, respectively.



(a)



(b)

Figure 4.8: *Variation of gap length, l_g; (a) S_{21}, S_{11}, and (b) $\Delta\phi_{21}$ for w_{slot} = 0.5 mm, w_g = 0.1 mm, l_{slot} = 4.50 mm.*

4.3 Slot vs. Dumbbell

4.3.1 Single Defect Element

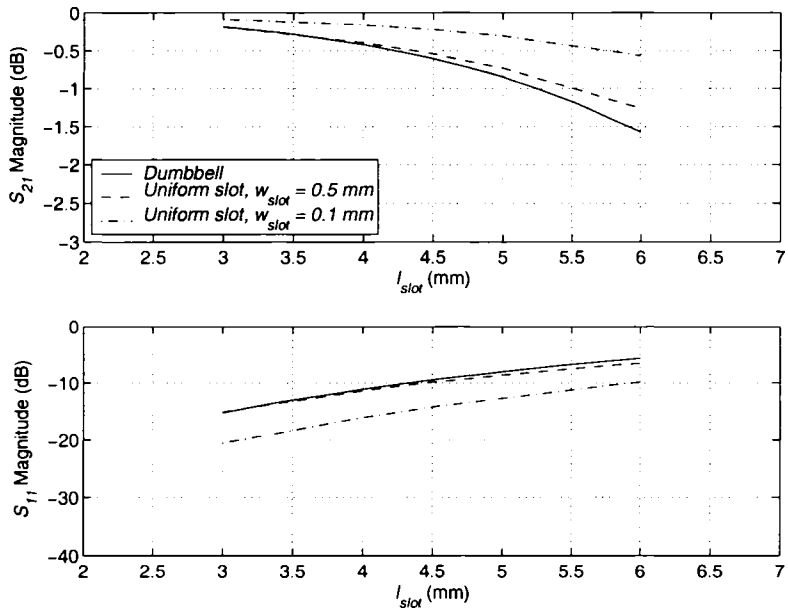
The improved performance by the dumbbell in comparison to the single uniform candidate slot established in Chapter 3 is examined in this section. Also presented for comparison is a uniform element having a slot width comparable to the gap width of the dumbbell. The dimensions of the newly adjusted dumbbell element, and the uniform defect structures are listed below:

- $w_{slot} = 0.5$ mm, $w_g = 0.1$ mm, $l_g = 1.5$ mm
- $w_{slot} = 0.5$ mm, $w_g = w_{slot} = 0.5$ mm, $l_g = l_{slot}$
- $w_{slot} = 0.1$ mm, $w_g = w_{slot} = 0.1$ mm, $l_g = l_{slot}$

The S_{11} and S_{21} magnitudes, and the differential insertion phase of the above defined element are presented in Figure 4.9, plotted with respect to the defect length. As observed in Figure 4.9 (b), a phase advantage exists by reducing the w_g and l_g dimensions of the slot, and transforming the unit element into a dumbbell configuration. Setting the uniform slot to $w_{slot} = w_g = 0.1$ mm, provides no phase advantage when comparing the slot lengths indicated. This structure cannot achieve a comparable phase while maintaining l_{slot} at a 1:1 ratio with the dumbbell. When w_{slot} is 0.5 mm and l_{slot} is equivalent to the dumbbell structure, a difference in phase of approximately 1° to 4° exists with the dumbbell structure, with the increased phase level observed with increasing defect length.

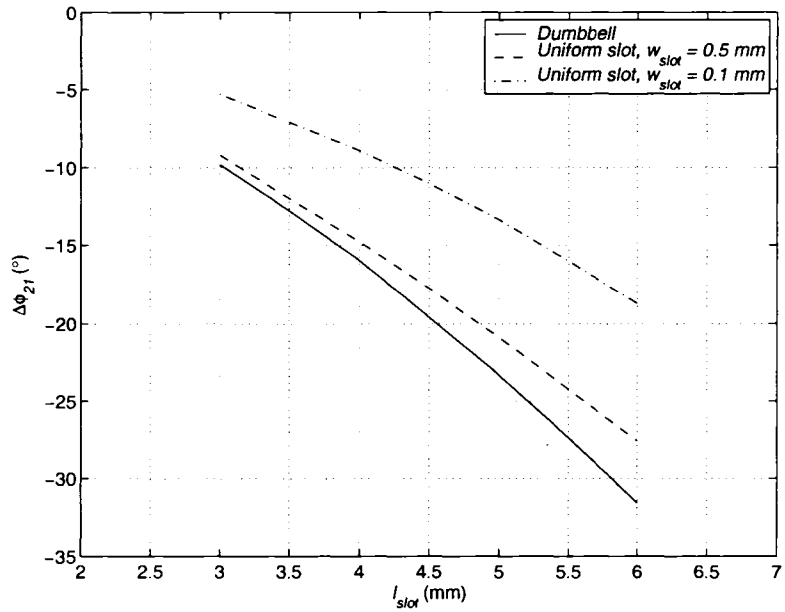
It is also important to note that with the structural increase in length, there is a gradual increase in the S_{21} of the dumbbell element. With this increase in insertion loss, due to the increasing mismatch shown in Figure 4.9 (c), the FOM with respect to the insertion loss, shown in Figure 4.9 (d) is identical to that of the uniform slot. While the FOM of the thinner 0.1 mm indicates a greater FOM with respect to the insertion loss, this is in fact an inaccurate comparison, since the phase level of this structure does not approach that of the wider dumbbell for the l_{slot} values in question. The mismatch for the

uniform slot of w_{slot} = 0.1 mm is lower, leading to a more advantageous FOM. The rising FOM with respect to the line loss is more representative of this trend, as the FOM improves with rising phase due to increasing l_{slot}. Peak FOM with respect to the line loss is illustrated at l_{slot} = 4.5 mm for the dumbbell and uniform slot having w_{slot} = 0.5 mm. This discrepancy between the insertion loss FOM and line loss FOM is due to the effect of the mismatch loss of the single element and can be corrected by pairing the defect elements, as shown in Chapter 3, and discussed further in the coming sections.

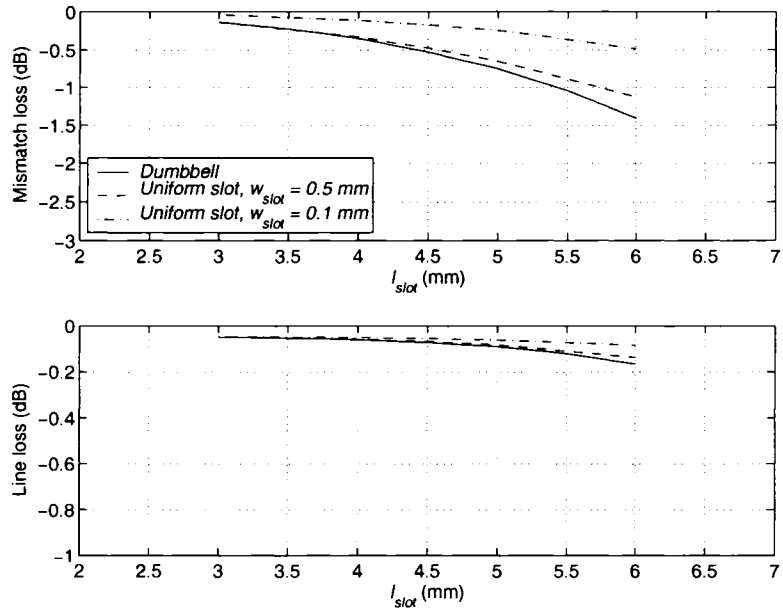


(a)

Figure 4.9: *Comparison of dumbbell element, w_{slot} = 0.5 mm, w_g = 0.1 mm, l_g = 1.5 mm, with uniform slot; case 1: w_{slot} = 0.5 mm; case 2: w_{slot} = 0.1 mm. (a) S_{21}, S_{11}, (b) $\Delta\phi_{21}$, (c) mismatch and line loss, and (d) figure of merit.*

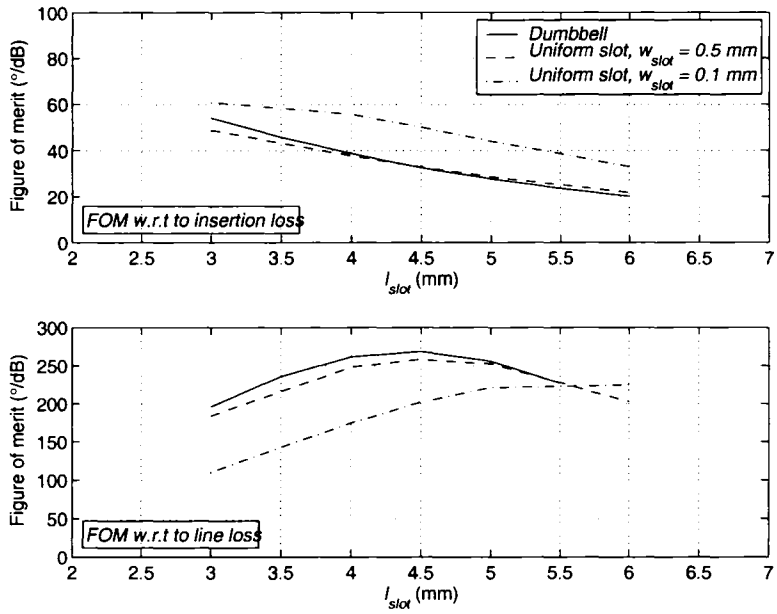


(b)



(c)

***Figure 4.9** continued*



(d)

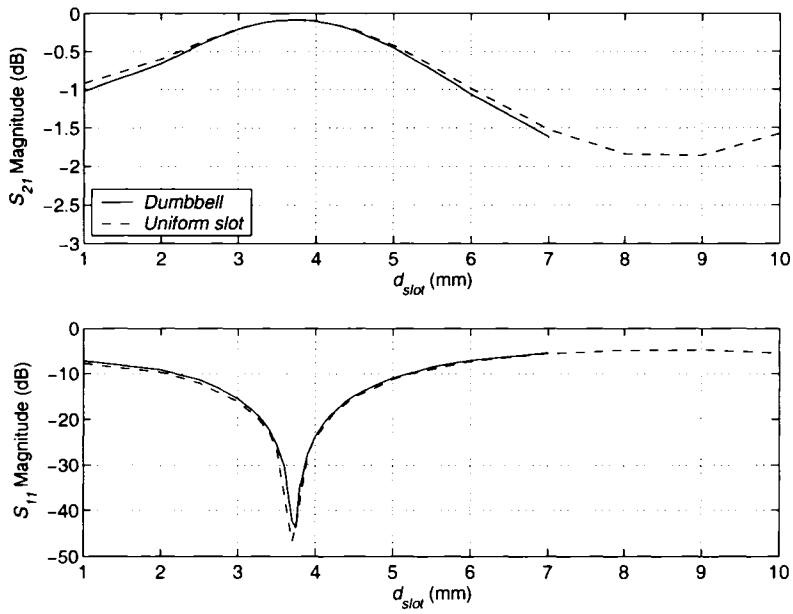
Figure 4.9 *continued*

4.3.2 Paired Defect Element

Paired configurations of the dumbbell candidate is briefly examined in this section in comparison to their uniform slot counterpart. Figure 4.10 exhibits the effect of a paired dumbbell structure, in addition to a paired uniform slot combination, each having dimensions of w_{slot} = 0.5 mm and l_{slot} = 4.5 mm. A gap width and length of w_g = 0.1 mm and l_g = 1.5 mm, respectively, are applied to the dumbbell. The differential insertion phase and *S*-parameter magnitudes of the paired dumbbell configuration are indicated for element separations between 2 and 6 mm where the S_{11} and S_{21} are most favourable. The S_{11} and S_{21} of the uniform and dumbbell structures are almost identical over this range of element separations, as shown in Figure 4.10 (a). While these *S*-parameter levels are very similar, the dumbbell combination consistently achieves around 5° of additional

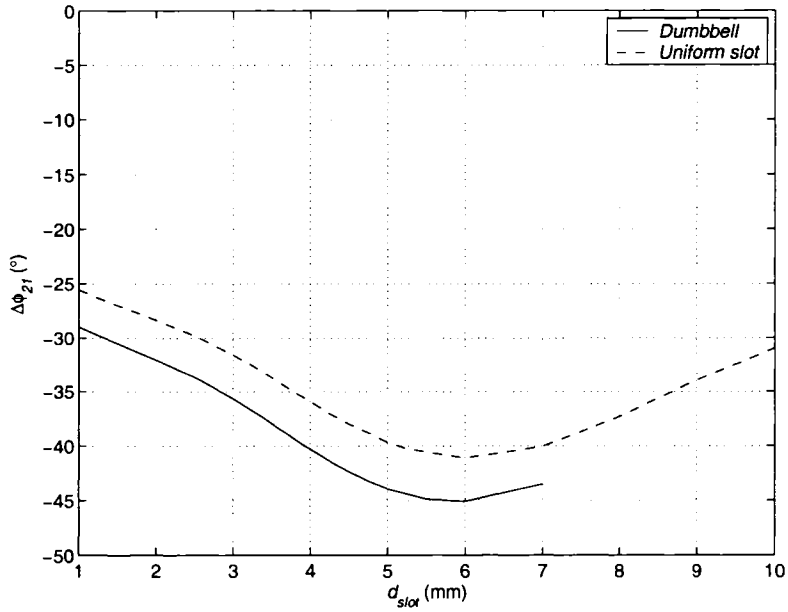
phase over the paired uniform slot, ranging from 33° to 44°, for d_{slot} between 2.2 mm and 5.2 mm.

The peak FOM revealed in Figure 4.10 (d) with respect to the insertion loss indicates almost 500°/dB at the impedance match, occurring for an element separation of d_{slot} = 3.75 mm (or $0.2\lambda_g$). The FOM level with respect to the line loss is almost identical, at just under 500°/dB, but is at a maximum for a slightly larger element separation of 4.5 mm (or $0.23\lambda_g$).

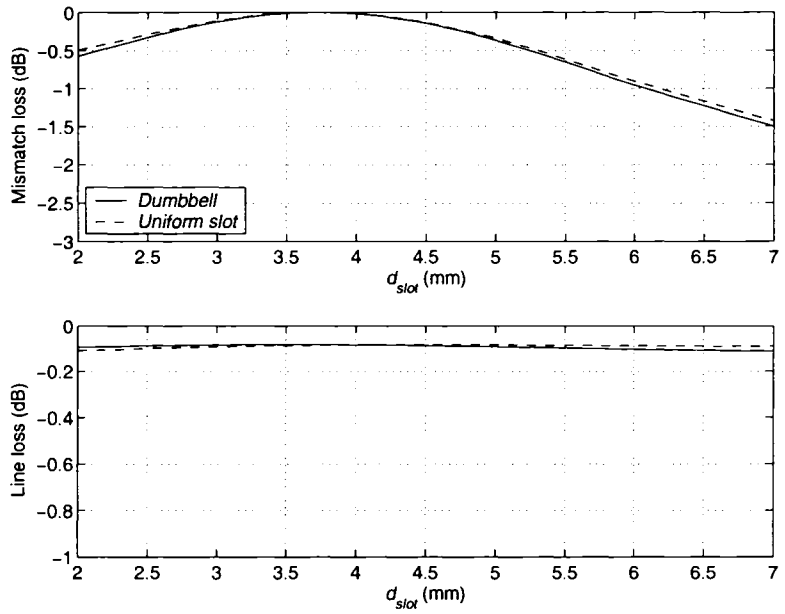


(a)

Figure 4.10: *Paired dumbbell vs. paired uniform slot respect to defect separation d_{slot}; (a) S_{21}, S_{11}, (b) $\Delta\phi_{21}$, (c) mismatch and line loss, and (d) figure of merit.*

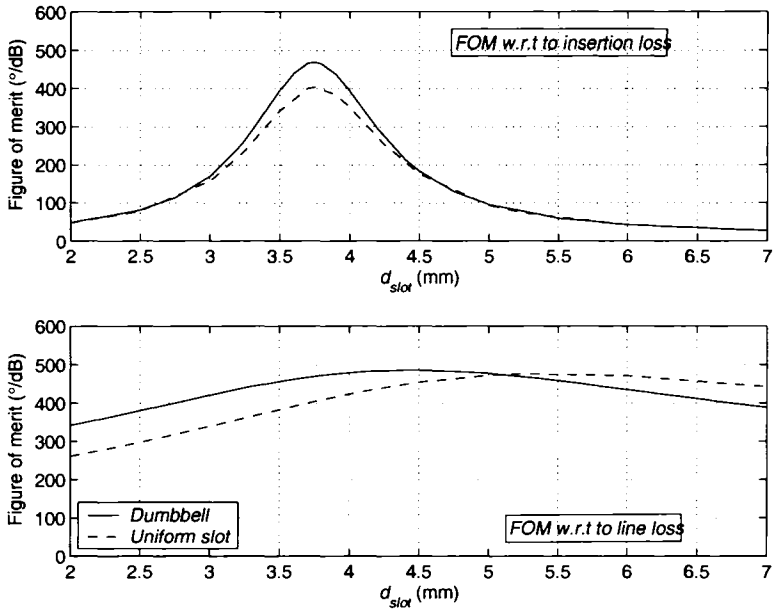


(b)



(c)

Figure 4.10 *continued*

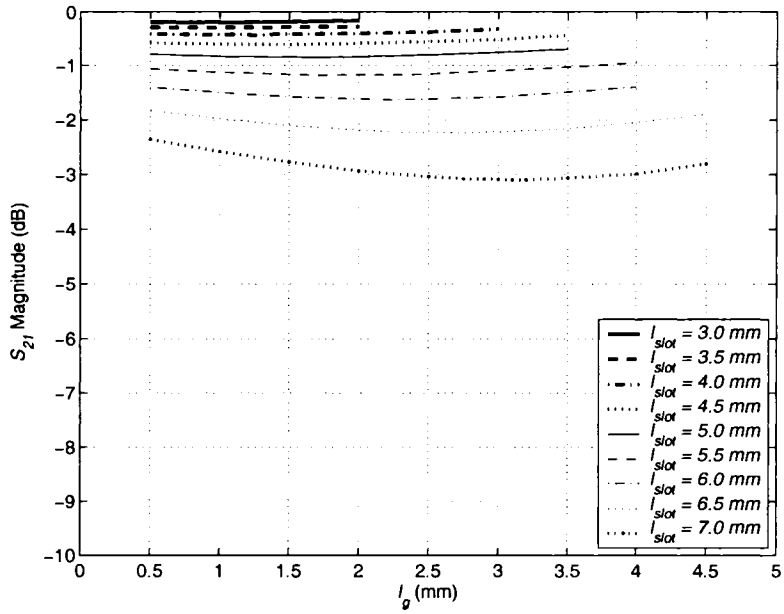


(d)

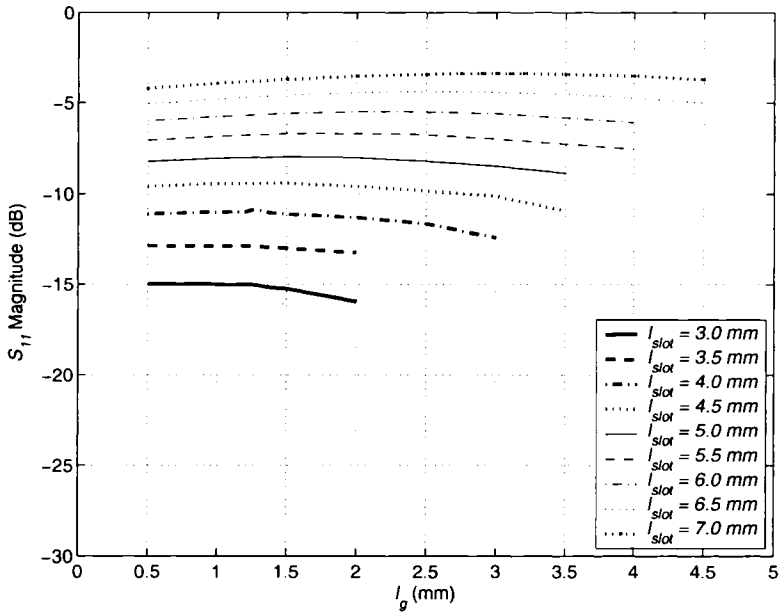
Figure 4.10 *continued*

4.4 Influence of Slot Length and Line Impedance on Gap Length

The geometry considered in Figure 4.6, utilized the candidate length and width selected in Chapter 3 for the slot defected 50Ω transmission line. Further study into the effect of the gap length is explored in this section, considering different slot lengths and line characteristic impedances. The effect of altering the system impedance on the dumbbell defect structure is similar to that of the uniform rectangular slot, in that lowering the system impedance increases the associated $\Delta\phi_{21}$. Figure 4.11 provides the S-parameter magnitude characteristics and $\Delta\phi_{21}$ for dumbbell lengths of l_{slot} = 3.0, 3.5, 4.0, 4.5, 5.0, 6.0, 6.5, and 7.0 mm, with w_{slot} = 0.5 mm, w_g = 0.1 mm, for varying gap length, l_g within a 50Ω system.

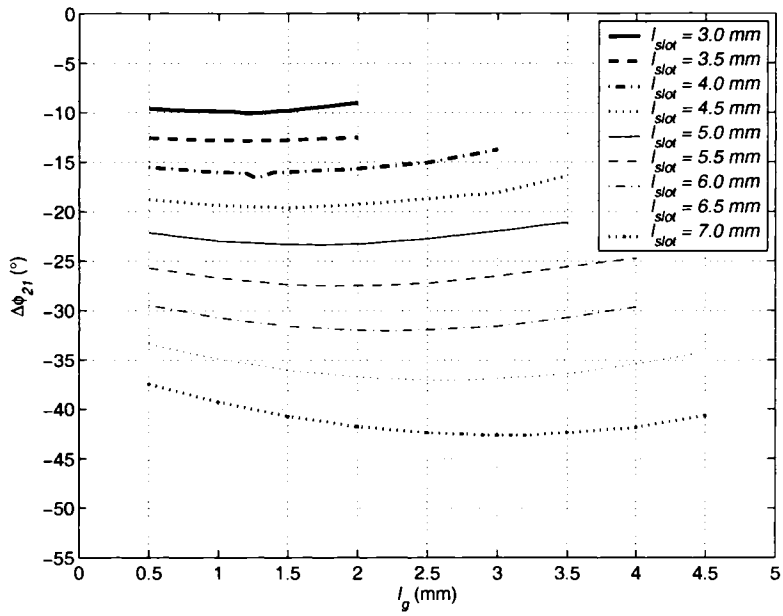


(a)



(b)

Figure 4.11: *Z_o = 50Ω; w_{slot} = 0.5 mm, w_g = 0.1 mm; Effect of variable l_g on (a) S_{21} (b) S_{11}, and (c) $\Delta\phi_{21}$ for l_{slot} as indicated.*



(c)

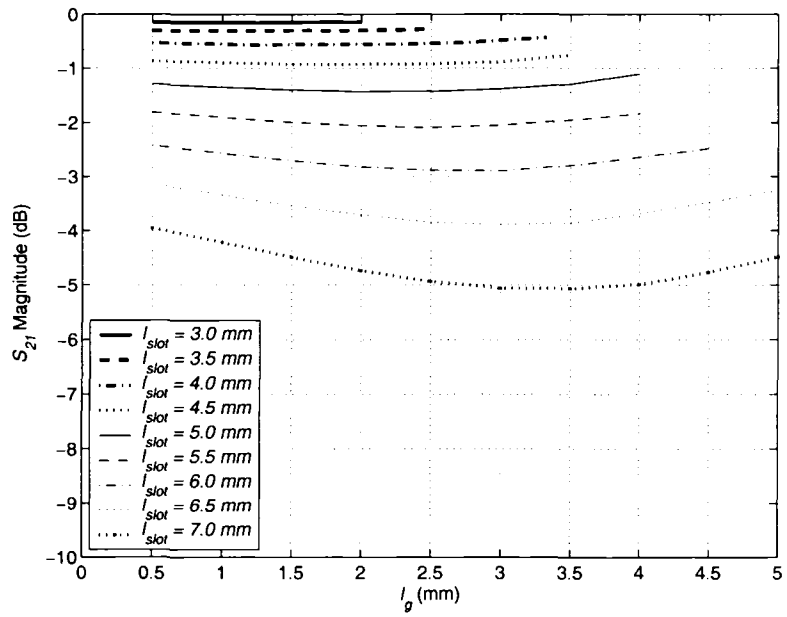
Figure 4.11 *continued*

As was observed in Chapter 3, with all other parameters held constant, lower impedance systems were found to provide greater phase shifts with smaller slot lengths. The *S*-parameter characteristics and $\Delta\phi_{21}$ for paired elements associated with 25Ω and 100Ω transmission lines are shown in Figures 4.12, and 4.13. It would appear that as the transmission line characteristic impedance drops, the optimal magnitude for the gap length approaches one half of the defect length. Figure 4.12 (b) for the 25Ω line illustrates this trend, with the maximum of the phase magnitudes occurring when l_g is approximately or very close to the value of $l_{slot}/2$. With a 100Ω line, optimal l_g is similar to that observed in Figure 4.11 (b) for longer slots, but drops with shorter slots whose phase levels are very low. The selection of $l_g < l_{slot}/2$, stated in section 4.2.2 is consistent with each dumbbell length selected for the defect in Figures 4.11 to 4.13.

Also discussed in the previous chapter, was the effect on the phase due to a lengthening of the individual defect, providing a greater phase shift, but also a greater deterioration in the matched characteristics of the transmission line, illustrated in Figures

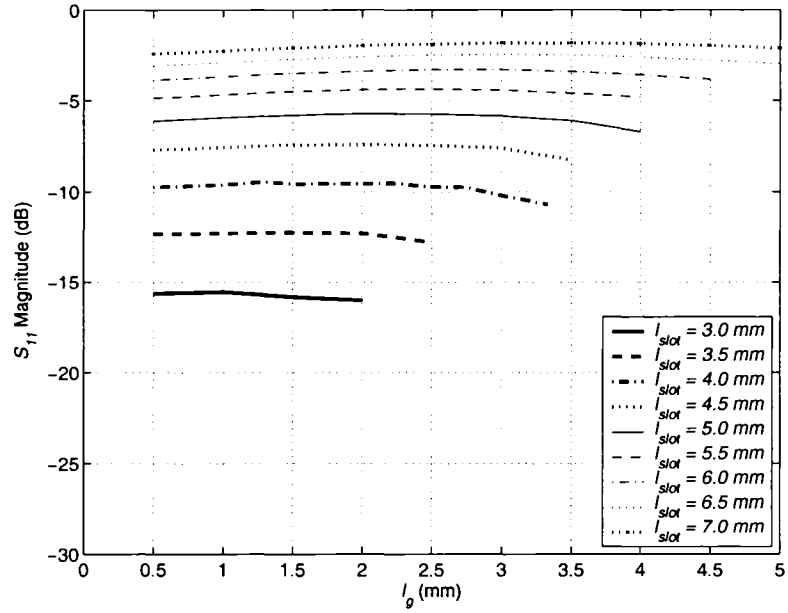
4.11 to 4.13 (a) and (b). In the cases considered in Figures 4.11 to 4.13, the length of the gap is influenced not only by the slot length, but also by the line impedance. Lower system impedance raises the potential upper limit on the gap length, when considering optimal phase. However, ensuring the gap length is selected at less than half the defect length is a safe initial approximation.

Also confirmed in these experiments is the increased level of phase as the impedance level is decreased. Note also that the $\Delta\phi_{21}$ for an individual dumbbell defect approaches 20°, irrespective of the impedance of the line, when the defect has a length that was deemed to be beneficial in terms of return loss, as discussed in Chapter 3, i.e. for l_{slot} = 4.0 mm at 25Ω, l_{slot} = 4.5 mm at 50Ω, and l_{slot} = 6.5 mm at 100Ω.

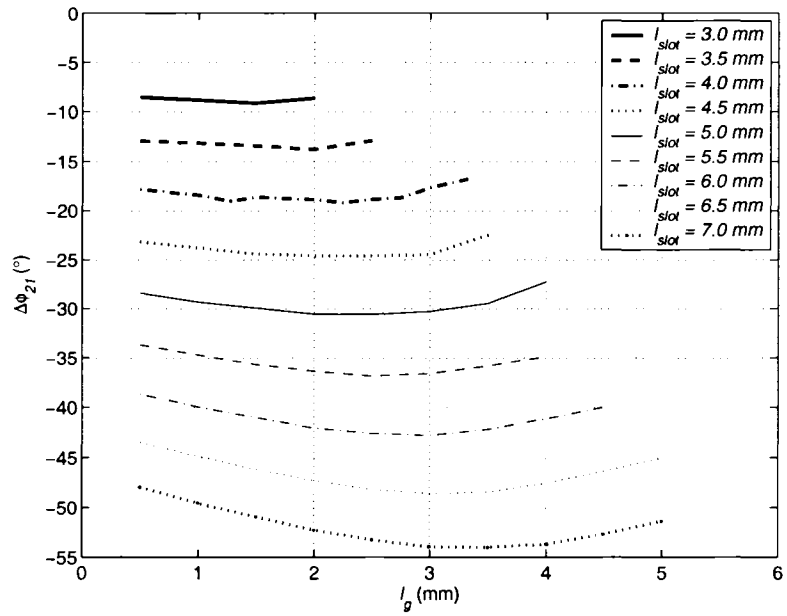


(a)

Figure 4.12: *Z_o = 25Ω; w_{slot} = 0.5 mm, w_g = 0.1 mm; Effect of variable l_g on (a) S_{21} (b) S_{11}, and (c) $\Delta\phi_{21}$ for l_{slot} as indicated.*

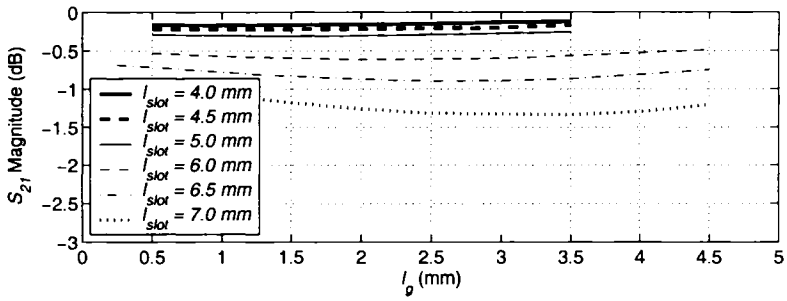


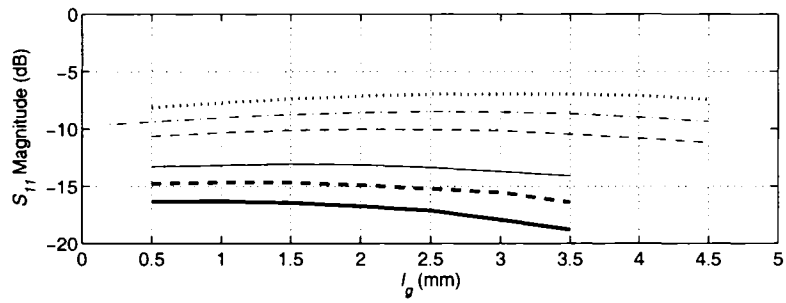
(b)



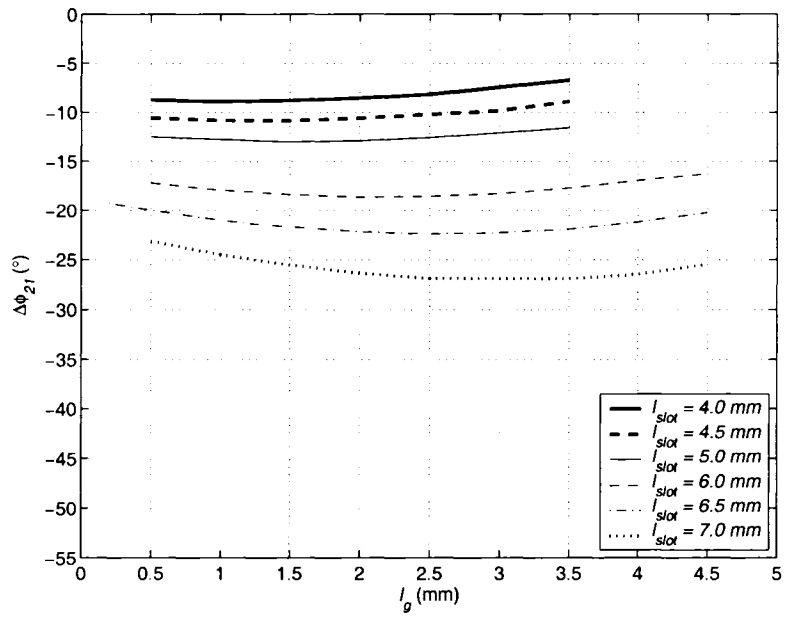
(c)

***Figure 4.12** continued*





(a)



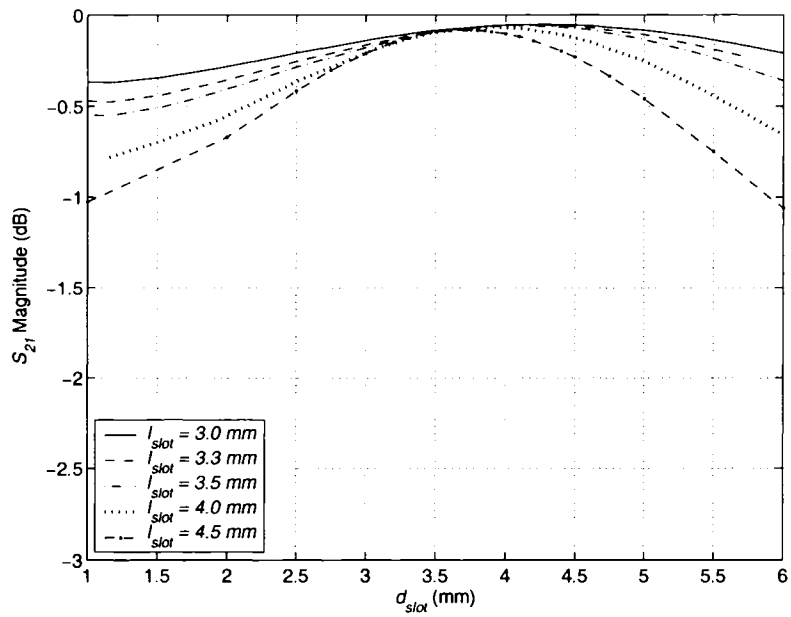
(b)

Figure 4.13: *Z_o = 100Ω; w_{slot} = 0.5 mm, w_g = 0.1 mm; Effect of variable l_g on (a) S_{21}, S_{11}, and (b) $\Delta\phi_{21}$ for l_{slot} as indicated.*

4.5 Paired Elements

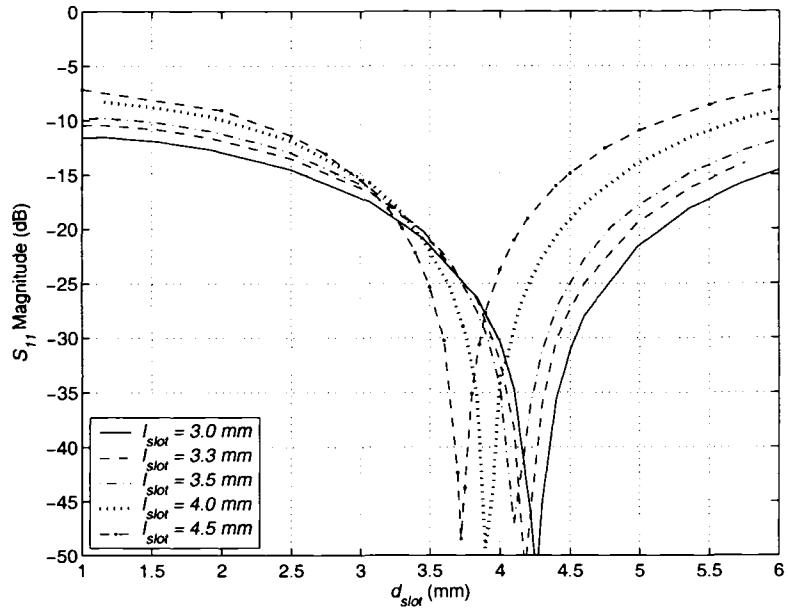
4.5.1 Effect of the Slot Length

As was done in Chapter 3 for uniform slots, this section investigates the performance characteristics of paired dumbbell elements, in particular, the effects of the dumbbell length. Figure 4.14 shows the S_{11}, S_{21}, and $\Delta\phi_{21}$ for select element separations, d_{slot}, for defects having l_{slot} = 3.0, 3.3, 3.5, 4.0, and 4.5 mm, with optimum l_g = 1.5 mm for l_{slot} = 4.5 mm, and l_g = 1.3 mm for l_{slot} = 3.0 to 4.0 mm, determined from data in 4.4. The corresponding results for l_{slot} = 5.0, 5.5, 6.0, 6.5, and 7.0 mm are shown in Figure 4.15, for l_g = 1.75, 1.9, 2.25, 2.65, and 3.1 mm, respectively. Both figures also show the resulting mismatch loss, line loss, and the FOM calculated with respect to insertion and line losses. In all cases the line impedance is 50Ω.

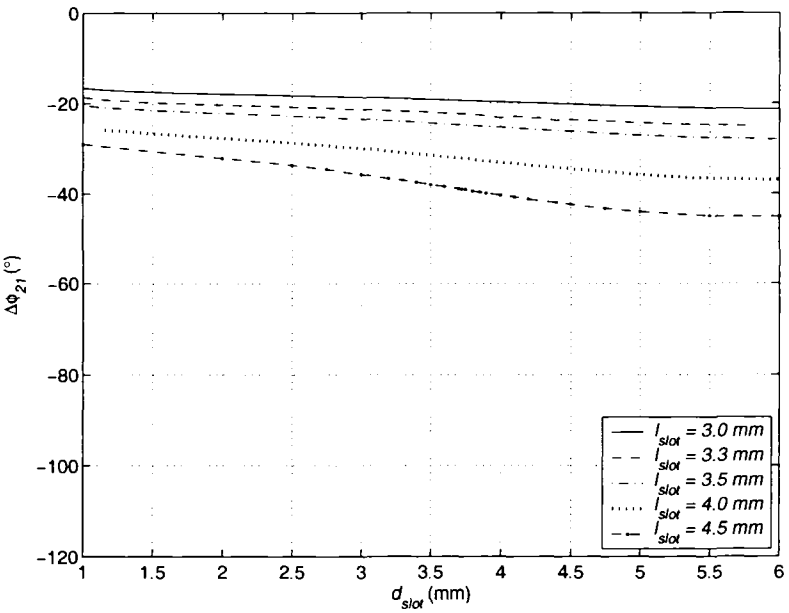


(a)

Figure 4.14: *Paired dumbbell combination for optimal l_g = 1.3 mm, for l_{slot} = 3.0 mm, 3.3 mm, 3.5 mm, 4.0 mm, and l_g = 1.5 mm for l_{slot} = 4.5 mm, with w_{slot} = 0.5 mm, and w_g = 0.1 mm; (a) S_{21}, (b) S_{11}, (c) $\Delta\phi_{21}$, (d) mismatch and line loss, and (e) FOM.*

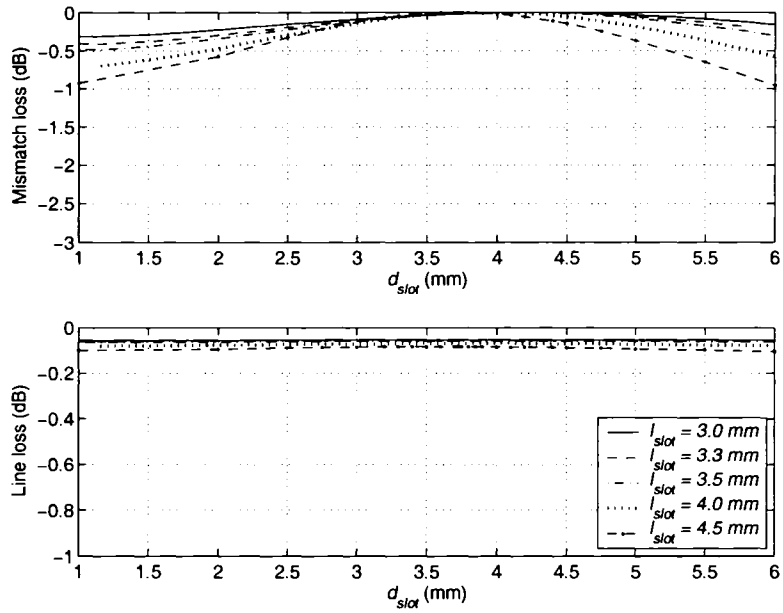


(b)

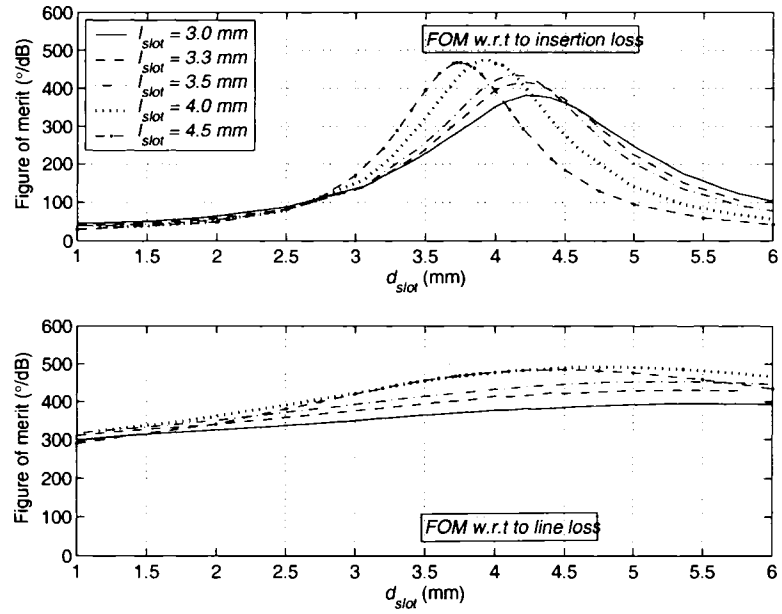


(c)

Figure 4.14 *continued*

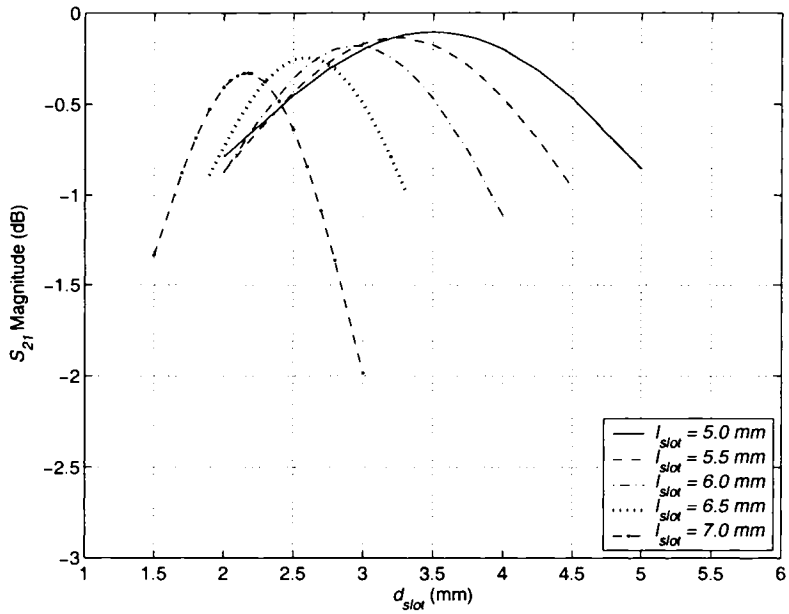


(d)

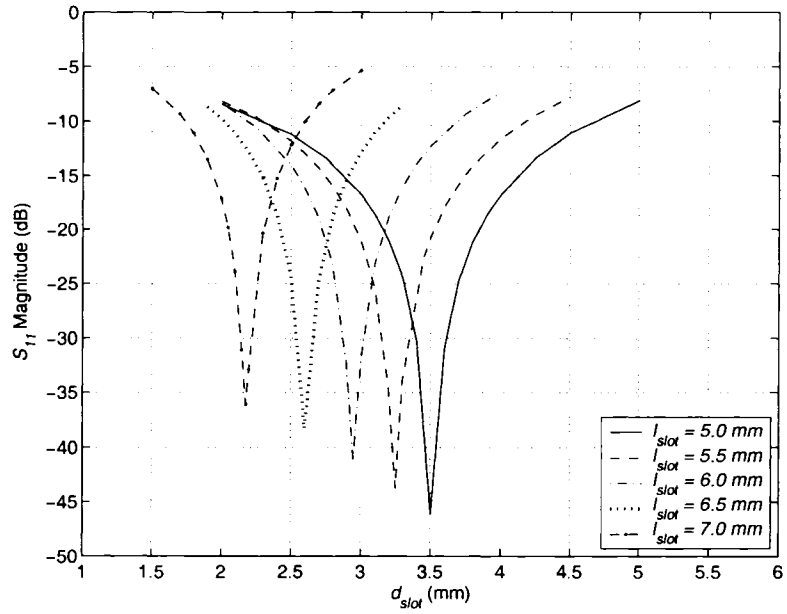


(e)

Figure 4.14 *continued*

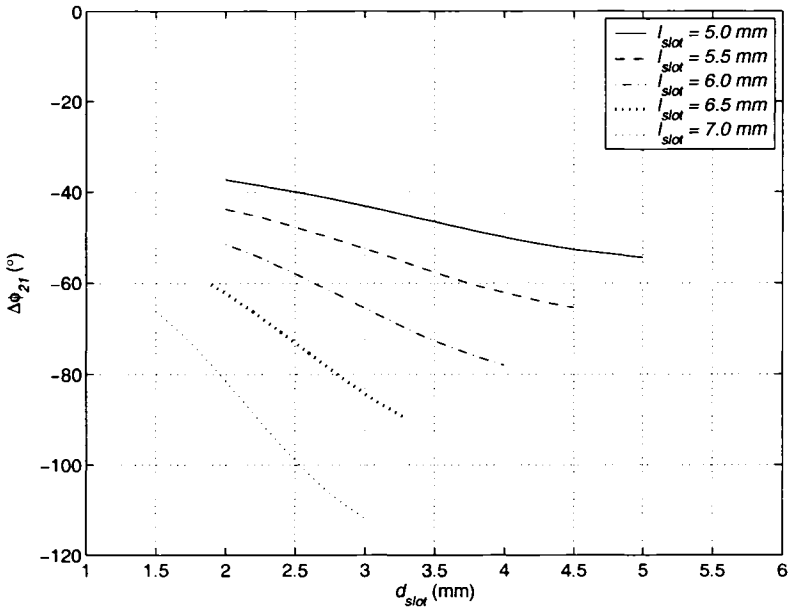


(a)

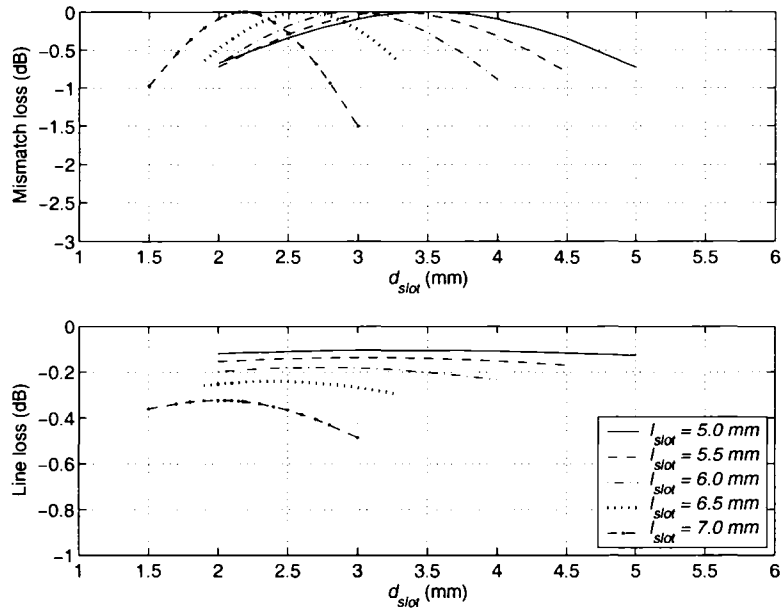


(b)

Figure 4.15: *Paired dumbbell combination for optimal l_g = 1.75, 1.9, 2.25, 2.65, and 3.1 mm for l_{slot} = 5.0 mm, 5.5 mm, 6.0 mm, 6.5 mm and 7.0 mm, respectively, with w_{slot} = 0.5 mm, and w_g = 0.1 mm; (a) S_{21}, (b) S_{11}, (c) $\Delta\phi_{21}$, (d) mismatch and line loss, and (e) FOM.*

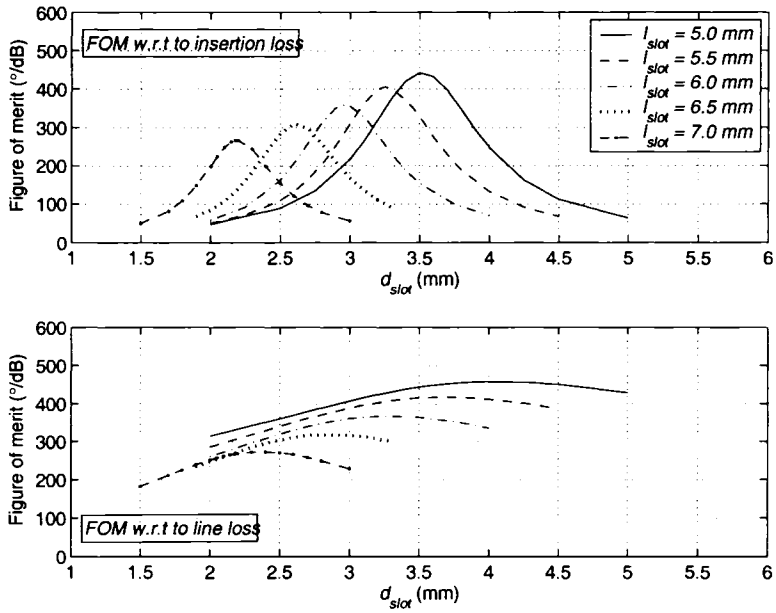


(c)



(d)

Figure 4.15 *continued*



(e)

Figure 4.15 *continued*

As in Chapter 3 for each dumbbell length, there exists an element separation d_{slot} that minimizes the return loss, indicating that the paired element configuration is more suitable for low return loss phase shifter designs. With a matched paired element combination, the insertion loss is primarily due to the line loss, which gradually increases due to the onset of radiation, especially beyond dumbbell lengths of 4.5 mm, and is more than compensated for by the phase shift increase due to the increase in dumbbell length. Consequently, the FOM of the pair maximizes around the dumbbell length of 4.5 mm.

4.5.2 Effect of Gap Length on Paired Elements

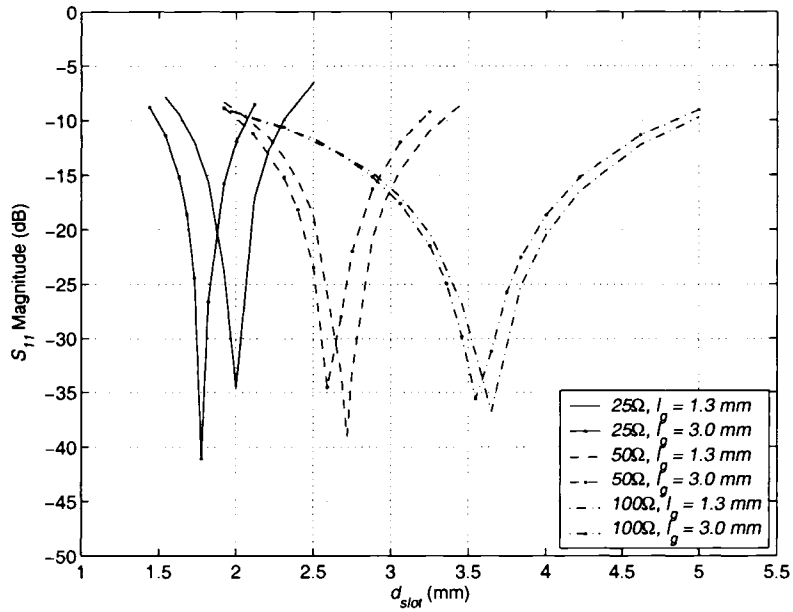
The gap length was originally selected following a brief initial study using a 4.5 mm x 0.5 mm slot, with w_g = 0.1 mm. This study provided only rough information on the necessary length and was slightly biased in the expectation that the gap length would

be most favourable when set to be similar to the dimensional width of the associated transmission line. Thus, the gap length was set at 1.3 mm, identical to the width of the transmission line structure having a 50Ω characteristic impedance.

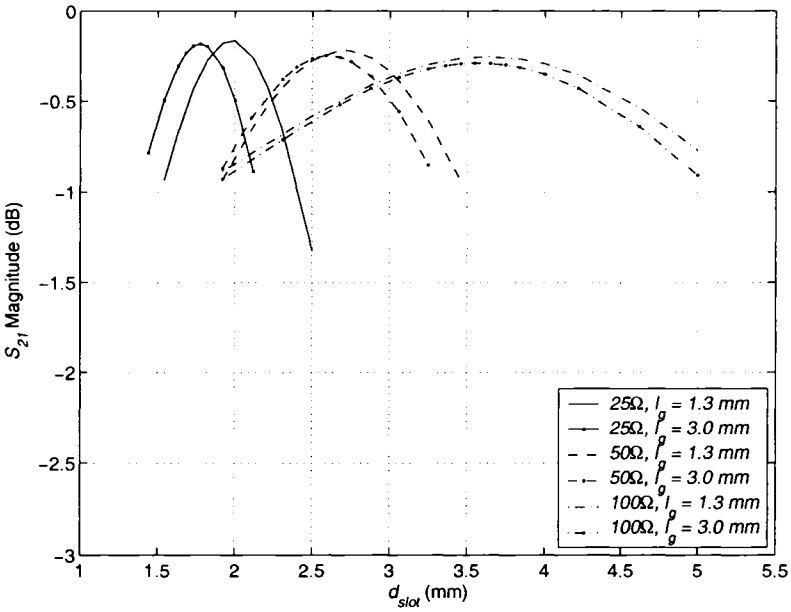
The initial study into the gap length was also limited with regard to the length of the slot. In examining the effect of the gap, only the 4.5 mm slot length was considered. With this limitation to the original study and the existing bias towards the expected result of l_g to mirror the magnitude of w_{line}, simulation studies and fabrication samples presented in the coming sections were implemented with an l_g equivalent to 1.3 mm when operating within a 50Ω system. Nonetheless, this selected gap length for the slot length in question satisfies the relationship of $l_g \leq l_{slot}/2$ to provide an improvement in the differential insertion phase over the original uniform slot.

Intuitively, for the 50Ω, 4.5 mm long slot, an l_g of 1.3 mm versus the optimum l_g of 1.5 mm would not significantly change the outcome of the achieved differential insertion phase. However, in the case of longer dumbbell structures, the difference in the possible $\Delta\phi_{21}$ may not be negligible. The $\Delta\phi_{21}$ documented in Figure 4.11 to 4.13 for l_{slot} = 6.5 mm, indicates that the phase levels at l_g = 1.3 mm are visibly less than those determined for an l_g of 2.5 mm or 3.0 mm, by approximately, 1° for 100Ω, 2° for 50Ω, and almost 4° for 25Ω. In a paired combination, these structures would be deficient by approximately double these respective phase levels.

With this in mind, the 6.5 mm dumbbell was implemented in a paired combination under two distinct scenarios. In the first instance, the gap length was set at 1.3 mm, the original predetermined l_g utilized in the coming sections. This value for l_g is applied to the dumbbell for the impedance levels of 25Ω, 50Ω and 100Ω. Secondly, the dumbbell was re-implemented with l_g set to 3 mm, selected for its advantageous phase levels in Figure 4.12 for the single 6.5 mm dumbbell. These two cases were implemented in respective paired combinations. The S_{11} and S_{21} for both combinations are shown in Figure 4.16 (a) and (b), and the associated differential insertion phase levels in Figure 4.16 (c). Direct comparison of the 100Ω, 6.5 mm dumbbell with the paired uniform 6.5 mm slots of Figure 3.19 indicates an additional phase of up to 10° by the paired dumbbell design over slightly smaller values of d_{slot}.

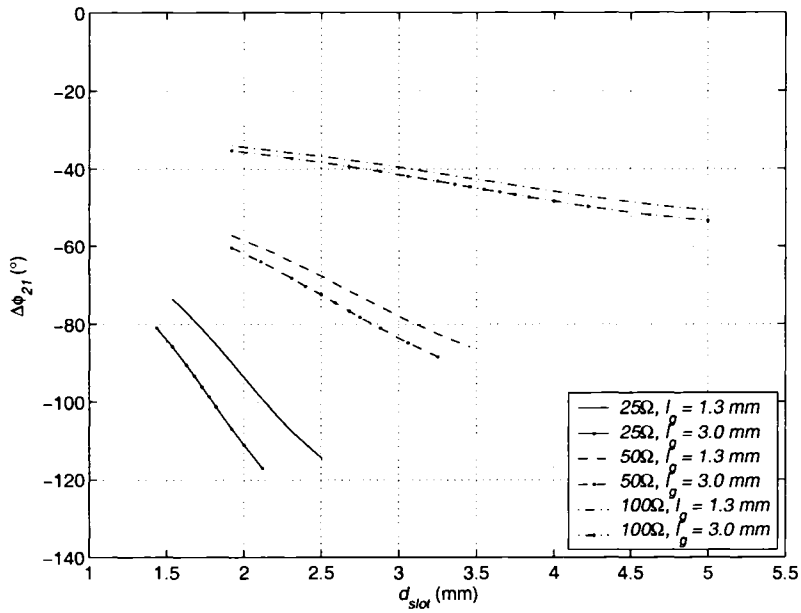


(a)



(b)

Figure 4.16: *Comparison of l_g = 1.3 mm, and l_g = 3.0 mm for paired dumbbell combinations of l_{slot} = 6.5 mm, w_{slot} = 0.5 mm, w_g = 0.1 mm with 25Ω, 50Ω, and 100Ω line characteristic impedance; (a) S_{11}, (b) S_{21}, and (c) $\Delta\phi_{21}$.*



(c)

***Figure 4.16** continued*

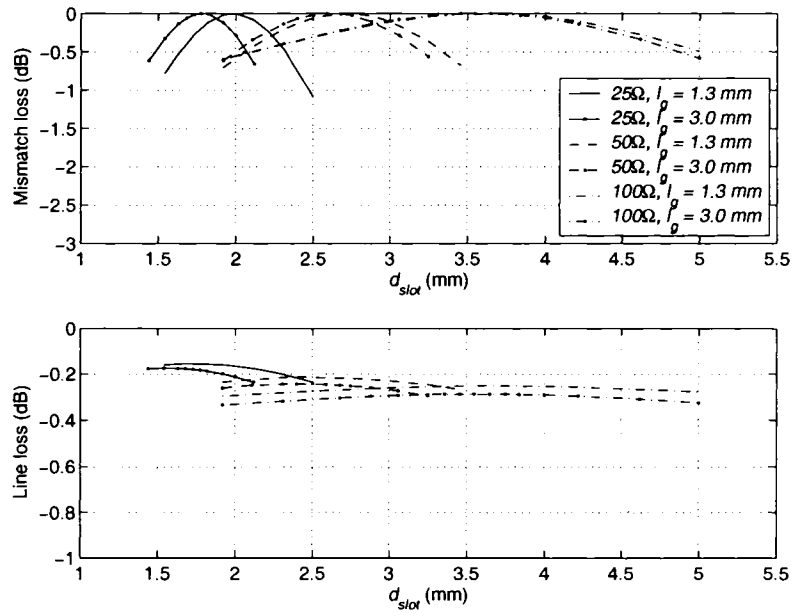
As can be seen in Figure 4.16 (a), while the relationship between the S_{11} and d_{slot} is similar for each respective impedance structure, the dumbbell combinations possessing the larger gap length of 3 mm illustrate that these results are achieved with a reduced element separation. This effect is most pronounced as the impedance is reduced. At 100Ω, the shift in the relationship between the S_{11} and d_{slot} is minimal.

The trends obtained for $\Delta\phi_{21}$ versus the element separation, shown in Figure 4.16 (c), depict increased phase for the l_g = 3.0 mm combination as expected. However, once again the effect is more pronounced with reduced impedance levels. The difference in the phase levels of the paired combinations is approximately 1.2°-2.8° for l_g = 1.3 mm and l_g = 3.0 mm, respectively at 100Ω, 2.5°-5.5° for 50Ω, and a significant 12°-17° for 25Ω. Thus, not only are the phase levels increased by introducing a more attractive magnitude for l_g, i.e. 3.0 mm, miniaturization of the total structure is pushed further as indicated by reduced magnitudes of d_{slot}. With regard to the S_{21} of each structure, the gap

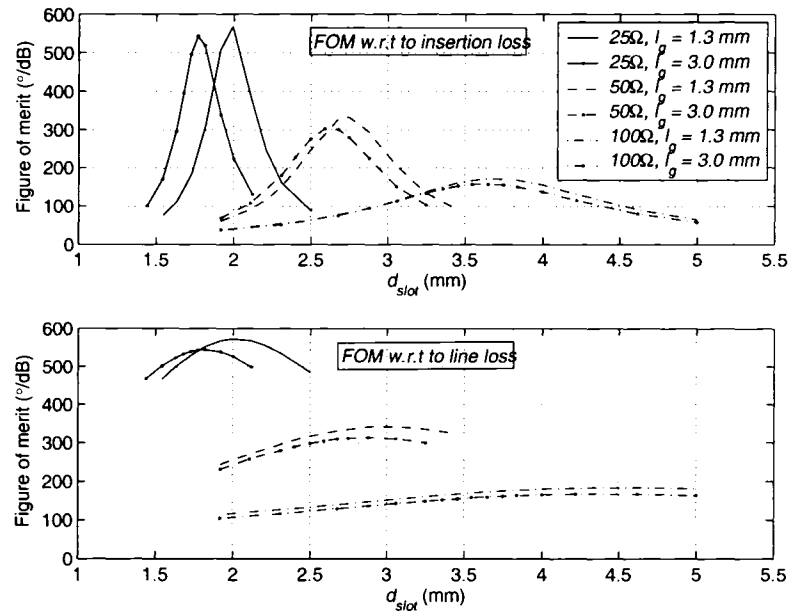
length of 1.3 mm produces peak S_{21} of –0.16 dB, –0.22 dB, and –0.25 dB, for each of the 25Ω, 50Ω, and 100Ω systems, versus –0.18 dB, –0.25 dB, –0.29dB with l_g = 3.0 mm. Higher losses overall are to be expected as the system impedance rises. The S_{21} at the limits of d_{slot} for an S_{11} of –10 dB, hover in and around –0.6 dB to –0.8 dB.

The results provided in Figure 4.16 detail the significant effect that the gap length can introduce on the phase and the size of the overall structure, as additional defect elements are added to increase the overall phase. In considering the higher impedance levels of 50Ω and 100Ω, the additional phase obtained by utilizing l_g = 3.0 mm for the 6.5 mm slot is recognized, but can also be comfortably interpreted to suggest that these systems provide a more robust environment for fabrication. This conclusion can also be inferred from the S_{11} and S_{21} results in Figure 4.10 for the 4.5 mm long dumbbell within the 50Ω system. While the paired dumbbell structure was shown to provide greater phase when compared directly to the paired uniform slot, identical S_{11} and S_{21} magnitudes were achieved for both the dumbbell and uniform slot combinations. Therefore, for higher impedance structures, the overall effect on the phase and *S*-parameter magnitudes is less significant if the etch of the gap length, and/or the element separation is slightly inaccurate. This may be inferred from Figure 4.17 detailing the mismatch loss, line loss, and in particular the figure of merit calculated with respect to these two loss components.

The above conclusion may not prove to be the case with lower impedance systems, such as that demonstrated by the 25Ω traces in Figure 4.16. Selecting 1.3 mm for l_g rather than 3.0 mm had a significant effect on the circuit size, requiring a larger element spacing to achieve a lesser degree of phase. A loss of 12°-17° in potential phase, would be significant when considering an application that utilizes a four- or five-bit digital phase shifter whose reference bit level is 22.5° and 11.25°, respectively. The structures yet to be introduced in the following chapter utilize slot lengths from 3 to 7 mm, with fabricated designs having slots of 3.5 to 5 mm long, all within a 50Ω system. However, with these fabricated designs, a gap length of 1.3 mm satisfies the requirement of $l_g \leq l_{slot}/2$.



(a)



(b)

Figure 4.17: *Comparison of l_g = 1.3 mm, and l_g = 3.0 mm for paired dumbbell combinations of l_{slot} = 6.5 mm, w_{slot} = 0.5 mm, w_g = 0.1 mm with 25Ω, 50Ω, and 100Ω line characteristic impedance; (a) Mismatch loss and line loss, and (b) figure of merit.*

4.6 Equivalent Circuit Approximation Design Rules

In the previous sections, full wave analysis using Ansoft Ensemble 8.0 was used to determine the characteristics of the dumbbell defect below the transmission line. A great deal was learned regarding the performance of this defect geometry as a circuit element to design a phase shifter, in terms of the influence of the gap dimensions and the full structural parameters of the dumbbell. In this section, an equivalent circuit of the structure is developed and discussed. The results are then used to determine an approximate, but efficient method for phase shifter or other circuit designs. This analysis is also applicable to the uniform slot as it is essentially a special case of the dumbbell.

4.6.1 Single Element Circuit Approximation

By etching a defect in the ground plane of the transmission line, an additional reactive component is introduced to the transmission line system. The exact electromagnetic solution of the structure was obtained through simulation in previous sections, while the equivalent circuit method to be discussed in this section is presented as an approximate solution. In the literature discussed in section 3.2, the equivalent circuit of the dumbbell structure has been compared to a parallel *LC* circuit, or a low-pass filter, as shown in Figure 4.18 (a). The parameter extraction of a dumbbell equivalent circuit has been explored by Ahn and Park *et al.* [74], further detailed in [90] by Park with discussion regarding fringing capacitance of the structure, and outlined in a similar fashion in [91] by Liu *et al.* with consideration given to the radiation resistance of the structure. In all cases, the analysis of the structure is carried out initially through field analysis with a commercial simulator. In [74], the defected ground structure is proposed for use as low-pass filter, whose simulation result can be matched to the response of a one-pole Butterworth filter. The parallel *LC* circuit is modelled as a series reactive element, shown in Figure 4.18 (b), represented by the prototype element value, g_1, provided in Matthaei *et al.* [92]. Prototype element values g_0 and g_2 represent the normalized input and output port impedances.

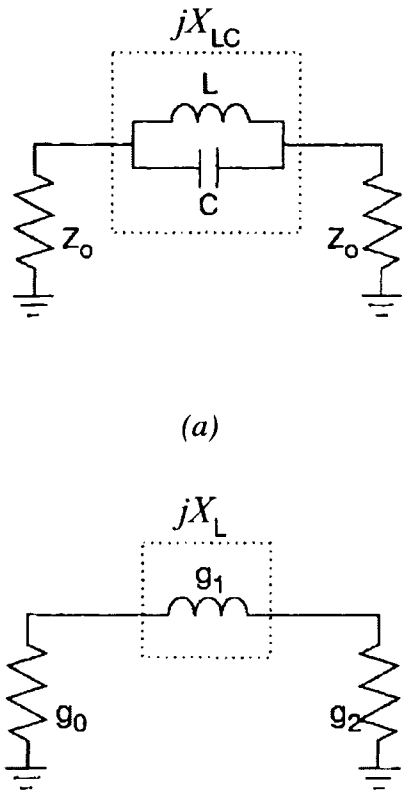


Figure 4.18: *(a) Proposed equivalent circuit; (b) one-pole prototype low-pass filter circuit [74].*

A parallel resistive element R is commonly used to represent the losses in the system for a parallel circuit, whose impedance is expressed as,

$$Z = \left(\frac{1}{R} + \frac{1}{j\omega L} + j\omega C \right)^{-1} \tag{4.1}$$

For the slot defect, the loss is primarily due to radiation, which below resonance is negligible. The resonant frequency of the circuit is defined when the combined inductive reactance and capacitive susceptance is zero. The angular resonant frequency, ω_0, is therefore expressed as,

$$\omega_o = \frac{1}{\sqrt{LC}} \tag{4.2}$$

The impedance of the reactive element, Z_{LC}, in Figure 4.18 (a) may be written as,

$$Z_{LC} = \frac{j\omega L}{1-\omega^2 LC} \tag{4.3}$$

Using the relationship for L and C at resonance from (4.2), and the impedance of the reactive element in (4.3), the series reactance, X_{LC}, may be expressed as,

$$X_{LC} = \frac{\omega}{C}\frac{1}{\omega_o^{\,2} - \omega^2} \tag{4.4}$$

To utilize the equivalent circuit approximation proposed in [73], the reactance of the parallel LC structure must be equated to the series inductance of the Butterworth one-pole prototype. The normalized series reactance, X_L', of the prototype Butterworth filter may be expressed as [92],

$$X_L^{'} = \omega' L' \tag{4.5}$$

where ω' is the normalized angular frequency, and L' is the normalized inductance of the filter. In the initial prototype of the Butterworth filter, the impedance elements are normalized to unity. The transformation of the inductance from its normalized value is achieved as follows [74], [92],

$$L = Z_o L' = Z_o g_1 \tag{4.6}$$

where g_1 is the Butterworth prototype and has a value of 2 for a one-pole attenuation filter [92]. It is necessary to scale the frequency dependence of the filter by $1/\omega_c$, where ω_c is the angular cutoff frequency, to transform the cutoff frequency from its normalized value of unity, to ω_c. Thus, substituting ω/ω_c for ω in (4.5) and applying (4.6), the transformed series reactance becomes,

$$X_L = \frac{\omega Z_o g_1}{\omega_c} \tag{4.7}$$

At cutoff, (4.4) is equivalent to (4.7) [74],

$$X_{LC}\Big|_{\omega=\omega_c} = X_L\Big|_{\omega=\omega_c} = Z_o g_1 \tag{4.8}$$

Thus, using (4.8) with (4.4), the capacitance of the proposed equivalent circuit becomes,

$$C = \frac{\omega_c}{Z_o g_1} \frac{1}{\omega_o^2 - \omega_c^2} \tag{4.9}$$

The inductance of the circuit can then be extracted, knowing the capacitive value of the equivalent circuit, using (4.2),

$$L = \frac{1}{\omega_o^2 C} \tag{4.10}$$

Upon obtaining the *S*-parameters through simulation of the dumbbell structure, it is thus possible to extract the inductive and capacitive components using the proposed equivalent circuit procedure outline in [74], assuming a 3dB cutoff frequency in the passband, and knowing the frequency of the attenuation pole in the stopband. This procedure, summarized in (4.1) to (4.10) was applied to the dumbbell structure introduced in this chapter, recognizing that the simulation results illustrated in the pages to follow are similar to that of a maximally-flat, low-pass filter when considering frequencies above the defect design frequency of interest.

4.6.1.1 Influence of the Gap Width and Length

As can be seen from the data summarized in Table 4.1, and shown in Figure 4.19, as the gap width is increased, both the cutoff and attenuation pole frequencies, f_o and f_c, gradually rise. The increase in the gap width causes an increase in both the structure inductance and capacitance, but has a greater significance on C as the frequency range from cutoff to attenuation also increases. The overall effect of decreasing w_g, for a dumbbell of w_{slot} = 0.5 mm and l_{slot} = 6.0 mm, is to render the equivalent impedance Z_{LC} as defined in (4.3) of the dumbbell increasingly inductive.

While w_g increases f_o and f_c, the effect of l_g is to lower the cutoff and attenuation pole frequencies as l_g increases in magnitude, as shown in Figure 4.20. The change in L and C then varies accordingly, with the rise in C more significantly affected than the resulting drop in the L, shown in Table 4.2 for select values of l_g. Thus, the gap region below the transmission line largely influences the capacitive component of the suggested equivalent circuit. The overall effect of increasing l_g, for a dumbbell of w_{slot} = 0.5 mm,

and l_{slot} = 6.0 mm, is to render the reactance of the dumbbell increasingly inductive, as summarized by Z_{LC} in Table 4.2.

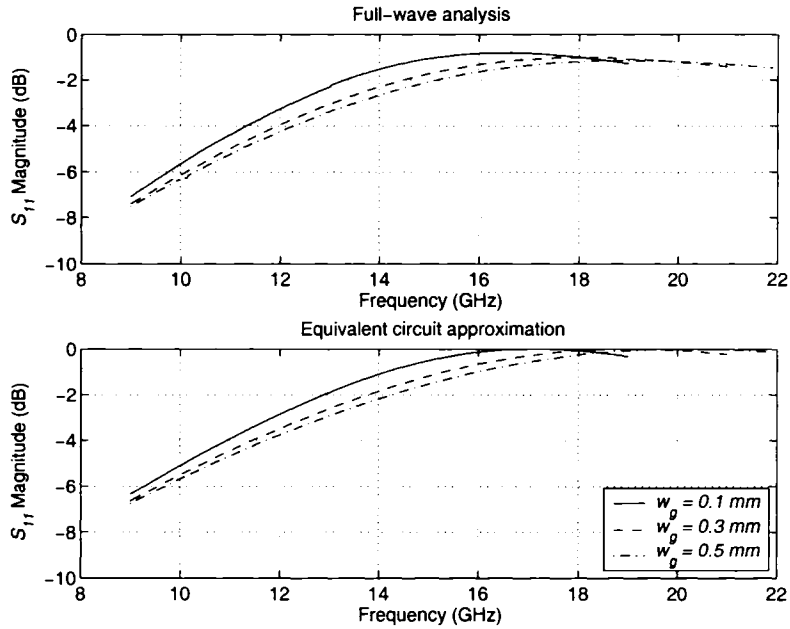
The S_{11} and S_{21} of the equivalent circuit approximations obtained using (4.2) to (4.4) are given in Figures 4.19 and 4.20 with their associated dumbbell structure. With variable w_g, l_g was constant at 1.3 mm, while for variable l_g, w_g was constant at 0.5 mm. Circuit simulations in this and the coming section were obtained using Ansoft Designer.

Table 4.1: *Summary of f_c, f_o, capacitance and inductance with regard to w_g; l_{slot} = 6 mm, w_{slot} = 0.5 mm, l_g = 1.3 mm.*

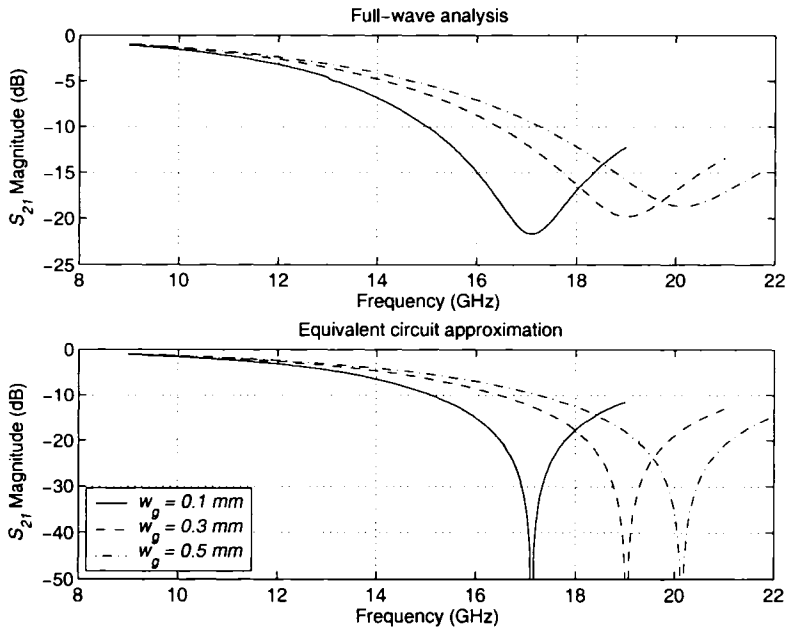
w_g (mm)	f_c (GHz)	f_o (GHz)	C (pF)	L (nH)	Z_{LC} (Ω)
0.1	11.84	17.12	0.12324	0.70128	j66.8
0.3	12.52	19.04	0.09684	0.72153	j62.6
0.5	12.88	20.16	0.08522	0.73130	j60.9

Table 4.2: *Summary of f_c, f_o, capacitance and inductance with regard to l_g; l_{slot} = 6 mm, w_{slot} = 0.5 mm, w_g = 0.1 mm.*

l_g (mm)	f_c (GHz)	f_o (GHz)	C (pF)	L (nH)	Z_{LC} (Ω)
0.50	12.28	18.56	0.10091	0.72869	j64.51
1.30	11.84	17.12	0.12324	0.70128	j66.88
2.00	11.52	16.24	0.13993	0.68637	j69.46

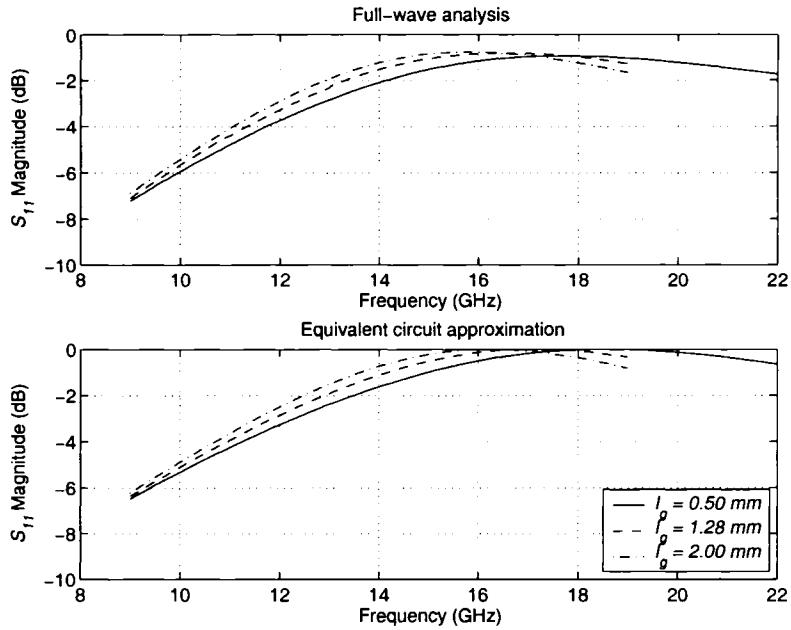


(a)

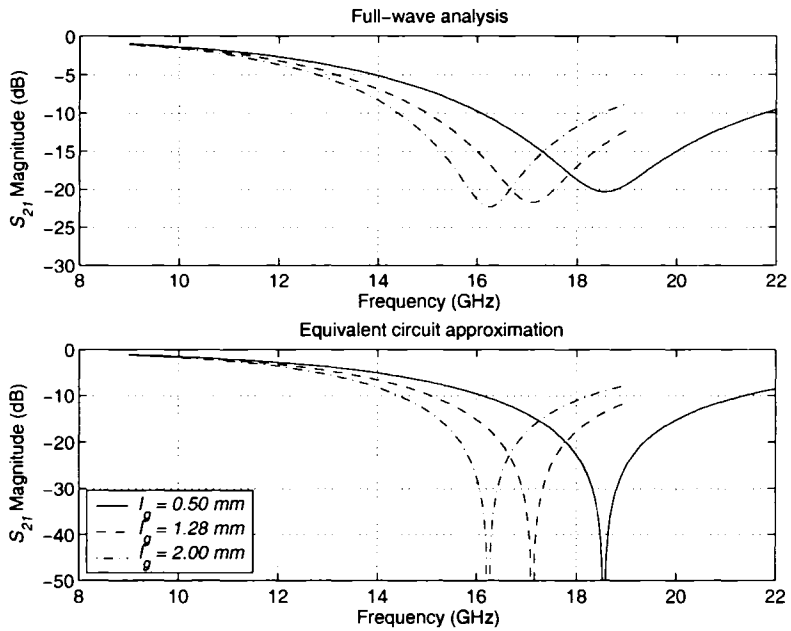


(b)

Figure 4.19: *Comparison of w_g; l_{slot} = 6 mm, w_{slot} = 0.5 mm, l_g = 1.3 mm. (a) S_{11}, top plot = full-wave analysis, bottom plot = equivalent circuit approximation (b) S_{21}, top plot = full-wave analysis, bottom plot = equivalent circuit approximation.*



(a)



(b)

Figure 4.20: *Comparison of l_g; l_{slot} = 6 mm, w_{slot} = 0.5 mm, w_g = 0.1 mm. (a) S_{11}, top plot = full-wave analysis, bottom plot = equivalent circuit approximation (b) S_{21}, top plot = full-wave analysis, bottom plot = equivalent circuit approximation.*

4.6.1.2 Influence of the Overall Structural Width and Length

While the gap length and width had a more significant effect on the capacitive component C of the defect structure, the slot length and width indicate a greater significance on the inductive component L of the structure. Increases in both the w_{slot} and l_{slot} produce a drop in the respective cutoff and attenuation frequencies, f_o and f_c, as detailed in Tables 4.3 and 4.4. For both w_{slot} and l_{slot}, the effect of increasing each respective dimension is to render Z_{LC} of the structure increasingly inductive.

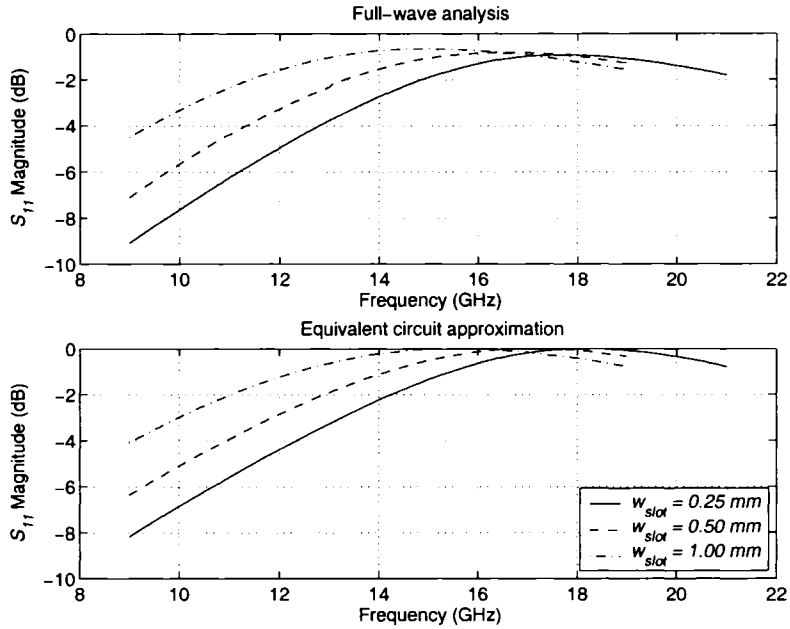
Figures 4.21 and 4.22 show the S_{11} and S_{21} magnitudes of the dumbbell structure, for the select cases of w_{slot} and l_{slot} indicated in Tables 4.3 and 4.4 respectively, and their associated equivalent circuit approximations obtained using (4.2) to (4.4). When investigating w_{slot}, l_{slot} was constant at 6.0 mm. As l_{slot} was varied from 4.5 mm to 6.0 mm, w_{slot} was 0.5 mm. Gap parameters, w_g and l_g, were constant at 0.5 mm and 1.3 mm, respectively.

Table 4.3: *Summary of f_c, f_o, capacitance and inductance with regard to w_{slot}; l_{slot} = 6 mm, w_g = 0.1 mm, l_g = 1.3 mm.*

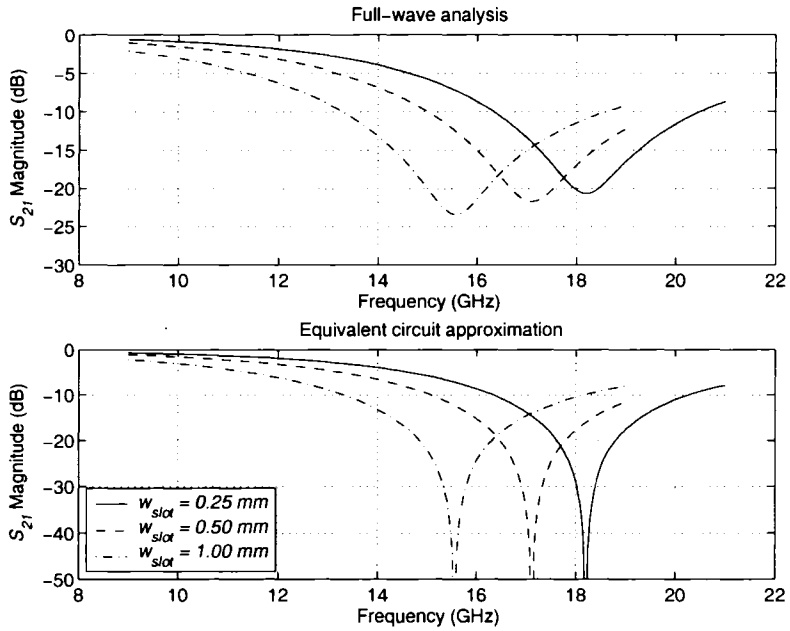
w_{slot} (mm)	f_c (GHz)	f_o (GHz)	C (pF)	L (nH)	Z_{LC} (Ω)
0.25	13.24	18.20	0.13153	0.56592	j50.36
0.50	11.84	17.12	0.12324	0.70128	j66.88
1.00	9.96	15.56	0.11092	0.94321	j100.96

Table 4.4: *Summary of f_c, f_o, capacitance and inductance with regard to l_{slot}; w_{slot} = 0.5 mm, w_g = 0.1 mm, l_g = 1.3 mm.*

l_{slot} (mm)	f_c (GHz)	f_o (GHz)	C (pF)	L (nH)	Z_{LC} (Ω)
4.5	15.36	21.68	0.10443	0.51606	j41.19
5.0	13.88	19.88	0.10906	0.58769	j49.40
6.0	11.84	17.12	0.12324	0.70128	j66.88

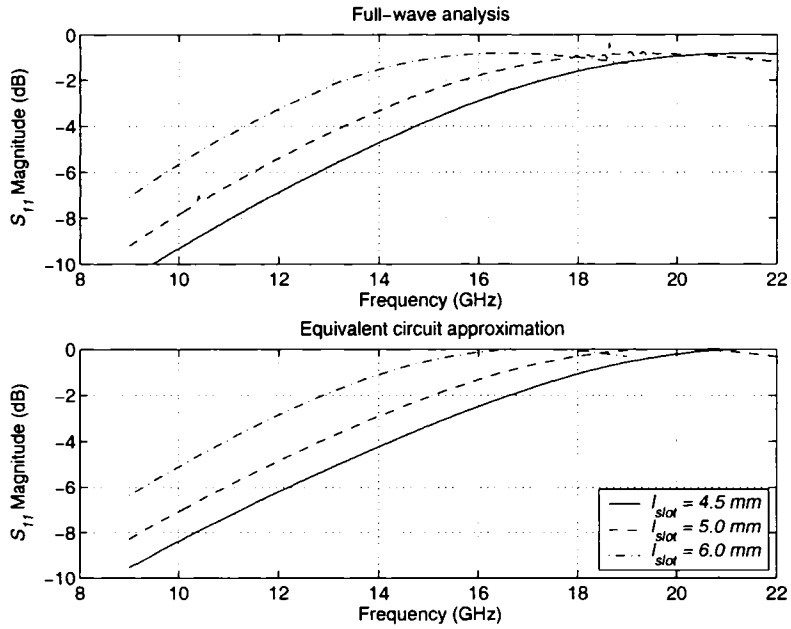


(a)

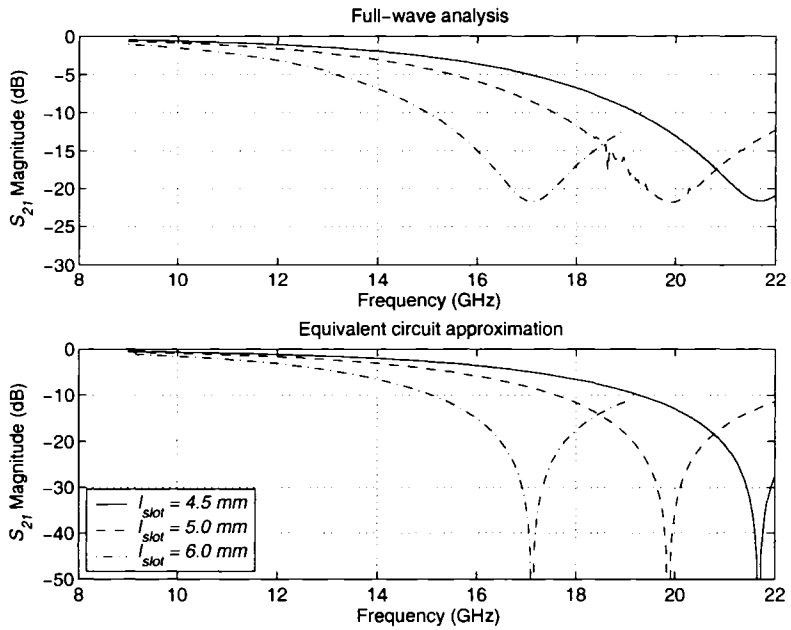


(b)

Figure 4.21: *Comparison of w_{slot}; l_{slot} = 6 mm, w_g = 0.1 mm, l_g = 1.3 mm. (a) S_{11}, top plot = full-wave analysis, bottom plot = equivalent circuit approximation (b) S_{21}, top plot = full-wave analysis, bottom plot = equivalent circuit approximation.*



(a)



(b)

Figure 4.22: *Comparison of l_{slot}; w_{slot} = 0.5 mm, w_g = 0.1 mm, l_g = 1.3 mm. (a) S_{11}, top plot = full-wave analysis, bottom plot = equivalent circuit approximation (b) S_{21}, top plot = full-wave analysis, bottom plot = equivalent circuit approximation.*

4.6.2. Paired Defect Elements

The equivalent circuit can be used to investigate more complex defect networks. The paired defect is a special case where two elements are separated by a length d_{slot}. When such a pair is placed below a transmission line of impedance Z_o, the equivalent circuit is then a cascade of the defect, separated from its pair by a transmission line of Z_o and length d_{slot}, terminated at both ends by ports of impedance Z_o, as shown in Figure 4.23. The input impedance, Z_{in}, of the cascaded circuit is given by,

$$Z_{in} = Z_{LC} + Z_o \frac{(Z_o + Z_{LC}) + jZ_o \tan(\beta d_{slot})}{Z_o + j(Z_o + Z_{LC})\tan(\beta d_{slot})} \tag{4.11}$$

where Z_{LC} is the defect impedance of (4.3), and β is the propagation constant of the transmission line, expressed in (3.3). The impedance in (4.11) is in series with the transmission line of impedance Z_o. Thus, for an optimum impedance match, Z_{in} should be equal to Z_o. This provides an equation for the unknown inter-defect spacing d_{slot}.

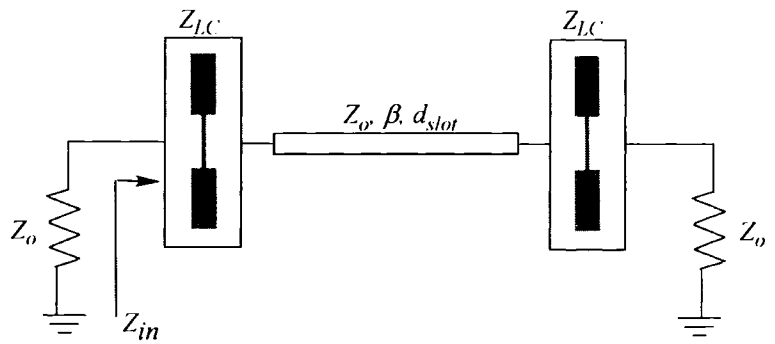


Figure 4.23: *Equivalent circuit of a paired defect configuration.*

As an example, for a defect element of l_{slot} = 4.5 mm, w_{slot} = 0.5 mm, w_g = 0.1 mm and l_g = 1.5 mm, the equivalent capacitance and inductance, extracted using the method detailed in 4.6.1, are 0.111 pF, and 0.516 nH, respectively. Thus, Z_D at 10 GHz is j41.8 Ω. For Z_o = 50 Ω, ε_r = 3, and h = 0.508 mm, the microstrip line β is 325.61 rad/m. Solving for $\tan(\beta d_{slot})$, by equating (4.11) with 50Ω, gives $\tan(\beta d_{slot})$ = 2.5. Thus, d_{slot} becomes 3.66 mm. The value obtained via full-wave analysis simulation in Figure 4.10 is 3.75 mm, and is in close agreement with the circuit approximation.

4.7 Conclusions

In this chapter, defect geometry in the form of a dumbbell was investigated, which provided additional geometrical parameters for optimization. Detailed investigation indicated that the gap width and length below the transmission line were influential in increasing the insertion phase of the individual element. The parametric study also showed that the gap length for maximizing the phase shift is dependent on the line impedance. For a 25Ω line, it was nearly half of the slot length, and decreased as the line impedance increased. The paired dumbbell defects were studied as matched elements, and their FOM determined. For three different line impedances of 25Ω, 50Ω and 100Ω, in Figure 4.17, the FOMs computed using the insertion losses were 563°/dB, 393°/dB and 173°/dB, respectively. These results are not necessarily optimum, but are representative of the cases studied. In comparison with the uniform slot cases of Chapter 3, these FOMs are higher for the first two lines. The circuit model, consisting of a parallel combination of inductance and capacitance, was presented for single element defects and extended for paired element configurations.

CHAPTER 5

PHASE SHIFTERS USING DEFECTED GROUND STRUCTURES

Chapters 3 and 4 investigated the phase shifting properties of uniform and dumbbell type ground defects. The phase shift requirements of phased arrays, and difficulties in generating continuous beam scan using discrete phase steps are discussed briefly in this chapter. A novel loaded line phase shifter is proposed for implementation with the defected ground elements. To demonstrate the feasibility of the beam scanning using such phase shifters, two three-element microstrip patch phased arrays are designed and investigated in two separate manners. In the first, which is the reference array, the input signals are applied with the required phased shifts to initiate the beam scan. In the second design, the defected ground phase shifting elements are introduced below the microstrip patch feed lines to cause the required phase shifts. The array radiation patterns are obtained, and the beam scan results compared with those of the reference array. Data presented in this chapter includes results compiled through simulation using Ansoft Ensemble 8.0, as well as fabrication and measurement of select design prototypes.

5.1 Phase Progression Along a Linear Array

A brief discussion concerning the phase progression along a linear array is presented in this section. Characteristics common to arrays such as grating lobes, nulls, sidelobe levels, etc. will not be discussed here. The reader will be referred to references [94] and [18] for further discussion on these topics.

The electric far-field radiation $\boldsymbol{E}$, of an N-element linear array can be expressed by the product of the far-field of a single radiator usually positioned at the origin of a reference axis and the array factor of that array [93],

$$\boldsymbol{E}(\text{total}) = \boldsymbol{E}[(\text{single element at a reference point})]\times[\text{array factor}] \quad (5.1)$$

The geometry of the array, the phase progression between the array elements, the relative element magnitudes, and finally the total number of these elements govern the final expression of the array factor

For simplicity, a linear array of uniform amplitude and spacing shall be considered having N isotropic radiators, i.e. "an array of identical elements all of identical magnitude and each with a progressive phase" [93]. In this case, the array factor can be given as [18], [94],

$$AF = \sum_{n=1}^{N} a_n e^{j(\psi_n - k(n-1)d\sin\theta_o)} \quad (5.2)$$

where a_n is the array element amplitude, $k = 2\pi/\lambda_o$ is the free space wavenumber, d is the array element spacing, and θ_o is measured from the direction normal to the array, with the element phase taper or phase progression ψ_n, of each radiator n, expressed as,

$$\psi_n = -nkd\sin\theta_o \quad (5.3)$$

Thus, from (5.2) the phase of an element n leads the phase of element n+1 by some value of $\Delta\psi = \psi_n - \psi_{n+1}$.

The phase progression represents the phase shift between two successive array elements, i.e.

$$\psi = -kd\sin\theta_o \quad (5.4)$$

which when appropriately selected enables the proper scanning of the array beam to the desired direction of θ_o. The array factor of (5.2) is at a maximum when the array elements are all in phase with each other, and under this condition, maximum radiation is directed towards θ_o,

$$\theta_o = \sin^{-1}\left(-\frac{\psi}{kd}\right) \quad (5.5)$$

As an example, for the special cases of broadside (θ_o = 0°) and end fire radiation (θ_o = 90°), $\psi = 0$ and $\psi = \pm kd$, respectively.

Assuming that the array radiators are known, in order to orient the direction of the main beam to a desired location, the phase progression of the array factor, as well as the element separation, must be judiciously determined. An increasingly large array of n radiating elements will require an increasingly large ψ_n for each subsequent radiator to achieve the necessary θ_o. As an example, with a simple four-element array (n = 4) with an element separation of $d = \lambda/2$, the phase progression necessary at each radiator to achieve a scan of the beam peak towards θ_o = 10° are as follows: ψ_1 = –31.26°, ψ_2 = –62.52°, ψ_3 = –93.78°, and ψ_4 = –125.04°. The single defect elements examined in Chapters 3 and 4 would not provide enough phase shift to satisfy the element phase requirements of this particular example. However, the multiple defect structures can be designed to produce the desired larger phase values.

5.2 Digital Phase Shifting

With digital phase shifters, discrete values are applied on the order of one, two, three, four, or five bits, i.e. 180°, 90°, 45°, 22.5°, or 11.25°, respectively. Four-bit digital phase shifters are the most commonly implemented, but increased phase accuracy can be achieved, as the phase increment is made finer by increasing the bit level, usually at the expense of cost.

Digital phase shifters impose on a signal introduced at their input, a phase change, that is apparent once the signal is output from the phase shifter. This change in phase is expressed by [94],

$$V_o = V_i e^{j\psi} \tag{5.6}$$

where V_o is the signal output, V_i is the signal input and ψ is the phase state. The number of phase states of the phase shifter, expressed by 2^J where J is the number of bits, is dependent on the bit configuration that is selected for implementation. For example, a four-bit digital phase shifter has,

$$2^J = 2^4 \text{ or} 16 \text{ phase states} \tag{5.7}$$

The number of phase states thus defines the phase increment. Therefore, for a four-bit digital phase shifter, the 16 phase states progress with an increment of,

$$i.e. \frac{360}{2^4} = 22.5° \tag{5.8}$$

where 22.5° is the least phase available by the phase shifter and corresponds to one-bit of the phase shifter. They include 0°, 22.5°, 45°, 67.5°, 90°, ..., up to 337.5°.

A disadvantage of digital phase shifters is the limitation of the beam scan step size. For the specific purpose of scanning to a desired θ_o, phase states must be appropriately selected to minimize the phase error of the beam. Only an approximation to the desired phase is possible, as the discrete nature of the digital phase shifter provides a staircase progression in phase along the array. As an example, using equation (5.4) with two adjacent array elements located a half wavelength apart, to achieve a $\theta_o = 25°$, the inter-element phase shift between these two elements needs to be 76.07°. With a four-bit digital phase shifter, phase states of 67.5° or 90° are closest to the required progression, but it would be most prudent to select the 67.5° state over 90° to minimize the phase error initiated using discrete phase states. A five-bit digital phase shifter would introduce a lesser phase error than the lower four-bit system. Thus, a disadvantage of using digital phase shifters is the precision of the beam scan, as each phase state is separated from the next possible state by a phase increment equivalent to the least significant bit of the digital phase shifter. With a four-bit phase shifter, the lowest phase state (other than 0°) is $\psi = 22.5°$, which has the capability to introduce a minimum step size of $\theta_o = 7.18°$. With the five-bit case, $\theta_o = 3.58°$ is possible. These discrete phase steps of digital phase shifters cause beam pointing errors in phased arrays, which are known as the quantization error.

Quantization error from digital phase shifters can be reduced by sophisticated beam forming algorithms [94]. Techniques have been developed to establish finer scan steps, while still utilizing the technology of digital phase shifters. However, a significant limitation in their use is that they offer only fine beam scanning for very large arrays. With small array antennas, such as those applied for use with smart antennas, a switching algorithm to fine tune the activation of digital phase shifters cannot be used to overcome

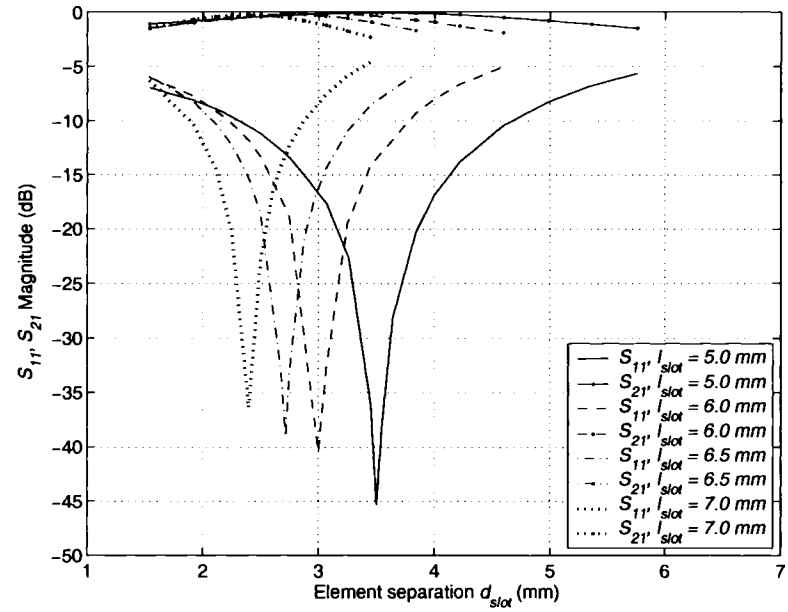
the phase error using discrete digital phase shifting. Rather, analog phase shifters are necessary to implement the desired phase when a lesser number of radiating elements exists in the array. Utilizing analog phase shifting allows the phase shifter to be set to the desired phase with minimal to no phase error.

5.3 Phase Shifter Bit Generation

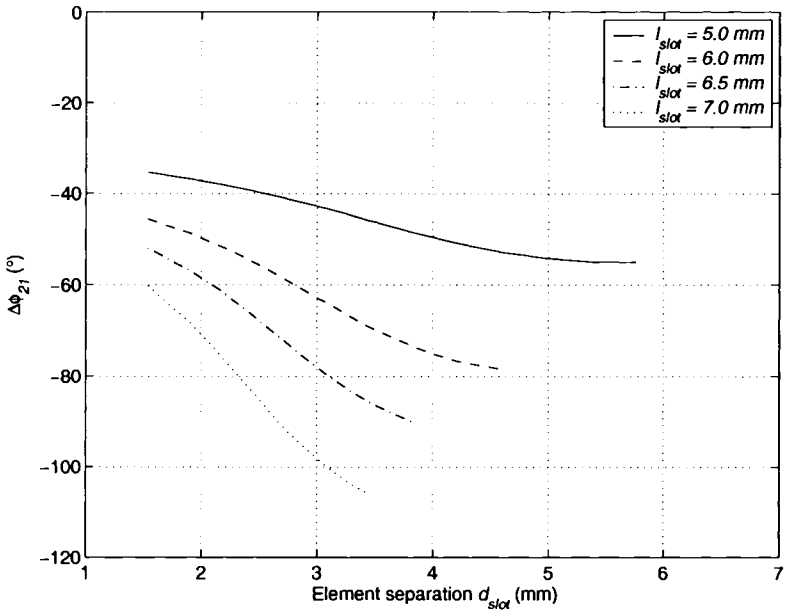
5.3.1 Design Based on Minimum Element Separation

From Chapter 4, it was noted that the optimised individual dumbbell element can provide a $\Delta\phi_{21} \leq 19°$ with an S_{11} of ≤ -10 dB. While this is in the proximity to the 22.5° bit requirement of a four-bit phase shifter, it was desired to achieve a design that could more consistently satisfy return loss specifications. Specifically, a single element design would offer the four-bit incremental phase level if the dumbbell structure was simply increased in length. However, a consequence of this design selection would result in an increase in the mismatch and return losses. It was concluded that in combination with another defect element, the return loss requirements of the individual element could be relaxed. This is not an option when utilizing the dumbbell on its own if there is no room to compromise on the return loss. Thus, in order to realize the base phase level of the popular four-bit phase shifter, a pair of dumbbells must be utilized to achieve the 22.5° phase increment. The dumbbell structure was therefore implemented in a paired arrangement to determine which configuration would produce the most desirable result.

Figure 5.1 provides the S_{11} and S_{21}, as well as the differential insertion phase for the paired dumbbells with respect to their element separation for slot lengths of 5.0 mm, 6.0 mm, 6.5 mm, and 7.0 mm, in conjunction with a 50Ω transmission line. Gap widths and lengths were 0.1 mm and 1.3 mm, respectively. The slot width was 0.5 mm.



(a)



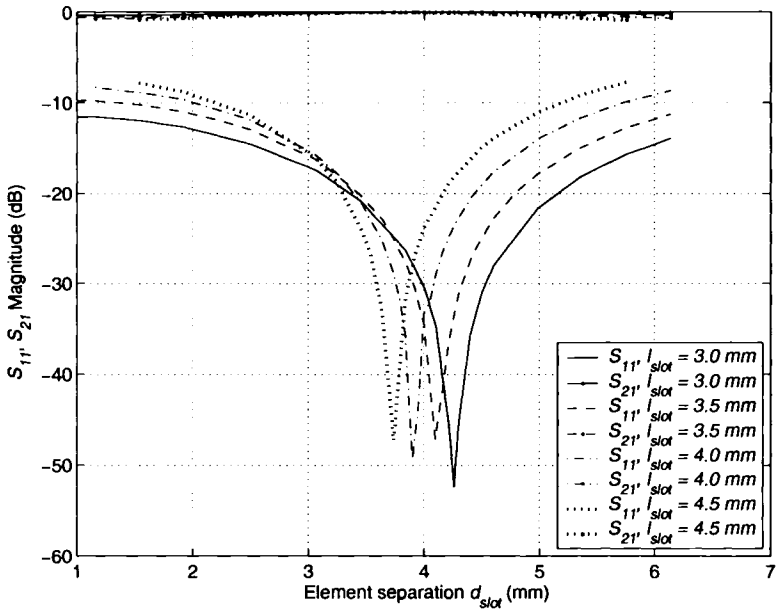
(b)

Figure 5.1: *Paired dumbbell combination with l_{slot} = 5 mm, 6.0 mm, 6.5 mm, and 7 mm for w_{slot} = 0.5 mm, w_g = 0.1 mm, and l_g = 1.3 mm; (a) S_{11} and S_{21}, (b) $\Delta\phi_{21}$.*

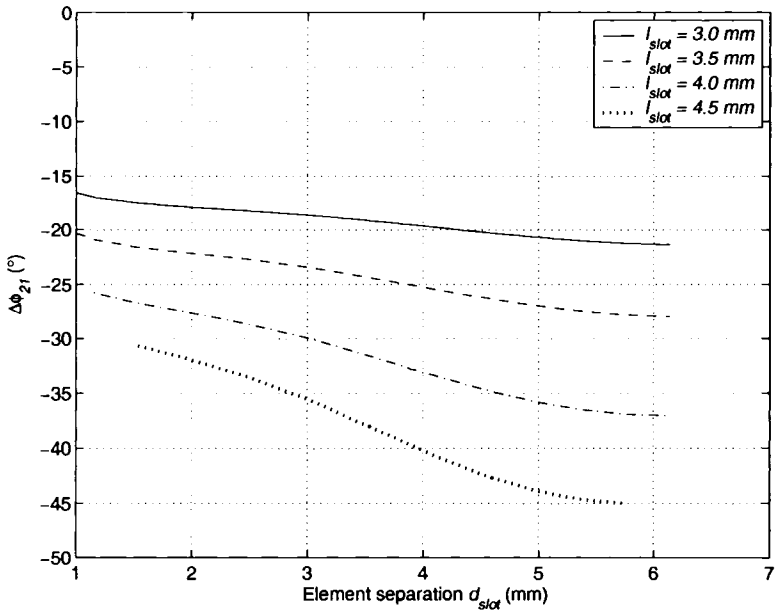
With these dumbbells lengths, several phase shifter implementations are possible, the most obvious being for the execution of lesser bit implementations, i.e. two- and three-bit digital phase shifters. Almost 100° of phase is possible with the 7 mm paired dumbbell grouping, while 45° degrees of phase is possible with elements of l_{slot} = 5 mm at d_{slot} = 3.26 mm. However, with the dumbbells lengths selected, the phase produced by a paired grouping is too great to implement with higher bit digital phase shifters.

Dumbells with lesser l_{slot} were examined to achieve a finer phase bit increment. Figure 5.2 illustrates the S_{21} and S_{11} obtained by a paired grouping of l_{slot} = 3.0 mm, 3.5 mm, and 4.0 mm elements along with the base 4.5 mm element. With l_{slot} significantly reduced, it is apparent that a wider range of d_{slot} values can maintain a satisfactory S_{11}. Over the range of d_{slot} in Figure 5.2 (b), the differential insertion phase possesses a less dramatic relationship to the element separation in Figure 5.1 (b). A maximum variation of only 7° in $\Delta\phi_{21}$ occurs for l_{slot} less than 4 mm over d_{slot} = 1.0 mm to 6.14 mm. The S_{11} for these cases also indicates that for the range of sampled d_{slot}, the return loss barely exceeds 10dB, a characteristic which is also hinted at should d_{slot} be increased further.

An l_{slot} of less than 4.0 mm is necessary in order to achieve the four-bit 22.5° phase increment. As such, paired dumbbells of l_{slot} = 3.5 mm were selected to generate 22.5°. When separated by 2.30 mm, the 2 elements produce the required differential phase, as shown in Figure 3.6 (b). Elements having l_{slot} of 3.0 mm could also be selected as the base element pair to initiate a 22.5°, however, an element separation of d_{slot} greater than 6.0 mm would be necessary. The S_{11} and S_{21} at 10 GHz are less than –10 dB and greater than –0.5 dB respectively, over the range of element separations sampled for l_{slot} = 3.5 mm. From Figure 5.2, it can also be concluded that for an even finer phase bit, such as 11.25° necessary for a five-bit digital phase shifter, a paired grouping with l_{slot} less than 3.0 mm is required. With the larger elements illustrated in Figure 5.2, it is interesting to note that the 2 4.5 mm pair falls just short of achieving the 45° required for a 3-bit phase shifter, losing its match for d_{slot} above 5.2 mm. Table 5.1 lists the bit configurations possible by the paired elements shown in Figures 5.1 to 5.2.



(a)



(b)

Figure 5.2: *Paired dumbbell combination with l_{slot} = 3.0 mm, 3.5 mm, 4.0 mm, and 4.5 mm for w_{slot} = 0.5 mm, w_g = 0.1 mm, and l_g = 1.3 mm; (a) S_{11} and S_{21}, (b) $\Delta\phi_{21}$.*

Table 5.1: *Possible least significant bit configurations optimized for phase by paired groupings of l_{slot} = 3.5, 4.5, 5.0, 6.5, and 7.0 mm elements, with $S_{11} \leq -10$ dB.*

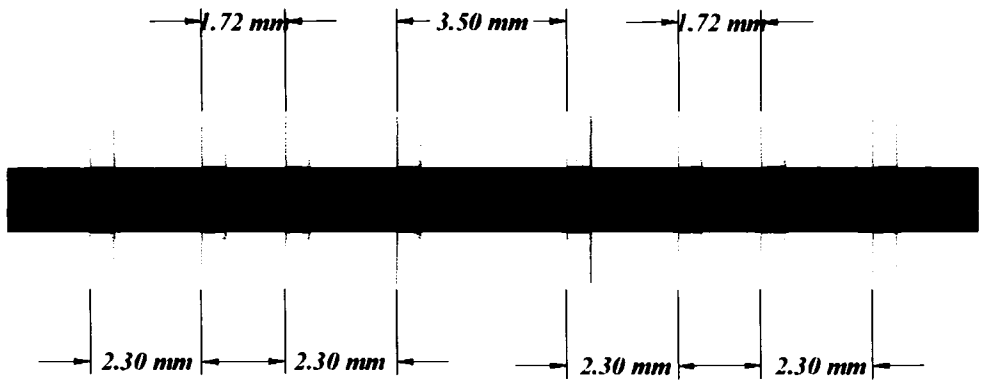
Bit level	*Element pairs*	*$\Delta\phi_{21}$ (°)*	*S_{11} (dB)*	*d_{slot} (mm)*
2	*2x7.0mm*	*89.6*	*-14.95*	*2.65*
3	*2x5.0mm*	*44.6*	*-22.64*	*3.26*
4	*2x3.5mm*	*22.5*	*-12.18*	*2.30*
4	*2x3.3mm*	*22.5*	*-26.49*	*3.84*

5.3.1.1 3.5 mm Element Based 4-Bit Phase Shifter

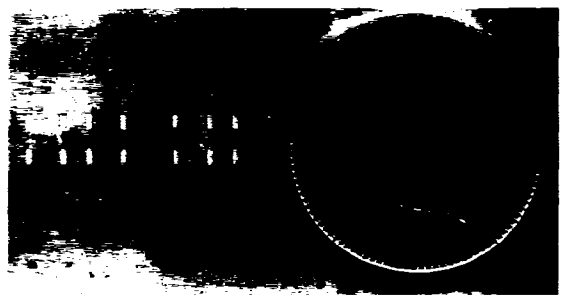
The most straightforward phase shifter design would be to employ the 22.5° bits in sequence to produce additional phase shift in 4-bit increments [95]. With 2 elements required for each bit increment, a total of 30 elements are necessary to acquire a phase shift of 337.5°. The S_{11} and S_{21} magnitudes and the differential insertion phase sampled at 10 GHz using Ensemble 8.0 are listed in Table 5.2. Through simulation, it was determined that while each 22.5° slot pair was to be separated by 2.30 mm, a 45° increment resulted when a second pair was added only a distance of 1.72 mm from the first. With a 2-paired structure, a third pair is added to the sequence at 3.50 mm, with the sequence then repeating itself every 2 pairs, as shown in Figure 5.3 (a).

Table 5.2: *Simulated phase, S_{11}, S_{21} for 3.5 mm element phase shifter.*

# of Elements	*$\lvert\Delta\phi_{21}\rvert$(°)*	*S_{11}(dB)*	*S_{21}(dB)*
2	22.48	-12.18	-0.33
4	45.06	-18.83	-0.14
6	67.50	-15.87	-0.19
8	89.61	-17.42	-0.20
10	113.47	-14.62	-0.29
12	134.54	-26.55	-0.14
14	157.82	-11.84	-0.47
16	179.75	-28.56	-0.17



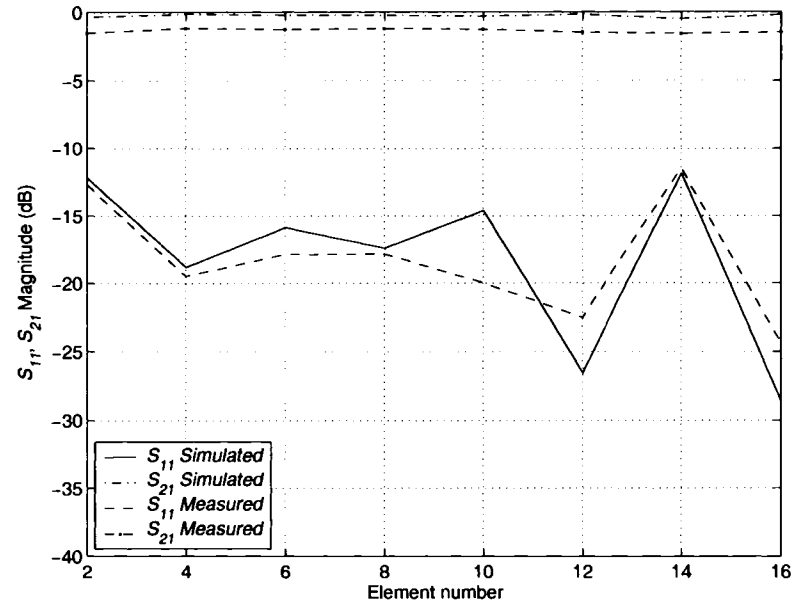
(a)



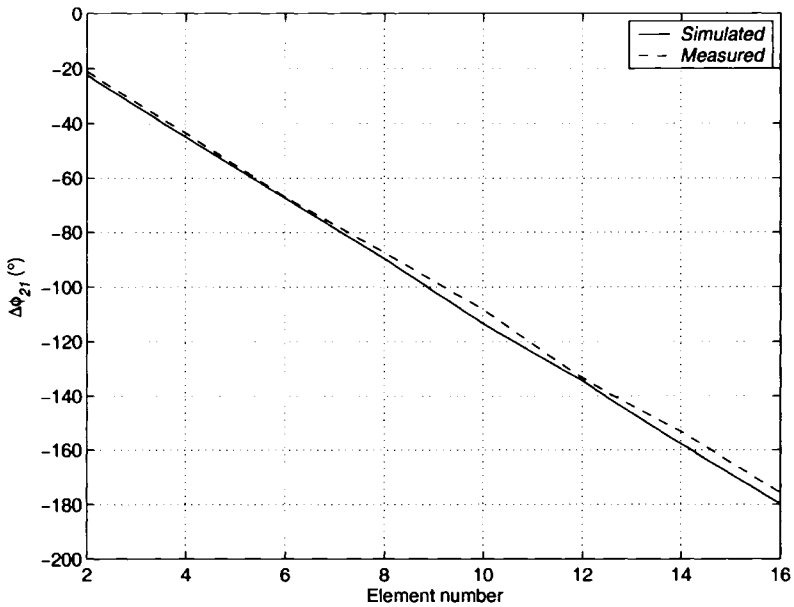
(b)

Figure 5.3: *90° phase bit configuration for 3.5 mm elements, (a) layout, (b) prototype.*

Prototypes of the 3.5 mm element 4-bit loaded-line phase shifter were fabricated and measured, and compared with simulated predictions. Fifteen defected microstrip line samples were implemented using Rogers 3003 copper substrate, of $\varepsilon_r = 3$, $\tan\delta = 0.0013$, and $h = 0.508$ mm, for each 22.5° increment up to 337.5°. The defected elements were shorted out using conducting copper tape in the ground plane to establish the absolute phase of the reference transmission line and ultimately the differential insertion phase of the defected line phase shifter. Measured and simulated S_{11}, S_{21}, and $\Delta\phi_{21}$ at 10 GHz for phase shifts up to 180° are presented in Figures 5.4 (a) and (b). Insertion loss of –1.46 dB was measured for a 10 cm line for $\Delta\phi_{21} = -175.69°$. However, the phase shifter length from defect to defect is 36 mm. Thus, the associated S_{21} of the phase shifter is scaled by 100mm/36mm = 2.78 to give a measured FOM of 334°/dB. The associated simulated FOM is 582°/dB.



(a)



(b)

Figure 5.4: *Comparison of simulated and measured S-parameters and differential insertion phase of the 3.5 mm phase shifter, (a) S_{21} and S_{11}, (b) $\Delta\phi_{21}$.*

5.3.1.2 5.0 mm Element Based 4-Bit Phase Shifter

It is evident from the data listed in Table 5.2 that while the structure has desirable S_{11} and S_{21} levels, it would be advantageous to minimize the required number of elements. It would be practical to achieve each 22.5° bit with a single dumbbell. From Figure 5.1, 45° increments were achieved by utilizing two 5.0 mm dumbbells with a separation of 3.26 mm. However, a single 5 mm defect could not provide the desired S_{11} magnitude. Thus, two designs were considered for comparison. The first design employed solely the 5.0 mm defect elements at a constant element separation of 3.26 mm. The second design applied the 3.5 mm defect pair at the beginning of the sequence, to provide the initial 22.5° increment, followed by 5.0 mm dumbbells in the sequence outlined in Figure 5.5 [95]. Figure 5.6 shows their S_{11} and S_{21} magnitudes, and the phase shift generation up to 180°.

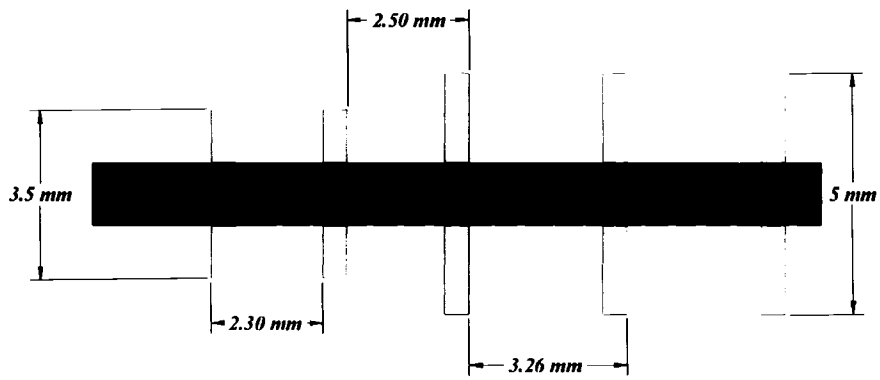


Figure 5.5: *90° phase bit configuration for 5 mm element (matched) phase shifter.*

Note that the necessary phase increments are achieved by both designs. However, the S_{11} and S_{21} magnitudes of the 8-element uniformly spaced structure are less preferable for odd element configurations. For a 180° phase shift, the 5 mm defect used in conjunction with the shorter 3.5 mm elements (matched design) requires only 9 elements.

This element total, as detailed in Table 5.3, is less than the 16 elements required for the 3.5 mm defect structure detailed in Table 5.2.

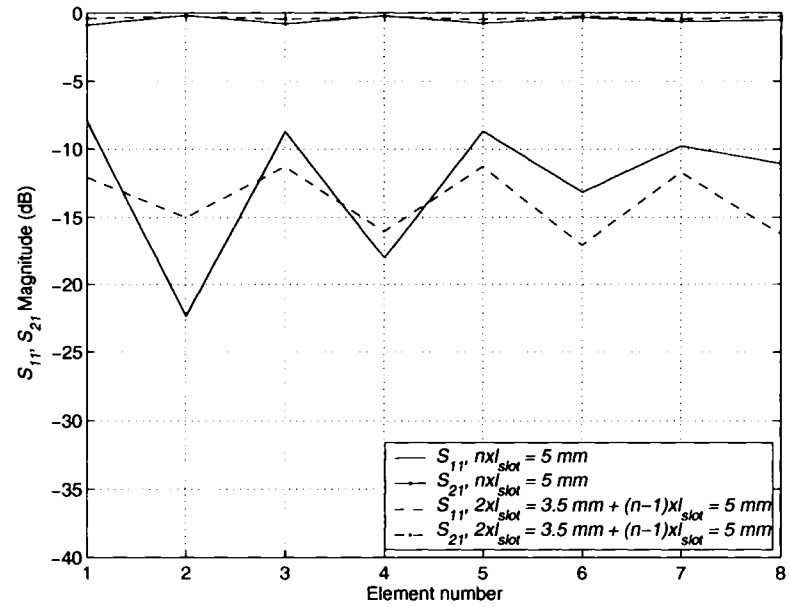
The simulated results for the matched 5.0 mm design in Figure 5.6 illustrates a more favourable *S*-parameter performance in comparison to the uniformly cascaded 5.0 mm dumbbell phase shifter. It was decided to fabricate and obtain measurement data for this prototype. The measurement and simulation results for the matched 5.0 mm loaded-line phase shifter are compared in Figure 5.7 up to 180° of phase shift at 10 GHz.

Insertion loss of –1.61 dB was measured for a 10 cm line for $\Delta\phi_{21}$ = -183.29°. However, the phase shifter length from defect to defect in this case is only 25 mm. Thus, the S_{21} corresponding to the actual phase shifter is scaled by a factor of 4 to obtain the measured FOM of 455°/dB, when including mismatch losses. The associated simulated FOM is 699°/dB.

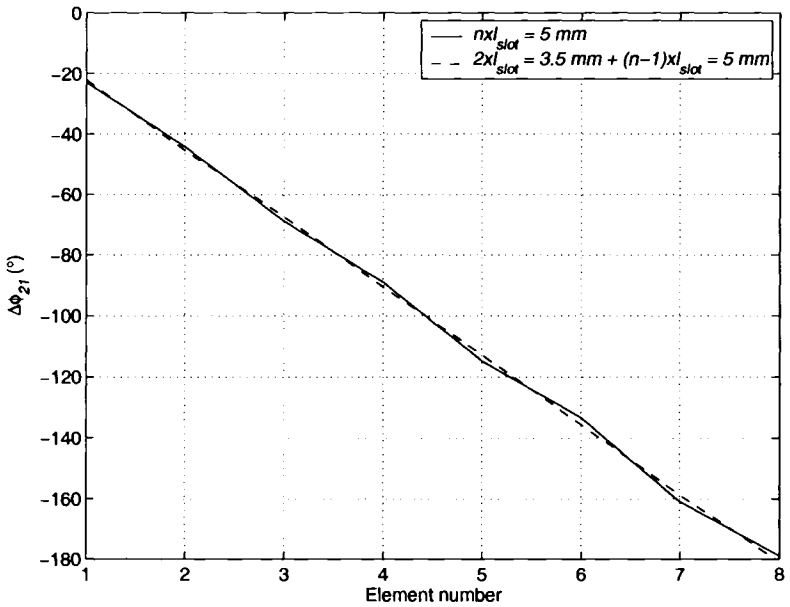
Table 5.3: *Element total, simulated $|\Delta\phi_{21}|$ for 3.5 mm and 5.0 mm (matched) element phase shifters.*

n Elements	*3.5 mm defect phase shifter $|\Delta\phi_{21}|$ (°)*	*5.0 mm defect phase shifter* $|\Delta\phi_{21}|$ (°)*
2	22.48	22.48
4	45.06	67.40
6	67.50	112.82
8	89.61	158.70
10	113.47	203.83
12	134.54	249.40
14	157.82	294.37
16	179.75	339.94

**For this design, the first two elements are 3.5 mm in length to improve matching. Each subsequent element is 5.0 mm long.*

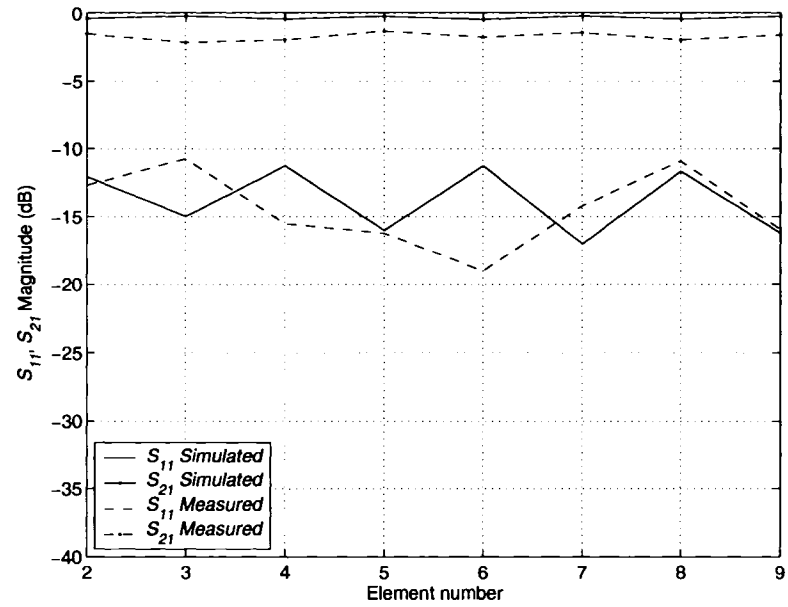


(a)

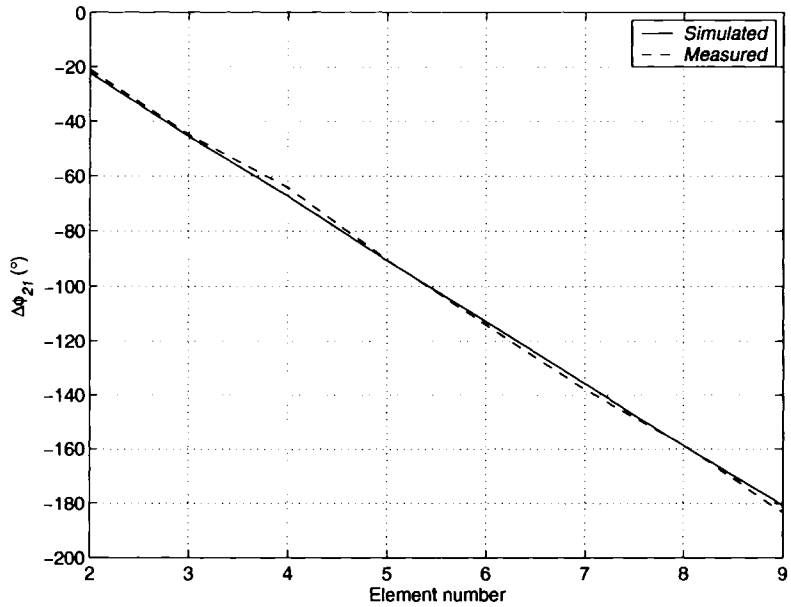


(b)

***Figure 5.6**: (a) S_{11} and S_{21}, (b) $\Delta\phi_{21}$, of 5.0 mm defect phase shifter designs (matched and unmatched designs).*



(a)



(b)

***Figure 5.7**: Comparison of the simulated and measured S-parameters and differential insertion phase of the matched 5.0 mm phase shifter, (a) S_{11} and S_{21}, (b) $\Delta\phi_{21}$.*

5.3.2 Design Based on Minimum Return Loss

5.3.2.1 Paired Element Isolation

In the previous section, phase shifter design based on minimum separation of elements was considered, studied, implemented and tested. The simulated and measured results were found to be in agreement. The criteria in that section involved satisfying the desired phase level, over minimum element separation, while maintaining the return loss below 10 dB. However, in some applications the return loss performance requirement is critical, and in such cases should be optimized.

One potential design technique is to implement the matched paired elements in series combinations. The paired elements of Chapters 3 and 4, using uniform slots or dumbbells, are well matched and may be cascaded to provide up to 360° phase shifts. For instance, paired 5.0 mm dumbbell elements generate a phase shift of 46.6° at 10 GHz for d_{slot} = 3.5 mm, with an S_{11} of –46.1 dB. With a 7.0 mm dumbbell pair and d_{slot} = 2.18 mm, a phase shift of –87.8° and S_{11} of –36.03 dB is obtained. These characteristics are illustrated in Figure 4.15 of Chapter 4. This technique will be useful if the paired-element interactions are small and the cascaded pairs remain well matched. Specifically, the success of such a design depends on the feasibility of cascading paired elements without loosing their phase control.

Two simulation experiments were conducted using two paired combinations and their return loss and differential insertion phase were determined. The results of these experiments are listed in Tables 5.4 and 5.5. The centre-to-centre spacing s between the two-cascaded pairs was changed from 1 mm to 5 mm. Since the dumbbell slot width is 0.5 mm, the minimum selected spacing of s = 1 mm provides 0.5 mm edge-to-edge slot spacing between the pairs. From the data in both tables, it would appear that a spacing of $s \geq 3.0$ mm is adequate for separating the fringing fields of the microstrip line over the slots, and thus minimizing their mutual coupling. The resulting phase beyond this separation is twice that of a single pair. The return losses are also all satisfactory. In terms of the substrate dimensional parameters, the separation of 3.0 mm corresponds to six times the height of the substrate, i.e. h = 0.508 mm. The above two dumbbell cases

were selected for their differing slot lengths, especially that of 7.0 mm, as it was the largest dumbbell investigated in Chapter 4 and is at the threshold of radiation, as indicated by larger S_{21} magnitudes in Table 5.5.

Table 5.4: *S-parameters and differential phase shift of two cascaded paired dumbbell elements, l_{slot} = 5.0 mm, w_{slot} = 0.5 mm, w_g = 0.1 mm, l_g = 1.75 mm, frequency = 10 GHz.*

Spacing s (mm)	S_{11} *(dB)*	S_{21} *(dB)*	$\Delta\phi_{21}$ (°)
1	-15.05	-0.26	-84.42
2	-23.45	-0.14	-90.42
3	-31.90	-0.11	-92.62
4	-40.13	-0.11	-93.22
5	-44.45	-0.11	-93.37

Table 5.5: *S-parameters and differential phase shift of two cascaded paired dumbbell elements, l_{slot} = 7.0 mm, w_{slot} = 0.5 mm, w_g = 0.1 mm, l_g = 3.1 mm, frequency = 10 GHz.*

Spacing s (mm)	S_{11} *(dB)*	S_{21} *(dB)*	$\Delta\phi_{21}$ (°)
1	-6.12	-1.59	-150.96
2	-13.01	-0.48	-167.05
3	-21.00	-0.25	-173.82
4	-29.28	-0.22	-175.93
5	-35.66	-0.23	-176.21

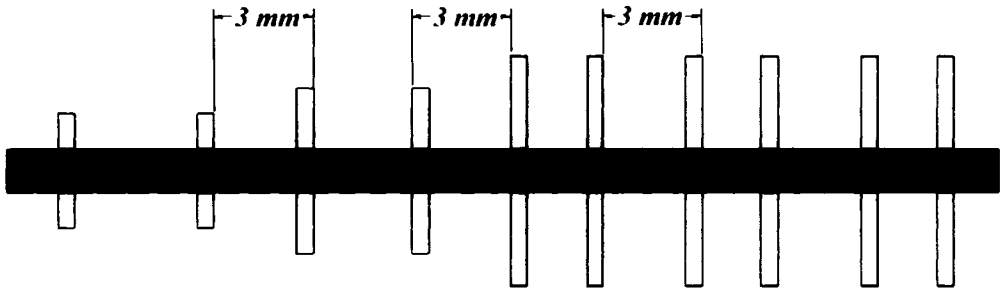
5.3.2.2 Optimum Return Loss Designs

Based on the results obtained in Tables 5.4 and 5.5, provided the matched paired elements are adequately separated, they can be cascaded to obtain the desired phase shifts. Since there are infinite different possibilities to form the pair, there are also unlimited design selections. A possible design for a 4-bit phase shifter is presented in this section and used to discuss switching methods for phase shift generation.

Using the optimized paired elements from Figure 4.15 in Chapter 4, individual pairs can be obtained to implement the necessary bit increments as shown in Figure 5.8.

[22.5°][45°][90°][180°]

(a)



(b)

***Figure 5.8**: Proposed matched 4-bit phase shifter configuration, (a) bit values, (b) geometry.*

The bracketed phase increments in Figure 5.8 (a) are represented by the following return loss optimized dumbbell combinations:

- [22.5°] = 2 × l_{slot} = 3.3 mm, l_g = 1.30 mm, d_{slot} = 4.18 mm
- [45°] = 2 × l_{slot} = 5.0 mm, l_g = 1.75 mm, d_{slot} = 3.50 mm
- [90°] = 2 × l_{slot} = 7.0 mm, l_g = 3.10 mm, d_{slot} = 2.18 mm
- [180°] = 4 × l_{slot} = 7.0 mm, l_g = 3.10 mm, d_{slot} = 2.30 mm

The widths of the slot and gap are 0.5 mm and 0.1 mm, respectively, in all cases. Note that in the above design for the 180° element, a special quadruple combination was used, as it is perfectly matched at the desired frequency of 10 GHz. Two 90° pairs separated by at least 3.0 mm could also have been implemented. With this design philosophy, slot

pairs of different lengths may be selected to optimize each individual bit. In the previous section, optimization was not performed at the bit level, rather element selection was based on satisfying the performance of the entire structure.

The above design was implemented with inter-bit spacings of 3 and 4 mm. With a 3 mm spacing, the matched frequency of the entire system was shifted from the design frequency of 10 GHz to 10.04 GHz. The S_{11} at these two frequencies had respective values of –18.3 dB and –29.1 dB. The associated differential insertion phases were 330.03° and 340.90°, instead of 337.5°. However, when the inter-bit spacing was increased to 4 mm, the matched frequency remained at the desired frequency of 10 GHz, with an S_{11} = -29.01 dB. The associated differential insertion phase was 335°, only 2.5° less than the desired phase of 337.5°. While the spacing of 3 mm is adequate for the selected substrate, the spacing of 4 mm further ensures isolation of the bit pairs, in agreement with the results obtained in Tables 5.4 and 5.5.

It should be noted that, all designs presented in this chapter used 50Ω line based elements, as they are automatically matched to other 50Ω hardware systems of the phased arrays. However, as it was noted in Chapters 3 and 4, lower impedance based elements are capable of generating larger differential insertion phases and FOMs, and may yield more compact phase shifter designs. Appropriate paired elements can be selected using the data presented in Chapters 3 and 4, then cascaded to generate the required phases following the design technique of this section.

The implementation of these defect phase shifter designs using a novel membrane technology is discussed in Chapter 6.

5.4. Phased Array Implementation

As it was desired to implement the defected transmission line phase shifters with phased arrays, designs selected from 5.3.1 have been used in this section to demonstrate beam scanning in phased arrays. For simplicity, a 3-element uniform microstrip patch array was designed with select element spacing *d*, for resonance at 10 GHz. Each patch, having a length of 8.263 mm and width of 10.607 mm, was fed by a 50Ω microstrip line,

impedance matched to the edge with the aid of a $\lambda_g/4$ transformer. The defected transmission line phase shifters were placed below the 50Ω feed line, illustrated in Figure 5.9 (b) and (c). In addition, to ensure that the array beam scan is controlled only by the phase shifters, the array elements are fed individually by separate ports, in lieu of a power divider implementation. Each element port is fed by an identical input signal in both phase and amplitude. A reference array was also studied for comparison, having no phase shifters beneath its feed lines as shown in Figure 5.9 (a). The phase shifts of the reference antenna elements are controlled by the input signal phases, i.e. $V_1 = V\angle 0°$, $V_2 = V\angle \psi$, $V_3 = V\angle 2\psi$, where ψ is the required phase shift for the beam scan, as in (5.4).

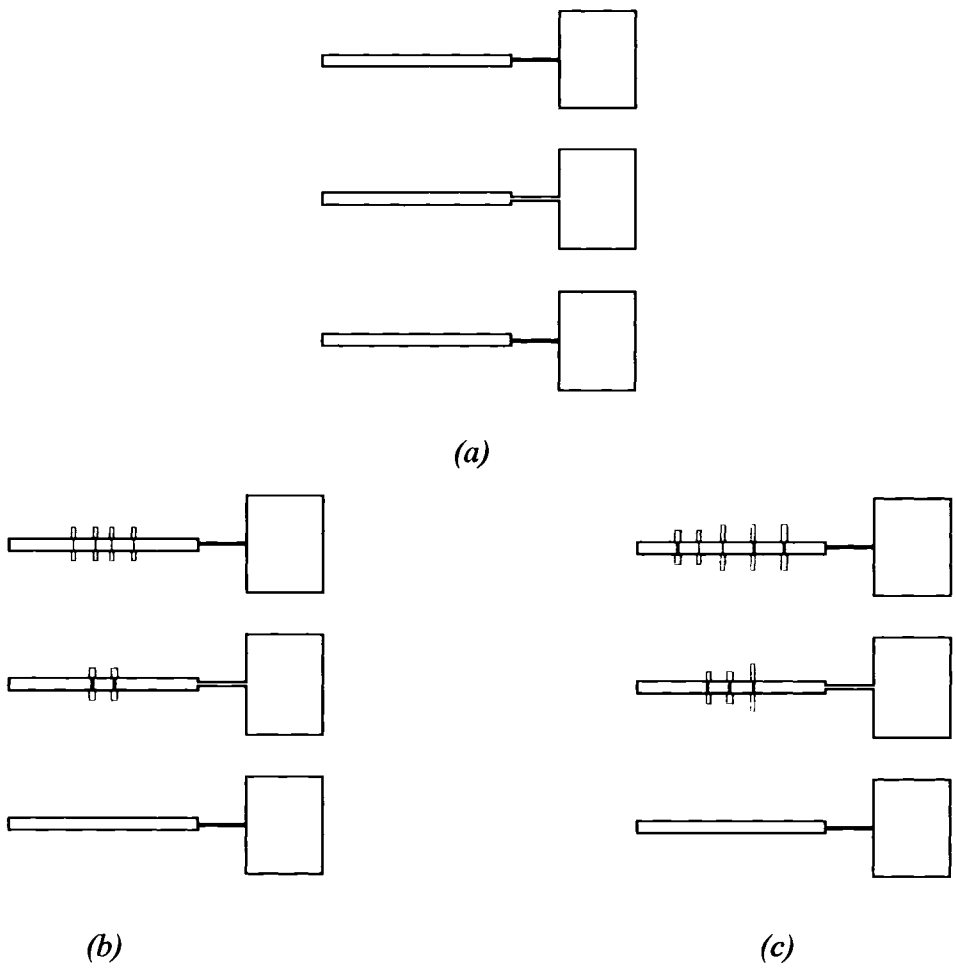


***Figure 5.9**: Array configurations, (a) reference array, (b) defect array with $\psi = 22.5°$, and (c) defect array with $\psi = 45°$.*

A comparison of the defected array and reference array radiation patterns for $\psi =$ 22.5° and $\psi = 45°$, and $d = 0.5\lambda_o$, is provided in Figure 5.10 for the $\phi = 90°$ scan plane. The scanned far field patterns are almost identical, indicating that the phase shifters function as designed. Figure 5.11 shows the far field radiation patterns of an identical but non-scanned array, i.e. $\psi = 0°$, and the defected array patterns with $\psi = 22.5°$ and $\psi =$ 45°. As expected the scan angle increases with the larger defect phase shift. Finally, Figure 5.12 compares the scanned beams of the defected phased array for different inter-element spacings. An increase in beam scanning occurs with a decrease in the array element spacing d, from $0.6\lambda_o$ to $0.4\lambda_o$, as expected from the relationship expressed in (5.5) for beam scan angle θ_o.

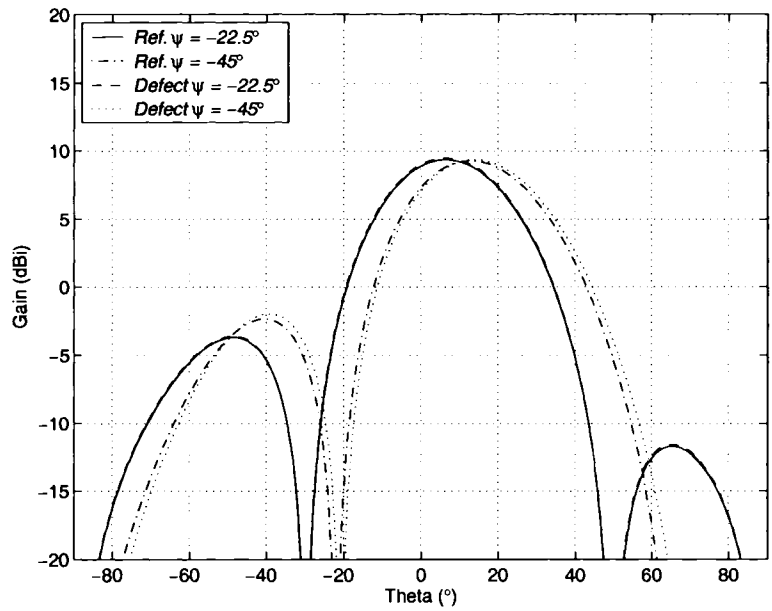


***Figure 5.10**: Computed radiation patterns of the reference and defected arrays for $\psi =$ 22.5° and $\psi = 45°$, and $d = 0.5\lambda_o$ in the $\phi = 90°$ scan plane.*

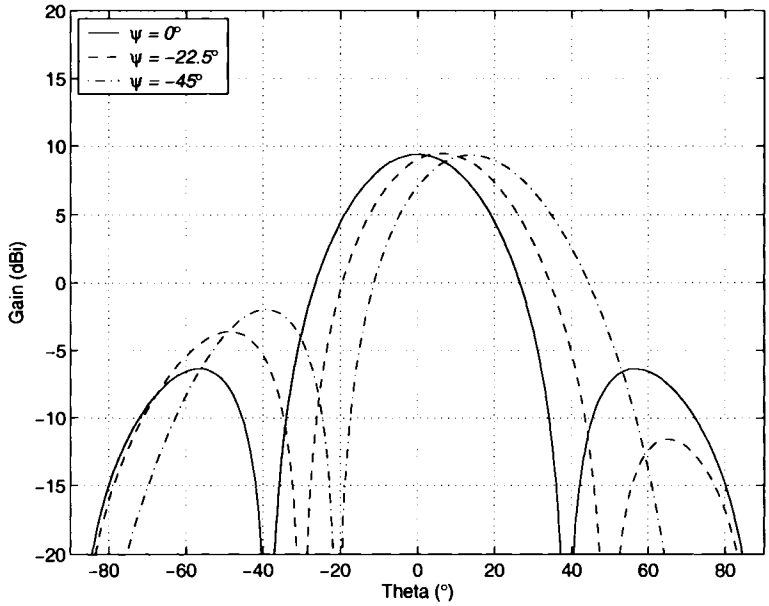


***Figure 5.11**: Computed radiation patterns of the array with no defect, and of the defected array for $\psi = 22.5°$ and $\psi = 45°$, and $d = 0.5\lambda_o$ in the $\phi = 90°$ scan plane.*

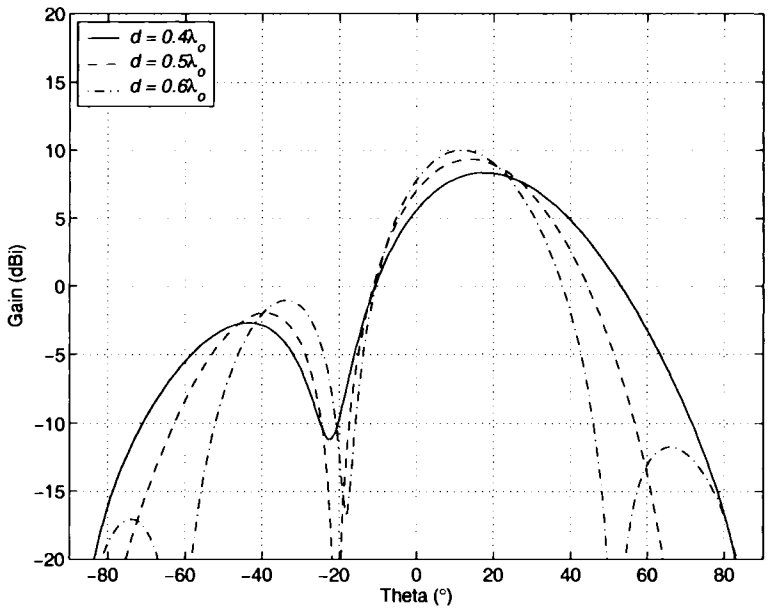


***Figure 5.12**: Computed radiation patterns of the defected array with $\psi = 45°$, for $d = 0.4\lambda_o$, $0.5\lambda_o$, and $0.6\lambda_o$ in the $\phi = 90°$ scan plane.*

Another issue of interest is the bandwidth in which the array must operate. Within this bandwidth, the array elements and their phase shifters influence the radiation pattern. In the present design, the patch element return loss bandwidth, for $S_{11} = -10$ dB, is from 9.9 GHz to 10.1 GHz. It would be useful to compare the phase progression between the array elements, using (5.4), to the phase shifts generated by the phase shifters. These are shown below in Tables 5.6 and 5.7, over the array bandwidth. The differences in ψ at the frequencies indicated, generated by (5.4) are within 0.93°, and within 1.75° for the defect phase shifters. In particular, the differences in the phase variation $\Delta\psi$, between Tables 5.6 and 5.7, are less than 1°. Thus, the selected phase shifters track the necessary phase variation over the bandwidth, as required by the phased array.

***Table 5.6**: Array element phase progression, generated by (5.4), for beam scan θ_o over 9.9 GHz to 10.1 GHz, $d = 0.5\lambda_o$.*

θ_o (°)	$\psi_{9.9GHz}$ (°)	ψ_{10GHz} (°)	$\psi_{10.1GHz}$ (°)	$\Delta\psi$ (°)
7.18	22.28	22.50	22.73	0.45
14.47	44.50	45.00	45.43	0.93

***Table 5.7**: Array element phase progression, generated by the defect phase shifters of Figure 5.9, for beam scan θ_o over 9.9 GHz to 10.1 GHz, $d = 0.5\lambda_o$.*

θ_o (°)	$\psi_{9.9GHz}$ (°)	ψ_{10GHz} (°)	$\psi_{10.1GHz}$ (°)	$\Delta\psi$ (°)
7.18	22.12	22.48	22.66	0.67
14.47	44.19	45.06	45.94	1.75

5.5 Conclusions

This chapter applied the knowledge gained in previous chapters to design ground plane defected phase shifters. The phase shift requirements of linear phased arrays were reviewed briefly. Two design philosophies were developed using the dumbbell structures. In the first design, the criterion involved the minimization of the inter-element spacing, providing the required phase shifts within a return loss limit of 10 dB. Prototypes were fabricated and demonstrated measured figures of merit of 334°/dB for the 3.5 mm element phase shifter, and 455°/dB for the matched 5 mm element design. For the second design philosophy, only matched paired elements were selected towards the minimization of return loss. A study was conducted, and determined that as long as the inter-paired element spacing was kept larger than 3 mm, the interaction between the pairs was minimal. That is, cascaded pairs remained well matched and their differential insertion phases additive. Based on this knowledge, a cascade of paired elements was incorporated into a 4-bit phase shifter design.

The performance of select defected transmission line phase shifters was verified using a three-element microstrip patch phased array. The scanned beams were determined for 22.5° and 45°element phase progressions, as well as for different array element spacing. Far field radiation patterns were compared with those of the reference array. The agreement in all cases was satisfactory, confirming the feasibility of implementing defected phase shifters within phased arrays. The phase progression generated by array theory in (5.4) and the defect phase shifters were also compared and found to be very similar.

CHAPTER 6

RECONFIGURABLE GROUND PLANE DEFECTS

Chapter 5 presented methodology for the design of phased array phase shifters based on defected ground structures. Sample designs for different phase bit generation and complete designs for 4-bit phase shifters were also provided. Each phase bit can be activated using conventional switching technology. However, this chapter presents a novel idea based on a micromachined membrane structure that allows both discrete and continuous phase shift generation. The membrane is defined as a section of microstrip line ground plane that is detached from its dielectric substrate and can be physically moved by an electrode from below. When a control voltage is applied to the electrode, the induced electrostatic force can conveniently generate membrane activation. The membrane surface may be smooth or corrugated. Smooth membranes are easier to fabricate and are more suitable for small displacements due to their increased stiffness. Imposing corrugations on the membrane reduces the structural stiffness, and thus the required voltage for displacement. As a result, they are more suitable for generating large displacements. This chapter discusses their properties and use for controlling the phase shift of ground plane defected phase shifters. Because the membrane is a mechanical device, whose operating speed is controlled by its mechanical resonance frequency, on the order of kilohertz, its switching speed is limited to millisecond operation (~0.5 sec).

6.1 Corrugated Membrane Structures as Phase Shifters

A novel approach to phase shifting incorporating MEMS principles, involves an "actuating" ground plane membrane, as discussed in [88] and [96]. A control electrode is placed beneath the ground plane of a microstrip patch or transmission line, where the electrode is separated from the membrane by a small cavity, as shown in Figure 6.1.

Application of a control voltage results in the contraction of the ground plane membrane towards the electrode, generating an air gap between the upper substrate layer and the ground plane. The effective dielectric constant of the substrate decreases, by an amount that is controllable by the applied DC electrode voltage. From (2.2), a change in the permittivity would correspondingly affect the propagation velocity, initiating change in the phase of the signal propagating along the structure. Thus, an actuating ground plane can be used to design a tunable microstrip antenna or transmission line. The structure was incorporated beneath a 50 Ω line for use as a phase shifter, achieving phase shifts of 45° to 263° at 10 GHz with multiple membranes, with return and insertion loss of 15 dB to 13 dB and 0.185 dB to 0.45 dB, respectively. In this configuration, complete isolation is achieved without external filters or isolators, as the RF signal and control voltages are physically separated [88].

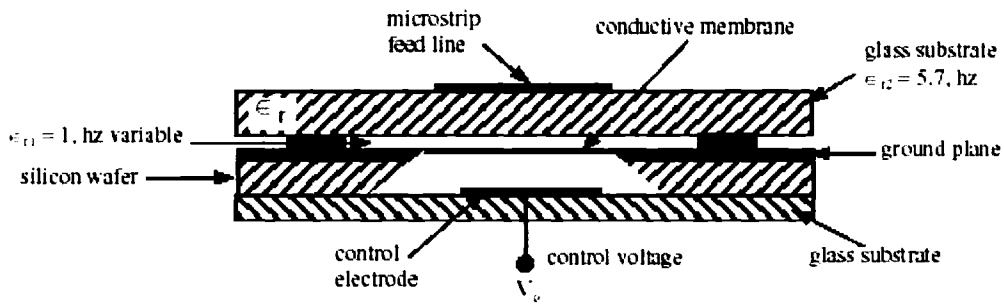


Figure 6.1: *Cross sectional geometry of an adaptive microstrip feed line placed above a control electrode [88].*

6.1.1 Design and Characteristics of Corrugated Membranes

Membrane structures can be approximated to simple plate geometry, with the exception that their depth is notably thin and their boundaries are fixed. The membrane possesses small-signal and large-signal operating regions, with smaller deflections

illustrating linear behaviour. The addition of corrugations along the membrane increases its effective surface area in comparison to a flat, uncorrugated membrane. This quality renders the structure more suitable for larger deflections possessing an extended linear range of deflection.

These structures are classified as capacitive sensors, whose capacitance and electrostatic energy respectively, can be established by the expression for the capacitance between two conducting parallel plates, separated by a distance d [97],

$$C = \frac{\varepsilon A}{d} \tag{6.1}$$

$$W_e = \frac{1}{2}CV^2 = \frac{1}{2}\frac{\varepsilon A}{d}V^2 \tag{6.2}$$

where A is the absolute plate area (neglecting fringing fields), V is the voltage potential difference, and ε is the permittivity of the material between the two plates, and the upper and lower plates are defined by the membrane diaphragm and the electrode. A cross section of the membrane structure is shown in Figure 6.2.

With the downward deflection of the membrane defined by z, the plate separation becomes $(d\text{-}z)$, and its corresponding energy becomes,

$$W_e = \frac{1}{2}CV^2 = \frac{1}{2}\frac{\varepsilon A}{(d-z)}V^2 \tag{6.3}$$

The magnitude of the electrostatic force after this incremental change z is determined through the differentiation of (6.3),

$$F = \frac{\partial W}{\partial z} = \frac{\varepsilon A V^2}{2(d-z)^2} \tag{6.4}$$

The electrostatic force is thus balanced by a restoring static spring force, which is relative to the spring displacement z, and has a magnitude of [97],

$$F = kz \tag{6.5}$$

where k represents the spring force constant that serves to identify the stiffness characteristics of the spring. Equating the electrical force in (6.4) to the resultant physical force of (6.5), it is possible to determine the required voltage V necessary for a specific membrane deflection. The voltage-to-actuation can then be expressed by the following equation [96],

$$V = \sqrt{\frac{2kz(d-z)^2}{\varepsilon_{eff}\pi R^2}} \tag{6.6}$$

where z is the vertical deflection, $(d\text{-}z)$ is the distance between the membrane and the driving electrode, πR^2 is the membrane area with radius R, and ε_{eff} is the effective permittivity of the air-gap and insulator region between the membrane ad the electrode.

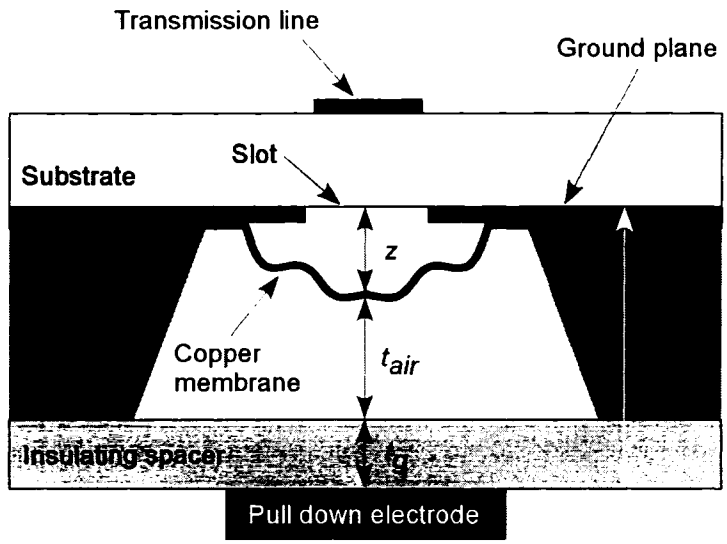


Figure 6.2: *Cross-section of the slot loaded transmission line backed by the copper membrane structure.*

The determination of the permittivity in this mixed air and insulator region is based on a quasi-static model of series capacitances. Expressing (6.1) for permittivity:

$$\varepsilon_{cavity} = \frac{C\left(t_{air} + t_g\right)}{A} \tag{6.7}$$

$$C_{cavity} = \left(\frac{1}{C_{air}} + \frac{1}{C_g}\right)^{-1} = \frac{\varepsilon_{air}\varepsilon_g A}{\varepsilon_{air} t_g + \varepsilon_g t_{air}} \tag{6.8}$$

Substituting (6.8) into (6.7), the effective permittivity of the cavity can be expressed as follows [99],

$$\varepsilon_{cavity} = \frac{\varepsilon_{air}\varepsilon_g\left(t_{air}+t_g\right)}{\varepsilon_{air}t_g+\varepsilon_g t_{air}} \tag{6.9}$$

where ε_{air} is the permittivity of the air-gap region, ε_g is the permittivity of the dielectric (the glass insulating spacer for the diagram in Figure 6.2), t_{air} is the thickness of the air-gap, and t_g is the substrate thickness.

The spring constant k of a circular, corrugated, clamped membrane is expressed by [96],

$$k = \frac{A_p \pi E t^3}{R^2} + \frac{B_p \pi E t z^2}{R^2} \tag{6.10}$$

where E is Young's modulus of the membrane material, and t is the membrane thickness. The parameter A_p represents a dimensionless stiffness coefficient, and B_p the dimensionless coefficient of non-linear tension, expressed by:

$$A_p = \frac{2(q+2)(q+1)}{3\left(1-\left(\nu/q\right)^2\right)} \tag{6.11}$$

$$B_p = \frac{32}{\left(q^2-9\right)}\left(\frac{1}{6}-\frac{3-\nu}{(q-\nu)(q+3)}\right) \tag{6.12}$$

with ν representing Poisson's ratio of the membrane material. For copper, $\nu = 0.3$.

Both A_p and B_p are dependent on the profile factor, or quality factor, q, a significant parameter in the design of a corrugated membrane. This quality factor is used to determine the ratio of the corrugation rigidity with respect to the structural bending, and thus is a critical membrane figure of merit. It is expressed as a function of the corrugation depth H, the corrugation period or wavelength L, and the arc length S,

$$q = \sqrt{\frac{S}{L}\left(1+\frac{3}{2}\left(\frac{H}{t}\right)^2\right)} \tag{6.13}$$

The above expression for q represents the corrugation quality factor for corrugations with a sinusoidal profile. However, membrane performance is not greatly influenced by the geometrical corrugation profile, and thus (6.13) may also be adopted for rectangular or trapezoidal profiles among others. As with the coefficients A_p and B_p in (6.11) and

(6.12), q is dimensionless. For uncorrugated membranes, $H = 0$ and q has a value of 1. For corrugated membranes, q increases (commonly possessing a magnitude of 5 to 15), with very high values of q promoting a membrane design of high rigidity and increased linearity.

Fabrication details are found in [96], and [99], and while briefly addressed in section 6.5.2, are beyond the scope of this thesis.

6.2 Cavity-Backed Single Slot Phase Shifter

Chapters 3, 4, and 5 focused on the use of single and multiple defects in a microstrip ground plane and the possible phase differences that can be achieved by their presence in comparison to a conventional microstrip structure. In order to apply an ON/OFF approach to the phase control, a switching structure is necessary. Conventional solid-state components such as diodes may be implemented as a proof of concept approach to the phase shifter. However, considerations that must be met in order for such a design to be a success include the implementation of the bias lines directly to the structure, to control the status of the diodes. By applying the membrane structure as the phase shifter control element, the membrane voltage control is separate from the defected microstrip structure and the RF signal. Such a design adds not only switching control, but also the flexibility of continuous phase variation as an analog control structure.

Membrane actuation creates an air cavity region behind the ground plane defect. Initial experiments involved the generation of a manually constructed cavity-backed slot, with the configuration shown in Figure 6.3, using conductive tape over spacers, at an initial depth of 4 mil. A single ground plane slot was milled into the ground plane of a microstrip substrate, having a permittivity of $\varepsilon_r = 2.5$, and a substrate thickness of 0.79 mm (31 mil) [100]. The microstrip line had a width of $w_{line} = 2$ mm (54Ω). The ground plane defect had dimensions of $w_{slot} = 1$ mm, and $l_{slot} = 10$ mm for the slot width and length, respectively, and a 0 mm offset.

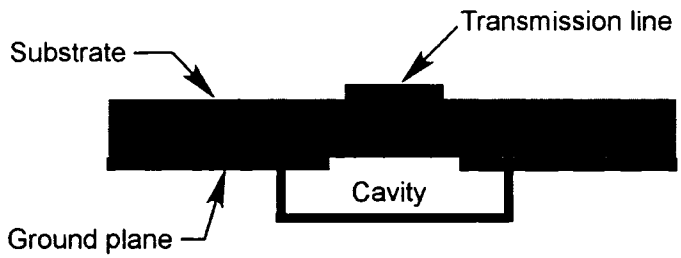
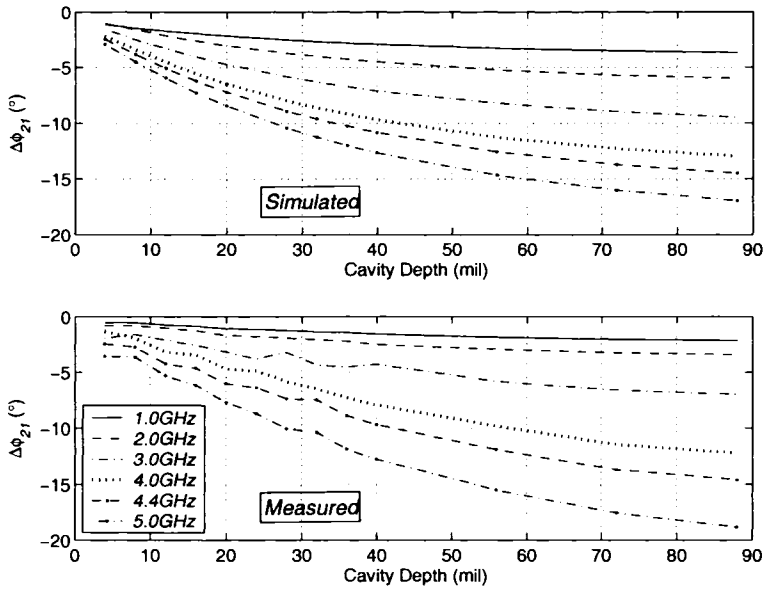
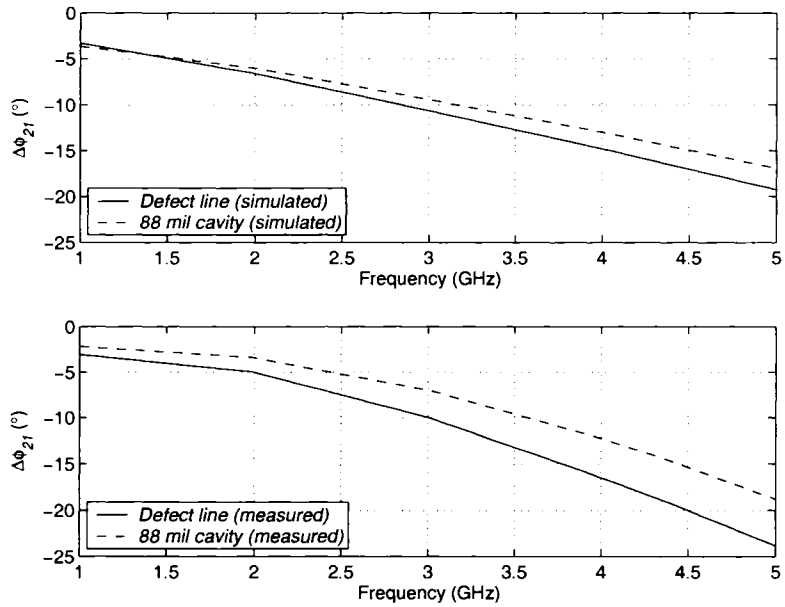


Figure 6.3: *Cross-section of the cavity-backed single-slot.*

Tests were conducted for different cavity depths, at 4 mil increments up to 40 mil, and then at 16 mil intervals with subsequent measurements at 56 mil, 72 mil and 88 mil. Measurements under a short circuit condition, i.e. the transmission line without a ground plane defect, were also obtained, as well as measurements for an open circuit condition, i.e. transmission line with defect and no cavity. The differential insertion phase $\Delta\phi_{21}$, of the structure was determined by comparing the insertion phase of the transmission line under the short circuit condition defined above, with that loaded by the cavity-backed slot. Increasing the depth of the cavity behind the slot has the effect of also increasing $\Delta\phi_{21}$, in the simulated and measured cases shown in Figure 6.4 (a). The effect of placing a cavity beneath the slot defect was approximated using Ansoft's Ensemble 8.0 software package. A parallel-plate infinite ground plane structure was simulated, i.e. a layer of air was sandwiched beneath a bottom ground plane layer and the defected ground plane layer, with the cavity defined between the two layers by a box with perfectly conducting walls. At a single frequency, measured data indicates a dependence on cavity height until the cavity depth exceeds twice the slot width, i.e. 2 mm or 80 mil, at which point the phase shift variation gradually becomes negligible.

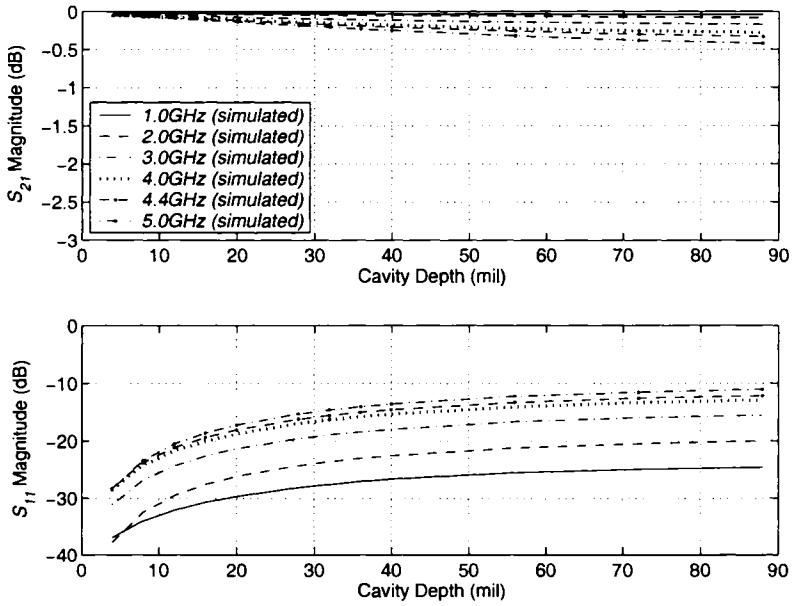


(a)

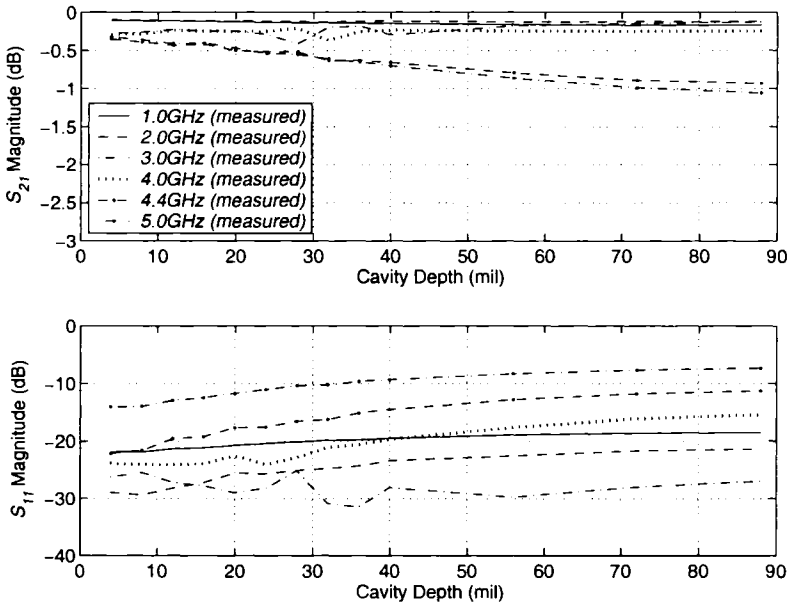


(b)

Figure 6.4: *Simulated and measured data for (a) $\Delta\phi_{21}$ at 1.0 GHz, 2.0 GHz, 3.0 GHz, 4.0 GHz, 4.4 GHz, and 5.0 GHz, with respect to the depth of the cavity backed slot, and (b) comparison of $\Delta\phi_{21}$ for the 88 mil cavity-backed slot and the open slot (no cavity) structure.*



(a)



(b)

Figure 6.5: *S_{11} and S_{21} at 1.0 GHz, 2.0 GHz, 3.0 GHz, 4.0 GHz, 4.4 GHz, and 5.0 GHz, for (a) simulated, and (b) measured results for the cavity backed defect line.*

At the upper limit of the cavity depth, $\Delta\phi_{21}$ is close to that observed with the defect line alone (non-cavity-backed structure), as illustrated in Figure 6.4 (b). Both simulated and measured differential insertion phase is provided over 1 to 5 GHz, with both plots suggesting the 88 mil cavity characteristics closely mirror those of its associated defect line. The predicted phase at 5.0 GHz for an 88 mil cavity depth is shown to be approximately 17°, seen in Figure 6.4 (a) and (b). From discussions in Chapter 3, it is known that this is the upper limit in achievable phase by a single slot, for a return loss of no greater than 10 dB. Upon examination of the S_{11} magnitude at this frequency and cavity depth, the magnitude level is within the –10 dB range. Simulated and measured results for the S_{11} and S_{21} magnitude are provided in Figure 6.5. Over the sampled frequencies for the measured data in Figure 6.5, the S_{11} is less than –10 dB from 1 GHz to 4.4 GHz. Below 4 GHz, the S_{21} is less than –0.5 dB. As this is a single defect slot, the insertion loss is primarily due to mismatch, as discussed in Chapter 3.

6.3 Membrane-Backed Single Slot Phase Shifter

The promising results from the manually constructed cavity led to the use of a flexible copper membrane in place of the discrete cavity [100]. The membrane, having a 5 mm radius, was fabricated on a 0.4 mm thick silicon wafer. It is separated from the electrode by an insulating layer of silicon dioxide having a thickness of 0.1 mm. The membrane surface has a corrugated profile that serves to increase structural flexibility and provide large deflections, in comparison to a similar but flat membrane. The corrugations have a depth of 10 μm and a period of 126 μm. The cross-section originally shown in Figure 6.2 illustrates the membrane-backed slot.

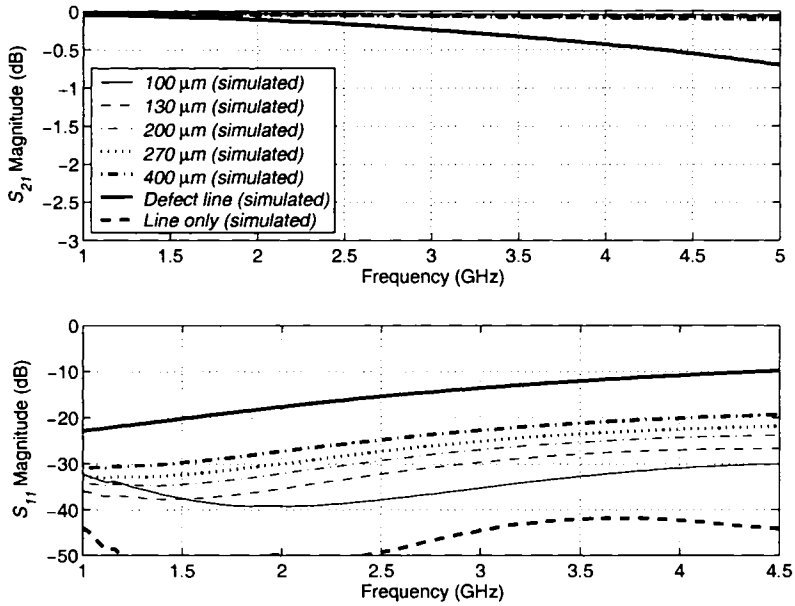
During measurement the membrane was mounted directly beneath the ground plane of the defect array line. Membrane deflection is induced through electrostatic actuation by applying DC voltage to the electrode below the membrane. As the membrane deflects away from the ground plane, an air-gap is formed beneath the slot. When the membrane is unbiased, its role is to short-circuit the defect array, leaving only the reference transmission line. When it is activated, the actuation of the membrane

initiates control of the phase shifter. The membrane is thus capable of providing the continuous generation of phase shift, from a zero value when unbiased, to a phase shift equivalent to that provided by the defect array alone, as the membrane is fully deflected.

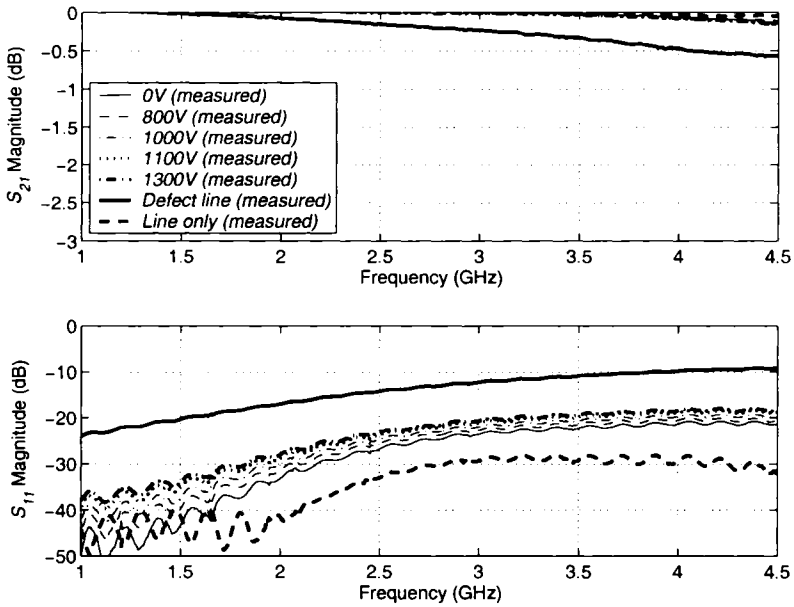
6.3.1 Experimental Implementation

6.3.1.1 Large-Slot Measurements

The slot used with the manually constructed cavity-backed structure was incorporated with the copper membrane. DC voltage between 0V and 1300V was applied to the electrode at discrete intervals. Figure 6.6 shows simulated predictions along with measured data, over the frequency range of 1 to 4.5 GHz, and comparison between the two indicates good agreement. Below 4.5 GHz, the S_{11} is less than –17 dB at the highest voltage, while the S_{21} is greater than –0.13 dB. However, beyond this frequency both parameters began to drop, suggesting that the cavity-backed defected transmission line structure was beginning to radiate. Because the dimensions of the slot are comparable to that of the membrane, the deflection distance of the membrane could not provide enough clearance below the slot to attain the phase level of the defect line with the membrane backing, as shown in Figure 6.6 (c). Due to the curvature of the membrane, the depth of the air gap region between the slot and the membrane is not uniform along the entire length of the slot. However, this discrepancy along the slot length is less significant, as it is understood from Chapter 4 that the critical location for the defect short circuit is at the slot center, directly beneath the transmission line. From preliminary experiments with the manually constructed cavity of section 6.2 it was observed that the phase levels at each frequency taper as the cavity depth approaches twice the slot width. With the membrane, a similar observation would require a deflection of 2 mm, which was not possible with the available membrane. For this reason, the original slot used with the manually constructed cavity was assumed to be too large for the available membrane.

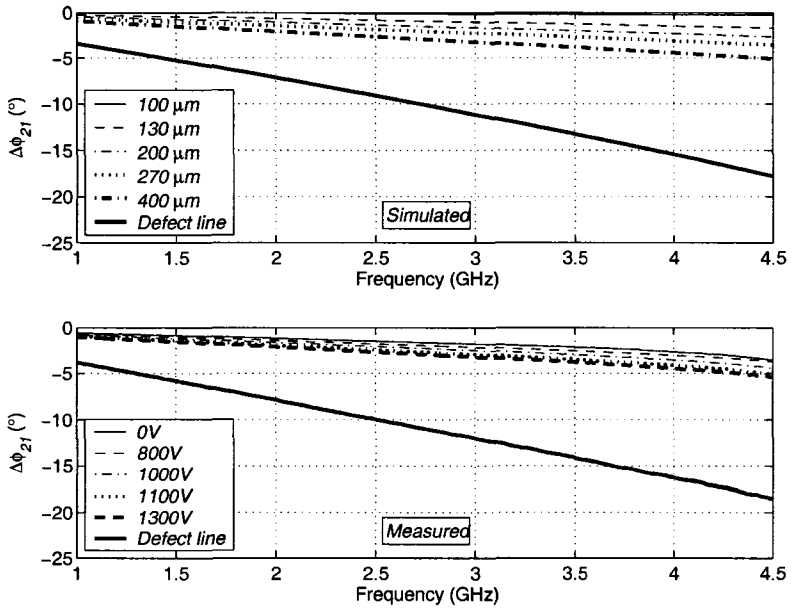


(a)



(b)

Figure 6.6: *(a) S_{11} and S_{21} (simulated) of the defect line, reference transmission line and large-slot with membrane backing at 100 μm, 130 μm, 200 μm, 270 μm, and 400 μm; (b) S_{11} and S_{21} (measured) of the defect line, reference transmission line and membrane-backed large-slot for 0V, 800V, 1000V, 1100V, 1300V applied to the electrode; (c) measured and simulated $\Delta\phi_{21}$.*



(c)

***Figure 6.6** continued*

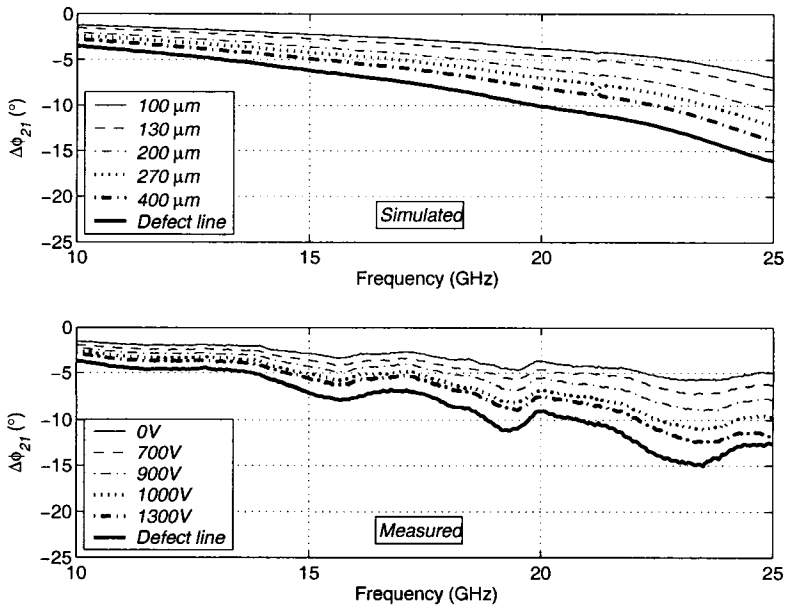
6.3.1.2 Small-Slot Measurements

A similar defect structure was implemented to that in the previous section, but having a slotted defect with significantly reduced dimensions, such that the deflection of the membrane approaches the necessary depth with respect to the slot width. A slot width of w_{slot} = 0.2 mm, and l_{slot} = 3 mm was selected, for a 1:2 ratio of w_{slot} with the maximum deflection of the membrane. The voltage levels applied to the membrane were in the same range as for the previous experiment involving the larger slot. In this case, phase shift within the frequency range of 1 GHz to 4.5 GHz were very low. Above 10 GHz, significant increases in $\Delta\phi_{21}$ were observed, as shown in Figure 6.7 (a) for simulated predictions and in Figure 6.7 (b) from measured results, up to 25 GHz. Phase shift of up to 13° was achieved at 25 GHz at a DC voltage of 1300V and deflection depth

of 400 μm. The sampled phase points in Figure 6.7 (b) suggests this phase level approaches 14° to 15° if a linear rise in phase is assumed.

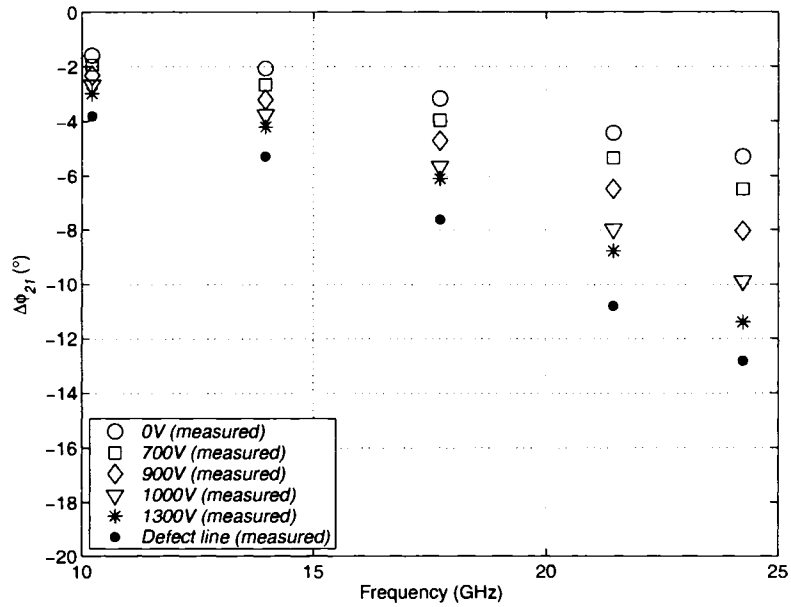
The associated S_{21} and S_{11} levels for each voltage are shown in Figure 6.7 (d), with simulated data shown in Figure 6.7 (c). A comparison of the S_{21} magnitude of the membrane-backed structure with the original transmission line illustrates very low levels of S_{21}, suggesting that the membrane-actuated cavity does not introduce additional loss into the system, with differences at lower frequencies falling in the measurement error range.

The unbiased *S*-parameter and phase shift levels in Figure 6.6 and 6.7, for the large slot and small slot respectively, indicate that phase shift is present despite the short circuit condition desired at a voltage level of 0V. This phenomenon is discussed further in section 6.4.1.2.



(a)

Figure 6.7: *(a) $\Delta\phi_{21}$ of the small-slot defect line, membrane-backed small-slot for select sampled voltages between 0V and 1300V and simulated membrane depths of 100 μm to 400 μm, (b) sampled phase points from measurement data, (c) simulated S_{21} and S_{11}, (d) measured S_{21} and S_{11}.*



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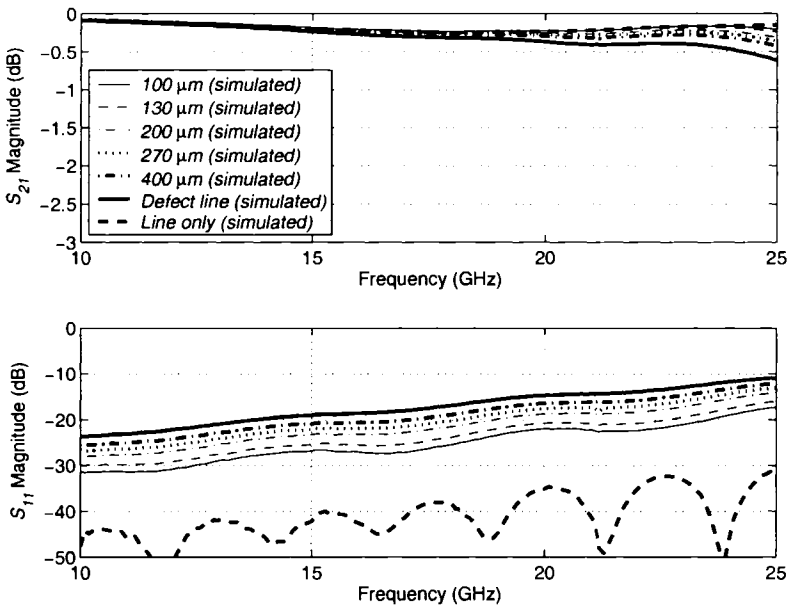
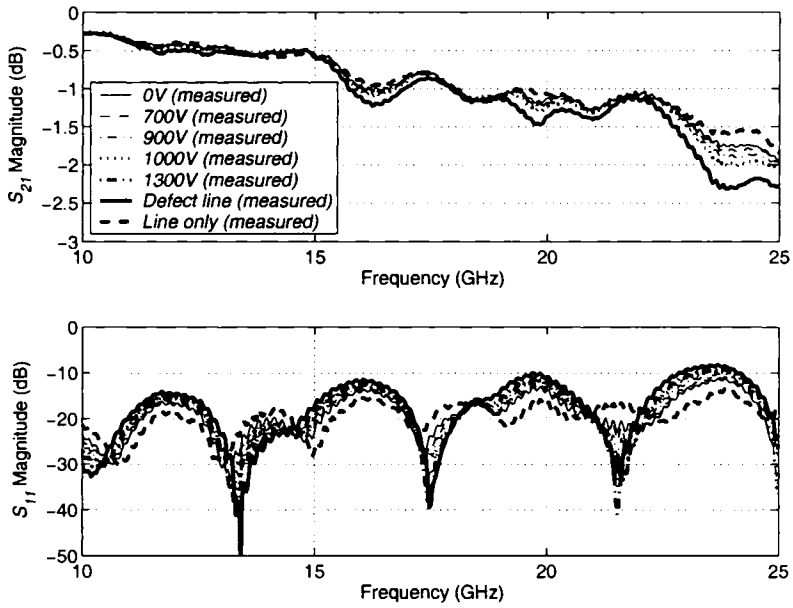


(c)

***Figure 6.7** continued*



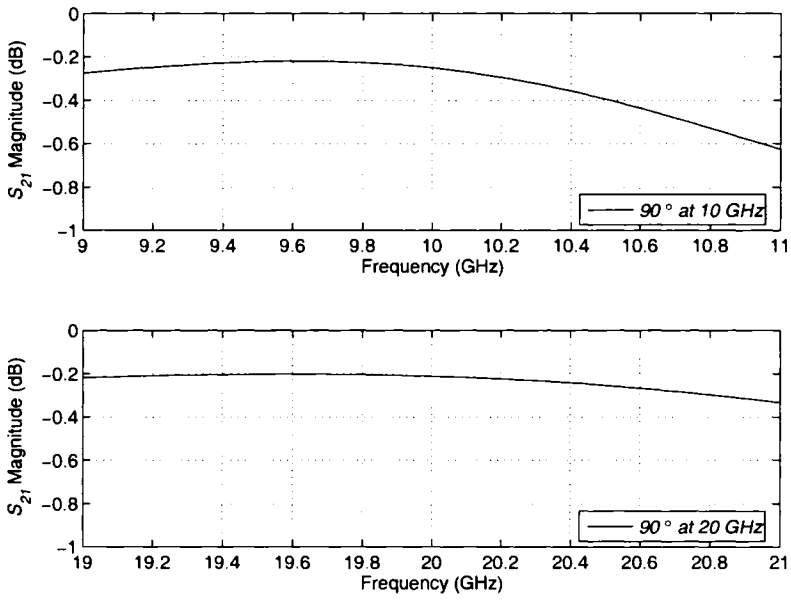
(d)

Figure 6.7 *continued*

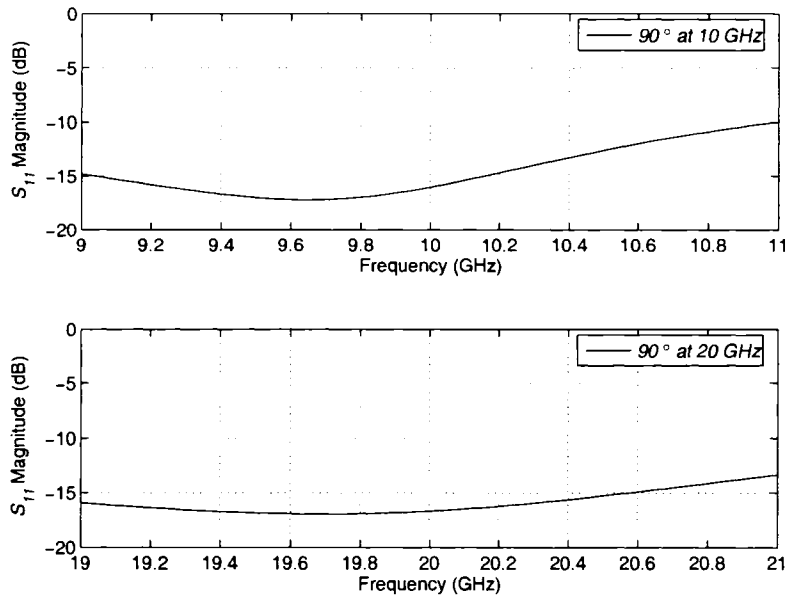
6.4 Membrane-Backed Defect Array Phase Shifter

If the membrane depth required for a full range of switching is twice the slot width, a deflection depth of 1 mm or 1000 μm is required for the slot structures introduced in Chapters 3 to 5. However, by simply reducing the width of the slot by approximately one half, to 0.2 mm, the required deflection depth is reduced to 400 μm. Because of the above factors, the design of the structures presented in previous chapters must be tuned for the new frequency in order to employ the available membrane.

The 90° phase shifter illustrated in Figure 5.4 was arbitrarily selected for operation at 20 GHz. The structure can be designed for operation at 20 GHz by scaling each dimension by one half, i.e. substrate thickness h, dumbbell parameters l_{slot}, w_{slot}, l_g, w_g, and transmission line width w_{line} (50Ω). Simulation results for this design are illustrated in Figure 6.8, and include data for the original 10 GHz design of Figure 5.4.

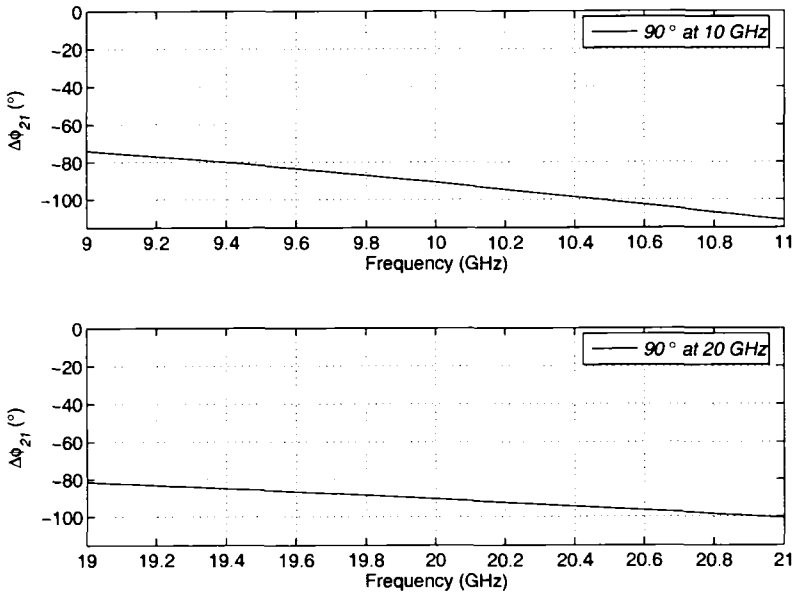


(a)



(b)

Figure 6.8: *(a) S_{21}, (b) S_{11}, and (c) $\Delta\phi_{21}$, of 90° phase shifter designed for 10 GHz and 20 GHz operation.*



(c)

Figure 6.8 *continued*

The membrane structure is used to provide a short circuit condition when unbiased, producing gradual phase change as it is actuated away from the defect array. The candidate structure used for measurement with the membrane actuator is shown in Figure 6.9 [101]. The ground plane defect of this transmission line structure is in essence very similar to that of the 20 GHz, 90° phase shifter. The structure consists of 5 slots milled into the copper ground plane with the dimensions given in Figure 6.9. The slot width is 50 μm smaller, with a uniform geometry adopted over the dumbbell design to facilitate ease of fabrication during the milling process. Material parameters and transmission line width differ from the 20 GHz, 90° design discussed previously, with a material thickness of 15 mil, permittivity of 2.5, and transmission line width of 2.1 mm, equivalent to a Z_o of 30Ω.

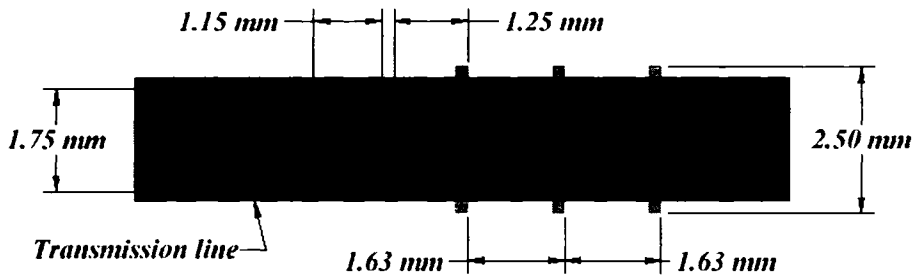
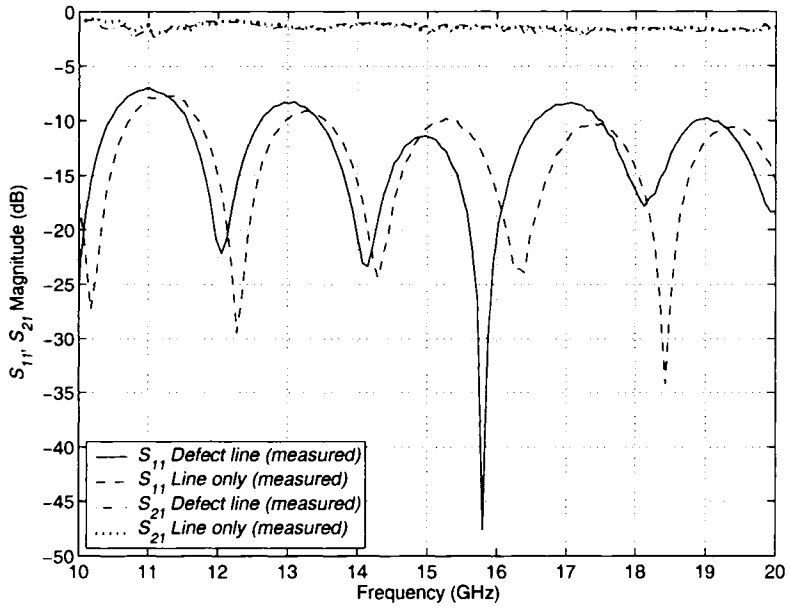


Figure 6.9: *Defected ground structure configuration.*

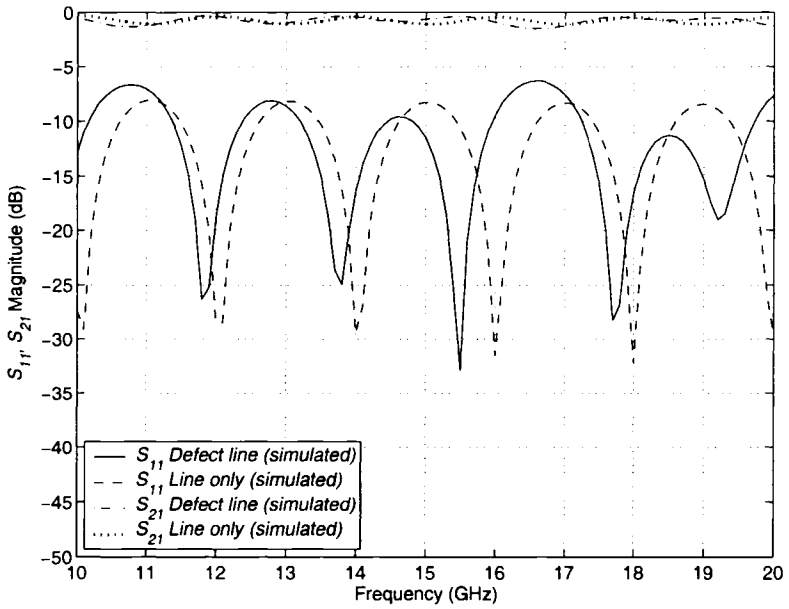
6.4.1 Candidate Performance

Measurements were performed using a vector network analyzer to obtain the *S*-parameter characteristics of a reference transmission line and the defect array independent of the membrane-control structure. The performance of the candidate structure was predicted using Ensemble 8.0. Both measurement and simulation results of the *S*-parameter characteristics are provided in Figure 6.10. The effect of the 50Ω terminations on the 30Ω transmission line is illustrated by the oscillating nature in the S_{11} and S_{21}. An S_{11} of less than –10 dB corresponds to an $S_{21} \geq -0.7$ dB (simulated), and a measured $S_{21} \geq -1.5$ dB.

Measured and simulated phase shift are contrasted in Figure 6.10 (c), with respect to an identical reference transmission line. Measured results indicate a differential insertion phase of 20° to 43° over the frequencies of 10 GHz to 20 GHz. Simulation predictions are slightly higher, from 24° to 55°, over the same frequency range. Some dissimilarity between measured and simulated data of the defect array is observed in the vicinity of 20 GHz, in both the phase and magnitude plots of Figure 6.10.

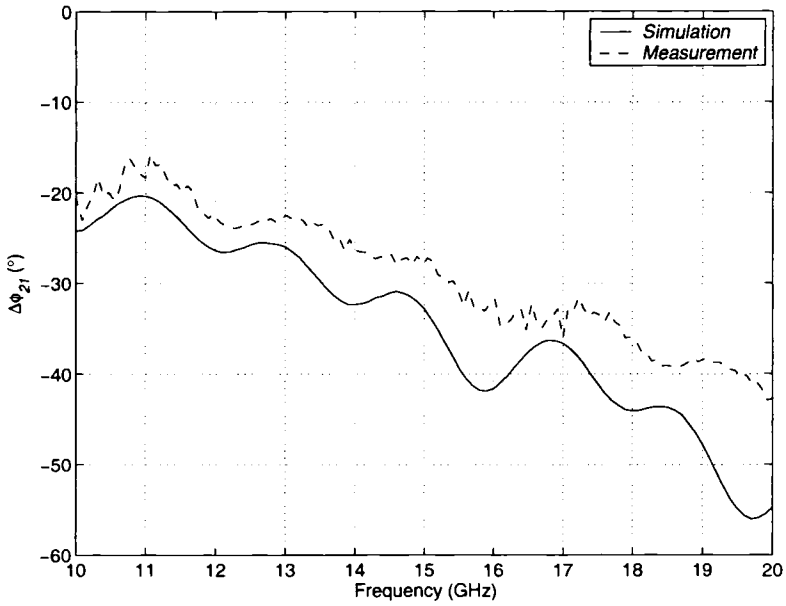


(a)



(b)

Figure 6.10: *(a) S_{11} and S_{21} (measured), (b) S_{11} and S_{21} (simulated), and (c) simulated and measured $\Delta\phi_{21}$ between the defect line and the reference transmission line.*



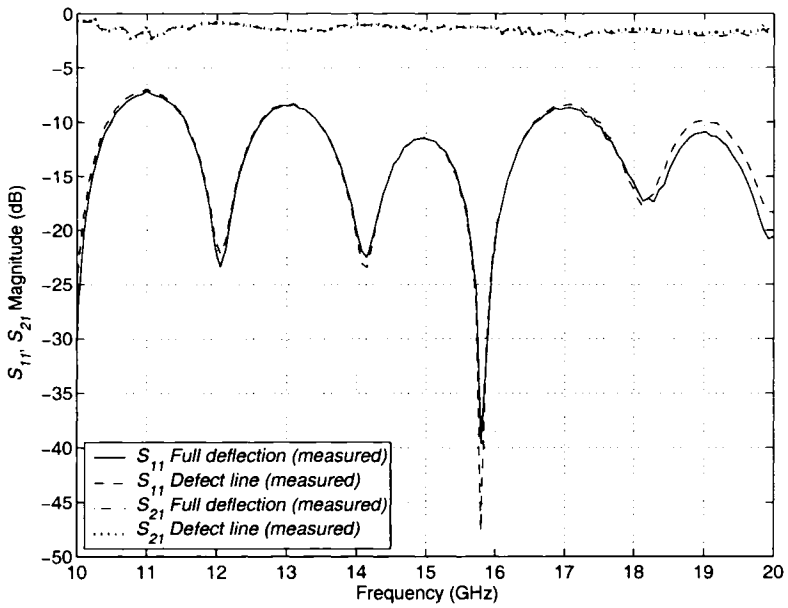
(c)

***Figure 6.10** continued*

6.4.1.1 Maximum Deflection

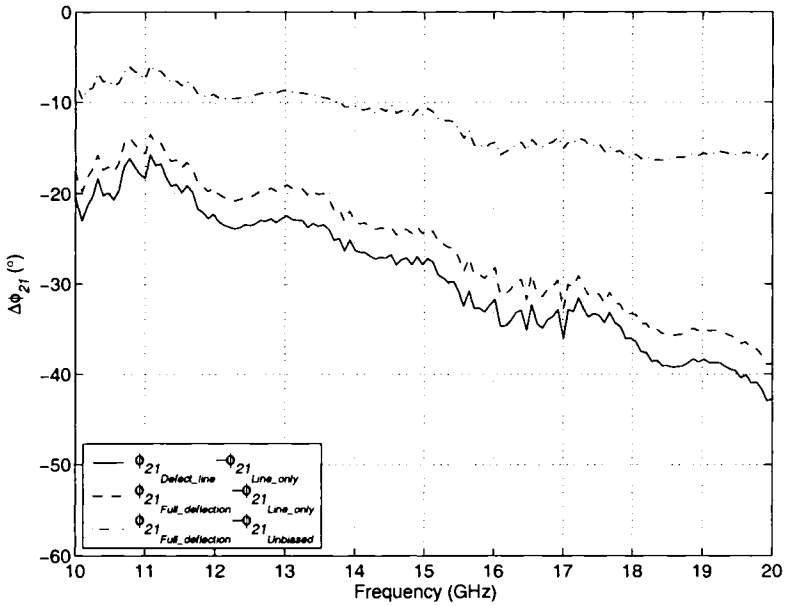
While the membrane-backed defect array can provide analog phase shift through continuous voltage variation, discrete DC voltages of 0V and 1500V were applied to the electrode. At maximum deflection of 0.4 mm, the *S*-parameter magnitudes are similar to the ground plane defect array when measured without the membrane backing. Ideally, at maximum deflection, measurements of the membrane-backed defect structure should be similar to the defect array. As shown in Figure 6.11 (a), under the condition of full deflection, the S_{21}, S_{11} of the membrane-backed defect array at full defection closely resemble the measured results of the defect array without the membrane (they are virtually identical). As well, the magnitude of the differential insertion phase with respect to the reference line, $\Delta\phi_{21}$, at full membrane deflection closely resembles the defect array, as illustrated in Figure 6.11 (b). The overall phase levels vary from approximately 20° at 10 GHz, to 40° at 20 GHz for the membrane-backed structure at full

deflection, and 20° to 43° for the defect array alone. The total line length of the measured sample was 5 cm, to facilitate measurement with the available sample holder. However, the membrane diameter was 1 cm. Therefore, the S_{21} corresponding to the phase shifter portion of the insertion loss is around 0.3 dB, when including the mismatch loss. Since the measured differential insertion phase at maximum deflection, and of the defect array alone, is 40° and 43° respectively, the corresponding FOM, with respect to the insertion loss, are 133°/dB and 143°/dB at 20 GHz, further indicating that the membrane does not introduce additional losses to the system.



(a)

Figure 6.11: *(a) Measured S_{11} and S_{21} of the membrane structure at full deflection and of the defect line; (b) measured $\Delta\phi_{21}$ of the defect line with respect to the reference line only, $\Delta\phi_{21}$ of membrane structure at full deflection with respect to the reference line, and $\Delta\phi_{21}$ of the membrane at full deflection with respect to the membrane at 0V.*



(b)

Figure 6.11 *continued*

6.4.1.2 Unbiased Condition

When unbiased, it is desired that the membrane act to short circuit the defect array, thus implementing a transmission line-only circuit. However, with the membrane in question, there is initial bending of the structure present when the membrane is not under any load, due to residual stresses resulting from the fabrication procedures [102]. A thermal evaporation technique was used for the fabrication of the copper membrane, which may be a significant contributing factor to this phenomenon. The heat associated with this procedure can impose significant stress on the copper and can contribute to the initial bending. Additionally, asymmetry in the membrane corrugations may be a strong contributing factor to this no-load bending. A KOH (potassium hydroxide) etching process is applied to etch the corrugation profile into the front-side of the silicon wafer [103]. The circular characteristics of the membrane are implied by what is in reality a many-sided polygon, since the KOH etch follows the crystal orientation of the silicon

[102]. Due to differences in the etch rate in contrasting planes of the silicon crystal, the corrugations are not symmetric, as shown in Figure 6.12. Stress distributed across the surface of the copper is not distributed evenly as a result.

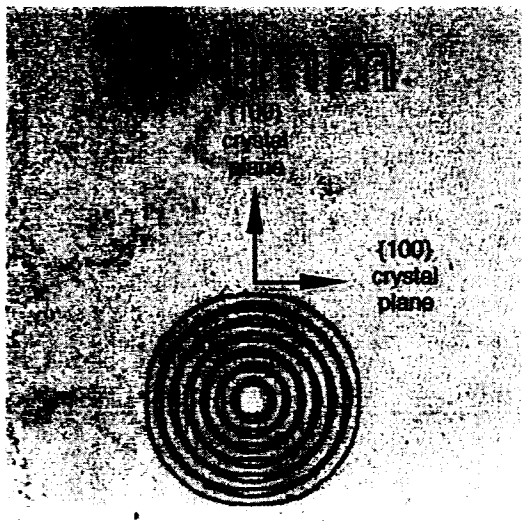
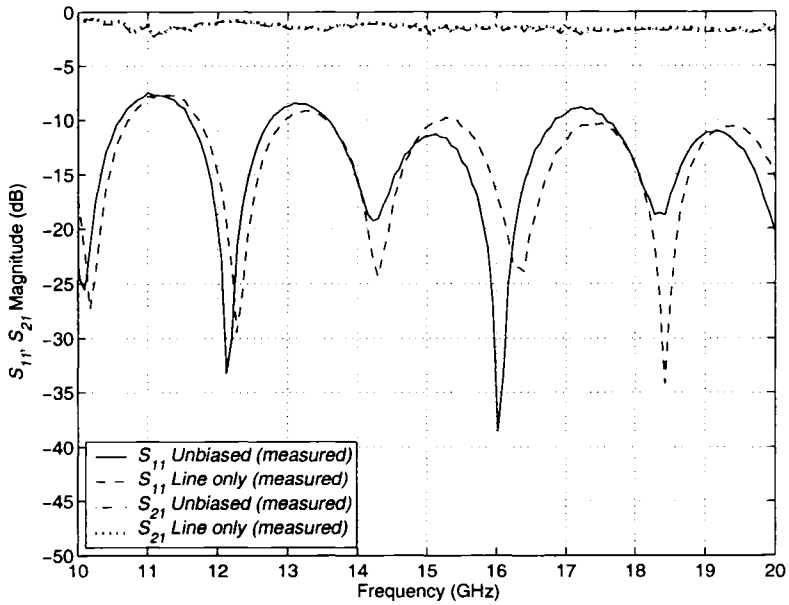


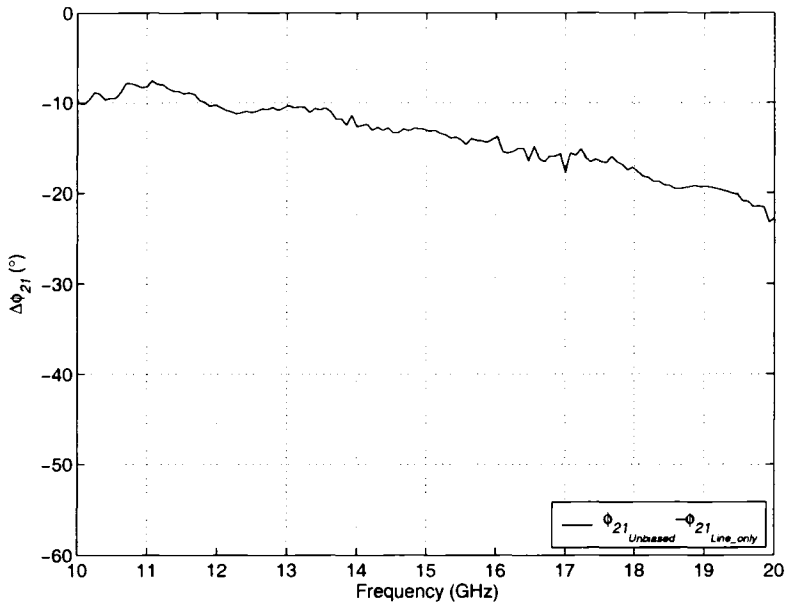
Figure 6.12: *Frontside KOH profile [103].*

The consequence of this no-load bending is shown in the plots of Figure 6.13 (a), contrasting the *S*-parameter magnitudes of the reference transmission line alone with the unbiased membrane backed defect array. While the trends are similar, the S_{11} and S_{21} of the unbiased structure and the reference line are not identical. Ideally, a differential insertion phase of zero should be observed, rather than the phase shown in Figure 6.13 (b). This phenomenon differs from the mechanism of "mechanical" hysteresis error, which is a function of applied mechanical stress [102], and was not studied by the membrane designers.

Potential stabilizing procedures to this bending phenomenon include annealing of the copper membrane, alternative materials suitable for electrostatic membrane operation, and/or considering an alternative copper deposition process. The option of considering alternative membrane geometries may resolve the issue of corrugation asymmetry. For example, a corrugated bridge architecture rather than a circular diaphragm would possess corrugations along a linear path and thus irregularities in the corrugation width resulting from a KOH etching process can be resolved.



(a)



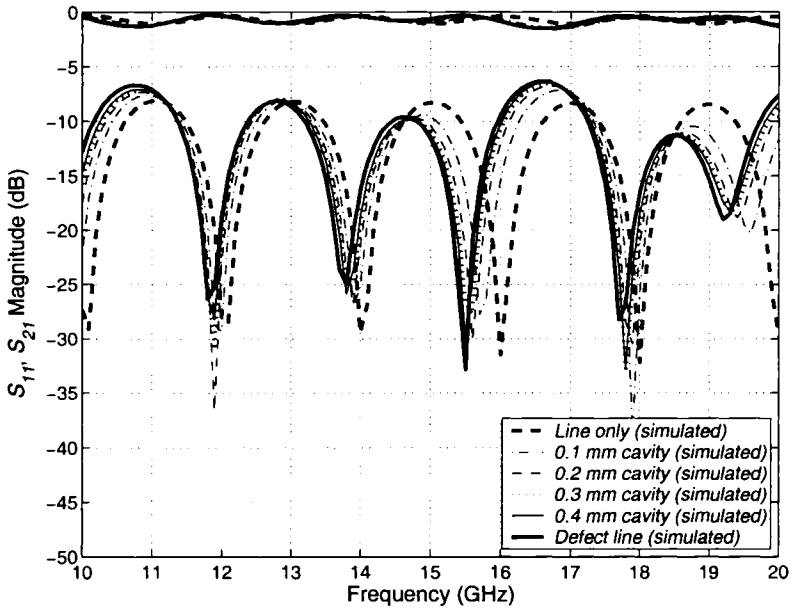
(b)

Figure 6.13: *(a) S_{11} and S_{21} of the membrane structure at rest and of the reference line; (b) $\Delta\phi_{21}$ of the unbiased membrane structure with respect to the reference line.*

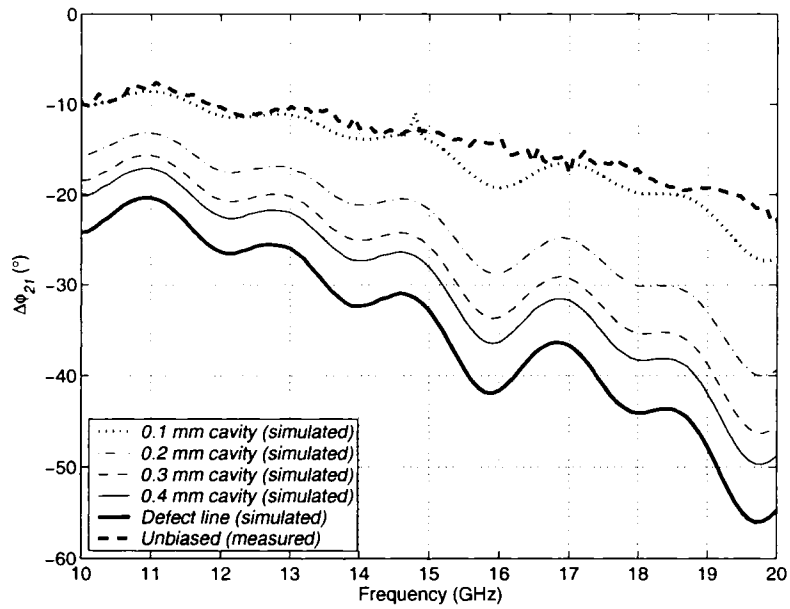
6.4.2 Air Cavity Simulations

The air cavity induced behind the defect array as the membrane is deflected was modelled assuming parallel-plate geometry between the ground plane of the defect array and the membrane. This is in contrast to the actual membrane, which possesses a curvature with a peak deflection at its center. Simulations of the structure shown in Figure 6.9 were performed using Ansoft's Ensemble 8.0 as a means to confirm the measurement data. Discrete depths of 0.1 mm, 0.2 mm, 0.3 mm, and 0.4 mm were considered. The S_{21}, S_{11}, and $\Delta\phi_{21}$ are given in Figure 6.14. The simulation results illustrate a slight shift in frequency from measured data, and an increase in the $\Delta\phi_{21}$ over frequency with an increase in the parallel-plate separation. The *S*-parameter characteristics approach the data for the individual defect array as the plate separation is increased. This trend is also observed in the differential insertion phase, which indicates a predicted phase shift ranging from 20° up to 50° by the 0.4 mm cavity simulation. This result approaches the predicted phase of the defect array without the membrane backing, ranging from under 25° to 55°. These values predict slightly greater $\Delta\phi_{21}$ than the measured differential insertion phase of 40° and 43°, at maximum deflection and by the defect array alone, respectively.

The measured phase shift observed for the unbiased membrane condition as discussed in the previous section, i.e. the differential insertion phase of the unbiased membrane-backed defect array with respect to a reference transmission line, was superimposed on the phase plot in Figure 6.14 (b). From a comparison of the phase curve with respect to the simulated data for the discrete cavity structures having depths of 0.1 to 0.4 mm, it can be inferred that a an unbiased deflection depth of approximately 0.1 mm may be present in the membrane. This approximation is in agreement with laboratory measurements by the membrane designers, which set the magnitude of this unbiased deflection at 130 μm. The simulated and measured level of this initial deflection is similar to the results also observed in Figures 6.6 and 6.7, for the membrane-backed single large slot and small slot defect experiments.



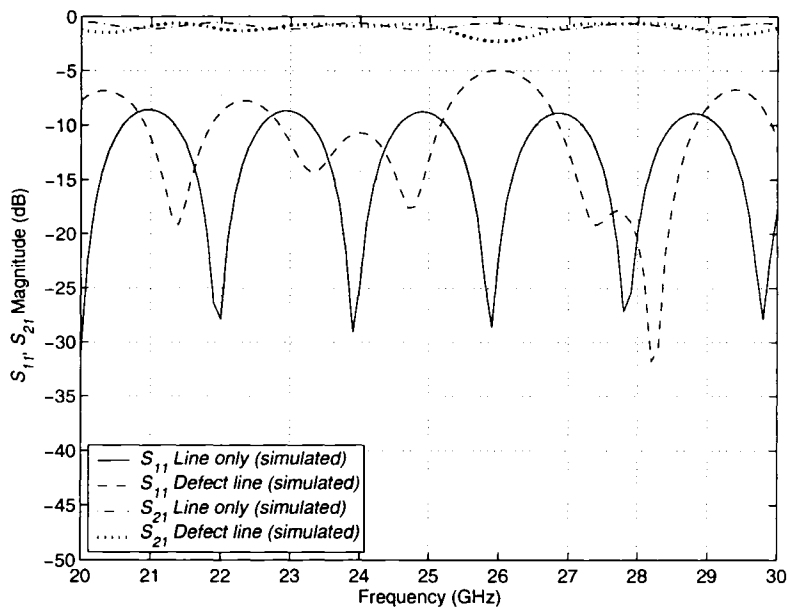
(a)



(b)

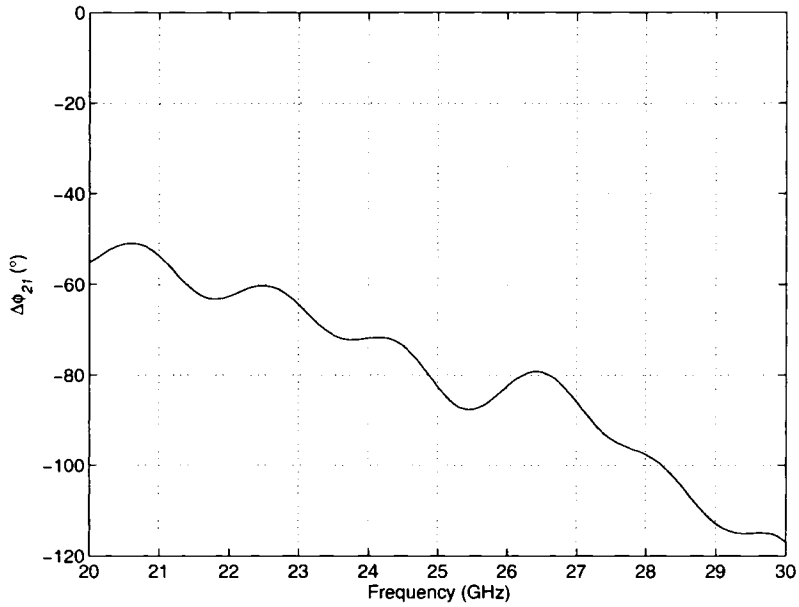
Figure 6.14: *(a) S_{11} and S_{21} of the simulated reference line, parallel plate structures, and the defect line; (b) $\Delta\phi_{21}$ of the simulated parallel plate structures and the defect line with respect to the reference line, and $\Delta\phi_{21}$ of the measured defect line with respect to the unbiased membrane condition.*

With reasonable agreement existing between the measured and simulated data, simulations of the defect array and the reference line were extended from 20 GHz to 30 GHz. For simulated S_{11} levels at less than –10 dB over this frequency range given in Figure 6.15 (a), the associated S_{21} is greater than or equivalent to –0.9 dB. As shown in Figure 6.15 (b), up to 117° of phase is achievable with this structure at 30 GHz.



(a)

Figure 6.15: *(a) S_{11}, S_{21}, of the simulated reference line, and the defect array, and (b) $\Delta\phi_{21}$, over 20 GHz to 30 GHz.*



(b)

Figure 6.15 *continued*

6.5 Implementation of the Membrane Actuator at High Frequency

The initial studies and designs proposed in Chapters 3, 4, and 5, were set for a conservative frequency of 10 GHz, to ensure that the measurement of prototypes were easily achieved, and to facilitate computation time by the commercial simulators used in this thesis study. However, from the discussion provided in 6.2 to 6.4, the required voltage to actuate a membrane having the characteristics detailed in 6.3 is very high. If the 10 GHz defected ground structures presented in Chapters 3, 4, and 5 were to be actuated by the membrane presented in 6.3 and 6.4, a membrane pull-down depth of at least 1 mm would be required. If a membrane were to be designed with the necessary air-cavity, but having the insulator, corrugation and thin-film characteristics of the structure in 6.3 and 6.4, actuation would require a voltage in excess 9000V, an impractical voltage requirement to say the least. A decrease in the absolute slot width would allow for a reduction in the necessary membrane pull-down distance.

6.5.1 Air-Gap Requirements

In considering a reduced width for w_{slot}, the following air-gap dimensions are practical for the existing defect designs present in Chapter 3 to 5:

- 400 μm air-gap for $w_{slot} \leq 0.20$ mm
- 300 μm air-gap for $w_{slot} \leq 0.15$ mm
- 200 μm air-gap for $w_{slot} \leq 0.10$ mm
- 100 μm air-gap for $w_{slot} \leq 0.05$ mm
- 60 μm air-gap for $w_{slot} \leq 0.03$ mm

The deflection depth indicated for each w_{slot} considered is twice the width of the slot. Figure 6.16 shows the required voltage levels for the deflections listed above. The membrane characteristics detailed in sections 6.3 to 6.4 were held constant for these calculations:

- Radius, $R = 5$ mm
- Membrane thickness, $t = 1$ μm
- Corrugation depth, $H = 10$ μm
- Corrugation period, $L = 126$ μm
- Insulator thickness, $t_g = 0.1$ mm

Membrane architecture with a 400 μm air-gap was implemented during the measurements of section 6.3. The actuation voltage in these experiments was 1300 V, which is similar to the voltage indicated by the 400 μm trace of Figure 6.16. It is also apparent from Figure 6.16 that the range of controllable deflection is somewhat limited, for a membrane with the characteristics listed above. As the deflection depth is increased, the controllable level of deflection drops from 71%, for the 60 and 100 μm air-gaps, to 69% in the case of the 200 μm wafer, 68% for 300 μm, 66% for 400 μm. Beyond this level of voltage control, the membrane response is immediate, resulting in a snap-action response over the remaining depth of the cavity.

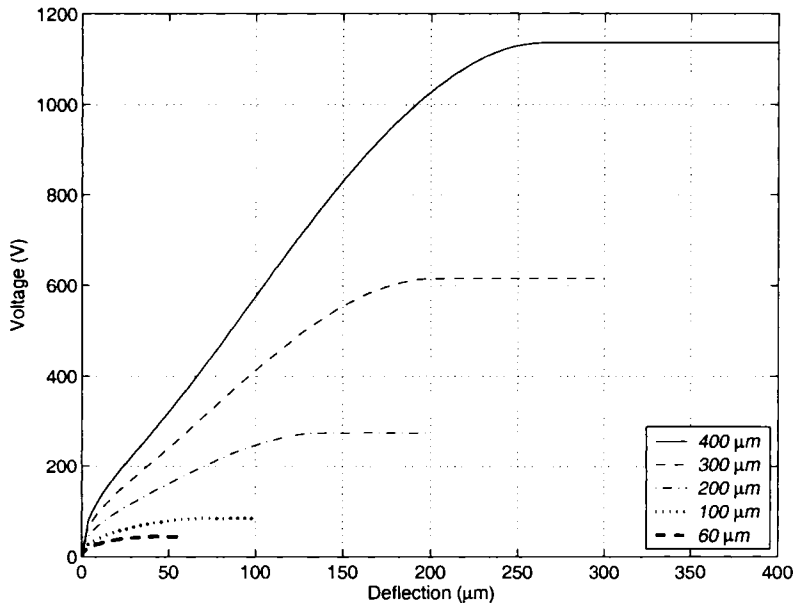


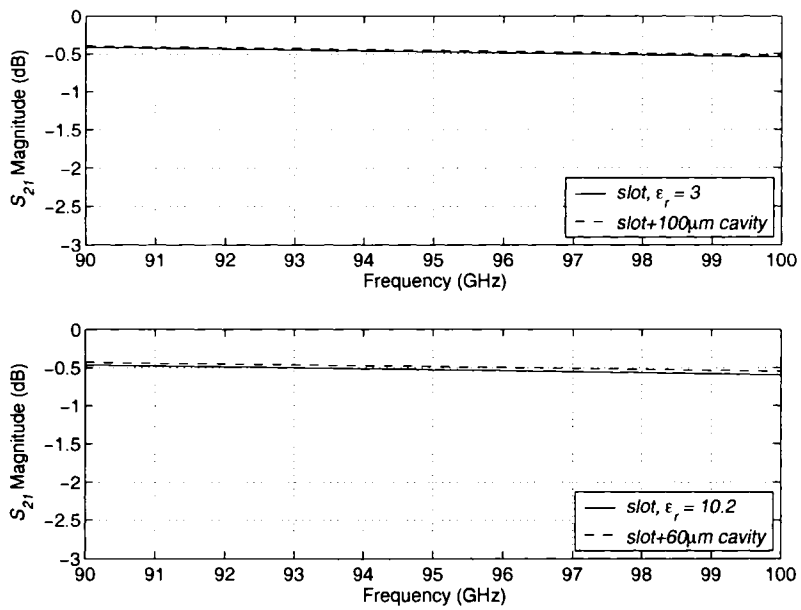
Figure 6.16: *Effect on voltage actuation due to variation in available pull-down depth.*

6.5.2 High Frequency Operation

A practical implementation of the slot widths selected in the previous section without considering a complete re-design of the defect structures in this thesis is to consider high frequency operation. Unlike the defect structure, which must be scaled for frequency operation as in the 20 GHz case discussed in section 6.4, the membrane geometry need not be adjusted for a change in frequency. The necessary depth of the membrane cavity is dependent only on the characteristics of the defect. Thus, while the electrical dimensions of the slot remain the same but physically become smaller and smaller as the frequency is made higher, the membrane structure is unaffected by frequency, in fact electrically increasing in size. This actuation structure is thus most practical for high frequency operation since the required actuation depth is reduced as the defect cavity-actuation dimensions for desirable phase shift lessen with increasing frequency.

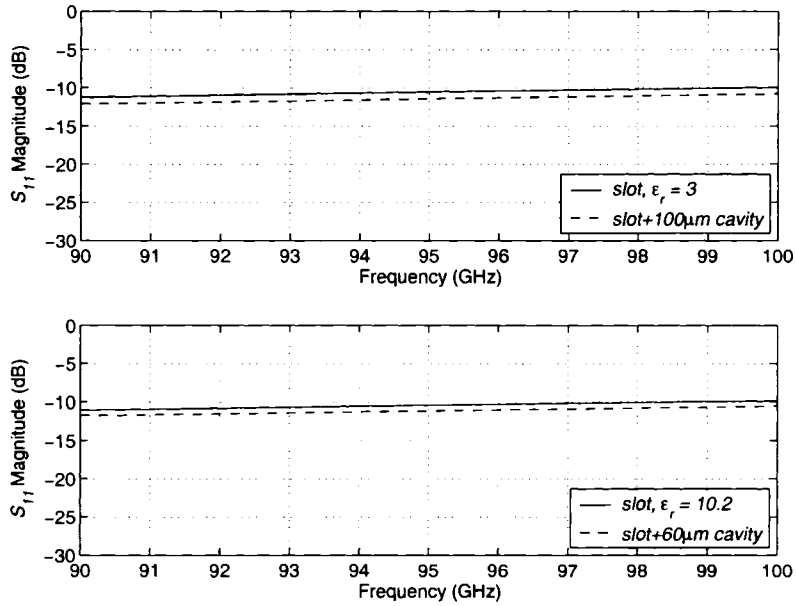
By scaling the defect structures presented in Chapter 3 to 5, they can be implemented for use at a higher frequency, as was presented in 6.4, and the necessary

distance for membrane deflection to approximate an open slot structure will be reduced. The original 50Ω line+optimized slot in Chapter 3, for $\varepsilon_r = 3$, $h = 0.508$ mm (20 mil), l_{slot} = 4.5 mm, w_{slot} = 0.5 mm, can be designed for operation at 100 GHz, by scaling the substrate and slot dimensions by 10. In doing so the slot width will be reduced to 0.05 mm, adequate for a membrane wafer thickness of 100 μm. In addition, the structure detailed in Figure 3.11 of section 3.2.4, having the substrate and defect parameters of ε_r = 10.2, h = 0.276 mm (10.9 mil), l_{slot} = 2.66 mm, w_{slot} = 0.271 mm, if scaled to 100 GHz can be operated with a membrane having a pull-down depth of at least 54 μm. This is illustrated below in Figure 6.17 over frequencies ranging from 90 to 100 GHz. An air-cavity of 60 μm is considered for the $\varepsilon_r = 10.2$ structure, and of 100 μm for $\varepsilon_r = 3$. With the membrane dimensional parameters listed in 6.5.1, the voltage to deflection relationship for a 100 μm and 60 μm cavity is highlighted in Figure 6.18.

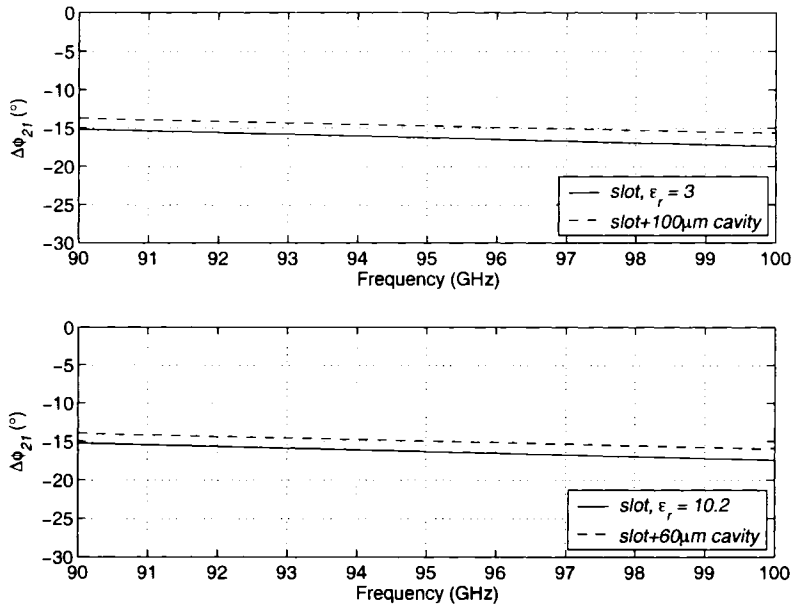


(a)

Figure 6.17: *Comparison of single open-slot with cavity backed-slot around 100 GHz. Two cases: $\varepsilon_r = 3$, $l_{slot} = 0.45$ mm, $w_{slot} = 0.05$ mm, 50Ω line, and $\varepsilon_r = 10.2$, $l_{slot} = 0.266$ mm, $w_{slot} = 0.0027$ mm, 28Ω line. (a) S_{21}, (b) S_{11}, (c) $\Delta\phi_{21}$.*



(b)



(c)

***Figure 6.17** continued*

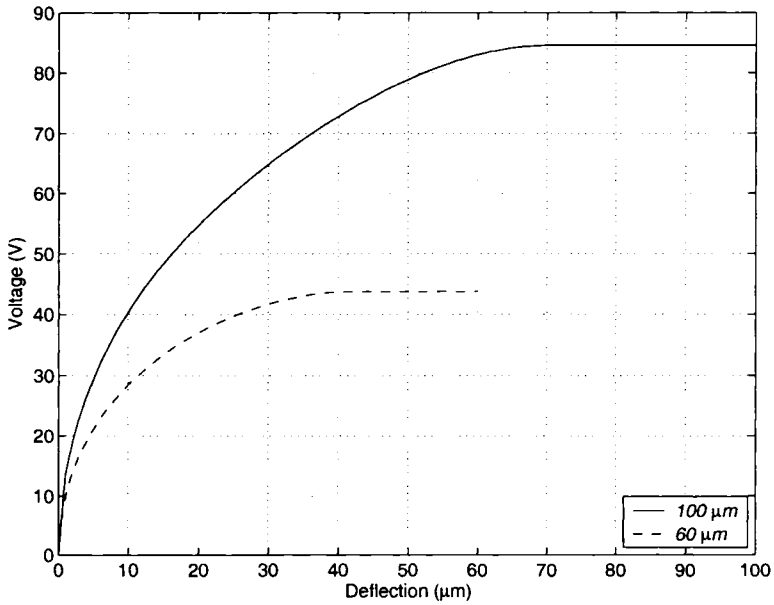


Figure 6.18: *Voltage vs. deflection for wafer thickness of 100 μm and 60 μm, R = 5 mm, H = 10 μm, L = 126 μm, t = 1 μm, t_g = 100 μm.*

6.5.3 Membrane Design for Optimal Phase Shift and Voltage Reduction

6.5.3.1 Voltage Reduction Schemes

Excluding the fabrication and integration of the complete membrane/slot device, practically, the implementation of the membrane structure is dependent on the reduction of the actuation voltage to more manageable levels. Membrane voltage can be decreased dramatically by adjusting some of the key parameters of the membrane structure. Some of these parameters can be determined by referring to equation (6.6),

$$\text{i.e.} \qquad V = \sqrt{\frac{2kz(d-z)^2}{\varepsilon_{eff}\pi R^2}} \tag{6.6}$$

It is apparent from (6.6) that a reduction in distance *(d-z)* separating the membrane from the electrode would result in a voltage decrease. The required magnitude of *(d-z)* was shown to be approximately twice the slot width, in order to achieve the complete phase shift possible by the open slot structure. The pull-down depths of 60 μm and 100 μm suggested in the previous section would be ideal for use with defect structures, as their voltage levels for actuation can be made to be reasonably low. With the original membrane structure, the voltage levels while less prohibitive than 1100V, are between 44V and 85V as shown in Figure 6.18.

From (6.6), there are considerable options that can be pursued to improve the voltage performance of the membrane, in particular for actuation to 60 μm and 100 μm. These include the following:

- The absolute thickness of the silicon wafer can be decreased towards the minimum required distance for deflection necessary for optimal phase, i.e. $2w_{slot}$ = 60 μm or 100 μm. The thickness of the silicon wafer controls the dimension t_{air}, the available air-gap for deflection. Reduction in the air gap is realistic if phase compromise is acceptable, or if the defected ground structure is designed with a reduced slot width. This alternative suggests that the membrane-backed design lends itself to high frequency operation, where the slot width would become physically small, and require a significantly reduced deflection distance.

- Because d represents the distance from the driving electrode to the membrane under zero bias, it is inclusive of the thickness of the insulating layer, t_g. Therefore, reducing t_g would result in a reduction in d, necessitating a lesser actuation voltage. The minimum thickness for t_g is properly selected knowing the desired limit for the maximum actuation voltage and the breakdown voltage of the insulator material, to ensure isolation between the membrane and pull-down electrode.

- The implementation of larger membrane diameters, rather than smaller structures for similar deflection would require a lesser voltage, since the actuation voltage is inversely proportional to the membrane radius, R. During experiment, the diameter was 10 mm, which when considering microscopic dimensions, is already significant. It was thus decided to maintain R at 5 mm for this study.

- The depth H of the membrane corrugations influences the stiffness k and linear range of deflection via its relationship with q. Altering this structural parameter will offer further membrane versatility. The actual shape (e.g. sinusoidal profile), period L, and consequently the number of corrugations, have little effect on the membrane stiffness and its displacement.

- Changing the thickness t of the membrane material offers an additional variable for the reduction in voltage. Like the membrane parameter H, it too shares a similar, but inverse, relationship with the quality factor q and thus influences the spring constant k.

6.5.3.1.1 Insulator Thickness

The breakdown voltage of the membrane insulator silicon dioxide (SiO_2) varies between 25000 V/mm to 40000 V/mm. This material property is the limiting criteria in determining the thickness of the insulating layer t_g, to ensure that the material acts as an effective insulator for the electrode. If a voltage limitation exists for actuation, the insulator will have a thickness that falls in a range between $t_{g\_low} < t_g < t_{g\_high}$, where:

$$t_{g\_low} = \frac{V_{\max}}{40000} \tag{6.14a}$$

$$t_{g\_high} = \frac{V_{\max}}{25000} \tag{6.14b}$$

It is desirable to obtain voltages below 100V, as this would be most feasible for practical applications. To err on the side of caution, (6.14b) is used to determine t_g. Table 6.1 lists possible thickness for select voltages less than 100V.

Table 6.1: *Minimum insulator thickness as determined by (6.14b) for select maximum voltage levels.*

Maximum voltage, V_{max} (V)	*Insulator thickness t_g (μm)*
1000	40.0
100	4.0
50	2.0
30	1.2
20	0.8
10	0.4

In the existing membrane, this dimension was fabricated at 100 μm. Since the existing maximum voltage, is 44V and 85V for 60 μm and 100 μm respectively, there is room to adjust the thickness of t_g. A voltage of less than 20V is not unrealistic for membrane actuation to 60 μm. For t_g, a value of 1.0 μm is selected to satisfy the level of desired maximum voltage. For 100 μm deflection, a more conservative voltage level on the order of 50V shall be considered, with an associated value of 2.0 μm selected for t_g. The voltage versus deflection characteristics associated with these values of t_g are shown in Figure 6.19. Reduction in the voltage levels is significant with this design adjustment, dropping to 17V and 41V, for the 60 μm and 100 μm cases, respectively, both actuation voltages below the threshold limit of 30V and 50V. However, there is some loss of analog control, with snap-down occurring at deflections of 22.8 μm for V_{max} of 17V (38% of 60 μm), and 46 μm (46% of 100 μm) for V_{max} of 40.6V.

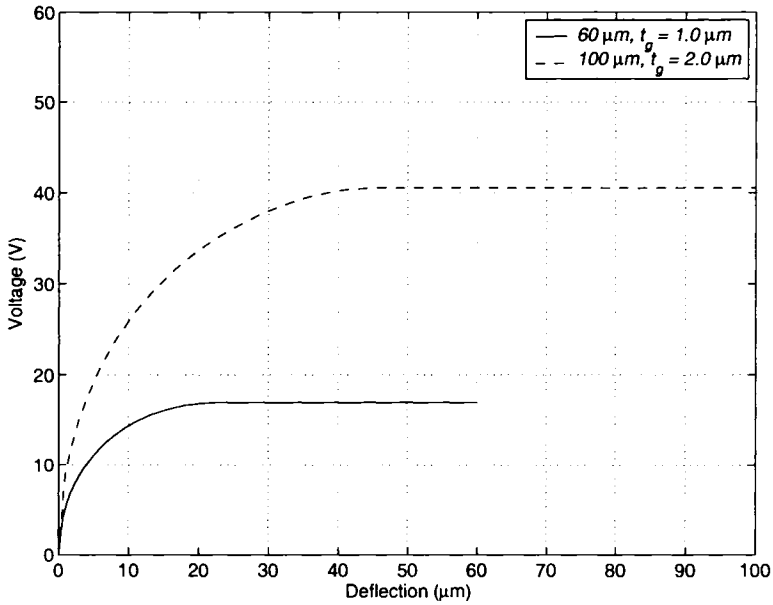


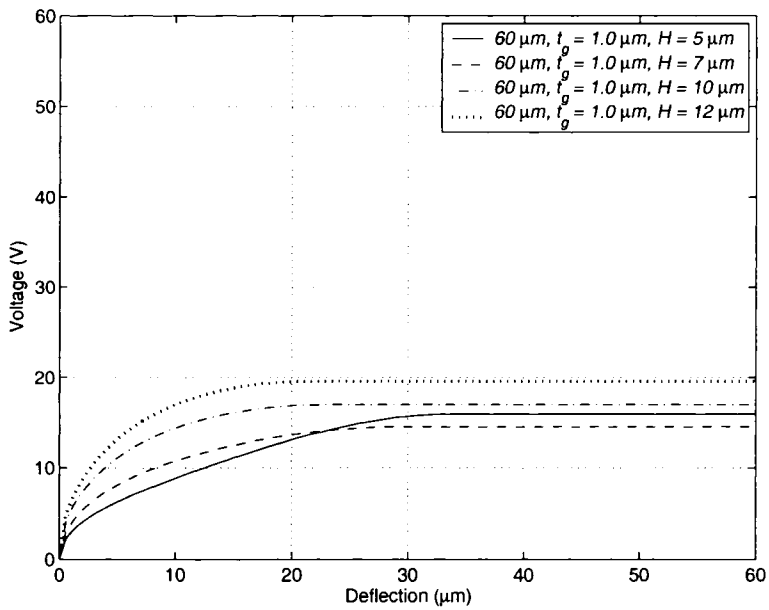
Figure 6.19: *Voltage vs. deflection characteristic following reduction of t_g to 1.0 µm for 60 µm cavity and 2.0 µm for 100 µm cavity.*

6.5.3.1.2 Corrugation Effect

The membrane corrugations provide additional flexibility to the thin-film copper structure, potentially easing the amount of voltage required for actuation. The structural corrugation variables introduced in section 6.1, include the corrugation depth H, the corrugation spatial period L, representing the wavelength between each corrugation, and the corrugation arc length S. The corrugation arc length can be easily calculated, knowing the depth of each corrugation, the period, and the incline of the corrugation (54.7° from the horizontal). The expression for k in (6.10) is dependent on the coefficients A_p and B_p in (6.11) and (6.12), respectively, in which they themselves are sensitive to the corrugation quality factor. Increases to q in (6.13) due to the increasing corrugation depth will result in rapid increases in A_p, while rapidly decreasing B_p [104]. As the first term in k is dependent on A_p, and the second on B_p, the membrane spring constant will rise as q increases due to the dominance of A_p. The depth of the corrugations can be altered to improve the voltage performance for actuation.

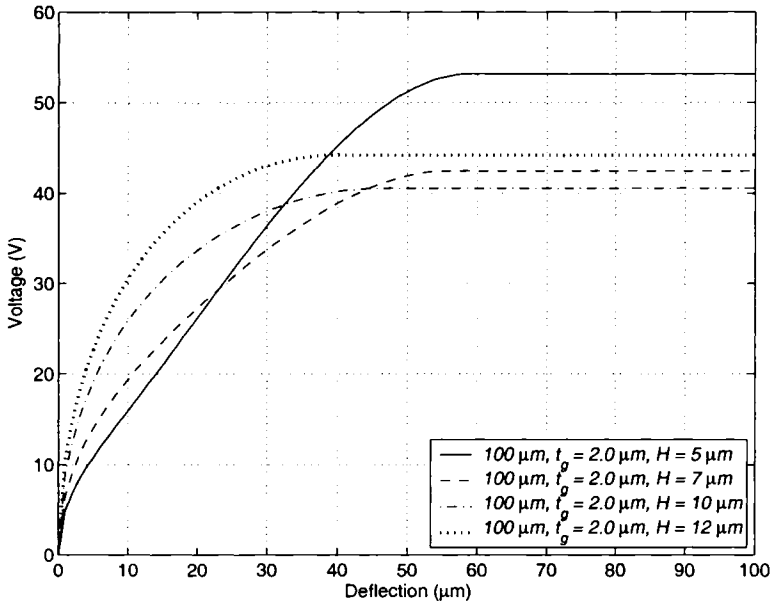
The fabricated membrane structure applied for measurements in 6.3 to 6.4 possessed a corrugation depth of 10 μm. For H values between 5 μm and 12 μm, the resultant voltage curves are shown in Figure 6.20. It is observed that some reduction in voltage levels is possible with H = 7 μm with the 60 μm cavity, from 17V to 14.5V. Improvement in analog control also occurs as a result of reducing H from 10 μm to 7 μm. A limit of 22.8 μm was possible in analog control with H = 10 μm for the 60 μm cavity. With H = 7 μm, this limit is raised to 29.4 μm, for a control limit of 50%. Selection of H below 7 μm resulted in increased voltage, but also improved analog control. For a magnitude of H above 10 μm, both desirable voltage and linear control is eroded. With the 100 μm cavity, there was no observed improvement in the voltage by changing H to one of the tested values.

Some attempt was made to adjust the corrugation period L, however, there was little to no effect on the maximum voltage levels, confirming statements in 6.5.3.1.



(a)

***Figure 6.20**: Effect of corrugation depth variation on the voltage and deflection relationship for a 60 μm and 100 μm cavity; (a) 60 μm, (b) 100 μm.*



(b)

Figure 6.20 *continued*

6.5.3.1.3 Membrane Thickness

When considering possible membrane thickness, the basic electrical properties of a conductor govern the selection of an appropriate dimension. Electrically, the skin depth of the membrane material at the operating frequency will determine the minimum material thickness. The skin depth is frequency dependent and is given by,

$$\delta = \frac{1}{\sqrt{\pi f \omega \sigma}} \tag{6.15}$$

Copper is the primary conducting material for the membrane, having a conductivity of 5.8×10^7 S/m. At 10 GHz, its skin depth is 0.661 μm, and at 100 GHz, it is 0.209 μm. There is therefore the possibility to reduce the membrane thickness from 1 μm, especially for higher frequency operation. Utilizing a membrane thickness of 0.8 μm offers the flexibility of applying the membrane from 10 GHz to 100 GHz, without concern for penetration of the RF signal through the membrane diaphragm. The voltage-to-deflection

relationship for t = 0.8 μm is given in Figure 6.21. A decrease of 7V in V_{max} to 33.6V was obtained for the 100 μm case, and a drop of 3V is observed for the 60 μm air-gap. Reduction in analog control occurs, with possible control existing over 46% for 60 μm, and 42% for 100 μm.

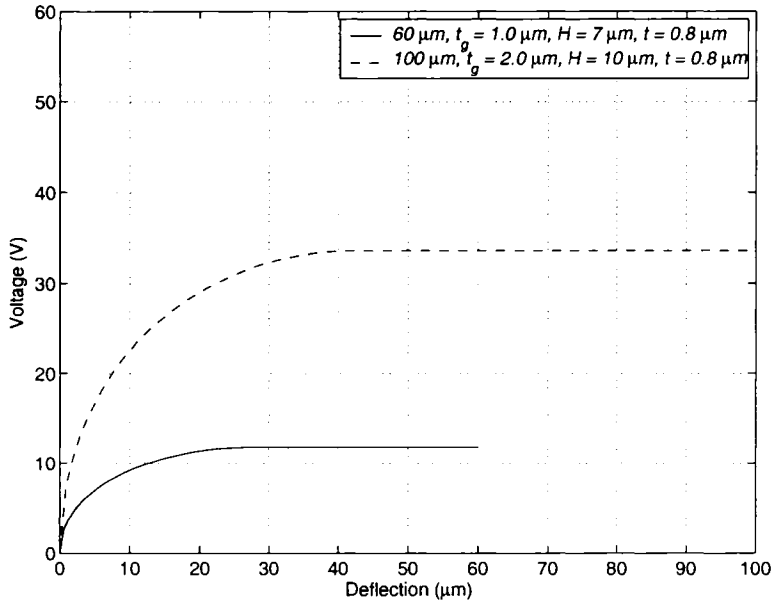


Figure 6.21: *Voltage vs. deflection characteristics following membrane thickness reduction from 1 μm to 0.8 μm.*

6.5.3.2 Optimal Phase Control

An attractive property of the membrane as control element for phase shift is the element of continuous phase shift. The final voltage-to-deflection relationship observed in Figure 6.21 indicates that significant voltage reduction is possible by the adjustment of membrane parameters within specific pre-determined guidelines, e.g. insulator dielectric breakdown, or material skin depth. However, the capacity for the membrane to act as an

analog phase shifter is restricted as the lower limits of voltage are attained. For analog control to be available, there must be voltage control over the desired deflection depth.

The three design parameters in 6.5.3.1 each influenced the potential analog control by the membrane. The overall depth of the gap between the two plates of the structure has a significant effect on this attribute. Thus, altering either the air region, or the insulator region will affect the quality of the phase control. With a larger parallel-plate region between the membrane diaphragm and the electrode, the necessary attraction force required for snap-down is not attained as rapidly as would be the case if the insulator were scaled to its minimum acceptable magnitude. Thus, the force for snap-down occurs at a greater deflection level and thus necessitates an increased voltage level for its realization.

- Knowing the necessary deflection depth, an air-gap of greater magnitude than required for deflection can be fabricated that possesses analog phase control over the desired deflection depth. For instance, the 100 μm trace in Figure 6.18 illustrates possible analog control to deflections of just under 70 μm. A membrane structure of similar wafer thickness may be considered when analog deflection control to 60 μm is necessary.

- The influence of the insulator on voltage control was observed in Figure 6.19, following the reduction in insulator thickness from 100 μm to 1.0 μm for the 60 μm air gap, and 2.0 μm for the 100 μm air gap. Implementing only the necessary wafer thickness for the required deflection while stacking the insulator dimension, also serves to increase the parallel plate region between the membrane and the electrode, and increase continuous phase control. This is evident when comparing Figure 6.18 to Figure 6.19.

- Corrugation depth was also shown to influence analog control as was observed in the previous section in Figure 6.20. The period and profile

have limited effect on the membrane performance. However, q and thus A_p, B_p, and k will be impacted should the ratio of S/L become significant.

Figure 6.22 illustrates voltage vs. deflection characteristics highlighting the design compromises outlined above for continuous deflection control. It should be noted that the samples shown in the plot of Figure 6.22 have not been optimized and are provided as a visual example of the suggested design alterations listed above. Four membrane design examples are shown in the figure and compared with the 60 μm air gap membrane of Figure 6.18, i.e. t_g = 100 μm, H = 10 μm, t = 1.0 μm:

- 60 μm air-gap with adjusted corrugation depth H from 10 μm to 5 μm
- 60 μm air-gap with adjusted corrugation depth H from 10 μm of 7 μm, and insulator thickness t_g of 140 μm
- 100 μm air-gap, with insulator thickness t_g of 50 μm
- 90 μm air-gap, with corrugation depth, insulator thickness and membrane thickness unchanged

It is evident form Figure 6.22 that continuous deflection and thus continuous phase control is possible through analog control of the actuation voltage. However, a trade-off exists between analog control and voltage reduction, as the voltage levels rise in the examples provided, in comparison to the 60 μm membrane of Figure 6.18.

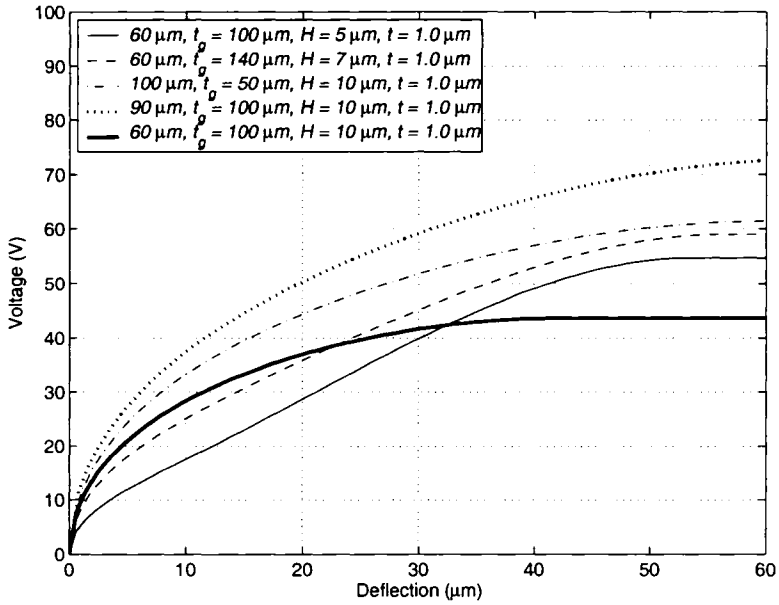


Figure 6.22: *Possible membrane design alternatives for continuous deflection control over 60 μm.*

6.5.4 Transmission Line Defect Design Alternatives

When considering the implementation of a corrugated membrane as a means of providing phase shift control, thorough consideration must be given to the required level of analog phase control, variability, frequency, and structural dimension. The membrane pull-down distance is a dimension that is relative the dimensions of the slot. Consequently, there is the flexibility of utilizing a specific membrane configuration at many frequencies of operation, limited only by the phase shift defect structure in the ground plane. It is possible to design the slot structures with a width less than 0.5 mm ($0.026\lambda_g$). Again, this dimension was selected for relative ease of fabrication. *S*-parameter characteristics of thinner slots were presented briefly in Chapter 3. A thinner slot implemented on a substrate identical to that utilized in Chapter 4 and 5, i.e. $\varepsilon_r = 3$, $h = 20$ mil, would undergo a slight lengthening of l_{slot}, if it is desired to maintain operation at 10 GHz.

A primary factor in the reduction in voltage level for necessary deflection is the reduction in the wafer air-gap to the minimum depth necessary for maximum phase shift by the defect structure. Lessening the pull-down distance between the electrode and the slot can reduce the voltage needed to actuate the membrane. It was observed that the deflection necessary to achieve the full phase shift obtainable by an open slot is dependent upon the width of the slot. Thus, by reducing the width of the slot, the deflection distance can be reduced, via a reduction in the thickness of the silicon wafer, and/or the insulating layer. This suggests that the membrane-backed slotted ground plane phase shifter is inherently suited for high frequency operation. The slot dimensions in section 6.4 were reduced by a factor of two for design at 20 GHz, to accommodate a more realistic pull-down distance for deflection. By reducing the dimensions by another factor of 2, the design can be scaled for operation at 40 GHz, with a slot width of 0.125 mm. At 0.125 mm, the required deflection for maximum phase shift becomes 250 μm. The wafer, insulator and corrugation parameters can be reduced accordingly, with the membrane radius remaining unchanged if desired.

However, if the air-gap depth is not sufficient, a consequence of the reduction of the wafer thickness is a decrease in the phase shift capability of the device, as the maximum deflection depth of the membrane is not adequate for the potential phase shift of the defect structure. Thus, the design of the membrane cannot simply be adjusted without considering the outcome with respect to the existing defect design. However, if the membrane structure is to remain unaltered, this consequence of phase loss can be addressed in a number of ways with respect to the design of the defect structure, most significantly by decreasing the physical size of the ground plane defect structure to compliment the membrane. In doing so, the following may be considered when attempting to achieve the desired phase at a specific frequency:

- Decreasing the defect line impedance
- Considering a reduction in the material thickness
- Increasing the permittivity of the transmission line substrate
- Selecting higher bit pairs to generate lower phase levels with reduced membrane displacement

The above compromises in the design of the defect structure offers a means to reduce the width of the defect elements by increasing the transmission line width, or selecting alternate material with thickness or permittivity levels that can offer dimensional reductions. However, in selection a thinner substrate or higher dielectric constant material, it must be recognized that higher substrate loss levels will be present.

The proposal to select higher phase producing defects suggests something of a phase compromise. By selecting a larger phase bit pair to generate a lesser phase level, as an example using a 90° configuration to generate 45°, the associated membrane can be actuated with a lesser control voltage to generate the desired phase level. This would also allow the potential for full analog control, as the membrane may function fully in its linear region. Also, if it is desired to use small membranes, a cascade of smaller bits may be used, each bit with their own membrane. If a restriction on membrane size is not present, an implementation with different phase bits, each of a physically different size, is possible, as in the proposed design of Figure 5.7.

6.6 Conclusions

This chapter investigated, implemented, and tested a novel micromachined membrane based phase shifter design, using ground plane defects. Initially, a cavity was placed below a ground defect and the influence of its height on the phase level was investigated. For the substrate parameters associated with the tested samples, it was shown that the full defect phase shift could be obtained as the cavity depth approached twice the defect width. This finding was used to set the range of the cavity depths in coming phase shifter designs.

A thin, conducting, micromachined membrane was used to implement the cavity structure below the defect. Sample prototypes using single and multiple defects for phase shift generation were fabricated and tested. The fabricated prototype membranes were dimensionally large and assembled using thick substrates, to simplify their fabrication. Consequently, the required voltage for membrane actuation was large. Despite this the membranes were actuated and the phase shifting properties of the membrane backed

defects were experimentally verified. The measured FOM values were 143°/dB for the defect array alone, and 133°/dB for the membrane-backed defect array at full deflection, indicating that the membrane does not introduce additional loss into the system.

Having established the successful operation of the membrane backed defect phase shifter, a study was conducted to determine design possibilities for reducing the required actuation voltage to levels that are commonly available in practice, e.g. for such systems as satellites, where voltage levels are normally less than 100V. It was shown that for such voltage levels the range of the membrane deflection must be small. This would promote high precision membrane integration, or operation at high frequencies, where the dimensional parameters are small. The precision requirements are however within practical range of RF circuitry and can be implemented by current fabrication technology.

CHAPTER 7

CONCLUSION

7.1 Conclusions

Chapters 3 to 6 provided in detail the research contributions of this thesis. In Chapter 3, the phase shifting properties of single uniform defect structures were examined. This involved a detailed parametric study that included the dimensional variables of the defect, as well as the specific substrate parameters. With regards to the defect dimensions, it was found that the phase shift magnitude increases with increasing the slot length and decreasing the slot width. The major finding of this study was that irrespective of the substrate parameters or slot dimensions, the maximum achievable phase shift of a single slot, when limited by a return loss of 10 dB, was approximately 18°. To minimize the return loss, the reflection of the slot may be eliminated by the addition of a second defect. In addition, with this paired slot configuration, the defect length could be increased beyond that selected at the 10 dB return loss limit for a single slot. Thus, the achieved phase by the paired slots was greater due to the presence of the second element, as well as due to the greater possible slot lengths. The figure of merit, defined as the achieved phase shift with respect to loss was examined with paired elements of different line impedance. A figure of merit of 487°/dB was obtained for 6 mm paired slots associated with a 25Ω line, which was larger than commonly reported in literature for other phase shift devices, as well as for identical slot configurations of greater line impedances.

The single defect geometry was further optimized in Chapter 4. Following investigation of the position of the slot beneath the transmission line and placement of a short across the slot, it was determined that the slot region below the transmission line was influential in increasing the phase shift produced by the individual element. A defect in the shape of a dumbbell was designed following a detailed investigation

of the dimensional gap widths and lengths of the slot directly below the transmission line. A minimum gap width was found to be influential for increased phase. The gap length was dependent on the slot length and line impedance, and approached half the slot length, as the line impedance decreased. As in Chapter 3, paired dumbbell elements were examined as matched systems. The figure of merits for the paired dumbbell elements studied also proved to be very high, up to 563°/dB for 6.5 mm pairs with a 25Ω line. A parallel circuit combination of an inductor and capacitor was presented for a single defect and was shown to be in reasonable agreement when compared with its full wave analysis. This circuit analysis was extended for paired combinations and was shown to successfully predict the optimum return loss separation for 4.5 mm paired dumbbells.

Chapter 5 proposed designs for defect loaded line phase shifters based on a philosophy of minimum size and minimum return loss. In the first case, two prototypes were fabricated and measured, and shown to provide the required phase shifts with a return loss of less than 10 dB, as designed and obtained through simulations. Measured figures of merit of 334°/dB and 455°/dB were obtained for the 3.5 mm element and 5 mm (matched) element phase shifter designs, respectively. With the second design philosophy, matched pairs were selected for their attractive return loss characteristics. The interaction between element pairs was found to be minimal if the inter-pair spacing was set larger than 3 mm, for the cases examined. From this conclusion, a cascaded design of matched element pairs were incorporated as a 4-bit phase shifter, as the differential insertion phases of each pair were additive and the entire structure was well matched. Utilizing the design philosophy of minimum return loss, the realization of a specific phase shifter design is more easily satisfied. The required spacing between the matched paired groupings is known and need not be optimized for the return loss or the additive phase, as in the case of the design implemented for minimum layout size.

Select defected line phase shifter designs were applied for use with a simple 3-element linear microstrip patch array. Array element phase shift progressions of –22.5° and –45° were examined and the resulting beam scans of the far field radiation patterns in the $\phi = 90°$ scan plane were computed for different element separations.

The patterns were in agreement with an identical undefected reference array, whose input port signals were excited by identical magnitudes and phase element progression levels, as in the defected array. The phase progressions provided by the defect phase shifters, over the array bandwidth, were found to be close to the theoretical values determined using the array theory.

Chapter 6 introduced the concept of reconfigurable ground plane defects based on an electrostatically actuated membrane. With this architecture, the electrode control voltage and the transmission line RF signal are physically separated, minimizing their signal interactions, and effectively reducing limitations in power handling capability resulting from signal distortion or switch malfunction. The membrane actuation allows continuous phase shift, eliminating quantization errors in an array beam scan. However, as a mechanical structure, the membrane deflection speed is controlled by its resonance frequency, which is in the kilohertz range. This will reduce the beam scan speed to the order of milliseconds, or hundreds of microseconds. Thus, the concept is useful for applications such as remote sensing, satellite broadcast, or smart hand set antennas, where the beam scan speed may not be critical.

Initially, an experiment was performed with the construction of a conducting cavity beneath a transmission line defect, and the cavity depth increased at discrete intervals. For the samples tested, it was shown that the cavity height significantly influenced the measured phase level, with the relationship of the cavity height for full defect phase approaching twice the slot width. Following this experiment a micromachined membrane was used to implement the cavity below the defect. In this case, the membrane electrode voltage provided control of the cavity height, thus allowing a continuous phase defected transmission line phase shifter. The sample membrane backed defect prototypes used during the experiment, utilizing single and multiple defects, were dimensionally large. As a result, the necessary actuation voltage was high. The successful operation of the membrane backed defect phase shifter was simulated and experimentally verified. The measured figures of merit of the defect array alone, and the membrane backed defect array at full deflection, were 143°/dB and 133°/dB, respectively, at 20 GHz, indicating that loss attributed to the

membrane is negligible. This may be compared with 86°/dB, at 18 GHz, for a semiconductor based phase shifter. This difference is expected to rise at higher frequencies, as the semiconductor losses become more significant.

The absolute dimensions of the defect phase shifter will decrease for high frequency operation. This will reduce the necessary membrane displacement distance, thus also reducing the required actuation voltage. Further reduction of the voltage levels were shown to be possible through the adjustment of the membrane material and structural parameters, including air gap and insulator thickness, corrugation depth, and the thin film copper membrane thickness.

7.2 Contributions

The novel contributions of this thesis research are summarized below:

- Proposing the ground plane defect as a phase shifting element.
- Presenting a full parametric investigation, based on substrate or slot dimensional parameters and establishing that for a return loss of 10 dB, the differential insertion phase shift of a single uniform slot is 18°, and 20° for a dumbbell shaped defect.
- Developing impedance matched paired elements and establishing that their differential insertion phase increases by reducing the line impedance.
- Establishing that the FOM increases with a reduction in line impedance.
- Determining that at 10 GHz, the FOM of paired element defect, approaches 400°/dB for 50Ω line and 600°/dB for 25Ω lines, considerably higher than the FOM of other existing phase shifting devices.
- Developing, and experimentally verifying, the defect loaded line phase shifter design technique for the minimization of overall size within a return loss threshold.

- Developing yet another defect loaded line phase shifter design technique through the cascade of matched paired elements, yielding an optimum impedance match.
- Developing a cavity backed defected ground plane phase shifter and establishing the relationship between the cavity depth and the full defect phase shift.
- Developing a reconfigurable ground plane defect structure using an electrostatically actuated membrane to enable phase shift control.
- Fabrication, testing, and performance evaluation of membrane backed defected ground plane phase shifters.
- Investigation and development of design techniques for low actuation voltage membranes.
- Development of novel reconfigurable defect loaded line hybrid digital-analog phase shifters using membrane backed matched paired elements of arbitrary phase bits, thus allowing paired element selection primarily based on membrane fabrication strategies rather than phase bit selection.

7.3 Future Research

The reconfigurable membrane backed ground plane defect phase shifter is a new concept and further research is needed to investigate its potential. Some immediate future research areas are:

- Alternative defect geometries for optimization of phase.
- Examination of the bandwidth performance of loaded line defected ground phase shifters.
- Alternative defect phase shifter architectures, e.g. switched-line, or reflection-type phase shifters.

- Design, fabrication and evaluation of low displacement membrane designs for high frequency, e.g. for Ka and W-band applications.
- Exploration of corrugated bridge vs. corrugated membrane architectures for the efficient reconfiguration of ground plane defects.
- Determination of stabilizing procedures for the reduction of membrane residual stresses, such as annealing of the membrane, alternative materials suitable for electrostatic operation, the consideration of an alternative deposition process, or alternative etching process, such as plasma etching.
- Evaluation of the switching speed attainable with electrostatic membrane actuators or alternative control architectures for use with defected transmission line phase shifters.
- Study of alternative actuation methods, such as piezoelectric or thermopneumatic, towards the reduction of actuation voltage.
- Investigation into the use of polymers and ceramic thin film material toward the reduction of membrane actuation voltage.

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