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**A MONOLITHIC BICMOS POWER AMPLIFIER FOR LOW POWER DIGITAL
RADIO TRANSMITTER**

by

Theodoros Varelas, Dipl. Eng.

**A thesis submitted to the Faculty of Graduate Studies and Research
in partial fulfilment of the requirements for the degree of
Master of Engineering**

**Department of Electronics
Carleton University
Ottawa, Ontario
December, 1992**

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submitted by Theodoros Varelas , Dipl. of Eng.
in partial fulfilment of the requirements for
the degree of Master of Engineering

Thesis Co-supervisor

Thesis Co-supervisor

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December 23, 1993.

ABSTRACT

This thesis reports on work that has been done on the design of a high frequency medium power amplifier suitable for digital radio applications. A class AB amplifier has been designed in a fine-line state-of-the-art BiCMOS process. The amplifier promises to provide 40 mW output power at 1.0 GHz, 29 mW output power at 1.6 GHz and 22.5 mW output power at 1.9 GHz. The circuit and the system environment that this amplifier is expected to operate in has also been studied during this design effort. It has been shown that such a BiCMOS power amplifier is suitable for directly driving the antenna of a low power personal communications transmitter. Issues of impedance matching and use of emitter follower shunt peaking are addressed as means of improving power efficiency and reducing distortion.

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Theodoros Varelas

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CHAPTER 1

Introduction

1.1 Motivation

A lot of attention is being paid at the present time to digital communication system applications such as wireless digital radio communications and fibre-optic data transmission. Monolithic integrated power amplifiers which can operate in the Gigahertz range are required for these applications. Until now, discrete component circuits have been used for the implementation of transmitter modules that operate in the Gigahertz region, because of performance limitations of the integrated devices and because of circuit tuning and impedance matching requirements.

Recent advances in silicon bipolar technology have resulted in the development of bipolar devices with high transconductance g_m , and high unity gain frequency f_T , and CMOS process compatibility with only minor process modifications [1]. High frequency integrated circuits such as voltage controlled oscillators (VCOs), mixers, amplifiers and phase comparators that are essential for a transceiver design have been presented recently [2]. The evolution of the technology makes the integration of all these circuits on a single chip transceiver feasible. BiCMOS technology

seems to be a real threat to other technologies in the race for the implementation of small and light weight personal communicators for the mobile digital radio applications, by allowing the direct implementation of one chip telecommunication systems that include the high frequency front-end module and the low frequency DSP part.

The last stage of a transmitter is the power amplifier. It is one of the most critical stages of the transmitter because it determines the power of the transmitted signal and it usually has a great impact on the transmitted signal quality. Until now, most of the power amplifiers that appear in the literature are able to transmit hundreds of watts and use silicon technologies that can have high power gain and can handle high power consumption. These technologies are not compatible with the technologies used in the design of the other stages of the transmitter, making the integration of all the stages on a single chip difficult if not impossible. In comparison, the power requirement for indoor and mobile communications systems is much lower; in the order of hundreds of milliwatts. Therefore, the design of monolithic integrated high frequency power amplifiers without using silicon technology specially made for the power devices seems feasible. One of the prime objectives of this thesis is to explore the opportunities provided by the new BiCMOS circuit technology to solve this problem.

1.2 Mobile Radio Transmitter

The choice of a suitable architecture for a mobile radio transmitter is primarily determined by the specific radio application standards. The

modulation technique is one of the standards that strongly affects the choice of one transmitter architecture over another.

Digital amplitude modulation, known as amplitude shift keying, seems to be out of the competition for mobile radio because of the severe impact of multipath fading upon the amplitude of the carrier. Frequency shift keying (FSK), in which different frequencies represent the level of the modulation code, and phase shift keying (PSK), in which discrete phase states represent the levels of the modulation code, are the preferred candidates for already implemented mobile radio applications or for the future ones, as Table 1.1 shows. Among them the Gaussian minimum shift key (GMSK) is the most popular.

Table 1.1 Various wireless systems [3]

System	Band (MHZ)	Channelization	Modulation
CT2	864-931	FDMA	GMSK
CT2+	930-931	FDMA	GMSK
DECT	1880-1990	TDMA	GMSK
GSM	890-915	TDMA	GMSK
PCN	1710-1785	TDMA	GMSK
IS-54	824-849	TDMA	$\Pi/4$ DQPSK
AMPS	824-849	FDMA	ANALOG FM
UDPCS	400-4000	TDMA	DQPSK

Currently two broad modulation techniques seem to battle for the designer's preference. The linear modulation technique requires a high

degree of linearity or low distortion in the translation from baseband frequencies up to the carrier frequencies and in the amplification. However, such modulation promises greater spectral efficiency. On the other hand, the constant envelope and/or continuous phase modulation technique can avoid the linearity requirements, resulting in a lower cost for the transmitter and in a more relaxed linearity specification for the power amplifier stage.

Figure 1.1. A simple transmitter architecture for continuous phase modulation

Figure 1.1 summarizes a low cost transmitter architecture based on a simplified continuous phase modulation technique described in [4]. The heart of the transmitter is a fractional-N frequency synthesizer as outlined

in [5]. A reference frequency f_{ref} is necessary to phase lock the voltage control oscillator (VCO) to a stable source. The output frequency f_O is a multiple of the reference frequency, $f_O = N f_{ref}$. By making the division rate N of the dual modulus divider a function of time, the instantaneous frequency or phase can be modulated. A power amplifier, the subject of this thesis, can then transmit the signal to the antenna.

1.3 Thesis Objective and Scope

The level of system integration of a mobile radio system that operates at frequencies greater than one GHz could be improved if the transmitter power amplifier stage were integrated on a single chip along with the previous stages. BiCMOS circuit technology may offer the circuit technology required to achieve this goal, and this thesis explores this possibility.

The work has concentrated on the key design issues that arose during the effort to design and lay out a monolithic bipolar power amplifier in BiCMOS that operates at frequencies higher than one GHz and has a supply voltage of five volts. Because a power amplifier is the last on-chip component, this work has also attempted to address some of the issues of interfacing the amplifier with the off-chip components required in such a transmitter, i.e. a matching network and an antenna.

The design, layout and experimental measurement of a complete transmitter is beyond the scope of the work. Many complex system and circuit issues must be solved before the complete design can be

implemented on a single chip with reasonable probability of success. Issues include modulation and demodulation schemes to reduce the high frequency analog component design complexities, and ways to lay out the circuit that reduce crosstalk and interference with sensitive analog circuits operating at radio frequencies.

The process technology used to implement the circuit design studied in this thesis was provided by Northern Telecom Electronics. High performance npn bipolar and complementary MOS transistors can both be fabricated within this BiCMOS process. The process features a polysilicon emitter bipolar transistor with a $0.8\text{ }\mu\text{m}$ wide emitter and (minimum) $7\text{ }\mu\text{m}$ base to base pitch, junction and field oxide device isolation, linear $750\text{ }\Omega/\text{sq}$ polysilicon resistors and three layer metallization for device interconnection. A unity gain frequency f_T of 10 GHz at a collector-emitter bias voltage of one and a half Volt ($V_{ce} = 1.5\text{ V}$) can be obtained by this technology for a minimum emitter size of $0.8 \times 4.0\text{ }\mu\text{m}^2$ [6] .

1.4 Thesis Outline

Chapter 2 attempts to describe the background knowledge that is necessary for this work. Various output driver topologies will be presented. These topologies will be evaluated in order to determine if they are suitable for radio frequency applications and for monolithic implementation with the current silicon technology. In addition, the system and circuit environment of the proposed design will be studied, because it strongly affects the power amplifier design.

A power amplifier design that can be monolithically implemented is designed and studied in Chapter 3. The problem of maximizing the power and the efficiency of a power amplifier that operates from a limited five volt power supply is more difficult when the amplifier operates at high frequencies. Chapter 3 will present the circuit design problems that arose from the effort, the effect of these problems on the amplifier performance, and possible approaches to maximizing the power and efficiency while alleviating the design problems.

Comparison between experimental and simulation results for an already existing power amplifier that is based on the same topology principle as the amplifier proposed in Chapter 3 will be presented in Chapter 4. This experimental work was done to evaluate how well the circuit simulators can predict the designed circuit performance.

Finally, some concluding remarks and recommendations for further research in this area are presented in Chapter 5 .

CHAPTER 2

Background

2.1 Introduction

Before being able to design a high frequency bipolar power amplifier one must first become familiar with the circuit elements and design principles necessary. In addition, one must become familiar with the effect that the system and circuit environment of the amplifier will have upon the amplifier design. This chapter will attempt to describe this necessary background knowledge.

2.2 Review of Output Stages and Power Amplifiers

A power amplifier usually consists of two stages, the output stage and the driving stage before it. The output stage must satisfy a number of special requirements. It must be able to deliver a substantial amount of power into a specified or deliberately chosen load, with acceptably low levels of signal distortion. A well designed output stage should be able to achieve these specifications while consuming low standby power and, in addition, should not cause a major limitation of the frequency response of

the overall amplifier. In this chapter, several output stages will be reviewed. A detailed analysis of output stages will be unnecessary, because their theory has been the subject of several books [7]. Instead, they will be categorized and their main characteristics, especially those of interest for the design of a power amplifier, will be highlighted.

2.2.1 The Emitter Follower as a Class A Power Output Stage

Figure 2.1 Emitter follower output stage

An npn-emitter follower output configuration shown in Figure 2.1 is chosen as an example. The internal biases are shown as current sources I_B and I_Q for simplicity, since most of the designers may realize these circuits

differently. The driving stage, consisting of Q_2 and I_B , is shown along with the output stage because it usually affects the performance of the output stage.

Even though the emitter follower can have a wide output swing under proper bias, it has unsymmetrical current drive capability. This is because the output transistor can only source current into the load, but cannot sink current. In other words, when V_A decreases, the maximum output current that can be drawn from the load is equal to the bias current I_Q of the output transistor. On the other hand, when V_A increases the output transistor can supply much larger currents, and a maximum positive output voltage swing that is equal to $V_{CC}-V_{CE(sat)}$.

Figure 2.2 shows the voltage transfer characteristic of the circuit of Figure 2.1. Since R_L is connected to the ground, V_O can be negative. It can be seen, if the load resistance R_L is sufficiently large to give the result that

$$V_{CC}/R_L < I_Q \quad (2.1)$$

then the current limitation will not be a problem and the output voltage can swing almost down to $-V_{CC}$. However, if R_L is not large enough to satisfy the inequality of equation 2.1, then the negative output swing will be limited to

$$(V_O\text{-max}) = -I_Q R_L \quad (2.2)$$

which will result in clipping for the negative input voltage V_A .

If I_Q is increased then the problem can be solved, but this will reduce the efficiency of the output stage since it increases the standby power dissipation.

The emitter-follower output stage discussed is an example of a class A amplifier. A class A amplifier is a linear amplifier; that is, the output signal is always directly proportional to the input signal. Such an amplifier conducts output current continuously during the complete cycle (360°) of a periodic input signal.

Figure 2.2 Voltage transfer function of the circuit of Figure 2.1

The major advantage of class A amplifiers is that they have low signal distortion due to their linearity. On the other hand, their major drawback is that they show poor conversion of dc input power (P_{dc}) to ac output power (P_{ac}). It has been shown that their maximum theoretical efficiency $\eta_{max} = P_{ac}/P_{dc}$ is only 25 percent [8] and that a typical maximum efficiency η_{max} for an IC emitter follower is 20 percent [9]. Both cases assume resistive load.

2.2.2 Class B Power Output Stage

2.3a. Simplified class B output stage

2.3b. All npn class B output stage

Class B power output stages can help to solve the low power efficiency problem of the class A stages, by having no power supplied when there is no input signal. By definition, an amplifier operates in class B mode when its output is a linear function of the input over 50 percent (180°) of the input waveform period.

Class B operation requires two output stages. One stage conducts for exactly one-half cycle of a periodic input signal and the other stage conducts for the alternate half cycle of the input signal. This kind of operation can be achieved by a double complementary emitter follower configuration shown in Figure 2.3a, also known as the "push-pull" configuration. The npn transistor conducts output current only when the input signal moves in the positive direction from its zero level, while the pnp transistor conducts output current when the input signal moves in the negative direction from the zero level.

Even though the complementary push-pull configuration is a good illustrative example of class B operation, its use is limited due to the lack of good pnp transistors. Substrate pnp transistors have limited current carrying capability in comparison with npn transistors. Also, pnp transistors are slower devices than npn transistors, because the hole mobility is at least three times less than the electron mobility. Therefore high frequency silicon and BiCMOS technologies are optimized for npn devices and pnp devices are not very common. All npn Class B output stages using only npn transistors like the one in Figure 2.3b, known as the totem pole configuration, have been suggested in order to overcome the limitations of the pnp structures.

The class B configuration has a maximum theoretical power efficiency of 78.5 percent, which is much higher than the class A configuration efficiency [10]. However, class A amplification produces less distortion than class B. Class B output stages suffer from crossover distortion, which occurs because of the nonlinear behavior of the bipolar transistors [11]. The silicon BJT requires its base to emitter junction to be forward biased by

approximately 0.7 volts before significant collector current flow, and this produces a threshold or dead zone, as will occur in the Figure 2.3a example.

The crossover distortion can be reduced by using class AB operation, which requires the output transistors to be slightly forward biased. In this case, the output voltage is a linear function of the input for more than 50 percent (180°) of the input waveform period but less than 100 percent (360°). Because some idle current will flow through the amplifier when there is no input signal the efficiency of class AB operation is between the efficiency of class A and class B, depending on the bias current levels.

2.2.3 Class C Power Output Stages

Class C operation occurs when the output stage conducts during less than a half cycle of the input signal. A simplified class C amplifier is shown in Figure 2.4 to illustrate the class C principle of operation. The collector load consists of a parallel LC circuit which is tuned to the frequency of the input signal. The periodic output current flows through the resonant circuit and generates a sinusoidal output voltage.

The theoretical efficiency of the class C operation can reach 100 percent. The efficiency factor for an inductively coupled transistor amplifier as given by H.L. Krauss et al. [10] is

$$\eta_{\max} = (2\theta - \sin 2\theta) / 4 (\sin \theta - \theta \cos \theta) \quad (2.3)$$

where θ is defined as one half of the conduction angle of the input waveform period. This is plotted in Figure 2.5. It can be seen from the plot

that when the efficiency tends towards 100 percent the conduction angle tends towards zero, forcing the output power to also tend towards zero. Therefore a compromise between good efficiency and high output power results in typical efficiency values around 85 percent [12].

Figure 2.4 Simplified class C output stage

Class C is a very nonlinear mode of operation. For amplitude modulation systems this presents considerable difficulty as the nonlinearity of the power amplifier causes unwanted spectral components to appear at the output of a transmitter. Some of these components are harmonically related to the carrier frequency and can be filtered and reduced to a negligible level, but often frequency components appear very close to the wanted signal due to intermodulation and cannot be removed by filtering. In order to avoid nonlinearity problems and still take advantage of the high efficiency of class C operation many linearization

techniques have been suggested [13]. However, these techniques may result in more complex systems that are more difficult to fully integrate in high frequency applications. Class C amplification is more acceptable when amplitude modulation is not present as in continuous phase Frequency Shift Keying. In this case, band pass filtering after the amplifier is required to remove harmonic frequency components arising from the amplifier nonlinearity. However, this not a major limitation, so class C amplifiers are more acceptable for continuous phase or frequency modulation.

Figure 2.5. Efficiency factor (from [10])

2.3 Gain Saturation

Amplifiers can be considered as a form of power converter. They convert both dc power, P_{dc} , and input ac power, P_{in} , to output power, P_o ,

at a specific frequency. Let us consider the two port power amplifier of Figure 2.6. The total power input must be equal to the total power output,

$$P_{in} + P_{dc} = P_o + P_{dis} \quad (2.3)$$

where P_{dis} is the dissipated power.

Defining power gain as : $G = P_o/P_{in}$ then

$$P_{dis} = P_{dc} - (G-1) P_{in} \quad (2.4)$$

Equation 2.4 shows that if the power gain G remains constant and greater than unity and P_{dc} is limited, then as the input power P_{in} increases, at some level of the input power the dissipated power P_{dis} would become negative. This is clearly in opposition with the fundamental rules of thermodynamics, and therefore the power gain cannot remain constant [14].

Figure 2.6 Active circuit power conservation

Figure 2.7 presents a typical output power versus input power for an amplifier. As the input power increases, a direct linear gain occurs in the output power until the output power saturates, as shown, and further increase in the input power no longer produces larger output power. Gain saturation is therefore defined as the saturation of the output power of an amplifier for a fixed dc power supply. Note that no assumptions about the

linearity of the devices used in the amplifier were made. Even if the devices were considered ideally linear, gain saturation would still occur as long as the amplifier operates with a finite source of dc power supply. If we define nonlinearities to include clipping because power supply limits have been reached, in addition to device nonlinearities, then nonlinearity is the mechanism which causes gain saturation to occur in general.

Figure 2.7 Output versus input power for an amplifier

Device nonlinearities reduce the gain saturation level resulting in reduction of the conversion efficiency. Conversion efficiency of an amplifier is defined as the ratio of the output signal power to the dc power of the amplifier:

$$n = \frac{P_o}{P_{dc}} \quad (2.5)$$

Equation 2.5 shows that maximum efficiency can be achieved when the output power is maximum, if P_{dc} is limited. Achievement of maximum output power requires nonlinear amplification within the amplifier as the saturation region condition is approached, because the output power keeps increasing in the nonlinear saturation region until it reaches the saturation point.

One of the main objectives of power amplifier design is to maximize power gain and efficiency. The most common ways of doing this are

- i) to optimize circuit techniques at the output stage, and
- ii) to use optimum loading and impedance matching

At the same time the quality of the transmitted signal is expected to be kept within certain specifications so that it can be reproduced by the receiver. Using NTs BiCMOS process a power amplifier that can be part of a single chip transmitter is restricted to operate from a single 5V power supply. This restriction forces the designer to operate the amplifier close to or in the gain saturation region, in order to achieve maximum output power and efficiency. Of course, the consequence of operating in a nonlinear region is the introduction of nonlinearities into the transmitted signal, such as AM/PM modulation, AM/AM modulation and intermodulation distortion, that may severely affect the transmission quality.

AM to PM modulation occurs in circuits whose phase characteristic depends on the instantaneous amplitude of the input signal. If a small amplitude (envelope) perturbation is assumed, these devices can be presented as a device with a AM/PM coefficient of K degrees/dB, Figure

2.8a. As an amplitude modulated signal passes through the device, K degrees of phase change of the output signal are produced for every decibel of variation in the amplitude of the input signal. For example, if the input voltage, V_{in} , to an AM/PM converter is

$$V_o = \text{Re}[u(t) e^{j\theta}] \quad (2.6)$$

then the output voltage V_o is

$$V_o = \text{Re}[u(t) e^{j(\theta + k u(t))}] \quad (2.7)$$

Similarly AM to AM modulation occurs in circuits whose gain characteristic depends on the instantaneous amplitude of the input signal. In this case the circuits can be characterized by an AM/AM coefficient K' dB/dB, Figure 2.8b. This describes the change of the amplitude of the output signal, in decibels, for every decibel of amplitude variation of the input signal. Let V_{in} be the input voltage to an AM/AM converter and be described by equation 2.6. Then the output voltage is

$$V_o = \text{Re}[(u(t) + K' u(t)) e^{j\theta}] \quad (2.8)$$

Figure 2.8a. AM to PM converter

Figure 2.8b. AM to AM converter

When the circuits operate in the linear region, the conversion coefficients K and K' are constant and cause linear AM/PM and AM/AM modulations that are easy to remove or compensate for. In the nonlinear

operation region, K and K' are functions of the amplitude of the input signal and this results in severe distortion of the output signal.

Intermodulation occurs when two or more signals pass through a nonlinear device. Suppose two frequency tones F_1 and F_2 are passed simultaneously through a nonlinear device. It has been demonstrated, in [15] for instance, that the nonlinearity of the device produces cross-products that generate new frequency components at frequencies that satisfy the following expression:

$$F_{m,n} = m F_1 \pm n F_2 \quad (2.9)$$

where m and n are positive integers, and $F_{m,n}$ is the frequency of the $m+n$ intermodulation product.

The effects of this nonlinearity can be reduced by :

- i) circuit techniques
- ii) system techniques

and iii) the use of certain modulation/demodulation techniques that are not severely affected by these nonlinearities

The major objective of all these approaches is to avoid a large reduction (back-off) in the output signal level relative to the maximum signal level that the amplifier can produce. For a multi-carrier operation, frequency division multiple access (FDMA) systems are more sensitive to the intermodulation problem because two or more signal carriers, operating at closely adjacent frequencies can occur in the same time slot. To reduce the consequences of intermodulation the amplifier will then usually require a generous back-off, in the range of 3-10 dB, that can not be afforded by a system that operates from a low voltage supply. Time

division multiple access systems (TDMA) tend to ease the intermodulation problem, because they transmit single modulated carriers at different time slots. The major consideration for TDMA systems is spectral spreading and AM/PM conversion in the amplifier, but they can generally operate much closer to saturation than FDMA systems.

Assuming that only a single modulated carrier signal is transmitted through the power amplifier, the amplifier can be used even closer to saturation if the transmitted signal has constant or near-constant envelope. In this case, there is not any AM and therefore AM/PM conversion does not occur. Unfortunately, in practical situations the modulated carrier signal is bandlimited, for example by IF filtering. The bandlimiting of the modulated carrier signal results in a ripple on the envelope. Therefore, the AM/PM conversion problem is not totally solved but is only reduced because the ripple amplitude is usually a small percentage of the envelope amplitude. In addition, if such a signal is fed to an amplifier that operates close to saturation, the envelope ripple is reduced resulting in a bandwidth increase that usually appears as spurious emissions in adjacent channels.

One of the most effective ways of improving the linearity of an amplifier at low frequencies is the use of negative feedback, but at microwave frequencies only a small amount of feedback may be applied because of stability problems. Because we are considering mostly narrowband modulation schemes, the output of the amplifier can be mixed down to lower frequencies, allowing the feedback to take place at lower frequencies. This way more feedback can be applied without risking instability. This method is often called the modulation feedback technique.

Two different linearization schemes that use the modulation feedback technique have been reported in [16]:

- 1) In a Cartesian Loop transmitter the modulated wave is carried in two channels known as the in phase (I) and quadrature (Q) channels. These two channels are mixed down to the required lower frequency and are then linearized by the system feedback.
- 2) In a polar loop transmitter the modulated wave is expressed in terms of instantaneous amplitude and phase of the carrier signal, and therefore two feedback loops are also required here to reduce the distortion caused by the high frequency components. One loop is required to correct the amplitude distortion and the other to correct the phase distortion.

The modulation feedback technique is based on two principles [17]. Firstly, the feedback is arranged in such a way that it contains only the modulation information of the amplified signal. Secondly the frequency of the feedback signal is much lower than the amplifier bandwidth. In this way, it is possible to have stable operation with a large amount of feedback.

The fractional-N Synthesizer, which is basic to the transmitters shown in Figures 1.1 and 2.9, inherently carries these two principles for a constant envelope continuous phase or a constant envelope frequency modulated signal, assuming that the power amplifier is inside the loop. In this case, only one feedback loop is required to linearize the phase or the frequency, assuming that there is not any amplitude modulation. The feedback to the phase detector contains the modulated information and has N times lower frequency than the carrier signal because it is fed through the dual modulus divider.

Figure 2.9 A simple transmitter architecture for continuous phase modulation

With the amplifier in the phase lock loop (PLL), as Figure 2.9 shows, the feedback cancels the incidental phase modulation caused by the nonlinear amplifier, allowing the use of the amplifier in the saturation region for higher power and efficiency. When the power amplifier is placed in the PLL and after the voltage controlled oscillator (VCO) the combination of the VCO and the power amplifier can be treated as a high power output voltage controlled oscillator (VCO'). The VCO' appears more nonlinear than the stand alone VCO but its nonlinearity is tolerable if the loop bandwidth is sufficiently larger than the modulating frequency. Therefore, in the case of a narrow band modulation, the loop bandwidth

can be made large enough to allow a high gain feedback to reduce the VCO' nonlinearities.

Alain Blanchard [18] has shown that a high power signal with pure spectrum can be achieved when the high power signal is derived from an oscillator that can be frequency modulated. The phase of the modulated signal can be "locked" to the phase of a signal of low power. The output signal will then have the power of the modulated signal and the spectral purity of the low power signal. Petrovic et. al. support this argument with experimental results for a VHF SSB polar-loop transmitter in [19], where they achieve outstanding linearity for the transmitter even though they use a nonlinear amplifier. They show third-order intermodulation products 61 dB lower than the carriers in a two-tone test.

The above result will apply for narrow-band constant envelope continuous phase modulation transmitters. In this case the polar loop technique can apply but there is need for only a phase feedback loop, as shown in Figure 2.9, because there is no amplitude modulation.

2.4 Output Impedance and Optimum Loading

The output power, gain and efficiency of an amplifier depend significantly on the load that the amplifier drives. The nature and the size of the output impedance of the amplifier determines the optimum load for that amplifier. It also affects the design of the matching network when the load is predetermined. In this section, the output of the emitter

follower will be reviewed because the emitter follower is often part of the output stage of class A, class AB and class B power amplifiers.

2.4.1 Emitter Follower Output Impedance and Transfer Function

The small signal a.c. model of a single transistor emitter follower is shown in Figure 2.10. The high frequency output impedance is given as [19]

$$Z_{out} = R_o \frac{1 + \frac{s}{z_1}}{\left(1 + \frac{s}{p_1}\right) \left(1 + \frac{s}{p_2}\right)} \quad (2.10)$$

where R_o is the low frequency output resistance,

$$z_1 = \frac{R_b + r_\pi}{r_\pi R_b (C_\pi + C_\mu)} \quad (2.11)$$

$$p_1 = \frac{1 + B_0}{r_\pi + C_\pi} \quad (2.12)$$

$$p_2 = \frac{1}{R_b C_\mu} \quad (2.13)$$

and

$$B_0 = g_m r_\pi \quad (2.14)$$

For the condition $p_1 > z_1$ and $p_2 > z_1$ the output impedance $|Z_{out}|$ of the emitter follower increases with increasing frequency. This is the behavior of an inductive impedance. If the emitter follower is driving a capacitive

load the inductive output impedance and the capacitive load will form a resonant circuit.

Figure 2.10 Small signal a.c. model of an emitter follower

The transfer function of the emitter follower in Figure 2.10, when capacitively loaded, is given as [2]

$$A_v(s) = \frac{V_{out}}{V_{in}} = \frac{A_{vo}(1-s z_1)}{\left(\frac{s}{\omega_{ef}}\right)^2 + \frac{2\zeta_{ef}}{\omega_{ef}}s + 1} \quad (2.15)$$

where

$$A_{vo} = \frac{R_E(1+B_o)}{R_b + r_{\pi} + (1+B_o)R_E} \quad (2.16)$$

and

$$z_1 = -\frac{g_m}{C_{\pi}} \quad (2.17)$$

ω_{ef} is the undamped natural frequency, which is given by

$$\omega_{ef}^2 = \frac{g_m}{R_b (C_\pi C_L + C_\mu C_L + C_\mu C_\pi)} \quad (2.18)$$

and ζ_{ef} is the damping factor

$$\zeta_{ef} = \frac{\omega_{ef}}{2} \left[\frac{(C_\pi + C_L)}{g_m} + R_b \left(C_\mu + \frac{C_\pi}{g_m R_E} + \frac{C_L}{1 + B_0} \right) \right] \quad (2.19)$$

The transfer function shows that the capacitively loaded emitter follower acts as a second order filter and therefore an underdamped response is possible. Peaking of the emitter follower frequency response is undesirable in most applications because it may cause excess phase shift and instability in the overall circuit response. However a carefully designed circuit can take advantage of the frequency response peaking. A capacitor can be used as a tuning element that can tune the gain peaking at a frequency of interest and therefore increase the output power of the circuit at that frequency. This is useful only in the case that the phase shift caused by the emitter follower does not make the circuit unstable.

2.4.2 Impedance Matching

An amplifier can be described as a generator with a complex impedance $Z_{out} = R_g + j X_g$. It is well known that the maximum power transfer between a generator, i.e. amplifier, and a load Z_L is achieved when the load is the complex conjugate of the generator impedance, $Z_L = R_g - j X_g$. This condition represents equal power dissipation at the generator and the load and that means that the efficiency of the power transfer is 50 percent

[20]. In practical situations, the amplifier does not drive the load directly. A transmission line is used to interconnect the amplifier with the load. The transmission line must be terminated with its characteristic impedance if reflections are to be eliminated and all the incident power is to be transferred to the load. Maximum power transfer can be achieved if the output impedance of the amplifier is transformed to provide a conjugate match for the characteristic impedance of the transmission line. High frequency transmission lines essentially have real characteristic impedance so this reduces the transformation requirements to a simple resistive match at both ends of the transmission line. In general, the amplifier output impedance and the load impedance are not equal to the characteristic impedance but lossless matching networks can be inserted to provide the conjugate match, as shown in Figure 2.11.

The impedance transformation in the matching network could be performed by lumped elements, i.e. capacitors and inductors or by transmission line matching elements, i.e. stubs. The choice between these two options is based upon the frequency of operation and the circuit technology. In this work, the frequencies of interest are from one to two Gigahertz. This frequency range corresponds to wavelengths between 15 to 30 centimeters. Typical lengths for transmission line matching elements are a quarter of a wavelength, one eighth of a wavelength and three eighths of a wavelength [21]. Considering these element lengths as the guideline for the choice between lumped elements and transmission line elements one can see that at one Gigahertz the length of the transmission line elements suggest the use of lumped elements for the matching networks because they result in a more compact design. However as we

reach the two Gigahertz range, the size of the transmission line elements is significantly reduced and they become strong candidates for the matching networks. In the low Gigahertz region the choice between lumped and distributed elements is not clear and sometimes the combination of both can give the solution to the matching problem [22].

Figure 2.11 Amplifier-load interconnection

2.5 Summary

Background knowledge that was considered necessary for the design of a high frequency BiCMOS power amplifier was presented in this chapter. Various types of output stages suitable for power amplifiers were presented. Their advantages and disadvantages, regarding high frequency and low power monolithic implementation were addressed. The class C output stage is very efficient but it is nonlinear at the same time and it

cannot be fully integrated on silicon yet. On the other hand, the class A output stage shows very good linearity but low efficiency. The best compromise between efficiency and linearity seems to be the class AB output stage.

The linearity issue is very important. Because the linearization of the amplifier tends to be difficult at high frequencies, alternative ways for linearization were studied. System level architectures that can help in that effort were reviewed. The modulation feedback techniques were found to be very promising, and a simple transmitter architecture for a continuous phase modulation that can improve the linearity of the amplifier was presented.

The next chapter will present the design of a high frequency medium-power amplifier.

CHAPTER 3

Design Approach

The design of this amplifier is not driven by a certain set of specifications. However, it is bounded by certain requirements that would make it useful and adequate for a single chip transceiver. In this chapter, these requirements will be presented and the design philosophy that was followed to satisfy them will be explained.

3.1 Class of Operation

The class A amplifier is favored by IC designers for microwave frequencies where it is difficult to employ other classes of amplification. However, its low efficiency suggests that it should be avoided, if possible, for a mobile radio application where power consumption must be low, to allow long battery life.

The demand for high efficiency suggests the use of either class B or class C operation. The latter one requires the use of a resonant LC circuit, as already described in the previous chapter. That means the use of external components, mainly inductors, resulting in reduction of the level of integration and in cost increase. In addition, the necessary bias circuitry

for a class C operation is quite complicated and may also require the use of external components. Miniature inductors fabricated directly on silicon have already appeared in the literature, but they suffer at present from low Q values and they are not yet well modeled and characterized [23]. However it seems that well characterized inductors might be available in the near future, possibly resulting in easier implementation of class C amplifiers.

Class B operation appears to be more promising for monolithic implementation because it does not require the use of external components, but it suffers from crossover distortion. Class AB operation that is biased as close as possible to the class B mode for better efficiency seems the most realistic design approach. Due to lack of good pnp transistors, the totem-pole output stage approach is considered as the best candidate. A variation of a totem-pole approach has been presented by Dr. R.G. Meyer and W.P. Mack [24] and is shown in Figure 3.1. This has been adapted as the basic amplifier topology for this thesis work.

The totem-pole output stage is driven by two amplifier stages that amplify the input signal. The input signal is split into two paths that we will call the upper path and the lower path. For negative input voltage swing, the upper path inverts the signal and the transistor Q₁ drives the load towards more positive output voltage, while the transistor Q₂ that acts as a current source is turned off. For positive input voltage swing, the output voltage moves negative as the current source Q₂ is boosted to increase the negative current handling capability of the output stage, while the idling current and control of the overall amplifier transfer function is still controlled by Q₁.

Figure 3.1 Basic amplifier topology

3.2 Power Requirements and Restrictions

The use of a five-volt BiCMOS technology for the design of this power amplifier imposes a main restriction on the power that this amplifier may be able to deliver into a 50 Ohm load. Because of the use of the totem pole configuration, the maximum output voltage swing can be 2.5 V peak value if the saturation voltage is considered zero. If we consider a saturation voltage of a half volt then the maximum output voltage swing will be two volts. That translates into 40 mW output power if this voltage swing can be transferred onto a 50 Ohm load. The output power can be doubled if the basic amplifier cell is used in a differential topology.

3.3 Differential versus Single-Ended Topology

Good dynamic range is very difficult to achieve in high frequency operation. Most high frequency analog circuits have small voltage swings in order to give high operating speeds. A differential drive topology provides an improvement to the dynamic range of these circuits because it doubles the available voltage swing, and therefore it is highly favored by high frequency analog circuit designers.

The use of fully-differential topology reduces signal harmonic distortion. Banu and Tsividis [25] have demonstrated that in a fully balanced differential circuit where the input signal is applied differentially and the output signal is taken differentially, all even-harmonics are canceled out. The cancellation of even-order nonlinearities by the use of fully-differential paths holds for every such circuit. Let us consider a nonlinear circuit with the following transfer function :

$$V_{out}=a_1 V_{in} + a_2 V_{in}^2 + a_3 V_{in}^3 + \dots \quad (3.1)$$

For the negative input $-V_{in}$ the transfer function (3.1) gives :

$$-V_{out} = a_1 (-V_{in}) + a_2 (-V_{in})^2 + a_3 (-V_{in})^3 + \dots \quad (3.2)$$

Subtraction of equation 3.2 from equation 3.1 gives the differential output V_d :

$$V_d = 2 V_{out} = 2a_1 V_{in} + 2a_3 V_{in}^3 + 2a_5 V_{in}^5 + \dots \dots \quad (3.3)$$

and thus even harmonics are cancelled.

Another important advantage of fully differential circuits is their immunity to power supply noise. Power supply noise is a common-mode signal. Therefore for the linear case it would be common to both outputs of a differential circuit and so would not be sensed if the output signal is taken differentially. This characteristic becomes especially valuable in a mixed analog/digital circuits when they coexist on the same chip, because digital circuits tend to introduce noise to the power supply lines.

The main disadvantage of using a fully differential approach is the additional design complexity and size of the circuit, because two complete signal paths must be provided. However, this fact is not enough to discourage a designer from the use of a differential approach.

3.4 The Basic Power Amplifier Cell

The circuit schematic of the proposed amplifier is shown in Figure 3.2. It will be shown that the upper signal path of the power amplifier (after Z_i as marked on the Figure 3.2) is mainly responsible for the gain and the transfer function of the power amplifier. The last transistor on the path, Q_1 is fairly large so it can be able to carry enough current to maintain a two volts peak output voltage swing onto a 50 Ohm load. The latter puts an additional requirement on the choice of the amplifier stage which must drive this transistor. This stage is supposed to provide not only a good gain-bandwidth product but also to be able to drive the fairly large input impedance of the output transistor Q_1 .

Figure 3.2 A more detailed schematic diagram of the proposed amplifier

The Darlington configuration as extracted in Figure 3.3 is a simple two transistor amplification stage that can accommodate the previous requirements. It also shows higher current gain than a single common emitter stage and was therefore preferred over the basic common emitter stage for the gain and drive stage of transistor Q_1 .

The power amplifier as proposed in Figure 3.2 is self-biased in order to avoid the use of external components. The current source I_{bias} sets the bias voltage V_{b0} at the emitter of the transistor Q_1 , to $V_{CC}/2$ via feedback resistor R_4 . It also sets the bias point at the input of transistor Q_4 at $2V_{BE}$ and thus allows inclusion of the emitter follower Q_5 , which drives the current source Q_2 when the output voltage V_O goes negative.

Figure 3.3 A Darlington pair stage

The dc bias voltage at the output is

$$V_{bo} = I_{bias} R_4 + 2 V_{BE} = \frac{V_{CC}}{2} \quad (3.4)$$

Assuming that $V_{BE}=0.85$ V gives

$$I_{bias} R_4 = \frac{V_{CC}}{2} - 2 V_{BE} = 0.8 \text{ V} \quad (3.5)$$

Equation 3.5 shows that the desired bias point can be achieved by adjusting the bias current I_{bias} and the feedback resistor R_4 . Resistor R_4 also controls the overall amplifier gain and transfer function. Device Q_4 is the input stage of a current feedback pair and device Q_1 is the output stage. The value of R_4 dictates the amount of current that is fed back to the input from the output. As is well known, the amount of feedback affects the bandwidth of the amplifier. Because the design targets high frequency operation a large amount of current feedback would be useful but on the other hand, large amounts of feedback could cause instabilities as mentioned in section 2.3. In addition, larger feedback current results in higher stand-by power dissipation. The trade-off between these factors was considered carefully and after extensive HSPICE simulations the value of R_4 was set to 350 ohms. During this optimization process, an effort was made to bias the output stage as close as possible to the class B mode in order to achieve good efficiency. At the same time, it was made sure that the gain through the two signal paths is almost the same to provide a symmetrical output voltage.

The sizing of the transistors is based on their collector current. Because the existing transistor library includes devices with fixed emitter width only the emitter length can be varied. The emitter length is chosen in such way that each transistor is allowed to operate at or near the maximum unity gain frequency, f_T , for the given collector current. Following this sizing rule the device Q₁ and the device Q₂ are sized to support the peak collector current of 40 mA that is necessary to sustain two volts peak output voltage swing on the 50 ohm load. They were biased through resistors R₃ and R₆ to have an idle current of 14 mA, corresponding to 70 mW static power dissipation for the totem pole stage. The totem pole stage is expected to provide 40 mW output power at full output. Therefore, the totem pole stage efficiency will be 57 percent that is well above the theoretical maximum of 25 percent for the class A stage and below the maximum theoretical class B efficiency of 78 percent. This efficiency level verifies that the amplifier operates in AB mode. This is only the efficiency of the totem pole stage and the overall efficiency of the amplifier, including the gain stage, will be much lower as will be shown later in this chapter. At this point is important to acknowledge that the quiescent current of the output stage is beta β_F dependent and therefore it might vary with process and temperature variations.

3.4.1 Gain and Transfer Function

A detailed circuit analysis to predict the gain and the transfer function of the amplifier is difficult due to the number of transistors used. Even the use of the small signal hybrid π -equivalent for the bipolar transistors

makes the analysis difficult because at high frequencies the effects of the base-emitter junction capacitance, C_{π} , and the collector-emitter capacitance, C_{μ} , are included. These effects and the circuit complexity introduce high-order terms that complicate the analysis, making the use of circuit simulators necessary.

Despite this difficulty a rough estimate of the gain can be obtained since the Darlington pair followed by the device Q_1 , which acts as an emitter follower, and the feedback resistor R_4 control the gain and the transfer function of the amplifier.

For the positive going output voltage, the upper signal path can be modeled as shown in Figure 3.4 for ac signals, where Z_o is the output impedance as shown in Figure 3.3. The impedance of Q_2 is assumed very high.

Figure 3.4 Amplifier model for positive output voltage swing

The open circuit voltage gain A of the upper path is [24]

$$A = \frac{R_4}{R_1 + Z_i} \quad (3.6)$$

where Z_i is the input impedance of the upper signal path as shown in Figure 3.2. This assumes that the gain of the upper signal path is high enough that the feedback elements control the gain.

Thus, the circuit gain G is

$$G = \frac{V_o}{V_{in}} = \frac{A R_L}{R_L + Z_o} \quad (3.7)$$

At low frequencies the output impedance Z_o is resistive and equal to 0.45 ohm. The input impedance Z_i is predicted by Touchstone-Libra (EEsof. Inc.) to be around 11 Ohm. Using equations 3.6 and 3.7, the circuit gain is expected to be $G=7.5$ or 17.5 dB. Hspice simulation predicts a gain of 17.25 dB at 100 MHz and a -3dB small signal bandwidth of 2.75 GHz. Figure 3.5 shows the small signal transfer function of the power amplifier shown in Figure 3.3. Some shunt peaking, as discussed in Chapter 2, is evident. This arises from the emitter followers in the circuit.

Figure 3.5. Simulated small signal transfer function of the power amplifier

3.4.2 Input and Output Impedance

The amplifier is expected to operate in a 50 Ohm environment. This is because most of the test equipment has 50 Ohm termination and because traditionally most amplifier designs anticipate 50 Ohm loads and 50 Ohm transmission lines. The input impedance of the amplifier is adjusted through resistor R_1 in Figure 3.2 to be 50 Ohm. If the resistor R_1 is set to 35 Ohm then Touchstone-Libra simulations predict that the input impedance will be $51.99-j\ 5.5$, $56.48-j\ 3.838$ and $58.384-j\ 3.738$ at 1.0 GHz, 1.6 GHz and at 1.9 GHz, respectively.

Table 3.1 Input and output impedance of the power amplifier

Pin (dBm)	F (GHz)	Z _{in}	Z _{out}
-100	1.0	51.99-j 5.50	0.46+j 3.19
-100	1.6	56.48-j 3.84	0.86+j 6.29
-100	1.9	58.38-j 3.74	1.76+j 8.27
-6	1.0	53.20+j 7.86	8.59+j 7.99
-6	1.6	68.45+j 6.47	15.32+j 12.23
-6	1.9	75.35-j 2.01	17.91+j 12.20
-2	1.0	68.40+j 13.64	13.62+j 10.95
-2	1.6	92.94-j 2.86	21.47+j 12.27
-2	1.9	94.15-j 14.57	23.51+j 11.94

Theoretically, maximum voltage transfer from the amplifier to a fixed load impedance can be achieved if the real part of the complex output impedance is zero [20]. In addition, by converting the 50 Ohm off-chip load to a low on-chip impedance, high current swings are required for high output power instead of high voltage swings. In this way we can alleviate the limited voltage swing problem imposed by the five volt BiCMOS

Frequency Sweep Between 100 MHz and 3000 MHz

Figure 3.6 Simulated small signal S11 and S22 of the power amplifier

technology. These two facts suggest that the design should target to minimize the output impedance. This is done by the use of the feedback resistor R_4 . Table 3.1 gives the input and output impedance at three different frequencies for three different input power levels.

The small signal parameters S_{11} and S_{22} for the amplifier for a frequency sweep between 100 megahertz to 3 Gigahertz, are shown on a Smith chart in Figure 3.6. For low input power the objectives of the design are successful, as the real part of the input impedance has values close to 50 Ohms over a wide band, while the output impedance has very low real part over the same wide band. However the picture does not stay ideal as the input power levels increase as the Table 3.1 shows. The output impedance increases when the input power level increases, but it remains lower than the expected 50 Ohm load.

3.4.3 Large Signal Behavior

The large signal behavior of the amplifier at high frequencies is set by slew rate limiting at the base of transistor Q_1 (the collectors of Q_3 and Q_4). Let I_{cd} be the collector current provided by the Darlington pair and C be the capacitance loading at the base of the device Q_1 . Then the slew limiting can be pictured as in Figure 3.7.

To calculate the frequency at which the amplifier slew limits, assume that the a.c. voltage v_{cd} at the collectors of Q_3 and Q_4 is sinusoidal. Because the device Q_1 behaves as an emitter follower, it has unity voltage gain and we can therefore assume that the ac voltage at the emitter of Q_1

and its base are equal. Thus the a.c. output voltage is equal to v_{cd} . The current in capacitor C is

$$i_c = \omega C V_{cd} \cos \omega t \quad (3.8)$$

and

$$V_{cd} = (I_c + I_{cd}) R_6 \quad (3.9)$$

At the onset of slew limiting, $I_{cd}=0$ and all the bias current through resistor R_6 supplies i_c and tries to charge capacitor C . For $V_{cc}=5$ V, $V_{cd}=1.688$ V and $R_6=160$ Ω we have 10.55 mA in R_6 . Using $C=727$ fF we find from equation (3.8) that the amplifier is expected to operate at full output voltage swing up to 1.368 GHz.

Figure 3.7 Model for the slew limiting

Another way to evaluate the large signal behavior of the amplifier at the frequency of interest is the one dB gain compression point. The one dB gain compression point is defined as the point where the power gain of

the amplifier is reduced by one dB compared to the small signal power gain.

Simulation results for the gain and the output power versus input power curve for 1.0, 1.6 and 1.9 GHz are plotted in Figures 3.8 to 3.10, respectively. Table 3.2 lists the input power level at the one dB compression point for different frequencies.

Table 3.2 Input power level at the one dB compression point

Frequency MHz	Small Signal Gain dB	1 dB gain comp. point
1000	17.7	-2 dBm
1600	18.4	-5.5 dBm
1900	18.3	-7.5 dBm

Figure 3.8 Simulated gain and output power versus input power at 1 GHz

Figure 3.9 Simulated gain and output power versus input power at 1.6 GHz

Figure 3.10 Simulated gain and output power versus input power at 1.9 GHz

The previous results suggest that the amplifier can provide a relatively high level of output power for frequencies up to one Gigahertz without entering the saturation region and without the use of any matching element. For higher frequencies though, the amplifier has to operate in the saturation region to achieve levels of output power comparable with the levels of output power at one Gigahertz. Table 3.3 summarizes the simulation results for peak output voltage, V_{out} , output power, P_{out} , and efficiency, $\eta\%$, for different frequencies at -2 dBm, which is the input power level at the one dB compression point at one Gigahertz.

Table 3.3 Simulation results for the amplifier

Frequency (MHz)	P_{in} (dBm)	V_{out} (V)	P_{out} (mW)	$\eta\%$
1000	-2	1.66	27.56	15.37
1600	-2	1.45	21.03	11.73
1900	-2	1.31	17.16	9.57

The overall amplifier efficiency is much lower than the 57 percent efficiency of the totem pole output stage as predicted in Section 3.4. Further improvement will arise by improving the output power with circuit techniques that will be described later.

3.4.4 Nonlinearities

As described in Chapter 2 the operation of an amplifier in the saturation region provides higher output power and power efficiency than the operation in the linear region but on the other hand introduces nonlinearities. Total harmonic distortion, THD, and third order intercept, IM3, are figures of merit often used for characterizing the nonlinearities of an amplifier. Harmonic distortion, D_n , is commonly described in terms of percentage of the harmonic component amplitude to the fundamental component amplitude.

$$D_n = \frac{|A_n|}{|A_1|} \quad (3.10)$$

where A_n ($n=2,3,4 \dots$) represents the amplitude of the n^{th} harmonic and A_1 is the amplitude of the fundamental. The total harmonic distortion, D , is defined as [14]

$$D = \sqrt{D_2^2 + D_3^2 + D_4^2 + \dots + D_n^2} \quad (3.11)$$

The intercept point describes the intermodulation performance of an amplifier. If we plot the two-tone output power level and the third order distortion power level versus the two-tone input level on a logarithmic scale we find that the third-order distortion increases by three decibels for each decibel increase in both input signal levels. If the amplifier did not limit, the distortion products would increase until they equaled the output signal level. This power level point is called the third-order intercept point [26], IM3.

Table 3.4 lists the simulation results for the total harmonic distortion and the third-order intercept for the basic amplifier cell at different frequencies. The total harmonic distortion is estimated by Hspice simulations, with Hspice calculating the harmonic distortion caused by the first nine harmonics. The distortion caused by any higher order harmonics than this can be neglected because their amplitude is very small. The third-order intercept was estimated by Touchstone-Libra simulations. Table 3.4 shows clearly the nonlinear behavior of the amplifier when it operates at the frequencies and power levels of interest. The third-order intercept for the 1.9 GHz was not estimated. The levels of total harmonic distortion can be reduced by placing a band-pass filter after the power amplifier. The total harmonic distortion is reduced for both the matched and the differential versions of the power amplifier as will be described later in this chapter.

Table 3.4 Simulation results for the total harmonic distortion and the third order intercept

frequency (MHz)	P _{in} (dBm)	THD %	IM3 (dBm)
1000	-2	9.4	20
1600	-2	9.7	18
1900	-2	8.9	-

The third-order intercept point is only a few decibels higher than the output power of the amplifier. This fact suggests that the amplifier will have high third-order intermodulation products.

Figure 3.11 Simulated second-and third-order harmonic power levels at 1 GHz

Figure 3.12 Simulated second-and third-order harmonic power levels at 1.6 GHz

But as it was mentioned in Chapter 2, TDMA systems do not suffer badly from intermodulation distortion and constant envelope modulation allows the use of a non-linear power amplifier.

Plots of the single-tone second-and third-order harmonic distortion power levels versus the input power level at 1.0 and 1.6 GHz are shown in Figures 3.11 and 3.12 respectively to further describe the nonlinear behavior of the amplifier.

3.4.5 Improving the Output Power of the Basic Cell

Due to the mismatch between the output impedance of the amplifier and the load the basic amplifier cell cannot provide the maximum possible output power. This suggests the need for a matching network. The possibility of increasing the amount of power that can be delivered to the load without the use of a matching network was also investigated because the matching network requires the use of off-chip components.

Figure 3.13 The Basic Amplifier with a Shunt Capacitor

Since the output impedance of the amplifier is inductive, a shunt capacitor can be used in parallel with the load, as shown in Figure 3.13. As was described in Chapter 2, shunt peaking of the amplifier can increase the output power at the frequencies of interest, and the shunt capacitor can be used as a tuning element for this. The underlying implication is that the emitter follower in the amplifier will cause such shunt peaking at the amplifier output.

A 4 pF capacitor and a 1 pF capacitor were used to tune the amplifier at 1.0 and 1.6 GHz, respectively. The simulation results for the output peak voltage, V_{out} , the output power, P_{out} , the efficiency, n , and the total harmonic distortion, THD, are summarized in Table 3.5. As can be seen by comparison to Table 3.3, an improvement of the output power, efficiency and harmonic distortion are observed for the one Gigahertz region. A smaller improvement of the amplifier performance was observed at higher frequencies also.

Table 3.5 Simulation results for the tuned basic cell

F (GHz)	P_{in} (dbm)	V_{out} (V)	P_{out} (mW)	n %	THD %
1.0	-2	1.90 (1.66)*	36.1 (27.56)	20.13 (15.37)	4.14 (9.4)
1.6	-2	1.53 (1.45)	23.4 (21.03)	13.05 (11.73)	9.19 (9.7)

*Note : The results for the basic cell, Table 3.3, are presented in the parentheses.

3.4.6 Matching Network

A pi-network was used to demonstrate the performance improvement that takes place when a matching network can be used. The pi-network, shown in Figure 3.14, was chosen for this study because its topology does not have any impedance regions which cannot be matched [27]. It also is a very simple structure to implement. Part of the network, the capacitor C_1 , can be fabricated on silicon and participates in shunt peaking also. In the near future, there is a good possibility that the whole pi-network could be implemented on silicon when on-chip inductors become available.

Figure 3.14 A pi-matching network

Assuming that all the following impedances are normalized to a 50Ω impedance, let us consider that the output impedance of the amplifier is

$$Z_{out} = R + jX \quad (3.12)$$

Then the output admittance will be

$$Y_{out} = \frac{1}{Z_{out}} = G - j B \quad (3.13)$$

Capacitor C_1 can be sized to cancel the imaginary part of the Y_{out} . Thus,

$$C_1 = \frac{B}{\omega} \quad (3.14)$$

And the output admittance including the capacitor C_1 is

$$Y_1 = G \quad (3.15)$$

The introduction of the inductor L will enable an output admittance with unity real part and the capacitor C_2 will cancel the imaginary part to achieve the matching. Thus the output admittance after the introduction of the inductor is

$$Y_2 = 1 - j B_1 \quad (3.16)$$

which corresponds to an impedance

$$Z_2 = R_1 + j X_1 \quad (3.17)$$

where

$$R_1 = \frac{1}{G} \quad (3.18)$$

$$Y_2 = \frac{1}{Z_2} = \frac{R_1 - jX_1}{R_1^2 + X_1^2} = 1 - jB_1 \quad (3.19)$$

$$X_1 = \frac{\omega L}{50} \quad (3.20)$$

and

$$C_2 = \frac{B_1}{\omega 50} \quad (3.21)$$

By solving equations (3.12) to (3.21) the component values for the pi network can be calculated. The results for different frequencies are included in Table 3.6.

Table 3.6 Component values for the matching network.

F (MHz)	C ₁ (pF)	L (nH)	C ₂ (pF)
1000	5.7	3.95	3.5
1600	2	2.46	1.7
1900	1.4	2.07	1.5

The required inductor values are relatively small. This suggests that the use of small size wire bonds as inductors might be a temporary solution to the matching problem until inductors on silicon are available. The matching network is expected to improve the performance of the amplifier. Table 3.7 summarizes the expected performance of the amplifier.

when it is matched to the 50 Ohm load. It shows further improvement of the output power efficiency and harmonic distortion comparing with the tuned amplifier performance of Table 3.5.

Table 3.7 Simulation results for the matched amplifier

F (MHz)	V _{out} (V)	P _{out} (mW)	η %	THD %
1000	2.0 (1.90)*	40.00 (36.1)	22.3 (20.13)	3.3 (4.14)
1600	1.71 (1.53)	29.94 (23.4)	16.3 (13.05)	6.5 (9.19)
1900	1.51 (1.31)	22.80 (17.2)	12.76 (9.57)	7.1 (8.9)

* Note: The results for the tuned basic cell, Table 3.5, are included in the parentheses.

Figure 3.15 Simulated output return loss for the amplifier matched at 1 GHz

Figure 3.16 Simulated output return loss for the amplifier matched at 1.6 GHz

Figure 3.17 Simulated output return loss for the amplifier matched at 1.9 GHz

The output return loss, as predicted by Touchstone-Libra simulation, is plotted in Figures 3.15 to 3.17. The low output return loss at the frequencies of interest suggests that the pi-network can give a very good matching to the 50 Ohm load.

3.5 Differential Approach

Figure 3.18 Differential topology

The output power can in principle be doubled if the basic amplifier cell is used in a differential topology as shown in Figure 3.18. In order to achieve this, the differential amplifier has to be terminated with a 100 Ohm load. If we consider that we still want to drive a 50 Ohm load then a transformer is necessary. The performance of the differential version was estimated by Hspice simulations. The simulation results are summarized in Table 3.7 with comparison to earlier equivalent single ended versions in brackets. The output power is doubled, efficiency is unchanged and

Table 3.7 Simulation results for the differential versions

Basic Cell, Differential Version				
F (MHz)	V _{out} (V)	P _{out} (mW)	η %	THD %
1000	3.32	55.12 (27.56)	15.37	2.54 (9.4)*
1600	2.9	42.06 (21.03)	11.73	0.935 (9.7)
1900	2.62	34.32 (17.26)	9.57	0.95 (8.9)
Basic Cell with shunt capacitor, Differential version				
F (MHz)	V _{out} (V)	P _{out} (mW)	η %	THD %
1000	3.8	72.2 (36.1)	20.13	1.36 (4.14)
1600	3.05	46.8 (23.4)	13.05	3.45 (9.19)
Matched Basic Cell, Differential Version				
F (MHz)	V _{out} (V)	P _{out} (mW)	η %	THD %
1000	4.0	80 (40)	22.3	1.97 (3.3)
1600	3.41	58.48 (29.94)	16.3	0.147 (6.5)
1900	3.02	45.60 (22.80)	12.76	0.8 (7.1)

* Note : The equivalent results for the single ended versions are included in the parentheses The efficiency column is identical for both versions

distortion is drastically reduced. These results are optimistic because they assume an ideal transformer and do not take into account the attenuation that a transformer will introduce. A typical transformer insertion loss is around 0.5 dB which is not large enough to discourage us from the use of the differential version [28]. For now, the differential version seems to be the solution to the effort for high power level out of a five volt process. To avoid the loss of output power due to the transformer use, one might

consider the use of a dipole instead of a monopole for the transmitter antenna because the dipole can be driven by a differential signal.

3.6 Comparison with Commercial Amplifiers

Table 3.8 Amplifier specification

	Small signal gain	-3dB bandwidth	Power output @ the 1dB comp. point @ 1 GHz*	Bias current	η % (inferred)
NEC UPC- 1678B	23 dB	1.90 GHz	—	48 mA	—
Avantek UTO-2055	9.5 dB	2.00 GHz	11.5 dBm (14.13 mW)	32 mA	8.07
Predicted Bicmos	17.25 dB	2.75 GHz	14.4 dBm (27.56 mW)	35.85 mA	15.37

* Note : The output power at the one dB compression point is at 1.0 GHz. This specification was not available for the NEC amplifier.

The basic amplifier cell that does not include any matching elements was compared with two available commercial power amplifiers manufactured by Avantek and NEC [29, 30]. These commercial amplifiers operate using a single five volt voltage supply and are categorized as medium output power amplifiers. They are manufactured in pure bipolar technology instead of BiCMOS technology and they were introduced in 1990. Table 3.8 lists the specifications for the three amplifiers. The efficiency, not given by the manufacturer, was inferred from the bias current to obtain standby power. The output power was at 1.0 GHz.

The BiCMOS amplifier predictions of this thesis compare favorably with the current state of the art pure silicon amplifiers. The efficiency at one Gigahertz is expected to be approximately doubled. The trade-off between dc gain and bandwidth is favorable for our BiCMOS amplifier.

3.7 Layout

Three single-ended and two differential versions of the basic amplifier cell were laid out. The single-ended versions were the basic cell and the basic cell optimized to operate at 1.0 and 1.6 GHz, using on-chip linear polysilicon capacitors for shunt peaking. The two differential versions were the differential version of the basic cell and the differential version of the basic cell optimized to operate at 1.6 GHz. The cell layouts were designed to support measurement and characterization by microwave probing. The layouts of the cells are shown in Figures 3.19 to 3.23. For the single-ended versions two ground-signal-ground pad arrays were used to provide access to the input and output signal and a signal pad was used to supply the rail voltage. The size of the ground-signal-ground pad array is $425\text{ }\mu\text{m} \times 135\text{ }\mu\text{m}$ and the size of the single pad is $120\text{ }\mu\text{m} \times 120\text{ }\mu\text{m}$. The size of the basic cell without the pads is $285\text{ }\mu\text{m} \times 230\text{ }\mu\text{m}$. The tuned basic cells are larger than the basic because they include a 15 pF on chip capacitor for dc decoupling. Their size without the pads is $465\text{ }\mu\text{m} \times 320\text{ }\mu\text{m}$. For the differential versions an eight pad array was used. Its size is $130\text{ }\mu\text{m} \times 1414\text{ }\mu\text{m}$. The size of the differential cells without the pads is $200\text{ }\mu\text{m} \times 1040\text{ }\mu\text{m}$ for the basic cell and $350\text{ }\mu\text{m} \times 1240\text{ }\mu\text{m}$ for the basic cell optimized to operate at 1.0 GHz.

Figure 3.19 Layout of the basic amplifier cell optimized to operate at 1 GHz

Figure 3.20 Layout of the basic amplifier cell optimized to operate at 1.6 GHz

Figure 3.21 Layout of the differential version

Figure 3.22 Layout of the differential version optimized to operate at 1.0 GHz

Figure 3.23 Basic amplifier layout

CHAPTER 4

Experimental Work

Fabrication of the amplifier described in Section 3.4 could not be completed within a reasonable timeframe for this thesis. However, a fabricated amplifier cell having a circuit topology similar to the one proposed in this thesis was available for testing. The objective of this experimental work was to evaluate the accuracy of the circuit simulators that were used to predict the performance of the proposed BiCMOS amplifier and thus to validate the predictions. This chapter will present the results of this experimental work.

4.1 The Tested Amplifier

The schematic of the tested amplifier is shown in Figure 4.1. The amplifier was designed and laid out by D. Rahn and is based on the circuit topology introduced by Dr. R.G. Meyer and W.P. Mack in [24]. This was the same topology used in this thesis. The principle of operation of the circuit has been already explained in Chapter 3 and therefore will not be repeated in this chapter. It is useful though to point out that the totem pole output stage of this experimental amplifier is exactly the same as the output stage of the proposed amplifier and both are realized in the same BiCMOS

Figure 4.1 Schematic of the tested amplifier

technology. The main difference between the two designs can be seen by comparing Figure 4.1 to Figure 3.2. The proposed amplifier has a current bias and a Darlington pair stage as the gain stage instead of the single common emitter gain stage seen in Figure 4.1. These facts suggest that this is a reliable test circuit to evaluate the accuracy of the predicted performance of the proposed amplifier.

Hspice and Touchstone-Libra were the two simulators that were used during this work. Hspice is a time domain simulator and Touchstone-Libra is a harmonic balance simulator [31]. They both use the Gummel-Poon model for the bipolar transistor [32]. Sample simulations were performed in both simulators and were cross checked against each other to verify that both simulators give the same results.

The amplifier was tested by high frequency wafer probing. All the measurement instruments were carefully calibrated to have the coplanar waveguide probe tips as the measurement reference plane. The only source of error in the measurements is the parasitic capacitance of the pads, but this error is very small because the pad parasitic capacitances are very small compared to the capacitance introduced by the devices under test. Therefore this error can be neglected.

4.2 Small Signal Behavior

The tested amplifier was found by experiment to have a bandpass transfer function with 21.5 dB gain at 1.1 GHz (see Figure 4.2) and 600 MHz bandwidth. The bandpass behavior of the tested amplifier is different than the predicted lowpass behavior of the proposed amplifier. The size of the dc decoupling capacitor at the input of the tested amplifier is responsible for the bandpass behavior. If a larger capacitor was used in the tested amplifier then a flatter gain at low frequencies could be achieved and the transfer function of the tested amplifier would have similar behavior to the proposed amplifier. Then it would be easier to notice the gain peaking due to emitter follower and capacitor interaction as described in Chapter 2.

In the experimental amplifier the shunt capacitor was sized to give a small signal gain peak at 1.1 GHz exactly as the shunt capacitors in Chapter 3 were sized to provide a gain peak at 1.0 and 1.6 GHz.

Figure 4.2 compares experimental to simulation results for the small signal gain of the tested amplifier. When the experimental circuit was simulated with the nominal target process file, the simulation predicted a bandpass transfer function with peak gain of 19.8 dB at 1.3 GHz, and 1.0 GHz bandwidth. Because the nominal process file seemed to give optimistic results compared to the experiment, the simulation was repeated with the worst case process file. This predicted bandpass behavior with peak gain of 19.7 dB gain at 1.1 GHz and 800 MHz bandwidth. The worst case process file gave results closer to the experimental results, but the small signal gain behavior was still not close enough as Figure 4.2 shows.

Having in mind that the test circuit was fabricated during the early experimental stage of the BiCMOS process we tried to investigate which process parameters might be partly responsible for the simulation discrepancies. The circuit topology suggests that variation of the forward transit time, T_F , and of the base resistance, R_B , can affect the circuit performance. The forward transit time is mainly responsible for the speed of the device, and therefore the speed of the circuit. The base resistance is responsible for the shape of transfer function of the circuit because it determines the transfer function of the emitter followers used. The base resistance measurement inherently can have a 15 percent error. This measurement is performed on small size devices and the results are

Figure 4.2 Comparison between measured and simulated small signal gain S21

extrapolated for larger size devices resulting in a larger measurement error for the large devices. Such large devices were used for the design of the tested circuit. Measurements performed on a single device showed that the forward bias beta, β_F , was high due to lower integrated base dose. High beta indicates that the base resistance is at the high end of the specification range. By setting the base resistance 20 percent higher than the target value and the transit forward time at the low end of the specifications it was possible to tune the simulation result closer to the experimental results, as shown in Figure 4.2. The tuned simulation results are in good agreement with experimental results for frequencies up to 1.4 GHz. For higher frequencies, the experimental results show a faster roll-off than the one predicted by the simulation results. This is probably due to the parasitic capacitances of the pads because they introduce greater measurement error as the frequency increases. The tuned simulation results predict peak gain of 20.3 dB at 1.1 GHz and a bandwidth of 700 MHz. Thus process variations are thought to explain the discrepancies between simulation and experiment. Such process variations are not expected to appear in a similar degree during the fabrication of the proposed amplifier as it is being fabricated later.

4.3 Large Signal Behavior

a) At 600 MHz

The large signal behavior of the experimental amplifier was investigated at 600 MHz, which was the frequency that the amplifier was optimized to operate at, and at 900 MHz. At 600 MHz simulations predict

that the amplifier has its one dB compression point at zero dBm. The measured results verify that the one dB compression point is at zero dBm. Figure 4.3 shows the simulated and the experimental results for the gain and the output power versus input power plots at 600 MHz. Experimental and simulation results match very well.

The second and third harmonic power levels are plotted in Figures 4.4 and 4.5, respectively. Measured and simulated results for the second harmonic power levels match very well. The experimental results for the third harmonic power levels are only a few decibels lower than the predicted results. The harmonic behavior of the amplifier at 600 MHz is successfully predicted by the simulations. The slight discrepancy between the simulation and experiment results is expected when the harmonic behavior of a nonlinear circuit is evaluated by experiment. The simulators do not take into account alternative signal paths that may exist on the circuit under test which can cause phase shift and partial cancellation of the harmonic components making the exact prediction of the harmonic behavior more difficult.

b) At 900 MHz.

The same set of measurements was performed at 900 MHz. Because the amplifier is slew limited for frequencies higher than 600 MHz it is not as "well behaved" at 900 MHz as it is at 600 MHz, and therefore its gain does not follow the gain predicted by simulation. Instead of having a linear gain region and then rolling off, it shows a peaked response. This causes the one dB compression point to be at -8.75 dBm instead of the expected 0 dBm. Figure 4.6 describes that behavior. The second-and third-harmonic

Figure 4.3 Measured and simulated output power and gain at 690 MHz

Figure 4.4 Measured and simulated second-harmonic power levels at 600 MHz

Figure 4.5 Measured and simulated third-harmonic power levels at 600 MHz

Figure 4.6 Measured and simulated output power and gain at 900 MHz

Figure 4.7 Measured and simulated second-harmonic power levels at 900 MHz

Figure 4.8 Measured and simulated third-harmonic power levels at 900 MHz

power level plots are shown in Figure 4.7 and 4.8, respectively, and they confirm that the amplifier is not "well behaved" at 900 MHz. The slew rate limitation at the output of the tested amplifier occurs for exactly the same reasons that cause slew limitation on the output of the proposed amplifier. These reasons were discussed in Section 3.4.3 and will not be repeated here. It is important though to point out that the proposed design slew limits for frequencies higher than 1.3 GHz, while the tested amplifier slew limits for frequencies higher than 600 MHz. The use of the Darlington pair in the proposed circuit to drive the output stage, instead of the common emitter approach used in the tested amplifier, and careful bias of the design, delays the appearance of the slew limit. This suggests that the predicted behavior of the tested amplifier should have good accuracy for frequencies up to 1.3 GHz. For higher frequencies, it is expected that the input power region for which the amplifier is linear and "well behaved" will be reduced and the amplifier will not follow the simulation models so closely.

Another reason that may result in discrepancies between experiment and simulation for the high frequency high signal behavior of the amplifier is the bipolar transistor model used by the simulators. Hspice and Touchstone-Libra define their transistor model as a lumped circuit model without taking into account the distributed nature of the transistor at high signal frequencies. One of the parameters defined in lumped element terms is the base resistance which affects the circuit performance as shown in Section 4.2. Defining the base as a distributed element could drastically affect the large signal characteristics of the bipolar transistor as shown in [33].

4.4 Evaluation

This experimental work gave some confidence in the simulators that were used for the design of the proposed amplifier. Experimental and simulation results agree favorably. The agreement between simulation and experiment seems to be strong at frequencies in which the amplifier does not slew limit and therefore the proposed amplifier specifications are expected to be met at 1.0 GHz. The simulators are optimistic in predicting the amplifier performance at high frequencies where the amplifier is slew limited but they can still give useful information for the design. The expected performance of the proposed amplifier might be optimistic at the 1.6 and 1.9 GHz. However the discrepancies raise the issue of the need for accurate large signal modeling of the high frequency bipolar transistor. This issue is beyond the scope of this thesis work, but a number of successful high speed silicon circuit designers have already demonstrated more accurate models for high speed bipolar transistors [34].

CHAPTER 5

Conclusions and Recommendations

This thesis has been concerned with the design of a high-frequency medium-power amplifier in a fine-line state of the art BiCMOS process. This amplifier could be the last amplifying stage of a low-power transmitter for a personal communication system. The amplifier design serves as a vehicle to explore the limits of the BiCMOS technology used. Now that the experimental and design work is finished, it is possible to consider the suitability of the BiCMOS technology used for digital radio applications. Taken as a given in this technology will be standard low-frequency digital signal processing and digital control as well as baseband switch-capacitor filtering, with the only question being if they can have low enough power and chip area for a given application. The major question is then whether adequate RF performance can be achieved on the same chip. This thesis has served to show for at least one important RF component, i.e., the power amplifier for a low-power personal communicator, that the BiCMOS process could provide adequate performance and reasonable power up to 1.0 GHz, as for example in the CT2+ application which requires 10 mW at 1.0 GHz. Depending on the power requirements operation up to 2 GHz is also feasible.

The only constraints set in the beginning of this design study were that the amplifier should use a single five volt power supply and should achieve full voltage swing at least in the one gigahertz region. In the process of designing and analyzing such a circuit, several important microwave analog circuit design issues were addressed, including how to design a high speed and power efficient circuit, negative feedback effects on the design, and nonlinearities and optimum loading. Important conclusions have been drawn in each of the above issues, as follows.

Firstly, a specific circuit design has been proposed which promises to provide 40 mW output power at one GHz, 29 mW output power at 1.6 GHz and 22.5 mW at 1.9 GHz. This is an amplifier that favorably compares to commercial medium power amplifiers fabricated in pure silicon technology instead of BiCMOS technology. As an additional important feature of such work, the amplifier of this thesis could be incorporated monolithically in BiCMOS along with other complex parts of the digital radio.

The amplifier design makes use of a totem pole output stage due to lack of high frequency pnp transistors. If high frequency pnp transistors were available, alternative circuit topologies that promise better performance could be explored. The totem pole output stage is biased in a class AB mode by a feedback self bias scheme which also controls the output impedance of the amplifier. The output impedance was kept as low as possible in order to take advantage of current swing instead of voltage swing due to the limitation that the five volt power supply puts on the output voltage swing. It was shown that losses due to impedance mismatch between the output impedance of the amplifier and the load

can be reduced by the use of matching networks. A design example of a matching network was given and its beneficial effects on the amplifier performance were demonstrated. It was shown that if additional power is required, a differential version of the amplifier is advantageous, almost doubling the output power. This however requires the use of a transformer. The design of on-chip silicon transformers is an area for future research.

It is obvious from the amplifier design studied in this thesis that use of complicated circuits is not a good avenue for high frequency circuit design except perhaps peripherally for tuning. In the main signal path, circuits with a small number of transistors are preferable because in this way the designer can see by experience, confidence in the simulation model, and quick simulation how the design can be tuned to achieve the desired performance. Complicated circuit performance is more difficult to predict as the number of devices gets larger due to the increasing number of parasitic elements. In the case of a complicated design, partitioning the circuit into subcircuits, if possible, and use of S-parameter design for each subcircuit would be suggested. These techniques are used by high frequency GaAs circuit designers. This thesis work has included an evaluation of existing circuit simulators and has shown the need for more accurate modeling for the high speed bipolar transistor.

As the BiCMOS process becomes faster it is obvious from the results of this work that such a process can be a major factor in the race for the low cost implementation of small and light weight personal communicators for mobile radio applications, by allowing the integration of high-frequency front-end modules, like the transmit amplifier, and low-

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PM-1 3½"x4" PHOTOGRAPHIC MICROCOPY TARGET
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frequency modules , such as DSP, on the same chip. This ability leads the designers to explore new transmitter architectures like the one presented in Chapter 2. The proposed amplifier can be used to evaluate and further study that architecture.

In summary, this work clearly demonstrated the RF capabilities of the BiCMOS technology. It also demonstrated that BiCMOS technology offers many unique opportunities for high frequency digital radio system and circuit designers by combining the density and low power advantages of CMOS with the high speed capabilities of bipolar circuitry.

For further work, the effect of the modulation feedback on the amplifier linearity has to be studied theoretically and through high level simulation. To complement this, the effect of the amplifier nonlinearity on the loop characteristics needs to be determined by experiment on the fabricated amplifier when available. After the evaluation of the effect of the amplifier nonlinearities on the loop stability, one can evaluate if the use of a more nonlinear and therefore more efficient amplifier is possible. Class C is the next mode of operation that should be examined in the BiCMOS technology. The use of on-chip inductors will allow full integration of a BiCMOS class C amplifier. Inductive loading can allow higher speed of operation. The use of on-chip transformers will allow the evolution of amplifier topologies that use current swing instead of voltage swing. This will be useful in the near future because of the already existing tendency to reduce the voltage supply from five volts to three volts.

The results which have been presented show that there is a need for extensive research that will allow the transfer onto silicon of transmission

line elements of the type that have been used by GaAs MMIC designers. This will allow fully integrated microwave low cost silicon products to become possible.

References

- [1] G.F. Wilson, "Advances in Bipolar VLSI", Proc. IEEE, vol. 78, no. 11, pp. 1707-1719, November 1990.
- [2] J.R. Long, "High Frequency Integrated Circuits in BiCMOS for Monolithic Timing Recovery", Thesis, Carleton University, 1992
- [3] P. Schneidrmg, "In Search of a New Market", Microwave&RF, pp. 33-43, August 1991.
- [4] T.A.D. Riley, "A Simplified Continuous Phase Modulation Technique" Unpublished.
- [5] T.A.D. Riley , M.A. Copeland & T.A. Kwasniewski, "Sigma Delta Modulation in Fractional-N Synthesis", IEEE JSSC, accepted for publication, date to be dertemined.
- [6] R.Hadaway et al, "A Sub-Micron BiCMOS Technology for Telecommunications", J. of Microelectronic Engineering, vol. 15, pp. 513-516, 1991
- [7] Gray and Meyer, Analog Integrated Circuits, John Wiley & Sons Inc., 1984.
- [8] David J. Comer, Modern Electronics Circuit Design, Addison-Wesley, 1976.
- [9] D.C. Pederson and K. Mayaram, Analog Integrated Circuits for Communications, Kluwer Academic Press, 1991.

- [10] H.L. Krauss et al, Solid State Radio Engineering, John Wiley & Sons Inc., 1980.
- [11] A.B. Grebene, Bipolar and MOS Analog Integrated Circuit Design, John Wiley & Sons Inc., 1984.
- [12] P.D. Van Der Puije, Telecommunication Circuit Design, John Wiley & Sons Inc., 1992.
- [13] A. Bateman & D.M. Haine, "Direct Conversion Transceiver Design for Compact Low-Cost Portable Mobile Radio Terminals", 1989.
- [14] S.M. Perlow, "Third-Order Distortion in Amplifiers and Mixers", R.C.A Review, Vol. 37, pp.235-267, June 1976.
- [15] V. Manassewitsch, Frequency Synthesizers Theory and Design, 3rd Ed. John Wiley & Sons Inc., 1987.
- [16] V. Petrovic & C.N. Smith, "The Design of the VHF SSB Polar-Loop Transmitters", I.E.E Conf. Publ. 209, "Communications equipment and Systems", pp. 148-158, 1982.
- [17] V. Petrovic, "Reduction of Spurious Emission from Radio Transmitters by the Means of Modulation Feedback", I.E.E Conf. Publ. 224, "Radio Spectrum Conservation Techniques", pp. 44-49, 1983.
- [18] A. Blanchard, Phase-Locked Loops Application to Coherent Receiver Design, John Wiley & Sons Inc., 1976.
- [19] J. Millman & A. Grabel, Microelectronics, 2nd Ed., McGraw-Hill International Editions.

- [20] C.W. Davidson, Transmission Lines for Communications, 2nd Ed.,
Macmillan Education LTD., 1989.
- [21] T Edwards, Foundations for Microstrip Circuit Design, 2nd Ed.,
John Wiley & Sons Inc., 1991.
- [22] C.V. Vendelin, A.M. Pavio & U.L. Rohde, Microwave Circuit Design
Using Linear and Nonlinear Techniques, John Wiley & Sons Inc.,
1990.
- [23] N.M. Nguyen and R.G. Meyer, "Si IC-Compatible Inductors and LC
Passive Filters", IEEE J. Solid State Circuits, Vol. 25, No. 4, pp. 1028-
1031, August 1990.
- [24] R.G. Meyer and W.D. Mack, "A Wide-Band Class AB Monolithic
Power Amplifier". IEEE J. Solid-State Circuits, Vol. 24, No. 1, pp. 7-11,
February 1989.
- [25] M. Banu and Y. Tsividis, " Fully Integrated Active RC Filters in MOS
Technology", IEEE J. Solid-State Circuits, Vol. SC-18, No.6, pp. 644-651,
December 1983.
- [26] W. Esabin and E.O. Schoenike, Single-Sideband Systems and Circuits,
McGraw-Hill Inc., 1987.
- [27] M.J. Underhil, " Wide Range Antenna Matching Networks", Radio
Receivers and Associated Systems, pp. 101-135, July 1981.
- [28] VARIL, Application Notes, Double Balanced Mixers and Transformers

- [29] Avantek Databook, Modular and Oscillator Components, Santa Clara Avantec Inc., 1990.
- [30] Nec, Microwave and RF Semiconductors, California Eastern Laboratories, 1989-1990.
- [31] Touchtone (A linear microwave design tool) and LIBRA (A non-linear microwave design tool), EESOF Inc., Westlake Village Ca., 1989
- [32] Meta-Software, HSPICE User's Manual, Metasoftware Inc., Campbell Ca., 1990
- [33] M.P.J.G. Versleijn, "Distributed High Frequency Effects in Bipolar Transistors", IEEE 1991 Bipolar Circuits and Technology Meeting, pp. 85-88.
- [34] H. Stubing and H.Rein, "A Compact Physical Large-Signal Model for High Speed Bipolar Transistors at High Current Densities. Part I: One-Dimensional Model", IEEE Tran. on Electron Devices, Vol. ED-34, No 5, pp. 1741-1751, August 1987.

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