Multi-Port Receivers System Analysis and Modeling

by

Jose Augusto Lima, B.Sc. M.Sc. M.A.Sc.

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Department of Electronics
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Abstract

Wireless communication has grown exponentially in the last few decades. Hence, the demand for more throughput and diverse communication standards (such as *GSM*, Bluetooth, *WiFi*, *LTE*), have increased over this time. Software-defined radio (SDR), which aims to be easily programmable, is a good candidate to meet current market demands. However, a number of technical challenges (e.g., dynamic range, wide band, sampling frequency, number of bits of the *ADCs* and power consumption, etc.) need to be addressed to make *SDR* a viable solution. This is in addition to the challenges presented by the architecture proposed by [1] - [8].

The design simplicity together with wideband characteristics of Multi-Port receiver structures provides a *RF* architecture that can solve many of the current *SDR* challenges. Multi-Port receivers use diodes as power detectors and in this work, contrasted to other results published in the literature, we not only provide a controlled continuous bias to the diodes, we also propose a novel blind algorithm that reduces the Error Vector Magnitude (EVM) by adaptively controlling the diode bias point. Another key feature of optimum diode bias control is the Local Oscillator (*LO*) power requirements decrease. Results presented show that a *LO* power variation of more than 10dB produces no EVM degradation. We also developed a novel methodology for estimating the initial diode bias voltage for the optimizer. Although we simulated the methodology for four different Schottky diodes from different vendors (Win Corp, HP, Hitachi and Siemens), the process can be applied to other diodes. The initial value is located at the maximum of the second derivative of the I-V curve. We also investigated how memory effects affect the performance of the Multi-Port receivers. The results obtained in this investigation allow us to simplify the representation of the diode to a finite power series. We also introduced a technique to mitigate high-order nonlinearities in the Multi-Port receivers. To verify the results of this research we used a Simulink model that emulates the radio frequency (*RF*) and digital baseband sections of a Six-Port receiver.

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Glossary

AC Alternate Current

ACI Adjacent Channel Interference

ACPR Adjacent Channel Power Ratio

ADC Analog to Digital Converters

ADS Advanced Design System

AFE Analog Front End

AGC Automatic Gain Control

ATSC Advanced Television System Comittee

AWGN Additive With Gaussian Noise

BB Baseband

BER Bit Error Rate

BPF Band Pass Filter

BTS Base Station

CPE Customer Premise Equipment

CTB Composite Triple Beat

CSO Composite Second Beat

DFE Digital Front End

DNL Differential Nonlinearity

DSP Digital Signal Processing

DVB-T Digital Video Broadcasting - Terrestrial

ENoB Equivalent Number of Bits

EVM Error Vector Magnitude

FM Frequency Modulation

FBMC Filter Banks Multi-Carrier

FPGA Field Programable Gate Array

GaAs Gallium Arsenate

GPS Global Positioning Satellite System

GSM Global System for Mobile

HR Harmonic Rejection

IF Intermediate Frequency

IIP2 Second-Order Input Intercept Point

IIP3 Third-Order Input Intercept Point

IMD Intermodulation Distortion

INL Integral nonlinearity

IP Intellectual Property

ISDB-T Integrated Service Digital Broadcast - Terrestrial

LNA Low Noise Amplifier

LNB Low Noise Block

LO Local Oscillator

LOS Line of sight

LTE Long Term Evolution

LTM Long Term Memory

MIMO Multi Input Multi Output

MCM Multi Carrier Modulation

NF Noise Figure

OBI Out of Band Interference

OFDM Orthogonal Frequency Division Multiplex

OSR Over-sampling Rate

PAPR Peak to Average Power Ratio

PA Power Amplifier

PD Power Detector

PHEMT Pseudomorphic High Electron Mobility Transistors

PN Phase Noise

PRBS Pseudo Random Bit Stream

PVT Process Voltage and Temperature

QAM Quadrature Amplitude Modulation

QPSK Quadrature Phase Shift Keying

RF Radio Frequency

RRC Root Raised Cosine Filter

RSSI Received Signal Strength Indicator

SDR Software Defined Radio

SNR Signal to noise ratio

SOC System On Chip

STB Setop Box

UFMC Universal Filtered Multi Carrier

VGA Variable Gain Amplifier

WiFi Wireless Fidelity

WCDMA Wideband Code Division Multiple Access

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Chapter 1

Introduction

1.1 Introduction

Present day mobile wireless devices are based upon the implementation of narrow-band RF Analog Front-End (*AFE*) architectures and System on a Chip (*SoC*) processing functions. This architectural approach is implemented to fulfill the application needs of customers as well as the multiple standards which co-exist within a typical mobile device. This method is employed to satisfy customer needs and address the competitive nature of the mobile market. As an example, *WiFi*, *GSM*, *GPS*, standards are normally expected to be present and supported within a mobile platform.

Some companies address the multi-function requirement by combining multiple *AFE*s into one package [9] and [10] through the use of multi-chip module (*MCM*) technology or subsystems. The factors which drive this type of integration are based upon the package limitations of the final product platform, power consumption, cost and performance requirement of each individual standard. The latter item being important since a front end optimized for a specific function will almost always be lower cost to implement (in terms of silicon) and out performs a generalized *RF* structure. This is mainly due to the specific *RF* requirements imposed on each of the individual standards.

1.2 Multi-Port Receivers

Multi-Port receivers were introduced, for the first time in the 70's, as a way to measure impedance characteristics of electronic devices. These structures are usually designed

with passive components and therefore, can operate in a wide frequency band. In the 90's came the requirement for the receivers to operate in a wide frequency band (*SDR*) in which, structures were introduced as a avenue for applications in wide band transceivers. The down conversion is achieved by using the nonlinear properties of the diodes. Therefore, these structures do not need complex circuits such as Gilbert Cell mixers. The estimation of I and Q is calculated using power measurements and, it can be done either in the analog or digital domain. We will focus on the estimation of I and Q using digital domain due the fact that implementation using digital circuits is not sensitivity to process voltage and temperature variation (PVT).

In this research our contribution are as follows:

1. An optimizer to adaptively find the optimum voltage to bias the diode
2. A design process to estimate the initial value to be given to the optimize
3. Analysis of memory effects on Multi-Port receivers
4. A process to mitigate nonlinearities in Multi-Port receivers

during the research of these novelties, a structure is proposed, based upon the Multi-Port receiver concept which can be configured as one *AFE* capable to address most of the standards without loss of performance. This architecture is capable of replacing the *MCM* concept while satisfying the requirement to provide optimized performance for each of the various *RF* standards. Through adaptive *RF* parameter optimization techniques, it will be shown that the system will provide optimal performance for each of the *RF* standards.

Multi-Port shown in Fig. 1.1 (Port 1 is the *RF* input, port 2 is the *LO* and ports 3 to 6 are the four power detectors), is one structure which conforms to any standard and can provide the same or better performance of the application specific *RF* front end available for the particular standard. Different mitigation needs to be applied due to the fact that Multi-Port is a different architecture. The Multi-Port receiver shown in Fig. 1.1 is composed by two *RF* front ends (*RF-FE*) and the baseband section. The baseband section is responsible to receive the four power measurements, convert them into digital domain and estimate the in phase (emphI) and quadrature (Q) signals. The quality of the estimated I and Q signals is measured as being the error vector magnitude (*EVM*) which, represents the difference from the optimum constellation point (Symbol) to the estimated (Symbol). Let S_{ideal} be an ideal constellation point

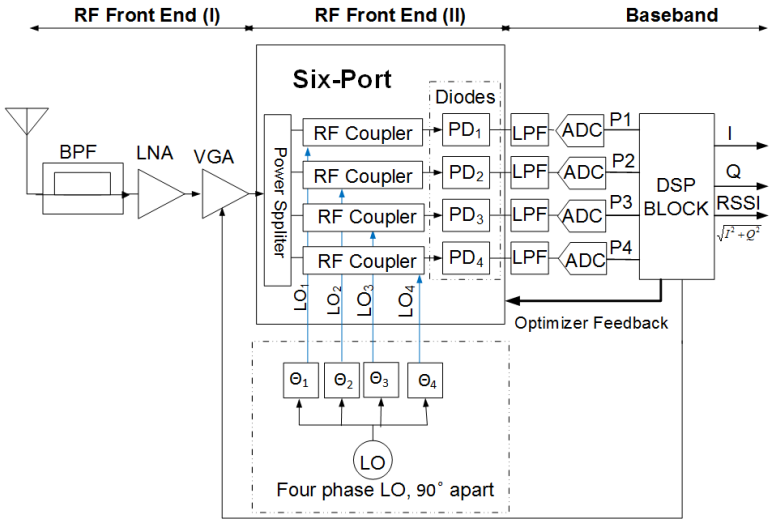

Figure 1.1: Six-Port Receiver.

($S_{ideal} = I + jQ$) where $[I, Q \in [\pm 1, \pm 3, \cdots \pm A]$ and A is a positive integer. Let $S_{estimated}$ be the estimated symbol by the **DSP** block. [62] provides the following equality for the error vector magnitude for a modulated signal:

$$\mathbf{EVM}_{RMS} = \left[\frac{\frac{1}{N}\sum_{r=1}^{N} |S_{ideal} - S_{estimated}|^2}{\frac{1}{N}\sum_{r=1}^{N} |S_{ideal}|^2} \right]^{\frac{1}{2}} \tag{1.1}$$

Fig 1.1 is one of the ways to show the functionality of a Multi-Port receiver. A more usual implementation is done using 90° hybrid couplers. For better clarity, we divided the Multi-Port receivers in two *RF-FE* (I and II) and the *DSP* block where the estimation of I and Q occurs in the digital domain. The focus of our research is on the *RF-FE* II and in the baseband blocks.

1.2.1 Receiver RF-AFE

The *RF-AFE* includes the *BPF*, *LNA*, *VGA*, *LO* and Six-Port down converter. The design of the band pass filter *BPF*, *LO*, *LNA* and *VGA* are not within the scope of this document but they must be designed to have a good performance in the frequency band of operation. Fig.1.1 illustrates a typical architecture for a Six-Port receiver. This architecture can be divided into three sections: *RF* front end (I), *RF* front end (II) and baseband.

***RF* Front End(I)**

This block is comprised of a (*BPF*), *LNA* and variable gain amplifier (*VGA*). Due to the fully occupied spectrum environment as depicted by Table 2.2 Adjacent Channel Interference (*ACI*) and out of band interference (*OBI*) will occur with high probability. Therefore, to operate under strong interference the *LNA* simulation includes nonlinearity effects. Another system impartment considered in the *LNA* is noise figure.

***RF* Front End (II)**

The *RF* front end II is typically designed using passive components. This structure is linear with wideband characteristics. The received signal amplified by the *LNA* and *VGA* is divided into four branches. Each signal is fed into a couple or an equivalent passive circuitry that provides the function of adding the input receiver signal and the *LO* signal. After the *LO* and received signal are added together, the signal resultant of the sum is then applied to a diode power detector (*PD*) and filtered by a *LPF*.

1.2.2 Baseband

The signal is transformed to digital domain by using analog to digital converters with adequate number of bits, and sampling frequency. After being in digital domain, the signals I and Q are calculated using the expression in Eq. 1.2 [11].

$$\vec{P} = M\vec{x} \Rightarrow \vec{x} = M^{-1}\vec{P} \tag{1.2}$$

where the matrix **M** is the system matrix, the vector $\vec{P}$ is the measured vector as shown in Fig. 1.1 and a vector $\hat{x}$ which is the instantaneous estimated value of **RSSI**, I and Q .

$$M_{(4\times3)} = \begin{pmatrix} 1 & A_{LO}\cos(\Theta_1) & -A_{LO}\sin(\Theta_1) \\ 1 & A_{LO}\cos(\Theta_2) & -A_{LO}\sin(\Theta_2) \\ 1 & A_{LO}\cos(\Theta_3) & -A_{LO}\sin(\Theta_3) \\ 1 & A_{LO}\cos(\Theta_4) & -A_{LO}\sin(\Theta_4) \end{pmatrix} \tag{1.3}$$

$$\vec{P} = \begin{pmatrix} P_1 - \frac{A_{LO}^2}{2} \\ P_2 - \frac{A_{LO}^2}{2} \\ P_3 - \frac{A_{LO}^2}{2} \\ P_4 - \frac{A_{LO}^2}{2} \end{pmatrix} \tag{1.4}$$

and

$$\hat{x} = M^{-1}\begin{pmatrix} P_1 \\ P_2 \\ P_3 \end{pmatrix} = \begin{pmatrix} RSSI \\ \mathrm{I} \\ \mathrm{Q} \end{pmatrix} \tag{1.5}$$

After this brief description about Multi-Port receivers next follows an enumeration of advantages and disadvantages of this architecture:

1.3 Advantages of Multi-Port Structures as Communication Receiver:

1. Wideband characteristics allows the system to operate in a multi-standards spectrum environment (e.g., *GSM, LTE, WiFi*)
2. The passive circuitry implementation provides high linearity and low loss
3. Biased power detector requires very low *RF* and *LO* power to operate adequately
4. The circuit is scalable with frequency and passivity provides by directionality. In time division duplex application, the Multi-Port can be used for transmitter and receiver simultaneously. Therefore, there is a significant reduction in circuitry for the transceiver.

1.4 Challenges of Multi-Port structures as Communication Receiver:

The Diode detector, a key element of the Multi-Port Structure, is highly nonlinear. Therefore, it requires precise *AGC* and *DSP* techniques to monitor and optimize the detector. The challenge associated with the implementation of a single architecture to address multi-standards is summarized:

- It is required to cover a wider band of frequency (i.e., more than 5 GHz to be able to cover applications/services in the band from 800 MHz to 6 GHz). Effectively, the solution now requires the consideration of wide band performance

requirements as opposed to narrow band performance requirements. The wide-band requirement of the *RF AFE* becomes significantly more complex and more expensive. For example, it is necessary to operate in the presence of and reject out of band interference (*OBI*) representing other standards within the sampling bandwidth of the Multi-Port receiver and operate with challenging Harmonic Rejection (*HR*) requirements.

- Thus, the *RF-AFE* is exposed to interference levels that a narrow-band radio is not (i.e., Narrow-Band radios are protected by their filters that are located in front of the Low Noise Amplifier (*LNA*). The *RF-AFE* requirements impose complexity and increased performance requirements when operating in a wide band environment. For example, the specification requirements imposed on overall Linearity, Noise Figure, Oscillator tracking range, all become amplified.

- Computationally, the wide band model imposes significant computational challenges on the digital algorithms. These algorithms must not only be able to address the wide band *RF* scenario presented to the Multi-Port front end but also, address and resolve non linearity which exist within the *RF* circuitry itself.

- Eq. [1.3 to 1.5] previously presented form the basis of the key equations required to overcome the challenges mentioned

The architectural concept of providing structure to demodulate any standard is similar to that of the *SDR*. In general, the *SDR* concept represents a collection of *DSP* and *RF* processing blocks that can be reprogrammed or reconfigured through the use of firmware/software interfaces without loss of performance.

The Chapters and Sections which follow provide the analytical and simulated results showing how the wide band Multi-Port receiver can achieve optimized performance equivalent to a narrow band application specific receiver. Furthermore, this can be implemented in a manner which allows for mass production and low cost processes.

1.5 Literature Review

Multi-Port structures originated many decades ago (i.e., 1960s and 1970s) when they were introduced as a means to perform *RF* and Microwave measurements. This

technology was initially used in *RF* measurements particularly for Radar applications. Today research in the area of measurements using Six-Ports structures continues due to its flexibility, capability and accuracy for application in instrumentation (Bensmida Ref: [12]).

Due to its architectural simplicity, a Six-Port down converter architecture remains an important topic in research for applications in the field of Wireless Communications.

Several papers in the literature describe implementing solutions with associated mathematical algorithms. Sebastien M. Winter at all in Ref: [13] presents a Six-Port receiver *AFE* structure based on a Wilkinson power divider and three hybrid couplers. Their solution was implemented using meandered structures implemented in a multilayer packaging process. The paper claims there is a size reduction of about 78% when compared with a planar design.

Tim Hetchel [14] presents a mathematical derivation of a Six-Port receiver. In Ref: [15] Sang-Yung at all implemented a Six-Port prototype operating at 2.4 GHz. The circuit is realized by using power dividers/combiners and polyphase networks.

[16] presents the *EVM* for a V-band down converter for modulation levels up to 32QAM. That is a very low modulation level for the in use DVB-S2x standard. Xing You Xu at all in Ref: [17] proposes an *SDR* receiver platform based on a new substrate integrated waveguide Six-Port structure. The authors claim that their *SDR* receiver platform operates from 22 to 26 GHz and is designed to be robust, low cost, and suitable for different communication schemes. Ref: [18] and [19] explore similar ideas. Mallat in Ref: [20] provides a comparison of Six-Port and standard Zero IF receivers in the 60 GHz band. Also, at the E-band, Tatu in [21] published this work applied radar for automobile application. Ref [22] - [25], present papers that are focused on the calibration of the Six-Port down converter. The above cited papers fail to provide a system analysis tied together with an implementation as we do in our research. [26] and [27] present the analysis of the Six-Port system applied to multi-carrier modulation. [28] introduces the idea of Carrier interleaving to support increased data rate in Six-Port receivers and complementary to this work, [29] publishes a balanced antenna design. Mallat et al in [30] propose a Milimiter wave Six-Port receiver using cross-polarized antennas.

In 1992, Mitola in Ref [1] introduced a new receiver architecture named Software Defined Radio. Abidi in Ref [8] describes with more in depth circuit design. This reference also proposes the path to this new architecture. In this thesis, the concept of *SDR* is combined with the Multi-Port concept.

The *SDR* architecture provides significant operating advantages as compared to present day multi-chip architectures. This architecture provides a solution that addresses as many standards as possible with one silicon mobile platform instead of using the approach of adding separate radio hardware for every application needed.

Today, Satellite Set Top Boxes (*STBs*) use a similar approach as what was described for Mobile Wireless. If a household desires to receive two simultaneous TV channels in different locations of the home, the box will need to support this functionality by using two down-converters. The solution is implemented in a similar manner as cell phones are implemented using today's technology. On the other hand, the requirements for the *AFE* for Satellite are not as strong as they are for cellular. The reason is because it is generally a Line of Sight (*LOS*) link. Another factor is that the interference generated by other communication systems are not in the same band. Therefore, *LNB* will not suffer strong *OBI* as it does for the application in the bands from 800 MHz to 6 GHz. An *AFE* that operates from 800 MHz to 6 GHz will suffer interference from Cell base stations at the same time it is receiving terrestrial TV (*ISDB-T, ATSC or DVB-T*), *WiFi* and possibly *LTE* signals. There are many publications on this topic e.g. [31] - [47].

1.6 Goal of the Thesis

This thesis proposes the analytical simulated model of an end-to-end communication system using Multi-Port down-converter techniques. This proposed model accompanied with simulation and mathematical analysis will be shown that the architecture concept is capable of addressing new and emerging mobile communication systems as well as the Satellite Low Noise Blocks (*LNBs*) and demodulators. This research proposal is based upon the following key steps:

1. Review existing similar algorithms and provide analytical insight not covered within the existing published papers. I.e., Optimization of the *EVM* through diode bias control.

2. Derive a variant of these algorithms to reduce the implementation effort. In addition, it can be shown that the new derived algorithm can be applied to the existing concepts and provide a performance improvement. This is especially important in the area of simultaneous channel demodulation [1].

[1]Simultaneous Channel Demodulation: This means simultaneous operation in different bands. This is the case when the receiver operates on networks bellow 6 GHz.

3. Developed a detailed Simulink model that emulates the radio frequency (*RF*) and Digital Baseband of a Six-Port receiver. In contrast to other published results, the technique described within this these only requires a controlled continuous bias to the diodes. The method in which this bias control is applied represents a novel algorithm that reduces the (*EVM*) through adaptive control of the diode bias point.

4. A detailed analysis analyses the impact of the system matrix illness on the receiving I and Q signals *EVM*. This analysis is done by verifying the condition number of the system matrix. The condition number of the system matrix ($\mathbf{M}$) serves as an indication of how well conditioned the matrix at a given frequency band.

5. A design process to estimate the initial diode bias voltage to be provided to the optimizer. This initial value will avoid the optimizer to get trapped into local optimum minimum points. Initial value is a critical point during optimization.

6. A process to mitigate nonlinearities of the diodes in Multi-Port receivers. By using a very precise AGC the signal at the diodes can be bounded to operate on a region of the I-V curve that can be well fit by a second-order polynomial.

7. The analysis modeling and simulation of memory effects on the performance of the system. This analysis reduces the diode mathematical representation to a power series polynomial. This avoids the need of usage of more complex representations such as Volterra series.

1.7 The organization of this Thesis.

In Chapter 2, the block diagram of the Six-Port down converter is provided and described. The function of each blocks as well as, the key interaction and integration aspects for each are explained. How to obtain performance results obtained by this integration blocks (including sensitivity analysis), is provided in detail in Chapter 3.

In Chapter 3, we provide explanation about the Simulink model such as: Why we select Simulink as the basis for our tool. It also provides how the impairments were modeled, how to select and run the communication system using these impairments. It also provides information in how to run the model and collect information about

the system performance. More details about the model can be found at E which the Simulink model is describing the Multi-Port down converter is presented. The behavioral model for each block is provided along with a comparison of the model with other *RF* simulation programs. The key elements of the model, the Diode, *LNA*, *LO* and Automatic Gain Control *AGC* are individually addressed. We also present the system optimization by measuring the Error Vector Magnitude (EVM) of the received signal [2].

In Chapter 4, the novel method that computes the optimum diode operation bias point and reduces the *LO* power requirements are described. A diode bias algorithm that optimizes the signal-to-noise ratio *SNR* as a function of varying or changing DC bias voltage at the anode. References [48], [49] and [50] previously introduced the concept of using a fixed bias to the power detectors however they did not present algorithms that search for the optimum bias point as is done within this thesis. Furthermore, the optimization analysis and algorithm for a Six-Port down converter, simulation results summarizing *SNR* and I and Q scatter plots resulting from optimization of the diode bias and *LO* power variation compensation is presented.

In Chapter 5, a method to determine the initial value setting for the diode bias voltage is presented. This chapter presents a method for which the designer can estimate and determine the initial diode voltage bias through a five step process. This process is implemented on four off the shelf diodes. The results are also presented in this chapter.

In Chapter 6, a study of memory effects of the diode on the performance of the system is analyzed. We characterize the diode capacitance in *ADS* and memory was added to the diode model. After the characterization of memory behavior, the diode with memory is introduced into the Simulink model. Simulation results are presented and discussed on this chapter.

In Chapter 7, we present the analysis of perturbation on the system matrix $\mathbf{M}$. This analysis has the purpose to verify the performance of the system when the Matrix $\mathbf{M}$ is perturbed. A metric based upon the condition number is analyzed and presented.

In Chapter 8, the mitigation of high-order intermodulation in Multi-Port receivers is analyzed. The problem is presented and a couple of solutions are proposed.) Limit the excursion of the AC voltage over Vbias or by increasing the size of the system

[2] Communication System Performance is usually measured by means of Bit Error Rate (BER). Systems in general operate with a *BER* less than 10^{-6}. To optimize a system by measuring *BER* it would take long time to respond to the feedback. Therefore it is more convenient to use *EVM* instead.

matrix **M** considering more nonlinear behavior or the system.

In Chapter 9, we present the Simulink model validation against the published measured results in [48], [49] and [50]. The objective of this validation is to show that the model simulation results are consistent with the tested implementation.

In Chapter 10, we conclude the research findings and we also suggest future research work to improve and answer questions not covered during this research.

Chapter 2

Background

Multi-Port receivers are wide band in nature, where down conversion is implemented using diodes instead of complex mixers and the estimation of I and Q is done using power measurements. These characteristics make Multi-Port receivers a good fit for multi standard demodulation i.e., *SDR*. This section will present the Multi-Port receiver system architecture with a mathematical analysis (how to estimate I and Q from power measurements) and estimation of interference levels for some standards (e.g., *WiFi*, *LTE*).
The literature review summarized most of the papers relevant to this thesis. However, these papers do not provide a system analysis that connects with an implementation. Additionally, none of the authors present system level *EVM* and or *SNR* performance results due to *LO* power variation.

2.1 Architecture Comparison

There are four most popular architectures in receivers: Super Heterodyne, Direct conversion (Zero-IF), Low IF and Bandpass sampling. Generally these architectures are selected for a project considering the following factors: power consumption (military and consumer in mobile applications.), cost (cellular and TV receivers applications) and performance.

Super Heterodyne: This is one of the most common architectures for receivers. It has the characteristics of translating one or more times the replica of the received signal by using mixers. It will deliver at the output a replica of the received signal centered at a given fixed intermediate frequency. The disadvantage of this architecture is the requirement of bulky filters after each conversion. That makes this solution less competitive in terms of pricing. [62] provides more details on this topic.

Direct Conversion (*Zero$_I$F*)**:** This solution translates the replica of the desired signal to zero frequency in one translation step. There is no need of bulky filters. The baseband filters are usually designed and integrated in the *RFiC* down-converter. [62] provides more details on this topic.

Low IF: This architecture is very similar to the superheterodyne architecture but the intermediate frequency is generally lower than superheterodyne and can be variable. In certain designs the value of the *IF* vary with respect to the carrier frequency. Usually this solution has the last down-conversion done digitally. The disadvantage for this type of solution is with respect to the Analog to Digital Converters' *ADC* price which increase when higher clock speeds are required. Low *IF* architecture presents some restrictions during its selection [62].

Bandpass Sampling: This architecture is very attractive because the sampling is done lower compared with the carrier frequency. The sampling frequency selection is done proportional to the value of the desired signal frequency bandwidth.[108], [62] and [109] provide more details on this topic.

2.2 Zero-IF Down Converter using Multi-Port Structures

The architecture for the Multi-Port receiver is implemented as a Zero-IF down-converter depicted in Fig. 2.1. Zero-IF architecture was selected because it is the most used *RF-FE* architecture for low cost devices. This block diagram forms the basis for which simulation results are obtained and presented. Within this architecture, Port 1 is the *RF* input signal split into four branches using power splitters. Port 2 is the *LO* input port and ports 3 through 6 are the measured power at each of the four branches.

The received signal amplified by the *LNA* and *VGA* is then split into four branches. Each signal is fed into a coupler that has one input connected to the received *RF* signal

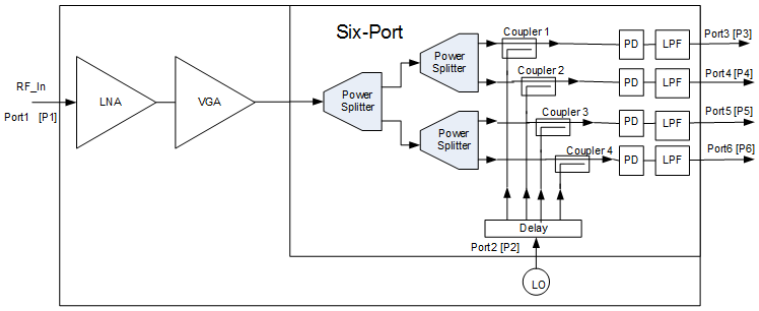

Figure 2.1: An implementation of the *RF* section of a Zero-IF Multi-Port Receiver

and the other input port connected to one of the four ports of the delay block. The delayed *LO* signal is summed with the received signal and the power is measured by the Power Detector (*PD*). That function is performed by the Schottky diodes.

With this configuration it can be shown in [11] that knowing $\vec{P}$ and the *LO* power and phases, the *RSSI*, *I* and *Q* values can be estimated using the following equation:

$$\vec{P} = M\vec{x} \Rightarrow \vec{x} = M^{-1}\vec{P} \tag{2.1}$$

where the matrix **M**(4x3), the vector $\vec{P_1}$ and a vector $\vec{x}$ are defined such that:

$$M_{(4\times3)} = \begin{pmatrix} 1 & A_{LO}\cos(\Theta_1) & -A_{LO}\sin(\Theta_1) \\ 1 & A_{LO}\cos(\Theta_2) & -A_{LO}\sin(\Theta_2) \\ 1 & A_{LO}\cos(\Theta_3) & -A_{LO}\sin(\Theta_3) \\ 1 & A_{LO}\cos(\Theta_4) & -A_{LO}\sin(\Theta_4) \end{pmatrix} \tag{2.2}$$

Where A_{LO} is the local oscillator amplitude. Using the output powers on the figure 2.1 the vector is constructed hence, [11] shows that the *RSSI*, *I* and *Q* can be estimated.

$$\vec{P} = \begin{pmatrix} P_1 - \frac{A_{LO}^2}{2} \\ P_2 - \frac{A_{LO}^2}{2} \\ P_3 - \frac{A_{LO}^2}{2} \\ P_4 - \frac{A_{LO}^2}{2} \end{pmatrix} \tag{2.3}$$

and

$$\hat{x} = \begin{pmatrix} \frac{\left(x_I^2(t)+x_Q^2(t)\right)}{2} \\ \hat{x}_I(t) \\ \hat{x}_Q(t) \end{pmatrix} = \begin{pmatrix} RSSI \\ \mathrm{I} \\ \mathrm{Q} \end{pmatrix} \tag{2.4}$$

M must be at minimum a (3x3) matrix in order to solve (2.1). Therefore, we can eliminate one power measurement (P_1, P_2, P_3 *or* P_4) and call this a Five-Port instead of Six-Port system. Once the row rank of the matrix **M** is equal to or greater than 3 (e.g., *rank*(**M**) ≥ 3)[1] and **M** is not ill-conditioned[2], the Six-Port and Five-Port systems are equivalent. In practice, Five-Port systems are more attractive due to their simplicity compared with Six-Ports.

A Five-Port system requires only three independent power measurements. Hence, (2.2) will be reduced to:

$$M_{(3\times3)} = \begin{pmatrix} 1 & A_{LO}\cos(\Theta_1) & -A_{LO}\sin(\Theta_1) \\ 1 & A_{LO}\cos(\Theta_2) & -A_{LO}\sin(\Theta_2) \\ 1 & A_{LO}\cos(\Theta_3) & -A_{LO}\sin(\Theta_3) \end{pmatrix} \tag{2.5}$$

The rank of **M** must be at least 3 and row linear independence of **M** is guaranteed by the *LO* phase differences. A reduced power vector $\vec{P_1}$ is given by:

$$\vec{P} = \begin{pmatrix} P_1 - \frac{A_{LO}^2}{2} \\ P_2 - \frac{A_{LO}^2}{2} \\ P_3 - \frac{A_{LO}^2}{2} \end{pmatrix} \tag{2.6}$$

Therefore, (2.1) can be written as:

$$\begin{pmatrix} RSSI \\ \mathrm{I} \\ \mathrm{Q} \end{pmatrix} = M^{-1} * \begin{pmatrix} P_1 - \frac{A_{LO}^2}{2} \\ P_2 - \frac{A_{LO}^2}{2} \\ P_3 - \frac{A_{LO}^2}{2} \end{pmatrix} \tag{2.7}$$

Let us assume that **M** is full Rank. Therefore, $\mathbf{M}^{-1}$ is given as:

$$M^{-1} = \begin{pmatrix} m_{(1,1)} & m_{(1,2)} & m_{(1,3)} \\ m_{(2,1)} & m_{(2,2)} & m_{(2,3)} \\ m_{(3,1)} & m_{(3,2)} & m_{(3,3)} \end{pmatrix} \tag{2.8}$$

The system is capable of functioning with many other impairments that can be present in the power measurements. *DC* offset and second-order type *RF* self mixing products are likely to be presented and result in the possibility of degrade estimation of I and Q. This structure and this thesis will demonstrate how the system operates

[1]The maximum number of linearly independent rows in a matrix M is called the row rank of M.

[2]A system is ill-conditioned, if small errors in the data will produce large errors in the solution.

with both signal level and device level nonlinearities. Details about how to mitigate these effects are detailed in [51] and [52].

2.3 Multi-Port Communication System Architecture and Modeling

This section provides the system level analysis, simulation and description for the Multi-Port receiver system. The system model is specifically designed to evaluate the Multi-Port receiver architecture proposed in this research. In addition, this model allows evaluation in stand-alone operation (ideal) and in wideband mode where the presence of multiple standards (i.e., Terrestrial TV and LTE) is encountered. The model also allows for the injection of nonlinearities to reflect real world conditions.
The analysis conveyed in this section is divided in two parts:

1. Analysis of the RF-FE considering impairments such as: *NF*, *PN*, *AGC* and *RF* nonlinearities (e.g., *IIP2*, *IIP3*). These impairments are considered in the Simulink model.

2. The *ADC* characteristics such as dynamic range, effective number of bits (*ENOB*

The wireless communication system model used for simulation and analysis carried on during our research is shown in Figure 2.2. Our focus in this thesis is on the receiver (e.g., *LNA* and *VGA*, Down converter and Demodulator) and most specifically on the Multi-Port receiver. The purpose of this model is to perform simulation using many communication system parameter settings and many impairments (see Chap. 3 for details). Chapter 3 is dedicated to the detailed explanation of the model and its validation which is based on the results of [48], [49] and [50] is covered in chapter 9. Also more information about the model design is presented in appendix E

2.3.1 Transmitter

The transmitter block is modeled by using an information source block that generates a *PRBS* signal. This block represents the user data to be transmitted to the other location (i.e., From *BTS* to *CPE*). It is also referred to as payload data either to or from the user. This data needs to be encoded, interleaved and mapped or modulated. The mapper will map a set of bits (2^N) bits into a symbol belonging from the set of

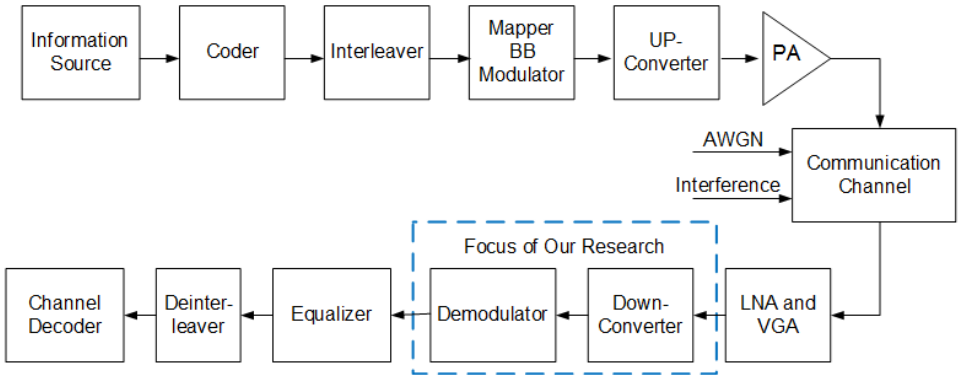

Figure 2.2: Communications System (Multi-Port system)

symbols available for a given digital modulation (e.g., 64QAM has an alphabet set of 64 symbols). The *RRC* filter has the purpose of shaping the signal bandwidth and therefore removing undesired out of band frequency components from the spectrum. The *DAC* is responsible to convert discrete symbols into an analog baseband signal. The analog (I and Q) signals will be up converted to the desired carrier frequency using the up-converter block. After the up-converter there is usually a power amplifier block. The power amplifier can be accompanied with a pre-amplifier. In the case of the study, we consider the *PA* to be both memoryless and nonlinear up to the third-order, which is mathematically represented by Eq. 2.9 and the block diagram is shown in Fig. 2.3. The assumptions and limitations of using this equation are discussed in [53].

$$y = \sum_{i=0}^{2} k_i x^{i+1} = k_0 x + k_1 x^2 + k_2 x^3 \tag{2.9}$$

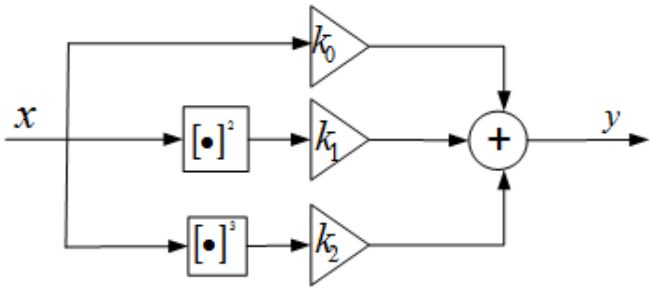

Figure 2.3: PA Model with Nonlinearities

k_0 is the gain (times) for the linear region of the *PA*. The coefficients $[k_1, k_2]$ are obtained from the following nonlinearities characteristics and specified during the

design: *P1dB*, *IIP2* and *IIP3*.

$$IIP_2 = 20\log_{10}\left(\frac{k_1}{k_2}\right) \tag{2.10}$$

$$IIP_3 = 20\log_{10}\left(2\sqrt{\frac{k_1}{3|k_3|}}\right) \tag{2.11}$$

$$P1dB = 20\log_{10}\left(0.38\sqrt{\frac{k_1}{|k_3|}}\right) \tag{2.12}$$

The complete mathematical derivation of these equations can be found in Appendix B. Therefore, by providing the intercept points for the device, the coefficients for the Eq. 2.9.

2.3.2 Communication Channel

The communication channel represents both free space attenuation (flat-fading) and multipath attenuation due to fading. This model allows the investigation of the proposed receiver structure in the presence of both flat fading and multipath fading. Mitigation techniques are provided.

2.3.3 Receiver RF-AFE

The *RF-AFE* includes the *BPF*, *LNA*, *VGA*, *LO* and Six-Port down converter. The design of the bandpass filter *BPF*, *LO*, *LNA* and *VGA* are not in the scope of this document but they must be designed to have a good performance in the frequency band of operation. Fig.2.4 illustrates a typical architecture for a Six-Port receiver. This architecture can be divided into three sections: *RF* front end (I), *RF* front end (II) and baseband.

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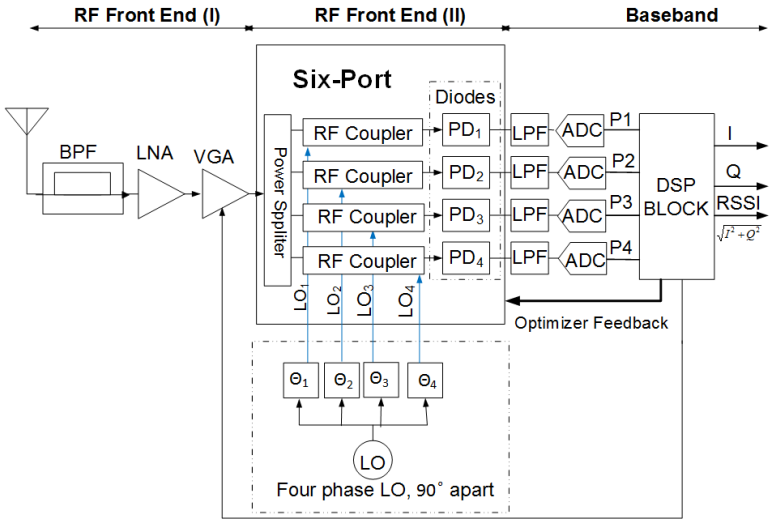


Figure 2.4: Six-Port Receiver.

RF Front End(I): This block is composed of a (*BPF*), *LNA* and variable gain amplifier (*VGA*). Due to the fully occupied spectrum environment Adjacent Channel Interference *(ACI)* and out of band interference (OBI) will occur with high probability. Interference is discussed in detail in Section 2.5. Therefore, to operate under strong interference, the *LNA* includes nonlinearity effects. Another system impartment considered in the *LNA* is noise figure *(NF)*. The *LNA* is modeled similar to the model used for the *PA* but considering *NF* effects and it is shown in Fig. 2.5.

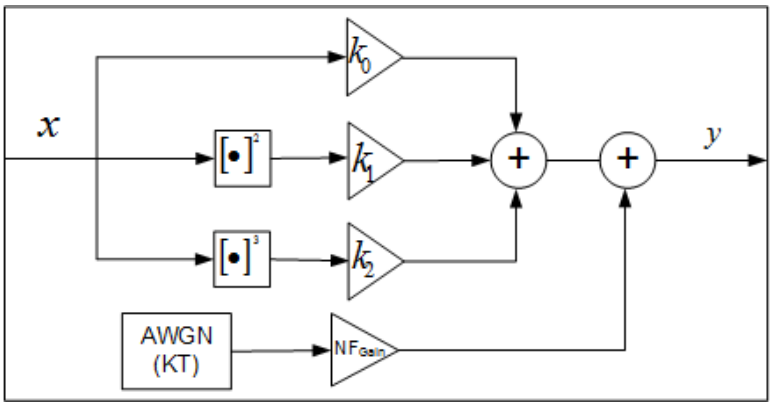


Figure 2.5: Low Noise Amplifier with NF and Nonlinearities.

The purpose of the *VGA* is to maintain the signal variation at the input of the Multi-Port receiver to a minimal dynamic range. The target is to maintain this variation within a maximum 20 dB swing (value established for our model). This improves

the performance of the receiver by ensuring the diode signal variation remains within a reasonable variation range. Further details describing the impact of the received signal power on the diode is provided in Chapter 8.

RF Front End (II): This block is composed of the Six-Port down converter, which includes power splitters, local oscillator (*LO*), *RF* couplers and diodes for power detection (*PD*).

Local Oscillator: It is not in the purpose of this document to describe how to design the Local Oscillator, but some *LO* architectures are more feasible than others, and within the feasible architectures we can mention the Rotary Traveling Wave Oscillator in [54] and Ring Oscillator [55, Chap.8]. In this architecture, the local oscillator needs to feed four couplers, each one with a different phase. In Fig. 2.1, the *LO* signal at Port 2 passes through a delay line. This line will delay the *LO* signal such that at each of the four couplers the *LO* signals will have their phase $\vec{\Phi} = [\phi_1, \phi_2, \phi_3, \phi_4] = [0, 90, 180, 270]$ degrees. The impact of either phase rotation $\vec{\Phi} = [90, 180, 270, 0]$ and or phase errors $\vec{\Phi} = [\phi_1 \pm \epsilon_1, \phi_2 \pm \epsilon_2, \phi_3 \pm \epsilon_3, \phi_4 \pm \epsilon_4]$ are shown in Chapter E.

Baseband: This section is composed of analogue low frequency blocks (*LPF* and *ADCs*) as well as the digital signal processing (*DSP*) block.

The *RF* front end signal from the *VGA* is divided into four paths by the power splitter. Orthogonal phases of the *LO* are added to each signal path using *RF* couplers. At this point the power of each received signal plus the *LO* power is fed into a nonlinear *PD*. The output of the *PD* is a nonlinear combination of the sum of *LO* and received signals. Each signal is filtered using a low pass filter (*LPF*)and converted to a digital word using analog-to-digital converters (i.e., $\vec{P} = [P_1\ P_2\ P_3\ P_4]^T$). The magnitude of the I and Q signals is calculated in *DSP* using a discrete time domain algorithm. The DSP block also calculates the received signal strength indicator (*RSSI*) value. The *RSSI* can be used to calculate the correction voltage for the *VGA*, and [14] provides detailed mathematical analysis of the Six-Port system including *I* and *Q* and *RSSI* calculations.

2.4 System Impairments

In the process of the Multi-Port system analysis, impairments will be introduced with specific conditions and underlying assumptions. The impairments represent real system effects encountered during practical system design. The system analysis identifies these key sets of parameters and underlying assumptions. The impairments are important as they translate to system noise. These system impairments translate into increased total noise as seen by the Multi-Port receiver structure. The net effect of this increased noise is a reduction in *SNR* and therefore increase in *BER*. The algorithms presented will be shown to operate in the presence of real system impairments.

2.4.1 Effective Number of Bits - *ENOB*

F Goodenough in [57] suggested a figure of merit for *ADC* based on power dissipation, resolution and sampling rate. Walden in [58] and [59] suggests the *ENOB* as being the figure of merit for analog-to-digital converters. The *ENOB* figure of merit is largely used in the designs and analysis. It is also appropriate to establish a baseline for this analysis.
As in [55], the effective number of bits (*ENOB*) is related to the *ADC*'s *SNR* by the expression:

$$ENOB = \frac{(SNR - 1.76)}{6.02} \tag{2.13}$$

2.4.2 Noise Bandwidth and Processing Gain

The noise bandwidth is defined as being the bandwidth of an ideal filter (brick-wall filter) that would let the same total integrated noise by the root raised cosine (*RRC*) filter implemented within each of the baseband modems. Processing gain is the gain provided by the ratio of the sampling rate and the Nyquist equivalent bandwidth. [56] provides a detailed requirements study of ADC performance for *WCDMA* base stations where this topic is covered in details. I.e., if a receiver is 1 Ghz wide and it is receiving a signal confined in 20 MHz. The noise bandwidth is the amount of noise integrated over the 20 MHz band width but not in 1GHz bandwidth.

$$Gain = 10\log_{10}\left(\frac{BW_{Nyq}}{BW_{\eta}}\right) \tag{2.14}$$

Notice that the noise is integrated over the channel band (Brick-wall filter bandwidth) even if the receiver is wideband.

2.4.3 PAPR

The peak-to-average power ratio (*PAPR*) is defined as the ratio of the maximum peak power to average power that a particular digitally modulated signal will produce. For an *MQAM* modulated signal the peak to average power will increase with the number of amplitude modulated levels allowed which is (2^M). [60] and [61] present a detailed analysis about this topic and propose methods of reducing *PAPR* for *OFDM* systems. The *PAPR* numbers must be taken into account when computing the maximum allowable *ADC* input signal to ensure the *ADC* does not saturate or clip. This will assure that the *BER* will not be degrade by the occurrence of nonlinearity effects due to peak power.

2.4.4 Received *SNR* at output of ADC

The received *SNR* at the output of the *ADC* will be calculated based on the theoretical *BER* curve for a given modulation. In a chip design, the *SNR* or requirement is usually provided by the *DSP* team. If we assume that for a 64QAM single carrier modulated signal the required *SNR* or *Eb/No* is approximately 26 dB for a Bit Error Rate of 10E-6. [70]

2.4.5 ADC Input Levels and AGC Dynamic Range

The *ADC* maximum peak-to-peak voltage is the bound for the system designer to estimate the *ADC* noise floor and the maximum input level allowable without degrading the system performance.

The maximum allowable *ADC* input level as being the ADC's full scale input voltage which should be backed off the worst case *PAPR* with some additional margin (e.g., 3.0 dB). This specification is used to calculate the *AGC* requirements or dynamic range.

The minimum detectable signal level at the *ADC* input is defined by the sum of the total noise at the *ADC* input and the required *SNR*. The total input noise is composed of several imperfections:

1. *RF* thermal noise floor
2. *RF* intermodulation noise floor
3. *LO* Phase Noise
4. Front-End Noise Figure
5. *ADC* noise floor defined by its *ENOB*

Fig 2.6 presents a scenario where shows the minimum *SNR* required for a system to perform under certain degradation. This figure shows the minimum signal strength that shall be present at the antenna on which by adding *NF* and all other k^th imperfections (e.g., *PN*, *IIP2*, *IIP3*, *I*,*Q* imbalance, *ADC* quantization, etc) listed above and represented by the index K in this figure will degrade the performance by certain amount of dB. This effect is graphically explained in Fig 2.6. At the antenna the signal is represented by the white blue (Desired signal) and the noise density which is represented by the *AWGN* (Black trace). After the *LNA*, its noise figure (plus any passive component loss in front of it) is added to *AWGN* which will reduce the *SNR* by the same amount as the *NF*. That is represented by the brown curve. The last noise contribution is added to the brown curve and the total noise is represented by the red curve in the figure.

If we assume that each and every imperfection will equally contribute for the decrease in *SNR*, the following equation of the total noise at the input of the *ADC* will hold and

$$\eta_{total} = \underbrace{-174dBm/Hz + 10\log_{10}(B)}_{10\log_{10}(KTB)} + \underbrace{\eta_{imp} + 10\log_{10}(k)}_{ImperfectionNoise} + 10\log(F) \tag{2.15}$$

Gu in [62] presents the derivation for the relative noise of interference level increment $R_{\Delta\eta}$ from all degradations. The formula he presented is expressed in Eq 2.16

$$R_{\Delta\eta} = 10\log_{10}\left(10^{\frac{\Delta\eta}{10}} - 1\right) \tag{2.16}$$

In other words, the $R_{\Delta\eta}$ noise (degradation due to implementation) value can be assume the maximum contribution for a certain value in dB of reduction in the *SNR*. This figure shows this effect at the input of the *ADC*. Therefore, *ADC* noise and nonlinearity is not

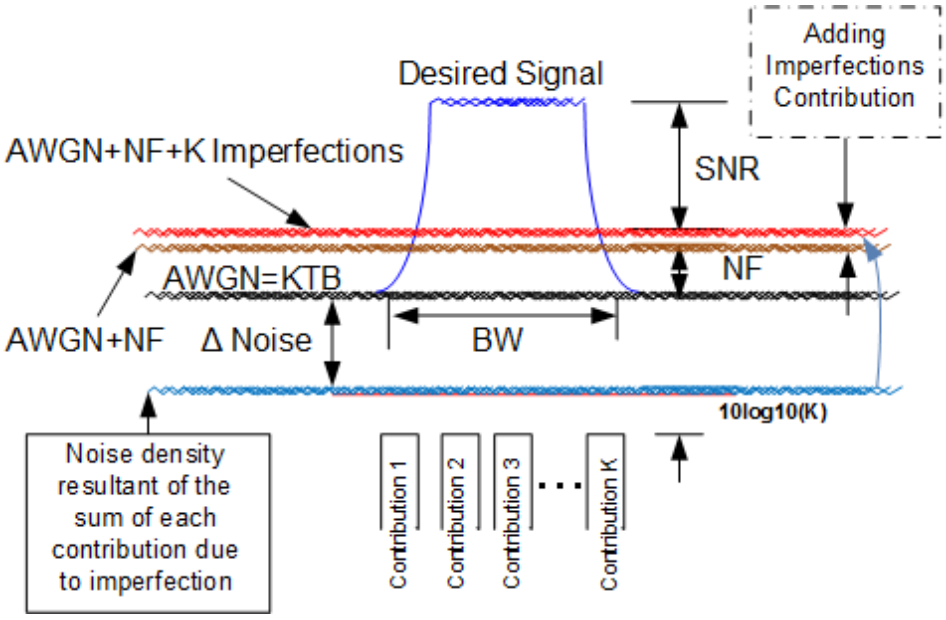


Figure 2.6: Estimation of the Minimum Received Signal Required at the Antenna.

considered in this figure but must be considered in the system level architecture. This effect of *SNR* reduction is shown in table 2.1.

Table 2.1: Relative Noise Level change vc. *SNR* degradation: Copy of [62]

SNR Degradation $\Delta(dB)$	Relative Noise/Interference Increment, $R_{\Delta\eta}$
0.1	-16.3
0.5	-9.14
1.0	-5.87
2.0	-2.33
3.0	-0.02

DNL, *INL* and quantization plus *ADC* clock jitter has to be added to the system performance degradation.

2.5 The Interference Problem in Wideband Communication Receivers

In previous sections, practical circuit related impairments that must be dealt with by any receiver or communication system was presented along with how these impairments are introduced into the system simulation model. In addition how the Multi-Port system computes the values of I and Q from power measurements was also presented. The most significant degradation effect present at the receiver input is due to man made interference. As this thesis proposes to operate in wideband mode, the presence of many standards and signal spectrums at the *ADC* input impose severe operational challenges. In the real world environment, the spectrum is almost fully used by many dierent services (e.g., *WiFi*, *LTE*, *FM* Broadcasting, Aviation, Police, Terrestrial TV, etcetera.) The most important two factors that makes a wideband receiver design challenging are:

1. Design circuits that have flat frequency response over a wide range of frequency.
2. Be able to cope and mitigate interferences (*ACI* and *OBI*) as presented by Allen in [63].

Interference can generate degradation by causing nonlinear behavior in the system. Table 2.2 shows many sub 6 GHz services operating in North America. A possible interfering scenario that can occur is to have a receiver operating at the end of 2.3 GHz band. Its desired signal has very low power strength and, at the same time, it is located very close to a *WiFi* AP operating at 2.4 GHz. Due to the fact that the system is wideband, even though the receiver is operating in a different service band, its *LNA* will also receive the *WiFi* signal at a very high power. Therefore, the *LNA* has to be designed with such a *IIP3* that can cope with both signals (The desired signal and *WiFi* interference) while still providing the required performance (low acceptable noise generated by the intermodulation products) for the required service.

One example of two different operation systems coexisting at the same band is the Radar on the ships' deck and *LTE* stations located at the coast. In this case, both systems operate at 3.5 GHz band and due to the proximity of the radars from the Navy ships close to the coast (*LTE* receivers stations) the interference occurs. Fig 2.7 borrowed from [64] illustrates this scenario in great detail. These ships transmit a large

Table 2.2: Spectrum Occupancy

Standard	Frequency Band	Maximum Power	Country
Terrestrial TV	470 - 693 MHz	+46 dBm or +60 dBmi [65]	Brazil
LTE	700 - 800 MHz	46 dBm+Ant_{Gain}	USA and Canada
LTE	850 MHz	24 dBm [66]	USA
AMPS	900 MHz	24 dBm (mobile) [62]	USA
GSM	900 MHz	33 dBm [62]	Americas
LTE	1700 MHz	23 dBm [67]	USA and Canada
GSM	1800 MHz	30 dBm (Mobile) [62]	USA and Canada
LTE	1900 MHz	23 dBm [67]	USA
LTE	2200 MHz	23 dBm [67]	
LTE	2300 MHz	23 dBm [67]	Canada
WiFi (B,G, N)	2400 - 2485 MHz	+26 dBmi	Worldwide
LTE	2500 MHz	Downlink (+46 dBm)	USA
LTE	2600 MHz	Uplink (+23 dBm)	Canada
LTE and Radar	3500 MHz	[64]	USA and Canada
ISM	4900 - 5150 MHz	+26 dBmi	North America
WiFi (A, N, AC)	5150 - 5890 MHz	+26 dBmi	Worldwide

amount of energy to be able to detect military target during operations. Therefore, degradation due to interference may occur.

Table 2.3 provides an estimation of the blockers' power for different interferences sources (different standards). The column "Interfered" represents the system suffering interference. That is: the interfered receiver has its transmitter located far away from the receiver. Column "Interferer" represents the communication system generating the interference signal which is located very close to the interfered receiver. Tx Power represents the irradiated power at the antenna of the interferer. In the column "Distance" the numbers represents the distance between the interfered receiver and the interfering transmitter. In the last column, we present the estimated interfering power present at the antenna of the receiver. To calculate the blocker power the free space law [62] is applied and is shown in Eq. 2.17. Where **D** is the distance in meters, λ is the wavelength in meters, **f** is the frequency in Hertz and **c** is the speed of the light in the vacuum.

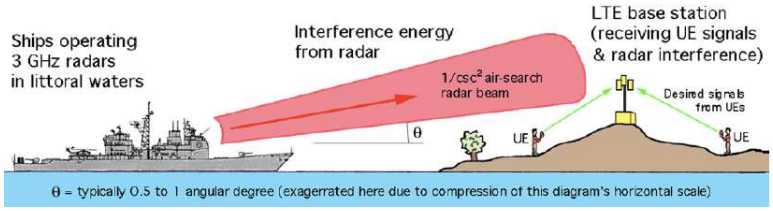


Figure 2.7: Possible interference between Radar UE and LTE (From [64]).

$$FSL = \left(\frac{4\pi D}{\lambda}\right)^2 = \left(\frac{4\pi D f}{c}\right)^2 \tag{2.17}$$

Fig. 2.8 shows the situation in detail. The receiver from station **B** desires to receive a weak signal from Station **A**. Station **C** is close by and has a frequency very much closer to the Station **A**, which will introduce interfere in station **B**. The red arrow indicates the interfering signal from station **C**. The estimation interfering power is provided in Table 2.3, these distances are believed to be practical for the associated technologies.

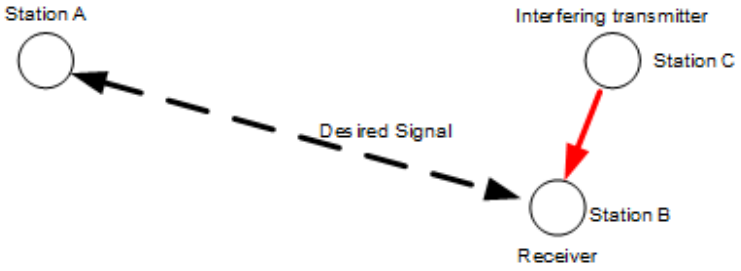


Figure 2.8: Interference from a close proximity station.

Table 2.3: Estimated Blockers' Power by Standard

Interfered	Interferer	Tx Power	Distance	Frequency	Attenuation	Blocker
WiFi	LTE	46 dBm	600 m	2.4 GHz	95.6 dB	-49.6 dBm
Terrestrial TV	LTE	53 dBm	400 m	693 MHz	81.3 dB	-28.3 dBm
LTE	WiFi	26 dBm	20 m	2.4 GHz	66.1 dB	-40.1 dBm
LTE	Radar	100 dBm	5K m	3.5 GHz	117.3 dB	-17.3 dBm

Fig. 2.9 shows a receiving signal spectrum centered at 5240 MHz and at the right without any visible interferer and its *EVM*. Observe that the value of the *EVM* is

much lower than the recommended by IEEE which is -25 dB. Therefore, its *SNR* has a high value. At the left of Fig. 2.10, we notice the presence of a strong interferer

Figure 2.9: Figure that representing signal with good EVM no interferer present.

located at 5200 MHz. Even though the interferer central frequency is 40 MHz away from the desired signal, when both signals pass through an *LNA*, the interferer will generate intermodulation and some spectrum regrowth will appear at both sides of the interferer. The intermodulation generated by the nonlinearity will fall in the frequency band of the desired signal and will reduce its *SNR*. Notice that the noise level at the left side of the desired signal is higher when the interferer is present. The increase of the noise at the right side of the desired signal is due to the third-order intermodulation spectrum density. It is created by the nonlinearity generated in the presence of the strong interferer.

The third-order intermodulation effect in the frequency domain is mathematically represented when we consider only third-order intermodulation products in Eq. 2.9 which becomes Eq.2.18 as in [53].

$$y(t) = k_0 x(t) + k_2 x(t)^3 \tag{2.18}$$

The Y(f) of the output y(t) will be given by Eq.2.19. Observe that the convolution in frequency domain will spread the occupied bandwidth twice of its value for each side of the main spectrum. Therefore, in this case it will reach up to 5250 MHz. That means $5200MHz + 10MHz(BW/2) + 2 \times 20MHz = 5250MHz$.

$$Y(f) = k_0 X(f) + k_2 X(f) * X(f) * X(f) \tag{2.19}$$

Yang in [68] provides an avenue for mitigating interferences in cognitive radios.

Figure 2.10: *EVM* degradation due to interference from a close proximity station.

2.6 Conclusion

In this chapter, an introduction to a Multi-Port communication system (Fig 2.2) was described. The section also provides system level explanation for every block constituent of the system. The key system blocks (e.g., *PA*, *LNA*, *LO*), Multi-Port down converter) will be discussed in further detail through subsequent chapters of this thesis. The mathematical analysis of the Multi-Port receiver is also provided. A few simplifications were applied during the derivation of the system matrix **M**. Full analysis of the system matrix **M**, its relevance and the information which can be obtained from this matrix is provided in Chapter (7) of this thesis. This chapter also provided a system analysis and simulation assumptions for both circuit level limitations and wideband input level spectrum assumptions. While both affect performance (available **SNR**), it is the impact of the multiple standards present at the wideband receiver input and how these effects are mitigated to form one of the most important contributions of this thesis. In the following chapters of this thesis, we discuss a methodology of biasing the diodes used for down conversion, an optimization algorithm based upon matrix **M** error minimization.

Chapter 3

Simulink Model

3.1 Introduction

In this chapter we introduce the Simulink model that was developed during our research.This model is used to capture the effects of the four novelties presented in this thesis (e.g., Optimizer, estimation of initial value for the optimizer, Memory effects and mitigation of diode nonlinearities). These four novelties are embedded in the model proving its flexibility. For instance, the user can select to run the model adding diodes memory effects on the system or not. The model is designed to run with or without the optimizer, memory effects and optimizer initial value. Adding to these options, the model includes other impairments such as nonlinearities, blockers, noise figure and carrier feedthrough (see table 3.1 for complete list).

3.2 Tool Selection

Several tools can build the communication systems. In contrast with other receiver architectures, specifically in Multi-Port receivers the estimation of I and Q are commonly done by solving a linear system (e,g., $\hat{x} = M^{-1} \times \vec{P}$) in the digital domain based on measured powers ($\vec{P}$). Therefore, a tool to model this type of receiver must have a good communications library combined with linear algebra functions. This capability allows us to focus on validating our research rather than building these capabilities. An implementation point to consider is that if we compare the amount of transistors used in a communication system, less than 10% is used in *RF* and analogue sections, the other 90% or more is used in the digital domain (*DSP*), which is generally built

using an *FPGA* during concept validation. After validation the design can stay in the *FPGA* or be ported to an *ASIC*. Therefore, a tool to synthesize the design directly to an *FPGA* and represents the *RF* behavioral, is very particularly suited to our research. For this reason, Simulink, with support of Matlab, is used. *ADS* was used for device characterization at the circuit level. In order to ensure the results obtained using this model are accurate, this model was validated using measured results. The validation process is described in details in chapter 9.

3.3 Simulink Model and Parameter Settings

One of the main contributions of this thesis is an optimizer which adaptively finds the optimum bias voltage for the diode. The optimization process happens by giving an initial value to the optimizer which in turn will find the optimum operational diode bias value. Chapters 4 and 5 cover these two points in detail. The impact on the system performance when memory effects are considered or not are is covered in chapter 6. In this section, we describe the main characteristics of the Simulink model, its purpose and the parameter settings options to run. The main purpose for building a Simulink model is to have a tool that is able to estimate the system performance due to imperfections in the Multi-Port receiver algorithm (estimation of I and Q) when there are no impairments (e.g., nonlinearities, noise figure, carrier feedthrough, etc) added to the system and when impairments are considered. The top level diagram of the model is shown in Fig. 3.1. On the left of this figure, it shows the *ADS* tools environment which is used for performing physical characterization of the diodes and filters. After the characterization of a device is done using the devices spice models in *ADS*, the characterization data is passed to Matlab on which the polynomials that represent the devices behaviours are found. These polynomials will be used in the Simulink model as a physical device behavioral model instead of using spice models. The third block from left to right is the model which is created using Simulink environment. Some sub-blocks were created using embedded Matlab, while other blocks used Simulink native blocks. The model is opened by running a script written in Matlab (see details at D). The model provides the most common options used in communication systems measurements for verification of the system performance (e.g., I and Q received constellation, *EVM*, signal spectrum and EYE diagram). Table 3.2 provides a list of configurations required for the model to run. These configurations are used to set the communication system and therefore, verify

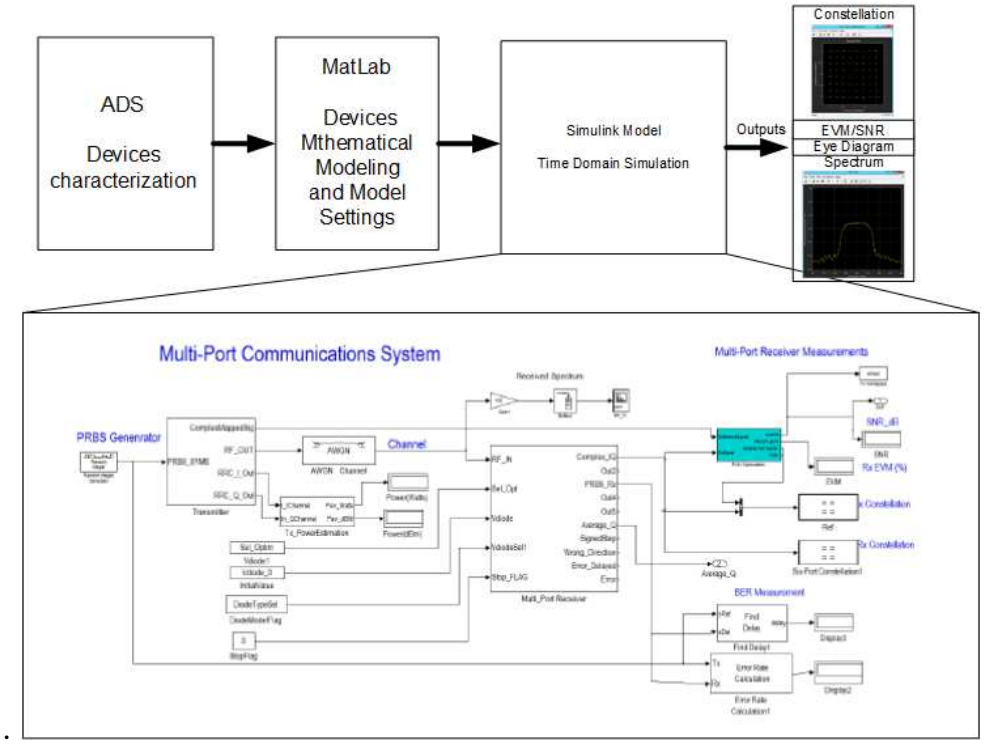


Figure 3.1: Simulink Model Block Diagram.

its performance. These configurations are selected and added to the model using the Matlab script. The selection of the configurations happen prior to open the model when the user manually set them in the script.

3.4 Transmitter

In this section we list and describe the main impairments supported by the model at the transmitter (e.g., carrier feed-through, I and Q imbalance, nonlinearities and adjacent channel interference). The model has capability to add these effects at the transmitter by setting the Matlab script file.

Carrier Feed Through: Carrier feed-through is an undesired effect that frequently occurs at the mixers. It occur when some fraction of the LO carrier appears at the output of the modulated signal and will decrease the performance of the modulated signal by increasing the EVM. The carrier feed through value is set in dB at script level. That correspond the relative value of the modulated carrier at the output referenced

Table 3.1: Model Impairments

Impairment	Block	Description
Carrier feed through		*BB* level
I and *Q* imbalance	*SSB* suppression	
Nonlinearities	*PA* and *LNA*	*P1dB*, *IIP2*and *IIP3*
AWGN	Channel	*SNR* can be set
Noise figure	*LNA*	Noise figure in dB
ACI	Adjacent Channel	Frequency and level
	Interference	of the interferer

with respect to the power of the LO signal. E. g., if we express the carrier feed through (cft) in the scripts to be 40 dBc and the modulated signal has a power of +10 dBm, the carrier feed through will have a power of -30 dBm.

Side Band Suppression: This model supports single channel, single carrier, Multi-Port communications systems. Therefore, the *RF LO* is usually set at the center of the channel which assumes perfect synchronization between transmitter and receiver. The *I* and *Q* signals should have equal amplitudes and their phases difference have to be 90° from each other. This condition assures perfect *I* and *Q* signal quality. Side Band Suppression is caused by difference in amplitudes and not having 90° phases difference. *SSB* measures the amount of energy that is generate by *I* and *Q* imbalance (phase and amplitude) that falls inside the channel and reduces the *SNR* at the transmitted signal (increases the *EVM*). In practice *I* and *Q* imbalance occurs at the up converter low pass filters, amplifiers and mixers. In practice, if the up converter is the block that generates *SSB*, this effect can be pre-correct at the baseband (*I* and *Q*) by applying amplitude and phase imbalance. All these scenarios can be implemented using the model.

Power Amplifier Nonlinearities: The second and third-order power amplifier nonlinearities can be mathematically described by Eq. 3.1. A Simulink model was created to represents these effects and is demonstrated in Fig. 3.2. In this figure there are three branches: The one on the top represents second-order nonlinearity effects, the branch at the middle represents the linear gain and at the bottom represents the third-order nonlinearity effects. The gain selections (K_0, K_1, K_2) are set at the Matlab script. The

additive white Gaussian noise block represents the noise at the transmitter. The noise at the transmitter is not as important as the noise added at the receiver because at the receiver, the signal strength is very low.

$$y = \sum_{i=0}^{2} k_i x^{i+1} = k_0 x + k_1 x^2 + k_2 x^3 \tag{3.1}$$

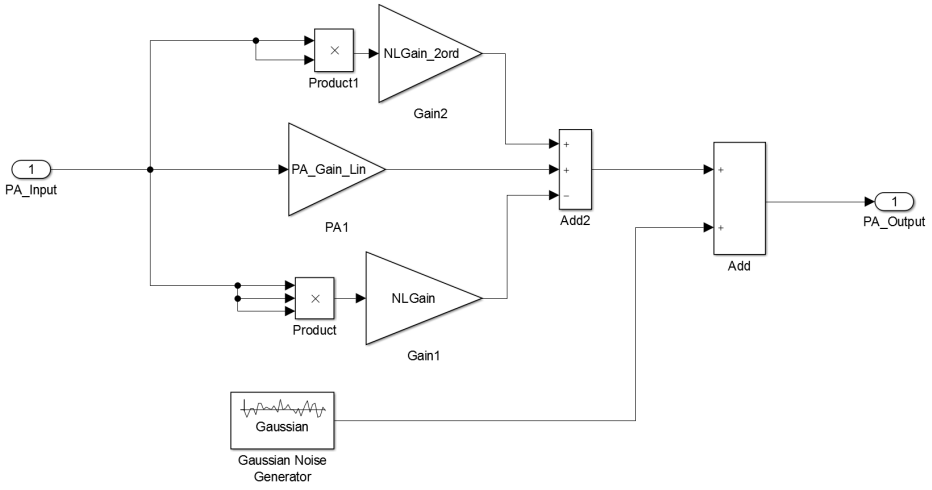


Figure 3.2: PA Model Block Diagram.

3.5 Channel

Due to the nonlinearity characteristics of the Multi-Port receivers we are also interested in verifying the performance of Multi-Port against blockers. Therefore, the model supports the addition of blockers that allows the verification of the system performance against adjacent channel interferer (*ACI*) and additive white Gaussian noise.

Adjacent Channel Interference - *ACI*: The *ACI* is added to the model by using an available replica of the transmitter which is operating in a different frequency: Power, frequency, modulation type and symbol are parameters that can be set. The blocker is added to the desired receiver at the channel.

AWGN: Noise is added to the receiver by setting the desired *SNR* value.

3.6 Multi-Port Receiver

Figure 3.3 represents a possible implementation of a Multi-Port receiver. This section presents a high level description of the design of each block of the Multi-Port receiver is built in Simulink and the possible imperfections that can be considered by the model.

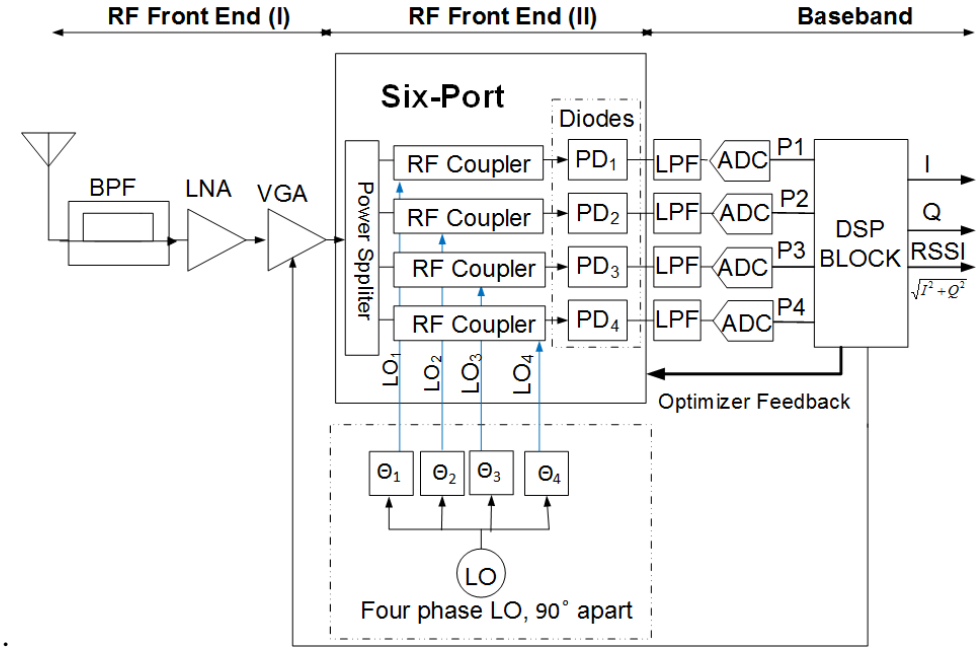


Figure 3.3: Possible Representation of Multi-Port Receiver.

3.6.1 Setting System Impairments

Similarly to the transmitter, at the receiver the following impairments can be added during simulation: Nonlinearities, noise figure and LO phase imperfections. These impairments are set in the Matlab script.

Nonlinearities and noise figure: Similar to the *PA*, second and third-order nonlinearities can be considered for the *LNA*. Noise figure also can be added to the *LNA*.

***LO* Phase Error:** As example, bellow we present how to set the LO phase error. k is the scaler error but it could be a random variable with a given distribution. $Alo = 1$; $Const1 = Alo * CoupFact$;

$ErrorDeg = k$; $error = ErrorDeg * \pi/180$;
$\Phi_0 = 0 - error$;
$\Phi_1 = \Phi_0 + \pi/2 + error$;
$\Phi_2 = \Phi_1 + \pi/2 - error$;
$\Phi_3 = \Phi_2 + \pi/2 + error$;

3.6.2 Multi-Port Receiver

A possible implementation of the Multi-Port receiver is shown in Fig. 3.3. This diagram is modeled using Simulink behavioral blocks. The Six-Port represented on this figure has the RF port, Lo plus four power detector ports. The representation of each internal block of the Six-Port receiver is described bellow:

Power Splitter Represented mathematically by a division

Couplers: Mathematically represented by a weighted sum of the *RF* and the *LO* signals. The weights represent insertion loss and coupling factor of the couplers

***LO*:** The local oscillator is represent by a sinusoidal block from Simulink and phases are added to each branch

Diodes: Represented by polynomials in the form of Eq. 3.2

$$V(t) = \sum_{n=0}^{L} a_n \left[V_{bias} + r_s(t) + K_{LO} V_{Lo}(t)\right]^n \tag{3.2}$$

Diode Characterization

The diode is used as power detector and in Multi-Port receivers it is the basis for the I and Q estimation that is the focus of this research. Therefore, it deserves a detailed description about how it is modeled in Simulink. The diode is a nonlinear device and it is characterized in *ADS*using its spice models from the manufacturers. After the characterization of I-V curve is complete, a polynomial fit was found using Matlab.

One example of polynomial fit is shown in Eq. 3.2.

$$\begin{aligned} P(x) = 2|(&0.5681x^{13} - 7.7066x^{12} + 46.2201x^{11} \\ &- 161.1933x^{10} + 361.7245x^{9} - 545.9367x^{8} \\ &+ 562.9422x^{7} - 395.3229x^{6} + 185.4621x^{5} \\ &- 56.0088x^{4} + 10.2275x^{3} - 1.0152x^{2} \\ &+ 0.0449x - 0.0006)|. \end{aligned} \tag{3.3}$$

where $x = V_d(t) + A_{LO}(t) + RF(t)$ This polynomial is than used in the Multi-Port receiver block of the Simulink model which is shown in Fig. 3.4.

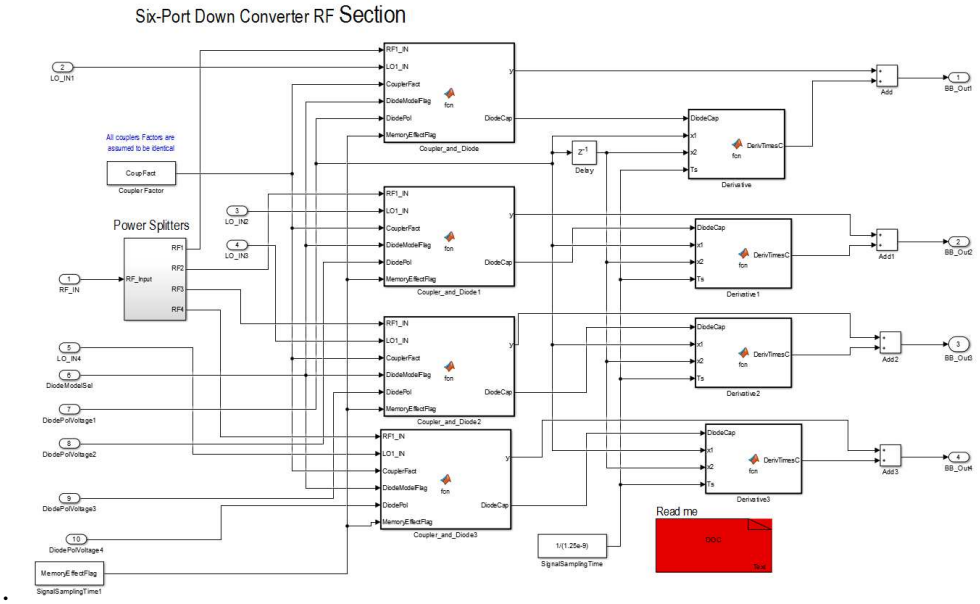


Figure 3.4: Implementation of Multi-Port in Simulink.

Table 3.2: Model Configuration Parameters

Setting	Block Affected	Description
Symbol Rate	*PRBS* Generator	Msps
Carrier Frequency	Tx and Rx *LO*	MHz
Modulation Type	Rectangular Mod	*QPSK*, 16, ... *MQAM*
Output Power	Power Amplifier	Watts
Free Space Loss	Channel	Watts
LNA Gain	*LNA*	dB
VGA Gain	*VGA*	dB
RRC Filter		
Roll Off factor (ROF)	*RRC* Filter	$0 \leq ROF \leq 1$
Ripple		dB
Stopband Attenuation		dB
Up-sampling Factor		*FUS* (*Integervalue* ≥ 2)
Diode Type	Multi-Port	Ideal Detector, BAS125, 1SS1663, HSMS2813, HSMS286 and WIN
Parametric Simulation	Multi-Port	
Diode Bias Variation		Diode bias voltage
LO Amplitude		Sweep *LO* power
LO Phase Error		Sweep *LO* phase
RF Input		Sweep input *RF* power
Optimizer and Memory Effects	Multi-Port	
Memory Effects		ON/OFF
Optimizer		ON/OFF

3.7 Conclusions

This chapter provides explanation about the Simulink model such as: Why we select Simulink as the basis for our tool. It also provides how the impairments were modeled, how to select and run the communication system using these impairments. It also provides information in how to run the model and collect information about the system performance.

Chapter 4

The Optimization of *EVM* through Diode Bias Control

4.1 Introduction

This chapter proposes an optimization analysis for the Six-Port receiver depicted by Fig. 2.4. The metric used for this analysis is the *EVM* or modulation imperfection. In a given communication system, *EVM* represents the combined imperfections of the down converter. These combined imperfections will cause an increase in bit error rate (*BER*). After presenting the most common contributions of *BER* degradation, we will focus our analysis on the effect of diode bias in *BER*. We propose an optimizer to dynamically locating the optimum diode bias voltage resulting in lower *BER*. In Section 4.3, we describe in detail the DC offset on the *I* and *Q* signals due to diode bias variation. A Simulink model was created and a comparison of the receiver *SNR* when the optimizer is operating and when it is off (only the automatic gain control (*AGC*) loop is running) is presented and results are shown. Since frequency conversion is required, the nonlinearities present in the diodes are the key characteristics for the Multi-Port receivers. Although the use of nonlinear devices may contradict requirements for high-order modulation (e.g. 64 *QAM*), Six-Port down-converters depend and would benefit from the concept of "controlled nonlinearities" (see Chapter 8) to achieve high *SNR* in the receiver. Results available in the literature have presented several Radio Frequency (*RF*) architectures suitable for the implementation of Six-Port down converters [14], [15], [17] - [20], [22], [25],[69] and [6]. Most of these published solutions require a high power *LO* (e.g., *LO* power $> -10dBm$)as shown in Table 4.2. These papers also

do not present the variation of the system performance with the *LO* power variation. In these papers, *LO* power requirements are necessary to switch the diodes between the conduction and the cut off regions. Instead, our proposed method always keeps the diodes in conduction by applying a controlled DC bias voltage. Therefore, the *LO* power requirement is alleviated.

4.2 Error Vector Magnitude Formulation

EVM is the metric used to measure the quality of the modulated signal (*I* and *Q*). It is a representation of the difference between the ideal constellation point and the estimated constellation point. Hence, it quantifies the overall signal "purity" by showing the sum of imperfections of a given transmitter or receiver. *EVM* is most commonly used to analyze the transmitted signal. *BER* is a more commonly used metric during receiver analysis and debugging. This method of analysis (i.e., *EVM* for the transmitter and *BER* for the receiver) is valid, but it is more appropriate in a real time system during debugging in the laboratory (during operation). Practical systems are required to have a raw *BER* on the order of 10^{-8} to 10^{-10}. Therefore, during the simulation phase, it would be impractical to measure *BER* of this order due to the amount of simulation time required[1]. To avoid this, it is common for system engineers to use *EVM* to optimize the systems during the design phase, unless the *BER* curves are essential.

The relationship between *SNR* and *BER* is well known and available in the literature for different types of digital modulation [70]. It is also possible to establish a mathematical relationship between *EVM* and *SNR*. Hence, it is possible to use *EVM* instead of *BER*. The interrelationship within these three metrics are interchangeable and one can write:

$$EVM \iff SNR \iff BER \tag{4.1}$$

It is shown in [71] that the relationship between *EVM* and *SNR* is:

$$SNR \approx \frac{1}{EVM^2}. \tag{4.2}$$

[1]Assume that the system has a symbol rate of 20Msps and 64QAM modulation. Therefore, the system runs 10^6 bits per second. Therefore, to simulate one bit error, we will need to perform 100 seconds of simulation. Let us assume that the system in question is small and for each mili-second of simulation time, it will take 10 seconds of workstation time. The total hours to simulate one error will be approximately 280 hours (more than 10 days)

In dB (4.2) is given as:

$$SNR \approx -20Log_{10}\left[\frac{1}{EVM(\%)}\right](dB). \tag{4.3}$$

Receivers usually have multiple sources of imperfections, i.e., phase noise, intermodulation distortion (*IMD3*), noise figure (*NF*), etc. Let us assume that the total imperfection of the system is the resultant of all these imperfections and let EVM_i be the error vector magnitude generated by a given imperfection (i). These imperfections are generated from each block of the Six-Port down converter (e.g., low noise amplifier (*LNA*), LO, etc). Once every imperfection is generated from each block, they can be assumed to be Gaussian random processes independently distributed. Hence, [62] shows that the total *EVM* is given by:

$$EVM^2_{Total} = \sum_{i=1}^{K} EVM^2_i. \tag{4.4}$$

For a Six-Port system such the one shown in Fig. 2.4, the imperfections can be enumerated as:

1. *ADC* jitter
2. Local oscillator phase noise (LO_{PN})
3. Local oscillator phase difference $(LO_{\Delta\phi})$
4. *LNA*'s *NF*
5. *LNA* IP3
6. *LO* amplitude variations
7. Group delay of the low pass filter (*LPF*) after each rectifier diode
8. Phase and amplitude variations in the hybrid couplers

The total *EVM* is a function of all these imperfections. Using (4.4) the total *EVM* can be written as:

$$\begin{aligned} EVM^2_{Total} = {} & EVM^2_{V_d} + EVM^2_{Jitter} + \\ & EVM^2_{LO_{PN}} + EVM^2_{LO_{\Delta\phi}} + \\ & EVM^2_{IMD_M} + \ldots \end{aligned} \tag{4.5}$$

where EVM_{V_d} is the diode contribution, EVM_{Jitter} is the contribution of the *ADC* clock jitter, $EVM_{LO_{PN}}$ the contribution of the *LO*'s phase noise, $EVM_{LO_{\Delta\phi}}$ is the contribution due to the phase differences of the *LO* and EVM_{IMD_M} is the contribution of the intermodulation. Our focus in this section is the analysis and simulation of the diode polarization effect on the received *SNR*.

4.3 *I* and *Q* Voltage Optimization

In the literature, Multi-Port down converters and legacy mixer designs, usually force the diodes to operate in switching mode by applying a large *LO* signal. The solution proposed in our research is to bias the diodes as depicted in Fig. 4.1. This figure shows that the *RF* signal and the *LO* signals have been added. This function is realized by the couplers in Fig. 2.1. This figure also shows an optimizer that has the purpose of adaptively finding the optimum *DC* operation bias point. The diodes will be continuously conducting independent of the *LO* and received signal strengths. Let $\vec{V_d}$ be the diodes DC voltage vector. These bias voltages ($\vec{V_d}$) are adjusted to their optimum values by the optimization algorithm and fed into the anode of the diode through an *RF* choke. The diode DC operation point or initial value for the optimizer is set by the value of the resistor *R*. The initial estimate for the diode bias point is covered in details in Chapter 5. The optimization algorithm will find the optimum operation point and will mitigate possible circuit sensitivity caused by the resistor tolerance.

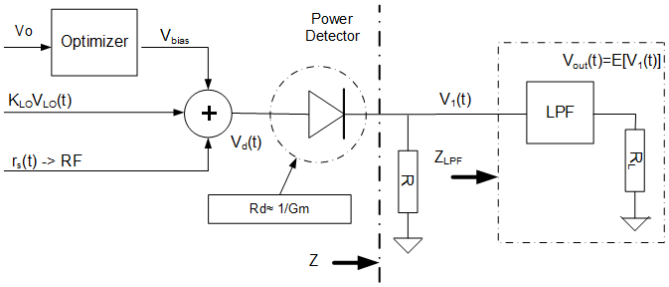


Figure 4.1: Diode bias circuit showing *DC* bias control, *LO* and *RF* Signals.

The advantages of this solution (bias the diode using an optimizer) compared with published literature is that the optimum diode bias point can be found in a real time manner. It is optimized for the best SNR and reduces power requirements. The *LO* power is lower when compared to published literature (see Table 4.2). The diode is

biased at the knee of the I-V curve as shown in Fig. 4.2, see Chapter 5 for detailed explanation.

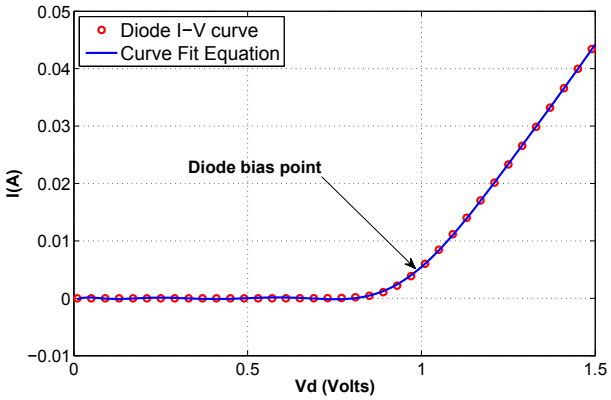


Figure 4.2: Actual diode I-V curve compared to curve fit equation.

The DC bias voltage of the diode is usually a constant voltage applied to it using the source V_d. The optimization process consists of finding the DC bias voltage for the diodes with the purpose of optimizing the error vector magnitude and completed in two steps. One condition for the optimum bias voltage to occur is when the I and Q DC components are zero the constellation plot is centered at the origin. Another condition is that the diode is operating outside a second-order fitting region. The optimum region of operation is discussed in detail in Chapter 5. Therefore, finding the optimum DC polarization point will require finding $min[EVM] = max[SNR] = f(\vec{Vd})$.

Let e_{Max} be the maximum DC offset voltage allowed to be present at either I or Q. Let $f_j(\vec{V_d})$ where j=1,2 be the DC offset voltage at I, Q resultant of the value of the diode bias voltage. In other words:

$$I_{DC} = f_1(\vec{V_d}) \tag{4.6}$$

$$Q_{DC} = f_2(\vec{V_d}) \tag{4.7}$$

The proposed system, containing the optimization algorithm is shown in Fig. 4.3. To prevent the *AGC* and diode bias optimization algorithm from working against each other, they co-exist using a time sharing scheme. The time sharing occurs before the optimization algorithm finds its optimum operation point. At power up, we let the *AGC* find its optimum point and thus the system holds the *AGC* control values and lets the optimization algorithm run until it either reaches the optimum point or it times

out. The *AGC* will be turned on again and the diode optimum bias voltage will be held constant.

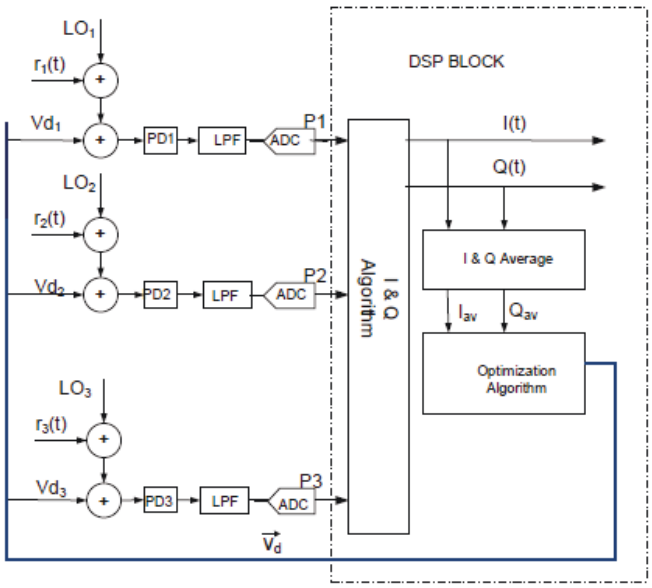


Figure 4.3: System including I and Q DC offset optimization.

Several diodes were tested(e.g., Winner PL15-10, HSMS286, BAS125, Hitachi1663, etc). We selected the Winner diode because the initial intent was to implement this design using an *MMIC* kit that includes this diode. The diode is modeled using a 0.15 um PHEMT GaAs diode model PL15-10 [72]. Firstly the diode's *I-V* curve was obtained using Advanced Design Systems (*ADS*) software [73]. The data was exported into Matlab and using a script. A curve fit polynomial of 13th order was found and is given by:

$$\begin{aligned} P(x) = 2|(&0.5681x^{13} - 7.7066x^{12} + 46.2201x^{11} \\ &- 161.1933x^{10} + 361.7245x^{9} - 545.9367x^{8} \\ &+ 562.9422x^{7} - 395.3229x^{6} + 185.4621x^{5} \\ &- 56.0088x^{4} + 10.2275x^{3} - 1.0152x^{2} \\ &+ 0.0449x - 0.0006)|. \end{aligned} \tag{4.8}$$

where $x = V_d(t) + A_{LO}(t) + RF(t)$. Therefore, the diode which is represented by $P(x)$ will be evaluated using x Volts.

This polynomial is used in the Simulink model to mimic the diode's behaviour (output current versus input voltage). Using this modeling approach we guarantee

that the diode's transfer function is very close to the real diode (see Fig. 4.2). The values obtained from *ADS* are depicted in red and the polynomial fit curve is depicted in blue. Therefore, the simulation results should adhere very well with a future design.

The values of I and Q signals are calculated by the *DSP* block shown in Fig. 2.4, using the expression: $[RSSI \;\; I \;\; Q]' = M^{-1}\vec{P}$. These I and Q signals pass through the slicer (decoder). The slicer has constant boundaries for each type of modulation that usually uses a maximum likelihood approach to decide which symbol it will associate for each I and Q pair (constellation point) within a finite set of symbols (i.e, for 16 *QAM*, there will be 16 possible symbols usually Grey Coded). For details see [70]. Once the slicer has fixed decision boundaries, the residual I and Q DC offset, if any, will drastically impact the *BER* result.

Ddiode DC Bias Sensitivity In Multi-Port down converters such as the one depicted by Fig. 2.4, the diode DC bias, if not optimized, will generate DC offset voltages at the I and Q signals. We conducted this simulation with the set up of table 4.1 using the following steps:

1. Diode characterization is done in *ADS*.
2. Polynomial fit is found using Matlab.
3. The diodes used in this simulation are identical.
4. Three diodes are sufficient to estimate the values of *RSSI* I and Q.
5. Using these results, the optimum Vbias operation point (i.e., 950 mV)was found based on SNR.
6. Next, two diodes are forced to operate at the optimum Vbias value, but a different Vbias is applied to the third diode.
7. The DC offset on the I and Q signals is measured.

Figs. 4.4, 4.5 and 4.6 show the impact of each diodes' bias voltage onto I and Q offset. These simulation results were obtained by applying parametric simulation at one of the diodes in the Six-Port receiver Simulink model. On the horizontal axis, one finds the DC voltage applied to the diode and on the vertical axis the I and Q DC offset voltage that results from the DC voltage differences applied to the diode. In the case of Fig. 4.4, Diode 2 and 3 were kept at 950 mV and we varied the voltage of diode

1 from 850 to 1050 mV. For this situation, the estimated DC voltage at the Q signal is approximately zero, but on the I signal it varies from -2 to 3 V. The DC offset voltage on diodes 2 and 3 are more sensitive than on diode 1. The numbers presented on this figure are the result of fixed point calculations. Therefore, they can be larger than the supply voltage. These figures provide us with three important characteristics of the system:

1. For identical diodes the DC offset differences seen on I and Q outputs are dependent upon the algorithm not the physical diodes.

2. The DC offset for the Q signal at diode 1 (P1) is insensitive to the diode DC bias voltage variation.

3. The DC offset for I and Q at diode 2 (P2) is equal and much more sensitive to voltage variation.

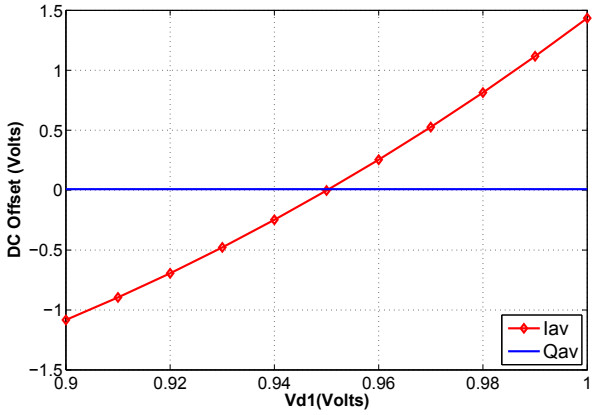


Figure 4.4: I and Q DC offset function of Vd_1 evaluated at $Vd_2 = Vd_3 = 950mV$.

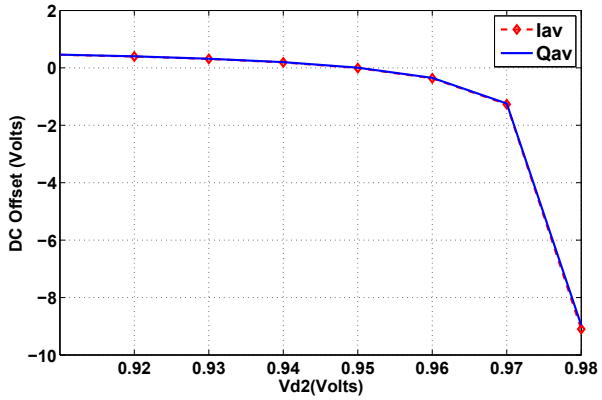


Figure 4.5: I and Q DC Offset Function of Vd_2 evaluated at $Vd_1 = Vd_3 = 950mV$.

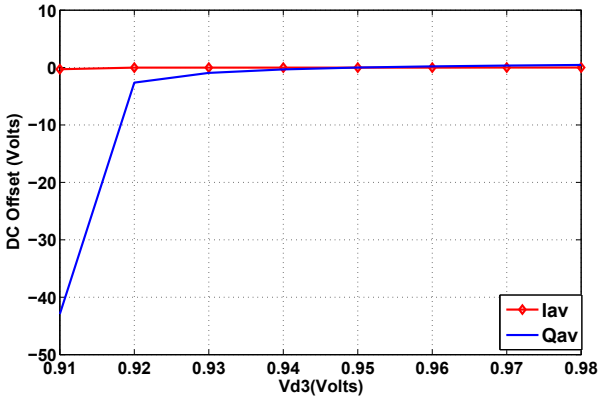


Figure 4.6: I and Q DC Offset Function of Vd_3 evaluated at $Vd_1 = Vd_2 = 950mV$.

4.4 Blind Search Algorithm

This section describes the algorithm used to find the optimum bias point of the diodes. This optimum point of operation is found when the DC component of I and Q is minimized (i.e., it is less than a pre-established error). Fig. 4.7 depicts the optimization algorithm's flowchart for the system presented in Fig. 4.3. After the values of I and Q are calculated by the Multi-Port algorithm described in Section 4.3, the mean of the I signal and the Q signal are calculated.

Description of Blind Search Algorithm: In this work, it is assumed that all diodes are identical, therefore, $V_{d1} = V_{d2} = V_{d3} = V_{d4}$. This simplification is valid because it is assumed that the diodes are fabricated on a common substrate. Let λ be the step size of the algorithm, $e(K)$ be the error at instant K and e_{max} be the positive error limit that determines when the algorithm has converged to an optimum point and stopped. The goal of the optimization algorithm is to find a vector ($\vec{V_d}(K+1)$) that will result in an error $\left|e\left(\vec{V_d}(K)\right)\right| < e_{max}$.
Since in general analytical expressions for $f_1(\vec{V_d})$ and $f_2(\vec{V_d})$ given in (4.6) and (4.7) are not known, therefore the blind search algorithm needs to first determine the direction in which the minimum lies. The blind search algorithm finds the direction of the minimum error empirically. The search for the minimum path is done by using the first iteration steps and it is graphically shown in Fig. 4.8. After finding the direction to the minimum, at every algorithm time step it will select the maximum of I_{av} and Q_{av} to calculate the error at that time step. It will use the magnitude and sign of the error to find the minimum as follows (starting with $K = 0$:

Step I - For the current time step K, the algorithm will use the value of the diode bias voltage $\vec{V}d(K)$ to calculate $I_{av}(K)$ and $Q_{av}(K)$. It will select the maximum value of $I_{av}(K)$ and $Q_{av}(K)$ to calculate $e(K)$.

$$e(K) = max\left[I_{av}(K), Q_{av}(K)\right] \tag{4.9}$$

Step II - The algorithm will randomly select a direction to calculate $\vec{V_d}(K)$ (e.g., $\vec{V_d}(K+1) = \vec{V_d}(K) + \lambda$), and repeat **Step I** for $K = 1$.

Step III - The algorithm will calculate the magnitude of the error. If, after the second step ($K = 1$), the magnitude of the error increased, the step was done in the wrong direction. The direction to the minimum is calculated as follows:

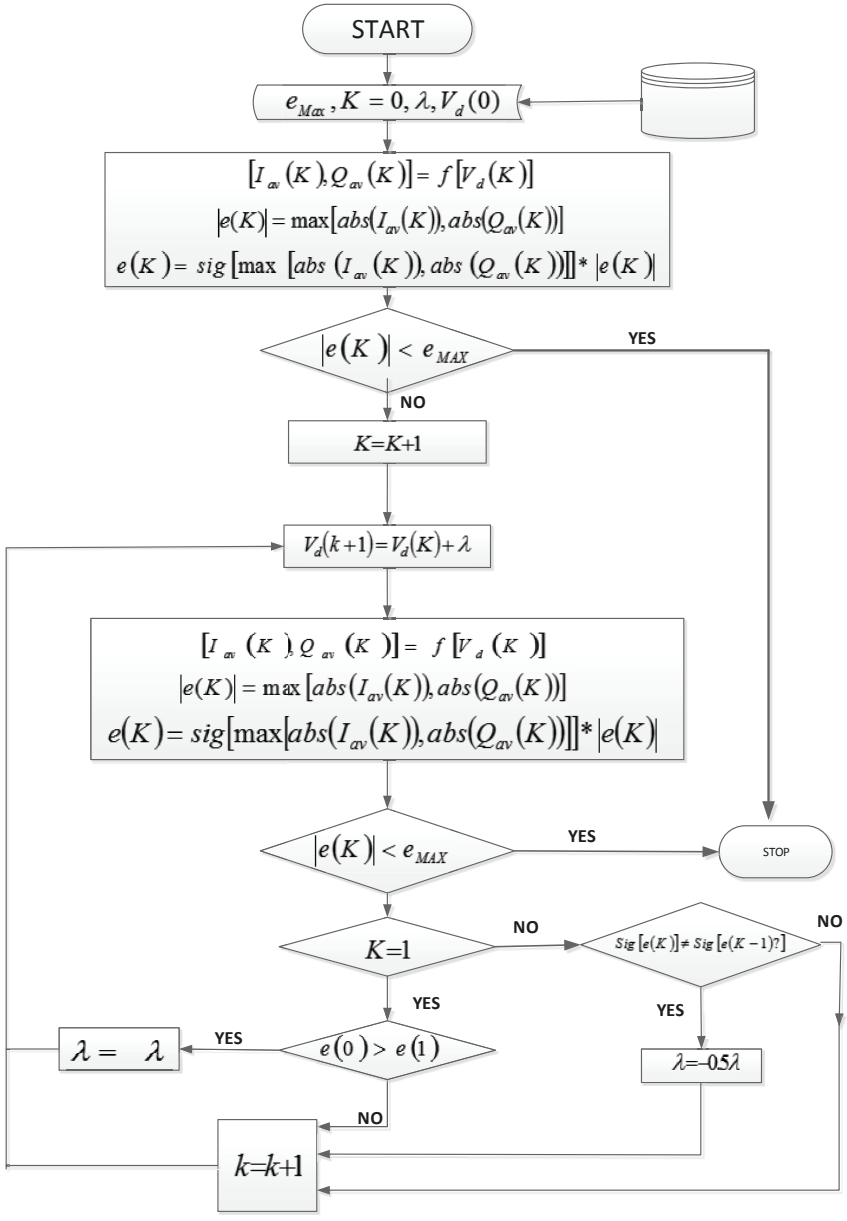


Figure 4.7: Blind Search Algorithm State Diagram.

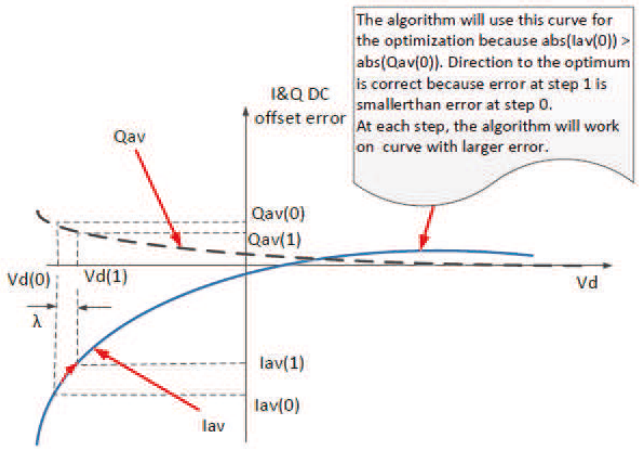


Figure 4.8: Illustration of finding the direction to the minimum.

$$max[|e(0)|,|e(1)|] = \begin{cases} |e(0)|, & \text{correct direction} \\ |e(1)|, & \text{wrong direction} \end{cases} \tag{4.10}$$

Case I: $max[|e(0)|,|e(1)|] = |e(1)|$ The error increased, which implies that the algorithm is not moving in the direction of the minimum. Therefore, requiring a change in direction by using the following Equation:

$$\vec{Vd}(K+1) = \vec{Vd}(K) - \lambda. \tag{4.11}$$

Case II: $max[|e(0)|,|e(1)|] = |e(0)|$ This means that the algorithm is moving in the correct direction moving towards to the minimum. Therefore, the search algorithm will need to keep using the iterative equation previously evaluated

$$\vec{Vd}(K+1) = \vec{Vd}(K) + \lambda. \tag{4.12}$$

Step IV - At this point, the algorithm will use either Eq. (4.11) or (4.12) to minimize the error. It will step the value of the diode bias voltage until the error is zero (very close to zero). There will be a step during the iterative algorithm search where the error changes sign (i.e., the error crosses zero). This is the indication that the minimum is located within the last two steps. Therefore, at every step the algorithm, will need to verify if the sign of the error has changed within two consecutive steps. In other words $sig[e(K)] \neq sig[e(K+1)]$ indicates that the algorithm crossed the optimum value. Therefore, when this happens the algorithm moves to step **V**.

Step V - To find a point closest to the minimum, it is required to compare the error at the instant $(K+1)$ and the value of e_{max}. If $|e(K+1)| < e_{max}$ the algorithm stops otherwise the algorithm will use half of the previous step size (e.g., $\lambda = \lambda/2$), calculate the value of $\vec{V}_d(K+1)$ using the new value of λ, calculate the error and repeat **Step IV**.

4.5 Simulation Results

This section presents the simulation results obtained using the Winner diode as follows: Optimizer ON, Optimizer OFF and Optimizer ON considering memory effects on the diodes only. The optimization algorithm is the same presented in Section 4.4. The simulation set up is described in Table 4.1. To generate these results, we run the Six-Port system designed in Simulink [74]. Fig. 4.9 presents the *SNR* at the receiver system when the optimization algorithm is on and when the algorithm is off. During simulation, we used parameters listed in table 4.1. In both cases the system kept the same settings. Notice that when the algorithm is in operation, the output *SNR* is not as sensitive to the initial diode voltage variation.

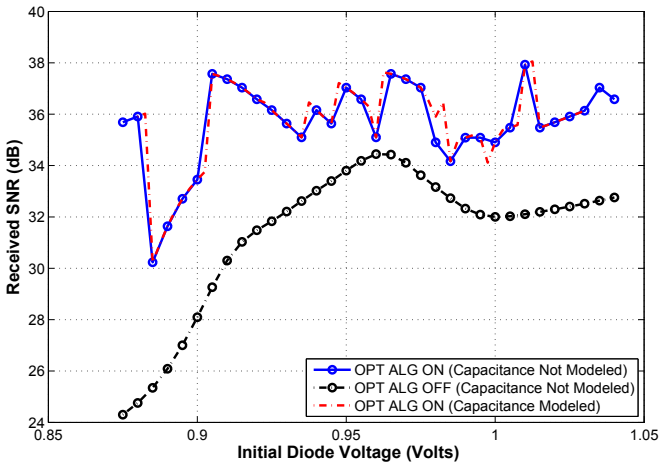


Figure 4.9: SNR with optimization algorithm and without.

Fig. 4.9 shows that for any diode bias voltage value between 850 mV and 1.05 V when we use the optimizer, the resultant *SNR* will be better than when we leave only the *AGC* loop operating. The variation of the optimized *SNR* curve (in blue) is due to the *AGC* loop. When the initial diode voltage is far from the optimal voltage a large improvement in *SNR* is observed. The impact of the EVM with respect to

the selection of the the initial voltage of the optimizer is presented in chapter 5. It is noticeable that when the initial value of the diode bias voltage happens to be close to the optimal value, the algorithm has much less impact on the performance because it does not get trapped into local minimum. This figure also shows simulation results when non linear capacitance (memory) is added to the diode model. Notice there is no degradation in *SNR* when memory is considered in the diode model. In a similar manner, Fig. 4.10 shows this difference in *SNR* presented by the constellation. This figure was obtained with the diode voltage equal to 850 mV. Notice that when the algorithm is turned ON (Blue: average EVM = 1.6%), the constellation points are noiseless when compared with the case when the algorithm is OFF (Red: average EVM = 6.3%). These results are in agree with Fig. 4.9.

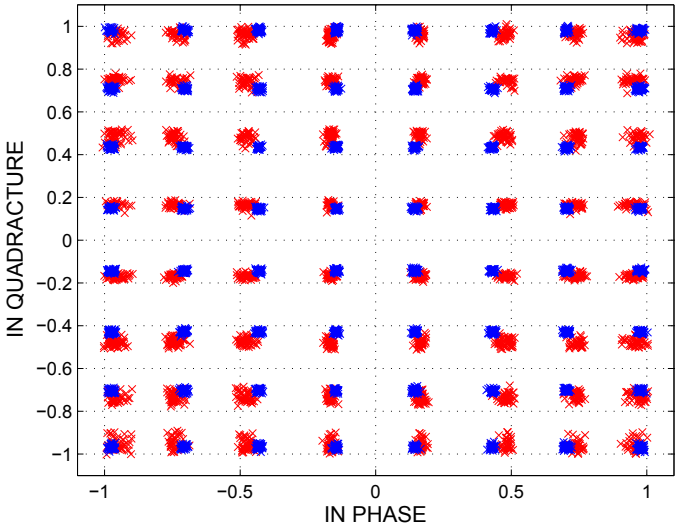


Figure 4.10: Constellation when algorithm is OFF and when it is ON .

***LO* and *RF* Power Sensitivity:** Simulations were performed to verify the sensitivity of the received *SNR* with respect to *LO* and *RF* power variation. This invariance of *SNR* with respect to *LO* power variation confirms our previous statement that in Six-Port applications the *LO* power can be very low and that the *SNR* is insensitive to the variation of this power (See table 4.2). This is due to the diode bias. In practical applications the *LO* output power is expected to have less than 6 dB variation with process, voltage and temperature (*PVT*). A simulation was carried out that shows that SNR is insensitive to LO power variation over the range of -10 to -30dBm. This is a good indication that in Multi-Port applications, the only important design parameter

for the *LO* is the phase matching. These advantages translate into a simpler and less expensive oscillator for this solution. The variation of *RF* power can be approximately 40 dB and is limited by the *AGC* range of the receiver. The *AGC* is equally divided into two loops; one for the *RF* section and one in the digital *BB*.

Table 4.1: Simulation Conditions

Item	Value	Comments
Carrier Feed Through	None	Not considered
I and *Q* Imbalance	None	Not Considered
Nonlinearities	*PA* and *LNA*	*P1dB*, *IIP2* and *IIP3*
AWGN	46 dB	See footnote [2]
LNA Noise Figure	None	Noise figure in dB
ACI	Adjacent channel	No interferer considered
Symbol Rate	20 Msps	Msps
Carrier Frequency	700 MHz	Tx = Rx *LO* MHz
Modulation Type	64 QAM	
LNA Gain	10 dB	dB
VGA Gain	*VGA*	Controlled by AGC
RRC Filter	Yes	
Roll Off Factor	0.5	$0 \leq ROF \leq 1$
Up-sampling Factor	8	*FUS* (*Integervalue* ≥ 2)
Diode Type	WIN	From Win Corp
Parametric Simulation	Yes	Diode bias voltage
LO power	-10 dBm	Fix value
LO Phase Error	0	Not applied
RF Input	-40 dBm	
Optimizer and Memory Effects	Multi-Port	
Memory Effects	ON/OFF	Simulated for both conditions
Optimizer	ON/OFF	Simulated for both conditions

Table 4.2: LO Power Comparison

Reference	*LO* Power	RF Power
[48]	0 dBm	-45 to -5 dBm
[15]	-10 dBm	-50 and -45 dBm
[20]	0 to 8 dBm	-6 4dBm
[75]	$\geq$ 0 dBm	-40 dBm
[69]	-8.45 dBm	unknown
[6]	-10 dBm	-37 to -10 dBm
[18]	-20 dBm	-36 dBm
This work	-20 to -12 dBm	-20 to 0 dBm

4.6 Conclusion

This chapter shows that by adding a constant DC voltage at the anode of the diode, the *LO* power can be significantly reduced when compared with existing Six-Port systems. It also introduces an optimizer that has a twofold purpose: firstly it will provide an *SNR* gain when compared with the same receiver's model turning OFF the optimizer and secondly it will reduce the sensitivity of the *SNR* with respect to diode bias voltage variation. This improvement alleviates the need of a precise DC voltage present at the anode of the diode.

Chapter 5

Finding the Initial Estimate for the Diode Bias Point

5.1 Introduction

This chapter, will present a novel methodology for estimating the initial diode bias voltage in Multi-Port receivers. We tested the methodology with four different Schottky diodes from different vendors (Win Corp, HP, Hitachi and Siemens) although the process can be applied to any diode. The analysis shows that setting the initial value for the optimizer where the diode's output DC voltage to input power sensitivity is highest will yield the fastest convergence time for the *EVM* optimizer algorithm. This point is located at the inflection point of the first derivative of the I-V curve fitting polynomial which was obtained in Matlab and assures that the optimizer will not be trapped into local minima. To verify the results of this research, we used a Simulink model that emulates the radio frequency (*RF*) and digital baseband parts of a Six-Port receiver. It was found that by reducing the voltage difference between the estimated initial value and the optimum point, the optimizer needed less steps to reach the optimum value of the bias voltage. This work also provides the behavior of the variation of the initial estimates of the diode voltage with the polynomial degree. Hence, the necessary degree for the fitting the polynomial can be determined based on the initial point variation analysis.

Many published works exit with regard to Multi-Port receivers [15] - [18] but fewer [48], [49] and [50] introduced the idea of biassing the diodes. In Chapter 4, the idea of finding the optimum bias point by using an adaptive blind algorithm was introduced.

This section presents a design methodology to find the estimates of the initial point for the algorithm to find the system's optimum bias point. The estimation of a proper initial point is a novel design process which assures that the algorithm will find a global optimum point during its convergence process. This section also presents the mathematical analysis that supports this novel idea. By using this process (section 5.5.1), the speed of convergence of the algorithm will be increased and it will also assure that the algorithm will not be trapped at a local minimum. With the lack of an optimization algorithm, the initial value estimates may be used as its operation point. This paper also presents a method to select the best fitting algorithm based on the variation of the section derivative maximum point.

Section 5.2 presents the effects in Multi-Port receiver caused by high-order intermodulation products (*IMD3*) in the *EVM* after applying the transformation matrix $\left(M^{-1}\right)$. Section 5.3 presents the mathematical derivation of the diode operating as a power detector. Section 5.5 presents a novel method to find the initial estimates of the optimum bias point. This section also presents simulation results that compare different polynomial fitting for different diodes. It shows that once the transformation matrix **M** is derived from a second-order polynomial, a higher order operation region can generate undesired products and increase the *EVM*. In section 5.7, we present the conclusion of this section.

5.2 Representation of Power Measurements and Transformation Matrix.

As an example, let us take a constellation point on the complex plane as shown in Fig. 5.1. If we apply the transformation matrix to this point, it will result in three powers (P_1, P_2, P_3). Fig. 5.1 shows that by applying this linear transformation, the resulting powers will be 90° apart from each other. In reality, what happens with the system (Multi-Port receiver) is the inverse of the transformation (that is why it is required to calculate the inverse of M). Fig. 5.2 depicts three power measurements and the transformation result after applying the inverse of the matrix M onto these measurements (i.e., this is the reverse of what we show in Fig. 5.1). These three powers are shown in a complex plane and for simplicity, we used 16QAM modulation. V_{bias} is located on the positive real axis ($V_{bias} \approx 950mV$ for *WIN* (*GaAs*) diode, see table 5.2). The three oscillator voltages are considered to have with respect to V_{bias} 90°, 180° and

$-270°$ of phase shift. The green vectors are the sum of V_{bias} and V_{LO}. The received signal $r(t)$ is added on top of the green resultant vector. This will generate three simultaneous constellations, each one with the phase difference imposed by the local oscillator phases. After applying the transformation matrix M^{-1} onto these three powers, we obtain the I and Q signal constellation points shown at the top of Fig. 5.2.

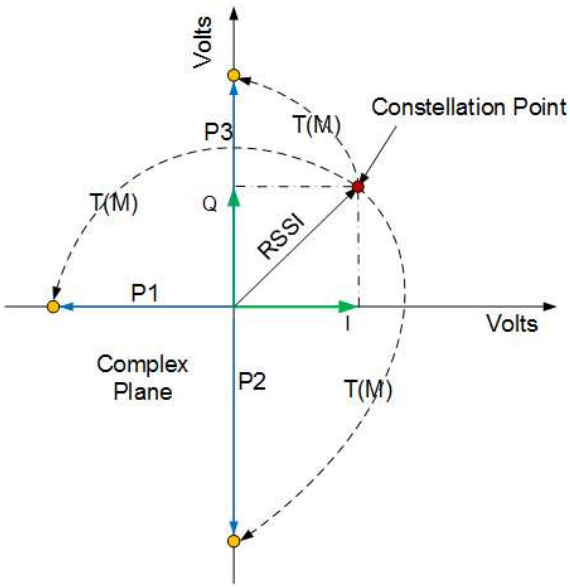


Figure 5.1: Transformation Matrix M in the Complex Plane.

5.3 Diode as a Power Detector

This section provides a detailed mathematical analysis of the diode as a power detector. The assumptions in this section are made in such a way that we can analyze the increase of the *EVM* due exclusively to the operation on the **I-V** curve of the diode but nothing else. These assumptions are valid because the imperfections in the receiver are independent random processes. Therefore, we will not consider all other imperfections, but only the one of interest of this research. Fig. 4.1 shows in detail the Schottky diode circuit operating as a power detector. Let us consider V_{bias} as an optimized diode voltage and represent the power detector as shown in Fig. 4.1. Let the LO voltage be: $V_{LO} = A_{LO}\cos\left(\omega_{LO}t + \phi_{LOi}\right)$ where $i = [1, 2, 3]$. V_0 is the estimated initial voltage point, V_{bias} is the optimum diode bias voltage that can be found by using the optimizer. Let K_{LO} be a scalar less than one that represents the local coupling

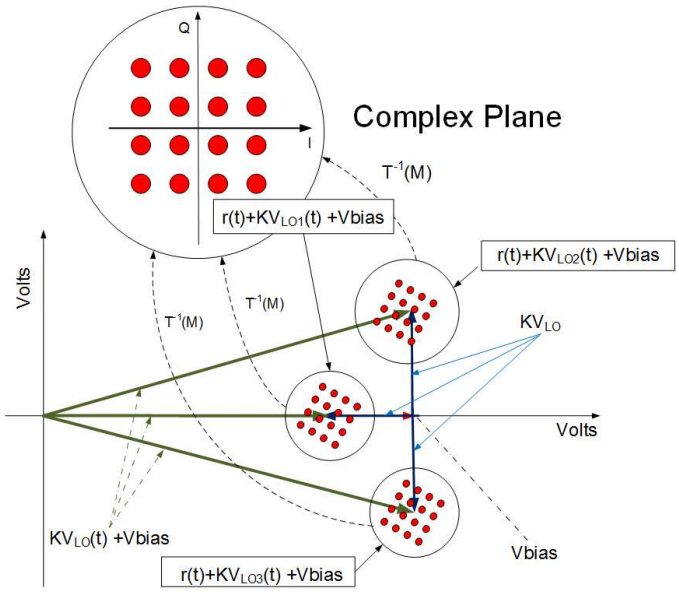


Figure 5.2: Effects of the Transformation Matrix into the three power measurements.

factor. Assuming the three couplers are equal, this means that the couplers will not present any phase differences. Hence, we can conclude that $K_{LO}V_{LO}(t)$ is the portion of the *LO* voltage coupled into the diode. Let $r_s(t)$ be the received signal, $\omega_{RF}(t)$ be the carrier frequency and ϕ_{RF} be its phase. $\phi_{RF}(t)$ is assumed to be a random process with a uniform distribution $[0, 2\pi]$.
Let Z_i be the impedance seen at each diode output and for simplicity let us assume that $Z_1 = Z_2 = Z_3 = Z$, Z_{LPF} is the impedance at the input of the low pass filter, and ω is the angular frequency. From Fig.4.1 the design of R and Z are done such that:

- When $\omega \approx 0 \Rightarrow Z \sim Z_1 \Rightarrow R \ll Z_1$.
- When $\omega \approx \text{inf} \Rightarrow Z \sim R \Rightarrow Z_1 \ll R$

The above condition at $\omega \sim 0$ shows that the low frequency power content of the signal is passing through the low pass filter instead of R. This happens because the *LPF* presents a lower impedance path to the signal compared with the resistance R. The high frequency content will only pass through the resistor because the filter will present a higher impedance. Let V_d be the voltage across the diode, R_s the series resistance and I the diode current and I_o the reverse saturation current. From [82], the diode I-V curve is approximated by:

$$I = I_o e^{\left[\frac{q}{\eta KT}(V - R_s I)\right]}. \tag{5.1}$$

By taking the first derivative (dI/dV) we find:

$$\frac{dI}{dV} = \frac{qI}{\eta KT\,(1 + IqR_s)} \approx \begin{cases} 0, & \text{for } I \to 0 \\ \frac{1}{\eta KTR_s} & \text{for } I \gg \frac{1}{\eta KTR_s} \end{cases} \tag{5.2}$$

Notice that the analysis of the limits of the first derivative when I is a small value and when it is a large value are in agreement with the first derivative curve shown in Fig 5.4. In Chapter 6 we show that memory effects do not affect the performance of the system. Therefore, we assume that the diode is memoryless and noiseless, and a_n is a scalar of index **n**. Where $n = 1, 2, 3 \ldots L$. $V_d(t)$ is the voltage across the diode. Therefore, from Eq. (5.1) the current can be represented by a power series polynomial $p(V_d(t))$ of degree **L** given bellow:

$$p(V_d(t)) = \frac{\sum_{n=0}^{L} a_n V_d^n(t)}{Z} = i_d(t) \tag{5.3}$$

where $p(.)$ is a polynomial representation of the diode's I-V curve. A method to obtain the diode polynomial curve fitting is described in detail in Section 5.5. Thus the instantaneous current $i_d(t)$ is given by evaluating the diode's voltage on the polynomial. R and R_L are designed such that the diode is properly biased. Notice that V_{bias} is adaptively controlled by the optimization algorithm. Let Z_i be the impedance seen at each diode output and for simplicity let us assume that $Z_1 = Z_2 = Z_3 = Z$. The signal at the input of the PD is given as:

$$V_d(t) = V_{bias} + r_s(t) + K_{LO} V_{Lo}(t) \tag{5.4}$$

Looking at Fig. 4.1, as in [31], the output signal of the *PD* is given as:

$$V_1(t) = \sum_{n=0}^{L} a_n \left[V_{bias} + r_s(t) + K_{LO} V_{Lo}(t)\right]^n \tag{5.5}$$

Let $\mu_x = E[.]$ be the estimation of the mean of the signal at the output of the low-pass filter. Therefore, after the low pass filter the signal can be calculated as:

$$E\left[V_1(t)\right] = \frac{1}{T} \int_T \left[\sum_{n=0}^{L} a_n \times \left[V_{bias} + r_s(t) + K V_{Lo}(t)\right]^n\right] dt \tag{5.6}$$

5.4 Bounds Analysis for the Optimum Second-Order Region of Operation

In a receiver front-end, *EVM* can be caused by many different imperfections (e.g., *PN*, *IMD*, *I* and *Q* DC offset, *NF*, etc.). This section will show the analysis of the *EVM* contribution due to power measurement errors in a Six-Port receiver.
From Eq.2.1 we can write the values of *I* and *Q* as:

$$\hat{I} = [m_{21}\ m_{22}\ m_{23}]\,\vec{P} = \vec{m_2} \times \vec{P} \tag{5.7}$$

$$\hat{Q} = [m_{31}\ m_{32}\ m_{33}]\,\vec{P} = \vec{m_3} \times \vec{P} \tag{5.8}$$

To estimate the *EVM* and assuming that $\vec{m}_2$ and $\vec{m}_3$ are constant over time at the same bandwidth. Therefore, the *EVM* is due to the input signal imperfection power which is consequently related to the power measurements. We will adopt a power error to represent the *EVM*. Let P_{ideal} be the ideal power value that the receiver should have received to output an ideal constellation.

$$\vec{P} = \vec{P}_{ideal} + \vec{P}_{error} \tag{5.9}$$

$$\vec{I}^2_{error} = \left(\vec{m_2}\vec{P}_{error}\right)^2 \tag{5.10}$$

$$\vec{Q}^2_{error} = \left(\vec{m_3}\vec{P}_{error}\right)^2 \tag{5.11}$$

$$\vec{I}^2_{error} + \vec{Q}^2_{error} = \left(\vec{m_2^2} + \vec{m_3^2}\right)\vec{P}^2_{error} = EVM^2 \tag{5.12}$$

The matrix **M** is constant for a given operational bandwidth. Therefore, if we want to minimize the *EVM*, P_{error} will have to be minimized. From the result presented in the appendix, $EVM^2 = Imp^2$.

The system may operate out of the second degree region due to two reasons:

1. The DC (V_{bias}) is out of the second-order region
2. A strong input signal at the diode will force it to operate beyond the second-order region. Therefore, forcing the diode to produce more intermodulation products.

We will now continue with the analysis of the maximum ($|V_{ac}| = V_d - V_{bias}$) voltage that keeps the diode operating under the best second-order polynomial region. This analysis will provide an estimated maximum AC (*RF* input signal) voltage to be added

to the diode bias voltage (V_{bias}) to minimize the *EVM* degradation. The analysis for the imperfections when considering second and third-order polynomial curve fitting is presented in section A and already considered in this document. For a second and third-order polynomial PD's approximation the output voltage of the diode is given respectively:

$$V_0(t) = K_5 + \frac{1}{T}\int_T V_{LO}(t) r_s(t) dt \tag{5.13}$$

$$V_0(t) = K_5 + \frac{1}{T}\int_T V_{LO}(t) r_s(t) dt + Imp \tag{5.14}$$

Where the imperfections (*Imp*) are given as:

$$\begin{aligned} Imp &= DC_{I1} + \frac{2a_3 V_{bias} K_{LO}}{T}\int_T V_{LO}(t) r_s(t) dt + \\ &+ \frac{2V_{bias} K_{LO} a_3}{T}\int_T r_s(t) V_{LO}(t) dt + \\ &+ DC_{I3} + \frac{2a_3 V_{bias} K_{LO}}{T}\int_T V_{LO}(t) r_s(t) dt \end{aligned}$$

Assuming that the imperfections will add (worst case) and DC_x is the sum of the *DC* components. The total imperfection component will be given as:

$$Imp = \frac{6a_3 V_{bias} K_{LO}}{T}\int_T V_{LO}(t) r_s(t) dt \tag{5.15}$$

Solving Eq 5.6 for the circuit and finding the voltage at the output of the *LPF* for a second-order polynomial we find:

$$V_{out}(t) = E\left[V_{out}(t)\right] = DC + \frac{1}{T}\int_T V_{LO}(t) r_s(t) dt \tag{5.16}$$

Similarly, for a third-order polynomial we find:

$$V_{out}(t) = DC + \frac{1}{T}\int_T V_{LO}(t) r_s(t) dt + \sum_{n=1}^{N} I_{imp} \tag{5.17}$$

[31] shows that the imperfections are only due to *IMD3* products. This occurs when considering up to a third-order polynomials at the proximity of V_{bias}. In the next section, we present a method to estimate the initial value for V_{bias} that will provide the optimizer with a good avenue to minimize the *IMD3* by finding an optimum operating

point. To minimize the *EVM* the ratio of the second and third-order intermodulation products must be very small. Therefore,

$$\left|\frac{a_2}{3a_3V_{bias}}\right| \sim \infty \tag{5.18}$$

or

$$\frac{3a_3V_{bias}}{a_2} \sim 0 \tag{5.19}$$

Let Err be the maximum *EVM* error that a certain modulation will require to operate. Therefore,

$$\left|\frac{a_3}{a_2}\right| \leq \frac{Err}{3V_{bias}} \tag{5.20}$$

Observe that there is a difference between Eq 5.20 in this section and the Eq 30 presented in [31]. In this solution presented here, the diode is biased which is not the case in [31]. Therefore, it is expected there will be differences between these equations.

5.5 Estimating the Initial Diode Bias Voltage Point

This section describes a method for finding the initial conditions (initial voltage) to be used by the optimization algorithm shown in Fig. 4.1. This point will assure it will reach the global minimum *EVM* with fewer iterations and without being trapped into any possible local minimum. In Section 5.4 we found the mathematical expressions which clearly shows the expected region for the optimum bias point. It is noticed that when using a second-order polynomial, the expected value of V_d is $E[V_d(t)]$ and it has a *DC* component plus the desired signal only. But when a third or greater order polynomial is used, the resultant of $E[V_d(t)]$ is composed of the sum of the desired signal plus other signals resultant from *IMD* products. Therefore, when the transformation (M^{-1} shown in Fig.5.2) is applied, the output constellation will suffer different rotations for each component and, consequently, imperfections in the symbols will occur. This happens because the optimum power vector points changed their positions due to the intermodulation product residues shown in Eq. (5.17).

5.5.1 Initial Value Estimation Process

This section provides design guidelines for the designer to be able to select a good initial point for the optimization algorithm. This process is straight forward and

also prevents getting trapped on a local minima. The optimizer will reach the global minima in fewer steps than if it was performing the optimization blindly. In Section 4.4, we proposed an algorithm for the Multi-Port receiver system which finds the optimum operation bias point for the diode. That algorithm will optimize the value of the diode bias voltage by measuring the *EVM* of the receiving signal and forcing it to its minimum value. The problem with most of the optimization algorithms (e.g., Quasi Newton, Gradient Minimax, Least Pth, etc.) is to provide an initial value estimate for the optimum searching point. The initial point is crucial because if not selected properly, the optimization exercise will start in a region where the optimizer may get trapped in a local minimum. To the best of the author's knowledge this is the first proposed methodology to estimate the initial bias voltage value for the search of the optimum diode bias point in Multi-Port receivers. However, there is existing literature [76] that provides an estimate for the initial point for calibration purposes of Multi-Port down converters.
The steps below provide an easy way to find the estimates for the initial value of the diode's voltage bias. These steps are useful for a designer to follow during the design of a Multi-Port receiver that uses optimized bias control.

1. **Find the diode's I-V curve:** This can be done by using a simulator such as *ADS*, Spice, SpectreRf, etc.

2. **Find the curve fit polynomial:** Use a mathematical package of your preference and the I-V data from the circuit simulator to find the polynomial fitting curve. This can also be done numerically.

3. **Find first derivative:** Calculate the polynomial's first derivative.

4. **Find the bounds of the linear region**: Plot the first derivative and find its linear region bounds.

5. **Find the initial point** The initial point is located at the maximum of the second derivative.

We propose in this paper that the initial point can be found by analyzing the second derivative of the fitting polynomial of the diode in question. It has been noticed that the optimum point is located near the point where the ratio of second and third derivative is highest. This will maximize the ratio of desired to undesired components in the output spectrum. We found that the optimal point, even with a real diode is located

near this point. Fig. 5.3 shows the second derivative (green), the third derivative (blue), the ratio of these derivatives (red) and the *SNR* results for the complete system in black. Where the ratio of the second derivative to the third derivative is high, the system behaves more like an ideal second-order system and the *EVM* performance is relatively good. The real diode's behavior is more complex due to the presence of higher-order nonlinearity in addition to third-order, however, by simply evaluating the second derivative (which aligns with the ratio of the second and third derivative) places the initial point almost at the middle of the two optimal bias points for good *SNR* and *EVM* performance.

5.6 Simulation Results

To be able to prove this approach, we followed the steps 1 through 5 described in 5.5.1 for four different diodes types. These diodes operate at different bias points and each linear region of the second derivative is located at different voltage ranges. The initial point and the voltage difference from the initial point to the optimum point is shown in Table 5.2. Fig. 5.4 shows the WIN [77] GaAs process' diode curve fitting (solid blue line), its fitting polynomial first and second derivative (solid and dashed black lines). This curve fitting was obtained using Matlab and the polynomial approximation is using a degree of 13 as shown in Eq. 6.2. During the process, the designer should not care about the polynomial degree but the error between the polynomial fitting and the original data. Do not expect to find a low degree polynomial because it will not effectively represent the real characteristics of the diode. Table 5.2 shows the value of the initial estimate for the bias point and the actual optimum value for the diode bias. Fig. 5.5 presents the comparison between their first and second derivatives (second derivative curves are normalized). Observe that it is clear that the inflection point on the second derivative provides a good estimate for the initial value to be used by the optimization algorithm. Fig. 5.6 was obtained by doing parametric sweeping on the *Vbias* using the Simulink model. The simulation parameter are listed in table 5.1.

The diode bias voltages were swept from 100 mV to 1.1 Volts in steps of 10 mV. The solid lines represent the behaviour of the system (*SNR*) for all four diodes. The dashed lines represent their normalized second derivatives. Notice that for these diodes the maximum point of the second derivative is located at the valley of the optimum points which is a good estimative for the initial value of the bias voltage to be provided to the optimizer.

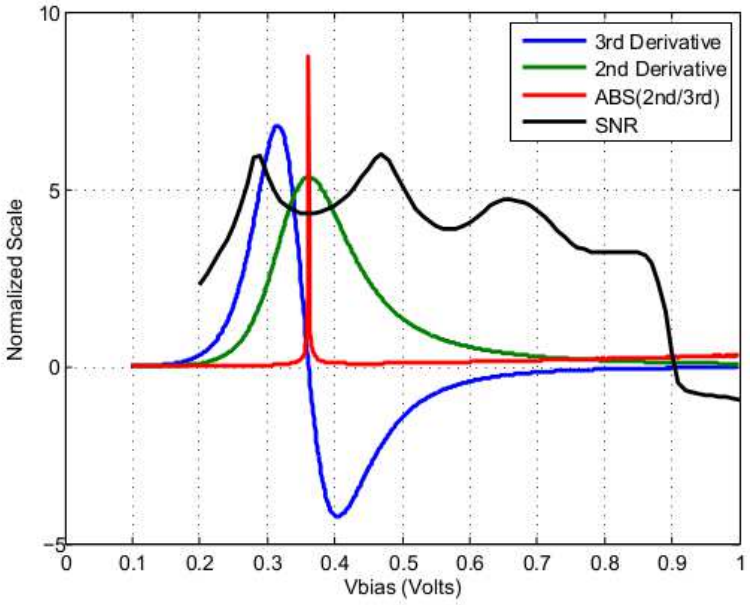


Figure 5.3: HSMS2813 second, third, ration between derivatives, and system *SNR*.

5.6.1 Determining the Polynomial Degree

One method to choose a good polynomial approximation is by analyzing the behaviour of the position of the second derivative's maximum point with respect to the polynomial degree. Fig. 5.7 shows the behaviour (variation) of the initial estimates with respect to the polynomial degree. This figure shows their variance for polynomials degrees from 3 to 10. As expected, with the increase of the polynomial, the approximation error between the results obtained in *ADS* (Fig 5.4) in cross-red and in blue the polynomial approximation will decrease. Therefore, instead of establishing a fitting error to select the polynomial, we will use the variance of the second derivative maximum value point. It is expected that the diode's I-V curve will change over temperature. The estimation of the initial point is done for ambient temperature only. This point is then provided to the optimizer which will search for the optimum bias point. In the case of temperature variation, the **I-V** curve will change but it is also true that the optimizer will adaptively follow diode changes due to temperature variation. Consequently, it will find a new optimum operation point.

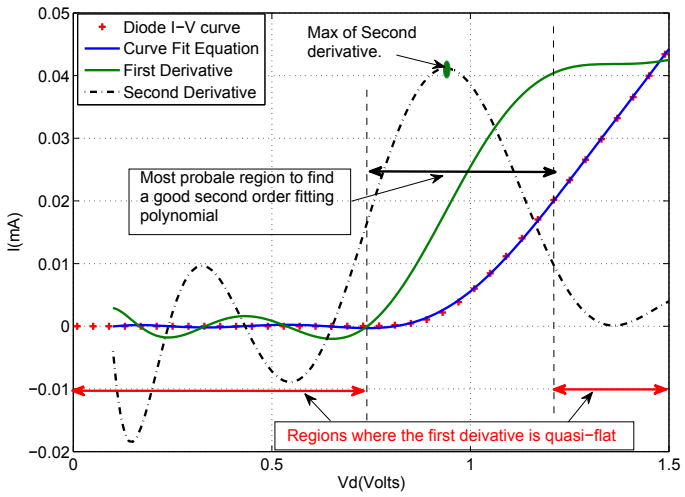


Figure 5.4: WIN GaAs Diode's Curve Fitting First and Second Derivative

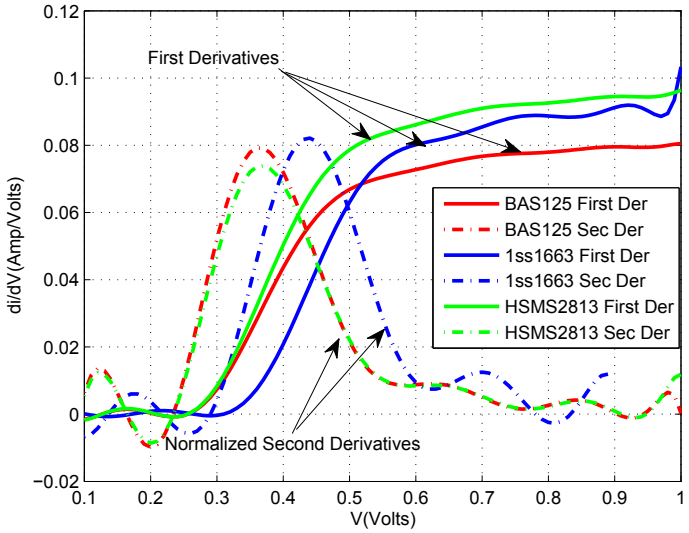


Figure 5.5: BAS125, 1ss1663 and HSMS2813 First and Second Derivatives.

Table 5.1: Simulation Conditions

Item	Value	Comments
Carrier Feed Through	None	Not considered
I and *Q* Imbalance	None	Not Considered
Nonlinearities	None	*PA* and *LNA*
AWGN	46 dB	
LNA Noise Figure	None	Noise figure in dB
ACI	Adjacent channel	No interferer considered
Symbol Rate	20 Msps	Msps
Carrier Frequency	700 MHz	Tx = Rx *LO* MHz
Modulation Type	64 QAM	
LNA Gain	10 dB	dB
VGA Gain	*VGA*	Controlled by AGC
RRC Filter	Yes	
Roll Off Factor (ROF)	0.25	$0 \leq ROF \leq 1$
Up-sampling Factor	8	*FUS* (*Integervalue* ≥ 2)
Diode Type	WIN, BAS125	From Win Corp
	Hitachi1663, HSMS2813	
Parametric Simulation	Yes	Diode Bias Voltage
LO Power	-10 dBm	Fix value
LO Phase Error	0	Not applied
RF Input	-40 dBm	
Optimizer and Memory Effects	Multi-Port	
Memory Effects	OFF	
Optimizer	OFF	

Table 5.2: Diode Bias Point Comparison

Diodes	Initial point	Opt Voltage (mV)	ΔV	Manufacturer
1SS1663	440 mV	360 and 530	80 mV	HITACHI
WIN	940 mV	960 and 1100	20 mV	WIN Semi
BAS125	370 mV	280 and 470	100 mV	Siemens
HSM2813	360 mV	290 and 470	110 mV	HP

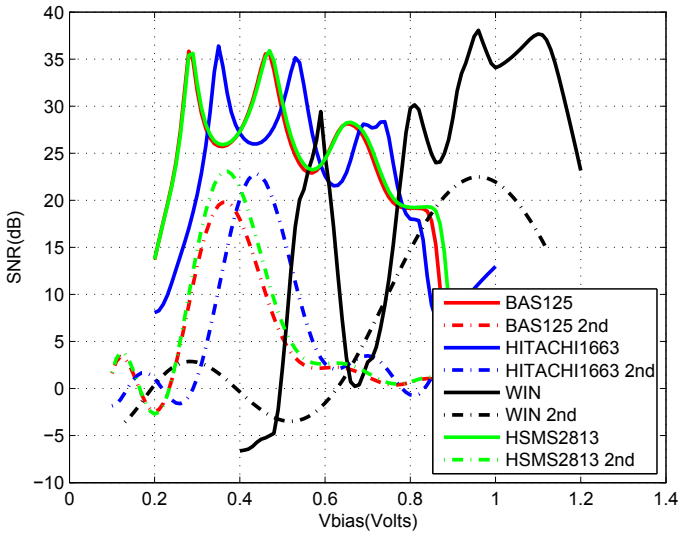


Figure 5.6: The Optimization Results and Second-Order Derivatives.

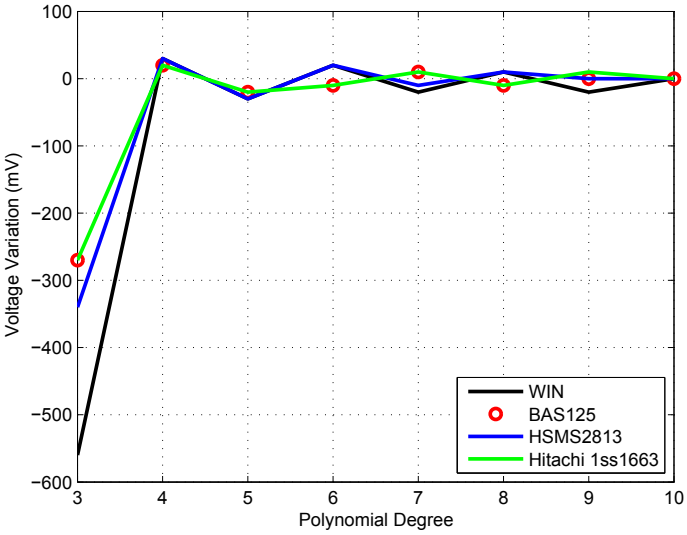


Figure 5.7: Second Derivative With Respect to Polynomial Degree.

5.7 Conclusion

In this section, we presented a method to estimate the initial bias voltage to be used by the optimization algorithm for Multi-Port receivers. This method is applicable for those receivers where the diodes use a bias voltage. It is based on finding the maximum of the second derivative of the fitting polynomial curve for the I-V curve of the diode. The advantage of using this method is that the designer, in a few steps, will find this point for any given diode. We also presented a method of selecting a good fitting polynomial degree by analyzing the variance of the maximum of its second derivative.

Chapter 6

Schottky Diode Memory Effect Characterization

6.1 Introduction

During this research, one topic investigated was the effect on the *EVM* caused by memory effects in the diode power detectors. This section provides a detailed theoretical model plus simulation results of memory effects on Multi-Port receivers. We investigated the effects of nonlinear capacitance in the diodes used in Multi-Port. The memory effects was verified in our system (Multi-Port receiver) and some interesting results in the behaviour of the diode when it is forward biased were found (the bias condition of operation in our model). It turns out that very close to the optimum point, the diode presented the minimum memory effect. We built a diode model that included memory effects and included it in our Simulink system model. Simulation shows that the memory effect presented by (PL15-10) from WIN foundry does not degrade the *SNR*. This information is shown in Fig.4.9 and more detailed information can be found in the following sections. A literature search was performed with many papers found on this subject. Most of these papers present rigorous studies of memory effects for high power devices such as PAs. Some, are listed in the bibliography [78] - [85]. To be able to study the memory effect in Multi-Port receivers, the diode I-V and C-V curves were characterized using ADS from Agilent. The memory effect was modeled and integrated in the Multi-Port receiver Simulink model.

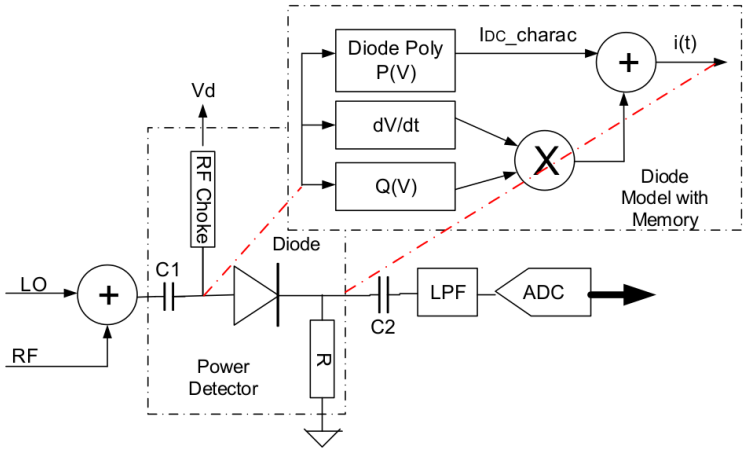


Figure 6.1: Model of the Diode with Memory

6.2 Diode Model With Memory

Figure 6.1 shows the diode polarization circuit that is similar to the one shown in Fig 4.1 with memory effects considered. The memory model is shown in Fig. 6.1 as an exploded view of the diode. The model is built using the **I-V** curve fitting polynomial as in Eq. 4.8, and its associate capacitance also described by the curve fitting polynomial Eq. 6.2. Therefore, the current through the diode is mostly described by the memoryless behaviour of the device and shown in the top branch of Fig. 6.1. The long term memory (LTM) occurs due to the presence of the current through its capacitance. Let $i_{DCCharc}$ be the effect of the current passing through the diode. This effect is modeled when it is forward biased. Therefore, the diodes current can be described as:

$$i(t) = \frac{dQ(t)}{dt} = C(V(t))\frac{dV(t)}{dt} + i_{DC_Char} \tag{6.1}$$

Using Eq. 6.1 the model of the diode with memory can be created and shown in Fig. 6.1.

6.3 Schottky Diode Memory Effect Characterization

The diode used in our research is the PL1510DIODE from WIN (NOF = 2 and Ugw = 20 μm). To characterize the Schottky diode a shunt to ground topology was used as shown in Fig. 6.3. A one port (S11) simulation was performed with the diode forward and reversed bias. The reverse bias simulation was done precisely for completion because our Multi-Port receiver model uses forward biased diodes.

6.3.1 Schematic

Figure 6.2 shows the schematic drawn in *ADS* used to characterize the diode and to find its C-V characteristics. Observe that in Fig. 6.3 there are two identical diodes connected back to back. Diode 1 is forward biased and diode 2 is reversed biased. The C-V curve for either forward or reverse bias is found by un-selecting one of the diodes and leaving the other one active. To calculate the capacitance as function of

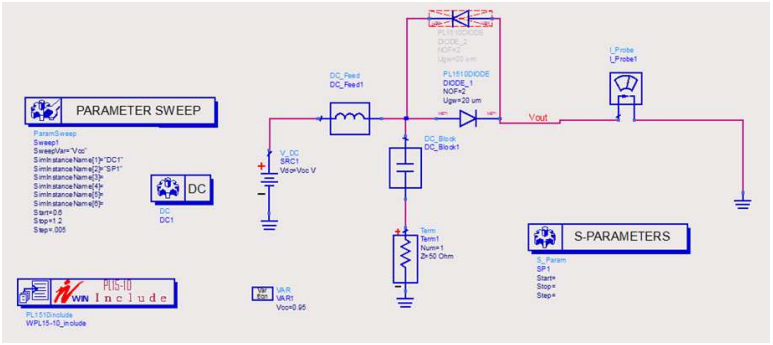


Figure 6.2: Schematic for Diode CV characterization

bias voltage the following steps are performed:

1. Select the diode to be either forward or reverse biased by disabling one of the diodes on the schematic.

2. Run parametric simulations for a given frequency and vary the bias voltage. e.g., Freq = 1900 MHz and Vdiode = 0.6 to 1.5 Volts.

3. Plot the Imaginary part of S11.

4. From Imaginary part of S11 (Imag(S11)) calculate the reactive component (Capacitor/Inductor).

6.3.2 Diode forward biased

Fig. 6.3 shows that when the diode is forward biased and $Vdiode > 925\ mV$, the diode reactance changes from Capacitive to Inductive (i.e., $\Im(S11) > 0$). Therefore, it presents an inductive behaviour instead of capacitive behaviour. It is noticed that this point is very close (25 cmV) to the optimum point found by the Six-Port simulator built in Simulink. That is also shown by the middle point of the second derivative of the fitting polynomial of the *I-V* curve depicted by Fig. 5.4.

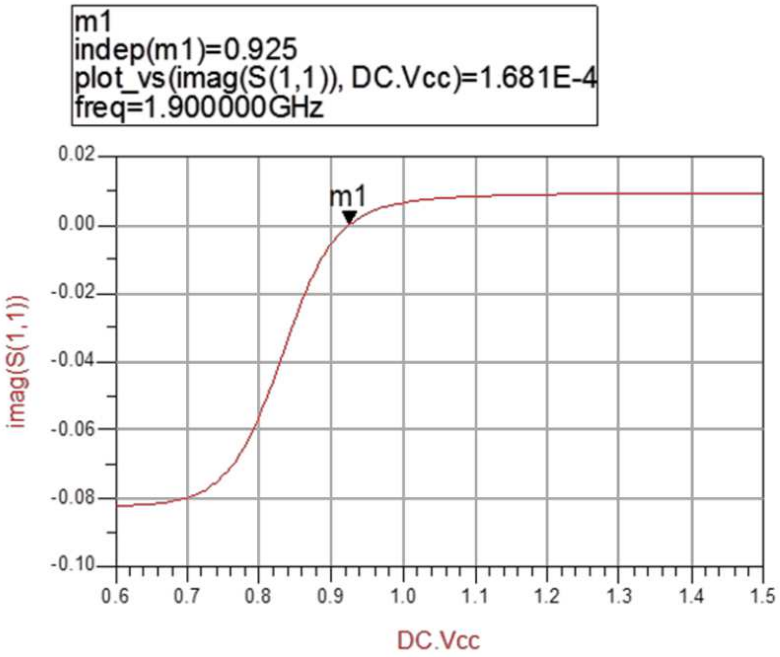


Figure 6.3: Diode Impedance

Fig. 6.3 and Fig. 6.4 shows the capacitance value for $Vdiode < 925\ mV$ and the inductance value for $Vdiode > 925\ mV$. Notice that closer to the optimum point, the reactance is approximately zero. Therefore, the memory surrounding the optimum point should be negligible. Fig. 6.5 shows the impedance of the diode for several diode voltages (0.6 to 1.5 Volts) seen on the Smith Chart.

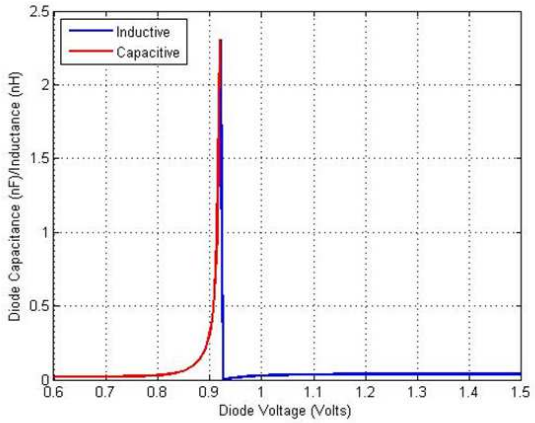


Figure 6.4: Diode Capacitance

6.3.3 Capacitive Curve Fitting

One of the steps to include the diode memory effect into the Simulink system model is to find an equivalent curve fit polynomial to mimic the diode reactance. Using any mathematical package, in our case Matlab, a curve fitting polynomial of order 15 was found for the capacitive behaviour of the circuit (See Eq. 6.2). The criteria to select the polynomial degree was such that the capacitance difference between ADS and polynomial fitting curve was less than 0.05 pF. The comparison between simulation and curve fitting is depicted by Figure 6.6.

$$\begin{aligned} P(x) = 10^5(&-0.0052x^{15} + 0.0600x^{14} + -0.3020x^{13} + 0.8719x^{12} - 1.5666x^{11} + \\ &- 1.6907x^{10} - 0.7006x^9 - 0.9609x^8 + 2.1437x^7 - 2.1877x^6 + 1.4508x^5 \\ &- 0.6674x^4 + 0.2131x^3 - 0.0453x^2 + 0.0058x - 0.0003). \end{aligned} \tag{6.2}$$

Once more we would like emphasize that the polynomial degree is important to provide accuracy at the operation point. The variable x in Eq. 6.2 is the voltage and

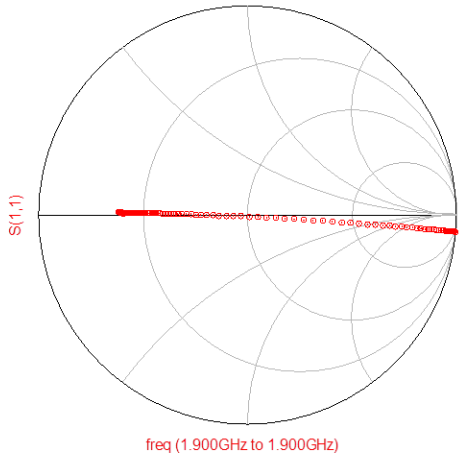


Figure 6.5: Diode Smith Chart Impedance

$P(x)$ is the resultant capacitance as shown in Fig. 6.2.

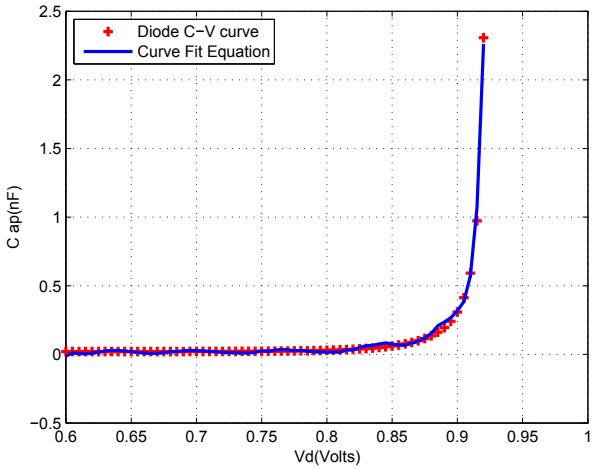


Figure 6.6: Diode CV Characteristics

6.4 Memory Effects Conclusion

Memory effects require complex modeling techniques, like Voltera series, which will add significant complexity to the Multi-Port receiver diodes behavioral modeling. We have shown that there is no significant performance degradation when memory effects are considered; therefore, they are not considered here. The behaviour of the diodes can be approximated by a power series. Figure 4.9 depicts the simulation results obtained by running the Simulink model. It shows the result on the received *SNR/EVM* in three different situations: 1) The curve in black is when the optimizer is turned **OFF**. 2) The curve in blue shows the behaviour of the system when the optimizer is **ON** but memory effects are not considered. 3) The curve in red shows the resultant *SNR* when the optimizer is **ON** and memory effects are modeled into the system. It also shows that there is no difference in the *SNR* when we either added memory effects or not in the model. This is seen because on the blue and red curves there is no significant differences. Notice that the red and blue curves are almost on the top of each other which indicates no or minimal ($\leq 0.5dB$) of difference.

Chapter 7

System Matrix Perturbation Analysis and its Impact on the *EVM*.

7.1 Introduction

In previous chapters we presented the Multi-Port architecture as a receiver. In Chapter 2 we showed that the system matrix **M** is the fundamental mathematical transformation that allows the estimation of the in-phase and quadrature signals from the *RF* receiving signal. The elements of **M** are derived from the physical properties of the Six-Port structure (e.g., Hybrids, couplers) plus the *LO* amplitudes and respective phases. So far the matrix **M** is assumed to have full rank and of course it is well conditioned. In this section we will analyze the degradation in the system's *EVM* performance due to errors in the elements of the system matrix **M**. [86] provides the following statement for this situation: "The matrix elements are afflicted with uncertainties or are perturbed". These source of errors can cause the matrix to present some illnesses (undesired) behaviour. In this chapter we list the system's imperfections in Multi-Port receivers can cause perturbation in the elements of the system matrix **M**. Within those imperfections, the focus of this analysis is the perturbations caused by nonlinearities.

7.2 Difficulties of Solving Linear Systems

To find the solution of a Linear System it is frequently required to manipulate matrices (SVD, LU and QR decompositions, etc). During the process of solving the system two

sources of errors are frequently found: the first is the error in the values of the matrix **M** elements. In the particular case of Multi-Port receivers the algorithm is required to calculate the solution. If the *SNR* is for instance 30 dB at low input level, then the calculated signal power error should be less than 10^{-4}, otherwise the resultant value will not be as precise as it needs to.

Errors in matrix elements: The values of the elements of **M** may be contaminated with errors from measurements (calibration of s-parameters is not accurate enough [48], [76] and [87]-[93].). Figure 7.1 shows that the Multi-Port frequency band can be divided into many sections. At each frequency step in the Multi-Port receiver, a set of s-parameters is found. At every point, a new set of s-parameter will generate a new system matrix **M**. Sometimes for simplicity and therefore implementation cost reduction, the system designer will use a single set of values for **M** for the full frequency band. Caution must be taken to verify if the variation of **M** in the band of interest will not affect the output value of I and Q. If this is the case, during operation, the system shall use different matrices. By using different matrices, the error due to the s-parameter variation will be minimized. **M**'s element errors can also occur due to system order reduction [1] minimization when the system uses the matrix **M** that is represented by a system in which the diodes operate in a second-order region fitting curve but the system is operating in a higher order nonlinear region. These non linear effects are analyzed in detail in Chapter 8.

Errors in the algorithm: A couple of source of errors can appear in Multi-Port receiver algorithms: The first source of error occurs due to the reduction of the precision of the solution by using a matrix **M** which has elements contaminated by errors. This contamination can occur due to calibration as mentioned in the last paragraph and also derived from a second-order diode power detector. Besides errors in the system matrix elements, another reason that errors occur in Multi-Port receivers is due to the usage of finite arithmetic during the algorithm implementation. Care needs to be taken such that numerical errors caused by implementation are not beyond the required precision of the system.

[1] We define system order reduction when a system is well defined by a higher order polynomial and the Multi-Port receiver I and Q estimator uses a matrix **M** derived from a lower order system.

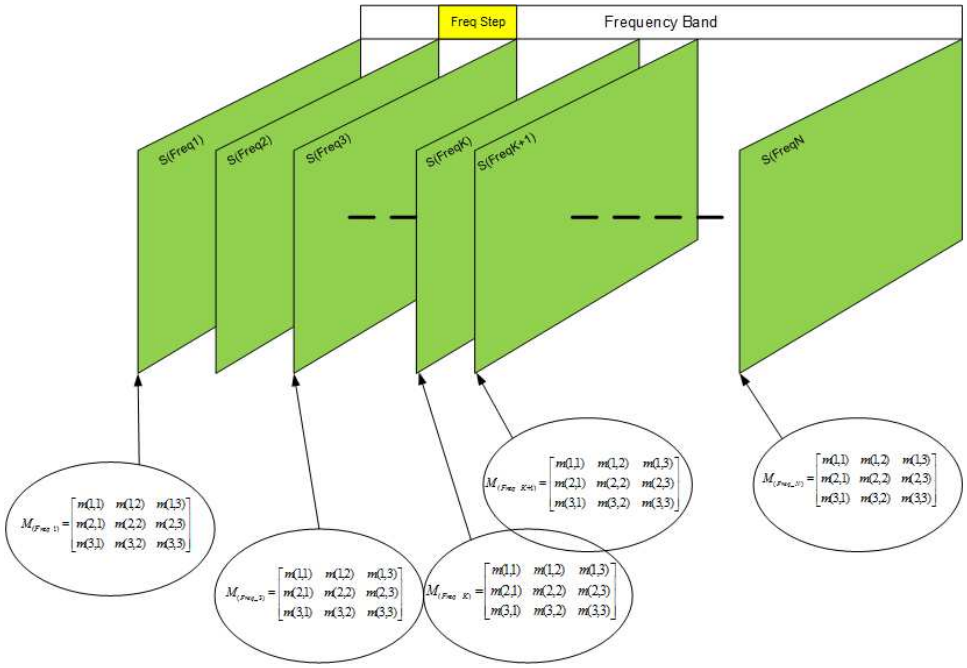


Figure 7.1: Matrix **M** function of S-parameters

7.3 Condition Number Bound

In the previous section, we discussed possible sources of errors in Multi-Port receivers. Fix-point and s-parameter calibration errors can be mitigated during the design of the receiver. On the other hand, the errors caused by letting the diode operate on a higher than a second-order curve fitting region is tough to be mitigated during design. One way to reduce the errors caused by nonlinear effects is to use the technique described in Chapter 4. Therefore, in this section we will focus our analysis on these type of errors. We will start our discussion by analyzing the ratio between the solutions (I and Q estimates) when the diodes are operating on the second and third-order (L=2 and L=3 respectively) fitting regions in Eq. 5.3. By using the matrix **M** with elements derived from an ideal second-order detector as it is given by Eq. 2.2. Let $\hat{x}_2$ and $\hat{x}_3$ be the estimated vector for the second and third-order operation conditions respectively. The estimation of received signals (vector $\hat{x}$) when we assume a second-order power detector is given by Eq. 7.1.

$$\hat{x}_2 = \mathbf{M}^{-1}\vec{P} \tag{7.1}$$

Now the estimation of received signals (vector $\hat{x}$) assuming a third-order power

detector can be expressed in Eq. 7.2

$$\hat{x}_3 = \mathbf{M}^{-1}\vec{P}_3 \tag{7.2}$$

For a given operating frequency band, the elements of 2.2 are kept constant independent of the operating condition of the diodes (e.g., $L = 2$ or $L = 3$). The elements of $\mathbf{M}$ are obtained from the physical characteristics of the scattered elements that built the Multi-Port receiver. Therefore, the power measurement vectors will suffer some perturbation when compared with the $L = 2$ condition, (see Eq 8.5):

$$\left\| \frac{\hat{x}_2 - \hat{x}_3}{\hat{x_2}} \right\| = \left\| \frac{\mathbf{M}^{-1}\vec{P}_3 - \mathbf{M}^{-1}\vec{P}}{\mathbf{M}^{-1}\vec{P}} \right\| \tag{7.3}$$

Let $\vec{e}$ be the signal error due to the algorithm calculation, that is the difference between an *L2* and *L3* condition being estimated by the same system using the same matrix $\mathbf{M}$.

$$\vec{e} = \|\hat{x}_2 - \hat{x}_3\| \tag{7.4}$$

Now with a few mathematical operations we find the value of the error vector dependence of the third-order nonlinearity coefficients.

$$\vec{e} = \|\mathbf{M}^{-1}\vec{P}_3 - \mathbf{M}^{-1}\vec{P}\| \tag{7.5}$$

Let $a_3 DC_{13}$ be the contribution of the third-order nonlinearities to the receiver's signal. Inserting Eq. 8.6 into 7.5 produces:

$$\vec{e} = \|\mathbf{M}^{-1}\| \times \| \left(\vec{P} - a_3 DC_{1,3} \right) - \vec{P}\| \tag{7.6}$$

Hence, the Euclidian norm of the error vector can be given as:

$$\vec{e} = \|\mathbf{M}^{-1}\| \times \| \left(a_3 DC_{1,3} \right) \| \tag{7.7}$$

If we substitute Eq. 7.7 into Eq. 7.4 and back into Eq. 7.3 it will result in the ratio of the norm of the error vector divided by the ideal (second-order operating conditions) received signal:

$$\frac{\vec{e}}{\|\hat{x}\|} = \left\| \frac{a_3 DC_{(1,3)}}{\vec{P}} \right\| \tag{7.8}$$

Equation 7.8 is similar to *EVM* which will be shown in detail in the next section. Another important relationship is shown by Eq. 8.6.

$$\begin{aligned} \vec{P}_3 = \vec{P}_2 + \Delta P &= \mathbf{M}\hat{x}_3 \\ &= \mathbf{M}\left[\hat{x}_2 + \vec{e}\right] \end{aligned}$$

$$\Delta P = \mathbf{M}\vec{e} \Rightarrow \left\|\vec{e}x\right\| = \left\|\mathbf{M}^{-1}\Delta P\right\| \leq \|M^{-1}\| \times \|\Delta P\| \tag{7.9}$$

Which leads to the bound:

$$\left\|\frac{\vec{e}}{\hat{x}_2}\right\| = \left\|\frac{\hat{x}_2 - \hat{x}_3}{\hat{x}_2}\right\| \leq Cond(\mathbf{M})\left[\frac{e}{\left\|\vec{P}\right\|}\right] \tag{7.10}$$

This lead us to the following statement: The condition number of **M** times the relative change of the received power vector due to the high-order operation region bound the relative change in the solution. Notice that by definition the condition number of a matrix is the ratio of its largest and smallest eigenvalues. For a matrix to be well conditioned, the condition number has to be closer to one. Therefore, if **M** is well conditioned, Eq. 7.10 becomes:

$$\left\|\frac{\vec{e}}{\vec{x_2}}\right\| = \left\|\frac{\hat{x}_2 - \hat{x}_3}{\hat{x}_2}\right\| \leq \frac{e}{\left\|\vec{P}\right\|} \tag{7.11}$$

7.4 *EVM* Contribution Analysis

The model calculates the values of the constellation by using matrix **M** instead of $\mathbf{M}_3$. Therefore, the error function caused by the algorithm imperfection can be written as:

$$\vec{e} = a_3 DC_{1,3}\left\|\mathbf{M}^{-1}\right\| \tag{7.12}$$

Looking at Eq.7.12 one notice that if the diode operates in the second-order region, the value of a_3 has to vanish. Therefore, the algorithm error will be reduced to its minimum. Another way to minimize the error would be to try different system matrices but this is not a practical way to reach the optimal solution. In practice, the best way is to force it to operate in the same region where the system matrix **M** is derived. Let S_{ideal} and $S_{estimated}$ be the idea and estimated I and Q signals. The error vector magnitude for a modulated signal is generally given by the following expression:

$$\mathbf{EVM}_{RMS} = \left[\frac{\frac{1}{N}\sum_{r=1}^{N}|S_{ideal} - S_{estimated}|^2}{\frac{1}{N}\sum_{r=1}^{N}|S_{ideal}|^2}\right]^{\frac{1}{2}} \tag{7.13}$$

Therefore, the *EVM* [62]contribution by the algorithm can be found by modifying Eq. 7.13 as:

$$\mathbf{EVM}_{RMS} = \left[\frac{\frac{1}{N}\sum_{r=1}^{N} |\hat{x}_2 - \hat{x}_3|^2}{\frac{1}{N}\sum_{r=1}^{N} |\hat{x}_2|^2} \right]^{\frac{1}{2}} \tag{7.14}$$

$$\mathbf{EVM}_{RMS} = \left[\frac{\frac{1}{N}\sum_{r=1}^{N} \left[\left\| \mathbf{M}^{-1} \right\| a_3 DC_{1,3} \right]^2}{\frac{1}{N}\sum_{r=1}^{N} |\hat{x}_2|^2} \right]^{\frac{1}{2}} \tag{7.15}$$

Eq. 7.15 represents the *EVM* contribution caused by the algorithm to use a second-order matrix to solve a third-order system.

7.5 Conclusion

In this section, we show some types of implementation errors that can occur in the system. They can be divided into two classes: contamination of the elements of **M** and implementation errors caused by using fix-point mathematics during the system implementation. We also show that the contamination of **M** can occur due to calibration and or by operating the system beyond a second-order fitting region on the diode's *I-V* curve. The reason for the nonlinearities to occur is due to the large dynamic range required in many wireless systems (e.g., Cellular, WiFi, etc). Even though the receiver uses *AGC*, we cannot guarantee that the system will operate on a given region of the diode I-V curve (e.g., L=2,3, 4 or even higher). Therefore, during system operation we will need to choose one **M** matrix to find the value of $\hat{x}$. This chapter shows that by using a constant matrix, the power measurement will suffer an effect that we can name perturbation of the power vectors. For $L = 3$ the power vector is given by Eq. 8.4. we conclude this chapter by showing mathematically the increase of the rms value of the *EVM* as a function of these errors.

Chapter 8

Mitigating High-Order Intermodulation in Multi-Port Receivers

8.1 Introduction

This section analyses the effect of high-order intermodulation products in the system and provides an avenue to mitigate these products up to fourth-order. It also provides a methodology to mitigate even higher order nonlinearity effects. One of the applications that Multi-Port receivers are suitable is *SDR*. The reason is due to the wideband behaviour of these devices. Published literature [48] claims that it is possible to design a Multi-Port receiver that operates within four octaves of bandwidth. These devices use diodes which present high-order nonlinearity effects. The linear system used to calculate I and Q from the power detected from the received *RF* signal is given in Eq.2.7. This assumes that the ideal diode behaviour can be approximated by a second-order polynomial, but the system will operate in optimized condition if the following conditions are met:

1. The optimizer finds the optimum bias point which is located on a second-order polynomial fitting region of the *I-V* curve.
2. The *AGC* will limit the maximum amplitude of the *RF* signal to a region of the I-V curve approximated by a second-order polynomial.

In this section we present a method for improving the algorithm precision when the diode is operating in a region of the I-V curve where it cannot be represented with acceptable error (See Eq: 5.20) by a second-order polynomial. If the diode is operating in such a region, to meet the *EVM* requirements for the system, it is required to modify the algorithm that calculates I and Q. This happens because the system matrix $\mathbf{M}$ will grow as we consider higher order polynomial fitting regions. This growth, if not considered during the calculation of I and Q, will generate more nonlinear products than those needed for a pure second-order region.

8.2 Analysis of Regions that Present Nonlinearity Greater than Two

Multi-Port system analysis for second-order detector is provided in the background section and also in already published literature, e.g., [14], [27]. The assumption that the system uses a second-order power detector has been used up to this section of the proposal. We saw that to achieve good algorithm precision the diode was biased on the second-order region and the *AC* signal (*RF* plus *LO*) is constrained into a range that does not allow the AC (LO + RF) signal at the diode to go beyond the second-order fitting region. In this section, we will present the analysis of the system for a higher order intermodulation mitigation. Hence, we will show how the $\mathbf{M}$ matrix shall be modified to accommodate these nonlinearities. We will start with a third-order system and provide analysis for a fourth-order system.

Third-Order System: L=3

At this point, we will use Eq 5.17, but considering $L = 3$. The voltages at the input of the diode is written as:

$$V_1(t) = [V_{diode}]^2 + \xi_1 [V_{diode}]^3 \tag{8.1}$$

with

$$V_{diode} = V_{bias} + K_{LO} V_{LO}(t) + r_s(t) \tag{8.2}$$

and ξ_1 being the coefficient (scalar) that represents the contribution of the third-order intermodulation contribution. Let y_{2LPF} and y_{3LPF} represent the second and third-order components the output of the low pass filter. Therefore, the voltage at the output of *LPF* is given as:

$$y_{LPF}(t) = V_{1LPF}(t) = y_{2LPF}(t) + \xi y_{3LPF}(t) \tag{8.3}$$

Adopting three phases $\left[\phi_1,\ \phi_2\ and\ \phi_3\right]$ for the oscillator a system equation similar to the one calculated for the case where L=2 is found:

$$M = \begin{pmatrix} (1 + 3\xi V_{bias}) & A_{LO}\,(1 + 3\xi V_{bias})\cos(\Theta_1) & -A_{LO}\,(1 + 3\xi V_{bias})\sin(\Theta_1) \\ (1 + 3\xi V_{bias}) & A_{LO}\,(1 + 3\xi V_{bias})\cos(\Theta_2) & -A_{LO}\,(1 + 3\xi V_{bias})\sin(\Theta_2) \\ (1 + 3\xi V_{bias}) & A_{LO}\,(1 + 3\xi V_{bias})\cos(\Theta_3) & -A_{LO}\,(1 + 3\xi V_{bias})\sin(\Theta_3) \end{pmatrix} \tag{8.4}$$

$$\vec{P_3} = \begin{pmatrix} P_1 - \left(V_{bias} + \frac{A_{LO}^2}{2} + \xi DC_{1,3}\right) \\ P_2 - \left(V_{bias} + \frac{A_{LO}^2}{2} + \xi DC_{1,3}\right) \\ P_3 - \left(V_{bias} + \frac{A_{LO}^2}{2} + \xi DC_{1,3}\right) \end{pmatrix} \tag{8.5}$$

or

$$\vec{P_3} = \vec{P_2} + \xi DC_{1,3} \tag{8.6}$$

Where P_1, P_2 and P_3 are scalar measured power values, $\vec{P_2}$ and $\vec{P_3}$ are vectors containing scalar measured power values from the second and the third-order regions of the I-V curve.

$$\vec{x} = \begin{pmatrix} \frac{\left(x_I^2(t) + x_Q^2(t)\right)}{2} \\ x_I(t) \\ x_Q(t) \end{pmatrix} = \begin{pmatrix} RSSI \\ \mathrm{I} \\ \mathrm{Q} \end{pmatrix} \tag{8.7}$$

The blue text are the extra values to be considered in Eq:2.2 and when a third-order polynomial is considered in the calculation. Therefore, to precisely calculate the value of I and Q without affecting the EVM it is necessary to change the matrix **M** elements but the size is kept the same as for second-order.

Fourth-Order System: L=4

Now we will consider up to the fourth-order operation region. In this section it is shown that the system matrix **M** needs to be enlarged. Let us start our analysis by assuming that ξ_1 and ξ_2 are scalars less than one that represent the contributions for the third and fourth-order components. Therefore, the non filtered voltage at the output of the diode will be given by Eq. 8.8 with the diode voltage (V_{diode}) given by Eq. 8.2.

$$V_1(t) = [V_{diode}]^2 + \xi_1\,[V_{diode}]^3 + \xi_2\,[V_{diode}]^4 \tag{8.8}$$

To find the system matrix **M**, we need to consider the second third (Eq. 8.9) and higher order effects as well as. We shall name it as **M4**. Observe that the combination of second and third-order is represented by a 3×3 matrix, whereas the fourth-order has to be represented by a 10×10 matrix. Therefore, we need to add **M0** to the first 3×3 elements of **M4**. Now, we can write:

$$M0_{3\times3} = \begin{pmatrix} (1+3\xi V_{bias}) & A_{LO}\,(1+3\xi V_{bias})\cos(\phi_1) & -A_{LO}\,(1+3\xi V_{bias})\sin(\phi_1) \\ (1+3\xi V_{bias}) & A_{LO}\,(1+3\xi V_{bias})\cos(\phi_2) & -A_{LO}\,(1+3\xi V_{bias})\sin(\phi_2) \\ (1+3\xi V_{bias}) & A_{LO}\,(1+3\xi V_{bias})\cos(\phi_3) & -A_{LO}\,(1+3\xi V_{bias})\sin(\phi_3) \end{pmatrix} \tag{8.9}$$

M4 is the equation that represents the behaviour of the system due to fourth-order nonlinearities. For presentation purpose only, we represent **M4** by a partition of **M1** and **M2**.

$$M1_{10\times5} = \begin{bmatrix} 2K_0 & K_2\cos(\phi_1) & K_3\sin(\phi_1) & \frac{1}{4}\cos\left(\phi_1\right) & \frac{3}{2}\cos\left(\phi_1\right) \\ 2K_0 & K_2\cos(\phi_2) & K_3\sin(\phi_2) & \frac{1}{4}\cos\left(\phi_2\right) & \frac{3}{2}\cos\left(\phi_2\right) \\ \vdots & & \ddots & & \vdots \\ 2K_0 & K_2\cos(\phi_{11}) & K_3\sin(\phi_{11}) & \frac{1}{4}\cos\left(\phi_{11}\right) & \frac{3}{2}\cos\left(\phi_1\right) \end{bmatrix} \tag{8.10}$$

$$M2_{11\times5} = \begin{bmatrix} \frac{3}{2}\sin\left(\phi_1\right) & \frac{3}{2} & \frac{3}{2}\sin\left(2\phi_1\right) & -\frac{9}{2}A_{LO}\cos\left(\phi_1\right) & \frac{3}{2}A_{LO}\cos\left(\phi_1\right) & \frac{3}{2} \\ \frac{3}{2}\sin\left(\phi_2\right) & \frac{3}{2} & \frac{3}{2}\sin\left(2\phi_2\right) & -\frac{9}{2}A_{LO}\cos\left(\phi_2\right) & \frac{3}{2}A_{LO}\cos\left(\phi_2\right) & \frac{3}{2} \\ \vdots & & \ddots & \vdots & & \\ \frac{3}{2}\sin\left(\phi_1\right) & \frac{3}{2} & \frac{3}{2}\sin\left(2\phi_{11}\right) & -\frac{9}{2}A_{LO}\cos\left(\phi_{11}\right) & \frac{3}{2}A_{LO}\cos\left(\phi_{11}\right) & \frac{3}{2} \end{bmatrix} \tag{8.11}$$

Where the K values in Eq. 8.10 and 8.11 are given in Eq.8.12 - 8.15 .

$$K_0 = 3V_{bias}^2 + \frac{3}{2}Alo^2 \tag{8.12}$$

$$K_1 = 3V_{bias}^2 + \frac{3}{2}Alo^2 \tag{8.13}$$

$$K_2 = 6Alo^2V_{bias}^2 + 2Alo^3 \tag{8.14}$$

$$K_3 = 6Alo^2V_{bias}^2 + \frac{3}{2}Alo^3 \tag{8.15}$$

$$M4_{11\times11} = \begin{pmatrix} M1_{11\times5} & M2_{11\times6} \end{pmatrix} \tag{8.16}$$

To precisely solve the system, the final **M** matrix shall be a 10×10 matrix. Observe the power vector as represented by a 11×1 size vector instead of a 3×1 as represented in Eq. 8.5. Another factor that needs to be considered is how the system will require 11 different phases which are not orthogonal within themselves anymore.

$$\vec{P} = \begin{pmatrix} P_1 - \left(V_{bias} + \frac{A_{LO}^2}{2} + \xi DC_{1,3} + K_1\right) \\ P_2 - \left(V_{bias} + \frac{A_{LO}^2}{2} + \xi DC_{1,3} + K_1\right) \\ P_3 - \left(V_{bias} + \frac{A_{LO}^2}{2} + \xi DC_{1,3} + K_1\right) \\ \vdots \\ P_{10} - \left(V_{bias} + \frac{A_{LO}^2}{2} + \xi DC_{1,3} + K_1\right) \end{pmatrix} \tag{8.17}$$

Consequently, the vector $\vec{x}$ also has size 10×1 and it is represented by Eq. 8.18. Observe that in this case many other unnecessary elements are calculated not only the second and third elements of $\hat{x}$ and $\left(x(2,1) = x_I(t) = I, x(3,1) = x_Q(t) = Q\right)$. Notice that all other elements of $\hat{x}$ are other values not I and Q.

$$\hat{x} = \begin{pmatrix} \frac{\left(x_I^2(t)+x_Q^2(t)\right)}{2} \\ x_I(t) \\ x_Q(t) \\ \frac{\left(x_I^2(t)-x_Q^2(t)\right)}{2} \\ x_I^3(t) \\ x_Q^3(t) \\ x_I^4(t) + x_Q^4(t) \\ x_I(t)x_Q(t) \\ x_I^2(t)x_Q(t) \\ x_I(t)x_Q^2(t) \\ x_I^2(t)x_Q^2(t) \end{pmatrix} \tag{8.18}$$

Observe that if we want to mitigate fourth-order intermodulations, we will need ten power detectors. This approach makes the solution impractical. Therefore, the best approach is to use an optimizer to find the best operation bias point for the diode's

power detectors.

8.3 Simulation Results

This section presets simulation results of the system operating with an ideal diode (Second-order law - $L = 2$) and when the diode polynomial fitting from the diode (HSMS8213) is obtained from *ADS* using the process described in Chap 4. The simulation set up is described in table 8.1.

Table 8.1: Simulation Conditions Idea and HSMS8213

Item	Value	Comments
Carrier Feed Through	None	Not considered
I and *Q* imbalance	None	Not Considered
Nonlinearities	*PA* and *LNA*	*P1dB*, *IIP2*and *IIP3*
AWGN	46 dB	See footnote [1]
LNA Noise Figure	None	Noise figure in dB
ACI	Adjacent channel	No interferer considered
Symbol Rate	20 Msps	Msps
Carrier Frequency	700MHz	Tx = Rx *LO* MHz
Modulation Type	64 QAM	
LNA Gain	10 dB	dB
VGA Gain	*VGA*	Controlled by AGC
RRC Filter	Yes	
Roll Off Factor (ROF)	0.5	$0 \leq ROF \leq 1$
Up-sampling Factor	8	*FUS* (*Integervalue* ≥ 2)
Diode Type	HSMS8213	HP
Parametric Simulation	Yes	Diode Bias Voltage
LO power	-10 dBm	Fix value
LO Phase Error	0	Not applied
RF Input	-40 dBm	
Optimizer and Memory Effects	Multi-Port	
Memory Effects	OFF	
Optimizer	OFF	

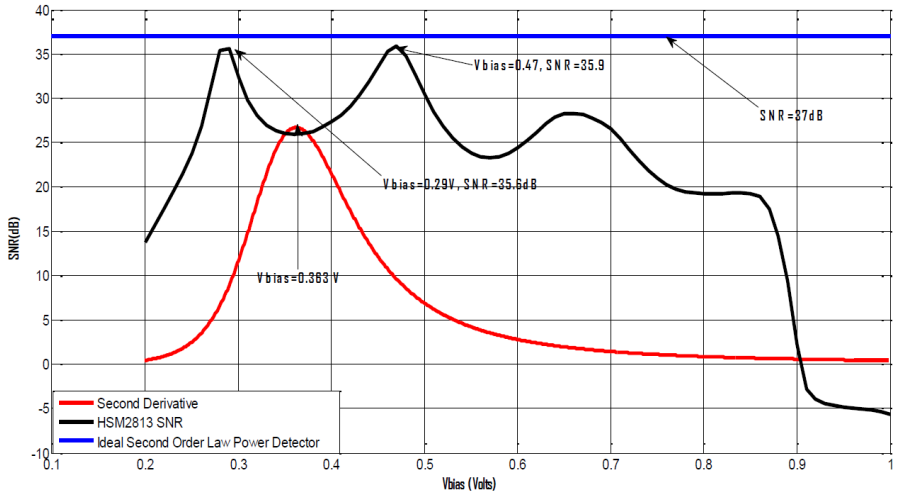


Figure 8.1: Comparing EVM when using an ideal diode and HSMS8213

Fig 8.1 shows in blue the *SNR* results obtained when the diode is represented by a second-order power detector (ideal diode). In black the SNR values were obtained when the diode was modeled as a polynomial (non-ideal). On both simulations (ideal and non-ideal) the bias voltage is swept from 0.2 to 1 Volt. When the system uses the ideal diode the SNR does not vary with respect to the diode bias voltage, but when the non-ideal diode is used the SNR value varies with its bias voltage. There are two optimum operating points located at 290 and 470 mV. These voltage values represent regions where the diode I-V curve is well fit by a second-order polynomial.

8.4 Conclusion

In this section we presented the mathematical analysis that describes how to reduce the intermodulation product's effect on *EVM* for Multi-Port receivers when operating in a region where they are not well represented by a second-order fitting polynomial. We noticed that by reducing the intermodulation effects, it is necessary to increase the size of the system matrix **M** to be able to minimizes the higher-order intermodulation effects. A mathematical solution can be calculated but at the system level this type of mitigation is impractical, firstly because it is unknown which is the higher order intermodulation level to be considered, and secondly because for each intermodulation order the system matrix **M** needs to be adjusted with different element values. Therefore, this section is useful in the sense that it demonstrates how to mitigate high-order intermodulation effects and how difficult it is to mitigate them without using an optimizer in Multi-Port receivers.

Chapter 9

Simulink Model Validation

9.1 Introduction

In previous chapters we discussed adding a bias voltage to the diode, use of an optimizer to find the optimum value for this bias and a process to find the best initial value. In order to prove this concept a Simulink Model was created to simulate, observe the performance of the Multi-Port receiver under many conditions (e.g., Using different diodes, *AWGN*, *ACI*, nonlinearities, etc.). This model shows the communication system *EVM*, *BER*, transmitted and received spectrum, and eye diagram. The model was validated against the published measured results in [48], [49] and [50]. The objective of this validation is to show that the model simulation results are consistent with the tested implementation.

One of the novelties of this thesis is to present a method to estimate the bias point for the diode power detectors using an optimization algorithm. It was shown that by using this optimum bias point the receiver *SNR* is maximized. The initial step is to find the bias voltage of the diode used in [48]. Next, we use this voltage to determine the *SNR* from the Simulink model discussed in this thesis. Finally, we compare the *SNR* to the value practically obtained in [48], [49] and [50].

9.2 Model Validation

This section provides a detailed description of the methodology used to validate the Simulink model presented in this thesis. The validation of the model is done in three steps as follows:

1. Find the bias voltage applied to the diode used in [48], [49] and [50].
2. Using the diode bias voltage, determine the *SNR* from the Simulink model discussed in this thesis.
3. Compare the *SNR* to the measured results obtained in [48], [49] and [50].

9.2.1 DC Analysis (Finding the Diode Bias Voltage)

Fig. 9.1 shows the circuit used in [48], [49] and [50]. This circuit is composed of three distinct sections: The first one is the diode detector which is biased at -1 Vdc. The second section is the low pass filter (RLP-50+) which is used as an anti-aliasing filter. The third section is the baseband amplifier (MAR-8A+) which provides gain to the detected filtered low frequency signal. To determine the diode voltage, we will focus our analysis on the first section of the circuit. Some details of the low pass filter will be required to clarify our analysis.

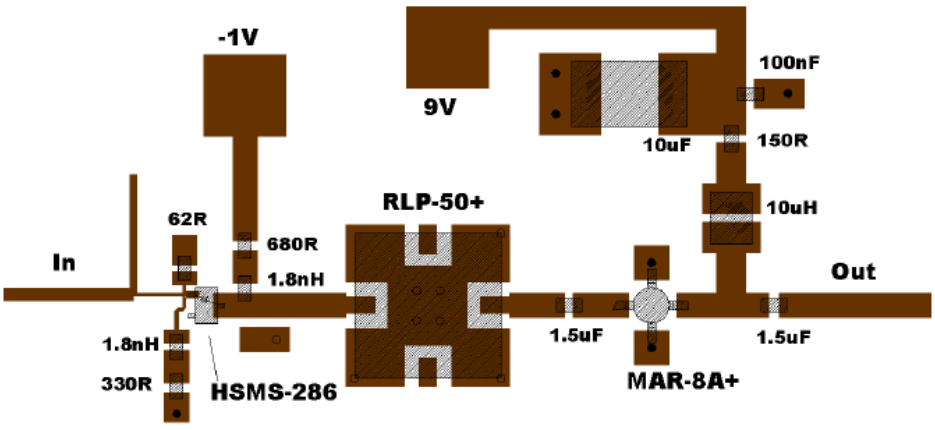


Figure 9.1: Power Detector (Borrowed from [50])

In order to determine the diode bias voltage the *ADS* test bench shown in Fig.9.2 was created. This circuit represents the first section of Fig. 9.1, which encompasses only the diode matching and its bias of -1 Vdc. During DC analysis, the inductors in Fig. 9.1 are considered short circuits. The square block with nets named va and vk are the HSMS286 cathode and anode respectively. The diode Spice model is graphically represented by the diode symbol above of the square block. The 330 Ω and 62 Ω

resistors in Fig 9.1 are in parallel and their equivalent parallel resistance is $R2 = 52\ \Omega$ as shown in Fig. 9.2.

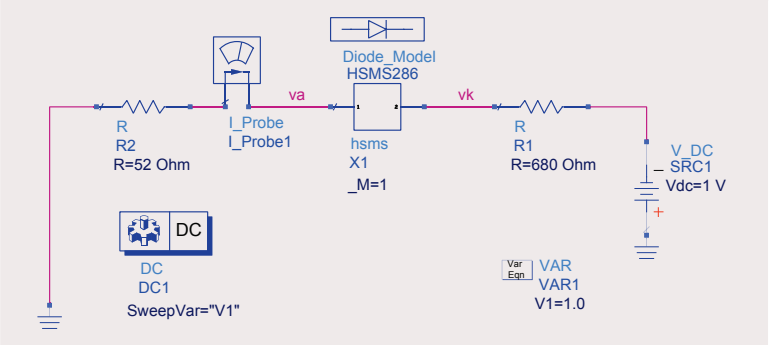


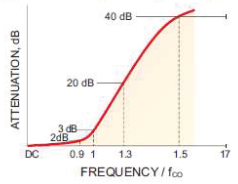
Figure 9.2: Equivalent Power detector DC Analysis Circuitry

In Fig. 9.1 the right and left sides of the first section of the baseband circuit are considered open during DC analysis. On the left side, where the net named **In** is located, the circuit is connected to the *LO* and *RF* signals via capacitors (open for DC analysis) and on the right side it is connected to the low pass filter RLP-50+. This filter provides a DC path as shown in Fig 9.3 (functional schematic), that is blocked using the $1.5\mu F$ capacitor shown in Fig. 9.1.

Low Pass Filter Electrical Specifications (T_{AMB}= 25°C)

PASSBAND (MHz) (Loss < 2dB)	fco, MHz Nom. (Loss 3dB)	STOPBAND (MHz) (Loss > 20dB)	STOPBAND (MHz) (Loss > 40dB)	VSWR (:1) Passband Typ.	VSWR (:1) Stopband Typ.
DC - 50	59	78 - 91	91 - 1000	1.1	20

Typical Frequency Response



Functional Schematic

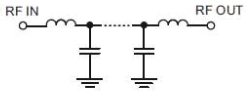


Figure 9.3: Low Pass Filter Equivalent Circuit. (Borrowed from [94])

After running *ADS DC* simulation the cathode and anode voltages, reference to ground, were found. Therefore, the DC voltage across the diode can be calculated as follows: $V_{bias} = -(V_k - V_a) = 280\ mV$. This simulation result is shown in Fig. 9.4

Eqn diode=va-vk

V1	va	vk	Vdiode
0.990	-50.86 mV	-334.9 mV	0.284
1.000	-50.86 mV	-334.9 mV	0.284

Figure 9.4: Diode DC voltage from ADS simulation

9.2.2 Simulation Results

After determining the diode voltage using *DC* analysis as described in the last section, the next step for the validation is to run the Simulink model and find the *SNR* value corresponding to the diode voltage we just found. This value of *SNR* will be compared with the *SNR* value published in [48], [49] and [50].

Fig. 9.5 presents the simulation results obtained using the Simulink model for a voltage sweep from 200 mV up to 1 V. We observe that the received *SNR* has the same trend as the other diodes (e.g., Siemens, Winner, Hitachi and HP(HSMS2813)) simulated using the Simulink model. Fig. 9.5 shows that when the bias voltage is 280 mV the receiver *SNR* is approximately 27.69 dB and the maximum *SNR* value is obtained for a Vdiode = 430 mV.

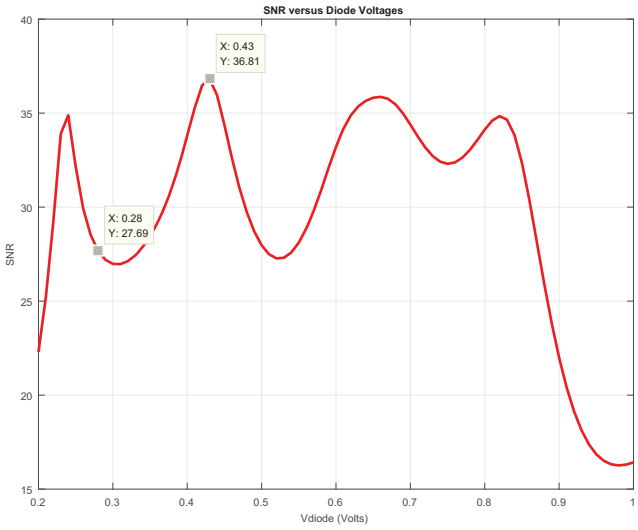


Figure 9.5: EVM obtained by our Simulation Model

9.2.3 *SNR* Comparison

After performing the DC analysis to obtain the value of the *DC* bias voltage that [50] used in her research, we used this voltage (280 mV) to determine the *SNR* from the Simulink model discussed in this thesis. Finally, we compare the *SNR* obtained using the Simulink value against the measured value obtained in [50]. Fig. 9.6 is a copy of a table published in [50] with the *EVM* values obtained during her experiments.

Table 3.6 Measured EVM, P_{LO}=0 dBm, P_{in}=-20 dBm.

Frequency (MHz)	Modulation	Bit Rate (Mbps)	EVM (%)
300	64-QAM	75	6.1
700	16-QAM	62.5	4.8
900	64-QAM	93.75	4.7
1800	QPSK	31.25	4.7
1900	16-QAM	62.5	4.6
2450	64-QAM	93.75	4.5
3500	16-QAM	50	4.4
4000	QPSK	25	4.5
5800	64-QAM	75	4.3
6000	QPSK	25	4.4

Figure 9.6: Measured EVM results from [48]

In order to compare the Simulink results with the results from [48], the EVM values from Fig. 9.6 are transformed to *SNR* values using the following relationship:

$$SNR = 20 \log_{10} \frac{1}{EVM(\%)} \tag{9.1}$$

The first column of table 9.1 shows the frequencies published in [50], the second column shows *EVM* measured results and the third column shows the corresponding *SNR* values. The last column is the difference between our Simulink model results and the results of [50].

(∗) Under same conditions as in [48], [49] and [50]

We can see from table 9.1 that *SNR* results are independent of frequency.

Table 9.1: Comparison between [50] and Simulink Model

Frequency (MHz)	Measured results *EVM* (%)	Measured Results *SNR*(dB)	*SNR* Predicted by our model (∗)	Difference (dB)
700	4.8	26.38	27.67	1.29
900	4.7	26.56	25.43	1.13
1900	4.6	26.74	27.69	0.95
2450	4.5	26.94	25.45	1.49
3500	4.4	27.13	27.69	0.56
5800	4.3	26.74	25.43	1.90

9.3 Conclusion

Table 9.1 illustrates that the results of the Simulink model are consistent with the results published in [48], [49] and in [50]. Fig. 9.5 shows that the DC diode bias voltage used in in [48], [49] and in [50] is not optimum. A bias voltage of 430 mV instead of 280 mV would improve the *SNR*. The *SNR* results of table 9.1 are relatively independent of frequency (27.13-26.38=0.75 dB). Therefore, the behavioral model, which is independent of frequency, is a good representation of a practical Multi-Port receiver.

Chapter 10

Conclusions and Future Work

10.1 Summary of Results

Chapter 3 describes the reasons the tools used in this thesis were selected. That is, the Simulink model that was designed to run the Multi-Port receiver, the settings required by the tool and the impairments the tool supports.

In Chapter 4 an optimization method was proposed that finds the optimum bias voltage for the power detectors that optimized the received signal (**I,Q**) *EVM*. The method was simulated using the model described in Chapter 3. The results obtained demonstrate that using the optimizer, allows for a significant improvements in the received *EVM*. This improvement is the result of the proposed blind optimization algorithm that finds the optimum bias point for the diodes.

Chapter 5 presents a method of finding the initial estimates for the diode bias point. The method is tested for four different Schotkky diodes from different vendors (Win Corp, HP, Hitachi and Siemens), however the method can be applied to any diode. The analysis and simulation shows that setting the initial value for the optimizer where the diode's output DC voltageto input power sensitivity is highest will yield the fastest convergence time for the *EVM* optimizer algorithm.

Chapter 6 discusses the impact of the Schottky diode memory effects on the Multi-Port system performance. The process to model memory effects in the diodes is shown in Fig. 6.1. We have shown that there is no significant performance degradation when memory effects are considered; therefore, they are not considered here. The behaviour of the diodes can be approximated by a power series.

Chapter 7 presents the analysis of the system when its matrix is perturbed and the

perturbation effects on the *EVM*. The perturbation causes error and they will degrade the *EVM* performance. The perturbation in question is caused by nonlinearities in the diodes. No other nonlinearities were considered. This chapter concludes that the system optimizer has to find a region of the diode's I-V curve that has the best fit for a second-order polynomial.

Chapter 8 presents an analysis of mitigating high-order intermodulation in multi-port receivers. It presents the effects of considering high-order intermodulation products on the system matrix **M** and how to mitigate them.

Chapter 9 presents the Simulink model validation. The validation was done comparing the *SNR* value obtained using our model to the value practically obtained in [48], [49] and [50].

10.2 Contributions of the Thesis

This thesis includes the following contributions:

- A blind algorithm that finds the optimum bias point of the diode. The methodology uses the *EVM* as a metric for the optimizer error function.
- To avoid the optimize getting trapped on a local minimum, an initial value is determined by a design methodology that finds the initial estimates for the diode bias point. The design methodology is tested using four diodes from different vendors and can be extended to other diodes.
- A system matrix perturbation analysis for Multi-Port receivers is carried out to show the impact of nonlinearities on *SNR*. A perturbation is produced by nonlinear effects for which a method of mitigation analysis is also proposed.
- We have shown that there is no significant performance degradation when memory effects are considered; therefore, they are not considered here. The behaviour of the diodes can be approximated by a power series instead of using Voltera series.

10.3 Future Work

Many interesting research topics regarding Multi-Port receivers remain uninvestigated. Some of these topics are listed below and described in more detail in the

following section:

1. Adaptive system matrix
2. LOW-IF System analysis and modeling
3. The system matrix ill-condition impact on Multi-Port performance
4. Multi-Carrier Environment
5. Multi variable optimization of *EVM* in Multi-Port receivers
6. Time sharing optimization
7. Multi variable optimizer

These topics I believe are currently the most important for Multi-Port receivers and to the best knowledge of the author they are still not published except in the author's publications: [95] and [96].

10.3.1 Adaptive System Matrix

During my research I noticed that the optimum operation point occurs in a I-V region where it can be very well fit by a second-order polynomial. If the diode bias is away from this point then a different matrix is more suited to be used. Once the model in Simulink calculates the values of I and Q using a second-order diode law, the algorithm will introduce less or minimal error if the diode operates in a second-order region. Therefore, in this case we call it the optimum solution $\hat{x}_{opt}$. The optimizer in Fig. 4.1 is the block responsible to keep the diode operating in a second-order region. This happens by finding a V_{bias} that will result in the minimum *EVM*.

10.3.2 LOW-IF System Analysis and Modeling

Low IF Multi-Port concept introduced by [97] has the advantage of the reduction of the number of *ADCs* required on the down conversion. The down conversion is done in two steps as a super-heterodyne type receiver. The disadvantage is the IF filters (a couple) that are required during the down conversion process. This architecture should add more requirements on the *ADC's* performance but it will require only a couple of *ADCs* instead of three in Five-Ports and four *ADCs* in Six-Ports. The final down conversion shall be done in the digital domain.

10.3.3 The System Matrix Ill-Condition Impact on Multi-Port Performance

In [96] it is mentioned that if the system's matrix **M** becomes ill conditioned the system's rank can be reduced either by lack of proper calibration or its dependance of the Multi-Port linear behaviour with frequency (s-parameters variation with frequency).

10.3.4 Multi-Carrier Environment

For *LTE* 5G some new waveform generation (e.g., Universal Filtered Multi-Carrier (*UFMC*) or Filter Bank Multi-Carrier (*FBMC*)) are being studied ([98]-[100]). In continuation of the research, I propose a research branch on multi-carrier environments that shows the impact of Multi-Port receiver degradation by using standard approaches such as Orthogonal Frequency Division Multiplexing, *FBMC*, *UFMC*, etc.

10.3.5 Multi-Variable Optimization of EVM in Multi-Port Receivers.

Fig. E.16 shows the degradation on *SNR* due to local oscillators phase error for Vdiode = 0.95V which is the optimal V_{bias} for the diode in question. This system is targeted to be low cost and wideband. Both of these requirements (cheap and wideband) will make the oscillator produce a phase error during production. Therefore, unless the system corrects the phase error, the performance will degrade. To avoid this, research of an algorithm to automatically correct the LO phase difference is proposed. This algorithm will use an optimizer instead of direct measurement and correct the phase error at the oscillator output. This is not phase noise but average phase error within LO phases.

10.3.6 Time Sharing Optimization

This optimization approach, imposes the Multi-Port to use multiple optimizers (e.g., Diode bias control, *LO* phase difference, Automatic gain control, *LO* amplitude variation) which operate in time sharing. The algorithm for each optimizer is developed separately. Therefore, to avoid them fighting against each other during the optimization process, they will need to operate in time sharing. Detailed research about the time sharing optimization approach shall be carried out to avoid the optimizers fighting against each other producing the best performance for the system.

10.3.7 Multi Variable Optimizer

Different from the previous approaches, the system will use a unique optimizer that uses a multi-variable optimization algorithm. By using multi-inputs and multi-outputs, the optimizer will optimize all parameters simultaneously instead of using a time sharing approach. Fig. 10.1 shows a block diagram that describes a possible solution for the Multi-Port optimization system. This optimizer will find the optimum operation point (i.e., smallest error vector magnitude of the I and Q signals) by applying corrections on the vector controllable variables on a multidimensional space simultaneously. There are many algorithms available including neural networks.

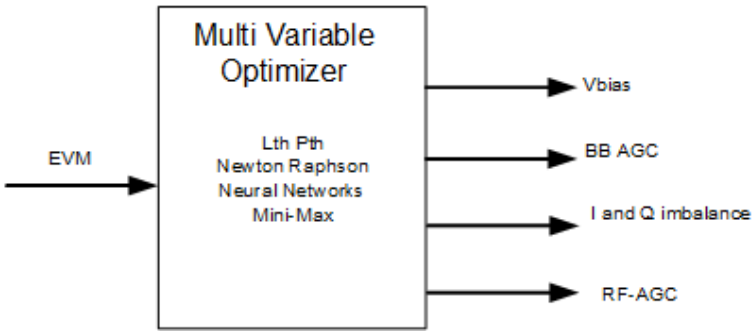


Figure 10.1: Multi Variable Optimization

Appendix A

Intermodulation Analysis

A.1 Introduction

Intermodulation of second and third orders are a subject of the great interest for *RF* system designs and architects. These type of impairments need to be taken in account during a the development of a new *RF* system. This section presents the mathematical derivation that shows the intermodulation signals generated by the non linear elements of a Multi-Port receiver. These non-idealities are generated when passing the received *RF* desired plus interference signal into the nonlinear diodes. On Multi-Port receivers as show in Fig. 1.1 before the *ADC* there is a filter for each diode branch therefore our calculation will be done considering the *LPF*. Now let us analysing only on detector branch of the Multi-Port receiver as shown by Fig. 4.1. Let K be a scalar expressed in Siemens. As per Eq. 5.3 the diode voltage $V_1(t)$ can be expressed as:

$$V_1(t) = K \times \sum_{n=0}^{L} a_n V_d(t)^L \tag{A.1}$$

The low pass filter takes the expected value of the input signal. Therefore, it can be mathematically represented by the following equation:

$$Vout(t) = E\left[V_1(t)\right] = \frac{1}{T}\int_T V_1(t)dt \tag{A.2}$$

Another form to represent the low pass filter is at the frequency domain.

$$LPF[.] = \begin{cases} 1, & \text{if; } \omega \leq \omega_{max} \\ 0, & \text{if } \omega > \omega_{max} \end{cases} \tag{A.3}$$

In the next section we will analyze the diode's voltage considering high-order nonlinearity effects [$L = 2, 3, \ldots$]. This means that we will consider intermodulation products up to maximum value of L.

A.1.1 Analysis of second-order polynomial

For simplicity, let us assume that the diode is operating on a region that the I-V curve can be represented by a second-order degree polynomial (i.e., ideal power detector). Therefore, $V_1(t)$ can be expressed as:

$$V_1(t) = a_0 + a_1 V_d(t) + a_2 V_d^2(t) \tag{A.4}$$

Be $E[.]$ the expected value of a function or random process. Therefore, the output voltage after the *LPF* (integrator) can be expressed as:

$$\begin{aligned} V_0(t) &= E\left[V_1(t)\right] = \frac{1}{T}\int_T V_1(t)dt \\ &= \frac{1}{T}\int_T \left[a_0 + a_1 V_d(t) + a_2 V_d^2(t)\right] dt \end{aligned}$$

The *LPF* will let pass frequencies less than ω_{max}. This means that for these frequencies the LPF is matched with the output of the diode. Looking at Fig 4.1, notice that when the expect value of a function is zero, it does mean that the resistance R is much smaller than the impedance Z_1 at that given frequency band. Therefore, the signal will be rejected by the *LPF* and it will be dissipated on the shunt resistor to ground. Mathematically one can write:

$$\frac{1}{T}\int_T f(t)dt = 0 \Rightarrow R \ll Z_1 \Rightarrow \omega > \omega_{max} \tag{A.5}$$

Let K_1 be a set of scalers which represent DC voltage values.

$$\begin{aligned} V_0(t) &= \underbrace{a_0 + \frac{a_1}{T}\int_T V_d(t)dt}_{=K_1, K_1 \in \Re} \\ &+ \frac{a_2}{T}\int_T \left[V_{bias} + K_{LO}V_{LO}(t) + r_s(t)\right]^2 dt \end{aligned}$$

$$V_0(t) = K_1 + \frac{a_2}{T}\int_T \left[V_{bias} + K_{LO}V_{LO}(t) + r_s(t)\right]^2 dt \tag{A.6}$$

After calculating the squares Eq. (A.6) can be rewritten as

$$\begin{aligned} V_0(t) &= \frac{a_2}{T}\int_T \left[V_{bias}^2 + 2V_{bias}\left(K_{LO}V_{LO}(t) + r_s(t)\right)\right] dt \\ &+ \frac{a_2}{T}\int_T \left[\left[K_{LO}V_{LO}(t) + r_s(t)\right]^2\right] dt + K_1 \end{aligned}$$

$$K_2 = K_1 + \frac{a_2}{T}V_{bias}^2 \int_T dt \tag{A.7}$$

$$\begin{aligned} V_0(t) &= \underbrace{K_1 + \frac{a_2 K_{LO}^2}{T}\int_T V_{LO}^2(t)dt}_{K_3} \\ &+ \frac{2a_2K_{LO}}{T}\int_T V_{LO}(t)r_s(t)dt \\ &+ \underbrace{\frac{a_2}{T}\int_T r_s^2(t)dt}_{K_4} \end{aligned}$$

Notice that the signal at the output will be a *DC* signal plus the desired signal. Let $K_5 = K_3 + K_4$. Thus,

$$V_0(t) = K_5 + \underbrace{\frac{2a_2K_{LO}}{T}\int_T V_{LO}(t)r_s(t)dt}_{desired\ BB\ signal}. \tag{A.8}$$

A.1.2 Analysis of third-order polynomial

In this section, we will proceed with the analysis for a the diode operating on a region which can be represented by a third-order polynomial. By using a third-order polynomial approximation, the *IMD3* products probably will appear at the output of the expected signal. Therefore, let us assume a diode approximation polynomial as shown in Eq. (A.9).

$$V_1(t) = \sum_{n=0}^{3} a_n V_d(t)^n = a_0 + a_1 V_d(t) + a_2 V_d^2(t) + a_3 V_d^3(t) \tag{A.9}$$

We expect an output voltage to be of the type:

$$\begin{aligned} V_0(t) &= E\left[V_1(t)\right] \\ &= K_5 + \underbrace{\frac{2a_2 K_{LO}}{T}\int_T V_{LO}(t) r_s(t) dt}_{\textit{desired signal}} \\ &+ \underbrace{K_n \int_T f(t) \times dt}_{\textit{intemod Products}} \end{aligned}$$

$$V_0(t) = \frac{1}{T}\int_T \left(a_0 + a_1 V_d(t) + a_2 V_d^2(t) + a_3 V_d^3(t)\right) dt \tag{A.10}$$

$$V_0(t) = \underbrace{\frac{1}{T}\int_T \left(a_0 + a_1 V_d(t) + a_2 V_d^2(t)\right) dt}_{K_5 + \frac{2a_2}{T}\int_T V_{LO}(t) r_s(t) dt} + \frac{a_3}{T}\int_T V_d^3(t) dt \tag{A.11}$$

We can observe that the first integral is already calculated in Eq: (A.8). Therefore, Eq. (A.11) can be rewritten as follows:

$$V_0(t) = K_5 + \frac{1}{T}\int_T V_{LO}(t) r_s(t) dt + \sum_{n=1}^{N} I_{imp} \tag{A.12}$$

Let *Imp* be the sum of all imperfections. That will cause the increase in the *EVM*. Therefore, the integral *Imp* is defined as:

$$Imp = \frac{a_3}{T}\int_T V_d^3(t) dt \tag{A.13}$$

Now if we substitute Eq.(5.5) into Eq. (A.13) we find:

$$Imp = \frac{a_3}{T}\int_T [V_{bias} + r_s(t) + K_{LO}V_{Lo}(t)]^3\, dt \tag{A.14}$$

$$Imp = \frac{a_3}{T}\int_T V_d^2\,[V_{bias} + r_s(t) + K_{LO}V_{Lo}(t)]\, dt \tag{A.15}$$

The integral *Imp* can be represented as a sum of these integrals

$$Imp = \underbrace{\frac{a_3}{T}\int_T V_d^2 V_{bias} dt}_{I_1} + \underbrace{\frac{a_3}{T}\int_T V_d^2 r_s(t) dt}_{I_2} \tag{A.16}$$

$$+ \underbrace{\frac{a_3}{T}\int_T V_d^2 K_{LO}V_{Lo}(t) dt}_{I_3} \tag{A.17}$$

(A.18)

Now let us solve each one of the three integrals I_1, I_2 and I_3 one by one. Starting with I_1 and using A.16 after some math manipulation one can write:

$$I_1 = \frac{a_3}{T}\int_T V_d^2 V_{bias} dt \tag{A.19}$$

$$I_1 = DC_{I1} + \frac{2K_6}{T}\int_T V_{LO}(t) r_s(t) dt + \frac{a_3 V_{bias}}{T}\int_T r_s^2(t) dt \tag{A.20}$$

Where

$$DC_{I11} = a_3 V_{bias}^3 + \underbrace{\frac{a_3 V_{bias} K_{LO}^2 A_{LO}}{2}}_{K_6} \tag{A.21}$$

Now in a similar manner, let us find the value of the integral I_2.

$$I_2 = \frac{a_3}{T}\int_T V_d^2 r_s(t) dt \tag{A.22}$$

$$I_2 = \frac{2V_{bias}K_{LO}a_3}{T}\int_T r_s(t) V_{LO}(t) dt$$

Let us now calculate I_3

$$I_3 = \frac{a_3}{T}\int_T V_d^2 K_{LO} V_{Lo}(t)dt \tag{A.23}$$

$$I_3 = \underbrace{\frac{2a_3 V_{bias} K_{LO}^2 A_{LO}}{2}}_{=DC_{I3}} + \underbrace{\frac{2a_3 V_{bias} K_{LO}}{T}\int_T V_{LO}(t) r_s(t)dt}_{IMD3} \tag{A.24}$$

Therefore, the voltage at the output of the filter is:

$$Imp = I_1 + I_2 + I_3 \tag{A.25}$$

$$\begin{aligned} Imp &= DC_{I1} + \frac{2a_3 V_{bias} K_{LO}}{T}\int_T V_{LO}(t) r_s(t)dt \\ &+ \frac{2V_{bias} K_{LO} a_3}{T}\int_T r_s(t) V_{LO}(t)dt \\ &+ DC_{I3} + \frac{2a_3 V_{bias} K_{LO}}{T}\int_T V_{LO}(t) r_s(t)dt \end{aligned}$$

Imp is responsible for increasing the *EVM* therefore we noticed that $Imp \sim 0 \Rightarrow p(v_d(t))$ is second-order. This happens because the imperfections are resultant from third-order intermodulation products.

Appendix B

Input IPn and P1dB Analysis

B.1 Linear System

A system with impulse response $h(t)$ is said to be linear if and only if the superposition theorem is applicable [101, Ch4]. Namely, suppose that when the system is excited by the input signal $v_1(t)$, the output signal is $y_1(t)$ and when the input is $v_2(t)$ the output is $y_2(t)$. When the input is $v_1(t) + v_2(t)$, the output is $y_1(t) + y_2(t)$ so the system is said to be linear.

For dynamic systems, the following differential equation applies, for some $m, n > 0$ [101, Ch4].

$$\frac{d^n v_{out}}{dt^n} + a_{n-1}\frac{d^{n-1} v_{out}}{dt^{n-1}} + \cdots + a_1\frac{dv_{out}}{dt} = b_m\frac{d^m v_{in}}{dt^m} + \cdots + b_1\frac{dv_{in}}{dt} + b_0 v_{in} \tag{B.1}$$

If the parameters a_i and b_i are constants, the system is called linear time-invariant [102, Ch1], [103, Ch2].

Any system to which we cannot apply the superposition theorem is said to be nonlinear. If the system is memoryless (i.e, the present output does not depend on past inputs) the power series applies to calculate the output signal v_{out} [103, Ch2]:

$$v_{out} = k_0 v_{in}(t) + k_1 v_{in}^2(t) + k_2 v_{in}^3(t) + \ldots \tag{B.2}$$

The values of $[k_0, k_1, k_2 \ldots]$ need to be modeled for each nonlinear electronic device.

When an electronic device is operating in nonlinear region, Eq. B.2 is applied and there will be undesired frequency components that will cause interference in other frequency bands. Nonlinearities could also cause self interference which is the case of two tone beats see Table B.1. Mitigation of the nonlinearities problem can be achieved

using techniques either during the design of the components (Integrated Circuits) as shown in [40] or pre-distortion applied at baseband Ref [104] [105].

Nonlinearities are present in most of electronic devices. They commonly occur on transmitter and receiver front-ends. Nonlinearities can have a devastating impact on the performance a system. In a communication system, the main electronic devices or subsystems that are very susceptible to nonlinearities are the PA (Power Amplifier) and *LNA* (Low Noise Amplifiers).

In this section we describe the effect of nonlinearities in electronic devices. We begin by analyzing the meaning of $P1dB$ ($1dB$ compression point) and explaining the two tone testing. This will walk us through in the calculation of the frequency components (second and third-order components) resulting from the intermodulation distortion and finally lead to the effects of the resulting non-desired frequency components in the system design.

Power Series vs Volterra

Mathematically, any nonlinear transfer function can be written as a series expansion of power terms. In the case of nonlinear memoryless systems, power series is applicable but if the system has memory, power series is not valid anymore. Therefore, Volterra series can be applied as in [106]

$$v_{out} = \lambda_0 + \lambda_1 v_{in} + \lambda_2 v_{in}^2 + \lambda_3 v_{in}^3 + \dots \tag{B.3}$$

Figure B.1 shows a symmetric saturation which can be modeled with series composed by odd order terms, for example

$$y = x - \frac{1}{10}x^3 \tag{B.4}$$

An exponential nonlinearity has the form given by

$$y = x + \frac{x^2}{2!} + \frac{x^3}{3!}. \tag{B.5}$$

The plot is shown by Figure B.2.

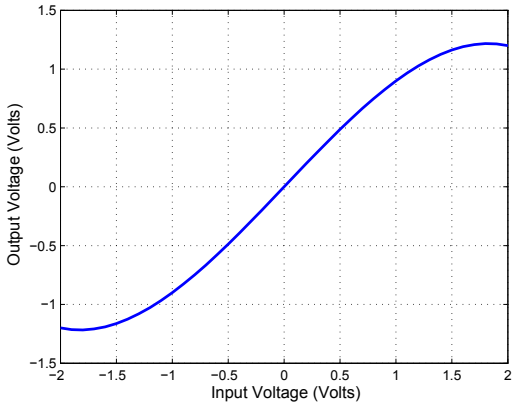


Figure B.1: Symmetric Saturation Model

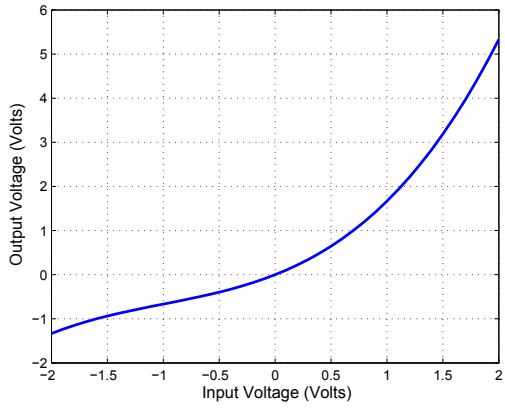


Figure B.2: Exponential Saturation Model

B.1.1 Intemodulation

Intermodulation or *IMD* (intermodulation distortion) is the loss of the characteristics of the transmitted information caused by the nonlinearity of electronic devices. Intermodulation occurs as result of mixing two or more tones present in the input of the electronic circuit. This mixing effect will generate other undesired frequencies at the output of the circuit. In other words, IMD_m is the power of the undesired signal generated by the intermodulation.

Two Tones Test

This is a common intermodulation test for characterizing electronic components such as amplifiers. One very important requirement for this test is to use to assure that the input power of the tones is in the linear region of the amplifier. In communication systems, the great majority of the transmitted signals are composed of more than one tone. Let us first focus on the case where two tones are present at the input of an amplifier, as shown in Figure B.3. Let ω be the angular frequency, f_n a frequency component, $n \in \Re^+$ and t is time. Let $v_1(t) = A_1 \cos(\omega_1 t)$ and $v_2(t) = A_2 \cos(\omega_2 t)$ where $\omega_n = 2\pi f_n$ be the two tones present at the input of the amplifier. For simplicity, let us consider that both signals have the same amplitude $A_1 = A_2 = A$. Therefore, the input signal can be written as $V_{in} = A\cos(\omega_1 t) + A\cos(\omega_2 t)$.

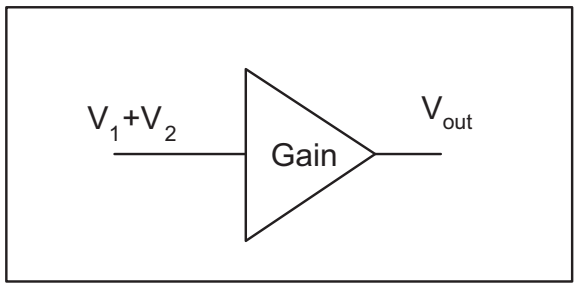


Figure B.3: Two tones input

The power series has an infinite number of terms [102, Ch1], but for simplicity only to the cubic terms are considered. The output voltage at the electronic device can be described as follows:

$$V_{out} = k_0 v_{in}(t) + k_1 v_{in}^2(t) + k_2 v_{in}^3(t) \tag{B.6}$$

The values of $[k_0, k_1, k_2 \dots]$ need to be adjusted (modeled) for each nonlinear electronic device. The second and third-order products from Eq. B.6 are discussed in in the next paragraphs.

Second-Order Intermodulation Products

A second-order intercept point (IP2) can be defined similarly we the third-order intercept point was defined. The decision of using either one of them or both depends on the RF-FE architecture in use and where the design chain, the designer is making the analysis. In some sections of the design second-order intermodulation products are not important but in other sections they might be. Let v_{2nd} be the output signal of the amplifier considering only the first and second-order terms of the power series. Removing the third-order terms from Eq. B.6 yields

$$V_{2nd} = k_1 v_{in}^2(t) = K_1 \left[v_1(t) + v_2(t)\right]^2 \tag{B.7}$$

When substituting the input signals $v_1(t)$ and $v_2(t)$ into V_{2nd}, the result is:

$$\begin{aligned} v_{2nd} = \underbrace{k_1 A^2}_{DC} + \underbrace{\frac{k_1 A^2}{2}\cos\left(\omega_1 + \omega_2\right)t + \frac{k_1 A^2}{2}\cos\left(\omega_1 - \omega_2\right)t}_{Second\ Order\ Intermodulation} \\ + \underbrace{\frac{k_1 A^2}{2}\cos 2\omega_1 t + \frac{k_1 A^2}{2}\cos 2\omega_2 t}_{Second\ Harmonics} \end{aligned} \tag{B.8}$$

The second-order intermodulation products will not generate fundamental frequency components. Therefore one method of removing or attenuating these undesired signals is using filter techniques such as *BPF* (Band Pass Filter).

Let P_{in} and P_{out} be respectively the input and output power of the amplifier in watts and G be the linear gain. One can write the output power of the amplifier with respect to its input power. The gain will be: $P_{out} = P_{in} * G$. If P_i and P_0 are respectively the input and output power expressed in *dBm* and *Gain* is the gain in *dB*. Therefore, P_0 can be written as:

$$P_0 = P_i + Gain \quad (\text{dBm}) \tag{B.9}$$

Let P_{2nd} be the power of the second intermodulation terms and I_2 be the intercept of

the linear Eq. B.9 with vertical power axis P_{out}.

$$\begin{aligned} P_{2nd} &= 10\log_{10}\left(\frac{k_1 A^2}{2}\right)^2 \\ &= \underbrace{10\log_{10}\left(\frac{k_1}{2}\right)^2}_{I_2} + \underbrace{2 * 10\log_{10} A^2}_{2P_i} \\ &= I_2 + 2 * P_i \end{aligned} \tag{B.10}$$

Eq. B.10 shows that for every dB in increase at the input power, the value of the power of the second-order intermodulation will increase by $2dB$.
Once $Gain > I_2$, these two lines Eq. B.9 and B.10 are going to intersect at a point called *Second Order Intercept Point*. The input power level is given as *IIP2* (Input IP2) and will generate the second-order intermodulation components at the output *OIP2* (Output IP2). Figure B.5 details this point and the slope of the lines.

The theoretical voltage at which the IMD2 term will be equal to the fundamental term is

$$\frac{k_2 v_{IP2}^2}{k_1 v_{IP2}} = 1 \tag{B.11}$$

Solving for v_{IP2} one finds:

$$v_{IP2} = \frac{k_1}{k_2} \tag{B.12}$$

Assume a device with gain G in dB, after measuring its output one finds the output power P_1 at fundamental frequency and P_2 at IMD2 frequency for a given input power P_i. From the one to one dB slope curve one writes

$$\frac{OIP_3 - P1}{IIP_2 - P_i} = 1 \tag{B.13}$$

From the 2 dB slope curve we find:

$$\frac{OIP_2 - P2}{IIP_2 - P_i} = 2 \tag{B.14}$$

observe that at the intercept point,

$$G = OIP_2 - IIP_2 = P_1 - Pi \tag{B.15}$$

$$IIP_2 = P_1 + [P_1 - P_2] - G = P_i + [P_1 - P_2] \tag{B.16}$$

B.1.2 General formulation for IIP_m

Figure B.4 shows the relationship between linear second and third-order slopes. Assuming that the input is an interference, a very useful general formula for IIP_m is given by

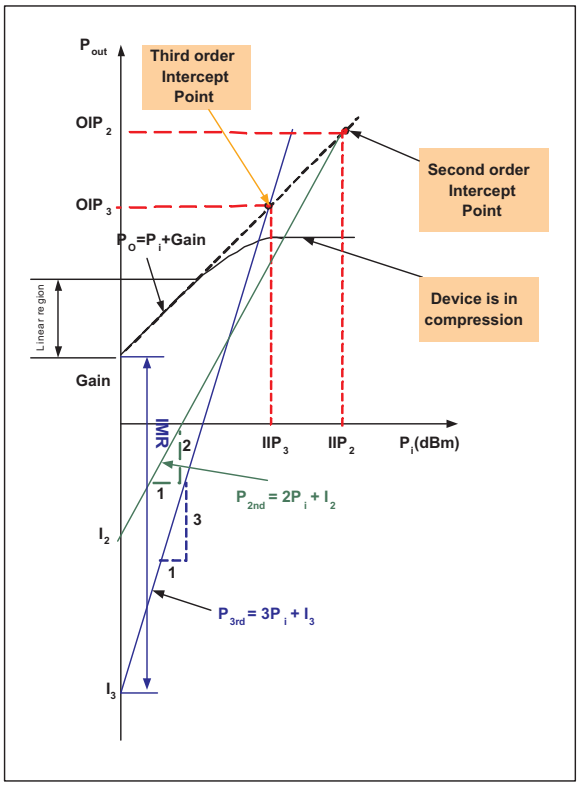


Figure B.4: intercept Points

$$IIP_m = \frac{mI - IMD_m}{m-1} \tag{B.17}$$

Where $m = 2, 3, 4 \ldots$

Third-Order Intermodulation Products .

Now let us consider only the third-order element of Eq. B.6. Let us proceed by expanding this term and calculate the components generated by the third-order nonlinearities when the circuit is excited by two tones. Let v_{3rd} be the output of the amplifier only considering the third-order components.

$$v_{3rd} = k_2 V_{in}^3(t) = K_2 \left[v_1(t) + v_2(t)\right]^3 = K_2 \left[v_1(t) + v_2(t)\right]^2 \left[v_1(t) + v_2(t)\right] \tag{B.18}$$

Applying simple trigonometry Eq. B.18 can be expressed as

$$
\begin{aligned}
V_{3rd} = & \underbrace{\frac{3k_2A^3}{2}\left[\cos\omega_1 t + \cos\omega_2 t\right]}_{Fundamental} + \\
& + \underbrace{\frac{k_2A^3}{2}\cos\left(2\omega_1 + \omega_2\right)t}_{Out\ of\ band\ Intermodulation} + \underbrace{\frac{k_2A^3}{2}\cos\left(2\omega_1 - \omega_2\right)t}_{In-band\ Intermodulation} + \\
& + \underbrace{\frac{k_2A^3}{2}\cos\left(2\omega_2 + \omega_1\right)t}_{Out\ of\ Band\ Intermodulation} + \underbrace{\frac{k_2A_1^2A_2}{2}\cos\left(2\omega_2 - \omega_1\right)t}_{In-band\ Intermodulation} + \\
& + \underbrace{\frac{k_2A^3}{4}\left[\cos 2\omega_1 t + \cos 2\omega_2 t\right]}_{Second\ Harmonics} + \\
& + \underbrace{\frac{k_2A^3}{4}\left[\cos 3\omega_1 t + \cos 3\omega_2 t\right]}_{Third\ Harmonics}
\end{aligned}
$$

This equation shows that third-order intermodulation produces additional frequency components. From Table B.1 we see that some of these components fall within the operating frequency band and therefore cannot be removed by filtering. The only way to mitigate this in-band interference is to operate the device in its linear region.

The harmonic distortion products will located at

$$HDProducts = n\omega_1 \pm m\omega_2, k = n + m \tag{B.19}$$

Therefore, these products can be eliminated by using filtering.

The intermodulation products will be located inside of the desired band and therefore, these undesired interferences cannot be eliminated by filtering because they coexist with the desired signal.

$$IMD_3 \Rightarrow [2\omega_1 - \omega_2, 2\omega_2 - \omega_1] \tag{B.20}$$

The second-order intermodulation products will be located at low frequency and they can sometimes be eliminated by a series capacitor which eliminates DC.

$$IMD_2 \Rightarrow [\omega_1 - \omega_2, \omega_2 - \omega_1] \tag{B.21}$$

Table B.1: Second and Third-order Intermodulation Products for Two Tones test

Frequency	Amplitude	Comments
0	$k_0 + \frac{k_2}{2}\left(v_1^2 + v_2^2\right)$	DC component due to second-order products
ω_1	$k_1 v_1 + k_3 v_1 \left(\frac{3}{4}v_1^2 + \frac{3}{2}v_2^2\right)$	second and third-order
ω_2	$k_1 v_2 + k_3 v_2 \left(\frac{3}{4}v_2^2 + \frac{3}{2}v_1^2\right)$	second and third-order
$2\omega_1$	$\frac{k_2 v_1^2}{2}$	second and third-order
$2\omega_2$	$\frac{k_2 v_2^2}{2}$	second and third-order
$\omega_1 \pm \omega_2$	$k_2 v_1 v_2$	Second-order
$\omega_2 \pm \omega_1$	$k_2 v_1 v_2$	Second-order
$3\omega_1$	$\frac{k_3 v_1^3}{4}$	Third-order
$3\omega_2$	$\frac{k_3 v_2^3}{4}$	Third-order
$2\omega_1 \pm \omega_2$	$\frac{3}{4}k_3 v_1^2 v_2$	Third-order
$2\omega_2 \pm \omega_1$	$\frac{3}{4}k_3 v_1 v_2^2$	Third-order

Example

Two frequencies ($f_1 = 7MHz$ and $f_2 = 8MHz$) are present at the input of a device. If we consider only the second and third-order components, what frequencies will appear at the output?

	Symbolic Freq	Freq (MHz)	Name	Comment
First-order	f_1, f_2	7,8	Fundamental	Desired Out
Second-order	$2f_1$, $2f_2$	14,16	HD2 (harmonics)	Can filter
	$f_2 - f_1$, $f_2 + f_1$	2,15	IMD2 (mixing)	
Third-order	$3f_1$ and $3f_2$	21,24	HD3(harmonics)	Can filter
Third-order	$2f_1 - f_2$	6	IMD3 (Intermod)	Close to
	$2f_2 - f_1$	9	IMD3 (Intermod)	fundamental
				difficult to filter

Let I_3 be the intercept point on the P_{out} axis depicted in Figure B.5. If we apply the same methodology as used in the second-order intermodulation analysis, we can find the following equation

$$P_{3rd} = I_3 + 3 * P_i \tag{B.22}$$

Eq. B.22 shows that for each dB in power increase at the input, the value of the power of the third-order intermodulation will increase by $3dB$.

Once $Gain > I_3$, these two Eq. B.9 and B.22 intersect in a point named *Third Order Intercept Point*, where the input power is named *IIP3* (Input IP3) and will generate the third-order intermodulation component *OIP3* (Output IP3). More details are shown in Figure B.5.

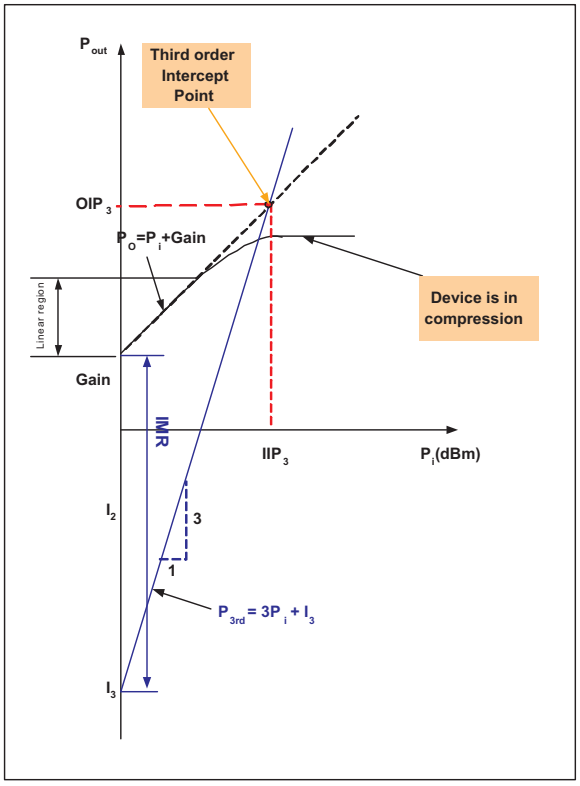


Figure B.5: Third-Order Intercept Point

B.1.3 IP3 Estimation

Theoretical point where the amplitude of the IMD3 tones are equal to the amplitudes of the linear fundamental tones.

Assume $v_1 = v_2 = v_i$

The amplitude of the fundamental tones is:

$$Fund = k_1 v_i + \frac{9}{4} k_3 v_i^3 \tag{B.23}$$

Observe that the linear component is given by

$$Fund_{Linear} = k_1 v_i \tag{B.24}$$

Can be compared with the third-order intermodulation term given by

$$IMD3 = \frac{3}{4} k_3 v_i^3 \tag{B.25}$$

Observe that for small input signal, the fundamental rises linearly (20 dB/decade) and that the IMD3 terms rise as the cube of the input (60 dB/decade).

A theoretical voltage at which these two tones will be equal can be defined:

$$\frac{\frac{3}{4} k_3 v_{IP3}^3}{k_1 v_{IP3}} = 1 \tag{B.26}$$

Solving for v_{IP3} one finds:

$$v_{IP3} = 2\sqrt{\frac{k_1}{3k_3}} \tag{B.27}$$

- Cannot actually be measured
- IIP3(Input referred), OIP3(Output referred)

From the one to one dB slope curve one writes

$$\frac{OIP_3 - P1}{IIP_3 - P_i} = 1 \tag{B.28}$$

From the 3 dB slope curve one writes

$$\frac{OIP_3 - P3}{IIP_3 - P_i} = 3 \tag{B.29}$$

observe that at the intercept point,

$$G = OIP_3 - IIP_3 = P_1 - Pi \tag{B.30}$$

$$IIP_3 = P_1 + \frac{1}{2}[P_1 - P_3] - G \tag{B.31}$$

$$IIP_3 = P_i + \frac{1}{2}[P_1 - P_3] \tag{B.32}$$

B.1.4 Single Tone Test, the P1dB Compression Point

Let us consider the electronic circuit depicted by Figure B.6 and the ideal input voltage described by $v_{in} = A\cos\omega t$; where A is the maximum amplitude, ω is the angular frequency and t is time. We substitute the input voltage v_{in} into Eq. B.2. For simplicity only the first, second and third terms of the output voltage are considered. The output voltage of the electronic device can be written as:

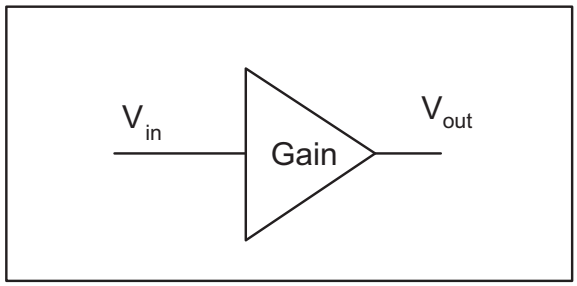


Figure B.6: Single tone input

$$V_{out} = k_0 v_{in} + k_1 v_{in}^2 + k_2 v_{in}^3 \tag{B.33}$$

Expanding Eq. B.33 it is possible to better visualize the terms that appear at the output of the electronic device and this voltage can be represented as follows.

$$V_{out} = \frac{k_1 A^2}{2} + \left(k_0 A + \frac{3k_2 A^3}{4}\right)\cos\omega t + \frac{k_1 A^2}{2}\cos 2\omega t + \frac{k_2 A^3}{4}\cos 3\omega t \tag{B.34}$$

Observe that the second and third harmonic terms appear at the output. These undesirable signal components may be removed by using a band-pass filter centered at ω. Table B.2 shows the amplitude of the output signal components.

Let n be the frequency component index. Then Eq. B.33 can be written as

$$v_{out} = \sum_{n=0}^{2} K_n \cos\left((n+1)\omega t + \theta\right) \tag{B.35}$$

where θ is the phase. When the electronic circuit operates in the linear region, $P_{out} = P_{in} + Gain$. For each dB of increasing at the input power at the circuit, it will correspond a one dB increase in power at the output. When the output power is 1dB lower than the expected value ($P_{out} = P_{in} + Gain - 1$), the circuit is in the nonlinear region and this point is named $P1dB$. This point is depicted by Figure B.7.

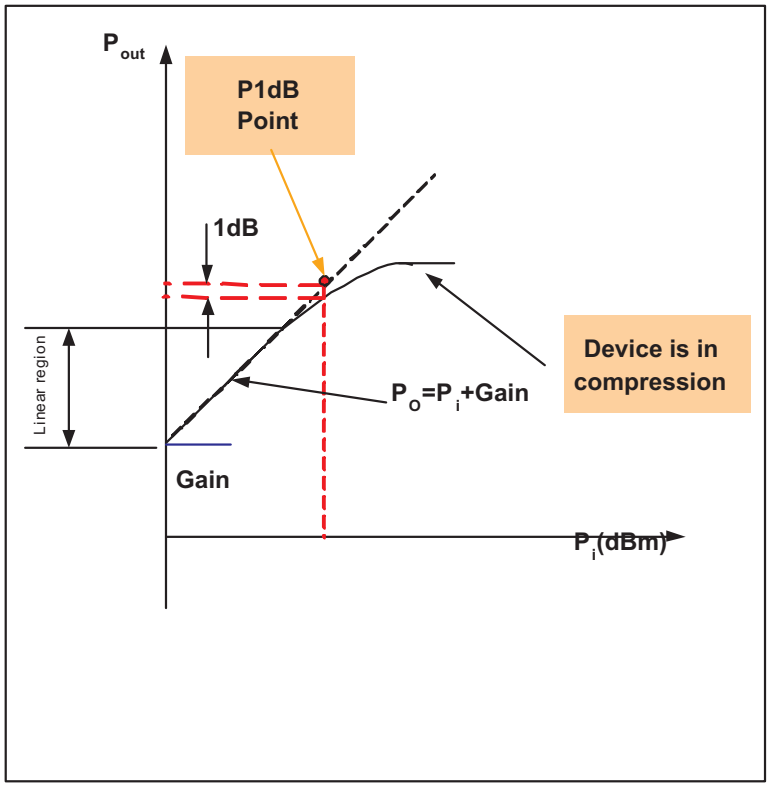


Figure B.7: P1dB point

Table B.2: Frequency Composition at V_{out}

Frequency	Amplitude	Comments
0	$\frac{k_1 A^2}{2}$	DC component
f_1	$k_0 A + \frac{3k_2 A^3}{4}$	Fundamental
$2f_1$	$\frac{k_1 A^2}{2}$	2^{nd} Harmonic
$3f_1$	$\frac{k_2 A^3}{4}$	3^{rd} Harmonic

P1dB and Coefficients of the Trigonometric Series This is another common measurement of linearity. This point is more directly measured than the previous two points (IIP3 and IIP2). To measure this point one requires only one tone. This point is specified either to the input or to the output. This is the point where the output power is 1dB bellow of the expected power.

We first notice that the ration between actual output voltage v_o and the ideal output voltage v_{oi} should be

$$20\log_{10}\left(\frac{v_o}{v_{oi}}\right) = -1dB \tag{B.36}$$

or in linear scale one has

$$\left(\frac{v_o}{v_{oi}}\right) = 0.89125 \tag{B.37}$$

now referring to the 2 tone test table

$$v_o = k_1 v_i + \frac{3}{4} k_3 v_i^3 \tag{B.38}$$

For an input voltage v_i the ideal output voltage is given by

$$\frac{k_1 v_{1dB} + \frac{3}{4} k_3 v_{1dB}^3}{k_1 v_{1dB}} = 0.89125 \tag{B.39}$$

Solving for v_{1dB} one finds:

$$v_{1dB} = 0.38\sqrt{\frac{k_1}{|k_3|}} \tag{B.40}$$

Relationship between 1dB Compression Point and IP3 Points

The relationship between 1 db compression point and IP3 can be found dividing the voltages:

$$\frac{v_{IP3}}{v_{1dB}} = \frac{2\sqrt{\frac{k_1}{|3k_3|}}}{0.38\sqrt{\frac{k_1}{|k_3|}}} = 3.04 \tag{B.41}$$

in dB one calculates

$$20\log_{10}\left(\frac{v_{IP3}}{v_{1dB}}\right) = 9.66dB \tag{B.42}$$

Notice that this analysis is valid for third-order nonlinearities, independent of the coefficients of the series.

B.1.5 Broadband Measures of Nonlinearity

Intercept points and 1 dB compression points are very common measures of linearity, they are by no means the only ones. Two other options in wideband measurement of linearity are:

- Composite triple-order Beat (CTB)
- Composite second-order Beat (CSO)

If we take three tones, then the third-order nonlinearity gets a little more complicated but it can be calculated as per:

$$(x_1+x_2+x_3)^3 = \underbrace{x_1^3+x_2^3+x_3^3}_{HM3} + \underbrace{3x_1x_2^2+3x_1^2x_3+3x_2^2x_1+3x_3^2x_1+3x_2^2x_3+3x_3^2x_2}_{IMD3} + \underbrace{6x_1x_2x_3}_{TB} \tag{B.43}$$

It can be shown that the maximum number of terms will fall in the middle of the band. With **N** tones, it can also be shown that the number of tones falling there will be:

$$Tones = \frac{3}{8}N^2 \tag{B.44}$$

If the fundamental tone is at a power level of P_s, then the power of the TB tones will be

$$TB = P_{IP3} - 3\left(P_{IP3} - P_s\right) + 6 \tag{B.45}$$

Where P_{IP3} is the IP_3 power level for the given circuit.

For the worst case, all tones add the power rather than voltage, and noting that CTB is usually specified as so many dB from the signal power,

$$CTB = P_s - \left[P_{IP3} - 3\left(P_{IP3} - P_s\right) + 6 + 10\log_{10}\left(\frac{3}{8}N^2\right)\right] \tag{B.46}$$

Appendix C

Analysis of the Algorithm Error for Different Operation Regions

C.1 Introduction

This section presents detailed analysis for the Six-Port receivers considering different regions of operations (second, third and fourth-order polynomials). It was shown in Chapter 8 that the best operation region is when the receiving signal fits a region of the diode's I-V curved that best fits a second-order approximation polynomial. This happens because the system matrix **M** is derived from the second-order polynomial as in Eq. C.8. This topic is already covered in Chapter 8 but in this appendix more detailed mathematic analysis is provided including the algorithm error estimation due to this approximation: Use a matrix **M** derived from a second-order approximation diode's polynomial and operate at higher-order region. Let V_{bias} be the diode bias voltage, K_{LO} a scalar that represents the local oscillator coupling factor, V_{LO} the local oscillator voltage and $r_s(t)$ the receiver RF input signal. From Fig. 4.1 we can write the voltage at the output of diode as:

$$V_1(t) = \sum_{n=1}^{L} a_n \left[V_{bias} + K_{LO} V_{LO}(t) + r_s(t)\right]^n \tag{C.1}$$

Once we consider ideal components for the system level investigation, will not consider any *LO* feedthough. Assuming that the maximum interested frequency is ω_c. Therefore, the *LPF* is considered ideal and it has the following frequency response expression:

$$H(j\omega) = \begin{cases} 1 & -\omega_c \leq \omega \leq +\omega_c \\ 0 & \text{otherwise} \end{cases} \tag{C.2}$$

C.1.1 Case where L = 1

In this section we will look at the case when $L = 1$ in Eq. C.1. The diode is considered as a linear element.

$$V_1(t) = [V_{bias} + K_{LO}V_{LO}(t) + r_s(t)] \tag{C.3}$$

Once there is no mixing behaviour, the output signal after the diode will be only the *DC* component.

C.1.2 Case where L = 2

For the case where $L = 2$ and $a_2 = 1$ one finds the following system

$$V_1(t) = [V_{bias} + K_{LO}V_{LO}(t) + r_s(t)] + [V_{bias} + K_{LO}V_{LO}(t) + r_s(t)]^2 \tag{C.4}$$

In order to perform the mathematical evaluation of the high-order polynomial, we used the Mathematica package from Wolfram [107] to do the perform the intermediate mathematical steps. Therefore, evaluating Eq. C.1 using Mathematica we find the following expression:

$$\begin{aligned} V_1(t) = {} & V_{bias}^2 + 2A_{LO}V_{bias}\cos\left(\omega_{LO}t + \phi\right) + A_{LO}^2 V_{bias}\cos^2\left(\omega_{LO}t + \phi\right) \\ & + 2X_I V_{bias}\cos\left(\omega_{LO}t + \phi\right) + 2X_I A_{LO}\cos\left(\omega_{LO}t + \phi\right) \\ & + X_I^2\cos^2(\omega_{RF}t) - 2V_{bias}X_Q\sin(\omega_{RF}t) \\ & - 2A_{LO}X_Q\cos\left(\omega_{LO}t + \phi\right) \times \sin(\omega_{RF}t) \\ & + X_I X_Q\cos^2(\omega_{RF}t)\sin(\omega_{RF}t) + X_Q^2\sin^2(\omega_{RF}t) \end{aligned}$$

Let $y_{LPF}(t)$ be the signal at the output of the low pass filter defined by Eq. C.2. Therefore,

$$y_{LPF}(t) = V_{bias}^2 + \frac{A_{LO}^2}{2} + X_I A_{LO}\cos\left(\phi\right) + \frac{{X_I}^2}{2} - A_{LO}X_Q\cos\left(\phi - \frac{\pi}{2}\right) - X_I X_Q\cos^2\left(-\frac{\pi}{2}\right) + \frac{X_Q^2}{2}$$

Rearranging one have

$$y_{LPF}(t) = V_{bias}^2 + \frac{A_{LO}^2}{2} + X_I A_{LO}\cos\left(\phi\right) - A_{LO}X_Q\sin\left(\phi\right) + \frac{{X_I}^2 + {X_Q}^2}{2} \tag{C.5}$$

$$\underbrace{y_{LPF}(t) - V_{bias}^2 - \frac{A_{LO}^2}{P}}_{P} = A_{LO}X_I\cos\left(\phi\right) - A_{LO}X_Q\sin\left(\phi\right) + \frac{{X_I}^2 + {X_Q}^2}{2} \tag{C.6}$$

Observe that we need three phases and three powers to build a linear system and find the values for X_I and X_Q

$$\vec{P} = M\vec{x} \Rightarrow \vec{x} = M^{-1}\vec{P} \tag{C.7}$$

where the matrix **M**(3x3), the vector $\vec{P}$ and a vector $\vec{x}$ are defined such that:

$$M = \begin{pmatrix} 1 & A_{LO}\cos(\Theta_1) & -A_{LO}\sin(\Theta_1) \\ 1 & A_{LO}\cos(\Theta_2) & -A_{LO}\sin(\Theta_2) \\ 1 & A_{LO}\cos(\Theta_3) & -A_{LO}\sin(\Theta_3) \end{pmatrix} \tag{C.8}$$

$$\vec{P} = \begin{pmatrix} P_1 - V_{bias} - \frac{A_{LO}^2}{2} \\ P_2 - V_{bias} - \frac{A_{LO}^2}{2} \\ P_3 - V_{bias} - \frac{A_{LO}^2}{2} \end{pmatrix} \tag{C.9}$$

the values for the in-phase and quadrature signals can be estimated by finding the vector $\hat{x}$

$$\hat{x} = \begin{pmatrix} \frac{\left(x_I^2(t) + x_Q^2(t)\right)}{2} \\ x_I(t) \\ x_Q(t) \end{pmatrix} = \begin{pmatrix} RSSI \\ \mathrm{I} \\ \mathrm{Q} \end{pmatrix} \tag{C.10}$$

C.1.3 Case where L = 3

Now we will evaluate the expression C.4 for the third-order (L=3) similarly of what we done for L=2..

$$V_1(t) = +V_d + a_2 V_d^2 + a_3 [V_d]^3 \tag{C.11}$$

$$V_d = V_{bias} + K_{LO} V_{LO}(t) + r_s(t) \tag{C.12}$$

Therefore, Eq. C.11 becomes

$$V_{1,3}(t) = [V_{bias} + K_{LO} V_{LO}(t) + r_s(t)]^3 \tag{C.13}$$

Now using Mathematic we find the following expression:

$$\begin{aligned} V_{1,3}(t) = {} & Vbias^3 + 3AloVbias^2 \cos\left(\omega_{LO}t + \phi_{LO}\right) + 3Alo^2 Vbias \cos^2\left(\omega_{LO}t + \phi_{LO}\right) \\ & + Alo^3 \cos^3\left(\omega_{LO}t + \phi\right) + 3Vbias^2 X_i \cos\left(\omega_{RF}t\right) + \\ & 6AloVbiasX_i \cos\left(\omega_{LO}t + \phi\right)\cos\left(\omega_{RF}t\right) + 3Alo^2 X_i \cos^2\left(\omega_{LO}t + \phi_{LO}\right)\cos\left(\omega_{RF}t\right) \\ & + 3VbiasX_i^2 \cos^2\left(\omega_{RF}t\right) + 3AloX_i^2 \cos\left(\omega_{LO}t + \phi\right)\cos^2\left(\omega_{RF}t\right) + X_i^3 \cos^3\left(\omega_{RF}t\right) \\ & - 3Vbias^2 X_Q \sin\left(\omega_{RF}t\right) - 6AloVbiasX_q \cos\left(\omega_{LO}t + \phi\right)\sin\left(\omega_{RF}t\right) \\ & - 3Alo^2 X_q \cos^2\left(\omega_{LO}t + \phi_{LO}\right)\sin\left(\omega_{RF}t\right) - 6VbiasX_iX_q \cos\left(\omega_{RF}t\right)\sin\left(\omega_{RF}t\right) - \\ & 6AloX_iX_q \cos\left(\omega_{LO}t + \phi_{LO}\right)\cos\left(\omega_{RF}t\right)\sin\left(\omega_{RF}t\right) - 3X_i^2 X_q \cos^2\left(\omega_{RF}t\right)\sin\left(\omega_{RF}t\right) + \\ & 3VbiasX_q^2 \sin^2\left(\omega_{RF}t\right) + 3AloX_q^2 \cos\left(\omega_{LO}t + \phi_{LO}\right)\sin^2\left(\omega_{RF}t\right) + \\ & 3X_iX_q^2 \cos\left(\omega_{RF}t\right)\sin^2\left(\omega_{RF}t\right) - X_q^3 \sin^3\left(\omega_{RF}t\right) \end{aligned}$$

Now let us calculate the value after the *LPF*

$$V_{1,3}(t) = Vbias^3 + \underbrace{3AloVbias^2\cos\left(\omega_{LO}t+\phi_{LO}\right)}_{=0} + 3A_{LO}^2 Vbias \quad \underbrace{\cos^2\left(\omega_{LO}t+\phi_{LO}\right)}_{=\frac{1}{2}\left[1+\underbrace{cos\left(2\omega_{LO}t+2\phi_{LO}\right)}_{=0}\right]}$$

$$+ Alo^3\underbrace{\cos^3\left(\omega_{LO}t+\phi_{LO}\right)}_{=0} + 3Vbias^2X_i\underbrace{\cos\left(\omega_{rf}t\right)}_{=0} +$$

$$6AloVbiasX_i \quad \underbrace{\cos\left(\omega_{LO}t+\phi_{LO}\right)\cos\left(\omega_{rf}t\right)}_{=\frac{1}{2}\left[\cos(\phi_{LO})+\underbrace{\cos\left(2(\omega_{RF}+\omega_{RF})t+\phi_{LO}\right)}_{=0}\right]}$$

$$+ 3Alo^2X_i\cos^2\left(\omega_{LO}t+\phi_{LO}\right)\cos\left(\omega_{rf}t\right)$$

$$+ 3VbiasX_i^2\underbrace{\cos^2\left(\omega_{rf}t\right)}_{=0.5} + 3AloX_i^2\underbrace{\cos\left(\omega_{LO}t+\phi_{LO}\right)\cos^2\left(\omega_{rf}t\right)}_{=0} + X_i^3\underbrace{\cos^3\left(\omega_{rf}t\right)}_{=0}$$

$$- 3Vbias^2X_Q\underbrace{\sin\left(\omega_{rf}t\right)}_{=0} - 6AloVbiasX_q \quad \underbrace{\cos\left(\omega_{LO}t+\phi_{LO}\right)\sin\left(\omega_{rf}t\right)}_{\frac{1}{2}\left[\underbrace{\cos\left(\left(\omega_{LO}+\omega_{RF}\right)t+\frac{\pi}{2}+\phi_{LO}\right)}_{=0}+\cos\left(\phi_{LO}-\frac{\pi}{2}\right)\right]}$$

$$- 3Alo^2X_q\underbrace{\cos^2\left(\omega_{LOo}t+\phi\right)\sin\left(\omega_{rf}t\right)}_{=0} - 6VbiasX_iX_q\underbrace{\cos\left(\omega_{rf}t\right)\sin\left(\omega_{rf}t\right)}_{\frac{1}{2}\left[\cos\left(\frac{\pi}{2}\right)+\cos(2\omega_{RF}t+\pi)\right]=0}$$

$$- 6AloX_iX_q\underbrace{\cos\left(\omega_{LO}t+\phi_{LO}\right)\cos\left(\omega_{rf}t\right)\sin\left(\omega_{rf}t\right)}_{=0} - 3X_i^2X_q\underbrace{\cos^2\left(\omega_{rf}t\right)\sin\left(\omega_{rf}t\right)}_{=0} +$$

$$3VbiasX_q^2\underbrace{\sin^2\left(\omega_{RF}t\right)}_{\frac{1}{2}[1+\cos(2\omega_{RF}t)]} + 3AloX_q^2\underbrace{\cos\left(\omega_{LO}t+\phi_{LO}\right)\sin^2\left(\omega_{RF}t\right)}_{=0} +$$

$$3X_iX_q^2\underbrace{\cos\left(\omega_{rf}t\right)\sin^2\left(\omega_{rf}t\right)}_{=0} - X_q^3\underbrace{\sin^3\left(\omega_{rf}t\right)}_{=0}$$

$$V_{1,3}(t) = \underbrace{Vbias^3 + \frac{3}{2}A_{LO}^2 Vbias}_{DC_{1,3}} + 3AloVbias\left[X_i\cos\left(\phi_{LO}\right) - X_q\sin\left(\phi_{LO}\right)\right] + \frac{3Vbias}{2}\left[X_i^2 + X_q^2\right]$$

$$V_{1,3}(t) = DC_{1,3} + 3AloVbias\left[X_i\cos\left(\phi_{LO}\right) - X_q\sin\left(\phi_{LO}\right)\right] + \frac{3Vbias}{2}\left[X_i^2 + X_q^2\right] \quad \text{(C.14)}$$

For simplicity let us rename $V_{(1,3)} = y_{3LPF}(t)$ and using Eq. C.11 and C.5 we can find the filter output signal expression:

$$y_{LPF}(t) = V_{1LPF}(t) = y_{2LPF}(t) + a_3 y_{3LPF}(t) \quad \text{(C.15)}$$

Adopting three phase $\left[\phi_1,\ \phi_2\ and\ \phi_3\right]$ for the oscillator an equation system similar to the one calculated for the case where L=2 is found:

$$M = \begin{pmatrix} (1 + 1.5a_3V_{bias}) & A_{LO}(1 - 3a_3V_{bias})\cos(\Theta_1) & -A_{LO}(1 + 3a_3V_{bias})\sin(\Theta_1) \\ (1 + 1.5a_3V_{bias}) & A_{LO}(1 - 3a_3V_{bias})\cos(\Theta_2) & -A_{LO}(1 + 3a_3V_{bias})\sin(\Theta_2) \\ (1 + 1.5a_3V_{bias}) & A_{LO}(1 - 3a_3V_{bias})\cos(\Theta_3) & -A_{LO}(1 + 3a_3V_{bias})\sin(\Theta_3) \end{pmatrix} \quad \text{(C.16)}$$

$$\vec{P} = \begin{pmatrix} P_1 - \left(V_{bias} + \frac{A_{LO}^2}{2} + a_3DC_{1,3}\right) \\ P_2 - \left(V_{bias} + \frac{A_{LO}^2}{2} + a_3DC_{1,3}\right) \\ P_3 - \left(V_{bias} + \frac{A_{LO}^2}{2} + a_3DC_{1,3}\right) \end{pmatrix} \quad \text{(C.17)}$$

and the values of the received in-phase and in-quadrature signals can be estimated by:

$$\hat{x} = \begin{pmatrix} \frac{\left(x_I^2(t) + x_Q^2(t)\right)}{2} \\ \hat{x}_I(t) \\ \hat{x}_Q(t) \end{pmatrix} = \begin{pmatrix} RSSI \\ \mathrm{I} \\ \mathrm{Q} \end{pmatrix} \quad \text{(C.18)}$$

The blue text are the extra values to be considered in Eq: C.8 and C.9 when a third-order polynomial is considered in the calculation.

C.1.4 Case where $L = 4$

At this section we will see the devastating changes in the system when a fourth-order polynomial is considered. This section will show that the matrix **M** needs to be enlarged. Let us start our analysis assuming that ξ_1 and ξ_2 are scalars less than one. Therefore, the non filtered voltage at the output of the diode will be:

$$V_1(t) = V_{diode} + [V_{diode}]^2 + a_3 [V_{diode}]^3 + a_4 [V_{diode}]^4 \tag{C.19}$$

with

$$V_{diode} = V_{bias} + K_{LO} V_{LO}(t) + r_s(t) \tag{C.20}$$

$$
\begin{aligned}
[V_{diode}]^4 = {} & Vbias^4 + 4AloVbias^3 \cos\left(\omega_{LO}t + \phi_{LO}\right) + 6Alo^2Vbias^2 \cos^2\left(\omega_{LO}t + \phi_{LO}\right) \\
& + 4Alo^3Vbias \cos^3\left(\omega_{LO}t + \phi_{LO}\right) + Alo^4 \cos^4\left(\omega_{LO}t + \phi_{LO}\right) \\
& 4Vbias^3X_i \cos\left(\omega_{RF}t\right) + 12AloVbias^2X_i \cos\left(\omega_{LO}t + \phi_{LO}\right)\cos\left(\omega_{RF}t\right) \\
& + 4Alo^3X_i \cos^3\left(\omega_{LO}t + \phi_{LO}\right)\cos\left(\omega_{RF}t\right) + 6Vbias^2X_i^2 \cos^2\left(\omega_{RF}t\right) \\
& + 12AloVbiasX_i^2 \cos\left(\omega_{LO}t + \phi_{LO}\right)\cos^2\left(\omega_{RF}t\right) \\
& + 6Alo^2X_i^2 \cos^2\left(\omega_{LO}t + \phi_{LO}\right)\cos^2\left(\omega_{RF}t\right) + 4V_{bias}X_i^3 \cos^3\left(\omega_{RF}t\right) \\
& + 4AloX_i^3 \cos\left(\omega_{LO}t + \phi_{LO}\right)\cos^3\left(\omega_{RF}t\right) + X_i^4 \cos^4\left(\omega_{RF}t\right) \\
& - 4Vbias^3X_q \sin\left(\omega_{RF}t\right) - 12AloVbias^2X_q \cos\left(\omega_{LO}t + \phi_{LO}\right)\sin\left(\omega_{RF}t\right) \\
& - 12Alo^2VbiasX_q \cos^2\left(\omega_{LO}t + \phi_{LO}\right)\sin\left(\omega_{RF}t\right) \\
& - 4Alo^3X_q \cos^3\left(\omega_{LO}t + \phi_{LO}\right)\sin\left(\omega_{RF}t\right) \\
& - 12Vbias^2X_iX_q \cos\left(\omega_{RF}t\right)\sin\left(\omega_{RF}t\right) \\
& - 24AloVbiasX_iX_q \cos\left(\omega_{LO}t + \phi_{LO}\right)\cos\left(\omega_{RF}t\right)\sin\left(\omega_{RF}t\right) \\
& - 12Alo^2X_iX_q \cos^2\left(\omega_{LO}t + \phi_{LO}\right)\cos\left(\omega_{RF}t\right)\sin\left(\omega_{RF}t\right) \\
& - 12VbiasX_i^2X_q \cos^2\left(\omega_{RF}t\right)\sin\left(\omega_{RF}t\right) \\
& - 12AloX_i^2X_q \cos\left(\omega_{LO}t + \phi_{LO}\right)\cos^2\left(\omega_{RF}t\right)\sin\left(\omega_{RF}t\right) \\
& - 4X_i^2X_q \cos^3\left(\omega_{RF}t\right)\sin\left(\omega_{RF}t\right) + 6Vbias^2X_q^2 \sin^2\left(\omega_{RF}t\right) \\
& + 12AloVbiasX_q^2 \cos\left(\omega_{LO}t + \phi_{LO}\right)\sin^2\left(\omega_{RF}t\right) \\
& + 6Alo^2X_q^2 \cos^2\left(\omega_{LO}t + \phi_{LO}\right)\sin^2\left(\omega_{RF}t\right) \\
& + 12VbiasX_iX_q^2 \cos\left(\omega_{RF}t\right)\sin^2\left(\omega_{RF}t\right) \\
& + 12AloX_iX_q^2 \cos\left(\omega_{LO}t + \phi_{LO}\right)\cos\left(\omega_{RF}t\right)\sin^2\left(\omega_{RF}t\right) \\
& + 6X_i^2X_q^2 \cos^2\left(\omega_{RF}t\right)\sin^2\left(\omega_{RF}t\right) - 4VbiasX_q^3 \sin^3\left(\omega_{RF}t\right) \\
& - 4AloX_q^3 \cos\left(\omega_{LO}t + \phi_{LO}\right)\sin^3\left(\omega_{RF}t\right) \\
& - 4X_iX_q^3 \cos\left(\omega_{RF}t\right)\sin^3\left(\omega_{RF}t\right) + X_q^4 \sin^4\left(\omega_{RF}t\right)
\end{aligned}
$$

In order to make our analysis more clear, we will split the above equation into three small ones and calculate its value after the filter.

$$[V_{diode}]^4 = V_{1,4a}(t) + V_{1,4b}(t) + V_{1,4c}(t) \tag{C.21}$$

$$V_{1,4a}(t) = Vbias^4 + 4AloVbias^3 \underbrace{\cos\left(\omega_{LO}t + \phi_{LO}\right)}_{=0} + 6Alo^2Vbias^2 \quad \underbrace{\cos^2\left(\omega_{LO}t + \phi_{LO}\right)}_{=\frac{1}{2}\left[1+\underbrace{\cos\left(2\omega_{LO}+2\phi\right)}_{=0}\right]}$$

$$+ 4Alo^3Vbias \underbrace{\cos^3\left(\omega_{LO}t + \phi_{LO}\right)}_{=0} + Alo^4 \quad \underbrace{\cos^4\left(\omega_{LO}t + \phi_{LO}\right)}_{\frac{3}{8}+\frac{3}{8}\underbrace{\cos\left(4\omega_{LO}t+4\phi_{LO}\right)}_{=0}}$$

$$+ 4Vbias^3X_i \underbrace{\cos\left(\omega_{RF}t\right)}_{=0} + 12AloVbias^2X_i \quad \underbrace{\cos\left(\omega_{LO}t + \phi_{LO}\right)\cos\left(\omega_{RF}t\right)}_{\frac{1}{2}\left[\cos(\phi)+\underbrace{\cos\left(\left(\omega_{LO}+\omega_{RF}\right)t+\phi_{LO}\right)}_{=0}\right]}$$

$$+ 12Alo^2VbiasX_i \underbrace{\cos^2\left(\omega_{LO}t + \phi_{LO}\right)\cos\left(\omega_{RF}t\right)}_{=0}$$

$$+ 4Alo^3X_i \quad \underbrace{\cos^3\left(\omega_{LO}t + \phi_{LO}\right)\cos\left(\omega_{RF}t\right)}_{\frac{1}{4}\left[1+\cos\left(2\omega_{LO}+2\phi_{LO}\right)\right]\left[\cos\left(\left(\omega_{LO}-\omega_{RF}t\right)-\phi_{LO}\right)+\cos\left(\omega_{LO}t+\omega_{RF}t+\phi_{LO}\right)\right]}$$

$$+ 6Vbias^2X_i^2 \quad \underbrace{\cos^2\left(\omega_{RF}t\right)}_{\frac{1}{2}+\frac{1}{2}\underbrace{\cos\left(2\omega_{RF}t\right)}_{=0}}$$

$$+ 12AloVbiasX_i^2 \underbrace{\cos\left(\omega_{LO}t + \phi_{LO}\right)\cos^2\left(\omega_{RF}t\right)}_{=0}$$

$$+ 6Alo^2X_i^2 \underbrace{\cos^2\left(\omega_{LO}t + \phi_{LO}\right)\cos^2\left(\omega_{RF}t\right)}_{\frac{1}{4}+\frac{1}{8}\cos\left(2\phi\right)} + 4V_{bias}X_i^3 \underbrace{\cos^3\left(\omega_{RF}t\right)}_{=0}$$

$$+ 4AloX_i^3 \underbrace{\cos\left(\omega_{LO}t + \phi_{LO}\right)\cos^3\left(\omega_{RF}t\right)}_{=\frac{3}{8}\cos\left(\phi\right)} + X_i^4 \underbrace{\cos^4\left(\omega_{RF}t\right)}_{=\frac{3}{2}}$$

$$- 4Vbias^3X_q \underbrace{\sin\left(\omega_{RF}t\right)}_{=0} - 12AloVbias^2X_q \quad \underbrace{\cos\left(\omega_{LO}t + \phi_{LO}\right)\sin\left(\omega_{RF}t\right)}_{\underbrace{\cos\left(\omega_{LO}t + \phi_{LO}\right)\cos\left(\omega_{RF}t + \frac{\pi}{2}\right)}_{-\frac{1}{2}\sin\left(\phi_{LO}\right)}}$$

$$- 12Alo^2VbiasX_q \cos^2\left(\omega_{LO}t + \phi_{LO}\right)\sin\left(\omega_{RF}t\right)$$

$$
\begin{aligned}
V_{1,4a}(t) = {} & Vbias^4 + 0 + 6Alo^2Vbias^2\frac{1}{2} + \frac{3}{8}Alo^4 \\
& + 12AloVbias^2X_i\frac{1}{2}\cos\left(\phi\right) \\
& + 4Alo^3X_i \underbrace{\cos^3\left(\omega_{LO}t + \phi_{LO}\right)\cos\left(\omega_{RF}t\right)}_{\underbrace{\frac{1}{4}\left[1+\cos\left(2\omega_{LO}+2\phi_{LO}\right)\right]\left[\cos\left(\phi_{LO}\right)+\cos\left(\omega_{LO}t+\omega_{RF}t+2\phi_{LO}\right)\right]}_{\frac{1}{4}\left[\cos\left(\phi_{LO}\right)+\cos\left(2\phi_{LO}-2\phi_{LO}\right)\right]}} \\
& + 6Vbias^2X_i^2\frac{1}{2} \\
& + 6Alo^2X_i^2\left[\frac{1}{4}+\frac{1}{8}\cos\left(2\phi\right)\right] \\
& + 4AloX_i^3\frac{3}{8}\cos\left(\phi\right) + X_i^4\frac{3}{2} \\
& - 12AloVbias^2X_q\left[-\frac{1}{2}\sin\left(\phi_{LO}\right)\right] \\
& - 4Alo^3X_q \underbrace{\cos^3\left(\omega_{LO}t + \phi_{LO}\right)\sin\left(\omega_{RF}t\right)}_{\underbrace{\frac{1}{4}\left[\left(1+\cos\left(2\omega_{LO}+2\phi_{LO}\right)\right)\left(\cos\left(\left(\omega_{LO}+\omega_{RF}\right)t+\phi_{LO}+\frac{\pi}{2}\right)+\cos\left(\phi_{LO}-\frac{\pi}{2}\right)\right)\right]}_{\underbrace{\frac{1}{4}\left[cos\left(\phi_{LO}-\frac{\pi}{2}\right)+\frac{1}{2}cos\left(2\phi_{LO}-\phi_{LO}-\frac{\pi}{2}\right)\right]}_{-\frac{3}{8}\sin\left(\phi_{LO}\right)}}}
\end{aligned}
$$

$$
\begin{aligned}
V_{1,4a}(t) = {} & Vbias^4 + 3Alo^2Vbias^2 + \frac{3}{8}Alo^4 \\
& + 6AloVbias^2X_i\cos\left(\phi\right) + 2Alo^3X_i\cos\left(\phi_{LO}\right) \\
& + 3Vbias^2X_i^2 + 6Alo^2X_i^2\left[\frac{1}{4}+\frac{1}{8}\cos\left(2\phi\right)\right] \\
& + \frac{3}{2}AloX_i^3\cos\left(\phi\right) + \frac{3}{2}X_i^4 \\
& - 12AloVbias^2X_q\left[-\frac{1}{2}\sin\left(\phi_{LO}\right)\right] + \frac{3}{2}Alo^3X_q\sin\left(\phi_{LO}\right)
\end{aligned}
$$

$$
\begin{aligned}
V_{1,4b}(t) = & -12Vbias^2X_iX_q \underbrace{\cos(\omega_{RF}t)\sin(\omega_{RF}t)}_{=0} \\
& -24AloVbiasX_iX_q \underbrace{\cos\left(\omega_{LO}t+\phi_{LO}\right)\cos(\omega_{RF}t)\sin(\omega_{RF}t)}_{=0} \\
& -12Alo^2X_iX_q \underbrace{\underbrace{\cos^2\left(\omega_{LO}t+\phi_{LO}\right)}_{\left[\frac{1}{2}+\frac{1}{2}\cos\left(2\omega_{LO}t+2\phi_{LO}\right)\right]} \underbrace{\cos(\omega_{RF}t)\sin(\omega_{RF}t)}_{\left[\frac{1}{2}cos\left(2\omega_{RF}t+\frac{\pi}{2}\right)+\frac{1}{2}cos\left(-\frac{\pi}{2}\right)\right]}}_{-\frac{1}{8}\sin\left(2\phi_{LO}\right)} \\
& -12VbiasX_i^2X_q \underbrace{\cos^2(\omega_{RF}t)\sin(\omega_{RF}t)}_{=0} \\
& -12AloX_i^2X_q \underbrace{\underbrace{\cos\left(\omega_{LO}t+\phi_{LO}\right)\cos^2(\omega_{RF}t)\sin(\omega_{RF}t)}_{\frac{1}{4}\left[\cos\left(\omega_{LO}t+\omega_{RF}t+\phi_{LO}\right)+\cos\left(\phi_{LO}\right)\right]\left[1+\cos(2\omega_{RF}t)\right]}}_{\frac{3}{8}\cos(\phi_{LO})} \\
& -4X_i^2X_q \underbrace{\underbrace{\cos^3(\omega_{RF}t)\sin(\omega_{RF}t)}_{\frac{1}{4}(1+\cos(2\omega_{RF}t))\left(\cos\left(2\omega_{RF}t+\frac{\pi}{2}\right)+\cos\left(-\frac{\pi}{2}\right)\right)}}_{=0} \\
& +6Vbias^2X_q^2 \underbrace{\sin^2(\omega_{RF}t)}_{=\frac{1}{2}} \\
& +12AloVbiasX_q^2 \underbrace{\cos\left(\omega_{LO}t+\phi_{LO}\right)\sin^2(\omega_{RF}t)}_{=0} \\
& +6Alo^2X_q^2 \underbrace{\underbrace{\cos^2\left(\omega_{LO}t+\phi_{LO}\right)}_{\frac{1}{4}\left[1+\cos\left(2\omega_{LO}t+2\phi\right)\right]} \underbrace{\sin^2(\omega_{RF}t)}_{[1+\cos(2\omega_{RF}t+\pi)]}}_{\frac{1}{4}-\frac{1}{8}\cos\left(2\phi\right)}
\end{aligned}
$$

$$V_{1,4b}(t) = -12Alo^2X_iX_q\left(-\frac{1}{8}\sin\left(2\phi_{LO}\right)\right) - 12AloX_i^2X_q\frac{3}{8}\cos\left(\phi_{LO}\right) + 3Vbias^2X_q^2 + 6Alo^2X_q^2\left[\frac{1}{4} - \frac{1}{8}\cos\left(2\phi\right)\right]$$

$$\begin{aligned}
V_{1,4c}(t) = {} & +12VbiasX_iX_q^2\underbrace{\cos\left(\omega_{RF}t\right)\sin^2\left(\omega_{RF}t\right)}_{=0} \\
& + 12AloX_iX_q^2\underbrace{\cos\left(\omega_{LO}t+\phi_{LO}\right)\cos\left(\omega_{RF}t\right)}_{\left[\frac{1}{2}\cos\left(\omega_{LO}t+\omega_{RF}t+\phi_{LO}\right)+\frac{1}{2}\cos\left(\omega_{LO}t-\omega_{RF}t+\phi_{LO}\right)\right]}\underbrace{\sin^2\left(\omega_{RF}t\right)}_{\left[\frac{1}{2}+\frac{1}{2}\cos\left(2\omega_{RF}t+\pi\right)\right]} \\
& \qquad = \tfrac{1}{8}\cos\left(\phi\right) \\
& + 6X_i^2X_q^2\underbrace{\cos^2\left(\omega_{RF}t\right)\sin^2\left(\omega_{RF}t\right)}_{\left(\frac{1}{2}+\frac{1}{2}\cos\left(2\omega_{RF}t\right)\right)\left(\frac{1}{2}+\frac{1}{2}\cos\left(2\omega_{RF}t+\pi\right)\right)} - 4VbiasX_q^3\underbrace{\sin^3\left(\omega_{RF}t\right)}_{=0} \\
& \qquad = \tfrac{1}{8} \\
& - 4AloX_q^3\underbrace{\cos\left(\omega_{LO}t+\phi_{LO}\right)\sin^3\left(\omega_{RF}t\right)}_{\frac{1}{4}\left[\cos\left(\phi_{LO}-\frac{\pi}{2}\right)+\cos\left(\left(\omega_{LO}+\omega_{RF}\right)t+\phi_{LO}+\frac{\pi}{2}\right)\right]\left[1+\cos\left(2\omega_{RF}t+\pi\right)\right]} \\
& \qquad -\tfrac{3}{8}\sin(\phi_{LO}) \\
& - 4X_iX_q^3\underbrace{\cos\left(\omega_{RF}t\right)\sin^3\left(\omega_{RF}t\right)}_{\frac{1}{4}\left[\underbrace{\cos\left(-\frac{\pi}{2}\right)}_{=0}+\cos\left(2\omega_{RF}t-\frac{\pi}{2}\right)\right]\left[1+\cos\left(2\omega_{RF}t+\pi\right)\right]} + X_q^4\sin^4\left(\omega_{RF}t\right) \\
& \qquad \left[\cos\left(2\omega_{RF}t+\tfrac{\pi}{2}\right)+\tfrac{1}{2}\left(\cos\left(-\tfrac{\pi}{2}\right)+\cos\left(\omega_{RF}t+\tfrac{3\pi}{2}\right)\right)\right]
\end{aligned}$$

$$
\begin{aligned}
V_{1,4c}(t) = {} & +12AloX_iX_q^2\left[\frac{1}{8}\cos\left(\phi\right)\right] + \frac{6}{8}X_i^2X_q^2 \\
& - 4AloX_q^3\left[-\frac{3}{8}\sin\left(\phi_{LO}\right)\right] \\
& - 4X_iX_q^3\underbrace{\left[\left[\cos\left(2\omega_{RF}t+\frac{\pi}{2}\right)+\frac{1}{2}\left(\cos\left(-\frac{\pi}{2}\right)+\cos\left(\omega_{RF}t+\frac{3\pi}{2}\right)\right)\right]\right]}_{=0} \\
& + X_q^4 \qquad \underbrace{\sin^4\left(\omega_{RF}t\right)}_{} \\
& \qquad \underbrace{\frac{1}{4}\left[1+\cos\left(w\omega_{RF}t+\pi\right)\right]^2}_{=\frac{3}{2}}
\end{aligned}
$$

$$
\begin{aligned}
V_{1,4c}(t) = {} & +12AloX_iX_q^2\frac{1}{8}\cos\left(\phi\right) + \frac{6}{8}X_i^2X_q^2 \\
& + 4AloX_q^3\left[\frac{3}{8}\sin\left(\phi_{LO}\right)\right] \\
& + \frac{3}{2}X_q^4
\end{aligned}
$$

$$
V_{1,3} = V_{1,4a}(t) + V_{1,4b}(t) + V_{1,4c}(t) \tag{C.22}
$$

$$
\begin{aligned}
V_{1,4}(t) = {} & Vbias^4 + 3Alo^2Vbias^2 + \frac{3}{8}Alo^4 \\
& + 6AloVbias^2X_i\cos\left(\phi\right) + 2Alo^3X_i\cos\left(\phi_{LO}\right) \\
& + 3Vbias^2X_i^2 + 6Alo^2X_i^2\left[\frac{1}{4} + \frac{1}{8}\cos\left(2\phi\right)\right] \\
& + \frac{3}{2}AloX_i^3\cos\left(\phi\right) + \frac{3}{2}X_i^4 \\
& + 6AloVbias^2X_q\sin\left(\phi_{LO}\right) + \frac{3}{2}Alo^3X_q\sin\left(\phi_{LO}\right) \\
& - \frac{3}{2}Alo^2X_iX_q\left(\sin\left(2\phi_{LO}\right)\right) - 12AloX_i^2X_q\frac{3}{8}\cos\left(\phi_{LO}\right) \\
& - 3Vbias^2X_q^2 + 6Alo^2X_q^2\left[\frac{1}{4} - \frac{1}{8}\cos\left(2\phi\right)\right] \\
& + 12AloX_iX_q^2\frac{1}{8}\cos\left(\phi\right) + \frac{6}{8}X_i^2X_q^2 \\
& + \frac{3}{2}AloX_q^3\sin\left(\phi_{LO}\right) + \frac{3}{2}X_q^4
\end{aligned}
$$

$$
\begin{aligned}
V_{1,4}(t) = & \underbrace{Vbias^4 + 3Alo^2Vbias^2 + \frac{3}{8}Alo^4}_{K_1} \\
& + \underbrace{\left[6AloVbias^2 + 2Alo^3\right]}_{K_2} X_i \cos\left(\phi_{LO}\right) \\
& + \left[\underbrace{3Vbias^2 + 6Alo^2\frac{1}{4}}_{K_0} + \frac{1}{8}\cos\left(2\phi\right)\right] X_i^2 \\
& + \frac{3}{2}AloX_i^3\cos\left(\phi\right) + \frac{3}{2}X_i^4 \\
& + \underbrace{\left[6AloVbias^2 + \frac{3}{2}Alo^3\right]}_{K_3} X_q \sin\left(\phi_{LO}\right) \\
& - \frac{3}{2}Alo^2X_iX_q\sin\left(2\phi_{LO}\right) - 12AloX_i^2X_q\frac{3}{8}\cos\left(\phi_{LO}\right) \\
& + \left[\underbrace{3Vbias^2 + 6Alo^2\frac{1}{4}}_{K_0} - \frac{1}{8}\cos\left(2\phi\right)\right] X_q^2 \\
& + \frac{3}{2}AloX_iX_q^2\cos\left(\phi\right) + \frac{6}{8}X_i^2X_q^2 \\
& + \frac{3}{2}AloX_q^3\sin\left(\phi_{LO}\right) + \frac{3}{2}X_q^4
\end{aligned}
$$

$$
M_{2,3} = \begin{pmatrix}
(1 + 3\xi V_{bias}) & A_{LO}\,(1 + 3\xi V_{bias})\cos(\phi_1) & -A_{LO}\,(1 + 3\xi V_{bias})\sin(\phi_1) \\
(1 + 3\xi V_{bias}) & A_{LO}\,(1 + 3\xi V_{bias})\cos(\phi_2) & -A_{LO}\,(1 + 3\xi V_{bias})\sin(\phi_2) \\
(1 + 3\xi V_{bias}) & A_{LO}\,(1 + 3\xi V_{bias})\cos(\phi_3) & -A_{LO}\,(1 + 3\xi V_{bias})\sin(\phi_3)
\end{pmatrix} \tag{C.23}
$$

The next equation is the **M** equation for forth-order only

$$M_4 = \begin{bmatrix} K_0 & K_2\cos(\phi_1) & K_1\sin(\phi_1) & \frac{1}{4}\cos\left(2\phi_1\right) & \frac{3}{2}\cos\left(\phi_1\right) & \frac{3}{2}\sin\left(\phi_1\right) & \frac{3}{2} & \frac{3}{2}\sin\left(2\phi_1\right) & kk & \frac{3}{2} \\ K_0 & K_2\cos(\phi_2) & K_1\sin(\phi_2) & \frac{1}{4}\cos\left(2\phi_2\right) & \frac{3}{2}\cos\left(\phi_2\right) & \frac{3}{2}\sin\left(\phi_1\right) & \frac{3}{2} & \frac{3}{2}\sin\left(2\phi_2\right) & kk & \frac{3}{2} \\ \vdots & & & & & \ddots & & & & \vdots \\ K_0 & K_2\cos(\phi_N) & K_1\sin(\phi_N) & \frac{1}{4}\cos\left(2\phi_N\right) & \frac{3}{2}\cos\left(\phi_1\right) & \frac{3}{2}\sin\left(\phi_N\right) & \frac{3}{2} & \frac{3}{2}\sin\left(2\phi_N\right) & kk & \frac{3}{2} \end{bmatrix} \tag{C.24}$$

To precisely solve the system the final **M** matrix shall be a 10×10 size matrix.

$$\vec{P} = \begin{pmatrix} P_1 - \left(V_{bias} + \frac{A_{LO}^2}{2} + \xi DC_{1,3} + K_1\right) \\ P_2 - \left(V_{bias} + \frac{A_{LO}^2}{2} + \xi DC_{1,3} + K_1\right) \\ P_3 - \left(V_{bias} + \frac{A_{LO}^2}{2} + \xi DC_{1,3} + K_1\right) \\ \vdots \\ P_{10} - \left(V_{bias} + \frac{A_{LO}^2}{2} + \xi DC_{1,3} + K_1\right) \end{pmatrix} \tag{C.25}$$

and the estimation of the in-phase and in-quadrature received signals can be estimated by using:

$$\hat{x} = \begin{pmatrix} \frac{\left(x_I^2(t)+x_Q^2(t)\right)}{2} \\ x_I(t) \\ x_Q(t) \\ \frac{\left(x_I^2(t)-x_Q^2(t)\right)}{2} \\ x_I^3(t) \\ x_Q^3(t) \\ x_I^4(t) + x_Q^4(t) \\ x_I(t)x_Q(t) \\ yy \\ x_I^2(t)x_Q^2(t) \end{pmatrix} \tag{C.26}$$

C.2 Algorithm Error Analysis

In the last section we calculate the system matrix for second, third and forth-order diode operation regions. The Simulink model as it is today, calculates the values of I and Q based on the second-order power detector matrix or transformation matrix $\mathbf{M_3}$

as given bellow:

$$\mathbf{M} = \begin{pmatrix} 1 & A_{LO}\cos(\Theta_1) & -A_{LO}\sin(\Theta_1) \\ 1 & A_{LO}\cos(\Theta_2) & -A_{LO}\sin(\Theta_2) \\ 1 & A_{LO}\cos(\Theta_3) & -A_{LO}\sin(\Theta_3) \end{pmatrix} \tag{C.27}$$

With its associated power vector is given by:

$$\vec{P} = \begin{pmatrix} P_1 - V_{bias} - \frac{A_{LO}^2}{2} \\ P_2 - V_{bias} - \frac{A_{LO}^2}{2} \\ P_3 - V_{bias} - \frac{A_{LO}^2}{2} \end{pmatrix} \tag{C.28}$$

If we consider higher-order power detectors (e.g., $n = 3$) in Eq. C.1 and let call $\mathbf{M}_3$ the system matrix derived from the third-order operation region.

$$\mathbf{M}_3 = \begin{pmatrix} \xi & A_{LO}\xi_1\cos(\Theta_1) & -A_{LO}\xi_2\sin(\Theta_1) \\ \xi & A_{LO}\xi_1\cos(\Theta_2) & -A_{LO}\xi_2\sin(\Theta_2) \\ \xi & A_{LO}\xi_1\cos(\Theta_3) & -A_{LO}\xi_2\sin(\Theta_3) \end{pmatrix} \tag{C.29}$$

Where $\xi = (1 + 1.5a_3V_{bias})$, $\xi_1 = (1 + 3a_3V_{bias})$, $\xi_2 = (1 - 3a_3V_{bias})$ and $\xi_3 = a_3\left(V_{bias}^3 + 1.5V_{bias}A_{LO}\right)$

$$DC_{1,3} = V_{bias}^3 + 1.5V_{bias}A_{LO}^2 \tag{C.30}$$

With has its associated power vector is given by:

$$\vec{P_3} = \begin{pmatrix} P_1 - \left(V_{bias} + \frac{A_{LO}^2}{2} + a_3DC_{1,3}\right) \\ P_2 - \left(V_{bias} + \frac{A_{LO}^2}{2} + a_3DC_{1,3}\right) \\ P_3 - \left(V_{bias} + \frac{A_{LO}^2}{2} + a_3DC_{1,3}\right) \end{pmatrix} = \begin{pmatrix} P_1 - \left(V_{bias} + \frac{A_{LO}^2}{2}\right) \\ P_2 - \left(V_{bias} + \frac{A_{LO}^2}{2}\right) \\ P_3 - \left(V_{bias} + \frac{A_{LO}^2}{2}\right) \end{pmatrix} - \xi_3 \tag{C.31}$$

We can write the following relationship between Eq. C.31 and C.28. Those are power vectors derived from second and third-order operation regions.

$$\vec{P}_3 = \vec{P} - \xi_3 \tag{C.32}$$

and similarly the estimate values for in-phase and quadrature signals can be calculated as:

$$\hat{x} = \begin{pmatrix} \frac{\left(x_I^2(t) + x_Q^2(t)\right)}{2} \\ \hat{x}_I(t) \\ \hat{x}_Q(t) \end{pmatrix} = \begin{pmatrix} RSSI \\ \mathrm{I} \\ \mathrm{Q} \end{pmatrix} \tag{C.33}$$

Once the model in Simulink calculates the values of I and Q using a second-order diode law, the algorithm will introduce less or minimal error if the diode operates on a second-order region. Therefore, in this case we call it the optimum solution $\hat{x}_{opt}$. The optimizer in 4.1 is the block responsible to keep the diode operating on a second-order region. This happen by find a V_{bias} that will result in a minimum EVM.

Appendix D

MatLab Scripts

This file shows the Matlab script used to initialize the variables used by *Simulink* model.

```
    clc
close all
clear all
%************************************************************************
%********************** Transmitter set up ****************************
M =64 ; % Modulation Index
Fs = 4e6 ; % Sampling frequency
Ts=1/Fs;
Pt = 1 ; % Transmitted power in Watts
Freq_LO_Tx = 760e6;
FUS=8;
RFAtt=1; %This attenuator is located just after the Tx output
RFAtt1 =1; %This attenuator is located after the AWGN block
FUS_LO = 4; % LO Frequency up-sampling factor.  Each LO period will have FUS samples
Freq_LO_Rx = Freq_LO_Tx;
Freq_LO_Tx1 =Freq_LO_Tx +40e6;
RRCFilt_Inp_SamplingPerSymb = Freq_LO_Tx*FUS_LO/Fs;
RRC_Rx_Filt_DownsamplinFactor = Freq_LO_Tx*FUS_LO/(FUS*Fs);
%************************************************************************
%********************** Channel set up ********************************
```

```
SNR_dB=46.0 % SNR in dBs
A = 1/100 %Channel attenuation
Pr = A*Pt %Received power
%*********************************************************************
%******************** Tx RF Filter specifications ***********************
Roll_Off = 0.5
FilterOrder = 8;
Freq_low = Freq_LO_Tx - (Fs/2)*(1+Roll_Off);
Freq_High = Freq_LO_Tx + (Fs/2)*(1+Roll_Off);
FiltRipple = 0.2;
StopBandAtt = 40;
%*********************************************************************
%********************* Spectrum Display ********************************
% This parameters will set the spectrum display
y_min = -100
y_max = -20
Freq_min = -5*Fs+Freq_LO_Tx
Freq_max = 5*Fs+Freq_LO_Tx
%*********************************************************************
%********** Six port set up Parameter Set up*****************************

%****************** Splitters Insertion Loss ***************************
Splitter_IL = 0.25 % Splitters Insertion Loss

%******************* Couplers factor ***********************************
CoupFact = 0.1;
%*********************************************************************
%******************** Diode Model ************************************
DiodeTypeSel = 0;
% When = 0 will use second order ideal model
% When = 1 will use Winner model with polynomial of order 13
% When = 2 will use HP HSMS286 modelp
% When = 3 will use Winner model with polynomial of order 10
% When = 4 will use BAS125 Siemens diode model with polynomial of order 13
% When = 7 will use Winner model with polynomial of order 5
```

```
% When = 8 will use Winner model with polynomial of order 3
    if DiodeTypeSel == 1
        Vdiode_0 =0.95;
        % When = 1 will use Winner model polynomial of order 13
    elseif DiodeTypeSel == 2
        Vdiode_0 =0.43; % HSMS286 Diode
        % When = 2 will use HP HSMS286 model polynomial of order 13
    elseif DiodeTypeSel == 3
        Vdiode_0 =0.95;
        % When = 3 will use Winner model polynomial of order 10
    elseif DiodeTypeSel == 4
        Vdiode_0 =0.37; % This needs update this is the initial
        %value but not the optimum.
        % When = 4 will use BAS125 model polynomial of order 13
    elseif DiodeTypeSel == 5
        Vdiode_0 =0.37; % This needs update this is the initial
        %value but not the optimum.
        % When = 4 will use BAS125 model polynomial of order 13
    elseif DiodeTypeSel == 6
        %Vdiode_0 = 0.44;
        Vdiode_0 = 0.51;
        %value but not the optimum.
        % When = 6 will use Hitachi model polynomial of order 13
    elseif DiodeTypeSel == 7
        Vdiode_0 =0.95;
        % When = 3 will use Winner model polynomial of order 5
    elseif DiodeTypeSel == 8
        Vdiode_0 =0.95;
        % When = 3 will use Winner model polynomial of order 3
    else
        Vdiode_0 =0.95;
        % When = 0 will use second order ideal model
     end

DiodeSweepStartVoltage = 0.94;
```

```
DiodeSweepEndVoltage = 0.95;
DiodevoltageSweepStep = .05;
Vdiode_x=DiodeSweepStartVoltage:DiodevoltageSweepStep:DiodeSweepEndVoltage;
TotalNumbIterations = (DiodeSweepEndVoltage - DiodeSweepStartVoltage)/DiodevoltageSweepSte
%*********************************************************************
%****************** Local Oscillator Amplitude *************************
ALo=1;
Alo = 1;
Const1= Alo*CoupFact;
% ************* Local Oscillator four Phases *************************
ErrorDeg = 0; % Value of the phase error which is equal to all phases
error = ErrorDeg*pi/180;
Phi_0 = pi/4 -error;
Phi_1 = Phi_0+pi/2 +error;
Phi_2 = Phi_1+ pi/2 -error;
Phi_3 = Phi_2+ pi/2 +error;

%*********************************************************************
%******************* LINEAR SYSTEM MATRIX ******************************
M1 =[ 1 CoupFact*ALo*cos(Phi_0) -CoupFact*ALo*sin(Phi_0); ...
1 CoupFact*ALo*cos(Phi_1) -CoupFact*ALo*sin(Phi_1); ...
1 CoupFact*ALo*cos(Phi_2) -CoupFact*ALo*sin(Phi_2)];

D = inv(M1); % Inverse of Matrix (Brute Force solution) The good thing is
% because this inverse needs to be calculated only once

%***************** End of Six-Port Parameters set up ********************
%*********************************************************************
%*********************************************************************

%EVM Buffer size calculation for display purpose only
if Fs == 10e6
        EVM_Buffer = 200;
else
        EVM_Buffer = 400;
```

```
end

%*********************************************************************
%************** DIODE VOLTAGE OPTIMIZATION PARAMETERS SETTING %**********
Ts_Opt = 2*1e-6;
OPT_Step = 0.01
Error_Max = 0.001;
%*********************************************************************
ParametricSimyulationFlag = 0; %ParametricSimulation Flag when equal to ONE
        %it will enter into parametric simulation loop
        % The parametric simulation can be on the
        % diode voltage, LO power, input signal
        % amplitude or memory effect
VdiodeParSim = 0; % When equal to one it will perform parametric
        % simulation on the diode voltage
ParVdiodeOptFlag = 1;

Sel_Optim = 0; % When equal to One,the model will use Diode voltage optimizer

    LOampFlag = 0; % When equal to One,during parametric simulation, the model
% will vary the LO amplitude

RFAttFlag = 0; % When equal to One,during parametric simulation, the model
% will vary the RF input signal amplitude

MemoryEffectFlag = 0; % Model uses diode with Memory

%*********************************************************************
%Selecting the Model Name
%mdl = 'SixPortModel_July20_2014.mdl';
%mdl = 'SixPortModel_August11_2014.mdl';
%mdl = 'SixPortModel_January08_2015.mdl';
%mdl = 'SixPortModel_January10_2015.mdl'
%mdl = 'SixPortModel_February05_2015.mdl';
%mdl = 'SixPortModel_February22_2015.mdl';
```

```
%mdl = 'SixPortModel_March13_2015.mdl';
mdl = 'SixPortModel_June08_2015.mdl';
%mdl = 'SixPortModel_Nov02_2015.mdl';

%**********************************************************************
%************ Starting Parametric Simulation ****************************

if ParametricSimyulationFlag == 1

                if VdiodeParSim == 0 %This means that the diode voltage will be
constant
            % It will perform parametric simulation either on LO Amplitude or RF
attenuation
         % This simulation will use the optimum value of voltages for the selected
         % diode

    if LOampFlag == 1 % It will vary the LO power %*************************************************
%*************** Parametric for LO Level %***************
        open_system(mdl); % Opening the model
        LO_Amp_x = .1:.1:1;

        for i = 1:length(LO_Amp_x)
           Alo = LO_Amp_x(i);
           [t, x, y] = sim(mdl);
           plot(t*1e3,y(:,1));
           hold on;
           grid on
           xlabel('Time (ms)')
           ylabel('EVM (                if i == 1
              testVec = find(t¿2.8e-3);
              ObsIndex = testVec(1);
              ObsTime = t(ObsIndex);
           else
              % DO NOTHING
           end
```

```
            VecSamp1(i) = [y(ObsIndex,1)];
            %VecSamp2(i) = [y(ObsIndex,2)];
clc
        end
LoPower = 10*log10((CoupFact*LO_Amp_x)/2*sqrt(2));
figure(2)
p=plot(LO_Amp_x', LoPower');
title('SNR versus Diode Voltages')
xlabel('Vdiode (Volts)');
ylabel('EVM')
grid on
set(p,'Color','red','LineWidth',2)

        elseif RFAttFlag == 1
%*************************************************************
%***************** Parametric for RF Level %***************

        open_system(mdl); % Opening the model
        RFAtt_x = 20:-1:1;
        Gain_x = 1:1:5;
        Gainy = [Gain_x];

    for i = 1:length(Gainy)
        RFAtt =Gainy(i);
        [t, x, y] = sim(mdl);
        figure(1)
        plot(t*1e 3,y(:,1));
        hold on;
        grid on
        xlabel('Time (ms)')
        ylabel('EVM (         if i == 1
        testVec = find(t¿2.8e-3);
        ObsIndex = testVec(1);
        ObsTime = t(ObsIndex);
     else
```

```
            % DO NOTHING
        end
 VecSamp1(i) = [y(ObsIndex, 1)];
 Calculated'_EVM=VecSamp1;
 clc

end
RFPower = Pt.*Gain;
figure(2)
p=plot(RFPower',Calculated_EVM')
title('SNR versus Input Signal Power')
xlabel('Imput Power ');
ylabel('SNR')
grid on
set(p,'Color','red','LineWidth',2)
%***********************************************************
%***********************************************************
else
% Do Nothing
end
 else
     % It will perform parametric simulation on diode's voltage.        % It will change
the diode voltage from a start and stop voltage.        % Store the EVM at certain time
and diode voltage        % It will plot the EVM function of diode's voltage
      if ParVdiodeOptFlag == 1
     open_system(mdl); % Opening the model
%*********************************************************************
%************* Modification on Feb 05 2015 ***********************
%************ Add this comment on Feb 05 2014 %**********************

     for i = 1:length(Vdiode_x)
         Vdiode_0 = Vdiode_x(i);
         [t, x, y] = sim(mdl);
         figure(1)
         plot(t*1e3,y(:,1));
```

```
        hold on;
        grid on
        xlabel('Time (ms)')
        ylabel('EVM (            if i == 1
           testVec = find(t¿2.8e-3);
           ObsIndex = testVec(1);
           ObsTime = t(ObsIndex);
        else
           % DO NOTHING
        end
        VecSamp1(i) = [y(ObsIndex,1)];
        clc
        TotalNumbIterations
        iteraction = i

    end
    figure(2)
    p=plot(Vdiode_x', VecSamp1')
    title('SNR versus Diode Voltages')
    xlabel('Vdiode (Volts)');
    %legend('MeanI')
    ylabel('SNR')
    grid on
    set(p,'Color','red','LineWidth',2)
else
    open_system(mdl); % Openning the model
    for i = 1:length(VdiodeSweep)
        Vdiode_0 = VdiodeSweep(i);
        [t, x, y] = sim(mdl);
        plot(t*1e3,y);
        hold on;
        grid on
        xlabel('Time (ms)')
        ylabel('DC offset (Volts)')
        if i == 1
```

```
            testVec = find(t¿2.98e-3);
            ObsIndex = testVec(1);
            ObsTime = t(ObsIndex);
        else
            % DO NOTHING
        end
        VecSamp1(i) = [y(ObsIndex,1)];
        VecSamp2(i) = [y(ObsIndex,2)];
        clc
        k=0.8/0.01;
        i
    end
    figure(2)
    p=plot(VdiodeSweep', VecSamp1', VdiodeSweep', VecSamp2')
    title('I&Q DC OFFSET versus Vdiode')
    xlabel('Vdiode (Volts)');
    legend('MeanI','MeabQ')
    ylabel('DC Offset (Volts')
    grid on
    set(p,'Color','red','LineWidth',2)
 end
end

saveDataFlag = 0;

    if saveDataFlag == 1
        Output=[VdiodeSweep' VecSamp1' VecSamp2']
        xlswrite('Vdiode2',Output)
    end
else
open_system(mdl); % Opening the model
end
```

Appendix E

Communications System Model - Simulink

E.1 Introduction

In the last chapters, we presented how the performance of *EVM* is affected with contamination of **M** due to nonlinearities, calibration and frequency response of the system. Mitigation options for this effect were also presented by using an optimization algorithm that finds the best bias point for the diodes. We also presented the estimation of the initial value of the diode bias point for the optimizer. Chapter 9 provides the validation methodology and the validation results of the model presented in this Appendix. To perform the Simulink model validation the work from [48] was selected. This appendix will provide in depth information about the system model developed in Simulink. A single-carrier Multi-Port (five-port) transceiver is modeled using Simulink native blocks. These blocks were built either using embedded Matlab or higher level blocks were built from Simulink native and embedded Matlab. The metric used to analyze the performance of the Multi-Port receiver is the *EVM*. This model brings other types of simulation results such as: *BER*, Eye diagram and frequency spectrum from several points inside the receiver chain in addition to the constellation diagram and *EVM*. The model also has capabilities to run parametric simulation for many variables (e.g., diode bias voltage, LO phase uncertainty, LO and received signals amplitude variation, etc.) To set the simulation parameters, a Matlab script is made available. The script has also the option to start the simulation by itself without the need to open Simulink; it does so automatically.

E.2 Setting the Simulation

A script is made available for the user to set the type of simulation desired to be run. The model can run either in parametric or non-parametric simulation modes. It can also run by either using ideal or already modeled off the shelf diodes (e.g., HP, Siemens, Hitachi, etc.). It also provides the capability to add new diodes and test them using different polynomial curve fitting (e.g., Order = 9,10, ... 14); see Chapter 5 for details. Table E.1 presents the variables that can be set to run parametric simulation. These variables can be set independently (one by one) or the user can set to run more than one variable during the same simulation.

Table E.1: Simulation Variable

Variable	Limits	Comments
Vbias	0 to 1.5 Volts	Typical
LO power	-20 to 0 dBm	Typical values but easily modified in the script
RF Power	-30 to 0 dBm	Limited by the BB AGC
LO Phase error	±5°	Typical but it can also be set for different values using the script
Modulation Type	QPSK, 16 adn 64QAM	Can be easily changed
LO Phase error	Up to 20 MSPS	

E.3 Top Level

The model's top level block can be divide into two sections: The transmitter (*Tx*) and the Multi-Port receiver (*Rx*). The system is shown in Fig. E.1. The transmitter is a single carrier transmitter. Adjacent channels can be added by replicating the transmitter and changing its *LO* frequency as well as amplitude to the desired level of interest. An *AWGN* channel from Simulink native block was added to the transmitter. The output of the channel is an observation point where the Spectrum analyzer is connected to the *AWGN* output and to the input of the receiver block. Notice that once this is a behavioral model, neither the spectrum analyzer nor the receiver block will load the channel. The transmitter also has another couple of outputs: one for *I* and

another for Q only to monitor the modulated signal power. The receiver will receiver the *RF* signal from the channel and output the demodulated complex *PRBS Rx* signal.

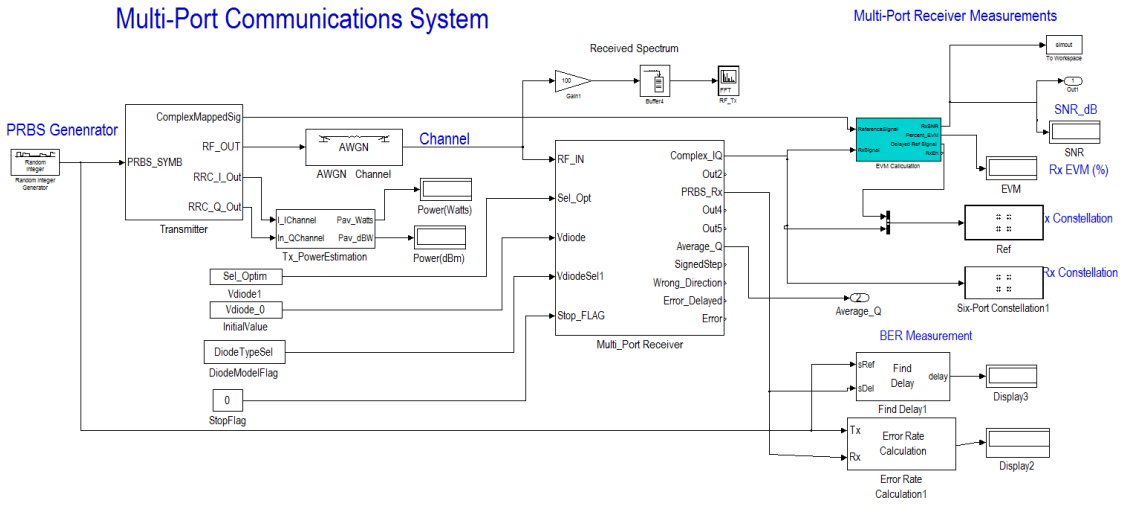


Figure E.1: Multi-Port System Top Block.

E.4 Tx Description

The transmitter is built mostly using Simulink native blocks. It is shown in Fig. E.2. The transmitter is assumed to be ideal. No imperfections such as *ACPR*, quantization noise, carrier feed-through in the mixers, etc. are considered.

E.4.1 Random Integer Generator - (*PRBS* Generator)

The random integer generator will generate random symbols within the modulation set defined by the selected modulation at the script. For instance: If we select 16QAM, the random generator will generate random values in the set $[-3, -1, 1, 3]$ for I and Q values.

E.4.2 Rectangular QAM Modulator

This block will generate a complex modulated signal composed of I and Q in accordance with the modulation chosen in the Matlab script. This is a wideband signal and needs to be filtered to remove undesired frequency components.

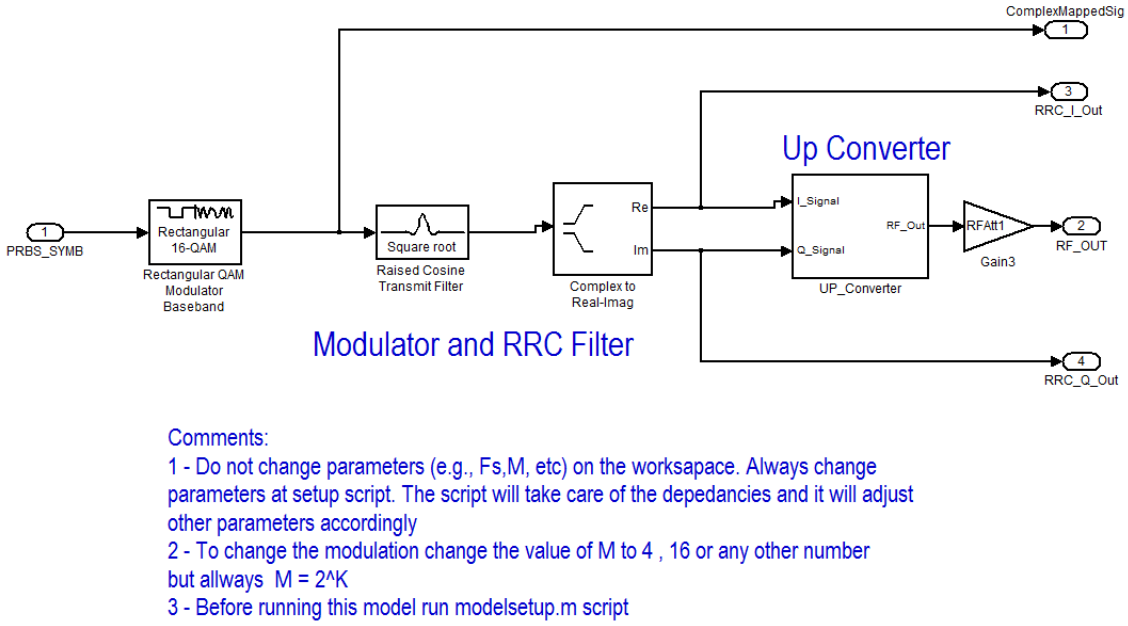


Figure E.2: Single Carrier Transmitter.

E.4.3 Root Raised Cosine Filter - (*RRC* Filter)

The root raised cosine filter removes the extra unnecessary spectrum energy at the transmitter. This filter will reduce the transmitter spectrum to the minimum necessary to be recovered at the receiver side.

E.4.4 Up Converter

This block is shown in Fig. E.3. It has two inputs (I and Q) and one output (RF_Out). The LO is built with a couple of sine waves with a difference in phase of $\pi/2$ from each other. On the right side, there is an example of the LO settings in Simulink. All the parameters are set in the Matlab script. There is no need to set any parameter directly in the model.

E.5 Rx Description

This section provides a detailed explanation about the Multi-Port receiver modeled in Simulink. The receive is built using a Six-Port Down converter block which is

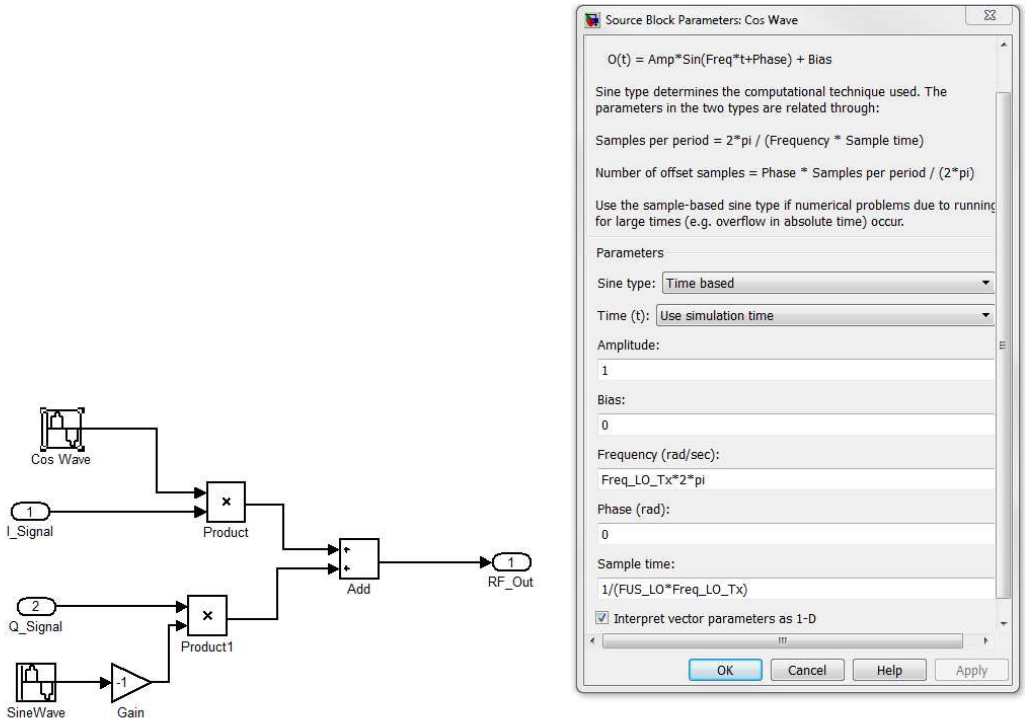


Figure E.3: Up Converter.

responsible to estimate the values of I and Q from the receiver signal. Following this block, there is the BB_Gain block which provides a different gain adjustment for each modulation. The Root Raised Cosine Filter, the *BB AGC*, Demodulator, Optimizer and Metrics. These blocks will be explained in details in the following sections.

E.5.1 Multi-Port Receiver

Fig. E.4 shows the block that represents the behavioral model for the *RF* section. It includes the power combiner, *LO* and diode detectors. It also includes the digital front-end (*DFE*) responsible for estimating the values of **RSSI**, I and Q based on the input power values and inverse of the system matrix **M**. The estimation of I and Q is done using Eq.2.1. The Table E.2 shows the Six-Port receiver's inputs and outputs parameters and ports.

Table E.2: Multi-Port Receiver

Variable	Description	Comments
Diode Voltage	Vbias	Input
DiodeSel	Selects the diode type and fitting	Input
	fitting polynomial	Input
RF_IN	Received RF signal	Input
D	Inverse of **M**	Input from script
$ALo * CouplFact$	Portion of *LO* signal coupled	Input
RSSI	Estimated receiver strength indicator	Output
I and *Q*	Calculated output *I* and *Q*	Output

Local Oscillator:

Multi-Port receivers require one *LO* with multiple phase branches. These different phase will need to construct the **M** matrix. This block provides the behavioral model for the *LO*. Neither phase noise *PN* nor spurious or harmonics are modeled. It is an ideal *LO* with a four phase output. Phase error between branches (not phase noise) can be added at the script level. See the script "Local Oscillator four Phases".

% ********** Local Oscillator four Phases **********

$error = ErrorDeg * pi/180;$

$Phi_0 = pi/4 - error;$

$Phi_1 = Phi_0 + pi/2 + error;$

$Phi_2 = Phi_1 + pi/2 - error;$

$Phi_3 = Phi_2 + pi/2 + error;$

Multi-Port Down Converter *RF* Section

This block is shown in Fig. E.5. It consists of power splitters, couplers and diode detectors (power detectors) blocks. It is responsible to receive the *RF* modulated signal, equally split this signal into four power signals, then using couplers, add each received signal branch to one *LO* signal with a different phase. After the *LO* signal and *RF* input signal are added, the diodes will output each branch power which is:(*RF* + *LO*). This block provides several options of approximation polynomial for a given diode as well as five options of detectors available to be selected. A piece of Matlab

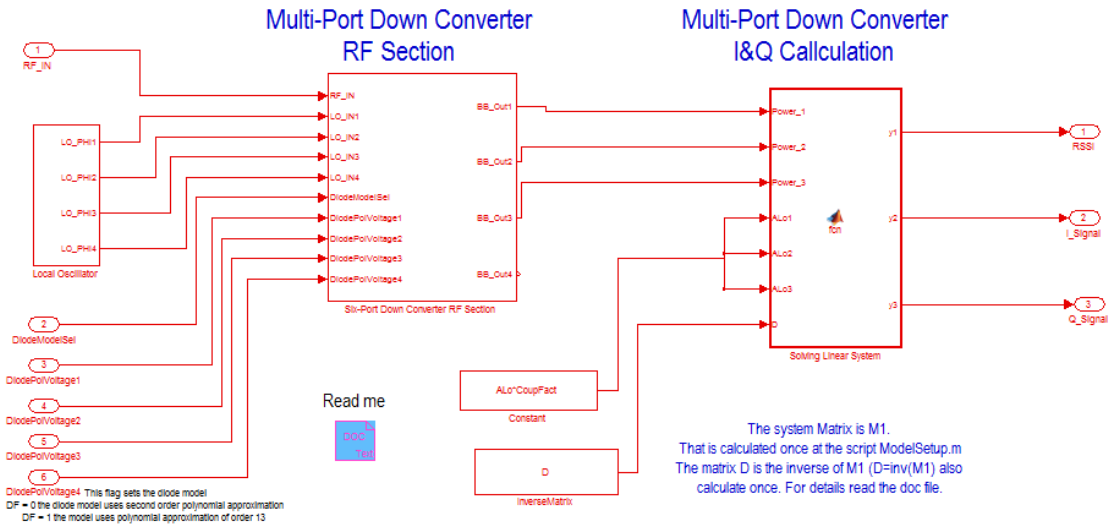


Figure E.4: Multi-Port Receiver.

code that describes the winer diode using an approximation polynomial of degree 13 is provided bellow.

% WINER diode p order = 13 P_{Winer1} = [0.5681 − 7.706646.2201 − 161.1933361.7245 − 545.9367562.9422];
P_{Winer2} = [−395.3229185.4621 − 56.0088 + 10.2275 − 1.01520.0449 − 0.0006];
P_{Winer} = [$P_W iner1 P_W iner2$];
*

This block also allows the user to include memory effects in the diodes. This is done by setting the MemoryEffectFlag flag to one at the Matlab script prior to starting the simulation. Table E.3 provides the list of inputs and outputs for this block.

Multi-Port Down Converter *I* and *Q* Calculation

The embedded Matlab function will calculate the I and Q signals based upon input measured powers plus the inverse of the system matrix already calculated in the script that starts the simulation.

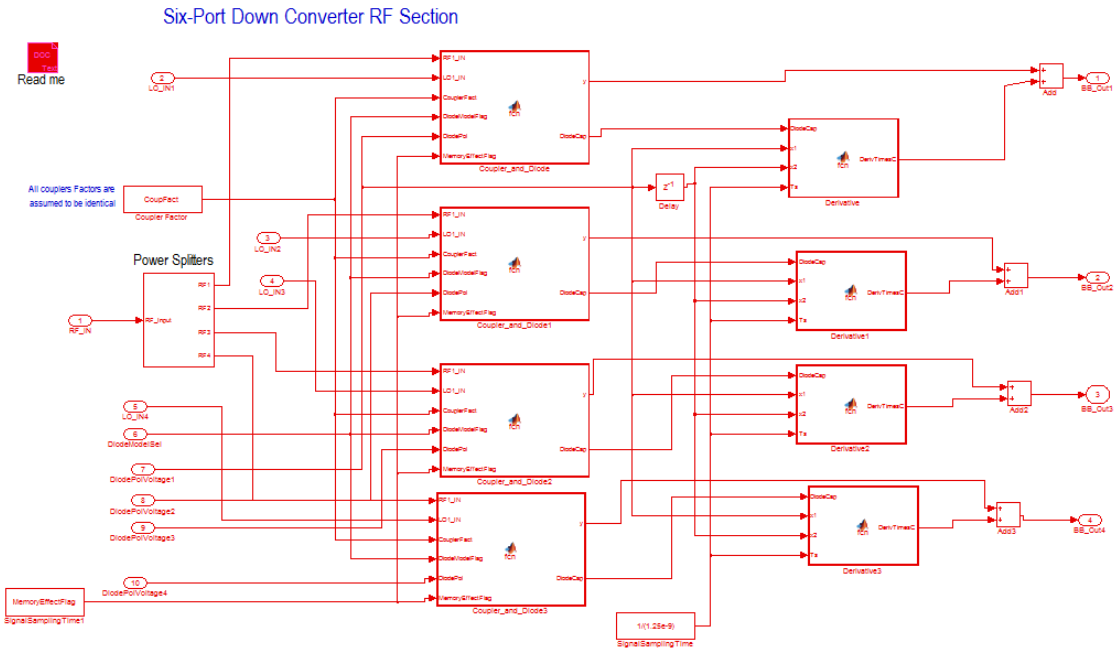


Figure E.5: Multi-Port RF Section.

********** MULTI-PORT DOWN CONVERTER **I** AND **Q** ESTIMATOR **********

function $[y1, y2, y3] = fcn(Power_1, Power_2, Power_3, ALo1, ALo2, ALo3, D)$

%This function solves the Linear system that contains three powers, the

%respective LO amplitudes and the Linear system Matrix.

% $Power_x$ is the measurement of the power at the output of diodes

% ALOx is the amplitude os the Local Oscillators

% D is the Linear system inverse Matrix already calculated at the Model

% set-up script. This matrix needs to be calculated only once because it is

% derivated based on the implementation of the Six-Port Hardware.

$k1 = Power_1 - ALo1^2/2$; % Removing DC component from the diodes output

$k2 = Power_2 - ALo2^2/2$; % Removing DC component from the diodes output

$k3 = Power_3 - ALo3^2/2$; % Removing DC component from the diodes output

vectK=[k1 k2 k3]'; % Forming AC Power vector

y=D*vectK; % Solving the linear System

y1 = y(1,1); % RSSI

y2 = y(2,1); % I signal

y3 = y(3,1); % Q Signal

Table E.3: Coupler and Diode I/Os

I/O	Description	Comments
RFx_IN	RF input signal	Input
LOx_IN	Local Oscillator Input	Input
CouplerFact	Coupler factor is the fraction of the *LO* power coupled into the path	Input
DiodeModelFlag	Selects the diode model. In the script its name is DiodeTypeSerl	Input
DiodePol	DC voltage applied to the diode	Input
MemoryEffetFlag	Sets the system to account with memory effects on the diode	Input
y	Power output value	Output
DiodeCap	Diode Capacitance value	Output

E.5.2 BB Gain

This block applies a fixed gain to the received I and Q signals. This fixed gain compensates for the differences in peak to average power ratio (*PAPR*) from different modulation types. Therefore, different gain values will be applied to different modulation types. See Matlab script "*BB* Gain Block".

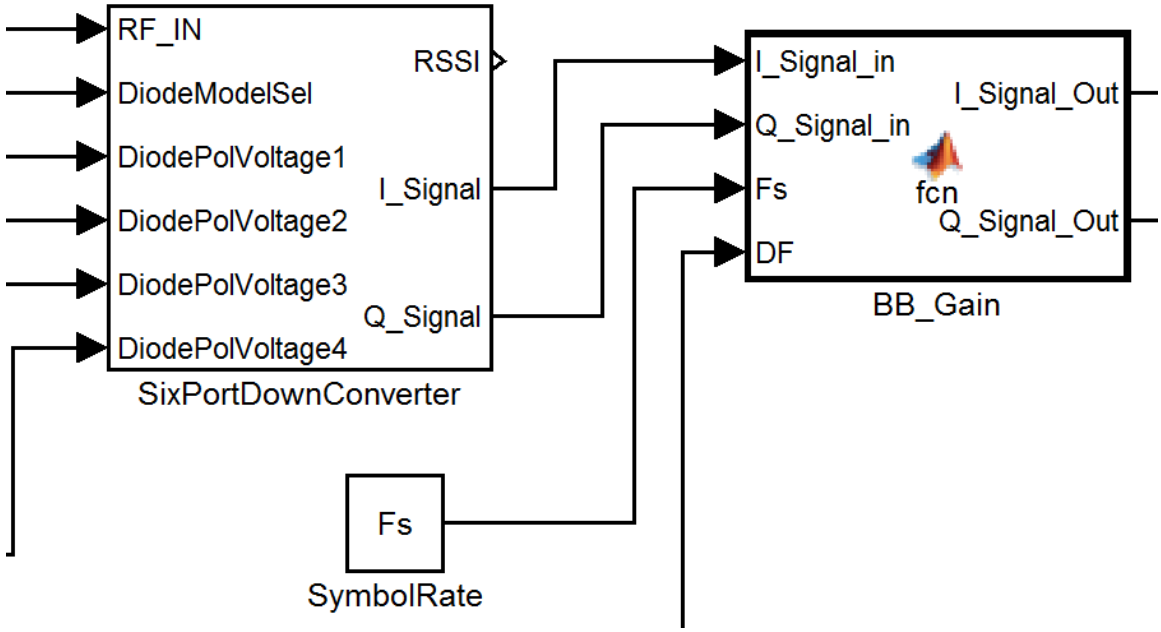


Figure E.6: BB Fix Gain Block.

```
****************************** BB Gain Block ********************************
function [Isignal_Out, Qsignal_Out] = fcn(Isignal_in, Qsignal_in, Fs, DF)
Fsx=Fs*1e-6;
if  DF == 0
  if  Fsx == 1
     Gain = 2;
  elseif  Fsx == 2
     Gain = 3;
  else
     Gain = 5;
  end
  Gain = 20;
end
I_Signal_Out = Gain * I_Signal_in;
Q_Signal_Out = Gain * Q_Signal_in;
```

E.5.3 Root Raised Cosine Filter - (*RRC* Filter)

This section describes the *RRC* filter which is shown in Fig. E.7. The settings of this filter matches the *RRC* transmitter filter. This will minimize the received signal degradation. The *I* and *Q* signals are down-sampled by a factor of 5 and combined to pass through the complex filter. After filtering the complex signal, the output is converted into two orthogonal vectors at the output.

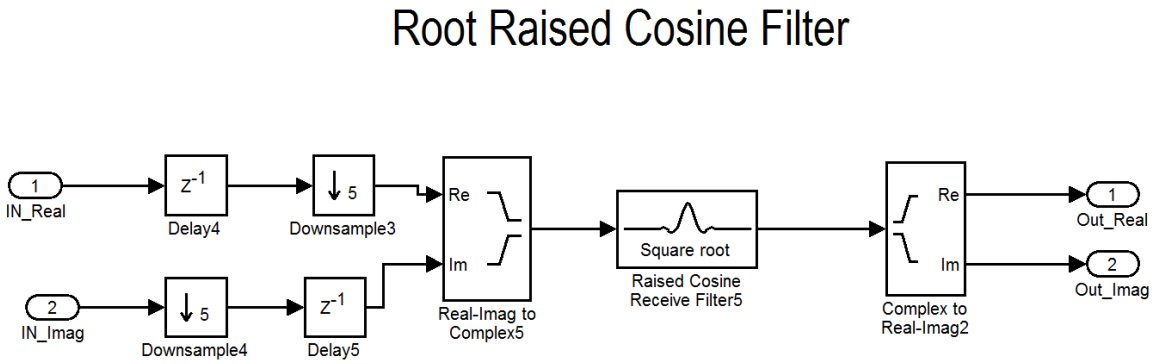


Figure E.7: Receiver Root Raised Cosine Filter.

E.5.4 BB AGC

To be able to keep the voltage at the input of the *ADC* constant within a certain dynamic range of the *RF* signal, it is required to use automatic gain control. Generally, the gain control of a receiver is done in three sections: *RF*, analog *BB* and Digital *BB*. The gain partition is done in such way that no matter the input signal level, it is within the receiver dynamic range, and the voltage at the input of the *ADC* will be constant. In this model, we only used gain control at the *BB* level. There is no control at *RF*. *I* and *Q* imbalance control is not performed in this block. This block contains two identical voltage gain amplifiers, one for *I* and the second one for *Q*. Therefore, the *VGAs* and respective control voltages are identical. This block represents the behavioral model for *BB AGC* including *I* and *Q* VGAs. The input and output ports for this block is shown in Table E.4.

The signal at the output of each *VGA* is re-sampled at rate Ts=1/Fs

Table E.4: BB AGG TOP I/Os

I/O	Description	Comments
IN_I	In phase input signal	Input
IN_Q	Quadrature input signal	Input
V_Ref	Reference voltage	Input
AGC_Sel	Selection of AGC	Input
Out_I	In phase signal output	Output
Out_Q	Quadrature signal	Output
ErrorValue	Error function	Output for observability
V_Control	Correction voltage to VGAs	Output for observability

E.5.5 Loop Filter

This block is shown in Fig E.6 and has the purpose to adjust the *I* and *Q* signals to their optimal values.

Table E.5: BB AGG TOP I/Os

I/O	Description	Comments
InputSignal	Input signal to be either amplified or attenuated	Input
VRef	Optimal maximum peak voltage to feed the *ADC* or demodulator. If the *ADC* is fed with lower or higher voltage, the dynamic range will be compromised.	Input
MaxValue	Maximum value of the input signal.	Output
ErrorValue	Is the difference between the reference voltage and the maximum value of the input signal.	Output
V_Control	*AGC* analogue Control voltage that will set the gain of the Variable Gain Amplifier *(VGA)*	Output

This block needs to assure that the peak voltage generated by the *VGA* is as close as possible to *VRef*. To generate *V_Contorl* this block uses three steps:

Step 1 Find the peak voltage of the input signal.

Step 2 Find the error between the input peak voltage and *VRef*.

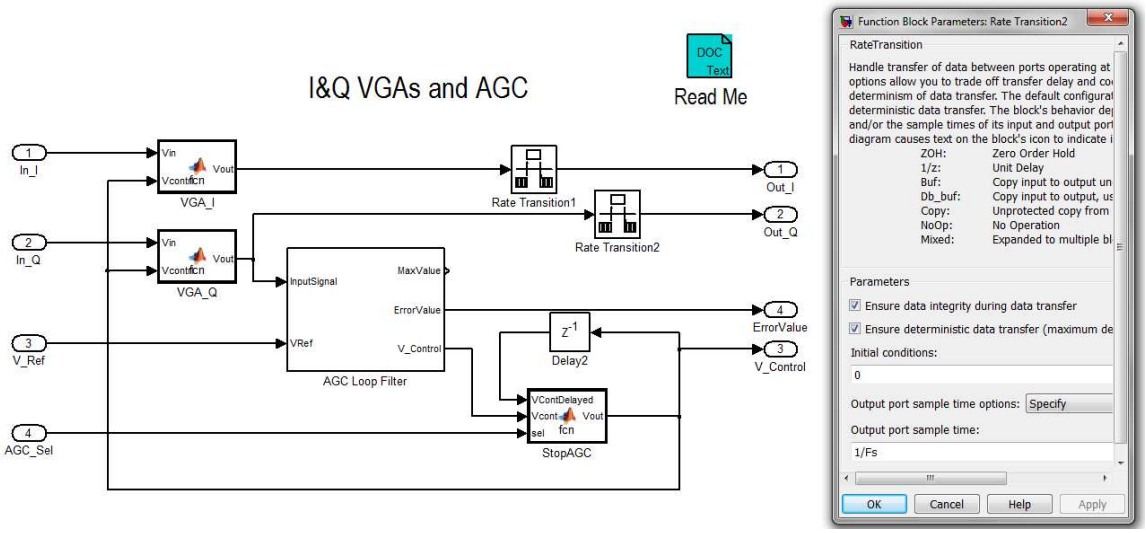


Figure E.8: BB AGC Top Level.

Step 3 Calculate the new *V_Control*.

Finding the Peak Voltage of Input Signal The peak voltage is found by buffering a certain amount of samples of the input RF signal and finding the maximum of these samples, assume a carrier signal with N samples per period. This carrier is then modulated by a baseband 16QAM signal. This carrier will have three possible peaks and multiple phases. The job of this block is to find the maximum peak. A compromise must be made between the number of samples to be buffered. If the number of samples are not enough, the AGC may introduce an error on the output voltage and consequently the demodulator may introduce bit errors.

ERROR VALUE: This is the error found by the difference between the maximum peak voltage and VRef.

LOOP Filter The loop filter is composed of an integrator and an exponential function. The integrator function is $H(z) = KTs/(Z-1)$ where $K = 8000$ and Ts is the sampling time. The exponential function is required because when the error is negative this function will generate a number less than one (attenuation) and when the error is positive the exponential function will generate a value greater than one.

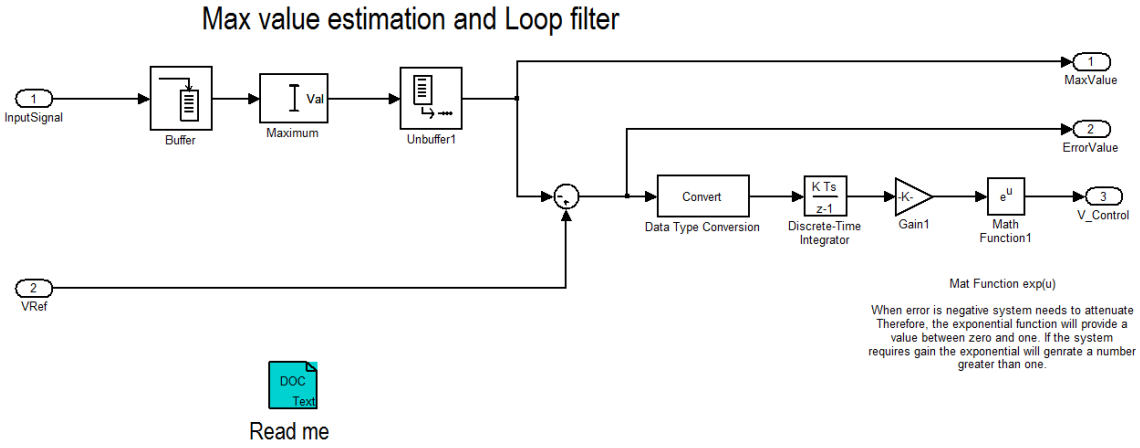


Figure E.9: BB AGC Control.

```
****************************** STOP AGC ********************************
function Vout = fcn(VContDelayed, Vcontrl, sel)
if  sel == 1
  Vout = Vcontrl;
else
  Vout = VContDelayed;
end
```

E.5.6 Demodulator

The demodulator uses a primitive Simulink block. The rectangular *QAM* demodulator block is set when the model set up script runs at the beginning of the simulation. The input of the block is a modulated complex signal and the output is a sequence of random symbols estimated from the constellation type being transmitted.

E.5.7 Optimizer

Chapter 4 is dedicated to the optimizer modeled in Simulink. After the *BB I* and *Q* signals pass through the *AGC* block it goes into the "blind" optimizer to find the optimum value for the diode bias point. Fig. E.10 shows the top level of the optimizer. Before using the **I** and **Q** estimated values and correcting the diode bias voltage, an average of these signals is taken (See Fig, E.11). A rate translate block follows the average block, it is used so that all signals at the input of the following inner block

present the same sampling time. Observe that before the rate adjustment blocks the I and Q signals have a blue color. However, after the rate conversion, all signals have red color. In Simulink, that means all signals at its input have the same sampling time.

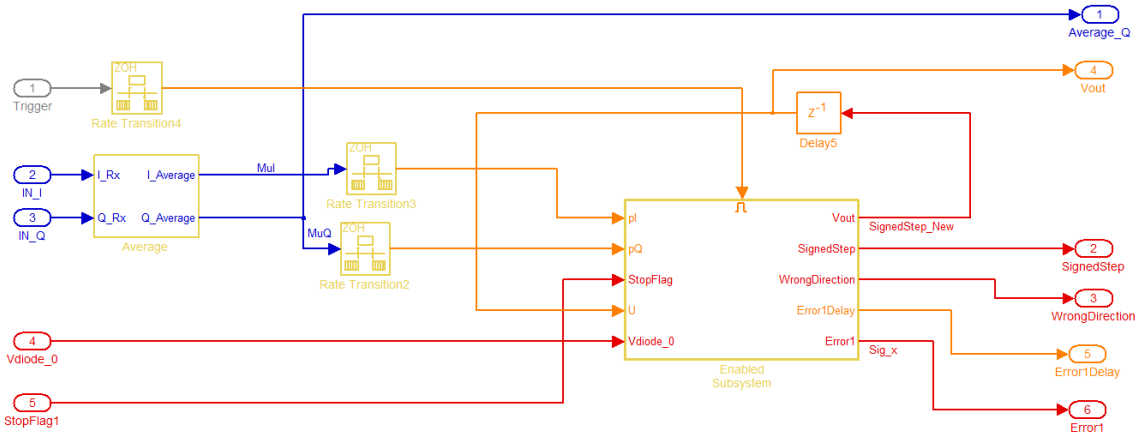


Figure E.10: Blind Optimizer Top.

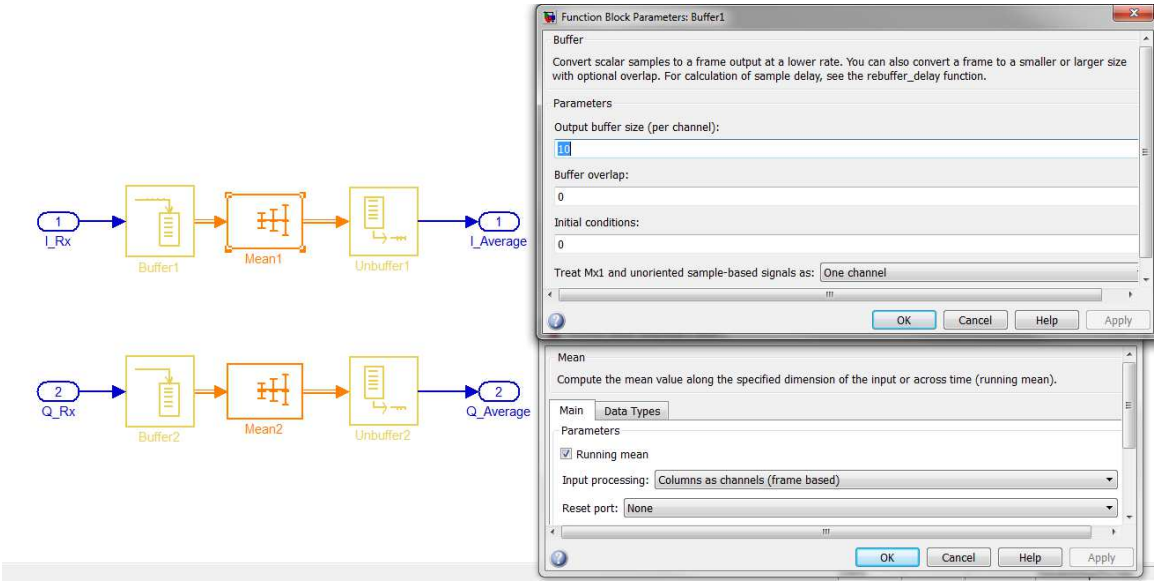


Figure E.11: Average of I and Q.

Blind Optimizer Chapter 5 and the work already published in [95] provides an initial estimate of the diode bias point. The purpose of the blind optimizer is to find

the optimum V_{bias} for the diode. Once the initial value is provided to the optimizer using for instance, the technique describe in Chapter 5, the optimizer will walk on a direction on the diode's I-V curve and will change direction if required. The blind optimizer is described in this thesis and already published in [96].

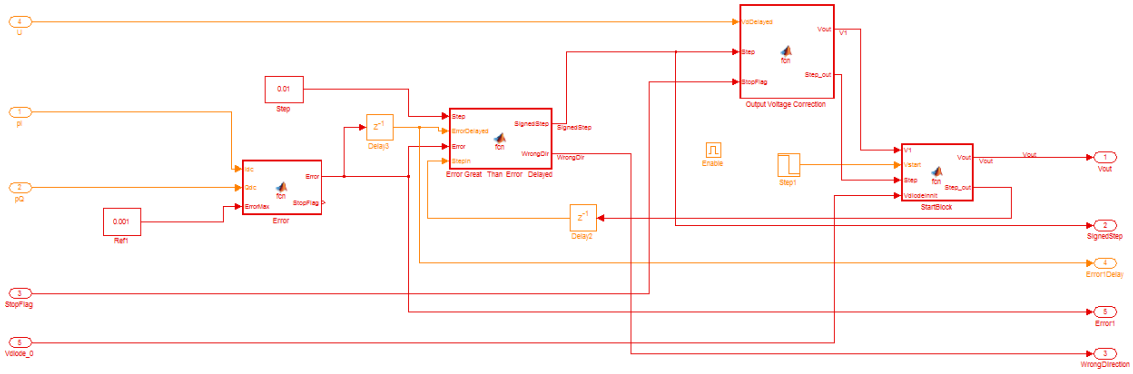


Figure E.12: Blind Optimizer.

```
************************ Min Error Direction Finding ***********
function [SignedStep,WrongDir] = fcn(Step, ErrorDelayed, Error, StepIn)
if abs(Step) >= abs(StepIn)    Step1 = StepIn;
else
  Step1 = Step;
end
if abs(Error) > abs(ErrorDelayed)    WrongDir = 1; else
  WrongDir = 0;
end
  if sign(ErrorDelayed) == sign(Error) % It is required to take care of zero crossing
    Sigx = 0;
  else
    Sigx = 1;
  end
if WrongDir == 0
  if Sigx == 0;
    SignedStep = Step1;
  else
    SignedStep = -0.5 * Step1;
  end
else
  if Sigx == 0;
    SignedStep = -Step1;
  else
    SignedStep = -0.5 * Step1;
  end
end
```

```
****************************** Function Error Calculation ***********
function [Error, StopFlag] = fcn(Idc, Qdc, ErrorMax)

Error1 = max(abs(Idc),abs(Qdc));
if  (abs(Idc) − Error1) == 0
  Error = Idc;
else
  Error = Qdc;
end

if  abs(Error1) < ErrorMax    StopFlag = 1;
else
  StopFlag = 0;
end
```

E.6 Metrics

This model is capable of providing various types of metrics. *EVM* is the most used metric on this thesis and the reason for that is because it is easy to measure the system performance using *EVM*.

E.6.1 Error Vector Magnitude - *EVM*

The value of the *EVM* in dB is calculated based upon the knowledge of the percentage of *EVM* using Eq. E.1 and described by the script bellow.

$$EVM_{dB} = 10 * \log 10\left(\frac{1}{(\%EVM)}\right) \tag{E.1}$$

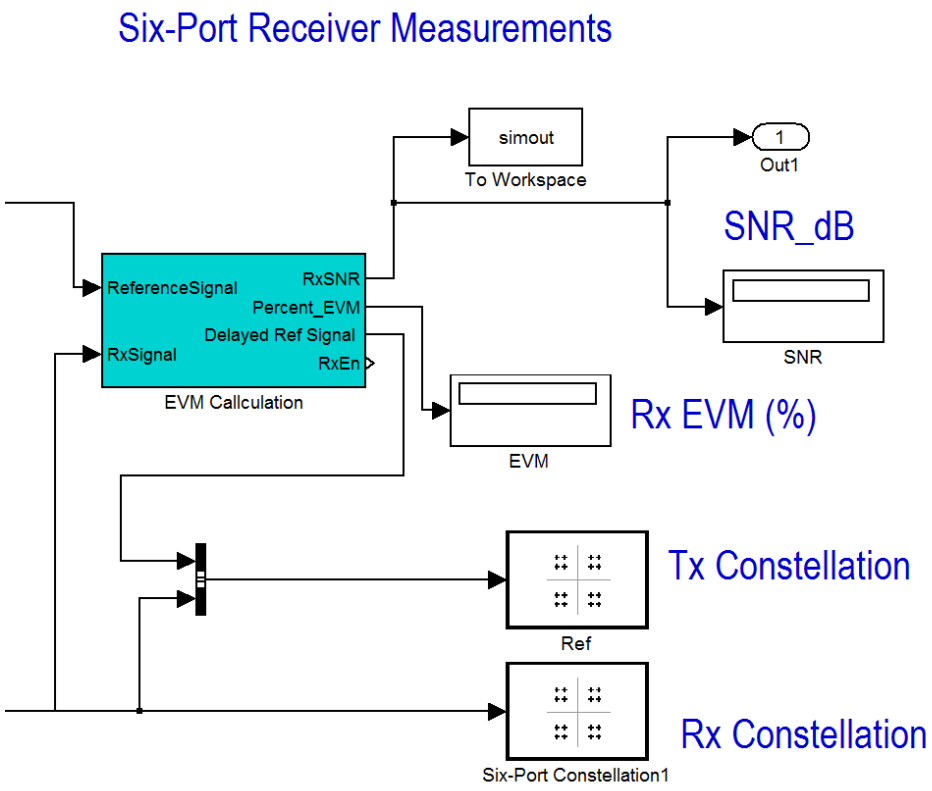


Figure E.13: Simulation Results TOP block.

**********Calculating the *EVM* **********

function $[EVMdB, Sel] = fcn(EVM_Percent)$

$EVM_{dB} = 10 * log10(1/((0.01 * EVM_Percent)^2));$
$if \;\; EVMdB > 18$
  $Sel = 1;$
else
  $Sel = 0;$
end

The percentage of *EVM* is calculated based upon a reference signal and the receiving signal. The receiving signal is provided by the demodulator at the receiver. The block that calculates the percentage of *EVM* is seen bellow at Fig. E.14.

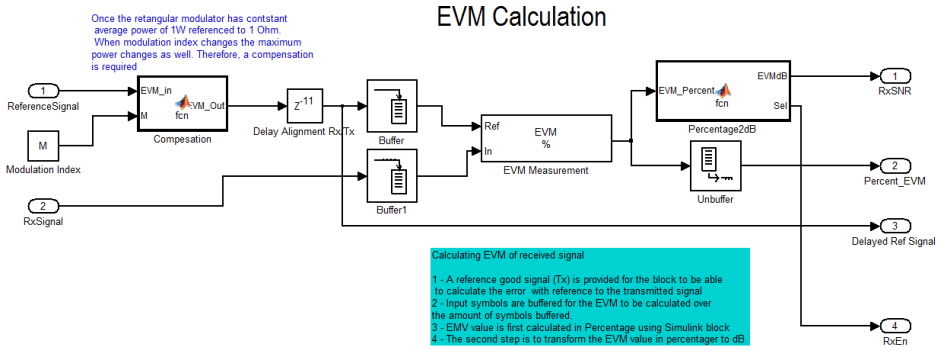


Figure E.14: *EVM* Calculator Block.

E.6.2 Constellation

Constellation is measured at the receiver *I* and *Q* signals. An example of constellation is provided in this Thesis in Fig. 4.10. In the model the constellation is displayed using a native Simulink block.

E.6.3 SNR

SNR results are shown throughout this thesis. Fig. E.16 shows the *SNR* at the *I* and *Q* resultant of the *LO* phase error. To produce this figure, an equal phase error was introduced at all three *LO* branches. E.g., if the phase error was +2°, we would add this error in all phases. We did not consider random phase error (Phase Noise). This error is static and constant. Another example of *SNR* results is shown in Fig. E.15. The horizontal axis is the simulation time in ms and the vertical axis is the resultant system simulation *SNR* in dB.

E.6.4 Simulating Rx LO Phase Error

This simulation was performed by setting the Diode voltage at the optimum point as per Fig. 4.1 to 0.95V and also setting the *ADC* voltage at its optimum value as per Fig. 5.6. One observes that over time the value of the *SNR* varies. This happens due to *AGC* loop adjustment. But for these conditions the SNR value does not degrade bellow 36 dB which is enough to operate using high-order modulation schemes such as 64QAM. Another way to visualize this performance degradation is to look at the

SNR versus phase error at a given simulation instant. This is represented in Fig E.16. The details about this figure were explained in the previous section.

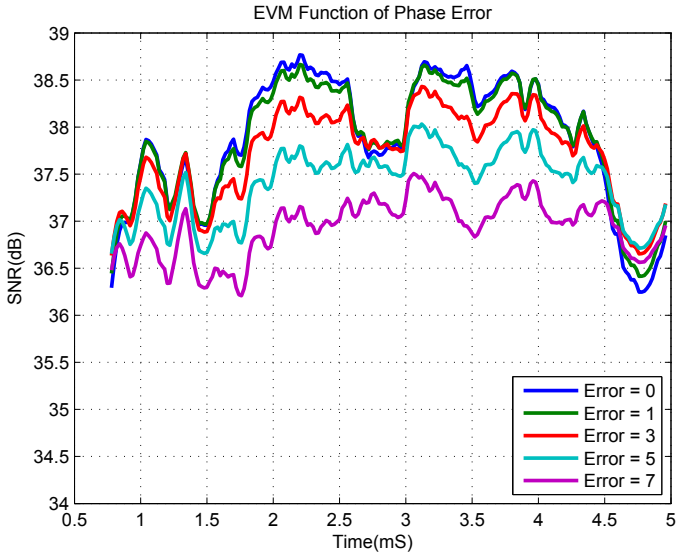


Figure E.15: EVM function of Oscillator Phase Error in Degrees

E.7 Conclusion

In this chapter we discussed the major aspects of the model used in this thesis. We introduce the model by presenting a script to set the model parameters which has the capability to automatically open and run the model. After becoming familiar with the creation of the model, the user can easily adapt the model for his/her particular needs.

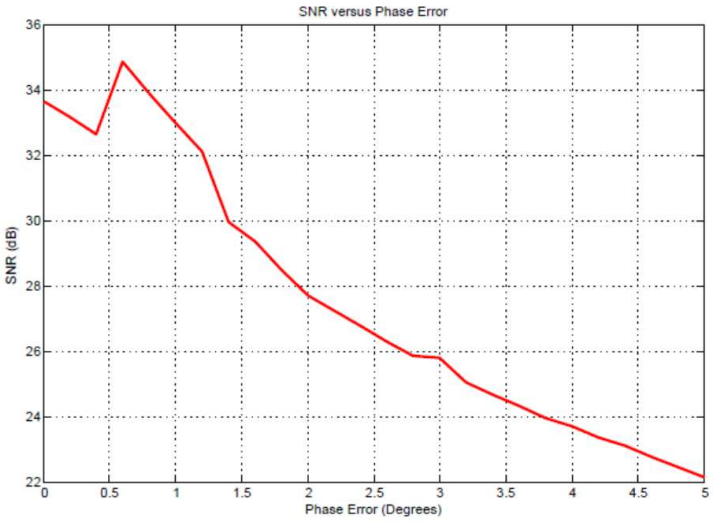


Figure E.16: SNR function of Oscillator Phase Error in Degrees

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