10+Gbps Serial Data Transmission Over a Tyco 34" FR4 Backplane Channel Using Amplitude-Optimized Bit-Edge Equalization with an Adjustment of LMS Error Derivation Points

by

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Important Information

The information used in this thesis comes in part from the research program of Dr. Tad Kwasniewski and his associates in the VLSI in Communications group. The research results appearing in this thesis represent an integral part of the ongoing research program. All research results in this thesis including tables, graphs and figures but excluding the narrative portions of the thesis are effectively incorporated into the research program and can be used by Dr. Kwasniewski and his associates for educational and research purpose, including publication in open literature with appropriate credits. The matter's intellectual property may be pursued cooperatively with Carleton University and Dr. Kwasniewski and where and when appropriate.

Abstract

In high-speed backplane serial data transmission systems, channel impairments such as amplitude attenuation and group-delay distortion cause intersymbol interference (ISI) that limits the maximum transmission distance and data rate. This dissertation presents a unique amplitude-optimized bit-edge equalization (BEE) scheme for 10+Gbps serial data transmission over high-loss backplane channels. The proposed BEE scheme intends to mitigate ISI and reduce the impact of channel group delay distortion by compressing data spectrum in conjunction with optimizing the sampling phase. Using a least-mean-square (LMS) adaptive algorithm as a receiver (RX) error convergence engine, the proposed BEE scheme aims to optimize the bit-edge amplitudes by equalizing only the edges of data bits with an adjustment of the LMS error derivation points, which in turn changes the error information and affects filter coefficients for pulse amplitude modulation. Thus, the proposed amplitude-optimized BEE eliminates the need for complicated algorithms that are required in the phase-optimized BEE.

This proposed BEE scheme employs a 5-post-tap symbol-spaced FIR (SSF) filter as the transmitter (TX) pre-emphasis/de-emphasis for bit-edge equalization. With TX data pre-coding, the channel's far-end 3-level signal to 2-level binary decoding depends only on the current received bit. No error propagation occurs.

In this research, a typical Tyco 34" FR4 backplane channel was used as the comparison benchmark. A Matlab script was generated and used to evaluate the link performance when comparing various channel equalization and signaling techniques. The

optimality of using the proposed BEE in channel efficiency, signal-to-noise ratio (SNR) enhancement, power constriction, as well as mitigating ISI and reducing the impact of channel group delay distortion was demonstrated and compared with those by using the phase-optimized pulse width modulation (PWM) and the conventional non-return-to-zero bit-center equalization (BCE) and duobinary signaling schemes.

It was demonstrated that, using the proposed BEE as TX pre-emphasis at a 12Gbps data rate, the channel's far-end bit-edge (BE) eye was enlarged by approximately 88.9% in eye height and 20.8% in eye width compared to the bit-center (BC) eye when using the conventional BCE scheme. In addition, the BE eye using the proposed BEE was enlarged by approximately 143% in eye height and 16.6% in eye width compared to the eye height and width when using the conventional duobinary signaling scheme.

It was also demonstrated that, by using the proposed BEE as the TX de-emphasis at a 10Gbps data rate, the channel's far-end bit-edge eye height was enlarged by approximately 77.5% with a 0.93% reduction in eye width compared to the bit-center eye when using the conventional BCE. In addition, the bit-edge eye height using the proposed BEE was enlarged by approximately 29.1% with a 5.8% reduction in eye width compared to the eye height and width when using the phase-optimized PWM.

It is concluded that the proposed BEE scheme has better performance for high speed (e.g. 10Gbps and exceed) data transmission over high loss channels.

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List of Abbreviations

<i>4-PAM</i>	4-level pulse amplitude modulation
<i>BC</i>	bit center
<i>BCE</i>	bit-center equalization
<i>BC-ZFE</i>	bit-center zero-forcing equalization
<i>BE</i>	bit edge
<i>BEE</i>	bit-edge equalization
<i>BE-ZFE</i>	bit-edge zero-forcing equalization
<i>CDR</i>	clock and data recovery
<i>CEI</i>	Common Electrical I/O
<i>CML</i>	Current Mode Logic
<i>DFE</i>	decision feedback equalization
<i>FFE</i>	feed-forward equalization
<i>FIR</i>	finite impulse response
<i>FSSF</i>	fractional-symbol-spaced FIR
<i>Gbps</i>	Giga-bit per second
<i>HSBI</i>	High Speed Backplane Initiative
<i>HSSF</i>	half-symbol-spaced FIR
<i>ISI</i>	inter-symbol interference
<i>LMS</i>	least mean square
<i>LR</i>	long reach
<i>LTI</i>	linear time-invariant

<i>M-PAM</i>	multi-level pulse amplitude modulation
<i>NE</i>	near-end
<i>NEXT</i>	near-end crosstalk
<i>NRZ</i>	non-return-to-zero
<i>OIF</i>	Optical Internetworking Forum
<i>PAM</i>	pulse amplitude modulation
<i>PCB</i>	printed circuit board
<i>PE</i>	pre-equalization
<i>PLL</i>	phase-locked loop
<i>PRS</i>	partial-response signaling
<i>PWM</i>	pulse width modulation
<i>RX</i>	receiver
<i>SNR</i>	signal-to-noise ratio
<i>SR</i>	short reach
<i>SSF</i>	symbol-spaced FIR
<i>TX</i>	transmitter
<i>UI</i>	unit interval
<i>ZF</i>	zero forcing

List of Symbols and Variables

$\oplus$	exclusive “OR” operator
$\{a_k\}$	amplitude modulated d_k signal
B	channel bandwidth
B_o	Nyquist bandwidth
$\{B_k\}$	decoded binary data from the duobinary sequence
$\{b_k\}$	input binary data sequence
C_n	filter tap coefficient
$\{c_k\}$	duobinary coded data sequence
D	constant group delay
$D(\omega), D(f)$	group delay of the transmission channel
ΔD	deviation from the constant group delay
$\{d_k\}$	precoded binary data sequence
$F(z)$	partial-response system polynomial
f_b	bit rate
$\{f_n\}$	sample values
f_s	symbol rate
$\Phi(\omega), \Phi(f)$	phase response of the transmission channel
ϕ_o	TX data sampling clock phase

ϕ_{TL}	linear phase of the channel
$H(z)$	transfer function of the transmission channel
$h(t)$	impulse response
N	number of samples
n_d	data delay relative to the bit center
$P(\omega), P(f)$	phase delay of the transmission channel
T	symbol period
T_b	bit duration
μ	step size
$u[k]$	distorted data at the channel's far-end
$u_d[k]$	delayed version of $u[k]$ by n_d
V_n	voltage noise at the intermediate level in multi-level pulse amplitude modulation
$\{x_k\}$	bit-edge data sequence

Chapter 1: Introduction

1.1 Research Motivations

In recent years, backplane serial data transmission has been one of the most commonly used techniques in high-speed wireline applications. Formed in 2002, the High Speed Backplane Initiative (HSBI) launched the feasibility of developing serial link technology capable of sending serial data at a multi-gigabit per second (multi-Gbps) data rate across a backplane environment up to a distance of 30 inches (including two connectors). HSBI also announced that future work of the group would address 10 Gbps and higher data rates over the same environment [1], [2]. The need to address the improvement of the bandwidth capacity in backplane applications has also been recognized by the Optical Internetworking Forum (OIF) [3]. In 2002, the OIF Physical and Link Layer (PLL) Working Group undertook the creation of the Common Electrical I/O (CEI) project, which defined the electrical specifications for 4.976 to 6+ Gbps and 9.95 to 11+ Gbps serial data transmission. These specifications were defined to support both short reach (“SR”: 0 to 200mm or 8 inches of printed circuit board trace with up to one connector) and long reach (“LR”: 0 to 1m or 39 inches of printed circuit board trace with up to two connectors, i.e. backplane) applications. The CEI project provided the interconnect building blocks that are now being used to build the equipment that will satisfy the industry’s immediate need for bandwidth. Currently, the OIF has authorized its PLL Working Group to begin the new CEI-25 project, which will define electrical specifications for 28Gb/s signaling for chip-to-chip applications and 25Gb/s signaling for backplane applications. These specifications

will provide the basis for the electrical interfaces that will be used to enable the higher capacities needed for the next generation of systems.

In many backplane serial links, data are often communicated by transmitting an electrical signal from one line card to another via copper traces. Despite its significant advantages of lower cost, reduced complexity and high reliability, high-speed backplane serial data transmission does have some technical challenges. In high-speed backplane serial data transmission systems, channel impairments such as amplitude attenuation and group-delay distortion cause intersymbol interference (ISI) that limits the maximum transmission distance and data rate. The skin effect and dielectric loss in the backplane channel cause frequency dependent attenuation and nonlinear phase dispersion [4]. At high data rates, a pulse representing a bit may not reach its full strength within a symbol period due to channel attenuation. The pulse will spread into adjacent symbols and cause ISI. Therefore, a pulse representing a bit not only gets attenuated in amplitude by the backplane channel, but is spread out in time which results in jitter. The amplitude attenuation and jitter cause vertical and horizontal eye closures of the received data at the far end of the channel. For a broadband signal, the superposition of un-attenuated low-frequency signal components with attenuated high-frequency signal components causes ISI. The main problem here is not the magnitude of the attenuation, but rather the interference caused by the frequency dependent nature of the attenuation.

In addition, the channel group delay distortion represents the channel's nonlinear phase dispersion. The dispersion of a physical backplane channel causes the different frequency components of a signal to have different travelling speeds as they propagate along the transmission channel. This nonlinear phase dispersion causes severe post-cursor signal

distortion that further reduces the signal amplitude and adds jitter to the received data eyes. The received data eyes are no longer peaked at bit centers, and the eye diagrams are no longer symmetric.

Overall, both the channel's frequency-dependent amplitude attenuation and group delay distortion cause ISI at high data rates. In recent multi-gigabit chip-to-chip and backplane serial data transmission systems, data rates are limited not by the operating speeds of the circuits in the transceivers but by the bandwidth of the transmission media. Therefore, in band-limited backplane serial data transmission, advanced techniques are required to achieve a better channel bandwidth utilization.

In high-speed serial data transmission over a band-limited channel, the techniques used to achieve a better bandwidth utilization fall into two categories, as illustrated in Figure 1.1. They are the channel equalization techniques to compensate for the channel frequency-dependent loss, and the advanced signaling techniques to compress the data spectrum.

Figure 1.1 Common Techniques for Increasing the Channel Bandwidth Efficiency

1) Channel Equalization

Channel equalization can be used to eliminate the problem of frequency dependent attenuation by filtering the transmitted or received signal so that the concatenation of the equalizing filter and the transmission channel gives a flat frequency response.

Both transmitter (TX) and receiver (RX) equalizations have been proven to be effective in dealing with the loss associated with the transmission channel. Choosing a right equalization technique is mainly dependent upon the application. In general, there are three possible ways to overcome transmission losses. They are TX pre-emphasis, RX equalization, or a combination of the two.

Currently, discrete-time symbol-spaced FIR (SSF) filters for pre-emphasis at the transmit side and/or decision feedback equalization (DFE) at the receive side have been widely used to compensate for the channel's frequency-dependent loss [5], [6]. However, conventional SSF filters only look at bit centers as the optimal sampling points to collect error information. This bit-center sampling approach is based on the assumption that the received data eyes are symmetric and peaked at bit centers. But at a high data rate, severe channel group delay distortion represents the backplane channel's nonlinear phase dispersion, which is another ISI contributor in addition to amplitude attenuation. This nonlinear phase dispersion causes severe post-cursor signal distortion. The received data eyes are no longer peaked at bit centers, and the eye diagrams are no longer symmetric [7], [8]. On the other hand, an FIR filter based on amplitude modulation not only changes pulse amplitudes, but also changes the slopes of the pulse rising and falling edges. Therefore, even though zero forcing received data bit centers is effective in correcting ISI at the sampling

points, more jitter could be injected at the transition edges if the data eyes are not symmetric, which results in a reduction in the timing margin.

In addition, the performance of an SSF filter is limited by aliasing, as a result of sampling at $1/T$ where T is the symbol period. An SSF filter cannot compensate for channel impairments beyond the sampling frequency. Theoretically, to overcome the aliasing issue, a fractional symbol spaced FIR (FSSF) filter can be used. A commonly used FSSF filter is the half-symbol spaced FIR (HSSF) filter [9], [10] that samples at both the bit centers and the bit edges, and forces the transition voltage level to be half of the signal amplitude. Ideally, an HSSF filter samples at a half of T and thus extends the compensation beyond $1/T$. However, an HSSF filter needs double of the tap numbers compared to an SSF filter to cover the same ISI time span. Doubling the tap numbers implies an increasing of power consumption in circuit implementation. In the mean time, an HSSF filter needs double of the sampling clock frequency compared to an SSF filter, which is difficult in circuit implementation at high frequencies. Moreover, the severe asymmetric signal distortion at high data rates adds difficulties to the HSSF filter optimization. The HSSF filter in [9] and [10] can't guarantee convergence, and leads to large filter coefficient variations.

Recent I/O standards such as IEEE 802.3ap have suggested the possibility of equalizing the data transition edges [11], [12] instead of equalizing the data bit centers as in conventional SSF filters [5], [6]. Previous publications [11]-[15] have shown that edge equalization reduces ISI at bit edges. Based on different error derivation approaches, edge equalization falls into two categories: amplitude-optimized and phase-optimized. The

amplitude-optimized approach performs equalization by looking at the signal amplitudes that occur at the bit edges of data, and seeking to drive those associated error terms to zero [11]-[13]. The phase-optimized approach is a different way of thinking of channel equalization by compensating for phase delay distortion instead of amplitude attenuation. The difficulty in phase-optimized edge equalization is that the reference zero crossing points shift in time with different data patterns and transmission rates. Hence, complicated algorithms are required to achieve phase equalization [14], [15]. In addition, in these publications [11]-[15], researchers do not seem to have considered the channel group delay effect at high frequencies by taking the centers of the bit time periods as the optimal bit-center sampling points, and ± 0.5 unit interval (UI) away from the centers of the bit time periods as the optimal bit-edge sampling points. However, such sampling approach is not suitable at high data rates where the received data eyes are no longer peaked at bit centers, and the eye diagrams are no longer symmetric due to the channel group delay distortion. Thus, neither the bit-center equalization nor the bit-edge equalization is optimal.

While the conventional non-return-to-zero (NRZ) bit-center equalization (BCE) [5], [6] and the amplitude-optimized bit-edge equalization (BEE) [11]-[13] schemes all use amplitude modulation, the pulse-width modulation (PWM) scheme proposed in [16] uses phase modulation that eliminates the need for the complicated algorithms as in [14], [15] by applying PWM to each bit. In this PWM scheme, only one coefficient needs to be set to fit the channel equalizer transfer function and no amplitude modulation is applied, an advantage in low-voltage high-speed CMOS processes. However, this PWM scheme not only shifts data transition edges, but also changes the data pattern that results in a wider data spectrum but with reduced DC and low frequency content as will be demon-

strated in Chapter 5. This wide PWM data spectrum limits the application of PWM in high-loss channels.

2) Multi-Level Pulse Amplitude Modulation (M-PAM)

An alternative technique for increasing the data rate in a band-limited channel is to compress the transmitted data spectrum using multi-level pulse amplitude modulation (M-PAM). As the name implies, M-PAM converts data by assigning $k = \log_2(M)$ bits to a set of M discrete amplitudes of a transmitted signal. For a given data rate, an M-PAM system reduces the effective symbol rate by a factor of $k = \log_2(M)$ compared to a conventional NRZ binary (2-PAM) system. This symbol rate reduction not only lowers the bandwidth requirements of the transceiver, but also reduces the maximum required on-chip clock frequency [17].

In an M-PAM communication system, the spectral efficiency is $2\log_2(M)$, which increases logarithmically with the number of PAM levels (M). However, with multi-level signaling, the signal-to-noise ratio (SNR) performance is sacrificed for a narrower bandwidth requirement.

4-PAM with channel equalization has been used by some vendors [18], [19] for high data rate transmission over band-limited channels. Encoding the binary data with 4-PAM reduces the effective symbol rate by a factor of 2, which lowers the bandwidth requirement of the channel and results in an increase in the SNR. However, with 4-PAM, there is a 9.5dB SNR penalty due to the four-level encoding. This technique of using 4-PAM with channel equalization has shown good performance at high frequencies and long

traces [18], [19]. However, these 4-PAM systems are typically complex leading to the difficulty in providing dense integration and significantly increased power consumption compared to standard NRZ signaling systems. In addition, the all level transitions in 4-PAM result in large jitter, which is a limiting factor for 4-PAM application. An even higher level (e.g. more than 8-level) PAM is not practical.

3) Partial Response (Correlative Coding)

Another alternative approach for compressing data spectrum is to use partial response signaling (i.e., correlative coding) techniques. Duobinary coding is a type of partial response signaling technique that can be helpful in reducing the required channel bandwidth. The concept of duobinary signaling was first introduced by Dr. Lender in 1963 [20]. It has been used in optical fiber communication systems for years. However, it is until recent years that the duobinary signaling technique is gaining more interest from researchers for high-speed backplane applications [21]-[23].

Duobinary signaling compresses the data spectrum by changing an uncorrelated 2-level binary signal into a correlated 3-level duobinary signal. Unlike 4-PAM, a duobinary signal has the same symbol rate as that of a 2-PAM (NRZ binary) signal. The spectrum of a duobinary signal is compressed to one half of the spectrum of an NRZ binary signal with the same transmission rate by redistribution of spectral density into highly concentrated energy density near DC and low frequencies.

The duobinary signaling technique can be used to accomplish the two tasks of data spectrum compression and simplification of implementation that is suitable for large scale integration. Additionally, duobinary signaling does not incur nearly as much SNR penalty

(relative to NRZ) as 4-PAM, since the 3-level duobinary coding only includes transitions between adjacent levels and has better immunity to crosstalk / reflection than 4-PAM.

The idea behind duobinary signaling is to take advantage of the “natural roll-off response” of the backplane channel, and use it to help shape the data bits that are to be sent to the receiver. But a question arises: should the binary to duobinary conversion be completed before or after a backplane channel, and what is the exact role that the backplane channel plays in a duobinary data transmission system? Different signaling schemes and sampling approaches will result in different eye opening of the received data at the far end of the channel.

Therefore, in order to propose the best signaling scheme for a specific backplane channel, one has to fully understand the concept behind each signaling techniques, as well as their advantages and disadvantages. In many applications, a good combination of these signaling techniques is essential.

1.2 Research Objective

In this research, a typical Tyco 34" (30" trace and 2×2 " connector) FR4 backplane channel was used as the working subject. The channel characteristic was known from the measurement results (.s4p files). The channel characteristic model based on these technology files had been established and widely used by colleagues [5]-[6], [9], [24]-[25], and had been proven to be effective. Therefore, this channel model was used as a base for this research. A Matlab script based link simulation tool [9], [24] was used to evaluate the link performance.

The main target of this research was to propose a signaling scheme for 10+ Gbps serial data transmission over this 34" FR4 backplane channel. The conventional NRZ bit-center-equalized SSF or FSSF / HSSF approaches as discussed in the previous section are not suitable at high data rates where the backplane channel's group delay distortion is crucial. In addition, using 4-PAM in compressing the data spectrum often has an SNR penalty due to the four-level encoding, and the 4-PAM transceiver circuits are typically complex leading to the difficulty in providing dense integration and significantly increased power consumption compared to those of the standard NRZ binary transceivers. Moreover, the all level transitions in 4-PAM result in large jitter, which limits the 4-PAM application on this backplane channel.

Thus, the proposed signaling scheme should have the features of simplicity in implementation, less SNR penalty in effectively compressing the data spectrum, and the reduction of the impact of channel group delay distortion on data transmission.

The research tasks include:

- 1) Studies of the backplane channel characteristics, especially the effect of channel group delay distortion on high-speed backplane data transmission. Equalization strategies for reducing the impact of channel group delay distortion are explored.

- 2) Evaluation and comparison of various channel equalization and signaling techniques. The effort is made to investigate the feasibilities of applying duobinary coding and edge equalization on high-speed serial data transmission over this FR4 backplane channel. Some published duobinary signaling and edge equalization schemes are reviewed, and their advantages and disadvantages are discussed.

3) To propose a unique amplitude-optimized bit-edge equalization (BEE) scheme for mitigating ISI in high-speed backplane applications. Using a least-mean-square (LMS) adaptive algorithm as an RX error convergence engine, the proposed BEE scheme is based on equalizing only the edges of data bits with an adjustment of the sampling points where the error information is collected. This proposed BEE method employs TX pre-coding in conjunction with TX pre-emphasis/de-emphasis using an SSF filter. With TX data pre-coding, the channel's far-end 3-level signal to 2-level binary decoding depends only on the current received bit. No error propagation occurs. The proposed BEE reduces the impact of channel group delay distortion by compressing the data spectrum in conjunction with optimizing the sampling phase. The optimality of using the proposed BEE in channel efficiency, SNR enhancement, as well as mitigating ISI and reducing the impact of channel group delay distortion is demonstrated and compared with those using the phase-optimized pulse width modulation (PWM) scheme [16] and the conventional NRZ bit-center equalization (BCE) and duobinary signaling schemes.

1.3 Thesis Organization

The format of this document is as follows:

Chapter 2 describes the important background information on backplane channel characteristics and data transmission. A study of the effects of channel amplitude attenuation and group delay distortion on high-speed backplane data transmission is presented in sections 2.2.1 and 2.2.2. The concepts, advantages and disadvantages of various channel equalization and signaling techniques are also discussed and compared, with a focus on the review of some recently published BEE system architectures in sections 2.3.4.

Chapter 3 discusses partial response techniques and duobinary signaling in detail. Different duobinary coding schemes are presented, and their effects on link performance are compared and illustrated.

Chapter 4 presents the proposed BEE scheme. An analytical comparison of the proposed amplitude-optimized BEE scheme with the phase-optimized PWM, the conventional BCE and duobinary schemes are included in section 4.1. Strategies for reducing the impact of channel group delay distortion using the proposed BEE and BCE with optimal sampling phase are explored and compared in section 4.2.

Chapter 5 presents the matlab simulation results and discussions. The optimality of using the proposed BEE in channel efficiency, SNR enhancement, power constriction, as well as mitigating ISI and reducing the impact of channel group delay distortion is demonstrated and compared with those by using the phase-optimized PWM and the conventional BCE, FSSF/HSSF and duobinary signaling schemes.

Chapter 6 draws the conclusion of this research, and some potential topics for future studies.

Chapter 2: Background

This chapter reviews the fundamental of data transmission theories and studies the characteristics of a backplane channel. The concepts, advantages and disadvantages of various channel equalization and signaling techniques are discussed and compared. A review of some recently published edge equalization schemes is presented.

2.1 Fundamentals of Data Transmission

In most applications, the transmission system is considered to be more cost effective if, in a given channel bandwidth, more bits per second can be transmitted [26]. In his patents on channel characteristics in 1920s, Nyquist defined the minimum channel bandwidth requirements and also the general channel characteristics required for ISI-free reception. For data transmission systems, the following are the most frequently used Nyquist theorems [26].

2.1.1 Nyquist's First Theorem (Minimum Bandwidth - Brick-Wall Channel)

The Nyquist's Minimum-Bandwidth Theorem states that "If synchronous impulses, having a transmission rate of f_s symbols per second, are applied to an ideal, linear-phase brick-wall low-pass channel having a cutoff frequency of $f_N = (f_s/2)$ Hz, then the responses to these impulses can be observed independently, that is, without intersymbol interference". Please note that when applying this Nyquist theorem to f_s rate rectangu-

lar pulses, an $(x/\sin x)$ -shaped amplitude equalizer has to be added to the ideal brick-wall channel. Thus, theoretically, it is possible to have an ISI-free transmission rate of 2 symbols/s/Hz.

In Nyquist's Minimum-Bandwidth Theorem, the cutoff frequency, also known as the Nyquist frequency, is defined to equal

$$f_N = \frac{1}{2T} = f_s/2, \quad (2.1)$$

where f_s is the symbol (Baud) rate, i.e., symbol per second, in (Hz);

$T = 1/f_s$ is the symbol duration (period), in seconds.

Define f_b to be the transmission rate in bit per second (b/s),

B is the channel bandwidth in (Hz),

then, f_b/B is the system efficiency in (b/s/Hz).

In binary systems, one transmitted symbol contains one bit of information. Therefore, the maximum bit rate in binary transmission is:

$$\text{bit rate } f_{b(\text{binary})} = \text{symbol rate } f_s = 2f_N. \quad (2.2)$$

Hence, the maximum bit rate in a binary transmission system is constrained by channel bandwidth.

In M-level pulse amplitude modulation (M-PAM), one symbol contains $\log_2 M$ bits of information. Therefore, the maximum bit rate in M-PAM transmission is:

$$\text{bit rate } f_{b(\text{M_PAM})} = n f_s = (\log_2 M) f_s = 2 f_N (\log_2 M). \quad (2.3)$$

From equations (2.2) and (2.3), it is clear that, in order to ensure maximum data transmission, one has to increase the transmission channel's bandwidth and/or use multi-level signaling techniques. However, in reality, the above ideal Nyquist transmission systems are difficult to achieve due to the frequency dependent loss of the backplane channel. An infinite number of filter sections would be required to synthesize the infinite attenuation slope of the brick-wall channel. In addition, in multi-level signaling, SNR is sacrificed for a narrower bandwidth requirement. Thus, Nyquist introduced a theorem on vestigial symmetry (Nyquist's second theorem).

2.1.2 Nyquist's Second Theorem (Vestigial Symmetry Theorem)

Nyquist's Vestigial Symmetry Theorem states that "The addition of a skew-symmetrical, real-valued transmittance function $Y(\omega)$ to the transmittance of the ideal low-pass filter maintains the zero-axis crossing of the impulse response. These zero-axis crossings provide the necessary condition for ISI-free transmission. The symmetry of $Y(\omega)$ about the cutoff frequency ω_N (Nyquist radian frequency $\omega_N = 2\pi f_N$) of the linear-phase brick-wall filter is defined by

$$Y(\omega_N - x) = -Y(\omega_N + x) \quad 0 < x < \omega_N$$

where $\omega_N = 2\pi f_N$ ".

A raised cosine function satisfies Nyquist's vestigial symmetry requirement. A larger roll-off factor α corresponds to a gradual cut-off of the transfer function compared with an ideal low-pass filter (corresponding to $\alpha = 0$) [26]. Theoretically, Nyquist's $\alpha = 1$ roll-off raised-cosine channel could lead to the simultaneous ISI and transition jitter free data transmission. However, the $\alpha = 1$ raised-cosine channel requires that the channel's impulse response has zero crossings at half of the symbol periods in addition to the usual zero crossings at integers of the symbol period. Therefore, in practice, a 2x sampling clock is required for the simultaneous bit-center and bit-edge equalization.

Moreover, the described Nyquist's minimum bandwidth and vestigial symmetry theorems all assume that the channel's phase response is linear. However, a real channel's nonlinear phase distortion at high frequencies would add more difficulties in achieving the simultaneous ISI and transition jitter free data transmission, as discussed in sections 2.2.2 and 5.3. This *nonlinear phase distortion* causes severe post-cursor signal distortion where the received data eyes are no longer peaked at bit centers and the eye diagrams are no longer symmetric. Thus, a half symbol-spaced FIR (HSSF) filter, as required for simultaneous ISI and transition jitter-free equalization, is more difficult to implement than a symbol-spaced FIR (SSF) filter at high frequencies where the channel's group delay distortion is crucial.

2.1.3 Eye Diagram Fundamentals

To evaluate the performance of a transmission system, eye diagrams are usually used. An open eye pattern corresponds to a minimal signal distortion [26]. The overlapped signal pattern does not cross the horizontal zero line at exact integer multiples of the sym-

bol period. The deviation from the nominal crossing points is known as the data transition jitter. This jitter has an effect on the timing recovery circuits.

Many communication links are also judged on their bit-error-rate (BER) performance, i.e., how many bits are received in error. Like a test at school, a BER tester will tell you the link's test score, whether 9 out of 10, or 1 out of 10. Unfortunately, BER doesn't tell the qualitative information on why that score was achieved, or how to get a better score. Thus, people have traditionally turned to sampling oscilloscopes to show eye diagrams.

Eye diagrams are an intuitive way of viewing parametric performance. If done correctly, eye diagrams should show every possible pattern combination overlaid, one on top of the other. With all combinations in one place, it becomes easy to see when rise time is too slow, when overshoot is present, or when the eye is being closed due to jitter. Therefore, in this research, eye diagram simulation is used to evaluate the link performance in combination with simulations of convergence errors and coefficient value variations to verify that the system is stable while evaluating the link performance.

2.2 Backplane Channel Characteristics

In many backplane applications, data are often communicated by transmitting an electrical signal from one line card to another via copper traces. Due to the skin-effect loss and dielectric loss, copper traces show a low-pass frequency response that limits the transmission channel bandwidth.

Figure 2.1 shows an example of the configuration of a backplane transceiver link[24].

Figure 2.1 Configuration of Backplane Network [24]

The signal loss, or attenuation, in a backplane channel is primarily composed of conductor and dielectric loss. The conductor loss has two components: the DC loss which is independent of frequency, and the skin effect loss which is proportional to square root of frequency. For standard FR4 printed circuit board (PCB) material, dielectric loss, which is proportional to frequency, becomes dominant above 2.5GHz.

The higher the frequency and the longer the PCB trace, the greater the signal loss. This is also known as the bandwidth limitation of the channel. At low frequencies, skin effect is the dominant loss. However, at frequencies higher than 2.5GHz, dielectric loss begins to dominate. Both the skin effect and dielectric loss are frequency dependent and can cause inter-symbol interference (ISI), because the attenuation of the channel prevents a pulse representing a bit from reaching the full strength within its symbol period, causing the pulse to spread into adjacent symbols.

2.2.1 The Effect of Channel Amplitude Attenuation on High-Speed Backplane Data Transmission

In this research, a typical Tyco 34" (30" trace and 2×2 " connector) FR4 backplane channel was used as the comparison benchmark, and a Matlab script based on [9] was used as the link simulation tool. The amplitude attenuation of the backplane channel as a function of frequency is illustrated in Figure 2.2(a). Figure 2.2(b) illustrates a short bit stream of non-return-to-zero (NRZ) data transmitted over the backplane channel at a rate of 10Gbps by the transmitter (TX) driver and the corresponding received signal at the far end of the channel.

Figure 2.2 (a) Attenuation of channel as a function of frequency
(b) Transmitted and received bit stream

Figure 2.2 shows that the transmitted signal is attenuated by the backplane channel. Because of the dispersion in the attenuation (caused by the frequency dependency of the conductor and dielectric losses), the response to a single bit is several bit lengths long. This dispersion in the attenuation results in ISI, which implies that the voltage level of a

bit at the receiver is determined not only by the value (0 or 1) of the current bit, but also by the value of the previous bits. The level of a 0 to 1 transition following a number of consecutive 1's is different from the level of that same transition following a number of consecutive 0's [27].

2.2.2 The Effect of Channel Group Delay Distortion on High-Speed Backplane Data Transmission

In backplane data transmission, skin effect, dielectric loss and reflections in the backplane channel cause frequency dependent attenuation and nonlinear phase dispersion [4]. A pulse representing a bit may not reach its full strength within a symbol period due to channel attenuation. The pulse will spread into adjacent symbols and cause ISI. In addition to pulse widening due to the channel's frequency dependent attenuation, the channel's nonlinear phase dispersion results in post-cursor signal distortions where the peak of the pulse representing a bit is no longer at the center of a bit time period. The channel's nonlinear phase dispersion is often measured by channel group delay distortion, which is another ISI contributor in addition to amplitude attenuation. Thus, there is a requirement to study both the amplitude response and the group delay response of transmission channels. This section presents a discussion of the backplane channel's group delay characteristics, and the impact of group delay distortion on channel's impulse / pulse response and the received data eye diagrams.

1) Definition of Phase Delay and Group Delay

Both phase delay and group delay are related to the phase response of the transmission channel. The phase delay of a linear time-invariant (LTI) system $H(z)$ with phase response $\Phi(\omega)$ is defined by

$$P(\omega) \triangleq -\frac{\Phi(\omega)}{\omega}, \text{ or } P(f) = -\frac{\Phi(f)}{2\pi f}, \quad (2.4)$$

while the group delay is defined by

$$D(\omega) \triangleq -\frac{d}{d\omega}\Phi(\omega), \text{ or } D(f) = -\frac{1}{2\pi} \cdot \frac{d}{df}\Phi(f). \quad (2.5)$$

If the input to a LTI system with frequency response $G(j\omega) = |G(j\omega)|e^{j\Phi(\omega)}$ is a complex sinusoid of unit amplitude, $x(t) = e^{j\omega t}$, then the output is

$$y(t) = G(j\omega)e^{j\omega t} = [|G(j\omega)|e^{j\Phi(\omega)}]e^{j\omega t} = |G(j\omega)|e^{j\omega[t + \Phi(\omega)/\omega]} = |G(j\omega)|e^{j\omega[t - P(\omega)]} \quad (2.6)$$

From equation (2.6), it can be seen that the phase delay expresses the channel phase response as a time delay.

When the channel's phase response $\Phi(f)$ is linear with frequency, both the phase delay and the group delay evaluate to a constant delay. If the amplitude response of the channel is nearly constant (i.e., $|G(\omega)| \approx 1$) over the bandwidth of an input signal, the output signal will be identical to the input signal, except that the output signal will have a time shift because of the linear phase delay. When the channel's phase response is nonlin-

ear with frequency, neither the phase delay nor the group delay is constant with frequency. Thus, the output signal will be distorted. The total delay of the transmission channel is often unimportant. However, the group delay distortion represents the channel's nonlinear phase distortion, which results in post-cursor signal distortions and adds jitters to the received data eyes. The received data eyes are no longer peaked at bit centers, and the eye diagrams are no longer symmetric.

Therefore, phase delay distortion represents the nonlinearity of the channel's phase response, and is expressed in units of time relative to frequency. Phase delay distortion often is measured by group delay distortion, which is the derivative of the phase shift with respect to frequency as defined in equation (2.5).

2) Group Delay Response of the Backplane Channel

For the purpose of demonstration, the typical Tyco 34" FR4 backplane channel was used as the working subject, and a Matlab script based on [9] was generated as the link simulation tool. Figure 2.3(a) shows the channel's amplitude response and group delay response. Figure 2.3(b) is a zoom of the channel's amplitude attenuation and group delay distortion at high frequencies. The channel's group delay response is composed of a constant group delay (D) and the deviations from this constant group delay (ΔD), as shown in Figure 2.3(b). The constant group delay results in a total delay of the received signal, as shown in Figure 2.4(a). This total delay determines the recovered clock phase at the receiver. The deviation (or distortion) from the constant group delay is the channel's group delay distortion, which reflects the channel's nonlinear phase distortion. The group delay distortion results in the post-cursor signal distortion, which is also a major ISI con-

tributor in addition to amplitude attenuation and requires an optimal sampling phase to compensate.

Figure 2.3 Tyco 34" FR4 Backplane Channel Frequency Response
(a) Amplitude response and group delay response (b) A zoom of Figure 2.3(a)

3) The Impact of Group Delay Distortion on the Impulse /Pulse Response of the Backplane Channel

Figure 2.4 shows the channel's impulse response. In Figure 2.4, the negative frequency component of the channel's transfer function was removed. Figure 2.4(a) shows the channel's impulse response at 12Gbps. From Figure 2.4(a), it can be seen that the impulse response is attenuated and symmetrically dispersed when the channel's group delay is constant. The differences in constant group delay result in a shift of the impulse response in time, but the shape of the impulse response remains the same. However, the impulse response is further distorted and becomes asymmetrical when the frequency-dependent group delay distortion is added. Figure 2.4(b) shows the channel's impulse

response with a constant group delay $D = 6.5625\text{ns}$ at different speed. From Figure 2.4(b), it can be seen that the impulse response is attenuated and symmetrically dispersed due to the channel's frequency-dependent attenuation. But the peak of the impulse response appears at the same time as the constant group delay ($D = 6.5625\text{ns}$).

Figure 2.4 Tyco 34'' FR4 Backplane Channel Impulse Response

(a) With and without group delay distortion at 12Gbps

(b) With a constant group delay $D = 6.5625\text{ns}$ at different speed

The normalized pulse responses of the backplane channel to an ideal trapezoidal pulse at 3.125Gbps, 5Gbps, 10Gbps, and 12Gbps data rates are shown in Figure 2.5. From Figure 2.5, it can be seen that as the data rate increases, a pulse representing a bit not only gets delayed and attenuated in amplitude by the backplane channel, but is distorted where the peak of the pulse representing a bit is no longer at the center of a bit time period due to the channel's severe group delay distortion at high frequencies. The resulting long tail of the pulse can cause more severe post-cursor ISI, degrading the received data eye opening as shown in Figure 2.6.

Figure 2.5 Pulse Response with Channel Group Delay Distortion

4) The Impact of Group Delay Distortion on the Channel's Far-End Data Eye Diagrams

Figure 2.6 shows the channel's far-end eye diagrams at a data rate of 3.125Gbps with and without group delay distortion. With group delay distortion (as seen in Figure 2.6(a)), the peak of the bit-center (BC) eye is not at the center of a bit time period where $n_d = 0$, and the bit-edge (BE) eye is not symmetric against the bit edges where $n_d = \pm 0.5 \text{ UI}$. This asymmetry implies signal distortion that further degrades the far-end eye opening. This signal distortion results in the far-end eye closure at both the bit centers and bit edges compared to the far-end eyes as shown in Figure 2.6(b), where the group delay distortion was ignored.

Figure 2.6 Tyco 34'' FR4 Channel Far-End Eye Diagrams at 3.125Gbps Data Rate
 (a) With phase (group) delay distortion (b) Without phase (group) delay distortion

Overall, the backplane channel's amplitude attenuation and group delay distortion cause ISI at high data rates, which in turn causes error in data recovery at the receiver. Hence, the data transmission rate and distance are limited. In addition to the data recovery error, ISI together with other non-ideal characteristics of the backplane channel also cause difficulty in clock recovery as the data rate of integrated circuits advances past the Gb/s rate. Thus, channel equalization has become an essential block of the high-speed backplane data transmission link in order to restore timing information and to achieve lower bit-error-rate (BER) data communications.

2.3 Channel Equalization Techniques

The data transmission over a backplane channel can be improved by adding an equalizer to the link to compensate for the channel frequency-dependent loss. Channel equalization eliminates the problem of frequency-dependent attenuation by filtering the

transmitted or received signal so the concatenation of the equalizing filter and the transmission channel gives a flat frequency response.

There exists a number of different equalization techniques: transmitter pre-emphasis/de-emphasis and/or receiver equalization, bit-edge equalization (BEE) or bit-center equalization (BCE), amplitude modulation or phase modulation, and using symbol spaced FIR (SSF) filter or fractional symbol spaced FIR (FSSF) filter, etc. To achieve the best system performance, a proper channel equalization scheme is required. This section reviews some commonly used channel equalization techniques from literature. A few recently published BEE schemes are studied.

2.3.1 Transmitter Equalization vs. Receiver Equalization

An equalizer can be implemented either at the transmitter side, referred to as pre-emphasis or de-emphasis, or at the receiver side, referred to as the receiver equalizer or simply the equalizer. Both techniques seek to either emphasize the high-frequency components or de-emphasize the low-frequency components of the transmitted or received signal in order to compensate for the effect that the high-frequency components are attenuated more than the low-frequency components through the channel.

Transmitter (TX) pre-emphasis/de-emphasis is relatively easier to be implemented compared with a receiver (RX) equalizer. However, it is complicated to incorporate an adaptive algorithm into the TX pre-emphasizer/de-emphasizer since there is no channel characteristic information at the transmitter end. In addition, to alleviate the near-end crosstalk (NEXT) problems that result from emphasizing high-frequency components at the transmitter end, de-emphasis is generally used. De-emphasis not only reduces the

power of low-frequency components of the transmitted signal, but also reduces the power of the received signal.

Receiver equalization may also be used to open the received data eye in a back-plane serial link. In receiver equalization, the signal is transmitted without any special processing but compensated at the receiver by using filtering techniques. In general, receiver equalization is implemented using a high-pass filter. Receiver equalization can be either analog or digital, and passive or active.

Receiver equalizers are generally more complex than transmitter pre-emphasizers / de-emphasizers. But at the receiver side, it is possible to infer the channel's characteristics from the received signal and to implement dynamic equalization to compensate for channel characteristic variations. To achieve the best system performance, a proper channel equalization scheme is required.

1) Transmitter (TX) Pre-Emphasis

When the channel characteristics can be anticipated, which is the case in this research, TX pre-emphasis can be used. The objective of TX pre-emphasis is to flatten the frequency response of the channel and increase the channel bandwidth, so as to reduce the ISI.

Pre-emphasis operates by boosting the high frequency energy whenever there is a transition in the data while reducing the low frequency energy where there is no transitions. Pre-emphasis adds additional output current during the transition of the bit. This increasing of current tends to speed up the transition edge's rising and falling time, and

also provides a bit of over-shoot to the signal at the driver output. Since high frequency components are attenuated more than lower frequency components, by TX pre-emphasizing, an equalized eye will be presented at the receiver side that enables the receiver to recover the signal more easily.

To illustrate, an SSF filter with only one post tap for simplicity was used as the TX pre-emphasis for the typical Tyco 34" FR4 backplane channel. Figure 2.7(a) shows a short bit stream transmitted by a regular driver and by a pre-emphasis driver. A pre-emphasis driver boosts the voltage level of the bit following a transition. The frequency response of an equivalent equalizer is shown in Figure 2.7(b). Boosting the voltage level of the bit following a transition results in an amplification of the power at higher frequencies, which compensates for the higher losses in the channel at these higher frequencies. Thus, the attenuation of the signal and the ISI are reduced, and the eye pattern improves as shown in Figure 2.8.

Figure 2.7 (a) Short bit stream transmitted by a regular driver and by a pre-emphasis driver (b) Equivalent equalizer frequency response

Evidently, a pre-emphasis driver uses more power than a driver without pre-emphasis. However, since only the power at transitions (i.e. at the higher frequencies) is increased, power consumption is less than what would be required for a regular driver with peak-to-peak voltage V_{PE} . The power consumption and the efficiency of the equalization are a function of V_{PE} . Boosting results in large signal swings which are difficult to implement, consume power and often present EMI challenges. Therefore, in practice, the maximum amount of boost that can be achieved is limited [27].

Figure 2.8 Received Bit Stream and Eye Pattern for a PRBS Signal with Pre-Emphasis
(a) Received bit stream @10Gbps (b) Eye diagram with pre-emphasis

A commonly used pre-emphasis driver is a discrete-time SSF filter. It is often implemented with direct current summing of different taps at the driver's output [28]. The SSF filter reduces ISI by inverting the channel's low-pass characteristic. The higher the boost given by the driver, the more the received eye pattern could be open. However, too much pre-emphasis can also be of concern. A large signal at TX could generate more noise and crosstalk, and increases power dissipation. One can define an optimal boost as the amount of boost needed to make the tail of the pulse response as short as possible.

2) Transmitter (TX) De-Emphasis

The problem of the higher power consumption and larger voltage swings associated with a TX pre-emphasis driver can be overcome by using de-emphasis. With a de-emphasis driver, the peak-to-peak voltage is the same as with a regular driver, but the voltage level of the bits not following a transition is attenuated more than that with a pre-emphasis driver. This is equivalent to boosting the voltage level of the bit following a transition, except now the voltage swings during a transition are the same as with a regular driver, and the power consumption is even less than with a regular driver since the power at the lower frequencies is attenuated. Figure 2.9(a) illustrates a short bit stream at the output of a regular driver and of a de-emphasis driver. The frequency response of an equivalent de-emphasis equalizer is shown in Figure 2.9(b).

Figure 2.9 (a) Short bit stream transmitted by a regular driver and by a de-emphasis driver (b) Equivalent equalizer frequency response

Figure 2.10 shows the received bit stream and the eye pattern for a PRBS signal with TX de-emphasis. Although the amplitude of the received signal in the case of using a

TX de-emphasis driver is smaller than that of using a regular driver, the eye pattern with the de-emphasis driver is more open than that with a regular driver. The de-emphasis driver reduces the dispersion in the attenuation of the channel by attenuating the lower frequency components. This reduction of dispersion in turn reduces the ISI and therefore the eye pattern is improved.

Because of the additional losses that are induced, de-emphasis is only useful in applications with a large signal swing at the driver and a sensitive receiver [27].

Figure 2.10 Received Bit Stream and Eye Pattern for a PRBS Signal with De-Emphasis
(a) Received bit stream @10Gbps (b) Eye diagram with de-emphasis

3) Analog Design vs. Digital Design in Receiver (RX) Equalization

Analog techniques use linear filter circuits, such as RC filters, to reverse the low pass effect of the backplane channel with a high pass filter to recover and restore the original signal. Its net effects are similar to that of pre-emphasis in opening the received data eye. Digital techniques use digital filters and analog to digital conversion for equalization.

A digital equalizer is equivalent to applying pre-emphasis techniques at the receive end of the channel.

Sometimes it is beneficial to place the equalizer at the receiver. Although a discrete-time FIR approach can be used, it is significantly more complicated than transmitter pre-emphasis since high-speed sampling, multiplication, and addition of analog values are required.

The main advantages of analog equalization are lower power, less silicon area, and capability of performing equalization at high speeds. Unfortunately, analog compensation of the channel frequency response comes at the expense of reduced SNR. For systems with analog equalization, careful system design should be performed to minimize deterministic high-frequency noise such as crosstalk and supply induced noise.

Digital receiver equalizers, using FIR filters, require high-resolution sampling ADCs that run at GHz speeds. The development of GHz rate ADCs is quite a challenging task. On the other hand, the disadvantage with analog continuous time equalization is the requirement of very wide-bandwidth front-end receiver circuits that run at the same speed as the input data.

4) Passive Design vs. Active Design in Receiver (RX) Equalization

Receiver equalizers can also be either passive or active circuits. Passive equalizers don't suffer from additional power consumption and the associated thermal requirements. However, the frequency range over which equalization can be achieved is larger when

using active equalizers. Active equalizers can amplify the power at higher frequencies, while passive circuits can only attenuate the power at the lower frequencies [27].

A passive equalization filter is made up of a number of lumped elements (resistors, inductors and capacitors). Because it induces additional losses, like de-emphasis, passive equalization is only used in applications with a large signal swing at the driver and a sensitive receiver [27].

An alternative is an active high-pass filter. Figure 2.11 shows an example circuit. The gain of this circuit goes up with frequency as the capacitor decreases the amount of source degeneration. The equalization gain can be adjusted through the variable resistors [28].

Figure 2.11 Active RC-Based Receiver Equalization

When maximum performance (i.e. the longest interconnection length) is needed, active receive equalizers must be used since active equalizers provide the greatest practical boost. An adaptive active equalizer circuit improves transmission over an interconnection link by compensating for the attenuation [27].

However, active receive equalizers often add additional timing jitter to the receiver output eye pattern. The amount of timing jitter that is being added can be reduced by adding a clock data recovery (CDR) circuit to the output of the equalizer. Active receiver equalization is normally more difficult to implement at high speed than transmitter pre-emphasis.

5) Receiver Equalization with DFE

Receiver based decision feedback equalization (DFE) may also be used for the removal of dispersion based ISI. A non-linear filter, such as a DFE, can further improve the margin by equalizing the signal without amplifying the crosstalk. In contrast, a high-pass linear filter commonly used to equalize the channel amplifies the high-pass crosstalk significantly [28]. However, error propagation and pre-cursor ISI are the issues when using DFE.

6) Transmitter Pre-Emphasis and Receiver Equalization Combo

The equalization techniques discussed above have a net effect of flattening the channel's amplitude response and improving the received data eye-opening. In some cases, however, the system requires a combination of transmitter pre-emphasis and receiver equalization.

High speed links often use pre-emphasis (PE) at the transmitter, DFE at the receiver, and near-end (NE) crosstalk cancellation for bidirectional links. The PE filter can improve channel's far-end signal integrity by boosting the high-frequency components of the transmitted signal. However, this boosting exacerbates near-end crosstalk and places

greater demands on the NE filter. The DFE can correct many of the same effects of ISI as with the PE filter, without incurring the PE's downsides of increased power consumption and near-end crosstalk. However, the DFE is sensitive to errors in the received data stream.

Overall, the transmitter pre-emphasis and the receiver equalization essentially accomplish similar functions, but they are implemented differently. Choosing the right equalization technique depends on the application. Pre-emphasis is preferred over receiver equalization if crosstalk is not a factor in the transmission channel. Otherwise pre-emphasis will make crosstalk more pronounced due to amplified transmitted signals. Receiver equalization is preferred over transmitter pre-emphasis if the signal-to-noise ratio (SNR) is not a factor in the transmission channel. Otherwise, receiver equalization will amplify the noise transmitted across the transmission channel at the receiver. The transmitter pre-emphasis is simple and effective for very high data rate design. However, receiver equalization also has an advantage over pre-emphasis, i.e., it can be adaptive.

At multi-gigabit per second data rate, transmitter pre-emphasis is typically implemented by current summation in the high-speed transmitter current mode driver using Current Mode Logic (CML) techniques. This method results in a small power overhead compared to a regular driver without pre-emphasis. Receiver equalization, however, requires dedicated high-power circuits to perform equalization, which consumes additional power on top of the power dissipated in the current mode transmitter driver. Transmitter pre-emphasis is useful when channel characteristics are known. Otherwise, adaptive receiver equalization is a choice.

2.3.2 Symbol Spaced FIR (SSF) Filter vs. Fractional Symbol Spaced FIR (FSSF) Filter

The structure of an FIR filter is shown in Figure 2.12.

Figure 2.12 FIR Filter Structure

For a symbol spaced FIR (SSF) filter, the delay T_D is equal to one symbol period

T . The transfer function of the FIR filter can be written in the z-domain as

$$H(z) = \sum_{n=0}^{N-1} c_n \cdot z^{-n} \quad (2.7)$$

where c_n are the tap coefficients and $z = e^{j2\pi f/f_s}$.

The sampling frequency is $f_s = \frac{1}{T}$ for SSF. The performance of an SSF filter is

limited by aliasing, as a result of sampling at $1/T$. It cannot compensate for channel impairments beyond the sampling frequency $f_s = 1/T$.

For a fractional symbol spaced FIR (FSSF) filter, T_D is equal to a fraction of T ,

$$T_D = mT/n \text{ (} m \text{ and } n \text{ are integers, and } m < n \text{). The sampling frequency is } f_s = \frac{n}{mT}$$

for FSSF. An FSSF filter can sample the input signal at a fraction of T and thus extends the compensation beyond $1/T$.

A commonly used FSSF filter is the half-symbol spaced FIR (HSSF) filter [9], [10] that samples at both the bit centers and the bit edges, and forces the transition voltage level to be half of the signal amplitude. Theoretically, an HSSF filter samples at a half of T and thus extends the compensation beyond $1/T$. However, an HSSF filter needs double of the tap numbers compared to an SSF filter to cover the same ISI time span. Doubling the tap numbers implies an increasing of power consumption in circuit implementation. In the mean time, an HSSF filter needs double of the sampling clock frequency compared to an SSF filter. At a 10Gbps data rate, an HSSF filter implies a 20GHz sampling clock frequency which is difficult in circuit implementation. Though a multi-phase clock can be used to reduce the required clock frequency [23], the structure is complicated.

Moreover, the channel's nonlinear phase dispersion at high data rates results in severe post-cursor signal distortions where the peak of the pulse representing a bit is no longer at the center of a bit time period and the eye diagrams are no longer symmetric. This severe post-cursor signal distortion adds difficulties to the HSSF filter optimization. The HSSF filters in [9] and [10] can't guarantee convergence, and leads to large filter coefficient variations.

2.3.3 Bit-Edge Equalization (BEE) vs. Bit-Center Equalization (BCE)

Conventional channel equalization improves link performance by minimizing ISI at bit centers, and the filter coefficients are adapted based on error information collected at the bit-center sampling instant. This conventional bit-center equalization (BCE) approach makes the assumption that ISI is only important at the bit-center sampling points, and the pulse representing a bit always peaks at the bit center. Such assumption is appropriate only for low-speed systems where the jitter is insignificant. But at a high data rate, severe channel group delay distortion represents the backplane channel's nonlinear phase dispersion, which is another ISI contributor in addition to amplitude attenuation. This nonlinear phase dispersion causes severe post-cursor signal distortion. The received data eyes are no longer peaked at bit centers, and the eye diagrams are no longer symmetric. On the other hand, an FIR filter based on amplitude modulation not only changes pulse amplitudes, but also changes the slopes of the pulse rising and falling edges. Therefore, even though zero forcing received data bit centers is effective in correcting ISI at the sampling points, more jitter could be injected at the transition edges if the data eyes are not symmetric, which results in a reduction in the timing margin.

Recent I/O standards such as IEEE 802.3ap have suggested the possibility of equalizing the data bit edges [11], [12] instead of equalizing the data bit centers as in the conventional BCE [5], [6]. In contrast to BCE, the bit-edge equalization (BEE) uses the error information collected at the bit edges. It tries to minimize the ISI distribution at the transitions of the data. Previous publications [11]-[15] have shown that edge equalization reduces ISI at bit edges. However, those previous publications again took the centers of the bit time periods as the optimal bit center sampling points, and ± 0.5 unit interval (UI)

away from the centers of the bit time periods as the optimal bit edge sampling points. This is not suitable at high data rates when the received data eyes are no longer peaked at bit centers and the eye diagrams are no longer symmetric. Thus, neither the bit-center equalization nor the bit-edge equalization is optimized.

In addition, the symbol-spaced edge-only equalization approach proposed in [12] demonstrates that the received bit-edge equalized signal has larger eye opening at bit edges than those at bit centers using either the bit-edge zero-forcing equalization (BE-ZFE) approach or the bit-center zero-forcing equalization (BC-ZFE) approach. This enlarged eye opening at the bit edges implies that one should use the 3-level bit-edge equalized signal for both clock and data recovery instead of using the bit edge for clock recovery and the bit center for data recovery. However, in [12], the author left the question of how to detect the original binary data from the received 3-level bit-edge equalized signal to readers. The various BEE schemes presented in [10]-[15] all use bit centers as the data sampling points. Therefore, solutions for decoding the original binary data from the 3-level bit-edge equalized signal are required. This decoding problem can be resolved by pre-coding a data sequence at the transmitter side as shown in Chapter 4.

2.3.4 Amplitude-Optimized BEE vs. Phase-Optimized BEE

Edge equalization can be used to minimize ISI at zero crossing transition edges. Based on different error derivation approaches, edge equalization falls into two categories: amplitude-optimized and phase-optimized, as illustrated in Figure 2.13. The amplitude-optimized edge equalization performs equalization by looking at the amplitudes of data that occur at the bit edges of a data signal and seeks to drive those associated error terms to

zero [10], [12]-[13], [23]. Phase-optimized edge equalization is a different way of thinking channel equalization by compensating for the nonlinear phase delay instead of amplitude attenuation. The difficulty in phase-optimized edge equalization is that the reference zero crossing points will shift in time with different data patterns and transmission rates. Therefore, complicated algorithms are required to achieve phase equalization [14]-[15]. This section reviews some of the commonly used BEE schemes reported in the recent years.

Figure 2.13 Error Derivation in Amplitude-Optimized and Phase-Optimized Edge Equalization (a) Amplitude-optimized edge equalization
(b) Phase-optimized edge equalization

1) Amplitude-Optimized Bit-Edge Equalization (BEE)

The amplitude-optimized BEE performs equalization by looking at the amplitudes of data that occur at the bit edges of a data signal and seeks to drive those associated error terms to zero. Based on this criteria, different equalization strategies have been reported recently [10], [12]-[13], [23].

a) Symbol-Spaced Edge-Only FIR Equalizer [12]:

Using the classical symbol-spaced feed-forward equalizer (FFE) at the transmit side, the criteria of the symbol-spaced edge-only FIR equalizer as presented in [12] is to

drive the equalized pulse response to have zero error at the bit edges, i.e., bit-edge zero-forcing equalization (BE-ZFE).

Unlike the traditional bit-center zero-forcing equalization (BC-ZFE) which takes values of the pulse response at the bit centers of the adjacent and neighboring bit periods and drives the associated error terms to zero, in the BE-ZFE, the bit edges of each bit period is maintained to have a zero crossing except that the bit edges immediately adjacent to the bit period in which the pulse of interest is located are not forced to zero.

The simulation results presented in [12] demonstrate that this edge-only equalization requires less frequency boost and bandwidth compared to both the classical BC-ZFE and duobinary signaling. When scaled for equal TX power, the received bit-edge equalized signal has the largest eye opening at bit edges than those at bit centers using BE-ZFE, BC-ZFE, or duobinary signaling. This enlarged eye opening at the bit edges implies that one should use the 3-level bit-edge equalized signal for both the clock and data recovery instead of using the bit edge for clock recovery and bit center for data recovery. However, in [12], the author left the question of how to detect the original binary signal from the received 3-level bit-edge equalized signal to readers. This problem can be resolved by pre-coding a data sequence at TX using the proposed BEE as shown in Chapter 4.

In addition, since the edge-only FIR equalizer in [12] was used at the transmitter side, noise enhancement could be an issue when using the zero-forcing algorithm.

b) X2 Oversampled Equalizer [23]:

The X2 oversampled equalizer as presented in [23] consists of two 5-tap SSF filters, one for bit-center equalization and the other for bit-edge equalization as illustrated in

Figure 2.14. The two 5-tap SSF filters are in parallel with shorted outputs at TX to improve the total vertical eye-opening by adding the bit-center equalized signal together with the bit-edge equalized signal. However, since the equalizer is used at the TX, this improvement of vertical eye-opening is limited by the TX peak-power constraints, especially in the submicron CMOS technologies. Moreover, the sampling phases as described in [23] are fixed at either the centers of the bit time periods as the bit-center sampling phase, or $\pm 0.5\text{UI}$ away from the centers of the bit time periods as the bit-edge sampling phase, which might not be the optimum sampling phase for both the bit-center equalization and the bit-edge equalization due to the channel's group delay effects at high frequencies where the received data eyes are not peaked at the centers of the bit time periods and the eye diagrams are no longer symmetric. The equalization approach in [23] could introduce more jitter if the bit-edge equalized signal is not perfectly aligned with the bit-center equalized signal, especially when neither the bit-center equalization nor the bit-edge equalization is optimized.

Figure 2.14 An X2 Oversampled Equalizer [23]

The sampling approach used in [23] is equivalent to that used for an HSSF filter, which samples at both the bit centers and bit edges and forces the transition voltage level to be half of the signal amplitude. An HSSF filter needs double of the tap numbers compared to an SSF filter to cover the same ISI time span. Doubling the tap numbers implies an increasing of power consumption in circuit implementation. In the mean time, an HSSF filter needs double of the sampling clock frequency compared to an SSF filter, which is difficult in circuit implementation at high frequencies. In [23], a multi-phase clock was used to reduce the required clock frequency. Each 5-tap filter uses a 4-phase clock to multiplex one-fourth-rate parallel input data. The clock phase difference between these equalizers is 45° , which corresponds to a half symbol period. The entire transceiver architecture introduced in [23] is complicated.

Furthermore, due to the channel's group delay distortion at high frequencies, the HSSF sampling approach used in [23] cannot guarantee convergence and could lead to large filter coefficient variations, as described in section 2.3.2.

c) Half-Symbol-Spaced TX FIR Edge Equalizer [10]:

Instead of using an FIR equalizer with a symbol-spaced delay chain to cancel the bit-edge ISI, the TX FIR edge equalizer as presented in [10] uses a half-symbol-spaced delay chain (denoted XFIR) that samples at both the bit centers and the bit edges, and zero-forces the transition voltage level to be half of the signal amplitude. Unlike the parallel structure in [23], this XFIR uses a single half-symbol-spaced delay chain for both bit-center and bit-edge equalizations. By defining the desired bit-edge sample values in the XFIR equalizer, the timing margin is enlarged. However, this larger time margin is at the

expense of the vertical eye opening. The XFIR in [10] can't guarantee convergence, and leads to large coefficient variations.

d) Half-Symbol-Spaced DFE Edge Equalizer [13]:

The half-symbol-spaced DFE (denoted Type 1 XDFF) in [13] is a similar implementation to the XFIR [10], which uses half-symbol delay taps, and therefore the similar trade-off as of the XFIR. Using a double rate DFE to equalize the bit edges is theoretically feasible but not practical due to the feedback delay.

e) Symbol-Spaced DFE with Edge Equalizer [13]:

The symbol-spaced DFE with edge equalizer (denoted Type 2 XDFF) as presented in [13] uses separated parallel equalizers for the bit-center equalization (i.e., the data path) and the bit-edge equalization (i.e., the transition path). In this type 2 XDFF, the bit-center equalizer is exactly the same as a conventional DFE, so voltage margin is not affected by the bit-edge equalizer. The bit-edge equalizer cleans the edge samples for the CDR. The type 2 XDFF decouples the trade-offs between timing and voltage margins by having two separated equalizers. Theoretically, since the type 2 XDFF cleans up the transition information without affecting the original bit-center eye, it achieves better BER than conventional DFE. However, similar to the X2 oversampled equalizer as in [23], the drawback of this type 2 XDFF is that the parallel structure in [13] could introduce more jitter if the bit-edge equalized signal is not perfectly aligned with the bit-center equalized signal, especially when neither the bit-center equalization nor the bit-edge equalization is optimized. The type 2 XDFF in [13] can't guarantee convergence. In addition, a RX discrete-time

FIR filter is more difficult to be implemented than a TX FIR filter. The transceiver architecture introduced in [13] is complicated.

2) Phase-Optimized Edge Equalization

Phase-optimized edge equalization is a different way of doing channel equalization by compensating for phase delay distortion instead of amplitude attenuation. The difficulty in phase-optimized edge equalization is that the reference zero crossing points will shift in time with different data patterns and transmission rates. Therefore, complicated algorithms are required to achieve phase equalization. Recently, phase-optimized edge equalizers using different approaches have been reported [14]-[16].

a) DFE Edge Equalizer with Modified LMS Adaptation Algorithm [14]:

To overcome the convergence problem in using the type 2 XDPE as described in [13], a modified LMS adaptation algorithm is used in [14]. The adaptation for the bit-edge tap coefficients γ_i is a second loop that uses the bit-edge samples in parallel with the bit-center equalizer. In order to converge, an additional constraint is imposed to a blind-LMS algorithm. The adaptation of γ_i is such that it adapts toward a predetermined reference edge. The reference edge position differs depending on the data sequence. By adapting all the other edges without moving the reference edge, the adaptation converges. In order to freeze the reference edge during the adaptation of the other edges, the possible values of γ_i are constrained. The drawback of using the modified LMS adaptation algorithm is that the reference edge position differs depending on the data sequence, which leads to different constraint equations. Therefore, there is a need to use sequence-detection logic, store

bit-center and bit-edge samples, and process the information off-chip. The scheme proposed in [14] introduces a very complicated algorithm and architecture.

b) Phase Pre-Emphasis Equalizer [15]:

The phase pre-emphasis equalizer in [15] is implemented through adjusting the transition time of a data sequence. The detection of each previous transition time is used to compensate the current transition time. The coefficients for the phase pre-emphasis are optimized by sampling the timing deviation at the receiver for particular transmitted data sequences. However, this technique cannot be applied to high loss channel, because the transition may not pass through the slicer threshold. The error would propagate since the adjustment of the current transition time is based on the detection of the previous transition. In addition, complicated logic algorithm is needed.

c) Pulse Width Modulated Equalizer [16]:

The pre-emphasis technique based on pulse-width modulation (PWM) mitigates jitter by shifting the bit edges of a differential signal in time [16]. The PWM scheme proposed in [16] uses phase modulation that eliminates the need for the complicated algorithms as described in [14], [15] by applying PWM to each bit. In this PWM scheme, only one coefficient needs to be set to fit the channel equalizer transfer function and no amplitude modulation is applied, an advantage in low-voltage high-speed CMOS processes. However, this PWM scheme not only shifts data transition edges, but also changes the data pattern that results in a wider data spectrum but with reduced DC and low frequency

content as demonstrated in Chapter 5. This wide PWM data spectrum limits the application of PWM in high-loss channels.

While channel equalization can cancel the frequency dependent part of the channel attenuation and flatten the bandwidth of the channel, it reduces the magnitude of the channel transfer function as well, which results in a reduced magnitude of the received data. The attenuation of the magnitude is ultimately a limiting factor to achieve an even higher data rate. As data rate increases, the level of magnitude attenuation increases as well. Therefore, it is difficult to achieve a high data rate (e.g. 10Gbps) by using channel equalization alone. Thus, applying proper signaling techniques to compress the transmitted data spectrum together with channel equalization is essential.

2.4 Multi-Level Pulse Amplitude Modulation

Multi-level pulse amplitude modulation (M-PAM) is an alternative technique used for increasing the data rate in a band-limited channel. A backplane channel's bandwidth is limited by the channel's frequency-dependent loss. The dielectric and skin effect losses limit the capability of scaling to ever higher symbol rates. Crosstalk, reflections, inter symbol interference (ISI), timing jitter, and substrate noise degrade the signal integrity of real links. Therefore, design for better bandwidth utilization is required. The above discussed channel equalization techniques are based on filtering the transmitted and/or received signal so the concatenation of the equalizing filter and the backplane channel gives a flat frequency response. However, in channel equalization, the magnitude of the attenuation is ultimately a limiting factor for ever increasing the symbol rate.

On the other hand, the M-PAM technique is based on compressing the transmitted data spectrum in order to increase the data transmission rate in a band limited channel. M-PAM converts data by assigning $k = \log_2(M)$ bits to a set of M discrete amplitudes of a transmitted signal. For a given data rate, M -PAM reduces the effective symbol rate by a factor of $k = \log_2(M)$ compared to a conventional binary (2-PAM) system. This symbol rate reduction compresses the data spectrum and reduces not only the ISI in the channel, but also the maximum required on-chip clock frequency [17]. The bandwidth of the transmitted data is predominantly determined by the symbol rate rather than the aggregate data throughput. Thus, this reduction in symbol rate by using M-PAM lowers the bandwidth requirements of the transceiver.

In an M -PAM communication system, the spectral efficiency is $2\log_2(M)$, which increases logarithmically with the number of PAM levels (M). However, with multi-level signaling, the signal-to-noise ratio (SNR) performance is sacrificed for a narrower bandwidth requirement.

In 4-PAM signaling, two bits are transmitted simultaneously, but at one-half of the original symbol rate. If the peak power is maintained, the voltage margin seen at the receiver is reduced by 1/3 (~10dB) as the voltage span is now shared by the four possible symbols. In channels for which the magnitude rolls off at greater than 10dB per octave, 4-PAM signaling may be considered.

Figure 2.15 compares the NRZ 2-PAM (2-Level) and 4-PAM (4-Level) eye diagrams at the same symbol rate. The horizontal eye opening of a 4-PAM signal is less than

that of a 2-PAM signal due to the limited slew rate. Furthermore, the vertical eye opening of a 4-PAM signal is less than 1/3 that of the 2-PAM signal due to the voltage noise at the intermediate level (V_n). Multi-level signaling often requires additional overhead bandwidth to ensure that enough useful transitions are presented for clock recovery. The exact benefit of multi-level signaling needs to be simulated on a per-channel basis [28].

Figure 2.15 A Comparison of 2-PAM and 4-PAM Eye Diagrams

For backplane applications, there remains the need for both 2-PAM and 4-PAM schemes. The criterion for determining whether to use 2-PAM or 4-PAM is based on the difference in signal attenuation at the two frequencies, as depicted in Figure 2.16 [29]. If the amplitude at frequency “ f ” is less than 3x that of “ $2f$ ”, the 2-PAM is the preferred signaling choice, otherwise 4-PAM is the correct choice.

Overall, M-PAM reduces the effective symbol rate by a factor of $k = \log_2(M)$, lowers the bandwidth requirements of the channel, and reduces ISI. The spectral efficiency ($2\log_2 M$) increases logarithmically with the number of PAM levels (M). However, with M-PAM, the SNR is sacrificed for a narrower bandwidth. M-PAM is complex in circuit implementation, and may significantly increase power consumption compared to conventional NRZ 2-PAM. The all level transitions in M-PAM could result in large jitter,

which is a limiting factor for M-PAM application. A higher than 4-level PAM is not practical.

Figure 2.16 The Criterion for Modulation Selection

2.5 Partial Response signaling

Partial response signaling is another alternative approach to compress data spectrum for high data rate transmission over a band-limited backplane channel.

The constraint on a permissible PAM signal as discussed in the previous sections is that the PAM signal should not cause ISI. The PAM signaling based on this criterion can sometimes lead to a complete intolerance of timing errors or to incompatibilities with some channel characteristics. Some of these disadvantages by using the conventional PAM can be removed with partial-response signal (PRS) processing (also known as correlative level coding) wherein the constraint on a transmitted signal is relaxed so as to allow a controlled amount of ISI. One of the merits of partial-response signaling is that the

controlled ISI can be used to shape the system spectrum, for instance, to place nulls in the frequency response. This spectral shaping can make the system less sensitive to timing errors, and potentially allows practical PRS systems to transmit data over the Nyquist bandwidth, a feature not possible with a conventional PAM system.

Duobinary signaling is a type of partial response signaling techniques that compresses the data spectrum by changing the uncorrelated 2-level signal into a correlated 3-level signal. In duobinary signaling, symbol rate is the same as that of an NRZ (2-PAM) signal. Therefore, duobinary signaling is more compatible to an NRZ signal than that of 4-PAM. The spectrum of a duobinary signal is compressed to one half of the spectrum of an NRZ signal with the same transmission rate by redistribution of spectral density into highly concentrated energy density near DC and low frequencies. The 3-level duobinary signal includes only transitions between adjacent levels. Therefore, duobinary signal reduces jitter than that of both NRZ and 4-PAM signals. With TX pre-coding and duobinary coding, the receiver (RX) duobinary to binary decoding depends only on the current received bit. No error propagation occurs. Duobinary signaling also has less SNR loss (relative to NRZ), simplification of implementation, and lower power consumption compared to 4-PAM. Hence, duobinary signaling is gaining more and more interests from researchers [21]-[23], [33].

The idea behind the duobinary signaling is to take advantage of the “natural roll-off response” of the backplane channel, and use it to help shape the data bits that are to be sent to the receiver. However, in these literature [21]-[23], [33], the function of each block in a duobinary system was not clearly describe. In some cases, it’s even misleading. Two questions arise: should the binary to duobinary conversion be completed before or after a

backplane channel, and what's the exact role of the backplane channel on this duobinary data transmission? Different duobinary signaling schemes and sampling approaches can result in different eye opening of the received data at the channel's far end.

Therefore, in order to make good use of the duobinary signaling technique, a thorough understanding of the duobinary system functions is essential. A more detailed discussion of partial response signaling and duobinary coding is presented in chapter 3.

2.6 Summary

This chapter presented a study on the backplane channel's characteristics and how the channel's amplitude attenuation and group delay distortion affect the high-speed data transmission. Some commonly used channel equalization and signaling techniques for mitigating ISI in high-speed data transmission over backplane channels were reviewed.

For this research, since the channel characteristic is known from the measurement results (.s4p files), TX pre-emphasis/de-emphasis can be used for the simplicity in implementation. However, the conventional bit-center-equalized SSF or FSSF / HSSF approaches as discussed in the previous sections are not suitable for high data rate transmission where the backplane channel's group delay distortion is crucial. The backplane channel's severe group delay distortion at high frequencies leads to the severe post-cursor signal distortion, which adds difficulties to the SSF and HSSF optimization. An amplitude-optimized BEE based on HSSF can't guarantee convergence, and leads to large filter coefficient variations. Though the phase-optimized BEE can also be used, complicated algorithms are usually needed to optimize the filter coefficients. In order to eliminate the

need for the complicated algorithms in phase modulation, the PWM scheme proposed in [16] applies simple PWM to each bit of the transmitted differential signal. However, this PWM scheme not only shifts data transition edges, but also changes the data pattern that results in a wider data spectrum but with reduced DC and low frequency content. This wide PWM data spectrum limits the application of PWM in high-loss band-limited channels.

In contrast, the symbol-spaced edge-only equalization approach proposed in [12] demonstrates that the received bit edge equalized signal has the largest eye opening at bit edges than those at bit centers using either the bit-edge zero-forcing equalization (BE-ZFE) approach or the bit-center zero-forcing equalization (BC-ZFE) approach. This enlarged eye opening at the bit edges implies that one should use the 3-level bit-edge equalized signal for both the clock and data recovery instead of using the bit edge for clock recovery and bit center for data recovery. However, in [12], the author left the question of how to detect the original binary data from the received 3-level bit-edge equalized signal to readers. Therefore, the symbol-spaced edge-only equalization approach as presented in [12] is helpful in our research, but solutions for decoding the original binary data from the 3-level bit-edge equalized signal and reducing the impact of group delay distortion are required.

Meanwhile, the magnitude attenuation in channel equalization is ultimately a limiting factor to further increasing the data rate. Thus, applying proper signaling techniques to compress the transmitted data spectrum together with channel equalization is essential. The duobinary signaling technique can be used to accomplish the two tasks of data spectrum compression and simplification of implementation that is suitable for large scale inte-

gration. Additionally, duobinary signaling does not incur nearly as much SNR penalty (relative to NRZ) as 4-PAM, since the 3-level duobinary coding only includes transitions between adjacent levels and has better immunity to crosstalk / reflection than 4-PAM. However, different duobinary signaling schemes and sampling approaches can result in different eye opening of the received data at the far end of the channel. Therefore, in order to make good use of the duobinary signaling technique, a thorough understanding of the duobinary system functions is essential.

The rest of the thesis will start with a discussion of the partial response signaling and duobinary coding as presented in chapter 3, followed by a proposed unique BEE scheme as presented in chapter 4. Simulation results and discussions are included in chapter 5, and conclusions are drawn in chapter 6.

Chapter 3: Partial Response signaling and Duobinary Coding

This chapter discusses the conventional partial response signaling (PRS) systems and compares different PRS schemes. Several desirable properties of a PRS system and their relation to the system transfer function $H(\omega)$ are studied, and a number of useful schemes are presented. Based on the requirements of minimum bandwidth, simplicity and spectral shapes, it is found that the duobinary and modified duobinary schemes are the two best candidates. Thus, a detailed discussion on duobinary and modified duobinary coding, precoding, and system implementation is included in this chapter.

3.1 Introduction to Partial Response signaling

An ideal and noiseless system (ideal in that there is no distortion due to channel imperfections or sampler offsets) can be characterized by the samples of the desired impulse response $h(t)$. Let N be the number of samples. Then, if $\{f_n\}$, $n = 0, 1, 2, \dots, N-1$ are these N sample values, the PRS system polynomial in z -domain is given by [31]

$$F(z) = \sum_{n=0}^{N-1} f_n z^{-n} \quad (3.1)$$

where $z = \exp(j2\pi f/f_s)$, f_s is the sampling frequency. For a given input symbol sequence $\{x_n\}$, the output sequence $\{y_n\}$ is given by [31]

$$Y(z) = X(z)F(z) \quad (3.2)$$

$$\text{where } X(z) = \sum_{n=0}^{\infty} x_n z^{-n}, \text{ and } Y(z) = \sum_{n=0}^{\infty} y_n z^{-n}.$$

Though most of the desirable properties of a PRS system can be stated in terms of the impulse response $h(t)$, many are best described in frequency domain. Figure 3.1 shows a conventional method of generating the PRS system transfer function $H(\omega)$ which gives an insight into frequency domain properties. The system consists of a tapped delay line with coefficients $\{f_n\}$ in cascade with a band-limiting filter with frequency response $G(\omega)$. The transversal filter has the periodic frequency response (period $2\pi/T$)

$$F(\omega) = F(z)|_{z=\exp(j\omega T)} = \sum_{n=0}^{N-1} f_n \exp(-j\omega nT) \quad (3.3)$$

where T is the symbol period. It can be shown that $h(t)$ has the sample values $\{f_n\}$ if and only if $G(\omega)$ satisfies Nyquist's first criterion, that is [31]

$$\sum_{k=-\infty}^{\infty} G\left(\omega - \frac{2\pi k}{T}\right) = T \quad (3.4)$$

As illustrated in Figure 3.1, the PRS system transfer function $H(\omega)$ is separated into two parts: $F(\omega)$ forces the desired sample values but is periodic, while $G(\omega)$ preserves the sample values but may be used to bandlimit the resulting system function.

Figure 3.1 General Partial-Response System Model [31]

3.2 Choosing the PRS System Polynomial $F(z)$ [31]

In order to maximize the data rate in a bandlimited channel transmission, many PRS systems are designed to occupy the minimum bandwidth which supports transmission without undesired inter-symbol interference (ISI), i.e., $H(\omega) = 0$ for $|\omega| > \pi/T$.

Therefore, for minimum bandwidth systems,

$$G(\omega) = \begin{cases} 1 \text{ (normalized), } |\omega| \leq \pi/T \\ 0, & \text{elsewhere} \end{cases} \quad (3.5)$$

The corresponding system impulse response is given by [31]

$$h(t) = \sum_{n=0}^{N-1} f_n \frac{\sin \frac{\pi}{T}(t-nT)}{\frac{\pi}{T}(t-nT)} \quad (3.6)$$

Other choices for $G(\omega)$ (occupying a larger bandwidth) are possible and allow the use of system polynomials (such as $1 - z^{-1}$) which are unsuitable for minimum bandwidth systems.

For minimum bandwidth systems, $F(\omega)$ must have a zero at π/T . For a null at $\omega = \pi/T$, $1 + z^{-1}$ must be a factor of $F(z)$. Sometimes, reduced low-frequency components in the spectrum are desirable in systems such as hard disk drive read channels [32], transformer coupled circuits, and dc powered cables. For a null at $\omega = 0$, $1 - z^{-1}$ must be a factor of $F(z)$.

With combinations of just the two factors $1 + z^{-1}$ and $1 - z^{-1}$, most of the common partial response systems can be developed. Table 3-1 shows a number of PRS system polynomials and the corresponding $H(\omega)$ and $h(t)$ [31]. Expressions for $H(\omega)$ and $h(t)$ are given in Table 3-2. The second system $1 - z^{-1}$ is not practical in the minimum bandwidth because of the resulting discontinuity in the system function $H(\omega)$. Modified duobinary has both a dc null and a null at $\omega = \pi/T$.

The number of output levels for a practical PRS system is limited both by the complexity of implementation and the inevitable distortions presented in real systems. In addition, there is a tendency for the SNR to degrade with a large number of output voltage levels. If the number of output levels is restricted to be less than 5 for binary inputs, and in addition it is required that $1 + z^{-1}$ and/or $1 - z^{-1}$ be a factor of $F(z)$ and that there be no nulls or severe ripples in the middle of the passband, then all the suitable PRS system

polynomials are listed in Tables 3-1 and 3-2 [31]. For binary input, $m = 2$, and these systems have either 3 or 5 output voltage levels.

The paper [31] presents a detailed comparison of these PRS systems in terms of propagation errors, speed tolerance, minimum zero crossing jitter, and SNR degradation. The two systems which stand out on the basis of performance, simplicity and useful spectral shapes are the duobinary $1 + z^{-1}$ and modified duobinary $1 - z^{-2}$. However, after a close look at Table 3-2, it is found that the frequency response and impulse response expressions for duobinary and modified duobinary are not accurate, according to Equations (3.3), (3.5) and (3.6). Therefore, the following sections will discuss duobinary and modified duobinary signaling in details, and their frequency response and impulse response will be verified.

Table 3-1 Partial Response Systems Formed From $1+z^{-1}$ and $1-z^{-1}$ [31]

$F(z)$	$H(\omega)$	$h(t)$
$1+z^{-1}$ (duobinary-class 1)
$1-z^{-1}$ (dicode)
$1-z^{-2}$ (modified duobinary-class 4)
$(1+z^{-1})^2$ class 2
$(1+z^{-1})^2(1-z^{-1})$
$(1+z^{-1})(1-z^{-1})^2$
$(1+z^{-1})^2(1-z^{-1})^2$ class 5
$(1+z^{-1})(2-z^{-1})$ class 3
$(1+z^{-1})(1-z^{-1})$ $(2+z^{-2})$

Table 3-2 Characteristics of Minimum Bandwidth Partial Response Systems[31]

System Polynomial $F(z)$	Frequency Response $H(\omega)$ for $ \omega \leq \pi/T$	Impulse Response $h(t)$	No. of Output Levels
$1 + z^{-1}$	$2T \cos \frac{\omega}{2} T$	$\frac{4T^2}{\pi} \frac{\cos(\pi t/T)}{t^2 - 4t^2}$	$2m - 1$
$1 - z^{-1}$	$j2T \sin \frac{\omega}{2} T$	$\frac{8Tt}{\pi} \frac{\cos(\pi t/T)}{4t^2 - T^2}$	$2m - 1$
$1 - z^{-2}$	$j2T \sin \omega T$	$\frac{2T^2}{\pi} \frac{\sin(\pi t/T)}{t^2 - T^2}$	$2m - 1$
$(1 + z^{-1})^2$	$4T \cos^2 \frac{\omega}{2} T$	$\frac{2T^3}{\pi t} \frac{\sin(\pi t/T)}{T^2 - t^2}$	$4m - 3$
$(1 + z^{-1})^2 (1 - z^{-1})$	$j4T \cos \frac{\omega}{2} T \sin \omega T$	$\frac{64T^3 t}{\pi} \frac{\cos(\pi t/T)}{(4t^2 - 9T^2)(4t^2 - T^2)}$	$4m - 3$
$(1 + z^{-1})(1 - z^{-1})^2$	$-4T \sin \frac{\omega}{2} T \sin \omega T$	$\frac{16T^2}{\pi} \frac{\cos(\pi t/T)(4t^2 - 3T^2)}{(4t^2 - 9T^2)(4t^2 - T^2)}$	$4m - 3$
$(1 + z^{-1})^2 (1 - z^{-1})^2$	$-4T \sin^2 \omega T$	$\frac{8T^3}{\pi t} \frac{\sin(\pi t/T)}{t^2 - 4T^2}$	$4m - 3$
$(1 + z^{-1})(2 - z^{-1})$	$T + T \cos \omega T + j3T \sin \omega T$	$\frac{T^2}{\pi t} \sin(\pi t/T) \left(\frac{3t - T}{t^2 - T^2} \right)$	$4m - 3$
$(1 + z^{-1})(1 - z^{-1})(2 + z^{-2})$	$-T + T \cos 2\omega T + j3T \sin 2\omega T$	$\frac{2T^2}{\pi t} \sin(\pi t/T) \left(\frac{2T - 3t}{t^2 - 4T^2} \right)$	$4m - 3$

3.3 Duobinary signaling ($1+z^{-1}$)

Duobinary signaling is a type of partial response signaling techniques that has the PRS system polynomial of $F(z) = 1 + z^{-1}$. This particular form of correlative-level coding is also called class I partial response. Duobinary signaling allows the spectral occu-

pancy of the transmitted data to be band-limited to about one half that of a conventional binary signal, but with the same symbol rate as that of the binary signal.

The concept of duobinary signaling was first introduced by Dr. Lender in 1963 [20]. However, the application of duobinary signaling on electrical backplane was first documented in June 2004[21].

Duobinary signaling converts a 2-level binary signal into a correlative 3-level duobinary signal. The duobinary signaling for backplane applications takes advantage of the “natural roll-off” tendency of a backplane channel, and uses it to help shape the data bits and provide a clean signal at the receiver. A duobinary signal occupies only half the bandwidth of a binary signal of the same data rate.

Consider a binary input sequence $\{b_k\}$ applied to a pulse amplitude modulator to produce a two-level sequence $\{a_k\}$:

$$a_k = \begin{cases} +1 & \text{if symbol } b_k \text{ is 1} \\ -1 & \text{if symbol } b_k \text{ is 0} \end{cases}$$

When this sequence is applied to a duobinary coder, it is converted into a three-level output, namely, -2, 0, +2.

Figure 3.2 illustrates the basic duobinary signaling scheme.

Figure 3.2 Duobinary signaling Scheme

In Figure 3.2, the sequence $\{a_k\}$ is first passed through a duobinary encoder involving a single delay element and summer. One may express the duobinary filter output c_k as the sum of the present input pulse a_k and its previous value a_{k-1} , as shown by

$$c_k = a_k + a_{k-1} \quad (3.7)$$

Equation (3.7) changes the input a_k of uncorrelated two-level pulses into a sequence c_k of correlated three-level pulses. Correlation between adjacent pulses may be viewed as introducing ISI into the transmitted signal in an artificial manner.

For T_b seconds delay element having frequency response $e^{-j2\pi f T_b}$, the frequency response of the duobinary encoder in Figure 3.2 is $1 + e^{-j2\pi f T_b}$. Hence, the overall frequency response of the encoder connected in cascade with an ideal Nyquist channel is

$$\begin{aligned}
H_I(f) &= H_{Nyquist}(f)[1 + e^{-j2\pi f T_b}] \\
&= H_{Nyquist}(f)[e^{j\pi f T_b} + e^{-j\pi f T_b}]e^{-j\pi f T_b} \\
&= 2H_{Nyquist}(f)\cos(\pi f T_b)e^{-j\pi f T_b}
\end{aligned} \tag{3.8}$$

For an ideal Nyquist channel of bandwidth $B = 1/(2T_b)$, one has (normalized)

$$H_{Nyquist}(f) = \begin{cases} 1, & |f| \leq 1/(2T_b) \\ 0, & \text{elsewhere} \end{cases} \tag{3.9}$$

The overall frequency response of the duobinary signaling scheme has the form of a half-cycle cosine function, as shown by

$$H_I(f) = \begin{cases} 2\cos(\pi f T_b)e^{-j\pi f T_b}, & |f| \leq 1/(2T_b) \\ 0, & \text{otherwise} \end{cases} \tag{3.10}$$

The normalized magnitude and phase responses are shown in Figures 3.3(a) and 3.3(b).

From the first line in Equation (3.8) and $H_{Nyquist}(f)$ in Equation (3.9), as well as Equation (3.6), the impulse response corresponding to $H_I(f)$ consists of two sinc pulses displaced by T_b seconds with respect to each other.

$$\begin{aligned}
h_I(t) &= \frac{\sin(\pi t/T_b)}{\pi t/T_b} + \frac{\sin[\pi(t-T_b)/T_b]}{\pi(t-T_b)/T_b} \\
&= \frac{\sin(\pi t/T_b)}{\pi t/T_b} - \frac{\sin(\pi t/T_b)}{\pi(t-T_b)/T_b} \\
&= \frac{T_b^2 \sin(\pi t/T_b)}{\pi t(T_b - t)}
\end{aligned} \tag{3.11}$$

Figure 3.3 Normalized Frequency Response of the Duobinary Filter
(a) Magnitude response (b) Phase response

From the above analysis, it can be seen that the $H(\omega)$ of a duobinary system as listed in Table 3-2 didn't include the term $e^{-j\pi f T_b}$. Though its normalized magnitude response is the same as that derived from Equation (3.10), their phase responses are different, which results in a phase shift of their impulse response. Figure 3.4 shows the duobinary system's impulse response derived from both Equation (3.11) and the expression from Table 3-2.

Compared Figure 3.4 with those listed in Table 3-1, it can be seen that the duobinary impulse response derived from Equation (3.11) is coincident with that from Table 3-1, while the impulse response from the expression in Table 3-2 has a phase shift. Therefore, Equations (3.10) and (3.11) provide more accurate descriptions of the duobinary system's frequency response and impulse response.

Figure 3.4 Normalized Impulse Response of the Duobinary Filter

The duobinary impulse response $h_f(t)$ as plotted in Figure 3.4 has only two distinguishable values at the sampling instants. The response to an input pulse is spread over more than one unit interval. Hence, the pulse response in any unit interval is “partial”.

The original two-level sequence $\{a_k\}$ may be detected from the duobinary-coded sequence $\{c_k\}$ by invoking equation (3.7).

Let $\hat{a}_k$ represent the estimate of the original pulse a_k as received by the receiver at time $t = kT_b$.

Subtracting the previous estimate $\hat{a}_{k-1}$ from c_k , one get

$$\hat{a}_k = c_k - \hat{a}_{k-1} \quad (3.12)$$

If c_k is received without error and if the previous estimate $\hat{a}_{k-1}$ corresponds to a correct decision, then the current estimate $\hat{a}_k$ will be correct too.

The technique of using a stored estimate of the previous symbol is called decision feedback. A major drawback of this detection procedure is that once errors are made, they tend to propagate through the output because a decision on the current a_k depends on the correctness of the decision made on the previous a_{k-1} .

3.4 Duobinary signaling with Precoding

A means to avoid the error propagation in duobinary signaling is to use precoding before the duobinary coding, as shown in Figure 3.5. The precoding converts the binary data sequence $\{b_k\}$ into another binary sequence $\{d_k\}$ defined by

$$d_k = b_k \oplus d_{k-1} \quad (3.13)$$

where “ $\oplus$ ” is an exclusive “OR” operator.

The precoded $\{d_k\}$ sequence is applied to a pulse-amplitude modulator, producing a corresponding two-level sequence $\{a_k\}$, where $a_k = \pm 1$. This sequence of short pulses is next applied to the duobinary encoder as described in Figure 3.2, thereby producing the sequence $\{c_k\}$ that is related to $\{a_k\}$ as follows:

$$c_k = a_k + a_{k-1} \quad (3.14)$$

Unlike the linear operation of duobinary coding, the precoding in Equation (3.13) is a non-linear operation.

The combined use of equations (3.13) and (3.14) yields

$$c_k = \begin{cases} 0 & \text{if data symbol } b_k \text{ is 1} \\ \pm 2 & \text{if data symbol } b_k \text{ is 0} \end{cases} \quad (3.15)$$

From equation (3.15), the decision rule for detecting $\{b_k\}$ from $\{c_k\}$ is

$$\begin{aligned} \text{If } |c_k| < 1, \text{ symbol } b_k \text{ is 1} \\ \text{If } |c_k| > 1, \text{ symbol } b_k \text{ is 0} \end{aligned} \quad (3.16)$$

Figure 3.5 A Precoded Duobinary Scheme

A block diagram of the detector is shown in Figure 3.6. A useful feature is that no knowledge of any input sample other than the present one is required. Hence, error propagation is avoided in the detector of Figure 3.6.

Figure 3.6 Detector for Recovering Original Binary Sequence from the Precoded Duobinary Filter Output

3.5 An Example of Duobinary signaling with Precoding

Consider data sequence 0010110 with an extra bit of “1” added to the precoder output for precoding. Using equation (3.13), the sequence $\{d_k\}$ at the precoder output is as shown in row 2 of Table 3-3. The polar representation of the precoded sequence $\{d_k\}$ is shown in row 3 of Table 3-3. Using equation (3.14), the duobinary filter output has the amplitude levels given in row 4 of Table 3-3.

Table 3-3 Illustrating Example on Duobinary Coding

Binary sequence $\{b_k\}$		0	0	1	0	1	1	0
Precoded sequence $\{d_k\}$	1	1	1	0	0	1	0	0
Two-level sequence $\{a_k\}$	+1	+1	+1	-1	-1	+1	-1	-1
Duobinary coder output $\{c_k\}$		2	2	0	-2	0	0	-2
Binary sequence obtained by applying decision rule of Eq. (3.16)		0	0	1	0	1	1	0

By applying the decision rule of equation (3.16), the detected original binary sequence is given in row 5 of Table 3-3. This result shows that, in the absence of noise, the original binary sequence is detected correctly.

3.6 Modified Duobinary signaling $(1 - z^{-2})$ and Precoding

The modified duobinary signaling is another type of partial response signaling techniques that has the PRS system polynomial of $F(z) = 1 - z^{-2}$. This particular form of correlative-level coding is also called class IV partial response. This class IV correlation is achieved by subtracting amplitude-modulated pulses spaced $2T_b$ seconds apart, as illustrated in Figure 3.7. The output of the modified duobinary filter is related to the input two-level sequence $\{a_k\}$ as follows:

$$c_k = a_k - a_{k-2} = (1 - z^{-2})a_k \quad (3.17)$$

With $a_k = \pm 1$, c_k takes one of the three values: +2, 0, -2. A three-level signal is generated.

The overall frequency response of the modified duobinary filter, which is composed of a modified duobinary encoder and the ideal Nyquist channel, as illustrated in Figure 3.7, is given by

$$\begin{aligned} H_{IV}(f) &= H_{Nyquist}(f)[1 - e^{-j4\pi f T_b}] \\ &= 2jH_{Nyquist}(f)\sin(2\pi f T_b)e^{-j2\pi f T_b} \end{aligned} \quad (3.18)$$

where $H_{Nyquist}(f)$ is defined in equation (3.9) and the overall frequency response in the form of a half-cycle sine function is

$$H_{IV}(f) = \begin{cases} 2j \sin(2\pi f T_b) e^{-j2\pi f T_b}, & |f| \leq 1/2T_b \\ 0, & \text{elsewhere} \end{cases} \quad (3.19)$$

The magnitude and phase response of the modified duobinary filter are shown in Figures 3.8(a) and 3.8(b), respectively. A useful feature is that its output has no DC component. This correlative coding exhibits the same continuity at the band edges as in duobinary signaling.

From the first line of Equation (3.18) and $H_{nyquist}(f)$ in Equation (3.9), as well as Equation (3.6), the impulse response of the modified duobinary filter consists of two sinc pulses displaced by $2T_b$ seconds with respect to each other,

$$\begin{aligned} h_{IV}(t) &= \frac{\sin(\pi t/T_b)}{\pi t/T_b} - \frac{\sin[\pi(t-2T_b)/T_b]}{\pi(t-2T_b)/T_b} \\ &= \frac{\sin(\pi t/T_b)}{\pi t/T_b} - \frac{\sin(\pi t/T_b)}{\pi(t-2T_b)/T_b} \\ &= \frac{2T_b^2 \sin(\pi t/T_b)}{\pi t(2T_b - t)} \end{aligned} \quad (3.20)$$

This impulse response is plotted in Figure 3.9. It has three levels at the sampling instants. Again, Equations (3.19) and (3.20) provide more accurate descriptions of the modified duobinary frequency response and impulse response than those expressions as listed in Table 3-2.

Figure 3.7 Modified Duobinary signaling Scheme

Figure 3.8 Normalized Frequency Response of the Modified Duobinary Filter
(a) Magnitude response (b) Phase response

Figure 3.9 Impulse Response of the Modified Duobinary Filter

To eliminate the error propagation in a modified duobinary system, prior to the generation of the modified duobinary signal, a precoder is used as illustrated in Figure 3.7. The precoder converts the binary sequence $\{b_k\}$ into another binary sequence $\{d_k\}$ defined by:

$$d_k = b_k \oplus d_{k-2} = \begin{cases} \text{symbol 1, if either } b_k \text{ or } d_{k-2} \text{ is 1} \\ \text{symbol 0, otherwise} \end{cases} \quad (3.21)$$

where $\{b_k\}$ is the incoming data sequence and $\{d_k\}$ is the precoder output. “ $\oplus$ ” is an exclusive “OR” operator. The precoded sequence $\{d_k\}$ is then applied to a pulse amplitude modulator and then to the modified duobinary filter.

In Figure 3.7, the output c_k equals to -2, 0, or +2, if the amplitude modulator assumes a polar representation for the precoded $\{d_k\}$. The detected b_k at the receiver output may be extracted from c_k by disregarding the polarity of c_k . Therefore, the following decision rule is formulated:

$$\begin{aligned} &\text{if } |c_k| > 1, \text{ symbol } b_k \text{ is 1} \\ &\text{if } |c_k| < 1, \text{ symbol } b_k \text{ is 0} \end{aligned} \quad (3.22)$$

As with the duobinary signaling, the modified duobinary signaling has the following characteristics:

- 1) In the absence of channel noise, the detected $\{b_k\}$ is exactly the same as the original $\{b_k\}$ at the transmitter input.

2) The use of equation (3.21) requires two extra bits to the precoded $\{a_k\}$. The composition of the decoded $\{b_k\}$ using equation (3.22) is invariant to the selection for these two bits.

Since the modified duobinary signal has different spectrum and pulse response shapes with that of the backplane channel, the modified duobinary signal has a potential to cause more ISI with reduced SNR than that of a duobinary signal. Therefore, the modified duobinary coding is not a choice for this research.

3.7 Spectrum Compression of Duobinary Signal

The purpose of duobinary coding is to compress the spectrum of the binary sequence a_k by a factor of 2. One of the effects of this transformation is to change the sequence of uncorrelated digits a_k into a correlated sequence of digits c_k . The consequence of this process is the redistribution of the spectral density of the sequence a_k into a highly concentrated energy density near DC and low frequencies for the sequence c_k . The spectral densities of sequences a_k are [20]:

$$W_1(f) = \frac{1}{4T} |X(f)|^2$$

The spectral densities of sequences c_k are

$$W_2(f) = \frac{1}{8T} |X(f)|^2 (1 + \cos 2\pi fT)$$

where $X(f)$ is the Fourier transform of the pulse. For the case of rectangular NRZ pulses with no shaping,

$$X(f) = T \frac{\sin \pi f T}{\pi f T}$$

$$\text{Therefore, for binary sequence } a_k, \quad W_1(f) = \frac{T}{4} \left(\frac{\sin \pi f T}{\pi f T} \right)^2 \quad (3.23)$$

$$\text{and, for duobinary sequence } c_k, \quad W_2(f) = \frac{T}{4} \left(\frac{\sin 2\pi f T}{2\pi f T} \right)^2 \quad (3.24)$$

Equations (3.23) and (3.24) illustrate exactly the 2:1 spectrum compression property of the duobinary sequence compared with that of the binary sequence. Since in 4-PAM, symbol duration T is double that of NRZ binary, the duobinary spectrum bandwidth is the same as 4-PAM, but half of that in NRZ binary.

3.8 Duobinary System Architecture

Several duobinary system architectures for high-speed data transmission over electrical backplane have been reported recently by researchers [21]-[23], [33]. However, in these literature, the function of each block in a duobinary system was not clearly described. In some cases, it's even misleading. Two questions arise: should the binary to duobinary conversion be completed before or after a backplane channel, and what is the exact role that the backplane channel plays in a duobinary data transmission system? Different signaling schemes and sampling approaches can result in different eye opening of the received data at the far-end of the channel.

The reference paper [33] presents an interesting receiver ADC circuitry that can be used to decode the received 3-level duobinary signal into a binary sequence, but not enough information on how to optimize the filter coefficients. The x2 oversampled equalizer in [23] consists of two 5-tap SSF filters in parallel with shorted output at the transmitter (TX) to improve the total vertical eye-opening by adding the bit-center equalized signal together with the bit-edge equalized signal. However, since this equalizer is used at the TX, this improvement of vertical eye-opening is limited by the TX peak power constraints. Furthermore, the equalization approach used in [23] could introduce more jitter if the bit-edge equalized signal is not perfectly aligned with the bit-center equalized signal. The transceiver architecture introduced in [23] is complicated, as described in section 2.3.4, and is not considered in this work. On the other hand, the conventional duobinary signaling scheme discussed in sections 3.3 and 3.4 is based on the general PRS system model, as described in [31], which completes the data conversion from a 2-level binary signal to a 3-level duobinary signal at TX before the FIR reshaping filter and the backplane channel. This conventional duobinary signaling scheme only adds a moderate amount of hardware to the conventional NRZ signaling scheme, and is discussed below.

According to the discussion in previous sections, a conventional duobinary transmission system is illustrated in Figure 3.10. An NRZ binary data source, a duobinary coder with precoding, an FIR reshaping filter, the backplane channel, a duobinary-to-binary decoder, and an NRZ binary data receiver comprise the entire system.

The duobinary precoder and coder complete the data conversion from a 2-level binary signal to a 3-level duobinary signal. The frequency response of a duobinary signal is a periodic cosine function as show in Equation (3.8). In order to band limit the duobin-

ary signal spectrum, a band-limiting filter is required. The backplane channel has the low-pass characteristic, and can work as a band-limiting filter. However, though the bandwidth of a duobinary sequence is only half of its binary counterpart, a typical low-cost backplane channel has a frequency roll-off that is much steeper than that of a duobinary signal at high frequencies. Therefore, the FIR reshaping filter is added and will have the task of pre-emphasizing the high frequency components of the transmitted signal. The FIR filter together with the backplane channel work as a band-limiting filter $G(\omega)$ as shown in Figure 3.1, or $H_{Nyquist}(f)$ as shown in Figure 3.2. The idea of the conventional duobinary signaling scheme is to compress the data spectrum by modulating a 2-level NRZ signal into a 3-level duobinary signal by duobinary coding; at the meantime, use an FIR filter as pre-emphasis and apply channel equalization techniques used for NRZ signaling to further optimize the channel response in order to approximate the ideal Nyquist channel.

Figure 3.10 A Conventional Duobinary System Architecture

In this conventional duobinary signaling scheme, data are sampled at bit centers. Since the binary to duobinary conversion is completed before the FIR reshaping filter, this conventional duobinary signaling is a 3-level to 3-level signal transmission over the concatenation of an FIR reshaping filter and the backplane channel. At high data rates, the channel's amplitude attenuation and group delay distortion cause severe signal distortions. The FIR filter optimization for a 3-level duobinary signal is more difficult than that of an NRZ signal.

3.9 Summary

This chapter presented a review of the partial response signaling techniques, and discussed the duobinary and modified duobinary signaling schemes in detail. Both the duobinary signaling and the modified duobinary compress data spectrum by half, and are involved in 3-level data transmission. However, due to the different coding and precoding strategies, the duobinary and modified duobinary schemes result in different spectral characteristics and impulse responses. It is found that since the modified duobinary signal has different spectral and pulse response shapes with that of the backplane channel, the modified duobinary signal has a potential to cause more ISI with reduced SNR than that of a duobinary signal. The simulation results in Appendix B demonstrate this. Therefore, the modified duobinary coding is not a choice for this research.

On the other hand, duobinary coding changes the uncorrelated 2-level NRZ signal into a correlated 3-level duobinary signal, and compresses the data spectrum by half. In duobinary signaling, symbol rate is the same as bit rate, and is more compatible to NRZ signal than that of 4-PAM. The 3-level duobinary signal includes only transitions between

adjacent levels. Therefore, duobinary signal has less jitter than that of both NRZ and 4-PAM signals. With TX pre-coding and duobinary coding, the receiver (RX) duobinary to binary decoding depends only on the current received bit. No error propagation occurs. Duobinary signaling also has less SNR loss (relative to NRZ), simplification of implementation, and lower power consumption compared to 4-PAM. Hence, duobinary signaling has obtained more and more interests from researchers for high speed data transmission over a band-limited channel.

However, the 3-level signal transmission in the conventional duobinary signaling scheme adds more difficulties to the FIR filter optimization than that with an NRZ signal. Therefore, new channel equalization techniques and solutions for the FIR filter optimization are worth exploring.

Chapter 4: The Proposed Bit-Edge Equalization (BEE) Scheme

This chapter presents a unique amplitude-optimized bit-edge equalization (BEE) scheme for mitigating ISI in high-speed backplane applications. An analytical comparison of the proposed amplitude-optimized BEE scheme with the phase-optimized pulse width modulation (PWM) [16], the conventional NRZ bit-center equalization (BCE) and duobinary schemes is conducted. Strategies for reducing the impact of channel group delay distortion using the proposed BEE and conventional BCE with optimal sampling phase are explored and compared. The optimality of the proposed BEE in reducing the impact of channel group delay distortion by compressing the data spectrum in conjunction with optimizing the sampling phase is discussed.

4.1 Introduction to the Proposed BEE

Edge equalization can be used to minimize ISI at zero crossing transition edges. Using an adaptive least-mean-square (LMS) algorithm as an RX error convergence engine, the proposed BEE scheme aims to optimize the bit-edge amplitudes by equalizing only the edges of data bits with an adjustment of the sampling points where the error information is collected. Thus, the proposed BEE eliminates the need for complicated algorithms that are required in the phase-optimized BEE [14], [15].

In backplane data transmission systems, the transmission channel is often considered as a LTI system. For a LTI backplane channel, the system's transfer function of apply-

ing the equalization filter at the receiver (RX) is equivalent to that of applying the filter at the transmitter (TX). In this research, the channel's characteristic is known from measurement results. Therefore, the proposed BEE is used as the TX pre-emphasis for the simplicity in real circuit implementation, which means pre-distorting a data sequence at the TX side such that at the RX side the data eyes can be opened. The proposed BEE TX pre-emphasis consists of four basic processes: TX pre-coding, defining the desired bit-edge data from the pre-coded data, decoding the received 3-level signal to a 2-level binary signal, and optimizing equalization with adjustment of the LMS error derivation points.

Figure 4.1 shows a conceptual illustration of the transceiver link model. The proposed BEE transceiver is compared with the PWM [16], and the conventional BCE (NRZ) and duobinary transceivers.

Figure 4.1 A Conceptual Illustration of the Proposed BEE Transceiver with Comparisons to the Conventional BCE, PWM and Duobinary Transceivers

4.1.1 A Comparison of the Proposed BEE with Conventional BCE and Duobinary signaling

As illustrated in Figure 4.1, conventional NRZ channel equalization improves link performance by minimizing ISI at bit centers, and the filter coefficients are adapted based on error information collected at the bit-center sampling instant. This conventional BCE approach makes the assumption that ISI is only important at bit-center sampling points, and the pulse representing a bit always peaks at the bit center. Such assumption is appropriate only for low-speed systems where the jitter is insignificant. But this conventional bit-center sampling approach is not suitable for high data rate transmission due to the channel's severe group delay distortion at high frequencies, as discussed in the previous sections. Moreover, the magnitude attenuation in conventional BCE is ultimately a limiting factor to further increasing data rate. Thus, applying proper signaling techniques to compress the transmitted data spectrum together with channel equalization is essential.

Duobinary signaling is a type of partial response signaling techniques (i.e., correlative coding) that compresses the data spectrum by changing the uncorrelated 2-level signal into a correlated 3-level signal. As discussed previously in chapter 3, the idea of the conventional duobinary signaling scheme is to compress the data spectrum by modulating a 2-level NRZ signal into a 3-level duobinary signal with duobinary encoding. At the meantime, use an FIR filter as pre-emphasis and apply channel equalization techniques as used for NRZ signaling to further optimize the channel response in order to approximate the ideal Nyquist channel. In this conventional duobinary signaling scheme, data are sampled at bit centers. Since the binary to duobinary conversion is completed before the FIR

reshaping filter, this conventional duobinary signaling is a 3-level to 3-level signal transmission over the concatenation of an FIR reshaping filter and the backplane channel. At high data rates, the channel's amplitude attenuation and group delay distortion cause severe signal distortion. The FIR filter optimization for a 3-level duobinary signal is more difficult than that of an NRZ signal.

Unlike the conventional BCE and duobinary signaling schemes where the equalizations are performed for bit-centers, the proposed BEE scheme is based on equalizing only the edges of data bits by adjusting LMS error derivation points. This proposed BEE approach performs equalization by looking at the signal amplitudes that occur at the bit edges of data and seeking to drive the associated error terms to zero. The proposed BEE scheme utilizes a TX pre-coding and decoding scheme that is similar to the differential encoder/decoder for a duobinary partial response channel as discussed in Chapter 3. By "XOR" pre-coding, the original PRBS binary sequence is converted into another binary sequence. The purpose of using "XOR" TX pre-coder is that, at the channel's far end, the 3-level signal to binary decoding could depend only on the current bit and no error propagation occurs. While duobinary signaling completes data spectrum compression by duobinary encoding at TX, the proposed BEE completes data spectrum compression by the TX SSF filter itself and no special coding is required. Both the proposed BEE and duobinary signaling compress data spectrum by half. However, the different sampling approach introduced in the proposed BEE could greatly improve the FIR filter optimization.

Due to the drawbacks of using HSSF in BEE for simultaneous ISI and transition jitter reduction as discussed in the previous sections, in this proposed BEE scheme, only bit-edge equalization is applied by using an SSF filter. Data are sampled at bit edges

instead of bit centers as in the conventional duobinary system. In the conventional duobinary signaling scheme, the differential sequence $\{a_k\}$ is first converted into a duobinary sequence $\{c_k\}$ before being transmitted, where $c_k = (a_k + a_{k-1})/2$ after normalization. The frequency response of a duobinary signal $(1 + z^{-1})$ is a periodic cosine function. In order to band limit the duobinary signal spectrum, a band-limiting filter is needed. The backplane channel has the low-pass characteristic, and can work as a band-limiting filter. However, though the bandwidth of a duobinary sequence is only half of its binary counterpart, the backplane channel has a frequency roll-off that is much steeper than that of a duobinary signal at high frequencies. Hence, the FIR reshaping filter is added to pre-emphasize the high frequency content of the transmitted signal. Therefore, in the conventional duobinary transceiver the FIR filter, together with the backplane channel, work as a band limiting filter $H_{Nyquist}(z)$ as shown in Figure 4.1. In contrast, the proposed BEE TX pre-emphasis scheme transmits $\{a_k\}$ through the FIR filter and channel directly, and seeks to drive the received bit-edge data at the far-end of the channel to be equal to the desired bit-edge data sequence $\{x_k\}$. $\{x_k\}$ is defined by

$$x_k = \begin{cases} \pm 1 & \text{if } a_k = a_{k-1} \\ 0 & \text{if } a_k \neq a_{k-1} \end{cases}. \quad (4.1)$$

With “XOR” TX pre-coding, the channel’s far-end 3-level BEE signal to 2-level binary decoding depends only on the current received bit. No error propagation occurs. The BEE signal decoding is defined by

$$b_k = \begin{cases} 1 & \text{if } x_k = 0 \\ 0 & \text{if } x_k = \pm 1 \end{cases} \quad (4.2)$$

In this proposed BEE TX pre-emphasis scheme, the 2-level to 3-level data converting is completed at the far end of the channel through the concatenation of the FIR filter and the backplane channel. Thus, the proposed BEE eliminates the need for a “delay and add” duobinary encoder that has a Z-transform of $1 + z^{-1}$ as in the conventional duobinary transceiver, and is more compatible with the conventional BCE transceiver. By simply bypassing the “XOR” precoder from the proposed BEE, the proposed BEE can perform as a conventional BCE. Therefore, a BEE/BCE dual-mode TX pre-emphasizer can be implemented.

4.1.2 A Comparison of the Proposed BEE with PWM [16]

While the proposed BEE as well as the conventional BCE and duobinary schemes all use amplitude modulation, the PWM scheme proposed in [16] uses phase modulation that eliminates the need for the complicated algorithms by applying PWM to each bit. In this PWM scheme, only one coefficient needs to be set to fit the channel equalizer transfer function and no amplitude modulation is applied, an advantage in low-voltage high-speed CMOS processes. However, this PWM scheme not only shifts data transition edges, but also changes the data pattern that results in a wider data spectrum but with reduced DC and low frequency content at the channel’s near-end, as will be demonstrated in Chapter 5. This wide PWM data spectrum limits the PWM application in high-loss channels.

4.1.3 Optimizing the FIR Filter

There are two basic processes involved in the adaptive filtering method: a filtering process and an adaptive process. The filtering process consists of computations of the output of a transversal filter produced by a set of tap inputs, and generates an estimation error by comparing this output to a desired response. The adaptive process performs iterative adjustments of the tap coefficients in accordance with the estimation error. Figure 4.2 illustrates the adaptive filtering process in Matlab simulation. Please note that the PLL block in Figure 4.2 is used to illustrate how the RX side data are sampled. It doesn't mean that the FIR filter is implemented at RX with PLL.

Figure 4.2 LMS Adaptive Filtering in BCE, Duobinary, and the Proposed BEE Schemes

In Figure 4.2, $u[k]$ is the “computed” received data at the channel’s far-end. n_d is a data delay relative to the bit center (BC) as illustrated previously in Figure 2.6. $u_d[k]$ is the delayed version of $u[k]$ by n_d . T is the delay operator, where T is equal to one sym-

bol period for an SSF filter. The TX data sampling clock phase (ϕ_o) is restored as $\phi_o + \phi_{TL}$ at RX, as shown in Figure 4.2, where ϕ_{TL} is the linear phase of the transmission channel. For conventional BCE and duobinary transceivers, $n_d = 0$, the RX sampling clock is aligned at bit centers. For the BEE transceiver, $n_d \approx \pm 0.5UI$, the RX sampling clock is aligned at bit edges. By adjusting n_d , optimal bit-center and bit-edge sampling phases can be obtained.

The output of the SSF filter is given by:

$$y[k] = \sum_{n=0}^{N-1} c_n[k] u_d[k-n] \quad (4.3)$$

where k is the k th bit of the data sequence, N is the number of taps, and c_n are the tap coefficients. c_n are updated using an error convergence algorithm. In this work, since the FIR filter was applied as the TX pre-emphasis, like other TX pre-emphasis techniques, noise enhancement could be an issue. Therefore, LMS instead of zero-forcing (ZF) adaptive algorithm was used to optimize the filter coefficients, in order to balance a reduction in ISI with noise enhancement [34] and to increase SNR. For LMS criterion:

$$c_n[k+1] = c_n[k] + \mu u_d[k] e_k \quad (4.4)$$

where μ is the step size, $u_d[k] = u[k - n_d]$, and $e[k]$ is the error between the desired data and the actual filter output $y[k]$. By adjusting n_d , one could get the different sampled data $u_d[k]$. Thus, when applying equation (4.3), the filter output $y[k]$ is updated. There-

fore, by comparing $y[k]$ with the desired bit-center data or bit-edge data, the error information $e[k]$ is updated accordingly. By inputting this updated $e[k]$ into the LMS adaptive equation (4.4), one can get the updated filter coefficients $c_n[k]$, which in turn updates the filter output $y[k]$ when using equation (4.3). Therefore, the error between the desired data and the actual filter output $y[k]$ is updated again. By repeating this process, the mean error square can be minimized and the filter coefficients are driven to their optimal values.

In using the proposed BEE method, n_d is adjusted around $\pm 0.5\text{UI}$ away from the bit center where $n_d = 0$. When using LMS adaptive algorithm for the proposed BEE, the error information is collected by comparing the computed channel's far-end signal amplitude at sampling instant to the desired bit-edge value $\{x_k\}$, as defined by equation (4.1), but not by comparing impulse / pulse response. The pulse response simulation is used only to verify if the sampling phase is optimized.

In determining the optimal sampling phase for BEE, n_d is iteratively adjusted based on the peak of the iteratively computed equalized pulse response. Theoretically, when the equalized pulse response is symmetric, n_d is optimized. However, such an optimization criteria of n_d requires a large number of iterations. Moreover, in real circuit implementation, the resolution of phase interpolation is constrained by the hardware complexity. Therefore, in this work, only 16 iterations per symbol period were used. Once the optimal BEE coefficients are obtained, an SSF filter can be used as TX pre-emphasis for bit-edge equalization.

4.2 Reducing the Impact of Channel Group Delay Distortion with Optimal Sampling Phase

Since the backplane channel's group delay distortion occurs at high frequencies, as shown in Figure 2.3, one way to reduce the impact of group delay distortion is to compress the data spectrum before the data is being transmitted through the backplane channel. Another approach for reducing the impact of group delay distortion is to use channel equalization with an optimal sampling phase. In channel equalization, discrete-time SSF filters for pre-emphasis at the transmitter (TX) side and/or DFE at the receiver (RX) side have been widely used to compensate for the channel frequency-dependent loss [5], [6]. However, conventional SSF filters only look at bit centers as the optimal sampling points to collect error information. This bit-center sampling approach is based on the assumption that the received data eyes are symmetric and peaked at bit centers. But at a high data rate, severe channel group delay distortion causes signal distortion where the received data eyes are no longer peaked at bit centers, and the eye diagrams are no longer symmetric, as illustrated in Figure 2.6(a). On the other hand, in real circuit implementation, a TX FIR filter based on amplitude modulation not only changes pulse amplitudes, but also changes the slopes of the pulse's rising and falling edges. Therefore, even though zero forcing of received data bit centers is effective in correcting ISI at the sampling points, more jitter could be injected on the transition edges if the data eyes are not symmetric, which results in a reduction in the timing margin. This group delay impact can be reduced by optimizing the sampling phase in channel equalization.

4.2.1 Using BCE with Optimal Sampling Phase

For the purpose of demonstration, a typical Tyco 34" FR4 backplane channel [9] was used as the comparison benchmark. A normalized 1Vpp PRBS $2^{11} - 1$ data sequence was transmitted through the backplane channel at a data rate of 12Gbps where the group delay distortion became crucial. The pulse response, as shown in Figure 4.3, illustrates that at a data rate of 12Gbps, the pulse representing a bit encounters severe post-cursor distortion rather than pre-cursor distortion due to the severe channel group delay distortion. Therefore, for the simplicity in real circuit implementation, a 5-post-tap SSF filter was applied as the TX pre-emphasis to compensate for the signal distortion. A Matlab script based on [9] was generated and was used to obtain the optimal filter tap coefficients.

Figure 4.3 Channel Pulse Response at 12Gbps Using BCE TX Pre-Emphasis With and Without Optimizing Sampling Phase

As illustrated in Figure 4.2, for the BCE transceiver, the error between the desired data $a[k]$ and the actual filter output $y[k]$ is $e[k] = a[k] - y[k]$. In conventional BCE,

$n_d = 0$, and the RX sampling clock is aligned at bit centers. However, this bit-center sampling approach is not suitable at high data rates when the received data eyes are severely asymmetric due to the channel's group delay distortion. Using BCE, the received data eye opening can be enlarged by optimizing the sampling phase. Figure 4.3 shows the channel's pulse response at a 12Gbps data rate using BCE with and without optimizing the sampling phase. Without TX pre-emphasis, the channel's pulse response presents significant post-cursor ISI. Figure 4.3 demonstrates that by optimizing the sampling phase with $n_d = 6/16UI$, the post-cursor ISI is reduced. The channel's pulse response with the optimal sampling phase is narrower and more symmetric against the bit center, at unit interval 14 in this case, and has approximately the same bit-center sampling peak values compared to the pulse response without the optimal sampling phase where $n_d = 0$. By optimizing the sampling phase, the peak of the channel's pulse response moves toward the bit-center sampling instance at unit interval 14, and the first pre-cursor and post-cursor ISI at unit intervals 13 and 15 are approximately even. Note that since the LMS adaptive algorithm was used instead of the zero-forcing (ZF) adaptive algorithm as the error convergence engine and only a post-tap FIR filter was used for the TX pre-emphasis, the channel's pulse response indicates that the first pre-cursor and post-cursor ISI are not entirely eliminated in this case.

Figure 4.4 shows the channel's far-end eye diagrams at a 12Gbps data rate using BCE with and without optimizing the sampling phase. Figure 4.5 shows the corresponding convergence of error.

Figure 4.4 Channel Far-End Eye Diagrams at 12Gbps With TX Pre-Emphasis Using BCE (a) $n_d = 0$ (b) $n_d = 6/16UI$

Figure 4.5 Convergence Error Using BCE (a) $n_d = 0$ (b) $n_d = 6/16UI$

From Figure 4.4, it is interesting to see that using the conventional BCE at a 12Gbps data rate, the channel's far-end bit-center (BC) eyes are completely closed while the bit-edge (BE) eyes are opened, as shown in Figure 4.4(a), without optimizing the sampling phase where $n_d = 0$. It should be noted that these clean and opened BE eyes are of no benefits here since BCE intends to equalize the bit center not the bit edge. Therefore, a large residual error occurs in error converging, as shown in Figure 4.5(a), and the channel's far-end signal is highly distorted. This abnormal far-end eye diagram can also be

explained from the channel's pulse response as shown in Figure 4.3. From Figure 4.3, it can be seen that when using conventional BCE without optimizing the sampling phase where $n_d = 0$, the channel's pulse response peaks at the middle between the two bit-center sampling instances, which are unit intervals 14 and 15 in this case. Therefore, at the channel's far end, the pulse representing a bit peaks at the bit edge instead of the bit center, which results in the BE eye being opened while the BC eye is closed. On the other hand, when using BCE with the optimal sampling phase where $n_d = 6/16\text{UI}$, the peak of the channel's pulse response is pushed to the bit-center sampling instance, which is unit interval 14 in this case. Therefore, using BCE with the optimal sampling phase, the channel's far-end BC eye is opened as shown in Figure 4.4(b), the impact of the channel group delay distortion is reduced, and the pulse that represents a bit is more symmetric against the bit center.

4.2.2 Using the Proposed BEE with Optimal Sampling Phase

Other than using BCE, a more effective way to reduce the impact of channel group delay distortion is to use BEE with optimal sampling phase. As illustrated in Figure 4.3, since the channel's pulse response without TX pre-emphasis peaks at the middle of the two bit-center sampling instances (unit intervals 14 and 15), instead of using BCE to push the peak of the pulse to the bit center, an alternative way is to make use of the channel's pulse response characteristics by using BEE. Previous works [7], [8] have demonstrated that by using the proposed BEE, the channel's near-end data spectrum has more DC and low frequency content compared to that using the BCE and duobinary schemes. Therefore, at the channel's far-end, the pulse that represents a bit is least attenuated by the chan-

nel, and a large SNR is expected. The simulation results shown in section 5.4.4 demonstrate the optimality of using the proposed BEE in reducing the impact of channel group delay distortion.

4.3 Implementation Considerations of the Proposed BEE

Though an RX adaptive DFE is able to adapt to different channels, error propagation and pre-cursor ISI could be the issue. A large number of post-taps are required to cancel post-cursor ISI, and the RX DFE circuits are usually complicated in implementation.

On the other hand, TX pre-emphasis has the advantages of simple circuit implementation and independent on RX CDR. Pre-cursor ISI is not an issue and can be removed by simply adding "pre-tap" to the TX FIR filter. However, TX FIR filter is not adaptive to different channel automatically. TX pre-emphasis is used if the channel's characteristics are known.

In this research, the channel characteristics were known from the measurement results (.s4p file). Therefore, the FIR filter was applied at the TX for pre-emphasis as shown in Figure 4.1, and its coefficients were obtained from Matlab simulations. These filter coefficients were pre-calculated according to channel characteristics.

Compared to the conventional BCE TX pre-emphasis scheme as presented in [5] and [35], the proposed BEE TX pre-emphasis scheme only needs to add the precoding circuitry which is composed of an XOR gate and a DFF. Using CML logic in CMOS 90nm technology, the precoding circuitry can be expected to consume only about 1.5mA at a

1.2V low-voltage power supply at 10Gbps [35], which is about 1.8mW. Therefore, when applying the circuitry as in [35], a power consumption of about 60mW could be expected for the entire BEE transmitter, including retiming circuits and pre-drive buffers. As a matter of fact, one of the goals of this research was to develop an effective signaling scheme to optimize the FIR filter while using the existing circuitry.

The circuitry as presented in [35] includes DFFs for retiming, XOR for the coefficient's sign controlling, buffers to provide driving ability for the pre-emphasis driver, a 5-bit DAC current source to control the weight of each tap, and a 6-bit register to store the optimal coefficient value. The filter coefficients can be loaded when the chip is initialized, and the coefficient values can be programmed through JTAG.

The proposed BEE eliminates the need for a “delay and add” duobinary encoder that has a Z-transform of $1 + z^{-1}$ as in the conventional duobinary transceiver, and is more compatible with the conventional BCE transceiver. By simply bypassing the “XOR” precoder from the proposed BEE, the proposed BEE can perform as a conventional BCE by adjusting the filter coefficients. Therefore, a BEE/BCE dual-mode TX pre-emphasizer can be implemented to accommodate different channel characteristics and data rates. In the progress of developing this dissertation, the candidate was asked to provide design parameters for a team member to implement in 90nm CMOS technology. Thus, this proposed BEE/BCE dual-mode TX pre-emphasis signaling scheme has been implemented in 90nm CMOS by that team member and included in his Master thesis [36]. The programmable pre-emphasis circuit as presented in [36] can also be used to compensate for channel characteristic variation.

4.4 Summary

This chapter proposed a unique amplitude-optimized BEE scheme for mitigating ISI in high-speed backplane applications. Using an adaptive LMS algorithm as an RX error convergence engine, the proposed BEE scheme aims to optimize the bit-edge amplitudes by equalizing only the edges of data bits with an adjustment of the sampling points where the error information is collected. Thus, the proposed BEE eliminates the need for complicated algorithms that are required in phase-optimized BEE.

This proposed BEE method employs TX pre-coding in conjunction with TX pre-emphasis using an SSF filter. With TX data pre-coding, the channel's far-end 3-level signal to 2-level binary decoding depends only on the current received bit. No error propagation occurs. The proposed BEE reduces the impact of channel group delay distortion by compressing the data spectrum in conjunction with optimizing the sampling phase. In addition, the proposed BEE compresses data spectrum by the SSF filter itself. No special coding is required. For generalization, the proposed BEE TX pre-emphasis can act as conventional BCE by simply bypassing the "XOR" TX pre-coder. Thus, a BEE/BCE dual-mode TX pre-emphasizer can be implemented to accommodate different channel characteristics and data rates.

The optimality of using the proposed BEE in channel efficiency, SNR enhancement, as well as mitigating ISI and reducing the impact of channel group delay distortion is demonstrated in Chapter 5.

Chapter 5: Simulation Results and Discussion

This chapter covers simulation results and discussions. A typical Tyco 34" (30" trace and 2×2 " connector) FR4 backplane channel was used as the working subject. The channel characteristic was known from the measurement results (.s4p files). The channel characteristic model based on these measurement results had been established and widely used by colleagues [5]-[6], [9], [24]-[25], and had been proven to be effective. Therefore, this channel model was used as a base for this research.

A Matlab script based on [9] was generated and used to evaluate the link performance when using different channel equalization and signaling techniques. NRZ, 4-PAM, duobinary and modified duobinary signaling techniques are compared, and their effects on link performance are demonstrated (simulation results have been moved to Appendices A and B as required by the Examination Board). The effects of channel efficiency, ISI mitigation and power constriction that result from using the proposed BEE scheme are discussed and compared with those using the phase-optimized PWM [16], and the conventional BCE and duobinary schemes. The optimality of the proposed BEE with optimal sampling phase in reducing the impact of channel group delay distortion is exhibited.

5.1 Channel Characteristics and Equalization

This section discusses the basics of channel equalization and its limitations. In this research, since the channel's characteristic was known from measurement results (.s4p file) [9], [24], an SSF filter can be used as the TX pre-emphasis [5], [9]. Figure 5.1(a)

shows the amplitude response of the backplane channel in frequency domain, and Figure 5.1(b) shows its impulse response in time domain, with and without pre-emphasis. The normalized pulse responses of this channel to an ideal trapezoidal pulse with period of 320psec (3.125Gbps), 160psec (6.25Gbps), and 100psec (10Gbps) are shown in Figure 5.2.

The plots in Figure 5.1(a) illustrate that the backplane channel has a low pass characteristic. The pre-emphasis FIR filter boosts the high frequency component of the channel while de-emphasizes the low frequency component, and the concatenation of the pre-emphasis filter and the transmission channel gives a flat frequency response.

Figure 5.1 (a) Channel amplitude response and (b) Channel impulse response [9] [24]

In the time domain, the channel's impulse and pulse responses also demonstrate that due to channel attenuation, the impulse and pulse responses exhibit long settling tails as shown in Figures 5.1(b) and 5.2. These long tails induce ISI that corrupts the current and adjacent transmitted symbols and reduces the effective pulse width and amplitude.

This high-frequency attenuation makes it difficult, in high-speed data transmission along PCB traces, for the receiver to interpret the information from the received data. The attenuation prevents a pulse from reaching its full strength within its symbol period, causing the pulse to spread into adjacent symbols. By TX pre-emphasizing, the tail is minimized and the pulse can be narrowed down, preventing it from spreading into the adjacent symbol.

Figure 5.2 Channel Pulse Response Without TX Pre-emphasis at Different Data Rates

While channel equalization can cancel the frequency dependent part of the channel attenuation and flatten the spectrum of the channel, it reduces the magnitude of the channel transfer function as well, which results in a reduced magnitude of the received data. The attenuation of the magnitude is ultimately a limiting factor to achieve an even higher data rate. As data rate increases, the level of magnitude attenuation increases as well, as shown in Figure 5.2. Therefore, it is difficult to achieve a high data rate (e.g. 10Gbps) by using conventional channel equalization alone. Thus, applying proper signaling tech-

niques to compress data spectrum before the data are being transmitted is essential in addition to channel equalization.

5.2 The Role of Channel on the Data Transmission Link

In order to further understand the role of the backplane channel on the data transmission link, simulations were performed for an NRZ binary signal using the conventional NRZ bit-center equalization (BCE) method as discussed previously in Chapters 1 and 2. Figure 5.3 illustrates the frequency responses of a PRBS $2^7 - 1$ sequence transmitted at a data rate of 5Gbps, using NRZ signaling with BCE.

Figure 5.3(a) shows the transmitted data spectrum at the near end of the channel with a buffer only. Figure 5.3(b) and (c) shows the received data spectrum at the far end of the channel without and with TX pre-emphasis, respectively. The data spectrum at the near end of the channel exhibits periodic ripples as shown in Figure 5.3(a). Because of its low-pass characteristic, the backplane channel band limits the transmitted data spectrum as shown in Figure 5.3(b). By pre-emphasizing, the DC and low frequency components of the channel are reduced while the high frequency components are emphasized, which result in an increased bandwidth of the received data spectrum as shown in Figure 5.3(c) but with reduced magnitude compared to the data spectrum as shown in Figure 5.3(b). This pre-emphasis effect confirms to the previous discussion in section 5.1.

Figure 5.3 Frequency Response of the Transmitted Data at 5Gbps Using NRZ Binary signaling with Conventional BCE

5.3 Using SSF and FSSF in Channel Equalization

NRZ bit-center equalization using a symbol spaced FIR (SSF) filter has been commonly applied as the TX pre-emphasis. To overcome the aliasing issue resulting from using an SSF filter, a fractional symbol spaced FIR (FSSF) filter can sometimes be used.

A commonly used FSSF filter is the half-symbol spaced FIR (HSSF) filter [9], [10] that samples at both the bit centers and the bit edges, and forces the transition voltage level to be half of the signal amplitude. Theoretically, an HSSF filter samples at a half of the symbol period T and thus extends the compensation beyond $1/T$. However, the channel's nonlinear phase distortion at high data rates results in severe post-cursor signal distortions where the peak of the pulse representing a bit is no longer at the center of a bit time period and the eye diagrams are no longer symmetric. Therefore, besides the implementation difficulties of an HSSF filter as discussed in Chapter 2, this severe post-cursor signal distortion adds difficulties to the HSSF filter optimization. An HSSF filter can't guarantee convergence and leads to large filter coefficient variations.

To demonstrate, this section exhibits the simulation results of an NRZ signal transmitted through the backplane channel using a bit-center equalized SSF filter and an HSSF filter, respectively, as the TX pre-emphasis. For the HSSF filter, a single half-symbol-spaced delay chain [10] was used for both the bit-center and the bit-edge equalizations.

For the purpose of comparison, a PRBS $2^{11} - 1$ data sequence was transmitted through the backplane channel at a rate of 5Gbps, using a 3-post-tap HSSF filter and a 7-post-tap HSSF filter, respectively, as the TX pre-emphasis. The channel's near end signal was normalized to $1V_{pp}$. The results are compared with those obtained using a 3-post-tap SSF filter. Figure 5.4 shows the eye diagrams of the received data at the far end of the channel.

Figure 5.4 Eye Diagrams at the Channel's Far End With TX De-Emphasis at 5Gbps
(a) Using 3-post-tap SSF (b) Using 3-post-tap HSSF (c) Using 7-post-tap HSSF

From Figure 5.4(a) and (b), it can be seen that the eye opening using a 3-post-tap HSSF filter is worse than that using a 3-post-tap SSF filter. However, the HSSF filter reduces jitter at the transition edges compared with that using an SSF filter, if the same ISI time span is covered. An HSSF filter needs double of the tap numbers compared to an SSF filter to cover the same ISI time span. Figure 5.4(c) shows that the 7-post-tap HSSF filter results in larger horizontal eye opening than that using the 3-post-tap SSF filter, as in Figure 5.4(a). However, this larger time margin is at the expense of the vertical eye opening.

In addition, a system is said to be stable if the output signal is bounded for the bounded input signals. Therefore, in this research, extensive simulations of convergence errors and coefficient value variations were conducted to verify if the system was stable while evaluating the link performance. Figures 5.5 and 5.6 demonstrate that using an HSSF filter can't guarantee convergence, which leads to larger coefficient variations and residual errors in error converging. Therefore, a more effective channel equalization scheme is required.

Figure 5.5 A Comparison of Filter Coefficient Variation at 5Gbps
(a) Using 3-post-tap SSF (b) Using 3-post-tap HSSF (c) Using 7-post-tap HSSF

Figure 5.6 A Comparison of Convergence Error
(a) Using 3-post-tap SSF (b) Using 3-post-tap HSSF (c) Using 7-post-tap HSSF

5.4 Using the Proposed BEE

This section exhibits the simulation results using the proposed bit-edge equalization (BEE) scheme. The effects of channel efficiency, ISI mitigation and power constriction that result from using the proposed BEE scheme are discussed and compared with those using the phase-optimized PWM [16], and the conventional BCE (NRZ) and duobinary schemes as discussed in previous chapters. The optimality of the proposed BEE with optimal sampling phase in reducing the impact of channel group delay distortion is demonstrated.

5.4.1 The Effect of Sampling Phase on Optimal Eye Opening

For the purpose of demonstration, a normalized $1V_{pp}$ PRBS $2^{11} - 1$ data sequence was transmitted at a rate of 10Gbps through the backplane channel. From the channel's impulse response as shown in Figure 5.1(b), it can be seen that pre-cursor ISI can be neglected. Thus, a 5-post-tap SSF filter was used as the transmitter pre-emphasis to counteract post-cursor ISI. Figure 5.7 shows the eye diagrams of the received data at the channel's far-end using the proposed BEE method with adjustments of delay n_d .

Figure 5.7 Channel's Far-End Data Eye Diagrams at 10Gbps Using the Proposed BEE as TX Pre-Emphasis with n_d adjustment

- (a) $n_d = 8/16UI$ (b) $n_d = 7/16UI$ (c) $n_d = 6/16UI$ (d) $n_d = 5/16UI$
 (e) $n_d = 9/16UI$ (f) $n_d = 10/16UI$ (g) $n_d = 11/16UI$

In Figure 5.7(a), $n_d = 0.5UI$. The SSF filter samples at ideal bit edges. In Figures 5.7(b)-(d), the data sequence is evenly left shifted by $1/16UI$ for each step, and in Figures 5.7(e)-(g), the data sequence is evenly right shifted by $1/16UI$ for each step. Shifting a data sequence in time is equivalent to shifting the sampling phase. Figure 5.8 shows the convergence error, accordingly.

Figure 5.8 Convergence Error at 10Gbps Using the Proposed BEE as TX Pre-Emphasis with n_d adjustment (a) $n_d = 8/16UI$ (b) $n_d = 7/16UI$ (c) $n_d = 6/16UI$ (d) $n_d = 5/16UI$ (e) $n_d = 9/16UI$ (f) $n_d = 10/16UI$ (g) $n_d = 11/16UI$

It is interesting to note that when time shifting a data sequence out of the bit-edge time margin, the bit-edge eyes are closed while the bit-center eyes are opened as shown in Figures 5.7(c) and (d), which results in big residual errors in error converging as shown in

Figures 5.8 (c) and (d), and 2-level signals instead of 3-level signals are received at the far end of the channel.

Figure 5.9 shows the channel's far-end eye opening using the proposed BEE method with n_d adjustment. Both the bit-center (BC) and bit-edge (BE) eye height and eye width are plotted as functions of n_d , respectively.

Figure 5.9 Channel's Far-End Data Eye Opening at 10Gbps Using the Proposed BEE as TX Pre-Emphasis with n_d adjustment

When n_d is shifted from $7/16UI$ to $6/16UI$, the sampling point moves out of the bit-edge time margin, towards to the bit center where $n_d = 0$, as illustrated in Figure 2.6. The bit-center data should be 2-level $(-0.5, 0.5)$ instead of 3-level $(-0.5, 0, 0.5)$ as at the bit edges. Therefore, adapting the bit-center data to a 3-level data sequence will cause large residual errors in error converging and large signal distortion, and the bit-edge eyes are closed. Using the proposed BEE method, the receiver side sampling (decision) is intended to be done at the bit edges. The optimal eye is evaluated as the percentage of enlargement in bit-edge eye height and / or eye width. Both Figures 5.7 and 5.9 illustrate that when

$n_d = 7/16UI$, the channel's far-end bit-edge eye opening is optimized. Further increasing n_d could enlarge the bit-edge eye width with a significant reduction in percentage of the bit-edge eye height. The convergence error plot in Figure 5.8 helps in identifying the optimal eyes. Figure 5.8(b) has the smallest residual error in error converging in this case, which corresponds to Figure 5.7(b) that has the optimal bit-edge eyes. This shifting of n_d verifies that at a high data rate, the optimal bit-center sampling phase is shifted from the centers of the bit time periods, and the optimal bit-edge sampling phase is no longer at $\pm 0.5UI$ away from the centers of the bit time periods.

5.4.2 A Comparison of the Proposed BEE Scheme with the Conventional BCE and Duobinary Schemes in TX Pre-Emphasis

In this section, simulations were performed using the proposed BEE scheme with optimal $n_d = 7/16UI$, the symbol-spaced BCE scheme, and the conventional duobinary signaling scheme, respectively. These equalization schemes being compared are all based on pulse amplitude modulation. For the purpose of demonstration, the same normalized $1V_{pp}$ PRBS $2^{11} - 1$ data sequence was transmitted at a rate of 10Gbps through the back-plane channel. A 5-post-tap SSF filter was used as the transmitter (TX) pre-emphasis for each case. The optimality of using the proposed BEE is demonstrated.

1) A Comparison of Channel's Near-End Data With TX Pre-Emphasis

Figure 5.10 shows a comparison of the channel's near-end data with TX pre-emphasis using the above discussed various approaches. "XOR" precoding was used for

the proposed BEE method, while the “XOR+duobinary” precoding was used for the conventional duobinary method. Figure 5.10(a) shows the pre-emphasized data using the traditional BCE (NRZ) with an SSF as the TX pre-emphasis. Figure 5.10(b) and (c) shows the pre-emphasized data using the proposed BEE and the conventional duobinary signaling methods, respectively. The results shown in Figure 5.10(b) and (c) illustrate that though the proposed BEE and the conventional duobinary signaling methods use the similar precoding and decoding algorithms, the pre-emphasized data patterns are totally different due to the different sampling approaches.

Comparing the results in Figure 5.10, it can be seen that the proposed BEE not only changes the pre-emphasized data pattern by optimizing the filter coefficients, but also combines with a phase shift, which results in enlarged eye opening at the channel’s far end compared to those using the traditional BCE and duobinary methods, as shown in Figure 5.12 and Table 5-1.

Figure 5.10 A Comparison of TX Pre-Emphasis Data at 10Gbps (a) BCE data with $n_d = 0\text{UI}$ (b) BEE data with $n_d = 7/16\text{UI}$ (c) Duobinary data with $n_d = 0\text{UI}$

2) A Comparison of Data Spectra and Eye Opening with TX Pre-Emphasis

Figure 5.11(a) shows the original data spectrum and the precoded data spectrum. “XOR” precoding was used for the proposed BEE method, while the “XOR+duobinary” was used for the conventional duobinary method. Figure 5.11(b) and (c) shows the channel’s near-end and far-end data spectra using the proposed BEE, the conventional BCE and duobinary methods, respectively.

Figure 5.11(a) illustrates that by “XOR” pre-coding, the shape of the data spectrum remains the same as that of the original data spectrum. While duobinary signaling completes data spectrum compression by duobinary encoding as shown in Figure 5.11(a), the proposed BEE completes data spectrum compression at the channel’s near end by the TX SSF filter itself as shown in Figure 5.11(b).

By TX pre-emphasizing, the DC and low frequency contents of the channel’s near-end data spectrum are reduced while the high frequency contents are emphasized as shown in Figure 5.11(b). Due to its low-pass characteristics, the backplane channel band limits the transmitted data spectrum, and results in the narrower and attenuated received data spectrum at the channel’s far-end as shown in Figure 5.11(c). Comparing Figure 5.11(a)-(c), it can be seen that, with TX pre-emphasis, the channel’s near-end data spectrum using the proposed BEE method has the most DC and low frequency content compared to those using either the conventional BCE or the duobinary signaling method. Therefore, at the channel’s far-end, the received data spectrum using the proposed BEE method is least attenuated by the channel, and the largest signal-to-noise ratio (SNR) is expected. Table 5-1 lists the optimal eye width and eye height at the channel’s far end by applying these different methods.

Figure 5.11 Data Spectra with TX Pre-Emphasis at 10Gbps
 (a) Original and precoded data spectra (b) Channel's near-end data spectra
 (c) Channel's far-end data spectra

Figure 5.12 illustrates a comparison of the channel's far-end eye diagrams using the proposed BEE method with optimal n_d , and the conventional BCE and duobinary methods, accordingly.

Figure 5.12 A Comparison of Channel's Far-End Data Eye Diagrams at 10Gbps with TX Pre-Emphasis using (a) Conventional BCE, $n_d = 0$ (b) Proposed BEE, $n_d = 7/16UI$ (c) Conventional duobinary, $n_d = 0$

3) A Comparison of Channel Frequency Response and Filter Tap Values

Figure 5.13 shows the channel's frequency response with TX pre-emphasis using the described methods.

Figure 5.13 A Comparison of Channel Frequency Response at 10Gbps with TX Pre-Emphasis

The plots in Figure 5.13 demonstrate that using the proposed BEE method needs the least high-frequency boost, which can also be represented by the filter tap coefficients as shown in Figure 5.14. Figure 5.14 shows the tap coefficient variation vs. iteration times. The normalized tap values are listed in Table 5-1. Since the proposed BEE needs the least high-frequency boost, it allows the use of the smallest sum of absolute tap values. Therefore, when applied to the TX pre-emphasis FIR filter, the proposed BEE is the least peak-power constrained, which is extremely important in low-voltage CMOS implementation. In addition, since the proposed BEE needs the least high-frequency boost, which implies a minimal amplification of crosstalk, the proposed BEE method is expected to be more immune to crosstalk than the conventional BCE and duobinary methods.

Figure 5.14 A Comparison of Filter Coefficient Variation at 10Gbps With TX Pre-Emphasis Using (a) BEE (b) BCE (c) Duobinary

The simulation results listed in Table 5-1 also demonstrate that using the proposed BEE method, the channel's far-end bit-edge (BE) eye height is enlarged by approximately 57.1% with an 8.4% reduction in eye width compared to the bit-center (BC) eye when using the conventional BCE method. In addition, the bit-edge eye height using the proposed BEE method is enlarged by approximately 76% with an 11.2% reduction in eye

width compared to the eye height and width when using the conventional duobinary signaling method. Hence, the proposed BEE method is more suitable for high-speed data transmission over relatively high-loss channels.

Table 5-1 Summary of Simulation Results at 10Gbps with TX Pre-Emphasis

Method		proposed BEE	conventional BCE	conventional Duobinary
Optimal delay n_d		7/16UI	0	0
Normalized tap values	main tap	1	1	1
	post tap 1	-0.0898	-0.6903	-0.4458
	post tap 2	-0.4807	0.1463	-0.2064
	post tap 3	0.2178	-0.1340	0.1316
	post tap4	-0.1157	0.1356	-0.0177
	post tap 5	0.0266	-0.0937	-0.0445
Main tap value		34.45	59.60	50.18
Sum of absolute tap values		66.51	131.11	92.63
far-end eye	Eye width (UI)	0.621	0.678	0.699
	Eye height (V)	0.132	0.084	0.075

However, an argument arises that in real IC design, the signal peak to peak value is limited by the power supply voltage, and can not be increased arbitrarily. Moreover, the increase in signal peak to peak value at the TX side not only increases the power, but also the near end crosstalk. Therefore, according to different processing technologies, TX de-emphasis is sometimes required instead of pre-emphasis as discussed in Chapter 2. The following section compares the results of using the proposed BEE as the TX de-emphasis with those using the phase-optimized PWM [16].

5.4.3 A Comparison of the Proposed BEE with PWM

In this section, simulations were performed using the proposed BEE scheme with optimal $n_d = 7/16\text{UI}$, the conventional symbol-spaced BCE scheme, and the PWM

scheme [16], respectively. For the purpose of demonstration, the same normalized $1V_{pp}$ PRBS $2^{11} - 1$ data sequence was transmitted at a rate of 10Gbps through the backplane channel. A 5-post-tap SSF filter was used as the TX de-emphasis FIR filter for both the BCE and the proposed BEE schemes. The optimal filter coefficients were normalized such that the maximum channel's near end data V_{pp} were equal to 1V. The optimality of using the proposed BEE is demonstrated.

1) A Comparison of Channel's Near-End Data

Figure 5.15 shows a comparison of the channel's near-end data. As illustrated in Figure 5.15(b), the optimized 56.25% PWM was applied on each bit without amplitude modulation. This PWM technique compensates for phase delay distortion instead of amplitude attenuation. However, PWM not only shifts data transition edges, but also changes the data pattern which results in a wider data spectrum but with significantly reduced DC and low frequency components, as shown in Figures 5.15(b) and 5.16(b). Therefore, PWM reduces the received data eye height significantly compared to those using the proposed BEE, as shown in Figure 5.17 and Table 5-2. On the other hand, Figure 5.15(c) illustrates that the proposed BEE not only changes the de-emphasized data pattern through amplitude modulation, but also applies an edge phase shift, which results in an enlarged eye opening at the channel's far-end as shown in Figure 5.17(c).

Figure 5.15 A Comparison of Channel's Near-End Data at 10Gbps Using
 (a) Conventional BCE with TX de-emphasis, $n_d = 0$ (b) 56.25%UI PWM
 (c) Proposed BEE with TX de-emphasis, $n_d = 7/16\text{UI}$

2) A Comparison of Data spectra and Eye Opening

Figure 5.16 shows the data spectra. Figure 5.16(b) illustrates that with BEE TX de-emphasis, the channel's near-end data spectrum using the proposed BEE is compressed and has the most DC and low frequency content, which enhances channel efficiency compared to those using either the BCE or the PWM method. Therefore, at the channel's far-end, the received data using the proposed BEE is least attenuated by the channel and a significant SNR improvement is expected. Table 5-2 lists the optimal eye width and eye height by applying these different methods.

Figure 5.17 shows the channel's far-end eye diagrams. From the previous discussion in section 5.4.1, the optimal n_d was set to $7/16\text{UI}$ for the proposed BEE. The proposed BEE combines the amplitude modulation in conjunction with the bit-edge phase shift, which results in an enlarged eye opening at the channel's far-end as shown in Figure 5.17(c).

Figure 5.16 Data spectra at 10Gbps

- (a) Original and precoded data spectra
 (b) Channel's near-end data spectra
 (c) Channel's far-end data spectra

Figure 5.17 A Comparison of Channel's Far-End Data Eye Diagrams at 10Gbps Using (a) Conventional BCE with TX de-emphasis, $n_d = 0$ (b) 56.25%UI PWM (c) Proposed BEE with TX de-emphasis, $n_d = 7/16\text{UI}$

Table 5-2 A Comparison of the Proposed BEE with the PWM [16] and Conventional BCE Schemes on Channel's Far-End Eye Opening

Method	Proposed BEE	Conventional BCE	PWM [16]
Optimal delay n_d	7/16UI	0	0
Far-end eye width (UI)	0.6719	0.6782	0.7133
Far-end eye height (V)	0.0678	0.0382	0.0525

The simulation results listed in Table 5-2 demonstrate that at a 10Gbps data rate, by using the proposed BEE, the channel's far-end bit-edge (BE) eye height is enlarged by approximately 77.5% with a 0.93% reduction in eye width compared to the bit-center (BC) eye when using the conventional BCE. In addition, the BE eye height using the proposed BEE is enlarged by approximately 29.1% with a 5.8% reduction in eye width compared to the eye height and width when using the PWM. Hence, the proposed BEE is more suitable for high-loss channels. Though PWM is effective in reducing jitter, its wide near-end data spectrum reduces channel efficiency and limits the eye-height at the channel's

far-end. Therefore, the PWM is not a choice for this high loss bandlimited backplane channel.

5.4.4 Using the Proposed BEE in Reducing the Impact of Channel's Group Delay Distortion

In this section, the optimality of the proposed BEE with optimal sampling phase in reducing the impact of channel group delay distortion is demonstrated.

For the purpose of comparison, the same normalized 1Vpp PRBS $2^{11} - 1$ data sequence was transmitted at a data rate of 12Gbps through the backplane channel where the channel's group delay distortion was crucial. A 5-post-tap SSF filter was used as the transmitter pre-emphasis. Simulations were performed using the proposed BEE method, the symbol-spaced BCE method, and the duobinary signaling method. The equalization methods being compared are all based on pulse amplitude modulation.

1) Using optimal sampling phase in reducing the impact of group delay distortion on eye opening

As discussed in previous sections, at a high data rate, the channel's group delay distortion causes severe signal distortions where the received data eyes are no longer peaked at bit centers, and the eye diagrams are no longer symmetric, as illustrated in Figure 2.6(a). On the other hand, an FIR filter based on amplitude modulation not only changes pulse amplitudes, but also changes the slopes of the pulse's rising and falling edges. Therefore, the bit-center sampling approach used in the conventional BCE could

cause the entire failure in opening the received data eyes at high data rates where the channel's group delay distortion is crucial, as shown in Figure 4.4(a). This group delay impact can be reduced by optimizing the sampling phase in channel equalization.

Figure 5.18 plots the channel's far-end eye height and eye width as functions of n_d at a 12Gbps data rate using the proposed BEE, the BCE and duobinary schemes as TX pre-emphasis, respectively. For the BEE scheme, only the bit-edge (BE) eye height and eye width are plotted (since that's what we are interested in), while for the BCE and duobinary schemes, only the bit-center (BC) eye height and eye width are plotted.

Figure 5.18 Channel's Far-End Eye Height and Eye Width as Functions of n_d at 12Gbps Using BCE, Duobinary and BEE Schemes as TX Pre-Emphasis

The plots in Figure 5.18 demonstrate that when using the conventional BCE and duobinary schemes at a data rate of 12Gbps with $n_d = 0$, the channel's far-end bit-center (BC) eyes are closed. These BCE and duobinary bit-center eyes can be optimized by shifting the sampling phase with an adjustment of n_d .

The plots in Figure 5.18 indicate that for the BEE scheme, when $n_d = 8/16UI$, the channel's far-end BE eye opening is optimized. Further increasing or decreasing delay n_d could result in a significant reduction in percentages of eye height. Similarly, the BCE eye opening is optimized when $n_d = 6/16UI$, and the duobinary eye opening is optimized when $n_d = 5/16UI$. None of these optimal sampling phases is at the center of the bit time period where $n_d = 0$. This shifting of delay n_d proves that at a high data rate, the optimal bit-center sampling phases are shifted from the centers of the bit time periods. In the following comparison, only the optimal cases are considered for each method.

2) Using BEE in data spectra compression

Figure 5.19 shows the data spectra at a 12Gbps data rate with TX pre-emphasis using the above described methods with optimal sampling phase. Figure 5.19(a) illustrates that with BEE TX pre-emphasis, the channel's near-end data spectrum using the proposed BEE is compressed and has the most DC and low frequency content, which enhances channel efficiency compared to those using either the BCE or the duobinary method. Therefore, at the channel's far-end, the received data spectrum using the proposed BEE is least attenuated by the channel as shown in Figure 5.19(b), and a significant SNR improvement is expected. Same as the discussion of Figure 5.11, the proposed BEE TX pre-emphasis scheme compresses data spectrum by half compared to its NRZ BCE counterpart at the channel's near end by the TX SSF filter itself. No special coding is required in compressing data spectrum in this proposed BEE TX pre-emphasis scheme.

Figure 5.19 Data Spectra With TX Pre-Emphasis at 12Gbps
 (a) Channel's near-end data spectra (b) Channel's far-end data spectra

3) A comparison of the channel's pulse response and eye opening

Figure 5.20 shows the channel's pulse responses when using the proposed BEE, the BCE and duobinary schemes as TX pre-emphasis at a 12Gbps data rate with optimal sampling phases. From Figure 5.20, it can be seen that unlike the BCE pulse response which approximates the [...0 1 0...] characteristics, both the proposed BEE and the duobinary schemes present similar pulse responses which approximate the [...0 1 1 0...] characteristics at the sampling instances. However, as demonstrated in Figure 5.19, with BEE TX pre-emphasis, the channel's near-end data spectrum using the proposed BEE method has more DC and low frequency content compared to the near-end data spectrum when using the duobinary signaling method. Therefore, at the channel's far end, the pulse that

represents a bit is less attenuated by the channel when using the proposed BEE method. By optimizing the sampling phase, the channel's pulse response using the proposed BEE is more symmetric compared to the pulse response when using the duobinary scheme. Therefore, less jitter is expected when using the proposed BEE instead of the duobinary scheme.

Figure 5.20 Channel Pulse Response at 12Gbps with TX Pre-Emphasis Using BCE, Duobinary, and the Proposed BEE with Optimal Sampling Phase

Figure 5.21 illustrates a comparison of the channel's far-end eye diagrams using the proposed BEE method, the BCE and duobinary methods, respectively, as TX pre-emphasis with optimal n_d . It can be seen that the proposed BEE still results in the largest channel's far-end eye opening at a "faster" data rate as high as 12Gbps. Table 5-3 lists the optimal eye width and eye height at the channel's far end by applying these different methods.

The simulation results as listed in Table 5-3 demonstrate that at a 12Gbps data rate, using the proposed BEE, the channel's far-end bit-edge (BE) eye is enlarged by approximately 88.9% in eye height and 20.8% in eye width compared to the bit-center (BC) eye when using the conventional BCE method with an optimal sampling phase. In addition, the BE eye using the proposed BEE method is enlarged by approximately 143% in eye height and 16.6% in eye width compared to the eye height and width when using the conventional duobinary signaling method with an optimal sampling phase. Hence, the proposed BEE is the most effective in reducing the impact of group delay distortion and mitigating ISI for high-speed data transmission over backplane channels compared with the conventional BCE and duobinary signaling schemes.

Figure 5.21 Channel's Far-End Eye Diagrams at 12Gbps With TX Pre-Emphasis Using (a) BCE, $n_d = 6/16\text{UI}$ (b) BEE, $n_d = 8/16\text{UI}$ (c) duobinary, $n_d = 5/16\text{UI}$

Table 5-3 A Comparison of Channel's Far-End Eye Opening at 12Gbps Using TX Pre-Emphasis with Optimal Sampling Phase

Method	Proposed BEE	BCE	Duobinary
Optimal delay n_d	8/16UI	6/16UI	5/16UI
Far-end eye width (UI)	0.603	0.499	0.517
Far-end eye height (mV)	80.78	42.76	33.24

5.4.5 The Criterion of Using the Proposed BEE

The allowed data transmission rate over a given backplane channel not only depends on the signaling scheme, but also depends on the channel's characteristic itself. The simulation results and discussions presented in the previous sections have demonstrated that the proposed BEE scheme is the most effective in channel efficiency enhancement, ISI mitigation, and reducing the impact of channel group delay distortion at high data rates (e.g. 10Gbps and 12Gbps), compared to the PWM, BCE and duobinary schemes. However, the proposed BEE scheme is not always the best.

To demonstrate the performance of the proposed BEE at a “lower” data rate, the same normalized 1Vpp PRBS $2^{11} - 1$ data sequence was transmitted at a data rate of 5Gbps through the backplane channel. A 5-post-tap SSF filter was used as the transmitter pre-emphasis. Simulations were performed using the proposed BEE method, the symbol-spaced BCE method, and the duobinary signaling method. Figure 5.22(a)-(c) plots the channel's far-end data eye diagrams at a 5Gbps data rate using the BCE, the proposed BEE, and the duobinary signaling schemes, respectively.

Figure 5.22 Channel's Far-End data Eye Diagrams at 5Gbps Using (a) BCE, $n_d = 0$ (b) BEE, $n_d = 6/16UI$ (c) duobinary, $n_d = 0$

It can be seen that at a 5Gbps data rate, the conventional BCE results in the largest channel's far-end eye height, compared to the proposed BEE and the conventional duobinary schemes. This is not surprising since both the proposed BEE and the conventional duobinary schemes are involved in a 3-level signaling. Like the conventional duobinary scheme, the proposed BEE is based on compressing the transmitted data spectrum by half in order to increase the data transmission rate over a band limited channel. However, with the proposed BEE, the SNR performance is sacrificed for a narrower bandwidth requirement, just like the conventional duobinary and other multi-level signaling schemes do. But since the channel's near-end data spectrum using the proposed BEE method has the most DC and low frequency content compared to those using either the conventional BCE or the conventional duobinary signaling scheme, at the channel's far-end, the received data spectrum using the proposed BEE method is least attenuated by the channel. Therefore, the criterion of determining whether to use the conventional BCE or the proposed BEE is based on the difference in channel attenuation at the two frequencies. If the amplitude at frequency " f " is less than 2x that of " $2f$ ", the conventional BCE is preferred; otherwise BEE is the right choice.

Table 5-4 lists a comparison of the channel's far-end optimal eye opening at 5Gbps, 10Gbps and 12Gbps data rates with TX pre-emphasis. The comparison results as listed in Table 5-4 indicate that the proposed BEE scheme is expected to have better performance for high speed (e.g. 10Gbps and exceed) data transmission over high loss channels. At lower data rates or low loss channels, the conventional NRZ BCE will still have better performance than the proposed BEE.

Table 5-4 A Comparison of the Channel's Far-End Data Eye Opening Using TX Pre-Emphasis with Optimal Sampling Phase at Different Data

Method		Proposed BEE	BCE	Duobinary
12Gbps	Optimal delay n_d	8/16UI	6/16UI	5/16UI
	Far-end eye width (UI)	0.603	0.499	0.517
	Far-end eye height (mV)	80.78	42.76	33.24
10Gbps	Optimal delay n_d	7/16UI	2/16UI	1/16UI
	Far-end eye width (UI)	0.621	0.694	0.726
	Far-end eye height (mV)	132.00	92.00	76.00
5Gbps	Optimal delay n_d	6/16UI	0	0
	Far-end eye width (UI)	0.454	0.923	0.929
	Far-end eye height (mV)	219.21	300.10	177.50

Therefore, for generalization, the proposed BEE TX pre-emphasis can act as conventional BCE by simply bypassing the “XOR” TX pre-coder with an adjustment of the filter coefficients. Thus, a BEE/BCE dual-mode TX pre-emphasizer can be implemented to accommodate different channel characteristics and data rates. Currently, this proposed BEE/BCE dual-mode TX pre-emphasis signaling scheme has been implemented in 90nm CMOS by a team member and included in his Master thesis [36]. The programmable pre-emphasis circuit as presented in [36] can also be used to compensate for channel characteristic variation.

5.5 Summary of Results and Discussion

This chapter presented simulation results and discussions regarding various signaling and channel equalization techniques. The optimality of the proposed BEE has been demonstrated.

It was shown, as in section 2.2.2, that at a high data rate, a pulse representing a bit not only was delayed and attenuated in amplitude by the backplane channel, but was distorted where the peak of the pulse was no longer at the center of a bit time period due to the channel's severe group delay distortion at high frequencies. The resulting long tail of a pulse could cause severe post-cursor ISI, degrading the received data eye opening. The received data eyes were no longer peaked at bit centers and the eye diagrams were no longer symmetric, which resulted in a shift in the optimal sampling phases. To overcome the impact of channel group delay distortion, techniques such as optimizing sampling phases in channel equalization and compressing data spectrum are required.

The simulation results as shown in section 5.1 illustrated that while channel equalization could cancel the frequency dependent part of the channel attenuation, it reduced the magnitude of the channel transfer function as well, which resulted in a reduced magnitude of the received data. The attenuation of the magnitude is ultimately a limiting factor to achieve an even higher data rate. Therefore, it is difficult to achieve a high data rate (e.g. 10Gbps) by using channel equalization alone. Thus, applying proper signaling techniques for compressing the transmitted data spectrum in conjunction with channel equalization is essential.

Recently, 4-PAM modulation has been used by researchers to compress data spectrum before the data are being transmitted through the channel. By using 4-PAM modulation, the symbol rate was reduced to half of its NRZ binary counterpart, as shown in Appendix A. Each symbol in a 4-PAM modulated signal transmitted two bits of binary data. Thus, the data spectrum bandwidth by using 4-PAM was compressed to approximately half of its NRZ counterpart as well, which resulted in a less magnitude attenuation at high bit rates (e.g. 6.25Gbps and 8Gbps) compared to NRZ. However, using 4-PAM in compressing the data spectrum often has an SNR penalty due to the four-level encoding, and the 4-PAM transceiver circuits are typically complex leading to the difficulty in providing dense integration and significantly increased power consumption compared to those of the standard NRZ binary transceivers. Moreover, the all level transitions in 4-PAM result in large jitter, which limits the 4-PAM application on this backplane channel.

The duobinary signaling technique can be used to accomplish the two tasks of data spectrum compression and simplification of implementation that is suitable for large scale integration. Additionally, duobinary signaling does not incur nearly as much SNR penalty (relative to NRZ) as 4-PAM, since the 3-level duobinary coding only includes transitions between adjacent levels. However, different duobinary signaling schemes and sampling approaches could result in different eye opening of the received data at the far end of the channel. Appendix B includes the simulation results and discussions of using the duobinary and modified duobinary signaling schemes.

In the conventional duobinary signaling scheme, data are sampled at bit centers. Since the binary to duobinary conversion is completed before the FIR filter, this conventional duobinary signaling is a 3-level to 3-level signal transmission over the concatena-

tion of an FIR filter and the backplane channel. At high data rates, the channel's amplitude attenuation and group delay distortion cause severe signal distortions. The FIR filter optimization for a 3-level duobinary signal is more difficult than that of an NRZ signal.

Recently, edge equalization has been used by some researchers in both duobinary [23] and NRZ [10]-[15] data transmission systems to reduce ISI at the data transition edges. However, in these previous publications [10]-[15], [23], the researchers did not seem to have considered the channel group delay effect at high frequencies by taking the centers of the bit-time periods as the optimal bit-center sampling points and $\pm 0.5UI$ away from the centers of the bit-time periods as the optimal bit-edge sampling points, and data are sampled (recovered) at bit centers. The HSSF sampling approach used in [10] and [23] for simultaneous bit-center and bit-edge equalization makes the system architecture more complicated than a conventional NRZ system which uses an SSF filter for bit-center equalization.

The simulation results presented in section 5.3 demonstrates that using a 7-post-tap HSSF filter resulted in a larger horizontal eye opening than that using a 3-post-tap SSF filter in NRZ signaling. However, this larger time margin was at the expense of the vertical eye opening. An HSSF filter needs double of the tap numbers compared to an SSF filter to cover the same ISI time span. Moreover, the channel's group delay distortion at high frequencies result in the severe post-cursor signal distortion, which adds difficulties to the HFFS filter optimization. Using an HSSF filter for simultaneous bit-center and bit-edge equalization can't guarantee convergence, which leads to large coefficient variations and residual errors in error converging. Thus, the conventional bit-center equalized SSF or

FSSF/HSSF approaches are not suitable at high data rates where the backplane channel's group delay distortion is crucial.

The phase-optimized PWM [16] can also be used to minimize ISI at transition edges. However, this PWM scheme not only shifted data transition edges, but also changed the data pattern that resulted in a wider data spectrum but with reduced DC and low frequency content, as shown in section 5.4.3. Though the PWM is effective in reducing jitter, its wide near-end data spectrum reduces channel efficiency and limits the eye-height at the channel's far-end. Hence, this wide PWM data spectrum limits the application of PWM for high-loss band-limited channels.

In contrast, the proposed amplitude-optimized BEE scheme mitigates ISI and reduces the impact of channel group delay distortion by compressing the data spectrum in conjunction with optimizing the sampling phase. Using the proposed BEE TX pre-emphasis, data spectrum is compressed at the channel's near end by the SSF filter itself. The proposed BEE aims to optimize the bit-edge amplitudes by equalizing only the edges of data bits with an adjustment of the sampling point where the error information is collected, and data are sampled (recovered) at bit edges. Therefore, in this proposed BEE scheme, only an SSF filter is required for the TX pre-emphasis.

The simulation results presented in section 5.4.2 exhibited that, at a 10Gbps data rate with TX pre-coding and pre-emphasis, the channel's near-end data spectrum using the proposed BEE scheme had the most DC and low frequency content compared to those using either the conventional BCE or the conventional duobinary signaling scheme. Therefore, at the channel's far-end, the received data spectrum using the proposed BEE

was least attenuated by the channel and need the least high-frequency boost, as shown in Figures 5.11 and 5.13, respectively. The filter tap coefficients presented in Figure 5.14 and Table 5-1 also illustrate that since the proposed BEE needs the least high-frequency boost, it allows the use of the smallest sum of absolute tap values. Therefore, when applied as the TX pre-emphasis, the proposed BEE was the least peak-power constrained and had the largest eye opening at the channel's far-end. The proposed BEE is expected to have the largest signal-to-noise ratio if the peak power remains the same. The least peak-power constrained feature of the proposed BEE makes it more suitable for low-voltage CMOS implementation. In addition, since the proposed BEE needs the least high-frequency boost, which implies a minimal amplification of crosstalk, the proposed BEE method is expected to be more immune to crosstalk than the conventional BCE and duobinary methods.

The simulation results in section 5.4.2 also illustrated that, using the proposed BEE as TX pre-emphasis at a 10Gbps data rate, the channel's far-end bit-edge eye height was enlarged by approximately 57.1% with an 8.4% reduction in eye width compared to the bit-center eye when using the conventional BCE method. In addition, the bit-edge eye height using the proposed BEE method was enlarged by approximately 76% with an 11.2% reduction in eye width compared to the eye height and width when using the conventional duobinary signaling method.

When used as the TX de-emphasis, the optimality of the proposed BEE scheme has also been verified and compared with the phase-optimized PWM [16] and the conventional BCE schemes, as presented in section 5.4.3. It was demonstrated that, by using the proposed BEE as the TX de-emphasis at a 10Gbps data rate, the channel's far-end bit-edge

eye height was enlarged by approximately 77.5% with a 0.93% reduction in eye width compared to the bit-center eye when using the conventional BCE. In addition, the bit edge eye height using the proposed BEE was enlarged by approximately 29.1% with a 5.8% reduction in eye width compared to the eye height and width when using the phase-optimized PWM.

The optimality of using the proposed BEE in reducing the impact of channel group delay distortion has also been demonstrated in section 5.4.4. The simulation results in section 5.4.4 demonstrate that at a 12Gbps data rate, using the proposed BEE, the channel's far-end bit-edge eye was enlarged by approximately 88.9% in eye height and 20.8% in eye width compared to the bit-center eye when using the conventional BCE method with an optimal sampling phase. In addition, the bit-edge eye using the proposed BEE method was enlarged by approximately 143% in eye height and 16.6% in eye width compared to the eye height and width when using the conventional duobinary signaling method with an optimal sampling phase. The simulation results in section 5.4.4 also illustrates that unlike the BCE pulse response which approximates the $[...0\ 1\ 0...]$ characteristics at sampling instances, both the proposed BEE and the duobinary schemes present similar pulse responses which approximate the $[...0\ 1\ 1\ 0...]$ characteristics at sampling instances. However, as demonstrated in Figure 5.19, with TX pre-emphasis, the channel's near-end data spectrum using the proposed BEE method has more DC and low frequency content compared to the near-end data spectrum when using the duobinary signaling method. Therefore, at the channel's far end, the pulse that represents a bit is less attenuated by the channel when using the proposed BEE method. By optimizing the sampling phase, the channel's pulse response using the proposed BEE was more symmetric compared to the

pulse response when using the duobinary scheme. Therefore, less jitter is expected when using the proposed BEE instead of the duobinary scheme. Thus, the proposed BEE is the most effective in reducing the impact of group delay distortion and mitigating ISI for high-speed data transmission over backplane channels compared with the conventional BCE and duobinary signaling schemes.

The proposed BEE scheme has been proven to have better performance for high speed (e.g. 10Gbps and exceed) data transmission over high loss channels. For generalization, the proposed BEE TX pre-emphasis can act as conventional BCE by simply bypassing the “XOR” pre-coder. Thus, a BEE/BCE dual-mode TX pre-emphasizer can be implemented to accommodate different channel characteristics and data rates, and variations of channel characteristic can be compensated by using programmable pre-emphasis circuits [36].

Chapter 6: Conclusions and Future Studies

6.1 Conclusions

High-speed backplane serial data transmission suffers from severe ISI due to the backplane channel's frequency dependent amplitude attenuation and group delay distortion. This research proposed a unique amplitude-optimized BEE TX pre-emphasis scheme that mitigates ISI and reduces the impact of channel group delay distortion by compressing data spectrum in conjunction with optimizing the equalization sampling phase.

Using an adaptive LMS algorithm as an RX error convergence engine, the proposed BEE scheme aims to optimize the bit-edge amplitudes by equalizing only the edges of data bits with an adjustment of the sampling points where the error information is collected, which in turn changes the error information and optimizes filter coefficients. In this proposed BEE scheme, only a single TX SSF filter is required for the edge only equalization. Data are sampled (detected) at bit edges. LMS instead of ZF adaptive algorithm is used in deriving filter coefficients. Equalization is performed by comparing the computed channel's far-end signal amplitude at sampling instant to the desired bit-edge value and seeking to drive the associated error terms to zero, but not by comparing the channel's impulse response to a target response. Thus, the proposed BEE scheme overcomes the drawback of using ZF in time domain where ZF only takes very limited number of samples of the time-domain channel response that could fail to give optimal results for very challenging channels. Using LMS, the number of taps is not limited by the channel's pulse

response. In this proposed BEE scheme, the pulse response simulation is used only to verify if the sampling phase is optimized. Theoretically, when the equalized pulse response is symmetric, the sampling phase (n_d) is optimized. LMS allows a minimal residual ISI and balances a reduction in ISI and noise enhancement, which is especially important in the TX FIR filter design. Thus, the proposed amplitude-optimized BEE eliminates the need for complicated algorithms that are usually required in the phase-optimized BEE.

The proposed BEE reduces the impact of channel group delay distortion by compressing the data spectrum in conjunction with optimizing the sampling phase. In this proposed BEE, data spectrum is compressed by the TX SSF filter itself. No special coding is required. With “XOR” TX data pre-coding, the channel's far-end 3-level signal to binary decoding depends only on the current received bit. No error propagation occurs.

The proposed BEE TX pre-emphasis has the advantages of simple circuit implementation and independent on RX CDR. Unlike that of an RX adaptive DFE, pre-cursor ISI is not an issue of the proposed BEE TX pre-emphasis. Both pre-cursor and post-cursor ISI can be removed by simply adding “pre-tap” and “post-tap” to the TX SSF filter, and the number to taps is not limited by the channel's pulse response. However, TX FIR filter is not adaptive to different channels automatically. Therefore, to overcome the drawback of not dynamically adaptive to different channels, the proposed BEE TX pre-emphasis can act as a conventional BCE by simply bypassing the “XOR” TX pre-coder with an adjustment of the filter coefficients. Thus, a BEE/BCE dual-mode TX pre-emphasizer can be implemented to accommodate different channel characteristics and data rates. Filter coefficients are obtained from Matlab simulations and are pre-calculated according to channel

characteristics. These filter coefficients can be loaded when the chip is initialized, and the coefficient values can be programmed through JTAG. Currently, this proposed BEE/BCE dual-mode TX pre-emphasis signaling scheme has been implemented in 90nm CMOS technology by a team member and included in his Master's thesis [36]. The programmable pre-emphasis circuit as presented in [36] can also be used to compensate for channel characteristic variation.

The criterion for using the proposed BEE TX pre-emphasis has been demonstrated over a typical Tyco 34" FR4 backplane channel at different data rates using a 5-post-tap TX SSF filter. The optimality of using the proposed BEE in channel efficiency, SNR enhancement, power constriction, as well as mitigating ISI and reducing the impact of channel group delay distortion at 10+Gbps data rates has been verified and compared with those by using the phase-optimized PWM and the conventional BCE, BEE with HSSF, and duobinary signaling schemes. The proposed BEE scheme has been proven to have better performance for high speed (e.g. 10Gbps and exceed) data transmission over long-reach high loss channels.

6.2 Summary of Contributions

In this dissertation, a unique amplitude-optimized BEE TX pre-emphasis scheme has been proposed for 10+Gbps serial data transmission over long reach backplane channels. The proposed BEE scheme mitigates ISI and reduces the impact of channel group delay distortion by compressing data spectrum in conjunction with optimizing the sampling phase. The main contributions to knowledge are summarized below.

1) In this proposed amplitude-optimized BEE TX pre-emphasis scheme, the compression of data spectrum is achieved by equalizing the signal amplitudes that occur at the bit edges of data to be equal to the desired bit-edge values. Unlike the conventional BCE and duobinary signaling schemes where the equalizations are preformed for bit centers, the proposed BEE TX pre-emphasis scheme aims to optimize the bit-edge amplitudes by equalizing only the edges of data bits with an adjustment of the sampling points where the error information is collected, which in turn changes the error information and affects filter coefficients. Thus, the proposed amplitude-optimized BEE eliminates the need for the complicated algorithms that are usually required in the phase-optimized BEE, and only an SSF filter is required for TX pre-emphasis. While duobinary signaling compress data spectrum with duobinary encoding, the proposed BEE compress data spectrum by half using the TX SSF filter itself. No special coding is required.

2) In this proposed amplitude-optimized BEE TX pre-emphasis scheme, the reduction of the impact of channel group delay distortion is achieved by optimizing the sampling phase in channel equalization. The optimality of the proposed BEE in reducing the impact of channel group delay distortion by compressing the data spectrum in conjunction

with optimizing the sampling phase has been exhibited over a typical Tyco 34" FR4 back-plane channel at a 12Gbps data rate where the channel's group delay distortion is crucial.

3) In this research, LMS instead of ZF adaptive algorithm is used in deriving filter coefficients. Using the proposed BEE TX pre-emphasis, equalization is performed by comparing the computed channel's far-end signal amplitude at sampling instant to the desired bit-edge value and seeking to drive the associated error terms to zero, but not by comparing the channel's impulse response to a target response. Thus, the proposed BEE scheme overcomes the drawback of using ZF in time domain where ZF only takes very limited number of samples of the time-domain channel response that could fail to give optimal results for very challenging channels. Using LMS, the number of taps is not limited by the channel's pulse response. LMS allows a minimal residual ISI and balances a reduction in ISI and noise enhancement

4) The proposed BEE TX pre-emphasis eliminates the need for a "delay and add" duobinary encoder that has a Z-transform of $1 + z^{-1}$ as is required in the conventional duobinary transceiver, and is more compatible with the conventional (NRZ) BCE transceiver. By simply bypassing the "XOR" precoder from the proposed BEE TX pre-emphasis scheme, the proposed BEE can perform as a conventional BCE by adjusting the filter coefficients. Therefore, a BEE/BCE dual-mode TX pre-emphasizer can be implemented to accommodate different channel characteristics and data rates.

In addition, since the proposed BEE only needs an SSF filter for the TX pre-emphasis and no 1/2 bit period operation is required, it avoids the drawbacks of using an HSSF-based BEE scheme. An HSSF filter needs double of the tap numbers compared to

an SSF filter to cover the same ISI time span. Moreover, the channel's group delay distortion at high frequencies result in the severe post-cursor signal distortion, which adds difficulties to the HFFS filter optimization. Using an HSSF filter can't guarantee convergence, which leads to large coefficient variations and residual errors in error converging.

The proposed BEE TX pre-emphasis scheme has the advantages of simple circuit implementation and independent on RX CDR. Unlike that of an RX adaptive DFE, pre-cursor ISI is not an issue of the proposed BEE TX pre-emphasis. Both pre-cursor and post-cursor ISI can be removed by simply adding "pre-tap" and "post-tap" to the TX SSF filter, and the number to taps is not limited by the channel's pulse response.

5) With "XOR" TX data pre-coding, the RX data detection depends only on the current received bit and no error propagation occurs. Using the proposed BEE TX pre-emphasis in conjunction with TX pre-coding, the RX clock and data recovery is intended to be done simultaneously at the bit edges, which eliminates the need of a 2x sampling clock for data and clock recovery as required in a conventional BCE NRZ transceiver.

In addition, the less peak-power constrained feature of the proposed BEE TX pre-emphasis scheme makes it more suitable for low-voltage CMOS implementation.

6.3 Recent Publication

This research has led to the following recent publications.

Journal Paper

[1] L. Zhang and T. Kwasniewski, "Comparison of amplitude-optimised bit-edge equalisation with pulse-width modulation in high-speed wireline application," *Electronics Letters*, vol. 45, no. 3, pp. 189-191, January 2009.

[2] L. Zhang and T. Kwasniewski, "Optimal equalization for reducing the impact of channel group delay distortion on high-speed backplane data transmission," (ELSEVIER) *Int J Electron Commun (AEU)* (2009), doi: 10.1016/j.aeue.2009.04.010.

[3] L. Zhang and T. Kwasniewski, "FIR filter optimization using bit-edge equalization in high-speed backplane data transmission," (ELSEVIER) *Microelectron. J* (2009), pp. 1449-1457.

Conference Paper

[1] L. Zhang and T. Kwasniewski, "Using bit-edge equalization in high-speed backplane data transmission," in *IEEE Third International Conference on Communications and Networking in China (ChinaCom 2008)*, 25-27 August 2008, pp. 642 - 646.

[2] L. Zhang and T. Kwasniewski, "ISI mitigation using bit-edge equalization in high-speed backplane data transmission," in *IEEE International Conference on Communications, Circuits and Systems (ICCCAS 2008)*, 25-27 May 2008, pp. 589 - 593.

6.4 Future Work

The amplitude-optimized BEE scheme proposed in this research provides a feasible methodology for mitigating ISI and reducing the impact of channel's group delay distortion in high-speed backplane data transmission. However, some issues remain to be explored:

1) In this research, the effects of crosstalk and noise were neglected based on the assumption that the crosstalk and noise had little effect on the link performance over this FR4 backplane, compared with that of ISI [9]. However, at high frequencies, the channel's amplitude response attenuates dramatically while the crosstalk amplifies. Therefore, for high data rate transmission, it's necessary to include the crosstalk effect. Unfortunately, the channel characteristic model that is currently used in this research haven't included this effect.

2) Using the proposed BEE as the TX pre-emphasis/de-emphasis in conjunction with TX precoding, the RX clock and data recovery is intended to be done simultaneously at the bit edges, which eliminates the need of a 2x sampling clock for data and clock recovery as required in a conventional BCE transceiver. Therefore, new CDR circuitry worth exploring to include the decoding from a 3-level signal into binary bits.

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Appendix A: NRZ vs. 4-PAM

This section exhibits the simulation results using NRZ and 4-PAM signaling techniques. A typical Tyco 34" (30" trace and 2×2 " connector) FR4 backplane channel was used as the data transmission channel. For the purpose of comparison, the same PRBS $2^7 - 1$ sequence was transmitted at data rates of 3.125Gbps, 6.25Gbps, and 8Gbps, using NRZ and 4-PAM modulations, respectively.

From the channel impulse response as shown in Figure 5.1(b), it can be seen that pre-cursor ISI can be neglected. Thus, only post-taps were used for the TX pre-emphasis FIR filter to counteract post-cursor ISI. It has been demonstrated in [24] that for an NRZ signal transmitted through the backplane channel at a data rate of 8Gbps, the optimum number of post-taps for TX pre-emphasis is four. For an NRZ signal transmitted at a data rate lower than 8Gbps, three post-taps for pre-emphasis would be sufficient.

Therefore, for the purpose of comparison, the pre-tap number was set to zero for both the NRZ and 4-PAM signals. The post-tap number was set to 4 when data rate was 8Gbps, and was set to 3 when data rate was lower than 8Gbps. For the NRZ signal, the peak to peak magnitude was set to 1 (-0.5, +0.5), and for the 4-PAM signal, the peak to peak magnitude was set to 3 (-1.5, -0.5, +0.5, +1.5). A symbol-spaced FIR (SSF) filter was employed as TX pre-emphasis for both cases, in order to counteract ISI due to the channel loss. Figures A.1 and A.2 show the eye diagrams of the received data at the far end of the channel using the NRZ modulation and the 4-PAM modulation at different data rates.

Figure A.1 Comparison of NRZ Eye Diagrams Without and With Pre-Emphasis
 (a) 3.125Gbps, 3 post-taps (b) 6.25Gbps, 3 post-taps (c) 8Gbps, 4 post-taps

Figure A.2 Comparison of 4-PAM Eye Diagrams Without and With Pre-Emphasis
 (a) 3.125Gbps, 3 post-taps (b) 6.25Gbps, 3 post-taps (c) 8Gbps, 4 post-taps

From Figures A.1 and A.2, it can be seen that TX pre-emphasis is essential for both the NRZ and 4-PAM signaling. Otherwise, the eye opening at the far end of the channel is small, even at a low data rate as 3.125Gbps. By 4-PAM modulation, the symbol rate is reduced to half of its NRZ binary counterpart, since each symbol in a 4-PAM modulated signal transmits two bits of binary data. Thus, the data spectrum bandwidth by using 4-PAM modulation is compressed to approximately half of its NRZ counterpart as well, which results in a less magnitude attenuation at high bit rates (e.g. 6.25Gbps and 8Gbps) compared to NRZ as shown in Figures A.1 and A.2. However, 4-PAM induces 4-level transitions with SNR penalty after normalization. This 4-level transition causes huge jitter as shown in Figure A.2. The huge jitter limits the application of 4-PAM. Therefore, 4-PAM is not a choice for this backplane channel.

Appendix B: Duobinary vs. Modified Duobinary

This section discusses duobinary and modified duobinary signaling techniques. A typical Tyco 34" (30" trace and 2×2 " connector) FR4 backplane channel was used as the data transmission channel. The simulated eye diagrams are illustrated and compared with those from NRZ and 4-PAM signaling.

For the purpose of comparison, the same PRBS $2^7 - 1$ sequence as used for NRZ and 4-PAM simulations was transmitted at data rates of 3.125Gbps, 6.25Gbps, and 8Gbps, using duobinary and modified duobinary signaling, respectively. Similarly, the pre-tap number was set to zero for both the duobinary and modified duobinary signals. The post-tap number was set to 4 when data rate was 8Gbps, and was set to 3 when data rate was lower than 8Gbps. The peak to peak magnitude was set to 2 (-1, 0, +1) for both the duobinary and the modified duobinary signals. Again, an SSF filter was employed as TX pre-emphasis, in order to counteract ISI due to the channel loss. Based on the discussions in Chapter 3, Tables B-1 and B-2 summarize the duobinary and modified duobinary coding schemes.

The duobinary and modified duobinary signals have the same symbol rate as that of the NRZ binary counterpart. With duobinary or modified duobinary correlative coding, the transmitted data spectrum is reshaped and compressed to approximately half of the NRZ counterpart as discussed in sections 3.3 and 3.6. Figures B.1 and B.2 show the eye

diagrams of the received data at the far end of the channel using duobinary and modified duobinary signaling at different data rates.

Figures B.1 and B.2 illustrate that TX pre-emphasis is also essential for both the duobinary and modified duobinary signaling. Otherwise, the eye opening at the far end of the channel is small, even at a low data rate as 3.125Gbps. This can be explained by that even though the spectrum bandwidth of a duobinary or modified duobinary signal is only half of its NRZ binary counterpart, the typical backplane channel has a frequency roll-off that is much steeper than that of the duobinary or modified duobinary data spectrum at high frequencies. Therefore, TX pre-emphasis is still essential for channel equalization.

In addition, from Figures B.1 and B.2, it can be seen that the eye opening of the received modified duobinary signal is smaller than that of the duobinary signal. This reduction in the received data eye opening indicates inherently higher ISI in the modified duobinary signaling than that in the duobinary signaling. The reason is that in duobinary signaling, the only transitions permitted in successive bits are between any two adjacent amplitude levels. For example, transitions from the top level to the bottom level or vice versa do not occur between successive bits in duobinary signaling. Such a restriction does not exist in the modified duobinary pulse train, as illustrated in Table B-1 and Figure B.2, resulting in the severe ISI and huge jitter. In addition, the modified duobinary coding induces a data spectrum which has no DC component as shown in Figure 3.8. The reduced DC and low frequency power also reduces the received data eye height. Hence, similar to 4-PAM, the huge jitter and ISI in the modified duobinary signaling limits its application on this FR4 backplane channel.

Table B-1 Duobinary and Modified Duobinary Coding Scheme

Duobinary (PR1):	Modified Duobinary (PR4)
input data sequence: $\{b_k\}$	input data sequence: $\{b_k\}$
precoded data sequence: $d_k = d_{k-1} \oplus b_k$	precoded data sequence: $d_k = d_{k-2} \oplus b_k$
amplitude modulated d_k signal: $a_k = \{1, -1\}$	amplitude modulated d_k signal: $a_k = \{1, -1\}$
duobinary coding: $c_k = a_k + a_{k-1}$	duobinary coding: $c_k = a_k - a_{k-2}$
decoded data: $B_k = \begin{cases} 0 & \text{if } c_k > 1 \\ 1 & \text{if } c_k < 1 \end{cases}$	decoded data: $B_k = \begin{cases} 1 & \text{if } c_k > 1 \\ 0 & \text{if } c_k < 1 \end{cases}$
<u>duobinary coding results:</u>	<u>modified duobinary coding results:</u>
➤ 3 level signal	➤ 3 level signal
➤ transitions from bottom (top) level to top (bottom) level are restricted	➤ transitions from bottom (top) level to top (bottom) level are not restricted
➤ bigger eye opening	➤ smaller eye opening
➤ data spectrum is compressed by half	➤ Data spectrum is compressed by half
➤ spectrum contain DC content.	➤ spectrum has no DC content

Table B-2 Duobinary and Modified Duobinary Coding Schemes (cont.)

Duobinary	Modified Duobinary

Figure B.1 Comparison of Duobinary Eye Diagrams Without and With Pre-Emphasis
 (a) 3.125Gbps, 3 post-taps (b) 6.25Gbps, 3 post-taps (c) 8Gbps, 4 post-taps

Figure B.2 Comparison of Modified Duobinary Eye Diagrams Without and With Pre-Emphasis
 (a) 3.125Gbps, 3 post-taps (b) 6.25Gbps, 3 post-taps (c) 8Gbps, 4 post-taps