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DC-Offset Mitigation of Direct-Conversion Receivers

by

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A Thesis submitted to
the Faculty of Graduate Studies and Research
in partial fulfillment of the requirements for the degree of
Master of Applied Science (Electrical)

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Abstract

In this thesis, various receiver architectures are reviewed and issues specific to direct-conversion receiver (DCR) design identified. The design of a DCR consisting of a low-noise amplifier and mixer is detailed. The DCR is targeted at the IEEE802.11a wireless LAN standard, which specifies operation in the 5 GHz unlicensed national information infrastructure (UNI) band, and is fabricated in IBM's 0.5 μ m 50GHz BiCMOS technology with analog metal option. The receiver has a simulated and measured voltage conversion gain of 31 dB at 5.25 GHz. It has a simulated noise figure of 4.7 dB, IIP3 of -9 dBm, IIP2 of +42 dBm and draws 16.1 mA of current from a 2.75 V supply.

Differential-mode feedback is investigated as a method of reducing DC offset. Criteria for the differential-mode feedback loop (DMFL), including loop-gain, frequency response and output noise are identified. Three circuits to implement the DMFL are designed and simulated.

It is found that the ratio of the corrected to uncorrected differential DC output voltage, with the application of feedback, is equal to the inverse of the open-loop gain of the DMFL. As well, noise generated by the DMFL circuit is suppressed by the frequency-dependent open-loop gain, such that at frequencies outside of the DMFL frequency bandwidth, the DMFL output noise is not suppressed.

The following requirements for the DMFL are identified: 1) to have high loop gain at 0 Hz to reduce DC offset, 2) to have low loop gain at frequencies of desired information so the desired signal is not attenuated, 3) to have low output noise at frequencies of desired information where the noise suppression by the loop is reduced, and 4) to be fully integrated to take advantage of the higher levels of integration achievable with a DCR architecture. This research has resulted in an improved understanding of the application of feedback to mitigate DC offsets in direct-conversion receivers.

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Abbreviations

AC	Alternating Current
BJT	Bipolar Junction Transistor
DC	Direct Current
DCR	Direct Conversion Receiver
DMFL	Differential-Mode Feedback Loop
F	Noise Factor
f_t	Unity Gain Frequency
GHz	Giga-Hertz
G_m	Transistor Transconductance
IC	Integrated Circuit
IF	Intermediate Frequency
IP2	Second-Order Intercept Point
IIP2	Input Referred Second-Order Intercept Point
IR	Image Rejection
kHz	Kilo-Hertz
k	Boltzmann's Constant
NF	Nose Figure
PA	Power Amplifier
Q	Quality Factor
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
Si	Silicon
SNR	Signal to noise ratio
UMTS	Universal Mobile Telephone Service
UNII	Unlicensed National Information Infrastructure
WLAN	Wireless Local Area Network
μm	Micron or micrometer

Signal Representation

The following signal representation will be used in this work [1].

$$v_A = V_A + v_a \quad (1)$$

Where V_A and v_a represent the DC and AC components, respectively, of the total signal v_A .

Chapter 1: Introduction

1.1 Motivation for this Work

The wireless industry has experienced a significant growth in the past several years [2]. In order to have smaller products with more features, lower power consumption, and shorter design cycles, the size and complexity of the radio frequency (RF) section of the product must be reduced. To explain this impact on the RF section one must briefly examine radio receiver architecture.

A radio receives signals at RF containing useful voice or data information. In order to extract this information the RF signal must be down-converted by a mixing process. A traditional method is to mix the RF signal with a signal generated by a local oscillator (LO) to produce a signal at an intermediate frequency (IF), which still contains the useful information. This IF signal can be amplified and filtered with moderate quality components and then demodulated to extract the useful information. A receiver utilizing this method is known as a superheterodyne receiver. Although the superheterodyne system was patented in 1917 by Edwin Armstrong [3], it is still considered state-of-the-art in mobile communications [4].

However, this architecture requires two frequency synthesizers to generate the LO signals required for the frequency conversion from RF to IF and then from IF to baseband. As well, image-reject and IF filters are required, which have typically been implemented with off-chip surface acoustic wave (SAW) filters.

The image-reject filter, located before the mixer, eliminates the signal at the image frequency, which is twice the IF away from the RF that would also be mixed to the IF. The IF filter allows channel selection. The requirement of these filters increases the cost of the receiver because of: a) the filter cost, b) higher packaging costs (a package with 2 more pins is required because the signal must be routed off the chip to the filter and then back onto the chip), and c) the additional space required on the printed circuit board.

Recently, two approaches have been used to overcome this. Image filtering has been successfully implemented on-chip [4]. A second approach is a direct down-conversion architecture in which the RF signal is mixed with a LO signal at the RF with the result that the input RF signal is down-converted directly to the baseband without an IF step [5].

There are, however, challenges involved with direct down-conversion design [2]: a) DC offsets, b) second order intermodulation, c) LO leakage, signal isolation, self-mixing, d) amplitude and phase mismatch, and e) $1/f$ noise at baseband.

This work focuses on the mitigation of DC offsets, which occur in the baseband section following the mixer. This is undesirable for two reasons. First, the downconverted spectrum is centered at 0 Hz so consequently the DC offset occurs in the middle of the spectrum. If information is contained at 0 Hz, the SNR will be degraded. In fact, the offset may be larger than the signal and much larger than thermal or flicker noise. A down-converted signal may have an amplitude of a few hundred microvolts while the DC offset may be in the range of millivolts [6]. Secondly, the DC offset can saturate the following stages [7].

The main causes of DC offsets are component mismatch and self-mixing of the LO signal and in-band interfering signals due to signal leakage resulting from substrate and bond-wire coupling [7]. DC offsets may be mitigated by capacitive AC coupling at the output of the mixer or by feedback.

1.2 Contributions

This work contributes to the knowledge of radio frequency integrated circuit (RFIC) design by providing insight into the implementation of feedback circuits for direct-conversion integrated receivers for the purpose of reducing DC offsets. In this work, the effect of differential-mode feedback was studied and criteria for designing a differential-mode feedback loop (DMFL) were identified. Three circuits to implement the DMFL were designed and simulated. It was found that the ratio of the corrected to uncorrected differential DC output voltage, with the application of feedback, is equal to the inverse of

the open-loop gain of the DMFL. As well, it was found that noise generated by the DMFL circuit is suppressed by the frequency-dependent open-loop gain, such that at frequencies outside of the DMFL frequency bandwidth, the output noise of the DMFL is not suppressed. Therefore, the feedback loop must be designed to have low output noise outside of this bandwidth. A differential op-amp, configured as Miller integrator, has been utilized for the DMFL to generate a dominant-pole low-pass frequency response to reduce the loop gain sufficiently with reasonably sized capacitors that can be realized on-chip.

Results of this research have been published in two conference papers [26] [27].

This work has also merited the award of an “Outstanding Student Designer Award” from Analog Devices Inc. which had a cash value of \$1500 USD.

A provisional patent was filed by Cognio Canada Inc., which was an industrial collaborator, covering the circuit detailed in reference [27].

A direct conversion receiver was designed and tested to allow the measurement of DC offsets due to process variation and LO signal leakage.

1.3 Thesis Overview

Chapter 2: a summary of receiver architectures is presented followed by a description of direct conversion receiver design issues. Suggested design techniques for direct conversion receivers are summarized from the literature. A table of published results is presented.

Chapter 3: gives an overview of the DCR system-level specification including a summary of the IEEE 802.11a standard. The linearity requirement of a DCR is defined in terms of the input-referred second-order intercept point (IIP2). The required IIP2 for this application is derived. The system and RF block specifications are presented.

Chapter 4: describes the DCR circuit design beginning with a summary of IBM's BiCMOS 5AM integrated circuit fabrication technology. A description of the differential LNA, double-balanced mixers and common-mode feedback circuits follow, as well as a figure of the layout.

Chapter 5: presents the theory of DC offset correction using differential feedback, beginning with a review of general system-level feedback. A system-level DC offset correction loop is analyzed, followed by a circuit-level analysis.

Chapter 6: details the design of three differential-mode feedback loop (DMFL) circuits: an initial DMFL circuit, an improved DMFL and a final solution.

Chapter 7: summarizes the experimental results of the DCR.

Chapter 8: presents the conclusions and suggested future work as well as summarizing contributions to the field of RFIC design. Published conference papers are listed as well as awards and provisional patents.

Appendix A presents an analysis of the single-side-band noise figure, double-side-band noise figure and the input referred noise of an ideal mixer, comparing hand-calculations to simulation results.

Chapter 2: Background

2.1 Summary of Receiver Architectures

The purpose of a radio receiver is to receive a modulated signal, containing useful information, and extract this information. Various architectures have been developed for this purpose.

2.1.1 Superheterodyne

The superheterodyne architecture (Figure 1) was first patented in 1917 by Edwin Armstrong [3]. His motivation for using this architecture was that the available technology at that time could not provide adequate gain at high frequencies. As a result Armstrong used this architecture to translate incoming signals to a lower frequency where more gain was available.

There were, however, other benefits to this architecture. The radio could be tuned to a specific channel by changing the frequency of the local-oscillator rather than the bandpass of an input filter. This architecture does, however, require band-select, image reject and channel select filters.

Figure 1 - Superheterodyne Architecture

The band-select filter removes out-of-band signals that may overload the low-noise amplifier (LNA) [8]. The image-reject filter attenuates signals at the image frequency that is twice the IF away from the LO frequency, which are mixed to the IF along with

the desired RF signal. The higher the IF, the more relaxed are the requirements of the image-reject filter, but a higher quality (Q) is required of the channel filter. Finally, the channel filter removes the unwanted channels.

There are disadvantages to the superheterodyne architecture. Traditionally, filters have been implemented with off-chip SAW filters or off-chip dielectric/ceramic resonators. Off-chip filters require inconvenient impedances and the required matching networks that may impact noise, gain, linearity and power consumption. Recently, however, research has been done to implement the image-reject filter on-chip [4]. Narrower bandwidths increase the sensitivity of the filtering to variations in the matching network element values. The requirement of an IF filter, which is designed for a specific channel bandwidth and therefore a specific standard, makes superheterodyne receivers unsuitable for multi-standard operation.

Advantages of the superheterodyne architecture include high selectivity and sensitivity due to the use of high-Q filters.

2.1.2 Image Reject

The image reject architecture utilizes the phase relationship between the desired and undesired image frequency to cancel the image frequency during mixing. Thus, with exact phase offsets an image-reject filter is not required. Two implementations are the Hartley and the Weaver architectures.

Hartley Image-Reject Architecture

In this implementation (Figure 2) the RF signal is down-converted to an IF by two separate mixers. The two LO signals differ in phase by 90° . In one branch, the down-converted image frequency and desired frequency are in phase. In the other branch the signals differ in phase by 180° . A 90° phase shifter is included in the branch with the in-phase desired and image IF products, which effectively shifts the phase of these signals so they are in-phase with the down-converted desired frequency in the other branch and 180° out-of-phase with the down-converted image frequency. The signals from the two

branches are then added and the down-converted image frequency terms cancel out and the desired terms add.

Figure 2 – Hartley Image-Reject Architecture

Weaver Image-Reject Architecture

This implementation (Figure 3) achieves the 90° relative phase shift of one path by the use of a second mixer.

Figure 3 - Weaver Image-Reject Architecture

Image Reject Ratio

Image rejection ratio (IRR) is defined as the ratio of the power in the desired signal to the image signal as follows [5]:

$$IRR = \frac{power_{desired}}{power_{image}} \quad (2)$$

Image rejection depends on the phase delay and amplitude gain of the branches of the image-reject receiver, and may be expressed as [3]:

$$IRR \approx \frac{4}{\varepsilon^2 + (\Delta\phi)^2} \quad (3)$$

Where ε is the relative voltage gain mismatch and $\Delta\phi$ is the phase imbalance in radians. As an example $IRR = 41$ dB with 0.1% gain error and 1° phase error.

Achieving a high IRR is a challenge with this architecture because gain and phase error are introduced by device mismatch which is inherent to fabrication processes. As well, the phase delay associated becomes larger as frequency increases. For example, the phase error of a 5 GHz signal is five times greater than a 1 GHz signal for a given length of transmission line. Typically IRR's of image reject receivers are in the range of 25-35 dB [5] in this frequency range. Therefore, the image reject architecture is not very suitable for operation in the unlicensed national information infrastructure (UNII) band, within the frequency range of 5 GHz – 6 GHz.

Calibration techniques may be implemented which reduce amplitude and phase imbalance, but also increase the complexity of the receiver. As an example a Weaver image reject receiver with a calibration technique that reduces the gain and phase errors has been reported in the literature. The uncorrected IRR is 25dB - this is improved to 57dB with calibration [9].

In summary, the disadvantage of this architecture is that achieving a high IRR requires exact amplitude and phase matching between the two branches, which is difficult to realize due to process variation. The main advantage is that it does not require an image reject filter.

2.1.3 Low IF Single Conversion

The low IF single-conversion architecture is a variant of the superheterodyne architecture (Figure 1), with the advantage that a high Q IF filter is not required because of the low center frequency of the IF filter. If the IF is low enough, image rejection must be accomplished with quadrature mixing with the advantage that the image reject filter is not

required. The advantages and disadvantages of the image-reject architecture, therefore, also apply. Another advantage is that DC offsets are not problematic as AC coupling may be utilized.

The low IF signal can be converted to baseband using another mixer or in the digital domain. A disadvantage is that this requires expensive, fast, and high-resolution A/D converters.

2.1.4 Wide-Band IF with Double Conversion

Another variant of the superheterodyne architecture (Figure 1) is the Wide-Band IF with Double Conversion architecture, in which the RF signal is mixed to the IF with a mixer utilizing an LO at a fixed frequency. All channels in the RF band are translated to IF, retaining their positions relative to one another. The advantage is the use of a wide-band IF filter, which therefore has a lower quality factor. A second mixer utilizes a tunable LO, thus selecting the desired channel to be translated to baseband. A subsequent low-pass filter suppresses adjacent channels.

A disadvantage is that two LO sources are still required.

2.1.5 Walking IF Superheterodyne

In yet another variant of the superheterodyne architecture (Figure 1), called the walking IF superheterodyne architecture, the RF signal is downconverted to an IF and this IF is then downconverted to baseband. The first and second LO frequencies are fractions of the RF. For example, for an RF of 5GHz, the first LO frequency could be $\frac{4}{5}$ of the RF or 4GHz. The second LO would then be $\frac{1}{5}$ of the RF or 1GHz. As the receiver is tuned for a different channel both the first and second LO frequencies remain at $\frac{4}{5}$ and $\frac{1}{5}$ of the RF. One advantage is that the LO signals can be generated from one frequency synthesizer. Another advantage occurs if the IF is high enough. An image-reject filter may not be required if the bandpass frequency response of the LNA attenuates signals at

the image frequency adequately. As well the problems associated with direct conversion, which will be outlined in Section 2.1.6, are avoided. A transceiver using this architecture has been reported in the literature [25].

2.1.6 Direct-Conversion

In the direct conversion architecture (Figure 4) the RF signal is amplified and demodulated directly to baseband in-phase (I) and quadrature-phase (Q) signals. Channel selection is achieved with on-chip low-pass filters. Gain control is achieved at baseband with an on-chip variable gain amplifier (VGA).

Advantages include:

1. IF filters are not required since channel filtering is now achieved with baseband analog filters.
2. Baseband filters may be programmable, making this architecture suitable for multi-band and multi-standard operation.
3. Higher levels of integration - fewer components are required and cost is lowered.
4. Only one LO is required and therefore only one phase noise contributor exists.
5. The image rejection problem is eliminated because the image to the channel is the channel itself.

Figure 4 - Direct-Conversion Architecture

There are however design challenges associated with direct conversion:

1. DC offsets
2. 2nd order nonlinearity
3. LO leakage
4. Gain and phase imbalance
5. $1/f$ noise

These challenges will be elaborated on in Section 2.2.

2.2 Direct Conversion Design Issues

2.2.1 DC Offsets

DC offsets may be attributed to four mechanisms as follows:

1. The LO signal may reach the mixer's RF input port by substrate or bondwire coupling, thus effectively mixing with itself, producing an unwanted DC component at the mixer output (Figure 5).

Figure 5 – Self-mixing due to LO Leakage

2. A strong in-band interference signal, once amplified by the LNA, may find a path to the LO-input port of the mixer, once again resulting in self-mixing (Figure 6) and an unwanted DC component at the output of the mixer.

Figure 6 - Self-mixing due to a Strong Interferer

3. Some amount of LO power will be conducted through the mixer and LNA (due to their non-ideal reverse isolation) to the antenna (Figure 7). Note, the LO frequency is within the passband of the LNA and RF port of the mixer. The radiated power, appearing as an interferer to other receivers in the corresponding

band, may violate the emissions standards of the given system. Additionally, the radiated LO signal can then be reflected by buildings or moving objects and re-captured by the antenna.

Figure 7 - Self-mixing due to LO leakage and Reflection/Refraction

4. Circuit imbalances cause DC offsets as well. For example, consider a differential amplifier with a resistive load (Figure 8). For this analysis the DC offset will be modeled by a mismatch (ΔR) in the load resistors (R_{L1} and R_{L2}) due to process variation.

$$R_{L2} = R_{L1} + \Delta R \quad (4)$$

Given the difference in resistor values, an uncorrected DC offset voltage (V_{DM_U}) is generated and may be calculated as follows:

$$V_{DM_U} = V_{cc} - I_o R_{L1} - (V_{cc} - I_o R_{L2}) \quad (5)$$

$$V_{DM_U} = I_o \times \Delta R \quad (6)$$

Figure 8 - Differential Amplifier with DC Offsets

Example: Effect of DC Offsets

This example illustrates how DC offsets at the DCR baseband output may be as large as the received desired signal, corrupting the desired signal and possibly saturating the following gain stages. The source of DC offset in this example is self-mixing due to LO leakage (Figure 9).

Assume the total gain from the antenna to input of the analog-to-digital converter (ADC), which follows, is approx. 100dB. The LO signal has a peak swing of 0.63V (0 dBm in a 50Ω system). The LO signal couples to the LNA input with 60dB of attenuation and the LNA/mixer gain = 20dB. The DC Offset at output of the mixer will then be 6.3mV.

Figure 9 - DC offset Example

The desired signal at the DCR input may be as small as -82 dBm [10] (17.8 uV in a 50 Ω system). The desired signal at the LNA/mixer output will then be 0.18 mV, which is an order of magnitude smaller than the DC offset.

As well, the DC offset, when multiplied by the remaining gain (80 dB) will saturate the output. Smaller offsets will corrupt the signal if it contains information at 0 Hz.

2.2.2 Second-Order Nonlinearity

Second-order nonlinearity can down convert continuous wave (CW) as well as amplitude modulated (AM) blockers to DC or near DC, causing SNR degradation. For the case of CW signals, consider a signal $v_{cw} = A \cos(\omega t)$. The second order non-linearity of the receiver will generate a DC signal as follows:

$$v_{2ndorder} = (A \cos(\omega t))^2 = \frac{1}{2} (A^2 + A^2 \cos(2\omega t)) \quad (7)$$

$$\therefore V_{DC} = \frac{1}{2} A^2 \quad (8)$$

Now, consider two CW blockers, $v_{cw1} = A_1 \cos(w_1 t)$ and $v_{cw2} = A_2 \cos(w_2 t)$. The second-order nonlinearity of the receiver will result in the generation of signals at other frequencies as shown below.

$$\begin{aligned}
 v_{2ndorder} &= a_2 (A_1 \cos(w_1 t) + A_2 \cos(w_2 t))^2 \\
 &= a_2 (A_1^2 \cos^2(w_1 t) + 2A_1 A_2 \cos(w_1 t) \cos(w_2 t) + A_2^2 \cos^2(w_2 t)) \\
 &= a_2 \frac{A_1^2}{2} (1 + \cos(2w_1 t)) \\
 &\quad + a_2 A_1 A_2 [\cos((w_1 - w_2)t) + \cos((w_1 + w_2)t)] \\
 &\quad + a_2 \frac{A_2^2}{2} (1 + \cos(2w_2 t))
 \end{aligned} \tag{9}$$

Therefore, the second-order non-linearity will result in a signal at the difference frequency of the two signals as follows:

$$v_{cw_interferer} = a_2 A_1 A_2 [\cos((w_1 - w_2)t)] \tag{10}$$

If the frequency difference ($w_1 - w_2$) is within the baseband channel bandwidth of the receiver, this will appear as an unwanted tone (noise) and reduce the SNR of the desired signal.

Next, consider an amplitude modulated signal $v_{am} = (1 + m(t))A \cos(wt)$. The second-order non-linearity will result in the demodulation of the signal as follows:

$$v_{2ndorder} = a_2 [(1 + m(t))A \cos(wt)]^2 \tag{11}$$

$$\begin{aligned}
 &= a_2 (1 + 2m(t) + m^2(t))A^2 \cos^2(wt) \\
 &= a_2 (1 + 2m(t) + m^2(t)) \left[\frac{A^2}{2} (1 + \cos(2wt)) \right]
 \end{aligned} \tag{12}$$

Equation (12) contains the following term, which arises from the demodulation of the AM signal by the second-order non-linearity of the receiver.

$$v_{am_interferer} = \frac{a_2 A^2}{2} [2m(t) + m^2(t)] \quad (13)$$

If the frequency of the modulated signal is within the baseband bandwidth it will appear as noise, again degrading the SNR of the received signal.

2.2.3 LO Leakage

Since the LO frequency is within the passband of the LNA and Mixers, spurious emissions may be difficult to suppress in a DCR. Spurious emissions result from the LO signal leaking through the mixer and the LNA to the antenna where it is radiated. These spurious emissions will act as blockers for other receivers and may be reflected/refracted from surrounding objects and received by the DCR, resulting in DC offsets which vary with time.

2.2.4 Amplitude and Phase Imbalance

Gain and phase mismatch between I and Q paths of the DCR can cause asymmetry and rotation in the signal constellation. Figure 10 is an example of the effect of gain mismatch between the I and Q paths. This causes error-vector-magnitude (EVM) degradation defined as follows [11]:

$$EVM = \sqrt{\frac{P_e}{P_r}} \quad (14)$$

$$P_e = power_{error_vector} \quad (15)$$

$$P_r = power_{reference_vector} \quad (16)$$

Where P_r is the ideal reference vector and P_e is the error vector due to mechanisms such as gain and phase mismatch. Allowable EVM degradation depends on modulation technique.

Figure 10 - Constellation with DCR I and Q Path Amplitude Imbalance

2.2.5 Flicker Noise

For direct conversion, the RF signal is mixed directly to baseband. A form of noise that occurs at low frequencies is called flicker noise ($1/f$ noise). Flicker noise can therefore degrade the signal-to-noise ratio (SNR) significantly depending on the demodulated signal bandwidth. Flicker noise is inversely proportional to frequency. It is technology dependant and is caused by various mechanisms, although in transistors it is attributed to charge trapping. Charge trapping can be caused by defects and impurities, which usually occur at the semiconductor surface. As well, forward-biased junctions exhibit flicker noise. Therefore, flicker noise occurs in MOSFETS, which have current flowing along the surface of the channel material and bipolar devices, which utilize forward biased base-emitter junctions [3].

A figure of merit for determining the significance of flicker noise is the “corner frequency,” which is the frequency where the flicker noise and thermal or shot noise components are equal. The corner frequency is typically below tens or hundreds of hertz for bipolar devices and in the tens of kilohertz to one megahertz range for MOSFET devices. The corner frequency is inversely proportional to gate area for MOSFET devices because the gate capacitance acts to reduce the fluctuation in channel charge. The corner frequency is inversely proportional to junction area for bipolar devices [3].

2.3 Suggested Design Techniques from the Literature

Various techniques have been suggested in the literature for overcoming the challenges associated with DCR design.

2.3.1 2nd Order Nonlinearity

Second-order linearity may be improved with circuits with high common-mode rejection [11]. As well, higher relative bias levels generally result in improved linearity.

Suppression of low-frequency components after 2nd-order distortion has been suggested by utilizing capacitive coupling between the LNA and mixer and capacitive degeneration of the LNA [7] (Figure 11). This will result in low gain at low frequencies. One concern with this is that a single-ended LNA with capacitive degeneration may have potential stability issues, since capacitance at the emitter will be transformed to a negative resistance at the base of the transistor.

Figure 11 - Mixer with capacitive degeneration.

Linearization of the RF path with feedback has also been suggested [7]. A single-balanced mixer with feedback from the mixer to LNA is shown in Figure 12. Capacitor C_2 senses the voltage at the emitter of Q_3 and provides a feedback voltage at the base of Q_1 . The collector current of Q_3 is then roughly equal to $V_{RF}C_1S$, indicating a very linear transconductance of the LNA/transconductance-stage of the mixer.

One consideration with this implementation is the significance of parasitics at higher frequencies such as 5GHz. A 1nH bondwire represents a reactance of 31Ω . It will be shown later that for a single-ended LNA optimized for a simultaneous noise and conjugate match in IBM's sige5am process, an emitter inductance of approximately 0.3nH is required. The designer may be forced to implement this inductance with a bondwire. The effect on the input match of the non-optimal bondwire inductance and its process dependency would need to be carefully considered.

Figure 12 - LNA/mixer with capacitive feedback.

2.3.2 LO Leakage

The reduction of LO leakage with fabrication techniques such as deep trench isolation will not only reduce DC offsets but also spurious emissions.

2.3.3 1/f Noise

Flicker noise can be minimized by the use of bipolar devices rather than MOSFET's or a low-IF architecture [11]. As well, as mentioned in Section 2.2.5, MOSFET devices may be sized to reduce flicker noise.

2.3.4 Amplitude/Phase Matching

Amplitude and phase imbalance may be reduced with poly phase networks, the use of a quadrature VCO [11] or analog/digital calibration techniques. A system-level example of phase correction from the literature utilizes a calibration loop [7] (Figure 13).

In calibration mode, LNA A1 is disabled and LNA A2 injects a signal slightly different in frequency than the LO signal. The down-converted quadrature signals are low-pass filtered and mixed to produce a DC voltage proportional to the phase difference. This voltage is used to adjust the phase shift of delay lines $\Delta 1$ and $\Delta 2$ until the phase shift between the I and Q signals is 90° . Obviously, this implementation requires additional circuitry to control the switches (S1 and S2) and disable/enable the amplifiers (A1 and A2).

Figure 13 - System-level I/Q Calibration Example

2.3.5 DC Offset Mitigation

DC offset mitigation can be achieved with:

1. Capacitive coupling with a DC-free modulation scheme [7]
2. Offset cancellation [7]
3. Dynamic calibration [11]
4. High linearity circuits [11]
5. Deep trench isolation to suppress LO leakages [11]
6. Sub- or super- or fractional harmonic down-conversion [11]

Capacitive Coupling

One way to remove unwanted DC offsets is to use capacitive coupling in the signal path. This is equivalent to high-pass filtering so one must ensure that the corner frequency of the filter is well below the frequency spectrum of the received data to avoid corrupting the signal.

Offset Cancellation

Some communication standards utilize time-division multiple access (TDMA) in which a transceiver only uses the communication channel for a specified amount of time so that multiple transceivers can share the channel. It is possible during the rest period to

measure the DC offset by charging a capacitor and then subtracting this offset voltage from the signal when it is being received.

Dynamic Calibration

Dynamic calibration of DC offsets may include the use of compensation schemes using digital sample-and-hold feedback or feedback-loops.

High Linearity Circuits

Circuits with high second-order linearity will reduce the generation of DC offsets by LO self-mixing and signal leakage as outlined in Section 2.3.1.

Deep trench Isolation

The use of deep-trench isolation, if available in the fabrication process, will improve signal isolation on the chip and reduce signal and LO self-mixing.

Sub-Harmonic Down-Conversion

In sub-harmonic down-conversion (Figure 14) the LO frequency is a fraction of the RF, for example $RF/2$. The LO signal is then multiplied by 2 before being applied to the mixer. This has two benefits. First, the voltage-controlled oscillator (VCO) is not operating at the same frequency as the power amplifier and will not suffer from frequency “pulling”, in which the power amplifier (PA) will cause the VCO to vary from the desired center frequency. As well, there will be less self-mixing of the LO signal since leakage from the VCO that reaches the input of the mixer will be half the frequency of the LO signal. This scheme would require tight coupling between the multiplier and mixer to reduce coupling of the multiplier output signal with the input of the mixer.

The multiplier could be implemented as a Gilbert Cell with quadrature input signals.

Figure 14 - Sub-harmonic Mixer Block Diagram

As well, the VCO could operate at $RF/3$ and a $x3$ multiplier used. A possible implementation of the $x3$ multiplier would use a limiter, which limits the VCO signal, creating a square wave and thus generating odd-order harmonics from which the 3rd harmonic could be filtered.

Super-Harmonic Down-Conversion

In this scheme the VCO operates at a multiple of the RF and has the same advantages as the sub-harmonic scheme. For example, one could use a VCO frequency of twice the RF (Figure 15).

Figure 15 - Super-harmonic Mixer Block Diagram

This scheme could be implemented with a digital $\div 2$ and Gilbert Cell Mixer.

Fractional-Harmonic Down-Conversion

In this scheme the VCO is operated at a fractional multiple of the RF (Figure 16) and has the same advantages as the sub-harmonic scheme or super-harmonic schemes. For example, one could use a VCO frequency of 1.5 times the RF. This could be implemented with a digital $\div 3$ with a Gilbert Cell multiplier.

Figure 16 - Fractional-harmonic Mixer Block Diagram

LO Multiplier Techniques

Each of the sub-, super- or fractional harmonic down-conversion schemes requires a multiplier for the VCO output signal. The following are possible implementations of this multiplier.

1. Phase Locked Loop – this well known method of frequency multiplication is relatively complex to implement.
2. Limiter with filtering – the VCO output signal could be limited, thus producing odd-order harmonics. The 3rd order harmonic could then be filtered. The filtering network may require significant die area.

3. Gilbert-cell Multiplier – the VCO output signal could be applied in quadrature to both ports of a Gilbert-cell multiplier.

LO Divider Techniques

A method for dividing the VCO frequency may also be required. The following are possible implementations of this divider.

1. Digital $\div 2$ Divider

A standard digital divide-by-two divider (Figure 17) could be implemented with D-latches. A benefit is quadrature outputs are available.

Figure 17 - Digital $\div 2$ Divider

2. Digital $\div 3$ Divider

A digital divide-by-three divider may also be utilized (Figure 18). This implementation utilizes a variant of the D-latch with an extra input (Θ); see Table 1. As Table 1 shows, the signal at D is only passed to the output Q when both the control signal (Θ) and the clock signal (CLK) have the same state. The divider has three outputs, Q1, Q2, and Q3 which will have 1/3 the frequency of the clock. Q2 will be 60° out of phase with Q1 and Q3 will be 60° out of phase with Q2.

Table 1 - Truth Table for Modified D-latch

D	Θ	CLK	Q
0	0	0	0
0	0	1	Hold
0	1	0	Hold
0	1	1	0
1	0	0	1
1	0	1	Hold
1	1	0	Hold
1	1	1	1

This logic could be implemented with emitter-coupled-logic (ECL) to allow high-frequency operation.

Figure 18 – Digital ÷3 Divider

Example: Double-Conversion with $w_{lo1}=w_{lo2}=w_{rf}/2$

An interesting special case of a sub-harmonic architecture (Figure 19) is implemented by moving the x2 multiplier function into the RF signal path (Figure 20). This is equivalent to a double-conversion architecture in which both the first and second LO frequencies are equal to half the RF [1].

Figure 19 - Subharmonic Architecture

Figure 20 - Double-Conversion Architecture with $w_{lo1}=w_{lo2}=w_{rf}/2$

The receiver performs two down-conversions, each using an LO frequency equal to half the RF. The input signal center frequency is therefore translated from the RF to an IF equal to half of the RF and then to zero.

This offers some advantages:

1. The image frequency is at 0Hz and can be suppressed using AC coupling.
2. As well, AC coupling between the mixers rejects the DC offset generated by the first mixer, while the signal is amplified.
3. There is no LO leakage to the antenna in the RF band.
4. The frequency synthesizer operates at half the input frequency (VCO and frequency dividers operate at lower frequencies and quadrature phases may be easier to generate).

An assumption here is the DC offset generated by LO leakage to the input of the second mixer is negligible.

Some design challenges are:

1. The image frequency is at 0Hz so flicker noise from the LNA and input stage of the first mixer is up-converted to the first IF, degrading the SNR.
2. The LO-IF feed-through of the first mixer is at the IF and therefore cannot be filtered. This is a mechanism for generating DC offsets and could be a significant problem.
3. The IF is at a high frequency and cannot be filtered so the second mixer must have high linearity.

Two receivers utilizing this technique have been reported in the literature. A SiGe RF front-end for use in direct-conversion receivers for the UNII bands has been reported [12]. The front-end is composed of an LNA, I and Q x2 sub-harmonic mixers (SHM) and an LO conditioning chain (Figure 21).

Figure 21 - A SiGe Active Sub-Harmonic Front-End for 5-6GHz Direct-Conversion Receiver Applications

A disadvantage of the receiver in Figure 21 is the requirement for quadrature LO signals in each of the I and Q channels. A phase imbalance in these LO signals results in an additional phase imbalance in the I/Q channels. Therefore, additional circuitry is required to generate these quadrature signals, increasing the complexity of the receiver. In this case poly-phase filters have been used and since these have loss, additional two-stage amplifiers were also included.

A 5.2 GHz CMOS Receiver with 62 dB Image Rejection has been reported [13] (Figure 22). In this case the LO frequency is 2.6 GHz. The receiver was implemented in a 0.25 μm digital CMOS technology and achieves a noise figure of 6.4 dB, an IIP3 of -5 dBm, and a voltage conversion gain of 43 dB, while dissipating 29 mW from a 2.5 V supply.

Figure 22 - A 5.2-GHz CMOS Receiver with 62 dB Image Rejection

One might expect this receiver to have a DC offset problem because, as previously mentioned, the LO-IF feed-through of the first mixer is at the IF and therefore cannot be filtered. Since the first and second LO signals are at the same frequency, an unwanted DC term will be generated at the mixer outputs.

2.4 Published Work

2.4.1 Summary of Published Work

Recently, there has been much research in the area of direct-conversion receivers. Table 2 is a summary of some published results. Note, the amount by which DC offset is reduced has not been reported in the literature. If the total gain of the receiver were required to be 100dB, than even for case 5, with the lowest reported DC offset, the remaining gain of the receiver would result in a 95mV DC offset at the output of the baseband gain stage.

Table 2 - Summary of Some Recently Published Direct-Conversion Receivers

	Ref.	Supply (V)	Gain (dB)	IIP2 (dBm)	Power (mW)	NF (dB)	Frequency Band	DC Offset	Technology
1	[12]	3.3	18	*	129	6.8	U-NII 5-6GHz	*	0.5um SiGe BiCMOS
2	[14]	1.8	21-47	+44.8	37.8	5.6	UMTS[15] 2140MHz	*	0.18 um CMOS
3	[16]	3.0	*	*	294	5.5	802.11a WLAN 5-6GHz	30mV at output of baseband amplifiers	0.5um SiGe BiCMOS
4	[17]	3.3	12	*	17.8	11.5	17GHz	<4mV at mixer ouput	0.5um SiGe BiCMOS
5	[18]	2.85	45.7	+37	71	4.3	UMTS 2140MHz	<300uV at mixer output	0.25um SiGe BiCMOS
6	[19]	1.8	74	*	108	4.4	WLAN 4.9 – 5.95 GHz	*	0.18um CMOS
7	[20]	2.5	31	+23	40	2.5	802.11a WLAN 4.9-6GHz	*	0.25um BiCMOS

* not reported

2.4.2 Additional Notes

1 – The reported noise figure is simulated.

2 – This receiver implements the DC-offset reduction at the variable gain amplifier (VGA), which follows the mixer. It requires 3mm/1um nMOS devices to have low 1/f noise and uses a Miller integrator with four 450pF on-chip capacitors for a total of 1.78-nF capacitance entirely integrated on-chip!

- 3 – This receiver uses DC offset cancellation servo circuitry and the residual DC offset is reported as 30mV!
- 4 – This work is on a Direct Down-Conversion Mixer and DC offsets were not addressed. The DC-offsets at the output of the chip were measured to be less than 4mV.
- 5 – LO is fed into chip at twice the RF.
- 6 – This paper did not mention how the DC offset issue was addressed.
- 7 - This paper did not mention how the DC offset issue was addressed.

2.5 Conclusion

This chapter presented an overview of research that has been reported on direct-conversion receivers and possible solutions to the individual design challenges associated with this architecture. Advantages and disadvantages of each approach have been listed.

Additionally, it is important to explain and justify the focus of this thesis. Of the five design challenges listed (Section 2.1.6), DC offsets were selected, rather arbitrarily, to address. Seven methods of correcting DC offsets have been listed which include: capacitive coupling with a DC-free modulation scheme [7], offset cancellation [7], dynamic calibration [11], high linearity [11], deep trench isolation to suppress LO leakages [11], and sub-, super- or fractional harmonic down-conversion [11].

This topic of dynamic calibration and the application of analog feedback to correct DC offsets was investigated first and became the topic of this thesis.

It was required to design a receiver to study the DC offsets. It is clear that a DCR design is highly dependant on its application. This research was performed in collaboration with Cognio Canada Inc. with the mandate that it apply to the IEEE 802.11a standard for wireless local area networks (WLANs), operating in the 5-6GHz unlicensed national information infrastructure (UNII) band. Choice of fabrication technology and circuit topology will be discussed in Sections 4.1 and 4.2, respectively

Chapter 3: DCR System Level Specification

3.1 Introduction

This chapter will provide an overview of the IEEE 802.11a standard and the impact it has on the receiver linearity. As mentioned earlier, second-order non-linearity is important for direct-conversion receivers because it generates DC offsets as well as demodulating amplitude-modulated signals which may corrupt the desired signal.

3.2 IEEE802.11a Standard

Developed by the IEEE, 802.11 refers to a family of standards for wireless local area networks (WLAN) [21]. It specifies an over-the-air interface between a wireless client and a base station or between two wireless clients. The IEEE accepted the specification in 1997. 802.11a is one extension to 802.11.

The 802.11a standard is allotted 300MHz in the 5GHz unlicensed national information infrastructure (UNII) band, from 5.15GHz – 5.35GHz and 5.725GHz – 5.825GHz. It uses the Orthogonal Frequency Division Multiplexing (OFDM) technique. The reason to use OFDM is to increase the robustness against frequency selective fading or narrowband interference. OFDM is a special case of multicarrier transmission in which a single data stream is transmitted over a number of lower rate subcarriers [22]. In this case a 20MHz wide carrier is subdivided into 52 sub-channels, each 312.5kHz wide. Of these, 48 are used for data and 4 for error correction. A centre sub-channel is left empty to allow for DC offset removal and frequency offset corrections.

Various types of modulation are used in combination with OFDM, which result in different data rates (Table 3).

Table 3 - Data Rates

Modulation	Total Data Rate (Mb/s)
Binary Phase Shift Keying (BPSK)	6
Quadrature Phase Shift Keying (QPSK)	12
16 Level Quadrature Amplitude Modulation (16 QAM)	24
64 Level Quadrature Amplitude Modulation (64 QAM)	54

3.3 Linearity Requirement

3.3.1 What is IP₂?

Nonlinearity of the receiver results in the generation of baseband second-order intermodulation products occurring at the difference frequency of two unwanted in-band interferers, as described in Section 2.2.2. A measure of this nonlinearity is a receiver's second-order intercept point (IP₂). The input referred IP₂ (IIP₂) is the input power level at which the magnitude of the second-order intermodulation products are equal to the magnitude of the fundamental tones. A practical amplifier will saturate below this power level so the intercept point must be found by extrapolation from a lower power level as follows.

IP₂ is calculated by injecting two closely spaced low-power tones into the receiver and measuring the power levels of the second-order inter-modulation products at the receiver

output. Since the second-order tones increase at twice the rate of the fundamental tones, as the input power is increased, the IIP_2 can easily be calculated as follows:

$$IIP_2 = P_f + (P_f - P_{so}) = 2 \bullet P_f - P_{so} \quad (17)$$

3.3.2 DCR IIP2 Requirement

The required linearity for the receiver is calculated as follows:

1. Determine the required minimum detectable signal,
2. Determine the signal-to-noise ratio (SNR) for the allowable packet error rate (PER) as defined by the standard,
3. Determine maximum allowable interfering signal, which in this case is the second order intermodulation (IM_2) product,
4. Calculate minimum second-order intermodulation product intercept (IIP_2).

The minimum detectable signal (sensitivity level) for each data rate is listed in Table 4:

Table 4 – Receiver Performance Requirements [10]

Data Rate (Mbits/sec)	Minimum Sensitivity (dBm)
6	-82
9	-81
12	-79
18	-77
24	-74
36	-70
48	-66
54	-65

The SNR's for a packet error rate (PER) < 10% at different data rates are listed in Table 5:

Table 5 – Required SNR for a PER < 10% at Different Data Rates

Data Rate (Mbits/sec)	SNR (dB)
6	1
54	18.5

Therefore, the minimum signal at the LNA input = -82 dBm – 3 dB (assumed filter loss in front of LNA) = -85 dBm. The maximum tolerable interferer = min. signal – SNR – NF = -85 dBm – 1 dB – 15 dB = -101 dBm. Therefore, the maximum tolerable IM_2 product (P_{so}) = -101 dBm.

The maximum input level amplitude of the interferer (P_f) is -30 dBm at the antenna or -33 dBm at LNA input [10]. The minimum IIP2 may be calculated from (17) as follows:

$$IIP_2 = 2 \bullet (-33) - 101 = +35 \text{ dBm} \quad (18)$$

Therefore, the required IIP_2 for a data rate of 6 Mbits/sec is +35 dBm. Similarly, the required IIP_2 for a data rate of 54 Mbits/sec is calculated to be +35.5 dBm. This is summarized in the following Table 6.

Table 6 – Required IIP2 for Different Data Rates

Data Rate (Mbits/sec)	SNR (dB)	Calculated Minimum IIP2 (dBm)
6	1	+35
54	18.5	+35.5

3.4 DCR System and Block Level Specifications

Specifications for the entire direct conversion receiver (DCR) compliant with the IEEE 802.11a WLAN specification follow:

Table 7 - Direct Down Conversion Receiver Specifications [5]

1	Frequency Range	5.15 – 5.35	GHz
2	Noise Figure	<10	dB
3	Maximum input signal	-30	dBm
4	Input P_{1dB}	>-26	dBm
5	IIP3	>-16	dBm
6	Limits on spurious emissions	<-57 dBm for freq.< 1GHz	dBm
		<-47 dBm for freq. > 1GHz	dBm

This work only includes an LNA and mixer. Requirements for the LNA/mixer are found in Table 8. The required IIP2 was determined in section 3.3.2. The voltage gain, noise figure, current consumption and supply voltage were selected to meet system-level requirements defined by Cognio. The IIP3 requirement and spurious emissions were found in the literature [5].

Table 8 – LNA/mixer Requirements

	LNA/Mixer	Units
Frequency Range	5.15GHz – 5.35	GHz
Voltage Gain	25	dB
NF	5	dB
IIP3	-16	dBm
IIP2	+35.5	dBm
Icc	18	mA

Additionally: $V_{cc} = 2.75V$

Spurious Emissions [5] = -57dBm $f < 1GHz$, -47dBm $f > 1GHz$

3.5 Conclusion

As explained in Section 3.2, the 802.11a standard utilizes orthogonal frequency division multiplexing (OFDM), allowing the reception of several sub-carriers simultaneously. The standard has left the center sub-carrier unused, which is centered at 0Hz when the RF signal is demodulated to base-band. This sub-carrier has a bandwidth of 156.25kHz. Therefore, a feedback loop can be implemented to reduce DC offsets, which operates within this bandwidth.

The impact of second-order non-linearity on DCR performance requires the definition of an IIP2 specification, which has been derived in Section 3.3.2. It was found that a minimum IIP2 of 35.5dBm is required to avoid degradation in packet error rate.

Requirements for the LNA/mixer performance were defined by a number of sources, including linearity requirements unique to direct-conversion receivers, the system-level requirements of Cognio and the 802.11a standard.

Chapter 4: DCR Circuit Design

4.1 Integrated Circuit Fabrication Technology - IBM's BiCMOS

5AM

The integrated circuit technology was selected by Cognio to be IBM's 0.5 μ m 50GHz BiCMOS technology with analog metal option [23]. This process offers two types of scalable npn heterojunction bipolar transistors (HBTs). The first is a standard device meant for high-speed, small-signal applications with a breakdown voltage (BV_{ceo}) of 3.3V and f_T and f_{max} of 50GHz and 65GHz, respectively. The second is a high-breakdown device meant for power amplifiers and other analog applications and has a BV_{ceo} of 5.8V and f_T and f_{max} of 30GHz and 50GHz, respectively.

As well, it offers n-type field-effect transistors (NFET) and p-type field effect transistors (PFET) with drawn gate lengths of 0.5 μ m. This allows mixed-signal circuits to be implemented.

This process is only available with four aluminum metal layers for multi-project wafer runs. The top-metal layer is 4 μ m thick for improved passives. Passive devices include: polysilicon and implanted resistors; varactor, schottky and PIN diodes; on-chip inductors; MOS and metal-insulator-metal (MIM) capacitors.

4.2 A 5GHz Direct-Conversion Receiver with Common-Mode Feedback

4.2.1 Introduction

The receiver consists of a differential LNA and two double-balanced mixers, as shown in Figure 23.

Figure 23 - Direct-Down-Conversion Receiver System-Level Diagram

As previously mentioned, DC offsets and second-order distortion are two of the design challenges of the DCR architecture. One mechanism for the generation of unwanted DC offsets is leakage of the LO signal into the LNA or mixer where second-order nonlinearity generates a DC component. As well, closely spaced AM and CW in-band blocking signals can be mixed down to baseband, by 2nd order distortion, degrading the signal-to-noise ratio.

For this reason a differential topology has been selected because of the lower second order distortion performance compared to a single-ended implementation. As well, operation in the 5-6GHz band is required and circuit parasitics become significant at this frequency. For instance, a bondwire with an inductance of 1nH will have a reactance of 31Ω at 5GHz. A differential topology allows the inductance in the emitter path of the LNA to be more accurately controlled because it can be implemented with an on-chip metal trace (having a per unit inductance of approximately 0.1nH/100um of length), rather than bondwires.

4.2.2 Differential LNA

The LNA is designed to have a simultaneous minimum NF and conjugate match and is resistively loaded allowing broadband operation. A schematic of the LNA is shown in Figure 24. A cascode differential pair is utilized for improved frequency response and reverse isolation. The amplifier is resistively loaded to avoid the use of on-chip inductors and provide broadband operation. R_{C1} and R_{C2} also behave as RF chokes. The bias current (I_{bias} in Figure 24) is 7.4 mA.

Figure 24 - LNA with resistive load

The collector current is steered into the low impedance input of the double-balanced mixers. Consequently, the LNA has a very small voltage gain when in cascade with the mixers. The use of inductive emitter degeneration, appropriate transistor sizing and biasing, allow a simultaneous minimum noise figure and conjugate input match [8]. The required emitter inductance is small enough to be provided by a short top-metal trace.

The series input inductance is provided by the input bond-wires. There are no other inductors on-chip. Component values for the LNA are listed in Table 9.

Table 9 – LNA Component Values

Device Type	Reference Designator	Parameters
npn transistor	Q_1, Q_2, Q_3, Q_4	EmitterArea = $27\mu\text{m}^2$
inductor	$L_{\text{transmission line}}$	0.3nH
resistor	R_{c1}, R_{c2}	150Ω

Simulation results for the LNA are listed in Table 10. Simulation results are also listed for the case of a 5% emitter area mismatch between Q1 and Q2.

Table 10 – LNA Simulation Results

Parameter	Simulated	Simulated (5% Area Mismatch)	Units
Voltage Gain	27.6	27.6	dB
S11	-14.7	-14.5	dB
NF	2.2	2.2	dB
IIP3	-3.4	-3.8	dBm
IIP2	+118	+83	dBm
Current	8.4	8.4	mA

Note: $V_{cc} = 2.75\text{V}$, Source and Load impedances = 100Ω , differentially.

4.2.3 Double-balanced Mixer

The mixers consist of Gilbert-cell style switching quads with feedback to control the common-mode collector DC bias point, allowing a large enough resistive load (R_L in Figure 25) to achieve an RF front-end voltage gain in excess of 25dB. A schematic of one of the mixers is shown in Figure 25. The small-signal collector current from the LNA is fed into the low-impedance emitters of the switching transistors. The LO signal is applied to the transistor bases and is not buffered on-chip. The output common-mode DC collector voltage is controlled with a feedback loop and the differential-mode

collector voltage is controlled with a second DC offset-correcting feedback loop and will be discussed in Section 4.2.4 and Chapter 6, respectively.

Figure 25 - Mixer with Gilbert Cell style switching quad and current steering PFET's

Component values for the mixer are listed in Table 11. The bias current (I_{bias2} in Figure 25) is 1.5mA.

Table 11 – Mixer Component Values

Device Type	Reference Designator	Parameters
npn transistor	Q_5, Q_6, Q_7, Q_8	EmitterArea = $10 \mu\text{m}^2$
PFET	M_1, M_2	$W/L = 1.127 \text{ mm}/3 \mu\text{m}$
PFET	M_3, M_4	$W/L = 147 \mu\text{m}/3 \mu\text{m}$
resistor	R_{L1}, R_{L2}	1800Ω
resistor	R_{s_dm}	$50 \text{ k}\Omega$
resistor	R_{s_cm}	$20 \text{ k}\Omega$
capacitor	C_{cc}	2.2 pF

Simulation results for the LNA and mixer are listed in Table 13 in Section 4.2.5.

4.2.4 Common-Mode Feedback

A schematic of the rest of the common-mode feedback (CMFB) circuit is shown in Fig. 26. The differential pair compares the reference voltage (V_{ref}), which is set off-chip, with the common-mode collector voltage of the switching quad shown in Figure 25. The drain current of M5 is then adjusted and mirrored to the two PFET's connected in parallel with the load resistors (R_L) in Figure 25. These PFET's shunt current from the load resistors allowing the collector voltage to be adjusted. With a high enough loop gain, V_{ref} and $V_{CM_{sense}}$ will be approximately equal. The value of V_{ref} is selected to optimize linearity by allowing the maximum range of output voltage swing. Component values for the common-mode feedback circuit are listed in Table 12. The bias current (I_{bias3} in Fig. 26) is 1.5mA.

Table 12 – Common-mode Feedback Component Values

Device Type	Reference Designator	Parameters
npn transistor	Q ₉ ,Q ₁₀	EmitterArea = 5 μm^2
PFET	M ₅	W/L = 196 μm /3 μm
capacitor	C _{cm}	40 pF

The phase margin of the common-mode loop with compensation is shown to be 45° in Figure 27. Uncompensated, the loop has a phase margin of -12° and a dominant pole, introduced by the parasitic capacitance of the PFET's and the associated driving point impedance, at 7 MHz.

Fig. 26 - Common Mode Feedback Circuit

A 40pF capacitor (C_{ccm} in Fig. 26) was added from the gate of the PFET's to the Vcc node, which moved this pole to 2.7 MHz and improved the phase margin to 45°. The open-loop gain is calculated as follows:

$$\frac{V_{BB_out}}{V_{ref}} = \frac{2r_{\pi}}{2r_{\pi} + \frac{R_{s_cm}}{2}} \frac{g_m}{2} \left(\frac{I_{D1}}{I_{C1}} \right) R_L \quad (19)$$

Note, the relatively large impedance in parallel with R_L is not included in the calculation. I_{D1} , R_L , and R_{s_cm} are defined in Figure 25, while I_{C1} and the small-signal parameters r_{π} and g_m are for the differential pair (Q_9 and Q_{10}), shown in Fig. 26. This gives a calculated open-loop gain of 24.7 dB. The simulated open-loop gain is 23.3 dB.

Figure 27 - Common-Mode Feedback Loop - Phase Margin

4.2.5 Results

The simulation results for the DCR are shown in Table 13.

Table 13- Direct-Conversion Specified and Simulated Parameters

	Specified	Simulated	Comments
Frequency Range	5.15GHz-5.35GHz	5.25GHz	
Voltage Gain	25dB	31dB	Input tone: 5.25GHz @ -50dBm, Output Frequency = 10MHz
NF	5dB	4.7dB	Spot double-sideband NF @ 150kHz offset
IIP3	-15dBm	-9dBm	5MHz tone spacing
IIP2	+35.5dBm	+42dBm	5MHz tone spacing
I _{supply}	18mA	16.1mA	Excluding DMFB loop

4.2.6 Layout

Figure 28 shows the receiver layout, which measures $1400\text{ }\mu\text{m} \times 1650\text{ }\mu\text{m}$. Extensive use of deep trench isolation is utilized to reduce substrate leakage of the LO signal. All pads have ESD protection.

Figure 28 - Direct-Conversion Receiver Layout

4.2.7 Conclusion

The receiver has a simulated voltage conversion gain of 25 dB at 5.25 GHz, noise figure of 4.7 dB, IIP3 of -9 dBm , IIP2 of $+42\text{ dBm}$ and draws 16.1 mA from a 2.75 V supply.

Chapter 5: Theory – DC-Offset Correction Using Feedback

5.1 General System-Level Feedback Configuration

The differential-mode DC offset correction loop may be analyzed using feedback theory. Figure 29 shows an ideal feedback configuration system block diagram [24]. The signals S_i , S_o , S_{fb} , and S_ϵ represent the input, output, feedback and error signals, respectively. As well, a and f represent the transfer functions of the basic amplifier and the feedback network, respectively.

Figure 29 - Ideal Feedback Configuration

The open-loop gain is defined as follows [3]:

$$T = af \quad (20)$$

It can be shown that the closed-loop gain, defined as A , is given by:

$$A = \frac{a}{1 + af} \quad (21)$$

As will be elaborated on shortly, and more applicable to the DC offset correction circuit, the ratio of the error signal and input signal may be solved for as:

$$\frac{S_\epsilon}{S_i} = \frac{1}{1 + af} \quad (22)$$

5.2 DC Offset Correction System-Level Feedback

To apply feedback analysis to the differential DC-offset correction loop, one must identify the signals as defined in Figure 29. In this case, as shown in Figure 30, the undesired DC offset voltage (V_{DM_U}) is the input signal to the system (S_i). The voltage (V_{FB}) generated by the ideal feedback loop is the feedback signal (S_{fb}) and the sum of these signals (V_{DM}) is the error signal (S_e).

The quantity of interest is the error signal transfer function, as given in equation (22). The transfer function when applied to the DMFB loop follows:

$$\frac{V_{DM}}{V_{DM_U}} = \frac{1}{1+T} \quad (23)$$

This is the same result that will be found from circuit analysis in (31).

Figure 30- DC Offset Correction Loop - Block Diagram

Additional observations can be made from this analysis. If the feedback loop is opened, the feedback signal (V_{FB}) becomes zero and the error signal (V_{DM}) becomes equal to the DC offset (V_{DM_U}), as one would expect, intuitively. When the loop is closed the error signal reduces to the difference between the DC offset and the feedback signal (V_{FB}). The larger the loop gain (T), the greater the reduction in the undesired DC offset.

5.3 DC Offset Correction Circuit-Level Feedback

A schematic of the DCR showing the LNA, VCO, mixer switching quad transistors (Q1-Q4), load resistors (R_{L1} , R_{L2}) and ideal current sources is shown in Figure 31.

Figure 31 - DCR with ideal DMFL

The differential-mode feedback loop (DMFL) is modeled with an ideal voltage-controlled frequency-dependent current source. The noise generated by the DMFL is modeled with an ideal current source, which injects a noise current (i_{DM_N}) at the mixer output. The DC offset is caused by component mismatch and LO signal self-mixing but for this analysis the DC offset is modeled only by a mismatch in the load resistors of the mixer. The mixer load resistors are shown as R_{L1} and R_{L2} . There is assumed to be a process variation mismatch (ΔR) in these resistors.

$$R_{L2} = R_{L1} + \Delta R \quad (24)$$

Given the difference in resistor values, an uncorrected DC offset voltage (V_{DM_U}) is generated and may be calculated as follows:

$$V_{DM_U} = V_{CC} - I_{BIAS} R_{L1} - (V_{CC} - I_{BIAS} R_{L2}) = I_{BIAS} \times \Delta R \quad (25)$$

The current (I_{FB}) generated by the dependent current source (which models the DMFL) is defined as:

$$I_{FB} = V_{DM} \times G_m \quad (26)$$

Where, G_m is the transconductance of the ideal DMFL. The feedback current (I_{FB}) will generate a feedback voltage (V_{FB}) given by:

$$V_{FB} = I_{FB} \times (R_{L1} + R_{L2}) = V_{DM} \times G_m (R_{L1} + R_{L2}) \quad (27)$$

Note, the open-loop gain can be defined as:

$$T = G_m \times (R_{L1} + R_{L2}) \quad (28)$$

$$\text{and} \quad V_{FB} = V_{DM} \times T \quad (29)$$

The differential voltage (V_{DM}), by superposition, is the sum of the uncorrected DC voltage (V_{DM_U}) and the feedback voltage (V_{FB}).

$$V_{DM} = V_{DM_U} - V_{FB} \quad (30)$$

Note, the negative sign results from the direction the current source is connected; this represents a negative feedback as it acts to reduce the undesired offset. Now equations (29) and (30) may be used to solve for the ratio of the corrected to uncorrected DC offset differential voltage:

$$\frac{V_{DM}}{V_{DM_U}} = \frac{1}{1+T} \quad (31)$$

and for $T \gg 1$,
$$\frac{V_{DM}}{V_{DM_U}} \approx \frac{1}{T} \quad (32)$$

Therefore, for a given DC offset the corrected differential voltage will be $1/T$ times the uncorrected DC offset. For example, with a loop gain of 100 ($T=100$), the corrected differential DC voltage will be approximately 1% of the uncorrected DC offset voltage.

The frequency response of the DMFL must also be considered. The DMFL will affect all differential signals at the output of the mixer. Therefore, the open-loop gain of the DMFL must be reduced at frequencies containing the down-converted baseband signal. For example, in the IEEE802.11a standard, the center sub-channel with a baseband bandwidth of 156.25 kHz is unused [9]. For this case, the DMFL should have a low-pass filter response with a dominant pole placed well below 156.25 kHz.

The devices utilized to implement the DMFL will add noise to the system. It can be shown that noise generated in the loop is reduced by the loop gain in the same manner as the DC offsets. With the noise modeled by a current source in parallel with the dependent current source (Figure 31) the open-loop differential-noise signal (v_{DM_OLN}) is given as follows:

$$v_{DM_OLN} = i_{DM_N} \times 2R_L \quad (33)$$

The closed-loop noise at the output is then:

$$v_{DM_N} \approx \frac{v_{DM_OLN}}{T} \quad (34)$$

5.4 Conclusion

The challenges in implementing a differential feedback loop for DC offset correction include: 1) the output noise of the circuit must be low enough not to degrade the receiver noise figure significantly, 2) the loop must have sufficient gain at DC to provide adequate DC offset reduction and 3) the loop must have low enough gain where the desired information is (at frequencies above 150 kHz in this case) so the desired signal is not attenuated significantly.

The reduction in gain can be achieved with a low pass frequency response (Figure 32). Two factors affecting the output noise of the loop are the noise sources within the loop and the transfer function from each of these sources to the loop output.

Figure 32 - Feedback Loop Low-Pass Frequency Response

Chapter 6: Circuit Design – Differential Mode Feedback Loop (DMFL) for DC Offset Correction

6.1 *The Initial DMFL*

6.1.1 Introduction

The purpose of the differential-mode feedback loop (DMFL) is to reduce DC offsets due to component mismatch and self-mixing.

6.1.2 Circuit Design

A simplified schematic of the differential-mode feedback loop is shown in Figure 33. The differential output voltage of the mixer is sensed with a high input impedance voltage amplifier, which is implemented with an NFET differential pair (M_{10} and M_{11}). This amplifier is designed to have a low pass frequency response with a cut-off frequency of 80kHz (in the IEEE802.11a standard the center sub-channel with a baseband bandwidth of 156.25kHz is unused [9]). A capacitor of 30 pF (C_{cdm}) and two 50k Ω resistors (R_{in1} and R_{in2}) are used to create this pole. The signal is then applied to a transconductance amplifier, which is implemented with an npn differential pair (Q_{11} and Q_{12}) and the resulting differential current is mirrored with a PFET current mirror ($M6$ and $M7$ in Figure 33, $M3$ and $M4$ in Figure 25). This allows the bias currents of the load resistors (R_L in Figure 25) to be adjusted differentially to adjust the differential output voltage.

Figure 33 - Differential-Mode Feedback Loop – Simplified Schematic

Component values for the differential-mode feedback circuit are listed in Table 14. The bias currents, I_{bias4} and I_{bias5} (Figure 33) are 1mA and 150 μ A, respectively.

Table 14 – DMFL Component Values

Device Type	Reference Designator	Parameters
npn transistor	Q_{11}, Q_{12}	EmitterArea = 5 μ m ²
PFET	M_6, M_7	W/L = 24 μ m/3 μ m
PFET	M_8, M_9	W/L = 49 μ m/3 μ m
PFET	M_{10}, M_{11}	W/L = 49 μ m/3 μ m
capacitor	C_{dm}	30pF
Resistor	R_{in1}, R_{in2}	50k Ω

The DMFB loop has a phase margin of 72° and an open-loop gain of 33.8dB as shown in Figure 34.

Figure 34 - Differential-Mode Feedback Loop - Phase Margin

6.1.3 Results

The DC offset for the fabricated circuit is a result of component mismatch and self-mixing of the LO signal. For simulation purposes, a DC offset is modeled by mismatching the mixer collector resistors (R_L in Figure 25) by 10%. With this model, the simulated open-loop differential DC offset voltage is 31mV (as previously mentioned the expected DC offset may be in the range of millivolts [6]). The closed-loop differential DC offset voltage is 428 μ V. Note, a drawback is the DMFB loop circuitry draws 1.4mA.

6.1.4 Conclusion

Direct-conversion receivers suffer from DC offsets caused by component mismatch and self-mixing due to LO leakage through the substrate, by bondwire coupling and spurious emission. The addition of DC offset correction circuitry has reduced the simulated differential DC offset voltage to less than 1.5% of the uncorrected offset.

There are three problems with this implementation: 1) the output noise of the loop is 190nV/ $\sqrt{\text{Hz}}$ and is excessive compared to the output noise of the DCR without the

differential feedback, which is $71\text{nV}/\sqrt{\text{Hz}}$, degrading the noise figure 2) the loop draws 1.4mA , which is a significant amount of current, and 3) relatively large resistors ($R_{\text{in1}} = R_{\text{in2}} = 50\Omega$) and a large capacitor ($C_{\text{cdm}} = 40\text{pF}$) are required for the low-pass response of the loop, and 4) the loop gain at 150kHz is 29dB , which is far too large and will reduce the desired signal. The differential feedback loop was revised to address these issues.

The FET devices used for the voltage amplifier differential pair generate flicker noise. One way to reduce the output noise of the loop is to use bipolar devices for the differential part of the loop circuit.

To reduce the current consumption an op-amp style topology for the differential feedback loop with active loads was explored. Active loads offer high impedances for large voltage gain that is independent of bias current. For example, the voltage gain of a simple common-emitter amplifier with an active load is given as follows:

$$\frac{v_c}{v_{be}} = gm(r_{o1} \parallel r_{o2}) \quad (35)$$

$$\text{let } r_{o1} = r_{o2} = \frac{V_A}{I_c} \quad (36)$$

$$\text{and } gm = \frac{I_c}{V_T} \quad (37)$$

$$\text{so } \therefore \frac{v_c}{v_{be}} = \frac{I_c}{V_T} \frac{V_A}{2xI_c} = \frac{V_A}{2xV_T} \quad (38)$$

Equation (38) indicates that the voltage gain is independent of bias current using this simple analysis.

The high output impedance of the op-amp style feedback loop also provides a high driving point impedance that can be used to produce a low-frequency pole with the gate capacitance of the PFET's, which are used to steer current from the load resistors.

These improvements were implemented in the next revision of the differential loop discussed in Section 6.2.

6.2 An Improved DMFL for DC Offset Correction

6.2.1 Introduction

This section analyzes an improved differential-mode feedback loop to mitigate the DC offset of a 5GHz direct-conversion receiver. The DC offset correction circuitry reduces the differential DC offset by 83dB. The noise contribution of the feedback circuit is examined. An op-amp style topology is used with active loads and common-mode feedback.

6.2.2 Circuit Design

The loop was implemented in IBM's 0.5 μ m 50GHz BiCMOS technology with analog metal option. There was a choice between using bipolar or MOSFET devices. The bipolar devices have high self-gain but a lower input resistance while MOSFET devices offer high input impedance and low self-gain.

MOSFET devices were chosen to allow voltage sensing with a high input impedance amplifier without using large resistors, which add thermal noise to the circuit. Low self-gain was overcome by using a cascode topology.

A simplified schematic of the DMFL is shown in Figure 35. The output voltage is sensed with high input impedance NFET differential pair (M3 and M4) with a cascode stage (M5, M6). This stage has an active load consisting of cascoded PFETs (M9-M12). The output voltage signal is applied to the gates of PFETs (M1 and M2) to steer current from the load resistors (R_{L1} and R_{L2}), setting the differential output voltage of the mixer. A current mirror sets the bias for this stage (M11-M13). A feedback loop is used to set the common-mode voltage at the drain of the cascode. The common-mode output voltage is sensed with NFETs (M7 and M8) and compared with a reference (V_{ref}) using a PFET differential pair (M17 and M18). The bias current for the NFET differential pair (M3-M6) is adjusted until the common-mode voltage is about equal to V_{ref} .

Figure 35- Differential-mode feedback loop circuit

Component values for the differential-mode feedback circuit are listed in Table 15. The bias currents, I_{bias1} and I_{bias2} (Figure 35) are $5\mu A$ and $1.5\mu A$, respectively.

Table 15 – DMFL Component Values

Device Type	Reference Designator	Parameters
PFET	M ₁ , M ₂	W/L = 1.127mm/3μm
PFET	M ₃ , M ₄	W/L = 1μm/10μm
PFET	M ₅ , M ₆ , M ₉ , M ₁₀ , M ₁₁ , M ₁₂ , M ₁₃ , M ₁₅ , M ₁₆ , M ₁₇ , M ₁₈	W/L = 100μm/5μm
PFET	M ₇ , M ₈ , M ₁₄	W/L = 200μm/5μm
capacitor	C _{dm}	30pF
Resistor	R _{L1} , R _{L2}	1800Ω

6.2.3 Results

The C_{gs} of these PFET's along with the associated driving point impedance introduces a dominant pole in both the common-mode loop and differential mode loop at 200Hz and 10Hz, respectively. The common-mode and differential-mode loops have phase margins of 70° and 90° , respectively and open-loop gains of 85dB and 83dB, respectively.

Simulation results indicate that with a 5% mismatch in the mixer collector resistors the simulated open-loop differential DC offset voltage is 54.9mV. The closed-loop differential DC offset voltage is 3.9 μ V. The simulated reduction in DC offsets is 83dB, which agrees with theory.

As well the simulated differential open-loop noise at the output of the loop is 101.9mV/ $\sqrt{\text{Hz}}$ at 10Hz and the closed-loop noise is 6.7 μ V/ $\sqrt{\text{Hz}}$. The simulated reduction in output noise is 83dB, which agrees with theory. Since the loop has a low-pass filter response the noise is not reduced at 150kHz, which is the lower edge of the first subchannel. The total loop output noise at this frequency is 102.8nV/ $\sqrt{\text{Hz}}$.

6.2.4 Conclusion

Direct-conversion receivers suffer from DC offsets. The addition of DC offset correction circuitry has reduced the simulated differential DC offset voltage by 83dB. Open-loop noise within the bandwidth of the DMFL is reduced 83dB at 10Hz and 6dB at 150kHz, where the loop has 0dB open-loop gain. There are two problems with this implementation: 1) it has 0dB of open-loop gain at 150kHz, and 2) the output noise is too great.

Having 0dB of open-loop gain at 150kHz is a problem because with the loop closed it reduces signals at the output of the mixer by a factor of 2 (Equation (31)). This reduces the voltage conversion gain of the receiver by 6dB and degrades the noise figure.

Therefore, a loop gain of -20dB is more appropriate, which gives a reduction in gain of only 0.8dB .

The output noise of the loop is $102.8\text{nV}/\sqrt{\text{Hz}}$. This is a problem because the output noise of the receiver is only $71\text{nV}/\sqrt{\text{Hz}}$, so it is clear this will further degrade the noise figure significantly.

6.3 The Final Solution - A Low-Noise DMFL for DC Offset Correction

6.3.1 Introduction

The requirements of the feedback loop are: 1) to have adequate loop gain at 0Hz to reduce the DC offset by the desired amount, 2) to have very small loop gain at frequencies above 150kHz, 3) to have low output noise at frequencies above 150kHz, and 4) to be completely integrated.

A solution was found and to explain the topology of this circuit let's first examine a differential two-stage op-amp (Figure 36). A compensating capacitor is used to achieve a dominant pole and a low-pass frequency response with 20dB/decade reduction in gain. The voltage gain of the second stage allows the Miller Effect to be used to generate an effective capacitance at the inter-stage of the amplifier which is approximately equal to the value of the compensation capacitance times the voltage gain of the second stage. This makes it possible to have the compensation capacitor small enough to be on-chip.

Figure 36 – DCR with Final DC Offset Correction Loop Design

For this circuit (Figure 36) the gain of the first stage is 32.5dB at 0Hz and -20dB at 150kHz. The output noise of the first stage is 21nV/ $\sqrt{\text{Hz}}$ at 150kHz. The output noise of the second stage is 500nV/ $\sqrt{\text{Hz}}$ at 150kHz. Recalling that the output noise of the receiver is 71nV/ $\sqrt{\text{Hz}}$, it is clear that using the second stage output as the output of the loop would significantly degrade the noise figure of the receiver.

If the output of the loop is taken at the output of the first stage, the noise from the loop will only be $21\text{nV}\sqrt{\text{Hz}}$ and the loop gain will be 32.5dB . This drastically reduces the output noise of the loop while still allowing the compensation capacitor to be small enough to be integrated on-chip. The output of the second stage is not connected to a load. This implementation is shown in Figure 37.

Figure 37 - Block-Level DCR showing DMFL

6.3.2 Circuit Design

As with the previous circuits, the loop was implemented in IBM's $0.5\mu\text{m}$ 50GHz BiCMOS technology with analog metal option.

The first op-amp (Figure 38) has a resistive voltage divider at the input with a voltage gain of -20dB . The op-amp has a DC gain of 32.5dB , including the voltage divider.

Figure 38 - 1st Stage Op-Amp

Component values for the 1st stage op-amp circuit are listed in Table 20. The bias currents, I_{bias1} and I_{bias2} (Figure 38) are 25 μ A and 50 μ A, respectively.

Table 16 – 1st Stage Op-Amp Component Values

Device Type	Reference Designator	Parameters
npn transistor	Q1, Q2	EmitterArea = 2.5 μ m ²
pnp transistor	Q3, Q4, Q5	EmitterArea = 1.65 μ m ²
PFET	M1, M2	W/L = 200 μ m/5 μ m
PFET	M3, M4, M5, M7,	W/L = 100 μ m/5 μ m
PFET	M6, M8, M9	W/L = 200 μ m/5 μ m
Resistor	R1, R3, R4, R5	50k Ω
Resistor	R2	20k Ω

The second op-amp (Figure 39) has a DC gain of 60dB. It is configured as a Miller Integrator with 1.5pF feedback capacitors (C_{c_dm}). The effective input capacitance is then 0.75nF. The common-mode loop is compensated with 4pF capacitors (C_{c_cm}).

Figure 39 – Miller Multiplier

Component values for the Miller Multiplier circuit are listed in Table 17. The bias currents, I_{bias1} and I_{bias2} (Figure 39) are 25 μ A and 50 μ A, respectively.

Table 17 – Miller Multiplier Component Values

Device Type	Reference Designator	Parameters
pnp transistor	Q ₁ , Q ₂ , Q ₃	EmitterArea = 1.65μm ²
PFET	M ₁ , M ₂	W/L = 200μm/5μm
PFET	M ₄ , M ₅ , M ₆ , M ₇	W/L = 100μm/5μm
PFET	M ₃ , M ₈ , M ₉	W/L = 200μm/5μm
Capacitor	C _{c_dm}	1.5pF
Capacitor	C _{c_cm}	4pF

6.3.3 Results

In summary, the first op-amp senses the differential output voltage of the mixer and sets the gate voltage of two PFET's, which steer current from the load resistors to adjust the differential output voltage. A second op-amp, configured as a Miller integrator, is used to create a large effective capacitance to compensate the loop. This loop, therefore, provides 32.5 dB of differential DC offset reduction. The loop output noise is 21 nV/√Hz and the degradation in receiver noise figure is simulated to be a negligible amount of 0.08 dB. The gain of the second op-amp is 60 dB, which allows a 1.5 pF-integrated capacitor to be used for compensation.

6.3.4 Conclusion

A DCR DC offset correction circuit has been demonstrated, which provides 33 dB of DC offset reduction with negligible degradation to the receiver noise figure. The differential feedback loop is completely integrated.

Chapter 7: Experimental Results

7.1 Introduction

The Direct Conversion Receiver detailed in Chapter 4 was fabricated in IBM's BiCMOS 5AM process. The DC bias voltages and currents as well as conversion gain of the receiver were measured.

7.2 Measurements

Simulated and measured DC bias currents and voltages are listed in Table 18.

Table 18 - Direct Conversion Receiver simulated and Measured Results

Parameter	Simulated	Measured	Comment
I_{bias1}	318 μA	304 μA	LNA voltage level-shift network bias
I_{bias2}	466 μA	438 μA	LNA current-mirror reference current
I_{bias3}	700 μA	661 μA	Mixer current-mirror reference current
I_{bias4}	573 μA	474 μA	Mixer voltage level-shift network bias
I_{LNA}	7.4 mA	6.8 mA	LNA collector current
I_{mixer}	6.8 mA	6.1 mA	Mixer switching quad bias current
I_{buffer}	11.8 mA	10.2 mA	Output buffer current
$V_{\text{o_cm}}$	0.9 V	0.9 V	Mixer common-mode output voltage

The voltage conversion gain of the receiver was measured with the LO offset 100kHz from the RF and is plotted in Figure 40. The RF was swept from 3.9 GHz to 5.4 GHz.

Figure 40 - Direct Conversion Receiver – Voltage Conversion Gain Versus Frequency

The DC offset at the output of one of the mixers was measured to be 13 mV with the LO signal off and 20 mV with the LO signal power set to -10 dBm. Note, this circuit does not have the differential mode feedback loop to reduce this undesired DC offset.

7.3 Conclusion

The measured DC bias currents are similar to the simulated values. The measured common-mode output voltage of the mixer agrees with the simulated value indicating that the common-mode feedback loop is functional.

The simulated conversion gain of the receiver is 31 dB with and RF of 5.25 GHz, which agrees with the measured value of 31 dB.

The DC offset due to process variation was measured to be 13 mV and an additional 7 mV was measured with the LO signal power set to -10 dBm. Note, this circuit does not have the differential mode feedback loop to reduce this undesired DC offset.

The noise figure and linearity of the circuit have not been measured yet.

Chapter 8:Conclusions and Summary

8.1 Conclusion

It has been shown that differential feedback can be used to reduce DC offset in a DCR. Care must be taken when implementing the feedback loop so it does not reduce the desired output signal of the receiver and has low output noise so it does not degrade the receiver noise figure. The use of an integrated differential op-amp configured as a Miller integrator allows a dominant-pole low-frequency response with the use of reasonably sized on-chip capacitors.

A direct-conversion receiver was designed and measured. The measured and simulated DC bias point and conversion gain of the circuit demonstrated reasonable agreement. DC offset due to process variation and LO signal leakage were measured.

Results of this research have been published in two conference papers [26] [27].

This work has also merited the award of a “2004 Outstanding Student Designer Award” from Analog Devices Inc. which had a cash value of \$1500 USD.

A provisional patent was filed by Cognio Canada Inc., which was an industrial collaborator, covering the circuit detailed in reference [27].

8.2 Future Work

Future work includes completing the evaluation of the receiver; noise figure and linearity need to be measured. Future work could also include implementing the differential feedback loop to verify its operation. As well, there are the other design challenges associated with direct-conversion design such as second-order nonlinearity, LO leakage, gain and phase imbalance and 1/f noise. Future work could also include studying various methods of addressing these challenges as listed in Section 2.3.

Appendix A - Mixer Noise Figure Analysis

The purpose of this analysis is to clarify the difference between single-sideband and double-sideband noise figure and verify which of these are reported by Spectre. The approach is to use an ideal mixer model and calculate by hand the noise figure and compare this to simulation.

A.1 - Simulaton of a Mixer Described with AHDL

To begin with, a single-conversion mixer is analyzed using a Cadence description language called Analog Hardware Description Language (AHDL). The Cadence schematic is shown in Figure 41.

Library: ahdlLib

Cell: phase_detector

Figure 41 - Cadence AHDL Mixer Simulation Schematic

A.1.1 RF and LO Signals

The RF (input signal) is assumed to a sinusoid of unit amplitude and with frequency, ω_{rf} . The LO signal is a square wave with amplitude ± 1 and frequency, ω_{lo} , as described mathematically below:

$$RF = 1 \cos(w_{rf} t) \quad (39)$$

LO is a square wave with 50% duty cycle

$$LO = \begin{cases} 1, |t| < T/4 \\ -1, T/4 < |t| < T/2 \end{cases}, \text{ over one period}$$

$$LO = \frac{4}{\pi} \cos(w_{lo} t) - \frac{4}{3\pi} \cos(3w_{lo} t) + \frac{4}{5\pi} \cos(5w_{lo} t) + \dots \quad (40)$$

A.1.2 Mixing Products

The resulting output signal is found from the product of the RF and LO signals:

$$RF \times LO = \frac{1}{2} x \frac{4}{\pi} [\cos((w_{rf} - w_{lo})t) + \cos((w_{rf} + w_{lo})t)] +$$

$$- \frac{1}{2} x \frac{4}{3\pi} [\cos((w_{rf} - 3w_{lo})t) + \cos((w_{rf} + 3w_{lo})t)] +$$

$$\frac{1}{2} x \frac{4}{5\pi} [\cos((w_{rf} - 5w_{lo})t) + \cos((w_{rf} + 5w_{lo})t)] + \dots \quad (41)$$

The calculated signal at the output of the mixer with the RF = 5GHz and the LO frequency = 4GHz consist of the mixing terms which are given in Table 19.

Table 19 - Mixer output signals with $w_{rf} = 5\text{GHz}$ and $w_{lo} = 4\text{GHz}$

Frequency (GHz)	V _{peak} (V)
1	+0.637
9	+0.637
7	-0.212
17	-0.212
15	+0.127
25	+0.127

The simulated output spectrum (Figure 42) agrees with the calculated values (Table 19.).
Note the magnitude of the spectrum is plotted in Figure 42.

Figure 42- Mixer output spectrum with RF = 5GHz and LO = 4GHz

The calculated amplitude of the signals at the output of the mixer with RF= 5GHz and LO frequency = 5GHz are given in Table 20. Note, there are mixing terms at the same frequencies that add vectorally. For instance, the signal at 10GHz has an amplitude of $0.637 - 0.212 = 0.424$ V.

Table 20 - Mixer output signals with $w_{rf} = 5\text{GHz}$ and $w_{lo} = 5\text{GHz}$

Frequency (GHz)	V _{peak} (V)
0	+0.637
10	+0.637
10	-0.212
20	-0.212
20	+0.127
30	+0.127

The simulated output spectrum (Figure 43) agrees with the calculated values (Table 20).

Figure 43 - Mixer Output Spectrum with RF = 5GHz and LO = 5GHz

A.2 - Noise Calculations

A.2.1 Thermal Noise

The thermal noise generated by a 50Ω resistor is given as follows:

$$v_n = \sqrt{4kTR} = 0.895 \text{ nV} / \sqrt{\text{Hz}} \quad (42)$$

$$R = 50\Omega$$

$$T = 290K$$

A.2.2 Input Noise

The noise sources at the input of the mixer are the 50Ω source-resistor and 50Ω mixer input-resistor. The noise at the input of the mixer from these noise sources is given as follows:

$$\begin{aligned}
v_{s_n} & \text{Noise from } 50\Omega \text{ source-resistor.} \\
v_{m_n} & \text{Noise from } 50\Omega \text{ mixer input-resistor.} \\
v_{s_n} = v_{m_n} & \tag{43}
\end{aligned}$$

$$\begin{aligned}
v_{s_in} & \text{Noise at input of mixer due to the } 50\Omega \text{ source resistor.} \\
v_{s_in} = \frac{v_{s_n}}{2} = 447 \text{ pV} / \sqrt{\text{Hz}} & \tag{44}
\end{aligned}$$

$$\begin{aligned}
v_{m_in} & \text{Noise at input of mixer due to the } 50\Omega \text{ mixer input resistor.} \\
v_{m_in} = 447 \text{ pV} / \sqrt{\text{Hz}} & \tag{45}
\end{aligned}$$

A.2.3 Output Noise Resulting from LO fundamental (SSB)

The noise at the output of the mixer resulting from the input noise mixing with the fundamental harmonic of the LO signal is calculated as follows:

$$v_{on1} = \left[\left(v_{s_in} \frac{4}{\pi} \frac{1}{2} \right)^2 + \left(v_{m_in} \frac{4}{\pi} \frac{1}{2} \right)^2 \right] \tag{46}$$

A.2.4 Output Noise Resulting from LO 3rd Harmonic (SSB)

The noise at the output of the mixer resulting from the input noise mixing with the third harmonic of the LO signal is calculated as follows:

$$v_{on3} = \left[\left(v_{s_in} \frac{4}{3\pi} \frac{1}{2} \right)^2 + \left(v_{m_in} \frac{4}{3\pi} \frac{1}{2} \right)^2 \right] \tag{47}$$

A.2.5 Output Noise Resulting from LO 5th Harmonic (SSB)

The noise at the output of the mixer resulting from the input noise mixing with the fifth harmonic of the LO signal is calculated as follows:

$$v_{on5} = \left[\left(v_{s_in} \frac{4}{5\pi} \frac{1}{2} \right)^2 + \left(v_{m_in} \frac{4}{5\pi} \frac{1}{2} \right)^2 \right] \quad (48)$$

A.2.6 Output Noise Contributions

The contributions to the mixer output noise are summarized in Table 21. Note the lower sideband (LSB) noise term results from noise at the frequency of the LO frequency minus the IF mixing with the LO signal. The upper sideband (USB) output noise results from noise at the LO frequency plus the IF mixing with the LO signal.

Table 21 – Mixer Output Noise Contributors

LO Harmonic	Output Noise LSB $\left(\frac{V^2}{\sqrt{Hz}} \right)$	Output Noise USB $\left(\frac{V^2}{\sqrt{Hz}} \right)$	Output Noise from the Source SSB $\left(\frac{V^2}{\sqrt{Hz}} \right)$
1	1.623×10^{-19}	1.623×10^{-19}	8.115×10^{-20}
3	1.803×10^{-20}	1.803×10^{-20}	9.015×10^{-21}
5	6.492×10^{-21}	6.492×10^{-21}	3.246×10^{-21}

A.2.7 Single Sideband Noise Figure

The single sideband noise factor is then calculated in (49) and the single sideband noise figure is given in (50). This agrees with the simulated single sideband noise figure given in (51).

$$F_{ssb} = \frac{n_{o_t}}{n_{o_s}} = \frac{3.7364 \times 10^{-19} \frac{V^2}{\sqrt{Hz}}}{8.115 \times 10^{-20} \frac{V^2}{\sqrt{Hz}}} = 4.604 \quad (49)$$

$$NF_{ssb} = 6.6dB \quad (50)$$

$$NF_{ssb_sim} = 6.6dB \quad (51)$$

A.2.8 Double Sideband Noise Figure

The double sideband noise factor is then calculated in (52) and the double sideband noise figure is given in (53). This agrees with the simulated single sideband noise figure given in (54).

$$F_{dsb} = \frac{n_{o_t}}{n_{o_s} + n_{o_si}} = \frac{3.7364 \times 10^{-19} \text{ V}^2 / \text{Hz}}{2 \times (8.115 \times 10^{-20}) \text{ V}^2 / \sqrt{\text{Hz}}} = 2.30 \quad (52)$$

$$NF_{ssb} = 3.6 \text{ dB} \quad (53)$$

$$NF_{ssb_sim} = 3.6 \text{ dB} \quad (54)$$

A.2.9 Input Referred Noise

The input referred noise is calculated in (55) and this agrees with the simulated input referred noise in (56).

$$IRN = \frac{\sqrt{n_{o_t}}}{CG} = \frac{\sqrt{3.7364 \times 10^{-19}}}{0.636} = 961 \text{ pV} \quad (55)$$

$$IRN_{sim} = 960 \text{ pV} \quad (56)$$

A.3 - Conclusion

The calculated single-sideband and double sideband noise figures for an ideal mixer model are found to agree with values found from simulation. The double sideband noise figure was found to be 3dB lower than the single sideband noise figure.

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