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**LNA AND MIXER DESIGN STUDY
FOR 900 MHz RECEIVER APPLICATIONS**

by
Michel Fréchette, B.Eng

A thesis submitted to
the Faculty of Graduate Studies and Research
in partial fulfilment of
the requirements for the degree of
Master of Engineering

Ottawa-Carleton Institute for Electrical Engineering
Department of Electronics
Faculty of Engineering
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**LNA AND MIXER DESIGN STUDY
FOR 900MHz RECEIVER APPLICATIONS**

submitted by
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in partial fulfilment of the requirements
for the degree of Master of Engineering.

Chair, Department of Electronics

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January 1996

The information used in this thesis comes in part from the research program of Dr. Miles A. Copeland and his associates in the Wireless Communications Group. This research was funded by the Telecommunications Research Institute of Ontario. The research results appearing in this thesis represent an integral part of the ongoing research program. All research results in this thesis including tables, graphs and figures but excluding the narrative portions of the thesis are effectively incorporated into the research program and can be used by Dr. Copeland and his associates for education and research purposes, including publication in the open literature with appropriate credits. Matters of intellectual property may be pursued collaboratively with Carleton University and Dr. Copeland where and as appropriate.

Abstract

The implementation of a radio frequency (RF) front end receiver operating in the 900 MHz band is explored in this thesis. The low noise amplifier (LNA) and mixer are designed using an advanced silicon bipolar process in which monolithic inductors and baluns are to be made available. The designs assumed model parameters which are generic for the next generation of high speed bipolar 0.5 μm technology, with f_T of the order of 25 GHz to 30 GHz.

The emphasis of the LNA design was placed on achieving a minimal power consumption while satisfying the desired performance. A cascode and common-emitter configuration for the LNA are explored. The parameters affecting the performance of the LNA are systematically explored, leading to a final design compromise. The information presented should be sufficient to easily modify the design to achieve a desired performance. An existing mixer, intended for 1.9 GHz operation and implemented in 0.8 μm BiCMOS technology was measured and simulated. The design was modified for 900 MHz operation using the advanced 0.5 μm silicon bipolar process.

At a supply voltage of 1.0 V, the common-emitter LNA has a power dissipation of 4 mW and third-order input intercept of -5.5 dBm, with a 1.27 dB noise figure and 13.9 dB gain. The cascode LNA has an input intercept of -5.6 dBm with a noise figure of 1.43 dB and 14.8 dB gain. At a supply voltage of 1.9V, the power dissipation of the cascode LNA is less than 6 mW. The 0.8 μm double-balanced mixer was measured to provide a conversion gain of 7.9 dB with a third order input intercept of -3.6 dBm and single-sideband (SSB) noise figure of 14.3 dB. Power dissipated is less than 25 mW at a supply voltage of 3V. In the advanced process technology, a double-balanced mixer gave an input intercept of +2.6 dBm with a 9.7 dB single-sideband noise figure and +3.4 dB power conversion gain. Power dissipated by this mixer is less than 18 mW at a supply voltage of 3V.

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List of Symbols and Abbreviations

BJT	bipolar junction transistor
$\beta(f)$	low-frequency transistor current gain
BW	bandwidth
C	capacitance
CE	common-emitter
F	noise factor
FFT	fast fourier transform
F_{min}	minimum noise figure for an intrinsic device
f_T	gain-bandwidth frequency
GaAs	Gallium Arsenide
g_m	transistor transconductance
G_p	power gain
IC	integrated circuit
IEEE	Institute of Electrical and Electronics Engineers
IF	intermediate frequency
IMPATT	impact avalanche transit time
IP_3	third-order intercept
JFET	junction field-effect transistor
L	inductor
LNA	low-noise amplifier
LO	local oscillator
MESFET	metal semiconductor field effect transistor
MOSFET	metal oxide semiconductor field-effect transistor
NF	noise figure

P_{1dB}	1 dB compression point
P_D	intermodulation distortion power
P_I	intercept point
Q	quality factor
R	resistor
r_b	base spreading resistance
RF	radio frequency
R_n	noise resistance
R_{OPT}	optimal source resistance
SAW	surface-acoustic wave
U	unilateral gain
Vpp	voltage peak-to-peak
X_{OPT}	optimal source reactance

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Chapter 1

Introduction

The wireless revolution of the 90's and its explosive growth in the cellular and cordless phone markets has driven the industry to market higher levels of integration with new RF integrated circuits (RFICs). These products, being consumer driven, dictate that the end-products be efficient and manufactured at low-cost. The ultimate goal of a single 'radio chip' for digital personal communications radio transceivers operating in the ~ 1 GHz band that meets industry standards is a challenging task.

The objective of this thesis is to investigate the opportunity provided by new processing technology to advance the performance of RFICs while making use of on-chip inductors. Inductors can enhance the stability of a device by emitter degeneration, while contributing a reduced amount of noise as compared to resistive feedback. They also allow operation of the device at very low d.c. supply voltages, which is a crucial factor for hand-held personal communication systems.

The viability of the bipolar transistor for this application stems from its high cutoff frequency as well as the relative maturity of its processing and manufacturing technology. Performance is not only determined by basic device characteristics or material properties, such as mobility (often a key argument for GaAs). Performance is strongly influenced by the understanding of device physics and design, the reliability of the process to fabricate the desired structures and the ability to interconnect the component to the rest of the circuit.

In these aspects, the BJT, in appropriate applications, will usually win over other microwave devices such as silicon metal-oxide semiconductor field-effect transistors (Silicon MOSFETs), junction field-effect transistors (JFETs), impact avalanche and transit time diodes (IMPATT diodes), and gallium arsenide-metal semiconductor field-effect transistors (GaAs MESFETs).

It is also essential to pay attention to the RF circuit or IC/package interface in order to fully exploit the technology at hand. RF integration is presently limited to packages with about 20 leads due to the ground leads and the increased parasitics associated with wirebonds and lead lengths [1]. This limits the amount of functions which can be integrated on a single IC.

In typical previous RF designs every module was specified with $50\ \Omega$ at every port. However, the IC designer is not limited by this constraint except at chip interfaces which must drive $50\ \Omega$. Faced with power consumption limitation, he can easily increase the load to achieve the required gain. As an example, there is normally some filtering action taking place between the LNA and the mixer to provide image rejection. This filter can be made to present input and output impedances which will optimize the overall RF front end.

A parallel resonant tank at the output can also be used to filter out unwanted harmonics but the benefit is, at present, quite limited due to the relative low Q of on-chip inductors. However they can still increase somewhat the overall linearity of the circuit. The parallel resonant tank also allows for easy matching to any real load less than or equal to the equivalent parallel resistance of the tank, without a need for an external output matching network.

1.1 Thesis Outline

This thesis is organized into six chapters. The parameters affecting the performance of an RF front-end, as well as the performance objectives for which the LNA and mixer are designed, are introduced in Chapter 2.

For a monolithic implementation, inductors that are compatible with a production integrated circuit process have been provided and designed by Mr. José Macedo from Carleton University.

A high performance npn bipolar process featuring a double polysilicon bipolar transistor with a 0.5 μm wide emitter is the process technology assumed in implementing the LNAs studied in this thesis. We have coined the high performance npn bipolar process with the acronym AP30 (Advanced process with 30 GHz speed) in later discussion. These devices are to provide a higher gain-bandwidth frequency (f_T) and lower base resistance than has been available previously in silicon. The expected performance characteristic of this transistor is discussed in Chapter 3.

Two LNA architectures, the common-emitter and cascode configurations, are explored in Chapter 4. The inherent compromises that must be made in the design are discussed and the simulated and theoretical results presented.

A double-balanced mixer previously designed in a 0.8 μm bipolar process by Mr. José Macedo for the 1900 MHz band, and implemented single-ended with an output buffer to 50 Ω matching, is analysed in Chapter 5. The mixer is then optimized in AP30 to provide a better overall performance at 900 MHz. The results of the mixer are presented and the various parameters affecting performance are discussed.

Layout and experimental measurements for the LNAs and optimized mixer were beyond the timeframe of this study and only Hspice (trademark of Meta-Software, Inc.) and Libra (trademark of HP/EEsof Software Inc.) simulations will be presented. However, the measured performance of the single-ended mixer provided by Mr. José Macedo will be presented to demonstrate the validity of the simulations.

The designs presented show that through access to an improved silicon bipolar technology and a good understanding of the parameters involved, one can achieve a design which will likely meet the specifications of next-generation portable radios. Finally, some concluding remarks and recommendations for further research are presented in Chapter 6.

1.2 Thesis Contributions

Many authors [3,6,27,39] have reported LNA/mixer designs having low power consumption, however the actual design methodologies have not been presented in detail. The main contributions of this thesis are:

- A systems IC design approach involving the trade-offs between noise, gain, isolation, and dc power consumption.
- Demonstration of the improvement in performance expected from an advanced silicon bipolar process having 25 GHz f_T and monolithic inductors.
- Comparison and validation of the simulation results from a time-domain simulator (Hspice, trademark of Meta-Software Inc.) and a harmonic-balance simulator (Libra, trademark of HP/EEsof Software Inc.) as well as certain analytic results.

Chapter 2

System Analysis

2.1 Introduction

Radio receiver designs are dependent upon channel impairments and the parameters specified for a particular application. The LNA is used as an initial stage to boost the power of the received signal while minimizing the addition of noise and distortion. The RF signal is then down-converted to the desired intermediate frequency (IF).

Frequency translation can be accomplished using active or passive mixers. For discrete versions the passive diode mixer is the preferred choice. However, most silicon RFIC mixer implementations use the bipolar Gilbert cell because of the inherent conversion gain, isolation and harmonic suppression and because it can be integrated more easily.

In this work the LNA and mixer are intended for a generic application where a gain of 15 dB with a noise figure of less than 1.5 dB could be required for the LNA. No specifications were given for the mixer. However, a commercially available 1GHz LNA and mixer (NE/SA600 from Philips Semiconductors RF Communications Products Data Handbook 1992), specified as a high-performance low-power communication IC for the 900 MHz band, will be used as a guideline. The combined 1 GHz LNA and mixer $IP3$ from Philips is specified as -13 dBm. Therefore if we assume that the input signal will not be greater than the P_{1dB} then we can expect a maximum signal strength of -23 dBm.

There are two main factors that affect receiver performance. These are how much noise is added by the receiver and the level of distortion caused by the receiver non-linearities. A simplified block diagram of an RF front-end IC is shown in Figure 2.1. A bandpass filter is used between the antenna and the front-end receiver while an image-reject filter is used between the LNA and the mixer. The external filter at the output of the mixer is usually a surface-acoustic wave (SAW) filter or a ceramic filter component at the intermediate frequency (IF).

Figure 2.1: Block diagram of a typical front-end receiver.

2.2 Noise Factor, Noise Figure

The noise factor has become a standard figure of merit for the amount of noise added by a system.

The IEEE definition for noise factor (F) can be stated as [36]

$$F = \frac{\text{available output noise power}}{\text{available output noise due to the source}} \quad (2.1)$$

The noise factor is often expressed in decibels and is then referred as noise figure (NF) where

$$NF = 10 \log_{10} F \quad (2.2)$$

For a cascade of N networks, the noise factor can be expressed as,

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \dots + \frac{F_n - 1}{G_1 G_2 \dots G_{n-1}} \quad (2.3)$$

where F_i , G_i are the noise factor and gain, respectively, of the i th network, $i=1, \dots, N$.

Equation (2.3) states that if the power gain of the first stage is large, the overall noise factor will be essentially that of the first stage. In practice, the LNA is normally designed with a gain of at least 10 dB to ensure that added noise from succeeding stages is minimized.

2.3 Intermodulation Distortion

All receivers contain some nonlinearities. These nonlinearities can cause a change in the frequencies of the input signal and/or a change in the network gain. The network nonlinearities can be described by the expansion

$$y(x) = k_1 f(x) + k_2 [f(x)]^2 + k_3 [f(x)]^3 + \text{higher order terms} \quad (2.4)$$

where $f(x)$ is the input signal, $y(x)$ is the output signal, k_1 is the linear transfer coefficient, and k_i , $i = 2, \dots, N$, are the nonlinear coefficients. Consider a two-tone input signal $f(x)$ where ω_1 and ω_2 are incommensurate frequencies.

$$f(x) = A_1 \cos \omega_1 t + A_2 \cos \omega_2 t \quad (2.5)$$

If ω_1 and ω_2 are sufficiently close together, k_i can be considered the same for both signals. For simplicity, we assume all the k_i 's to be real.

Then the network's response to input $f(x)$ results in the following:

$$\begin{aligned}
 y &= k_1(A_1 \cos \omega_1 t + A_2 \cos \omega_2 t) + k_2(A_1 \cos \omega_1 t + A_2 \cos \omega_2 t)^2 \\
 &+ k_3(A_1 \cos \omega_1 t + A_2 \cos \omega_2 t)^3 \\
 &= k_1(A_1 \cos \omega_1 t + A_2 \cos \omega_2 t) + k_2[A_1^2 \frac{1 + \cos 2\omega_1 t}{2} + A_2^2 \frac{1 + \cos 2\omega_2 t}{2} \\
 &+ A_1 A_2 \{ \cos(\omega_1 + \omega_2)t + \cos(\omega_1 - \omega_2)t \}] + k_3 \{ A_1^3 (\frac{3 \cos \omega_1 t}{4} + \frac{\cos 3\omega_1 t}{4}) \\
 &+ A_2^3 (\frac{3 \cos \omega_2 t}{4} + \frac{\cos 3\omega_2 t}{4}) + A_1^2 A_2 (\frac{3 \cos \omega_2 t}{2} + \frac{3 \cos(2\omega_1 + \omega_2)t}{4} + \frac{3 \cos(2\omega_1 - \omega_2)t}{4}) \\
 &+ A_1 A_2^2 (\frac{3 \cos \omega_1 t}{2} + \frac{3 \cos(2\omega_2 + \omega_1)t}{4} + \frac{3 \cos(2\omega_2 - \omega_1)t}{4}) \} \quad (2.6)
 \end{aligned}$$

One effect of the nonlinearity that can be deduced from (2.6) is that the amplitude of the signal at ω_1 has become

$$A'_1 = k_1 A_1 + k_3 \left(\frac{3}{4} A_1^3 + \frac{3}{2} A_1 A_2^2 \right) \quad (2.7)$$

k_3 will normally be negative and therefore reduces the signal at ω_1 . As a consequence, if a large signal A_2 at ω_2 is present, it could effectively mask a smaller signal at ω_1 due to the $3/2(A_1 A_2^2)$ term. To avoid the "gain compression", the third-order coefficient k_3 must be reduced.

If we refer to Figure 2.2, we can see that the terms in (2.7) cause the power gain to deviate from its idealized curve. The point at which the power gain is down 1 dB from the ideal curve is referred to as the 1 dB compression point (P_{1dB}). The receiver must operate several dB below this level if it is to avoid the non-linear region of operation.

Another important effect of receiver nonlinearity is the intermodulation distortion caused by the cubic term in (2.4). This term generates the intermodulation products $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ as seen in (2.6). If ω_1 and ω_2 are close enough together, they can actually fall within the passband of the system and appear at the output as signal distortion. The third-order intermodulation distortion power (referred to 1 Ω) can be defined as,

$$P_D = \frac{\left(\frac{3}{4} \cdot k_3 \cdot A_1^2 \cdot A_2\right)^2}{2} \quad (2.8)$$

If the two-tone input amplitudes are equal, then (2.8) states that the intermodulation distortion power grows as the cube of the input power, i.e for every 1-dB change in input power there is a 3-dB change in the power of the intermodulation terms. Figure 2.2 demonstrates the effect of the intermodulation distortion power on the network.

Figure 2.2: Output power vs. input power response for a non-linear device.

The point at which the intermodulation distortion power is equal to the output power contributed by the linear term $(k_1 A_1)^2/2$ is referred to as the *intercept point* P_I . This measure is further referred to as $IP3$ where it implies the intermodulation products due to the cubic term. It can either be referred to in term of input power, $IP3_i$, (dotted line crossing x-axis in Fig. 2.2) or in term of output power, $IP3_o$, (dotted line crossing y-axis in Fig. 2.2).

Chapter 3

Technology

A 0.5 μm self-aligning double-poly bipolar technology is assumed for the LNA and the mixer circuits. The cross-section of a typical double-poly bipolar junction transistor (BJT) is shown in Figure 3.1 [38]. Bipolar devices were chosen for the front-end because of their superior transconductance when compared to MOS devices. The generic features of a double-poly bipolar technology structure are:

- i) deep trench isolation to minimize collector-substrate capacitance
- ii) polysilicon base contact to minimize collector-base capacitance C_C
- iii) an emitter self-aligned to the extrinsic base to minimize base resistance r_b

There are two figures of merit that are commonly used to describe the performance of a BJT. These are the gain-bandwidth frequency (f_T), which is the frequency where the short-circuit gain $|h_{fe}(\omega)|$ approximates unity, and the maximum frequency of oscillation (f_{max}) which is the frequency where the maximum available power gain of the transistor is equal to 1. The npn bipolar devices used in this thesis have an expected maximum f_T of 25 GHz and f_{max} of 30 GHz. The model parameter file assumed for the AP30 npn transistors is given in Appendix A.

Figure 3.1 Cross-section of a generic bipolar transistor utilizing two levels of polysilicon. P⁺ polysilicon is used to contact the base region and N⁺ polysilicon serves as the source for the self-aligned polysilicon emitter.

The noise figure for a common-emitter amplifier can be given by [24]

$$\text{Noise Figure} \propto g_m \cdot r_b \left(\frac{f}{f_T} \right)^2 \quad (3.1)$$

The noise figure of a transistor can be optimized by reducing the base resistance while increasing f_T . The base resistance is a physical property of the device where increasing the device size by adding emitter fingers will reduce the base resistance but increase the capacitance and consequently decrease the f_T . The circuit shown in Figure 3.2 is used to define the possible trade-off between the gain and noise power of the largest device available in AP30. The Hspice circuit configuration file is shown in Appendix B. The AP30_80 has an assumed emitter size of 80 μm x 0.5 μm .

One of the primary goals of the LNA design is to achieve low power consumption. For this reason, the power gain and noise figure dependence on bias current is to be investigated.

Figure 3.2: The common-emitter circuit configuration used to simulate the noise power of AP30_80. The transistor is operated at a collector supply voltage of 1.0V. The input ac signal is set at a frequency of 915 MHz while the VBB is swept to give a collector bias current from 1 to 10mA.

Figure 3.3 illustrates the relation of bias current to the noise power of the BJT configured as in Figure 3.2. The main sources of noise in a BJT are: 1) the thermal noise in the resistive elements which are the base, emitter and collector resistors (r_b , r_e and r_c), 2) the shot noise in the collector current (i_c) and base current (i_b), which is related to discrete electron emissions across a barrier; and 3) the 1/F noise, often referred to as flicker noise, which is related to charge or mobility fluctuations.

It can be seen from Figure 3.3 that the base resistance is a significant component contributing to the output noise power while the collector shot noise is limited beyond a current of 5mA. The base resistance depends on device structure and is inversely proportional to device size. Figure 3.4 demonstrates the effect of transistor size on the total output noise power.

Figure 3.3: Relative component contribution to the noise power for the BJT AP30_80 as configured in Figure 3.2. The output flicker noise due to base current and the output thermal noise due to collector resistor (r_c) were found to be negligible.

There is marginal decrease in output noise power as the base resistance becomes less dominant for a device size with an area greater than $160 \times 0.5 \mu m$. The device is modeled on the Spice Gummel-Poon model, which does not take into account the high current density effect which results in an optimistic performance at high currents. However, the low-noise amplifier developed in this thesis will be operated in class A and therefore accurate performance is expected.

Figure 3.4: Total relative output noise power for a ($n \times \text{AP30_80}$) transistor size, where $n = 1, 2$ and 3 . The test circuit is as shown in Figure 3.2 where transistors are connected in parallel to provide the required sizes.

There are several definitions of power gain in use for transistor amplifiers. Unilateral gain U is obtained when a device is made unilateral by adjustment of a lossless reciprocal feedback network, and then matched at both ports. $U(f)$ has the general form[28]

$$U(f) = \frac{U_o}{\sqrt{1 + U_o \left(\frac{f}{f_{max}} \right)^4}} \quad (3.2)$$

At 915 MHz (f/f_{max})⁴ $\ll 1$ and $U(f)$ is approximately U_o . At low frequencies the current gain of the device provides a better indication of circuit performance.

The high-frequency current gain of the transistor is given by the following expression,

$$\beta(f) = \frac{\beta_o}{\sqrt{1 + \left(\frac{j\omega\beta_o}{\omega_T}\right)^2}} \equiv \frac{\omega_T}{j\omega} \quad (3.3)$$

with the approximation valid for $j\omega\beta_o/\omega_T \gg 1$.

As can be seen from Figure 3.5, for a device that is too large, the small feedback base-collector capacitance known as the Miller effect, tends to effectively reduce the maximum achievable gain.

Figure 3.5: AC beta for a ($n \times \text{AP30_80}$) transistor size, where $n = 1, 2$ and 3 . The test circuit is as shown in Figure 3.2 where transistors are connected in parallel to provide the required sizes. The ac beta is determined using (3.3) and the f_T is obtained from the simulation at 915 MHz.

Chapter 4

LNA Design

4.1 Common Emitter Low-Noise Amplifier

The objective of the LNA design is to achieve a noise figure below 1.5 dB while maintaining a gain greater than 10 dB.

Figure 4.1: Topology of the common-emitter LNA with input matching network and reactive elements modelled with losses. A resonant RLC network is used at the output to resonate the transistor's parasitics while inductive feedback is used at the emitter.

The common-emitter low-noise amplifier (LNA) topology shown in Figure 4.1 is used in order to provide the required gain while minimizing the noise figure [23]. Desirable characteristics for the LNA are large power gain, low noise figure, a wide dynamic range linear transfer function, dynamic stability, reverse isolation, and frequency selectivity. The operating characteristics for the LNA are a compromise between these options.

4.1.1 Introduction

The supply current is very important in portable applications in order to minimize power consumption. From Figures 3.4 and 3.5 a transistor area of $160 \times 0.5 \mu\text{m}$ is selected with a supply current of 4 mA. The use of an LC resonant network at the collector output allows the transistor to operate in the forward-active mode for supply voltages as low as 0.9 Volts. At a supply voltage of 1.0 volt the power consumption is still relatively low at 4mW. The current selection will also affect the level of linearity of the circuit. This will be dealt with in section 4.1.2, non-linear analysis.

Any resistive elements placed at the input of the transistor or at its emitter will greatly affect the noise figure of the LNA. The inductor at the emitter is used to improve the noise match of the BJT as well as providing negative feedback which is traditionally accomplished using resistors (R). The inductive emitter degeneration, L_E , shown in Figure 4.1, helps stabilize the amplifier with respect to variations in active device parameters. It also minimizes the noise that would otherwise be generated by an equivalent purely resistive element. Due to quality-factor (Q) limitations of less than ten, for on-chip inductors, there will still be some lossy component associated with the inductor, however.

A trade-off is then necessary between the amount of feedback required for stability and that for low noise figure. Another advantage of an inductive element at the emitter is that it also facilitates the matching requirement to $50\ \Omega$ at the input. This is due to the so called gyration from inductance to resistance caused by the ac beta ($\beta(f)$) of the transistor (see (3.3)).

The amount of gyration is given by [6],

$$R_{gyrated} = \beta(f) \cdot j\omega L_E = \omega_T \cdot L_E \quad (4.1)$$

It is possible to select L_E such that it becomes gyrated exactly to $50\ \Omega$. However, this may yield in a gain reduction which is deemed unreasonable. On the other hand, if we choose L_E too small, then little feedback will be present and consequently a larger matching inductor will result, further degrading the noise figure. An inductor value of 1 nH was selected for this common-emitter LNA design, which minimized the noise figure while providing the necessary gain.

4.1.2 Stability

The stability of a two-port device is normally expressed through the K-factor [20].

Mathematically, unconditional stability exists when:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2 \cdot |S_{12} \cdot S_{21}|} > 1 \quad (4.2)$$

and

$$B = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 > 0 \quad (4.3)$$

where the elements of the scattering matrix are S_{11} , S_{12} , S_{21} , S_{22} and the determinant of the S-matrix is,

$$|\Delta| = |S_{11}S_{22} - S_{21}S_{12}| \quad (4.4)$$

If the two-port satisfies both requirements, it is defined to be unconditionally stable. Otherwise, it could be potentially unstable. A newer criteria, the μ -factor [21], combines the above two requirements into one more practical form where relative stability of devices can be compared.

Figure 4.2: Relative stability factor (μ) for the AP30_80 transistor, with an area of $160 \times 0.5 \mu\text{m}$, configured in the common-emitter configuration, (a) with the emitter grounded, (b) with inductive emitter degeneration added, and (c) with a *RLC* resonant network at the output and matching network at the input to provide input and output 50Ω match.

The μ -factor, which must be greater than one for unconditional stability, is expressed as,

$$\mu = \frac{1 - |S_{22}|^2}{|S_{11} - \Delta(S_{22}^*)| + |S_{21}S_{12}|} > 1 \quad (4.5)$$

The larger the μ -factor, the greater is the device's stability. Figure 4.2 shows the stability of the transistor with and without the inductor, for a current bias of 4mA. The inductor L_E provides a definite improvement in stability. However, the two-port network is still only conditionally stable. That means that there are certain input/output load conditions which could lead the circuit to oscillate. Since the scattering parameter S_{12} can not be ignored, the procedure used is to resonate the output to present $50\ \Omega$ to the following stage and then conjugate match the input for maximum power transfer.

For the 900 MHz application it is important that the LNA be stable down to 100 MHz because this is where the commercial FM band resides. These signals can easily have signal strength much greater than the signal of interest and could cause the LNA to oscillate even with a bandpass filter between the antenna and the amplifier. Figure 4.2 shows the relative stability factor μ for the common-emitter LNA. The K and B factor of stability are shown in Figure 4.3 where the LNA, under matched conditions, can be observed to be stable from 0.1 to 3 GHz.

Figure 4.3: K, left axis, and B, right axis, stability factors for the common-emitter LNA shown in Figure 4.1. The conditions for stability are $K > 1$ and $B > 0$.

4.1.3 Matching Networks

Libra (trademark of HP/EEsof Software Inc.) was used to simulate the output impedance of the transistor with inductive emitter degeneration to initially resonate the output capacitive parasitics at the collector output. The schematic and test bench files are shown in Appendix C. An inductor of 5 nH with a Q of 5 is selected at the collector output. The series resistance of the inductor is given by,

$$r_s = \frac{\omega L}{Q} \quad (4.6)$$

The series resistance of an inductor can be transformed to its parallel equivalent using the following,

$$R_p = r_s (Q^2 + 1) \quad (4.7)$$

This should provide an adequate output matching range with a maximum available output resistive load of 150 Ω . A load capacitance of 4.8 pF was initially required to resonate the parasitics of the transistor. However, after matching the input of the LNA some fine tuning was necessary and a final load capacitance of 3 pF completes the output LC resonant circuit. On-chip capacitance used in the designs are assumed to have a Q of 20. The capacitance of 3 pF has therefore a series resistance of 2.6 Ω . The input of the BJT transistor always has a capacitive reactance which is easily resonated with an inductor.

A bias current of 4mA gives a good compromise between the noise figure and input reactance since ω_T is related to the bias current as,

$$\omega_T \approx \frac{I_C / V_{TH}}{C_\pi} \quad (4.8)$$

where V_{TH} is the thermal voltage (26mV at room temperature) and C_π is the base-emitter capacitance. From (4.8), one can realize that proper biasing level and transistor size also affects the amount of gyration applied. Hence, a compromise must again be reached between the amount of feedback, noise figure, linearity and matching requirements of the LNA.

In order to obtain a good noise figure the matching inductor must be made reasonably small in order to keep the associated lossy component to a minimum as it directly adds to the noise figure. It is thus beneficial to reduce the input reactance as well as the base resistance. Due to Q limitations for on-chip inductors, a 16 nH inductor at 915 MHz with a maximum Q of 10, exhibits an associated series resistance of

$$r_s = \frac{X_L}{Q} = \frac{2\pi f L}{Q} = 9.2 \Omega \quad (4.9)$$

Off-chip inductors with Q s of 50 are available yielding a series resistance of about 1.8 Ω . The use of an off-chip inductor leads to a 0.64 dB noise improvement, when simulated with Libra, when compared to the use of an on-chip inductor.

Using (4.1) it is determined that a 1 nH inductor will gyrate into a 95 Ω resistor. This is the required value to approximately match the input to 50 Ω as the Miller effect tends to reduce the effective input impedance. The Miller effect on the input impedance can be seen by analysing the small-signal Π -model shown in Figure 4.4.

Figure 4.4: Simplified small-signal Π -model used to determine the input impedance of the common-emitter LNA.

The lossy component of L_E is assumed negligible. Z_L represents the RLC output resonant network while R_L is the output load resistance. The input impedance can be determined by applying a test current i_T at the input of the Π -model as shown in Figure 4.4 and subsequently solving for v_T/i_T , where v_T is the test voltage. The test current is given as,

$$i_T = i_1 + i_2 \quad (4.10)$$

where

$$i_1 = V_\pi j\omega C_\pi \text{ and} \quad (4.11)$$

$$i_2 = \frac{v_\pi \left[(1 - \omega^2 L_E C_\pi + g_m Z_{equ}) + j\omega L_E g_m \right] j\omega C_\mu}{1 + j\omega C_\mu Z_{equ}} \quad (4.12.a)$$

We can assume that the emitter and collector currents are much larger than the base current and consequently (4.12.a) can be reduced to,

$$i_2 = \{ [V_\pi + (g_m V_\pi j\omega L_E)] + g_m V_\pi Z_{equ} \} j\omega C_\mu \quad (4.12.b)$$

where Z_{equ} is given as:

$$Z_{equ} = \left[\frac{1}{Z_L} + \frac{1}{R_L} \right]^{-1} = \left[\frac{1}{j\omega L_C} + j\omega C_L + \frac{1}{R_p} + \frac{1}{R_C} + \frac{1}{R_L} \right]^{-1} \quad (4.13)$$

with R_p being the equivalent parallel resistance of the inductor as given by equation (4.7).

At 915 MHz, substitution of data, given in Appendix D, into equation (4.13) yields

$$Z_{equ} = 18 + j 14.42;$$

The voltage across C_π is given by,

$$V_\pi = \frac{v_T}{1 + j\omega g_m L_E} \quad (4.14)$$

Solving for the ratio v_T/i_T , after substitution of (4.14) into (4.11) and (4.12), yields the following for Z_{in} ,

$$Z_{in} = \left[\frac{j\omega C_{\pi}}{1 + j\omega g_m L_E} + j\omega C_{\mu} \left(\frac{1 + Z_{equ}}{r_e + j\omega L_E} \right) \right]^{-1} + r_{bb} \quad (4.15)$$

The second term in (4.15) represents the Miller effect of C_{μ} on the input impedance. Substitution of Hspice simulated data given in Appendix C.5 yields, at 915 MHz, an input impedance of

$$Z_{in} = (50.2 - j83.6) \Omega.$$

From Figure 4.5, the calculated input impedance is seen to be in fair agreement with the Hspice (trademark of Meta-Software Inc.) simulated result. The Hspice configuration file is given in Appendix C.4.

Figure 4.5: Hspice simulated input impedance of the common-emitter LNA shown in Figure 4.1 over 30 MHz, prior to the input matching network. (a) The real part of the input impedance and (b) The imaginary part of the input impedance.

The input impedance of the LNA can be matched to 50Ω by selecting a *series L-shunt C* matching network as shown in Figure 4.6 where the normalized input impedance is indicated by point A.

□ Common_Emitter_Linear_tb
S1J2
Common-
S[1,1]

Frequency 915.0 to 915.0 MHz

Figure 4.6: Design of the *series L-shunt C* input matching network, for the common-emitter LNA shown in Figure 4.1, using a Smith chart. Point A represents the normalized input impedance of the LNA while point C represents the 50 Ω impedance of the antenna.

The transformation from point A [i.e. $z_{in} = (42.7 - j77.2)/50 = 0.85 - j1.5$] to point B is along a constant-resistance circle, and we obtain for the matching inductor impedance $z_L = j1.5 + j0.35 = j1.85$. Observe that point B is along a unit constant-conductance circle. The admittance at point B is $y_B = 1 - j0.4$.

The transformation from point B to point C (i.e., the origin) is along a constant-conductance circle, and we obtain the capacitor admittance $y_C = 0 - (-j0.4) = j0.4$ (or $z_C = 1/j0.4 = -j2.5$). Therefore at point C, $y_{in} = z_{in} = 1$ (or $Z_{in} = 50 \Omega$) and the LNA is matched to the 50 Ω generator. The matching network can be seen in Appendix D, Figure D.1.

At 915 MHz, the value of L is

$$L_{mi} = \frac{1.85 \cdot 50}{2\pi(915 \times 10^6)} = 16 \text{ nH} \quad (4.16)$$

and the value of C is

$$C_{mi} = \frac{1}{3.1 \cdot 50 (2\pi) 915 \times 10^6} = 1.4 \text{ pF} \quad (4.17)$$

Slight adjustment of C_{mi} to 1.1 pF, in the input matching network, is required since the inductor has some associated loss. The input matching network can be seen to provide narrowband matching to 50 Ω , in Figure 4.7, at the centre frequency of 915 MHz. The narrowband matching is caused by the off-chip matching input inductor which has a relatively high- Q . The Hspice configuration file is shown in Appendix F.2.

Figure 4.7: Common-emitter LNA (Figure 4.1) real and imaginary input impedance under 50 Ω matched condition.

Moving now to the output of the LNA, the resonant RLC network at the collector output of the BJT effectively matches the output to any resistive load simulated to be less than or equal to 85 Ω , the equivalent parallel resistance of the tank.

This value is less than the $150\ \Omega$ previously mentioned which was determined from the Q of the LC resonant network only. However, the effective Q at the output will be less due to the bandlimiting effects of the device parasitic capacitances at the collector.

A shunt resistor of $140\ \Omega$ for the resonant network was used to provide a $50\ \Omega$ match at the output. This greatly simplifies on-chip integration to a following stage. The output RLC resonant network is designed with on-chip inductor with a low- Q which will provide a relatively wideband matching to $50\ \Omega$ at the output. This can be seen from Figure 4.8.

Another amplifier parameter of importance is the voltage standing wave ratio (VSWR). The VSWR represents the impedance mismatch (both input and output) of the amplifier to the system. A VSWR of 1.0:1 represents a perfect match. Hspice does not provide VSWRs per se but they can be easily determined from the magnitude of the scattering parameters S_{11} and S_{22} ,

$$VSWR_i = \frac{1 + |S_{ii}|}{1 - |S_{ii}|} \quad (4.18)$$

The resulting VSWRs are shown in Figure 4.9. At ~ 15 MHz, Figure 4.9 shows that maximum power transfer takes place between the antenna and the LNA and between the LNA and the mixer. Under real conditions one would be required to do a layout of the circuit from which parasitics are extracted and compensated for in the design. Also, off-the-shelf components come in standard sizes and perfect matching in a production environment is rarely achieved.

Figure 4.8: Common-emitter LNA, shown in Figure 4.1, real and imaginary output impedance under $50\ \Omega$ matched condition.

Figure 4.9: Common-emitter LNA, shown in Figure 4.1, input and output VSWR under matched condition. The VSWRs are determined from equation (4.18).

This is equivalent to an input return loss of less than -20 dB over the band, where the input return loss is given as:

$$\text{Input Return Loss} = 20\log|S_{11}| \quad (4.19)$$

The output return loss is in terms of S_{22} .

4.1.4 Noise Analysis

The noise figure specifies how the amplifier degrades the signal to noise ratio. The contributions to noise factor by the low-noise amplifier can be approximated by using the following formula [16]

$$F = 1 + \frac{1}{R_s} \times \left[r_{bb}' + \frac{r_e'}{2} + \frac{(r_{bb}' + R_s)^2}{2 \times \beta \times r_e'} + \frac{(r_{bb}' + R_s)^2}{2 \times r_e'} \times \left(\frac{f}{f_T} \right)^2 \right] \quad (4.20)$$

where

$$r_b' = r_b + r_{LMI} \text{ and}$$

$$r_e' = r_e + r_{LE}$$

Substitution of data, given in Appendix F, gives

$$F = 1.357 \text{ or equivalently NF} = 1.33 \text{ dB}$$

Libra predicts a noise figure of 1.27 dB at 915 MHz. Figure 4.10 shows the simulated 50 Ω noise figure as a function of frequency. The Libra schematic and test bench files are shown in Appendix E.

The largest contribution from the transistor is the output shot noise due to base current, as can be seen from Figure 4.11. The Hspice configuration file and resulting data file are shown in Appendix F. It can also be seen that the series resistance from the input matching inductor and the base resistance adds a significant amount of noise, totalling $6.0 \times 10^{-19} \text{ V}^2/\text{Hz}$. This is equivalent to 7.6% of the overall output noise. The Hspice model for noise calculation is shown in Appendix F.6.

Figure 4.10: Common-emitter LNA 50 Ω noise figure.

Figure 4.11: Hspice noise allocation for the common-emitter LNA shown in Figure 4.1, all noises are output referred.

The Hspice noise figure can be determined from

$$NF = 10 \log \left(\frac{\text{total output noise power}}{\text{output noise power due to the source resistance}} \right) \quad (4.21)$$

Substituting data given in Appendix F.5 gives a noise figure of 1.38 dB at 915 MHz. As stated in (4.21), the relative contribution of the transistor noise sources to the overall signal-to-noise ratio depends upon the source impedance seen at the transistor input terminal, and there is an optimum source impedance which will result in the lowest noise figure.

In general, maximum gain and minimum noise figure can not be obtained simultaneously. The design equation used to obtain a given noise figure is [20]

$$F = F_{min} + \frac{R_n}{G_g} \left[(G_{on} - G_g)^2 + (B_{on} - B_g)^2 \right] \quad (4.22)$$

Here $(G_g + jB_g)$ is the generator admittance presented to the input of the LNA, and $(G_{on} + jB_{on})$ is the generator admittance that provides optimal noise performance. R_n is the noise resistance and indicates the sensitivity of F to generator admittance, while F_{min} is an intrinsic property of active devices. Hawkins [28] calculated the noise parameters of a silicon BJT based on the T-equivalent circuit as shown in Figure 4.12.

Figure 4.12: Hspice noise model for vertical silicon BJT.

The final results presented as equation (4.23) and (4.24) can be used to approximate the optimal input impedance which will result in the optimal noise figure.

The optimal source resistance is,

$$R_{opt} = \sqrt{r_b^2 - (X_{opt})^2 + \left(1 + \frac{f^2}{f_b^2}\right) \times \frac{r_e(2r_b + r_e)}{\alpha_o a}} \quad (4.23)$$

and the optimal source reactance is,

$$X_{opt} = \left(1 + \frac{f^2}{f_b^2}\right) \times \frac{2\pi f C_{te} r_e^2}{\alpha_o a} \quad (4.24)$$

where,

$$a = \left\{ \left(1 + \frac{f^2}{f_b^2}\right) \left(1 + \frac{f^2}{f_e^2}\right) - \alpha_o \right\} \times \frac{1}{\alpha_o} \quad (4.25)$$

Transistor parameters can be found in Appendix E.4.

The low frequency common-base gain (α_o) is given by,

$$\alpha_o = \frac{\beta}{(\beta + 1)} = 0.991 \quad (4.26)$$

The total base resistance (r_b) is current dependent and can be determined from the noise analysis. Appendix E.5 indicates an output noise due to the base resistance of $2.62\text{e-}19 \text{ V}^2/\text{Hz}$ or equivalently an input noise of $1.09\text{e-}19 \text{ V}^2/\text{Hz}$. The base resistance is then given by

$$r_b = \frac{V_N}{4kT} = 6.67 \, \Omega \quad (4.27)$$

where k is the Boltzmann's constant ($1.374 \times 10^{-23} \text{ J/K}$), T is in degrees Kelvin (298 at room temperature), and V_N is the voltage noise due to the resistor. The emitter-base junction capacitance (C_{te}) is, from equation (4.8), equal to 2.01 pF .

The emitter resistance (r_e) is given by

$$r_e = \frac{kT}{qI_c} = 6.6 \, \Omega \quad (4.28)$$

where the electron charge (q) is 1.62×10^{-19} C and I_c is the collector current of 4mA.

The base cut-off frequency (f_b) can be approximated by

$$f_b = \frac{1}{2\pi\tau_x} \quad (4.29)$$

where τ_x is the base-collector transit time.

The emitter-base junction cut-off frequency (f_e) is given by

$$f_e = \frac{1}{2\pi r_e C_{ie}} = 12 \, \text{GHz} \quad (4.30)$$

Since $\alpha \sim \alpha_o$ we make the assumption that $f_b \gg f_e$ (i.e base-limited case). Then equations (4.23), (4.24) and (4.25) can be reduced to:

$$R_{opt} = \sqrt{r_b^2 - (X_{opt})^2 + \frac{r_e(2r_b + r_e)}{\alpha_o a}} \quad (4.23a)$$

$$X_{opt} = \frac{2\pi f C_{ie} r_e^2}{\alpha_o a} \quad (4.24a)$$

where

$$a = \left\{ \left(1 + \frac{f^2}{f_e^2} \right) - \alpha_o \right\} \times \frac{1}{\alpha_o} = 0.01393 \quad (4.25a)$$

Substitution of the above data yields the following input source impedance

$$Z_{OPT} = (90.7 + j 36.4) \, \Omega$$

The resulting optimal noise figure is given as:

$$F_{min} = 1 + a \left(\frac{r_b + R_{OPT}}{r_e} \right) = 1.21 \quad (4.31)$$

This translates into a minimum noise figure of 0.83 dB.

This approximation obtained through Hspice data is somewhat lower than that obtained from Libra, which predicts an optimal noise figure of 0.87 dB for a Z_{OPT} equal to $85 + j39$. Matching the generator to this impedance yields the optimal noise figure. However, the LNA is no longer matched to the $50\ \Omega$ antenna with a resulting input VSWR of 2.3. This is not a viable approach since additional components may now be required for antenna-amplifier isolation, which in itself may degrade the NF as well as adding to the receiver cost, size and weight.

4.1.5 Gain Analysis

The power gain of an amplifier is given as the ratio of the output power (P_{out}) to the available input power (P_{av})

$$G_p = \frac{P_{out}}{P_{av}} = \frac{V_{out}^2 / R_L}{V_{in}^2 / 4R_s} = 4 \cdot \frac{R_s \cdot V_{out}^2}{R_L \cdot V_{in}^2} \quad (4.32)$$

where V_{out} and V_{in} are specified as root-mean square (rms) voltages. Equation (4.32) states that if both input and output are perfectly matched to the same impedance then the power gain equates the small signal voltage gain (S_{21}) squared. In this case, the S_{21} can be defined as the ratio of the output signal (V_{out}) compared to the available input signal ($V_{in}/2$).

The condition for a conjugate match at the input and output ports are satisfied at one frequency only. The maximum power gain is realized when the LNA input and output are impedance matched to the source and load. The LNA shown in Figure 4.1 is properly matched to the source and load at a frequency of 915 MHz and under these conditions the LNA can be represented by the simplified hybrid Π -model shown in Figure 4.13.

Figure 4.13: Simplified small-signal Π -model of the common-emitter LNA (shown in Figure 4.1) from which the transfer function V_{out}/V_{av} is determined using nodal analysis. Here V_{av} is actually half of V_{in} (shown in Figure 4.1). The Norton theorem has been applied to facilitate the analysis. The voltage gain of the amplifier is taken as the ratio of the voltage across the load to the available voltage at the LNA input.

The power gain of the common-emitter LNA can be approximated, assuming the simplified model shown in Figure 4.13, by solving the small-signal gain transfer function (S_{21}) using two nodal equations, at node 1 and 2 respectively.

At node 1:

$$\frac{V_{av}}{r_{bb'} + j\omega L_{mi}} = \frac{V_{\pi} + g_m V_{\pi} Z_E}{r_{bb'} + j\omega L_{mi}} + V_{\pi} j\omega C_{\pi} + V_{\pi} (g_m Z_E j\omega C_{\mu} + j\omega C_{\mu}) - V_{out} j\omega C_{\mu} \quad (4.33)$$

where $r_{bb'}$ is the base resistance plus the resistive component of the inductor L_{mi} while Z_E represents the emitter inductor with its associated lossy component. V_{av} can be isolated by manipulating the above equation to yield:

$$V_{av} = (V_{\pi} \cdot A) - V_{out} [-\omega^2 C_{\mu} L_{mi} + j\omega C_{\mu} r_{bb'}] \quad (4.34)$$

where A is defined as,

$$A = 1 + g_m Z_E + j\omega C_{\pi} + j\omega g_m Z_E C_{\mu} r_{bb'} - \omega^2 L_{mi} g_m Z_E C_{\mu} + j\omega r_{bb'} C_{\mu} - \omega^2 L_{mi} C_{\mu} \quad (4.35)$$

Applying continuity of current at node 2 gives:

$$\{V_{\pi} [1 + g_m Z_E] - V_{out}\} \cdot j\omega C_{\mu} = g_m V_{\pi} + \frac{V_{out}}{Z_L} \quad (4.36)$$

Rearranging equation (4.36) yields,

$$V_{\pi} \left[j\omega C_{\mu} Z_L \left(\frac{1}{g_m} + Z_E \right) - g_m Z_L \right] = V_{out} (1 + j\omega C_{\mu} Z_L) \quad (4.37)$$

Let the multiplier of V_{π} in (4.37) be B , where B is

$$B = j\omega C_{\mu} Z_L \left(\frac{1}{g_m} + Z_E \right) - g_m Z_L \quad (4.38)$$

Then we get,

$$V_{\pi} = \frac{V_{out} (1 + j\omega C_{\mu} Z_L)}{B} \quad (4.39)$$

If we combine (4.39) and (4.34) we can solve for the LNA matched power gain at $f_o = 915$ MHz.

$$|S_{21}|^2 = \left| \frac{B}{A (1 + j\omega_o C_{\mu} Z_L) + B (\omega_o^2 C_{\mu} L m - j\omega_o C_{\mu} r'_{bb})} \right|^2 \quad (4.40)$$

Equation (4.40) is the classical equation of feedback mechanism. The second term in the denominator of (4.40) provides the negative feedback which is the result of C_{μ} and the emitter inductor in (4.38). The simulated Libra S_{21} parameter is shown in Figure 4.14. The Hspice simulated S_{21} small signal gain is 13.6 dB.

The simulated LNA gain at 915 MHz is 13.9 dB while the approximate theoretical value, using (4.40) and data shown in Appendix E.4, is 13.2 dB. The small difference can be attributed to the fact that C_{mi} was not included in the analysis for simplification.

Figure 4.14: Frequency response of the common-emitter LNA shown in Figure 4.1. A maximum gain of 13.9 dB at 915 MHz is observed with a 3dB bandwidth of 648 MHz centred at 890 MHz.

Note that in an integrated circuit where the LNA, filter and mixer coexist, there is no longer a requirement to have the LNA output matched to $50\ \Omega$. The LC output network can then be resonated to a larger load to further increase the gain of the LNA. A greater load also allows a larger output voltage swing. From Libra simulation and the RLC network match to a $75\ \Omega$ load, a gain of 16 dB, NF of 1.2 dB and a P_{1dB} of -20.4 dBm are obtained for the $75\ \Omega$ output match common-emitter LNA.

If a $50\ \Omega$ match is necessary, the gain and P_{1dB} can still be improved by adding a matching network to transform the LC $75\ \Omega$ network to the required $50\ \Omega$. Appendix F.2 shows the complete schematic for the LC resonant network matched to a $50\ \Omega$ load. This configuration results in a gain, simulated by Libra, of 15.7 dB, a noise figure of 1.23 dB, and a P_{1dB} of -19 dBm. However, in this instance an inductor between the LNA and subsequent stage is not as attractive a solution.

4.1.6 Bandwidth Analysis

One reason the output power varies with frequency is the frequency dependence of the matching networks. However, the most important factor that limits the frequency response is the variation of the transistor S -parameters with frequency. The input inherent bandwidth, $(BW)_{in}^i$, is the bandwidth obtained under conjugate matched conditions. The input port, under conjugate matched conditions, can be represented by the network shown in Figure 4.15.

Figure 4.15: Equivalent network of the input port under conjugate match conditions.

A conjugate match means that $\Gamma_s = \Gamma_{in}^*$ or $Y_s = Y_{in}^*$ with

$$Y_{in} = G_{s,M} + jB_{s,M}$$

and

$$Y_s = G_{s,M} - jB_{s,M}$$

The input inherent bandwidth is given by [20]

$$(BW)_{in}^i = \frac{f_o}{Q_{in}} \quad (4.41)$$

where f_o is the frequency at which the conjugate match values were obtained and Q_{in} is the quality-factor of the equivalent input network.

The value of Q_{in} can be expressed as,

$$\frac{1}{Q_{in}} = \frac{2G_{s,M}}{|B_{s,M}|} \quad (4.42)$$

where $G_{s,M}$ is the input conductance and $B_{s,M}$ is the input susceptance. Similarly, the output inherent bandwidth is given by

$$(BW)_{out}^i = \frac{2f_o G_{s,M}}{|B_{L,M}|} \quad (4.43)$$

For the common-emitter low-noise amplifier shown in Figure 4.1, under matched conditions, we find that at 915 MHz the admittances are from (4.15)

$$Y_{in} = (5.49 + j 9.91) \times 10^{-3} S$$

and from $1/Z_L$ in (4.13)

$$Y_{out} = (13.84 + j 27.11) \times 10^{-3} S$$

From Y_{in} and Y_{out} , it follows that $G_{s,M} = 5.49 \times 10^{-3}$, $B_{s,M} = 9.91 \times 10^{-3}$, $G_{L,M} = 13.84 \times 10^{-3}$, and $B_{L,M} = 27.11 \times 10^{-3}$.

Therefore, from (4.41) and (4.43),

$$(BW)_{in}^i = \frac{2(915 \times 10^6) 5.49 \times 10^{-3}}{9.91 \times 10^{-3}} = 1.01 \text{ GHz}$$

and

$$(BW)_{out}^i = \frac{2(915 \times 10^6) 13.84 \times 10^{-3}}{27.4 \times 10^{-3}} = 0.92 \text{ GHz}$$

Since the inherent output bandwidth is less than the inherent input bandwidth we conclude that the bandwidth limitations due to the matching networks are determined by $(BW)_{out}^i$. The broad inherent output bandwidth can not be obtained in practice because of the transistor S -parameter variations with frequency. In fact, the overall 3dB bandwidth of the common-emitter amplifier, as shown in Figure 4.14, is 648 MHz.

4.1.7 Isolation

The isolation between the input and output ports of the LNA can be expressed by the magnitude of the reverse scattering parameter S_{12} . It is essentially the insertion loss of the amplifier with the signal incident to the output port. This isolation can effectively reduce the amount of leaked LO signal that may come from the mixer. The amount of isolation for this configuration, simulated by Hspice, is limited by the Miller-effect and is in the order of -20 dB as can be seen from Figure 4.16.

Figure 4.16: Input/output port isolation of the common-emitter LNA shown in Figure 4.1. An isolation greater than -20 dB is observed from 800 to 1200 MHz.

4.1.8 Non-Linear Analysis

The measures of distortion and overload are measured by the 1-dB compression point and *IP3* respectively. If the gain is set too high, overload will occur at the output and will be a major source of nonlinearity. Reduced bias level will result in overload at the BJT input as the transistor enters saturation, effectively reducing the dynamic range of the LNA. Linearity improvement can therefore be achieved, for a given load, at the expense of gain or power consumption.

The maximum output voltage swing that can be achieved without distortion, for a bias current of 4 mA and 50 Ω system (25 Ω effective resistance for a perfect output match), and class A operation, is 200 mV peak-to-peak (mVpp). The common-emitter LNA was shown to have a linear gain of 4.97, which would translate into a maximum available signal power at the input of -24 dBm (40 mVpp), being the expected P_{1dB} . The theoretical peak voltage value of the 1dB compression point for a voltage-driven bipolar transistor is given as, [17]

$$V_{1dB} = \sqrt{0.88} \cdot \frac{kT}{q} \quad (4.44)$$

This corresponds to a 48 mVpp voltage swing at the input. This suggests that the common-emitter LNA, under the present bias conditions, will be limited by the maximum available output voltage swing. Figure 4.17 shows the time domain response of the common-emitter LNA where a 40 mVpp 915 MHz signal is applied to its input (80mVpp, -18 dBm, at the generator). From Figure 4.17(c) we have an output voltage swing of 188.32 mVpp and from (b) we get an available voltage swing of 38.4 mVpp. Using (4.32) we get a gain of 13.8 dB which is within 1 dB of the simulated linear gain. This indicates that the input stage of the LNA is linearized to some extent by the effective high-frequency emitter degeneration contributed by L_E .

Figure 4.17: Time-domain waveforms for the common-emitter LNA shown in Figure 4.1 with an input power source of -18 dBm. (a) $V(\text{src})$ represents the voltage supplied by the generator, (b) $V(\text{in})$ is the signal seen at the LNA input, and (c) $V(\text{out})$ is the signal across the $50\ \Omega$ load.

Figure 4.18: Time-domain waveforms for the common-emitter LNA shown in Figure 4.1 with an input power source of -12 dBm. (a) $V(\text{src})$ represents the voltage supplied by the generator, (b) $V(\text{in})$ is the signal seen at the LNA input, and (c) $V(\text{out})$ is the signal across the $50\ \Omega$ load.

Figure 4.18 shows the time domain waveforms when a source signal of 160 mVpp is applied to the common-emitter LNA. The allowed current swing at the output is dictated by

$$i_c = I_C e^{v_{be}/V_T} \quad (4.45)$$

If $v_{be} \ll V_T$ then equation (4.43) can be approximated by

$$i_c = I_C \left(1 + \frac{v_{be}}{V_T} \right) \quad (4.46)$$

Equation (4.46) implies that as long as the signal is small enough the device will operate along an almost linear segment of the i_c - v_{be} exponential curve. From Figure 4.18, the signal at the collector output of the common-emitter LNA can be seen to be less distorted than the signal at the LNA input. The slewing to the right of the output waveform is an indication of an even harmonic content. This can be seen by displaying the fast-fourier transform (FFT) of the time-domain output waveform shown in Figure 4.18.

Displaying the FFT of the output waveform
 F.F.T. of V(out)
 Power Spectral Density
 dBm

Figure 4.19: Power spectrum density of the time domain signal V(out) shown in Figure 4.18.

The 1 dB compression point is measured under single tone operation. A plot of output power versus input power, as in Figure 4.20, for the common-emitter LNA indicates a P_{1dB} of -21.4 dBm. The measure of distortion is commonly related to a fixed ratio of 10 dB above the 1dB compression point [25]. Therefore the third-order input referred intercept should be -11.4 dBm.

The $IP3_i$ can be determined by the following expression,

$$IP3_i(dBm) = P_{av} + \frac{1}{2}(P_{out} - P_{3I}) \quad (4.47)$$

where P_{av} is the available input power to the LNA (either f_1 or f_2), P_{out} is the output power of one of the fundamental tones (where both tones are of equal magnitude), and P_{3I} is the 3rd order intermodulation ($2\omega_2 - \omega_1$ or $2\omega_1 - \omega_2$) products output power.

Figure 4.20: Power response of the common-emitter LNA shown in Figure 4.1. An RF tone of 915 MHz is applied at the input. The RF source and load impedance are set to 50Ω

From Figure 4.21, with two RF tones at -50 dBm, we determined a third-order intermodulation output power of -125.17 dBm, and a fundamental output power of -36.09 dBm. Therefore, the common-emitter LNA, according to (4.47), has an $IP3_i$ of - 5.46 dBm. The simulated $IP3_i$ is therefore 15.94 dB higher than the simulated 1dB compression point.

A usual way to increase the third order intercept is to operate from a higher VCC which can increase the voltage swing available across the load resistor. However, in this design, the output swing can only be increased by operating at a higher bias, or larger output impedance, as the VCC is basically applied to the collector of the transistor. There is also an upper limit as to the level of bias current which can be applied as the base-collector voltage must remain reverse biased for class A operation.

Figure 4.21: Two RF tones of 915 MHz and 915.03 MHz at a power of - 50 dBm are applied at the common-emitter LNA input generating third-order intermodulation products of 914.7 MHz and 915.06 MHz.

Figure 4.22: Variation of IP_{3i} with log of the emitter bias current: The IP_{3i} is measured according to the 10 dB rule. The input and output impedance of the common-emitter LNA were kept matched to 50Ω .

The relationship of the IP_{3i} to the emitter bias current of the common-emitter LNA is shown in Figure 4.22. A monotonic increase is observed from 2 to 5 mA. This can be intuitive since the major non-linearity of the amplifier can be attributed to the exponential relationship that exists between the base-emitter junction of the transistor. For this reason an upper limit is reached as the v_{be} of the transistor exceeds the thermal voltage.

4.1.9 Sensitivity Analysis

The disadvantage of not using feedback (apart from the effect of L_E) is the temperature dependence of the LNA. This causes about 0.6 dB/°C variation from -40 to 0 °C which is excessive if compared to the Philips SA600 component where a -0.008dB/°C is achieved. This variation can be compensated by on-chip generation of regulated power supplies with temperature dependence designed to first-order cancel the temperature variation of the gain [17]. Graphs showing the effect of temperature variation on gain, noise figure and VSWR are given in Appendix H as well as variation with VCC. The variation of any of the RF parameters with VCC is negligible.

4.2 Cascode Low-Noise Amplifier

The cascode amplifier configuration is used in order to reduce the Miller capacitance multiplication effect of the common-emitter configuration. The topology of the cascode LNA is shown in Figure 4.23. A resonant matching network is used at the collector output of Q_2 while a *series L-shunt C* matching network is used at the input terminal of Q_1 . The emitter area selected for Q_1 is 0.5 X 160µm while the common-base transistor Q_2 has been selected with an emitter area of 0.5 X 80 µm to reduce overall space, as this transistor does not greatly affect the LNA's overall performance.

The cascode LNA should provide the relative following advantages:

- i) greater gain
- ii) reduced emitter inductor due to greater gyration
- iii) better isolation between input and output port
- iv) possibility of a better noise figure

The emitter inductor Z_E is a high-frequency lumped model provided by Mr. José Macedo (Doctorate in progress) and is shown in Appendix I.3.

Figure 4.23 Topology of the cascode low-noise amplifier.

4.2.1 Introduction

The cascode amplifier inherently requires a larger dc supply than the common-emitter LNA. The power consumption of the cascode LNA is approximately twice that of the common-emitter, if operated at the same current level.

A current of 3mA is selected for this configuration which, as shown in Figure 3.4, does not greatly deteriorate the optimal noise figure of the device. The power consumption of the cascode LNA is less than 6 mW. However, a higher gain and lower current will result in a lower $IP3$. This issue will be addressed in section 4.2.2, non-linear analysis.

4.2.2 Stability

The cascode configuration is first simulated without input or output matching networks to determine the stability of the circuit. The stability factors obtained from the Libra (HP/EEsof Software Inc.) simulation yields a K-factor less than one and a B-factor slightly larger than zero. The conditions for unconditional stability stated in (4.2) and (4.3) are therefore not satisfied and there are certain load conditions which may cause the amplifier to oscillate.

The same design procedure as followed with the common-emitter will be applied to the cascode amplifier. An *RLC* tank circuit is applied to the collector output of Q_2 to resonate at $50\ \Omega$. This makes the cascode configuration unconditionally stable and a conjugate match can be applied at the input terminal of Q_1 .

The stability of the match cascode LNA is relatively better than that of the common-emitter LNA, which can allow for greater margin in process variation and component tolerances. The improved stability can be attributed to the reduction of the Miller-effect in the cascode configuration. Since the stability of the cascode LNA is in part due to the output resonant network, the stability as shown in Figure 4.24 can be seen to degrade as the frequency is increased. The K and B factor of stability, as defined in (4.2) and (4.3), are shown in Figure 4.25. The cascode LNA also remains stable from 0.1 to 3 GHz.

Figure 4.24: Comparison of the relative stability factor (μ) of the cascode and common-emitter LNA under $50\ \Omega$ match conditions.

Figure 4.25: K, left axis, and B, right axis, stability factors for the cascode LNA shown in Figure 4.23. The conditions for stability are $K > 1$ and $B > 0$.

4.2.3 Matching Networks

An on-chip inductor of 5nH is selected as with the common-emitter LNA. An ideal conjugate match would require a capacitor of 6 pF at 915 MHz but due to some parasitics from Q_2 a capacitor of 5.6 pF is selected. A resistance of 95 Ω is required to provide maximum power transfer to the 50 Ω output load.

An f_T of 10.21 GHz is obtained from Hspice (trademark of Metasoftware Inc.) simulation, shown in Appendix J.3, for transistor Q_1 at a current of 3mA. Therefore an inductor of 0.5nH at the emitter of Q_1 will gyrate, according to (4.1), to a resistance of 32.1 Ω as seen from the base terminal. A given series resistance of 1.04 Ω for Z_E indicates a Q of 2.76 for this on-chip inductor at a frequency of 915 MHz.

The input reactance of a cascode configuration is [37],

$$X_c^{in} \equiv \frac{1}{2\pi f_o (C_{\pi 1} + 2C_{\mu 1})} \quad (4.46)$$

Substitution of data found in Appendix J.3 into (4.46) gives an input impedance of

$$Z_{in} = (32.1 - j87.4) \Omega$$

The reason for a 0.5 nH inductor is that a high-frequency lumped model was available from Mr. José Macedo. Figure 4.26 shows the transmission response (S_{21}) of the high-frequency model simulated with Libra. From Figure 4.26, there is only a 0.02 dB variation from 0.1 to 2 GHz. Therefore any of the parasitics of the high-frequency lumped model inductor can be assumed negligible, and we conclude that the simplified L - R model is sufficient for our analysis.

Figure 4.26: Frequency response of the on-chip high-frequency inductor lumped model shown in Appendix I.3 and provided by Mr. José Macedo.

Figure 4.26: Frequency response of the on-chip high-frequency inductor lumped model shown in Appendix I.3 and provided by Mr. José Macedo.

The input impedance of the cascode amplifier LNA obtained from Hspice simulation is found to be $(34.1 - j 92) \Omega$, at 915 MHz. The Hspice configuration and data files are shown in Appendix J. The simulated input impedance is in close agreement with the theoretical value.

The input impedance of the LNA can be matched to 50Ω by selecting a *series L-shunt C* matching network as shown in Figure 4.27 where the normalized input impedance is indicated by point A and obtained with Libra. The transformation from point A [i.e. $z_{in} = (38.74 - j99)/50 = 0.78 - j1.98$] to point B is along a constant-resistance circle, and we obtain for the matching inductor impedance $z_L = j1.98 + j 0.45 = j2.38$. Observe that point B is along a unit constant-conductance circle.

The admittance at point B is $y_B = 1 - j0.5$. The transformation from point B to point C (i.e., the origin) is along a constant-conductance circle, and we obtain the capacitor admittance $y_C = 0 - (-j 0.5) = j 0.5$ (or $z_C = 1/j 0.5 = -j 2$). Therefore at point C, $y_{IN} = z_{IN} = 1$ (or $Z_{in} = 50 \Omega$) and the LNA is matched to the 50Ω generator. At 915 MHz, the value of L is

$$L_{mi} = \frac{2.38 \cdot 50}{2\pi(915 \times 10^6)} = 21 \text{ nH}$$

and the value of C is

$$C_{mi} = \frac{1}{2 \cdot 50 (2\pi) 915 \times 10^6} = 1.7 \text{ pF}$$

If we assume a Q of 50 for off-chip inductors we have a series resistance of 2.4Ω associated with the input matching inductor.

```
□ Cascode_Linear_1b
  S1J3
  Cascode
  S[1,1]
```

Frequency 915.0 to 915.0 MHz

Figure 4.27: Design of the *series L-shunt C* matching network, for the cascode LNA shown in Figure 4.23, using a Smith chart. Point A represents the normalized input impedance of the LNA while point C represents the 50Ω impedance of the antenna.

The resulting simulated Libra VSWRs are shown in Figure 4.28. A VSWR very close to one at a frequency of 915 MHz indicates that the derived matching networks effectively provide the conjugate match required for maximum power transfer to the load. The degradation in VSWR as the frequency is increased is worst at the input due to the off-chip inductor, which results in a narrowband input match.

Figure 4.28: Libra simulated input and output VSWR under match conditions, for the cascode LNA shown in Figure 4.23.

4.2.4 Noise Analysis

The $50\ \Omega$ noise figure simulated by Libra is 1.43 dB at 915 MHz as illustrated in Figure 4.29, which is, in accordance with (4.21), yielding an Hspice NF of 1.41 dB. The noise added by the circuit can be approximated by (4.20). Substitution of data given in Appendix J yields a noise figure of 1.48 dB. It can be seen from Figure 4.30 that most of the noise can be attributed to the input transistor. The output shot noise (of Q_1) due to base current is the largest transistor contributor to the total output noise.

1.0000E+00
1.0000E+00
1.0000E+00
1.0000E+00
1.0000E+00

Figure 4.29: Cascode LNA 50 Ω noise figure vs. frequency.

Figure 4.30: Hspice noise allocation for the cascode LNA shown in Figure 4.23 all noises are output referred.

An optimal source impedance of $(80 + j51) \Omega$ given by Libra results in an optimal noise figure of 0.82 dB. The optimal source impedance will result in a VSWR given by:

$$VSWR_{in} = \frac{1 + |\Gamma_{in}|}{1 - |\Gamma_{in}|} \quad (4.47)$$

where Γ is given by,

$$\Gamma_{in} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \quad (4.48)$$

Substitution of Z_0 (50Ω) in (4.47) yields an input VSWR of 2.47 and as explained earlier is deemed unsatisfactory.

4.2.5 Gain Analysis

The power gain, which is the small-signal S -parameter S_{21} squared, can be derived for the cascode LNA with the small-signal Π -model shown in Figure 4.31 where use of the Norton theorem has been applied to facilitate the analysis.

Figure 4.31: Simplified small-signal Π model of the cascode LNA (shown in Figure 4.21) from which the transfer function V_{out}/V_{av} is determined using nodal analysis. V_{av} is the available voltage to the LNA. Under matched condition the available input voltage (V_{av}) is equal to half the voltage supplied by the generator (V_{in}).

We can solve by setting up a nodal equation at node 1,

$$\frac{V_{av}}{r_{bb'} + j\omega L_m} = \frac{V_{\pi 1} (1 + g_{m1} Z_E)}{r_{bb'} + j\omega L_m} + V_{\pi 1} j\omega (C_{\pi 1} + 2C_{\mu 1}) \quad (4.49)$$

This equation can be simplified to:

$$V_{av} = V_{\pi 1} (1 + g_{m1} Z_E) + V_{\pi 1} (j\omega r_{bb'} - \omega^2 L_m) (C_{\pi 1} + 2C_{\mu 1}) \quad (4.50)$$

If we let $V_{\pi 1} \equiv V_{\pi 2}$ then we can express V_{out} as a function of V_{av}

So,

$$V_{av} = V_{\pi 2} (1 + g_{m1} Z_E) + V_{\pi 2} (j\omega r_{bb'} - \omega^2 L_m) (C_{\pi 1} + 2C_{\mu 1}) \quad (4.51)$$

Let the multiplier of $V_{\pi 2}$ in (4.51) be A, where A is

$$A = 1 + g_{m1} Z_E - \omega^2 L_m (C_{\pi 1} + 2C_{\mu 1}) + j\omega r_{bb'} (C_{\pi 1} + 2C_{\mu 1}) \quad (4.52)$$

The output voltage can then be expressed as :

$$V_{out} = -g_{m2} V_{\pi 2} Z_L' \quad (4.53)$$

where Z_L' is given as the parallel combination of the RLC tank circuit with R_L and $C_{\mu 2}$.

Combining (4.51) and (4.53) yields the matched LNA gain at $f_o = 915$ MHz:

$$|S_{21}|^2 = \left| \frac{V_{out}}{V_{av}} \right|^2 = \left| \frac{-g_{m2} Z_L'}{A} \right|^2 \quad (4.54)$$

The LNA gain simulated with Libra and Hspice are in very close agreement: at 915 MHz Hspice predicts a gain of 14.76 dB while Libra predicts 14.82 dB. The approximate theoretical value, using (4.54) and data found in Appendix J, yields a gain for the cascode LNA of 14.8 dB. The Libra S_{21} simulation is shown in Figure 4.29.

Figure 4.32: Frequency response of the cascode LNA shown in Figure 4.23.

Figures 4.32: Frequency response of the cascode LNA shown in Figure 4.23. A maximum gain of 14.8 dB at 915 MHz is observed with a 3dB bandwidth of 560 MHz centred at 890 MHz.

4.2.6 Isolation

The amount of isolation for this configuration is not limited by the Miller-effect and is in the order of - 60 dB as can be seen from the Libra simulation shown in Figure 4.33.

Figure 4.33: Input/output port isolation of the cascode LNA shown in Figure 4.23.

Figure 4.33: Input/output port isolation of the cascode LNA shown in Figure 4.23. An isolation greater than -60 dB is observed from 800 to 1200 MHz.

4.2.7 Non-Linear Analysis

For a 3 mA bias current, 50 Ω system (25 Ω effective), and class A operation, a maximum output voltage swing of 150 mVpp can be achieved, at the output, without distortion. The cascode LNA was shown to have a linear gain of 5.89, which translates into a P_{1dB} of -28 dBm. This corresponds, by the 10 dB rule, to an $IP3_i$ of approximately -18 dBm. Figure 4.34 shows the time domain response of the cascode LNA where a 50 mVpp 915 MHz signal is applied to the LNA input (100 mVpp from generator or -22 dBm).

Figure 4.34: Time-domain waveforms for the cascode LNA shown in Figure 4.22. (a) V_{src} is the signal provided by the generator, (b) V_{in} is the available signal at the LNA input, and (c) V_{out} is the signal across the $50\ \Omega$ load.

Figure 4.34 indicates that distortion occurs first at the output. The Libra simulated P_{1dB} can be seen from Figure 4.35 to be $-26.4\ \text{dBm}$. The $IP3i$, from (4.47) and Figure 4.33, is $-5.6\ \text{dBm}$. This is much higher than the 10 dB rule which is very consistent in practice, therefore the simulated $IP3i$ should be taken with caution.

The reason for a lower P_{1dB} , if compared to the common-emitter LNA, is that the choice of bias current for the cascode LNA results in a smaller available voltage swing at the output. It can also be partly attributed to a reduced emitter degeneration. As well, the cascode LNA has a higher gain, for the same output load, which will further limit the linearity range of the cascode LNA.

Figure 4.35: Power response of the cascode LNA shown in Figure 4.22. An RF tone of 915 MHz is applied to the input.

Figure 4.35: Power response of the cascode LNA shown in Figure 4.22. An RF tone of 915 MHz is applied to the input.

Figure 4.36: Two RF tones at 915 MHz and 916 MHz at a power of -50 dBm are applied at the cascode LNA input generating third-order intermodulation products at 914 MHz and 916 MHz.

Figure 4.36: Two RF tones at 915 MHz and 916 MHz at a power of -50 dBm are applied at the cascode LNA input generating third-order intermodulation products at 914 MHz and 916 MHz.

Chapter 5

Mixer Design

5.1 Introduction

The mixer is of fundamental importance in the design of RF and microwave systems. The purpose of the mixer is basically that of frequency translation which in turns simplifies RF and microwave systems design. The frequency translation required is determined by the signal processing capability of the following digital stages. A circuit which can serve the purpose of frequency translation is a linear multiplier, where a linear response is required with respect to only one of the inputs. This input is known as the modulating input.

The LO input on the mixer is sourced by an oscillator that would be matched for maximum power transfer to ensure minimum reflection, corruption, and harmonic distortion of the oscillator signal. The most important figure of merit for the LO is double sideband noise. This phase noise on the LO will be translated directly to the IF output at the same ratio as it appeared on the LO.

The output of the mixer is followed by an IF filter which is used to further suppress adjacent channel interferers or other unwanted signals. The demodulation stage should be presented a signal which has the specified in-band SNR and has out-of-band suppression.

Filters used at this stage will normally be high Q components to pass single channel information at the given IF frequency and modulation bandwidth. They may come in the form of SAW, crystal, ceramic, or active tuned filters.

The circuit configuration explored in this thesis is based on the cross-coupled differential stage shown in Figure 5.1.

Figure 5.1: Generic balanced modulator. The modulating signal which is taken to be the RF signal from the LNA is applied to terminal v_{RF} . The second signal, known as the LO signal, is applied to the non-linear terminal v_{LO} . This terminal is driven by an LO signal of constant amplitude.

The advantages of the double-balanced mixer are that it provides high isolation from both the RF and LO signals and low signal distortion.

The name “double-balanced” stems from the fact that even-order RF and LO intermodulation products are greatly suppressed due to the differential symmetry of the circuit. It follows that because both RF and LO signals are suppressed, the performance requirement of the IF section will not be as stringent as if a single-ended or single-balanced mixer was used. This is an important aspect when considering a monolithic approach, where spurious signals could interfere with other circuits integrated on the same IC. In addition to these benefits, the double-balanced mixer has lower loss, associated with a 100% duty cycle, conducting on both polarities of the LO signal.

If the two inputs of the circuit shown in Figure 5.1 are driven by two sinusoidal input signals $v_{LO}(t)$ and $v_{RF}(t)$ given as,

$$v_{LO}(t) = V_{LO}\cos\omega_{LO}t \text{ and } v_{RF}(t) = V_{RF}\cos\omega_{RF}t$$

then the output voltage $v_o(t)$, derived in Appendix K, is given as,

$$v_o(t) = K \sum_{n=1}^{\infty} \frac{A_n v_{RF}}{2} [\cos(\omega_{RF} + n\omega_{LO})t + \cos(\omega_{RF} - n\omega_{LO})t] \quad (5.1)$$

where the coefficient K is,

$$K = \frac{R_L}{R_E + r_e} \quad (5.2)$$

with r_e being the dynamic emitter resistance of Q_3 (or Q_4).

5.2 Study of a Double-Balanced Single-Ended Mixer

The double-balanced mixer shown in Figure 5.2 has both inputs and output connected single-ended. This may generate some common-mode currents which will increase the level of harmonics at the output as well as the level of feedthrough.

The RF port is easily matched to $50\ \Omega$ by placing a shunt resistance (R_4) across the high impedance mixer input to ground. This same technique is used on the LO port. The use of an emitter follower buffer at the mixer output provides some degree of wideband output matching under varying load conditions.

Figure 5.2: 0.8 μm bipolar single-ended double-balanced mixer (courtesy of Mr. José Macedo). Note: $\bullet$ are input/output ports to the packaged device.

Transistors Q_1 and Q_2 with resistors R_1 and R_2 provide a bias current of 1 mA. The nominal size of the transistors is $0.8\mu\text{m} \times 4\mu\text{m}$ which implies $0.8\mu\text{m} \times 1\text{x}$. Transistors Q_{3-4} are size 15x in order to reduce the noise contribution from their base resistance. Transistors Q_{5-8} are size 2x in order to provide a better f_T which is necessary for fast switching and good gain. Transistors $Q_{9,10}$ are 15x as they do not require high f_T since at this point we are only interested in the IF.

Transistor Q_{11} provides a current of 5.17 mA at the collector of Q_{10} , which is necessary to provide good matching from the $500\ \Omega$ load of the double-balanced mixer collectors to the buffer output impedance of $50\ \Omega$. Resistor R_3 ($41.5\ \Omega$), which is mathematically equivalent to $2R_E$ in (5.2), is used to provide emitter degeneration in order to increase the linearity of the mixer. This linearity, as one would expect, is gained at the expense of the mixer conversion gain.

Note that this circuit was intended to operate for an RF of 1.9 GHz, down-converted to 300 MHz with an LO of 2.2 GHz, but the mixer should operate equally well down to the frequency range intended in this thesis.

5.2.1 Simulated, Theoretical and Experimental Results

The resulting Libra (HP/EEsof Software Inc.) simulated VSWR for the RF port is shown in Figure 5.3. A VSWR of 1.32, obtained from Libra and confirmed with (4.47), can be attributed to the wire bonding used in the package for interconnections which result in an input impedance, at the RF port, of $(52 + j14)$. The input impedance is obtained using the Libra schematic shown in Appendix L with the LO port terminated with a shunt $50\ \Omega$ resistor.

Figure 5.3: RF port VSWR for the double-balanced modulator shown in Figure 5.2. The LO port is terminated with a $50\ \Omega$ load making the mixer a two-port device during the simulation.

The next parameter of interest is the isolation provided by the mixer. The isolation can be defined as the amount of attenuation provided when a signal is applied to one port of a mixer and measured at another port. The LO power level is generally significantly greater than either the RF or IF signals. High isolation between the LO-to-RF port and LO-to-IF port is desirable to prevent the LO signal from leaking back to the antenna or overloading the IF circuitry.

The Libra software allows one to effectively look at the LO-to-RF and LO-to-IF isolation. An expected maximum signal of $-12\ \text{dBm}$ is applied to the RF port while the LO signal is swept from -10 to $+10\ \text{dBm}$. From Figure 5.4, at $0\ \text{dBm}$, an LO-to-IF isolation of $38\ \text{dB}$ with an LO-to-RF isolation of $42\ \text{dB}$ can be observed.

Figure 5.4: LO-to-IF and LO-to-RF isolation for the double-balanced mixer shown in Figure 5.2.

The conversion gain is one of the most important specifications on a mixer. It is a measure of how efficiently a mixer converts energy from one frequency to another and is defined as the ratio of the output power to the input power for a given local oscillator power applied.

The available voltage conversion gain (VG_C) of a mixer can be defined as the ratio of the voltage at the IF frequency (V_{IF}) to the available voltage at the RF frequency (V_{RF}).

$$VG_C = 20 \log \left(\frac{V_{IF}}{V_{RF}} \right) \quad (5.3)$$

The theoretical voltage gain can be determined by solving (5.1) with $n = 1$. From equation (25) in Appendix J, we get $A_1 = 4/\pi$. The emitter dynamic resistance r_e of Q_4 is, from (4.28), 26Ω . The net resistance at the collector output of Q_8 can be determined by looking at the input impedance of the buffer circuit alone with a shunt resistance, equivalent to R_7 , at the base of Q_9 . The Libra simulation indicates an input impedance of $(443.8 - j 43.69)\Omega$.

Solving for K of (5.2), we get,

$$K = \frac{R_L}{R_E + r_e} = \frac{443.8}{25 + 26} = 8.7$$

The voltage ratio V_{IF}/V_{RF} can be obtained from (5.1),

$$\frac{V_{IF}}{V_{RF}} = \frac{KA_n}{4} = \frac{8.7 \times 4}{4 \cdot \pi} \cong 2.74$$

The extra factor of 2 added in the denominator is to take into account a single-ended output. Substitution of the above ratio in (5.3) results in a theoretical voltage conversion gain of 8.76 dB. The simulated voltage gain is obtained from a transient analysis in Hspice (Metasoftware Inc.). The Hspice configuration and data files are given in Appendix L.

An RF signal of 112.47 mVpp (- 15 dBm) at 915 MHz is fed to the lower terminals while a 632mVpp LO signal (0 dBm) at 1015 MHz is fed to the upper terminals. The Hspice transient analysis of the mixer is shown below in Figure 5.5. A beat pattern between the 100 MHz IF and the 1015 MHz LO can be seen in waveform (b) of Figure 5.5.

Substitution of the amplitudes of the waveforms shown in Figure 5.5 into (5.3) yields a voltage gain of 7.96 dB. The ~1 dB disagreement with the theoretical value could be attributed to transistor $Q_{5,8}$ lowering down the output impedance or additional external device resistance present in the model.

Figure 5.5: Time-domain waveforms of the 0.8 μm double-balanced mixer shown in Figure 5.2. (a) V(IN4) represents the available RF voltage (~ 60 mVpp) to the mixer input, (b) V(I1) represents the IF voltage at the collector node of Q_8 (~ 150 mVpp).

The spectrum shown in Figure 5.6, of the buffer output waveform at the IF port, is performed with Libra to determine the 2nd harmonic intercept (SHI) of the double-balanced mixer shown in Figure 5.2 for later comparison with the optimized mixer.

The n th harmonic intercept is defined as [35]:

$$nHI = S + \frac{D}{n-1} \quad (5.4)$$

where

S = the power of the fundamental (100 MHz)

D = the difference between the level of the fundamental and the level of the n th harmonic from $f_{LO} = f_{IF} - nf_{RF}$

Figure 5.6: Power spectrum density of the output waveform taken across the 50 Ω load at the IF port of the 0.8 μm double-balanced mixer shown in Figure 5.2 for an RF power level of -20 dBm and LO power level of 0 dBm.

Figure 5.6: Power spectrum density of the output waveform taken across the 50 Ω load at the IF port of the 0.8 μm double-balanced mixer shown in Figure 5.2 for an RF power level of -20 dBm and LO power level of 0 dBm.

Reading the signal levels from Figure 5.6 shows that the power of the fundamental (S) is -11.8 dBm and the difference (D) between the second harmonic (815 MHz) at -43.2 dBm and S is 31.4 dBc. According to (5.4) this results in a SHI of 19.6 dB.

A Libra simulation of the IF output power versus RF input power, for an LO of 0 dBm is shown below in Figure 5.7. Recall from chapter 4 that the voltage gain, as expressed by (5.3) equates the power gain if both the input and output impedances are matched to the same impedance.

Figure 5.7: Power response of the double-balanced mixer shown in Figure 5.2. A tone of 915 MHz is applied to the RF port with a tone of 1015 MHz, 0 dBm, applied at the LO port. All ports are terminated in $50\ \Omega$.

A conversion gain of 8.12 dB with a $P_{IdB} = 12$ dBm can be observed from Figure 5.7. By the 10 dB rule, this yields an $IP3_i$ of -2.0 dBm. Using (4.47), the two-tone Libra simulation shown in Figure 5.8 gives an $IP3_i$ of -4.2 dBm. The power conversion gain obtained with Libra is in close agreement with the voltage conversion gain obtained with the transient analysis performed with Hspice. The mixer was in a standard enclosed package with $50\ \Omega$ SMA ports. The measurements were performed using the HP 8970B Noise Figure Meter (which also provides gain measurement) whose ports are also $50\ \Omega$. The interconnections were made with SMA-to-BNC cables. The resulting measured gain of the packaged mixer was determined to be 7.88 dB with a measured $IP3_i$ of -3.64 dBm. This is also in close agreement with the Libra simulated results.

Figure 5.8: Two RF tones of 915 MHz and 916 MHz at a power of -50 dBm are applied to the RF port of the double-balanced mixer shown in Figure 5.2 for an LO power level of 0 dBm.

Figure 5.8: Two RF tones of 915 MHz and 916 MHz at a power of -50 dBm are applied to the RF port of the double-balanced mixer shown in Figure 5.2 for an LO power level of 0 dBm.

The next parameter of importance is the noise figure of the mixer. The noise figure of a mixer is often referred to in terms of single-side band (SSB) or double-side band (DSB). The DSB measure takes into account the fact that the image frequency (f_{IM}) may be present at the RF port of the mixer. The image frequency is given as,

$$f_{IM} = 2f_{IF} + f_{RF} \quad (5.5)$$

Once this signal is mixed with the LO it also produces a signal at the IF frequency which cannot be filtered out. The resulting noise power spectrum due to the RF is then halved and the DSB measure is 3 dB lower than the SSB.

Unlike the gain of the mixer, the noise figure is rather a complicated process to analyse. However the same basics apply to the mixer as to the LNA. Any resistors in the input path of the RF will degrade the noise figure of the mixer.

Bias currents must be optimized to provide good device noise figure. The switching speed of the quad Q_{5-8} is also important in reducing the noise figure. When the LO signals fed to the mixer are at the same level, little of the RF signal appears at the IF port and all four transistors are forward biased and contribute to the noise figure. Consequently the signal to noise ratio is very low during this interval and fast switching of the quad is desired. The other condition will be when half the quad is in the active region and the other half is off (e.g. Q_5 and Q_8 on while Q_6 and Q_7 are off). During this cycle the transistors in the active mode operate in the common-base configuration and the dominant noise sources are the collector shot-noise and noise from the extrinsic base resistance [24].

The non-linear noise analysis capability of Libra (HP/EEsof Software Inc.) was used to simulate the mixer noise figure as a function of LO power which is shown in Figure 5.9. The Libra test bench is shown in Appendix M, Figure M.1. A simulated noise figure (SSB) of 16.7 dB is obtained for an LO power level of 0 dBm. The measured SSB noise figure of the double-balanced mixer shown in Figure 5.2, under the same conditions, was 17.3 dB or equivalently, a DSB noise figure of 14.3 dB.

□ Noise Figure (dB) vs. Power (dBm)

Figure 5.9: Double-balanced mixer 50 Ω noise figure vs. LO power.

From a system perspective, if we take the common-emitter LNA previously discussed with a noise figure of 1.27 dB and a gain of 13.9 dB then the combined noise figure of the LNA and mixer would be, according to (2.3),

$$10\log F = 10\log\left(1.34 + \frac{46.77 - 1}{24.55}\right) = 5.1\text{ dB}$$

If we reduce the LO power to -10 dBm, the noise figure from Figure 5.8 becomes 18.4 dB, resulting in a system noise figure of 6.15 dB. This is an increase of 1.05 dB in system noise figure, for a 10 dB reduction in LO power. At an LO power level of -10 dBm, the mixer displays a conversion gain of 6.75 dB, a reduction of 1.37 dB.

it may be worth considering operating the mixer at an LO power level which does not optimize its noise figure, if the VCO is to be integrated on the same IC. The advantages in doing so is that a 10 dB reduction in LO drive greatly reduces the design constraint placed on the VCO.

There is also a lesser chance of LO leakage which can occur through parasitic signal paths that exist on-chip within the IC package. The system noise figure can be improved from increasing the LNA gain by appropriate selection of the LNA output impedance. A lower conversion gain can be easily compensated for in the mixer design.

It was observed during measurement of the noise figure that there was a large difference of the noise figure depending on the LO source used. If the HP8673C RF generator was utilized a noise figure of 27 dB was recorded, while the Rohde & Schwarz generator gave a noise figure of 14.2 dB. A look at the phase noise of the two generators revealed that the HP8673C had a noise floor of -115 dBc/Hz at 50 KHz from the carrier while the Rohde & Schwarz generator was found to have a noise floor of -125 dBc/Hz, again at 50 kHz from the carrier. This confirms that phase noise on the LO is translated directly to the IF output at the same ratio as it appears on the LO. This emphasize the importance of a clean LO.

5.3 Performance Analysis

It is the intent to optimize this mixer as to be operational with the common-emitter LNA presented in chapter 4. The common-emitter LNA was found to have an input P_{1dB} of -21.4 dBm with a gain of 13.9 dB. Therefore the maximum input signal which can be provided to the mixer is -7.5 dBm. The current double-balanced mixer has a 1 dB compression point of -12 dBm for a conversion gain of 8.12 dB and consequently is the limiting component. The linearity of the mixer must be increased by 4.5 dB to take full advantage of the dynamic range provided by the LNA.

A high resistive degeneration at the emitter of $Q_{2,3}$ is required when high linearity is to be achieved. However while effectively increasing the $IP3$ it also causes a large degradation in the noise figure of the mixer. Figure 5.10 shows the relationship between noise figure and conversion gain as the resistive emitter degeneration is varied.

Figure 5.10: Noise figure and conversion gain vs. resistive emitter degeneration for the double-balance mixer shown in Figure 5.2.

Linearity improvement can generally be assumed to be inversely proportional to conversion gain if the compression takes place at the output. Under this assumption, the mixer should be operated at a conversion gain of 3.6 dB to achieve a P_{1dB} of -7.5 dBm. From Figure 5.10, a resistive emitter degeneration of $\sim 100 \Omega$ is required to obtain a conversion gain of 3.6 dB, leading to a noise figure of 20 dB.

Figure 5.11: Noise figure and conversion gain vs. inductive emitter degeneration for the double-balanced mixer shown in Figure 5.2. The unit of measure for the inductor is the nanohenry (nH).

One way to diminish the impact of emitter degeneration on noise figure is to use an on-chip inductor. Figure 5.11 shows the noise figure and conversion gain obtained for an inductor varying from 0.1 nH to 20.1 nH. An inductor of 8.5 nH yields an impedance of $(49.54 \angle 80^\circ) \Omega$. We can see from Figure 5.10 that there is indeed an improvement in noise figure as well as a slight increase in conversion gain. If we recall equation (5.2) and replace R_E with $r_s + j\omega L_E$, we get,

$$K = \frac{R_L}{(r_s + j\omega L_E) + r_e} = \frac{443.8}{41.57 + j24.4} = 9.21 \angle -30.4^\circ$$

which explains the slight improvement in gain.

Following the study of the mixer in $0.8\mu\text{m}$ BiCMOS, the double-balanced-mixer shown in Figure 5.2 was simulated in the advanced silicon bipolar technology (AP30) with the same bias levels applied to the quad and buffer. The Libra schematic is shown in Appendix N. The optimal transistor size for the quad $Q_{5,8}$ is summarized in Table 5.1 while the optimal size for transistor Q_3 and Q_4 is summarized in Table 5.2.

Table 5.1: Double-Balanced Mixer Noise Figure and Conversion Gain for Various Upper Quad ($Q_{5,8}$) Transistor Sizes. Transistors $Q_{3,4}$ are $0.5 \times 60 \mu\text{m}$ (1xAP30_60).

Transistor ($Q_{5,8}$) Size (μm)	Noise Figure(dB)	Conversion Gain (dB)
0.5 X 10	15.82	6.95
0.5 X 40	15.73	6.93
0.5 X 60	15.71	6.52
0.5 X 80	15.76	6.31

Table 5.2: Double-Balanced Mixer Noise Figure and Conversion Gain for Various $Q_{3,4}$ Transistor Sizes. Transistors $Q_{5,8}$ are $0.5 \times 60 \mu\text{m}$ (1xAP30_60).

Transistor ($Q_{3,4}$) Size (μm)	Noise Figure(dB)	Conversion Gain (dB)
0.5 X 60	16.6	6.02
0.5 X 80	15.6	6.55
0.5 X 120	15.58	6.45
0.5 X 180	15.81	6.00

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From Table 5.1, an emitter area of $0.5 \times 60 \mu\text{m}$ (AP30_60) is selected for transistors Q_{5-8} . Table 5.2 indicates that an emitter area, for Q_{3-4} , of $0.5 \times 120 \mu\text{m}$ (2X AP30_60) will yield the lowest noise figure. Selection of these transistors for the mixer topology shown in Figure 5.2 leads to a simulated Libra noise figure and conversion gain of 15.58 dB and 6.45 dB, respectively, with a P_{1dB} compression of -14 dBm.

This gives a 1.12 dB noise figure improvement over the $0.8 \mu\text{m}$ technology. The noise figure can be improved if inductive emitter degeneration is used. An emitter degeneration of 8.5 nH with an assumed Q of 6 yields a simulated Libra noise figure of 13.53 dB with a conversion gain of 8.14 dB and P_{1dB} of -15 dBm.

5.4 Mixer Optimization

The mixer configuration of Figure 5.2 is limited in the bias current under which the upper quad will remain in the active mode. This can be corrected if either the VCC is increased or resistors R7 and R8 lowered. The first approach will increase the power consumption for the same bias current and goes against the fundamental requirement of low battery operation for hand-held devices. The second approach will result in a conversion loss. A modified design is therefore needed to achieve the performance sought.

The double-balanced mixer shown in Figure 5.12 will be optimized in the advanced process (AP30) to obtain a P_{1dB} of at least -7.5 dBm with a noise figure of less than 10 dB. The overall power conversion gain of the NE/SA600 from Philips is given as +13.4 dB, for a net resistance of 500Ω at the IF frequency at the IF port, with overall noise figure of 3.5 dB and overall P_{1dB} of -23 dBm.

The optimized mixer can therefore have a conversion gain as low as -0.5 dB and still meet this specification. Transistors Q_{1-2} with resistors R_1 and R_2 provide a total bias current of 6 mA from a 3.0 volt battery. The power consumption of the device should therefore be 18 mW.

Figure 5.12: Optimized double-balanced mixer using an advanced silicon bipolar technology. An on-chip balun at the RF port is assumed while an off-chip balun is used at the IF port.

A $50\ \Omega$ shunt resistor (R_{LO}) at the LO port will provide satisfactory matching as long as the input impedance at the base of Q_5 and Q_8 is fairly high. This condition is somewhat degraded due to the large devices required at the RF port. A matching inductor is therefore required to resonate the reactance present at the LO port.

The LO is fed single-ended with on-chip capacitor C_1 providing an RF ground to the base of Q_{6-7} . The use of a transformer at the output facilitates matching to $50\ \Omega$. An on-chip transformer at the IF frequency is not practical due to its size and loss. An off-chip surface mount transformer is therefore required at the IF port. An off-the-shelf centre-tapped transformer is available from MINI CIRCUITS, part number T4-1-KK81, usable for IF frequencies of 0.2-350 MHz. The cost per unit is \$3.25 U.S. This transformer has a turns ratio 1:4. A collector load resistance (R_c) of $500\ \Omega$ at the secondary presents a close match to $50\ \Omega$ at the IF port.

The transformer at the RF port is used to match the source impedance to the mixer and improve the overall noise figure. Typically, a shunt resistor is used at the RF port, which greatly facilitates matching, but at the expense of a higher noise figure. The transformer also provides a differential input which will cancel external noise that may couple onto the RF signal path. An on-chip transformer at the RF port is feasible but will require a space of about $700\mu\text{m} \times 700\mu\text{m}$ to $800\mu\text{m} \times 800\mu\text{m}$. All losses from such a transformer are incorporated into the lossy component (R_{mi}) of the input matching inductor. Ideal behaviour of the transformer is also assumed if we consider that the transformer primary and secondary can be resonant tuned.

The reactance to the differential input of the RF port is initially analysed using the configuration shown in Figure 5.13. RF port matching affects all of the mixer parameters, and therefore the final solution is a compromise of them all. The Libra schematic is shown in Appendix N, Figure N.3. A substantial differential input reactance can be expected at the RF port if we are to use a significant amount of resistive emitter degeneration. Increasing the transistor size will effectively reduce the reactance but will also decrease the real input impedance.

A transistor emitter area of $0.5 \times 240 \mu\text{m}$ is selected for transistors $Q_{3,4}$. A resistive total emitter degeneration of 140Ω ($2R_E$) is chosen in order to keep the noise figure under 10 dB. However, the resistive emitter degeneration is not sufficient to provide the required linearity and inductive degeneration is also necessary. Two 10 nH inductors (L_E) are placed in series with the resistive emitter degeneration $2R_E$.

Figure 5.13: Circuit configuration to determine how to optimize the double-balanced mixer to provide a feasible on-chip solution.

A transformer with a turns ratio of 1:1.5 is subsequently found adequate in providing an input reactance that could be resonated using on-chip inductors. A resulting Libra simulated input impedance of $(16 - j 69)\Omega$ is obtained at the primary input of the RF port transformer. An R - L series network of 12 nH and 34Ω adequately brings the input impedance to 50Ω . The resulting Libra simulated matching performance for the RF, LO and IF ports are shown in Appendix N. The LO-to-RF and LO-to-IF ports are isolated by the transformers.

Note that the symmetry of the transformer response between the inverting and non-inverting ports, which is necessary to achieve good isolation, is ideal in the present simulations and therefore non-realistic isolation is obtained. The second harmonic intercept (2HI) of the double-balanced mixer shown in Figure 5.12 is determined from the power spectrum shown in Figure 5.14 below.

Figure 5.14: Power spectrum density of the output waveform taken at the IF port of the double-balanced mixer shown in Figure 5.12 for an RF power level of -20 dBm and LO power level of 0 dBm.

Reading the signal levels from Figure 5.14 shows that the power of the fundamental (100 MHz) is -16.7 dBm and that the difference between the second harmonic (200 MHz) and the fundamental is 66.9 dBc. According to (5.4), this results in a SHI of 55.2 dB. This is a 36 dB improvement over the double-balanced mixer shown in Figure 5.2. A Libra simulation of the IF input power, for an LO of 0 dBm, is shown below in Figure 5.15, where a conversion gain of 3.4 dB with a P_{1dB} of -7.2 dBm can be observed. By the 10 dB rule, this yields an $IP3_i$ of +2.8 dBm. Using (4.47) and Figure 5.16, the simulated $IP3_i$ is calculated to be +2.6 dBm.

100.00000000
 1.00000000
 100.00000000
 1.00000000
 100.00000000

Figure 5.15: Power response of the double-balanced mixer shown in Figure 5.12. A tone of 915 MHz is applied to the RF port with a tone of 1015 MHz, 0 dBm, applied at the LO port. All ports are 50 Ω match.

100.00000000
 1.00000000
 100.00000000
 1.00000000
 100.00000000

Figure 5.16: Two RF tones of 915 MHz and 916 MHz at a power of -50 dBm are applied to the RF port of the double-balanced mixer shown in Figure 5.12 for an LO power level of 0 dBm.

The noise figure and conversion gain of the advanced silicon bipolar mixer, shown in Figure 5.17, was simulated with Libra, as a function of LO power. The SSB noise figure of the optimized mixer is found to be 9.73 dB for an LO power of 0 dBm.

Figure 5.17: Advanced silicon bipolar double-balanced mixer 50 Ω noise figure and conversion gain vs. LO power. An 915 MHz RF tone of -30 dBm is applied to the RF port.

The optimized mixer presented in this chapter would require a large chip area. If the mixer is to be used as a stand-alone device then the transformer at the RF port could be replaced with an off-chip type. Also the large inductors required for emitter degeneration may not be practical for layout considerations. This approach would seem better suited for a design at 1.9 GHz where inductors are reduced by almost half. The losses involved in the on-chip transformer are also greatly reduced.

Chapter 6

Conclusions and Recommendations

6.1 Conclusions and Summary

The growing number of users of digital radio service has led to the demand for better technology and novel architectures which can be implemented in a monolithic environment in both an efficient and economical manner.

The individual contribution of this thesis was in the area of radio front-end design for the 900 MHz band application. The architectures proposed in this thesis should work equally well, if not better, in the 1.9 GHz frequency range. The circuits designed in this thesis were investigated by simulation only, except for a mixer, used to validate the simulation capability. Both Libra (HP/EEsof Software Inc.) and Hspice (Metasoftware Inc.) software simulators were used to ensure validity of the results. In addition an analytical approach to the designs was also performed to enhance the comprehension of the design parameters involved.

On-chip inductors were extensively used in all designs to ensure that an overall monolithic RF front-end could be achieved. The scattering parameter $\dot{S}_{21}$ of an initial 0.5 nH on-chip inductor high frequency model was found to have little impact in the 900 MHz region and a low-frequency model was used for all simulations.

A common-emitter and a cascode configuration were investigated for the low-noise amplifier. The LNA designs, as proposed in Figure 4.1 and 4.23, provide insight to the trade-offs involved between achieving low power consumption while maintaining reasonable gain and a low noise figure. Both configurations were designed using the same technique where the model parameters provided by Nortel allows the simulators to solve for the required s-parameters. The concept of inductive emitter degeneration was implemented with on-chip inductor to improve noise matching. The use of a resonant on-chip *RLC* network provides an easy means to achieve a real output impedance match. This also gives great flexibility to the IC designer, as the gain of the device can easily be set by proper selection of the output load. Note that there is still a requirement for 50 Ω match at the chip interface since measurements are not easily made for impedance other than 50 Ω due to the test equipment in use. Another advantage to using a shunt inductor to VCC at the output is that it allows for very low voltage operation, hence reducing the power consumption of the circuit. This is a critical factor for hand-held portable communication systems.

The common-emitter configuration, being a single transistor topology, can be operated to VCCs as low as 0.9 Volt. A noise figure of 1.27 dB was attained for a device size of 0.5 X 180 μm . The larger device increases the base-collector capacitance and thus diminishes the effective input/output port isolation, which was found to be -20 dB. The transistor size can always be decreased if a better isolation is required. This will reduce the Miller effect and in light of the noise performance obtained, it would seem more efficient than opting for the cascode configuration.

The base-emitter capacitance also increases with device size, which reduces the input inductance required for resonance. A low value input matching inductor is preferred since its associated losses will degrade the noise figure. The common-emitter LNA was designed with a P_{1dB} of -21.4 dBm and a gain of 13.9 dB, for a bias current of 4 mA. A simulated $IP3_i$ of -4.3 dBm was determined using the output power spectrum under a two-tone simulation.

A 10 dB relationship between the P_{1dB} and $IP3$ normally exists for a well-behaved amplifier. The relationship is derived on the assumption that no reactive feedback is present. Regardless, in practice, this rule seems to hold within a few dBs. It is therefore preferable, for this work, to state the performance of the single tone 1 dB compression point which is verified with both Libra, in the frequency domain, and Hspice, in the time domain. The 1 dB compression point was also found to agree with theoretical expectation.

The cascode configuration offers the advantage of higher input/output port isolation as well as better stability. However, the power consumption required to achieve the same linearity as a single device is increased by a factor of about two due to the inherent requirement to operate from a higher VCC. A bias current of 3 mA from a 1.9 V supply was selected to minimize the power consumption, however a resulting P_{1dB} of -26.4 dBm might be insufficient. The P_{1dB} could have been improved if a higher emitter degeneration inductor had been selected, which would have also brought the input impedance closer to $50\ \Omega$. A noise figure of 1.43 dB and gain of 14.8 dB was simulated for an input transistor size of $0.5 \times 180\ \mu\text{m}$.

A double-balanced mixer, designed with $0.8\ \mu\text{m}$ technology, was provided by Mr. José Macedo. The mixer was simulated with Libra and Hspice and tested using the HP8970 noise figure meter, which also provides gain measurement. The measured and simulated results were found to be in close agreement, which demonstrates the validity of the simulations. A mixer conversion gain of 7.9 dB with a SSB noise figure of 17.3 dB was measured. The $IP3_i$ was measured to be -3.64 dBm. The LO-to-IF isolation was simulated to be 24 dB with an LO-to-RF isolation of 41 dB for an LO power level of 0 dBm. The mixer operates from a 3V power supply for a total power consumption of ~25mW.

The double-balanced mixer was redesigned with an advanced silicon bipolar technology and optimized to take full advantage of the common-emitter LNA dynamic range. The mixer operates from a 3 V power supply and has a total bias current of 6 mA for an 18 mW power consumption. The performance of the mixer was improved from the use of on-chip inductors and transformer. An output off-chip transformer is used to obtain a $50\ \Omega$ match, eliminating the use of a buffer which takes up a significant amount of power. This has allowed to increase the current of the bias sources to 3 mA each. A SSB noise figure of 9.7 dB with a conversion gain of 3.4 dB and $IP3_i$ of +2.6 dBm was simulated with Libra. Use of ideal transformers results in LO-to-IF and LO-to-RF isolation which do not reflect reality. However, other parameters of interest are not so much influenced by the quality of the transformer symmetry.

The combined common-emitter LNA and optimized mixer has an overall power consumption of 22 mW. An overall power gain of 17.3 dB with a third-order input intercept of -21.4 dBm is achieved with an overall noise figure, according to (2.3), of 2.3 dB.

Based on the analytic and simulated results reported in this work, some recommendations for design of an LNA and mixer intended for 900 MHz receiver applications can be made. The transistor size must be carefully selected to minimize noise while providing adequate gain and isolation, particularly for a common-emitter configuration. A cascode LNA provides better isolation at the expense of increased power dissipation. The effects of package parasitics must be included early in the design process and should be an integral part of the overall design. Many concepts common to microwave circuit design, such as impedance-matching, power transfer, and s-parameters device characterization, should be used.

6.2 Recommendations for Future Work on the LNA

The simulated results for the two low-noise amplifiers are promising. The common-emitter LNA appears to be the logical choice for a monolithic implementation where power consumption is the driving criteria. The inductor used for emitter degeneration could be replaced with the inductance from the package lead frame, which is typically 2-4 nH/lead. The lead inductance itself will likely be greater than the required inductor sought. However, multiple lead frames could be connected in parallel to reduce the overall inductance. Selection of which leads to use must be done with care as adjacent leads may have mutual coupling, resulting in a marginal inductance reduction as opposed to what one may expect.

The advantage of using the package lead inductance is that it has very little loss (i.e. high Q) which will further improve the noise figure of the LNA. Part of the output inductor could also be formed in the same manner reducing the required size of the on-chip inductor. What still requires to be done is a study in the non-linear behaviour of the LNA to explain the deviation from the 10 dB rule which normally takes place between the P_{1dB} and $IP3$. The implementation of one of the designs will help shed some light on this matter.

6.3 Recommendations for Future Work on the Double-Balanced Mixer

The double-balanced mixer described in this work was greatly simplified by using an ideal transformer at the RF port. Due to the requirement for high $IP3$, a large emitter degeneration was required, resulting in large on-chip inductors.

The mixer would therefore be very large, and the benefits/cost balance may not be favourable to its implementation. The $IP3$ requirement placed on the mixer could be relaxed if we were to make use of the feedthrough mode of the common-emitter LNA, where the scattering parameter S_{21} is -7.5 dB. A lower $IP3$ requirement would reduce the amount of degeneration needed which would in turn reduce the input matching and inductive emitter degeneration inductors.

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Appendix A

This section contains the assumed models of an advanced silicon bipolar BJT. Note that some of the parameters such as the forward bias (BF) have been turned off and their effects are compensated for through other parameters. As well, the 0.8 μm npn parameters file, as supplied by Nortel to the Canadian Microelectronics Corporation, is included.

Advanced silicon bipolar models

.SUBCKT AP30_60 3 2 1 9

Q 3 2 1 9 MOD

.MODEL MOD NPN

+ IS=9.95E-17 NF=1.0209 VAF=1.62E+01 IKF=6.92E-02

+ BF=1.00E+10 ISE=4.81E-19 NE=1.0029 VAR=0.000E+00 BR=1.0E20

+ TF=4.53E-12 XTF=2.200E+05 ITF=5.142E+01 VTF=1.500E+00 PTF= 20.0

+ RB= 7.83 RBM= 1.77 RE= 1.17 RC= 3.26

+ CJE=1.76E-13 VJE=0.931 MJE=0.445 FC=0.70

+ CJC=1.02E-13 VJC=0.814 MJC=0.250 XCJC=0.352

+ CJS=9.36E-14 VJS=0.702 MJS=0.402

+ EG=1.170 XTB= 1.50 XTI= 3.00

+ TRB1=0.170E-02 TRM1=0.314E-01 TRC1=0.113E-02

+ KF=3.62E-15 AF=2.00E+00

.ENDS AP30_60

*

.SUBCKT AP30_10 3 2 1 9

Q 3 2 1 9 MOD

.MODEL MOD NPN

+ IS=1.66E-17 NF=1.0209 VAF=1.62E+01 IKF=1.16E-02

+ BF=1.00E+10 ISE=8.04E-20 NE=1.0029 VAR=0.000E+00 BR=1.0E20

+ TF=4.53E-12 XTF=2.200E+05 ITF=8.590 VTF=1.500E+00 PTF= 20.0

+ RB= 45.16 RBM= 9.43 RE= 7 RC= 5.18

+ CJE=2.97E-14 VJE=0.931 MJE=0.442 FC=0.70

+ CJC=2.01E-14 VJC=0.81 MJC=0.233 XCJC=0.142

+ CJS=3.73E-14 VJS=0.702 MJS=0.402

+ EG=1.170 XTB= 1.50 XTI= 3.00

+ TRB1=0.170E-02 TRM1=0.102E-01 TRC1=0.113E-02

+ KF=4.65E-12 AF=2.00E+00

.ENDS AP30_10

.SUBCKT AP30_20 3 2 1 9

Q 3 2 1 9 MOD

.MODEL MOD NPN

+ IS=3.32E-17 NF=1.0209 VAF=1.62E+01 IKF=2.31E-02

+ BF=1.00E+10 ISE=1.60E-19 NE=1.0029 VAR=0.000E+00 BR=1.0E20

+ TF=4.53E-12 XTF=2.200E+05 ITF=17.14 VTF=1.500E+00 PTF= 20.0

+ RB= 23.50 RBM= 5.30 RE= 3.50 RC= 2.74

+ CJE= 5.85E-14 VJE=0.931 MJE=0.445 FC=0.70

+ CJC= 3.62E-14 VJC=0.814 MJC=0.238 XCJC=0.155

+ CJS=5.77E-14 VJS=0.702 MJS=0.402

+ EG=1.170 XTB= 1.50 XTI= 3.00

+ TRB1=0.170E-02 TRM1=0.105E-01 TRC1=0.113E-02

+ KF=2.93E-13 AF=2.00E+00

.ENDS AP30_20

*

.SUBCKT AP30_80 3 2 1 9

Q 3 2 1 9 MOD

.MODEL MOD NPN

+ IS=1.33E-16 NF=1.0209 VAF=1.62E+01 IKF=9.23E-02

+ BF=1.00E+10 ISE=6.42E-19 NE=1.0029 VAR=0.000E+00 BR=1.0E20

+ TF=4.53E-12 XTF=2.200E+05 ITF=6.855E+01 VTF=1.500E+00 PTF= 20.0

+ RB= 5.88 RBM= 1.32 RE= 0.88 RC= 3.52

+ CJE=2.34E-13 VJE=0.931 MJE=0.445 FC=0.70

+ CJC=1.35E-13 VJC=0.814 MJC=0.252 XCJC=0.419

+ CJS=1.12E-13 VJS=0.702 MJS=0.402

+ EG=1.170 XTB= 1.50 XTI= 3.00

+ KF=1.14E-15 AF=2.00E+00

.ENDS AP30_80

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* Canadian Microelectronics Corporation
* BiCMOS Technology for Cadence Analog Artist
* Version 0.2
* May, 1994
*
* 0.8-micron BiCMOS HSPICE library for 5V bipolar models
*
* You should have the following options set in order to suppress the
* printing of the model parameters, to make the nominal temperature
* compatible with SPICE, and to make HSPICE use the same device models
* as SPICE 2G.6:
*
* .OPTIONS NOMOD TNOM=27 DCAP=1
*
*****
****
*
*
* VERTICAL NPN:
* CALLING CARD: Q_ C B E S NN5 _____
*
*
.LIB TYPICAL
*
* BIPOLAR PARAMETER LIBRARY
*
* 2X NPN CONTACTED WITH METAL 1
.MODEL BJT_2X NPN
+   IS= 7.07E-18    BF= 1.03E+02    NF= 1.00E+00
+   VAF= 1.18E+02    IKF= 1.01E-02    ISE= 8.47E-18
+   NE= 1.50E+00
+   BR= 1.00E+00    NR= 1.00E+00    VAR= 5.50E+00
+   IKR= 0.00E+00    ISC= 0.00E+00    NC= 2.00E+00
+   RB= 1.44E+02    IRB= 0.00E+00    RBM= 1.44E+02
+   RE= 6.88E+00    RC= 4.64E+01
+   CJE= 2.77E-14    VJE= 8.00E-01    MJE= 2.67E-01
+   TF= 1.06E-11    XTF= 7.83E+02    VTF= 1.35E+00
+   ITF= 1.72E-01    PTF= 2.00E+01
+   CJC= 3.14E-14    VJC= 7.10E-01    MJC= 3.97E-01
+   XCJC= 2.80E-01    TR= 4.00E-09
+   CJS= 5.28E-14    VJS= 3.70E-01    MJS= 1.34E-01
+   XTB= 1.62E+00    EG= 1.11E+00    XTI= 5.82E+00
+   KF= 2.78E-10    AF= 1.86E+00    FC= 8.00E-01
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* 2X NPN CONTACTED WITH METAL 1 AND METAL 2
+   IS= 7.07E-18   BF= 1.03E+02   NF= 1.00E+00
+   VAF= 1.18E+02   IKF= 1.01E-02   ISE= 8.47E-18
+   NE= 1.50E+00
+   BR= 1.00E+00   NR= 1.00E+00   VAR= 5.50E+00
+   IKR= 0.00E+00   ISC= 0.00E+00   NC= 2.00E+00
+   RB= 1.44E+02   IRB= 0.00E+00   RBM= 1.44E+02
+   RE= 6.88E+00   RC= 4.64E+01
+   CJE= 2.77E-14   VJE= 8.00E-01   MJE= 2.67E-01
+   TF= 1.06E-11   XTF= 7.83E+02   VTF= 1.35E+00
+   ITF= 1.72E-01   PTF= 2.00E+01
+   CJC= 3.14E-14   VJC= 7.10E-01   MJC= 3.97E-01
+   XCJC= 2.80E-01   TR= 4.00E-09
+   CJS= 5.28E-14   VJS= 3.70E-01   MJS= 1.34E-01
+   XTB= 1.62E+00   EG= 1.11E+00   XTI= 5.82E+00
+   KF= 2.78E-10   AF= 1.86E+00   FC= 8.00E-01

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* 4X NPN CONTACTED WITH METAL 1 AND 2
+   IS= 1.50E-17   BF= 1.04E+02   NF= 1.00E+00
+   VAF= 1.18E+02   IKF= 1.97E-02   ISE= 1.63E-17
+   NE= 1.50E+00
+   BR= 1.00E+00   NR= 1.00E+00   VAR= 5.50E+00
+   IKR= 0.00E+00   ISC= 0.00E+00   NC= 2.00E+00
+   RB= 8.32E+01   IRB= 0.00E+00   RBM= 8.32E+01
+   RE= 4.44E+00   RC= 2.56E+01
+   CJE= 5.30E-14   VJE= 8.00E-01   MJE= 2.67E-01
+   TF= 9.89E-12   XTF= 8.77E+02   VTF= 1.45E+00
+   ITF= 3.14E-01   PTF= 2.00E+01
+   CJC= 5.34E-14   VJC= 7.10E-01   MJC= 3.97E-01
+   XCJC= 2.80E-01   TR= 4.00E-09
+   CJS= 8.00E-14   VJS= 3.70E-01   MJS= 1.34E-01
+   XTB= 1.62E+00   EG= 1.11E+00   XTI= 5.82E+00
+   KF= 1.80E-11   AF= 1.67E+00   FC= 8.00E-01

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```

**
* 15X NPN CONTACTED WITH METAL 1,2 AND 3
+   IS= 5.78E-17   BF= 1.04E+02   NF= 1.00E+00
+   VAF= 1.18E+02   IKF= 7.30E-02   ISE= 5.99E-17
+   NE= 1.50E+00
+   BR= 1.00E+00   NR= 1.00E+00   VAR= 5.50E+00
+   IKR= 0.00E+00   ISC= 0.00E+00   NC= 2.00E+00
+   RB= 2.52E+01   IRB= 0.00E+00   RBM= 2.52E+01
+   RE= 1.74E+00   RC= 7.25E+00
+   CJE= 1.95E-13   VJE= 8.00E-01   MJE= 2.67E-01
+   TF= 8.60E-12   XTF= 1.04E+03   VTF= 1.62E+00
+   ITF= 9.94E-01   PTF= 2.00E+01
+   CJC= 1.32E-13   VJC= 7.10E-01   MJC= 3.97E-01
+   XCJC= 2.80E-01   TR= 4.00E-09
+   CJS= 1.86E-13   VJS= 3.70E-01   MJS= 1.34E-01
+   XTB= 1.62E+00   EG= 1.11E+00   XTI= 5.82E+00
+   KF= 9.82E-14   AF= 1.36E+00   FC= 8.00E-01
**
**
**

```

.ENDL TYPICAL

as the configuration test file for analysis of their performance.

Appendix B

This section contains the Hspice configuration file relating to the circuit schematic shown in Figure 3.2 of chapter 3.

* AP30_80 @ 915MHz, 0.5 micron technology

.OPTIONS NOMOD BRIEF TNOM=27 DCAP=1

.OPTION INGOLD=1

.OPTION ABSVAR=0.025 DVDT RELVAR=0.05 NEWTOL

.OPT POST=2 ** hsplot plot format

.include '/home/frec/technology/NEWTECH'

vcc 7 0 dc=1.0

* define input signal source

vin 1 0 0.8185 ac=1

*

* C B E SUB

xq1 2 1 0 0 AP30_80

xq2 2 1 0 0 AP30_80

xq3 2 1 0 0 AP30_80

co out 2 10nF

Ro out 0 50MEG

* DC bias

L2 2 7 1000nH

*

.ac poi 1 915e06

.op

.noise v(out) vin 1

.end

Appendix C

This section contains the Libra schematic and test bench files utilized to determine the elements of the resonant output network as well as the Hspice configuration and data files to determine the input impedance at the input terminal of the transistor.

*Michel's LNA @ 915MHz, 0.5 micron technology
* 915Mhz with (2) AP30_80 in parallel,@ 2mA each

```
.OPTIONS NOMOD BRIEF TNOM=27 DCAP=1
.OPTION INGOLD=1
.OPTION ABSVAR=0.025 DVDT RELVAR=0.05 NEWTOL
.OPT POST=2 ** hsplot plot format
.include '/home/frec/technology/NEWTECH'
vcc 7 0 dc=1.0
* define input signal source
vin src 0 0.808 ac=1
rs src 1 0
*
* C B E SUB
xq1 2 1 3 0 AP30_80
xq2 2 1 3 0 AP30_80
Lc 2 4 5nH
cL 2 6 3pF
rsc 6 7 2.6
rsl 4 7 5.75
rL 2 7 140
Le 3 5 1nH
* on-chip inductor,Q assumed to be 5
rse 5 0 1.44
co out 2 10nF
* input matching network
* TBD
Ro 0 out 50MEG
*
.ac poi 1 915e06
.op
.net v(out) vin rout=50 rin=50
.print ac ZIN(R) ZIN(I)
*
*
.end
```


*michel's Ina @ 915mhz, 0.5 micron technology
 * 915mhz with (2) AP30_80 in parallel, @ 2ma each

.options nomod brief tnom=27 dcap=1
 warning 0:rs resistance limited to 1.000E-05
 total voltage source power dissipation= 3.897e-03 watts

**** bipolar junction transistors

subckt	xq1	xq2
element	1:q	2:q
model	1:mod	2:mod
ib	1.627e-05	1.627e-05
ic	1.935e-03	1.935e-03
vbe	0.8024	0.8024
vce	0.9730	0.9730
vbc	-0.1706	-0.1706
vs	-0.9718	-0.9718
power	1.896e-03	1.896e-03
betad	118.9703	118.9703
gm	7.171e-02	7.171e-02
rpi	1.594e+03	1.594e+03
rx	5.8325	5.8325
ro	8.456e+03	8.456e+03
cpi	8.202e-13	8.202e-13
cmu	5.401e-14	5.401e-14
cbx	7.489e-14	7.489e-14
ccs	7.898e-14	7.898e-14
betaac	114.3550	114.3550
ft	1.202e+10	1.202e+10

***** ac analysis tnom= 27.000 temp= 27.000

x

freq	zin	zin
	real	imag
9.1500e+08	42.8647	-77.1741

Appendix D

This section contains the Libra schematic for the common-emitter LNA.

Figure D.1: Libra schematic view of the common-emitter LNA at 4 mA. Vcc is one volt and both input and output ports are 50 Ω matched.

Appendix E

This section contains the Libra generic test bench for d.c, small-signal, 1-tone and 2-tones analyses for the low-noise amplifiers.

Figure E.1: Libra test bench for dc analysis

Figure E.2: Libra test bench for small-signal analysis.

Figure E.3: Libra test bench for single tone harmonic balance analysis

Figure E.4: Libra test bench for two tone harmonic balance analysis

Appendix F

This section contains the Hspice configuration file and the linear data and noise analysis data files for the common-emitter LNA.

*Michel's LNA @ 915MHz, 0.5 micron technology
* 915Mhz with (2) AP30_80 in parallel,@ 2mA each

.OPTIONS NOMOD BRIEF TNOM=27 DCAP=1
.OPTION INGOLD=1
.OPTION ABSVAR=0.025 DVDT RELVAR=0.05 NEWTOL
.OPT POST=2 ** hspplot plot format

.include '/home/frec/technology/NEWTECH'
vcc 7 0 dc=1.0
* define input signal source
*dc value is increased to 0.8106 during noise analysis to keep $I_E = 4\text{mA}$
vin src 0 0.808 ac=1
* For noise analysis, make $r_s = 50$
rs src in 0
*
* C B E SUB
xq1 2 1 3 0 AP30_80
xq2 2 1 3 0 AP30_80
Lc 2 4 5nH
cL 2 6 3pF
rsc 6 7 2.6
rsl 4 7 5.75
rL 2 7 140
Le 3 5 1nH
* on-chip inductor, Q assumed to be 5
rse 5 0 1.44
co out 2 10nF
* input matching network
Lmi in 8 16nH
* Q of 50 is assumed
rLmi 8 1 1.84
Cmi in 0 1.4pF
* no output matching network required
* For noise analysis, make $R_o = 50$
Ro 0 out 50MEG
*
.ac lin 100 800e06 1200e06
.op
*.noise v(out) vin 1 * this line is added during noise analysis
* The next two lines are removed during noise analysis
.net v(out) vin rout=50 rin=50
.print ac S11(M) S11(P) S22(M) S22(P) S21(db) ZIN(R) ZIN(I) ZOUT(R) ZOUT(I)
*
.end

*michel's Ina @ 915mhz, 0.5 micron technology
 * 915mhz with (2) AP30_80 in parallel,@ 2ma each

.options nomod brief tnom=27 dcap=1

***** H S P I C E -- 95.2 (950213) 17:11:47 96/01/04 sun4
 ***** operating point information tnom= 27.000 temp= 27.000

**** voltage sources

subckt
 element 0:vcc 0:vin
 volts 1.0000 0.8080
 current -3.864e-03 -3.247e-05
 power 3.864e-03 2.624e-05

total voltage source power dissipation= 3.890e-03 watts

**** resistors

subckt
 element 0:rs 0:rsc 0:rsi 0:rl 0:rse 0:rlmi
 r value 1.000e-05 2.6000 5.7500 140.0000 1.4400 1.8400
 v drop 3.247e-10 0. -2.134e-02 -2.134e-02 5.610e-03 5.975e-05
 current 3.247e-05 0. -3.711e-03 -1.524e-04 3.896e-03 3.247e-05
 power 1.054e-14 0. 7.919e-05 3.253e-06 2.186e-05 1.940e-09

subckt
 element 0:ro
 r value 5.000e+07
 v drop 0.
 current 0.
 power 0.

**** bipolar junction transistors

```

subckt  xq1    xq2
element 1:q    2:q
model  1:mod   2:mod
ib      1.624e-05 1.624e-05
ic      1.932e-03 1.932e-03
vbe      0.8023  0.8023
vce      0.9731  0.9731
vbc     -0.1707  -0.1707
vs     -0.9719  -0.9719
power   1.893e-03 1.893e-03
betad   118.9791 118.9791
gm       7.159e-02 7.159e-02
rpi     1.597e+03 1.597e+03
rx        5.8327  5.8327
ro     8.470e+03 8.470e+03
cpi     8.196e-13 8.196e-13
cmu     5.401e-14 5.401e-14
cbx     7.489e-14 7.489e-14
ccs     7.898e-14 7.898e-14
betaac  114.3673 114.3673
ft     1.201e+10 1.201e+10

```

***** ac analysis tnom= 27.000 temp= 27.000

freq	s11 mag	s11 phase	s22 mag	s22 phase	
9.1500e+08	9.733e-03	117.6510	3.691e-02	70.9207	

freq	s21 mag	s21 phase	s12 mag	s12 phase	
9.1500e+08	4.7742	85.8018	7.356e-02	32.3902	

freq	s21 db	zin real	zin imag	zout real	
9.1500e+08	13.5780	49.5430	0.8543	51.0951	

freq	zout imag	s12 db	
9.1500e+08	3.5690	-22.6675	

***** job concluded

*michel's Ina @ 915mhz, 0.5 micron technology
 * 915mhz with (2) AP30_80 in parallel,@ 2ma each

***** noise analysis tnom= 27.000 temp= 27.000

frequency = 9.150e+08 hz

**** resistor squared noise voltages (sq v/hz)

element	0:rs	0:rsc	0:rsi	0:rl	0:rse
total	4.769e-18	8.155e-21	7.069e-20	7.546e-20	1.155e-19
rx	119.9400	1.1310	4.9519	25.2459	3.1681

element	0:rlmi	0:ro
total	1.930e-19	2.113e-19
rx	4.6292	25.2453

**** transistor squared noise voltages (sq v/hz)

element	1:q	2:q
rb	1.310e-19	1.310e-19
rc	2.307e-21	2.307e-21
re	1.765e-20	1.765e-20
ib	3.214e-19	3.214e-19
ic	8.745e-20	8.745e-20
fn	0.	0.
total	5.599e-19	5.599e-19

**** total output noise voltage = 6.563e-18 sq v/hz
 = 2.562e-09 v/rt hz

transfer function value:

v(out)/vin = 2.3988

equivalent input noise at vin = 1.068e-09 /rt hz

Figure F.1: Hspice, Vertical Transistor, BJT AC Noise Analysis.

Appendix G

This section contains the Libra schematic files for the common-emitter LNA with various matching networks.

Figure G.1: Libra schematic of the common-emitter LNA with *RLC* output resonant network matched to 75Ω .

Appendix H

This section contains the figures related to the sensitivity analysis described in section 4.1.9. The sensitivity analysis was performed with Hspice.

Figure H.1: Common-emitter LNA S_{21} vs. Temperature at $f_o = 915$ MHz.

Figure H.2: Common-emitter LNA 50 Ω Noise Figure Temperature at $f_o = 915$ MHz.

Figure H.3: Common-emitter LNA VSWR vs. Temperature at $f_0 = 915$ MHz.

Figure H.4: Common-emitter LNA S₂₁ vs. Frequency and V_{cc}.

Appendix I

This section contains the Libra schematic file for the cascode LNA as well as the schematic view of the high-frequency lumped-model of Z_E shown in Figure 4.23 of Chapter 4.

Figure I.1: Libra schematic view of the cascode LNA at 3 mA. Vcc is 1.9 volt and both input and output ports are 50 Ω matched.

Figure I.2: High-frequency lumped model for Z_E shown in Figure 4.23.

Appendix J

This section contains the Hspice configuration file and the linear data and noise analysis data files for the cascode LNA.

File configuration for the cascode LNA.

.OPTIONS NOMOD BRIEF TNOM=27

.OPTION INGOLD=1

.OPTION ABSVAR=0.025 DVDT RELVAR=0.05 NEWTOL DCAP=1

.OPT POST=2 ** hsplot plot format

.include '/home/frec/technology/NEWTECH'

vcc 10 0 dc=1.9

* define input signal source

* The vbe must be increased to 0.799 during noise analysis to keep $I_E = 3\text{mA}$.

vin src 0 0.798 ac=1

*sin(0 0.200 915e06 0 0) * for transient analysis

rs src 1 0 * set to 50 during noise analysis

*

* C B E SUB

xq1 2 1 3 0 AP30_80

xq2 2 1 3 0 AP30_80

xq3 6 5 2 0 AP30_80

Cd 5 11 20pF

rCd 11 0 0.6

rbb 10 5 1K

Lc 10 7 5nH

*on-chip inductor, Q is assumed to be 5

rLc 7 6 5.75

cL 8 10 5.6pF

rcL 8 6 2.6

rL 6 10 95

Le 3 4 0.5nH

* on-chip inductor, Q assumed to be 5

rse 4 0 1.0

co out 6 10nF

* input matching network, once installed, rs is connected between nodes src and in

*Lmi 9 in 21nH

* Q of 50 is assumed

*rLmi 9 1 2.4

*Cmi in 0 1.7pF

* no output matching network required

Ro 0 out 50MEG * set to 50 during noise analysis

.ac poi 1 915e06

.op

*.noise v(out) vin 1

.net v(out) vin rout=50 rin=50

.print ac S11(M) S11(P) S21(M) S21(P) S21(db) S12(db) S22(M) S22(P) S12(M)

S12(P) ZIN(R) ZIN(I) ZOUT(R) ZOUT(I)

**.tran .01ns 249.96ns start=245.03ns * used during transient analysis

*.print tran v(out)

.end

***** operating point information tnom= 27.000 temp= 27.000

***** operating point status is all simulation time is 0.

node =voltage node =voltage node =voltage

+0:1 = 0.7980 0:2 = 1.0590 0:3 = 3.025e-03

+0:4 = 3.025e-03 0:5 = 1.8743 0:6 = 1.8839

+0:7 = 1.9000 0:8 = 1.8839 0:10 = 1.9000

+0:11 = 0. 0:out = 0. 0:src = 0.7980

total voltage source power dissipation= 5.720e-03 watts

**** bipolar junction transistors

subckt xq1 xq2 xq3

element 1:q 2:q 3:q

model 1:mod 2:mod 3:mod

ib 1.242e-05 1.242e-05 2.575e-05

ic 1.500e-03 1.500e-03 2.974e-03

vbe 0.7950 0.7950 0.8153

vce 1.0560 1.0560 0.8249

vbc -0.2610 -0.2610 -9.620e-03

vs -1.0537 -1.0537 -1.8734

power 1.594e-03 1.594e-03 2.474e-03

betad 120.7714 120.7714 115.5258

gm 5.584e-02 5.584e-02 0.1090

rpi 2.088e+03 2.088e+03 1.007e+03

rx 5.8791 5.8791 5.7374

ro 1.097e+04 1.097e+04 5.446e+03

cpi 7.437e-13 7.437e-13 9.978e-13

cmu 5.280e-14 5.280e-14 5.658e-14

cbx 7.322e-14 7.322e-14 7.846e-14

ccs 7.748e-14 7.748e-14 6.642e-14

betaac 116.6124 116.6124 109.8681

ft 1.021e+10 1.021e+10 1.532e+10

***** ac analysis tnom= 27.000 temp= 27.000

freq	s11 mag	s11 phase	s21 mag	s21 phase
9.1500e+08	0.7490	-52.2396	3.6440	134.4798

f: eq	s21 db	s12 db	s22 mag	s22 phase
9.1500e+08	11.2316	-66.1112	6.656e-03	73.6605

freq	s12 mag	s12 phase	zin real	zin imag
9.1500e+08	4.948e-04	81.6151	34.0966	-91.9954

freq	zout real	zout imag
9.1500e+08	50.1835	0.6411

***** job concluded

***** ac analysis with both ports match to 50 ohms, with matching networks
 ***** determined with Libra

freq	s11 mag	s11 phase	s21 mag	s21 phase
9.1500e+08	0.1265	54.7299	5.2693	54.1946

freq	s21 db	s12 db	s22 mag	s22 phase
9.1500e+08	14.4351	-62.8953	3.723e-03	71.8447

freq	s12 mag	s12 phase	zin real	zin imag
9.1500e+08	7.165e-04	1.3099	56.5592	11.8771

freq	zout real	zout imag
9.1500e+08	50.1149	0.3546

***** job concluded

***** noise analysis tnom= 27.000 temp= 27.000

frequency = 9.150e+08 hz

**** resistor squared noise voltages (sq v/hz)

element	0:rs	0:rcd	0:rbb	0:rlc	0:rci
total	5.719e-18	2.442e-21	3.093e-22	6.948e-20	2.779e-20
rx	131.3466	0.2973	4.3196	4.9094	2.0878

element	0:rl	0:rse	0:rlmi	0:ro
total	1.093e-19	1.013e-19	3.401e-19	2.077e-19
rx	25.0294	2.4726	7.0172	25.0294

**** transistor squared noise voltages (sq v/hz)

element	1:q	2:q	3:q
rb	1.722e-19	1.722e-19	2.448e-20
rc	3.892e-21	3.892e-21	6.479e-23
re	2.229e-20	2.229e-20	3.892e-21
ib	4.347e-19	4.347e-19	6.342e-21
ic	1.039e-19	1.039e-19	3.676e-20
fn	0.	0.	0.
total	7.370e-19	7.370e-19	7.153e-20

**** total output noise voltage = 8.123e-18 sq v/hz
 = 2.850e-09 v/rt hz

transfer function value:

v(out)/vin = 2.6269

equivalent input noise at vin = 1.085e-09 /rt hz

Appendix K

This section contains the derivation of the balanced modulator transfer function shown in Figure 5.1.

Referring to Figure 5.1, we can see that $v_o^+ = R_L(I_1+I_3)$ and $v_o^- = R_L(I_2+I_4)$

Consequently,

$$v_o = v_o^+ - v_o^- = R_L [(I_1 + I_3) - (I_2 + I_4)] = R_L [(I_1 - I_2) + (I_3 - I_4)] \quad (1)$$

The currents in the respective branches are related to the total bias current levels as,

$$\frac{I_1}{I_1 + I_2} = \frac{1}{1 + (I_2/I_1)} \quad (2)$$

and

$$\frac{I_2}{I_1 + I_2} = \frac{I_2/I_1}{1 + (I_2/I_1)} \quad (3)$$

where

$$I_2 = I_S e^{v_{LO}/V_{TH}} \text{ and } I_1 = I_S e^{v_{LO}^*/V_{TH}} \quad (4)$$

Therefore

$$\frac{I_2}{I_1} = e^{-v_{LO}/V_{TH}} \quad (5)$$

and

$$\frac{I_1}{I_1 + I_2} = \frac{1}{1 + e^{-v_{LO}/V_{TH}}} \quad (6)$$

and

$$\frac{I_2}{I_1 + I_2} = \frac{e^{-v_{LO}/V_{TH}}}{1 + e^{-v_{LO}/V_{TH}}} \quad (7)$$

solving for I_1 - I_2 yields

$$I_1 - I_2 = (I_1 + I_2) \left[\frac{1 - e^{-v_{LO}/V_{TH}}}{1 + e^{-v_{LO}/V_{TH}}} \right] \quad (8)$$

Recall that the hyperbolic function is given as,

$$\tanh x = \frac{e^x - e^{-x}}{e^x + e^{-x}} = \frac{1 - e^{-2x}}{1 + e^{-2x}} \quad (9)$$

then

$$I_1 - I_2 = (I_1 + I_2) \tanh\left(\frac{v_{LO}}{2V_{TH}}\right) = I_S \tanh\left(\frac{v_{LO}}{2V_{TH}}\right) \quad (10)$$

Similarly

$$\frac{I_3}{I_3 + I_4} = \frac{I_3/I_4}{1 + (I_3/I_4)} \quad (11)$$

and

$$\frac{I_4}{I_3 + I_4} = \frac{1}{1 + (I_3/I_4)} \quad (12)$$

where

$$I_4 = I_S e^{v_{LO}/V_{TH}} \text{ and } I_3 = I_S e^{-v_{LO}/V_{TH}} \quad (13)$$

therefore

$$\frac{I_3}{I_4} = e^{-v_{LO}/V_{TH}} \quad (14)$$

and

$$\frac{I_4}{I_3 + I_4} = \frac{1}{e^{-v_{LO}/V_{TH}} + 1} \quad (15)$$

and

$$\frac{I_3}{I_3 + I_4} = \frac{e^{-v_{LO}/V_{TH}}}{e^{-v_{LO}/V_{TH}} + 1} \quad (16)$$

so that,

$$I_3 - I_4 = (I_3 + I_4) \left[\frac{e^{-v_{LO}/V_{TH}} - 1}{1 + e^{-v_{LO}/V_{TH}}} \right] = -(I_3 + I_4) \left[\frac{1 - e^{-v_{LO}/V_{TH}}}{1 + e^{-v_{LO}/V_{TH}}} \right] \quad (17)$$

or,

$$I_3 - I_4 = -I_6 \tanh\left(\frac{v_{LO}}{2V_{TH}}\right) \quad (18)$$

therefore,

$$v_o = R_L (I_5 - I_6) \tanh\left(\frac{v_{LO}}{2V_{TH}}\right) \quad (19)$$

for $I_5 R_E \gg V_{TH}$ and $I_6 R_E \gg V_{TH}$, i.e v_{be} is very small compared to v_{RE} and the current is for most practicality determined by v_E/R_E , then

$$I_5 - I_6 = \frac{v_{RF}^+}{R_E} - \frac{v_{RF}^-}{R_E} = \frac{v_{RF}}{R_E} \quad (20)$$

hence the output waveform is given as

$$v_o = \frac{R_L}{R_E} v_{RF} \tanh\left(\frac{v_{LO}}{2V_{TH}}\right) \quad (21)$$

For modulator applications, the local oscillator input are usually driven by a high amplitude squarewave. If $(v_{LO}/2) \gg V_{TH}$ then,

$$\tanh\left(\frac{v_{LO}}{2V_{TH}}\right) \approx \pm 1 \quad (22)$$

As a result the upper transistors act as fast switches effectively “chopping” the modulating input at the frequency of the LO signal to produce an output waveform of the form,

$$v_o(t) = \frac{R_L}{R_E} v_{RF}(t) S_1(t) \quad (23)$$

where $S_1(t)$ is given as

$$S_1(t) = \sum_{n=1}^{\infty} A_n \cos n\omega_{LO}t \quad (24)$$

where

$$A_n = \frac{\sin\left(\frac{n\pi}{2}\right)}{\frac{n\pi}{4}} \quad (25)$$

So the output of the modulator then becomes,

$$v_o(t) = K \sum_{n=1}^{\infty} A_n v_{RF} \cos \omega_{RF} t \cos n \omega_{LO} t \quad (26)$$

or

$$v_o(t) = K \sum_{n=1}^{\infty} \frac{A_n v_{RF}}{2} [\cos (\omega_{RF} + n \omega_{LO}) t + \cos (\omega_{RF} - n \omega_{LO}) t] \quad (27)$$

with $K = R_L/R_E$.

One of the issues of interest is to investigate the drawback of feeding the modulator single-ended as opposed to differential.

The non-linear input, the LO, can be analysed repeating the steps above but with v_{LO} input grounded. Then equation (27) becomes,

$$I_2 = I_S e^{-v_{LO}/2V_{TH}} \text{ and } I_1 = I_S e^{v_{LO}/2V_{TH}} \quad (28)$$

and

$$\frac{I_2}{I_1} = e^{-v_{LO}/V_{TH}} \quad (29)$$

So under those given conditions, it appears that no effect is seen from being single-ended.

Appendix L

This section contains the Libra schematic file of the double-balanced mixer shown in Figure 5.2 as well as the Hspice configuration file for the transient analysis.

Figure L.1: Libra schematic file of the double-balanced mixer shown in Figure 5.2.

Hspice configuration file for the transient analysis of the double-balanced mixer shown in Figure 5.2.

```
** Transient Analysis
.OPTIONS NOMOD BRIEF TNOM=27 DCAP=1
.OPTION INGOLD=1
.OPTION ABSVAR=0.025 DVDT RELVAR=0.05 NEWTOL
.OPT POST=2 ** hspice plot format

.lib '/home/frec/technology/typbipol' TYPICAL
* DC Bias
vcc 20 0 dc=3.0 * VCC
vb1 21 0 dc=2.8 * VLO
Lc1 10 21 1000nH * RF choke
vb2 22 0 dc=1.8 * VRF
Lc2 6 22 1000nH * RF choke
vbb1 30 0 dc=0.915 * Bias for Iref

* define input signal source
** LO input
vLO src1 0 sin(0 0.316 1015e06 0 0) * 0 dBm in 50 Ohms
rs1 src1 in1 50
c1 in1 in2 10nF
L1 in2 10 2nH
** RF input
vRF src2 0 sin(0 0.056 915e06 0 0) * -15 dBm in 50 Ohms
rs2 src2 in3 50
c2 in3 in4 10nF
L2 in4 6 2nH
*
* C B E SUB
Q_1a 2 1 4 0 T4X
Q_1b 2 1 4 0 T4X
Q_2a 3 1 5 0 T4X
Q_2b 3 1 5 0 T4X
Q_3 8 6 2 0 T15X
Q_4 9 7 3 0 T15X
Q_5 12 10 8 0 T4X
Q_6 11 13 8 0 T4X
Q_7 12 13 9 0 T4X
Q_8 11 10 9 0 T4X
Q_9 20 11 14 0 T15X
Q_10 14 15 16 0 T15X
Q_11 15 15 17 0 T4X
R1 4 0 100
```

R2 5 0 100
R3a 2 300 25
R3b 300 3 25
R4a 6 18 50
R4b 18 7 50
Lb1 18 180 1.5nH
Lb2 7 180 1.5nH
Cd1 180 0 330pF
R5a 10 19 50
R5b 19 13 50
Lb3 19 190 1.5nH
Lb4 13 190 1.5nH
Cd2 190 0 330pF
R6 12 20 500
R7 11 20 500
R8 17 0 500
R9 15 20 1.5K
R10 16 0 100
Rb 30 1 0
Lbo 14 140 2nH
Co 140 out 10nF
Ro out 0 50

.op

.tran .05ns 60ns start=40ns

.print tran v(out)

*

.end

Appendix M

This section contains the **Libra** generic test bench for the harmonic balance 1-tone and 2-tones analyses of the mixers.

Figure M.1: Single-tone harmonic test bench for mixers.

Figure M.2: Two tones harmonic balance Libra test bench to measure $IP3$ of mixers.

Appendix N

This section contains the Libra schematic of the double-balanced mixer topology shown in Figure 5.2 but implemented in an advanced silicon bipolar technology, and the Libra schematic of the optimized double-balanced mixer shown in Figure 5.12. The LO,RF and IF ports match performance of this mixer is also included.

Figure N.1: Double-balanced mixer topology of Figure 5.2, implemented with an advanced silicon bipolar technology.

Figure N.2: Libra schematic file of the double-balanced mixer shown in Figure 5.12.

☐ Mixer_L2_10
☐ S11
☐ Mixer_Optimized
☐ S11

Figure N.3: LO port S_{11} scattering parameter for the mixer shown in Figure N.2. A 50 Ω match can be observed in the vicinity of the LO frequency of 1015 MHz.

END

2 1 / 1 1 - 9 6

FIN