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**INVESTIGATION OF TAPER AND FORWARD-FEED
IN GaAs MMIC DISTRIBUTED AMPLIFIERS**

by

Michael Ross, B. Eng.

A thesis
submitted to the
Faculty of Graduate Studies and Research
in partial fulfilment of the requirements
for the degree of
Master of Engineering
in
Electrical Engineering

Ottawa-Carleton Institute for Electrical Engineering
Department of Electronics
Faculty of Engineering
Carleton University

June 1987

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ISBN 0-315-39434-X

The undersigned recommend to the Faculty of Graduate Studies and Research, the acceptance of the thesis

**"Investigation of Taper and Forward-Feed
in GaAs MMIC Distributed Amplifiers"**

submitted by Michael Ross, B. Eng., in partial fulfilment of the requirements for the degree of Master of Engineering in Electrical Engineering.

Professor R. G. Harrison,
Thesis Supervisor

Professor M. A. Copeland,
Chairman

June 1987

ABSTRACT

A procedure for designing an ultra-broadband distributed amplifier is established. The amplifier operates on the principle of using the input and output capacitances of transistors, together with inductive elements to form the shunt and series elements of artificial low-pass transmission lines, respectively. These transmission lines are coupled with the transconductances of the field-effect transistors (FETs) and offer unprecedented broad-bandwidth capabilities in several ways.

Computer-aided-design (CAD) techniques are used. These aid the design of the 'artificial' gate and drain transmission lines. The SUPER-COMPACT and MAC-SYMA programs are found to be invaluable tools in the analysis and optimization of the distributed amplifier.

A 1-12-GHz distributed amplifier based on GaAs monolithic microwave integrated circuit (MMIC) technology is designed, fabricated, and measured to verify and validate the design procedure. The performance is achieved by incorporating the principle of forward-feed. Experimental and simulated results are found to be in very good agreement.

ACKNOWLEDGEMENTS

I would like to express my gratitude to my thesis supervisor, Prof. R. G. Harrison, for his continuous support, guidance and involvement during the course of this work. His help in creating an arrangement with Bell-Northern Research in which research work could be carried out with them is much appreciated.

At Bell-Northern Research, I am indebted to Dr. W. D. Westwood and Dr. R. R. Jackson, for giving me the opportunity to conduct advanced research there and to use the available research facilities. I would like to express my gratitude to Dr. R. K. Surridge for his continuous help, support, and especially for suggesting the research topic. Special thanks go to Dr. J. E. Sitch, for our many discussions on various topics, and to Mr. Gordon Rabjohn, who helped with the testing of the devices.

At Northern Telecom, I would like to thank Mr. Ian Fewe for supplying the optical photographs of the chip.

Financial support was provided by Carleton University in the form of a Research Assistantship, by the Natural Sciences and Engineering Research Council of Canada in the form of a Postgraduate Scholarship, and by Bell-Northern Research in the form of a Research Grant and is gratefully acknowledged.

I wish to thank my parents Mrs. Florence Ross and Mr. Patrick Ross and a very dear friend Ms. Louise Dorais, for their encouragement during the course of this work. Mr. Didier DiCamillo also deserves credit for his assistance in typing.

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LIST OF PRINCIPAL SYMBOLS

A	Magnitude of voltage gain
A_0	dc voltage gain
$\bar{A}_0$	Process-independent normalized dc gain
A_{0max}	Maximum dc voltage gain
A_I	Input voltage
A_{Ii}	Input voltage of the i-th port
A_N	Normalized voltage gain
A_O	Output voltage
A_{Oi}	Output voltage of i-th port
A_d	Drain line attenuation per section
A_g	Gate line attenuation per section
a	Gate line characteristic parameter
α_d	Drain line normalized loss
α_g	Gate line normalized loss
B	Width of square cross-section conductor
b	Drain line characteristic parameter
C	Height of square cross-section conductor
C	Shunt-arm capacitance
C_{DT}	Capacitance of drain line termination
C_d	Effective drain line shunt capacitance
C_{dc}	Dipole layer capacitance
C_{dg}	Drain-gate capacitance of space-charge region
C_{ds}	Substrate capacitance
C_{fj}	Forward-feed capacitance ($j=1,3$)
C_{gs}	Gate-source capacitance of space-charge region
C_{geff}	Total effective gate line shunt capacitance per section

C_p	Shunt capacitance
DA	Distributed amplifier
ΔV_{in}	maximum gate line input voltage swing
d	Distance between conductors
E_{pk}	Electric field at which electron drift velocity peaks
FF	Forward-feed
f	Frequency
f_{1dB}	1-dB roll-off frequency
f_T	Unity current-gain frequency
f_c	Cut-off frequency
f_{max}	Maximum frequency of oscillation
G	Gain
GBW	Gain-bandwidth product
$\bar{G}_{BW}$	Normalized gain-bandwidth product
Γ	FET voltage transfer
γ	Propagation function
γ_H	Half-section propagation function
γ_d	Drain line propagation function per section
γ_g	Gate line propagation function per section
g_m	Transconductance
g'_m	Extrinsic transconductance
HF	High frequency
I_{di}	FET transconductance current
I_{Dss}	Maximum FET drain saturated current
I_{Dsat}	FET drain saturated current
K^j	Proportionality parameters ($j=1,14$)
k_{Rds}	FET output resistance constant independent of FET width
k_{Ri}	FET input resistance constant independent of FET width

k_c	FET capacitance constant independent of FET width
k_{gc}	Transconductance to gate capacitance ratio
k_{gm}	Transconductance constant independent of FET width
k_n	FET Loss ratio independent of FET width
k_w	Drain line characteristic impedance normalized loss ratio independent of FET width
L	Series-arm inductance
L_{SC}^j	Inductance values obtained from SUPER-COMPACT ($j=1,14$)
L_d	Drain line series-arms inductances
L_{dj}	Drain line inductance ($j=1,5$)
L_g	Gate line series-arms inductances
L_{gj}	Gate line inductance ($j=1,5$)
L_{int}^j	Inductances of the interconnects ($j=1,14$)
L_m	Effective mutual-inductance between the spiral inductor and its interconnect
L_s	Source terminal inductance
L_{sj}	Series-drain inductance ($j=1,4$)
L_{spiral}^j	Inductances of the laid-out spiral inductors ($j=1,14$)
L_{tap}	Tap inductance
L_{tot}^j	Total laid-out inductances of both spiral inductors and interconnects ($j=1,14$)
$L_{tot'}^j$	Optimized total inductances of both spiral inductors and interconnects ($j=1,14$)
l	Channel length
λ_s	Shortest wavelength used on microstrip
M	Mutual inductance
MAG	Maximum small-signal gain of a FET
m	Degree of mismatch
NF	Noise Figure

N_{opt}	Optimum number of stages
n	Number of stages
Ω	Normalized frequency
Ω_{1dB}	1-dB roll-off normalized frequency
ω	Frequency
ω_{1dB}	1-dB roll-off frequency
$\bar{\omega}_{1dB}$	Process-independent 1 – dB roll-off normalized frequency
ω_{HF}	Upper frequency of operation
ω_c	Cut-off frequency
ω_{cd}	Drain line cut-off frequency
ω_{cg}	Gate line cut-off frequency
ω_g	FET gate-terminal corner frequency
Φ	Phase shift per section
Φ_d	Drain line phase shift per section
Φ_g	Gate line phase shift per section
P_{in}	Input power
P_{inmax}	Maximum gate line input power
P_o	Output power
p	Total FET periphery
p_{opt}	Optimum total FET periphery
R_{DT}	Resistance of drain line termination
R_{GT}	Resistance of gate line termination
R_d	Drain resistance
R_{ds}	Active channel resistance beneath the depletion region
R_g	Gate metallization resistance
R_i	Channel series resistance of gate-source space-charge region
R_{int}^j	Resistances of the interconnects ($j=1,14$)
R_s	Source resistance
R_{spiral}^j	Resistances of the laid-out spiral inductors ($j=1,14$)

R_{tot}^j	Total laid-out resistances of both spiral inductors and interconnects ($j=1,14$)
$R_{tot}^{j'}$	Optimized total resistances of both spiral inductors and interconnects ($j=1,14$)
SC	SUPER-COMPACT
S_{ij}	S-parameters ($i,j=1,2$)
T_H	Half-section transformer transfer function
τ	Electron transit time
τ	Degree of taper
V_0	Output voltage
V_G	Gate line voltage generator
V_{IN}	Gate line input voltage
V_{bi}	Schottky-barrier forward conduction voltage
V_c	Voltage across C_g
V_{dn}	Drain voltage across the n -th FET
$V_{ds,br}$	Maximum drain-source voltage
V_{gi}	Gate terminal voltage of i -th FET
V_j	Port voltages ($j=1,2$)
V_p	Pinch-off voltage
v_s	Electron saturation velocity
W	Gate width of FET
W_{opt}	Optimum FET width
Y_{ds}	FET output admittance
Y_o	Port admittance
$Z(\omega, m, \tau, \alpha_g, \alpha_d)$	Characteristic impedance of drain line
Z_1	Line series-arm impedance
Z_2	Line shunt-arm impedance
Z_{DT}	Drain line terminating impedance
Z_{GT}	Gate line terminating impedance
Z_I	Image impedance

Z_{IG}	Internal impedance of generator
Z_{Π}	Π -section image impedance
Z_{Ii}	Port terminating image-impedances ($i=1,2$)
Z_L	Load impedance
Z_d^{ch}	Drain line characteristic impedance
Z_{d1}	Drain line series-arm impedances
Z_{d2}	Drain line shunt-arm impedances
Z_{do}	Drain line low frequency characteristic impedance
Z_{g1}	Π -section series-arms impedances of gate line
Z_{g2}	Π -section shunt-arms impedances of gate line
Z_{go}	Gate line low frequency characteristic impedance
Z_{gs}	FET input impedance
Z_l	Reactance of series-arm inductors
Z_o	Characteristic impedance of the gate line
Z_{ocj}	Port impedance when the other port is open-circuited ($j=1,2$)
Z_{pi}	Port impedances ($i=1,2$)
Z_{scj}	Port impedance when the other port is short-circuited ($j=1,2$)

1

Introduction

1.1 Thesis Motivation

In the past several years, distributed amplification has experienced a renewed interest due to the tremendous progress in the area of GaAs material and device development. This progress has resulted in the transferring of the gallium arsenide (GaAs) technology out of the research laboratories and into production lines of companies some of which offer foundry services to interested customers.

The distributed amplifier (DA) is based on the principle of utilizing the input and output capacitances of transistors, together with inductive elements to form the shunt and series elements of artificial low-pass transmission lines, respectively. These transmission-lines are coupled with the transconductances of the field-effect transistors (FETs) and offer unprecedented broad-bandwidth capabilities in several ways. These include:

- (a) Ultra-broadband gain exceeding several decades of bandwidth can be accomplished over frequencies ranging from dc up to and exceeding 40 GHz.
- (b) For such bandwidths, low input- and output-port VSWRs are realizable; this enables several DAs to be cascaded without sacrificing gain flatness.
- (c) The DA is inherently unconditionally stable if properly designed.
- (d) Due to its parallel architecture a failure of one of the FETs does not result in the DA's complete failure.
- (e) The use of the DA as an ultra-broadband power amplifier is restricted mainly by FET power limitations and is not in principle inherently limited by the DA's design.

- (f) For amplifiers operating at dc and having bandwidths exceeding 10 GHz the DA outperforms the reflective-match amplifier, the lossy-match amplifier, the feedback amplifier, and the active-match amplifier in terms of gain flatness, stability and especially input/output (I/O) reflection coefficients [78].

Typical applications for a DA built with single- or dual-gate FETs include:

- (1) Automatic gain control (AGC) through bias control.
- (2) High speed RF switching.
- (3) High frequency AM modulation.
- (4) PCM (Pulse Code Modulation) modulation at very high bit rates.
- (5) Limiters capable of covering wide bandwidths.
- (6) Ultra-broadband mixers.
- (7) Power amplification over wide bandwidths.
- (8) Use in radar receiver systems which can exploit their large dynamic range.
- (9) Insertion of extra gain to overcome unanticipated additional losses incurred by system components.
- (10) Splitters and combiners capable of distributing and combining several ultra-broadband signals simultaneously for use in multiplexing and demultiplexing circuits.—

1.2 Approach-Objectives

At the start of the present work the literature on DA research only covered artificial transmission lines having identical series inductor elements generally formed with 'real' transmission lines. It was conjectured that several techniques previously not covered experimentally could be applied to increase the performance of DAs. These include the tapering in value of the inductors along the artificial transmission lines, the use of lumped spiral inductors instead of 'real' transmission lines for a

tapered DA, and the incorporation of forward-feed (FF) capacitors to enhance the high-frequency gain and extend the useful bandwidth.

With this in mind a 1-12-GHz four-stage DA using GaAs monolithic microwave integrated circuit (MMIC) technology was designed, manufactured, and measured. To accomplish this, four metal-semiconductor field-effect transistors (MESFETs) were fabricated on a GaAs substrate forming the active devices and interconnected with lumped element spiral inductors to form the artificial transmission lines. However, MESFET and inductor losses due to active-channel resistance and skin-effect, respectively, contributed significantly to gain degradation at high frequencies close to 12GHz. Several techniques are discussed to overcome this. These include the tapering of the spiral inductor values along the gate and drain lines and of the values of the inductors inserted in series with the drain terminal (series-drain inductors) of each FET. Further improvements in gain can be realized through the use of forward-feed capacitors connecting the drain terminal of each FET to the gate terminal of the following FET. The use of series-drain inductors, in itself, increases the gain, but especially enhances the performance-improving properties of forward-feed when used concurrently. The bandwidth and the maximum chip area were defined by R. K. Surridge at BNR [105] while the FET width and the number of stages were computed by the author with the help of SUPER-COMPACT.

The basic characteristics of a DA using forward-feed capacitors and tapered gate and drain lines formed of lumped-element spiral inductors are:

- (1) Increased gain and bandwidth are obtained through the use of the performance-improving mechanisms.
- (2) Because of the use of spiral inductors instead of microstrip sections the circuit can be realized without using a ground-plane.
- (3) Input and output matching and stability are improved over the 1-12GHz bandwidth.

The aims of this thesis are:

- (i) To optimize and predict the performance-improving mechanisms with the aid of a symbolic algebraic manipulator and the use of a CAD method.
- (ii) To design, manufacture, and measure a DA implemented with GaAs MMIC technology.
- (iii) To verify the accuracy of GaAs MMIC-based standard-cell models experimentally.

1.3 Thesis Organization

Improving the performance of DA's involves the analysis of several factors. These are discussed in detail in the subsequent chapters. In Chapter 2, a brief review of the electrical properties of GaAs and microwave characteristics of MESFETs is presented. A historical overview of the DA performance-improving techniques reported in the literature is also given. Finally, first-order equations expressing gain and bandwidth limitations are presented.

Chapter 3 presents a detailed theoretical analysis. This was performed with the help of MACSYMA (a symbolic algebraic manipulator program) taking into account FET losses. The analysis results in a graphical gain-optimization procedure by solving for the optimum number of stages and FET widths. Definitions of tapering and mismatching are given which serve to illustrate their potential effects towards increasing the DA's performance. A brief description and theory of ultra-broadband splitter and combiner circuits utilizing the concept of distributed amplification is given.

The performance-degrading effects due to inductor and FET losses are analyzed through the use of complete circuit-element models and CAD methods and are presented in Chapter 4. Solutions to circumvent the limitations in gain are given, such as tapering and the use of forward-feed capacitors, and series-drain inductors. Also, an investigation into the effects on gain due to FET width, bandwidth, the

number of stages, and gain flatness is discussed.

Chapter 5 describes the details of the iterative process involved in the concurrent layout and computer-aided optimization procedure for the DA chip based on GaAs MMIC technology. Also, an account of the difficulties encountered during the layout of the DA's circuit elements is given. From the finalized layout based on the particular optimized design arrived at in Chapter 4, the frequency performance under various bias conditions is predicted for the fabricated chip.

In Chapter 6, the measurement apparatus and setup are described along with the experimental performance of the DA. The DA's frequency performance is presented in terms of S-parameters, stability, group-delay, 1-dB gain-compression point, and process variations. From this, an explanation of the discrepancies between predicted and measured results is given. Agreement is achieved with simulated results when the effects due to process variations are accounted for.

Finally, in Chapter 7 conclusions are drawn as well as suggestions for further work.

Background

2.1 Introduction

Interest in the electrical properties of GaAs and its use as a material for building high-speed devices over the past few years has increased to an all-time high. One just has to browse through the numerous research papers published in various publications.

In this chapter a brief introduction to the numerous types of GaAs active devices utilized in high-speed applications is given. Details on the subject can be found in the abundant literature available and will be pointed out to the reader in the following sections.

2.2 GaAs and FET Technology

2.2.1 Overview

GaAs is a binary compound which has long been known to exhibit attractive electrical properties. Its semiconducting properties were first reported by Welker in 1952 [1]. During the same period Shockley developed a formal algebraic derivation of the JFET (Junction Field Effect Transistor) and demonstrated its relatively simple topology [2]. Then in 1964, Cronin et al. were able to reproducibly grow SI (Semi-Insulating) GaAs through the doping of a deep acceptor such as Cr [3]. Shortly afterwards, Mead in 1966 reported on the first electrical characteristics of a fabricated GaAs MESFET (MEtal Semiconductor FET) by replacing the p-n junction with a Schottky-barrier contact, thus simplifying gate formation [4]. Although the device did not exhibit a microwave response and was slower than the BJTs (Bipolar Junction Transistors) available at the time, it did trigger extensive

research into GaAs devices. Consequently, one year later Hooper et al. reported on the first microwave GaAs MESFET with an f_{max} greater than 3 GHz [5]. Surprisingly, the first MMIC (Monolithic Microwave Integrated Circuit) did not include a MESFET as an active device and yet operated at 94 GHz. The circuit contained a Gunn diode operating as an oscillator and was constructed by Mehal et al. in 1968 [6]. In 1976 Pengelly et al. reported on the first fully monolithic GaAs X-band amplifier [7]. From then on extensive research into ultra-high-speed devices escalated to a level that has brought us to the current state in which commercial foundries are flourishing. These foundries are capable of mass-producing tailor-made MMIC chips profitably. For a more complete historical perspective on the subject one is referred to the numerous publications upon which this overview was based [1,8-10].

2.2.2 Electrical Properties of GaAs

There are several properties which make GaAs a very attractive material. It has a very high low-field mobility (typically $4500 \text{ cm}^2/\text{V sec}$ and $8000 \text{ cm}^2/\text{V sec}$ for lightly doped material) approaching 6 times that found in Si. At the same time it has twice the peak electron drift velocity found in Si. The electron drift velocity as a function of electric field for GaAs and Si is shown in Fig. 2.1. One can see that the maximum drift velocity of GaAs reaches approximately $2 \times 10^7 \text{ cm/s}$ at an electric field of 3 kV/cm (E_{pk}) and then decreases to a saturated value approaching that of Si for large electric fields [11]. This higher velocity implies that devices can be made to have lower parasitic resistances, higher currents (therefore a larger transconductance), and lower electron transit times than for Si based devices.

Intrinsic GaAs inherently has a very high resistivity (greater than $10^7 \Omega\text{cm}$ as compared to $30 \Omega\text{cm}$ for Si) making it semi-insulating (SI), and hence an ideal substrate for applications in which low parasitic capacitances are desirable. Its SI properties have the effect of simplifying the design of MMICs since isolation implants between active devices are in general not necessary. Since the relative dielectric constant of GaAs is 12.9 [12], this makes it a suitable candidate for inter-

Figure 2.1 Electron Saturated-Velocity Versus Electric Field [11].

digitated capacitors and transmission lines (when a ground plane exists).

The large bandgap of GaAs (1.4 eV as compared to 0.8 eV for Si) enables devices made of this material to function up to greater temperatures, and hence to higher power levels [1]. This larger bandgap in conjunction with a short minority carrier lifetime permits GaAs devices to operate in harsher radiation environments.

Nevertheless, the substrate material does possess several drawbacks as compared to Si, such as a lack of native oxide, it is a binary semiconductor, diffusion of impurities is practically impossible, and the wafers can easily be broken due to the brittle nature of GaAs [1]. The first of these drawbacks relates to the difficulty in fabricating GaAs MOSFETs (Metal Oxide Semiconductor FET), the second implies that high temperature processing may cause disassociation of the substrate's surface.

2.2.3 Principles of the Schottky Barrier MESFET

Several types of transistors are presently under investigation. The most promising of these include the MISFET (Metal Insulator Semiconductor FET), JFET, MESFET, HEMT (High Electron Mobility Transistor), and some of the more exotic devices, such as the PBT (Permeable Base Transistor), and the HBT (Heterostructure Bipolar Transistor). Since a detailed description of the MESFET is beyond the scope of this work and a detailed description of these devices can be obtained from several publications [1,13-15], only a brief description will be given in this section. A schematic of the MESFET geometry showing the physical origin of the circuit elements (of Fig. 2.2(a)) is given in Fig. 2.2(b) [16] for a common-source configuration. The device consists of a semi-insulating (SI) substrate with an n -doped active channel on top. Two ohmic contacts form the source and drain terminals of the device. Between these terminals is deposited a narrow metal layer forming a Schottky-barrier and an underlying depletion region in which the active channel can be constricted by biasing the gate negatively with regards to the source. A detailed description of the fabrication of these devices has been given by Williams

[12] and a typical three-dimensional section of a completed MMIC incorporating active and passive elements is depicted in Fig. 2.3.

In the traditional FET theory of Shockley the phenomenon of current saturation is governed by channel pinch-off [12,16-18]. However, in GaAs MESFETs, this phenomenon is superseded by velocity saturation of the electrons due to high electric fields $\gg E_{pk}$. Under transient conditions, for gate lengths shorter than 3 μm , electrons do not reach equilibrium transport conditions, and thus can be accelerated to twice their equilibrium velocity [18-21]. This electron velocity overshoot effectively shortens the electron transit time through the channel, and therefore increases the cut-off frequency of the transistor. It has been demonstrated that this phenomenon is not the only hot-electron effect found in short-gate-length devices and that electron temperature gradients contribute significantly to the electrical characteristics of the MESFETs [21].

The drain current as a function of drain and gate voltage (relative to the source terminal) is presented in Fig. 2.4. Three regions of operation exist: the linear region, the saturated region, and the breakdown region. Contrary to conventional expectations, FETs operating as linear devices do not operate in the linear region (as defined within the figure), but rather in the saturated region. In this region drain current excursions are approximately bounded by 0 and I_{Dss} , the gate voltage by V_p and V_{bi} , where $I_{Dss} = I_{Dsat}|V_{gs}=V_{bi}$, while V_{bi} and V_p are respectively, the Schottky-barrier forward conduction voltage and pinch-off voltage.

The intrinsic elements of the FET model shown in Fig. 2.4 include:

R_s , the channel series resistance of gate-source space-charge region,

C_{gs} , the gate-source capacitance of space-charge region,

C_{dg} , the drain-gate capacitance of space-charge region,

C_{dc} , the dipole layer capacitance,

g_m , the transconductance,

R_{ds} , the active channel resistance beneath the depletion region including the

(a)

(b)

Figure 2.2 (a) MESFET Circuit Model.

(b) Physical Origin of the Circuit Elements [16].

Figure 2.3 Three Dimensional Section of an MMIC [13].

Figure 2.4 Drain Current Characteristics of a MESFET [16].

extrinsic (parasitic) elements,

R_g , the gate metallization resistance,

R_s , the source resistance,

R_d , the drain resistance,

C_{ds} , the substrate capacitance [18].

This model is found to adequately describe the high-frequency effects of the MESFET. Generally the values of these parameters are obtained empirically through microwave S-parameter measurements.

The MESFET cut-off frequency is defined as being the frequency at which the current of the transconductance equals that of C_{gs} and is given as

$$f_T = \frac{g_m}{2\pi C_{gs}} = \frac{1}{2\pi\tau} \quad (2.2.1)$$

where the channel transit time for an electron to traverse the channel is given by $\tau = \frac{l}{v_s}$, l is the channel length, and v_s is the saturation velocity. This expression states that to increase the maximum useful frequency, either the gate length can be reduced or the saturated velocity of the electrons can be increased. One can extend the expression for f_T to include the source-resistance feedback effect. The extrinsic transconductance (obtained from the measured drain current and gate voltage transfer curves) then becomes

$$g'_m = \frac{g_m}{1 + R_s g_m} \quad (2.2.2)$$

The maximum frequency of oscillation, at which the input power to the gate equals the power generated by the output under matched conditions, is

$$f_{max} = \frac{f_T}{2} \sqrt{\frac{R_{ds}}{R_i}} \quad (2.2.3)$$

This parameter is a useful figure of merit and is commonly utilized in the literature. An empirically obtained version of this is

$$f_{max} = \frac{40GHz}{l} \quad (2.2.4)$$

where l is the gate length in μm [11]. From this one can deduce that FETs having 0.25 μm long gates should have an f_{max} approaching 160 GHz.

It can be shown [1,11] that the maximum small-signal gain of a FET is given by

$$MAG = \frac{(\frac{L_f}{f})^2}{4g_{ds}(R_g + R_i + R_s + \pi f_T L_s) + 4\pi f_T C_{dg}(2R_g + R_i + R_s + 2\pi f_T L_s)} \quad (2.2.5)$$

where L_s is the inductance in series with R_s and f is the frequency of operation. From this it is clear that the MAG is proportional to $\frac{1}{f}$, which represents a -6 dB/octave roll-off.

An investigation of the most recent MESFETs and HEMTs operating at microwave frequencies reveals that, contrary to most expectations, MESFETs outperform HEMTs in terms of f_{max} and power-per-unit-width. The reason for this is that MESFETs are manufactured using a more mature and simpler processing technology. Experimental measurements given by Smith et al. [22] demonstrate that a MESFET with a 0.25 μm gate length achieves an f_{max} of 160 GHz, a 30 GHz power-per-gate-width of 0.44 W/mm and a 60-GHz gain of 8.5 dB. For a comparable HEMT of the same gate length one obtains 120 GHz, 0.32 W/mm, and 5.7 dB, respectively. However the same authors believe that due to current extensive efforts to improve the high-frequency performance of HEMTs, the latter devices should become the victor in the foreseeable future. Nevertheless, at the time of this writing, MESFETs are the only transistors that have experimentally demonstrated oscillations at 110 GHz with 0.2 μm gate lengths [23]. Power amplifiers delivering 6 Watts of power have been reported for 11.7 GHz and 14.7 GHz and have exhibited gains of 7 dB and 6 dB, respectively, at the 1-dB gain-compression point [24]. Such performance indicates the feasibility of utilizing GaAs MESFETs in MMICs

at millimeter-wave frequencies.

Due to the evident high-frequency capability of the HEMT a brief summary of the best reported experimental results is given in Table 1.1.

Table 2.1 Current Performance of HEMTs.

Frequency (GHz)	Gain (dB)	NF (dB)	Reference	Comment
8	19	0.6	[25]	
17	13.1	0.85	[26]	-60 C°
18	11.6	1.2	[25]	
30	9.7	1.8	[25]	
40	7.0	2.1	[25]	
60	5.7	2.8	[25]	

The outlook for the future promises further improvements. For example, exotic devices such as the VFET (Vertical FET), could demonstrate cut-off frequencies exceeding 240 GHz [27].

2.3 Overview of Distributed Amplification

2.3.1 Introduction

The concept of distributed amplification is based on the principle of utilizing the normally undesirable input and output capacitances of transistors in a constructive manner so as to form input and output artificial transmission lines. These capacitors, in conjunction with inductors, form the shunt-arm and series-arm impedances, respectively, of the artificial transmission lines. These transmission lines, in turn, coupled by the transconductance of the FETs provide a propagating medium in which travelling waves can exist.

A schematic of a 4-stage distributed amplifier having the spiral inductors of the gate- and drain-lines and series-drain inductors taper in value along its longitudinal axis is shown in Fig. 2.5.

The schematic also includes forward-feed capacitors and drain-line shunt capacitors and are discussed in greater detail in the following sections.

2.3.2 History

The distributed amplifier (DA) was first proposed by Percival in 1937 [28] as a solution to increasing the gain-bandwidth product of broadband amplifiers by separating the terminal capacitances of individual tubes while adding their transconductances, thus resulting in an amplifier with an f_T greater than that which would be obtained if the tubes were simply connected in parallel. It was not until the first detailed theoretical paper by Ginzton et al. [29] (who were the first ones to coin the term 'distributed amplification') in 1948 that further interest in this concept resurfaced in the literature. But it was Horton et al. in 1950 [30] who extended the theoretical analysis and also reported the first experimental results. From then on, until the late 1950s, numerous researchers further extended the analysis and also reported on experimental results [31,32]. This even included the use of BJTs (Bipolar Junction Transistors) [33]. This was followed by a period (lasting up to the late 1970s) in which few papers were published; this was possibly due to the profuse coverage of the subject. Exceptions to this include the use of Si MESFETs and MOSFETs, as they include extremely attractive properties for incorporation as active devices within DAs. This is due to their relatively high output resistance and dominant effective input and output capacitive impedances [33-35]. It was not until GaAs processing became mature enough to produce devices of sufficient yield, that the first distributed amplifier utilizing GaAs devices appeared in the form of a hybrid MIC [36]. Almost simultaneously, the first GaAs MMIC distributed amplifier was reported by Ayasli [37,43]; this incorporated series-drain inductors between the drain line and FET drain terminals. This research work triggered a renewed

Figure 2.5 4-Stage Distributed Amplifier Configured with Forward-Feed Capacitors, Drain-Line Shunt Capacitors, and Tapered Gate- and Drain-Lines and Lumped-Element Series-Drain Inductors.

interest in further research and several papers resulted (and are enumerated in the following sections). The distributed amplifier has attracted much attention since then due to the potential broad bandwidths that can be achieved, the ease with which the fundamental principles of operation can be grasped (although the intricate details may not be so obvious, as will be shown), and also its topology makes it an ideal candidate for the implementation on a planar substrate.

2.3.3 Series-Drain Inductor

At frequencies exceeding several GHz it is inevitable that losses cause considerable gain-reduction. Significant research and experimental work has been devoted to surmounting this. A possible solution includes the insertion of a so-called 'series-drain inductor' between the drain of the FETs and the drain line [37-54]. This reduces the cut-off frequency of the drain line, causing drain-line resonance which produces a peaking of the gain, as well as better impedance matching of the FETs to the drain line at the higher frequencies, while simultaneously avoiding degradation of the low frequency performance. This method has become universally accepted and is found in most, if not all, distributed amplifier articles published to date.

2.3.4 Tapering

Another way to increase the HF gain, which will be described in detail in this thesis, is to use a TDA (tapered distributed amplifier) design in which the inductor values monotonically increase along the gate line and monotonically decrease along the drain line. The main contributor to an increase in gain is the drain line in which part of the reverse-travelling wave on the line is redirected towards the load impedance by enhancing the signal emanating out of each FET to interfere constructively with the forward-travelling wave. In addition, because of the tapered nature of the gate and drain lines, these lines behave in a manner resembling the impedance matching obtained by multiple-section transformers [55]. This has the additional effect of improving the input and output port reflection coefficients. This

also enables the gate line to contribute to an increase in gain by redistributing the input signal to deprived FETs (due to line losses) furthest away from the input. It has been reported that phase concurrency between the gate and drain lines is improved through the tailoring of the propagation velocity along the lines [56]. Although this concept is not new since it has been presented by Espley in 1944 and Ginzton et al. in 1948 [29,57], only recently has it been incorporated practically in MIC or MMIC distributed amplifiers utilizing GaAs FETs [39,46,49,54,56,58-60].

2.3.5 Forward-Feed

Another approach, which will also be described in detail in this thesis, is referred to as a DAF (distributed amplifier with forward-feed) [49] in which the high frequency components appearing at the outputs of the FETs are, through the use of capacitors, re-routed away from the lossy drain line towards the input of the following FETs. Therefore, the high frequencies appear to propagate within the distributed amplifier in a manner resembling propagation in a conventional cascaded amplifier. The low frequencies, on the other hand, because of the high-pass characteristic of the capacitors, cannot propagate in this fashion and therefore propagate in the conventional sense of the distributed amplifier. Thus the advantages of greater gain obtained from the conventional cascaded scheme is utilized to compensate for gain roll-off attributable to gate and drain line losses, while at the same time retaining the large bandwidth, low reflection coefficients and flat gain advantages of the distributed amplifier. Although this technique has been reported previously [61], we will present here the first reported experimental results (to the knowledge of the author). A brief description of the experimental results has also been given by Surridge and the author [49].

2.3.6 FET Configurations

Other approaches have been reported to improve the performance of distributed amplifiers. These include utilizing series-gate capacitors [45,58,59], splitting the

input into two gate lines whilst maintaining a common drain line [41], cascoding transistors [46,62-64], and utilizing dual-gate FETs [44]. The first two of these approaches are predominantly exploited for their ability to overcome the power limiting mechanism imposed by gate and drain terminal voltage swing restrictions. The latter two are applied to amplifiers in which gain and gain flatness are of primary importance. In addition, through the common connection of the second gate terminals, it permits the gain of the distributed amplifier to be modulated over a wide range of controlling voltages, and therefore can be used in systems whereby there is a need for AGC (Automatic Gain Control), a RF switch, an AM (Amplitude Modulation) or PCM (Pulse Code Modulation) modulator, or a limiter. This is by no means a complete list.

The large dynamic range of distributed amplifiers makes them good candidates for use in radar receiver systems [65]. Their excellent stability, flat gain, and low port reflection coefficients makes them ideal for use such as in the insertion of an extra general amplifier block to overcome unanticipated additional losses due to system components [66].

2.3.7 Coplanar Waveguide

An interesting variation that has been reported is to replace the inductive lines by CPWs (Coplanar Waveguides) to minimize interconductor coupling. Nontapered and tapered versions have demonstrated the feasibility of using coplanar lines up to and exceeding 20 GHz [39,67]. However, there exists some concern regarding the excessive losses incurred by current crowding along the line edges. Also included in their study is the examination of the effects of variable gate width on amplifier performance. They indicate (as has been found by this author and other sources [39,44,46]) that the main advantage of this approach is not to increase gain but rather to improve port reflections and gain flatness.

2.3.8 Series-Gate Inductor

It has been found by the author that a series-gate inductor inserted in series with the gate terminal of each FET causes an increase in gain at high frequencies similar to what is observed with the insertion of series-drain inductors. However, it should be mentioned that this improvement in gain was found to be insignificant. This is achieved by lowering the gate line cut-off frequency by resonating the FET gates and thus only achieves increased gain at high frequencies without affecting the low-frequency response.

2.3.9 Spiral Inductors

Although most distributed amplifiers constructed to date have utilized transmission lines made by depositing metallized conductors on to a substrate having a ground plane on its back side, thus forming inductive lines, some have been fabricated with discrete spiral inductors so as to minimize chip area, conductor intercoupling, and to obtain better gain and VSWR characteristics [60,64,68,69]. Nevertheless, the use of distributed elements might be necessary if the band of interest is above Ku band.

2.3.10 Hybrid Distributed Amplifiers

Although most broadband distributed amplifiers are constructed on GaAs substrates, exceptionally good bandwidths have been achieved by hybrid MIC amplifiers. For example, 4.8 dB gain over a frequency range of 2 GHz to 30 GHz has been attained. In this case discrete GaAs FETs were wire-bonded to transmission lines formed of gold conductors deposited on a dielectric substrate [54,70]. On the other hand, due to the precise fabrication of active and passive devices of minute dimensions, the MMIC approach provides more repeatable and predictable amplifier performance than is obtainable by the hybrid approach. This micro-fabrication

has resulted in the fabrication of ultra-broadband distributed amplifiers with bandwidths of 40 GHz [38].

2.3.11 Ultra-Broadband Mixer

A novel use for the distributed amplifier has been reported by several authors in which the FET nonlinearities, which always exist under large signal driving conditions, are utilized to yield signal mixing. The simplest approach is the simultaneous injection of the LO (Local Oscillator) and RF signals on to a single gate line of a conventional distributed amplifier to produce the IF (Intermediate Frequency) on the drain line. A more attractive and better approach, which provides excellent isolation between input signals, is the separate injection of the LO and RF on to two individual gate lines utilizing dual-gate FETs and sharing a common drain line. Bandwidths approaching 12 GHz have been reported with a maximum conversion gain of 0.5 dB for an IF frequency ranging between 0.4 GHz and 1.5 GHz [71-74].

2.3.12 Travelling-Wave FET

If one increases the number of FETs while decreasing their widths and at the same time brings them closer to each other until the overall amplifier begins to resemble a very wide FET with a single gate, a TWF (Travelling-wave FET) results [75-77]. It has been proposed that such a device could exhibit a small-signal gain proportional to the total gate width if the phase velocities of both lines are equalized. This amplification, in which an exponentially growing wave is established, is achieved by designing the amplifier so as to guarantee that the proper travelling mode is generated. Unfortunately, this can only be attained through the use of complex matching and balanced inputs and outputs at all ports together with signal generators to establish the proper mode along the drain line. An interesting aspect of this concept is the fact that inductive coupling between the two lines is responsible for the exponentially growing wave, in which part of the drain signal is fed back onto the gate line providing some sort of signal regeneration.

This regeneration considerably resembles the forward-feed phenomenon previously described in this section. Although the predicted performance for such an exotic device demonstrates potential broad bandwidths, experimental results to date have not corroborated the predictions. To circumvent the complex and difficult-to-realize growing mode circuitry, a quasi-TWF is realized in which the advantages of the conventional distributed amplifier (which include gain peaking due to line resonance and the relative ease with which propagation can be realized) are incorporated. Such a configuration has demonstrated experimentally a respectable performance over a 10 GHz bandwidth.

2.3.13 Conventional Ultra-Broadband Amplifiers

An excellent comparison of various ultra-broadband (2 - 18 GHz) multi-stage single-ended GaAs MESFET amplifiers has been given by Niclaus [78], in which the distributed amplifier's (DA's) performance is compared to four other types such as the reflective-match amplifier, the lossy-match amplifier, the feedback amplifier, and the active-match amplifier. It is reported that all of these types of amplifiers exhibit similar gain and NF (noise figure), while the distributed amplifier excels in the areas of gain flatness, stability and especially input/output (I/O) reflection coefficients. Moreover, the distributed amplifier is much superior to the other types when system requirements necessitate the cascading of several amplifiers. In such a situation, the resultant amplifier achieves a much flatter gain (due to excellent matching between cascaded amplifiers), excellent I/O VSWR, and an equal if not better gain. For bandwidths not exceeding 10 GHz the DA may prove not to be the optimum solution.

It has been shown that not much can be done to improve the NF of a distributed amplifier without significantly degrading its gain [79-81].

2.3.14 Large-Signal Characteristics

The large-signal performance of a distributed amplifier has been analyzed

through the use of power and Volterra series representations to predict intermodulation distortion and the power saturation level [41,45,56,70,82-85]. It can be shown that there exist five power-limiting mechanisms in distributed amplifiers. The first one is the limited voltage swing that can be applied to the gate of a FET. This implies that the maximum positive voltage is determined by the forward conduction of the gate's Schottky junction. The maximum negative voltage is equal to the pinch-off voltage of the active channel. If the amplifier is designed to operate as a power amplifier then the FETs should be designed to function under a maximum gate voltage swing. With this in mind, one can arrive at the maximum allowable input power

$$\begin{aligned}
 P_{inmax} &= \frac{\Delta V_{in}^2}{8 \times Z_0} \\
 &= \frac{(0.5 + 4)^2}{8 \times 50} \\
 &= 51mW
 \end{aligned}
 \tag{2.3.1}$$

for a $Z_0 = 50\Omega$ where Z_0 is the characteristic impedance of the gate line, 0.5 V and 4 V are the magnitudes of the maximum voltage excursions (relative to the source) that the gate of the FET can experience without breakdown.

Similarly, the drain line also has a maximum voltage swing in which the gate-drain breakdown and pinch-off voltages limit the peak voltage, while the knee voltage constrains the lower voltage limit, resulting in a 23 V [11] swing for a typical microwave MESFET. This implies a maximum output power of 1.3 W for a 50Ω load and is independent of the number of stages and represents the second power-limiting mechanism.

The third mechanism pertains to FET output ac load-line matching to extract the maximum power deliverable by each FET, and should not be confused with FET impedance matching (which primarily affects the small-signal gain of the amplifier). The maximum deliverable power is constrained by $V_{ds,br}$ and I_{dss} from which the optimum load impedance, as seen by each FET, is simply the ratio of these two

parameters. $V_{ds,br}$ is the maximum permissible drain voltage before the drain breaks down.

The fourth is due to the equation

$$P_o = GP_{in} \quad (2.3.2)$$

where, given a maximum input power and gain, where the latter is constrained (due to losses) once the maximum frequency is specified, the maximum output power is found to be constrained even if the second mechanism is not a limiting factor.

The fifth and last mechanism pertains to the maximum thermal power that the chip can dissipate.

It can be seen that to extract the maximum output power of each FET, several factors have to be taken into consideration.

The microwave gain and output power of various distributed amplifiers published in the literature are presented in Figures 2.6 and 2.7, respectively. Although most of the amplifiers are of the MMIC type, some utilize discrete FETs bonded on to substrates such as alumina, and interestingly, achieve a very respectable broadband gain. Some of the amplifiers utilize tapered lines, series-drain inductors, cascoded FETs, and/or dual-gates, while the 1-Watt 2 to 8 GHz DA made by Raytheon includes series-gate capacitors to redistribute the input power more evenly to each FET, and one of the Varian amplifiers incorporates CPWs to reduce intercoupling.

2.4 Overview of Theory

The voltage gain of a lossless distributed amplifier utilizing unilateral GaAs MESFETs is

$$A = \frac{ng_m Z_d}{2} \quad (2.4.1)$$

where n is the number of stages, g_m is the FET transconductance, and Z_d is the drain line characteristic impedance. According to this first-order expression, gain

Figure 2.6 Published Microwave Gain of Distributed Amplifiers
[37,38,40-48,50,53,56,58,60,68].

Figure 2.7 Published Microwave Output Power Characteristics
[37,38,40-48,50,53,56,58,60,68].

monotonically increases with n , g_m , and Z_d , and is independent of frequency, without any upper frequency limit. This expression is obtained by noting that the n FETs (each having a transconductance g_m) are 'effectively' in parallel and generate a current $\frac{ng_m}{2}$ into load Z_d . The ratio of g_m to C_d is approximately independent of FET width. C_d is the effective drain-line shunt capacitance (which is equal to C_g , by definition) due to the imposed constraint of equal gate and drain line phase velocities and characteristic impedances (see Section 3.3.2 for more details). Then the voltage gain can be written

$$A = \frac{3nk_{gc}}{4\omega_{1dB}} \quad (2.4.2)$$

and the gain-bandwidth product (GBW) is

$$GBW = A\omega_{1dB} = \frac{3nk_{gc}}{4} \quad (2.4.3)$$

where

$$k_{gc} = \frac{g_m}{C_d} \quad (2.4.4)$$

$$C_d = \frac{2}{\omega_c Z_d} \quad (2.4.5)$$

and in general it is found that the 1-dB roll-off frequency at which the gain rolls-off by 1 dB is

$$\omega_{1dB} \approx \frac{3\omega_c}{4} \quad (2.4.6)$$

Expression (2.4.2) implies that for a fixed number of FETs of variable width, the overall gain is inversely proportional to ω_{1dB} . Therefore GBW is proportional to n or is a constant if a fixed number of FETs is utilized.

If one includes gate-line loss, which is the dominant source of loss at high frequencies, while neglecting drain line loss, one can show that

$$A = \frac{nk_{gc}}{\omega_{HF}} e^{\frac{-n\omega_{HF}}{2\omega_g}} \quad (2.4.7)$$

by utilizing (3.3.34), (A3-31), (A3-13), (A3-10), (3.3.30), (3.3.9) and assuming $\omega_c \approx \omega_{HF}$ where the latter is the upper frequency of operation. ω_g is the corner frequency

of the FET's input R-C reactance and is independent of the width of the FET (see Section 3.3.2 for more details). Since all the parameters except n are constants for a specific FET type and upper frequency of operation, one can see that there is an optimum number of FETs for which the gain is maximized. This optimum value is

$$N_{opt} = \frac{2\omega_g}{\omega_{HF}} \quad (2.4.8)$$

where the maximum gain for an upper frequency ω_{HF} is

$$A_{max} = \frac{2\omega_g k_{gc}}{e\omega_{HF}^2} \quad (2.4.9)$$

(where $e = 2.71828$) and demonstrates that the gain varies inversely with the square of the upper frequency. Therefore, one can say that the gain of wide-band distributed amplifiers exhibits considerable degradation with an increase in upper frequency due to gate-line loss. One can arrive at the optimum gate width and total gate periphery

$$\begin{aligned} W_{opt} &\approx \frac{2}{k_{gc} Z_d \omega_{HF}}, \\ P_{opt} &\approx \frac{4\omega_g}{k_{gc} Z_d \omega_{HF}^2} \\ &= \frac{\text{constant}}{\omega_{HF}^2}, \end{aligned} \quad (2.4.10)$$

respectively. It is found that the total gate periphery cannot be increased beyond an optimum value which is constrained by the upper frequency of operation. Any increase beyond this value results in a degradation of performance. It should be mentioned that these equations are presented to bring out the most salient properties of the distributed amplifier's gain and are not intended to be used where accuracy is of uttermost importance.

Chapter 3

Distributed Amplifier Theory

3.1 Introduction

In the second chapter a brief theoretical overview of the maximum achievable gain of a distributed amplifier as a function of bandwidth was presented. The equations obtained were derived under certain simplifying assumptions. In this chapter a more rigorous theoretical analysis of the distributed amplifier is presented.

Firstly, the frequency response in terms of gain of a basic distributed amplifier is given in which the model of a unilateral and lossy FET is used. The resultant gain equation is then used to arrive at a graphical gain-optimization procedure from which the optimum number of stages and FET gate width can be obtained. Finally, the concept of tapering and mismatching with their effects on gain, bandwidth, gain-bandwidth product, and input and output VSWRs are presented. Their usefulness in improving the performance characteristics of the distributed amplifier will be discussed.

Some of the equations presented in this chapter were derived with the help of MACSYMA (Project MAC's SYmbolic MANipulation System) [104]. This software program enables a user to perform symbolic algebraic manipulations quickly and accurately on a computer. It permits the manipulation of linear and polynomial equations in various ways such as: expanding, factoring, differentiation, integration, obtaining Taylor series of functions, and matrix algebra (just to name a few). It has been found that a tremendous amount of time and tediousness can be alleviated through the help of this program.

3.2 Image Parameters

3.2.1 Introduction

The technique of image impedance matching plays a major role in filter design due to its inherent simplification of mathematical computations. Since the gate and drain lines are basically made of loaded constant- k filter sections cascaded to form a low-pass filter, it will be shown how image impedance matching helps simplify the mathematical analysis of distributed amplifiers (DAs). But first, it is important that the concepts of image impedance and propagation functions of arbitrary networks be understood.

3.2.2 General Networks

Referring to Fig. 3.1(a), a schematic representation of a general 2-port network terminated with its image impedances is shown. The image parameters of this network are defined as being the image impedances and propagation function of the two ports. The parameters Z_{p1} and Z_{p2} are defined as being the impedances seen looking into ports 1 and 2, respectively. Z_{p1} is the impedance seen looking into port 1 when port 2 is terminated with its image impedance Z_{I2} ; conversely, Z_{p2} is the measured impedance looking into port 2 when port 1 is terminated with its image impedance Z_{I1} . Image impedance matching implies that the impedance of each port is equal to the impedance connected to the same port. In other words, Z_{p1} equals Z_{I1} and similarly Z_{p2} equals Z_{I2} .

The propagation function describing the transmission properties of the network is

$$\gamma = A + j\Phi \quad (3.2.1)$$

where A is the attenuation, or sometimes also referred to as the attenuation per section, and Φ is the phase shift. Similarly, the phase shift parameter is sometimes

Figure 3.1 (a) 2-port Network Terminated with its Image Impedances.
 (b) Half-Section Schematic.
 (c) T-Section Schematic.
 (d) Π -Section Schematic.

referred to as the phase velocity.

The propagation function describing the electrical transmission properties of the network shown in Fig. 3.1(a) as given by Ragan [86], is

$$\frac{V_2}{V_1} = e^{-\gamma} \sqrt{\frac{Z_{I2}}{Z_{I1}}} \quad (3.2.2)$$

where a voltage generator has been inserted in series with Z_{I1} . For the case of a symmetrical network, Z_{I2} and Z_{I1} are equal, so that Eqn. (3.2.1) simplifies to

$$\frac{V_2}{V_1} = e^{-\gamma} \quad (3.2.3)$$

and is the equation used to describe analytically the propagation function of the gate and drain lines.

Ragan [86] has also shown that the image parameters are given as follows (after being simplified for symmetric networks):

$$Z_I = \sqrt{Z_{oc} Z_{sc}}, \quad (3.2.4)$$

$$\gamma = \tanh^{-1} \sqrt{\frac{Z_{sc}}{Z_{oc}}} \quad (3.2.5)$$

The last expression may also be written

$$\gamma = \frac{1}{2} \ln \frac{1 + \sqrt{Z_{sc}/Z_{oc}}}{1 - \sqrt{Z_{sc}/Z_{oc}}} \quad (3.2.6)$$

where Z_{sc} and Z_{oc} represent the impedance seen looking into either port while the other port is short-circuited and open-circuited, respectively.

3.2.3 Half-Section

Both the gate and drain lines are formed by cascading the half-sections shown in Fig. 3.1(b) with transposed half-sections. It will be seen that this relatively simple

network can be used to adequately describe the frequency response of a distributed amplifier. Therefore it is of great importance that its propagation function be well understood.

The propagation function describing the port voltages of the image impedance matched half-section having a generator in series with Z_{I1} is [86]

$$\begin{aligned}\frac{V_2}{V_1} &= \sqrt{\frac{Z_{I2}}{Z_{I1}}} e^{-\gamma_H} \\ &= T_H e^{-\gamma_H}\end{aligned}\quad (3.2.7)$$

where γ_H is the propagation function and T_H is the transformer action of the half-section. The propagation function γ_H is a complex parameter comprised of real and imaginary terms. The real term describes the attenuation due to lossy elements and the imaginary term describes the phase shift per section. Using Eq. (3.2.5) we obtain the propagation function for nonsymmetric sections as

$$\gamma_H = \tanh^{-1} \sqrt{\frac{Z_{sc1}}{Z_{oc1}}} = \tanh^{-1} \sqrt{\frac{Z_{sc2}}{Z_{oc2}}}\quad (3.2.8)$$

where

$$Z_{sc1} = \frac{Z_1}{2},\quad (3.2.9)$$

$$Z_{oc1} = \frac{Z_1}{2} + 2Z_2,\quad (3.2.10)$$

$$Z_{sc2} = \frac{1}{\frac{1}{2Z_2} + \frac{2}{Z_1}},\quad (3.2.11)$$

and

$$Z_{oc2} = 2Z_2.\quad (3.2.12)$$

The parameters Z_1 and Z_2 are the series and shunt arm impedances, respectively, as depicted in Fig. 3.1(b). From Eqns. (3.2.4) and (3.2.9) through (3.2.12), inclusive, the image impedance Z_{I1} and Z_{I2} are

$$Z_{I1} = \sqrt{Z_1 Z_2 \left(1 + \frac{Z_1}{4Z_2}\right)} \quad (3.2.13)$$

and

$$Z_{I2} = \sqrt{\frac{Z_1 Z_2}{1 + \frac{Z_1}{4Z_2}}} \quad (3.2.14)$$

respectively. By inserting Eqs. (3.2.9) and (3.2.10) into (3.2.8) we obtain after simplifying

$$\gamma_H = \tanh^{-1} \sqrt{\frac{1}{1 + \frac{4Z_2}{Z_1}}} \quad (3.2.15)$$

Further simplification and rearrangement results in

$$\gamma_H = \frac{1}{2} \cosh^{-1} \left(1 + \frac{Z_1}{2Z_2}\right) \quad (3.2.16)$$

or

$$\gamma_H = \frac{1}{2} \ln \left(1 + \frac{Z_1}{2Z_2} \pm \sqrt{\left(1 + \frac{Z_1}{2Z_2}\right)^2 - 1}\right) \quad (3.2.17)$$

Inserting Eq. (3.2.4) into the term T_H of (3.2.7) we obtain

$$T_H = \sqrt{\sqrt{\frac{Z_{oc2} Z_{sc2}}{Z_{oc1} Z_{sc1}}}} \quad (3.2.18)$$

Noting in Eq. (3.2.8) that

$$\frac{Z_{sc1}}{Z_{oc1}} = \frac{Z_{sc2}}{Z_{oc2}} \quad (3.2.19)$$

and substituting this equality into Eq. (3.2.18) it is found that

$$\begin{aligned}
 T_H &= \sqrt{\frac{Z_{oc2}}{Z_{oc1}}} \\
 &= \sqrt{\frac{Z_{sc2}}{Z_{sc1}}}
 \end{aligned}
 \tag{3.2.20}$$

Inserting Eq. (3.2.10) and (3.2.12) obtained from Fig. 3.1(a) into (3.2.20) we obtain after simplification

$$T_H = \frac{1}{\sqrt{1 + \frac{Z_1}{4Z_2}}} \tag{3.2.21}$$

In other words, the voltage transfer function of a half-section with the generator in series with port 1 is

$$\frac{V_2}{V_1} = \frac{e^{-\gamma_H}}{\sqrt{1 + \frac{Z_1}{4Z_2}}} \tag{3.2.22}$$

where γ_H is given by Eq. (3.2.16). For the converse case where the generator is connected in series with port 2, Ragan [86] defines the reverse transfer function as

$$\frac{V_1}{V_2} = \sqrt{\frac{Z_{I1}}{Z_{I2}}} e^{-\gamma_H} / T_H = \sqrt{1 + \frac{Z_1}{4Z_2}} e^{-\gamma_H} \tag{3.2.23}$$

where γ_H , due to the reciprocity theorem, is identical to the forward propagation function given in (3.2.16). Both (3.2.22) and (3.2.23) are the building block equations used in Section 3.3 to arrive at the gain of the DA.

3.2.4 T-Section

One important building block that is used in Appendix 3 to calculate the drain line propagation function is the T-section shown in Fig. 3.1(c). The voltage transfer function can easily be derived by noting that the T-section is formed by cascading a half-section with a transposed half-section.

The voltage transfer ratio of port 2 to port 1 is simply the product of (3.2.22) and (3.2.23) in which the transformer action terms cancel since the resultant section is symmetrical

$$\begin{aligned}\frac{V_2}{V_1} &= e^{-2\gamma_H} \\ &= e^{-\gamma}\end{aligned}\quad (3.2.24)$$

where we define γ to be equal to twice the half-section propagation function. From equation (3.2.24) one can determine that for a lossless section, since γ becomes purely imaginary, its magnitude equals one.

3.2.5 Π -Section

Another building block used for both gate and drain lines is the Π -section shown in Fig. 3.1(d). The image parameters are easily found by noting that the Π -section is formed by cascading a transposed half-section with an unchanged half-section. Therefore, the propagation function is again derived from the product of (3.2.22) and (3.2.23), yielding:

$$\frac{V_2}{V_1} = e^{-\gamma} \quad (3.2.25)$$

Note that this result is the same as (3.2.24). An important and noteworthy point is that the propagation functions of Π - and T -sections are exactly equal. This fact will be used to simplify the derivation of the drain line propagation function in Appendix 3. The image impedance of a Π -section, Z_{Π} , is easily derivable by noting that it is equal to Z_{I2} (3.2.14) of the image impedance matched half-section (Fig. 3.1(a)). Therefore

$$Z_{\Pi} = \sqrt{\frac{Z_1 Z_2}{1 + \frac{Z_1}{4Z_2}}} \quad (3.2.26)$$

The necessary building blocks with their corresponding image parameters have now been presented. They will next be used to obtain the frequency and gain

characteristics of a general distributed amplifier.

3.3 DA Theory Using Image Parameters

3.3.1 Introduction

A schematic representation of a basic distributed amplifier is shown in Fig. 3.2. The circuit consists of two artificial transmission lines coupled by the transconductances of a number of FETs. The two artificial transmission lines are referred to as the gate line and the drain line and are used as a propagating medium for the input and output signals, respectively. These artificial transmission lines are formed by cascading filter sections and are terminated with an impedance equal to the characteristic impedance of the transmission line. The series-arms and shunt-arms of the filter sections are formed by using lumped inductors and capacitors, respectively. Microstrip lines are sometimes used to replace lumped inductors. For this application the phase shift per microstrip section must be less than 45 degrees.

The shunt capacitors are formed by using the intrinsic capacitances C_{gs} and C_{ds} of the FETs for the gate- and drain-lines, respectively. These intrinsic capacitances, usually undesirable in conventional broadband amplifiers where they cause gain degradation, can be advantageously used in artificial transmission lines by using them as the shunt elements.

A signal applied at the input of the distributed amplifier will propagate along the gate line until absorbed by the gate line terminating impedance. As the signal propagates, the gates of the FETs are consecutively excited. The corresponding FET transconductances excite a forward and a reverse travelling wave on the drain line. The forward wave is directed towards the load and the reverse wave towards the impedance which terminates the drain line. By designing the drain and gate line phase velocities to be identical, the forward wave progressively increases in magnitude as it approaches the output. On the other hand, the reverse travelling

Figure 3.2 Schematic Representation of a Basic Distributed Amplifier [87].

wave does not constructively interfere with the signal sources, and any uncanceled signal arriving at the drain line terminating impedance is absorbed.

These artificial transmission lines are the backbone to the functionality and usefulness of the distributed amplifier. They have the following properties:

- (i) They present matched impedances to the load and signal generator, respectively.
- (ii) They achieve some impedance matching to both the gate and drain complex impedances of the FET.
- (iii) They constructively use the complex impedances of the FET which are normally a nuisance.
- (iv) They ensure identical phase velocity on both gate and drain lines.

The equivalent circuit diagram of a basic distributed amplifier is shown in Fig. 3.4 and includes the equivalent FET model of Fig. 3.3.

In the accompanying theory the following assumptions are made:

- (a) The FET model is unilateral.
- (b) The gate and drain lines do not reflect any signal back to the input and output, respectively.

Since the unilateral FET approximation is used, the gate line can be analyzed independently of the drain line. This greatly simplifies the theory.

3.3.2 DA Theory Using Image Parameters

The equivalent models of the gate and drain lines of a generalized distributed amplifier are shown in Fig. 3.5.

The gate and drain lines differ from Fig. 3.4 in the sense that they have been broken down into cascaded Π - and half-sections with image-impedance matched terminations. The reason for this is that the image parameters, more specifically the propagation functions, of the overall amplifier can easily be obtained through relatively simple mathematical manipulation of the Π - and half-sections. The overall

Figure 3.3 Equivalent Model of a Lossy and Unilateral MESFET [87].

Figure 3.4, Equivalent Model of a Distributed Amplifier Including Lossy FET Model [87].

Figure 3.5 Equivalent Model of Distributed Amplifier Using Cascaded Π -Sections.

simplification is realizable mainly due to the cascading of identical Π -sections.

The gate line is driven by a voltage generator V_G with an internal impedance Z_{IG} generating an input voltage V_{IN} . Each of the Π - and half-sections are properly image-impedance matched. The input port and gate lines are terminated with Z_{IG} and Z_{GT} , respectively. The shunt arms of the Π -sections $2Z_{g2}$ are formed by splitting in two the effective shunt impedance on the gate line (i.e. the input impedance of a FET), into two identical parallel impedances each having twice the impedance of the original shunt impedance. The voltages across these shunt impedances are the voltages appearing across the FET's gate and source terminals.

The drain line is similarly constructed except for the fact that gate-line coupled transconductances are inserted between each Π -section. These current sources are generally indirectly controlled by the corresponding voltage on the gate line. Both ends of the drain line are image-impedance matched by the drain-line impedance termination and output load impedance Z_{DT} and Z_L , respectively.

The output voltage V_0 appearing across Z_L is derived from (3.2.23) to produce

$$V_0 = V_{dn} \sqrt{1 + \frac{Z_{d1}}{4Z_{d2}}} e^{-\gamma_d/2} \quad (3.3.1)$$

where V_{dn} is the drain voltage across the n -th FET and $\gamma_d = A_d + j\Phi_d$ is the Π -section propagation function. A_d and Φ_d are the drain line attenuation and phase shift per section, respectively. Z_{d1} and Z_{d2} are the drain series and shunt arm impedances, respectively. One important point is that the magnitude of the ratio V_0/V_{dn} is not necessarily unity, even for the lossless case in which the exponential term has a magnitude of one. This is simply due to the resonating effect caused by the reactive components of the drain line. V_{dn} is obtained by summing up all the contributions due to each FET transconductance, yielding

$$V_{dn} = \frac{Z_{\Pi}}{2} \sum_{i=1}^n I_{di} e^{-(n-i)\gamma_d} \quad (3.3.2)$$

where Z_{Π} is the image impedance of a drain line Π -section, I_{di} is the current

produced by each of the FET's internal transconductances, and n is the number of transistors. By inserting Eqs.(3.2.26) and (3.3.2) into (3.3.1) one obtains

$$V_0 = \frac{\sqrt{Z_{d1}Z_{d2}}}{2} \sum_{i=1}^n I_{di} e^{-[2(n-i)+1]\gamma_d/2}. \quad (3.3.3)$$

From Fig. 3.5

$$I_{di} = g_m V_{gi} \Gamma. \quad (3.3.4)$$

This can also be expressed as

$$I_{di} = g_m V_{ci} \quad (3.3.5)$$

where V_{ci} is the voltage across the internal electrical element controlling the transconductance of the i -th transistor. For a FET, V_c is normally defined as the voltage across C_{gs} , the equivalent gate-source capacitance. In (3.3.4), V_{gi} is the gate-source voltage and Γ is defined as being the ratio of V_{ci} to V_{gi} . For a FET, this is given as

$$\Gamma = \frac{1}{1 + j\omega R_i C_{gs}} \quad (3.3.6)$$

where ω is the radian frequency and R_i and C_{gs} are the effective input resistance and series capacitance, respectively.

The above expression can also be rewritten as

$$\Gamma = \frac{1}{1 + j\omega/\omega_g} \quad (3.3.7)$$

or

$$\Gamma = \frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega_g}\right)^2}} e^{-j\Phi_\Gamma} \quad (3.3.8)$$

where

$$\omega_g = \frac{1}{R_i C_{gs}} \quad (3.3.9)$$

and

$$\Phi_\Gamma = \tan^{-1} \frac{\omega}{\omega_g} \quad (3.3.10)$$

By following similar procedures for the gate line as was done for the drain line we can derive the voltage at the i -th gate to be

$$V_{gi} = V_{g1} e^{-(i-1)\gamma_g} \quad (3.3.11)$$

where $\gamma_g = A_g + j\Phi_g$ is the gate line propagation function per section. A_g and Φ_g are, respectively, the gate line attenuation and phase shift per section. One can easily derive the voltage across the first gate to be

$$V_{g1} = \frac{V_{IN} e^{-\gamma_g/2}}{\sqrt{1 + \frac{Z_{g1}}{4Z_{g2}}}} \quad (3.3.12)$$

where V_{IN} is the input voltage, Z_{g1} and Z_{g2} are the gate line series and shunt arm impedances, respectively. From (3.3.11) and (3.3.12) one can determine the gate voltage across the i -th gate to be

$$V_{gi} = \frac{V_{IN} e^{-(2i-1)\gamma_g/2}}{\sqrt{1 + \frac{Z_{g1}}{4Z_{g2}}}} \quad (3.3.13)$$

Combining Eqs. (3.3.4), (3.3.8), and (3.3.13) into (3.3.3) one arrives at the voltage gain of the overall amplifier

$$G = \frac{-g_m |\Gamma|}{2} \sqrt{\frac{Z_{d1} Z_{d2}}{1 + \frac{Z_{g1}}{4Z_{g2}}}} e^{+j\Phi_\Gamma} \sum_{i=1}^n e^{-((2i-1)\gamma_g + [2(n-i)+1]\gamma_d/2)} \quad (3.3.14)$$

This represents the exact voltage gain of a distributed amplifier with the assumptions that:

- (i) The unilateral FET model is as shown in Fig. 3.3.
- (ii) The gate and drain line terminations, the input source and output load are all image-impedance matched.

(The frequency-dependent image-impedances can be adequately matched to frequency-independent impedances, such as resistors, through the use of m -derived half-sections without significantly affecting the accuracy of (3.3.14).

Even the electron transit time can be included in (3.3.14) by replacing g_m with

$$g_m e^{-j\omega\tau} \quad (3.3.15)$$

where τ is the active channel effective electron transit time. This will only cause an extra phase shift term to be added to the gain equation (3.3.14) and will not cause any gain roll-off simply due to the lack of feedback within the amplifier. This is primarily due to the unilateral FET model assumed.

The summation term in (3.3.14) can be shown (see Appendix 1) to simplify and thus produce

$$G = \frac{-g_m |\Gamma|}{2} \sqrt{\frac{Z_{d1} Z_{d2}}{1 + \frac{Z_{g1}}{4Z_{g2}}}} \frac{e^{-n(\gamma_d + \gamma_g)/2} \sinh[n(\gamma_d - \gamma_g)/2]}{\sinh[(\gamma_d - \gamma_g)/2]} e^{+j\Phi} \quad (3.3.16)$$

One can further simplify (3.3.16) by formulating a valid assumption that does not necessarily affect its accuracy noticeably. The drain line propagation velocity or phase shift per section Φ_d can be made to be equal to the gate line's phase shift Φ_g by forcing both lines to have the same cut-off frequency. The cut-off frequency of a line is the frequency at which the line cannot support the propagation of a signal. For the basic distributed amplifier where the reactive elements of Z_{g1} and Z_{g2} are equal to Z_{d1} and Z_{d2} , respectively, the cut-off frequencies are the same. Therefore we have $\Phi = \Phi_g \approx \Phi_d$ which in turn simplify the propagation functions within (3.3.16) i.e.

$$\gamma_d + \gamma_g = A_d + A_g + j2\Phi \quad (3.3.17)$$

and

$$\gamma_d - \gamma_g = A_d - A_g. \quad (3.3.18)$$

Inserting these equations into (3.3.16) we obtain

$$A = |G| = \frac{g_m |\Gamma|}{2} \sqrt{\frac{Z_{d1} Z_{d2}}{\left[1 + \frac{Z_{g1}}{4Z_{g2}}\right]}} e^{-n(A_d + A_g)/2} \frac{\sinh[n(A_d - A_g)/2]}{\sinh[(A_d - A_g)/2]} \quad (3.3.19)$$

and

$$\angle G = \Phi_\Gamma - n\Phi \quad (3.3.20)$$

where A and $\angle G$ are the magnitude and phase angle of G , respectively.

This gain equation is a generalized equation valid for most distributed amplifiers with the following two assumptions: image impedance matched terminations and equal gate and drain line phase velocities.

The following section will treat a more specific case in which the lossy unilateral FET model shown in Fig. 3.3 is assumed. For this specific case the series and shunt arm of the gate and drain lines, as shown in Fig. 3.5, can be expressed as

$$Z_{g1} = j\omega L_g, \quad (3.3.21)$$

$$Z_{g2} = R_i + \frac{1}{j\omega C_{gs}}, \quad (3.3.22)$$

$$Z_{d1} = j\omega L_d, \quad (3.3.23)$$

and

$$Z_{d2} = \frac{1}{G_{ds} + j\omega C_{ds}} \quad (3.3.24)$$

where L_g and L_d are the series gate and drain line inductances, respectively, and C_{gs} and C_{ds} are the gate-source and drain-source shunt capacitances, respectively. R_i is the effective series input resistance, G_{ds} is the effective shunt drain-source conductance equal to $\frac{1}{R_{ds}}$, and ω is the radian frequency.

It should be noted that in most distributed amplifier designs both gate and drain line characteristic impedances and cut-off frequencies are equal. Therefore L_d is forced to equal L_g and similarly, C_{ds} is made to equal to C_{gs} . But generally, most FETs do not have equal gate and drain capacitances. In order to fulfill the need for identical characteristic impedances and cut-off frequencies a shunt capacitance C_p is placed in parallel to C_{ds} so that

$$C_{gs} = C_d \quad (3.3.25)$$

or

$$C_{gs} = C_{ds} + C_p \quad (3.3.26)$$

where C_d is defined as the effective drain line shunt capacitance.

The square root term of the gain equation (3.3.19) describes the frequency dependent drain line characteristic impedance. It is

$$\sqrt{\frac{j\omega L_d}{[G_{ds} + j\omega C_{ds}] \left[1 + \frac{j\omega L_g}{4 \left(R_i + \frac{1}{j\omega C_{gs}} \right)} \right]}} \quad (3.3.27)$$

where the parameters Z_{g1} , Z_{g2} , Z_{d1} , and Z_{d2} have been replaced with equations (3.3.21) through (3.3.24), respectively. For the case of an amplifier with less than moderate losses on both the gate and drain lines, the parameters R_i and G_{ds} of (3.3.27) may be equated to zero without significantly affecting the equation. Therefore, (3.3.27) simplifies to

$$\frac{Z_{do}}{\sqrt{1 - \left(\frac{\omega}{\omega_c}\right)^2}} \quad (3.3.28)$$

where

$$Z_{do} = \sqrt{\frac{L_d}{C_{ds}}} \quad (3.3.29)$$

and

$$\omega_c = \frac{2}{\sqrt{L_g C_{gs}}} \quad (3.3.30)$$

Z_{do} and ω_c are the drain line low frequency characteristic impedance and cut-off frequency, respectively. The cut-off frequency is the maximum frequency at which the gate and drain lines can support signal propagation.

By "less than moderately lossy" we mean that

$$R_i \leq Z_{go}/4 \quad (3.3.31)$$

and

$$R_{ds} \geq 4Z_{do} \quad (3.3.32)$$

where

$$Z_{go} = \sqrt{\frac{L_g}{C_{gs}}} \quad (3.3.33)$$

is the gate line low frequency impedance. By inserting (3.3.8), (3.3.21) through (3.3.24), (3.3.28), and (3.3.29) into (3.3.19) one obtains the simplified voltage gain equation of a distributed amplifier using the model of a simplified lossy unilateral FET to obtain

$$A = \frac{g_m Z_{do} e^{-n(A_d + A_g)/2} \sinh [n(A_d - A_g)/2]}{2\sqrt{1 + \left(\frac{\omega}{\omega_g}\right)^2} \sqrt{1 - \left(\frac{\omega}{\omega_c}\right)^2} \sinh [(A_d - A_g)/2]} \quad (3.3.34)$$

This expression is similar to the one derived by Beyer et al. [87] except for the fact that they have included an ideal broadband impedance transformer at the output and therefore impedance-matched it to the gate line of another cascaded amplifier. It is difficult to believe that a practical ultra-broadband impedance transformer could actually achieve the bandwidth of typical distributed amplifiers (12GHz or higher). Two errors exist in the derivation which, coincidentally, result in a correct solution. Details of the corrections are given in Appendix 2.

One can show that by differentiating the voltage gain (3.3.24) with respect to n (the number of stages) and equating the resultant expression to zero and solving for n one obtains the optimum number of stages:

$$N_{opt} = \frac{\ln(A_d/A_g)}{A_d - A_g}. \quad (3.3.35)$$

This expression states that while keeping most distributed amplifier parameters constant, such as FET periphery, characteristic impedance, maximum amplifying frequency, etc., (except for the number of stages) the optimum number of stages for maximizing the gain is simply a function of the gate and drain line attenuations only. Any further increase in the number of stages simply results in the degradation of the amplifier's overall gain, especially at the higher frequencies where losses are most severe. As the signal propagates along the gate line towards the termination and becomes progressively more attenuated, less signal is available to excite each successive FET sufficiently to surmount the additional gate and drain line losses incurred by the extra stage. It is assumed that the FETs are identical. This is generally the case in a MMIC based technology.

Unfortunately, the optimum number of stages cannot be easily obtained since the gate and drain line attenuation functions are complex and depend on the operating and cut-off frequencies and also on the intrinsic FET parameters.

3.3.3 Gate and Drain Line Attenuation

The gate and drain line attenuation functions are derived in Appendix 3 and

are, respectively:

$$A_g = \frac{2\Omega^2 \alpha_g}{\sqrt{1 - [1 - (2\alpha_g)^2]\Omega^2}}, \quad (3.3.36)$$

$$A_d = \frac{\alpha_d/2}{\sqrt{1 - \Omega^2}}$$

where Ω is the normalized frequency defined as

$$\Omega = \frac{\omega}{\omega_c} \quad (3.3.37)$$

The parameters α_g and α_d are the gate and drain line normalized loss, respectively, and are defined by

$$\alpha_g = \frac{R_i}{Z_{go}} \quad (3.3.38)$$

$$\alpha_d = \frac{Z_{do}}{R_{ds}} \pm \frac{G_{ds}}{Y_{do}}$$

These parameters are defined with the intent of having them proportional to the line attenuation. For the gate line this simply translates to being proportional to R_i . On the other hand, the drain line loss is inversely proportional to R_{ds} , or proportional to G_{ds} . The gate and drain line attenuations versus normalized frequency for various values of normalized loss are shown in Fig. 3.6 and 3.7, respectively.

It can be seen that the losses on both lines increase with both frequency and α . At high frequencies it is apparent that the gate line has more of an impact than the drain line on determining the upper frequency limit of the distributed amplifier. Also, the gate line is more frequency sensitive. These considerations and the fact that R_i is usually the dominant parameter affecting the FET's high frequency gain imply that considerable effort should be directed to reducing the gate line losses. Although the drain line losses are less significant, due to inherently high values of R_{ds} , they are solely responsible for the low frequency losses. Hence the distributed

Figure 3.6 Gate Line Attenuation per Section Versus Frequency
for Various Values of Normalized Loss.

Figure 3.7 Drain Line Attenuation per Section Versus Frequency for Various Values of Normalized Loss.

amplifier's gain at low frequencies is solely affected by the drain line, and mainly due to the gate line at high frequencies.

3.3.4 Parameter Substitution

One can see from equations (3.3.34), and (3.3.36) that the amplifier's gain is a function of nine parameters in which three are derivable from the remaining six. We will attempt to simplify the gain equation by noticing within it groups of parameters that appear several times of which the parameters themselves do not exist separately.

Using parameter definitions similar to those of Beyer et al. [87], one obtains

$$A = \frac{g_m Z_{do} e^{-\left[\frac{b}{\sqrt{1-\Omega^2}} + \frac{a\Omega^2}{\sqrt{1-\left(1-\frac{4a^2}{n^2}\right)\Omega^2}} \right] \sinh \xi}}{2\sqrt{1+\frac{4a^2\Omega^2}{n^2}}\sqrt{1-\Omega^2}\sinh(\xi/n)} \quad (3.3.39)$$

where we define

$$\begin{aligned} a &= n\alpha_g \\ b &= \frac{n\alpha_d}{4} \\ \xi &= \frac{b}{\sqrt{1-\Omega^2}} - \frac{a\Omega^2}{\sqrt{1-\left(1-\frac{4a^2}{n^2}\right)\Omega^2}} \end{aligned} \quad (3.3.40)$$

One then defines the normalized voltage gain as

$$A_N = \frac{A}{A_0} \quad (3.3.41)$$

where A_0 is the dc voltage gain

$$A_0 = \frac{g_m Z_{do} e^{-b} \sinh(b)}{2\sinh(b/n)} \quad (3.3.42)$$

Inserting (3.3.39) into (3.3.41) one obtains

$$A_N = \frac{\sinh\left(\frac{b}{n}\right) \sinh(\xi) e^{\left[b - \frac{b}{\sqrt{1-\Omega^2}} - \frac{a\Omega^2}{\sqrt{1-\left(1-\frac{a^2}{n^2}\right)\Omega^2}} \right]}}{\sinh(b) \sinh(\xi/n) \sqrt{\left[1 + \left(\frac{2a\Omega}{n} \right)^2 \right] [1 - \Omega^2]}} \quad (3.3.43)$$

This equation is identical to the one given by Beyer et al. [87]. For typical values of a , b , n and Ω this equation can be simplified to

$$A_N \approx \frac{e^{-\left[\frac{b+a\Omega^2}{\sqrt{1-\Omega^2}} - b \right]}}{\sqrt{1-\Omega^2}} \quad (3.3.44)$$

which is a function of a , b , and Ω only and is independent of n . In other words the normalized frequency response of the distributed amplifier can be characterized by using only three parameters. This is the reason why the parameter substitution in (3.3.40) has been done. In Fig. 3.8, the normalized voltage gain of (3.3.43) is shown as a function of normalized frequency for various values of a and b .

The frequency characteristic is for a four stage amplifier and does not vary significantly for 3 or more stages. One can observe that any increase in the gate or drain line parameter a or b , respectively, reduces the bandwidth considerably. Interestingly, the dc gain given by (3.3.42) is independent of the parameter a . This should not be surprising since the gate line does not contribute to low frequency losses. On the other hand, due to the shunting effect of R_{ds} on the drain line, the parameter b does have an effect on the low frequency losses, even at dc.

For the lossless case, i.e. when $a = b = 0$, the gain is seen to increase monotonically with frequency. This effect is solely due to the gate line in which the lossless LC network is basically a constant- k lowpass filter. As the cut-off frequency is approached, the gate line's response is somewhat similar to a resonating series LC tank. This can be shown algebraically by inserting

Figure 3.8 Normalized Gain Versus Normalized Frequency of a Distributed Amplifier, for $n=4$.

$$\begin{aligned}
Z_{g1} &= j\omega L_g, \\
Z_{g2} &= \frac{1}{j\omega C_{gs}}, \\
\gamma_g &= j\Phi/2, \\
\Omega &= \frac{\omega}{\omega_c}, \\
\omega_c &= \frac{2}{\sqrt{L_g C_{gs}}}
\end{aligned} \tag{3.3.45}$$

into (3.3.12) and taking the magnitude to obtain

$$\left| \frac{V_{g1}}{V_{IN}} \right| = \frac{1}{\sqrt{1 - \Omega^2}} \tag{3.3.46}$$

where V_{g1} is the voltage appearing at the gate terminal of the first FET. This equation is responsible for the denominator of (3.3.44). A similar resonating behavior exists on the drain line. Here

$$I_0 = \frac{nI_{gm}}{2\sqrt{1 - \Omega^2}} \tag{3.3.47}$$

where I_0 is the output current and I_{gm} is the current generated by the transconductance within each FET. In this last case the drain line has been simplified to be a lossless one in order to help visualize the behaviour of signal flows. This resonant behaviour does not affect the output voltage because of the frequency-dependence of the output impedance, i.e.

$$Z_0 = Z_{do} \sqrt{1 - \Omega^2} \tag{3.3.48}$$

where Z_{do} is the dc output characteristic impedance. The output voltage is simply the product of the two previous equations or

$$\begin{aligned}
V_0 &= I_0 Z_0 \\
&= \frac{nI_{gm} Z_{do}}{2}
\end{aligned} \tag{3.3.49}$$

which is independent of frequency and therefore confirms that the gate line is responsible for the increase in gain.

This increase in gain is not observed in the travelling-wave transistor presented by Podgorski and Wei [75] in which the gain is found to decrease monotonically due to the gate and drain line losses. The advantage of the distributed amplifier utilizing discrete transistors over the travelling-wave transistor is that the increase in gain is responsible, to some extent, for overcoming the loss in gain attributable to the gate and drain line losses.

Beyer et al. [87] present a graphical technique characterizing distributed amplifiers in terms of the parameters a , b , and n . In turn these parameters are dependent on the intrinsic parameters of the FET, namely, g_m , R_i , C_{gs} , etc. Also required for the analysis are extrinsic parameters of the FET such as n , Z_o , ω_c , and ω_{1dB} where the latter is the frequency at which the gain drops by 1 dB relative to the dc gain.

Their technique necessitates that intrinsic parameters specific to each FET and extrinsic parameters n and ω_c be used to obtain the dc gain and the 1-dB roll-off frequency. By trial and error these parameters are varied until a satisfactory gain and 1-dB roll-off frequency is achieved. More importantly, the optimum values of n and ω_c are not normally known and the latter is of no direct interest except for cases where group delay is of primary concern.

The graphical technique of [87] requires the circuit designer to plot a curve for each parameter value being tested for amplifier performance. The intersection of these and other (non-parameter-dependent) curves eventually produce the frequency response of the amplifier with the given parameters. For the case where several FETs of different gate widths, number of stages, or gate and drain line cut-off frequencies are under investigation as possible candidates for optimum performance, this can become a very time-consuming effort.

3.3.5 Optimizing Design Curves

3.3.5(a) FET Model

We here propose a simple and straightforward graphical technique for arriving at the optimum FET gate width, number of stages, gain, and gain-bandwidth product (GBW) without any need for the designer to resort to plotting curves for each parameter under consideration. The results are in agreement with the ones obtainable from SUPER-COMPACT, SPICE, and FORTRAN based programs. The technique eliminates the need for ω_c to be guessed or known.

One begins by making the assumption that the intrinsic parameters to the FET are approximately proportional or inversely proportional to the gate width [47,88]. This assumption can be stated algebraically as

$$\begin{aligned} g_m &= k_{gm} W, & R_i &= \frac{k_{Ri}}{W}, \\ C_{gs} &= k_c W, & R_{ds} &= \frac{k_{Rds}}{W}, \\ C_d &= C_{gs} \end{aligned} \quad (3.3.50)$$

where k_{gm} , k_c , k_{Ri} , and k_{Rds} are process-dependent constants independent of FET gate width. The parameter W is simply defined as the width of the gate. If required the secondary effects of width on the intrinsic parameters of the FET, not included in (3.3.50), can be neglected under a certain condition. This condition is achieved by simply resorting to a highly convergent technique in which the process-dependent constants are selected close to the operating point at which the optimum FET width is located. In other words, one assumes the previous assumption to be valid and obtains the optimum FET width by following the steps in the following sections. One then obtains improved process-dependent constants (from experimental data) valid for widths close to this new optimum FET width. One repeats these iterations until a suitable convergent solution is found.

The process constants are referred to as such simply because under a repeatable FET manufacturing process the intrinsic parameters do not change for constant

geometry FETs. These constants do not vary so long as the processing used to fabricate these transistors is kept unchanged. This also requires gate and drain voltage biases be maintained constant at predetermined values.

By inserting the expressions given by (3.3.50) into the equation (2.2.3) describing f_{max} one obtains

$$f_{max} = \frac{k_{gm}}{4\pi k_c} \sqrt{\frac{k_{Ri}}{k_{Rds}}} \quad (3.3.51)$$

which is independent of W . This implies that to a first order approximation, the maximum frequency of oscillation achievable does not change significantly with an increase or decrease in FET width. Therefore for each type of FET, f_{max} is a constant and hence is a figure of merit characterizing the manufacturing process.

Generally the approach used to arrive at the optimum distributed amplifier design is to first determine the maximum frequency of operation.

This frequency is usually defined as the frequency at which the gain rolls-off by a predetermined amount. We define this roll-off frequency as ω_{1dB} where the gain drops by 1 dB below the dc gain. In other words this occurs when the normalized voltage gain $A_N = 0.8913$.

From the specification of the 1-dB roll-off frequency, with knowledge of the FET process constants, and characteristic impedance Z_{do} , one then obtains the gate width, number of stages, gate and drain line inductor values, line cut-off frequency, voltage gain, and gain-bandwidth product of the optimum design. Before this procedure can be further explained, certain fundamental notions must first be introduced.

3.3.5(b) Constant FET Process Curves

From the definitions (3.3.38) and (3.3.40) one can show that

$$ab = \frac{n^2 \alpha_g \alpha_d}{4} \quad (3.3.52)$$

or

$$ab = \frac{n^2 R_i Z_{d0}}{4 Z_{g0} R_{ds}} \quad (3.3.53)$$

If we assume that the gate and drain lines have the same characteristic impedance, which is generally the case, then one obtains

$$ab = \frac{n^2 R_i}{4 R_{ds}} \quad (3.3.54)$$

Inserting the expressions of (3.3.50) for R_i and R_{ds} into the above expression one gets the important result

$$ab = \frac{n^2}{k_n} \quad (3.3.55)$$

where

$$k_n = \frac{4 k_{Rds}}{k_{Ri}} \quad (3.3.56)$$

One important property of the product of a and b is that it is independent of the gate width and simply dependent on n . By following similar steps one arrives at

$$\frac{b}{a} = \frac{(Z_0 W)^2}{4 k_{Ri} k_{Rds}} \quad (3.3.57)$$

or

$$W = \sqrt{\frac{b}{a}} k_w \quad (3.3.58)$$

where

$$k_w = \frac{2}{Z_0} \sqrt{k_{Ri} k_{Rds}} \quad (3.3.59)$$

Since Z_0 , k_{Ri} and k_{Rds} are constants during a design we can see that the width is a simple function of a and b and is independent of n .

Equation (3.3.55) is one of several design constraints that exist between a , b , and n . This expression is shown in Fig. 3.9 on the $a - b$ plane for various values of k_n , and $n = 4$, and describes a set of curves for which a is inversely proportional to b . Similarly, (3.3.58) is also shown and describes a set of straight lines with a slope inversely proportional to the gate width squared. These latter lines are only used to obtain the gate width once the operating point on the $a - b$ plane has been found. On the other hand, the former curves are incorporated in other graphs with other curves and the resulting intersection point produces the desired optimum operating point giving the maximum achievable gain for the frequency bandwidth required.

3.3.5(c) Constant Normalized Frequency Curves

One can expand on the definition of (3.3.37) and obtain

$$\omega_{1dB} = \Omega_{1dB} \omega_c \quad (3.3.60)$$

where Ω_{1dB} is the 1 dB roll-off frequency normalized to the artificial transmission line cut-off frequency ω_c .

The parameter Ω_{1dB} is a function of a , b , and n and is obtained by equating the normalized gain A_N in (3.3.43) to -1 dB or 0.8913. This is obtained numerically and shown in Fig. 3.10 for the case of $n = 4$. As derived in (3.3.44); Ω_{1dB} is almost independent of n and therefore, if required, a further and quite valid approximation can be made by assuming that the curves shown also represent the solutions for all cases of n greater than 3 inclusively. This implies as was previously mentioned that the analysis of a distributed amplifier can be characterized by only two parameters, i.e. a and b , thus simplifying the solution to 2-dimensional space.

The cut-off frequency is defined in (3.3.30) to be

$$\omega_c = \frac{2}{\sqrt{LC}} \quad (3.3.61)$$

where we have constrained the gate and drain lines to be identical or

Figure 3.9, Curves for $ab = \text{Constant}$ and $\frac{b}{a} = \text{Constant}$, for $n=4$.

Figure 3.10 Fractional 1-dB Bandwidth Curves:

$\Omega_{1dB} = \text{Constant Curves, } n=4.$

$$\begin{aligned} L &= L_g = L_d, \\ C &= C_{gs} = C_d. \end{aligned} \quad (3.3.62)$$

From (3.3.61) and

$$Z_0 = \sqrt{\frac{L}{C}} \quad (3.3.63)$$

one can arrive at

$$\omega_c = \frac{2}{Z_0 C} \quad (3.3.64)$$

or

$$\omega_c = \frac{2}{Z_0 k_c W}. \quad (3.3.65)$$

Inserting this equation and (3.3.58) into (3.3.60) one obtains the important normalized result

$$\bar{\omega}_{1dB} = \sqrt{\frac{a}{b}} \Omega_{1dB} \quad (3.3.66)$$

where

$$\begin{aligned} \bar{\omega}_{1dB} &= \omega_{1dB} k_c \sqrt{k_{Ri} k_{Rds}} \\ &= \frac{\omega_{1dB} k_{Rds} k_{gm}}{2\omega_{max}} \end{aligned} \quad (3.3.67)$$

The parameter $\bar{\omega}_{1dB}$ in (3.3.66) is defined as the process-independent 1-dB roll-off normalized frequency and is a function of a , b , and n only. It is independent of the width and the manufacturing technology. One can see that the right-hand side of (3.3.67) is a constant once the frequency of operation is chosen.

Equation (3.3.66) describes the interdependence of the parameters a , b , and n with the 1-dB gain roll-off frequency (independent of the FET's intrinsic parameters) and is shown in Fig. 3.11 for $n = 4$. For each value of $\bar{\omega}_{1dB}$ a curve exists made

up of two sections which are connected midway at which their respective slopes are discontinuous. These curves can be separated into two groups. The first group includes the curves having large values of a and the second includes the remaining ones with smaller values of a . Since a larger value of a corresponds to a greater gate line loss, the former group describes a region in which the gate and drain line losses determine the maximum achievable frequency.

Similarly, the latter group corresponds to the lower-loss case where the artificial transmission line cut-off frequency determines the maximum achievable frequency. This is more clearly understood if one refers to Fig. 3.12. For the case where the line losses determine the 1-dB roll-off frequency the gain decreases monotonically. If one reduces the line losses, the gain obviously increases, but more importantly, the DA has higher gain especially at high frequencies (but lower than cut-off) than the dc gain. This gain monotonically increases as the cut-off frequency is approached, but due to unavoidable line losses, peaks and then rapidly decreases to zero with even minute increases in frequency. This frequency response is depicted in Fig. 3.12 as the curved line which does not monotonically decrease. This describes the case of the second group and can be expressed algebraically using (3.3.66) and approximating $\Omega_{1dB} \approx 1$ to give

$$\bar{\omega}_{1dB} \approx \sqrt{\frac{a}{b}}. \quad (3.3.68)$$

Once the 1-dB roll-off frequency and process constants are known and $\bar{\omega}_{1dB}$ is consequently constrained to one specific value given by (3.3.67), only points lying on this curve can satisfy the equality given by (3.3.66). From Fig. 3.11 one can see for the family of curves belonging to the higher values of a , that as the drain line loss is increased and hence there is a corresponding increase in b or a shift to the right, a decrease in normalized frequency occurs, as expected. Similarly, while maintaining a constant drain line loss and travelling downwards, corresponding to a decrease in gate line loss, one notices an increase in normalized frequency. This means that once the 1-dB roll-off frequency and the process constants are known,

Figure 3.11 Constant Normalized-Frequency Curves

$\bar{\omega}_{1dB}$ = Constant curves, for $n=4$.

Figure 3.12 Frequency Characteristics of a Distributed Amplifier Limited by Cut-off Frequency and by Line Losses.

the values of a , b , and n are selected such that the equality (3.3.66) is satisfied.

3.3.5(d) Constant Normalized Gain Curves

A final and important expression necessary in characterizing the distributed amplifier in terms of the parameters a , b , and n only will be shown in this section. This will complete the constraints that have to be satisfied in order to correctly obtain the optimum operating point in terms of a , b , and n . This expression is derived from the dc voltage gain given by (3.3.42) and is found to be

$$\bar{A}_0 = \sqrt{\frac{b}{a}} e^{-b} \frac{\sinh(b)}{\sinh(b/n)} \quad (3.3.69)$$

where

$$\begin{aligned} \bar{A}_0 &= \frac{A_0}{k_{gm} \sqrt{k_{Ri} k_{Rds}}} \\ &= \frac{A_0}{2k_{Ri} k_c \omega_{max}} \end{aligned} \quad (3.3.70)$$

The expression (3.3.69) defines the parameter $\bar{A}_0$ as the process-independent normalized dc gain and is simply a function of a , b and n . The latter equation expresses the dc gain as a function dependent on $\bar{A}_0$ and the process constants. The former expression may be simplified to

$$\bar{A}_0 \approx n \sqrt{\frac{b}{a}} e^{-b} \quad (3.3.71)$$

for typical values of b and n , i.e. less than 0.4 and greater than or equal to 3, respectively. Contour lines of constant $\bar{A}_0$ on the $a - b$ plane of equation (3.3.69) are shown in Fig. 3.13 for the specific case of $n = 4$.

The most important comment that can be made about these curves is that an increase in gain and hence $\bar{A}_0$ requires one to opt for an operating point closest to the horizontal axis, in other words small values of a and hence low gate line losses. This is exactly what one expects to see. One subtle point that can also be extracted

Figure 3.13 Constant Normalized Gain Curves:
 $\bar{A}_0 = \text{constant}$, for $n = 4$.

is that for low values of a , an increase in b and hence drain line losses, ironically, has the effect of increasing the gain. This is solely due to an increase in g_m caused by an increase in gate-width. This can be seen algebraically from (3.3.58) where W monotonically increases as b increases.

If we introduce the concept of width-dependence to the intrinsic parameters of a FET to the dc gain expression (3.3.42) one obtains

$$A_0 = \frac{k_{gm} Z_{do} n W e^{-b} \sinh b}{b} \quad (3.3.72)$$

for $\frac{b}{n} < 0.8$. It can be shown that this can be re-expressed as

$$A_0 = k_{gm} k_{Rds} (1 - e^{-\frac{p Z_{do}}{k_{Rds}}}) \quad (3.3.73)$$

where

$$p = nW \quad (3.3.74)$$

and the latter is defined as the total gate periphery and is equal to the sum of all FET gate widths in the distributed amplifier. If one opts to increase the dc gain by adding stages or using wider FETs one finds that the greater total gate periphery will result in a peaking of the dc gain to

$$A_{0max} = k_{gm} k_{Rds} \quad (3.3.75)$$

It can be seen that the low frequency gain is primarily determined by the drain line losses and the FET transconductances. This expression is valid for the case where the periphery is increased by using numerous FETs without excessively wide gates. In other words it is valid for the case in which the distributed amplifier begins to resemble a continuous structure such as the travelling-wave transistor described by Podgorski et al. [75]. Their maximum low frequency gain resembles (3.3.75)

apart from differing in parameter labeling. For the case at the other extreme where the periphery is increased by using a single extremely wide FET one finds that

$$A_{0max} = 0. \quad (3.3.76)$$

This solution is incorrect since $\frac{b}{n}$ is no longer less than 0.8. If one uses a different approach in which the drain line inductors at dc behave as short circuits and therefore effectively parallel the FETs and terminations together, one finds the analysis to be simplified. It can be shown that under this condition using (2.4.1)

$$A_0 = \frac{ngm}{\frac{2}{Z_{do}} + \frac{n}{R_{ds}}} \quad (3.3.77)$$

or

$$A_0 = \frac{pk_{gm}}{\frac{2}{Z_{do}} + \frac{p}{k_{Rds}}} \quad (3.3.78)$$

and as $p \rightarrow \infty$

$$A_{0max} = k_{gm}k_{Rds} \quad (3.3.79)$$

independent of the approach the periphery is increased (i.e. by increasing the number of stages or the width of each FET).

3.3.5(e) Gain-Bandwidth Product

A final relation which expresses the gain-bandwidth product of a distributed amplifier is given by

$$GBW = A_0 f_{1dB} = \tilde{G}_{BW} f_{max} \quad (3.3.80)$$

where

$$\begin{aligned} \bar{G}_{BW} &= \frac{4\sqrt{abe}^{-b}\Omega_{1dB}\sinh(b)}{n\sinh(b/n)} \\ &\approx 4\sqrt{abe}^{-b}\Omega_{1dB} \end{aligned} \quad (3.3.81)$$

and f_{max} is also referred to as the maximum frequency at which the maximum available gain (MAG) of the FET equals one. The parameter $\bar{G}_{BW}$ is defined as the normalized gain-bandwidth product to f_{max} . This parameter defines a figure of merit for the distributed amplifier. It is the ratio of the GBW of the amplifier to the GBW of the FETs. Due to the fact that the gain-bandwidth product of an FET cannot be exceeded at any frequency whatever ideal matching conditions are imposed, this figure of merit is an indicator of the matching conditions achieved between the FETs and the distributed amplifier. Its value cannot exceed 1.122 (+1dB) under ideal internal matching conditions. The maximum value that can be obtained for $\bar{G}_{BW}$ using (3.3.81) has been found to be equal to 0.85 and demonstrates that even a distributed amplifier cannot create a perfect match internally with its own active devices. This implies that part of the input and output signals travelling on the gate and drain lines respectively cannot be completely prevented from reaching the line's terminations thus wasting some valuable high frequency power. The principal cause of wasted power is the reverse travelling wave on the drain line.

3.3.6 Graphical Optimization

3.3.6(a) Optimization Procedure

The three equations necessary to determine the optimum design point on the $a-b$ plane have been derived. The two most important ones are given by (3.3.55) and (3.3.66) and are plotted in Fig. 3.14, Fig. 3.15, and Fig. 3.16 for $n=3, 4$, and 5, respectively.

It is necessary to plot the functions for each value of n on separate graphs because these curves describe surfaces of constant value in 3-D space. Unfortunately,

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Figure 3.14 Graphical Optimization Curve, for $n=3$.

Figure 3.15 Graphical Optimization Curve, for $n=4$.

Figure 3.16 Graphical Optimization Curve, for $n=5$.

because of the need for accuracy and curves suitable for a wide range of distributed amplifier designs, several surfaces would be required. Since these cannot be adequately plotted as is, it is necessary to "slice" these surfaces at practical values of n .

These figures in conjunction with expression (3.3.69) constitute the necessary information to determine the optimum design point.

The general procedure in deriving the optimum design point is the following:

- (1) Obtain the process constants satisfying (3.3.50).
- (2) From the process constants and 1-dB roll-off frequency obtain $\bar{\omega}_{1dB}$ from (3.3.67).
- (3) Similarly, from (3.3.56) obtain k_n .
- (4) Arbitrarily choosing $n = 4$, select the constant contour lines for $\bar{\omega}_{1dB}$ and k_n in Fig. 3.15 and determine the intersection point. Note the values of a and b . If two solutions exist, select the one closest to the horizontal axis. If no solution exists, this implies that the solution is not achievable with this value of n .
- (5) From expression (3.3.69) determine the value of $\bar{A}_0$.
- (6) Repeat steps 4 and 5 for $n = 3$ and 5 (or higher if necessary as is discussed in Section 3.3.6(c)) using Fig. 3.14 and Fig. 3.16, respectively.
- (7) Determine the parameters a , b , and n which maximize $\bar{A}_0$. These parameters are the optimum design points from which the gain, gate width, cut-off frequency, and series-arm inductor values are derived using (3.3.70), (3.3.58), (3.3.82), and (3.3.83), respectively.

The latter two equations are

$$\omega_c = \frac{\omega_{1dB}}{\bar{\omega}_{1dB}} \sqrt{\frac{a}{b}} \quad (3.3.82)$$

$$L = \frac{2Z_d}{\omega_c} \quad (3.3.83)$$

3.3.6(b) Optimization Example

We now proceed to demonstrate the usefulness and simplicity of this graphical technique. The design example will be based on the FET parameters and ω_{1dB} given by Beyer et al. [87] as a comparison. By extracting their FET intrinsic parameters one obtains

$$g_m = 0.04\text{S},$$

$$C_{gs} = 0.27\text{pF},$$

$$C_d = C_{ds} + C_p$$

$$= C_{gs},$$

$$R_{ds} = 300\Omega,$$

$$R_i = 7\Omega$$

for a $300\mu\text{m}$ wide gate. From this, one then gets

$$k_{gm} = 1.33 \times 10^{-4}\text{S}/\mu\text{m},$$

$$k_c = 0.9\text{fF}/\mu\text{m},$$

$$k_{Ri} = 2100\Omega\mu\text{m},$$

$$k_{Rds} = 90000\Omega\mu\text{m},$$

$$f_{max} = 77.2\text{GHz}$$

We select $Z_{do} = Z_{go} = 50\Omega$, $f_{1dB} = 16.52\text{GHz}$ or $\omega_{1dB} = 1.04 \times 10^{11}\text{rads/sec}$ and obtain

$$\bar{\omega}_{1dB} = 1.28$$

$$k_n = 171$$

from (3.3.67) and (3.3.56), respectively. We then proceed to Fig. 3.15 for $n = 4$ where the contour lines of constant $\bar{\omega}_{1dB} = 1.25$ and $k_n = 175$ are selected. From

the intersection of these two curves one finds

$$a = 0.49 ,$$

$$b = 0.186 .$$

One then refers to equation (3.3.69) and obtains

$$\bar{A}_0 = 2.06 .$$

From (3.3.58), (3.3.82), (3.3.60) and (3.3.82) one then finds

$$W = 339 \mu m ,$$

$$\omega_c = 132 \times 10^9 \text{ rads/sec } (21.0 \text{ GHz}) ,$$

$$\Omega_{1dB} = 0.79 ,$$

$$L = 0.758 \text{ nH} ,$$

respectively. Finally, by using (3.3.70) one finds the dc gain to be

$$A_0 = 3.77$$

and the normalized gain-bandwidth product to be

$$\bar{G}_{BW} = 0.81$$

from (3.3.81).

By repeating these steps for $n = 3$ and 5 one obtains Table 3.1. The example given by Beyer et al. [87] is also given for comparison even though their design has not been optimized for maximum gain. It should be noted that for the 3-stage example there are two solutions of which the one offering the higher gain is shown. The amplifier offering the highest gain is the 4-stage design. Although the maximum gain for the 3-stage amplifier is quite similar to the 4-stage example, it

is expected to be lower than predicted due to the cut-off frequency being close to the 1-dB roll-off frequency i.e. $\Omega_{1dB} \approx 1$. In practice, due to the highly resonant situation, Ω_{1dB} is not expected to significantly approach unity and hence prevent the gain from becoming what is predicted in Table 3.1. The main reason for this discrepancy is that the gate- and drain-line expressions are valid for values of Ω less than 0.9. For higher values these expressions tend to underestimate the losses and therefore slightly inflate the actual gain.

Table 3.1 Graphically Determined Parameters of DA

n	3	4	5	Beyer[87]
a	0.29	0.49	1.62	0.56
b	0.178	0.186	0.088	0.17
A_0	1.98	2.06	1.07	1.87
A_0	3.62	3.77	1.96	3.27
$W(\mu m)$	431	339	128	300
G_{BW}	0.77	0.81	0.42	0.7
Ω_{1dB}	1.0	0.79	0.30	0.7
$f_c(GHz)$	16.5	21.0	55.5	23.6
$L(nH)$	0.96	0.76	0.29	0.67
$g_m(mS)$	57	45	17	40
$R_i(\Omega)$	4.9	6.2	16.4	7.0
$C_{gs}(pF)$	0.39	0.31	0.12	0.27
$R_{ds}(\Omega)$	209	265	703	300

The main causes for the lower gain of the 3-stage as compared to the 4-stage example is that there exists an insufficient number of FETs and Ω_{1dB} approaches unity. The latter implies that the widths can no longer be increased since this would result in a decrease in cut-off frequency and in turn ω_{1dB} .

For the 5-stage example, the extra transistor results in a lower ω_{1dB} mainly due to gate line losses and therefore requires that the gain be less frequency-dependent. This is accomplished by increasing the cut-off frequency at the expense of gain due

to the resultant decrease in FET width.

3.3.6(c) Procedure for $n > 5$

To obtain the optimum performance for 5 stages or more, one is not required to plot curves for $n > 5$. One simply follows the same procedures as for $n = 5$, including using Fig. 3.16, except that k_n is multiplied by

$$\frac{n^2}{25}$$

The remaining parameters can be extracted by following the standard procedures as described in Section 3.2.4. This can be extended to larger values of n simply because of the characterization of the distributed amplifier in terms of the parameters a , b , n and Ω which for large values of n cause expression (3.3.66) to be practically independent of the number of stages. Also, expression (3.3.55) is a simple function of n and therefore can be used without excessive computations. This permits the analysis of the frequency response for values of n larger than 5 with only 3 graphs.

3.3.6(d) Comparison with SUPER-COMPACT Analysis

The frequency response of the analytically-optimized 4-stage distributed amplifier using the FET intrinsic parameters previously obtained is shown in Fig. 3.17. Also shown is the frequency response of the identical amplifier (also excluding inductor losses) as analyzed using SUPER-COMPACT where the optimum width was found to be $350\mu\text{m}$. This value compares favorably with the $339\mu\text{m}$ width obtained analytically. The frequency response agrees within 1 dB with the analytical prediction except for frequencies below 5 GHz. This discrepancy is due to the approximation made to the low-frequency characteristic impedance of the drain line. This approximation is deemed appropriate simply because of the good mid- and upper-frequency agreement. As a comparison, the non-optimized gain obtained by Beyer et al. [87] is also given to demonstrate the improvements achieved through

the use of the optimization technique. An improvement of 1 dB was attained over their design.

Becker et al. [89] have presented an extension to their original theory (Beyer et al. [87]) whereby from the gain and 3-dB cut-off frequency design requirements and the selection of the number of stages one can derive the necessary FET intrinsic parameters. In other words the gate and drain lines are not designed around the already-existing FET manufacturing process but rather the other way around. Thus the characteristic impedances and cut-off frequencies of the lines are considered to constrain the FET intrinsic parameters so as to result in the required frequency response. This design technique requires the FET to be specifically tailored. The task of designing an FET from its intrinsic parameters is not a trivial one and therefore seems to be an inappropriate way of arriving at the optimum amplifier design. A more practical design approach is to use the existing FET manufacturing process and derive the gate width that optimizes the amplifier's performance. This is the basis of the theory presented in this chapter.

3.4 Tapering and Mismatching

3.4.1 Introduction

The previous section showed how the maximum available gain of a distributed amplifier can be achieved by optimizing the active channel width of the FETs. The resultant amplifier comprised gate and drain lines constructed of identical and cascaded T-sections and image-impedance-matched terminations, all having characteristic impedances equal to those presented by the frequency-dependent impedances of the generator and load.

In this section the effects on gain and port reflections due to tapering and mismatching of the gate and drain lines will be discussed. A distributed amplifier circuit model is proposed in which an algebraic definition of tapering and mismatching is defined. This forms a basis for the explanation of the observed increase in

Figure 3.17 Comparison of Frequency Characteristics Obtained from Beyer[87], SUPER-COMPACT, and Graphical Method.

gain.

3.4.2 Definition of Tapering and Mismatching

The proposed distributed amplifier circuit model that will give insight into the causes and effects of tapering and mismatching is shown in Figure 3.18. The amplifier consists of 4 stages each having identical, unilateral, and lossy FETs. Although the analysis is restricted to this number, the resultant frequency responses are also applicable to other numbers. Also, it was not considered necessary to incorporate results for other numbers since this would be quite repetitive and therefore not very productive in clarifying the salient features of tapering and mismatching.

On the other hand, FET losses contribute considerably to degradations in gain and must therefore be included. Since there are an infinite number of values for R_i and R_{ds} , one is forced to narrow the possibilities to specific values. The gate and drain attenuation parameters of the FET were constrained to be $\alpha_g = 0.2$ and $\alpha_d = 0.1$, respectively. Typically, for gate and drain line characteristic impedances of 50Ω , this represents an FET with $R_i = 10\Omega$ and $R_{ds} = 500\Omega$. These are typical values for FETs in distributed amplifiers having input and output port characteristic impedances of 50Ω .

The input and output ports are terminated by frequency-independent resistive terminations supplied by the generator and load terminations, respectively. The magnitudes of these terminations are assumed to be constant (i.e. independent of the DA's tapering and mismatching) and equal to each other.

Tapering is defined here as a progressive increase or decrease in 'intermediate' characteristic impedance of an artificial transmission line as one travels along the line towards its termination. The gate and drain lines, as was seen in the previous section, can be viewed as being constructed of cascaded ('intermediate') T-sections. If these sections have their ports image impedance matched and are analyzed individually, one finds that the impedance (at low frequencies) of each section is

Figure 3.18 4-Stage Distributed Amplifier Model Including Taper, Mismatching, and Lossy Unilateral FET Model.

$$\sqrt{\frac{L}{C}}$$

where L is the total inductance of the series-arms and C is the shunt-arm capacitance. One can see that upon increasing L , the characteristic impedance increases. Similarly, this also holds true if C decreases. Generally, by varying these parameters independently from section to section, one can tailor the 'intermediate' characteristic impedances along the line to suit one's needs. There is an optimum configuration which maximizes the performance of the distributed amplifier. This optimum configuration is described as follows.

Initially, consider the drain line, since it is the simplest line to understand. The gain equation (3.3.34) of an untapered distributed amplifier shows that its gain is proportional to the drain line characteristic impedance. In other words, one can achieve greater gain by simply increasing the drain-line's characteristic impedance. However, the increase in impedance will cause a mismatch to the load impedance and create undesirable reflections, which for cascaded amplifiers results in a degradation in gain flatness. Therefore, one is obliged to opt for a compromise in which some of the 'intermediate' characteristic impedances are selected to increase gain while others are selected to achieve better matching to the load.

It has been found through the use of SUPER-COMPACT that the optimum design is to have the 'intermediate' characteristic impedances gradually increase in magnitude as one recedes from the load impedance. The reason for this is that the T-sections furthest away from the load can be permitted to have larger characteristic impedances (and thus contribute to increasing the gain), while the T-sections joining them to the output load perform some sort of impedance matching similar to that encountered in a tapered-transmission-line transformer. Although the T-sections closest to the load do not contribute as much to the amplifier's increase in gain as the other T-sections do, they contribute significantly to the improvement in matching to the load impedance.

Another way of increasing the gain is simply to increase the impedance of

the load in unison with that of the drain line, thus minimizing, if not eliminating, reflections. Unfortunately, this is not always a possibility since system specifications can impose restrictions which prevent any such increase.

For the case of the gate line, as has been found for the drain line, tapering does improve input matching. It has been found that the optimum configuration, in most instances, has the 'intermediate' characteristic impedance increase as one approaches its termination impedance.

Figure 3.18 shows the schematic of the distributed amplifier model used in the analysis of the effects of tapering and mismatching. These effects are specified using, respectively, the parameters τ and m . For mismatching the overall characteristic impedance of each intermediate section increases as the square of m . This also includes the line termination. Tapering has a similar effect except for those inductors furthest away from the line termination. Here, these inductors decrease in magnitude with increasing τ .

The shunt-arm capacitor values are kept constant since it has been found from simulations that little can be gained by the tapering of the widths of the FETs along the longitudinal axis of the DA.

In summary, the tapering of the line such that the 'intermediate' characteristic impedances increase as one approaches the termination side of the line has four beneficial effects. First, it increases the gain through an increase in characteristic impedance along the line. Secondly, the intermediate sections away from the termination behave analogously to a tapered-transmission-line transformer, thus reducing the increased mismatching created by the previous increase in impedance. Thirdly, since the impedance seen by the FET looking towards the termination is greater than the impedance seen looking towards the load, a greater portion of the current generated by each FET will manifest itself as a more pronounced forward-travelling wave as compared to the reverse-travelling wave. And fourthly, if the inductance of the series-arms is increased, the frequency at which the characteristic impedance peaks will decrease and hence create an increase in gain at a

lower frequency than the cut-off frequency of the original untapered line. These four points demonstrate the intricacies involved in a more detailed understanding of the distributed amplifier.

3.4.3 Tapering and Mismatching Simulations

This section presents the results of simulating a 4-stage distributed amplifier. The schematic of the distributed amplifier model was given in Figure 3.18. In the simulations all the circuit elements are normalized to the characteristic impedance of the lines and the cut-off frequencies of the lines. The circuit elements are normalized to the parameters

$$Z_o = \sqrt{\frac{L}{C}}, \quad (3.4.2)$$

and

$$\Omega = \frac{\omega}{\omega_c}, \quad (3.4.3)$$

where

$$\omega_c = \frac{2}{\sqrt{LC}}. \quad (3.4.4)$$

An important point is that all of these parameters are independent of the parameters τ and m . The parameters ω_c and Z_o are respectively the cut-off frequency and the characteristic impedance of an untapered and unmismatched distributed amplifier at dc. Algebraically, the latter is equivalent to

$$Z_o = Z(\omega, m, \tau, \alpha_g, \alpha_d) |_{\omega=\alpha_g=\alpha_d=0, m=\tau=1.0}$$

where $Z(\omega, m, \tau, \alpha_g, \alpha_d)$ is the characteristic impedance of the line as a function of the parameters ω , m , τ , α_g , and α_d .

Rearranging equations (3.4.2) through (3.4.4):

$$C = \frac{2}{Z_o \omega_c}, \quad (3.4.5)$$

$$L = \frac{2Z_o}{\omega_c}, \quad (3.4.6)$$

and

$$Y_o = \frac{1}{Z_o}. \quad (3.4.7)$$

In turn, one can arrive at the impedances of the circuit elements to obtain

$$\begin{aligned} Z_{gs} &= R_i + \frac{1}{j\omega C} \\ &= Z_o \left(\alpha_g + \frac{1}{j\Omega 2} \right), \end{aligned} \quad (3.4.8)$$

$$\begin{aligned} Y_{ds} &= G_{ds} + j\omega C \\ &= Y_o (\alpha_d + j\Omega 2), \end{aligned} \quad (3.4.9)$$

$$\begin{aligned} Z_l &= j\omega L \\ &= j\Omega 2 Z_o \end{aligned} \quad (3.4.10)$$

$$\begin{aligned} Z_{l/2} &= \frac{Z_l}{2} \\ &= j\Omega Z_o. \end{aligned} \quad (3.4.11)$$

where α_g, α_d, R_i , and G_{ds} are related to FET losses and have been defined in Section 3.3.3. Z_{gs} and Y_{ds} are the effective input impedance and output admittance of the FET, respectively. The series-arm inductors have a reactance of Z_l except at the line extremities where they are $Z_l/2$. And lastly, we have constrained the gate and drain capacitors of the FET to be equal (as was seen in section 3.3.3).

If one tries to obtain an algebraic expression for the frequency characteristics of a 4-stage distributed amplifier using equations (3.4.2) through (3.4.11), one quickly realizes that the solution cannot be simplified to any reasonable form that might

disclose the amplifier's internal workings. For example, the gain equation is found to contain more than 200 terms. Therefore one has to rely on software tools to extract the necessary information to obtain a clear understanding of the internal workings of the amplifier. This results in Figures 3.19 through 3.24 in which (excluding Figure 3.19) the horizontal axis refers to the parameter τ and the axis going into the page refers to the parameter m .

These figures describe, respectively, as a function of tapering and mismatching, the normalized 1-dB roll-off gain, Ω_{1dB} , normalized GBW (gain-bandwidth product), and passband-averaged input and output reflection coefficients. Figure 3.20 depicts the bandwidth effects due to tapering and mismatching. Circled grid points indicate for which values of τ and m the gain and bandwidth are greater than for the untapered and unmismatched case (i.e. $\tau = m = 1$). The doubly circled point refers to the latter case. Normalized-gain ($\overline{\text{Gain}}$) is defined here as the gain normalized to that of a 4-stage lossless DA with $\tau = m = 1$. The normalized-gain-bandwidth product is defined to be the product of Ω_{1dB} and $\overline{\text{Gain}}$.

One can deduce from the group of points which exhibit greater gain and bandwidth that the normalized 1-dB bandwidth increases with mismatching for values up to 1.4. This corresponds to gate and drain line termination impedances up to 70Ω for a 50Ω system. Within this same group, an increase in τ up to 1.1 also has the same effect except for $\tau = m = 1.1$. This is also true even for values of τ less than 1, although this is restricted to a relatively smaller range.

The bandwidth is particularly sensitive to degradation for $\tau > 1.1$. This does not imply that gain has decreased, especially at the higher frequencies. If anything, the contrary is true, i.e. the gain increases. The apparent bandwidth reduction is simply due to the fact that the bandwidth is specified by the 1-dB roll-off frequency and not by the absolute gain. What is actually happening is that (referring to Figure 3.19) the high frequency gain does not increase appreciably compared to the gain at lower frequencies. Since the high frequency gain does not increase concurrently with the low frequency gain and the bandwidth, as defined here by its 1-dB drop, the

Figure 3.19 Normalized Gain Versus Frequency for Various Values of τ and m , for $n=4$.

Figure 3.20 1-dB Bandwidth as a Function of r and m , for $n=4$.

Figure 3.21 Normalized Gain as a Function of τ and m , for $n=4$.

Figure 3.22 Normalized Gain-Bandwidth Product as a Function of τ and m , for $n=4$.

Figure 3.23 Average of Passband $|S_{11}|$ as a Function of τ and m , for $n=4$.

Figure 3.24 Average of Passband $|S_{22}|$ as a Function of r and m , for $n=4$.

bandwidth is seen to decrease. From this, if one ignores the 1-dB roll-off definition of bandwidth and defines it as the frequency range over which the gain is greater than a pre-specified amount (such as for $\tau = m = 1.0$), one then does not observe this drastic decrease in bandwidth. Instead, one finds that the bandwidth hardly decreases with increasing in τ .

If one is primarily interested in increasing bandwidth, then the choice $m = 0.6$ and $\tau \leq 1.0$ results in a bandwidth increase from 0.56 to 0.7, which represents a 25% improvement. Unfortunately, a corresponding decrease in gain from 0.56 to 0.43 (23%) also results; as can be seen in Figure 3.21 which presents the normalized gain as a function of τ and m . From this figure a simple relationship between gain, tapering and mismatching is found. Gain is in general a simple monotonically increasing function of these two parameters. In other words, it is desirable to increase these parameters indefinitely if gain is the underlying goal. Of course, as previously shown, bandwidth does not improve for extreme values of τ and m .

At the other extreme, where the bandwidth increases, gain experiences considerable degradation. Therefore, one has to select an optimum operating point on the $\tau - m$ plane which best satisfies the requirements of the system. For this, Figure 3.22 is useful in this respect. It depicts the effects of τ and m on the normalized GBW product. A maximum value of 0.60 is found while a more realistic value of 0.57 is obtained for $\tau = 1.1$ and $m = 1.4$. This 33% improvement compares favorably with the gain-bandwidth product of 0.43 obtained for the untapered and unmismatched case.

Lastly, the averages of the input and output reflection coefficients are presented in Figures 3.23 and 3.24, respectively. They represent the reflection coefficients averaged out over the 1-dB roll-off bandwidth and not over a fixed and predetermined bandwidth. An important comment that should be made at this point is that it is difficult to pinpoint optimum values of τ and m while remaining realistic, especially when referring to the average of the reflection coefficients. For example, an ultimate minimum in the average of the output reflection approaching 0 can be easily

attained. However, this implies a drastic and unrealistic degradation in gain and bandwidth. Therefore, without going into impractical examples, more meaningful solutions are presented as follows.

Surprisingly, no reduction in input reflection coefficient below what is achievable by the untapered and unmismatched case can be realized without a reduction in gain or bandwidth. The next best thing is a 11% and 14% reduction in bandwidth and improvement in gain, respectively, for an equivalent input reflection coefficient.

On the other hand, the average value of the output reflection coefficient can be improved from 0.10 to 0.07 (30% improvement) for values of τ and m equal to 1.1 and 1.2, respectively, without degrading the bandwidth. For these values of τ and m , an increase in gain and gain-bandwidth product to 0.94 and 0.53, respectively, is observed. This corresponds to a 24% improvement. Coincidentally, this operating point can be viewed as being the optimum operating point (in terms of τ and m) for which the bandwidth, gain-bandwidth product, and the sum of both the input and output reflection coefficients are found to demonstrate the best overall performance as compared to the untapered and unmismatched case.

One finds that for frequencies approaching dc, the gain simplifies to

$$G = 2ng_m Z_o \left(\frac{k}{k+1} \right)^2 \quad (3.4.12)$$

where $k = m^2 \tau^2$. One can readily see that, at the limit of tapering and mismatching when $k \rightarrow \infty$, gain quadruples in value as compared for $k = 1$. Tapering and mismatching cannot increase gain indefinitely. Also, it should be mentioned that at this extremity, the input and output reflection coefficients cannot be maintained within reasonable limits. Therefore, one is compelled to make a compromise between gain and the magnitude of the input and output reflections.

This quadrupling in gain is attributed to two effects. Exactly half of this quadrupling is created by the gate line while the other half is due to the drain line. In both instances, the doubling of the signal as it propagates along the lines results

from the gradual and monotonic change in the characteristic impedance along the lines and is analogous to what occurs within tapered-transmission-line transformers. For the case of the gate line, the voltage 'wave' increases with the characteristic impedance. For the case of the drain line, the currents generated by the FETs produce forward- and reverse-travelling voltage waves. Due to the greater impedance as seen looking towards the drain line termination by the FET, the forward-travelling wave acquires a greater share of the available current. This translates to a correspondingly larger output voltage as long as the voltage waves generated by the FETs interfere constructively.

3.5 Ultra-Broadband Splitter and Combiner

An interesting extension to the basic distributed amplifier circuit is shown in Fig. 3.25 and is referred to as a DISS (Distributed Signal Splitter). This new type of splitter has also been arrived at independently by others [90,91]. It comprises two distributed amplifiers sharing a common gate line with the two drain lines providing identical output signals. Due to the incorporation of active devices, amplification can be achieved. Conventional signal splitters, such as Lange couplers and Wilkinson dividers, exhibit loss. The frequencies over which this new circuit can be made to operate ranges from as low as dc up to and exceeding 40 GHz. This represents several decades of bandwidth. The main factors limiting the upper frequency are the f_{max} of the FET and inductor losses. The splitter does not have any inherent upper and lower frequency limits of operation. This makes it an ideal candidate for an ultra-broadband splitter. It is capable of producing very flat gain and excellent input and output matching throughout its designed bandwidth.

Due to its symmetrical topology, concurrent phases and amplitudes are produced at the outputs. One can envisage extending the number of outputs to a number greater than two. Through the use of dual-gate FETs and the interconnection of the gain-controlling gates for each port, it is possible to achieve a number of functions. These include both analog and digital demultiplexing, variable sig-

Figure 3.25 Schematic of Ultra-Broadband Distributed Signal Splitter.

nal splitting with voltage-controllable weighting, signal attenuation, and high-speed switching with gain.

The exact analysis of the DISS is extremely lengthy if one includes FET and inductor losses and also feedback effects due to C_{dg} . For this reason a simplified version of the circuit will be analyzed algebraically to bring out its most salient properties. This simplified circuit excludes any losses, forward-feed capacitors, capacitively-coupled gates, and series-drain inductors and assumes that nontapered inductor values are used along the lines with properly matched line-terminations. Drain line shunt capacitors are only used to equalize the phase velocities along the lines. One can show with the help of (2.4.1) that the voltage gain is given by

$$\frac{A_{O_i}}{A_I} = \frac{ng_m Z_d}{2} \quad (3.5.1)$$

where A_{O_i} , A_I , n , g_m , and Z_d are, respectively, the output voltage of i -th port, input voltage, number of stages, transconductance of each FET, and the drain line characteristic impedance. This expression is independent of the number of output ports and frequency.

One can extend the analysis by utilizing

$$g_m = k_{gc} C_{gs}, \quad (3.5.2)$$

$$mC_{gs} = C_{g\text{eff}} = \frac{2}{Z_g \omega_c}, \quad (3.5.3)$$

$$C_{ds} + C_p = C_d = \frac{2}{Z_d \omega_c}, \quad (3.5.4)$$

$$L_g = \frac{2Z_g}{\omega_c}, \quad (3.5.5)$$

and

$$L_d = \frac{2Z_d}{\omega_c} \quad (3.5.6)$$

and assuming identical phase velocities on all lines:

$$\omega_{cg} = \omega_{cd} = \omega_c \quad (3.5.7)$$

to produce

$$\frac{A_{O_i}}{A_I} = \frac{nk_{gc}Z_d}{m\omega_{HF}Z_g} \quad (3.5.8)$$

In general, since $Z_d = Z_g$,

$$\frac{A_{O_i}}{A_I} = \frac{nk_{gc}}{m\omega_{HF}} \quad (3.5.9)$$

where we have approximated

$$\omega_c = \omega_{HF} \quad (3.5.10)$$

and have assumed that

$$C_{ds} < \frac{2}{Z_d\omega_c} \quad (3.5.11)$$

where m is the number of output ports, $C_{g_{eff}}$ is the total gate line capacitance at each stage, C_d is the effective drain line shunt capacitance for each FET, C_p is intentionally added as a phase-velocity equalizing capacitance, and ω_{cg} and ω_{cd} respectively are the gate and drain line cut-off frequencies. An important point resulting from this is that the voltage gain varies inversely with the number of outputs and the upper frequency (ω_{HF}).

One can devise a circuit complementary to the DISS in which the resultant network is referred to as a DISC (Distributed Signal Combiner) and is composed of a number of distributed amplifiers sharing a common drain line. The schematic

of this circuit is presented in Fig. 3.26. Similarly to the splitter, it can be extended to any number of input ports.

The schematic of the DISC shown in Fig. 3.27 incorporates dual-gate FETs and also includes series-drain inductors, forward-feed capacitors, drain line shunt-capacitors and capacitively-coupled gates. It should be noted that the resistors in parallel with the capacitors coupling the gates only serve to supply gate bias and are used only when it is deemed necessary. Although not shown, tapering of the inductor and capacitor values along the lines and also variation of the widths of the FETs can be introduced to enhance the performance of the combiner in general or to suit specific critical needs, such as in applications where very low port reflections are of primary importance and gain flatness can be sacrificed.

Its algebraic analysis can be shown to result in

$$\frac{A_O}{A_{I_i}} = \frac{nk_{gc}Z_d}{\omega_{HF}Z_g} \quad (3.5.12)$$

or in general since $Z_d = Z_g$ then

$$\frac{A_O}{A_{I_i}} = \frac{nk_{gc}}{\omega_{HF}} \quad (3.5.13)$$

if one follows the same procedure as outlined for the DISS. The parameters A_O and A_{I_i} refer to the output voltage and the input voltage of the i -th port, respectively. The difference between these two gain expressions and the ones obtained for the DISS is that they are independent of the number of ports.

Experimental results were first reported by Barta et al. [51] in which a packaged 1-to-11 GHz 2-port splitter composed of lumped spiral inductors and eight MESFETs was constructed. The device exhibited unity gain up to 8 GHz with ± 0.5 dB gain flatness. Gain and phase balance between output ports were better than ± 0.4 dB and ± 1.5 degrees, respectively. Output port-to-port isolation exceeded 24 dB up to 9 GHz while reverse isolation was better than 27 dB. The input and output VSWR's, of a packaged device, were better than 2:1. This level

Figure 3.26 Schematic of Ultra-Broadband Distributed Signal Combiner.

Figure 3.27 Schematic of Improved Ultra-Broadband Distributed Signal Combiner.

of performance demonstrates the potential of active splitters in ultra-broadband applications. Also, experimental results for a combiner assembled with discrete MESFETs have demonstrated 1.5 dB gain over the frequency band covering 2 - 18 GHz [91]. Further improvements should be expected in the foreseeable future.

3.6 Conclusion

A detailed theoretical analysis with the help of MACSYMA (a symbolic algebraic manipulator program) taking into account FET losses has been presented for a distributed amplifier. From this a graphical gain-optimization procedure was obtained from which the optimum number of stages and FET width can be solved for. Excellent agreement between the results presented here and that obtained from a SUPER-COMPACT optimization has been found.

Definitions of tapering and mismatching were presented and served to illustrate their potential effects towards increasing the DA's performance. It was found that they do provide improved performance characteristics by increasing the gain and better matching the input and output ports of the amplifier. Due to a more efficient use of the amplifying potential of the FETs, greater bandwidths can be achieved while maintaining the same gain as a DA without tapering and mismatching.

A brief description and theoretical analysis of ultra-broadband splitter and combiner circuits utilizing the concept of distributed amplification was given. Their potential as broadband splitter and combiner circuits having an arbitrary number of ports has been demonstrated.

Design Considerations

4.1 Introduction

In the previous chapter we have looked at several techniques in which the DA's frequency response can be tailored to suit the designer's needs. Some of the more pertinent performance-improving techniques found in this thesis, such as tapering and width optimization of the FETs, have been analyzed theoretically with certain assumptions made. More specifically, the inductor and FET models have been simplified so as to enable a practical, yet sufficiently accurate theoretical analysis to be carried out. In this section we attempt to go further in the analysis by using the full FET and inductor models available to the circuit designer. The FET model will not only include the gate and drain losses but also the capacitive feedback effects that degrade the high frequency (HF) gain. More importantly, the inductor model will no longer be considered lossless but will include the effects of dc resistance and, more significantly, losses due to skin-effect. The latter will be shown to play a dominant effect (especially at HF) in both gate and drain lines as well as in the series-drain inductors. Unfortunately, because of the complex nature of skin effect, its exact effect on the gain of the DA cannot be treated in simple algebraic terms, hence the need to resort to the use of the less elegant but very accurate analytical techniques. This involves the creation of an inductor model which takes into account the frequency effects. Such a model has to be compatible with currently-existing circuit analysis programs such as SPICE, SCAMPER, and especially SUPER-COMPACT (SC). The latter is particularly important since it is equipped with an optimizer capable of numerically computing the circuit component values such that the amplifier's performance is optimized to the designer's specifications.

4.2 Inductance

This section presents a brief description of the self- and mutual-inductances of conductors differently positioned relative to each other.

As there exist many possible cross-sectional shapes and relative positionings, we direct the reader to an extensive compilation of useful inductance equations [92] and only the most useful ones from this compilation are given in this section. The equations presented here are valid up to approximately 10 GHz for the types of conductors considered here. They do not take into account skin-effect.

The concept of inductance is a very geometrically-dependent one. Nevertheless, certain basic equations can be obtained from simple conductor arrangements. One of these fundamental expressions is

$$M = \frac{l}{5} \left[\ln \left(\frac{l}{d} + \sqrt{1 + \left(\frac{l}{d} \right)^2} \right) - \sqrt{1 + \left(\frac{d}{l} \right)^2} + \frac{d}{l} \right] \quad (4.2.1)$$

and describes the mutual-inductance M (in pH) between two identical, infinitesimally fine, and parallel conductors of length l , separated by a distance d and is shown in Fig. 4.1(a). All physical dimensions used here are in μm unless otherwise indicated.

For two dissimilar but parallel conductors, as shown in Fig. 4.1(b) one obtains

$$M = \frac{1}{10} \left[\alpha \sinh^{-1} \frac{\alpha}{d} - \beta \sinh^{-1} \frac{\beta}{d} - \gamma \sinh^{-1} \frac{\gamma}{d} + \delta \sinh^{-1} \frac{\delta}{d} - \sqrt{\alpha^2 + d^2} + \sqrt{\beta^2 + d^2} + \sqrt{\gamma^2 + d^2} - \sqrt{\delta^2 + d^2} \right] \quad (4.2.2)$$

where $\alpha = l + m + \delta$, $\beta = l + \delta$, $\gamma = m + \delta$.

This equation is particularly useful for the determination of the mutual inductance between two arbitrarily positioned rectangular inductors by summing up each individual contribution. It should be mentioned that these previous equations are, in general, quite accurate for conductors having cross-sectional dimensions up to half

Figure 4.1 (a) Parallel and Identical Conductors.
 (b) Parallel Dissimilar Conductors.
 (c) Self-Inductance of Rectangular Cross-Section.
 (d) Self- and Mutual-Inductance of (a) and (c).

of the center-to-center spacing. An interesting point to note is that the mutual-inductance between perpendicular wires is exactly zero.

Finally, a very useful equation for the determination of the self-inductance of an interconnect with a square cross-section of dimensions B and C and length l is

$$L = \frac{l}{5} \left[\ln \left(\frac{2l}{B+C} \right) + \frac{1}{2} + 0.2235 \frac{B+C}{l} \right]. \quad (4.2.3)$$

For example, Fig. 4.1(d) shows the theoretical self-inductance of a 10- μm -wide and 1- μm -thick conductor ($B+C=11$). These expressions were utilized during the layout of the distributed amplifier presented in this research work.

The equivalent circuit model of the lossy spiral inductor extensively used throughout this chapter is given in Fig. 4.2 and consists of lumped resistors, capacitors, and lossless inductors. The model is based on the original theory given by Wheeler [93] on the modeling of the skin-effect of coaxial cables, and afterwards adapted to spiral inductors [103]. The model values (for the numerous standard-cells available) have been obtained empirically since the accuracy obtainable from fundamental theory was found to be inadequate [103]. To obtain the necessary accuracy it would have necessitated the use of the very computationally extensive, and therefore impractical, finite-element analysis method.

4.3 SUPER-COMPACT

SUPER-COMPACT (Computerized Optimization of Microwave Passive and Active Circuits) is an extremely useful tool in the analysis and design of linear microwave circuits. It is a circuit analysis program capable of computing the frequency responses of a variety of circuit topologies composed of passive and active elements. In some respects it is very similar to commonly available software packages such as SPICE. What distinguishes it from these circuit analysis programs is that it has a very useful optimizer capable of computing the parameter values so as to optimize the overall performance of the circuit under analysis.

Figure 4.2 Lossy Spiral Inductor Model.

The optimization and analysis capabilities of SUPER-COMPACT were extensively used throughout this research work. For this reason, a brief description of the program's 'error function' follows. Details of the internal-workings of SUPER-COMPACT can be found in its User Manual [94].

The 'error function' describes a weighted difference between the simulated performance and the targeted performance of the circuit being optimized. The performance can be specified using a number of parameters such as gain, S_{11} , and noise-figure, just to name a few, over the frequency band of interest. An 'error' value results describing the degree of discrepancy between the simulated and targeted objectives. From this value a gradient or random optimizer selects circuit element values such that this 'error' is minimized. Once the 'global minimum' is achieved, the performance of the circuit under investigation is said to be optimized. Difficulties arise when there exist several 'local minima' as this may complicate the process and lengthen the time taken to arrive at the optimum circuit.

A typical error function is of the following form:

$$E = \frac{1}{n} \sum_{f_1}^{f_n} \left[w_1 |S_{11}|^2 + w_2 |S_{22}|^2 + w_3 \left| \frac{1}{S_{21}} \right|^2 \right] \quad (4.3)$$

where

E = error,

n = number of frequencies,

f_1 = first frequency,

f_n = last frequency,

w_1 , w_2 , and w_3 are user-supplied weighting factors,

S_{11} , S_{22} , and S_{21} are the parameters to be optimized.

4.4 DA Analysis with SUPER-COMPACT

In this section different configurations of the DA are analyzed using more com-

plete FET and inductor models than were employed in the previous chapter. These models represent the most complete ones available and are based on measurements done on test wafers.

The aim of this section is to devise different practical DA configurations which enable the frequency response to be tailored to the designer's needs. Different configurations include tapering, forward-feed, number of stages, and FET width, just to name a few.

The schematic of a 4-stage DA was shown in Fig. 2.5. It includes the tapering of the gate and drain lines as well as series-drain inductors. Also, drain-line shunt capacitors and forward-feed capacitors are included in the DA model so that their usefulness may be fully characterized. Although the inductors are represented by lossless inductor symbols, they are in fact modeled in SC in terms of their full equivalent circuits. This SC inductor model is further explained in the previous section and is based on measurements of standard cells.

All the transistors, unless specified otherwise, are modeled from $1\ \mu\text{m} \times 150\ \mu\text{m}$ GaAs MESFETs available at Bell-Northern Research (BNR). Throughout this thesis they are assumed to be biased at $V_{gs} = 0\ \text{V}$, $V_{ds} = 2.5\ \text{V}$, and $I_{ds} = 20\ \text{mA}$ unless indicated otherwise. Similarly, the DAs are assumed to be biased at $V_i = 0\ \text{V}$, $V_o = 2.5\ \text{V}$, and $I_o = 80\ \text{mA}$ unless indicated otherwise.

The SC circuit description of the DA used throughout this chapter is given in Appendix 4. It is used to analyze the frequency response of the DA taking into account the following effects:

1. gate line taper
2. drain line taper
3. series-drain inductors
4. tapering of series-drain inductor values
5. drain-line capacitors

6. tapering of drain-line capacitor values
7. forward-feed
8. tapering of forward-feed capacitor values
9. tapering of FET widths
10. number of stages (FETs)
11. FET width optimization
12. FET intrinsic-parameter variations
13. amplifier bandwidth
14. inductor losses

These effects are analyzed individually and in combination in the following section to determine their advantages and disadvantages. From the frequency responses obtained, the optimum configuration is selected.

4.5 The Effects of Tapering and Forward-Feed

In the previous chapter the effects of tapering and mismatching have been investigated theoretically using a simplified algebraic approach so as to achieve an overall understanding of their salient effects. In this section the analysis is extended so as to obtain a better and more accurate understanding of the underlying mechanisms that make the DA function and how they can be tailored to a designer's requirements.

To achieve the necessary accuracy, one is obliged to opt for analytical simulations using either a user-written FORTRAN program or better, SUPER-COMPACT. The latter has the advantage in that a designer simply supplies a description of the circuit topology and circuit elements being analyzed as an input file without requiring any knowledge of nodal analysis. We begin the analysis by assuming that the inductors are lossless.

A shorthand notation is used to simplify the labeling of each DA configuration. The labels consist of 6 characters defined as:

G : Gate line,

D : Drain line,

S : Series-drain inductors,

C : drain line shunt capacitors,

F : Forward-feed capacitors,

T () : Tapering of elements specified by the characters within the brackets.

For example, T(GDSF)C means that the DA is composed of gate and drain lines, series-drain inductors, forward-feed capacitors, and drain-line shunt-capacitors. More importantly, all of these elements except for the latter have their values tapered, including the forward-feed capacitors.

The effects due to partial or complete tapering of the inductor values within the DA are shown in Fig. 4.3 for the 1-11 GHz band. Also shown is the effect of forward-feed (FF) when the FF capacitor values are also tapered. The frequency response for a completely untapered DA without series-drain inductors and forward-feed is depicted by the GDC curve.

It should be noted that the gate and drain line resistive termination values are not constrained to equal the dc characteristic impedances of the lines. This is to allow the optimizer to select their optimum values. Typically, the gate and drain line resistive terminations are usually found to be approximately 35Ω and 125Ω , respectively.

The gain of the GDC DA peaks to 7.4 dB at 5 GHz. It then decreases to 6 dB at 11 GHz partly due to drain-line losses incurred by the drain-source shunt-resistance of the FETs (R_{ds}), but is mainly because of the gate-line losses due to R_i . The latter is the usual cause of HF losses in most DA designs found in the literature. This

Figure 4.3 Effects of Taper, FF, and Insertion of Series-Drain Inductors on 4-Stage DA with Lossy FETs and Lossless Inductors.

resistive loss can be generally ascribed to the limited gate-source active channel and gate-finger conductance. Similarly, a reduced low frequency (LF) gain of 6.8 dB is primarily caused by R_d , which effectively shunts the transconductances of the FETs.

If identical series-drain inductors are inserted in series with the drain terminals of the FETs, a 1-dB increase in gain is observed; this effect is shown by GDSC.

An important point to note is that throughout these simulations the error function used in SC is defined so as to prevent the I/O (input and output) reflection coefficients, S_{11} and S_{22} , from exceeding a pre-defined value of 0.2. It is possible to redefine this function so as to force the optimizer to increase the gain at the expense of S_{11} and S_{22} . Similarly, a gain or I/O reflection coefficient improvement can be obtained by sacrificing flatness.

A technique to further increase the gain by 1 dB is to taper the gate and drain lines, and the series-drain inductors while maintaining the drain-line shunt-capacitors untapered. The corresponding frequency response is given by T(GDSC)C which shows a similar flatness in gain as is demonstrated by GDSC. By also allowing the drain-line shunt-capacitors to taper one obtains a further increase in gain to 9.8 dB and a slight improvement in flatness as exhibited by T(GDSC). A final gain of 10.9 dB can be extracted out of the 4 FETs at the expense of flatness by introducing forward-feed. This is shown in Fig. 4.3 as T(GDSCF). Excellent flatness is achieved in the low and mid frequencies while the slight degradation at HF is probably caused by the reverse-travelling voltage signal on the drain line interfering destructively close to the drain-line termination. Any remaining uncanceled part of the reverse wave can be fed back into the gate terminals of the first and second FETs and then re-amplified to constructively or destructively interfere with the output wave, causing the highly frequency-sensitive gain at HF.

One way to greatly reduce this effect is to connect the FF capacitors directly to the drain terminal of the FETs instead of to the adjacent drain-line nodes. Hence, the reverse travelling wave has to flow through an extra series-drain inductor, and

therefore its magnitude is expected to be attenuated (especially if the inductor is lossy). This decreases the injection of the reverse-travelling signal on to the gate of the FET and therefore reduces unwanted feedback. More importantly, the HF signal (emanating out of each FET and directed towards the gate of the following FET) avoids going through this inductor and therefore the unattenuated signal can be directly fed to the following gate through the FF capacitor. Thus the technique of connecting the FF capacitors to the drains of the FETs, instead of to the adjacent drain line nodes, has a two-fold advantage. This novel concept has not been previously reported in literature and is the first reported case of its kind.

The effect of increasing the number of stages of a fully tapered DA T(GDSCF) for the 1-12 GHz band is given in Fig. 4.4. The gain is found to increase from 10.2 dB through 11.8 dB to 13.6 dB for 4, 5, and 6 stages, respectively. This represents a 3.4 dB increase in gain by simply inserting 2 extra stages. Presented in Fig. 4.5 is a plot of gain vs. the number of stages where one finds a 1.7 dB/stage relationship. From this, one can estimate the achievable gain for greater than 6 stages.

4.6 Frequency Response with Lossy Inductors

The potential of increasing gain through the use of FF, tapering, and the insertion of series-drain inductors has been introduced. We here present results of numerical simulations supporting the hypothesis that through the use of FF one can further increase the number of FETs and, hence, the gain beyond what is achievable without FF. Unfortunately, because of drain line losses and the high-pass filter characteristic of FF, the LF gain cannot be increased indefinitely. It has been found in the previous chapter that the maximum LF gain (as the total gate periphery of the FETs approaches infinity) is $A_o = k_{gm} k_{R_d}$ for an untapered DA (see Section 3.3.5.1 for the definition of these parameters).

In the previous sections we have seen the significant increases in gain through the use of FF and tapering. In this section we show the disastrous effects on gain when one uses manufacturable MMIC spiral inductors (available as standard cells).

Figure 4.4 Frequency Response in Terms of the Number of Stages, for T(GDSCF) Type DA.

Figure 4.5 Gain Versus Number of Stages, for T(GDSCF) Type DA.

These inductors exhibit significant losses above 6 GHz due to skin-effect, which in turn are due to a limited dc conductance of the $10\ \mu\text{m} \times 2\ \mu\text{m}$ cross-sectional area of the gold conductor. Typically, the effective resistance of the inductors triples as the frequency is increased from dc to 12 GHz. These inductors vary in physical dimensions from $50\ \mu\text{m} \times 50\ \mu\text{m}$ to $200\ \mu\text{m} \times 200\ \mu\text{m}$ and are of the "air-bridge" type, i.e. they are suspended in air above the substrate by posts so that the capacitive coupling between conductors is reduced.

In Fig. 4.6 the frequency response of a completely lossless and untapered DA without FF is given (see curve GDC). Also presented are the effects due to lossy FETs and lossy inductors. The gain of the lossless amplifier increases monotonically as the cut-off frequency of the gate line is approached. The use of lossy FETs results in a decrease in gain especially at HF where approximately 4 dB are lost. When inductor losses are included, the gain drops even further to 2 dB at 12 GHz (this represents an 8 dB reduction).

Clearly the latter situation exhibits an intolerable gain reduction and therefore requires careful attention during the design phase of the DA.

4.7 Forward-Feed and Tapering of the Lossy Inductors

A possible solution to this problem is to taper the inductors on the gate and drain lines as well as the series-drain inductors. The effects on the frequency response due to the tapering of the gate and drain lines and also the drain-line shunt-capacitors are shown in Fig. 4.7. Although there is an increase in gain due to the tapering of the drain-line shunt-capacitors, a greater increase (especially at HF) can be achieved through drain-line tapering. On the other hand, by allowing both the gate and drain lines to taper one achieves a 2 dB increase.

Two other solutions exist: the insertion of series-drain inductors and FF capacitors. The corresponding results are plotted in Fig. 4.8, respectively, as GDSC and GDSCF. Although the former does not significantly increase the HF gain, this

Figure 4.6 Frequency Characteristics Effects due to FET and Inductor Losses, for GDC Type DA.

Figure 4.7 Gain Effects due to Tapering of GDC Type DA.

can be overcome by tapering both the gate and drain lines as will be shown further in this section. Even though the 12 GHz gain does not seem to be much better (due to insufficient "weighting" put on the gain portion of the error function of the SUPER-COMPACT circuit description), it seems that FF does help increase the gain above 7 GHz. This is demonstrated by the extra 2 dB obtained, compared to the amplifier without FF and series-drain inductors. A greater improvement in gain can be achieved through the concurrent use of FF, series-drain inductors, and tapering of the gate and drain lines than can be achieved by the sum of their individual contributions. The slight drop in gain below 6 GHz can be attributed to negative feedback created by the negative gain of the FET and the feedback loop formed by the FF capacitors and the gate-line inductors. This negative feedback problem is practically non-existent at HF owing to the 'effective' noninverting behaviour of the FET.

One important point is that all of these simulations have the gate and drain line terminations unconstrained. That is, the optimizer selects values so as to minimize the error function, or in other words, these values are optimized so as to improve the amplifier's performance.

We shall now demonstrate the advantages that exist in not only using FF or tapering, but in using both of them concurrently. It will be shown how tapering aids FF tremendously in further increasing the amplifier's gain.

The improved frequency response obtained through the simultaneous use of FF and tapering is depicted in Fig. 4.9. The fully-tapered case includes the tapering of the gate and drain lines, series-drain inductors, drain-line shunt-capacitors and the FF capacitors. Although the amplification attained by full tapering including FF (see $T(\text{GDCSF})$) does not significantly increase the LF gain as compared to the fully untapered case without FF (see GDC) an impressive increase in gain of 6.5 dB at 12 GHz is achieved. This performance is achieved without sacrificing the input and output reflection coefficients, which are below 0.25 across the 1-12 GHz band. The gain and flatness of the amplifier are, respectively, 8.2 dB and ± 0.8 dB across

Figure 4.8 Frequency Response Effects due to Series-Drain Inductors and FF (Nontapered).

the frequency band. These respectable values demonstrate that neither has to be sacrificed at the expense of the other.

The curve for the untapered case with FF is also given. Here one can see the dramatic improvements attributable to tapering over nontapering. The 3 dB improvement in gain at LF magnifies itself to over 6 dB at 12 GHz.

The major sources of gain are presented as follows in decreasing order of importance:

- (1) FF
- (2) drain line taper
- (3) gate line taper
- (4) series-drain inductor taper
- (5) series-drain inductors
- (6) FF capacitor taper
- (7) drain-line shunt-capacitor
- (8) drain-line shunt-capacitor taper
- (9) tapering of FET widths.

The tapering of FET widths is found to increase the gain of the amplifier by less than 0.2 dB. Only one paper has been published to support the use of this type of tapering for the purpose of increasing the gain. This is by Kennan et al. [44] where they have reported reducing the widths of the FETs closest to the input and output ports in order to reduce FET capacitive loading of the lines. It was found that gain could not be increased in this way. The apodizing of the FET widths was used to compensate for the capacitive loading incurred by the wire bonds used to interface to the chip. It can therefore be concluded that FET width tapering does not sufficiently improve the frequency response of a DA to warrant its use. Similarly, the last four items of the list do not affect the DA's performance

Figure 4.9 Gain Effects due to Tapering and FF.

sufficiently to justify their use.

The effects arising from the first four items are given in Fig. 4.10 in which a comparison between tapering of the gate and drain lines (see curve T(GD)C), and the fully untapered case (curve GDC) is presented. An improvement in gain of 2 dB is achieved for frequencies above 11 GHz while the mid-band gain is hardly affected. This frequency-dependent improvement is due to the tapering of the lines and has the effect of violating the phase-velocity matching requirements of the gate and drain lines, hence creating frequency-dependent constructive and destructive interference of the signals on the drain line.

For the case of the curve T(GDCS), a small 1-dB increase in gain at 8 GHz is partly attributable to the tapering of the drain-line shunt-capacitors, but is primarily caused by the addition of tapered series-drain inductors. Although the latter should monotonically increase the gain with frequency, destructive interference (due to differing phase-velocities) results in a lower improvement in gain at 12 GHz. The series-drain inductors reduce the drain-line cut-off frequency, and therefore increase the amount of resonance on the lines, which in turn increase the gain. Although a large increase in gain is not achieved, the 3-dB bandwidth has been improved from 8.5 GHz to 11.4 GHz; this represents a 34% increase.

More importantly, by incorporating FF capacitors, the gain can be tremendously improved as can be seen by the T(GDCSF) curve. Although the FF capacitors have been allowed to taper in value, it has been found that this hardly has any effect on the amplifier's overall gain.

Since it has just been shown that the only way to achieve a reasonable 8-dB gain with less than ± 0.9 dB deviation across the 1-12 GHz band is through the use of tapering and FF, a more detailed analysis concentrating on a "fully tapered" DA with FF is presented in the following section.

Figure 4.10 Series-Drain Inductor, Tapering, and FF Effects on the Frequency Response.

4.8 Design Considerations for a Fully Tapered DA with Forward-Feed

This section extends the analysis to a more specific DA configuration, namely a fully tapered DA with FF. The amplifier includes gate and drain line inductors, and series-drain inductors, and FF, but does not include drain-line shunt-capacitors, all of which have their values tapered. These capacitors were excluded because it has been found that they do not bring about an improvement in the gain or in the input/output reflection coefficients. It is generally found that these inductor and capacitor values monotonically increase or decrease in value along the longitudinal axis of the DA. For example, gate-line inductors and drain-line shunt-capacitors (when used) increase in magnitude as one progresses towards the output port. On the other hand, the drain-line and series-drain inductors progressively decrease in value as one approaches the output. One can conclude from this that in (since the characteristic impedance increases with inductance and is inversely related to capacitance) the gate-line, and especially the drain-line, characteristic impedances increase as the terminations of the lines are approached. Also agreeing with this fact is that the drain-line termination resistor has a value exceeding the characteristic impedance of the drain-line's T-section closest to it. On the other hand, the gate-line termination does not conform to this rule of thumb. This exception results from the termination's greater effect on the input reflection coefficient than on the amplifier's gain.

4.8.1 Number of Stages

The effect of the insertion of extra stages on the gain of a fully tapered DA with FF of the T(GDSF) type is depicted in Fig. 4.11. The procedure used to obtain the frequency response of the 3-, 4-, 5- and 6-stage amplifiers was to allow SC to determine the optimum inductor and capacitor values to minimize the error-function. This error-function was selected in such a way so as to maximize gain

as much as possible while ensuring that the magnitudes of the input and output reflection coefficients did not exceed 0.25, and at the same time guaranteeing that the fluctuations in gain did not exceed 1 dB over the frequency band. The latter required a considerable effort on the part of the designer and computer in error-function weight tweaking and number crunching, respectively. Typical optimization runs included 8 gradient optimizations, each solving for 20 variables and consuming some 60 seconds of CPU time on a large mainframe computer.

It is seen that for a constant bandwidth of 12 GHz, gain increases monotonically with the addition of extra stages for at least up to 6 stages. The use of FF allows an increase in the number of stages beyond the optimum number for DAs without FF. Except for the 6-stage design (where so many feedback paths exist) the remaining amplifiers demonstrate a considerable degree of flatness. That is, maximum fluctuations in gain are less than 2 dB.

In Fig. 4.12 the average gain across the 12 GHz band is plotted as a function of the number of stages. Also shown is a line interpolating these points with a 1.5 dB/stage slope. The good linear fit demonstrates the potential of the DA with respect to increasing gain by the simple addition of stages to both ends of the amplifier.

4.8.2 Gain Versus Bandwidth

Another design consideration is the effect of bandwidth on gain for a four-stage DA with constant-width FETs. The amplifier chosen comprises four identical FETs each 150 μm wide. As for the previous analysis in this section, this amplifier is also fully tapered including the FF capacitors, and also excludes drain-line shunt-capacitors. The frequency responses for 9 GHz, 10 GHz, 12 GHz, and 14 GHz are presented in Fig. 4.13. As described earlier in this section, similar guidelines were used to ensure that the input and output reflection coefficients and gain flatness were kept within imposed limits. The results indicate that gain fluctuations of less than 2 dB are attainable in the pass-band, and better than 1 dB for designs

Figure 4.11 Frequency Response Versus the Number of Stages of T(GDSCF) Type DA.

Figure 4.12 Gain Versus the Number of Stages
T(GDSCF) Type DA.

having moderate gains on the order of 8 dB or less. The accompanying diagram, Fig. 4.14, presents a summary of the previous results in which the average gain in the pass-band is plotted against the designed bandwidth. The resultant points are then interpolated with a straight line having a -0.9 dB/ GHz slope. From this line one can extrapolate and obtain an approximate estimate of the gains at the two extremities of bandwidth. These two points include the low frequency gain of 18.5dB as the bandwidth approaches zero and, more importantly, the unity-gain bandwidth of 21 GHz.

4.8.3 Bandwidth Versus Number of Stages

The effects on bandwidth due to the number of stages is given in Fig. 4.15 for the 3-, 4-, and 5-stage examples. The restrictions on the input and output reflection coefficients and the gain flatness were identical to one ones previously used. The only exception to this is the optimization of the gain; here a minimum gain of 5 dB was required across the specified frequency-band. Of course, fluctuations in gain were kept well below 1 dB. The maximum achievable bandwidth was obtained by modifying the SC command within the circuit listing that specifies the bandwidth over which the optimization is to be done. One obtains the maximum achievable bandwidth for a minimum 5 dB gain by iteratively increasing the upper frequency and optimizing the circuit until the minimum gain across the frequency band drops below 5 dB.

The results indicate that by increasing the number of stages the bandwidth increases. There seems to be an ultimate limit to the upper frequency achievable as the number of stages reaches 5. This seems to indicate that because of accumulative losses incurred by the FETs and inductors, and due to mismatching between the FET and the gate and drain lines, the maximum achievable bandwidth for which a minimum of 5 dB gain can be maintained is 15.2 GHz.

Figure 4.13 Frequency Response Versus Bandwidth, for T(GDSCF) Type DA.

Figure 4.14 Gain Versus Bandwidth,
for T(GDSCF) Type DA.

Figure 4.15 Bandwidth in Terms of the Number of Stages,
for T(GDSCF) Type DA.

4.8.4 Gain Versus FET Width

Another design consideration is the effect on gain of FET width. One would expect the gain to increase with FET width W due to a proportional increase in g_m as predicted by first-order theory, which assumes a lossless DA (some of the parameters presented here are described in greater detail in Section 3.3):

$$A = \frac{g_m Z_d n}{2} \quad (4.8.1)$$

and also

$$g_m = k_{gm} W \quad (4.8.2)$$

so that

$$A = \frac{k_{gm} W Z_d n}{2} \quad (4.8.3)$$

This expression is valid for operating frequencies less than the cut-off frequency of the gate and drain lines. One can show from this expression and the following three equations:

$$Z_d = \sqrt{\frac{L_d}{C_d}}, \quad (4.8.4)$$

$$C_d = k_c W, \quad (4.8.5)$$

$$L_d = \frac{2Z_d}{\omega_c}, \quad (4.8.6)$$

and setting

$$\omega_c \approx \frac{3\omega_{1dB}}{2} \quad (4.8.7)$$

that

$$A = \frac{2k_{gm}n}{3k_c\omega_{1dB}} \quad (4.8.8)$$

and

$$\omega_c = \frac{2}{Z_d k_c W} \quad (4.8.9)$$

if the gate and drain line cut-off frequencies determine the maximum operating frequency, which is generally the case. Since k_{gm} and k_c are constants, then one finds from (4.8.8) that the gain is inversely proportional to the 1-dB roll-off frequency ω_{1dB} . The increase of FET width W not only increases the gain but also unavoidably reduces the bandwidth by a proportional amount. This can be obtained algebraically from (4.8.8) which shows that the gain-bandwidth product is

$$GBW = A\omega_{1dB} = \frac{2k_{gm}n}{3k_c} \quad (4.8.10)$$

and is a constant value (for a fixed n). Therefore any increase in gain due to a widening of the width of the FET, will be at the expense of bandwidth.

When analyzing the FET width effects on gain, one cannot therefore view the problem with the intent of keeping the bandwidth constant, since for large FET widths it may not be possible to attain the desired bandwidth. In Fig. 4.16 the effects on gain due to FET width are presented. As was done for the previous simulations given in this section the input and output reflection coefficients and gain flatness were optimized to a maximum of 0.25, and ± 1 dB, respectively. The frequency band of optimization was empirically selected by determining for each FET width specified the optimum bandwidth over which the amplifier could operate. In other words, the frequency-band of amplification was increased up to a point where the amplifier's overall gain significantly decreased.

Figure 4.16 FET Width Effects on Gain,
for T(GDSCF) Type DA.

For the 100-, 150-, 225-, and 300- μm FET widths it was possible to obtain bandwidths of 14, 12, 10, and 8 GHz, respectively, as expected.

4.8.5 Gain Versus Gain Flatness

A final and interesting design consideration is the relationship between gain and its flatness under the constraints of constant bandwidth, maximum input and output reflection coefficients, and circuit topology. Although the FET widths in this case were allowed to vary independently of each other, it was found that this did not contribute significantly to the amplifier's performance. It has been found that this scheme increases the gain by less than 0.5 dB. Therefore, it was deemed futile to incorporate variable-width FETs into the actual layout described in the following chapter. Fig. 4.17 presents the approximate trade-offs that exist between gain and peak-to-peak fluctuations in gain for a fully tapered DA having FF, of the T(GDSWF) type. This figure is intended to demonstrate the sensitivity that exists between gain and gain flatness, in which a reduction from 2 dB to 1 dB in gain fluctuations reduces the gain by 3.7 dB, i.e. from 11.9 dB to 8.2 dB. This represents a costly reduction of approximately 3.7 dB in gain for each dB improvement in flatness.

4.9 Conclusion

In this chapter the theory of the self-inductance of parallel wires and conductors of rectangular cross-sections has been covered. Also presented was a spiral inductor model which included skin-effect losses.

SUPER-COMPACT simulations of the effects on the DA frequency performance of FET and inductor losses, tapering of the inductor values of the gate- and drain-lines and series-drain-inductors along the axis of the DA, and FF have been presented. It has been shown that FET losses, especially R_i , play a considerable role in the reduction of gain. More importantly, skin-effect losses of spiral inductors have a significant impact on the high-frequency characteristics. Nevertheless, it has been

Figure 4.17 Gain-Flatness as a Function of Gain, for T(GDSCF) Type DA.

shown how these losses can be dramatically overcome through FF, tapering, and the insertion of series-drain-inductors. The simultaneous use of tapering and FF increases the high-frequency gain (at 12 GHz) by more than 6.5 dB as compared to the nontapered case. This means that greater than 7 dB gain, with less than ± 0.75 ripple, over the 1-12 GHz frequency band can be achieved with currently available GaAs MMIC technology.

Finally, the relationship that exists between the DA's gain and its bandwidth, the flatness of the gain, FET width, and the number of stages used has also been presented.

Design and Layout of Distributed Amplifier

5.1 Introduction

In the previous chapter several different DA configurations and their performance have been presented. A specific configuration was selected based on the simulation results. This DA is formed using gate- and drain-line inductors and series-drain inductors, all of which are tapered in value along the DA. FF capacitors are used to overcome degradations in gain created by the losses of these spiral inductors.

This chapter contains a detailed description of the iterative process involved in the layout of the DA based on a GaAs MMIC fabrication technology. The circuit elements forming the DA are discussed in terms of their physical arrangement and their magnetic coupling. The predicted frequency response of the laid-out DA is presented under different bias conditions.

5.2 Description of the Circuit Elements

5.2.1 Standard Cells

Standard cells are used whenever possible for the same reasons as in digital logic design. They alleviate some of the tediousness involved in a layout while facilitating and speeding up the overall design process. More importantly, they reduce if not eliminate human-created design-rule errors which are difficult to avoid and detect. The repertoire of standard cells includes such element types as spiral inductors, FETs, resistors, and MIM capacitors. Because of their sparseness in the amplifier and their simplicity, the last two types of elements were designed completely from

scratch. On the other hand, the first two types were chosen from a vast selection of standard cells from which complicated FET topologies, for example, could be formed. The available basic FET standard-cells had a single $1\text{-}\mu\text{m}$ long gate finger with a gate width ranging from less than $10\text{ }\mu\text{m}$ to more than $150\text{ }\mu\text{m}$. From these, and the use of 1-ME (first level metal) and 2-ME (air-bridge metal), FETs having large gate widths and complex topologies could be created to minimize either area or parasitics. Thus, standard cells allow one to create any desired FET topology without having to experience the difficulties involved in the alignment between different layers.

An important consideration during the layout phase (prior to the submission of the pattern to the mask developers) is that GaAs-based processing is not, as yet, a mature technology as silicon-based processing is, especially in the area of commercially available products. This implies a considerable number of design-rules changes (by the integrated circuit manufacturers) during the design phase. This was experienced during the design of the distributed amplifier in which a change in the specifications expressing the maximum air-bridge span without posts was experienced. This had to be included in the layout by repositioning all posts.

5.2.2 FET Layout

In Fig. 5.1 the layout of the complete 4-Stage distributed amplifier is shown (for a schematic see Fig. 5.3). Fig. 5.2 shows an expanded view of the layout of the FETs found in Fig. 5.1. The device is the result of the side-by-side placement of two identical FET standard cells each having a gate width and length of $80\text{ }\mu\text{m}$ by $1\text{ }\mu\text{m}$, respectively. The resulting FET has the advantage of having a lower effective gate resistance R_i , because it avoids using a single $160\text{ }\mu\text{m}$ -wide gate, of which the first $80\text{ }\mu\text{m}$ would unacceptably attenuate the signal reaching the remaining $80\text{ }\mu\text{m}$. Another advantage is that the two sub-FETs share a common drain terminal and thus minimize C_{ds} . Also, the device is also more area efficient. At the same time, the other intrinsic parameters to the FET such as g_m , C_{gs} , and R_{ds} are not significantly

Figure 5.1 Layout of 4-Stage Distributed Amplifier.

Figure 5.2 Expanded Layout of a Single FET.

affected. Extending this idea further, one can conceive another configuration using four 40 μm -wide FETs interconnected together. Although this arrangement seems appealing, it is not used here since the extra drain and source terminals do not significantly reduce the parasitics to warrant the extra topological complications.

A gate width of 160 μm was selected for three reasons. The first and main reason is that this width offered a good frequency response in terms of gain, S_{11} , S_{22} , and gain flatness. Secondly, it is found that the maximum practical current density permissible on the drain-line is achieved with this particular width. For a total gate periphery of 640 μm this corresponds to a drain-line current (closest to the output terminal) of approximately 80 mA. This current is approximately the maximum current permissible for spiral inductors having 10 μm -wide gold conductors. Finally, to compare differences between tapering and nontapering, a nontapered version of the distributed amplifier was constructed and has been reported elsewhere [49]. This DA included FETs with the same dimensions as the ones used here.

An important characteristic of the FETs is that in the manufacturing process used here, the active-channel formation is intended to produce devices used in digital-logic gates. These FETs have an active-channel doping density and thickness different from FETs designed to operate as analog devices. Typically, for FETs operating as linear devices in analog circuits, the active-channel doping and thickness are $9 \times 10^{16} \text{cm}^{-3}$ and 0.3 – 0.4 μm [43,95], respectively, with a gate pinchoff voltage of -2.3 V. The design objective for these devices is linearity and high power. For a 'digital' device the drain current of the FET must switch between the 'on' and 'off' states with a minimal change in gate voltage. This narrower range of gate voltage necessitates a thinner and more highly doped active channel than is used in an 'analog' device. Typically, this implies an active-channel doping density and thickness of $2.5 \times 10^{17} \text{cm}^{-3}$ and 0.15 – 0.20 μm [96,97], respectively, resulting in a lower pinchoff voltage of -1.5 V. This increased doping is necessary to compensate for the narrower active channel. It also results in a lower gate-to-drain reverse breakdown voltage (and incidentally explains why a lower doping is desirable in

analog FETs).

MESFETs on GaAs substrates can, to some extent, exhibit some active-channel modulation or drift. This is attributable to voltage fluctuations of adjacent active and passive devices residing directly on the GaAs (without having an intermediate isolating dielectric). This phenomenon is commonly known as backgating [98]. It is of some concern to digital circuit designers but is generally of much lesser concern to MMIC designers since devices are usually sufficiently distanced from each other. This situation was found to be the case during the layout of the DA, where it was found that the 700- μm spacing between FETs did not create adverse effects.

The two gate fingers are extended outside the FETs and terminate at gate-metal bonding pads where 1-ME metal forms an electrical contact to it. These gate-metal pads rest directly on the semi-insulating GaAs substrate but have no ion-implanted donors underneath and thus have no space-charge region to capacitively load the gate. On the other hand, since these pads lie directly on the GaAs material, which has a high relative dielectric constant of 12.9 [12], and since the source terminals connected to the ground-bus are close by, there exists a possibility of increasing the gate-to-source capacitive loading. To minimize this parasitic loading, the source-terminal conductors have been laid out to avoid the gate pads as much as possible without excessively narrowing the conductors, as this would increase their series inductance. These conductors are each 120 μm long and 40 μm wide. They have less than 30 pH per conductor and cause a gain-reduction of less than 0.2 dB, at 12 GHz.

The ground-bus to which these conductors are connected is used as a wrap-around-ground instead of using vias. This technique is possible since the distributed amplifier has a relatively simple planar topology which allows the FETs to be placed to one side of the chip. Vias, on the other hand, would not have been very useful for this type of circuit and would have increased the source inductance and added extra processing steps. Wrap-around-ground simplifies the ground connection to the outside world through the use of bond-wires or conductive epoxy [99]. Making

contact to the ground bus is a relatively simple task due to its large size. It has been found to exhibit insignificant reactance even at high-frequencies.

5.2.3 Spiral-Inductors and Interconnect

During the early phases of the layout, one finds that the interconnections, particularly those to the inductors, contribute significantly to additional series inductance and therefore have to be taken into consideration as early as possible in the design. This means that the circuit models used in the simulations have to adequately describe the electrical properties of the corresponding physical elements. Complications arise due to differing electrical characteristics of the spiral inductors and the interconnections because they have unequal inductance-to-resistance ratios. There are two ways to solve this. One solution is to treat the interconnection model separately from the spiral inductor model. The other solution is to devise a function in which the inductance of the interconnect is included in the model for the spiral inductor within SUPER-COMPACT (SC). An 'effective' inductance value L_{tot} (see Section 5.3) results for each spiral inductor within SC. The latter solution was selected here.

Another complication that arises during the layout process is that the spiral-inductor standard-cells (in their original state) exclude conductors to their center and peripheral terminals. This poses the problem that these terminals are not necessarily on opposite sides of the spiral inductor. This complicates the layout process. The actual routing of the 1-ME layer (passing under the air-bridges) from the center terminal is not a major problem, but accounting for the self- and mutual-inductances between this interconnect and the complete spiral inductor certainly is. Because of the possibility of excessive current density in the 1-ME layer of the under-passes of the drain-line spiral inductors, particularly close to the output terminal, care must be taken to ensure that the conductor is not permanently damaged. This problem is alleviated by widening the under-pass as shown in Fig. 5.1.

Whenever possible, the 2-ME layer (air-bridge metal) is widened to minimize

the losses at the highest frequency of operation. Unfortunately, this cannot be done for the spiral inductors since this would alter their inductance. Spiral inductors were not tailored because their low-frequency inductance is very difficult to model. More importantly, high-frequency phenomena such as skin- and distributed-effects are more difficult to analyze.

Distributed effects, in which an undesired phase-shift along a conductor contributes considerably to the per-section phase-shift, are believed to have negligible effects on the amplifier's over-all frequency response. This belief is based on the fact that the conductors are extremely short and have high phase-velocity due to their very high characteristic impedance resulting from the rise of air-bridges and the absence of an intentional ground-plane. The latter point would still be valid even after the intentional addition of a ground-plane since the 500- μm substrate is thick compared to the width of the conductors. This substrate thickness and absence of ground-plane is due to the intentional tailoring of the manufacturing process for 'digital' circuits.

'Distributed' transmission lines were not considered for this distributed amplifier because of the difficulties involved in fabricating them without excessive use of real estate.

For the above reasons, and also because distributed amplifiers with lumped inductors tapered in value along the gate- and drain-lines have not been reported in the literature, it was decided to use lumped spiral inductors instead of 'distributed' transmission-lines. It was found that this was the only solution which would permit all of the passive and active elements to fit within an area of dimensions 2 mm $\times$ 0.75 mm.

An important parasitic is the mutual inductance between conductors. There are three categories to be considered:

- (a) wire-to-wire
- (b) wire-to-coil
- (c) coil-to-coil.

The latter is found to exhibit minimal magnetic coupling and therefore can be considered to have a negligible effect on the frequency response of the amplifier. This is in total agreement with the findings of Strid et al. [68]. Nevertheless, the mutual coupling effects were included in early SUPER-COMPACT (SC) simulations where it was immediately apparent that they could indeed be completely omitted even for spacings approaching $50\text{ }\mu\text{m}$.

The wire-to-coil coupling was analyzed next. It was found that, in most if not all cases, the only coupling that has to be taken into account is for long and/or close conductors. Typically, as a rule of thumb, this involves lengths and spacings of more than $100\text{ }\mu\text{m}$ and less than $75\text{ }\mu\text{m}$, respectively.

Wire-to-wire coupling was found to be the greatest source of mutual inductance. Therefore, special care has to be taken to include the mutual inductance between conductors. But fortunately, in the case of the present distributed amplifier, there existed only a few isolated conductors of sufficient closeness and length to warrant special care. The primary reason for this was that it was decided early in the layout design phase to ensure sufficient spacing between the spiral inductors. This was a precautionary measure in case there were unexpected and unaccounted-for multiple coupling paths between spiral inductors which could result in feedback loops causing oscillations, especially at the high frequencies. Another reason for the spacing between spiral inductors is that the input- and output-port pads had to be positioned close to the edges of the wafer. This pad positioning was intended to facilitate wire-bonding to the chip. This pad position requirement results in the spiral inductor spacing shown in Fig. 5.1.

5.2.4 Forward-Feed Interconnect

Finally, the last interconnect requiring attention is the series-inductance of the FF capacitors. This interconnect, which was omitted in the original simulations, is found to contribute significantly to the impedance of the forward-feed capacitors, especially at the high frequencies. The equivalent circuit which models forward-

feed includes a capacitor and an inductor. The model of the inductor excludes any effects due to metal resistance. This is found to be adequate considering the minimal series resistance of the inter-connect attributable to its short length. An undesirable effect of the interconnect on the forward-feed circuit is to cause a resonant frequency at which the admittance peaks to a large value (dependent on the interconnects resistance) and then gradually diminishes with increasing frequency. In ideal cases where the interconnect inductance can be neglected, this admittance simply increases linearly with frequency without ever decreasing at high frequencies. In other words, the effect of the interconnect is to reduce the 'effective' resonant frequency from infinity to a value dependent on the LC product. This resonant frequency has to be designed so as to avoid any unwanted peaks in gain at all frequencies, particularly in the amplifying band. It has been found that this can be easily obtained by paying careful attention to the magnitude of the forward-feed capacitor and the layout of its interconnect. The behaviour of the latter is more difficult to predict and control. This means that the inductance of the interconnect requires considerable attention.

As seen from the FETs drain terminal, there exist two ways in which the forward-feed capacitor can be connected to the gate terminal of the following FET. The first and most obvious approach is to simply connect a conductor between the terminals and insert a capacitor in series somewhere along it. Although this may appear quite simple, it is important to note that there is a gate-line inductor in the way. One simple solution would be to push the gate-line inductor aside. But because this has to be applied to two other inductors also, the distributed amplifier's chip area would become excessive and yet the series inductance would be significant.

The second approach, and the one adopted in this research work, is to lay out the gate-line spiral inductor in such a way as to use its outer winding as an interconnecting conductor between the forward-feed capacitor and the following gate terminal. Although this approach reduces chip area and makes efficient use

of currently existing conductors, without significantly increasing the inductance of the interconnect, it does complicate modeling of the inductance. This is not to say that the first approach is without its own difficulties. It has been found that both ways impose similar difficulties in accounting for the mutual-inductances between the spiral inductor and the forward-feed interconnect.

The main difficulty in the selected approach is that the forward-feed interconnect forms part of the spiral inductors inductance. That is, the forward-feed capacitor 'taps' into the outer winding of the spiral inductor. This requires that three of the gate-line inductors, namely L_{g2} , L_{g3} , and L_{g4} , have their models modified to account for this 'tapping'. This is achieved by breaking the model of the lumped-spiral inductor into two components: the outer-winding and the remaining core. It should be remembered that careful attention has to be paid to properly account for the mutual inductance between these two components. The resultant equivalent circuit model is obtained by taking the original model and dividing the inductor element L_1 into two. This results in $L_1 - L_{tap}$ and L_{tap} , where L_{tap} is the equivalent inductance between the forward-feed capacitor and the gate terminal of the following FET. It should be noted that L_{tap} includes all of the mutual-inductances with the wire segments of the core. $L_1 - L_{tap}$ represents the equivalent core inductance. Although this equivalent model is not perfect it is expected to be valid for small values of L_{tap} . It should be mentioned that the skin-effect of L_{tap} is not accounted for. Nevertheless, the spiral inductor, as a whole, retains its complete skin-effect model.

After several layout iterations and concurrent SUPER-COMPACT simulations of the distributed amplifier, and self- and mutual-inductance estimations of all the inductors, the value $L_{tap} = 450pH$ was arrived at. As we shall see from experimental results to be presented in Chapter 6, this value is found too large. Simulations done to explain the differences between the experimental and the predicted results indicate that its value should be approximately $250pH$.

5.2.5 Line-Termination Elements

The other elements not yet discussed are the resistors and capacitors of the gate- and drain-line-terminating impedances and the forward-feed capacitors. The capacitors have the design and layout constraints of small size, of being modellable, and of being relatively process-insensitive. Two types of capacitors exist within the manufacturing process used here. They are the MIM capacitor and the inter-digitated capacitor. Although the latter is more attractive in terms of increased yield (due to the lack of a thin inter-electrode dielectric) MIM capacitors were exclusively selected on the basis of their accurate and simple modeling and on their small size. The inter-digitated capacitors suffer from the lack of accurate, experimentally verifiable models and also a lack of compactness. For frequencies above 12 GHz, for the typical values of capacitance on the order of 100fF considered here, they are prone to resonate due to the distributed nature of their relatively long inter-digitated fingers which rest on the GaAs substrate. These considerations suggest that MIM capacitors are the only real choice available. Unfortunately, they are prone to considerable fluctuations because of variations in the thin sandwiched dielectric. They can be a significant contributor to limiting the yield [13]. Nevertheless, they were selected due to their small size and the known accuracy of their models.

The drain-line terminating impedance includes a line-matching resistor R_{DT} and dc decoupling capacitor C_{DT} in series. The resistor is used for two purposes. Firstly, it is used to absorb part of the reverse-travelling wave on the drain-line. Secondly, it is used to reflect part of this reverse-wave to constructively interfere with, and thereby increase, the amplitude of the forward-travelling wave, resulting in a greater gain. The capacitor is only used to DC-block the drain-line bias, thereby avoiding excessive and unnecessary power dissipation to the resistor. Without this capacitor, approximately 54 mW of power would have to be dissipated by a resistor of dimensions $40\text{ }\mu\text{m}$ by $1000\text{ }\mu\text{m}$. This corresponds to an unacceptable power density of 1400 W/cm^2 , especially if long-term reliability is of concern. With the

capacitor, acceptable values of 6 mW and $160\text{W}/\text{cm}^2$ are achieved, respectively. Also, because of the greater drain-line current without it, a voltage drop along the drain-line would exist. Different drain biases from FET to FET would thus result.

Similarly, gate-line termination is provided by a line-matching resistor R_{GT} . In this case it is unnecessary to include a dc-decoupling capacitor because the gate-line bias voltages are only $\pm 0.5\text{V}$. It is estimated that this resistor dissipates less than 4 mW of power.

The 10 pF drain-line dc-block capacitor used is of the MIM type, in which the Si_3N_4 dielectric is sandwiched between the 1-ME and 2-ME metal layers, and covers an area of $500\ \mu\text{m}^2$. It would be impractical to use an inter-digitated capacitor as this would have resulted in a prohibitively large-area device.

5.2.6 Input and Output Pads

Two $50\text{-}\mu\text{m}$ -square pads with a $50\text{-}\mu\text{m}$ spacing between them are used at the input and output ports to permit off-chip interfacing. This allows wire-bonding to the circuit which embeds the chip and permits easy measurement access. More importantly, these pads are intended to be probed using coplanar-transmission-waveguides (available at BNR) similar to the ones described by Strid [68]. These probes permit the nondestructive testing of any amplifier on a large 3-inch wafer within minutes. They permit accurate measurements up to 18 GHz since they provide a 50Ω characteristic impedance up to the probe tips. This ensures that the amplifier is properly matched at its input and output ports, and thus minimizes unwanted reflections which degrade accuracy. More on the characteristics of the probes can be found in Chapter 6.

5.3 Iterative Procedure of the Layout

In this section the details of the layout procedure used in arriving at the final version of the distributed amplifier's circuit element topology is given. Because

of the complexities involved in accounting for all of the coupling effects between circuit elements of the complete amplifier (such as the mutual-inductance between wire elements), the analysis can become an intensive task. As there is a very large number of interactions between circuit elements, some have to be treated independently of others. Fortunately, most can be treated in this way without degrading the accuracy of the SC simulations because there is negligible coupling. Circuit elements that may require attention include:

- (a) spiral inductors and their interconnections,
- (b) FETs,
- (c) forward-feed capacitors and their interconnections,
- (d) gate- and drain-line-termination impedances.

The last three can easily be treated independently of each other. On the other hand, the interconnections of the spiral inductors pose significant modeling problems because of their considerable inductance and resistance. The problems are compounded by the fact that the inductance-to-resistance ratio of the interconnections is slightly different to that of the spiral inductors. This means that there is no simple one-to-one relationship between the inductance of the interconnect and spiral inductor. Hence during the layout design process the inductance of the interconnect cannot be increased with a corresponding decrease in inductance of the spiral inductor because this would result in an overall resistance different from the starting value. Consequently a complex iterative process is used involving a convergent solution between the DA's topology and the values of the circuit elements (especially the inductors).

In the following description of the procedure, the steps involved in arriving at the final layout, particularly for the spiral inductors and their interconnects, are explained in detail.

In steps 1 to 5 of the procedure the approximate spiral inductor and interconnect topologies are obtained while approximating a one-to-one relationship between the inductance of the spiral inductors and that of the interconnect.

- (1.) Assume $L_{int}^j = 0$ for all inductors.
- (2.) Let $L_{spiral}^j = L_{SC}^j - L_{int}^j$.
- (3.) Lay out the amplifier using standard cells having self-inductance L_{spiral}^j and the necessary interconnections.
- (4.) From the layout determine the interconnect inductance L_{int}^j (which also includes the mutual inductance between the spiral inductor and the interconnect).
- (5.) Repeat steps 2 through 4 (for each inductor j concurrently) until the inductance of the interconnections and the spiral converge in value.

Here L_{SC}^j is the inductance value obtained from SUPER-COMPACT, L_{spiral} and L_{int} are the inductances of the laid-out spiral inductor and the interconnect, respectively.

Although the total inductance (which is equal to the sum of the self-inductances of the spiral inductor and the interconnect and the mutual inductance between the two) has been achieved according to the values given by SC specifications, the total resistance is slightly different to what is modeled by SC, since the ratio of inductance to resistance for a spiral inductor is slightly different from that of an interconnect. This requires the layout and the electrical optimization to be done concurrently.

- (6.) From the layout, find $R_{tot}^j = R_{spiral}^j + R_{int}^j$ and $L_{tot}^j = L_{spiral}^j + L_{int}^j + L_m^j$ (where L_m^j is the equivalent mutual-inductance between the spiral inductor and its interconnect, and the subscript 'tot' means 'total'. L_{tot}^j is the sum of the self- and mutual-inductances of the spiral inductor and its interconnect. Within the

SC circuit listing, it is assumed that the total resistance [including that of the interconnects] is linearly proportional to the total inductance. This assumption is valid for values close to R_{tot}^j and L_{tot}^j [i.e. for values of K^j close to 1.0].

- (7.) Within the SC circuit listing, define $R_{tot'}^j = K^j R_{tot}^j$ and $L_{tot'}^j = K^j L_{tot}^j$ (where the intrinsic parameters of the inductor model are calculated from the parameters $R_{tot'}^j$ and $L_{tot'}^j$ by SC. K^j are proportionality constants initially set to 1.0.)
- (8.) Using SC, optimize the amplifier's S-parameters and gain flatness by allowing the parameters R_{GT} , R_{DT} , C_{DT} , and all of the K^j parameters to vary.
- (9.) Determine whether any of these parameters varied sufficiently enough to warrant a modification of the layout. If not, then the layout is complete. Otherwise, select and lay out an appropriate spiral inductor standard-cell with its interconnection such that the sum of the self- and mutual-inductances equals or best approximates $L_{tot'}^j$.
- (10.) Lay out the gate- and drain-line-termination elements from the parameters produced by the SC optimization.
- (11.) Repeat steps 6 through 10 (for each inductor j concurrently) until convergence in the circuit component values has been obtained.

By following these iterative steps one obtains the layout shown in Fig. 5.1. This is the actual circuit-element topology of the DA and is used in the fabrication of the masks.

5.4 Circuit Description and Design

5.4.1 S-Parameters Versus Bias

In Fig. 5.3 the schematic representation of Fig. 5.1 is shown and is used to arrive at the circuit element listing used by SUPER-COMPACT. Figs. 5.4 through 5.6, respectively, show the effects of gate-line bias voltage on gain and the input and

Figure 5.3 Schematic of Laid-Out 4-Stage T(GDS)F Type DA Incorporating "Tapping" of the Gate Line Inductors L_{gi} . L_{di} Denotes Drain-Line Inductors; L_{si} Series-Drain Inductors; R_{gt} Gate-Line Termination Resistor; R_{di} Drain-Line Termination Resistor; C_{di} Drain-Line Termination Capacitor; C_{gi} Forward-Feed Capacitors; C_{di} Parasitic Capacitors.

output reflection coefficients. The circuit simulated is a fully-tapered DA with FF, and incorporates the full inductor and FET models. The difference between this circuit topology and those presented in the previous chapter is that this one is based on the final laid-out design and therefore includes the effects of the interconnect's inductance and "tapping" inductance. The latter is the inductance in series with the FF capacitors.

The gain is shown for gate-line voltage biases V_i between the -1.5V pinchoff voltage of the FET and the maximum allowable gate-source forward-conduction voltage of 0.5 V (relative to the FET source) for a drain-line voltage bias $V_o = 2.5V$. It should be noted that the amplifier is designed to operate at a bias of $V_i = 0$ V. Over a range of 0.5 V to -1.25 V the amplifier exhibits a relatively flat gain over the complete 1 GHz to 12 GHz band, except for a slight dip for a -1.0 V bias for frequencies above 9 GHz. For the case in which the bias voltage is -1.25 V, the DA does not amplify below 7 GHz and attenuates the signal above this. Finally, for a bias of -1.5 V, which pinches off the FETs active channels, only the passive elements take part in the propagation. For frequencies below 7 GHz the forward conduction is dominated by the gate- and drain-line coupling capacitors, i.e. the FF capacitors and the C_{dg} capacitances. For frequencies above this, the improvement in isolation is mainly due to inductor losses and is partly due to destructive interference created by the multiple signal paths that exist between the input and output ports. It should be mentioned that the port-to-port isolation, including the reverse isolation, can be improved by decreasing the magnitude of the FF capacitance.

The DA constructed as described in this work was not designed with the intention of having exceptionally flat gain and high port-to-port isolation for gate biases close to the pinch-off voltage of the FET.

Although the amplifier's gain exhibits a considerable sensitivity to gate voltage, S_{11} does not. For voltages above -1 V, S_{11} does not change much and remains below 0.3 across the complete band. Only when the active channels of the FETs are pinched off does S_{11} rise to 0.55 at 3 GHz. This is probably due to the change

Figure 5.4 Predicted Gain of Designed 4-Stage DA as a Function of Gate Line Bias.

Figure 5.5 Predicted Input Reflection Coefficient as a Function of Gate Line Bias.

Figure 5.6 Predicted Output Reflection Coefficient as a Function of Gate Line Bias.

in C_{gs} from 0.3 pF to 0.1 pF.

Similar results are observed for S_{22} . Considerable changes occur when the active channels of the FETs are pinched off. The only exception to this is an increase to 0.4 for a -1 V gate bias for frequencies above 11 GHz.

5.4.2 FET Parameter Sensitivity

Simulations to determine the sensitivity of the frequency response of the constructed DA to the variations in the intrinsic parameters of the FET are shown in Fig. 5.7 through Fig. 5.12. The plots are given for $\pm 25\%$ variations of the parameters C_{gs} , R_i , C_{gd} , g_m , G_{ds} , and C_{ds} , respectively.

The increase in gain observed with a decrease in C_{gs} is attributable to a greater share of the gate voltage appearing across C_{gs} due to its increased impedance (resulting in a correspondingly larger transconductance current). Similarly, a decrease in R_i has the effect of increasing the gain.

A much less pronounced effect is observed for C_{gd} , due to the reverse-biased gate-drain Schottky junction, because of its relatively small magnitude. At the other extreme, the g_m has the greatest effect on the frequency response. Unlike the previously-described parameters in which the LF gain is negligibly affected, g_m affects the amplifying-band uniformly. Nevertheless, since the amplifier incorporates capacitive FF, a frequency-dependent gain is observed. Also, the drain-line conductance G_{ds} has a similar, but less drastic, effect on the frequency response. This can be seen from equation (3.3.36) which shows drain-line loss increasing monotonically with frequency, but importantly, does not vanish even at extremely low frequencies. Finally, C_{ds} is found to hardly affect the gain, even at HF because of its insignificant value.

Figure 5.7 Gain Sensitivity due to $\pm 25\%$ Variations in C_{gs} .

Figure 5.8 Gain Sensitivity due to $\pm 25\%$ Variations in R_i .

Figure 5.9 Gain Sensitivity due to $\pm 25\%$ Variations in C_{dq} .

Figure 5.10 Gain Sensitivity due to $\pm 25\%$ Variations in g_m .

Figure 5.11 Gain Sensitivity due to $\pm 25\%$ Variations in G_{ds} .

3

of/de

3

Figure 5.12 Gain Sensitivity due to $\pm 25\%$ Variations in C_{ds} .

6

Experimental Results

6.1 Introduction

This chapter presents test results of a 1 - 12 GHz tapered distributed amplifier formed with discrete-element spiral-inductors and incorporating forward-feed. The amplifier consists of four $1\ \mu\text{m}$ by $160\ \mu\text{m}$ GaAs FETs interconnected with planar inductors resulting in a GaAs MMIC. The objective of this design is to validate the modeling of the amplifier discussed in the previous chapter. The use of forward-feed capacitors demonstrates the feasibility of overcoming gate and drain line losses.

A description of the test setup used in the measurement of the electrical performance of the distributed amplifier is presented. Measured S-parameters under various bias conditions are demonstrated along with the amplifier's 1-dB gain-compression point.

6.2 S-Parameter Measurement Setup

The frequency responses of FETs and distributed amplifiers are characterized through the use of S-parameters, as they permit simple and yet very accurate measurements without the necessity of providing short- and open-circuits at the actual terminals of the device under test (DUT) for each frequency (as is required for Z-, Y- and H-parameter measurements). Because of this, most if not all, commercially available network analyzers utilize this S-parameter measurement technique. Most of the other types of parameters can be easily derived from S-parameters through the use of matrix algebra. Therefore, all the measurements reported here are done using this method.

The measurement apparatus used to characterize the FET and DA can be broken into two separate parts: the network analyzer and the coplanar waveguide probes. Firstly, the HP8510 network analyzer setup consisting of microwave sources, detectors, and a controlling computer (equipped with a comprehensive software package and peripheral I/O devices) is shown in Figure 6.1.

The network analyzer is capable of accurately extracting the S-parameters of the DUT across the 45MHz to 26.5GHz frequency band with the help of a comprehensive and user-friendly software package. Once the complete system is fully calibrated with standardized on-chip impedances, which permit the characterization of the connectors up to the probe tips, the software makes it possible to arrive at virtual real-time error-corrected measurements, and thus to completely de-embed the DUT. This powerful tool eliminates most of the tediousness previously encountered whenever accurate measurements were essential. At the same time, the complete system provides excellent measurement accuracy; typically ± 0.1 dB and ± 1.5 degrees resolutions are readily achievable [100].

Information such as conditional stability, group-delay, gain and other parameters can be computed from the error-corrected measured data. Even the intrinsic parameters of FETs can be obtained through the use of a parameter fitter. Transformation from the frequency domain to the time domain is also possible. This permits visualization of the DUT's transient response to an applied pulse. Last but not least is the determination of the 1-dB gain-compression point at which the active DUT saturates.

Although extremely good precision is achievable with this setup, in no way does this guarantee a practical measurement technique. In other words, what is required is a simple and quick setup which, while being accurate, is also repeatable. For these reasons, coplanar waveguide transmission-line probes were utilized, as shown in Figure 6.2.

Such probes provide an extremely good 50Ω characteristic impedance up to the contacting tips, thus minimizing parasitic reflections and mismatching to the

Figure 6.1 S-Parameter Measurement Apparatus.

Figure 6.2 Coplanar Waveguide Transmission-Line Probes.

(a) Side View, and (b) Bottom View

(From Rabjohn et al. at Bell-Northern Research [101])

(Adapted From Strid et al. [68]).

DUT [68,101]. They also carry the ground return path to the DUT's ground terminal, hence eliminating imbalances due to unequal path lengths, as commonly experienced with needle probes. This concurrency between signal and ground conductors in terms of electrical length is vital in cases where crosstalk can become a detrimental source of noise, such as in high-speed digital probing.

The probes are fabricated by photolithographically defining a coplanar waveguide transmission-line conductor pattern on to a 0.01 in. thick and 1 in. long alumina substrate. SMA connectors, having minimal parasitic mismatching, join the probes with the network analyzer's coaxial transmission lines. These probes exhibit low transmission losses and good return losses on the order of 3 dB and 15 dB, respectively, at 20 GHz. An important point is that they operate down to dc, thereby permitting dc biasing of the DUT without requiring additional probes and pads on the chip to supply the power.

Through the use of on-chip calibration circuit elements such as a 50Ω resistor, a thru-line, and open- and short-circuits, probe imperfections can be de-embedded resulting in almost perfect measurements. In addition, these probes form an extremely good and repeatable contact to the DUT even after the probing of numerous dies.

It should be mentioned that the probes exhibited a slight and inexplicable resonance over a 0.5 GHz bandwidth resulting in a ± 0.5 dB measurement accuracy in the vicinity of 6 GHz.

6.3 FET Measurements

The low-frequency I-V transfer curves for the drain and source terminals are presented in Figure 6.3 for various gate-source biases ranging between gate terminal forward conduction (+0.5V) and active channel pinchoff (-1.5V) for a $160\text{ }\mu\text{m}$ wide and $1\text{ }\mu\text{m}$ long gate.

From these curves one can arrive at the low frequency transconductance and drain-source leakage conductance of $g_m = 20\text{mS}$ and $1/G_{ds} = 2.5\text{K}\Omega$, respectively.

Figure 6.3 Measured I-V Characteristics of a Typical $1\text{ }\mu\text{m} \times 160\text{ }\mu\text{m}$ GaAs MESFET on Wafer X87A-151 30794.

The former parameter compares favourably to the expected value of $21.5mS$ used throughout the simulations presented in Chapter 4. On the other hand, the latter does not correspond so well to the measured value of 909Ω obtained at high-frequencies through the S-parameter technique. This discrepancy is attributable to a greater drain-source leakage current observed at high frequencies as compared to dc (from I-V measurements) due to an excess charge accumulation and discharge, with each cycle, residing on deep traps at the substrate-channel interface [98].

Although not shown, the drain-source breakdown voltage (V_{br}) is approximately 13V. An indication of this is seen for the case where $V_{ds} = 10V$ and $V_{gs} = -1.5V$ whereby the reverse biased gate-drain Schottky junction begins to break down and conduct.

From the measured S-parameters of the FET one can empirically obtain the intrinsic parameters of the FET shown in Table 6.1. These intrinsic parameters were calculated by R. K. Surridge for a typical MESFET [99]. For comparative reasons, the original parameters used throughout the simulations presented in the previous chapters are also given.

Evidently, the model parameters of the fabricated FETs do not coincide exactly with the expected and desired values. The parameters which affect the performance of the amplifier the most (as will be shown in Section 6.4.2) are R_i and R_{ds} . Although the input resistance R_i has undergone a 40% reduction which has the effect of reducing gate line losses, this improvement in FET performance under the conditions of this design is undesirable. The reason for this is that in microwave design the intrinsic parameters should not vary between the design phase and the testing phase, as this can adversely affect the amplifier's behaviour, even with an improvement of the FET's performance. This is different from digital circuits where improved FETs can result in faster gates and/or lower power consumption. Because the microwave amplifiers were fabricated with a manufacturing process directed towards digital logic gates rather than microwave amplifiers, these parameters were found to have improved due to the maturing of the process. Nevertheless, as will be

Table 6.1 Predicted and Measured FET Model Parameters
of a Typical $1\text{ }\mu\text{m} \times 160\text{ }\mu\text{m}$ GaAs MESFET on Wafer
X87A-151 30794 for $I_{ds} = 20\text{ mA}$, $V_{ds} = 2.5\text{ V}$, and $V_{gs} = 0\text{ V}$.

Parameter	Values in Design	Measured [99]	$\Delta(\%)$
$g_m(mS)$	21.5	18.9	-12
$R_i(\Omega)$	20	12	-40
$C_{gs}(fF)$	232	242	4
$C_{ds}(fF)$	45	36	-20
$R_{ds}(\Omega)$	526	909	73
$C_{dg}(fF)$	27	13	-52
$\tau_d(pS)$	2.5	3.5	40
$L_s(pH)$	30	30	0

seen in Section 6.3, the amplifiers do exhibit some insensitivity to these variations throughout the low and mid frequencies. Unfortunately this is not the case for the high frequencies between 11 and 13 GHz.

Figure 6.4 illustrates the maximum achievable unilateral gain of a single $160\text{ }\mu\text{m}$ -wide FET with its input and output ports conjugately matched. The transistor has a maximum stable gain of 36 dB at dc. Through extrapolation of the -0.7 dB/GHz curve one obtains a unity-gain frequency of 27.3 GHz. This frequency is usually referred to as f_{max} and is the maximum frequency at which the FET can self-oscillate under ideal matching conditions.

6.4 DA Measurements

6.4.1 S-Parameters of DA

Optical photographs of the 1.9mm by 0.75mm 4-Stage distributed amplifier, a

Figure 6.4 Calculated Maximum Unilateral Gain from Measured S-Parameters of a Typical $1\ \mu\text{m} \times 160\ \mu\text{m}$ GaAs MESFET on Wafer X87A-151 30794 for $I_{ds} = 20\ \text{mA}$, $V_{ds} = 2.5\ \text{V}$, $V_{gs} = 0\ \text{V}$.

$1\ \mu\text{m} \times 160\ \mu\text{m}$ GaAs MESFET, and a gate line spiral inductor are shown in Figs. 6.5 through 6.7, respectively. Details of these can be found in Chapter 5.

Referring to Figs. 6.8 through 6.10, where the designed, measured, and simulated performances of the DA are compared, it can be seen that the measured low- and mid-frequency gain is approximately 1 dB lower and yet similar in shape to the designed response. The former is attributable to the g_m of the fabricated FETs being 12% smaller than expected. At the high frequency end of the band (11 GHz and greater), on the other hand, the similarity vanishes; indicating that the amplifier is not as tolerant to FET parameter variations as it is at lower frequencies. An explanation for this discrepancy will be given in the following section.

For the input reflection coefficient $|S_{11}|$ (see Fig. 6.9) the differences between the designed and measured responses are quite small considering the crests and troughs of the responses occur at very similar frequencies. In addition, their magnitudes are in reasonable agreement especially if one considers the differences in the FET parameters.

Similarly, the output reflection coefficient $|S_{22}|$ (see Fig. 6.10) behaves in a similar fashion, whilst not having as good a match in terms of the magnitudes of the crests and troughs. This greater discrepancy is to be expected since it has been found through SUPER-COMPACT simulations that the S_{22} parameter is the most difficult S-parameter to optimize.

Interestingly, it is found that the magnitude of the measured S_{11} does not have an erratic frequency response, even though the FET intrinsic parameters are known to differ considerably from the expected and desired values. On the other hand, measured $|S_{21}|$ and $|S_{22}|$ exhibit strongly frequency-dependent responses for the 11 GHz to 15 GHz range, not surprisingly.

Fortunately, it has been possible to simulate the measured response with considerable accuracy. From these simulations a tapping inductance value of 250 pH instead of 450 pH has been found. This discrepancy is not unexpected considering the difficulties in estimating its value accurately in the midst of all the mutual

Figure 6.5 Optical Photograph of 4-Stage GaAs MMIC
Distributed Amplifier.

Figure 6.6 Optical Photograph of $1\text{ }\mu\text{m} \times 160\text{ }\mu\text{m}$ GaAs MESFET.

Figure 6.7 Optical Photograph of a Gate Line Inductor.

Figure 6.8 Comparison Between Designed, Measured, and Simulated Gains of a Typical Distributed Amplifier on Wafer X87A-151 30794 for $V_D = 2.5$ V, $V_i = 0$ V.

Figure 6.9 Comparison Between Designed, Measured, and Simulated Input Reflection Coefficients of a Typical Distributed Amplifier on Wafer X87A-151 30794 for $V_o = 2.5$ V, $V_i = 0$ V.

Figure 6.10. Comparison Between Designed, Measured, and Simulated Output Reflection Coefficients of a Typical Distributed Amplifier on Wafer X87A-151 30794 for $V_o = 2.5$ V, $V_r = 0$ V.

couplings between the numerous conductors.

6.4.2 Explanation of measured results

As has been mentioned in the previous sections there exists an unexpected resonant peak close to and around 12 GHz. In this section a method is devised which enables one to 'probe' into the internal workings of the distributed amplifier. One requires a method to determine node voltages, branch currents and power flows. Unfortunately, physical probing of the amplifier is almost impossible since the parasitics of the probes would disturb the electrical characteristics of the amplifier. The only alternative is to probe the simulation rather than the physical device. Since it is possible to model the experimental results accurately, one expects the simulated results to correlate very well with the corresponding internal signals within the chip.

Based on this reasoning, it was decided to use SCAMPER (BNR's in-house circuit simulator) since it is capable of computing the power flow and current through any branch, and of course the voltage at any node too, of lumped circuit elements.

The numerical results (which include 66 voltage, current, or power values for each frequency) show that no simple explanation can account for the resonant peak. This situation is understandable in view of the multiple feedback and forward-feed loops that exist, as seen in Fig. 6.11. These loops complicate the analysis by making it difficult to pin-point the exact source of the gain peak. By carefully analyzing the data one comes to the conclusion that there exist three feedback loops of significance. The most important one consists of the first FET and its forward-feed (FF) capacitor (C_{f1}) and also L_{g2} (loop A in Fig. 6.11). The second loop, which is found to be of lesser importance, is composed of the second FET and its FF capacitor (C_{f2}) as well as L_{g3} (loop B). The last and least important loop consists of the output of the second FET driving a backward-travelling wave on to the drain line, which in turn generates a backward flowing power wave (relative to the expected flow of the designed circuit) through the first series-drain inductance (L_{s1}) (loop D).

Figure 6.11 Schematic of Fabricated Distributed Amplifier Showing Feedback Paths.

The difficulty in analyzing the cause of the gain peak arises from uncertainty about which of these feedback loops is responsible for the increase. By carefully scrutinizing the compiled data one can gain insight into the causes of the increase in gain. A -114% decrease (since it is less than -100% this implies a change in direction) in power flow is observed for L_{s1} and a corresponding 160% increase for C_{f1} . These numbers are obtained by comparing the simulated values to the designed values. This implies that the power emanating out of the FET has a tendency to prefer flowing through C_{f1} rather than through the L_{s1} . One also observes a preference for the power flowing through C_{f1} to flow backwards into the gate of the first FET rather than forwards into the gate of the second FET. This feedback has the effect of increasing the output power of the first FET by 300%.

Although the series connection of C_{f1} and L_{g2} seems to form an LC feedback loop with a short-circuit resonant frequency close to the frequency at which the amplifier's gain peaks, this simple explanation in itself cannot be the dominant contributor. The reason for this is that no peaking in gain is observed for the designed DA even though its inductor and capacitor values are almost identical to the ones found in the experimental DA. The peaking in gain is attributable to the lower FET losses, i.e. R_i and R_{ds} (especially the former) play a considerable role in conjunction with the feedback loop formed by C_{f1} and L_{g2} . The lower losses imply that each FET is more efficient and hence has a greater gain potential.

This phenomenon also explains the feedback loop B, although to a lesser degree. Feedback loop C, on the other hand, does not follow this behavior. It is simply attributable to the 270% increase in power appearing at the output of the FETs resulting from the effective cascading at high frequencies of FETs 1 and 2. The excessive output power generated by FET 2 flows backwards on the drain line and because of its magnitude appears as a backward flow through L_{s1} . However, this feedback loop is the least dominant of the three described here.

6.4.3 Frequency Response Effects due to Bias

The effects of input and output bias on the S-parameters are illustrated in Figs. 6.12 through 6.16. For the input line, bias voltages (V_i) of 0.5 V, 0 V, -1 V, -1.5 V, and -2.5 V were selected. However, certain S-parameters such as S_{12} , are relatively bias-insensitive. Fewer bias voltages were used in such cases. The output line bias (V_o) was set to 2.5 V.

As can be seen, the gain ($|S_{21}|$) is maximized by setting $V_i = 0V$, the designed operating point. Nevertheless, at 0.5 V the low and mid frequency gains are identical. However, at the high-frequencies a decrease in gain is found and has the desirable effect of producing a flatter frequency response. The reverse biasing of the FETs (relative to their sources) has the interesting and predictable effect of increasing the resonant frequency at which the gain peaks. This is due to a decrease in C_g , which, when coupled with the gate line inductors, results in an increase in resonating frequency. At the same time, for frequencies below the resonant peak, gain fluctuations diminish due to an observed increase in R_i , creating a lower gain especially at the higher frequencies and resulting in a flatter gain. For the case whereby the FETs are pinched off and offer no amplification, the amplifier exhibits better than -4 dB port-to-port isolation. This non-ideal isolation is attributable to the signal leakage between the gate and drain lines by the forward-feed capacitors. For frequencies below 10 GHz, the input and output return losses are better than 10 dB and 7 dB, respectively, for reverse bias voltages less than 1.5 V ($V_i > -1.5V$). And finally, as expected, for the bias condition in which the transistors do not amplify (and therefore the distributed amplifier can be considered passive), S_{21} is equal to S_{12} . An exception to this occurs at the extreme low frequencies and is attributable to imperfect bias tees.

For the output line, bias voltages of 1.5 V, 1.75 V, 2 V, and 2.5 V were selected. As expected, a reduction in gain is observed with a decrease in output bias, but more so near 14 GHz, whilst the power-supply current is found to fluctuate by less

Figure 6.12 Measured $|S_{21}|$ for Various Values of Input Bias V_i for a Typical DA on Wafer X87A-151 30794 for $V_o = 2.5$ V.

Figure 6.13 Measured $|S_{11}|$ for Various Values of Input Bias - V_i for a Typical DA on Wafer X87A-151 30794 for $V_o = 2.5$ V.

Figure 6.14 Measured $|S_{22}|$ for Various Values of Input Bias V_i for a Typical DA on Wafer X87A-151 30794 for $V_o = 2.5$ V.

Figure 6.15 Measured $|S_{12}|$ for Various Values of Input Bias V_i for a Typical DA on Wafer X87A-151 30794 for $V_o = 2.5$ V.

Figure 6.16 Measured $|S_{21}|$ for Various Values of Output Bias V_o for a Typical DA on Wafer X87A-151 30794 for $V_i = 0$ V.

than 10% over the full bias range.

This insensitivity to output bias demonstrates the versatility of the distributed amplifier and its attractiveness in adverse environments such as in remote communications posts.

6.4.4 Stability and Group Delay

Figures 6.17 and 6.18, present the amplifier's stability constant (K) [94] and group delay for frequencies between 50 MHz and 14.05 GHz. It can be seen that the amplifier is unconditionally stable ($K > 1$) throughout the frequency band and, very importantly, near 12 GHz, thus demonstrating the non-existence of self-oscillations throughout the band.

6.4.5 Process Variations

The curves of Figs. 6.19 through 6.22 show the effects of process variations on the S-parameters for 5 distributed amplifiers located on wafer 30794 under identical bias conditions of 0 V and 2.5 V for the input and output ports, respectively. It can be seen that the frequency responses exhibit a high degree of uniformity in which gain fluctuations of less than 1.5 dB are observed for frequencies below 10 GHz. Exceptionally good uniformity is found for S_{11} , and especially for S_{22} , and S_{12} . It can be said that the distributed amplifier is truly insensitive to process variations when one considers its wide bandwidth and the FET intrinsic parameter variations it experiences.

6.4.6 1-dB Gain-Compression

Although the amplifier was not designed with the intention of operating as a power amplifier, it was decided to measure the output power as a function of the input power so as to determine the 1-dB gain-compression point. Three frequencies, 2 GHz, 4 GHz, and 10 GHz were utilized. Other frequencies close to 6 GHz were not

Figure 6.17 Calculated Stability Constant K as a Function of Frequency from Measured S-Parameters of a Typical DA on Wafer X87A-151 30794 for $I_o = 80$ mA, $V_o = 2.5$ V.

Figure 6.18 Calculated Group Delay as a Function of Frequency from Measured S-Parameters of a Typical DA on Wafer X87A-151 30794 for $I_o = 20$ mA, $V_o = 2.5$ V.

Figure 6.19 Measured $|S_{21}|$ of Five Distributed Amplifiers Located Closest to Center of Wafer X87A-151 30794, Showing Variations from Die to Die for $V_i = 0$ V, $V_o = 2.5$ V.

• **Figure 6.20** Measured $|S_{11}|$ of Five Distributed Amplifiers Located Closest to Center of Wafer X87A-151 30794, Showing Variations from Die to Die for $V_i = 0 \text{ V}$, $V_o = 2.5 \text{ V}$.

Figure 6.21 Measured $|S_{22}|$ of Five Distributed Amplifiers Located Closest to Center of Wafer X87A-151 30794, Showing Variations from Die to Die for $V_i = 0 \text{ V}$, $V_o = 2.5 \text{ V}$.

Figure 6.22 Measured $|S_{12}|$ of Five Distributed Amplifiers Located Closest to Center of Wafer X87A-151 30794, Showing Variations from Die to Die for $V_i = 0$ V, $V_o = 2.5$ V.

selected due to a slight and inexplicable resonance in the probes in the vicinity of this frequency. A diagram of the setup is shown in Figure 6.23. Probe, connector, and coaxial cable losses have been taken into account when de-embedding the amplifier's input and output power levels. The results are shown in Figure 6.24 where it is found that the 1-dB gain-compression point occurs at output powers of 16.2 dBm, 16.2 dBm, and 12.8 dBm for 2 GHz, 4 GHz, and 10 GHz, respectively. As the frequency increases, the behaviour of the amplifier, due to forward-feeding, becomes characteristic of cascaded, rather than parallel FETs. Thus, instead of each FET supplying a fourth of the output power, the FET closest to the output is the only one, at the limit of cascading, to be given the task of supplying most of the output power. This means that due to its limited driving capability, the maximum output power is lower than at lower frequencies.

6.5 Conclusions

A major objective of this thesis was to demonstrate the feasibility of utilizing spiral inductors within a distributed amplifier designed and fabricated within the constraints of a GaAs MMIC fabrication technology. Also demonstrated, is the use of forward-feed capacitors to overcome HF gain-degradation by rerouting the signals which pass through the lossy inductors. To the author's knowledge this is the first reported experimental verification of the use of forward-feed, and also of the tapering of lumped-element inductor values within a distributed amplifier.

Other objectives were to determine the accuracy of the circuit models and the prediction of the experimental performance of a distributed amplifier comprising several of these models. The results presented herein support these objectives.

Figure 6.23 Power Measurement Apparatus.

Figure 6.24 Measured Power Performance of a Typical DA on Wafer X87A-151 30794, for $V_i = 0$ V, $V_o = 5.24$ V, $I_o = 80$ mA.

Summary, Conclusions, and Recommendations

7.1 Summary and Conclusions

Tapering of the inductor values along the gate- and drain-lines and of the series-drain inductors, and the use of forward-feed capacitors have the beneficial properties of improving the frequency response performance in terms of gain, input and output VSWR, and gain flatness for a four stage 1-12-GHz distributed amplifier fabricated using a GaAs MMIC based technology.

In Chapter 1, a brief outline of the motivations, approach, objectives, and organization of this thesis has been given. A brief review and a historical background of GaAs and MESFET technology, as well as an up-to-date overview of gain and power-improving mechanisms for distributed amplifiers reported in the literature has been presented in Chapter 2.

With the help of a symbolic algebraic manipulator program (MACSYMA), an algebraically derived analysis of a DA was given in Chapter 3 in which FET losses were taken into account. This led to a graphical optimization procedure for arriving at the optimum number of stages and FET widths. A definition of tapering and mismatching of the gate- and drain-lines in terms of the two parameters τ and m , respectively, has been presented. From this, the effects of tapering and mismatching on the frequency response in terms of gain, gain-bandwidth product, 1-dB gain-roll-off bandwidth, and input and output VSWRs were graphically presented and discussed. It was found that indeed tapering and mismatching do provide improved performance characteristics by increasing the gain and better matching the input and output ports of the amplifier. Due to a more efficient use of the amplifying

potential of the FETs, greater bandwidths can be achieved while maintaining the same gain as a DA has without tapering and mismatching.

In Chapter 4, a more detailed and accurate analysis of a DA under more realistic operating conditions found in a GaAs-based technology was discussed. To achieve this, the SUPER-COMPACT CAD program was used to analyze and optimize DA circuit models using the most accurate circuit element models available to the author. With this extremely valuable tool, it was possible to include FET and spiral inductor losses. The latter loss is directly due to skin-effect of the conductive segments of the square spiral inductors and was found to contribute significantly to degradations in gain at high frequencies close to 12 GHz. A solution was devised which included the use, in part, of the above-mentioned technique of tapering. Also required was the incorporation of forward-feed capacitors to redirect high-frequency signals away from the lossy inductors by arranging the interconnections between FETs so that the DA effectively resembled a conventional cascaded amplifier. It was shown how these mechanisms can be used effectively to achieve gain and flatness in gain and yet still arrive at an unconditionally stable amplifier.

To verify experimentally the performance-improving mechanisms introduced in Chapter 4, a four-stage distributed amplifier based on GaAs MMIC technology covering the 1-12 GHz frequency band was designed, laid-out, and discussed in Chapter 5. A detailed description of the iterative design method involved in the layout and concurrent optimization, especially of the spiral inductors and the interconnections and their mutual inductances, using a CAD technique was given. The laid-out circuit elements forming the DA were discussed along with the predicted performance under various bias conditions of the completed chip.

The DA was fabricated and tested. The results were discussed in Chapter 6 and included accurate measurements of the S-parameters under various bias conditions, stability, group-delay, 1-dB gain-compression point, and process variations. These were expressed in terms of frequency characteristics obtained through the concurrent use of CPW probes and a fully-automated network analyzer capable

of de-embedding the device under test. Comparisons were made between the experimental results and simulations to validate circuit models used throughout the design phase. It was revealed that the circuit models were sufficiently accurate and that the DA could function over its designed bandwidth with the gain improving mechanisms previously mentioned, such as tapering and the use of forward-feed capacitors.

Conclusions of this research work described in this thesis are:

- (a) The use of forward-feed capacitors provides significant performance advancements in terms of bandwidth, flatness in gain, and especially overall gain. This is achieved by redirecting the high-frequency signals away from the lossy inductors through the use of capacitors to result in a circuit topology resembling (in terms of signal flow), a conventional cascaded amplifier. This is the first reported case in which experimental results support the use of forward-feed.
- (b) Series-drain inductors have been found to serve two desirable functions. Firstly, they increase gain by affecting the resonance of the drain line, i.e. by reducing its cut-off frequency. Secondly, they reduce the amplitude of the reverse travelling-wave flowing on the drain line from reaching the forward-feed capacitors, significantly improving the gain flatness.
- (c) Tapering and mismatching of the inductor values along the gate- and drain-lines and of the series-drain inductors has been found to validate the hypothesis that these mechanisms increase gain and improve the input and output VSWRs.
- (d) Tapering the values of the lumped-element rectangular spiral inductors of the 'air-bridge' type has been found to improve the performance characteristics of a 1-12 GHz DA. This is the first instance in which measurements of a fabricated DA support their predicted beneficial properties.
- (e) SUPER-COMPACT was demonstrated to be an invaluable CAD technique, permitting a complete analysis and optimization of the distributed amplifier under investigation. With it the inclusion of the most accurate circuit element

models available was made possible.

- (f) From the experimental results, the circuit-element models and the self- and mutual-inductance equations were verified and shown to be sufficiently accurate.
- (g) MACSYMA was found to be a useful tool as a symbolic algebraic manipulator to arrive quickly and accurately at complex and tedious equations.

7.2 Recommendations for Further Work

Although significant progress has been made in this thesis, further work could be undertaken in the following areas:

- (1) The concurrent use of 'real' transmission-lines and forward-feed capacitors over broader bandwidths should be investigated.
- (2) A DA similar to the one presented herein, or with greater bandwidth based on a hybrid design in which discrete MESFETs are wire bonded to a substrate having thin-film 'real' transmission-lines should be designed, fabricated and measured.
- (3) The concept of forward-feed should be extended by inserting various circuit elements such as capacitors between nodes within a DA in order to tailor the flow in signal so as to result in improved performance. This includes feedback and higher-order forward-feed between stages.
- (4) The theoretical analysis of the performance-affecting effects such as tapering, insertion of series-drain inductors, and forward-feed should be improved with the help of a symbolic algebraic manipulator (MACSYMA).
- (5) Models should be derived which express algebraically and numerically the performance degradation due to the skin-effect of both straight conductors and spiral inductors of arbitrary shape.
- (6) Ways should be devised to lower losses exhibited by spiral inductors by widening and thickening the conductors.
- (7) Of primary importance, especially for cases in which DAs are cascaded within a confined area, is the bias circuit which supplies power to the drain terminals

of the FETs. The required bandwidths necessitate considerable design effort especially in view of the lack of literature on this subject.

- (8) Techniques should be investigated for increasing the maximum input and output powers of a DA through control of the constructive voltage interference pattern existing on the drain-line.

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Appendix 1

Simplification of distributed amplifier gain equation (3.3.14) of Section 3.3

The right-hand summation term of (3.3.14) is

$$\sum_{i=1}^n e^{-\{(2i-1)\gamma_g + [2(n-i)+1]\gamma_d\}/2} \quad (A1-1)$$

The constants are brought out of the summation to produce

$$e^{-n\gamma_d} e^{-(\gamma_d - \gamma_g)/2} \sum_{i=1}^n e^{i(\gamma_d - \gamma_g)} \quad (A1-2)$$

The substitution

$$\gamma = \gamma_d - \gamma_g$$

is made into (A1-2) to give

$$e^{-n\gamma_d} e^{-\gamma/2} \sum_{i=1}^n e^{i\gamma} \quad (A1-4)$$

Both the numerator and denominator are then multiplied by

$$e^{\gamma} - e^{-\gamma} \quad (A1-5)$$

producing

$$e^{-n\gamma_d} e^{-\gamma/2} \frac{\sum_{i=1}^n e^{(i+1)\gamma} - \sum_{i=1}^n e^{(i-1)\gamma}}{e^{\gamma} - e^{-\gamma}} \quad (A1-6)$$

and after expanding the summation sign

$$\frac{e^{-n\gamma_d}e^{-\gamma/2}}{e^\gamma - e^{-\gamma}} \left[\sum_{i=1}^{n-2} e^{(i+1)\gamma} + e^{n\gamma} + e^{(n+1)\gamma} - \sum_{(i=1)}^{n-2} e^{(i+1)\gamma} - 1 - e^\gamma \right] \quad (A1-7)$$

Rearranging the above equation gives

$$\frac{e^{-n\gamma_d}e^{-\gamma/2}e^{n\gamma/2}e^{\gamma/2}}{e^\gamma - e^{-\gamma}} \left[(e^{\gamma/2} + e^{-\gamma/2})(e^{n\gamma/2} - e^{-n\gamma/2}) \right] \quad (A1-8)$$

which, after both the numerator and denominator are multiplied by

$$e^{\gamma/2} - e^{-\gamma/2}$$

simplifies to

$$\frac{e^{-n\gamma_d}e^{n\gamma/2}(e^{n\gamma/2} - e^{-n\gamma/2})}{e^{\gamma/2} - e^{-\gamma/2}} \quad (A1-9)$$

Using the mathematical identity

$$\sinh x = \frac{e^x - e^{-x}}{2} \quad (A1-10)$$

(A1-9) can be expressed as

$$e^{-n(A_d+A_g)/2} \frac{\sinh [n(A_d - A_g)/2]}{\sinh [(A_d - A_g)/2]} \quad (A1-11)$$

Appendix 2

Correction to Beyer's Equation

Expression (1) of Beyer et al. [87]

$$I_0 = \frac{1}{2} g_m e^{-\theta_d/2} \left[\sum_{k=1}^n V_{ck} e^{-(n-k)\theta_d} \right] \quad (A2-1)$$

should be expressed as

$$I_0 = \frac{\frac{1}{2} g_m e^{-\theta_d/2} \left[\sum_{k=1}^n V_{ck} e^{-(n-k)\theta_d} \right]}{\sqrt{1 - \left(\frac{\omega}{\omega_c} \right)^2}} \quad (A2-2)$$

since the drain line resonates as the cut-off frequency is approached.

The other erroneous expression in [87] is

$$V_{ck} = \frac{V_i e^{-(2k-1)\theta_g/2 - j \tan^{-1}(\omega/\omega_g)}}{\left[1 + \left(\frac{\omega}{\omega_g} \right)^2 \right]^{1/2} \left[1 - \left(\frac{\omega}{\omega_c} \right)^2 \right]} \quad (A2-3)$$

which should be

$$V_{ck} = \frac{V_i e^{-(2k-1)\theta_g/2 - j \tan^{-1}(\omega/\omega_g)}}{\left[1 + \left(\frac{\omega}{\omega_g} \right)^2 \right]^{1/2} \left[1 - \left(\frac{\omega}{\omega_c} \right)^2 \right]^{1/2}} \quad (A2-4)$$

since the gate line also behaves as a resonating circuit as the cut-off frequency is approached. It just so happens that when the two incorrect expressions, (A2-1) and (A2-3), are combined they produce the same result as produced by the two correct expressions, (A2-2) and (A2-4).

Appendix 3

Gate and Drain line Attenuation

Gate Line Attenuation

The gate line propagation function is

$$\gamma_g = A_g + j\Phi_g = \cosh^{-1} \left(1 + \frac{Z_{g1}}{2Z_{g2}} \right) \quad (A3-1)$$

where A_g and Φ_g are the attenuation and phase shift per section, respectively. The attenuation is

$$A_g = R_e \cosh^{-1} \left(1 + \frac{Z_{g1}}{2Z_{g2}} \right) \quad (A3-2)$$

where R_e signifies taking the real part of the expression. Using the hyperbolic identity

$$\cosh^{-1} x = \ln(x + \sqrt{x^2 - 1}) \quad (A3-3)$$

given by Beyer [102], where we define

$$x = 1 + \frac{Z_{g1}}{2Z_{g2}} \quad (A3-4)$$

one obtains

$$A_g = R_e \ln \left(1 + \frac{Z_{g1}}{2Z_{g2}} + \sqrt{\left(\frac{Z_{g1}}{2Z_{g2}} \right)^2 + \frac{Z_{g1}}{Z_{g2}}} \right) \quad (A3-5)$$

The gate line series and shunt arm impedances Z_{g1} and Z_{g2} are

Figure A3-1 Gate Line Π -Section Schematic.

$$Z_{g1} = j\omega L_g \quad (A3-6)$$

and

$$Z_{g2} = R_i + \frac{1}{j\omega C_{gs}} \quad (A3-7)$$

We now define Z_{go} , ω_c , and Ω as, respectively, the dc characteristic impedance, the cut-off frequency, and the normalized frequency with respect to the cut-off frequency. Differently stated

$$Z_{go} = Z_{\pi}|_{\omega=0} = \sqrt{\frac{L_g}{C_{gs}}} \quad (A3-8)$$

$$\omega_c = \frac{2}{\sqrt{L_g C_{gs}}} \quad (A3-9)$$

and

$$\Omega = \frac{\omega}{\omega_c} \quad (A3-10)$$

where ω is the radian frequency. Combining (A3-8) and (A3-9) and solving for L_g and C_{gs} one obtains

$$L_g = \frac{2Z_{go}}{\omega_c} \quad (A3-11)$$

and

$$C_{gs} = \frac{2}{Z_{go}\omega_c} \quad (A3-12)$$

By defining

$$\alpha_g = \frac{R_i}{Z_{go}} \quad (A3-13)$$

and inserting it, together with (A3-10), (A3-11) and (A3-12), into (A3-6) and (A3-7) one finds the series and shunt arm impedances:

$$Z_{g1} = j2\Omega Z_{g0} \quad (\text{A3-14})$$

$$Z_{g2} = Z_{g0} \left(\alpha + \frac{1}{j2\Omega} \right) \quad (\text{A3-15})$$

respectively, in terms of normalized parameters. Inserting these equations into the attenuation function (A3-5), we find, after simplification

$$A_g = R_e \ln \left[\frac{\sqrt{\Omega^2 - 1 - j2\Omega\alpha_g} - \Omega}{\sqrt{\Omega^2 - 1 - j2\Omega\alpha_g} + \Omega} \right] \quad (\text{A3-16})$$

After much further simplification one obtains

$$A_g = \frac{1}{2} \ln \left[\frac{(\sqrt{C'} + \Omega)^2 + D'}{(\sqrt{C'} - \Omega)^2 + D'} \right] \quad (\text{A3-17})$$

where

$$C' = \frac{\sqrt{(1 - \Omega^2) + (2\Omega\alpha_g)^2} + \Omega^2 - 1}{2} \quad (\text{A3-18})$$

$$D' = \frac{\sqrt{(1 - \Omega^2) + (2\Omega\alpha_g)^2} - \Omega^2 + 1}{2} \quad (\text{A3-19})$$

Equation (A3-17) can be approximated by rearranging it in the form

$$A_g = \frac{1}{2} \ln \frac{1+k}{1-k} \quad (\text{A3-20})$$

where k is defined as

$$k = \frac{2\Omega\sqrt{C'}}{C' + D' + \Omega^2} \quad (\text{A3-21})$$

By using the logarithmic identity given by Beyer [102]

$$\ln \frac{1+k}{1-k} = 2 \left[k + \frac{k^3}{3} + \dots \right] \quad (A3-22)$$

and discarding the third-order terms and higher, one obtains

$$A_g \approx \frac{2\Omega\sqrt{C'}}{C' + D' + \Omega^2} \quad (A3-23)$$

which is valid for $A_g < 0.4N_p/\text{section}$ (Nepers). By letting

$$k' = \sqrt{(1 - \Omega^2) + (2\Omega\alpha_g)^2} + \Omega^2 \quad (A3-24)$$

one obtains for the gate line attenuation

$$A_g \approx \frac{\Omega\sqrt{2(k' - 1)}}{k'} \quad (A3-25)$$

The parameter k' can be expressed as

$$k' = (1 - \Omega^2)\sqrt{1 + k''} + \Omega^2 \quad (A3-26)$$

where

$$k'' = \left(\frac{2\Omega\alpha_g}{1 - \Omega^2} \right)^2 \quad (A3-27)$$

Using the binomial series

$$(1 + x)^{1/2} = 1 + \frac{x}{2} - \frac{x^2}{8} + \dots \quad (A3-28)$$

one obtains for k'

$$k' = (1 - \Omega^2) \left[1 + 2 \left(\frac{\Omega\alpha_g}{1 - \Omega^2} \right)^2 \right] + \Omega^2 \quad (A3-29)$$

when higher than first-order terms are excluded. Simplifying the above equation, one obtains

$$k' \approx 1 + \frac{2\Omega^2 \alpha_g^2}{1 - \Omega^2} \quad (\text{A3} - 30)$$

After inserting this into (A3-25) and further simplifying one finally obtains

$$A_g \approx \frac{2\Omega^2 \alpha_g}{\sqrt{1 - [1 - (2\alpha_g)^2] \Omega^2}} \quad (\text{A3} - 31)$$

This equation is identical to the one given by Beyer [87] (equation (8)) except for the fact that it has been expressed with different parameters.

Drain line attenuation

Contrary to Beyer's [87] assertion, the drain line attenuation cannot be solved using equation (3.2.16), unfortunately, as was done for the gate line. The reason for this is that if we substitute the proper series and shunt arm impedances of Fig. A3-2 into the T-section port image-impedance equation (3.2.14) we obtain

$$Z_I = \sqrt{\frac{j\omega L_d}{G_{ds} + j\omega C_d} \left(1 + \frac{j\omega L_d (G_{ds} + j\omega C_d)}{4} \right)}. \quad (\text{A3} - 32)$$

At dc when $\omega = 0$ the image impedance as seen from either port 1 or 2 of Fig. A3-2 is

$$Z_I|_{\omega=0} = 0$$

which implies that the impedance as seen looking into the output of the distributed amplifier would appear as a short circuit. Practically this is not the case, therefore the propagation function cannot be solved using equation (3.2.16). The reason for this is that by cascading an infinite number of 'T'-sections, one can show that at dc the equivalent circuit is an infinite number of paralleled conductances G_{ds} as

Figure A3-2 Drain Line T-Section Schematic.

seen across any port on the line. In other words, a short circuit appears across the section under measurement and this explains why $Z_I = 0$.

Another approach to solving the problem is to treat it by considering power flow attenuation instead of voltage magnitude decay. Here we use the following equation to define the propagation function:

$$\frac{V_2}{V_1} = e^{-(A_d + j\Phi_d)} \quad (\text{A3} - 33)$$

where A_d and Φ_d are the drain line attenuation and phase shift per section, respectively.

Since

$$\begin{aligned} V_1 &= I_1 Z_1 \\ V_2 &= I_2 Z_2 \end{aligned} \quad (\text{A3} - 34)$$

and assuming that the image impedances Z_1 and Z_2 shown in Fig. A3-3, are approximately equal, one obtains

$$\frac{I_2}{I_1} = \frac{V_2}{V_1} = e^{-(A_d + j\phi_d)} \quad (\text{A3} - 35)$$

From this equation it can be shown that

$$\frac{I_2^*}{I_1^*} = e^{-(A_d + j\phi_d)} \quad (\text{A3} - 36)$$

where * signifies the complex conjugate. The ratio between the power flowing into Z_2 from port 2 and the power flowing into port 1 is given by the product of (A3-35) and (A3-36) or

$$\frac{P_2}{P_1} = \frac{V_2 I_2^*}{V_1 I_1^*} = e^{-2A_d} \quad (\text{A3} - 37)$$

Since A_d is a positive real value, this power ratio is also a real value. In other words, on a complex plane, the vector P_2 is aligned exactly with P_1 . The projection

Figure A3-3 T-section Used to Obtain A_d with Normalized Impedances.

of these vectors on to the real and imaginary axis forms similar triangles from which one can deduce that

$$\frac{P_{2R}}{P_{1R}} = \frac{P_{2I}}{P_{1I}} = \frac{P_2}{P_1} = e^{-2A_d} \quad (\text{A3-38})$$

where the subscripts R and I signify the real and imaginary components, respectively. The real power P_R flowing into a complex load Z with applied voltage V is

$$P_R = \left| \frac{V}{Z} \right|^2 \frac{R_e Z}{2} \quad (\text{A3-39})$$

Substituting this equation into (A3-38), one obtains

$$\frac{P_{2R}}{P_{1R}} = \left| \frac{V_2}{V_1} \frac{Z_1}{Z_2} \right|^2 \frac{R_e Z_2}{R_e Z_1} = e^{-2A_d}. \quad (\text{A3-40})$$

Rearranging this equation:

$$A_d = \frac{1}{2} \ln \left[\left| \frac{V_1}{V_a} \frac{V_a}{V_2} \frac{Z_2}{Z_1} \right|^2 \frac{R_e Z_1}{R_e Z_2} \right] \quad (\text{A3-41})$$

where V_a has been defined as the voltage across the shunting impedances Y_R and Y_C shown in Fig. A3-3. From this figure one can derive

$$\begin{aligned} \frac{V_1}{V_a} &= \frac{Z_1}{Z_1 - j\Omega Z_{do}} \\ \frac{V_a}{V_2} &= \frac{Z_2 + j\Omega Z_{do}}{Z_2} \\ Z_2 &= Z_{do} \sqrt{1 - \Omega^2} \\ Z_1 &= Z_{do} \left(j\Omega + \frac{1}{\alpha_d + \sqrt{1 - \Omega^2} + j\Omega} \right) \end{aligned} \quad (\text{A3-42})$$

where, similarly to the gate line attenuation derivation,

$$\begin{aligned}
\frac{1}{Y_{do}} &= Z_{do} = \sqrt{\frac{L_d}{C_d}} \\
\alpha_d &= \frac{G_{ds}}{Y_{ds}} \\
\Omega &= \frac{\omega}{\omega_c} \\
\omega_c &= \frac{2}{\sqrt{L_d C_d}}
\end{aligned} \tag{A3-43}$$

It should be noted that an imposed constraint is that both the gate and drain line cut-off frequencies be equal so as to satisfy the need for identical phase shift per section on both lines. Inserting (A3-43) and (A3-42) into (A3-41), one obtains after much simplification

$$A_d = \frac{1}{2} \ln \left[\frac{|\alpha_d + \sqrt{1 - \Omega^2} + j\Omega|^2 R_e \left(j\Omega + \frac{1}{\alpha_d + \sqrt{1 - \Omega^2} + j\Omega} \right)}{\sqrt{1 - \Omega^2}} \right] \tag{A3-44}$$

Further simplification yields

$$A_d = \frac{1}{2} \ln \left(1 + \frac{\alpha_d}{\sqrt{1 - \Omega^2}} \right) \tag{A3-45}$$

To simplify this equation, the logarithmic expansion

$$\ln(1 + x) = x - \frac{1}{2}x^2 + \dots \tag{A3-46}$$

is used. By only keeping the first term on the right-hand-side, knowing that $\alpha_d/\sqrt{1 - \Omega^2} \ll 1$, one obtains

$$A_d \approx \frac{\alpha_d/2}{\sqrt{1 - \Omega^2}} \tag{A3-47}$$

for $A_d \leq 0.4 N_p/\text{section}$.

One important comment about this equation is that the drain line is lossy even at dc ($\Omega = 0$) if $\alpha_d \neq 0$. This equation is identical to the one given by Beyer [87] (equation 9) except for the fact that it has been expressed with different parameters.

Appendix 4

SUPER-COMPACT File for the Distributed Amplifier

FILE AUDIT DATA A BELL-NORTHERN RESEARCH

SUPER-COMPACT Version 1.7 + 001 04/09/84 08 56 40 01/04/86

RTO 1 166
TAP 500PH

LSOR 30PH

.....
LG1 157PH
LG2 1577PH
LG3 1986PH
LG4 1986PH
LG5 948PH

Gate-Line Inductance Parameters of
Inductor Cell and Interconnect.

.....
RG1 0 5
RG2 4 60
RG3 5 31
RG4 5 31
RG5 3 12

Gate-Line DC Resistance of Inductor
Cell and Interconnect.

.....
LF1 891PH
LF2 727PH
LF3 515PH
LF4 568PH

Series-Drain Inductance Parameters of
Inductor Cell and Interconnect.

.....
RF1 2 76
RF2 2 63
RF3 1 69
RF4 1 81

Series-Drain DC Resistance of Inductor
Cell and Interconnect.

.....
LD1 1552PH
LD2 1156PH
LD3 1277PH
LD4 796PH
LD5 94PH

Drain-Line Inductance Parameters of Inductor
Cell and Interconnect.

.....
RD1 4 0
RD2 2 98
RD3 3 04
RD4 2
RD5 0 14

Drain-Line DC Resistance of Inductor Cell
and Interconnect.

.....
CP1 298 871FF

Forward-Feed Capacitance.

.....
BLK

IND 15 0 L LSOR
FET 12 17 15 G+0 0215 CGS=0 232PF
+ T=2 50E-12 CDG=27FF CDS=45FF
+ RI=20 GDS=0 0019
FETT 2POR 12 17
END

MESFET Model.

```

.....
..
.. THE FOLLOWING (GIN*) SUBCIRCUITS ARE THE EQUIVALENT MODELS ..
.. OF THE GATE LINE INDUCTORS ..
..
.....

```

```

BLK
SRL 1 2 R=(RTO*RG1) L=((LG1)/4 22-20/(1E12))
RES 1 2 R=(7*RG1)
IND 2 3 L=(LG1)
CAP 1 3 C=(8.81/(1E15)+6.65/(1E6)*(LG1))
CAP 1 0 C=10FF
GIN1 2POR 1 3
END
BLK
SRL 1 2 R=(RTO*RG2) L=((LG2)/4 22-20/(1E12))
RES 1 2 R=(7*RG2)
IND 2 3 L=(LG2-TAP)
IND 3 4 L=TAP
CAP 1 3 C=(8.81/(1E15)+6.65/(1E6)*LG2)
CAP 1 0 C=10FF
GIN2 3POR 1 4 3
END
BLK
SRL 1 2 R=(RTO*RG3) L=((LG3)/4 22-20/(1E12))
RES 1 2 R=(7*RG3)
IND 2 3 L=(LG3-TAP)
IND 3 4 L=TAP
CAP 1 3 C=(8.81/(1E15)+6.65/(1E6)*LG3)
CAP 1 0 C=10FF
GIN3 3POR 1 4 3
END
BLK
SRL 1 2 R=(RTO*RG4) L=((LG4)/4 22-20/(1E12))
RES 1 2 R=(7*RG4)
IND 2 3 L=(LG4-TAP)
IND 3 4 L=TAP
CAP 1 3 C=(8.81/(1E15)+6.65/(1E6)*LG4)
CAP 1 0 C=10FF
GIN4 3POR 1 4 3
END
BLK
SRL 1 2 R=(RTO*RG5) L=(LG5/4 22-20/(1E12))
RES 1 2 R=(7*RG5)
IND 2 3 L=LG5
CAP 1 3 C=(8.81/(1E15)+6.65/(1E6)*LG5)
CAP 1 0 C=10FF
GIN5 2POR 1 3

```

```

.....
..
.. THE FOLLOWING (DIN*) SUBCIRCUITS ARE THE EQUIVALENT MODELS
.. OF THE DRAIN LINE INDUCTORS
..
.....

```

```

BLK
SRL 1 2 R=(RTO*RD1) L=(LD1/4 22-20/(1E12))
RES 1 2 R=(7*RD1)
IND 2 3 L=LD1
CAP 1 3 C=(8 81/(1E15)+6 65/(1E6)*LD1)
DIN1 2POR 1 3
END

```

```

BLK
SRL 1 2 R=(RTO*RD2) L=(LD2/4 22-20/(1E12))
RES 1 2 R=(7*RD2)
IND 2 3 L=LD2
CAP 1 3 C=(8 81/(1E15)+6 65/(1E6)*LD2)
DIN2 2POR 1 3
END

```

```

BLK
SRL 1 2 R=(RTO*RD3) L=(LD3/4 22-20/(1E12))
RES 1 2 R=(7*RD3)
IND 2 3 L=LD3
CAP 1 3 C=(8 81/(1E15)+6 65/(1E6)*LD3)
DIN3 2POR 1 3
END

```

```

BLK
SRL 1 2 R=(RTO*RD4) L=(LD4/4 22-20/(1E12))
RES 1 2 R=(7*RD4)
IND 2 3 L=LD4
CAP 1 3 C=(8 81/(1E15)+6 65/(1E6)*LD4)
DIN4 2POR 1 3
END

```

```

BLK
SRL 1 2 R=(RTO*RD5) L=(LD5/4 22-20/(1E12))
RES 1 2 R=(7*RD5)
IND 2 3 L=LD5
CAP 1 3 C=(8 81/(1E15)+6 65/(1E6)*LD5)
DIN5 2POR 1 3
END

```



```

.....
..
.. THE FOLLOWING (FIN*) SUBCIRCUITS ARE THE EQUIVALENT MODELS ..
.. OF THE SERIES DRAIN INDUCTORS ..
.....
.
BLK
SRL 1 2 R=(RTO*RF1) L=(LF1/4 22-20/(1E12))
RES 1 2 R=(7*RF1)
IND 2 3 L=LF1
CAP 1 3 C=(8.81/(1E15)+6.65/(1E6)*LF1)
FIN1 2POR 1 3
END
BLK
SRL 1 2 R=(RTO*RF2) L=(LF2/4 22-20/(1E12))
RES 1 2 R=(7*RF2)
IND 2 3 L=LF2
CAP 1 3 C=(8.81/(1E15)+6.65/(1E6)*LF2)
FIN2 2POR 1 3
END
BLK
SRL 1 2 R=(RTO*RF3) L=(LF3/4 22-20/(1E12))
RES 1 2 R=(7*RF3)
IND 2 3 L=LF3
CAP 1 3 C=(8.81/(1E15)+6.65/(1E6)*LF3)
FIN3 2POR 1 3
END
BLK
SRL 1 2 R=(RTO*RF4) L=(LF4/4 22-20/(1E12))
RES 1 2 R=(7*RF4)
IND 2 3 L=LF4
CAP 1 3 C=(8.81/(1E15)+6.65/(1E6)*LF4)
FIN4 2POR 1 3
END
. ....

```

```

.....
.. THE FOLLOWING (MDA) BLOCK DESCRIBES THE INTERCONNECTS AND THE ..
.. CIRCUIT ELEMENTS OF THE DA (DISTRIBUTED AMPLIFIER). ..
.....

```

```

BLK

```

```

.....
.. FIRST STAGE OF THE DA ..
.....

```

```

GIN1 11 12
GIN2 12 22 19
FETT 12 16
FIN1 16 17
DIN1 15 17
CAP 17 0 C=15FF
.....
CAP 16 19 C CP1

```

```

.....
.. SECOND STAGE OF THE DA ..
.....

```

```

GIN3 22 32 29
FETT 22 26
FIN2 26 27
DIN2 17 27
CAP 27 0 C=15FF
.....
CAP 26 29 C CP2

```

```

.....
.. THIRD STAGE OF THE DA ..
.....

```

```

GIN4 32 42 39
FETT 32 36
FIN3 36 37
DIN3 27 37
CAP 37 0 C=15FF
.....
CAP 36 39 C CP3

```

```

.....
.. FOURTH STAGE OF THE DA ..
.....

```

```

GIN5 42 43
FETT 42 46
FIN4 46 47
DIN4 37 47
CAP 47 0 C=15FF
DIN5 47 48

```

```

.....
..
.. GATE AND DRAIN TERMINATIONS AND PARASITIC INPUT/OUTPUT PAD ..
.. CAPACITANCES ..
..
.....

```

```

RES 42 0 R=732 8597
SRC 15 0 P=2127 52 C=5PF
CAP 11 0 C=20FF
CAP 48 0 C=20FF
MDA 2POR 11 48
END

```

```

.....
..
.. FREQUENCY BAND OF INTEREST ..
.. - SCATTERING PARAMETERS OF DA WITH STABILITY AND GROUP DELAY ..
..
.....

```

```

FREQ
STEP 1GHZ 12GHZ 1 GHZ 13GHZ
END
OUT
PRI MDA SK GD
END

```

```

.....
..
.. OPTIMIZATION DESCRIPTION ..
..
.....

```

```

OPT
MDA
MS11= 25 LT W=2000 MS22= 25 LT W=2000 MS21=7 5DB W=9
END

```

END

22-06-88

FIN