NOTE TO USERS

Microwave Coplanar Waveguide Tunable Filters Using RF MEMS

by

Michael Mariani, B. Eng.

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Ottawa-Carleton Institute for Electrical Engineering
Department of Electronics
Faculty of Engineering
Carleton University
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Abstract

The objective of the thesis is to create an integrated tunable microwave bandpass filter in the coplanar waveguide (CPW) line regime. Finger patterning within the centre metal trace will provide the filtering structure and micro electro mechanical systems (MEMS) switches will provide the tuning capability.

An existing uniplanar bandpass CPW filter structure is selected. Modification of the filter is investigated using Ansoft HFSS 3D-modeling software tool to change the filtering characteristic to the desired frequency range and meet fabrication requirements. A lumped equivalent circuit of the final CPW filtering structure is created.

Two MEMS switch locations are investigated and lumped equivalent circuits for the switches are proposed. The resulting CPW filtering structure is novel in that the switches are extremely narrow in width and they are over a patterned centre conductor, providing prescribed transmission characteristics in both states.

Modeling of the CPW filter with the MEMS switches is done using both HFSS and by adding the switch equivalent circuit to the filter equivalent circuit. A bridge in the middle of the CPW filtering structure produces a 2 GHz tuning effect and a bridge placed after the filter primarily alters the reflection coefficients at a separate location.

The proposed tunable filter is fabricated using Carleton University's fabrication facilities. The measured results and HFSS theoretical results are well correlated. A 2.75 GHz shift of the notch frequency from 25 GHz to 22.25 GHz with insertion loss of 25 dB and 21.75 dB respectively is measured when actuating one of the bridges.

Acknowledgements

I would like to thank first and foremost both of my co-supervisors, Dr. Langis Roy and Dr. Niall Tait for their guidance and support during this research.

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Finally, I am also grateful to my family for their patience and support. They have seen my at my worst and helped me to achieve my best.

Thank you all.

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List of Acronyms

3D	three dimensions
ADS	Advanced Design System (Agilent Technologies simulation software)
CMOS	complimentary metal oxide semi conductor
CPS	coplanar strip line
CPW	coplanar waveguide
DC	direct current
EM	electro magnetic
GSG	ground signal ground
HFSS	Ansoft HFSS (simulation software)
HF	hydro fluoric acid
HMDS	hexamethyldisilizane
IC	integrated circuit
MEMS	micro electro mechanical systems
GHz	giga hertz
MMIC	monolithic microwave integrated circuit
0	oxygen
RF	radio frequency
Si	silicon

Chapter 1

Introduction

1.1 Motivation

As mobile communication systems require increasingly accurate frequency selection, while physical volume, component count and cost considerations prohibit the redundancy of several filtering devices at different frequencies, there is a growing need to have a single component that can be adjusted to satisfy a variety of applications.

One area where tunability is particularly valuable is with filters, where tunability can not only provide compensation of fabrication tolerances, but may also allow for filters to select multiple frequencies that are very far apart. One example would be a filter that could be used on a satellite receiver to select either a received signal from an earth station or a signal from another satellite which is at a different frequency.

There are many possible ways of implementing a tunable microwave filter. Planar microwave circuits are attractive and a large body of work exists on the realization of filters using microstrip transmission line regime. Fewer studies have been done to realize the same structures with coplanar waveguides (CPW). However, CPW uniplanar design is particularly desirable to work with for several reasons. There is no need for via holes to connect metal lines to ground. This reduces the parasitic inductance

associated with through substrate connections. Also, coplanar ground planes help to decouple adjacent signal lines. Finally, miniaturization of circuit designs can be easily accomplished in CPW through patterning of the centre conductor as will be seen in subsequent chapters.

There are also several ways to achieve tunability of microwave devices. One approach that is compatible with planar circuits is the use of micro electro mechanical switching elements to change the frequency. The CPW uniplanar designs are ideal for adding micro electro mechanical systems (MEMS) technology because most MEMS fabrication uses the same processes that are used in integrated circuit (IC) air bridge fabrication. High isolation and low insertion loss also make MEMS switches an attractive option when compared to lossier alternatives [1] [2].

The most conventional operation of a MEMS switch is to alter a signal conduction path by allowing the signal to pass in one state but not in the other. It would be interesting to examine the loading effect that a MEMS bridge has on a patterned CPW centre conductor when the signal is allowed to pass in both states. One could alter the characteristics of a CPW filter without completely impeding the signal. The change in height of a switch multiplies the capacitive, inductive and resistive load on the filter, thereby changing the filter response in perhaps a simpler way then previously possible.

There are several advantages to pursuing a solution using MEMS technology. By integrating the tuning mechanism with the filter design, one can potentially increase reliability and decrease the parasitic capacitances while decreasing the physical layout dimensions.

Batch fabricated devices are separately constructed, cut and tested before assembling the components together. Although all individual components may have a lower price than a fully integrated unit, a device assembled from separate components is generally less reliable than an integrated solution. Integrated solutions also provide

lower interconnection and parasitic losses than assembled components due to the elimination of input and output matching networks and due to the effects of physical assembly.

1.2 Thesis Objectives

The overall objective of the thesis is to create an integrated tunable microwave filter. Coplanar waveguide (CPW) lines are chosen as the transmission medium, finger patterning of the centre metal trace are to provide the filtering mechanism and micro electro mechanical systems (MEMS) switches are to provide the tuning capability. In order to meet this general goal, the following specific objectives are to be pursued.

The first thesis objective is to identify and modify a currently existing CPW filter structure. Modification of the filtering structure is done to change the filtering characteristic to the desired frequency range and to meet Carleton University fabrication facilities. For design purposes, a lumped equivalent circuit of the final CPW filtering structure is to be developed.

The second thesis objective is to design, fabricate, and model two MEMS switches that will allow tuning of the filter structure.

The third thesis objective is to explore a novel tunable filter design using both 3D EM modeling tools and lumped element circuits to determine if the desired filtering and tuning effect are obtained.

The final thesis objective is to fabricate, test, and compare the measured results of the tunable filter with the simulation results.

1.3 Thesis Organization

The thesis is divided into six chapters. The first chapter gives a general overview of the proposed work, comprising the motivation, objectives and organization.

The second chapter provides additional information on the different technologies that will be used to achieve the proposed goals and a comparison of the proposed design with other technologies.

The third chapter describes the modeling and simulation of the CPW filter and the necessary changes to the equivalent circuit that will be needed to adapt the proposed structure for our desired frequency range and to be compatible with our fabrication facilities. An overview of the design of the MEMS switch that will be fabricated and the considerations that were used to determine the dimensions will be presented. Fabrication and measurements of the proposed switch will described as will the creation of an equivalent circuit of the proposed switches. Discussions regarding approximate hand calculations and simulation results will be discussed.

The fourth chapter provides a description of the process steps that have been followed in the fabrication procedure.

The fifth chapter describes the testing method and gives the measured results of the CPW and MEMS tunable filter. Discussion of the results and proposed modifications and improvements are also included.

The sixth chapter contains the thesis conclusions and recommendations for future work.

Chapter 2

Review of coplanar waveguides and MEMS devices

In today's society, there is constant research to fabricate devices that are more compact, energy efficient, and cheaper to construct. These devices not only are increasingly demanded by consumers but they also allow manufacturers to increase their profit and lower their prices. One of the developing technologies that shows promise to achieve all these goals simultaneously is micro electro mechanical systems (MEMS). This thesis will exploit characteristics that a MEMS switch imposes on a fundamental circuit structure, a coplanar waveguide filter, to address all the concerns listed above.

As a signal is received, the desired frequency must be selected from the entire bandwidth to isolate it from interference from other signals. For this reason, one of the fundamental circuit functions is filtering. Although there are several different ways to create a filter, only CPW filters will be examined.

In this chapter, advantages of a coplanar waveguide medium is discussed with a concentration on patterned discontinuities. A review of common micro electro mechanical systems systems follow and several radio frequency MEMS applications are presented.

2.1 Coplanar Waveguides

2.1.1 Advantages of coplanar waveguides

Since 1969 when C.P. Wen first fabricated a coplanar waveguide (CPW) on a dielectric surface [3], CPW technology has been improved to develop and design compact and better performing devices for both microwave integrated circuits (MIC) and monolithic microwave integrated circuits (MMIC).

Conventional CPW consists of a centre conductor of size S with two finite ground planes on either side separated by a gap of size W as shown below:

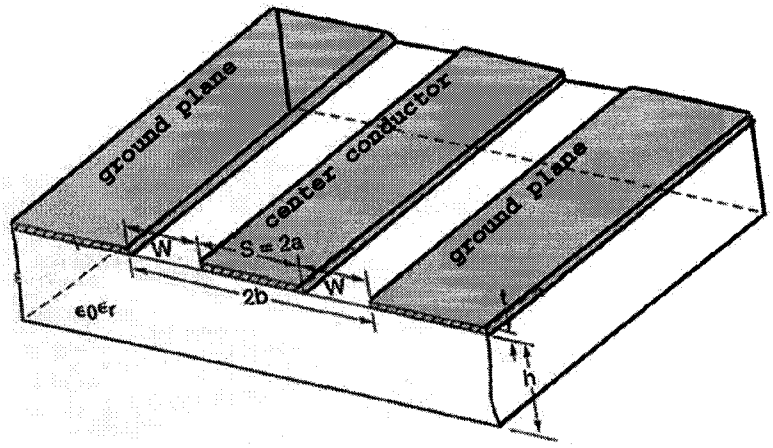

Figure 2.1: Schematic of a coplanar waveguide layout modified from [4]

With respect to microstrip, having the ground lines in the same plane as the centre conductor has several advantages. First by having parallel ground lines, one can eliminate the need for wraparound metallization and via holes that would go to the wafer backside. This reduces the parasitic inductance which lowers the associated losses. Also with ground planes separating parallel conducting lines, there is less cross talk between signals, thus allowing the lines to be closer to one another. Furthermore, the ground planes aid in reducing the amount of radiated losses. Another general advantage to CPW is that shunt and series surface mounting of active and passive devices are easy to mount on a surface that has conduction lines and ground planes

on the same surface. Finally, the characteristic impedance of the centre conductor can be determined by the ratio between the width of the centre conductor, shown as $2a$ in Figure 2.1, and the width of half of the centre conductor combined with the gap width, shown as b in Figure 2.1. By accepting a higher generated loss, one can reduce the size of the centre conductor and gap if the proper proportions are maintained. As a result, CPW lines can be made denser than conventional microstrip.

2.1.2 Discontinuities

One of the most useful techniques used to create a filter response within a CPW line is by introducing discontinuities. The most general types that will be found are open end, short end, and series gap in both the centre conductor and in the ground planes. Step changes in the width of the centre strip conductor and right angle bends are also very common.

There are several different studies that further examine the possibilities of creating filters using patterned discontinuities, as shown by Hettak [5], Ho [6], Chang [7], Ida [8], and Swanson [9]. Patterned designs on the interior of the ground plane and the interior of the centre conductor are both common. Capacitance and inductance are dependent on the CPW substrate dielectric constant, the CPW characteristic impedance, the length of the lines, and the gap thickness [4].

There are benefits to locating patterned structures in either the ground plane or centre conductor. Ponchak and Katehi determined that varying a stub's position in the ground planes instead of the centre conductor can vary the Q that is obtained[10]. A typical stub for microstrip lines is a length of transmission line that is connected to the main line placed at specific places to eliminate reflections at a given frequency. For CPW, finger traces in the ground planes or in the centre conductor can act as stubs. Furthermore, stubs in the ground planes have the same resonant frequency

as those in the centre conductor but the capacitance is doubled and the inductance is halved for the same stub in the centre conductor. But Hettak found that a lower radiation loss, higher compactness, and a lower number of potentially expensive air bridges can be obtained with patterned traces in the centre conductor [11].

There is a push to make designs smaller as designers demonstrate how to combine different structures together, as in [5]. The ability to group different discontinuities together as building blocks to be able to build a custom filter has a strong appeal to many designers. This would greatly decrease the amount of time needed to fabricate designs. Unfortunately, attempts to make general equivalent circuits are difficult. Dib, Katehi, Ponchak, and Simons have created equivalent circuits for both a short and open CPW series stubs discontinuities [12]. The equivalent circuits are reported to be valid for variations in the length of the filter structure, but all other CPW characteristics, such as the centre conductor size S, gap width W, and trace thickness must remain unchanged in order for the equivalent circuit to predict the response.

This thesis proposes to further increase the value of coplanar waveguide resonators by attempting to make them more versatile through the use of MEMS technology for circuit tunability. We step look at how a typical MEMS switch can affect the coplanar waveguide structures.

2.2 Micro Electro Mechanical Systems

Micro electro mechanical systems (MEMS) is a technology that has developed from the integrated circuit (IC) industry. It uses micromachining techniques to add new layers or selectively etch parts of the silicon wafer to create devices that form mechanical and electromechanical devices.

Although many applications can be done without incorporating MEMS technology, there are several advantages that are typically associated with MEMS devices over conventional designs. MEMS provides a new set method to miniaturize the physical structure of layouts. This reduction not only is beneficial in reducing the size and weight of devices, but the miniaturization has also shown increased signal speeds and signal quality compared to other technologies.

The fabrication methods used to create these devices are generally the same processes used in current clean-room manufacturing for high-volume integrated circuit semiconductor devices. This makes them ideal for their integration with current applications. Most of the applications that are currently using MEMS are large batch, high volume applications.

One of the high volume applications is ink jet actuators and print heads. For instance, Epsons ink jet POS printer TM-J710 uses an alternating DC voltage between a pressure plate and electrodes to actuate the plate up and down due to electrostatic forces as shown in Figure 2.2. In the process ink droplets are ejected from the storage cavity as shown in Figure 2.3.

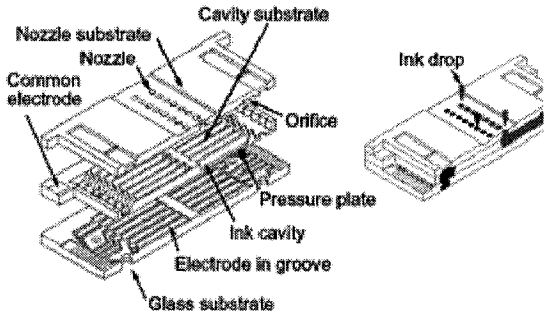

Figure 2.2: Exploded View of SEAJet(R) Printhead from [13]

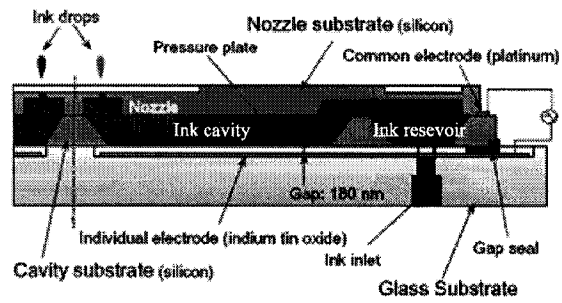

Figure 2.3: Cross-Sectional View of SEAJet(R) Printhead from [13]

Given that the power consumption is much less than other technologies, thermal printheads use one thousand times more power and piezoelectric print heads use ten times more power, Epson is looking at using battery driven printers. The technology is so versatile that they are examining applying the same MEMS process to other materials instead of ink, such as biomaterials and proteins.

Another high volume application is inertial MEMS sensors which can sense movement in all three linear axes by measuring capacitance changes in between fixed and moving structures. Structures can be arranged like interlocking combs to create linear accelerometers, such as in automobile airbags, or in a circular pattern like the spokes of a wheel to create rotational accelerometers, which are used in gyroscopes and rollover prevention monitoring for automobiles. As the comb fingers shown in Figure 2.4 move, the distance between stationary fingers and moving fingers changes. The change in distance causes a change in capacitance which can be measured.

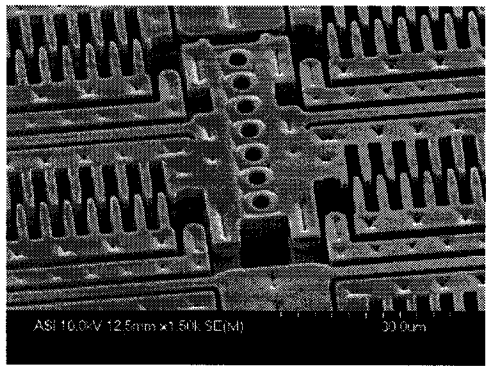

Figure 2.4: Large Force Electrostatic MEMS Actuator Segment- Photo Courtesy of MEMX inc. (www.memx.com)

Medical fields are also looking into MEMS based research. Silicon micromachined pressure sensors are currently the most actively researched biomedical MEMS application but chemical sensing and microfluidic systems fields are growing rapidly. The most common pressure sensors are blood pressure, bladder pressure, and cerebral spinal fluid pressure sensors. NovaSensor, which was acquired by General Electric in 2002 and is now a part of GE Infrastructure's sensing business, was one of the companies that built MEMS biomedical test instruments and devices.

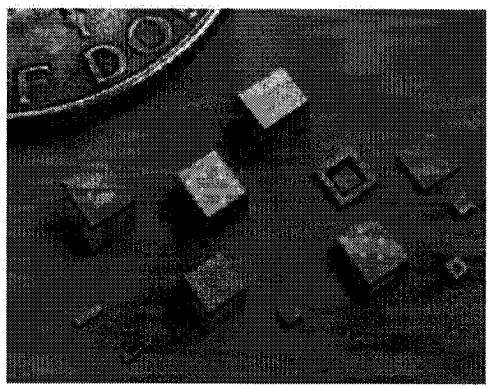

Figure 2.5: Pressure sensors created by NovaSensor from [14]

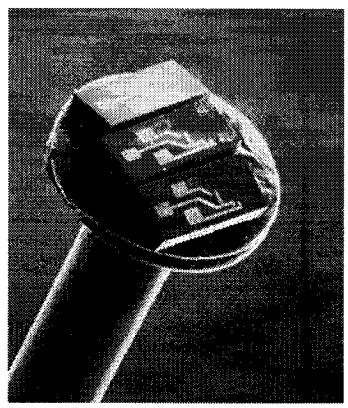

Figure 2.6: Intercardial catheter-tip sensors created by NovaSensor from [15]

Figure 2.5 displays multiple sensors that are inserted into a catheter and inserted into arteries. Figure 2.6 shows intercardial catheter-tip sensors MEMS transducers that monitor blood pressure during cardiac catheterization.

Military and commercial application often require strict signal requirements. Military communication is one such application where multiple transmitters and receivers are on the same platform. This generally requires filtering on both transmitters and receivers to insure that one does not interfere with the other.

The possibility that MEMS technology can implement minor or dramatic tuning adjustments to a system's frequency, phase, matching and other system parameters while consuming low amounts of power have created a developing interest in radio frequency (RF) MEMS applications. The devices that have gained the highest interest include tunable capacitors, RF switches, high-Q inductors and high-Q mechanical resonators and filters.

2.2.1 RF MEMS

RF MEMS are typically described as miniaturized components that are used to alter, tune, or inhibit the conduction of microwave signals.

One of the more common uses for RF MEMS has typically been as a switch to impede a signal from passing underneath it in the actuated state and little interference when not actuated, or vice versa. One example is given by Malczewski, et al. who described phase shifters using RF MEMS [2]. In their design, a signal is allowed to pass in a delay line and is typically reflected at the shorted line at the end. Switches were placed on top of the delay line and have no effect while in the up position. When a switch is actuated, it provides a RF short at a different point to change the length that the signal will pass down the delay line and thus change the phase. The authors report that MEMS devices are typically slower than GaAs transistors or p-i-n diodes, however MEMS are reported to enable the creation of smaller designs that have lower

loss and resistance.

This thesis concentrates on changing the load on the conducting signal path but not completely impeding the signal. Muldavin and Rebeiz examined how to model a MEMS switch connected to the ground conductor on a silicon substrate [16]. They modeled the capacitance in the up state of the switch using the measured S_{11} parameter and neglected the inductance and the resistance because the effect of the resistance and inductance is minimal. In the up state, the authors used a microwave circuit simulator (Libra) to create an equivalent circuit. By using similar equations, one can create approximation of the equivalent circuits of other switch designs and one can use the equivalent circuits to determine how the switch will affect the signal that passes under the bridge. Unfortunately, this also requires knowing the equivalent circuit of the system underlying the switch and how to incorporate the switch in the equivalent circuit.

Even with these obstacles, there are many researchers who have developed tuning devices using several approaches. Lakshminarayanan and Weller proposed in [17] a tunable RF MEMS bandpass filter that operated between 16.5 GHz and 22 GHz by actuating 33 capacitive bridges at voltages between 45 and 50 V. The design has six open stubs that are $\lambda/2$ long and three series $\lambda/4$ long connecting lines between the open stubs. There are four capacitive bridges separated by 350 μm on each open stub that change from 0.2 pF in the up state to 0.4 pF in the down. There are also three capacitive bridges over each series connecting line that change from approximately 0.07 pF to 0.1 pF. MIM capacitors are placed 40-50 μm away from each MEMS capacitor.

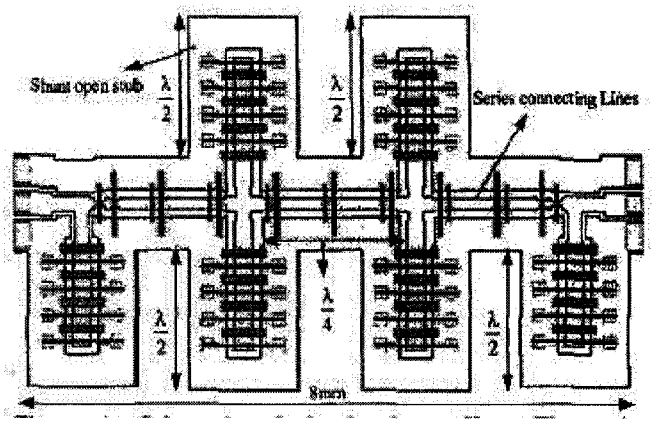

Figure 2.7: Schematic from Lakshminarayanan and Weller bandpass filter [17]

CPW is not the only transmission line that is currently being researched for use with MEMS tuning capacitors. Nordquist et al used surface-micromachined capacitors to vary capacitance on a coupled coplanar strip filter to alter the resonant frequency [18]. The resonant frequency altered from 15.5 GHz to 10.7 GHz by switching two RF MEMS switches from 0 to 20 volts.

MEMS bridge switches are not the only MEMS device currently used as tuning devices. Cantilever switches were used in [19] to tune an interdigital coplanar filter with tapped line feeding. Their structure was able to tune from 21 GHz to 18.5 GHz by actuating cantilever switches typically at voltages between 60 to 70 V.

The goal of this thesis is to demonstrate that using a MEMS capacitive switch one can tune the filter response of a CPW filter.

This chapter has reviewed the advantages of using a coplanar waveguide medium as a transmission line and has discussed research that has concentrated on patterned structures that have been used to change the general characteristics of CPW lines.

A review of common micro electro mechanical systems systems were presented and several radio frequency MEMS applications have been discussed.

Chapter 3

Analysis of CPW filters with RF MEMS switches and design of a tunable filter

This thesis proposes to use a pre-existing filter topology and add a MEMS tuning element. Before starting to design the tuning element, a filtering structure must be selected, verified, and adapted for our desired frequency range and modified to be compatible with our fabrication facilities. Two MEMS switch topologies will be presented and equivalent circuits will be created. This will be followed by a complete tunable filter design.

3.1 Filter Modeling

As stated in chapter 2, CPW is selected as the transmission medium because the resulting uniplanar designs are compact, low loss and provide an accessible surface to mount any tuning devices.

Although there are several different studies that have shown promising uniplanar designs that act as filters, the type of filter that was ultimately selected is from Hettak

and Dib [20]. These simple filter structures are an ideal starting point because the types of discontinuities have been widely studied by several organizations, the filtering responses are well defined, and the layouts are easily modified to change the filtering response.

The types of filters described in [20] implement patterned traces in both the inner conductor (centre conductor line of the CPW), outer conductor (the ground planes of the CPW) or both. A variety of Ka-band filters and their dimensions are shown in Figure 3.1 while the corresponding performance curves are shown in 3.2.

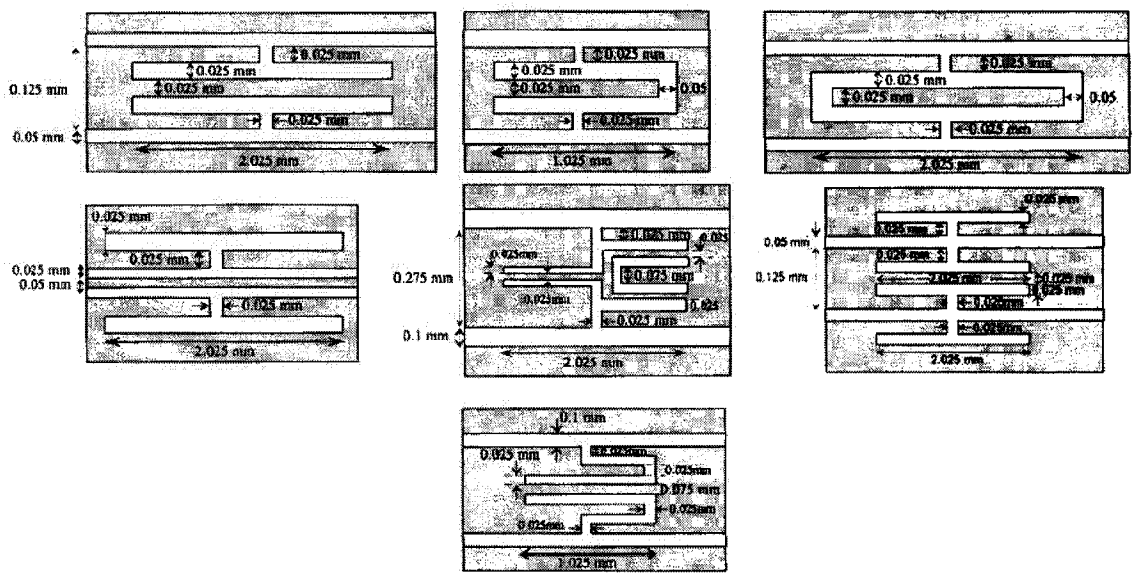

Figure 3.1: Dimensions of CPW filters, Hettak [20]

The CPW lines's interdigitated conductors and gaps create equivalent capacitive and inductive effects that can be controlled to produce filtering characteristics.

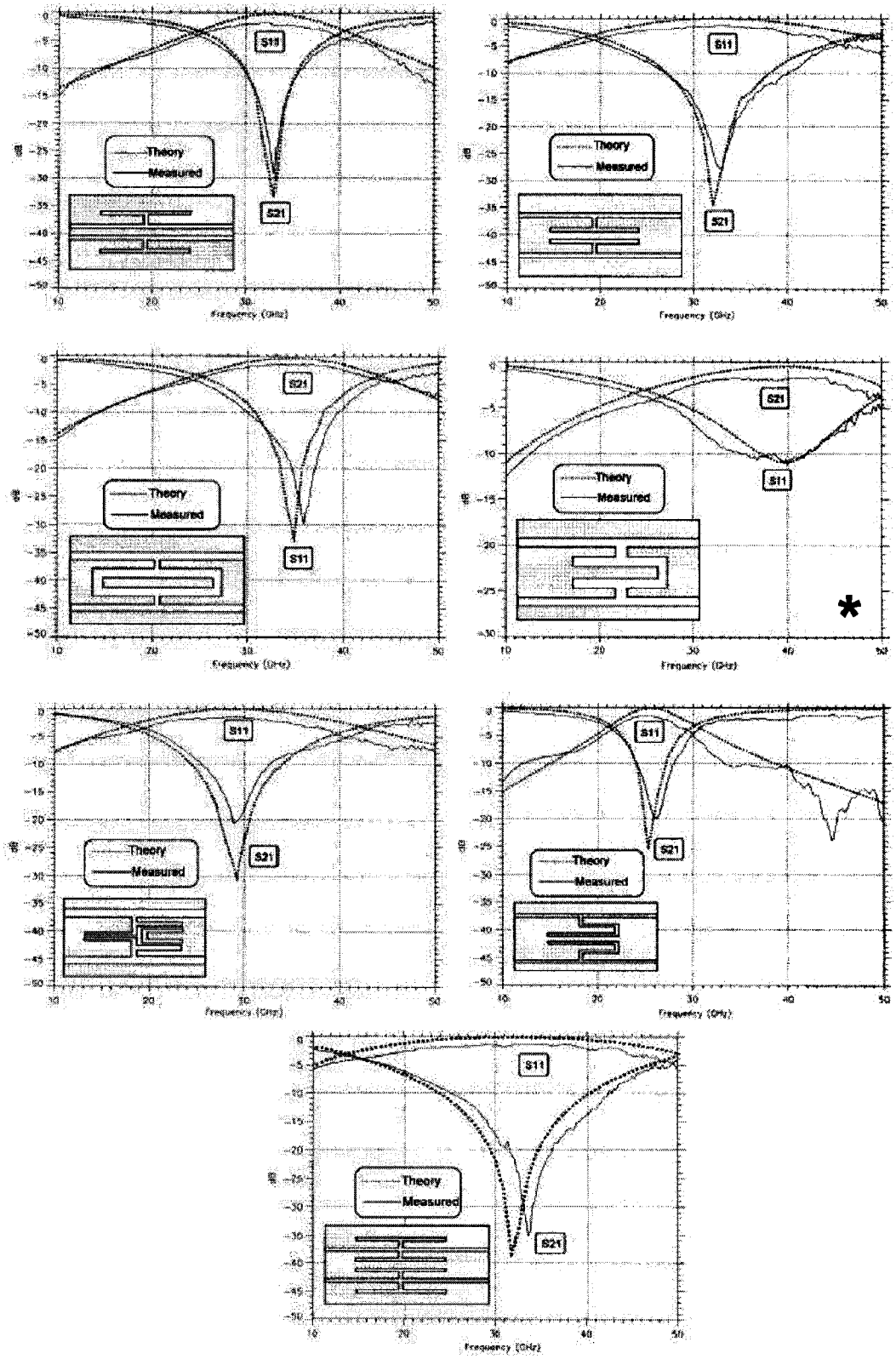

Figure 3.2: Experimental and theoretical results for structures shown in Figure 3.1, Hettak 1998 [20] (* denotes selected structure for this work)

For this thesis, it was decided to focus on filters that have patterned traces in the inner conductor only as these are well suited to MEMS bridge tuning. Several of the CPW layouts were examined and one primary structure, that of 3.3 was selected. A simplified equivalent circuit of the structure has been presented as an inductor in series with a capacitor.

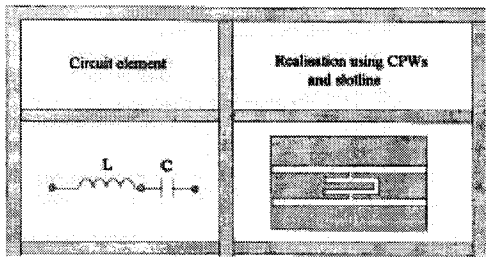

Figure 3.3: Selected structure, Hettak [20]

This design is selected over the other possibilities because its filtering action provides a pass band response instead of a stop band response and its dimensions are the smallest.

For verification the patterned coplanar lines are recreated using Ansoft HFSS EM simulation tool. HFSS is chosen since it offers the capability of analyzing the final 3D structure proposed in this work. Figure 3.4 and 3.5 show the 3D circuit representation employed using the provided dimensions and layout of Figure 3.3.

The simulated results are presented in Smith chart format and magnitude format in Figure 3.6 and Figure 3.7 respectively.

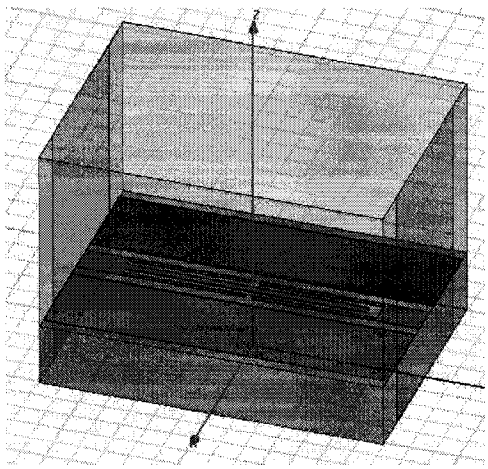

Figure 3.4: Angle view of HFSS simulation layout

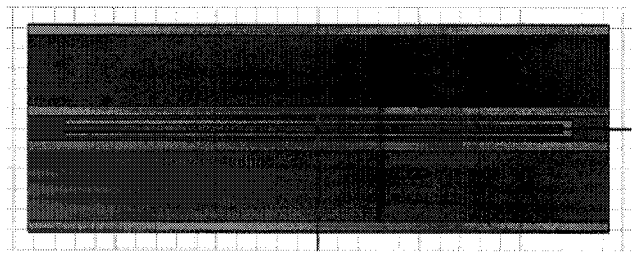

Figure 3.5: Top view of HFSS simulation layout

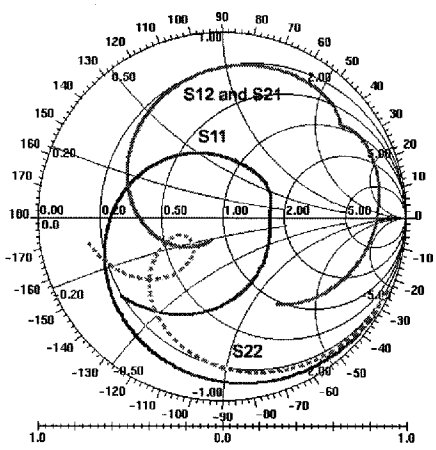

Figure 3.6: HFSS simulated results for gold CPW lines of length 1025 μm - Smith chart plot

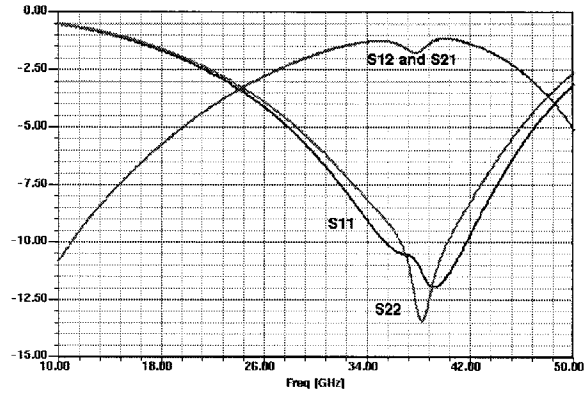

Figure 3.7: HFSS simulated results for gold CPW lines of length 1025 μm - magnitude plot

As can be seen, the simulated and published results are well correlated with a centre frequency of 40 GHz and a maximum input return loss of approximately 12 dB. Given that the simulator yields acceptable results, the next step is to alter the filter layout to accommodate our purposes.

The initial changes to be considered are those which facilitate the fabrication process of the filter in the Carleton University micro fabrication laboratory.

In [20] the metal deposition for the patterned coplanar lines was done in 3 μm

gold. Such a metal thickness and material is usually chosen to minimize the losses that occur along the CPW line. In our case, the metal thickness is decreased to 1 μm and the conductor material is changed to aluminum instead of gold. Both changes have the effect of increasing the loss of the line, but the losses are found to be acceptable given that the fabrication process would be greatly simplified. Another reason for reducing the line thickness is related to the tuning method that will be proposed in section 3.2.

Further considerations are made to change the cross sectional dimensions of the centre conductor line and the gaps on either side. These dimensions determine the characteristic impedance of the waveguide. If the uniform section of the centre conductor is not found to be 50 Ω the layout must be changed appropriately. Assuming that the ground planes and the dielectric widths are infinite, and knowing that the substrate has a thickness of approximately 300 μm, the following equations can be used [21]:

$$Z_0 = \frac{30\pi}{\sqrt{\varepsilon_{re}}} \frac{K(k')}{K(k)} \tag{3.1}$$

$$\varepsilon_{re} = 1 + \frac{(\varepsilon_r - 1)}{2} \frac{K(k')}{K(k)} \frac{K(k_1)}{K(k_1')} \tag{3.2}$$

$$k = \frac{a}{b} \tag{3.3}$$

$$k' = \sqrt{1 - k^2} \tag{3.4}$$

$$k_1 = \frac{sinh\left(\frac{a\pi}{2h}\right)}{sinh\left(\frac{b\pi}{2h}\right)} \tag{3.5}$$

$$k_1' = \sqrt{1 - k_1^2} \tag{3.6}$$

where:

- Z_0 is the characteristic impedance of the line
- ε_r is the permittivity of the substrate,

- ε_{re} is the effective relative permittivity of the substrate,
- K is the complete elliptical integral of the first kind,
- a is half the width of the centre conductor
- b is the gap width plus half the width of the centre conductor
- h is the height of the substrate

However, the $\frac{K(k')}{K(k)}$ can be approximated by:

$$\frac{K(k)}{K(k')} = \frac{ln\left(2\frac{1+\sqrt{k}}{1-\sqrt{k}}\right)}{\pi} when 0 \leqq k^2 \leqq 0.5 \tag{3.7}$$

$$\frac{K(k)}{K(k')} = \frac{\pi}{ln\left(2\frac{1+\sqrt{k}}{1-\sqrt{k}}\right)} when 0.5 \leqq k^2 \leqq 1 \tag{3.8}$$

Solving equations for 3.2 to 3.8 given a=62.5, b=112.5, h=300, ε_r=9.4 for alumina gives:

Table 3.1: Calculated parameters for the characteristic line impedance of the CPW line

Component name	Value
k	0.5556
k'	0.8315
k_1	0.5341
k_1'	0.8454
$\frac{K(k')}{K(k)}$	1.2
$\frac{K(k_1)}{K(k_1')}$	0.813
ε_r	5.10
Z_0	50.1

Considering how close the calculated line impedance is to 50 Ω, the centre conductor width and the gaps do not need to be changed.

Another change that must be implemented is to shift the filtering response. The filtering effect of the chosen filter occurs at approximately 40 GHz. It is preferred

to have the filtering response between 20 and 30 GHz to show that the design can easily be modified to target specific starting frequencies and to have a response in a range that would be easier to measure with the available equipment. HFSS is used to model the effects of altering the CPW filter. In order to lower the frequency, the patterned conductor length is elongated to 2500 μm from the initial 1025 μm length. The remaining filter dimensions are left unchanged.

With the proposed changes in materials, thickness, and trace length, only the alumina substrate material remains the same from the original design. An HFSS circuit is constructed and the results presented in Figures 3.8 and 3.9 are obtained:

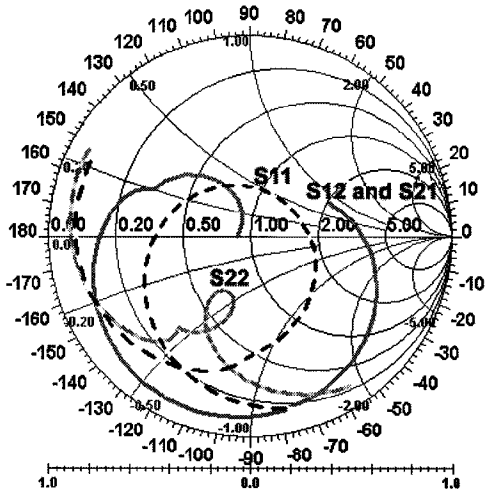

Figure 3.8: HFSS Smith chart plot simulated results for aluminum CPW lines of length 2500 μm

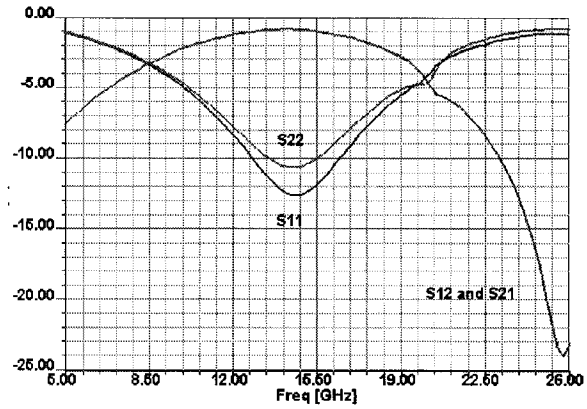

Figure 3.9: HFSS magnitude plot simulated results for aluminum CPW lines of length 2500 μm

The simulation demonstrates a decrease in centre frequency of the filter's pass band to approximately 14 GHz. The increase in losses of approximately 0.75 dB due to the decrease of metal thickness and change of metal material are found to be acceptable. A transmission notch at 25.5 GHz is also apparent.

The design was fabricated to ensure that the simulated values are accurate and the results are shown in Figure 3.10 and Figure 3.11.

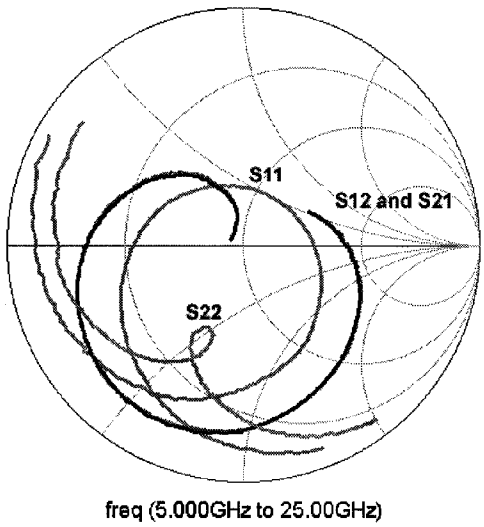

Figure 3.10: Measured S-parameter Smith chart plot for 1 μm thickness aluminum CPW lines of length 2500 μm

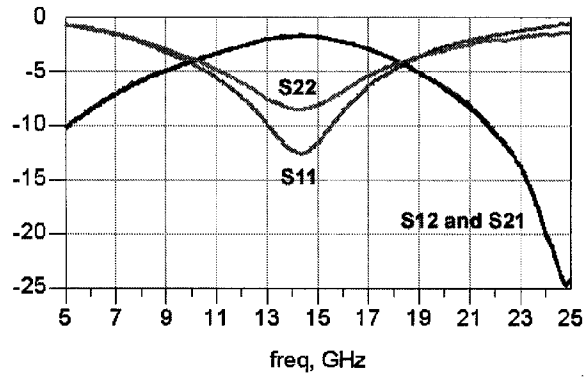

Figure 3.11: Measured S-parameter magnitude plot for 1 μm thickness aluminum CPW lines of length 2500 μm

As can be seen, the filtering response of the fabricated device is closely correlated to the HFSS simulations. The S_{12} minimum is at 24.5 GHz at -25 dB and the S_{11} minimum is at 14 GHz at -12.5 dB. This was deemed to be sufficiently close to the prediction to accept the HFSS simulation as accurate.

Based on the new filter layout a lumped equivalent circuit of the design can now be pursued. This is necessary as the equivalent L-C circuit shown in Figure 3.3 is only a first order expression of the circuit behavior. The lumped equivalent circuit would be used to determine what elements and values are needed to properly tune the filtering response in a desired manner. In order to create a lumped equivalent circuit of the design [4] and [12] are referenced. The two papers have equivalent circuits for short ended and open ended coplanar waveguide series stubs as shown in Figures 3.12 to 3.15. These two stub configurations are employed together to for the selected filter of Figure 3.3.

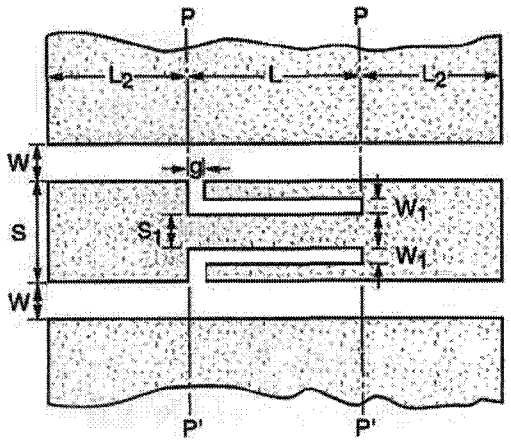

Figure 3.12: Short end coplanar waveguide series stub layout proposed by [12] taken from [4]

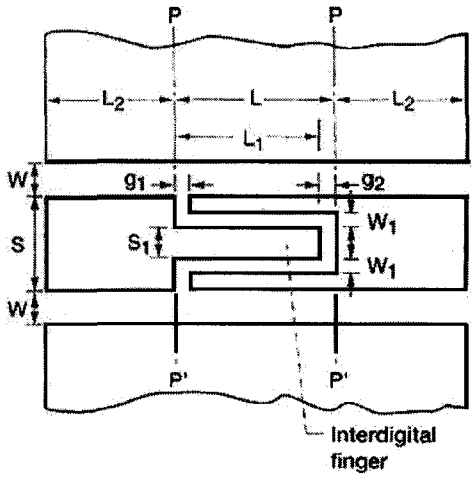

Figure 3.13: Open end coplanar waveguide series stub layout proposed by [12] taken from [4]

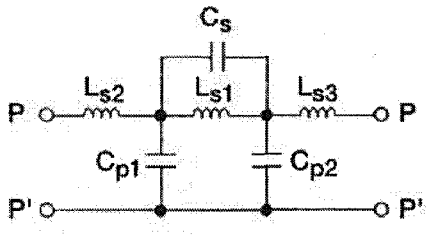

Figure 3.14: Short end coplanar waveguide series stub equivalent circuit proposed by [12] taken from [4]

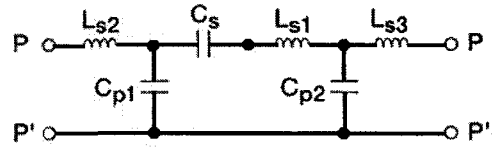

Figure 3.15: Open end coplanar waveguide series stub equivalent circuit proposed by [12] taken from [4]

Unfortunately, the presented equivalent circuits are stated to be strictly valid for specific dimensions that are not the same as in the selected design. Furthermore, since the desired design is a series combination of both the open ended and the short ended coplanar waveguide series stubs, no equivalent circuit exists for the entire structure.

Using nonetheless their equivalent circuit as a starting point along with the simulation results provided by HFSS, the equivalent circuit shown in Figure 3.16 was derived. It is simulated using Agilent Technologies Advanced Design System (ADS). The equations for the capacitance and inductor values per unit length given in [4] provide a starting point for selecting the order of magnitude of the components. Modifications to the parameters are subsequently done to approximate the simulated

results. The values are presented in Table 3.2.

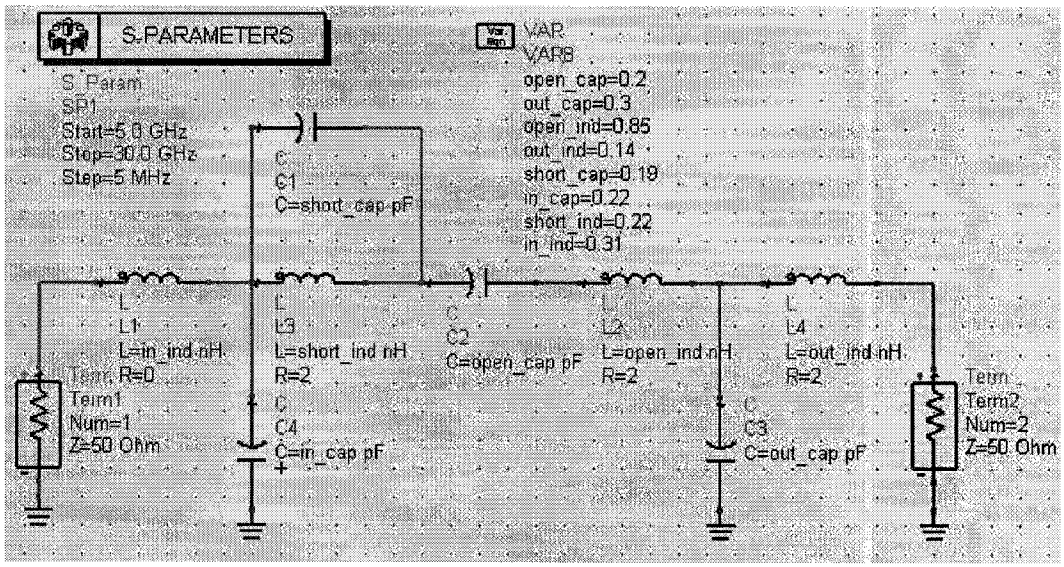

Figure 3.16: Equivalent circuit of filters in ADS

Table 3.2: Equivalent circuit components and values for chosen CPW filter

Component name	Component label	Value	Associated resistance
Input inductor	in_ind	0.31 nH	0 Ω
Input capacitor	in_cap	0.22 pF	-
Short inductor	short_ind	0.22 nH	2 Ω
Short capacitor	short_cap	0.19 pF	-
Open inductor	open_ind	0.85 nH	2 Ω
Open capacitor	open_cap	0.20 pF	-
Output inductor	out_ind	0.14 nH	2 Ω
Output capacitor	out_cap	0.30 pF	-

The simulation results of the lumped equivalent circuit from ADS are shown in Figure 3.17 and Figure 3.18.

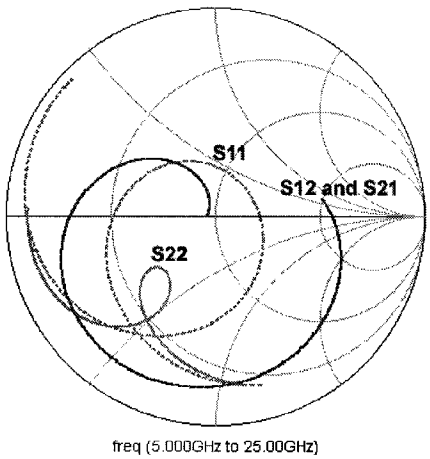

Figure 3.17: ADS equivalent circuit simulation result - Smith chart plot

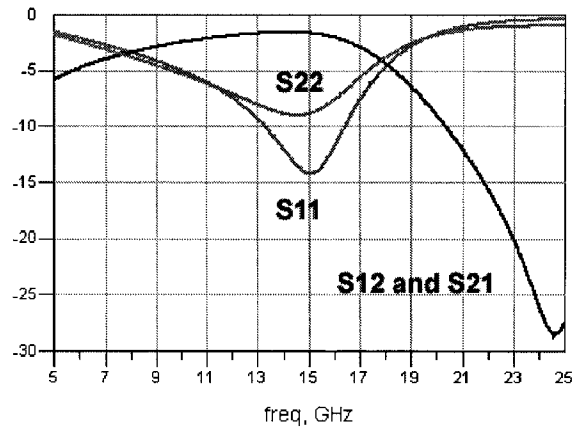

Figure 3.18: ADS equivalent circuit simulation result - magnitude plot

For comparison purposes the simulated HFSS results are shown again in Figures 3.19 and Figure 3.20. It can be seen that above 9 GHz agreement of the S_{12} parameter is within 1 dB.

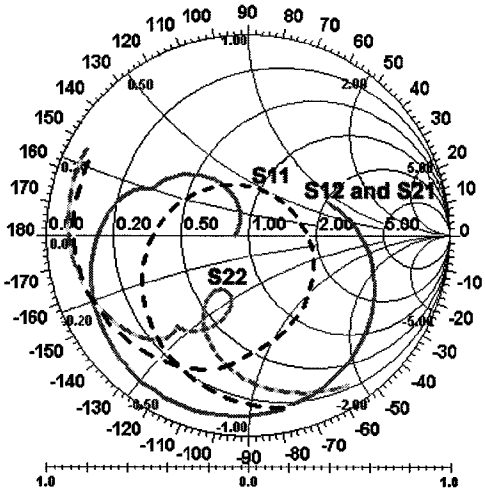

Figure 3.19: HFSS simulation result - Smith chart plot

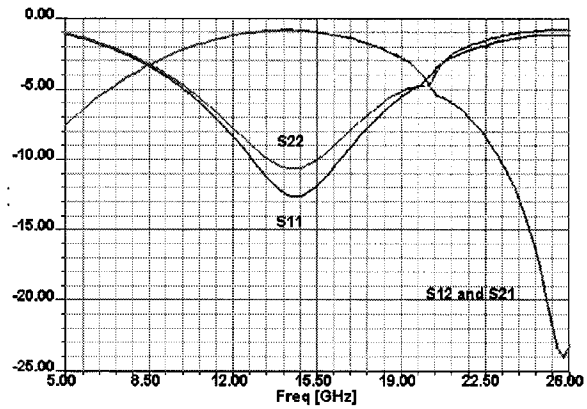

Figure 3.20: HFSS simulation result - magnitude plot

Given that the equivalent circuit plots are very close to the simulated plots, and realizing that designing a more exact equivalent circuit for the layout would be a

complete study in itself, the equivalent circuit of Figure 3.16 is accepted to be accurate enough for use in the tunable filter design.

3.2 Switch modeling

With the basic filter verified, modified and modeled, the next step is to incorporate a tuning capability. In order to tune the CPW filter, a micro electro mechanical systems (MEMS) switch such as the one shown in Figure 3.21 is proposed.

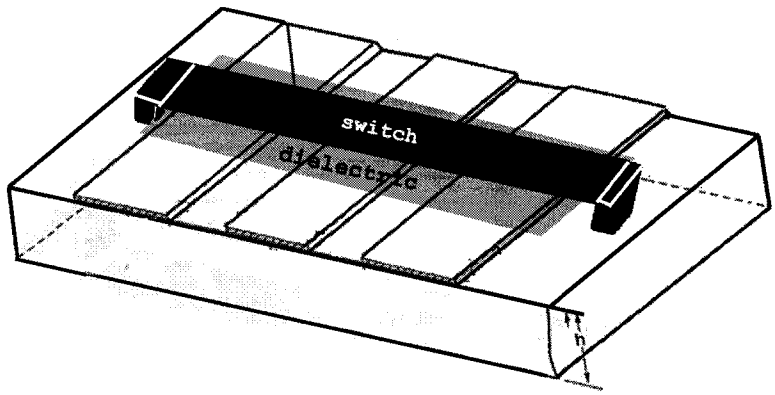

Figure 3.21: Schematic of a coplanar waveguide with switch

3.2.1 Switch design considerations

The bridge can be viewed as a shunt loading of the CPW line. The equivalent circuit of the loading consists of a series capacitor, inductor and resistor [16]. The bridge changes form during actuation and has different properties. It is these properties that will be used to alter the signal transmission along the underlying coplanar line. For the selected bridge structure the capacitance change is expected to cause the most dominant loading effect on the conduction line that passes underneath it. Therefore, the following analysis will concentrate on capacitive effects of the switch in both the actuated (bridge down) and non-actuated (bridge up) states. Note that the underlying CPW lines are now coated with a thin dielectric layer in order to prevent DC shorting of the bridge and CPW conductor in the down state.

Up state capacitance

As a first approximation, a basic parallel plate capacitor model with multiple dielectric materials can be used to approximate the capacitance of the switch. Assuming that the dielectric layer used to separate the centre conductor and the bridge in the down state is small in comparison to the air space between the dielectric the following model can be used: [16]

$$C_{pp} = \frac{\varepsilon_0 A}{g + t_d} \tag{3.9}$$

where:

- C_{pp} is the parallel plate capacitance,
- ε_0 is the permittivity of free space,
- g is the nominal gap height of the bridge,
- t_d is the finite thickness of the dielectric,
- A is the area of the two plates

If the dielectric thickness is the same order of magnitude as the gap height, then the permittivity of the dielectric becomes more important. The equation then becomes: [16]

$$C_{pp} = \frac{\varepsilon_0 A}{g + t_d/\varepsilon_r} \tag{3.10}$$

where:

- ε_r is the relative permittivity of the dielectric material

The fringing field capacitance of the MEMS switches, C_f, is a large portion of the capacitance that is not taken into account in equations 3.9 and 3.10. For this reason, simulation software is generally used to account for this missing contribution which can be up to 50% [16] of the total capacitance.

Up to this point we have assumed that the bridge metal is solid. In general, in order to fabricate MEMS switches, holes must be inserted into the bridge membrane to allow etchants to dissolve the sacrificial layer underneath the bridge, reducing the amount of time needed to dissolve the sacrificial layer that will support the bridge during fabrication. Holes also help to increase the speed at which the bridge can actuate by allowing air or other gases to pass through the holes as the bridge actuates. The dimensions of the holes in this study are selected to be 10 μm in diameter with a separation of 10 μm between each other. This diameter and spacing combination is selected due to previous work in the Carleton University micro fabrication laboratory environment by Rose [22].

It was found, that given the types of etchants available and the material typically used for the sacrificial layer, this combination provides the most reliable releasing results. Unfortunately, a typical rule of thumb is that if the diameter of the hole is larger than twice the cantilever bridge height, then the fringing fields will have an effect on the capacitance. Therefore, in this case only a rough estimate of the capacitance can be obtained and a final capacitance value will be found when the fabrication is completed. However the estimate should give the order of magnitude that is expected, which is a good starting point.

Down state capacitance

When the switch is actuated and the bridge is in the down state, the capacitance can be calculated using the parallel plate capacitance assumption: [16]

$$C_{pp} = \frac{\varepsilon_0 \varepsilon_r A}{t_d} \tag{3.11}$$

The fringing fields can be neglected because the dielectric thickness is considered

to be very small.

Dielectric thickness

There are several important factors to consider when selecting a dielectric layer thickness. The consideration is that the thinner the dielectric layer is made, the higher the capacitance that can be obtained in the down state. In order to see a substantial change in filtering response, it is expected that a large capacitance change will be required. Unfortunately, there are two problems with making the dielectric very thin and thus a large capacitance change possible.

First, it becomes increasingly difficult to evenly deposit dielectric at smaller thicknesses. If pin holes develop in the dielectric material, the bridge may create an electrical short to the layer below. Also, the evaporated deposition might be rough in certain places, giving an uneven height when the bridge actuates. Given that small changes in the bridge separation with respect to the metal underneath give large changes in capacitance, the desired value of capacitance might not be achieved reliably. Furthermore, it is very difficult to measure the thickness after the fabrication is completed since thicknesses are generally measured by the apparatus used in depositing the material. Other measuring apparatus may damage the dielectric or the switch when measuring the dielectric thickness.

Second, the dielectric must be able to withstand the actuation voltage that will be across it. If the dielectric is too thin, the dielectric will break down. Therefore, the dielectric must be made thick enough to withstand the maximum voltage that will be put across it. This leads to considering the actuation voltages when determining the dielectric thickness.

Actuation voltage calculation

In order to actuate the switch there must be a DC bias differential that would cause the bridge to actuate. This can be accomplished in two ways.

First, the MEMS bridge is grounded and connected to the ground planes and thus has no DC voltage. The DC bias differential between the grounded bridge and the CPW centre line will cause the bridge to actuate and come down. The advantage of this method is that the bridge requires no connection and it will not build up a residual charge because it is connected to the ground planes. Unfortunately, this also means that the biasing must be done to the centre conductor signal. Goldsmith, et al. have a created a similar switch which is depicted in Figures 3.22 and 3.23 [23].

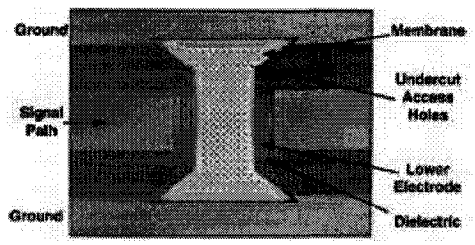

Figure 3.22: Top view of RF MEMS capacitive switch design proposed by [23]

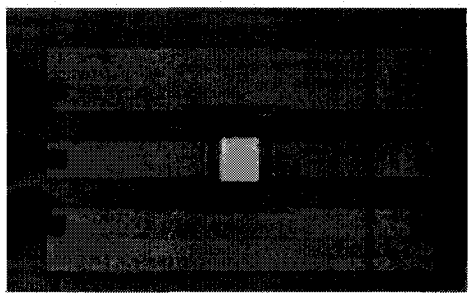

Figure 3.23: Micrograph of RF MEMS capacitive switch [23]

The second method is to separate the bridge from the ground planes and to assign separate biasing to the MEMS bridge. The differential between the bridge and the ground planes will create the pull down force needed to actuate the bridge. This requires an additional biasing line for each bridge but it allows the signal to pass through the conduction line without any additional connections. Furthermore, it allows for individual bridges to be actuated independently. It should be noted that there is very little power loss from biasing the bridge because it is separated from the centre conductor by the dielectric. The dielectric ensures that there is no conduction

path for the bridge to discharge and therefore, the only power loss will be through leakage current. This latter design method is selected because designing a single unaltered feed is preferred, and biasing bridges independently would be required if more then one bridge would be used.

In order to calculate the amount of voltage that will be needed to pull down the bridge, the dimensions of the bridge and the mechanical forces must be examined.

The pull down voltage that is needed to actuate the bridge can be expressed as:[16]

$$V_p = \sqrt{\frac{8kg_o^3}{27\varepsilon_0 A}} \tag{3.12}$$

where:

- V_p is the pull down voltage needed,
- k is the effective spring constant of the membrane,
- g_o is the nominal height of the bridge,
- ε_0 is the permittivity of free space,
- A is the area which the bridge creates a parallel plate capacitance over the ground planes

The effective spring constant k can be represented by:[16]

$$k = \frac{32Et^3w}{L_m^3} + \frac{8\sigma(1-v)tw}{L_m} \tag{3.13}$$

where:

- k is the effective spring constant of the membrane,
- E is Youngs modulus of the membrane material,

- t is the membrane thickness,
- σ is the residual tensile strength of the membrane,
- v is Poisson's ratio for the membrane material,
- w is the membrane width,
- L_m is the length of the membrane.

Although it is desirable to try to minimize the pull down voltage of the bridge, one must consider how the bridge will be released back to its unactuated state after the DC bias is removed.

Stiction

One of the forces that prevent the bridge from restoring itself is that of stiction. As a general definition, stiction is the unintentional adhesion of surfaces. Stiction problems can occur at the fabrication stage or while the MEMS device is in use.

During the fabrication stage, liquids can be trapped in between surfaces. This will be discussed further in the fabrications chapter.

The second manner in which stiction can occur for the proposed device is during use. Wherever there are moving components, when two surfaces come into contact, there are electrostatic forces and Van Der Waals forces that attract the surfaces together. Electrostatic forces are generally a result of attractive forces that occur due to trapped electric charges. Van Der Waals forces deal with the inter-molecular forces. Once Van Der Waals and electrostatic forces overcome the restoring force, the bridge will be stuck in the down position. It can no longer be moved and the bridge cannot be released from its actuated state.

If the pull down voltage is low, there is a higher risk that the Van Der Waals forces will prevent the bridge from restoring itself after the DC supply is removed. It was decided that a target voltage should be between 10-15 volts for the bridge to be actuated.

3.2.2 Calculating switch parameters

Bridge dimensions

Given all the considerations above, the MEMS switch design in Figure 3.24 was implemented.

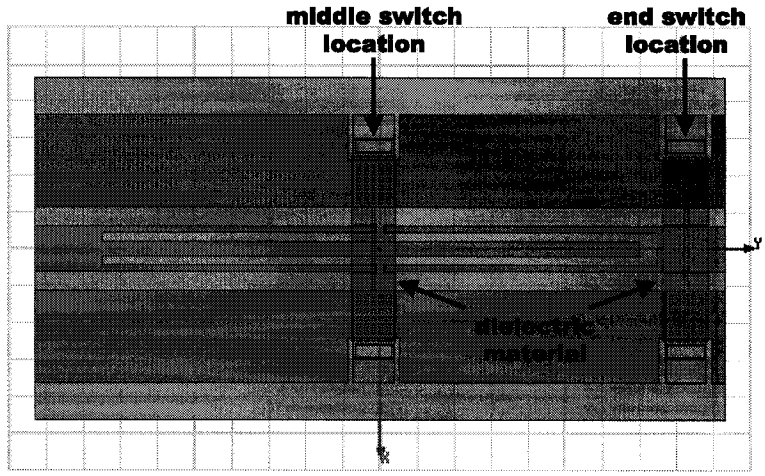

Figure 3.24: Top view of MEMS switches and proposed locations

In order to incorporate a switch with the CPW filter structure, there are two locations to consider, shown in Figure 3.24. The first location is after the CPW filter and has a uniform centre conductor line underneath it. The second location is at the middle of the filter where the short and the open components meet. Here the bridge is over the patterned centre conductor.

The dielectric material was selected to be SiO_2. The bridge was fabricated out of

1 μm aluminum. The length of the bridge is 450μm. The width of the bridge is 110 μm over the ground planes and 10 μm over the CPW centre line and CPW gaps. The area of the switch is approximately $1.25 * 10^{-9} m^2$ over the centre conductor line. The height of the bridge in the non-actuated state was set to 1.5 μm above the dielectric layer.

As the bridge actuates, the capacitance gradually increases until the bridge makes contact with the dielectric separation layer. The following graph shows the gradual change in capacitance as the bridge actuates for different dielectric thicknesses using the equations 3.9 to 3.13:

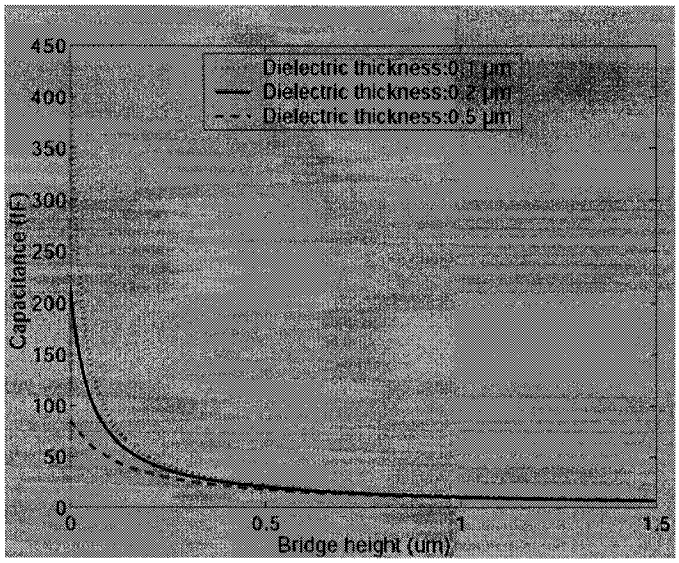

Figure 3.25: Calculated capacitance versus bridge height for various dielectric thicknesses (uniform centre conduction section)

The target dielectric thickness was 0.2 μm. For a uniform centre conductor line a maximum capacitance is expected to be 216 fF when the switch is down and a minimum capacitance of 7 fF when the switch is up.

The code to generate the plots can be found in Appendix A - Capacitance calculations.

For the patterned conductor line, the maximum capacitance is expected to be 129

fF when the switch is down and a minimum capacitance of 4 fF when the switch is up. The graph is shown below in Figure 3.26.

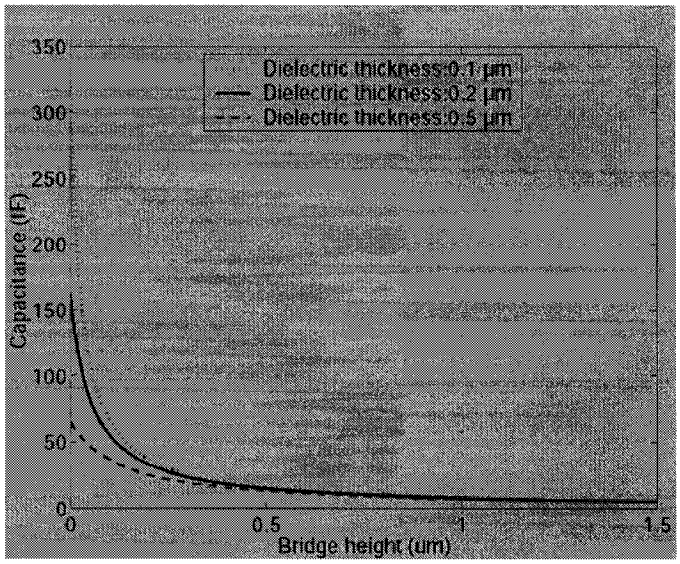

Figure 3.26: Calculated capacitance versus bridge height for various dielectric thicknesses (patterned centre conduction section)

It should be noted that for our application, the switch will alter between two capacitance values. Continuous control over the full range of the capacitance value is not obtainable as the bridge will pull down at voltage Vp 3.12.

Bridge locations

As stated earlier, the bridges are placed at the middle and at the end of the filter. These locations are chosen because it is believed that equivalent circuits of the switches could easily be added to the specific nodes of the lumped element filter circuit. The end switch equivalent circuit could be inserted at the output matching network because it will load the output impedance. The middle switch equivalent circuit could be added in between the open and short stub circuit elements because it is located at the junction of the two stubs. The proposed locations are shown in Figure 3.27:

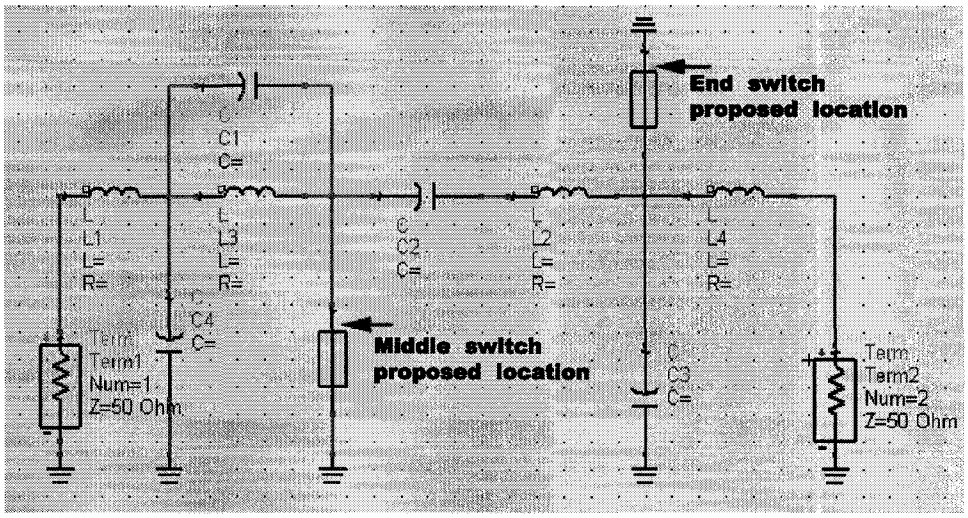

Figure 3.27: Equivalent circuit with proposed switch locations shown

Although the switches have been modeled with the capacitor equations above, simple capacitance does not fully express the entire effect that the switch will have over the CPW line. Furthermore the switch that is located in the centre of the device has a much smaller overlap with the centre conductor line and the patterning may have different effect on how the switch will react. In order to get a complete equivalent circuit for the switch, it is necessary to simulate or fabricate the switch in an isolated manner to extract its equivalent circuit.

Figures 3.28 and 3.29 show two isolated switches, one above a uniform section of CPW line and one above a patterned section of CPW line.

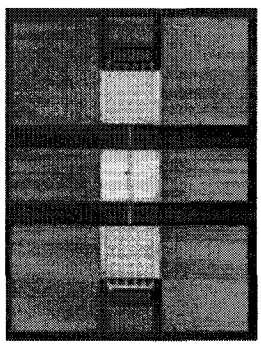

Figure 3.28: Fabricated test structure of end bridge above uniform line

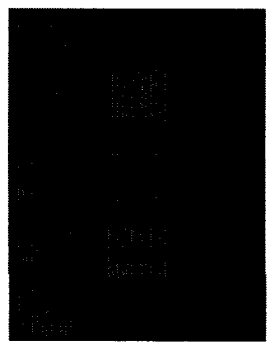

Figure 3.29: Fabricated test structure of middle bridge above patterned line

In order to avoid any discrepancy between simulation and actual conditions, fabricated test structures are employed for the modeling exercise.

The test structures are fabricated in the Carleton University micro fabrication laboratory. Test structures were constructed both with and without the air gap in between the bridge and the dielectric layer. Measurement of both test structures would give the maximum capacitance change between the switches in the up and down positions. Using the test structures with the air gap, the actuation voltage of the switches were found to be between 11.2 and 13.5 volts. In addition to the switch test structures, a bare 50 Ω line CPW line was also fabricated for characterization as shown in Figure 3.30.

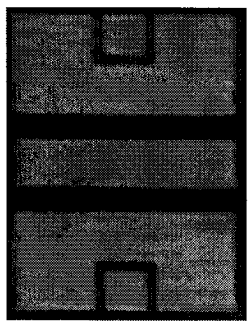

Figure 3.30: Test structure - 50 Ω line

Measured 50 Ω line S-parameters were used to extract the effect that the CPW access lines will have on the behavior of the bridge structure. By removing the phase shifts of the 50 Ω lines from both sides of the switches, one can determine the effect that an isolated bridge structure should have. This de-embedding operation is carried out with the ADS software tool.

The 50 Ω test structure has the same dimensions as the filter CPW lines. Its length is 200 μm corresponding to the line length on each side of the switch.

Measurements for the 50 Ω line test structure are shown in Figures 3.31 and 3.32.

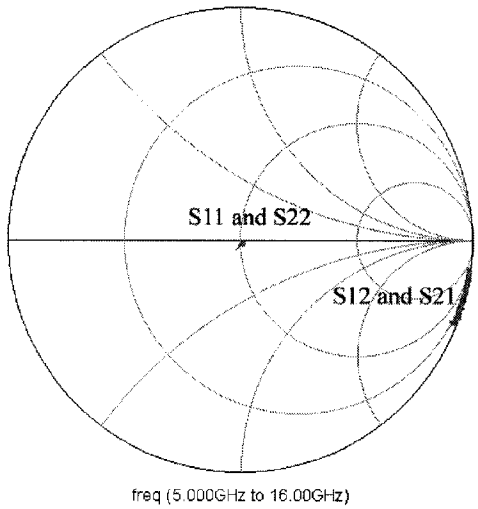

Figure 3.31: Test structure - 50 Ω line measurements - Smith chart plot

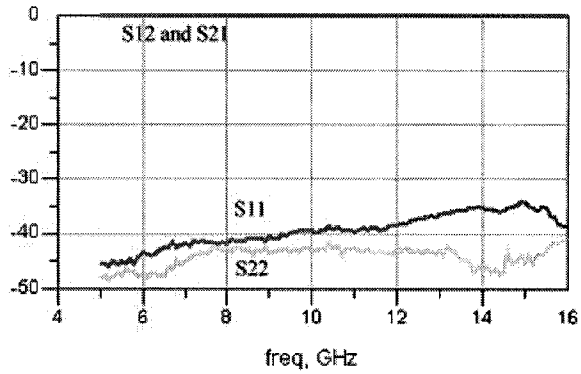

Figure 3.32: Test structure - 50 Ω line measurements - magnitude plot

As can be seen, the measured S-parameters are found to be very close to the desired 50 Ω line behavior that was predicted by the calculations performed in filter modeling.

A 50 Ω line segment is simulated in ADS using TLIN waveguide elements to give results as close as possible in magnitude and phase to the measured 50 Ω line test structure 3.30. The measured 50 Ω line results are shown in Figures 3.33 and 3.34 and the simulated ADS results are shown in Figures 3.35 and 3.36.

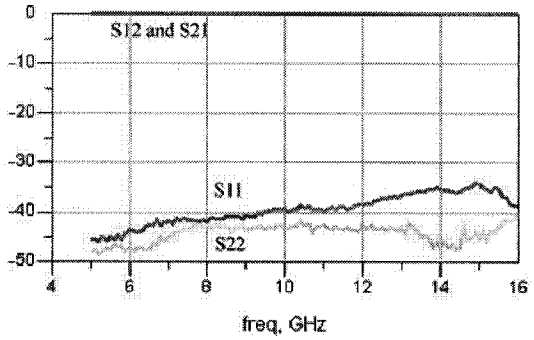

Figure 3.33: Test structure - 50 Ω line measurements - magnitude plot

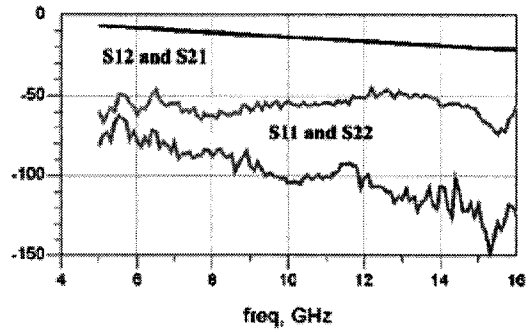

Figure 3.34: Test structure - 50 Ω line measurements - phase plot of S21

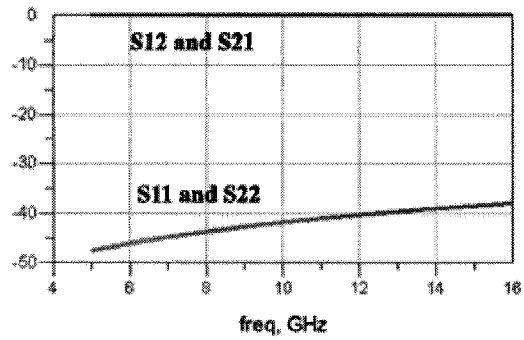

Figure 3.35: Simulated 50 Ω line in ADS - magnitude plot

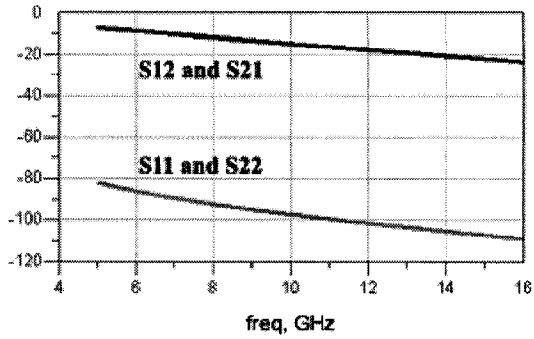

Figure 3.36: Simulated 50 Ω line in ADS - phase plot

Agreement between the fabricated and simulated values were found to be within 2 percent.

The simulated structure is then reduced in size to be 200 μm which is the size of the CPW transmission line on either side of the switch shown in Figure 3.30.

The accurately defined 200 μm TLIN element can now be used to de-embedded the measured switch results. In order do so the inverse of the tranfer matrix for the 200 μm CPW transmission line was multiplied before and after the switch in each position, thus providing a curve showing only the effects of the switch. De-embed block are used in ADS to calculate the inverse transfer matrix. The corresponding ADS circuit is shown in Figure 3.37.

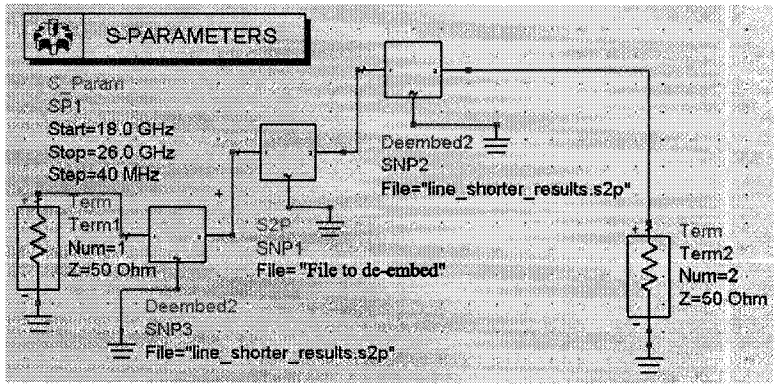

Figure 3.37: Switch - De-embedding operation in ADS

The de-embedding procedure is done for the end switch in both the actuated and non actuated states. The results obtained for the isolated switch having a uniform CPW line beneath it are presented in Figures 3.38 to 3.41:

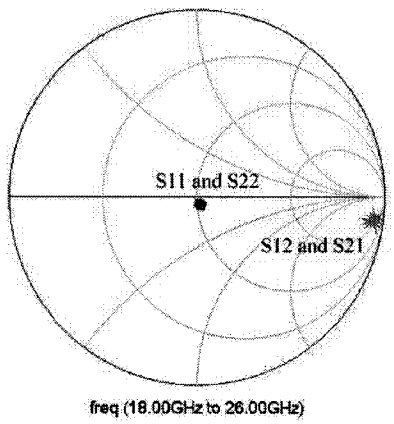

Figure 3.38: De-embedded S-parameters plot for the switch over the uniform CPW line (up position)

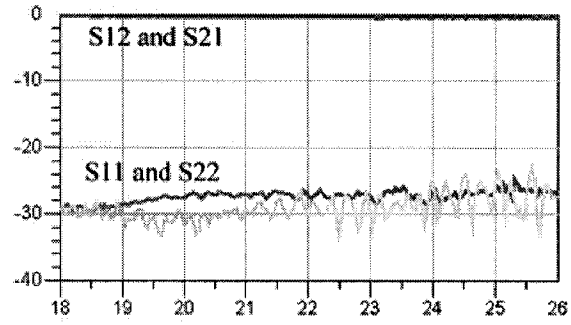

Figure 3.39: De-embedded magnitude plot for the switch over the uniform CPW line (up position)

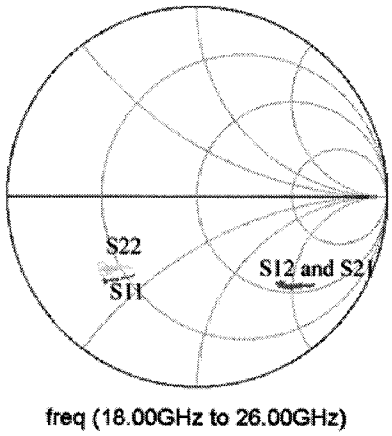

Figure 3.40: De-embedded S-parameter plot for the switch over the uniform CPW line (down position)

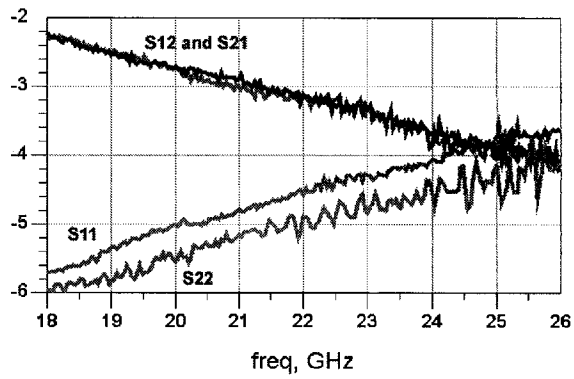

Figure 3.41: De-embedded magnitude plot for the switch over the uniform CPW line (down position)

It can be noted that the end switch in the up state causes very little obstruction to the line. For the end switch in the down state, there is a significant change in the signal response, which will be fully modeled in 3.2.3.

Unfortunately, the middle switch located over the patterned CPW line cannot be de-embedded in the same manner. This is because the filtering lines underneath the switch cause the line to have an impedance other than 50 Ω. As was mentioned in [20], the centre conductor patterning that is implemented in the test structure of Figure 3.29 would give an inductor as an equivalent circuit. Figures 3.42 to 3.45 show nonetheless the S-parameters for the patterned line.

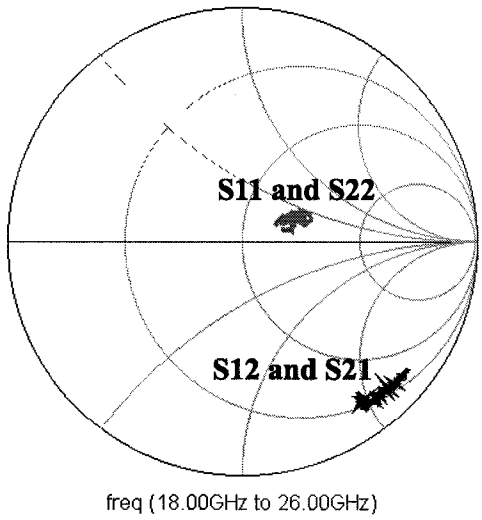

Figure 3.42: Embedded S-parameter plot for the switch over the patterned CPW line (up position)

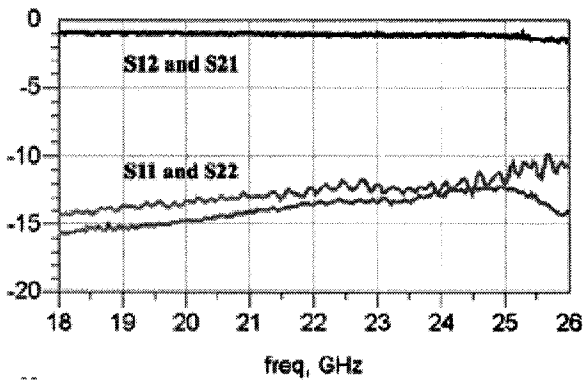

Figure 3.43: Embedded S-parameter magnitude plot for the switch over the patterned CPW line (up position)

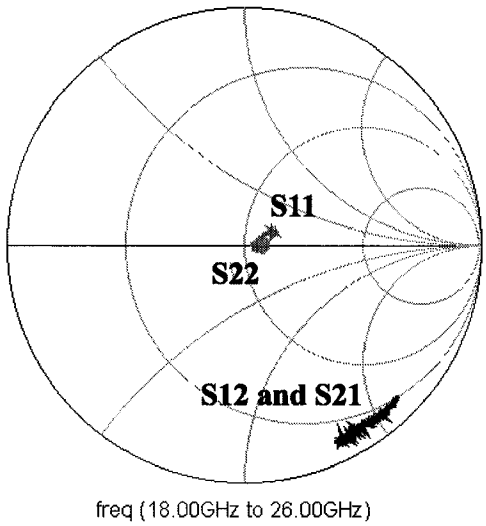

Figure 3.44: Embedded S-parameter plot for the switch over the patterned CPW line (down position)

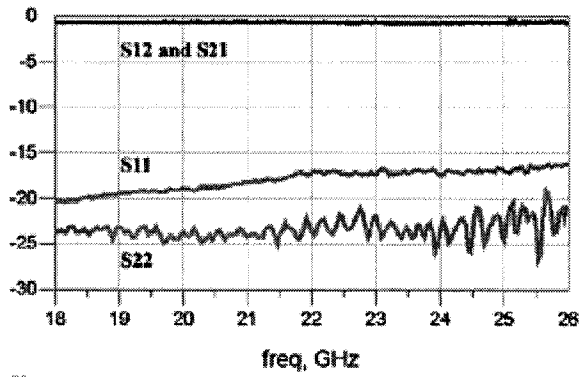

Figure 3.45: Embedded S-parameter magnitude plot for the switch over the patterned CPW line (down position)

Examining the plots of the middle switch in the up and down position, it can be seen that there is little noticeable change in the S-parameters in either case. This may indicate that the bridge did not properly couple with the conduction lines as expected for the test switch. Once the equivalent circuit is determined, the capacitance can then be compared with the expected value.

From the S-parameters obtained for the isolated test switches, the next step is to convert the results into an equivalent circuit.

3.2.3 Equivalent circuits and simulations

The switch over the uniform CPW line (middle switch) will be examined separately from the switch over the patterned CPW line (end switch).

End switch equivalent circuit

Since there is no noticeable change in response for the end switch in the up state and the bare CPW 50 Ω test line, only the down state equivalent circuit needs to be created. For the up state it is assumed that the line is unaffected by the switch.

From the Smith chart plot of the isolated switch in the down state, the impedance and admittance can be obtained as presented in Table 3.3.

Table 3.3: Impedance and admittance values for end switch in the down state.

	Frequency	Impedance		Admittance	
	(in GHz)	real	imaginary	real	imaginary
S_{11}	18	0.384	-0.428	1.162	1.295
	26	0.236	-0.315	1.245	1.929
S_{22}	18	0.386	-0.382	1.308	1.294
	26	0.263	-0.315	1.56	1.867

Ideally the S_{11} and S_{22} parameters would be overlapped since the test structure is symmetrical. It is assumed that a slight error in the calibration of the measuring apparatus causes the small S-parameter difference. The measurement technique and equipment is further discussed in chapter 5.

From the real and the imaginary parts of the admittance one can determine the equivalent circuit. From Muldavin and Rebeiz have determined that typical equivalent circuits for MEMS bridge structures can be expressed as an inductor, capacitor and resistor in series [24] and [25] as shown in Figure 3.46.

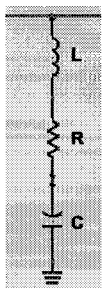

Figure 3.46: Equivalent circuit for switch over uniform CPW line

The inductance is generally found at the resonance. Since there is no resonance in the desired frequency range for this case, the inductance is assumed to be very small and is omitted. The following equations are used to determine the values of the equivalent capacitance and resistance.

$$\begin{aligned} Z_i &= \left(R + \frac{1}{jwC}\right) \parallel 50 = \left(\frac{jwCR+1}{jwC}\right) \parallel 50 = \left(\frac{wCR-j}{wC}\right) \parallel 50 \\ &= \left(\frac{wC}{wCR-j} + \frac{1}{50}\right)^{-1} \end{aligned} \tag{3.14}$$

$$\begin{aligned} Y = Z_i^{-1} &= \frac{wC}{wCR-j} + \frac{1}{50} \\ &= \frac{wC(wCR+j)}{(wCR-j)(wCR+j)} + \frac{1}{50} = \frac{w^2C^2R+jwC)}{(w^2C^2R^2-1)} + \frac{1}{50} \\ &= \left(\frac{w^2C^2R}{(w^2C^2R^2-1)} + \frac{1}{50}\right) + j\left(\frac{wC}{(w^2C^2R^2-1)}\right) \end{aligned} \tag{3.15}$$

Using the real and imaginary parts of (3.15) and solving for both the capacitance and resistance, the results given in Table 3.4 are obtained.

Table 3.4: Capacitance and resistance calculation from impedance and admittance values for switch in the down state.

	Frequency (in GHz)	Capacitance (in pF)	Resistance (in Ω)
S_{11}	18	0.232	4.76
	26	0.240	3.24
S_{22}	18	0.241	8.70
	26	0.249	7.36

Taking average values, the switch in the down state acts as a 240 fF capacitor in series with a 6 Ω resistor which is shunt loading the uniform CPW line.

Comparing the capacitance value found in the de-embedding technique of approximately 240 fF to the value of 216 fF obtained in Figure 3.25, agreement seems to be within 10%.

Using the calculated capacitance and resistance values, the equivalent circuit is simulated, as shown in Figure 3.47, to verify its response agrees with the measured response. The simulated plots are shown in Figures 3.48 and 3.49.

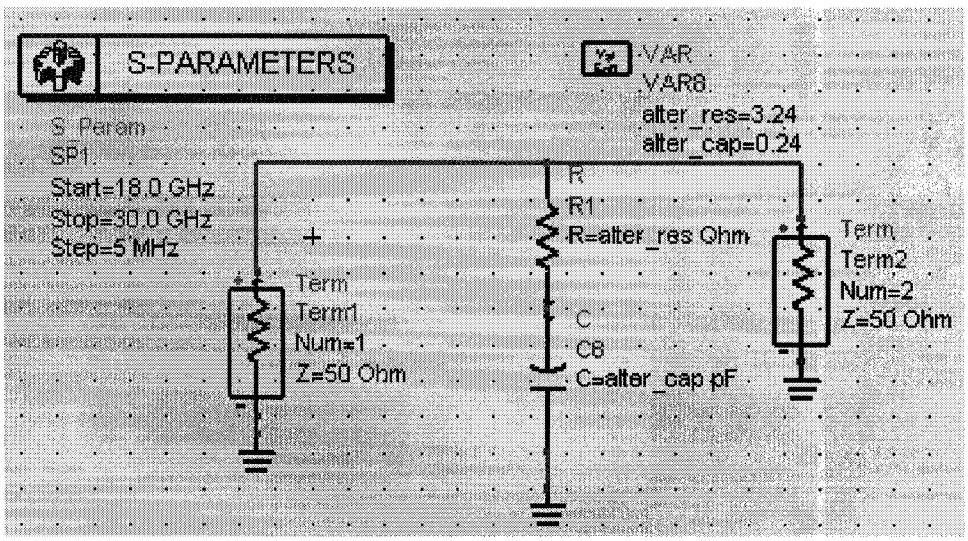

Figure 3.47: Equivalent circuit for the end switch in ADS

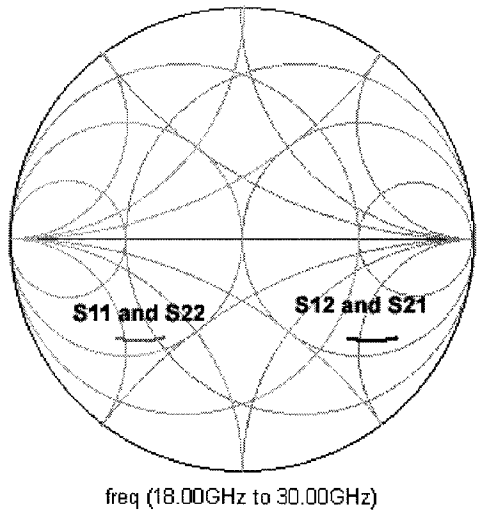

Figure 3.48: S-parameter of end switch from equivalent circuit (down position)

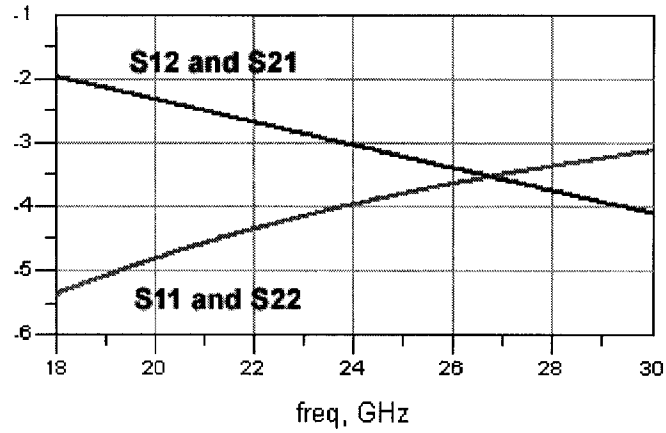

Figure 3.49: Magnitude of S-parameter of end switch from equivalent circuit (down position)

Comparing with the measured results of Figure 3.41, agreement is seen to be excellent. Therefore, the capacitance and resistance values are accepted.

Middle switch equivalent circuit

The middle switch test structures could not be de-embedded due to the fact that there is a patterned centre conductor. The patterning gives a different line impedance than is seen in the uniform line case and therefore, the 50 Ω line cannot be used to de-embed the coplanar access line's effect from the switch. In order to understand the effects of the patterned line, the following steps are followed.

The first step is to assume that the switch in the up position will have little effect on the conduction line, as we have seen is true for the switch over the solid conduction line. With this assumption, it is assumed that the response shown from the measured results of the switch in the up position will be primarily the effect of the patterned CPW line. If the change from the middle bridge up measurements and the middle bridge down measurements can be determined, this change can be attributed to the

switch.

Creating the equivalent circuit for the middle switch up results requires a little knowledge of the effect that the traced conduction line has on the signal transmission path. The layout of the patterned line test switch is the same as the layout for the uniform line test switch, except for the pattern in the centre conductor. From [20] it can be noted that the pattern in the centre conductor has an inductive effect on the signal transmission. The length, thickness, and width of the traces contribute to the amount of inductance the pattern will generate. In order to model this layout, transmission lines on both sides of a symmetric series of inductors and resistors are used to produce the response. A symmetric inductor and resistor structure is created in order to allow the placement of the switch equivalent circuit in the middle. Knowing that the transmission lines on both sides of the switch are 200 μm in length, the setup shown in Figure 3.52 is implemented.

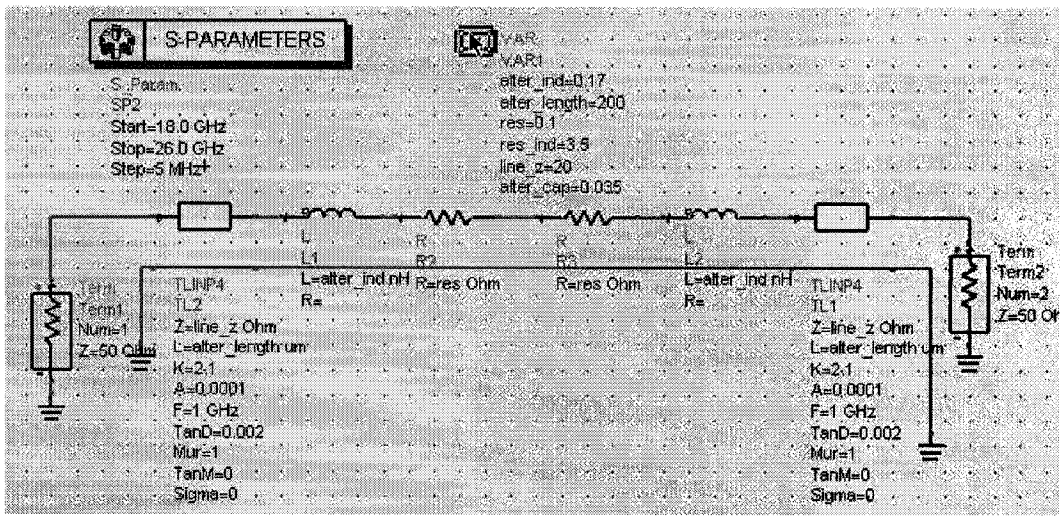

Figure 3.50: Equivalent circuit for the patterned line switch in the up position

The results are given in Figures 3.51 and 3.52 which correlate well with those obtained from measurements in Figures 3.42 and 3.43.

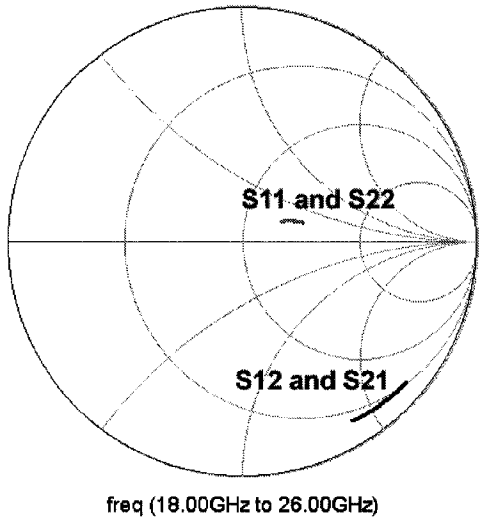

Figure 3.51: S-parameter of middle switch obtained from the equivalent circuit (up position)

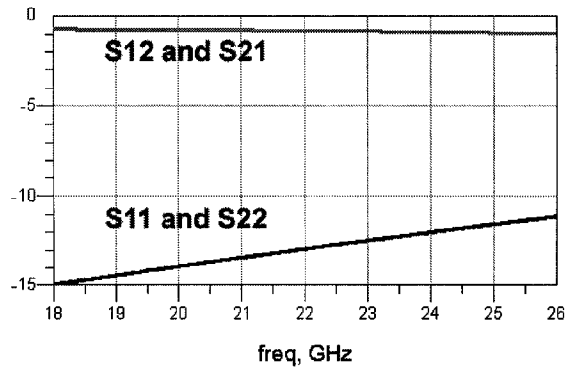

Figure 3.52: Magnitude of the S-parameter of middle switch obtained from the equivalent circuit (up position)

In order to change the response from the up state to the down state, a capacitor is added in between the two resistors to the ground as shown in Figure 3.53.

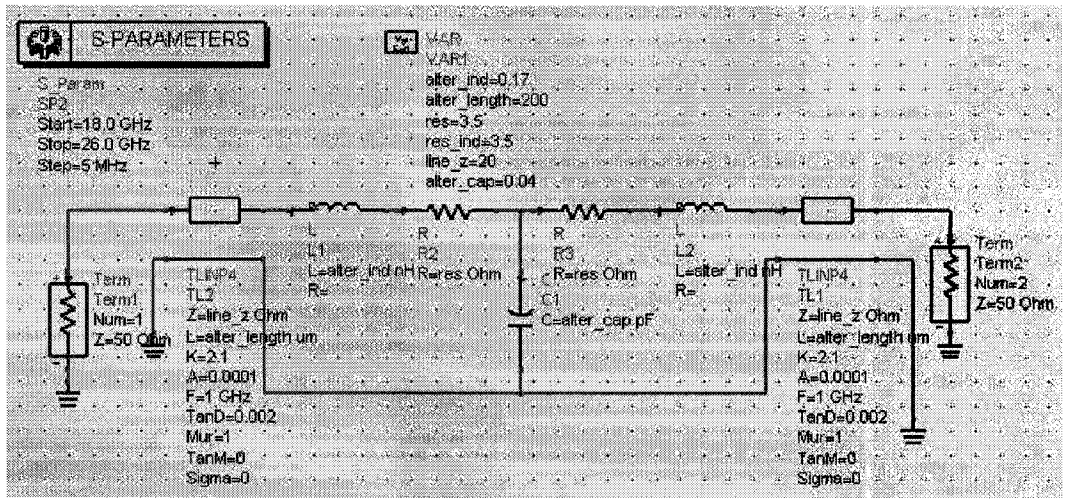

Figure 3.53: Equivalent circuit for the patterned line switch in the down position in ADS

The results that best fit the measured data were obtained for a switch capacitance value of 40 fF. These are shown in Figures 3.54 and 3.55 and compare favorably with the measured results in Figures 3.44 and 3.45.

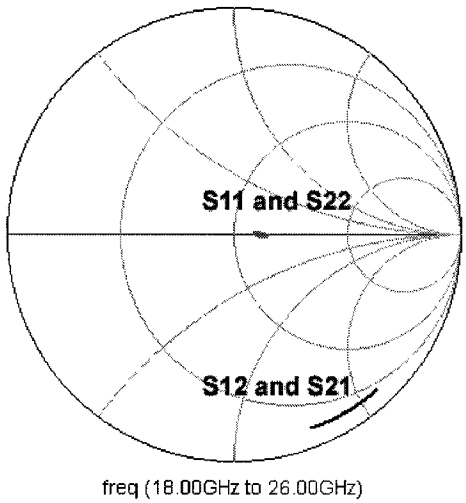

Figure 3.54: S-parameter of middle switch obtained from the equivalent circuit show in Figure 3.52 (down position)

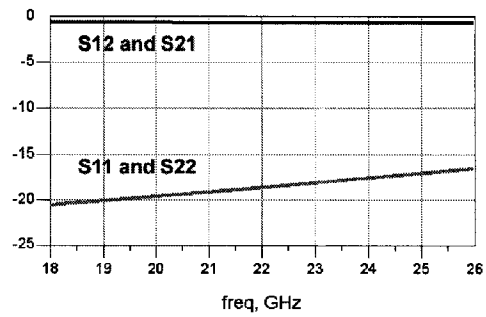

Figure 3.55: Magnitude of S-parameter of middle switch obtained from the equivalent circuit show in Figure 3.52 (down position)

The switch capacitance of 40 fF, is much smaller then the expected 129 fF. There could be a slight misalignment of the bridge with the patterned coplanar lines. For the case of the uniform line, a misalignment would have no effect because the centre conductor is solid and therefore there would be no dependency on position. For the case of the patterned centre conductor, a misalignment could mean the bridge of the switch would not be completely over metal trace and therefore, the capacitance would be reduced. Another possible explanation is that the bridge does not come down perfectly flat due to the additional ridges in the centre conductor.

Another problem with attempting to determine the switch effect on the centre conduction line is the problem of determining the resistance of the switch in the actuated position. On the patterned centre conductor, there is no resistance due to the fact that the capacitance change alone was sufficient to approximate the down

state results from the up state equivalent circuit.

3.3 Tunable CPW filter Design

The next step is to examine the performance of a patterned centre conductor CPW filter combined with the RF MEMS switch tuning elements.

HFSS with be used to simulate the tunable coplanar filter with the switches and the results will be compared with complete equivalent circuit predictions in ADS.

3.3.1 ADS equivalent circuit simulation

The filtering equivalent circuit for the CPW filter structure is used as a template and the modeled switch components in various states were then added to the circuit layout. For reference the filter response initially obtained in section 3.1 corresponds to the expected performance of the tunable filter with both switches up. Figure 3.17 and Figure 3.18 are now repeated as Figures 3.56 and 3.57 for convenience.

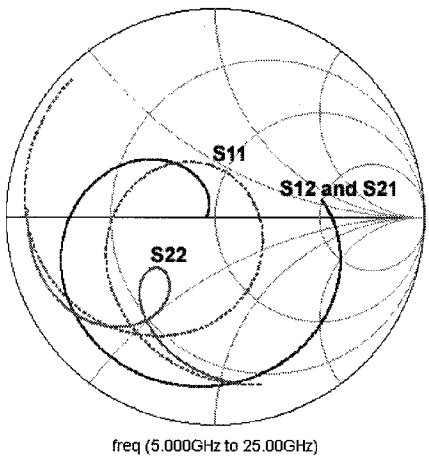

Figure 3.56: ADS equivalent circuit simulation result - Smith chart plot

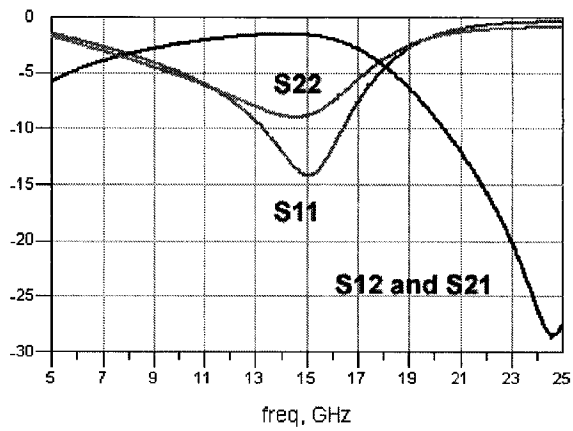

Figure 3.57: ADS equivalent circuit simulation result - magnitude plot

ADS end switch actuated

The ADS equivalent circuit with the end switch actuated and the other switch in the up position appears as shown in Figure 3.58. The dark shaded area indicates where the original circuit of Figure 3.16 has been augmented by the switch equivalent circuit.

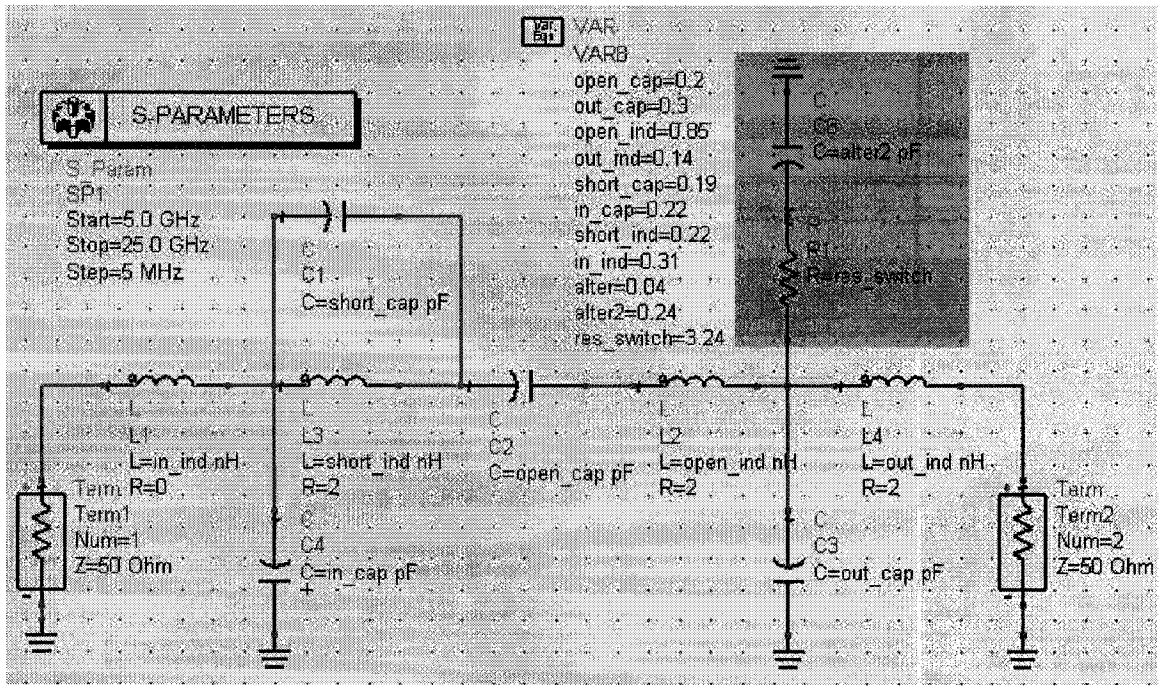

Figure 3.58: Equivalent circuit with end switch actuated

The ADS simulation results are shown in Figures 3.59 and 3.60.

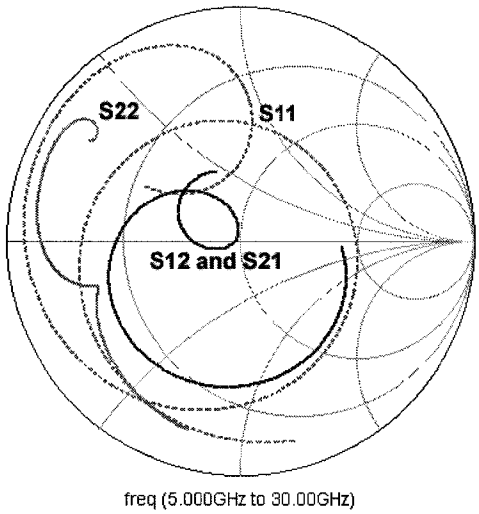

Figure 3.59: S-parameter of filter with end switch down (ADS simulation)

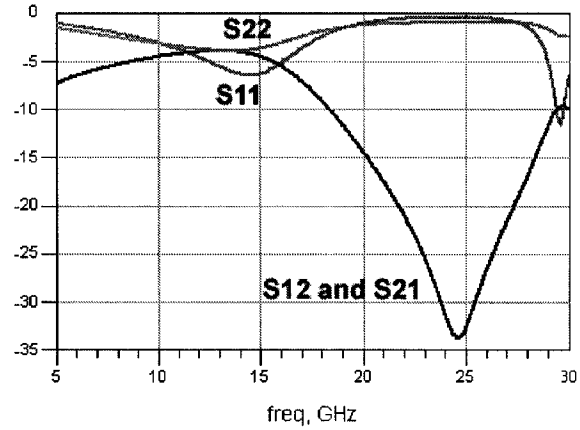

Figure 3.60: Magnitude of S-parameter of filter with end switch down (ADS simulation)

As can be seen, the S_{12} notch frequency has not changed from the referenced response in Figure 3.57, remaining at 24.5 GHz although the insertion loss has changed from -26.6 dB to -33.6 dB.

It can also be noted at 15 GHz that the minimum input reflection $|S_{11}|$ of -14 dB has increased to -6.4 dB. The minimum output reflection $|S_{22}|$ has changed as well from -8 dB to -3.9 dB.

The actuation of the end switch over the uniform line section does not show any frequency shift.

ADS middle switch actuated

The ADS equivalent circuit with the middle switch actuated and the other switch in the up position appears is shown in Figure 3.61. The dark shaded area is where the middle switch equivalent circuit has been added to the the original circuit of Figure 3.16.

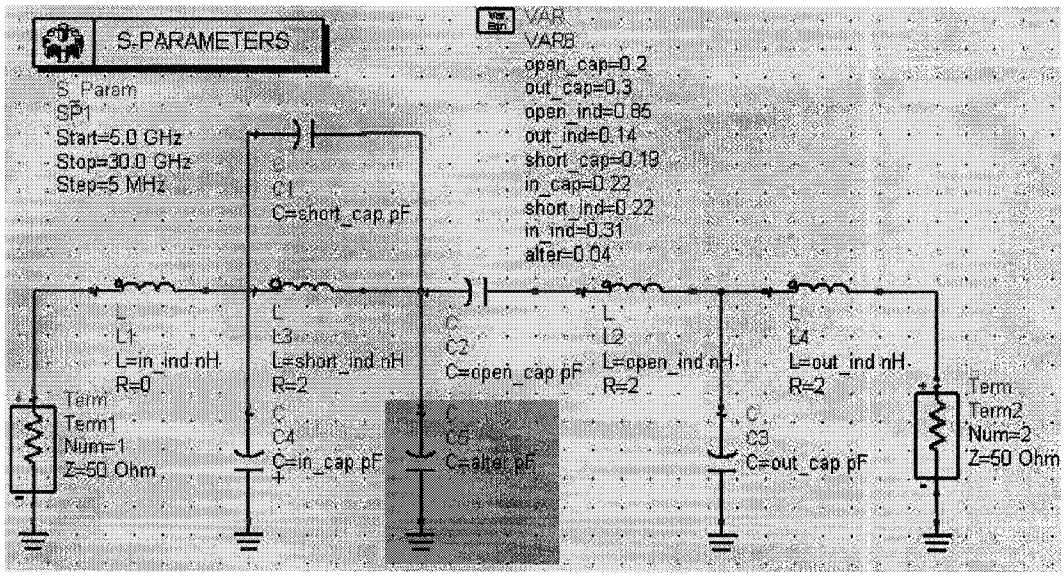

Figure 3.61: ADS equivalent circuit with middle switch actuated

The ADS simulation results are shown in Figures 3.62 and 3.63.

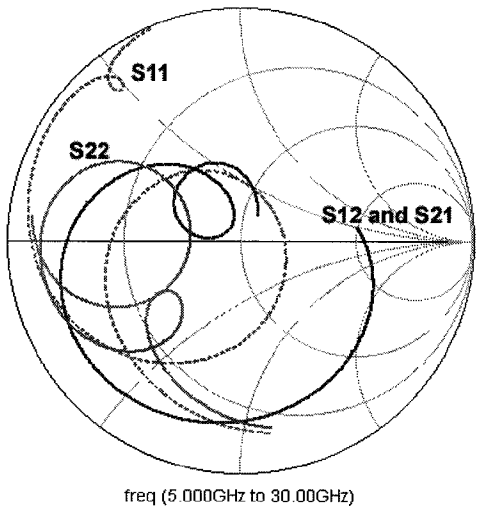

Figure 3.62: S-parameter of filter with middle switch down (ADS simulation)

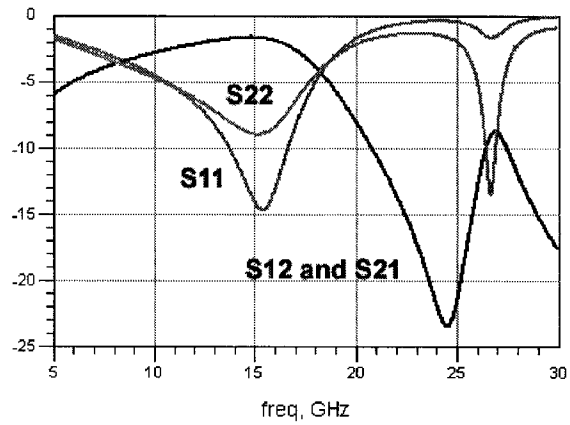

Figure 3.63: Magnitude of S-parameter of filter with middle switch down (ADS simulation)

As can be seen, the S_{21} notch has not changed from the referenced response in Figure 3.57 but has changed in magnitude to become -23.4 dB. However a second notch now appears above 30 GHz.

Although neither of the switches produced a significant frequency shift of the filter response (they primarily affect the amplitude of the S_{21} of S_{11} minima), it must be remembered that the analysis so far is based on approximate equivalent circuit representation. An EM simulation such as HFSS may reveal different results.

3.3.2 HFSS filter simulation

The HFSS based analysis that was previously used in section 3.1 for the reference filter response is altered to include the two MEMS switches. The resulting circuit is shown in Figure 3.64.

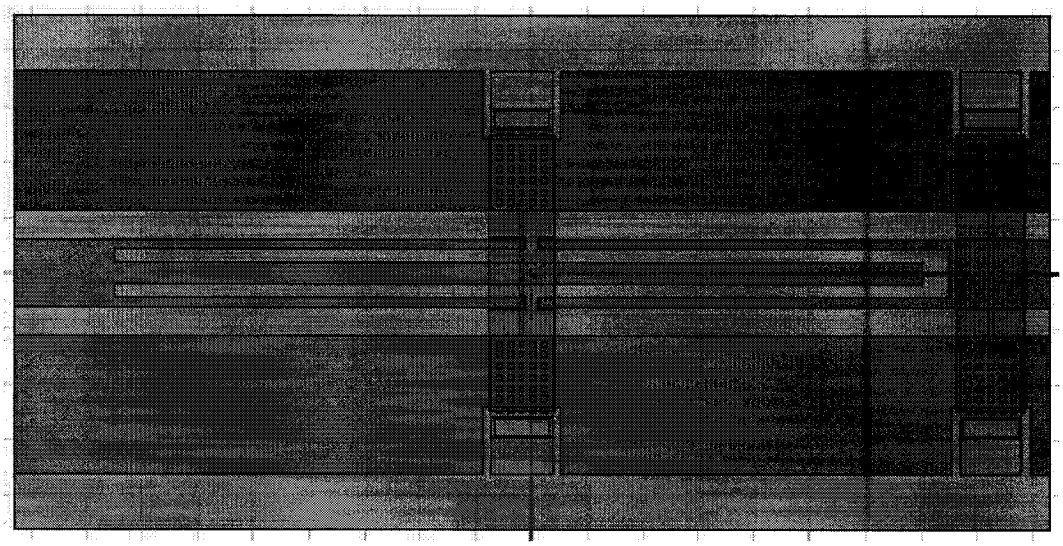

Figure 3.64: Top view of a CPW filter showing MEMS switch locations for HFSS simulation

To begin, the simulation results for both switches in the up position are shown in Figures 3.65 and 3.66:

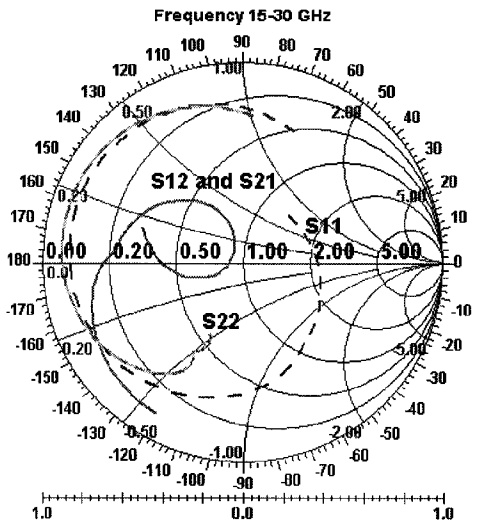

Figure 3.65: S-parameter of filter with both switches up (HFSS simulation)

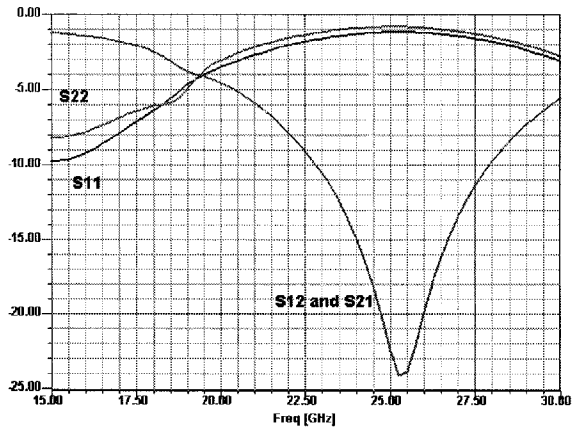

Figure 3.66: Magnitude of S-parameter of filter with both switches up (HFSS simulation)

As can be seen, there is little change from the measured results of the filtering structure without switches shown in Figure 3.11 and the simulated results with no switches, shown in Figure 3.20. This was expected because the switches in the up position are known to have little effect on the CPW filter sections.

HFSS end switch actuated

The simulation results for the end switch in the down position and the middle switch in the up position are shown in Figures 3.67 and 3.68:

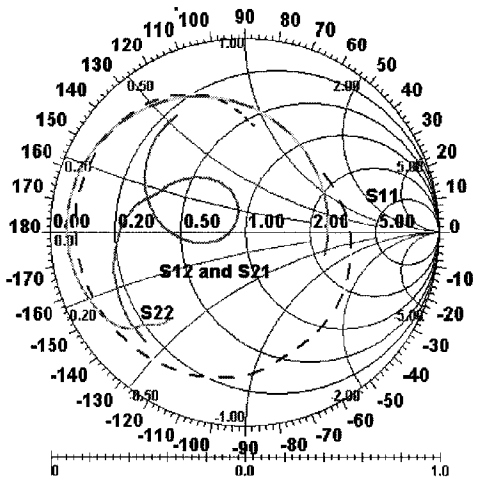

Figure 3.67: S-parameter of filter with the end switch down (HFSS simulation)

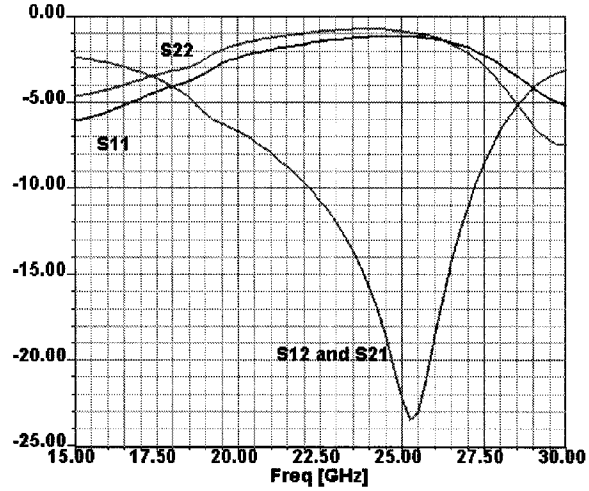

Figure 3.68: Magnitude of the S-parameter of filter with the end switch down (HFSS simulation)

The S_{21} notch in filter response has remained at 25.5 GHz with a slightly changed insertion loss of 23.5 dB. But a change in the input and output reflection magnitude has been noted at 15 GHz. The S_{11} magnitude has increased to -6 dB from -9.75 dB and the S_{22} magnitude has increased to -4.7 dB from -8 dB. These results are consistent with the changes observed in the equivalent circuit based ADS analysis shown in Figure 3.60.

HFSS middle switch actuated

The simulation results for the middle switch in the down position and the end switch in the up position are shown in Figures 3.69 and 3.70:

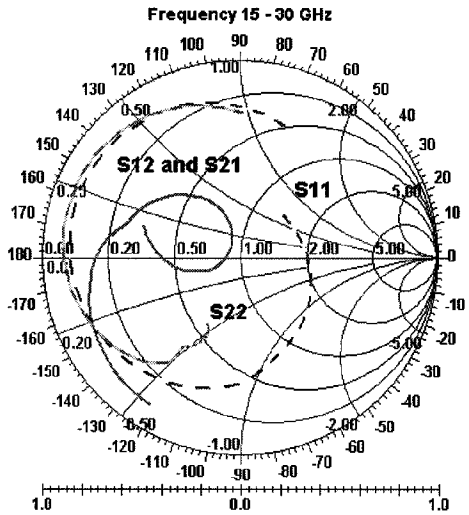

Figure 3.69: S-parameter of filter with middle switch down (HFSS simulation)

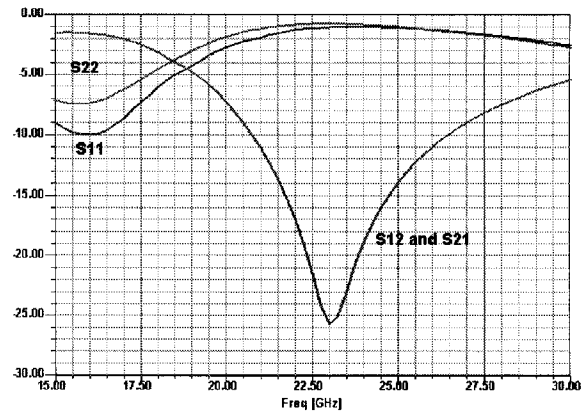

Figure 3.70: Magnitude of S-parameter of filter with middle switch down (HFSS simulation)

Compared to the reference filter response, the S_{21} notch has changed to 22.5 GHz from of 24.5 GHz with negligible change to its insertion loss of -25 dB. This substantial shift was not predicted by the equivalent circuit based analysis.

It is assumed that HFSS is more accurate than the ADS element representation for determining the effect that the switches will have on the filtering structure. Given that HFSS has shown a frequency shift when actuating the traced centre conductor, the next step is to fabricate the design and verify the results experimentally.

In this chapter, a patterned centre conductor CPW filter was verified, modified and modeled. To add tunability, two switch locations were proposed and equivalent circuits for these tuning elements were derived. The circuits were subsequently added to the filter circuit and their predicted effects were analyzed using both and equivalent circuit based simulator (ADS) and an EM solver (HFSS). Results from the HFSS simulation show that a significant frequency shift of the S_{21} notch is obtained with the actuation of the middle switch.

Chapter 4

Fabrication Process

This chapter will describe the fabrication process that is used to implement the CPW filter with MEMS tunable devices.

4.1 Masks and materials

The fabrication process that will be described builds upon a fabrication process that was developed for Carleton University micro fabrication laboratory which was created by Dr. Niall Tait and Jason Rose for a quartz substrate process. The etch times have been altered to properly etch different metal and SiO_2 thicknesses. Bake times and temperatures have been altered to compensate for the change in substrate material. A full listing of the timed steps and temperatures can be found on the process sheet in Appendix B - Process Summary.

All masks were drawn using Tanner EDA L-Edit layout editor software. The masks were transferred onto glass plates. Both light and dark field masks were used.

The photoresist that was used was S1811 and the exposed areas were dissolved in photoresist developer for 1 minute. The wafers were placed into a plasma etcher to remove residual photoresist particles and to straighten the edges of the photoresist pattern.

The aluminum depositions were etched in phosphoric acid at 60°C. The etches must be carefully timed to ensure that there is as little undercutting as possible. Undercutting occurs when the etchant dissolves the material below the photoresist, which will modify the desired pattern. Undercutting in the first metal layer may result in a change in the filter response, but due to the larger dimensions of the design and with carefully timed etches, the undercutting effect would be minimal. Undercutting on the second metal layer, i.e., the bridge, would have a more substantial effect because the bridge is composed of features with smaller dimensions. If there is noticeable undercut in the bridge, there will be a noticeable change in the capacitance of the switch.

The photoresist was removed by immersing the wafer in a bath of Microstrip 2001.

The following sections will provide a more individual and specific details.

4.1.1 Wafer

In order to mimic the filter structure that was created in [20], ceramic 2 inch square alumina wafers were used. Unfortunately, alumina's surface is generally a rougher surface then silicon or quartz but alumina's higher dielectric constant allowed the design to be smaller in size then if it would have been created on the other two substrates.

4.1.2 Metal layer 1

The first metal deposition layer was a 1 μm layer of aluminum, deposited using an E-beam evaporator. The metal layer is patterned, developed, dissolved and etched. The layer was patterned using mask number CU-241-01, shown in Figure 4.1. The light field mask outlined the uniplanar coplanar line filter as well as the base metal layer for the alignment marks and test structures.

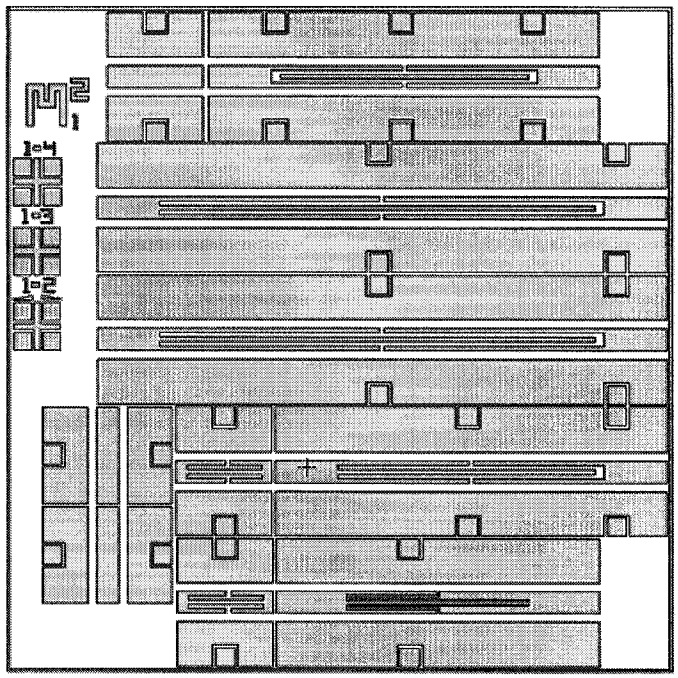

Figure 4.1: Metal 1 layer mask - CU-241-01

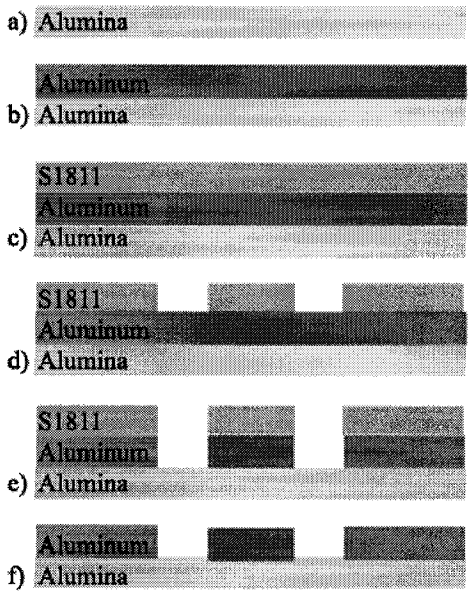

Figure 4.2: Metal 1 deposition fabrication steps - a) cleaned alumina wafer b) e-beam evaporation of metal 1 aluminum c) spin-coating of photoresist S1811 d) photoresist is patterned and developed e) metal is etched using phosphoric acid f) remaining photoresist is stripped using Microstrip 2001

4.1.3 Dielectric material

The chosen dielectric material SiO_2 was deposited using an E-beam evaporator from a quartz source which results in a dielectric layer of SiO_x, where x is predominately 2. The layer was patterned using mask number CU-241-02, shown in Figure 4.3. The purpose of the dielectric layer is to provide a separation between metal 1 CPW filter and the metal bridge when it actuates. It prevents a short that would occur when the biased bridge is attracted to the lower potential ground lines and centre conductor lines. The thickness of this separation determines the capacitance that will be achieved as described in 3.2. The fabricated thickness was 0.25 μm thick.

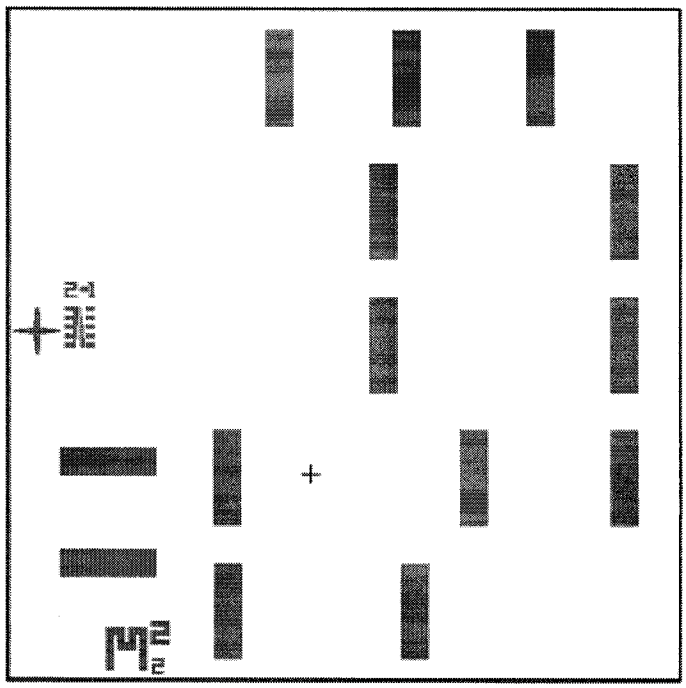

Figure 4.3: Dielectric layer mask - CU-241-02

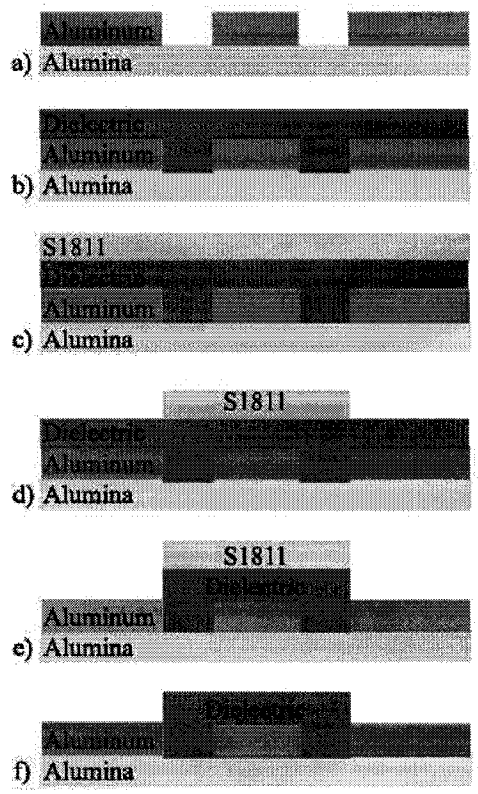

Figure 4.4: Dielectric deposition fabrication steps - a) wafer before processing b) e-beam evaporation of dielectric SiO_2 c) spin-coating of photoresist S1811 d) photoresist is patterned and developed e) dielectric is etched using siloxide f) remaining photoresist is stripped using Microstrip 2001

The dielectric was patterned and developed using S1811 photoresist and etched in a buffered hydrofluoric acid mixture called siloxide. The photoresist was removed by immersing the wafer in a bath of Microstrip 2001.

4.1.4 Sacrificial layer - S1811 photoresist

The purpose of this layer is to provide a temporary buffer material which is used to separate the previous layers from metal 2 that will be applied afterwards. The thickness of the sacrificial layer will be the thickness of the air gap of the switch and unlike other procedures, it will not be removed after it is patterned. The next metal layer must be deposited on top of it, and removing the sacrificial layer will release

the bridge.

In order to vary the height of the bridge, the speed at which the S1811 is deposited by spin-coating is reduced from the standard 4000 rpm to 2000 rpm for 30 sec. This corresponds to approximately 1.5 μm. The layer was patterned using the dark field mask number CU-241-03, shown in Figure 4.5. The mask is used to create openings in the sacrificial layer where the bridges will contact the first metal layer to create supporting beams.

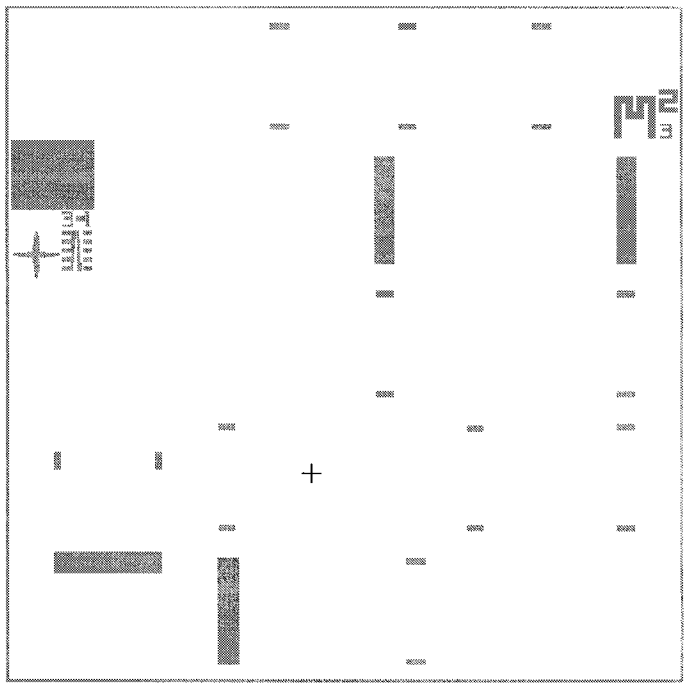

Figure 4.5: Sacrificial layer mask - CU-241-03

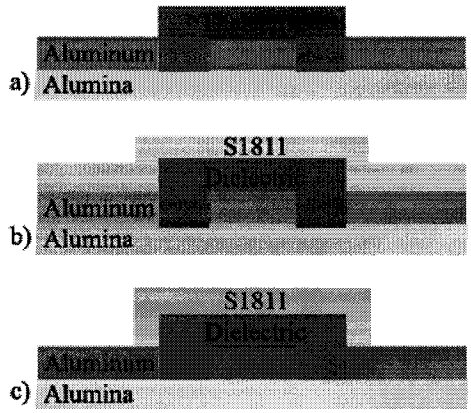

Figure 4.6: Sacrificial layer deposition fabrication steps - a) wafer before processing b) spin-coating of photoresist c) photoresist is patterned and developed Note: photoresist is not removed

4.1.5 Metal 2 layer

The last layer to deposit was a second layer of aluminum using an electron beam evaporation. Once etched, the metal will be used to become the bridges and post that comprise the MEMS switch. The metal layer is patterned, developed, and the developed photoresist is dissolved. The metal is etched but not released in the same manner as was done for the first metal layer. The fourth mask to etch the metal layer is shown in Figure 4.7.

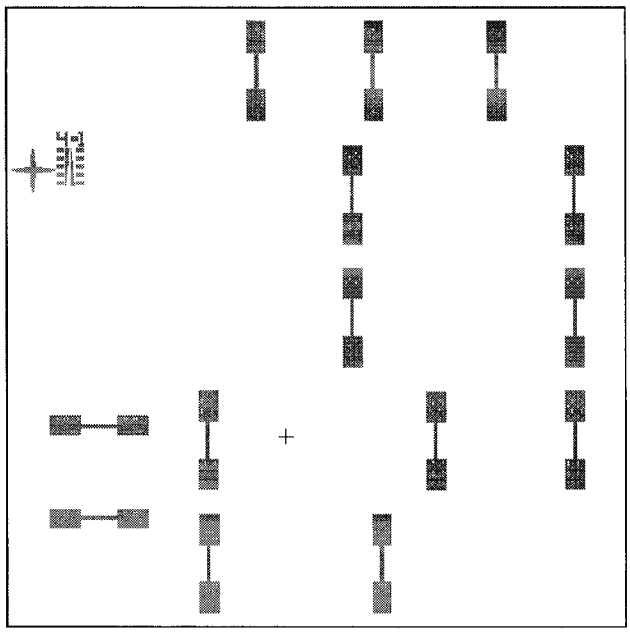

Figure 4.7: Metal 2 layer mask - CU-241-04

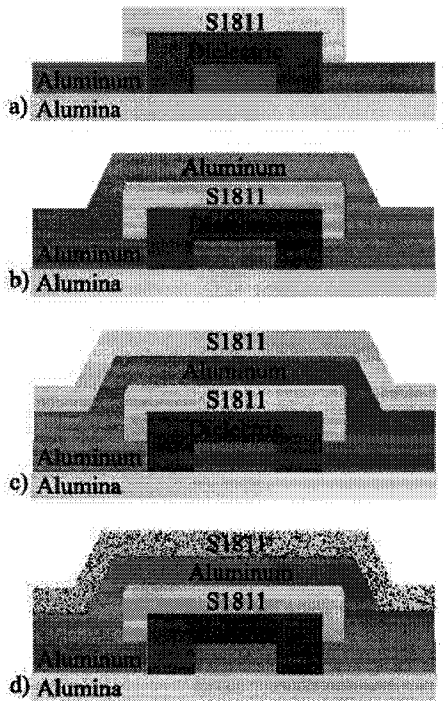

Figure 4.8: Metal 2 deposition fabrication steps - a) wafer before processing b) e-beam evaporation of metal 2 aluminum c) spin-coating of photoresist S1811 d) photoresist is patterned and developed and metal 2 is etched using phosphoric acid

A more detailed description of each process step can be found in Appendix B - Process Summary. It has additional process descriptions including exposures, bake times, bake temperatures, ion etching durations and power settings, spin coating speeds and release steps and times.

4.2 Final release

There are two considerations that must be made when releasing the final switch. The first consideration regards dissolving the photoresist remaining on the wafer. It must be noted that the sacrificial layer must be dissolved along with the photoresist which is above the second metal layer. Therefore, a longer etch is generally used at a higher temperature to ensure that the buried sacrificial layer is removed. It should also be mentioned that while the sacrificial layer is being removed and for all forthcoming steps, there should be no vigourous agitation. The bridge structures are delicate and may break or bend. The removal of the photoresist is followed by a soak in deionized water to dissolve and clean all chemicals left on the surface of the wafer and the devices.

The wafers were then submersed in an isopropanol (IPA) bath for one minute to rinse the remaining solvents from the surfaces of the filter structure and the wafer.

The second consideration regards another type of stiction that may also cause problems. During the release process, liquids can be trapped in between surfaces. Liquids can be etchants which are used in order to wet etch sacrificial layers, solvents which are used in the cleaning process, or it can simply be humidity that accumulates over time. The liquids can form a meniscus in between surfaces which cause attractive forces on the separated layers. These forces may cause adhesion or, in the extreme case it may cause suspended structures to collapse completely. This type of stiction due to trapped liquids may be overcome by using multiple techniques i.e.: textured surface may be used to limit the amount of contact area; a drying step for the structure in high pressure and temperature to prevent the meniscus from forming; or chemically treating the surface with a coating to prevent sticking. In this thesis, a hexamethyldisilizane (HMDS) wash was used to coat the surfaces of the wafer, the CPW lines, and the MEMS structure. HMDS is primarily used as an adhesion promoter at Carleton University fabrication facility. The coating makes the

wafers hydrophobic which helps to reduce interfacial forces. Initial research in this application for HMDS was previously done by Rose [22].

The wafer was placed in an HMDS solution for a minute to make the surfaces of the device hydrophobic and reduce the risk of stiction occurring.

The last bath that was used was a methyl alcohol bath for a minute. This step was used to lower the surface tension that will be placed on the device when the liquid evaporates.

The wafer was then baked for 45 seconds to encourage the alcohol to evaporate and the switch was ready for testing.

The release steps are shown below:

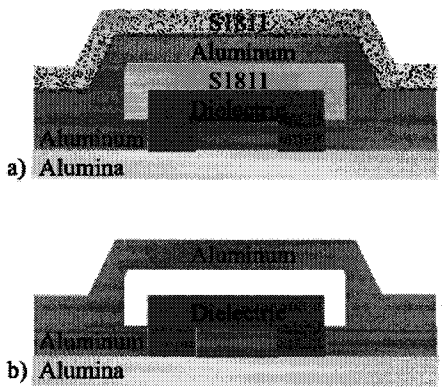

Figure 4.9: Final release fabrication steps - a) wafer before release b) wafer is put into successive baths of Microstrip 2001, deionized water, isopropanol, HMDS, and methanol. The bridge is now released and the device is complete.

This chapter has described the fabrication process that is used to implement the CPW filter with MEMS tunable devices including the masks that are used and the release process.

Chapter 5

Experimental verification of CPW tunable filter

This chapter presents the results obtained for the CPW tunable filter developed in chapter 3. First the equipment that was used to take the measurements will be described. Comparisons will be done with the theoretical equivalent circuits and possible improvements to the EM elements will be discussed.

5.1 Equipment

A micrograph of the the final fabricated MEMS tunable CPW filter is given in Figure 5.1. The aluminum circuit has dimensions of 3.2 mm by 0.725 mm.

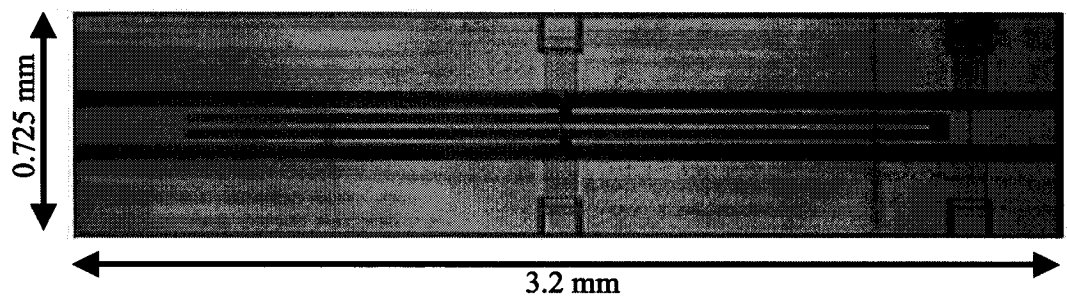

Figure 5.1: Top view of the final filtering structure

The CPW filter was tested using a pair of ground signal ground (GSG) three probe pin picoprobe, 40 A-GSG-150-DP, with 150 μm separation between the pins. The switches were actuated using DC ground signal (GS) pins placed at the switch pads. Only one switch was actuated at a time.

An Agilent 8722ES 50 MHz to 40 GHz S-parameter Network Analyzer was used to measure and record the S-parameters. A Hewlett-Packard E3610A DC power supply was used to actuate the switches.

The equipment was calibrated using a picoprobe CS-5 GSG calibration substrate. Using a calibration substrate removes the imperfections of the equipment on the measured results down to the S-parameter reference plane located at the probe tips.

Measurements were done on a grounded chuck after verifying with simulations that the presence of the ground plane does not alter the CPW line behaviour.

5.2 Measurements

5.2.1 Switches in the up state

Figures 5.2 and 5.3 show measured results obtained when the switches were both in the up state:

The shape and form of the S-parameters are very similar to the expected results given in Figure 3.66. As can be seen the S_{21} notch frequency occurs at approximately 24.9 GHz with 25.6 dB of insertion loss. This is almost identical to the notch frequency of the CPW filter with no bridges. HFSS simulation predicted a notch frequency of approximately 25.25 GHz with 23.7 dB of insertion loss. Since HFSS results for the coplanar lines with no bridges was off by approximately the same amount, this discrepancy is acceptable. The output reflection coefficient at this frequency was found to be -0.96 dB and the expected HFSS simulation result is -0.84 dB, which is very close.

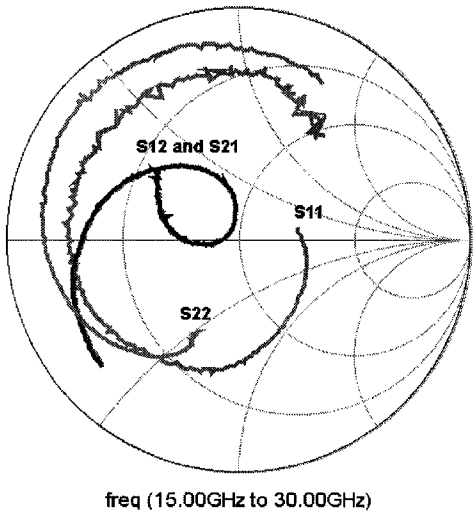

Figure 5.2: S-parameter of filter with both switches up (measured results)

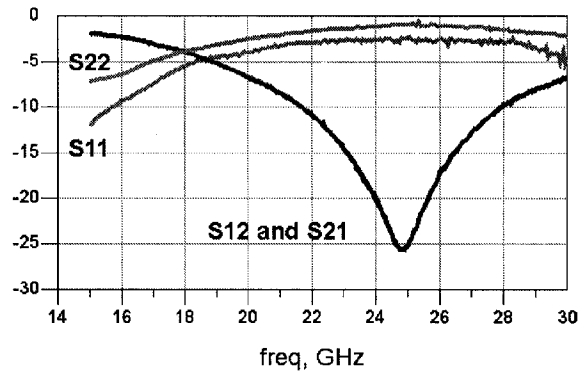

Figure 5.3: Magnitude of S-parameter of filter with both switches up (measured results)

The measured input reflection coefficient also compares favorably with simulations. At the notch frequency a value of 2.6 dB is obtained, which is identical to the HFSS prediction.

5.2.2 End switch in the down state

Since there is no change expected for the notch frequency, the measurements focused on the reflection coefficients minima around 15 GHz. Thus the graphs are obtained from 5 GHz to 20 GHz in order to better show this characteristic. The results are given in Figures 5.4 and 5.5.

The shape and form of the S-parameters are similar to the expected results from simulations. At 15 GHz, input return loss has changed from 12.2 dB in the up state to 8.3 dB in the down state, a change of 3.9 dB. The expected simulated results were -6 dB in the down state as shown in Figure 3.68.

The output return loss has changed to 3.8 dB while the expected HFSS result is -4.7 dB at 15 GHz as shown in Figure 3.68.

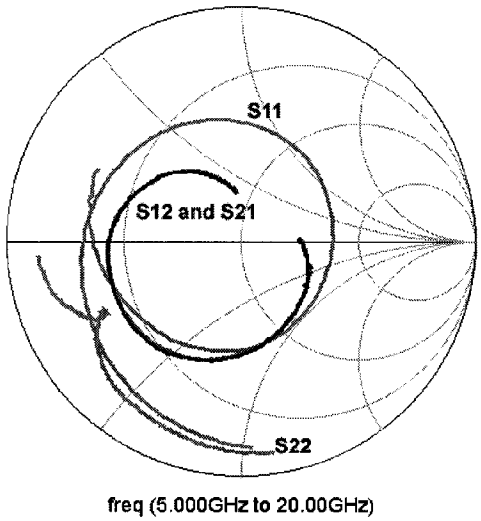

Figure 5.4: S-parameter of filter with end switch down (measured results)

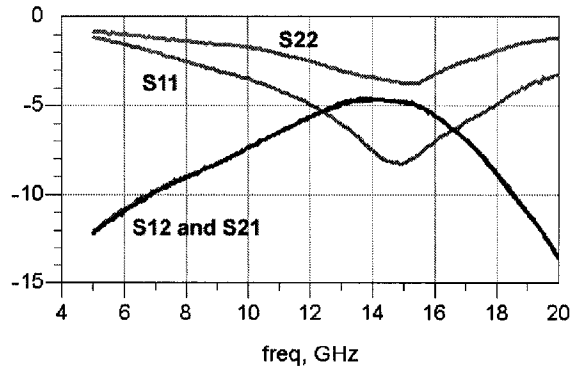

Figure 5.5: Magnitude of S-parameter of filter with end switch down (measured results)

The corresponding insertion loss is now 4.7 dB while the expected HFSS result is unchanged at -1.5 db as shown in Figure 3.68.

For the measurements with the end switch actuated, the ADS measurements were in close agreement with the HFSS measurements indicating that the equivalent circuit modeling is a powerful method for rapid CPW/MEMS circuit design.

As expected, the end switch over the uniform section of line did not change the notch frequency of the insertion loss. The measured results did show a magnitude change of the input and output return losses. The similarity of the measured and simulated results indicate that the equivalent circuits proposed can predict the effect that a switch will have at that location. The shape and trends of the two sets of results agree but some discrepancy in magnitude is noticed. This could be due to the fact that the form of the actuated switch cannot be handled in simulation. Unfortunately, it does not appear that a switch at this location will demonstrate a frequency shifting tuning capability.

5.2.3 Middle switch in the down state

Figures 5.6 and 5.7 show the measured results obtained when the middle switch was actuated and the end switch was not actuated.

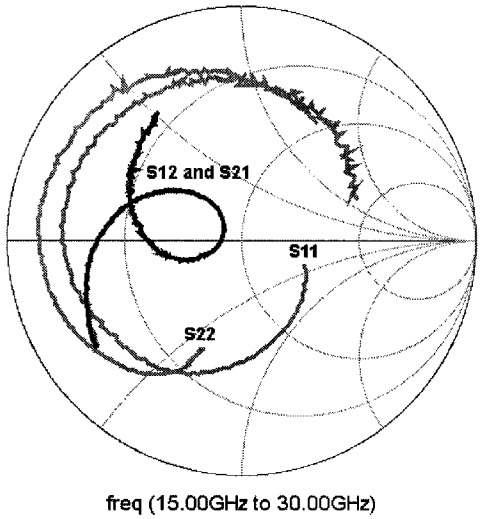

Figure 5.6: S-parameter of filter with middle switch down (measured results)

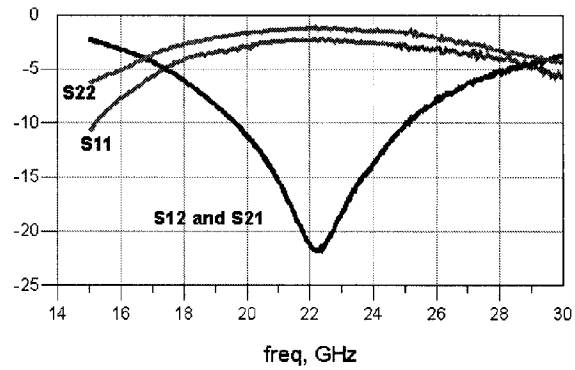

Figure 5.7: Magnitude of S-parameter of filter with middle switch down (measured results)

The shape and form of the S-parameters are very similar to the expected HFSS results. As can be seen in Figure 5.7 the S_{21} notch frequency occurs at 22 GHz with a level of -21.75 dB. HFSS simulation predicted a notch frequency of approximately 23 GHz at a level of -25.7 dB as shown in Figure 3.70. The lumped equivalent circuit did not predict this type of response.

The input return loss at 22 GHz is 2.35 dB. Comparing this with the HFSS results, the return loss of 2.6 dB is remarkably close. The measured output return loss is 1.2 dB and the expected HFSS simulation result was 0.8 dB, which is also very close.

5.2.4 Overlaying results of the actuated middle switch compared with the results of both switches up

Figure 5.8 shows the measured results for both switches up, the measured results for the middle switch down and the HFSS simulated results for the middle switch down.

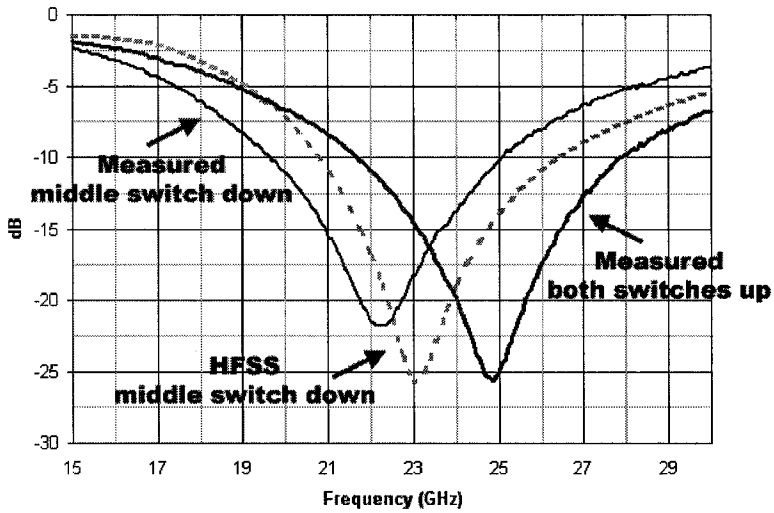

Figure 5.8: Magnitude of S_{12} and S_{21} S-parameter plots showing measured both bridges up, measured middle switch down and HFSS middle switch down

Figures 5.9 and 5.10 overlay the S_{12} and S_{21} S-parameters of the measured results for bridges in both the up state and for the case where only the switch over the patterned centre conductor is actuated.

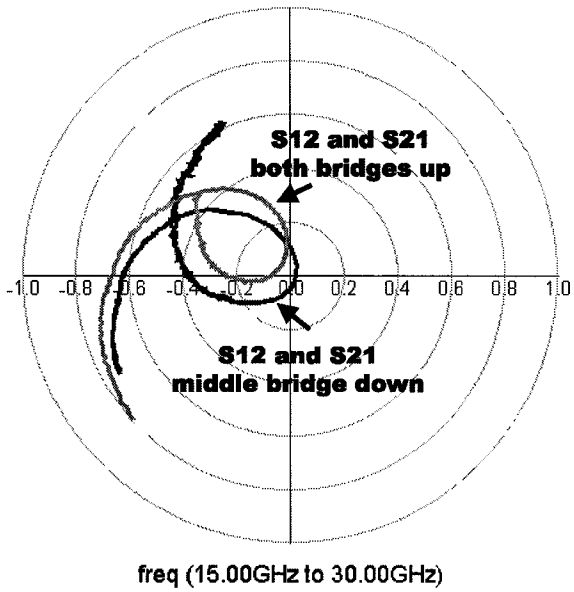

Figure 5.9: S_{12} and S_{21} S-parameter polar plot showing both bridges up results and for the middle switch actuated results

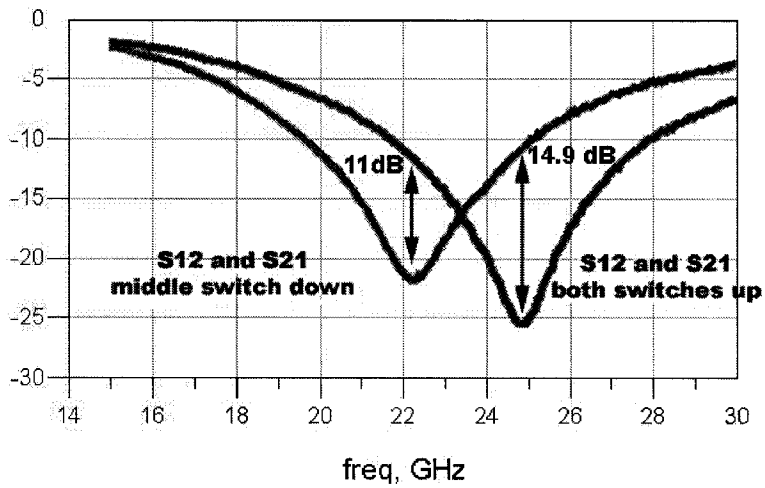

Figure 5.10: Magnitude of S_{12} and S_{21} S-parameter plot showing both bridges up results and for the middle switch actuated results

As can be seen in Figure 5.10, the notch shifts from 24.9 GHz to 22.25 GHz. At 25 GHz there is an insertion loss change of 14.9 dB, and at 22.25 GHz there is an insertion loss change of 11 dB between the two states. This represent a significant variation of the filter's rejection characteristic through the use of MEMS switches.

The switch over the patterned centre conductor has a 2.75 GHz shift in the notch frequency of the insertion loss. The similarity of the measured and HFSS simulated results indicate that HFSS can predict the effect that a switch has at that location. A substantial frequency shift has been obtained, fulfilling one of the main objectives of the thesis.

This means that the lumped equivalent circuit cannot accurately predict the change that occurs when the switch equivalent circuit is added in this particular location. This is due to the fact that the equivalent circuit of the switch has not been properly incorporated with the lumped equivalent circuit of the entire filter structure. However it is believed that with careful examination of this issue will allow an improved circuit to be developed.

5.3 Possible Improvements to increase the frequency shift

Although filter tunability has been demonstrated in this work, the achievement of even greater frequency shifts would be beneficial. In order to increase the frequency shift one of the possible methods could be to reduce the switch dielectric thickness. A larger shift would result because the height of the actuated bridge is decreased which leads to a larger capacitance. Using HFSS to simulate the same structure but with a dielectric thickness of 0.1 μm produces the simulation results shown in Figures 5.11 and 5.12.

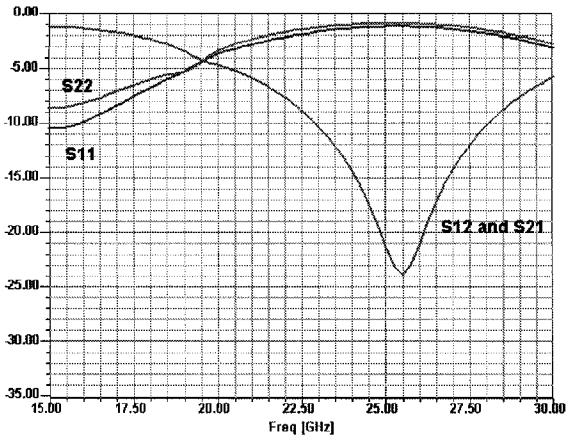

Figure 5.11: Magnitude of S-parameter plot of filter with both switches up and a 0.1 μm dielectric thickness(HFSS simulation)

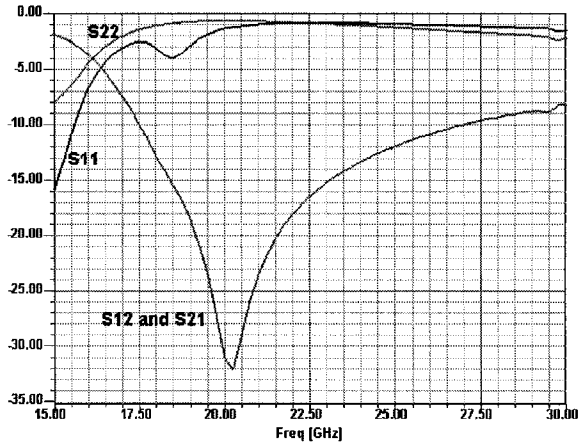

Figure 5.12: Magnitude of S-parameter plot of filter with middle switch down and a 0.1 μm dielectric thickness(HFSS simulation)

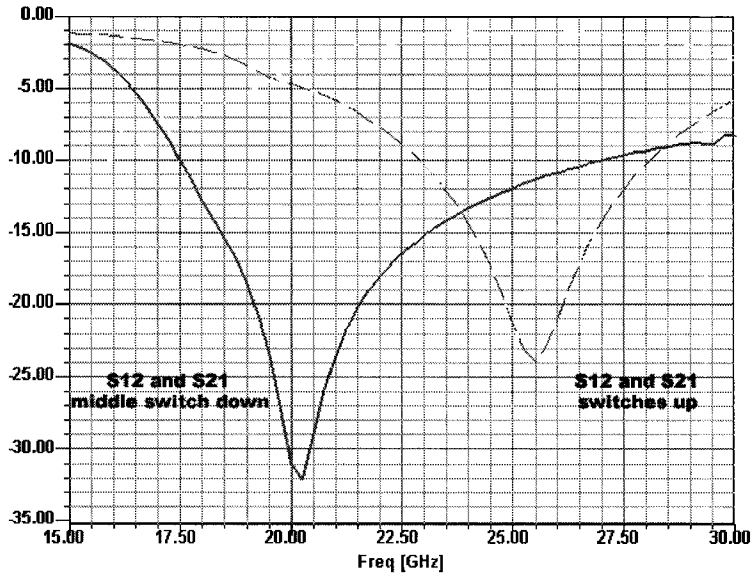

Figure 5.13: Magnitude of S-parameter plot of filter for 0.1 μm dielectric thickness for bridges in both states (HFSS simulation)

As is expected, the bridge in the up state has changed very little from the 0.25 μm bridge up simulation and fabrication results, with the S_{21} notch at 25 GHz.

The results for the bridge in the down state show that the S_{21} notch frequency has

shifted much further to the left, to 20.25 GHz. Now, at 20 GHz there is a 25 dB variation in signal rejection between states.

5.4 Summary

The equipment that was used to take the measurements has been described. Measurements of the final fabricated tunable CPW filter have been presented and discussed. Comparisons have shown that both the lumped equivalent circuit and the EM simulator can predict the effect that the end switch has. The middle switch was properly predicted by the EM simulator but not by the lumped equivalent circuit at this time. A possible method of improving the performance of the filter has been discussed.

Chapter 6

Thesis Conclusions and Future Work

6.1 Conclusions

In this thesis, the design methodology for altering a coplanar waveguide filter was investigated and performed. An equivalent circuit for the filter was created using lumped components.

Two micro electro mechanical series switches were modeled and fabricated. Equivalent circuits were created for switches that were located over a uniform centre conductor line and a patterned centre conductor line of the coplanar waveguide filter.

When the equivalent circuit of the switches were combined with the lumped equivalent circuit of the filter, it was determined that the switch located over the uniform centre conductor line gave a good approximation of the expected results, which shows the usefulness of the lumped equivalent circuit approach. In it's present form, the equivalent circuit of the switch located over the patterned centre conductor line did not yield correct results. However, the full effect of the switch on the filtering structure can be determined with a simulator such as HFSS.

The filtering structure was fabricated in the Carleton University micro fabrication facility using a four-layer, surface micro-machining process.

The testing and corresponding performance results of the filter is described. Testing results show that the transmission notch frequency changed from 24.9 GHz with both switches up to 22 GHz by actuating the middle switch. The insertion losses were found to be -25.6 dB to -21.75 dB respectively. A 2.9 GHz shift was achieved.

6.2 Thesis contributions

This thesis has demonstrated the adaptation of a coplanar waveguide filtering structure to an in house fabrication process. It was analyzed through simulations and verified by measured fabricated devices.

The effect of micro electro mechanical switch loading to predict the effect on the filtering response using simulations has been shown.

The tunability of the filter has been demonstrated by fabricated, measured and compared with simulations.

It has been determined that simple lumped equivalent circuits are difficult to extract and that further investigations would be needed to determine if a lumped equivalent circuit can be designed that can take into account a bridge located in the middle of the filtering structure. It has been found that a simulator such as HFSS can be used to model the filtered structure and the effect that switches will have on the filter.

6.3 Future work

The main goal of providing a frequency shift using a MEMS capacitive switch was achieved however, there are possible areas of future work that may provide additional interest.

6.3.1 Correcting the equivalent circuit

The equivalent circuit did not work as expected. The switch located over the patterned centre conduction line did not model the obtained result. In order to come up with a more accurate equivalent circuit, both the open ended and the short ended coplanar waveguide series stubs could be fabricated separately and equivalent circuits could be created of the separate design.

Putting these equivalent circuits together and comparing with the measured equivalent circuit would show if the components could be created as block and combined or if the separate equivalent circuits do not reflect the interaction that occurs when the traces are combined.

6.3.2 Increasing the shift

As discussed in section 5.2, one could try to increase the frequency shift of the filtering structure by decreasing the dielectric thickness. It was shown using HFSS that the notch frequency has shifted to 20.25 GHz, an additional 1.75 GHz, by decreasing the dielectric thickness to 0.1 μm.

Although one could continue to try to lower the frequency further by decreasing the dielectric thickness, one would have to be careful that the pull down voltage would not exceed the breakdown voltage of the dielectric.

Another way to increase the shift would be to change the dielectric material to a higher dielectric constant, such as SiN. With a higher dielectric constant, one could have a thicker dielectric but still obtain a larger shift. The effect of the different dielectric materials could could also be combined with different thicknesses.

Altering the switch dimensions

One other possible solution to shifting the filter response more would be to increase the bridge size over the centre conduction line of the CPW. Increasing width of the

bridge over the centre conductor would provide a larger area over the centre conductor and increase the capacitance.

RF MEMS is a field that holds a tremendous amount of potential to help push the miniaturization of common devices. Further research in this work can aid in that pursuit.

Appendix A

Capacitance calculations

The following section contains the code used to determine the expected capacitance of the bridge.

```
function capacitances=capacitance_cal(bridge_width, heights,
centre_cond_width, die_thickness, over_ground_width, gap,
bridge_length)
%Function purpose is to calculate expected capacitance
%between the bridge and the conduction line.
%  bridge_width:          bridge width in um
%  heights:               heights of bridge in um
%  centre_cond_width:     width of the centre conductor in um
%  die_thickness:         dielectric thickesses to graph in um
%  over_ground_width:     bridge width over ground portion in um
%  gap:                   gap width of cpw lines in um
%  bridge_length :        width of the bridge
%
%A typical function call would be:
%cap = capacitance_cal2(10, [0:0.01:1.5], 125,[0.1,0.2,0.5],
                        110, 50, 450)

format compact;                              %Compact the output
format long;                                 %Print more decimal
clc;                                         %Clear previous outputs
colour_array=['r','g','b','c','m','y'] ; %graph colours array
```

```
centre_cond = centre_cond_width*10^(0-6);%size of centre conductor
len         = centre_cond;       %second val of conductor

e0 = 8.8542*10^(0-12);          %Permittivity of free space
K1 = 1;                         %Dielectric constant air
K2 = 3.9;                       %Dielectric constant silicon oxide
%K2 = 7.6;                      %Dielectric constant silicon nitrate
e  = e0;                        %combined permittivity

width = bridge_width*10^(0-6); %width of the bridge
area = width*len;              %bridge area over centre conductor

%calc pad size over ground planes, store in area_contact
gap_in_um = gap*10^(0-6);                %convert gap to um
actual_width = over_ground_width*10^(0-6); bridge_length_in_um
=bridge_length*10^(0-6); subtract_amount =
centre_cond_width*10^(0-6)+ 2*gap_in_um; L  =
bridge_length_in_um-subtract_amount;
area_contact = actual_width.*L*3/4;   %3/4 added for bridge holes
area=area;%+area_contact;

air_height = (heights).*10^(0-6)
%convert heights of air separation potion of bridge to um
num_die = size(die_thickness);
%get the number of dielectric heights
num=num_die(2);
%get the number of dielectric thicknesses
die_height=0;
%delete all stored dielectric thicknesses
legend_vals='';
%clear all stored legend values
capacitances=[];
%clear all possibly stored capacitances values
handle = figure(1); excel_file=[]; one_caps=[];
for n=1:num
%for each dielectric thickness
 die_height = die_thickness(n)*10^(0-6);
 %convert heights of dielectric separation potion of bridge to um
 one_cap = e*area./(air_height*1/K1+die_height*1/K2);
 %calculate bridge capacitances
 capacitances=[capacitances;one_cap];
 excel_file=[excel_file;die_height,one_cap];
 legend_vals=strvcat(legend_vals,strcat(strcat(
 'Dielectric thickness:', num2str(die_thickness(n)),' um')));
 figure(2);plot(air_height, one_cap,colour_array(n));grid on;
```

```
 %plot the values
if (n==1)
%if the first plot has just been done
    hold on;
    %freeze figure to have all dielectrics plot on same axis
end
%end of if statement
end
%end the for loop
hold off;
%release the plot so others can overwrite it
capacitances
ylabel('Capaciatances')
%add the label for the y axis
xlabel('Bridge height')
%add the label for the x axis
title1 = 'Bridge height versus capacitances ';
%Give a title to the plot
title(title1);
%add the title to the graph
lable1 = strcat(' Material dielectric is:',num2str(K2));
%put the dielectric constant used
text(mean(air_height),max(one_cap),lable1,'FontSize',10)
%put the dielectric constant on the graph
legend(legend_vals,0)
%put a legend on the graph for each dielectric height
```

Appendix B

Process Summary

Here is the MEMS switch process sheet that was used in the Carleton University Micro Fabrication Laboratory for fabricating the final coplanar waveguide MEMS tuned filter.

MARIANI MEMS CAPACITIVE SWITCH PROCESS

Starting material:
Alumina

Metal 1:
E-beam 10000 Å Al (1 um)
HMDS 4000rpm, bake 60 sec @ 105°C
S1811 4000rpm, bake 90 sec @ 105°C
Mask M1 CU-241-01
Expose 41 sec, develop MF321, bake 4 min @ 115°C
PR descum O_2 0.3 Torr 100W 1 min
Al etch phosphoric acid 3 min @ 60°C
Microstrip 7.5 min + 7.5 min @ 70°C, 15 min DI water rinse

Dielectric:
E-beam 2500 Å SiO_2 - Set to evaporator to 650 Å
HMDS 4000rpm, bake 90 sec @ 105°C
S1811 4000rpm, bake 90 sec @ 105°C
Mask M1 CU-241-02
Expose 41 sec, develop MF321, bake 4 min @ 115°C

PR descum O_2 0.3 Torr 100W 1 min
Siloxide etch (***HF***) etch 10 sec/1000A, 10 min rinse DI water
Bake 5 min @ 105°C
Microstrip 7.5 min + 7.5 min @ 70°C, 15 min DI water rinse

Sacrificial spacer:
Bake 2-3 hrs 165C to thoroughly dehydrate surface, cool 2.5 min before coating
HMDS 2000rpm, bake 60 sec @ 105°C
S1811 2000rpm, bake 90 sec @ 105°C ***REDUCED SPIN SPEED***
Mask M1 CU-241-03
Expose 41 sec, develop MF321, bake 5 min @ 120°C
PR descum O_2 0.3 Torr 100W 1.5 min
NO ETCH OR STRIP, PR STAYS ON UNDER M2

Metal 2:
E-beam 10000 Å Al (1 um)
HMDS 4000rpm, bake 60 sec @ 105°C
S1811 4000rpm, bake 90 sec @ 105°C
Mask M1 CU-241-04
Expose 41 sec, develop MF321, ***DO NOT HARD BAKE***
PR descum O_2 0.3 Torr 100W 1.5 min
Al etch phosphoric acid 2-4min @ 60_2C

Release:
Microstrip 10min+10min @ 70°C
DI cascade 8 min
IPA 1 min
HMDS 8 min
Methanol 1 min
Hotplate dry 45sec @ 110°C

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