1

PM-1 3 1/2"x4" PHOTOGRAPHIC MICROCOPY TARGET
NBS 1010a ANSI/ISO #2 EQUIVALENT

PRECISIONSM RESOLUTION TARGETS

National Library
of Canada

Acquisitions and
Bibliographic Services Branch

395 Wellington Street
Ottawa, Ontario
K1A 0N4

Bibliothèque nationale
du Canada

Direction des acquisitions et
des services bibliographiques

395, rue Wellington
Ottawa (Ontario)
K1A 0N4

Your file - Votre référence

Our file - Notre référence

NOTICE

The quality of this microform is heavily dependent upon the quality of the original thesis submitted for microfilming. Every effort has been made to ensure the highest quality of reproduction possible.

If pages are missing, contact the university which granted the degree.

Some pages may have indistinct print especially if the original pages were typed with a poor typewriter ribbon or if the university sent us an inferior photocopy.

Reproduction in full or in part of this microform is governed by the Canadian Copyright Act, R.S.C. 1970, c. C-30, and subsequent amendments.

AVIS

La qualité de cette microforme dépend grandement de la qualité de la thèse soumise au microfilmage. Nous avons tout fait pour assurer une qualité supérieure de reproduction.

S'il manque des pages, veuillez communiquer avec l'université qui a conféré le grade.

La qualité d'impression de certaines pages peut laisser à désirer, surtout si les pages originales ont été dactylographiées à l'aide d'un ruban usé ou si l'université nous a fait parvenir une photocopie de qualité inférieure.

La reproduction, même partielle, de cette microforme est soumise à la Loi canadienne sur le droit d'auteur, SRC 1970, c. C-30, et ses amendements subséquents.

**GaAs/AlGaAs HBT MODELLING
AND ITS APPLICATION TO A 14GHz
CLASS A MEDIUM POWER AMPLIFIER**

Somsack Sychaleun

**A Thesis submitted to
the Faculty of Graduate Studies and Research
in partial fulfilment of
the requirements for the degree of**

Master of Electrical Engineering

**Ottawa-Carleton Institute of Electrical Engineering
Department of Electronics
Carleton University
Ottawa, Canada**

January 1996

© Copyright S. Sychaleun 1996

National Library
of Canada

Acquisitions and
Bibliographic Services Branch

395 Wellington Street
Ottawa, Ontario
K1A 0N4

Bibliothèque nationale
du Canada

Direction des acquisitions et
des services bibliographiques

395, rue Wellington
Ottawa (Ontario)
K1A 0N4

Your file Votre référence

Our file Notre référence

The author has granted an irrevocable non-exclusive licence allowing the National Library of Canada to reproduce, loan, distribute or sell copies of his/her thesis by any means and in any form or format, making this thesis available to interested persons.

L'auteur a accordé une licence irrévocable et non exclusive permettant à la Bibliothèque nationale du Canada de reproduire, prêter, distribuer ou vendre des copies de sa thèse de quelque manière et sous quelque forme que ce soit pour mettre des exemplaires de cette thèse à la disposition des personnes intéressées.

The author retains ownership of the copyright in his/her thesis. Neither the thesis nor substantial extracts from it may be printed or otherwise reproduced without his/her permission.

L'auteur conserve la propriété du droit d'auteur qui protège sa thèse. Ni la thèse ni des extraits substantiels de celle-ci ne doivent être imprimés ou autrement reproduits sans son autorisation.

ISBN 0-612-08985-1

Canada

Name SOMSAK SYCHALEUN

Dissertation Abstracts International is arranged by broad, general subject categories. Please select the one subject which most nearly describes the content of your dissertation. Enter the corresponding four-digit code in the spaces provided.

GaAs/AlGaAs HBT Modelling and Its Application to a 14GHz
Class A Medium Power Amplifier SUBJECT TERM

0544
SUBJECT CODE

U·M·I

Subject Categories

THE HUMANITIES AND SOCIAL SCIENCES

COMMUNICATIONS AND THE ARTS
Architecture 0379
Art History 0377
Cinema 0900
Dance 0378
Fine Arts 0357
Information Science 0723
Journalism 0391
Library Science 0399
Mass Communications 0708
Music 0413
Speech Communication 0459
Theater 0465

EDUCATION
General 0515
Administration 0514
Adult and Continuing 0516
Agricultural 0517
Art 0273
Bilingual and Multicultural 0282
Business 0688
Community College 0275
Curriculum and Instruction 0727
Early Childhood 0518
Elementary 0524
Finance 0277
Guidance and Counseling 0519
Health 0680
Higher 0745
History of 0520
Home Economics 0278
Industrial 0521
Language and Literature 0279
Mathematics 0280
Music 0522
Philosophy of 0998
Physical 0523

Psychology 0525
Reading 0535
Religious 0527
Sciences 0714
Secondary 0533
Social Sciences 0534
Sociology of 0340
Special 0529
Teacher Training 0530
Technology 0710
Tests and Measurements 0288
Vocational 0747

LANGUAGE, LITERATURE AND LINGUISTICS

Language
General 0679
Ancient 0289
Linguistics 0290
Modern 0291
Literature
General 0401
Classical 0294
Comparative 0295
Medieval 0297
Modern 0298
African 0316
American 0591
Asian 0305
Canadian (English) 0352
Canadian (French) 0355
English 0593
Germanic 0311
Latin American 0312
Middle Eastern 0315
Romance 0313
Slavic and East European 0314

PHILOSOPHY, RELIGION AND THEOLOGY

Philosophy 0422
Religion
General 0318
Biblical Studies 0321
Clergy 0319
History of 0320
Philosophy of 0322
Theology 0469

SOCIAL SCIENCES

American Studies 0323
Anthropology
Archaeology 0324
Cultural 0326
Physical 0327
Business Administration
General 0310
Accounting 0272
Banking 0770
Management 0454
Marketing 0338
Canadian Studies 0385
Economics
General 0501
Agricultural 0503
Commerce-Business 0505
Finance 0508
History 0509
Labor 0510
Theory 0511
Folklore 0358
Geography 0366
Gerontology 0351
History
General 0578

Ancient 0579
Medieval 0581
Modern 0582
Black 0328
African 0331
Asia, Australia and Oceania 0332
Canadian 0334
European 0335
Latin American 0336
Middle Eastern 0333
United States 0337
History of Science 0585
Law 0398
Political Science
General 0615
International Law and Relations 0616
Public Administration 0617
Recreation 0814
Social Work 0452
Sociology
General 0626
Criminology and Penology 0627
Demography 0938
Ethnic and Racial Studies 0631
Individual and Family Studies 0628
Industrial and Labor Relations 0629
Public and Social Welfare 0630
Social Structure and Development 0700
Theory and Methods 0344
Transportation 0709
Urban and Regional Planning 0999
Women's Studies 0453

THE SCIENCES AND ENGINEERING

BIOLOGICAL SCIENCES

Agriculture
General 0473
Agronomy 0285
Animal Culture and Nutrition 0475
Animal Pathology 0476
Food Science and Technology 0359
Forestry and Wildlife 0478
Plant Culture 0479
Plant Pathology 0480
Plant Physiology 0817
Range Management 0777
Wood Technology 0746

Biology
General 0306
Anatomy 0287
Biostatistics 0308
Botany 0309
Cell 0379
Ecology 0329
Entomology 0353
Genetics 0369
Limnology 0793
Microbiology 0410
Molecular 0307
Neuroscience 0317
Oceanography 0416
Physiology 0433
Radiation 0821
Veterinary Science 0778
Zoology 0472

Biophysics
General 0786
Medical 0760

EARTH SCIENCES

Biogeochemistry 0425
Geochemistry 0996

Geodesy 0370
Geology 0372
Geophysics 0373
Hydrology 0388
Mineralogy 0411
Paleobotany 0345
Paleocology 0426
Paleontology 0418
Paleozoology 0985
Polymology 0427
Physical Geography 0368
Physical Oceanography 0415

HEALTH AND ENVIRONMENTAL SCIENCES

Environmental Sciences 0768
Health Sciences
General 0566
Audiology 0300
Chemotherapy 0992
Dentistry 0567
Education 0350
Hospital Management 0769
Human Development 0758
Immunology 0982
Medicine and Surgery 0564
Mental Health 0347
Nursing 0569
Nutrition 0570
Obstetrics and Gynecology 0380
Occupational Health and Therapy 0354
Ophthalmology 0381
Pathology 0571
Pharmacology 0419
Pharmacy 0572
Physical Therapy 0382
Public Health 0573
Radiology 0574
Recreation 0575

Speech Pathology 0460
Toxicology 0383
Home Economics 0386

PHYSICAL SCIENCES

Pure Sciences
Chemistry
General 0485
Agricultural 0749
Analytical 0486
Biochemistry 0487
Inorganic 0488
Nuclear 0738
Organic 0490
Pharmaceutical 0491
Physical 0494
Polymer 0495
Radiation 0754
Mathematics 0405
Physics
General 0605
Acoustics 0986
Astronomy and Astrophysics 0606
Atmospheric Science 0608
Atomic 0748
Electronics and Electricity 0607
Elementary Particles and High Energy 0798
Fluid and Plasma 0759
Molecular 0609
Nuclear 0610
Optics 0752
Radiation 0756
Solid State 0611
Statistics 0463

Applied Sciences
Applied Mechanics 0346
Computer Science 0984

Engineering
General 0537
Aerospace 0538
Agricultural 0539
Automotive 0540
Biomedical 0541
Chemical 0542
Civil 0543
Electronics and Electrical 0544
Heat and Thermodynamics 0348
Hydraulic 0545
Industrial 0546
Marine 0547
Materials Science 0794
Mechanical 0548
Metallurgy 0743
Mining 0551
Nuclear 0552
Packaging 0549
Petroleum 0765
Sanitary and Municipal 0554
System Science 0790
Geotechnology 0428
Operations Research 0796
Plastics Technology 0795
Textile Technology 0994

PSYCHOLOGY

General 0621
Behavioral 0384
Clinical 0622
Developmental 0620
Experimental 0623
Industrial 0624
Personality 0625
Physiological 0989
Psychobiology 0349
Psychometrics 0632
Social 0451

The undersigned recommend to
the Faculty of Graduate Studies and Research
acceptance of the thesis.

**GaAs/AlGaAs HBT MODELLING
AND ITS APPLICATION TO A 14GHz
CLASS A MEDIUM POWER AMPLIFIER**

submitted by

Somsack Sychaleun, B.Eng.

in partial fulfilment of the requirements for the degree of

Master of Electrical Engineering

Thesis Supervisor

Thesis Co-Supervisor

Chair, Department of Electronics

Carleton University

January 1996

Abstract

The increasing demand for high-performance microwave circuits has led to the need for better performance transistors. With the recent advance in high-precision epitaxial growth systems, developments in heterojunction bipolar transistor (HBT) technology show that it possesses a number of performance advantages for both high-speed digital and analog circuit applications. For microwave applications, HBT combines the strengths of the Si BJT and GaAs FET. High power density and low $1/f$ noise characteristics make HBT suitable for microwave power amplifiers and for low phase-noise oscillators.

This thesis presents large-signal modelling of the Rockwell $360\mu\text{m}^2$ HBT as well as the design and performance of a 14.0GHz, class A, HBT medium power amplifier. The proposed model is based on the modified Gummel-Poon topology and its parameters are extracted through the fitting of the model responses to various DC and multiple bias S -parameters measurements. Load-pull simulation technique is employed in the design of the amplifier in order to achieve optimum output power. The amplifier circuit offers 7.4dB small-signal gain, 16.4dBm output power and 30% power added efficiency at 13.5GHz.

Acknowledgements

I would like to express my sincere gratitude to Professor Jim Wight, my thesis supervisor, for his continuous encouragement and support throughout my graduate studies at Carleton University.

I would like to thank Dr. Malcolm G. Stubbs, Mr. Michel Cuhaci and Mr. René Douville of the Communications Research Centre (CRC) for providing me the opportunity to carry out this research.

I would also like to thank the staff of the CRC for their technical assistance. Special thanks to Mr. Hien Do-Ky for his valuable guidance and support throughout this work.

I wish to thank my parents for their support throughout my academic career. Finally, I would like to thank Ms. Khai-Loi Nhan for her continuous encouragement, tolerance and support throughout the course of this thesis.

Table of Contents

	Page
Acceptance Sheet	ii
Abstract	iii
Acknowledgements	iv
Table of Contents	v
List of Tables	viii
List of Figures	ix
List of Symbols	xiii
 CHAPTER 1: Introduction	 1
1.1 Introduction	1
1.2 Thesis Objectives	3
1.3 Thesis Organization	4
 CHAPTER 2: Amplifier Design Theory	 7
2.1 Introduction	7
2.2 Microwave Power Amplifier	8
2.2.1 Class A Amplification	8
2.2.2 Class B Amplification	13
2.2.3 Class AB Amplification	17
2.2.4 Summary	22
2.3 Amplifier Design Techniques	24
2.3.1 Non-linear Computer-Aided Design	24
2.3.2 Load-Pull Technique	27
 CHAPTER 3: Device Modelling	 31
3.1 Introduction	31
3.2 Heterojunction Bipolar Transistor (HBT)	32
3.2.1 HBT Brief History	32
3.2.2 HBT Principle	32
3.2.3 HBT Fabrication	35
3.2.4 HBT Common Characteristics	38

3.3	Modified Gummel-Poon Model	43
3.3.1	The Intrinsic Device Model	44
3.3.2	The Extrinsic Parasitics	49
3.3.3	The Thermal Sub-circuit	59
3.4	Parameter Extractions	54
3.4.1	Intrinsic Device Model Parameter Extractions	54
3.4.2	Extrinsic Parasitics Parameter Extractions	61
3.4.3	Thermal Sub-circuit Parameter Extractions	62
3.5	Optimization Process and modelling Results	66
3.5.1	DC Optimization	67
3.5.2	Small-Signal AC Optimization	70
3.5.3	Small-Signal to Large-Signal Conversion	74
3.5.4	Large-signal Model Verification	79
3.6	Summary	81
CHAPTER 4:	Power Amplifier Design	83
4.1	Introduction	83
4.2	Circuit Fabrication Technology	84
4.3	Amplifier Design	85
4.4	Matching Network Design	90
4.4.1	Input Matching Network	91
4.4.2	Output Matching Network	93
4.5	Bias Network Design	95
4.6	Network Integration and Design Iterations	98
4.7	Summary	103
CHAPTER 5:	Amplifier Results and Discussions	105
5.1	Introduction	105
5.2	Amplifier Biasing	106
5.3	Small-signal S-parameters Response	109

5.4	Output Power and Gain Characteristics	118
5.5	Third-Order Intermodulation Product	124
5.6	Power Added Efficiency	126
5.7	Summary	128
CHAPTER 6: Conclusions		129
6.1	Summary	129
6.2	Future Work	131
APPENDIX I: Derivation of DC Component for Class AB Waveform		133
APPENDIX II: Derivation of Fundamental Component for Class AB Waveform		135
APPENDIX III: OSA90/Hope™ Circuit File Listing of the Load-Pull Simulation		137
APPENDIX IV: OSA90/Hope™ Circuit File Listing of the HBT Amplifier		144
REFERENCES		151

List of Tables

Table	Description	Page
3.1	Model Parameters of the Modified Gummel-Poon Model	53
3.2	Parameter Values Extracted from Gummel Plots	58
3.3	The Extracted Slopes and Y-intercepts for Data in Figure 3.17	64
3.4	The Extracted Slopes and Y-intercepts for Data in Figure 3.18	66
3.5	The Optimized Parameter Values Resulted from DC Optimization	70
3.6	The Optimized Extrinsic Parasitics Values	71
3.7	The Optimized Parameters for the Non-linear Capacitances	74

List of Figures

Figure	Description	Page
2.1	Collector Current Waveforms for (a) Class A (b) Class AB (c) Class B (d) Class C Power Amplifier	8
2.2	Simplified Power Amplifier Circuit for Class A,B and AB	9
2.3	The Operation of Class A Amplifier	10
2.4	The Operation of Class B Power Amplifier	14
2.5	The Operation of Class AB Power Amplifier	17
2.6	General Collector Current Time Domain Waveform	18
2.7	Normalized DC and Fundamental Amplitudes of Collector Current versus the bias ratio x for Class AB Operation	21
2.8	A Basic Setup for Load-Pull Measurement System	28
2.9	Typical Output Power Contours as a Function of Load Impedance	29
3.1	Typical Band Diagrams of (a) a BJT and (b) an HBT Under Forward Bias	33
3.2	The Typical Schematic Cross Section of an AlGaAs/GaAs HBT	36
3.3	Bandgap Energy versus Lattice Constant for Some III-V Compounds	37
3.4	Physical Structure of the $360\mu\text{m}^2$ AlGaAs/GaAs HBT	38
3.5	I_C versus V_{CE} Characteristic of Rockwell $360\mu\text{m}^2$ HBT	39
3.6	Forward and Reverse Gummel-Plots for Rockwell $360\mu\text{m}^2$ HBT	39
3.7a	Measured S_{11} , S_{12} and S_{22} for Rockwell $360\mu\text{m}^2$ HBT ($I_B = 1.5\text{mA}$ $V_{CE} = 3.0\text{V}$)	42
3.7b	Measured S_{21} for Rockwell $360\mu\text{m}^2$ HBT ($I_B = 1.5\text{mA}$ $V_{CE} = 3.0\text{V}$)	43

3.8	The Intrinsic Modified Gummel-Poon Model for HBT	44
3.9	The Extrinsic Parasitic Model	50
3.10	The Thermal Sub-Circuit	51
3.11	The Complete Modified Gummel-Poon Model as Proposed	52
3.12	Parameter Extractions from Forward Gummel Plot	56
3.13	Parameter Extractions from Reverse Gummel Plot	57
3.14	Plot of Z_{12} versus $1/I_E$ for R_E Extraction	59
3.15	Plot of Real Part of Z_b versus Frequency for Extraction of R_B	60
3.16	Plot of Imaginary Part of Z_b versus Frequency for Extraction of L_B	60
3.17	The Plot of I_C versus P_{diss} at Different T_{base}	64
3.18	The Plot of I_C versus T_{base} at Different P_{diss}	65
3.19	The Simulated and Measured I_C versus V_{CE} Characteristics	68
3.20	The Simulated and Measured V_{BE} versus V_{CE} Characteristics	68
3.21	The Simulated versus Measured Forward Gummel Plot	69
3.22	The Simulated versus Measured Reverse Gummel Plot	69
3.23	The Bias Dependent Characteristics of C_{BE}	72
3.24	The Bias Dependent Characteristics of C_{BC}	73
3.25	The Bias Dependent Characteristics of delay τ	73
3.26	The Simulated versus Measured S-parameters at $I_B = 0.5\text{mA}$, $V_{CE} = 4.0\text{V}$	76
3.27	The Simulated versus Measured S-parameters at $I_B = 1.5\text{mA}$, $V_{CE} = 3.0\text{V}$	77
3.28	The Simulated versus Measured S-parameters at $I_B = 2.5\text{mA}$, $V_{CE} = 2.0\text{V}$	78

3.29	Simulated and Measured P_{out} versus P_{in} Characteristics of $360\mu\text{m}^2$ HBT	80
3.30	The Measured Active Load-Pull Contours of $360\mu\text{m}^2$ HBT	81
4.1	The Circuit Diagram of a Microwave Amplifier	83
4.2	The Q Point for Class A Power Amplifier	86
4.3	The Load-Pull Simulation Result (Input Power = 7.0dBm @ 14.0GHz)	89
4.4	Input Double Stubs Matching on the Smith Chart	92
4.5	Optimized Dimensions of the Input Matching Network	93
4.6	Output Single Stubs Matching on the Smith Chart	94
4.7	Optimized Dimensions of the Output Matching Network	95
4.8	The Structure of the Ideal Biasing Network	96
4.9	The Quarter-Wave Sections Biasing Network	96
4.10	The Physical Dimensions of the Biasing Network	97
4.11	The Frequency Response of the Biasing Network	98
4.12	The Simulated S-parameters of the Power Amplifier	99
4.13	The Stability Factor of the Amplifier	100
4.14	The S-parameter of the Third Iteration Design Amplifier	102
4.15	The K Factor of the Third Iteration Design Amplifier	102
4.16	The Final Dimensions of the HBT Power Amplifier	103
4.17	The Physical Layout of the Amplifier Circuit	104
5.1	Mounting of the Amplifier onto the Universal Test Fixture	106
5.2	Measured HBT I_C versus V_{CE} Characteristic on the Amplifier Circuit	107

5.3	HBT I_C versus V_{CE} Characteristic with Ferrite Beads and External Bias Tee	108
5.4	The Experimental Setup for Amplifier S -parameters Measurement	110
5.5a	Simulated and Measured $ S_{11} $ of the Amplifier	111
5.5b	Simulated and Measured $ S_{21} $ of the Amplifier	111
5.5c	Simulated and Measured $ S_{21} $ of the Amplifier in Narrow Band	112
5.5d	Simulated and Measured $ S_{12} $ of the Amplifier	112
5.5e	Simulated and Measured $ S_{22} $ of the Amplifier	113
5.6a	Corrected and Measured $ S_{11} $ of the Amplifier	116
5.6b	Corrected and Measured $ S_{21} $ of the Amplifier	116
5.6c	Corrected and Measured $ S_{12} $ of the Amplifier	117
5.6d	Corrected and Measured $ S_{22} $ of the Amplifier	117
5.7	The Experimental Setup for Output Power Characteristics Measurement	119
5.8	Output Power versus Input Power Characteristics	120
5.9	Power Gain versus Input Power Level	121
5.10	Simulated Time Domain Output Voltage Waveforms at Different Input Power Levels	122
5.11	The Output Power Spectrum Content of the HBT Amplifier	123
5.12	Experimental Setup for Intermodulation Product Measurement	124
5.13	A Typical Intermodulation Product Measurement Result	125
5.14	Intermodulation Product versus Input Power Level	126
5.15	Power Added Efficiency versus Input Power Level	127

List of Symbols

°	degree
Å	angstrom
A/D	analog to digital
AC	alternating current
AlGaAs	aluminum gallium arsenate
β	transistor current gain
BJT	bipolar junction transistor
CAD	computer aided design
D.U.T.	device under test
D/A	digital to analog
dB	decibel
dBc	decibel relative to carrier level
DC	direct current
E_g	Energy gap
ϵ_r	relative dielectric constant
eV	electron volt
f	frequency
FET	field effect transistor
$f_{\max}$	maximum oscillation frequency
f_0	fundamental frequency
f_c	cutoff frequency

G	power gain
γ	emitter injection efficiency
Γ	reflection coefficient
GaAs	gallium arsenate
GaInAs	gallium indium arsenate
GBits/s	giga-bits per second
GHz	giga-Hertz
η	collector efficiency
HB Γ	heterojunction bipolar transistor
HEMT	high electron mobility transistor
Hz	Hertz
InP	indium phosphate
j_n	electron current density
j_p	hole current density
K	Boltzmann's constant
K	stability factor
kHz	kilo-Hertz
λ	wave length
mA	mili-ampere
MBE	molecular beam epitaxy
MIC	microwave integrated circuit
μm	micro-metre
MOCVD	metal organic chemical vapor deposition

mW	mili-watt
nH	nano-Henry
<i>n_i</i>	intrinsic carrier density
<i>P_{1dB}</i>	first order compression point
<i>P_{3dB}</i>	Third order intercept point
<i>PAE</i>	power added efficiency
pF	pico-Farad
Q	quality factor
RF	radio frequency
SCR	space charge region
Si	silicon
SiGe	silicon germanium
<i>T</i>	temperature
tanδ	dielectric loss tangent
TRL	through-reflect-line
V	volt
VCO	voltage controlled oscillator
VSWR	voltage standing wave ratio
W	watt
x	bias ratio
ω	angular frequency
Ω	ohm
Ωm	ohm metre

CHAPTER 1: INTRODUCTION

1.1 Introduction

Heterojunction bipolar transistors (HBTs) have gained an important role in both high speed digital and microwave analog circuit applications in recent years due to their superior performance relative to BJTs, FETs and HEMTs [1, 2]. Compared to its predecessor Si BJTs, HBT offers higher frequency of operation and is often known as the high frequency version of the Si BJT. Due to its structural similarity to BJTs, current is conducted vertically which results in higher power handling capability compared to the lateral current flow devices, such as FETs and HEMTs. In addition, carrier flow in HBTs is isolated from the surface and the substrate-interface; thus, trapping effects are reduced and low $1/f$ noise properties result. Furthermore, HBTs offer higher transconductance, efficiency and gain. In short, HBTs combine the strength of the Si BJT and GaAs FET for microwave applications. This makes them suitable candidate for high performance microwave circuits in the future.

In addition to the above advantages, HBT technology is also more cost effective. Again, because its current flows vertically, the cross sectional active area is more compact than the FETs and HEMTs for the same order of power density. This results in a potential saving of the substrate real estate which is still an expensive factor today. Furthermore, HBTs do not require complex electron-beam lithography (used for FET and HEMTs processing) in defining its active area [3]. These make HBTs more attractive in the current competitive market.

Essentially, an HBT is a BJT with a wider band-gap energy at the emitter

side. The different energy gap in the emitter-base junction gives rise to the name heterojunction and its superior performance [4]. The junction is usually formed by two different materials with different band gap energies and closely matched lattice constants. AlGaAs/GaAs, InP/GaInAs and SiGe/Si HBTs have been successfully processed and reported, with AlGaAs/GaAs HBTs being the most mature. As an example, AlGaAs/GaAs HBTs consist of AlGaAs material in the emitter area while the base and collector regions are made of GaAs. In order to achieve the construction of a heterojunction, a sophisticated device growth technique is needed.

With the recent advances in high-precision epitaxial growth systems for III-V compounds such as molecular beam epitaxy (MBE) and metal organic chemical vapor deposition (MOCVD) technology, highly improved experimental HBTs are made possible [5]. These techniques allow deposition of AlGaAs material onto a GaAs substrate (for an AlGaAs/GaAs HBT) layer by layer; nearly on an atomic scale. As a result, both the composition and the doping density can be precisely controlled. Also, the recent self-aligned technique [6], which minimizes the lateral distances between device terminals (typically $0.2\mu\text{m}$ apart), further reduces the unwanted surface recombinations and parasitics effects. With these, HBTs with f_t and f_{max} of 100~200GHz have been reported [1].

Over the years, many HBT digital and analog circuits have been demonstrated [1, 2]. In particular, A/D and D/A converters, phase detector, sampling and hold circuits and voltage comparators have been developed for GBits/s digital applications. For microwave analog circuits, high performance power amplifiers, wide-band amplifiers, low noise oscillators and VCO's using HBTs have been achieved. For

example, a two stage power amplifier having an output power of 12.5W with 10.8dB gain and 36% *PAE* has been achieved at X band [7]. In fact, HBT amplifiers currently hold the record for the highest power output for a single chip at X band. Phase noises of -76dBc/Hz and -102dBc/Hz are obtained at 10 and 100kHz from the carrier frequency for a dielectric resonator oscillator at 11.06GHz [8]. These values are about 10dB better than those of FET oscillators.

One of the most important application of HBTs is in microwave power amplifiers. These amplifiers are important in the transmitting chain of radar, communication and electronic warfare systems where higher output power and efficiency are in constant demand. HBT power amplifiers are most often designed in Class A, AB and B mode of operation although it has been shown to have advantages also in Class C. In particular, Class A amplifiers offer the highest output power and linearity but have the lowest efficiency among the classes. With output power being the important parameter for microwave systems, efficiency is usually traded off making the Class A power amplifier the most important.

1.2 Thesis Objectives

The first objective of this work is to develop a non-linear HBT model for non-linear microwave circuit applications. An accurate non-linear (large-signal) device model is essential in the design of non-linear circuits such as power amplifiers, oscillators and mixers because of the non-linear nature of these circuits. Here, a lumped-element, user-defined HBT model is investigated and the model is incorporated in the CAD design

tool OSA90/HopeTM for future design purposes. The model accurately predicts DC characteristics, multiple bias small-signal S-parameters and large-signal responses.

The second objective is to design an amplifier to gain experience with microwave integrated circuit (MIC) applications using an HBT and at the same time to further examine the validity of the model developed. Specifically, a 14.0GHz Class A HBT power amplifier is designed and demonstrated. The amplifier design is based entirely on the CAD tool utilizing the HBT model obtained earlier. Upon completion, the performance of the amplifier circuit is measured and compared with the simulation.

1.3 Thesis Organization

This thesis consists of six chapters. Chapter 1 is this introduction. Chapter 2 provides the background theory on the operation of various classes of power amplifiers and their design techniques. Among all classes of power amplifiers, the most common and suitable for microwave applications are class A, B and AB, and these are discussed at length. There are mainly two design techniques for power amplifiers. One is the non-linear CAD design technique which obtains the initial design based on power amplifier theory, and the optimum design through CAD tool optimization. This technique therefore relies on the accuracy of the device model and computer simulations during the designing process. On the other hand, the second technique is the load-pull measurement technique which obtains the optimum design parameters based mainly on measurements.

In Chapter 3, the circuit modelling of the $360\mu\text{m}^2$ power HBT is

described. An HBT model topology is first selected from the literature along with the equations describing it. For this model 36 parameters are involved and are extracted in 2 stages. The parameters that influence the DC responses are first extracted and optimized against various DC measurements. Then, the parameters that affect the AC responses are extracted and also optimized against *S*-parameters at several DC biases. Finally, by converting the bias dependent parameters to their related large signal parameters, a true non-linear HBT model which is capable of predicting DC and AC performance simultaneously with acceptable accuracy is obtained.

Chapter 4 describes the design procedures of a power amplifier. The amplifier is to operate at 14.0GHz with reasonable gain and maximum output power. Requirements regarding bandwidth and power added efficiency are of only secondary concern. The design technique used is the combination of the non-linear CAD technique and the load-pull technique. That is, using the large signal HBT model, load-pull simulations are performed to obtain the optimum source and load impedance required for the device maximum output power. The input and output matching networks, as well as the biasing network, are then designed from the impedances obtained from the simulated load-pull result.

Amplifier measurements and a discussion are given in Chapter 5. After the DC operating point of the amplifier was made stable, the small signal *S*-parameters of the amplifier are measured and compared with the simulation. The discrepancies are discussed and corrections made. Large-signal measurements such as the output power versus input power characteristic, intermodulation product levels, and power added efficiency are also measured and discussed.

The final chapter, Chapter 6, concludes on the overall work done on both the HBT modelling exercise and the power amplifier performance. Further improvements in device modelling, circuit design and measurement techniques are suggested for future work.

CHAPTER 2: AMPLIFIER DESIGN THEORY

2.1 Introduction

This chapter discusses the basic theory behind microwave power amplifiers. In general, power amplifiers are classified in class A, B, AB, or C according to the conduction angle of the transistor output current waveform. Figure 2.1 illustrates the classification of power amplifiers according to the conduction angles. By definition, in a class A power amplifier the amplifying device conducts at all times or equivalently, the conduction angle is 360° . In a class AB power amplifier, the transistor conducts between 180° to 360° while for class B, the transistor conducts 180° or half of the signal cycle. Finally, a class C power amplifier conducts less than 180° . Among the classes, class A, B, and AB power amplifiers are the most common in the current microwave industry due to their relative ease in realization. A discussion of these power amplifiers will be given in detail in this chapter. The operation of a class C power amplifier requires a very high gain transistor which is not commonly found at microwave frequencies, and therefore, will not be discussed. Also, other power amplifiers operated in class D, E, F, G, H and S, which make use of either the circuit topology or mode of operation or both to achieve high efficiency [9], will not be discussed either.

Various power amplifier design techniques are discussed also in this chapter. In general, the main task involved in power amplifier design is to find the appropriate input and output matchings for a transistor to satisfy certain specifications. This is similar to the small-signal amplifier design to a certain degree. However, the difficulties are transistor characteristics become non-linear with increasing input drive

level. Consequently, conjugate matching using small-signal S -parameters technique is no longer valid for power amplifier design. Also, because of its complex nature, the theory behind power amplifier design is not well developed. This makes the design of a power amplifier more challenging and time consuming.

Figure 2.1 Collector current waveforms for (a) class A (b) class AB (c) class B (d) class C power amplifier

2.2 Microwave Power Amplifier

2.2.1 Class A Amplification

Figure 2.2 shows a simplified microwave power amplifier circuit. This basic amplifier circuit applies to Class A, B, and AB power amplifiers although the parallel resonant circuit is not necessary for class A operation. It is usually added at the

output of Class B and AB amplifiers to suppress the higher harmonics. Here, the RF chokes are assumed to present infinite impedances while the DC blocking capacitors are designed as short circuits near the frequency of interest. Furthermore, in the following analysis, the bipolar transistor is assumed to have infinite input and output impedances and its idealized DC-IV characteristic is similar to that shown in Figure 2.3. The analysis below (section 2.2.1 to 2.2.2) is based on the method used by Walker [10].

Figure 2.2 Simplified power amplifier circuit for class A, B and AB

The operation of class A amplifier can be explained with the aid of figure 2.3. In an ideal class A operation, the transistor is DC biased at a voltage V_{CEQ} which is the middle of V_K and $V_{CE,MAX}$ (i.e. $(V_K + V_{CE,MAX})/2$) and at a current I_{CQ} at the middle of the DC-IV curves (i.e. $I_{C,MAX}/2$) as shown by the Q point. Here, V_K is the knee voltage while $V_{CE,MAX}$ and $I_{C,MAX}$ are the breakdown voltage and current. Then, with a sinusoidal signal input, the signal is amplified (according to RF gain of the transistor) and appears as the collector (output) current waveform $i_c(t)$ as shown. The load line defines the load resistance R_L and the swing of collector current along the load line results in the swing of the output voltage waveform $v_{ce}(t)$. It must be noted that the output current and voltage

waveforms are 180° out of phase.

Figure 2.3 The operation of class A amplifier

As seen in the time voltage and current waveforms above, the transistor is conducting at all times, thus, the conduction angle of the transistor is 360°. The maximum output power prior to saturation occurs when the output signal fully swings along the load line on both axes. Therefore the maximum linear RF output power, with the peak voltage and current assuming their greatest values, is given by equation (2.1)

$$P_{RF,MAX} = \frac{v_{ce,peak,max} \cdot i_{c,peak,max}}{2} \quad (2.1)$$

From Figure 2.3

$$v_{ce,peak,max} = \frac{V_{CE,MAX} - V_K}{2} \quad (2.2)$$

and

$$i_{c,peak,max} = \frac{I_{C,MAX}}{2} \quad (2.3)$$

thus equation (2.1) becomes:

$$P_{RF,MAX} = \frac{1}{8} \cdot I_{C,MAX} \cdot (V_{CE,MAX} - V_K) \quad (2.4)$$

The above expression is the maximum linear RF output power that can be achieved in class A operation. As a numerical example, a transistor with $I_{C,MAX}$ of 100mA, $V_{CE,MAX}$ of 5V and V_K of 1V gives a maximum linear RF power output of 50mW or 17dBm. In order to achieve maximum output power, $I_{C,MAX}$ and $V_{CE,MAX}$ of the transistor must be maximized while V_K is minimized.

One other important parameter for a power amplifier is the efficiency. The collector efficiency, by definition, is given by:

$$\eta = \frac{P_{RF}}{P_{DC}} \cdot 100\% \quad (2.5)$$

where P_{RF} is the RF output power and P_{DC} is the DC power in watts dissipated by the transistor and is given by:

$$P_{DC} = I_{BQ} \cdot V_{BEQ} + I_{CQ} \cdot V_{CEQ} \cong I_{CQ} \cdot V_{CEQ} \quad (2.6)$$

where
$$I_{CQ} = \frac{I_{C,MAX}}{2} \quad (2.7)$$

and
$$V_{CEQ} = \frac{V_{CE,MAX} + V_K}{2} \quad (2.8)$$

for class A operation. Here, it is assumed that $I_{CQ} \cdot V_{CEQ} \gg I_{BQ} \cdot V_{BEQ}$. Substituting equation (2.7) and (2.8) into (2.6), equation (2.9) is obtained as follows:

$$P_{DC} = \frac{1}{4} \cdot I_{C,MAX} \cdot (V_{CE,MAX} + V_K) \quad (2.9)$$

From equation (2.5), since P_{DC} does not change with input drive level, the maximum collector efficiency occurs when P_{RF} is maximum. Thus by substituting

equation (2.4) and (2.9) into equation (2.5), the maximum collector efficiency is found to

$$\eta_{MAX} = \frac{1}{2} \cdot \frac{(V_{CE,MAX} - V_K)}{(V_{CE,MAX} + V_K)} \cdot 100\% \quad (2.10)$$

Using the numerical example cited on page 11, the maximum collector efficiency, η_{MAX} , at maximum linear output power is 33%. This is different from the result obtained from conventional analysis of 50% maximum collector efficiency [11] for class A amplifier when the knee voltage V_K is not taken into account. Note that in equation (2.10) when V_K is 0, the result agrees with the conventional analysis.

While collector efficiency is a simple measure of amplifier efficiency, a more commonly used figure of merit is power added efficiency *PAE*. It is defined as:

$$PAE \equiv \frac{P_{RF} - P_{IN}}{P_{DC}} = \left(1 - \frac{1}{G}\right) \cdot \frac{P_{RF}}{P_{DC}} \cdot 100\% \quad (2.11)$$

where G is the power gain of the amplifier on a linear scale. *PAE* is widely used to prevent optimistic evaluation of low gain amplifiers in which a significant fraction of the output comes from the input power. It can be seen from the above equation that when the device gain is high, *PAE* approaches the collector efficiency η . Once again for class A operation, P_{RF} and P_{DC} were found earlier as in equation (2.4) and (2.9) respectively and the *PAE* becomes

$$PAE = \frac{1}{2} \cdot \left(1 - \frac{1}{G}\right) \cdot \frac{(V_{CE,MAX} - V_K)}{(V_{CE,MAX} + V_K)} \cdot 100\% \quad (2.12)$$

Using the same numerical example and a typical amplifier gain of 10 (linear scale), the maximum power added efficiency at maximum linear output power is now 30%.

The optimum load resistance R_L is the reciprocal of the slope of the load

line from figure 2.3 and is given by:

$$R_L = \frac{V_{ce,peak,max}}{i_{c,peak,max}} \quad (2.13)$$

or

$$R_L = \frac{V_{CE,MAX} - V_K}{I_{C,MAX}} \quad (2.14)$$

when equations (2.2) and (2.3) are used. The value for the optimum load resistance R_L is 40Ω for the numerical example employed in this section. This optimum load resistance can be quite different from the value that is needed for a good impedance match and may yield poor output VSWR.

2.2.2 Class B Amplification

Figure 2.4 shows the operation of class B amplification. Here, the transistor is biased at the same voltage as that of class A operation, namely, V_{CEQ} of $(V_K + V_{CE,MAX})/2$ but with no collector current (i.e. $I_{CQ} = 0$) as shown by the Q point. With a sinusoidal input, only the positive cycle of the input signal is amplified according to the gain of the transistor. On the negative cycle, the transistor is not able to provide negative collector current as depicted by the $DC-IV$ characteristic, thus the output current is zero. This results in a half sinewave collector current since the transistor is turned on only half of the signal cycle. The conduction angle is thus only 180° . The voltage waveform, however, still swings fully between V_K and $V_{CE,MAX}$ as before. Note that in the case of class B amplification, the load line consists of two segments and the optimum load impedance is no longer given by the slope of the load line as shown in figure 2.4.

Figure 2.4 The operation of class B power amplifier

Due to the half sinewave nature of the collector current and from Fourier Transform theory, class B operation produces high levels of harmonics and as a result, a parallel tuned circuit is usually added at the output as shown in figure 2.2. Ideally, the resonant circuit behaves as a short circuit for all higher harmonics, leaving only the fundamental component to be dissipated in the load R_L . The collector current waveform in class B operation can be expressed mathematically as:

$$i_c(t) = \begin{cases} i_{c,peak} \cdot \sin(\omega t) & 0 < t \leq T/2 \\ 0 & T/2 < t \leq T \end{cases} \quad (2.15)$$

where T is the signal period and is equal to $2\pi/\omega$. From Fourier analysis, the above half-sine waveform with an amplitude of $i_{c,peak}$ is expanded into the following series:

$$i_c(t) = i_{c,peak} \cdot \left(\frac{1}{\pi} + \frac{1}{2} \sin(\omega t) - \frac{2}{\pi} \sum_{n=2,4,\dots}^{\infty} \frac{1}{n^2 - 1} \cos(n\omega t) \right) \quad (2.16)$$

The amplitudes of the DC and fundamental components are $i_{c,peak}/\pi$ and $i_{c,peak}/2$ respectively. The implication of the above result is that with an RF input, the DC operating point is changed to a non-zero current which is a function of RF output power. Also, the waveform consists of only the even order harmonics, and further, it can be seen that a class B amplifier always generates harmonics even when operating in its linear region. Also, the level of the second harmonic is only 7.4dB below the fundamental and for that, an output parallel tuned circuit is usually needed. With the amplitude of the fundamental current component being $i_{c,peak}/2$, the maximum RF output power is therefore given by:

$$P_{RF,MAX} = \frac{v_{ce,peak,max} \cdot i_{c,peak,max} / 2}{2} \quad (2.17)$$

where $v_{ce,peak,max}$ is again given by equation (2.2), and from figure 2.4

$$i_{c,peak,max} = I_{C,MAX} \quad (2.18)$$

Substituting equation (2.2) and (2.18) into (2.17) gives:

$$P_{RF,MAX} = \frac{1}{8} \cdot I_{C,MAX} \cdot (V_{CE,MAX} - V_K) \quad (2.19)$$

This is the expression for maximum RF linear output power for class B operation. It is identical to class A result (equation 2.4) since the effective fundamental peak current amplitude in class B is still the same as that of class A.

As has been shown earlier, the DC power dissipated in the transistor for class B operation results from the input drive. When there is no signal present at the input, the transistor dissipates no power (i.e. $I_{CQ} = 0$). On the other hand, with an input signal that results in the maximum RF output power, the maximum collector DC current

becomes:

$$I_{CQ} = \frac{i_{c,peak,max}}{\pi} = \frac{I_{C,MAX}}{\pi} \quad (2.20)$$

and the DC voltage is the same as in equation (2.8). This result in a DC power of

$$P_{DC} = \frac{1}{2 \cdot \pi} \cdot I_{C,MAX} \cdot (V_{CE,MAX} + V_K) \quad (2.21)$$

dissipating in the transistor. The collector efficiency is then given by

$$\eta_{MAX} = \frac{\pi}{4} \cdot \frac{(V_{CE,MAX} - V_K)}{(V_{CE,MAX} + V_K)} \cdot 100\% \quad (2.22)$$

With the same numerical values used for class A, the maximum collector efficiency for class B operation is 52.4% which is much higher than class A result. Again if V_K is 0, the conventional result of 78.5% or $\pi/4$ is obtained. Accordingly, the power added efficiency is given by

$$PAE = \frac{\pi}{4} \cdot \left(1 - \frac{1}{G}\right) \cdot \frac{(V_{CE,MAX} - V_K)}{(V_{CE,MAX} + V_K)} \cdot 100\% \quad (2.23)$$

Assuming the device gain of 10, the power added efficiency PAE has a value of 47.1%.

The optimum load resistance R_L in class B operation cannot be obtained from the slope of the load line. Yet, it can be calculated from the peak voltage and current at the output as:

$$R_L = \frac{v_{ce,peak,max}}{i_{c,peak,max}/2} \quad (2.24)$$

Substituting equation (2.2) and (2.18) into (2.24) gets:

$$R_L = \frac{V_{CE,MAX} - V_K}{I_{C,MAX}} \quad (2.25)$$

which again is similar to class A operation as depicted in reference [12]. Basically, class

B operation results in an effective load line that is different from the conventional one due to the increase in the DC current from the input drive.

2.2.3 Class AB Amplification

The operation of class AB amplification is shown in figure 2.5. The DC collector voltage bias of the transistor is the same as in class A and B, namely, V_{CEQ} of $(V_K + V_{CE,MAX})/2$ while the DC collector current bias falls somewhere between class A and B (i.e. between 0 and $I_{C,MAX}/2$) and is usually expressed as ratio or percentage of maximum collector current (i.e. $x \cdot I_{C,MAX}$) where x is the bias ratio and is defined as $I_{C,Q}/I_{C,MAX}$. Consequently, the limit of x lies between 0 to 0.5, with $x=0$ results in pure class B operation and $x=0.5$ results in class A operation. In figure 2.5, 25% of $I_{C,MAX}$ (or $x=0.25$) collector current bias is used for illustration.

Figure 2.5 The operation of class AB power amplifier

With a sinusoidal input, the signal is amplified according to the gain of the transistor and appears as $i_c(t)$ at the collector side. Before reaching the cutoff region of the transistor, the signal is amplified in a fashion similar to that of class A operation. However, during a portion of the negative cycle when the output reached the cutoff region of the transistor, zero current results. Afterward, the amplification action is back to normal. The result is that collector current waveform takes the shape of a raised sinewave with part of the negative cycle chopped off as shown.

In order to derive the theoretical maximum linear output power and efficiency for class AB operation, a more general case of collector current time waveform is examined in figure 2.6. Here, the upper current limit is $I_{C,MAX}$ and the current bias is, in general, $x \cdot I_{C,MAX}$. Furthermore, the waveform is periodic over the interval $(-T/2, T/2)$ and has zero value in the intervals $(-T/2, -t_0)$ and $(t_0, T/2)$.

Figure 2.6 General collector current time domain waveform

The collector current waveform above can be expressed mathematically as a function of time as:

$$i_c(t) = \begin{cases} 0 & -T/2 \leq t < -t_o \\ x \cdot I_{C,MAX} + I_{C,PEAK} \cdot \cos(\omega t) & -t_o \leq t < t_o \\ 0 & t_o \leq t < T/2 \end{cases} \quad (2.26)$$

where $I_{C,PEAK}$ is $(I_{C,MAX} - x \cdot I_{C,MAX})$ or $(1-x) \cdot I_{C,MAX}$. Expression for t_o in terms of x is found as follows:

$$x \cdot I_{C,MAX} + (1-x) \cdot I_{C,MAX} \cdot \cos(\omega t) = 0 \quad (2.27)$$

The above equation yield:

$$t = \pm \frac{\cos^{-1}\left(-\frac{x}{1-x}\right)}{\omega} \quad (2.28)$$

where the positive solution corresponds to t_o and the negative term corresponds to $-t_o$.

The DC component I_{CQ} can be found from the average value of Fourier series expansion of $i_c(t)$.

$$I_{CQ} = \frac{1}{T} \cdot \int_{-\frac{T}{2}}^{\frac{T}{2}} x \cdot I_{C,MAX} + (1-x) \cdot I_{C,MAX} \cdot \cos(\omega t) dt \quad (2.29)$$

where T is the period of the signal and is equal to $2\pi/\omega$. Since $i_c(t)$ is zero outside the interval $(-t_o, t_o)$, and using equation (2.28), the above integral becomes

$$I_{CQ} = \frac{\omega}{2\pi} \cdot \int_{-\frac{\cos^{-1}\left(-\frac{x}{1-x}\right)}{\omega}}^{\frac{\cos^{-1}\left(-\frac{x}{1-x}\right)}{\omega}} x \cdot I_{C,MAX} + (1-x) \cdot I_{C,MAX} \cdot \cos(\omega t) dt \quad (2.30)$$

and finally, I_{CQ} is found to be:

$$I_{CQ} = \frac{I_{C,MAX}}{\pi} \cdot \left[\sqrt{1-2x} + x \cdot \cos^{-1}\left(-\frac{x}{1-x}\right) \right] \quad (2.31)$$

The details of the above calculation are shown in Appendix I. The above result is the general expression of the DC component of the collector current for class AB, although it also applies to class A and B as well. As verification, when x equals to 0.5, equation (2.31) gives $I_{CQ} = 0.5 \cdot I_{C,MAX}$ which is precisely the result for class A operation. For class B operation, x has a value of 0 and equation (2.31) results in $I_{C,MAX}/\pi$ as expected from equation (2.20).

The fundamental f_o component of $i_c(t)$ is needed in order to calculate the maximum output power. The higher harmonics such as $2f_o, 3f_o, \dots$ are in general not of interest because the output parallel resonant circuit passes only the fundamental component. Also, due to the even symmetry of the waveform, all of the Fourier coefficients for sine terms are zero and only the Fourier coefficients for cosine terms are to be evaluated. The amplitude of the fundamental component, a_1 , can be found from:

$$a_1 = \frac{2}{T} \cdot \int_{-\frac{T}{2}}^{\frac{T}{2}} i_c(t) \cdot \cos(\omega t) dt \quad (2.32)$$

$$\text{or} \quad a_1 = \frac{\omega}{\pi} \cdot \int_{\cos^{-1}\left(-\frac{x}{l-x}\right)}^{\cos^{-1}\left(\frac{x}{l-x}\right)} [x \cdot I_{C,MAX} + (l-x) \cdot I_{C,MAX} \cdot \cos(\omega t)] \cdot \cos(\omega t) dt \quad (2.33)$$

From the above integral equation, a_1 is found to be:

$$a_1 = \frac{I_{C,MAX}}{\pi} \cdot \left[\frac{x \cdot \sqrt{l-2x}}{l-x} + (l-x) \cdot \cos^{-1}\left(-\frac{x}{l-x}\right) \right] \quad (2.34)$$

The details of the above calculation are shown in Appendix II. Equation (2.34) is the general expression for the fundamental component amplitude of the collector current that

applies to class A, B and AB. Again, with x equal to 0.5, a_1 is equal to $I_{C,MAX}/2$ which is the fundamental amplitude for class A amplification. When x is 0 (i.e. class B operation), the above equation yields $a_1 = I_{C,MAX}/2$ which again is the result for class B operation. The plot of normalized (i.e. $I_{C,MAX}$ is unity) DC and fundamental amplitudes of collector current versus the bias ratio x for class AB operation is shown in figure 2.7. The DC collector current through the transistor rises as x increases, with the minimum occurring in class B operation and the maximum occurring in class A operation. On the other hand, the fundamental component has minimums at both class A and class B operations (solid curve in figure 2.7). Ideally, the optimum class AB operation can achieve a little higher output power than class A and B operations.

Figure 2.7 Normalized DC and fundamental amplitudes of collector current versus the bias ratio x for class AB operation

The maximum linear RF output is given by:

$$P_{RF,MAX} = \frac{v_{ce,peak,max} \cdot a_1}{2} \quad (2.35)$$

where $v_{ce,peak,max}$ is still given by equation (2.2) and a_1 is given by equation (2.34) and equation (2.35) becomes:

$$P_{RF,MAX} = \frac{V_{CE,MAX} - V_K}{4} \cdot a_1 \quad (2.36)$$

The DC power dissipated by the transistor is still given by equation (2.6) and V_{CEQ} is the same as before. Thus:

$$P_{DC} = \frac{V_{CE,MAX} + V_K}{2} \cdot I_{CQ} \quad (2.37)$$

where I_{CQ} is given by equation (2.31). The collector efficiency is therefore given by:

$$\eta_{MAX} = \frac{1}{2} \cdot \frac{(V_{CE,MAX} - V_K)}{(V_{CE,MAX} + V_K)} \cdot \frac{a_1}{I_{CQ}} \cdot 100\% \quad (2.38)$$

and finally, the power added efficiency is given by:

$$PAE = \frac{1}{2} \cdot \left(1 - \frac{1}{G}\right) \cdot \frac{(V_{CE,MAX} - V_K)}{(V_{CE,MAX} + V_K)} \cdot \frac{a_1}{I_{CQ}} \cdot 100\% \quad (2.39)$$

Using the same numerical example and $x=0.25$, the maximum linear output power, collector efficiency and power added efficiency are 53.1mW (or 17.3dBm), 46.9% and 42.3% respectively.

2.2.4 Summary

The ideal theoretical maximum linear output power, collector efficiency and power added efficiency of class A, B and AB power amplifier have been developed.

In the above analysis, only the transistor DC characteristics are used to predict the performance at microwave frequencies and the transistor is assumed to have infinite output impedance. Although simple in nature, the analysis is quite accurate in predicting amplifier performance. For instance, excellent agreement between simple theory and measurement was reported by Geller and Goettle [12] for their 1W class AB amplifier operating at 4.1GHz. In practice, the transistor has finite output impedance which often consists of an output resistance in parallel with a capacitance. The effect of the parallel capacitance can be tuned out with inductance while the effect of the parallel resistance means that a fraction of RF power is dissipated in the transistor. At higher frequencies, the analysis becomes inadequate and more accurate design techniques are needed. These techniques will be discussed in the next section.

As a comparison between class A, B and AB power amplifiers, the advantage of the class A power amplifier is that it provides high gain and linearity. However, it offers low efficiency, typically on the order of 30%. One other drawback in class A operation is that the transistor dissipates constant DC power whether the input is present or not. On the other hand, a class B power amplifier provides higher efficiency. It also provides the same order of maximum linear output power as in class A. One attractive feature of the class B power amplifier is that it does not consume DC power when no AC input is present. A serious disadvantage of class B as compared to class A is that it requires twice as much AC input peak current to have the same RF output power. This implies that class B operation has ideally 1/4 times or 6dB less gain compared to the same transistor operating in class A mode and providing the same output power. Finally,

class AB operation can be viewed as a compromise of class A and B operations, in the sense that higher gain is achieved by sacrificing amplifier efficiency.

Amplifier Design Techniques

2.3.1 Non-linear Computer-Aided Design

Non-linear computer simulators are widely used in power amplifier design as they provide insight to the circuit behavior that conventional linear theory cannot. Specifically, these simulators can predict circuit performances such as output power versus input power characteristic, gain and efficiency of a power amplifier circuit. Commercially available non-linear circuit simulators such as LibraTM, OSA90/HopeTM and Microwave HarmonicaTM are based on the harmonic balance technique which is a steady-state, frequency domain method of analyzing non-linear circuits. Time domain circuit simulators such as Microwave SpiceTM are not commonly used for non-linear circuit simulation because of their slow speed, unless the transient response of the circuit is required. As analysis tools, these simulators offer further understanding of circuit performances and limitations.

In general, the first step in designing a power amplifier is to choose an appropriate transistor. The transistor should meet specifications such as output power capability and stable gain requirements at the operating frequency. These transistor characteristics are usually specified by the manufacturer and sometimes, a transistor model is given. In the case where the transistor characteristics are not known, non-linear device modelling is usually carried out.

After the transistor is chosen, approximations and engineering judgment are used to generate an initial design. The initial design goal is to obtain optimum source and load impedances for the transistor. For a class A power amplifier, the above theory and the small signal S -parameters can be employed to obtain the initial design. An example design similar to the one given by Maas [13] is presented below.

A transistor has the following DC characteristics and small-signal S -parameters at a class A bias at 14.0GHz of

$$\begin{aligned} I_{C,MAX} &= 100\text{mA} & S_{11} &= 0.903 \angle 169.58^\circ \\ V_K &= 1.0\text{V} & S_{21} &= 1.059 \angle 47.467^\circ \\ V_{CE,MAX} &= 5.0\text{V} & S_{12} &= 0.0513 \angle -2.576^\circ \\ & & S_{22} &= 0.497 \angle -166.02^\circ \end{aligned}$$

From equation (2.14), the load resistance R_L is:

$$R_L = \frac{V_{CE,MAX} - V_K}{I_{C,MAX}} = \frac{5.0 - 1.0 \text{ V}}{100 \text{ mA}} = 40 \Omega \quad (2.40)$$

The load conductance $G_L (= 1/R_L)$ is then 0.025S. At high frequency, the transistor output typically consists of a finite conductance in parallel with the output capacitance, thus the output resistance of 40Ω alone will not yield the optimum performance. It is therefore necessary to estimate the transistor output admittance Y_{22} so that its imaginary part can be negated using the admittance of the load. The value of the transistor output admittance Y_{22} can be calculated from the S -parameters as [14]:

$$Y_{22} = \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} = 0.130 + j0.0417 \text{ S} \quad (2.41)$$

Here, the imaginary part of Y_{22} must be resonated out, and therefore the imaginary part of the load admittance B_L takes on a negative value i.e. $-j0.0417$ S. Thus the total load admittance Y_L is $0.025 - j0.0417$ S and the load impedance Z_L is:

$$Z_L = \frac{1}{Y_L} = \frac{1}{0.025 + j0.0417 \text{ S}} = 10.6 + j17.6 \Omega \quad (2.42)$$

The source impedance Z_S can be estimated from the conjugate of Z_{11} for the initial design.

Z_{11} is again calculated from the S -parameters as [14]:

$$Z_{11} = \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}} = 3.22 + j5.35 \Omega \quad (2.43)$$

and finally the source impedance Z_S is:

$$Z_S = Z_{11}^* = 3.22 - j5.35 \Omega \quad (2.44)$$

These are the source and load impedances that are needed to be presented at the terminals of the transistor for class A power amplifier initial design and must include the effects of bond wire inductances and parasitics. As a sidenote, the transistor characteristics above are from the actual HBT that is to be used to design a power amplifier circuit.

For class B power amplifier design, care must be taken in using S -parameters in calculating the impedances because the transistor is biased near cutoff. For the load impedance, the method used above in class A cannot be applied. However, it was found in Section 2.2.2 that a class B power amplifier has the same load resistance R_L as a class A power amplifier. For this reason, the load impedance Z_L for class A operation can be used for class B operation as the initial design value. Strictly speaking, the source impedance cannot be obtained from the conjugate match to the input impedance as is done in class A because the transistor is at cutoff. However, a practical

class B power amplifier usually has collector current biased at $0.1 \cdot I_{C,MAX}$ (i.e. class AB) instead of zero to achieve higher gain. Therefore, the source impedance can be estimated from the conjugate match, as before, using the S -parameters values at class B bias. In general, the source and load impedances approximated for class B power amplifier are not as close to their optimized values as those of class A.

After the initial design is completed, the transistor non-linear model, terminated with appropriate source/load impedances, can be simulated and the amplifier's performance obtained, such as output power versus input power, gain and efficiency characteristic. Typically, the initial design does not yield optimum performance and the source and load impedances must be further optimized through the built-in optimization routines in the simulator. Eventually, the optimum source and load impedances with respect to the design specifications will be obtained. In practice, the impedances are close to the initial calculated values, especially for class A operation as shown by [13]. Finally, the input and output matching networks, and biasing networks can be designed accordingly at the frequency of interest. This completes the power amplifier design cycle.

2.3.2 Load-Pull Technique

The load-pull technique of designing a power amplifier is the most practical method of all. Figure 2.8 shows a basic setup for load-pull measurement system. It involves two tuners connected at both input and the output of the device under test. The operation of the setup is very straightforward as follows. At the input, power-meter A measures the power level that is applied to the system while power-meter B

senses the reflected power due to mismatch between the input tuner and the input of the transistor. At the output, power-meter C measures the output power. From these measurements, simple calculations can be carried out to compute output power, gain and efficiency as a function of input power, tuner settings, bias condition, and frequency of interest.

Figure 2.8 A basic setup for load-pull measurement system

Typically, for a given input power, the output tuner is adjusted so that power meter C measures a given level of power (say 10dBm) and the input tuner is adjusted until minimum reflection (measured at power-meter B) is achieved. At this point, the input of the transistor is conjugately matched and the effective input and output impedances presented to the transistor are measured. The output power level as a function of that output impedance is then plotted on the Smith chart. This process is carried on at that given output power level for different output impedance values. With enough impedance points, the result forms a constant-power contour on the Smith chart.

Then for different output power levels, the whole process is repeated again and finally, a family of power contours results. Typical power contours as a function of load impedance are shown in figure 2.9. Note that the power contours are also functions of input power, DC bias point and frequency.

Figure 2.9 Typical output power contours as a function of load impedance (at a fixed frequency, bias point and input power)

In the above figure, each contour corresponds to an output power level as shown. Furthermore, the contour appears to be elliptical in shape and becomes smaller for higher output power. At maximum output power, the contour becomes a single point. The corresponding load impedance is the optimum load impedance for the highest output power while the input is still conjugately matched. These source and load impedances can then be used to generate the matching networks in the power amplifier design. In general, the contour plots are power contours. However, sometimes constant gain or

constant efficiency contours are used.

In summary, it is seen that load-pull measurements can be very tedious and time consuming if performed manually. In practice, an automated load-pull system is used to perform these measurements. The automation typically involves a stepping motor (controlled by a computer) driving the mechanical slug inside the tuner while the computer collects and plots data on a Smith chart. Even so, a large quantity of data is generated and needs to be stored and managed. The load-pull technique has other disadvantages such as entering the regions of instability, uncontrolled impedances at harmonic frequencies and limits on maximum tuner VSWR. However, for a newly developed device where the model is difficult to obtain, the load pull measurement is perhaps the fastest and easiest way to achieve an optimum amplifier design.

CHAPTER 3: DEVICE MODELLING

3.1 Introduction

Device modelling plays an important role in the non-linear microwave circuit design process. Because the fabrication cost of microwave circuits are high, revisions after circuits are processed are highly undesirable. This leads to the need for an accurate large-signal device model and, with non-linear CAD tools available today such as Libra™, Microwave SPICE™, and OSA90/Hope™, accurate circuit performances can be predicted. In addition, current and voltage waveforms at any point in the circuit can also be simulated, thus providing useful design insights. An accurate device model therefore not only speeds up the design cycle, it also increases the circuit yield and lowers the production cost.

A good model should be able to predict the device performance in many aspects, yet be simple enough to be implemented in existing CAD tools. There are many “physics based” HBT models being reported [15,16] which involve complex equations and which are difficult to implement in the design tools. Furthermore, these “physics based” models often require physical parameters such as transistor geometry and doping profiles that usually are not made available to the end users. As they stand, these models are not very useful in the circuit design cycles. In this thesis, the aim in HBT modelling is not to address the physical effects in device operation. Instead, a circuit model similar to that of the Gummel-Poon model for the BJT [17], which consists of circuit elements such as diodes, resistors, non-linear capacitances and non-linear current sources, is used to approximate the device electrical behavior. The basic principle and characteristics of

the HBT are discussed in the following section.

3.2 Heterojunction Bipolar Transistor (HBT)

3.2.1 HBT Brief History

The principle of the heterojunction bipolar transistor (HBT) was first suggested by Shockley in 1951. Later in 1958, further theory and advantages of the HBTs were proposed by Kroemer [18]. The HBT was called a wide-gap emitter transistor at that time and no experimental work had ever been realized. In 1969, the first HBT was fabricated by Feucht et al [19]. By the 1980's, much of HBT work was still in an experimental stage. At the present time, HBT technology is fairly mature and many foundries have fabricated promising HBTs and their application related circuits.

3.2.2 HBT Principle

Essentially, the HBT is a bipolar transistor with a wide band-gap emitter. To achieve this, the emitter of an HBT is made of a material different from the base and collector. The dissimilar band-gap energies at the emitter-base junction form the heterojunction and hence the name heterojunction bipolar transistor. The principle of the HBT can be explained by studying its band structure. Figure 3.1 shows the typical band diagrams of a conventional BJT compared with an HBT, both under forward bias. For the BJT, the energy gap (E_g) is constant throughout the device, which is sometimes referred to as the homojunction bipolar transistor. In the conduction band, the electrons are injected into the base from the emitter and likewise, in the valence band, the holes are

back injected into the emitter from the base. At the emitter side, the ratio of the electrons to the overall carriers (electrons and holes) constitutes the emitter injection efficiency γ . The closer the emitter injection efficiency to unity, the higher the DC current gain β becomes. Therefore, in order to achieve high emitter injection efficiency and thus high DC current gain, the emitter side of the conventional BJT is usually heavily doped (n^+).

(a) Homojunction Bipolar Transistor Band Diagram

(b) Heterojunction Bipolar Transistor Band Diagram

Figure 3.1 Typical band diagrams of (a) a BJT and (b) an HBT, both under forward bias

On the other hand, the emitter of the HBT has a wider energy gap (E_{ge}) compared to the base and collector (E_g). Again, the electrons are injected into the base in the conduction band. In the valence band, however, far fewer holes are back injected into the emitter because of the large energy barrier (an additional ΔE_g) presented to them. This results in much lower hole current density at the emitter, and thus a much higher injection efficiency. Therefore in an HBT, high injection efficiency is achieved through the band-gap variation instead of high emitter doping (which in practice reaches a practical limit on the magnitude of doping).

Quantitatively, the emitter injection efficiency γ of an npn transistor is defined as:

$$\gamma = \frac{j_n}{j_n + j_p} \quad (3.1)$$

where j_n is the electron current density and j_p is the hole current density. Dividing top and bottom by j_n , equation (3.1) becomes:

$$\gamma = \frac{1}{1 + \frac{j_p}{j_n}} \quad (3.2)$$

and thus the smaller the ratio j_p/j_n , the closer γ becomes unity. Due to the band-gap variation, the ratio of the hole current density to the electron current density (j_p/j_n) in an HBT is decreased by the factor [18]

$$e^{-\frac{\Delta E_g}{kT}} \quad (3.3)$$

where ΔE_g is the difference in band-gap energies, k is the Boltzmann's constant and T is the absolute temperature. The exponential term is important because if ΔE_g is 0.2 eV and,

at room temperature, kT is about 0.025 eV , then the ratio j_p/j_n is decreased by a factor of $1/3000$. With this magnitude of decrease in j_p/j_n , the injection efficiency of an HBT is typically very close to unity and the DC current gain β can be in the order of 1000.

Another immediate advantage of HBT's is that, since its emitter does not need to be heavily doped, the minority carrier charge storage in the emitter becomes negligible and, the base-emitter capacitance C_{BE} is significantly lowered compare to a conventional BJT. This reduction in junction capacitance increases the unity gain bandwidth f_t of the transistor thus allowing higher frequency operation. Moreover, the emitter area can be increased to obtain better power handling capability for the same frequency response.

In practice, since the injection efficiency is so high that it can be sacrificed and still have useful transistor's properties, the base of an HBT can be heavily doped (p^+) to drastically reduce the base spreading resistance as shown in figure 3.1. Lower base resistance R_b further increases the f_t of the transistor and also makes HBT's suitable for power applications.

3.2.3 HBT Fabrication

Although the idea of the HBT is as old as the bipolar junction transistor itself, an actual HBT was not demonstrated until much later. This was mainly due to the technical difficulties in forming an acceptable heterojunction of III-V semiconductors of unequal band gap [19]. However, with recent advance in the material growth techniques such as molecular beam epitaxy (MBE) and metal-organic chemical vapor deposition

(MOCVD), high performance HBTs are made possible. These techniques allowed deposition of one material onto the other layer by layer, nearly on an atomic scale. As the result, both the compositions (hence the band structures and hence the inherent electric field) as well as the doping levels of the HBT can be precisely controlled. Figure 3.2 shows the typical schematic cross section of an AlGaAs/GaAs HBT grown by these techniques.

Figure 3.2 The typical schematic cross section of an AlGaAs/GaAs HBT

The HBT shown above consists of several layers (sometimes referred to as epitaxial layers) of varying thickness and doping densities. This is typically done in practice to optimize the transistor performance. By fabricating an HBT using GaAs material, higher frequency operation results due to the higher electron mobility in GaAs than Si. Furthermore, the self-aligned processing technique [20] which reduces the lateral separation between the emitter and base metallizations to about $0.2\mu\text{m}$, greatly reduces the base resistance and results in higher f_t . Using the above techniques, HBT's with f_t , f_{max} of the order of 100–200 GHz have been reported [1].

Since the emitter layer of an HBT needs to be made of different material (hence different energy gap), structural mismatches may occur at the interface of the heterojunction because of unequal atomic lattice constants. Lattice mismatch generally causes degradation in device performance and it is highly desirable to reduce this ratio to a minimum. In practice, an 8% mismatch can be accommodated without degrading crystalline quality. Figure 3.3 shows the bandgap energy versus lattice constant of some III-V compounds. It can be seen that AlGaAs compound provides good match to the GaAs material and for this reason, many AlGaAs/GaAs HBTs have been reported. Although not very mature, InGaAs/InP HBTs have also been fabricated and reported [21].

Figure 3.3 Bandgap energy versus lattice constant for some III-V compounds

3.2.4 HBT Common Characteristics

The physical structure of the $360\mu\text{m}^2$ (total emitter area) AlGaAs/GaAs HBT used in this thesis is shown in Figure 3.4. This particular HBT was provided by Rockwell International. The transistor is in a common emitter configuration and was designed so that it can be on-wafer evaluated using microwave ground-signal-ground probes. In order to improve the device heat flow problem, the transistor was divided into 9 cells, each of which consisted of two emitter fingers as shown at the right; each finger being $2 \times 10\mu\text{m}^2$. The input to the base of the transistor (B) was divided into 4 lines as shown and was connected to the base terminals of all cells through airbridges. The collector terminals of the cells were combined together at the output of the transistor (C) while the emitter of each cell was grounded through the 3 via-holes (E) in the middle.

Figure 3.4 Physical structure of the $360\mu\text{m}^2$ AlGaAs/GaAs HBT

Figure 3.5 shows the I_C versus V_{CE} characteristic (I_B of 0 to 3.5mA in steps of 0.5mA) of the Rockwell $360\mu\text{m}^2$ HBT. The negative slope (or negative output resistance) in the forward active region of the DC IV curve is well known for HBTs. It is mainly caused by a self-heating effect due to the combination of high power density in the HBT and the poor thermal conductivity property of the GaAs substrate [22]. In general, HBTs dissipate power in their base-collector junction and this power is converted into heat energy. With a poor thermal conductivity substrate such as GaAs, the heat energy does not conduct away and this causes the junction temperature to rise. As the junction temperature rises, current gain decreases, resulting in lower collector current.

Figure 3.5 I_C versus V_{CE} characteristic of Rockwell $360\mu\text{m}^2$ HBT

In the conventional BJT, the heating problem is not pronounced because Si possesses good thermal conductivity properties. In fact, a BJT has a positive slope (positive output resistance) in the active region of DC IV curve. This is due to the base-width modulation effect (also known as the Early effect). Here, the effective base width

changes as the result of collector-emitter voltage variation. In an HBT, however, due to the very high base doping, the base-width modulation effect is negligible and the Early voltage can be assumed to be infinite [23]. Another typical characteristic of an HBT is the offset voltage (ΔV_{CE}) in the I_C versus V_{CE} characteristic. This is due to the higher turn on voltage of the base-emitter heterojunction compared to the base-collector homojunction.

The measured forward and reverse Gummel-plots of the HBT are shown Figure 3.6. At extremely low level of current, currents saturate because of the finite parallel conductance effect, perhaps from the measurement system and/or the substrate conductance. On the other hand, at high current levels, the currents saturate again due to the series resistances (R_B , R_C and R_E) effect.

Figure 3.6 Forward and reverse Gummel-plots for Rockwell 360 μm^2 HBT

Unlike the case for conventional BJT, there are no parallel regions in these plots and thus HBTs do not exhibit a region of constant current gain (i.e. I_C/I_B is not constant) over the bias condition. The collector and emitter currents are still the same as those in a BJT since their ideality factors n_c , n_e , respectively were found to be close to 1.0 (i.e. they obey the $\exp(qV/kT)$ law). The base current (in the forward Gummel plot), however, showed an ideality factor of 1.6 to 2.0 over the bias range. Generally in a bipolar transistor, electron-hole injection and space charge region (SCR) recombination mechanisms give rise to the base current. The electron-hole injection current takes on an ideality factor of 1 since it is mainly driven by diffusion while the space charge region (SCR) recombination current has an ideality factor of close to 2. In a BJT, the electron-hole injection mechanism is more dominant and therefore there exists a parallel region (thus constant gain) in the Gummel plot. However in an HBT, SCR recombination is much stronger and the combination of the two current components gives a base current ideality factor of closer to 2.

Because of the self-heating effect, the HBT junction temperature changes dynamically over the DC-IV bias conditions and it is therefore essential to account for the temperature dependence of the parameters in HBT modelling. In particular, the temperature dependence of the saturation currents and DC current gain are of great importance. Normally in bipolar transistors, the saturation currents are temperature dependent due to the fact that the intrinsic carrier density, n_i^2 , is very sensitive to temperature change. For a BJT, the saturation currents are proportional to the cubic power of the junction temperature [24]. For the HBT, however, the temperature

dependence of saturation currents follow expressions which are considerably different from the BJT, as proposed by Wang [25]. The DC current gain β of an HBT is also temperature dependent. It is inversely proportional to the junction temperature. This is in contrast to the BJT where the current gain increases with the junction temperature and is the main cause of thermal runaway. Although there is no thermal runaway problem in an HBT, self-heating effects have caused severe problems in a comparator circuit [22].

The measured two port S -parameters of the Rockwell $360\mu\text{m}^2$ HBT are shown in Figures 3.7a and 3.7b. They were measured using the HP8510 network analyzer at a frequency range from 0.4GHz to 40GHz. The HBT was biased near class A operation, with the base current I_B of 1.5mA and collector-emitter voltage V_{CE} of 3.0V. In general, the AC characteristic of HBT are comparable to other devices such as FETs and HEMTs. However, the input impedance S_{11} is found to be low and it is more difficult to be matched to a 50Ω system.

Figure 3.7a Measured S_{11} , S_{12} and S_{22} for Rockwell $360\mu\text{m}^2$ HBT ($I_B = 1.5\text{mA}$ $V_{CE} = 3.0\text{V}$)

Figure 3.7b Measured S_{21} for Rockwell $360\mu\text{m}^2$ HBT ($I_B = 1.5\text{mA}$ $V_{CE} = 3.0\text{V}$)

3.3 Modified Gummel-Poon Model

The very first step in the modelling process is to select a proper model topology. In modelling FETs and HEMTs, the well-known Curtice and Meterka model [26] topology is often used, and conveniently, these topologies are available as built-in models in many commercial softwares. For HBT's however, being a relatively new device, there is no built-in model topology available and the model has to be user-defined. As a result, this adds an extra degree of difficulty in HBT modelling, especially at large signal levels. In spite of this, from the literature [22, 23, 27] and preliminary simulation results, it was decided that the large signal HBT model topology consisted of three parts, the intrinsic device model, extrinsic parasitics and the thermal sub-circuit. They are discussed in more detail below.

3.3.1 The Intrinsic Device Model

The intrinsic device model represents the active area of the device, that is, it does not take into account parasitic effects. Due to many similarities (i.e. physical structure and vertical bipolar operation) between the HBT and the BJT, the conventional BJT Gummel-Poon model with some modifications was chosen as the intrinsic model [22, 23]. It consists of terminal resistances, diodes, non-linear capacitances and a non-linear current source as shown in Figure 3.8.

Figure 3.8 The intrinsic modified Gummel-Poon model for HBT

The terminal resistances R_B , R_C , R_E were used to model the lateral contact resistances and spreading resistances from the metallization contacts prior to the region where the transistor action taken place. These resistances were assigned as constant parameters.

The diodes D_{BF} , D_{BR} , D_E and D_C were used to model the electron-hole injections and space-charge region (SCR) recombination mechanisms in the HBT which

gave rise to the overall base current. The equations that govern these diodes are identical in form. Specifically, diode D_{BF} was used to model the electrons injected from the emitter into the base and holes that are injected from the base into the emitter. Its current-voltage relationship is given by [28]:

$$I_{D_{BF}} = \frac{I_{SAT}(T)}{\beta_f(T)} \cdot \left[\exp\left(\frac{qV_{be}}{n_f kT}\right) - 1 \right] \quad (3.4)$$

where q is the electron charge, k is the Boltzmanns constant and T is the junction temperature in degrees Kelvin. In addition, $I_{SAT}(T)$ is the saturation current and $\beta_f(T)$ is the ideal forward current gain and are both temperature dependent. As previously mentioned, this electron-hole injection current is typically diffusion driven and therefore has an ideality factor n_f of close to 1.

The other diode between the base-emitter junction D_E was used to model the space-charge region recombination in the junction. Again, it follows similar form as equation (3.4):

$$I_{D_E} = I_{SDE}(T) \cdot \left[\exp\left(\frac{qV_{be}}{n_e kT}\right) - 1 \right] \quad (3.5)$$

here, $I_{SDE}(T)$ is the saturation current for base-emitter SCR recombination current and its ideality factor n_e is generally close to 2. In fact, the two currents I_{DBF} and I_{DE} give the overall base current in the forward Gummel-plot (Figure 3.6) since, when measuring the forward Gummel-plot, the base and collector terminals are short circuited. For HBT's, $I_{SDE}(T)$ is typically much greater, several order of magnitudes greater, than $I_{SAT}(T)$. Therefore the combination of the two current gives overall base current ideality of closer to 2.

The diode D_{BR} was used to model both the electrons injected from the collector into the base and holes that are injected from the base into the collector. It has an I - V characteristic of:

$$I_{D_{BR}} = \frac{I_{SAT}(T)}{\beta_f} \cdot \left[\exp\left(\frac{qV_{bc}}{n_f kT}\right) - 1 \right] \quad (3.6)$$

where β_f is the ideal reverse current gain and was assigned as a constant parameter. Again, since this current represents the injection of carriers, its ideality n_f is close to 1.

Finally, diode D_C was used to model the space-charge region recombination in the base-collector junction. It has the form of:

$$I_{D_C} = I_{SDC}(T) \cdot \left[\exp\left(\frac{qV_{bc}}{n_c kT}\right) - 1 \right] \quad (3.7)$$

and $I_{SDC}(T)$ is the saturation current for base-collector SCR recombination current. The ideality n_c is generally close to 2. At DC, the sum of the above four current components give rise to the overall base current in the HBT.

The temperature dependence of the saturation currents and the ideal forward current gain followed the expressions that were proposed by Wang [27]. They are as follows:

$$I_{SAT}(T) = I_{SAT_0} \cdot \left(\frac{T}{T_0}\right)^{x_{TI}} \cdot \exp\left(-\frac{E_g}{kT} + \frac{E_g}{kT_0}\right) \quad (3.8)$$

$$\beta_f(T) = \beta_{f_0} \cdot \left(\frac{T}{T_0}\right)^{-x_{TB}} \cdot \exp\left(-\frac{E_{inf}}{kT} + \frac{E_{inf}}{kT_0}\right) \quad (3.9)$$

$$I_{SDC}(T) = I_{SDC_0} \cdot \left(\frac{I_{SAT}(T)}{I_{SAT_0}}\right)^{\frac{1}{n_c}} \cdot \left(\frac{\beta_{f_0}}{\beta_f(T)}\right) \quad (3.10)$$

$$I_{SIX}(T) = I_{SIXo} \cdot \left(\frac{I_{SAT}(T)}{I_{SATo}} \right)^{\frac{1}{n_e}} \cdot \left(\frac{\beta_{fo}}{\beta_f(T)} \right) \quad (3.11)$$

here, T_o is the room temperature at 300K. I_{SATo} , I_{SDEo} and I_{SDCo} are the respective saturation currents at room temperature that are extractable from the forward and reverse Gummel-plot. Similarly, β_{fo} is the ideal forward current gain at room temperature. XTI is the saturation current temperature exponent and has a value of 6.0. XTB is the forward current gain temperature exponent and has a value of 1.0. The minus sign in front of XTB signifies decreasing forward current gain with increasing temperature. In fact, for the conventional BJT, XTB also has a value of 1.0 but with a plus sign. E_g is the band gap energy for the substrate material, which is 1.41eV for GaAs. The last temperature parameter E_{mf} is a constant fitting parameter employed to account for the temperature dependent characteristic of the forward current gain.

The non-linear current source I_{CE} of figure 3.8 has the similar form as the standard Gummel-Poon model. It is given by:

$$\begin{aligned} I_{CE} &= I_{DBF} \cdot \beta_f(T) - I_{DBR} \cdot \beta_r \\ &= I_{SAT}(T) \cdot \left[\exp\left(\frac{qV_{be}(t-\tau)}{n_f kT}\right) - \exp\left(\frac{qV_{bc}}{n_r kT}\right) \right] \end{aligned} \quad (3.12)$$

In general, I_{CE} is the amplified component of the two current components I_{DBF} and I_{DBR} . Here, an excess time delay term τ was added to the base-emitter voltage as proposed by Teeter et al [29] to account for the transit time effect.

Similar to a BJT, the HBT has two non-linear capacitances, namely, the base-emitter capacitance C_{BE} and the base-collector capacitance C_{BC} . Each of the non-

linear capacitances consists of diffusion and depletion components. The diffusion capacitance models the excess charge storage effect during forward bias and, the depletion capacitance models the space-charge region capacitance similar to a parallel plate capacitance having a width equal the width of the space charge region. As previously mentioned, due to low emitter doping in HBT, C_{BE} is small. The equation of C_{BE} is as follows:

$$C_{BE} = C_{BE, diff} + C_{BE, depl} \quad (3.13)$$

where

$$C_{BE, diff} = \frac{\tau_f \cdot q \cdot I_{SAT}(T)}{n_f kT} \cdot \exp\left(\frac{qV_{BE}}{n_f kT}\right) \quad (3.14)$$

In the above equation, τ_f is the forward transit time and its dependence on V_{BC} is given by [30]:

$$\tau_f = \tau_{fo} \cdot \left[1 - XTF \cdot \exp\left(\frac{V_{BC}}{1.44 \cdot VTF}\right) \right] \quad (3.15)$$

the parameters τ_{fo} , XTF and VTF are the SPICE coefficients for dependency of τ_f on V_{BC} . The base-emitter depletion capacitance follows the standard SPICE equation and is given by:

$$C_{BE, depl} = \begin{cases} C_{JE} \cdot \left(1 - \frac{V_{be}}{V_{JE}}\right)^{-M_{JE}} & V_{be} \leq F_C \cdot V_{JE} \\ \frac{C_{JE}}{(1 - F_C)^{1+M_{JE}}} \cdot \left[1 - F_C(1 + M_{JE}) + \frac{M_{JE} V_{BE}}{V_{JE}}\right] & \text{Otherwise} \end{cases} \quad (3.16)$$

where C_{JE} is the base-emitter zero-bias depletion capacitance, V_{JE} is the base-emitter built-in potential and M_{JE} is the base-emitter junction exponent. Since the base-emitter

junction of this particular HBT is graded, M_{JE} takes on a value of 0.333 [17].

Because the collector-base junction is a homojunction, the standard BJT SPICE equation holds for the non-linear capacitance C_{BC} . It is given by:

$$C_{BC} = C_{BC,diff} + C_{BC,depl} \quad (3.17)$$

where

$$C_{BC,diff} = \frac{\tau_r \cdot q \cdot I_{SAT}(T)}{n_r kT} \cdot \exp\left(\frac{qV_{BC}}{n_r kT}\right) \quad (3.18)$$

where τ_r is the reverse transit time and:

$$C_{BC,depl} = \begin{cases} C_{JC} \cdot \left(1 - \frac{V_{bc}}{V_{JC}}\right)^{-M_{JC}} & V_{bc} \leq F_C \cdot V_{JC} \\ \frac{C_{JC}}{(1 - F_C)^{1+M_{JC}}} \cdot \left[1 - F_C(1 + M_{JC}) + \frac{M_{JC} V_{BC}}{V_{JC}}\right] & \text{Otherwise} \end{cases} \quad (3.19)$$

Again, the parameter C_{JC} is the zero-bias depletion capacitance, V_{JC} is the built-in potential and M_{JC} is the junction exponent for base-collector junction. Since the base-collector junction of this particular HBT is abrupt, M_{JC} has a value of 0.5 [17]. This completes the description of the intrinsic device model.

3.3.2 The Extrinsic Parasitics

At microwave frequencies, parasitics become significant and can influence the device S -parameter responses. Because their effect is difficult to calibrate out, it is most convenient to include them in the device model. The extrinsic parasitics model is shown in Figure 3.9. It consists of inductors L_B , L_C and L_E and capacitors C_{BE}' , C_{BC}' and C_{CE}' . These components were used to model the parasitic inductances and stray

capacitances introduced by the probe pads, short length of transmission lines and via holes around the device active area. These are also constant parameters and typically small in values.

Figure 3.9 The extrinsic parasitic model

3.3.3 The Thermal Sub-circuit

One limitation of the Gummel-Poon model is that it cannot predict the negative slope in the I_C versus V_{CE} characteristic of HBT. As mentioned earlier, this negative slope is mainly due to the device self-heating effect. It is due to the poor thermal conductivity of the GaAs substrate and this effectively can be modelled as a thermal resistance for a heat conduction process. A thermal sub-circuit has been widely used to account for this self-heating effect [22] and is shown in Figure 3.10. It is an

electrical equivalent circuit of the thermal conduction process. For the DC response, the mathematical equivalent of the thermal sub-circuit is given by

$$T_J = T_O + R_{TH} \cdot (I_B V_{BE} + I_C V_{CE}) \quad (3.20)$$

Here, the junction temperature T_J output from this sub-circuit modifies the temperature parameter T in the diode and non-linear current source equations in the intrinsic Gummel-Poon model. In equation (3.20), the currents and voltages output from the Gummel-Poon model are used in the thermal sub-circuit to compute the effective junction temperature. Note that the thermal resistance R_{TH} has an unit of $^{\circ}/W$. The thermal capacitance C_{TH} combines with R_{TH} to a thermal time constant which was reported to be in the order of μs [21].

Figure 3.10 The thermal sub-circuit

Finally, combining the intrinsic model, extrinsic parasitics and the thermal sub-circuit, the complete modified Gummel-Poon model topology is shown in Figure 3.11. This topology was used throughout the modelling exercise.

The complete modified Gummel-Poon model consists of 36 model parameters. They are summarized in Table 3.1 below.

Figure 3.11 The complete modified Gummel-Poon model as proposed

	Parameter	Description	Unit
Intrinsic Gummel- Poon Model	I_{SAT0}	Saturation current for diodes D_{BF} and D_{RK} at T_0	A
	I_{SDE0}	Saturation current for diode D_F at T_0	A
	I_{SDC0}	Saturation current for diode D_C at T_0	A
	XTI	Saturation currents temperature exponent	
	E_g	Band gap energy	eV
	n_f	Forward ideality factor for diode D_{BF}	
	n_r	Reverse ideality factor for diode D_{RK}	
	n_e	Ideality factor for diode D_F	
	n_c	Ideality factor for diode D_C	
	R_B	Base series resistance	Ω
	R_E	Emitter series resistance	Ω
	R_C	Collector series resistance	Ω
	β_{f0}	Ideal forward current gain at T_0	
	XTB	Current gain temperature exponent	
	E_{inf}	Current gain temperature dependence parameter	eV
	β_r	Ideal reverse current gain	
	τ	Excess time delay	sec
	τ_{f0}	Forward transit time fitting parameter	sec
	XTF	Forward transit time V_{BE} dependence coefficient	
	VTF	Forward transit time bias dependence coefficient	V
	C_{JE}	Base-emitter zero-bias depletion capacitance	F
	V_{JE}	Base-emitter built-in potential	V
	M_{JE}	Base-emitter junction exponent	
	FC	Forward bias depletion capacitance coefficient	
	τ_r	Reverse transit time	sec
	C_{JC}	Base-collector zero-bias depletion capacitance	F
	V_{JC}	Base-collector built-in potential	V
	M_{JC}	Base-collector junction exponent	
Extrinsic parasitics	L_B	Base parasitic series inductance	H
	L_C	Collector parasitic series inductance	H
	L_E	Emitter parasitic series inductance	H
	C_{BE}'	Base-emitter parasitic capacitance	F
	C_{BC}'	Base-collector parasitic capacitance	F
	C_{CE}'	Collector-emitter parasitic capacitance	F
Thermal sub-circuit	R_{TH}	Thermal resistance	$^{\circ}\text{C/W}$
	C_{TH}	Thermal capacitance	J/ $^{\circ}\text{C}$

Table 3.1 Model parameters of the modified Gummel-Poon model

3.4 Parameter Extractions

After defining the model topology and its governing equations, the next step in device modelling is to obtain the values of model parameters. Typically, the parameter value is obtained by means of parameter extraction, that is, from the theory of device operation, a specific measurement is undertaken so that the model parameter can be calculated from the measured results (i.e. slope or intercept). For the HBT, with many parameters present in the model, the parameter extraction process can be very measurement intensive. However, one common difficulty in device modelling is that not all of the model parameters can be extracted, due to the complexity of the model. In this work, there are totally 36 model parameters in the non-linear HBT model and only 11 of them were extracted, or at the moment known to be extractable. The extraction techniques for these parameters are described in this section. For non-extractable parameters, an optimization technique was used to approximate their values. The optimization process is discussed in Section 3.5.

3.4.1 Intrinsic Device Model Parameter Extractions

For the intrinsic device model, only 9 parameters were extracted. These are saturation currents I_{SAT0} , I_{SE0} , I_{SC0} , ideality factors n_f , n_r , n_c , n_e and terminal resistances R_E and R_B . The extraction techniques of these parameters are described below.

(i) Saturation currents and ideality factors:

The room temperature saturation currents I_{SAT0} , I_{SE0} , I_{SC0} and the ideality factors n_f , n_r , n_c , n_e can be approximated from the forward and reverse Gummel plots as

for the case in the conventional BJT. In the forward Gummel plot, V_{bc} was set to 0.0 V and $\log(I_C)$, $\log(I_B)$ were measured as a function of V_{be} (hence V_{ce}). For simplicity, the device junction temperature is assumed to be the same as room temperature in the following analysis (i.e. no self-heating effect). With V_{bc} being 0.0 V, the current components that depends on V_{bc} vanish and the collector current I_C becomes:

$$I_C = I_{SAT0} \cdot \left[\exp\left(\frac{qV_{be}}{n_f kT_0}\right) - 1 \right] \approx I_{SAT0} \cdot \left[\exp\left(\frac{qV_{be}}{n_f kT_0}\right) \right] \quad (3.21)$$

since the term $\exp(qV_{be}/n_f kT_0) \gg 1$. Similarly, the base current I_B becomes:

$$I_B \approx \frac{I_{SAT0}}{\beta_{fo}} \cdot \left[\exp\left(\frac{qV_{be}}{n_f kT_0}\right) \right] + I_{SDE0} \cdot \left[\exp\left(\frac{qV_{be}}{n_e kT_0}\right) \right] \quad (3.22)$$

The logarithm of I_C in equation (3.21) becomes:

$$\log(I_C) \approx \log(I_{SAT0}) + \frac{q \cdot \log(e)}{n_f kT_0} \cdot V_{be} \quad (3.23)$$

The above equation is in the form of a straight line and therefore, from the intercept of the $\log(I_C)$ versus V_{be} curve, the saturation currents I_{SAT0} can be calculated and also, from its slope, the ideality factors n_f can be calculated. Figure 3.12 shows the parameter extraction technique for the measured forward Gummel plots. By drawing best fit straight lines to the measurement curve, the intercepts and the slopes were estimated as shown.

The base current I_B in equation (3.22) consists of two current components and the combination of the two results in a varying slope for the $\log(I_B)$ curve as shown in Figure 3.12. However at low base current, the SCR recombination current component (the second term in equation (3.22)) is more dominant for an HBT and, by drawing best

fit straight lines to the $\log(I_B)$ curve at low current level, the saturation current I_{SDE0} and ideality factor n_e can be crudely approximated. Because these two parameters are not very accurate, they will be subsequently optimized with loose constraint.

Figure 3.12 Parameter extractions from forward Gummel plot

The parameter extraction method from the reverse Gummel plot is shown in Figure 3.13. Here, V_{be} was set to 0.0 V and $\log(I_B)$, $\log(I_E)$ were measured as a function of V_{bc} . Again, assuming the room temperature and that $\exp(qV_{bc}/n_x kT_o) \gg 1$ (where n_x can be n_r or n_c), the base current is given by:

$$I_B \approx \frac{I_{SAT0}}{\beta_r} \cdot \left[\exp\left(\frac{qV_{bc}}{n_r kT_o}\right) \right] + I_{SIX0} \cdot \left[\exp\left(\frac{qV_{bc}}{n_c kT_o}\right) \right] \quad (3.24)$$

and the emitter current is given by:

$$I_E \approx I_{SAT0} \cdot \left[\exp \left(\frac{qV_{bc}}{n_r k T_0} \right) \right] \quad (3.25)$$

Although the base current I_B in equation (3.24) consisted of two current components, the SCR recombination current completely dominates the other for all bias conditions. Therefore the $\log(I_B)$ curve still yields a unique slope. Thus, from the $\log(I_B)$ curve, the saturation current I_{SDC0} and ideality factor n_c can be extracted. Further, from the $\log(I_E)$ curve, only the ideality factor n_r needs to be extracted.

Figure 3.13 Parameter extractions from reverse Gummel plot

In general, the assumption of the device junction temperature being the same as the room temperature is valid only at low current levels, for only at low current is the power dissipated by the device minimal. In both parameter extraction exercises, because all the slopes were taken at relatively low current levels, this temperature

assumption holds.

From the slopes and the intercepts of the forward and reverse Gummel plots, the parameters I_{SATo} , I_{SEo} , I_{SCo} , n_f , n_r , n_c and n_e are calculated and tabulated in table 3.2.

Forward Gummel Plot			Reverse Gummel Plot		
$\log(I_C)$	I_{SATo}	1.6889e-22 A	$\log(I_B)$	I_{SLXo}	2.4752e-14 A
	n_f	1.1294		n_c	1.7398
$\log(I_B)$	I_{SDEo}	1.1354e-18 A	$\log(I_E)$	n_r	1.0267
	n_e	1.5484			

Table 3.2 Parameter values extracted from Gummel plots

(ii) Series resistances:

Because DC techniques of extracting series resistances such as the open collector method had been shown to be inaccurate [23], AC methods based solely on the S parameters were used to extract the series resistance R_E and R_B . The emitter series resistance R_E was extracted using the technique proposed by Maas [31]. In his technique, by analyzing the small signal equivalent model of the common emitter HBT, and because the fact that the base-emitter capacitance C_{BE} was small, the impedance Z_{12} was practically real at low frequency (i.e. 1GHz) and is given by:

$$Z_{12} = R_E + R_{JE} \quad (3.26)$$

where R_E is the constant emitter series resistance and R_{JE} is the bias dependent resistance. Furthermore, it was shown by Maas that R_{JE} is related to the DC emitter current I_E by:

$$R_{JE} = C/I_E \quad (3.27)$$

where C is a constant. Substituting the above equation into equation (3.26) yields:

$$Z_{12} = R_E + C/I_E \quad (3.28)$$

Therefore, by plotting Z_{12} versus $1/I_E$, R_E can be found from the intercept of the graph.

The plot of Z_{12} versus $1/I_E$ for the $360\mu\text{m}^2$ Rockwell HBT is shown in Figure 3.14. Here, the data points were taken from S -parameters at 1.0GHz measured at $I_B = 0.5\text{mA}$ to 3.0mA in steps of 0.5mA while V_{CE} was kept at 3.0V for all I_B conditions. These data were then converted into Z parameters and for each point I_E was found from the sum of base and collector currents. A best fit straight line through the data points was drawn and the emitter R_E was found from the intercept to be $0.9512\ \Omega$.

Figure 3.14 Plot of Z_{12} versus $1/I_E$ for R_E extraction

The extraction of R_B followed the technique proposed by Pavlidis [32]. In

his analysis, again from the small signal equivalent model, a term Z_b which was the impedance of the extrinsic base series inductance L_B in series with the base series resistance R_B was defined as:

$$Z_b = R_B + j\omega L_B \quad (3.29)$$

Furthermore, analytically, it was shown that Z_b can be obtained from the hybrid H -parameters as:

$$Z_b = \frac{H_{11}H_{22} - H_{12}H_{21} - H_{12}}{H_{22}} \quad (3.30)$$

Thus, by converting the measured S -parameters into H -parameters and calculating Z_b from equation (3.30), the base resistance R_B can be obtained from the real part of Z_b .

The plot of real part of Z_b versus frequency is shown in Figure 3.15. Here, the S -parameters data used were measured at $I_B = 0.5\text{mA}$ to 3.5mA in steps of 0.5mA and $V_{CE} = 3.0\text{V}$. Z_b was calculated by using LibraTM.

Figure 3.15 Plot of real part of Z_b versus frequency for extraction of R_B

In the above figure, the base resistance R_B was found to be bias dependent. At low base currents of 0.5mA and 1.0mA, R_B followed a different trend compared to the rest of the curves for reasons that are not known at the moment. However, at high base currents, the base resistance was very much constant over the bias and frequency. For the modelling purpose, an average value over the bias and frequency was taken for R_B as 1.5923 Ω .

3.4.2 Extrinsic Parasitics Parameter Extractions

There are 6 parameters in the extrinsic parasitics model, but only the base series inductance L_B , was extracted with a good degree of confidence. Although all of the extrinsic parasitics can be extracted as proposed by Costa [33], his technique required test structures that consisted only of the extrinsic structure without the transistor itself, which was not available for this work and therefore other technique were employed. Here, the extraction of L_B followed the similar technique for the extraction of R_B . Recall that in equation (3.29), the imaginary part of Z_b was $j\omega L_B$ and by plotting the imaginary part of Z_b versus frequency, L_B was extracted from the slope of the curve.

The plot of the imaginary part of Z_b versus frequency of the HBT used in this work is shown in Figure 3.16. Here, the S-parameter data were the same as in Section 3.4.1. The result shows a linear characteristic with frequency and insignificant deviation over the base current bias condition except at the lowest base current level. The curve was then fit to a straight line to determine an average value for the slope and was found to be 0.3619 j Ω /GHz. Subsequently, the base series inductor L_B was found to be

0.0576nH.

Figure 3.16 Plot of imaginary part of Z_b versus frequency for the extraction of L_b

3.4.3 Thermal Sub-circuit Parameter Extractions

There are 2 model parameters in the thermal sub-circuit, namely, the thermal resistance R_{TH} and the thermal capacitance C_{TH} . Only R_{TH} was extracted. The method used in extracting the thermal resistance followed the work done by Gupta [34]. The theory behind this technique is described below. In general, the overall DC current gain β is defined as follows:

$$\beta \equiv I_C / I_B \quad (3.31)$$

By assuming that the current gain β is linearly dependent with temperature, the above equation can be expanded into equation (3.32):

$$I_C(T_f) = \left[\beta_1 + \frac{\Delta\beta}{\Delta T} \cdot (T_f - T_1) \right] \cdot I_B \quad (3.32)$$

where T_j is the average device junction temperature, T_l is the temperature close to T_j where the linear approximation is made, β_l is the current gain at T_l and $\Delta\beta/\Delta T$ is the slope of the current gain versus temperature.

The thermal sub-circuit relates the junction temperature T_j and the thermal resistance R_{TH} by:

$$T_j = T_{base} + R_{TH}P_{diss} \quad (3.33)$$

Here, T_{base} is the base-plate temperature and P_{diss} is the DC device power dissipation.

Substituting the above expression for T_j into equation (3.32), it becomes

$$I_C(T_{base}, P_{diss}) = \left[\beta_l + \frac{\Delta\beta}{\Delta T} \cdot (T_{base} - T_l) + \frac{\Delta\beta}{\Delta T} \cdot R_{TH} P_{diss} \right] \cdot I_B \quad (3.34)$$

The above equation shows that I_C is a linear function of the base-plate temperature as well as the device power dissipation.

From the above equation, R_{TH} can be extracted as follows: First, by plotting I_C versus P_{diss} at a constant T_{base} while holding I_B constant, the slope of this plot gives the term $(\Delta\beta/\Delta T)R_{TH}I_B$ as depicted by equation (3.34). In order to obtain R_{TH} from this, the term $(\Delta\beta/\Delta T)I_B$ is needed to be calculated. This leads to the second part in which the plots of I_C versus T_{base} at constant P_{diss} and constant I_B are generated. From the slope of this plot, the term $(\Delta\beta/\Delta T)I_B$ can be obtained again depicted by equation (3.34). Finally, by dividing the value of the first slope by the second, R_{TH} is obtained.

The graph of I_C versus P_{diss} at several T_{base} while holding I_B constant is shown in Figure 3.17. In this measurement, the HBT chip was placed on top of a thin copper carrier and underneath it, a Peltier cooler was used to vary the base-plate temperature. The base-plate temperature was closely monitored.

Figure 3.17 The plot of I_C versus P_{diss} at different T_{base}

The base current was fixed at 2.5 mA for all of the measurements. For each value of T_{base} above, V_{CE} was varied from 2.0V to 4.5V in steps of 0.5V and I_C , P_{diss} were noted and plotted. The above curves in fact showed very linear characteristics as predicted by the theory. The slopes and y-intercepts at each T_{base} were extracted and given in Table 3.3 below.

T_{base} [°C]	Slope [mA/mW]	Intercept [mA]
26.4	-0.065705	69.983
35.8	-0.065323	66.783
46.0	-0.064585	63.197
59.4	-0.063204	58.752
72.4	-0.061437	54.485
86.0	-0.058872	50.190
95.9	-0.056884	47.215

Table 3.3 The extracted slopes and Y-intercepts for data in Figure 3.17

To plot I_C versus T_{base} at different P_{diss} for a constant I_B , the data were extracted from Figure 3.17. For one value of P_{diss} in Figure 3.17, I_C at each T_{base} can be calculated, since the slope and the Y-intercept of the all T_{base} lines are known. Then, the variation of I_C as a function of base-plate temperature, with P_{diss} as the parametric parameter, is plotted in Figure 3.18.

Figure 3.18 The plot of I_C versus T_{base} at different P_{diss}

Again, the above curves show linear characteristics and in fact, the straight lines of both figures verify the previous assumption that DC current gain, β , linearly varies as a function of temperature. Again, straight lines were fit to the data points, and the slopes and y-intercepts of the straight lines are tabulated in Table 3.4. From the slopes of Figures 3.17 and 3.18, the nominal thermal resistance R_{TH} was found to be approximately 190 °C/W.

P_{diss} [mW]	Slope [mA/°C]	Intercept [mA]
120	-0.32926	70.684
160	-0.32619	67.968
200	-0.32312	65.251

Table 3.4 The extracted slopes and Y-intercepts for data in Figure 3.18

3.5 Optimization Process and Modelling Results

The final step in device modelling is the optimization process. Generally in the optimization procedure, the device model is applied to a CAD tool with the unknown model parameters set as variables with assumed initial values. Then, DC responses as well as multiple bias small-signal AC responses are simulated and are matched to their corresponding measurements. This process is completed when the simulations agree with the measurements and the resultant parameter values lie within reasonable ranges. In an ideal situation where all model parameters can be extracted, optimization is usually carried out to further refine the parameter values. In this work, because many model parameters are still non-extractable, the optimization technique was used to approximate their values.

The CAD tool used for HBT modelling in this work was OSA90/HopeTM V2.5. It is a general-purpose microwave device modelling/circuit design tool that allows implementation of a complex user-defined model. Also, it has a wide selection of built-in optimization routines for device modelling and circuit design optimization. Concerning device modelling, it is understood that the built-in optimization routines perform best with the least number of unknown variables. Due to a large number of variables to be

optimized in the modified Gummel-Poon model, the optimization process was carried out in several steps to reduce the number of variables at each time. Without affecting the model, the optimization process was carried on in three steps, namely, DC optimization, small-signal AC optimization, and small-signal to large-signal conversion. Each step is described in more detail below.

3.5.1 DC Optimization

Initially in the optimization process, model parameters that affect the DC responses were first optimized and obtained. By optimizing only to the DC characteristics, parameters that affect the AC responses such as capacitors and inductors could be ignored temporarily. Here, the DC parameters included the series resistances, saturation currents and their temperature dependent parameters, ideality factors, forward current gain and those temperature dependent parameters, reverse current gain and finally, the thermal resistance. With the extracted parameters set as variables with tight constraints while allowing loose constraints for the non-extractable parameters, the model was optimized until the simulations agreed with the DC measurements such as I_C versus V_{CE} characteristic, V_{BE} versus V_{CE} characteristic, forward and reverse Gummel plots.

The simulated and measured I_C versus V_{CE} characteristic (I_B of 0.0mA to 3.5mA in steps of 0.5mA) are shown in Figure 3.19. In Figure 3.20, the simulated and measured V_{BE} versus V_{CE} characteristics for I_B from 0.5mA to 3.5mA in steps of 0.5mA is given. In addition, the simulated versus the measured forward and reverse Gummel plots are shown in Figure 3.21 and 3.22 respectively.

Figure 3.19 The simulated and measured I_C versus V_{CE} characteristics

Figure 3.20 The simulated and measured V_{BE} versus V_{CE} characteristics

Figure 3.21 The simulated versus measured forward Gummel plot

Figure 3.22 The simulated versus measured reverse Gummel plot

From the above results, the simulated DC responses agreed reasonably well with the measurements except for the I_E component in the reverse Gummel plot. This is because during the optimization process, the weighting factor for the reverse Gummel plot was set low to obtain better fits for other responses as compromises. Since the transistor is usually operated in the forward active region, the inaccuracy of I_E above in the reverse bias region can be tolerated.

The optimized results for the DC parameters are shown in Table 3.5.

Parameter	Extracted Value	Optimized Value
I_{SAT0}	1.6889e-22 A	2.0224e-22 A
I_{SDE0}	1.1354e-18 A	1.2017e-18 A
I_{SDC0}	2.4752e-14 A	3.2573e-14 A
XTI		6.4961
E_g		1.4162
n_f	1.1294	1.1473
n_r	1.0267	1.1204
n_e	1.5484	1.5741
n_c	1.7398	1.7664
R_R	1.5923 Ω	1.6952 Ω
R_F	0.9512 Ω	1.0796 Ω
R_C		1.1884 Ω
β_{fo}		46.3854
XTB		1.2252
E_{mf}		0.0545 eV
β_r		0.1680
R_{TH}	190 $^{\circ}\text{C}/\text{W}$	188.195 $^{\circ}\text{C}/\text{W}$

Table 3.5 The optimized parameter values resulted from DC optimization

3.5.2 Small-Signal AC Optimization

Now, with the DC parameters obtained earlier fixed at their optimized values, the parameters that affect AC responses are to be optimized and obtained by

fitting the simulated small-signal S -parameters to the measured data over a wide range of bias conditions. These AC parameters include extrinsic parasitics, non-linear capacitances, transit time delay and the thermal capacitance. The extrinsic parasitics are constant parameters throughout the bias ranges. The non-linear capacitances can be modelled here as linear capacitors because of the small-signal excitation. Over a wide range of bias conditions, these non-linear capacitances become bias-dependent linear capacitances. The excess time delay is also a bias-dependent parameter. The thermal capacitance was set at a large value of $1.0\mu\text{J}/^\circ\text{C}$ throughout the optimization exercise because the thermal time constant is in the order of μsec . These parameters and their corresponding circuit elements were applied to the existing model and the small-signal AC optimization process was performed.

Initially, the extrinsic parameters were obtained through fitting the simulated S -parameters to the measured S -parameters for five bias points simultaneously. These bias conditions were chosen to include high, medium and low I_B and V_{CE} biases to allow large variation in the bias conditions during the fitting process to obtain a more realistic set of extrinsic parameters. After the simulated S -parameters agreed reasonably well with the measurements (from 0.4GHz to 40GHz) for all five bias conditions, the optimized values of the extrinsic parameter are as shown in Table 3.6 below.

Parameter	Extracted Value	Optimized Value
L_B	0.0576 nH	0.0623 nH
L_C		0.0540 nH
L_E		0.0023 nH
C_{EY}'		0.1339 pF
C_{BC}'		0.1333 pF
C_{CE}'		0.0974 pF

Table 3.6 The optimized extrinsic parasitics values

Then, with the extrinsic parameters fixed at above values, the bias-dependent parameters were obtained again by fitting simulated S -parameters to the measured S -parameters but at one bias point at a time. At each bias point, after the simulated S -parameters agree reasonably well with the measurement, the optimized values of the bias-dependent parameters for that bias were obtained. This process was repeated over a total of 42 bias points in the forward active region (i.e. I_B from 1.0mA to 3.5mA step of 0.5mA and V_{CE} of 1.5 V to 4.5 V step = 0.5 V). The optimized bias-dependent parameters; namely, base-emitter capacitance C_{BE} , base-collector capacitance C_{BC} and the excess time delay τ obtained from the small-signal AC optimization are shown in Figures 3.23, 3.24 and 3.25 respectively. It can be seen that the optimized bias-dependent parameters followed a consistent trend which behaved as physically expected.

Figure 3.23 The bias dependent characteristics of C_{BE}

Figure 3.24 The bias dependent characteristics of C_{BC}

Figure 3.25 The bias dependent characteristics of delay τ

3.5.3 Small-Signal to Large-Signal Conversion

The HBT model obtained thus far is merely a bias-dependent model and not yet a complete large-signal model. In fact, it is sometimes referred to as the quasi large-signal model. In order to obtain the true large-signal HBT model, the parameters for the non-linear capacitances (i.e. C_{JE} , V_{JE} , M_{JE} ...etc.) must be obtained. Here, these parameters were obtained by fitting the above bias-dependent characteristics for C_{BE} and C_{BC} to their corresponding non-linear equations given in Section 3.3.1. In other words, the capacitance evaluated from the non-linear equation at a particular bias should agree with the corresponding bias-dependent value. As a result, the optimized non-linear capacitances parameters are given in Table 3.7 below. Because the bias-dependent characteristics were evaluated only in the forward active region, the diffusion capacitance for C_{BC} cannot be obtained and was omitted for the model. Furthermore, due to the program limitation in OSA90/HopeTM, only a single value was allowed for the bias-dependent excess delay τ and therefore it was not matched to some forms of equations.

Parameter	Optimized Value
τ_{μ}	8.2152 psec
XTF	0.5897
VTF	2.8704 V
C_{JE}	0.4002 pF
V_{JE}	2.0452 V
M_{JE}	0.3333
C_{JC}	0.1970 pF
V_{JC}	1.5240 V
M_{JC}	0.5000

Table 3.7 The optimized parameters for the non-linear capacitances

Finally, the corresponding non-linear charge equations for the

capacitances were implemented in OSA90/Hope™ and the large-signal HBT model was obtained. The non-linear charge equations were similar to SPICE equations and were provided by Optimization Systems Associates Inc. The overall model circuit netlist can be found in Appendix III. Using this large-signal model, DC characteristics were simulated and compared with the measurements. The results were found to be identical to the ones given earlier in Section 3.5.1 as expected. Furthermore, using the large-signal model, multiple bias S -parameters mainly in the active region were simulated and compared to the measurements with frequency range from 0.4GHz to 40GHz in steps of 0.4GHz. For each bias in the above simulations, the excess delay τ took on a single value obtained from its bias-dependent characteristics at the corresponding bias. Here, three typical biases of the above S -parameters comparisons are shown in Figures 3.26, 3.27 and 3.28. From Figures 3.26, 3.27 and 3.28, the agreement between the simulated and measured S -parameters was found to be acceptable at frequencies up to 30 GHz. In fact, similar agreements are found for all bias points (42 points) that were simulated. At higher frequencies beyond 30.0 GHz, however, the accuracy of the model degraded and thus resulted in larger discrepancies between simulations and measurements.

At this point, a large-signal HBT model has been obtained through a parameter-extraction and optimization process. It is capable of predicting DC characteristics such as the I_C and V_{BE} versus V_{CE} characteristics, and the forward Gummel plot. In addition, it can also predict multiple biases of S -parameters responses in the forward active region with acceptable accuracy up to 30GHz. In the following Subsection, the large-signal performance of the model will be examined.

Figure 3.26 The simulated versus measured S -parameters at $I_B = 0.5\text{mA}$, $V_{CE} = 4.0\text{V}$

Figure 3.27 The simulated versus measured S -parameters at $I_D = 1.5\text{mA}$, $V_{GS} = 3.0\text{V}$

Figure 3.28 The simulated versus measured S -parameters at $I_B = 2.5\text{mA}$, $V_{CE} = 2.0\text{V}$

3.5.4 Large-Signal Model Verification

In the above modelling process, the large-signal HBT model was obtained through fitting only to DC and small-signal AC measurements. It is therefore of interest to see if the large-signal model characteristic is valid. In order to verify the large-signal characteristics of the model, several non-linear measurements were performed on the $360\mu\text{m}^2$ HBT device. These measurements included output power versus input power characteristic at both class A bias ($I_B = 1.5\text{mA}$, $V_{CE} = 3.0\text{V}$) and class AB bias ($I_B = 0.5\text{mA}$, $V_{CE} = 4.0\text{V}$), and also the load-pull measurements [35].

In the output versus input power characteristic measurement, the HBT chip was wafer-probed using the microwave ground-signal-ground probes. An HP8350A sweep oscillator was connected to the bias tee which, in turn, was connected to the input probe. At the other side, the output probe was connected to another bias tee which in turn connected to a band-pass filter (0.2 to 18GHz passband). Finally, the HP437B power meter was connected to the bandpass filter output to measure the output power.

After the HBT was biased correctly with the input frequency set at 14.0GHz, the input power was manually swept and the corresponding output power was measured. Also, with the same operating conditions, the output power versus input power characteristics were simulated. The measured and simulated output power characteristics versus the input power level for both class A and class AB are shown in Figure 3.29. From Figure 3.29, in the linear region, the simulation agreed well with the measurement for class AB bias, yet a 0.8dB discrepancy was found between the simulation and measurement for class A bias. As indicated, when the device was driven

2 of/de 2

PM-1 3½"x4" PHOTOGRAPHIC MICROCOPY TARGET
NBS 1010a ANSI/ISO #2 EQUIVALENT

PRECISIONSM RESOLUTION TARGETS

into saturation, the simulations were still in acceptable agreement with the measurements for both biases.

Figure 3.29 Simulated and measured P_{out} versus P_{in} characteristics of $360 \mu\text{m}^2$ HBT

Load-pull measurement of the $360 \mu\text{m}^2$ HBT was performed at École Polytechnique of Montréal using a six-port, active load-pull system [35]. In this measurement, the HBT was biased at class A operation of $I_B=1.5\text{mA}$ and $V_{CE}=3.0\text{V}$ and the operating frequency was set at 14.0GHz . Furthermore, the input power absorbed by the device was adjusted to a constant 12.0dBm for each load condition. By varying the output load, the output power was measured at each load point and from these measurement points, a family of constant output power contours of 12.0 to 16.0dBm were interpolated as shown in Figure 3.30.

Again for the same operating conditions as in the case of the measurement,

the load-pull simulation in OSA90/Hope™ was performed for each load point. The result showed a maximum of 0.8~1.5dB discrepancy between the simulated and the measured output power.

Figure 3.30 The measured active load-pull contours of $360\mu\text{m}^2$ HBT

3.6 Summary

In this chapter, the procedure of obtaining the large-signal HBT model has been described. Initially, the principle of HBT operation and its common characteristics were introduced. Then, from the literature, the modified Gummel-Poon model topology

appropriate for HBT was established. At the beginning of the modelling process, some parameter extraction techniques were described. Due to the large number of model parameters which could not be extracted from measurements, the model fitting procedure was partitioned into DC, small-signal AC and large-signal conversion steps. In the end, the large signal HBT model capable of predicting DC characteristics and multiple bias small-signal *S*-parameters was obtained. In verifying the large-signal characteristics of the model, some large signal measurements such as output versus input power and load-pull were performed. The comparison between the large-signal measurements and model simulations showed a maximum discrepancy of 1.5dB output power.

CHAPTER 4: POWER AMPLIFIER DESIGN

4.1 Introduction

As shown in Figure 4.1, a microwave transistor amplifier consists mainly of the input source impedance network Z_S , the transistor and the output load impedance network Z_L . The main work in designing an amplifier is thus to find the optimum source and load impedances for the transistor to satisfy a given set of performance specifications. For example, typical requirements for a low noise amplifier are low noise figure and high gain within the operating frequency bandwidth. On the other hand, a power amplifier is required to achieve optimum output power, high gain and/or high efficiency at a certain range of input power level. By properly selecting source and load impedances for a particular design, desired amplifier performance can be achieved.

Figure 4.1 The circuit diagram of a microwave amplifier

In designing a linear amplifier, small-signal S -parameters of the transistor can be used, as the complete theory and systematic procedure behind S -parameter amplifier design are well established [14]. Furthermore, with the sophistication of

today's network analyzers, S -parameters of the transistor can be easily characterized to facilitate the design of a small-signal amplifier.

In the case of a power amplifier, however, small-signal S -parameters can no longer be used because it predominantly operates in a non-linear mode. Although in practice, small-signal S -parameters are sometimes used for designing class A power amplifiers, strictly speaking, this approach is not appropriate. For instance, Cripps [36] has shown that an extra 2~3dB of output power can be achieved for class A power amplifier when it is tuned for output power instead of using small-signal S -parameter design. Therefore, small-signal S -parameters alone cannot be used to properly design an optimum power amplifier. Instead, a set of power dependent large-signal S -parameters is needed. Unfortunately, large-signal S -parameters are not properly defined when higher harmonics are present and large-signal measurements such as the load-pull technique is generally difficult and equipment oriented. For this reason, non-linear CAD techniques and optimization features are the most popular method for designing power amplifiers.

4.2 Circuit Fabrication Technology

In this design, Microwave Integrated Circuit (MIC) technology was chosen for the amplifier circuit fabrication because it is readily offered with CRC's in-house process. In addition, it is inexpensive and requires little processing time. This technology is straightforward as compared to Miniature Hybrid Microwave Integrated Circuit (MHMIC) and Monolithic Microwave Integrated Circuit (MMIC) technology. In MIC technology, only a metal layer which forms transmission lines and distributed

matching elements are deposited onto the substrate and then etched by photolithography. Lumped passive elements and discrete active devices are subsequently epoxied or soldered onto the substrate and bond wires are used for the inter-connections.

A wide variety of dielectric substrates are available for microwave circuit fabrication and among them, substrate with high dielectric constant are preferable for circuit applications because of lower radiation loss. In this application, 10mil thick alumina (Al_2O_3) substrate with a dielectric constant, ϵ_r , of 9.8 and dielectric loss tangent, $\tan\delta$, of 0.001 was used. Gold of $2.0\mu\text{m}$ thickness with resistivity of $2.44 \times 10^{-8} \Omega\text{m}$ was employed as the metal layer. Furthermore, the width of a 50Ω characteristic impedance line using the above substrate was calculated by LinecalcTM [37] to be approximately $245.0\mu\text{m}$. Finally, the bond wires used for inter-connections had an inductance of approximately 0.8 nH/mm .

4.3 Amplifier Design

The design criteria of the HBT power amplifier are as follows. The amplifier is to operate at a centre frequency of 14.0GHz and the main requirements are to provide optimum output power with acceptable gain. In this case, the bandwidth and efficiency of the amplifier are not of main concern.

Due to the gain requirement, class A amplification is the most suitable for this design since it offers both high gain and output power among class A, AB and B operations. From the I_C versus V_{CE} characteristic of the HBT, a quiescent point (Q point) of base current I_B of 1.5mA ($V_{BE} = 1.40\text{V}$) and collector voltage V_{CE} of 3.0V ($I_C =$

34.5mA) was chosen as shown in Figure 4.2. Here, $I_{C,MAX}$ is about 90mA and $V_{CE,MAX}$ are 1V and 5V respectively and from equation (2.4), the theoretical maximum linear RF output power was calculated to be about 16.5dBm. In general, higher output power can be achieved by biasing the transistor at higher current and voltage. However, this may result in too much self-heating and breakdown of the HBT, which in turn degrade the reliability of the transistor and hence the circuit.

Figure 4.2 The Q point for class A power amplifier

Usually at this stage, the design starts with the DC characteristic and the small-signal S -parameters (as described in Chapter 2), and the initial source and load impedances are obtained. Together with the device non-linear model implemented in the CAD tool, these impedances can be further optimized to meet a certain output power requirement. In practice, the output power requirement is usually specified as a limitation

on the first order power compression point (i.e. $P_{1dB} \geq 18.0\text{dBm}$). After the optimum source and load impedances are obtained, matching and biasing networks are designed and the first design cycle is completed.

Here, however, the requirement is to achieve the optimum output power and this adds an extra degree of difficulty in the optimization process. The practical solution is thus to perform a load-pull simulation on the HBT non-linear model to generate a family of constant-power contours, from which the source and load impedances corresponding to the optimum output power can be readily obtained. The design can thus be carried out using these contours. The advantage of this approach is that it provides insight into output power variation as a function of input and output impedance changes.

Ideally, at a particular input power level and an initial source impedance of 50Ω , the output power contours are generated by sweeping the load impedance across the entire Smith chart. The optimum load impedance is then found. Now, keeping the load impedance at its optimum value, the source impedance is swept across the entire Smith chart. The optimum source impedance is thus obtained. This process is repeated for several iterations until the source and load impedances converge to fixed values. As a result, the optimum source and load impedances are obtained for one input power level. For different input power levels, the process can be repeated and the optimum source and load impedances can be determined for the 1dB compression point. When the above process was performed, however, during the source-pull simulation, a convergence problem occurred and the corresponding contours could not be generated. This was

mainly due to the complexity of the user-defined HBT model, which caused computational (numerical) overflow or underflow.

Instead, to minimize the convergence difficulties in simulation, the source impedance was conjugately matched from small-signal S -parameters for each output load. This should still yield fairly close results relative to the conventional method. Initially, an arbitrary load impedance Z_L was selected, the source impedance Z_S was conjugately matched as follows. First, the load reflection coefficient Γ_L was calculated from [14]:

$$\Gamma_L = \frac{Z_L - Z_o}{Z_L + Z_o} \quad (4.1)$$

Then, the input reflection coefficient Γ_{IN} (looking into the transistor from the input) was calculated by:

$$\Gamma_{IN} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \quad (4.2)$$

where the S -parameters used in the above equation are the simulated S -parameters at 14.0GHz at class A bias. Once Γ_{IN} was found, Γ_S (looking into the input from the transistor) which is given by its complex conjugate (i.e. $\Gamma_S = \Gamma_{IN}^*$) was calculated and finally, the input load Z_S was found by:

$$Z_S = \frac{1 + \Gamma_S}{1 - \Gamma_S} \quad (4.3)$$

With the input power level kept at 7.0dBm at 14.0GHz, the output power was simulated and recorded. Then, a new Z_L was selected and the process was repeated. The load impedance Z_L was varied (load-pull) to cover the entire Smith chart. Only certain output power levels were selected and plotted on the Smith chart as shown in Figure 4.5. Shown in Figure 4.5 is a family of power contours on the Smith chart. Still,

it was found that when the load impedance is close to the edge of the Smith chart, convergence difficulty occurred in the harmonic balance simulation and therefore no result was obtained in that region.

Figure 4.3 The load-pull simulation result (input power = 7.0dBm @ 14.0GHz)

The CAD tool used for the above implementation was again OSA90/Hope™ V2.5. The detailed circuit file listing for the simulation is given in Appendix III. Note that such a load-pull simulation could not be implemented in Libra™ or Microwave harmonica™ at the time due to their limitations. From the data, the optimum power point can be readily obtained. The optimum load impedance Z_L at the maximum output power point was found to be $12.0 + j17.5 \Omega$ and the corresponding source impedance was $1.32 - j4.28 \Omega$. These loads correspond to a maximum output power of 17.4 dBm with a power gain of 10.4 dB. The load-pull simulation was repeated

for 8.0 and 9.0dBm of input power and the optimum source and load impedances were found to be identical as before. However, the power gain decreased as the amplifier begins to saturate. Finally, the source and load impedances obtained above are close to the values obtained by applying simple theory from the example given in Chapter 2.

4.4 Matching Network Design

A matching network is generally used to provide maximum power transfer between two different impedances in a microwave amplifier design. As shown earlier, Figure 4.1 illustrates the typical situation for the need of matching networks in a microwave amplifier. In Figure 4.1, the input of the transistor is to be matched to the 50 ohms source impedance via the input matching network so that maximum power is delivered from the source V_S to the transistor. Consequently, low loss, and thus high Q elements, should be used in the construction of the matching networks. If for some reason, the input matching network is not present, mismatches occur and only a portion of the input power is delivered to the transistor. The rest of the power reflects back to the source and results in inefficiency or even damage to the source. Similarly, the output matching network ensures the maximum power transfer from the transistor output to the 50 Ω load.

After the optimum source and load impedances were obtained, the matching networks were designed. Microstrip lines are widely used in building microwave matching networks because of their excellent performance characteristics and because they can be easily and precisely fabricated on a substrate. At 14.0GHz, lumped

elements such as multilayer capacitors and chip-inductors typically have significant losses and large component tolerances. Therefore, lumped elements were not considered for the matching networks. Specifically, transmission lines and open circuit stubs were used for matching. The main reason that short-circuit stubs are seldom used is that they are more difficult to tune than the open circuit stubs, and physically require more fabrication steps. In the following sections, the design of input and output matching network are discussed.

4.4.1 Input Matching Network

The optimum source impedance Z_S to be presented to the input of the transistor was found to be $1.32 - j4.28 \Omega$. This is a relatively low impedance to be matched to a 50 ohms source. As a general rule, the lower the impedance, the more difficult the task is in matching network design. Initially, the single balanced stub matching network was designed and it was found that it offered too narrow a bandwidth and was rejected. In order to achieve a wider bandwidth, the quarter-wave transformer in conjunction with balanced stubs were used. Yet, the line widths needed for the quarter-wave transformer were found to be too wide to be practical. Finally, a double balanced stub matching network was selected, although a narrow bandwidth resulted.

The procedure in designing the double stub matching network is as follows. Typically, a tentative double stub matching procedure is as shown on the Smith chart in Figure 4.4. Starting with Z_S on the Smith Chart at point A, the matching network must bring the impedance to the centre of the Smith Chart (50 ohms) at point E. From

point A, the effect of the bond wires (typically two in parallel) was modeled as a single inductor. Each bond wire was estimated to be about 0.31 mm long thus giving 0.25 nH ($0.31 \text{ mm} \times 0.8 \text{ nH/mm}$) of inductance. With two equal length bond wires in parallel, the total inductance should be halved, yet, a ratio of 0.6 was found to be more accurate as found from a CRC's in-house study. This resulted in a total bond wire inductance of 0.15 nH. The effect of this inductor on the Smith chart is the transformation of impedance from point A to point B. Immediately, a balanced capacitive stub followed and moved point B along a constant admittance circle to point C. Then a transmission line which follows a constant VSWR circle on the Smith Chart was used to move the impedance from point C to point D. Finally, a second set of capacitive stubs brought the admittance of the network to the centre of the Smith chart.

Figure 4.4 Input double stubs matching on the Smith chart

With the aid of a Z-Y Smith chart, the approximate transmission line and

stubs lengths can be readily obtained. For the path from B to C, the change in normalized admittance was about $j2.4$. In a balanced stub configuration, the top and the bottom lines are effectively in parallel and either stub contributed to half of the total admittance or equivalently, $j1.2$. Each stub length was found to be about 0.139λ from the Smith chart. For the path from C to D, the transmission line length was found to be 0.374λ . Finally, the second set of balanced stubs (path D to E) required 0.125λ for the length of each. The wavelength λ above is the effective wavelength in the microstrip line and was found (by LinecalcTM) to be about $8341\mu\text{m}$. Thus, the calculated lengths of the above stubs and line were found to be $1159\mu\text{m}$, $3120\mu\text{m}$ and $1043\mu\text{m}$ respectively. These lengths were then applied to the CAD tool and further optimized. Note that a DC blocking capacitor and extra line were added to the matching network. The resulting dimensions of the input matching network after optimization are shown in Figure 4.5.

Figure 4.5 Optimized dimensions of the input matching network

4.4.2 Output Matching Network

The output matching design involves similar steps as the input matching

network. The optimum load Z_L was found to be $12 + j17.5\Omega$ using the load-pull simulation. A single stub was chosen for the output matching network, and the matching procedure is as shown in Figure 4.6.

Figure 4.6 Output single stub matching on the Smith chart

Again, the effect of the bond wires was modeled as a 0.15nH inductor and its effect on the Smith Chart is the transformation of impedance from point A to point B. Then, a transmission line was used to move the impedance from point B to point C. Finally, a balanced capacitive stub was followed and its effect is shown in path C to D.

The approximate line lengths were obtained from a Z-Y Smith chart as before. The transmission line and the balanced stub lengths were found to be $721\mu\text{m}$ and $876\mu\text{m}$ respectively. These lengths were also applied to the CAD tool and further optimized. As before, a DC blocking capacitor and extra line were added to the matching network. The resulting dimensions of the output matching network after optimization are

shown in Figure 4.7.

Figure 4.7 Optimized dimensions of the output matching network

4.5 Bias Network Design

The bias networks are important part of an active microwave circuits. Without a proper bias network, the amplifier will not function as designed and, in the worst case, oscillation can occur in practice. The key function of a bias network is to provide the DC bias to the transistor without influencing the amplifier's RF performance and, at the same time, to isolate the RF energy generated by the amplifier from the DC power supply. In ideal or lumped-element form, a bias network consists of large-value inductors and capacitors. Figure 4.8 shows the structure of the ideal bias tee circuit. At DC, the inductor is a short circuit and the DC current can flow to the terminal of the device while the capacitor is an open circuit and does nothing to influence that current. At microwave frequencies, the inductor presents a high impedance thus blocking the microwave signal through this path while the capacitor presents a very low impedance therefore shorting out any leakage signal to the ground instead of to the DC source.

At higher frequencies (above 10 GHz), ideal lumped inductances and capacitances are difficult to achieve thus transmission line elements are used. Shown in

Figure 4.9 is a quarter-wave section bias network that is widely utilized to provide DC bias at microwave frequencies.

Figure 4.8 The structure of the ideal biasing network

Figure 4.9 The quarter-wave sections biasing network

Here the bias network behaves as an open to the main circuit at the frequency of interest. This is achieved by having a physical open circuit at the end (point A) and two quarter-wave ($\lambda/4$) transmission line sections. The first quarter-wave section is usually made of low impedance line to increase bandwidth and transforms the open to a short circuit at point B. The other quarter-wave section transforms the impedance back to an open circuit looking in from point C. It is usually made of high impedance line to

further reduce the RF energy flowing in the bias network. It is generally good practice to place the DC bias line at the voltage minimum (short circuit) for minimum interference. Thus, the DC bias line is placed at one side of point B. On the other side of point B, a capacitor in series with a 50 ohms resistor to ground is used to stabilize the transistor and suppress low frequency oscillation due to high transistor gain at low frequency. Also, point C of the bias network is usually connected to a voltage minimum of the main RF circuit to minimize interference.

The initial dimensions of the bias network were calculated and then applied to OSA90/HopeTM to have the line lengths optimized. The final dimensions of the bias network are shown in Figure 4.10. The bias network obtained here was used at both the input and the output of the amplifier.

Figure 4.10 The physical dimensions of the biasing network

The frequency response of the bias network is shown in Figure 4.11. It acts as an open circuit (i.e. magnitude of $S_{11} \sim 1.0$, phase of $S_{11} \sim 0$) near the operating

frequency of 14.0GHz as desired.

Figure 4.11 The frequency response of the biasing network

4.6 Network Integration and Design Iterations

After the matching and the bias networks were designed, these individual circuits were integrated together and the overall amplifier performance examined. Because these networks were designed mainly at the operating frequency, their integrated effects at other frequencies are not known. It is therefore important that the amplifier be studied in a range much wider than the bandwidth of interest. Specifically, circuit stability out of band must be carefully studied. The design must be corrected until it is stable at all frequencies.

The integrated amplifier circuit was implemented in OSA90/HopeTM and preliminary *S*-parameters responses of the power amplifier were simulated. The result is

shown in Figure 4.12.

Figure 4.12 The simulated S parameters of the power amplifier

From the simulation, it was seen that the amplifier performs reasonably well at the centre frequency of 14.0GHz. It had a small signal gain of 10.4dB and good input match. The output match was about -7.0dB since the amplifier was tuned for optimum output power. However, the 20dB gain near 1~2GHz range was undesirable because, in general, an amplifier should have the highest gain near the operating frequency. In addition, the magnitude of S_{11} was greater than 0dB in that frequency range. With such high gain and large reflection coefficient, it is very likely that the amplifier will oscillate in that frequency range. As a confirmation, the stability factor K was also simulated and the result is shown in Figure 4.13.

Here, the K factor was much less than 1 in the 1~2GHz frequency range.

This confirmed that the amplifier would likely oscillate. Hence, this amplifier topology will not operate properly and must be redesigned.

Figure 4.13 The stability factor of the amplifier

One solution to lower the gain in the low frequency region is to add a high pass filter in front of the input or after the output of the amplifier. Such a high pass filter can take on the form of a capacitor in series connection. Since the DC blocking capacitors will be used at those locations, they can be selected for the high-pass filtering purpose. The capacitor value was iteratively found to be 0.18pF to effectively suppress the low frequency gain. Since the impedance of the capacitor is now significant, the input and output matching networks were re-optimized. Again for the second iteration, the amplifier *S*-parameters and the *K* factor were simulated.

It was found from the above simulation that the low frequency gain was completely removed as desired. However, the *K* factor was still less than 1 and it was not

satisfactory. Hence, more work was still required in the design of the power amplifier.

In general, in order to stabilize a circuit, some form of loss is introduced to the circuit. However, this loss should not hamper performance at the frequency of interest. Since it is known that the bias network does little to influence the circuit at the operating frequency, it is best to introduce some loss here. Recall that in the biasing network (Figure 4.9), there is already a stabilizing circuit consisting of a resistor in series with a capacitor. The important point to realize is that this resistor is effectively in parallel with the transistor at low frequencies. Therefore, in order to introduce loss, the value of the resistor is to be decreased.

With a $10\ \Omega$ resistor for the biasing network, the amplifier S -parameters and the K factor were again simulated and were found to be satisfactory. The simulated results are shown in Figure 4.14 and 4.15 below. The circuit file for the above simulations is given in Appendix IV. In Figure 4.14, the low frequency gain was removed and the magnitude of S_{11} was less than 0dB over the whole frequency range. Also, the amplifier gain at operating frequency was unaffected. In addition, the K factor in Figure 4.15 showed that the amplifier is unconditionally stable at all frequencies.

Using this final circuit file, the large signal performance of the amplifier was also simulated. The simulations included the output power versus input power characteristic and the power added efficiency as a function of the input power. The results will be shown in Chapter 5 (Figure 5.9 and 5.17) where they are compared with the measurements. The final dimensions of the overall amplifier circuit are shown in Figure 4.16.

Figure 4.14 The S-parameter of the third iteration design amplifier

Figure 4.15 The K factor of the third iteration design amplifier

Figure 4.16 The final circuit dimensions of the HBT power amplifier

The amplifier structure was laid out using DW-2000, a CAD software for circuit layout purpose. After the circuit mask was made, the amplifier substrate was etched by CRC's in-house thin film processing. Via holes and a rectangular slot were drilled. The transistor and lumped components were then epoxied onto the substrate and the metal carrier. Finally, bond wires were used for interconnections. A photograph of the amplifier's physical structure is shown in Figure 4.17. The actual size of the amplifier circuit is about $0.8\text{cm} \times 1.5\text{cm}$.

4.7 Summary

In this Chapter, steps involved in the design of a 14.0GHz HBT class A power amplifier circuit were described. The amplifier utilizes the MIC circuit fabrication technology. Initially, load-pull simulation was performed to obtain the optimum input and output impedances to achieve the optimum output power requirement. With these

impedances obtained, the matching networks were designed. The bias network was also designed. These networks were then integrated together to complete the design of the amplifier. The design was thoroughly simulated and modified to ensure unconditional stability. The modifications involved lowering the value of the DC blocking capacitor and adding resistive loss to the bias networks.

Figure 4.17 The physical layout of the amplifier circuit

CHAPTER 5: AMPLIFIER RESULTS AND DISCUSSIONS

5.1 Introduction

In this chapter, the preliminary measurements on the HBT power amplifier and the accompanying results are discussed. Although the small-signal S -parameter response is not within the specifications of a power amplifier, it is useful when visualizing the amplifier performance and stability over a wide range of frequency. In practice, the small-signal S -parameters are always measured first to see whether the amplifier is working properly. In the case of an amplifier that does not appear to operate as expected, tuning is usually performed at this stage and other subsequent measurements can then be made.

Other than the small-signal response of the amplifier, important characteristics that characterize a power amplifier are the output-power-versus-input-power characteristic, amplifier power gain, linearity, intermodulation distortion products and power-added efficiency. The first order power compression point P_{1dB} , obtained from the output power versus input power characteristic, is generally used to determine the power handling capability of the amplifier. Consequently, P_{1dB} also defines the upper limit of the dynamic range of the amplifier. The second harmonic ($2f_o$) content is generally used to evaluate the linearity of the amplifier. In the case of this amplifier, the second harmonic content can be easily filtered out and will not be discussed. Meanwhile, the third-order intermodulation characteristic is a measure of in-band multiple-tone distortion which is an important source of distortion in a power amplifier. As a rule of thumb, a good power amplifier typically has intermodulation products of about 20dB

below the carrier level at P_{1dB} . Finally, amplifier power gain and power added efficiency are figures of merits that describe the amplifier performance. Each of these characteristics was measured and compared with simulation where possible. The discrepancies between simulations and measurements are discussed and corrections are proposed.

5.2 Amplifier Biasing

Figure 5.1 shows the physical structure of the amplifier circuit mounted on the Wiltron universal test fixture. The input and the output of the test fixture consisted of K to V adapters which can be connected to other test instruments such as a network analyzer. The inner sides of the test jig consisted of V type connectors whose centre conductors were pressed against the input and output of the amplifier to provide contact. The HBT device was DC biased through the pair of bias wires which are epoxied to the DC bias pads of the amplifier circuit and connected to the DC current and voltage sources.

Figure 5.1 Mounting of the amplifier onto the universal test fixture

Before any measurement can be performed on the amplifier circuit, the active device (in this case, the HBT) must be biased correctly at the intended DC operating condition. Such verification is performed in practice to ensure that the device has not been damaged through handling or aging. In this case, the HBT was biased through the HP4142B DC biasing network with the base side (amplifier input) at a constant current of 1.5mA and the collector side (amplifier output) at a constant voltage of 3.0V. With the above bias conditions, the collector current was measured and found to be approximately 11mA. This collect current contradicted the expected value of 35mA from the usual I_C versus V_{CE} curves. To investigate this problem, with the same experimental setup as above, the I_C versus V_{CE} characteristic with the base current I_B from 0 to 3.5mA in steps of 0.5mA was measured and the result is shown in Figure 5.2.

Figure 5.2 Measured HBT I_C versus V_{CE} characteristic on the amplifier circuit

The above figure indeed showed a poor I_C versus V_{CE} characteristic. From the status report of the measurement system, it revealed that oscillation has occurred. It was believed that this oscillation occurred at a low frequency (about several tens of MHz) and was perhaps due to the high gain and potentially unstable characteristic of the HBT at low frequencies.

In order to suppress the low frequency oscillation, ring-shaped ferrite beads and external HP bias tees were added at the input and output DC bias wires. It is known that the ferrite beads acts as high-pass filters and in effect, the low frequency oscillation was blocked from the DC sources. Furthermore, the use of external bias tees was found to be helpful to further stabilize the device. The I_C versus V_{CE} characteristic was re-measured on the amplifier circuit, and the familiar result is shown in Figure 5.3.

Figure 5.3 HBT I_C versus V_{CE} characteristic with ferrite beads and external bias tee

Although Figure 5.3 shows a much better I_C versus V_{CE} characteristic, from the comparisons between the above characteristic to the usual HBT I_C versus V_{CE} characteristic in Chapter 3, it was found that the collector current from the above amplifier measurement was still lower than the usual HBT measurement. A noted maximum of 10mA reduction in collector current was observed. This may have been caused by excessive heating of the HBT during assembly, resulting in degradation of the DC current gain β and thus lower collector current. Another possible reason may be due to the substrate carrier imposing extra series and/or thermal resistances that may degrade the collector current. Much effort was spent investigating this problem with no solid improvement. The main effect of this problem would likely be some degradation in RF gain and output power.

5.3 Small-signal S -parameters Response

Once the DC operating condition has been made stable, subsequent amplifier characteristics can readily be measured. The first measurement performed on the amplifier was the small-signal S -parameter response. The experimental setup was as shown in Figure 5.4. Here, the amplifier (D.U.T.) was secured by the Wiltron test fixture and the input and output of the test fixture were connected directly to the HP8510C network analyzer. Furthermore, the amplifier DC bias was supplied by the HP4142B DC biasing network which was in turn controlled by an HP computer running the Interactive Measurement Analysis (IMA) software. For simplicity, the ferrite beads and external HP bias tees between the DC biasing network and the D.U.T. are not shown in the diagram.

They were however present for all amplifier measurements.

Figure 5.4 The experimental setup for amplifier *S*-parameters measurement

Initially, the through-reflect-line (TRL) calibration was performed for the above setup. Here, the reference planes for the calibration were set at the input and output of the amplifier. The calibration kit used was the commercial Wiltron TRL calibration kit consisting of a reference through line, an open reflect line and several delay lines. The particular delay line used in the *S*-parameter measurement was chosen to cover the frequency range of 2.0 to 18.0GHz.

After the calibration was performed, the amplifier circuit was re-inserted into the test fixture and the *S*-parameters of the amplifier were measured. The amplifier was again DC biased at $I_B=1.5\text{mA}$ and $V_{CE}=3.0\text{V}$ bias condition. For comparison purposes, the physical layout of the amplifier circuit and the HBT model developed earlier were applied to the OSA90/HopeTM simulation package to simulate the amplifier *S*-parameters. The simulated and measured amplifier *S*-parameters are compared below in Figures 5.5a, b, c, d and e.

Figure 5.5a Simulated and measured $|S_{11}|$ of the amplifier

Figure 5.5b Simulated and measured $|S_{21}|$ of the amplifier

Figure 5.5c Simulated and measured $|S_{21}|$ of the amplifier in narrow band

Figure 5.5d Simulated and measured $|S_{12}|$ of the amplifier

Figure 5.5e Simulated and measured $|S_{22}|$ of the amplifier

From Figures 5.5a, b, c, d and e, the simulated and measured amplifier S -parameters exhibited similar trends, however, some major discrepancies existed. The similarities in the simulated and measured S -parameter showed that the amplifier was working normally. However, it was found from all four S -parameters that the operating frequency of the amplifier was shifted to 13.5GHz instead of the 14.0GHz design frequency. Furthermore, from the individual S -parameter such as the magnitude of S_{11} in Figure 5.5a, the measured input match was much worse (approximately -7.0dB) compared to the simulated value (-18.5dB). Also, from Figure 5.5c, the actual amplifier peak gain S_{21} was about 7.5dB compared to 10.4dB from the simulation; 2.9dB lower gain than expected. Similar discrepancy was found between the measured and simulated reverse transmission S_{12} . Finally, the measured amplifier S_{22} in Figure 5.5e showed a

spiky characteristic near the operating frequency compared to the smooth characteristic from the simulation.

The disagreements between the simulated and measured S -parameters may be due to many reasons. One known reason was that the HBT model itself over-estimated the gain by about 0.8~1.5dB as mentioned in Chapter 3. Also, the degradation in DC collector current (discussed in section 5.2) may cause some degradation in amplifier gain S_{21} and output power. Other reasons may be due to inaccurate estimation of bond-wire inductances, component drifts, and excess substrate parasitics.

The under-estimated bond wire inductances at the input and output of the transistor may be the primary cause for the shift of the operating frequency. These bond wire inductances were originally estimated to be 0.15nH in the design process. After the amplifier was built, the bond wire lengths were measured and found to be 0.32mm and 0.34mm at the input and output accordingly. The equivalent inductances were then calculated and found to be approximately 0.19nH for both the input and the output. It was found from simulation that these increases in the inductance lowered the operating frequency significantly. In fact, the uncertainty of bond wire lengths (hence inductances) during the design process is always a problem in MIC circuits.

Another minor reason for the shift in operating frequency may be due to the under-estimated bond wire inductances connected to the input and output DC block capacitors. Referring to the physical structure of the amplifier in Figure 4.17, the input and output DC blocking capacitors are connected to the transmission lines by two parallel bond wires which were not taken into account during the design process. Again, these bond wire lengths were measured and the bond wire inductances were found to be about

0.24nH for both input and output. This resulted in a further downward shift in operating frequency, yet it is very minor compared to the bond wires connecting directly to the transistor.

The second gain peak near 5GHz and the spiky characteristic in S_{22} may be caused by the change in value of the DC blocking capacitors due to component tolerance. It was found that increasing DC blocking capacitances in the simulation (both input and output) resulted in higher gain peak near 5GHz. In addition, the spiky characteristic in S_{22} was also noted. Here, the capacitance was increased to 0.3pF in the simulation. Finally, this increase in capacitance also resulted in a minor downward shift in operating frequency as well.

The lower value in the measured S_{21} may be partially due to the under-estimation of substrate parasitics. Although the transmission lines were made of gold, because of the surface roughness and other processing reasons, they may have higher resistivity. Similarly, the substrate loss tangent $\tan\delta$ may be larger than the published value. By increasing the resistivity of gold and the loss tangent of the substrate by 5 times in the simulation, the resulting S_{21} was found to be in closer agreement with the measurement. Other factor that caused the lower value in S_{21} may be due to the component losses as they were not accounted for in the simulation.

With the above proposed modifications, the amplifier S -parameters were re-simulated and again compared to the measurement. The comparisons are shown below in Figure 5.6a, b,c and d.

Figure 5.6a Corrected and measured $|S_{11}|$ of the amplifier

Figure 5.6b Corrected and measured $|S_{21}|$ of the amplifier

Figure 5.6c Corrected and measured $|S_{12}|$ of the amplifier

Figure 5.6d Corrected and measured $|S_{22}|$ of the amplifier

It can be seen from the above figures that the agreement between the simulated amplifier S -parameters with proposed corrections and the measured amplifier S -parameters was significantly improved. The major improvement was considered to be the fit in S_{21} , especially around the second gain peak near 5GHz. Also, the corrected and measured S_{12} are in closer agreement with each other. Furthermore, in Figure 5.6d, the corrected S_{22} started to track the measurements better. As the result, the overall trends of the corrected S -parameters are in better agreement with the measurement including the downward shift in operating frequency. However, no improvement was made for the input match S_{11} .

In summary, the major disagreements between the simulated and measured amplifier S -parameters were caused by the under-estimated bond wires inductances, component drifts and substrate parasitics. Taking into account the fact that the model over-estimated the gain by 0.8~1.5dB, the agreement between the measurement and the corrected simulation is considered to be quite acceptable.

5.4 Output Power and Gain Characteristics

The measurement set-up for the HBT amplifier output power versus input power characteristic measurement is shown in Figure 5.7. Here, the HP8350A sweep oscillator was used as the input RF source and was connected to the input of the Wiltron universal test fixture. Within the test fixture, the amplifier circuit (D.U.T.) was mounted as shown. As before, the amplifier DC biasing was provided by the HP 4142B DC biasing network which was controlled by the HP computer. At the test fixture output, a

band-pass filter (12 to 18GHz) which accepts only the signal at the fundamental frequency was connected to the HP437B power meter to measure the output signal level.

Figure 5.7 The experimental setup for output power characteristics measurement

Initially, the HP437B power meter was calibrated before the measurement was performed. Then, with the frequency of the sweep oscillator set at 13.5GHz instead of 14.0GHz (i.e. the operating frequency), the input power level was varied until the amplifier was driven into saturation. For each input power level, the output power level was measured. The cable, adapter, test jig and filter losses were determined separately using a network analyzer. After de-embedding the various component losses, the output power versus the input power level at the fundamental frequency (13.5GHz) is shown in Figure 5.8. The output power versus input power characteristic was also simulated using OSA90/HopeTM. Note that the input frequency was at 14.0GHz for the above simulation. Also shown in Figure 5.8 is the "corrected" output power characteristic simulation based on the previously proposed modifications. Here, for the "corrected" simulation, the input frequency was at 13.5GHz.

Figure 5.8 Output power versus input power characteristics

From the above figure, the measured output power was approximately 3dB lower compared to the simulation. This is not unexpected and in fact, is consistent with the S -parameters measured in Section 5.3 where the measured S_{21} peak was nearly 3dB lower compared to the simulation. The “corrected” output power characteristic is in closer agreement with the measurement yet it is still approximately 1dB higher than the measured output power. This can be explained by the fact that HBT model over-estimates the gain or power by 0.8~1.5dB as mentioned in Chapter 3. Taking the model over-estimation into account, the “corrected” and measured output power characteristic agree reasonably well with one another. When the input power level was small, the output power followed the input in a linear fashion. As the amplifier was driven harder, the output power started to saturate and the measured 1dB compression point P_{1dB} of the

amplifier was found to be 16.4dBm for approximately 10.0dBm input power.

The power gain characteristic of the amplifier can be obtained directly from the above output power versus input power characteristic since the power gain G is given by

$$G_{(dB)} = P_{out(dB)} - P_{in(dB)} \quad (5.1)$$

where P_{out} and P_{in} are output power and input power respectively. By using equation (5.1), the power gain of the HBT amplifier was calculated and plotted versus input power level as shown in Figure 5.9. Within the amplifier's linear region, the power gain stayed approximately constant with the input power level. As the amplifier was driven harder into its saturation region, the power gain decreases with increasing input power level.

Figure 5.9 Power gain versus input power level

In addition to the output power and gain characteristics, the simulated time domain output voltage waveforms at different input power levels is shown in Figure 5.10 below. Here, at small input power levels (i.e. when the amplifier is operating in its linear region), the output voltage waveform is sinusoidal with no harmonic distortion. However, as the input power level increases, the amplifier starts to saturate and distorted output voltage waveforms were observed.

Figure 5.10 Simulated time domain output voltage waveforms at different input power levels

Although the small signal S -parameters of the amplifier showed no signs of instability over a wide range of frequency, a stable operation was not guaranteed under large-signal excitation. In order to verify the large signal stability of the HBT amplifier, the HP437B power meter in the measurement set-up in Figure 5.7 was replaced with the HP8569A spectrum analyzer and, with the amplifier driven into saturation at the 1dB

compression point, the amplifier output power spectrum over the full frequency range (1.7GHz to 22GHz) was photographed and is shown in Figure 5.11.

Figure 5.11 The output power spectrum content of the HBT amplifier

From Figure 5.11, it can be seen that the HBT amplifier was also stable under the large-signal operation since no out-of-band oscillations were detected. Note that the two sub-harmonics shown were not low frequency oscillations generated by the amplifier but were due to the input signal generator. Typically, in a commercial signal generator, in order to generate a high frequency signal, a lower frequency signal is generated and this signal is multiplied up to the desired frequency in several steps. Furthermore, in order to prevent any interference with the frequency of interest, the levels of the sub-harmonics are made as low as possible. In the picture above, the sub-harmonics levels were in fact as low as the maximum noise floor of the spectrum analyzer and no interference with the HBT amplifier was found. As a final note, the stepped noise floor was due to the different dynamic ranges of the multiple frequency band receivers of the spectrum analyzer.

5.5 Third-Order Intermodulation Products

The measurement set-up for the third-order intermodulation products measurement is shown in Figure 5.12. Here, two signal sources centred near 13.5GHz and separated by about 7MHz were combined via the power divider/combiner (5 to 18GHz) and applied to the HBT amplifier. The output of the amplifier was then connected to the HP8569A spectrum analyzer where the intermodulation products were measured. This measurement set-up is similar to the technique suggested in [39].

Because the frequencies of the intermodulation products were close to the two input carriers, their levels could not be measured directly through the power meter since there was no narrow band-pass filter available to filter out the carriers. The most convenient and practical method to measure these products is to use a spectrum analyzer where the power levels are read directly from the screen display. Consequently, the accuracy of such a measurement is reduced due to the reading error and the fact that the spectrum analyzer is not calibrated for accurate power measurement. Thus, for this type of measurement, a minimum of ± 1 dB error is typical.

Figure 5.12 Experimental setup for intermodulation product measurement

Furthermore, for the intermodulation product measurement, the two signal sources were adjusted to have the same power levels applied to the amplifier. This was to ensure the intermodulated products at both sides of the carriers would have equal amplitudes. A typical intermodulation distortion view from the spectrum analyzer is shown in figure 5.13. Here, with low input carriers powers, the intermodulation product was typically very low, about 36dB below the carriers or -36dBc.

Figure 5.13 A typical intermodulation product measurement result

With the input signal power levels varied, the intermodulated product levels at each input power level were measured and the result is shown in Figure 5.14. Due to the limited output power of the sweep generators and various component losses, only several intermodulated products at low input power level were measured. In addition, due to the convergence difficulties in the CAD tool OSA90/HopeTM, the simulated third-order intermodulation characteristic was not available for comparison. Also shown in Figure 5.14 are the extrapolations of the fundamental and third-order

intermodulation power characteristics. The intersection of these extrapolations is the well known third-order intercept point P_{3dB} . It was determined graphically to be about +24.3dBm. Furthermore, from the extrapolation, the intermodulation distortion level at the 1dB compression point P_{1dB} was found to be about -16dBc. Again, this corresponds to an input power level of 10.0dBm.

Figure 5.14 Intermodulation product versus input power level

5.6 Power Added Efficiency

The power added efficiency PAE for an amplifier was defined in Chapter 2 (equation 2.11) and is repeated here for convenience:

$$PAE \equiv \frac{P_{out} - P_{in}}{P_{dc}} \times 100\% = (G - 1) \cdot \frac{P_m}{P_{dc}} \times 100\% \quad (5.2)$$

where P_{out} and P_{in} are output and input power in linear scale, G is the RF power gain and

P_{dc} is the transistor DC power dissipation and is given here again by:

$$P_{dc} = I_B \cdot V_{BE} + I_C \cdot V_{CE} \quad (5.3)$$

The measurement set-up for power added efficiency measurement was the same as the output power versus input power characteristic measurement in Figure 5.7, but with the DC bias currents and voltages (for DC power dissipation calculation) also measured. Then, using equations (5.2) and (5.3), the power added efficiency for each input power level was calculated and the results plotted in Figure 5.15. The simulated and the corrected power added efficiency are also shown in Figure 5.15 for comparison purposes.

Figure 5.15 Power added efficiency versus input power level

The large disagreement between the simulated and measured power added efficiency is again not altogether unexpected. This is because power added efficiency is heavily depended on the output power or the power gain of the amplifier as demonstrated

by equation (5.2). For a moderate gain amplifier, a 3dB decrease in gain or output power results in a nearly half-fold in power added efficiency. This is consistent with Figure 5.15 where the measured power added efficiency was nearly half of the value simulated. However, after the proposed corrections, the corrected power added efficiency agrees reasonably well with the measurement. Here, the power added efficiency of the amplifier at 1dB compression point was measured to be about 30%. This is a typical efficiency for a Class A power amplifier [39].

5.7 Summary

In this chapter, various HBT amplifier characteristic measurements were performed. After the DC biasing of the HBT was made stable, the small signal S -parameters of the amplifier were measured and compared with the simulation. It was found that the simulation over-estimated the gain by about 3dB while the amplifier operating frequency was shifted downward to 13.5 GHz. Also, there were some discrepancies between the simulated and measured input and output matches. However, with the proposed corrections, the corrected and measured S -parameters agreed reasonably well. Other large signal measurements such as output power characteristic and power added efficiency also agreed reasonably well with the corrected simulations. For the HBT amplifier, the measured 1dB compression point P_{1dB} was found to be 16.4dBm at input power level of 10.0dBm and the corresponding power added efficiency was about 30% which is typical for class A operation. Finally, the third order intermodulation measurement showed a third order intercept point P_{3dB} of 24.3dBm.

CHAPTER 6: CONCLUSIONS

6.1 Summary

In this thesis, a large-signal model for the Rockwell $360\mu\text{m}^2$ heterojunction bipolar transistor (HBT) has been developed using a lumped-element topology based on the modified Gummel-Poon model. With this selected topology, there were a total of 36 parameters involved in the model. In this work, only 11 model parameters were extracted using various extraction techniques. A computer optimization technique through fitting of the model simulations against various measured DC and multiple bias S -parameter responses was used to estimate the values of the other 25 parameters. With all model parameters obtained, the modelling process was completed and the large-signal HBT model was then obtained.

The proposed large-signal HBT model is adequate in predicting DC current-voltage characteristics such as I_C versus V_{CE} , V_{BE} versus V_{CE} and the forward Gummel characteristics. In addition, it is also capable of predicting S -parameter responses at multiple bias points mainly in the active region, from 0.4GHz up to 30.0GHz with acceptable accuracy. However, one short-coming of the model is that it cannot predict the reverse Gummel characteristic. Furthermore, from the large-signal measurements, the model simulation shows a 0.8~1.5dB discrepancy compared to the measurements.

Also in this work, a class A medium power HBT amplifier operating at 14.0GHz was designed using the HBT model developed earlier. The amplifier design criteria included reasonable power gain and optimum output power. Because of the gain

requirement, class A operation was chosen for the amplifier. Furthermore, in order to achieve the optimum output power criteria, the power amplifier design made use of the simulated load-pull technique where the optimum source and load impedances subject to optimum output power were found from the simulated power contours.

Conventional microwave integrated circuit (MIC) technology was used for the building of the amplifier. An alumina substrate with a dielectric constant of 9.8 and $2\mu\text{m}$ thick gold lines were used. With the optimum source and load impedances obtained using the load-pull simulation technique, the microstrip input and output matching networks were designed. Also, the quarter-wave section bias network was designed to bias the transistor at DC. The amplifier was designed to achieve unconditional stability at small-signal levels.

Once built, the amplifier's performance was measured and compared to the simulations. From the small-signal S -parameter measurements, the actual amplifier operating frequency was shifted downwards to 13.5GHz, and a nearly 3dB decrease in gain was found. The disagreements between the simulated and measured amplifier S -parameters were traced to the model's inaccuracy and component tolerances. Taking into account such tolerances, the simulations were found to be in much closer agreement with the measurements, including the large-signal cases. For the HBT amplifier, the measured first-order compression point $P_{1\text{dB}}$ was 16.4dBm at 10.0dBm input power level with a corresponding power added efficiency PAE of 30%. The third-order intercept point was found to be 24.3dBm.

In conclusion, a large-signal HBT model for non-linear microwave circuit

applications was developed. Although the model was not able to predict all aspects of the device performances, it was adequate for the application of amplifier design. In fact, the validity of the model was further verified by the building and testing of the class A HBT medium power amplifier. It was believed that with future improvement on the device model, more accurate circuit prediction can be obtained.

6.2 Future Work

In spite of all the effort, more work remains in both the areas of HBT modelling and amplifier design. Some possible improvements are as follows.

There are several improvements that can be made in the HBT modelling procedure. It is believed that with more time and effort, the HBT model would be capable of predicting accurately all the DC characteristics, including the reverse Gummel characteristic. One improvement in the device modelling is the characterization of the non-linear capacitances C_{BE} and C_{BC} . In this work, they were obtained merely from optimization. In order to achieve a more accurate result, these non-linear capacitances could be measured as functions of the controlling voltage(s) (i.e. the C-V characteristics) with appropriate equipment. These measurements cover both saturation and active regions of the transistor and consequently, more accurate capacitances parameters can be obtained.

Another area in need of improvement is the design of the power amplifier. In this work, due to the convergence difficulties with the CAD tool, the appropriate source/load-pull simulation could not be fulfilled. This is due to the complexity of the

model and the software limitations. In fact, the same load-pull simulation was performed on the CAD supplied FET model and the smooth family of power contours resulted with no convergence difficulties. It is believed that with the convergence problem resolved, a better amplifier design procedure can be achieved. Also, operating bandwidth can certainly be improved. Although this was not part of the design goal in this work, in practice, it is often desirable to achieve a wider bandwidth (depending on the application). Yet, above all, the most important improvement that is needed for the amplifier is the stable DC biasing condition. Due to extremely high gain at low frequency, the HBT amplifier is prone to out-of-band oscillation. External bias tees and the ferrite beads had to be added to the bias line to obtain meaningful results. More work is required to eliminate this low frequency oscillation.

APPENDIX I

Derivation of DC Component for Class AB Waveform

Equation (2.30) reads

$$\begin{aligned}
 I_{CQ} &= \frac{\omega}{2\pi} \cdot \int_{-t_o}^{t_o} x \cdot I_{C,MAX} + (1-x) \cdot I_{C,MAX} \cdot \cos(\omega t) dt \quad \text{where } t_o = \frac{\cos^{-1}\left(-\frac{x}{1-x}\right)}{\omega} \\
 &= \frac{\omega}{2\pi} \cdot x \cdot I_{C,MAX} \cdot \int_{-t_o}^{t_o} dt + \frac{\omega}{2\pi} \cdot (1-x) \cdot I_{C,MAX} \cdot \int_{-t_o}^{t_o} \cos(\omega t) dt \\
 &= \frac{\omega}{2\pi} \cdot x \cdot I_{C,MAX} \cdot [t]_{-t_o}^{t_o} + \frac{\omega}{2\pi} \cdot (1-x) \cdot I_{C,MAX} \cdot \left[\frac{\sin(\omega t)}{\omega} \right]_{-t_o}^{t_o} \\
 &= \frac{\omega}{2\pi} \cdot x \cdot I_{C,MAX} \cdot 2t_o + \frac{\omega}{2\pi} \cdot (1-x) \cdot I_{C,MAX} \cdot \left(\frac{\sin(\omega t_o)}{\omega} - \frac{\sin(-\omega t_o)}{\omega} \right) \\
 \therefore I_{CQ} &= \frac{x \cdot I_{C,MAX}}{\pi} \cdot \cos^{-1}\left(-\frac{x}{1-x}\right) + \frac{(1-x) \cdot I_{C,MAX}}{\pi} \cdot \sin\left(\cos^{-1}\left(-\frac{x}{1-x}\right)\right) \quad (A.1)
 \end{aligned}$$

Now, from the unit circle and the right angle triangle below

$$\begin{aligned}
 \sin\left(\cos^{-1}\left(-\frac{x}{1-x}\right)\right) &= \sqrt{1 - \left(-\frac{x}{1-x}\right)^2} \\
 &= \frac{\sqrt{1-2x}}{1-x} \\
 &\quad (A.2)
 \end{aligned}$$

Substituting equation (A.2) into (A.1) and

$$I_{cQ} = \frac{x \cdot I_{C,MAX}}{\pi} \cdot \cos^{-1}\left(-\frac{x}{1-x}\right) + \frac{(1-x) \cdot I_{C,MAX}}{\pi} \cdot \frac{\sqrt{1-2x}}{1-x}$$

Finally, $I_{cQ} = \frac{I_{C,MAX}}{\pi} \cdot \left[\sqrt{1-2x} + x \cdot \cos^{-1}\left(-\frac{x}{1-x}\right) \right]$ as given by equation (2.31).

APPENDIX II

Derivation of Fundamental Component for Class AB Waveform

Equation (2.33) reads

$$\begin{aligned}
 a_1 &= \frac{\omega}{\pi} \int_{-t_o}^{t_o} (x \cdot I_{C,MAX} + (1-x) \cdot I_{C,MAX} \cdot \cos(\omega t)) \cdot \cos(\omega t) dt \quad \text{where } t_o = \frac{\cos^{-1}\left(-\frac{x}{1-x}\right)}{\omega} \\
 &= \frac{\omega}{\pi} \cdot x \cdot I_{C,MAX} \cdot \int_{-t_o}^{t_o} \cos(\omega t) dt + \frac{\omega}{\pi} \cdot (1-x) \cdot I_{C,MAX} \cdot \int_{-t_o}^{t_o} \cos^2(\omega t) dt \quad (A.3)
 \end{aligned}$$

Using the identity $\cos^2(\theta) = \frac{1 + \cos(2\theta)}{2}$, equation (A.3) becomes

$$\begin{aligned}
 a_1 &= \frac{\omega}{\pi} \cdot x \cdot I_{C,MAX} \cdot \int_{-t_o}^{t_o} \cos(\omega t) dt + \frac{\omega}{\pi} \cdot (1-x) \cdot I_{C,MAX} \cdot \int_{-t_o}^{t_o} \left(\frac{1 + \cos(2\omega t)}{2} \right) dt \\
 &= \frac{\omega}{\pi} \cdot x \cdot I_{C,MAX} \cdot \int_{-t_o}^{t_o} \cos(\omega t) dt + \frac{\omega}{2\pi} \cdot (1-x) \cdot I_{C,MAX} \cdot \int_{-t_o}^{t_o} dt \\
 &\quad + \frac{\omega}{2\pi} \cdot (1-x) \cdot I_{C,MAX} \cdot \int_{-t_o}^{t_o} \cos(2\omega t) dt \\
 &= \frac{\omega}{\pi} \cdot x \cdot I_{C,MAX} \cdot \left[\frac{\sin(\omega t)}{\omega} \right]_{-t_o}^{t_o} + \frac{\omega}{2\pi} \cdot (1-x) \cdot I_{C,MAX} \cdot [t]_{-t_o}^{t_o} \\
 &\quad + \frac{\omega}{2\pi} \cdot (1-x) \cdot I_{C,MAX} \cdot \left[\frac{\sin(2\omega t)}{2\omega} \right]_{-t_o}^{t_o}
 \end{aligned}$$

Then,

$$a_1 = \frac{\omega}{\pi} \cdot x \cdot I_{C,MAX} \cdot \left(\frac{2 \sin(\omega t_o)}{\omega} \right) + \frac{\omega}{2\pi} \cdot (1-x) \cdot I_{C,MAX} \cdot 2t_o \\ + \frac{\omega}{2\pi} \cdot (1-x) \cdot I_{C,MAX} \cdot \left(\frac{2 \sin(2\omega t_o)}{2\omega} \right) \quad (A.4)$$

Substituting the expression for t_o into equation (A.4) gives:

$$a_1 = \frac{2 \cdot x \cdot I_{C,MAX}}{\pi} \cdot \sin \left(\cos^{-1} \left(-\frac{x}{1-x} \right) \right) + \frac{(1-x) \cdot I_{C,MAX}}{\pi} \cdot \cos^{-1} \left(-\frac{x}{1-x} \right) \\ + \frac{(1-x) \cdot I_{C,MAX}}{2\pi} \cdot \sin \left(2 \cos^{-1} \left(-\frac{x}{1-x} \right) \right) \quad (A.5)$$

Using the identity $\sin(2\theta) = 2 \sin(\theta) \cos(\theta)$, equation (A.5) becomes:

$$a_1 = \frac{2 \cdot x \cdot I_{C,MAX}}{\pi} \cdot \sin \left(\cos^{-1} \left(-\frac{x}{1-x} \right) \right) + \frac{(1-x) \cdot I_{C,MAX}}{\pi} \cdot \cos^{-1} \left(-\frac{x}{1-x} \right) \\ + \frac{(1-x) \cdot I_{C,MAX}}{2\pi} \cdot 2 \sin \left(\cos^{-1} \left(-\frac{x}{1-x} \right) \right) \cdot \cos \left(\cos^{-1} \left(-\frac{x}{1-x} \right) \right) \quad (A.6)$$

Substituting equation (A.2) into (A.6) yields:

$$a_1 = \frac{2 \cdot x \cdot I_{C,MAX}}{\pi} \cdot \left(\frac{\sqrt{1-2x}}{1-x} \right) + \frac{(1-x) \cdot I_{C,MAX}}{\pi} \cdot \cos^{-1} \left(-\frac{x}{1-x} \right) \\ + \frac{(1-x) \cdot I_{C,MAX}}{2\pi} \cdot \frac{2\sqrt{1-2x}}{1-x} \cdot \left(-\frac{x}{1-x} \right) \quad (A.7)$$

Finally, by rearranging equation (A.7)

$$a_1 = \frac{I_{C,MAX}}{\pi} \cdot \left[\frac{x \cdot \sqrt{1-2x}}{1-x} + (1-x) \cdot \cos^{-1} \left(-\frac{x}{1-x} \right) \right] \text{ as given by equation (2.34).}$$

APPENDIX III

OSA90/Hope™ Circuit File Listing of the Load-Pull Simulation

```
!HBT MODEL USING:
! NON-LINEAR CONTROLLED CURRENT SOURCE
! BUILT IN DIODE ELEMENT
! THERMAL SUB-CIRCUIT
!
! HBT FROM ROCKWELL INTERNATIONAL, MEASURED ON JULY 29/93
```

```
! FILE:lsmodelloadpullmatchjuly11.ckt
```

```
CONTROL
```

```
DISPLAY_N_DIGITS = 5;
```

```
END
```

```
EXPRESSION
```

```
#DEFINE N_VCE_POINTS 161
#DEFINE N_IB_POINTS 9
#DEFINE N_FREQ_POINTS 100
#DEFINE N_VBCG_POINTS 101
#DEFINE N_VBEG_POINTS 126
```

```
!***Constants***
```

```
To = 300.0;      ! Initial temperature
k = 1.3806E-23;  ! Boltzmann's Constant
qe = 1.602E-19;  ! Electron Charge
qbyk = qe/k;
```

```
!***Index Variables***
```

```
I = 1;
J = 1;
L = 1;
P = 1;
Q = 1;
```

```
!*****Model Parameter Values*****
```

```
!***Saturation Currents***
```

```
ISATO = 2.02241;
ISDEO = 1.20172;
ISDCO = 3.25729;
ISATot = ISATO*1E-22;
ISDEot = ISDEO*1e-18;
ISDCot = ISDCO*1E-14;
```

!*Ideality Factors*****

NF = 1.14726;
 NR = 1.12039;
 NE = 1.57408;
 NC = 1.76639;

!*Device Resistances*****

RB = 1.69524;
 RE = 1.07957;
 RC = 1.1884;

!*Current Gains*****

BFO = 46.3854;
 BR = 0.168046;

!*Saturation Current Temperature Exponent*****

XTI = 6.49606;

!*Forward BETA (BFO) Temperature Exponent*****

XTB = 1.22518;

!*Thermal Resistance*****

Rth = 188.195;

!*Energy Gap*****

Ego = 1.4162;
 Eg = Ego*qc;

Einfo = 0.0544986;
 Einf = Einfo*qc;

!*Large resistor in series with DC sources for better convergence*****

RSWITCH=1E6;

!*Base Current And Collector Voltage Variables*****

IBASE : 1.5MA;
 VCOL : 3.0V;

!*Extrinsic Parasitic Elements*****

CBASE':0.13391pF;
 CCOL' :0.0973844PF;
 CBC' :0.13334PF;
 LB' :0.0622708NH;
 LC' :0.0540358NH;
 LE' :0.0023197NH;

!*Parameters For Cbc,depletion*****

CJCO = 0.197032PF;
 VJC = 1.52397;
 MJC = 0.5;

!*Parameters For Cbe,depletion*****

CJEO = 0.400214PF;
 VJE = 2.04518;
 MJE = 0.3333333;

!***Parameters For Cbe,diffusion***

TFO=8.21516PS;

XTF=0.589692;

VTF=2.87041;

!TFO=9.07495PS;

!XTF=0.600689;

!VTF=3.18464;

!***Input Power Level At Fundamental Frequency***

PIN=-10.0DBM;

!***Output Load***

RPORT = 1.0;

XPORT = 0.0;

END

MODEL

!*****

!* Voltage And Current Labels *

!*****

VLABEL	4	6	NAME = VBEDELAY
			TAU = 2.37704ps; ! Delayed Intrinsic Base-Emitter Voltage
VLABEL	4	6	NAME = VBE ; ! Intrinsic Base-Emitter Voltage
VLABEL	4	5	NAME = VBC ; ! Intrinsic Base-Collector Voltage
VLABEL	@IB1	0	NAME = VBE1; ! Extrinsic Base-Emitter Voltage
VLABEL	@IC1	0	NAME = VCE1; ! Extrinsic Base-Collector Voltage
ILABEL	@IB1	10	NAME = IB; ! Base Current Label
ILABEL	@IC1	20	NAME = IC; ! Collector Current Label

!*****

!* Definition Of Thermal Subcircuit *

!*****

VSOURCE		80	0	NAME=TEMP VDC=To;
RES	80	81		R=RTH;
CAP	80	81		C=12NF;
NLCCS	0	81		I=(IC*VCE1+IB*VBE1);
VLABEL		81	0	NAME=TEST;

! guard against floating point errors by ensuring that T is within the correct range

T= IF ((TEST > 600) + (TEST < To)) (600) ELSE (MAX(To,TEST));

!*****

!* Temperature Dependent Saturation Currents And Forward Current Gain *

!*****

ISAT = ISATot*((T/To)^XTI)*Exp(MAX(1E-99,(Eg/k)*(-1/T+1/To)));

BFT = BFo*((T/To)^(-1*XTB))*Exp(-1*MAX(1E-99,(Einf/k)*(-1/T+1/To)));

ISDBF = ISAT/BFT;

ISDBR = ISAT/BR;

ISDE = ISDEot*((ISAT/ISATot)^(1/NE))*(BFo/BFT);

ISDC = ISDCot*((ISAT/ISATot)^(1/NC))*(BFo/BFT);

```

*****
!* Input Biasing Tee And DC Source *
*****
CAP  41    40    C=1000PF;
RES  40    90    R=1.0E-2;
IND  90     1    L=1000NH;
ISOURCE  1     0    NAME=BASE  IDC=IBASE;
RES   1     0    R=RSWITCH;

*****
!* HBT Model *
*****
!* Extrinsic Elements *
*****
IND  40    @IB1  L=LB';
CAP  @IB1  30    C=CBASE';
IND  30     0    L=LE';
CAP  @IB1  @IC1  C=CBC';
CAP  @IC1  30    C=CCOL';
IND  50    @IC1  L=LC';

*****
!* HBT Model *
*****
!* Intrinsic Device Elements *
*****
RES  10     4    R=RB;
RES   6    30    R=RE;
RES   5    20    R=RC;

DIODE 4     5    IS=ISDC N=NC TEMP=T;      ! DC
DIODE 4     6    IS=ISDE N=NE TEMP=T;      ! DE
DIODE 4     5    IS=ISDBR N=NR TEMP=T;      ! DBR
DIODE 4     6    IS=ISDBF N=NF TEMP=T;      ! DBF

*****
!* Dummy Variables *
*****
xa = qbyk*VBEDELAY/(NF*T);
xab = qbyk*VBE/(NF*T);
xb = qbyk*VBC/(NR*T);
xaa = EXP(MIN(60,xa));
xbb = EXP(MIN(60,xb));
xabb= EXP(MIN(60,xab));
*****

QBC  = IF (VBC < 1.1) ( (-CJCO*VJC/(1-MJC))*((1-VBC/VJC)^(1-MJC)-1) )
      ELSE (CJCO);
NLCQ 4     5    Q=QBC;

TAUF  = IF (VBC<1.1) (TFO*(1-XTF*EXP(VBC/(1.44*VTF)))) ELSE (TFO);
QBEDIFF = ( TAUF*ISAT*(xabb-1));
NLCQ 4     6    Q=QBEDIFF;

```



```

QBEDEP = IF (VBE < 1.7) ( (-CJEO*VJE/(1-MJE))*((1-VBE/VJE)^(1-MJE)-1) )
      ELSE (CJEO);
NLCQ  4      6      Q=QBEDEP;

NLCCS 5      6      I=(ISAT*(xaa-xbb));

!*****
!* Input Biasing Tee And DC Source      *
!*****
CAP   51      50      C=1000PF;
RES   50      70      R=1.0E-2;
IND   70      2       L=1000NH;
VSOURCE 2      0      NAME=COLLECTOR   VDC=VCOL;
RES   2      0      R=RSWITCH;

!*****
!* Input And Output Ports      *
!*****
S11M=0.897062;
S11P=169.959DEG;
S21M=1.123210;
S21P=45.978DEG;
S12M=0.051058;
S12P=-1.729DEG;
S22M=0.483651;
S22P=-161.423DEG;

GAMR=(RPORT^2+XPORT^2-1)/((RPORT+1)^2+(XPORT^2));
GAMI=(2*XPORT)/((RPORT+1)^2+(XPORT^2));

RI2MP( GAMR ,GAMI ,GAMM ,GAMP );

TOPM=S12M*S21M*GAMM;
TOPP=S12P+S21P+GAMP;

MP2RI( (S22M*GAMM) , (S22P+GAMP) , TEMPR , TEMPI );

BOTR=1.0-TEMPR;
BOTI=0.0-TEMPI;

RI2MP( BOTR , BOTI , BOTM , BOTP );

TOTM=-TOPM/BOTM;
TOTP=-TOPP-BOTP;

MP2RI( TOTM , TOTP , TOTR , TOTI );
MP2RI( S11M , S11P , S11R , S11I );

GINR=S11R+TOTR;
GINI=-1.0*(S11I+TOTI);

RI2MP( GINR , GINI , GINM , GINP );

RIN = (1-GINR^2-GINI^2)/((1-GINR)^2+GINI^2);
XIN = (2*GINI)/((1-GINR)^2+GINI^2);

```

```

PORT 41      0      NAME=INPUT R=(RIN*50.0) X=(XIN*50.0) P[1]=PIN;
PORT 51      0      NAME=OUTPUT R=(RPORT*50.0) X=(XPORT*50.0);

```

```
CIRCUIT HARM = 6;
```

```
!***Output Power In dBm***
```

```
Poutput[0:N_SPECTRA]=10*LOG10(PWoutput)+30;
```

```
!***Real Part Of Gamma***
```

```
GARE=( RPORT^2+XPORT^2 - 1)/( (RPORT+1)^2+(XPORT^2) );
```

```
!***Imaginary Part Of Gamma***
```

```
GAIM=(2*XPORT)/( (RPORT+1)^2 + (XPORT^2) );
```

```
GAMMARE11=IF ( POUTPUT[1] >= 10.90 & POUTPUT[1] <= 11.10 ) (GARE) ELSE (NAN);
```

```
GAMMAIM11=IF ( POUTPUT[1] >= 10.90 & POUTPUT[1] <= 11.10 ) (GAIM) ELSE (NAN);
```

```
GAMMARE12=IF ( POUTPUT[1] >= 11.90 & POUTPUT[1] <= 12.10 ) (GARE) ELSE (NAN);
```

```
GAMMAIM12=IF ( POUTPUT[1] >= 11.90 & POUTPUT[1] <= 12.10 ) (GAIM) ELSE (NAN);
```

```
GAMMARE13=IF ( POUTPUT[1] >= 12.90 & POUTPUT[1] <= 13.10 ) (GARE) ELSE (NAN);
```

```
GAMMAIM13=IF ( POUTPUT[1] >= 12.90 & POUTPUT[1] <= 13.10 ) (GAIM) ELSE (NAN);
```

```
GAMMARE14=IF ( POUTPUT[1] >= 13.90 & POUTPUT[1] <= 14.10 ) (GARE) ELSE (NAN);
```

```
GAMMAIM14=IF ( POUTPUT[1] >= 13.90 & POUTPUT[1] <= 14.10 ) (GAIM) ELSE (NAN);
```

```
GAMMARE15=IF ( POUTPUT[1] >= 14.90 & POUTPUT[1] <= 15.10 ) (GARE) ELSE (NAN);
```

```
GAMMAIM15=IF ( POUTPUT[1] >= 14.90 & POUTPUT[1] <= 15.10 ) (GAIM) ELSE (NAN);
```

```
GAMMARE16=IF ( POUTPUT[1] >= 15.90 & POUTPUT[1] <= 16.10 ) (GARE) ELSE (NAN);
```

```
GAMMAIM16=IF ( POUTPUT[1] >= 15.90 & POUTPUT[1] <= 16.10 ) (GAIM) ELSE (NAN);
```

```
GAMMARE17=IF ( POUTPUT[1] >= 16.90 & POUTPUT[1] <= 17.10 ) (GARE) ELSE (NAN);
```

```
GAMMAIM17=IF ( POUTPUT[1] >= 16.90 & POUTPUT[1] <= 17.10 ) (GAIM) ELSE (NAN);
```

```
END
```

```
SWEEP
```

```
HB: FREQ : 14.0GHZ
```

```
PIN : 7.0DBM
```

```
RPORT : 0.03 0.05 0.07
```

```
0.10 0.14 0.18 0.20 0.24 0.28
```

```
0.32 0.36 0.40 0.44 0.48 0.52
```

```
0.56 0.60 0.64 0.68
```

```
0.70 0.80 0.90 0.95
```

```
1.00 1.10 1.20 1.30 1.40 1.50
```

```
1.60 1.70 1.80 1.90 2.00 2.20
```

```
XPORT : FROM -1.0 TO 2.0 STEP=0.05
```

```
POUTPUT[1],MIC,GARE,GAIM,
```

```
GAMMARE17,GAMMAIM17,GAMMARE11,GAMMAIM11,GAMMARE12,GAMMAIM12,
```

GAMMARE13,GAMMAIM13,GAMMARE14,GAMMAIM14,GAMMARE15,GAMMAIM15,
GAMMARE16,GAMMAIM16,MTEST[0],RPORT,XPORT

{SMITH RI=(GAMMARE11,GAMMAIM11).TRIANGLE.GREEN &
(GAMMARE12,GAMMAIM12).X.YELLOW &
(GAMMARE13,GAMMAIM13).SQUARE.GREEN &
(GAMMARE14,GAMMAIM14).DIAMOND.YELLOW &
(GAMMARE15,GAMMAIM15).CROSS.GREEN &
(GAMMARE16,GAMMAIM16).DOT.YELLOW &
(GAMMARE17,GAMMAIM17).CIRCLE.YELLOW
X=XPORT RPORT=ALL }

END

SPEC

END

APPENDIX IV

OSA90/Hope™ Circuit File Listing of the HBT Amplifier

```
! HBT POWER AMPLIFIER
! HBT MODEL USING:
! NON-LINEAR CONTROLLED CURRENT SOURCE
! BUILT IN DIODE ELEMENT
! THERMAL SUB-CIRCUIT
!
! HBT FROM ROCKWELL INTERNATIONAL, RWCE9F6 MEASURED ON JULY 29/93
! LBOND=0.15NH CBLOCK=0.18pF
! FILE = ~/osa90/hbtamp/AmpLP15CP18mar7.ckt
! MON MAR 7 1994
```

CONTROL

```
DISPLAY_N_DIGITS = 5;
!Newton_EPS_Relative = 0.1;
```

END

EXPRESSION

```
#DEFINE N_VCE_POINTS 161
#DEFINE N_IB_POINTS 9
#DEFINE N_FREQ_POINTS 100
#DEFINE N_VBCG_POINTS 101
#DEFINE N_VBEG_POINTS 126
```

!***Constants***

```
To = 300.0;      ! Initial temperature
k = 1.3806E-23;  ! Boltzmann's Constant
qe = 1.602E-19;  ! Electron Charge
qbyk = qe/k;
```

!***Index Variables***

```
I = 1;
J = 1;
L = 1;
P = 1;
Q = 1;
```

!*****Model Parameter Values*****

!***Saturation Currents***

```
ISATO = 2.02241;
ISDEO = 1.20172;
ISDCO = 3.25729;
ISATot = ISATO*1E-22;
ISDEot = ISDEO*1e-18;
```

ISDCot = ISDCO*1E-14;

!***Ideality Factors***

NF = 1.14726;

NR = 1.12039;

NE = 1.57408;

NC = 1.76639;

!***Device Resistances***

RB = 1.69524;

RE = 1.07957;

RC = 1.1884;

!***Current Gains***

BFo = 46.3854;

BR = 0.168046;

!***Saturation Current Temperature Exponent***

XTI = 6.49606;

!***Forward BETA (BFo) Temperature Exponent***

XTB = 1.22518;

!***Thermal Resistance***

Rth = 188.195;

!***Energy Gap***

Ego = 1.4162;

Eg = Ego*qc;

Einfo = 0.0544986;

Einf = Einfo*qc;

!***Large resistor in series with DC sources for better convergence***

RSWITCH=1E6;

!***Base Current And Collector Voltage Variables***

IBASE : 1.5MA;

VCOL : 3.0V;

!***Extrinsic Parasitic Elements***

CBASE':0.13391pF;

CCOL' :0.0973844PF;

CBC' :0.13334PF;

LB' :0.0622708NH;

LC' :0.0540358NH;

LE' :0.0023197NH;

!***Parameters For Cbc,depletion***

CJCO = 0.197032PF;

VJC = 1.52397;

MJC = 0.5;

!***Parameters For Cbe,depletion***

CJEO = 0.400214PF;

VJE = 2.04518;
MJE = 0.3333333;

!***Parameters For Cbe,diffusion***
TFO=8.21516PS;
XTF=0.589692;
VTF=2.87041;

!***Input Power Level At Fundamental Frequency***
PIN=-10.0DBM;

!***Output Load***

LBOND = 0.15NH;
CBLOCKIN= 0.18PF;
CBLOCKOUT= 0.18PF;
RBIASIN= 10;
RBIASOUT= 10;

! inmatchdoubleLP15CP3.ckt
!INSTUB1=1226.24UM;
!INLINE2=2640.98UM;
!INSTUB2=1424.76UM;
INSTUB1=1236UM; !1235.5UM;
INLINE2=2654UM; !2654.43UM;
INSTUB2=1466UM; !1466.45UM;

OUTLINE=805UM; !805.478UM; !1215.007UM;
OUTSTUB=1261UM; !1260.75UM; !912.897UM;

THININ=2091UM;
THINLINE=1500UM;
WIDEWIDTH=300UM;
WIDELENGTH=1946UM;

END

MODEL

MSUB EPSR=9.96 H=254.0UM T=1.0UM TAND=0.001 ROC=2.44E-8 RHS=0.0;

!*****
!* Voltage And Current Labels *
!*****

VLABEL	4	6	NAME = VBEDELAY
			TAU = 2.37704ps; ! Delayed Intrinsic Base-Emitter Voltage
VLABEL	4	6	NAME = VBE ; ! Intrinsic Base-Emitter Voltage
VLABEL	4	5	NAME = VBC ; ! Intrinsic Base-Collector Voltage
VLABEL	@IB1	0	NAME = VBE1; ! Extrinsic Base-Emitter Voltage
VLABEL	@IC1	0	NAME = VCE1; ! Extrinsic Base-Collector Voltage
ILABEL	@IB1	10	NAME = IB; ! Base Current Label
ILABEL	@IC1	20	NAME = IC; ! Collector Current Label

```

*****
!* Definition Of Thermal Subcircuit *
*****
VSOURCE      80      0      NAME=TEMP VDC=To;
RES          80      81      R=RTH;
CAP          80      81      C=12NF;
NLCCS        0      81      I=(IC*VCEI+IB*VBEI);
VLABEL       81      0      NAME=TEST;
! guard against floating point errors by ensuring that T is within the correct range
T= IF ( (TEST > 600) + (TEST< To) ) (600) ELSE ( MAX(To,TEST) );
!T=319.505;

*****
!* Temperature Dependent Saturation Currents And Forward Current Gain *
*****
ISAT = ISATot*((T/To)^XTI)*Exp(MAX(1E-99,(Eg/k)*(-1/T+1/To)));
BFT  = BFo*((T/To)^(-1*XTB))*Exp(-1*MAX(1E-99,(Einf/k)*(-1/T+1/To)));
ISDBF = ISAT/BFT;
ISDBR = ISAT/BR;
ISDE  = ISDEot*((ISAT/ISATot)^(1/NE))*(BFo/BFT);
ISDC  = ISDCot*((ISAT/ISATot)^(1/NC))*(BFo/BFT);

*****
!* Input Biasing Tee And DC Source *
*****
IND   40    303    L=LBOND;
MCROSS 303    304    305    306    W1=245.0UM W2=245.0UM W3=245.0UM;
MOPEN304    W=245.0UM L=INSTUB1;
MOPEN306    W=245.0UM L=INSTUB1;
MSL   305    307    W=245.0UM L=INLINE2;
MCROSS 307    308    309    310    W1=245.0UM W2=245.0UM W3=245.0UM;
MOPEN308    W=245.0UM L=INSTUB2;
MOPEN310    W=245.0UM L=INSTUB2;
MSL   309    311    W=245.0UM L=1000UM;
MTEE  311    315    322    W1=245.0UM W2=245.0UM W3=75.0UM;
MSL   315    316    W=245.0UM L=1125UM;
CAP   316    317    C=Cblockin;
MSL   317    318    W=245.0UM L=2000UM;

MSL   322    323    W=75.0UM L=THININ;
MCROSS 323    324    325    326    W1=75.0UM W2=75.0UM W3=WIDEWIDTH;

MOPEN325    W=WIDEWIDTH L=WIDELENGTH;

RES   324    327    R=Rbiasin;
CAP   327    399    C=100PF;
IND   399    0      L=0.07NH;

MSL   326    328    W=75.0UM L=THINLINE;
MSTEP 328    329    W1=75.0UM W2=750.0UM;
MOPEN329    W=750.0UM L=750.0UM;

ISOURCE 329  0      NAME=F:ASE IDC=IBASE;
RES      329  0      R=RSWITCH;

```

```

*****
!* HBT Model *
*****
!* Extrinsic Elements *
*****
IND 40 @IB1 L=LB';
CAP @IB1 30 C=CBASE';
IND 30 0 L=LE';
CAP @IB1 @IC1 C=CBC';
CAP @IC1 30 C=CCOL';
IND 50 @IC1 L=LC';

*****
!* HBT Model *
*****
!* Intrinsic Device Elements *
*****
RES 10 4 R=RB;
RES 6 30 R=RE;
RES 5 20 R=RC;

DIODE 4 5 IS=ISDC N=NC TEMP=T; ! DC
DIODE 4 6 IS=ISDE N=NE TEMP=T; ! DE
DIODE 4 5 IS=ISDBR N=NR TEMP=T; ! DBR
DIODE 4 6 IS=ISDBF N=NF TEMP=T; ! DBF

*****
!* Dummy Variables *
*****
xa = qbyk*VBEDELAY/(NF*T);
xab = qbyk*VBE/(NF*T);
xb = qbyk*VBC/(NR*T);
xaa = EXP(MIN(60,xa));
xbb = EXP(MIN(60,xb));
xa1 = EXP(MIN(60,xab));
*****

QBC = IF (VBC < 1.1) ( (-CJCO*VJC/(1-MJC))*((1-VBC/VJC)^(1-MJC)-1) )
      ELSE (CJCO);
NLCQ 4 5 Q=QBC;

TAUF = IF (VBC<1.1) (TFO*(1-XTF*EXP(VBC/(1.44*VTF)))) ELSE (TFO);
QBEDIFF = ( TAUF*ISAT*(xab-1));
NLCQ 4 6 Q=QBEDIFF;

QBEDEP = IF (VBE < 1.7) ( (-CJEO*VJE/(1-MJE))*((1-VBE/VJE)^(1-MJE)-1) )
      ELSE (CJEO);
NLCQ 4 6 Q=QBEDEP;

NLCCS 5 6 I=(ISAT*(xaa-xbb));

*****
!* Output Biasing Tee And DC Source *
*****

```



```

IND      50      202      L=LBOND;
MSL      202     203      W=245.0UM L=OUTLINE;
MCROSS   203     204      205      206      W1=245.0UM W2=245.0UM W3=245.0UM;
MOPEN    204     W=245.0UM L=OUTSTUB;
MOPEN    206     W=245.0UM L=OUTSTUB;
MSL      205     207      W=245.0UM L=1000UM;
MTEE     207     208      222      W1=245.0UM W2=245.0UM W3=75.0UM;
MSL      208     209      W=245.0UM L=1125UM;
CAP      209     210      C=Cblockout;
MSL      210     211      W=245.0UM L=2000UM;

```

```

MSL      222     223      W=75.0UM L=THININ;
MCROSS   223     224      225      226      W1=75.0UM W2=75.0UM W3=WIDELWIDTH;

```

```

MOPEN    225      W=WIDELWIDTH L=WIDELLENGTH;

```

```

RES      224     227      R=Rbiasout;
CAP      227     299      C=100PF;
IND      299     0        L=0.07NH;

```

```

MSL      226     228      W=75.0UM L=THINLINE;
MSTEP    228     229      W1=75.0UM W2=750.0UM;
MOPEN    229      W=750.0UM L=750.0UM;

```

```

VSOURCE   229     0        NAME=COLLECTOR VDC=VCOL;
RES      229     0        R=RSWITCH;

```

```

!*****
!* Input And Output Ports *
!*****

```

```

PORT      318     0        NAME=INPUT P[1]=PIN;
PORT      211     0        NAME=OUTPUT;

```

CIRCUIT HARM = 6;

!***Output Power In dBm***

Poutput[0:N_SPECTRA]=10*LOG10(MAX(1E-20,PWoutput))+30;

DB_MS11=20*LOG10(MS11);

DB_MS21=20*LOG10(MS21);

DB_MS12=20*LOG10(MS12);

DB_MS22=20*LOG10(MS22);

PDC = MIB[0]*MVBE1[0]+MIC[0]*MVCE1[0];

PINLIN = 10^((PIN-30)/10);

PAE = ((PWOUTPUT[1]- PINLIN) /PDC)*100;

END

SWEEP

AC: FREQ: FROM 0.4GHz TO 40GHz STEP = 0.2GHz

DB_MS11,PS11,DB_MS21,PS21,DB_MS12,PS12,DB_MS22,PS22,SK

{XSWEPT X=FREQ Y=DB_MS11.GREEN & DB_MS21.YELLOW & DB_MS12.YELLOW &

```

DB_MS22.WHITE
XMIN=0 XMAX=28 NXTICKS=4
YMIN=-40 YMAX=20 NYTICKS=6}

```

```

{XSWEEP X=FREQ Y=SK.GREEN
XMIN=0 XMAX=28 NXTICKS=4
YMIN=0 YMAX=10 NYTICKS=10};

```

```

HB: FREQ : 14.0GHZ
PIN : !FROM -5.0 TO 7.0 STEP = 1.0
      -5.0 -4.0 -3.0 -2.0 -1.0 0.0 1.0 2.0 3.0 4.0
      5.0 5.5 6.0 6.5 7.0 7.5 8.0 8.5 9.0

```

```

POUTPUT[1],PWOUTPUT[1],PINLIN,T,MIB[0],MVBE1[0],MIC[0],MVCE1[0],PDC,PAE
{XSWEEP X=PIN Y=POUTPUT[1].GREEN & POUTPUT[1].TRIANGLE.GREEN
XMIN=-5 XMAX=10 NXTICKS=15
YMIN=0 YMAX=20 NYTICKS=20 }

```

```

{XSWEEP X=PIN Y=PAE.GREEN & PAE.TRIANGLE.GREEN
XMIN=-5 XMAX=10 NXTICKS=15
YMIN=0 YMAX=50 NYTICKS=10 };

```

```

! HB: FREQ :14.0GHz
! PIN : 5 6 7 8 9 10
! MVOUTPUT,PVOUTPUT,PWOUTPUT
!
! { Waveform Spectrum=(MVOUTPUT,PVOUTPUT)
! Tmin=0 Tmax=0.5ns NT=256
! PIN=all};

```

END

SPEC

END

REFERENCES

- [1] B. Bayraktaroglu, "GaAs HBT's for Microwave Integrated Circuits", *Proceedings of the IEEE*, Vol. 81, No. 12, December 1993, pp. 1762-1785.
- [2] B. K. Oyama and B. P. Wong, "GaAs HBT's for Analog Circuits", *Proceedings of the IEEE*, Vol. 81, No. 12, December 1993, pp. 1744-1761.
- [3] M. E. Kim et al, "GaAs Heterojunction Bipolar Transistor Device and IC Technology for High-Performance Analog and Microwave Applications", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 37, No. 9, September 1989, pp. 1286-1303.
- [4] H. Kroemer, "Heterostructure Bipolar Transistors and Integrated Circuits", *Proceedings of the IEEE*, Vol. 70, No. 1, January 1982, pp. 13-25.
- [5] P. M. Asbeck et al, "Heterojunction Bipolar Transistors for Microwave and Millimeter-wave Integrated Circuits", *IEEE Transactions on Electron Devices*, Vol. ED-34, No. 12, December 1987, pp. 2571-2579.
- [6] P. M. Asbeck et al, "GaAs-Based Heterojunction Bipolar Transistors for Very High Performance Electronic Circuits", *Proceedings of the IEEE*, Vol. 81, No. 12, December 1993, pp. 1709-1726.
- [7] M. A. Khatibzadeh, B. Bayraktaroglu and T. Kim, "12 W Monolithic X-band HBT Power Amplifier", *IEEE Microwave and Millimeter Wave Monolithic Circuits Symp. Tech. Dig.*, 1992, pp. 47-50.
- [8] M. A. Khatibzadeh and B. Bayraktaroglu, "Low Phase Noise Heterojunction Bipolar Transistor Oscillator", *Electron. Lett.*, Vol. 26, 1990, pp. 1246-1247.
- [9] Herbert L. Kraus, Solid State Radio Engineering, Wiley, 1980.
- [10] John L. B. Walker, High-Power GaAs FET Amplifiers, Artech House, 1993.
- [11] Adel S. Sedra and Kenneth C. Smith, Microelectronic Circuits, 2nd Edition, HRW, 1987.
- [12] B. D. Geller and P.E. Geotlle, "Quasi-Monolithic 4GHz Power Amplifier with 65% Power Added Efficiency", *Proc. IEEE MTT-S Int. Microwave Symp.*, New York, NY, May 24-25, 1988, pp. 835-838.

- [13] Stephen A. Maas, Nonlinear Microwave Circuits, Artech House, 1988.
- [14] Guillermo Gonzalez, Microwave Transistor Amplifiers Analysis and Design, Prentice-Hall, 1984.
- [15] M. S. Lundstrom, "An Ebers-Moll Model for the Heterostructure Bipolar Transistor", *Solid-State Electronics*, Vol. 29, No. 11, November 1986, pp. 1173-1179.
- [16] B. K. Ryum and Ibrahim M. Adbel-Motaleb, "A Gummel-Poon Model for Abrupt and Graded Heterojunction Bipolar Transistors (HBTs)", *Solid-State Electronics*, Vol. 33, No. 7, July 1990, pp. 869-880.
- [17] Ian E. Getreu, Modeling the Bipolar Transistor, Elsevier Scientific Publishing Company, 1978.
- [18] Herbert Kroemer, "Theory of a Wide-Gap Emitter for Transistors", *Proceedings of the IRE*, Vol. 45, No. 11, November 1957, pp. 1535-1537.
- [19] Dale K. Jaus and Donald L. Feucht, "The realization of a GaAs-Ge Wide Band Gap Emitter Transistor", *IEEE Transactions on Electron Devices*, Vol. ED-16, No. 1, January 1969, pp. 102-107.
- [20] Fazal Ali and Aditya Gupta, HEMPs and HBTs: Devices, Fabrication, and Circuits, Artech House, 1991.
- [21] Richard N. Nottenburg et al, "InGaAs/InP Double-Heterostructure Bipolar Transistors with Near-Ideal β Versus I_C Characteristic", *IEEE Electron Device Letters*, Vol. EDL-7, No. 11, November 1986, pp. 643-645.
- [22] P. Chris Grossman and John Choma, "Large Signal Modeling of HBT's Including Self-Heating and Transit Time Effects", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 40, No. 3, March 1992, pp. 449-464.
- [23] Madjid E. Hafizi et al, "The DC Characteristics of GaAs/AlGaAs Heterojunction Bipolar Transistors with Application to Device Modeling", *IEEE Transactions on Electron Devices*, Vol. 37, No. 10, October 1990, pp. 2121-2129.
- [24] P. Antognetti and G. Massobrio, Semiconductor Device Modeling with SPICE, McGraw-Hill, 1988.
- [25] H. Wang et al, "Temperature Dependence of DC Currents in HBT", *IEEE MTT-S Digest*, 1992, pp. 731-734.

- [26] Yusuke Tajima et al, "GaAs FET Large-Signal Model and its Application to Circuit Designs", *IEEE Transactions on Electron Devices*, Vol. ED-28, No. 2, February 1981, pp. 171-175.
- [27] Seonghearn Lee and Anand Gopinath, "New Circuit Model for RF Probe Pads and Interconnections for the Extraction of HBT Equivalent Circuits", *IEEE Electron Device Letters*, Vol. 12, No. 10, October 1991, pp. 521-523.
- [28] HSPICE User's Manual-Elements and Models, Vol. 2, Version H92, Meta-Software, 1992.
- [29] Douglas A. Teeter et al, "Large-Signal Numerical and Analytical HBT Models", *IEEE Transactions on Electron Devices*, Vol. 40, No. 5, May 1993, pp. 837-845.
- [30] Fatima S. Corraera and Saied Tadayon, "A modified Gummel-Poon model applied to HBTs", *23rd European Microwave Conference*, September 1993, pp. 96-98.
- [31] S. A. Maas and D. Tait, "Parameter-Extraction Method for Heterojunction Bipolar Transistor", *IEEE Microwave and Guided Wave Letters*, Vol. 2, No. 12, December 1992, pp. 502-504.
- [32] David R. Pehlke and Dimitris Pavlidis, "Direct Calculation of the HBT Equivalent Circuit From Measured S-Parameters", *IEEE MTT-S Digest*, 1992, pp. 735-738.
- [33] Damian Costa et al, "Direct Extraction of the AlGaAs/GaAs Heterojunction Bipolar Transistor Small-Signal Equivalent Circuit", *IEEE Transactions on Electron Devices*, Vol. 38, No. 9, September 1991, pp. 2018-2024.
- [34] Dale E. Dawson et al, "CW Measurement of HBT Thermal Resistance", *IEEE Transactions on Electron Devices*, Vol. 39, No. 10, October 1992, pp. 2235-2239.
- [35] Rached Hajji, Fadhel M. Ghannouchi and Renato G. Bosisio, "Large-Signal Microwave Transistor Modeling Using Multiharmonic Load-Pull Measurements", *Microwave and Optical Technology Letters*, Vol. 5, No. 11, October 1992, pp. 580-585.
- [36] Steve C. Cripps, "GaAs FET Power Amplifier Design", Matcom, Inc. Technical Note 3.2.
- [37] LineCalc User's Manual, Version 3.5, EEsof, November, 1991.
- [38] Thomas S. Laverghetta, Handbook of Microwave Testing, Artech House, 1981.
- [39] Nan-Lei Wang et al, "7.5-14 GHz CE HBT MMIC Linear Power Amplifier", *IEEE Microwave and Guided Wave Letters*, Vol. 3, No. 3, March 1993, pp. 64-66.

END

0|5-06-9|6

FIN