CURRENT MODE LOGIC LATCH AND PRESCALER DESIGN OPTIMIZATION IN 0.18μm CMOS TECHNOLOGY

by

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Abstract

This thesis begins with a discussion of clocked storage elements in general, and then narrows its focus to current-mode logic (CML) after simulation results for high speed applications have been considered. Emphasis is given to the more important circuit characteristics, especially those involving timing and metastable behavior.

The results of simulations involving high-speed devices using a number of established technologies decisively militated for the CMOS current-mode logic model, at least in the case of 0.18μm CMOS design rules.

A consideration of past efforts to improve the characteristics of CML devices results in a new 'clock feedback' CML (CFCML) latch being proposed.

An explicit circuit example to demonstrate the advantages of CFCML was needed. What was selected for this purpose was the high-frequency static frequency divider, two versions of which were designed and fabricated (TSMC 0.18μm CMOS technology). It was found that a 10GHz CFCML divider requires only 350μA current from a 1.2V supply (0.42 mW) and has an input sensitivity of 10mV at 9.4GHz. The performances of two different implementations of a 3/4 dual-modulus prescaler, one involving an external modulus control block, and the other an embedded one, are compared. A model for an asynchronous divider architecture which offers savings of 20% for each of power consumption and chip area is reported.

Important Information

The information used in this thesis comes in part from the research program of Dr. Tad A. Kwasniewski and his associates in the VLSI in Communications group. The research results appearing in this thesis represent an integral part of the ongoing research program. All research results in this thesis including tables, graphs and figures but excluding the narrative portions of the thesis are effectively incorporated into the research program and can be used by Dr. Kwasniewski and his associates for education and research purposes, including publication in open literature with the appropriate credits. Matters of intellectual property may be pursued cooperatively with Carleton University and Dr. Kwasniewski where and as appropriate.

Acknowledgments

Most importantly, Dr. Tad A. Kwasniewski must be thanked for the guidance, support and patience he showed in his capacity as my Research Supervisor. It was he who provided the inspiration for this work, and he whose guidance saw it through to completion. I wish him all the best in life. I would also like to express my gratitude to Dr. Shoujun Wang from Altera Ottawa, for expressing his interest in research results on D-latch optimization.

I would also like to express my appreciation for the efforts of several faculty members, staff and fellow students in the Department of Electronics, ones who collectively provided the intellectual ethos which encouraged me to take full advantage of the excellent learning environment which surrounded me. Special thanks are due to Syed Irfan Ahmed for his selfless guidance at every step on the way, whose insight and knowledge made many problems easier, and also to Muhammad Arsalan for providing motivation to proceed. I am also thankful to Robert Lamont for a final review of this document.

Financial support and research facilities from Carleton University and Cadabra Technologies is gratefully appreciated. The technical support and chip fabrication facilities provided by the Canadian Microelectronics Corporation proved to be essential to the completion of my work, and the contributions of this organization are sincerely acknowledged.

The help and love of my family members has been invaluable.

Especially I would like to dedicate this thesis to my brother Ahmed Shemail, whose encouragement and support made it impossible to stop working.

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List of Symbols and Abbreviations

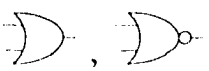

Power supply

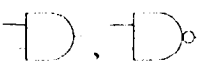

Ground


NMOS

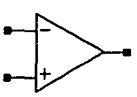

PMOS


Inverter


OR/NOR gate


AND/NAND gate


Buffer or amplifier


Op-amp

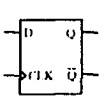

Resistor

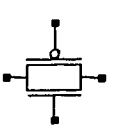

Capacitor


Inductor


Diode


Port/pin (input or output)


D-type latch or D-type flip-flop


Transmission gate

Nomenclature

CLK ..... Clock signal

C_x ..... Capacitance at any node X

D ..... Data signal of any CSE

f ..... Frequency of a periodic signal

I_S ..... Source/Biasing current

l ..... CMOS transistor's gate length

N, M ..... Any general division ratio

Q ..... Output of CSE

R, S ..... Set/Reset inputs of SR latch

R_L ..... Load Resistance

T, T_{CLK} ..... Time period of a signal/Clock

τ, T_p ..... Propagation delay (50% input - 50% output)

T_{CQ} ..... Clock to output delay in a CSE

T_{DC} ..... Data to clock time

T_{DQ} ..... Data to output delay

Tf, Tr ..... Fall/Rise time (10% - 90% transition time)

T_H, T_S ..... Hold/Setup time

Ti ..... Intrinsic time delay

T_w ..... Pulse width

V_{DD} ..... Supply voltage

V_{TH} ..... Threshold voltage of a CMOS transistor

W ..... CMOS transistor's gate width

ΔV ..... Voltage swing

Abbreviations

APS. . . . . Analytical Probe Station

BiCMOS. . . . . Bipolar Complementary-Metal-Oxide-Semiconductor

BJT . . . . . Bipolar Junction Transistor

C^2MOS. . . . . Clocked CMOS

CFCML. . . . . Clock Feedback CML

CI . . . . . Clocked Inverter

CL. . . . . Capturing Latch

CML . . . . . Current Mode Logic

CMOS. . . . . Complementary-Metal-Oxide-Semiconductor

CMOSP18. . . . . Fabrication technology (0.18μm)

CMRR. . . . . Common Mode Rejection Ratio

CSE. . . . . Clocked Storage Element

CVSL . . . . . Cascode Voltage Switch Logic

DC. . . . . Direct Current

DSTC . . . . . Dynamic Single Clocked Transistor

DUT . . . . . Device Under Test

ESD. . . . . Electrostatic Discharge

ETDFF . . . . . Edge Triggered D-Flip-Flop

FB . . . . . Feedback

FCP24. . . . . Flat Ceramic Pack (A 24-pin package)

FF . . . . . Flip-flop

FSM . . . . . Finite State Machine

HLFF . . . . . Hybrid Latch Flip-Flop

HSPICE™ ..... A circuit simulator

IC ..... Integrated circuit

ICFCUMU1, 2 ..... Fabricated chips

IF ..... Intermediate Frequency

LO ..... Local Oscillator

LVS ..... Layout vs. Schematic, a tool

MCML ..... MOS Current Mode Logic

MOSFET ..... Metal-Oxide-Semiconductor Field Effect Transistor

MS(L) ..... Master-Slave (Latch)

N.A. ..... Not Available/Not Applicable

PCB ..... Printed Circuit Board

PDN ..... Pull Down Network

PFD ..... Phase-Frequency Detector

PG ..... Pulse Generator

PLL ..... Phase-Locked Loop

PN ..... Phase noise

PTL ..... Pass Transistor Logic

PSRR ..... Power Supply Rejection Ratio

PVT ..... Process, Voltage and Temperature

RAM ..... Random Access Memory

RF ..... Radio Frequency

RLC ..... Resistance, Inductance, Capacitance

SA(FF) ..... Sense Amplifier (Flip-Flop)

SC ..... Switched-Capacitor

SDFF ..... Semi-Dynamic Flip-Flop

SSR . . . . . Signal to Slope Ratio

SSTC . . . . . Static Single Clocked Transistor

SpectreS™ . . . . . A circuit simulator

TG . . . . . Transmission Gate

TSPC . . . . . True Single Phase Clock

TYPICAL . . . . . A process corner

VCO . . . . . Voltage-controlled oscillator

VLSI . . . . . Very Large Scale Integration

VSR . . . . . Voltage Swing Ratio

CHAPTER 1

Introduction

1.1 Chapter Overview

This chapter describes what motivated the research described in the thesis, and also the organization of the work.

1.2 Introduction

The issue of clock signal generation and distribution in synchronous digital systems becomes ever more important as the performance (speed) demands on systems continue to rise dramatically, doubling approximately every three years [1]. However, timing uncertainties have not remained proportional to frequency increases, and an increasingly large portion of the clock cycle has been spent on the clocking overheads. It has been predicted that traditional clocking techniques will cease to be useful in the 5 to 10 GHz range [2]. New ideas are needed, for clock design and for the design of the systems they drive.

The difficulties are the results of the overheads imposed by clocked storage elements' (CSE) delay, and of the clock period uncertainties. The abilities to set clock frequencies correctly, and to identify and optimize clock-signal critical paths are becoming increasingly important. The performance overheads associated with accomplishing these

goals directly, adversely and critically affect the performance of contemporary systems. It turns out that the most important elements in circuit performance optimization involve clocked storage elements, namely latches and flip-flops.

1.3 Thesis Motivation

Therefore, this thesis will describe our contribution towards the development of a CSE structure which is optimized for multi-gigahertz operation, and is also compatible with modern high-speed and low-power VLSI system designs. The totality of available clocked storage elements is far too large to permit an in-depth discussion of everyone of them in this thesis, so our exploration will be limited to CMOS structures only.

1.4 Thesis Organization

This document comprises the present Introduction plus an additional five chapters:

Chapter 2 – a comprehensive literature review of the CMOS clocked storage elements used in modern microprocessors. Their fundamental timing parameters are described in detail. Delay and power-consumption figures for the various logic styles are summarized.

Chapter 3 – explains the design constraints imposed on a digital system clocking by the CSEs. It also provides a detailed analysis of CMOS current mode logic (CML) style.

Chapter 4 – considers the design and analysis of current mode logic latches and their application in frequency prescalers. A detailed analysis of CML latch metastability as a function of clock rise and fall times is presented. Other performance limiting factors are also mentioned. A new clock feedback CML latch is proposed, whose design was

inspired by modified CML latch structures described in the literature. Some new ideas for synchronous and asynchronous digital dividers are also presented.

Chapter 5 – Post-layout simulation results and design procedures for the implementation of the proposed circuit structures are described.

Chapter 6 – outlines the conclusions drawn from this work and proposes some future research possibilities.

The appendices contain information about MOSFET capacitance, component schematics, chip layout, die photographs, pin-out diagrams, test fixtures, and so on.

References cited in this thesis are listed at the end.

CHAPTER 2

Review of Modern CMOS Latches and Flip-Flop Structures

2.1 Chapter Overview

Presented in this chapter is a comprehensive review of modern CMOS clocked storage elements, with emphasis on basic timing parameters. The most important of the device operating principles are reviewed. Operational comparisons are facilitated using 0.18μm technology simulation results.

2.2 Introduction

The one-bit digital storage element plays a fundamental role in digital signal processing circuitry. Because of its pervasiveness in such designs, it is perhaps the principal performance determinant, affecting the key characteristics of speed and power consumption. The two most common forms of this element are the latch and the flip-flop.

Of these, the clocked D-latch ('data' latch) is the simplest in construction, the storage function being accomplished by a pair of cross-coupled inverters.

Of the various flip-flop structures available (J-K, S-R,...), the one used most frequently in synchronous digital circuits is the DFF ('data' flip-flop), by reason of its sim-

plicity and resulting high speed of operation and also the fact that it is very easily implemented using contemporary IC fabrication technologies.

2.3 Clocked Storage Elements

The function of a clocked storage element, be it a flip-flop or a latch, is one of capturing a data bit at a particular time, and then to preserve it as long as necessary.

2.3.1 D-Latch

The D-latch (see Figure 2.1) is such a device: it is a memory element having at least two inputs, namely a clock signal (*CLK*) and a data signal (*D*) and an output (*Q*) (and often its complement). The device is 'transparent' during one of the clock levels – the *transparent phase* – during which the output *Q* follows the input *D*. But when the clock level is complemented – to its *isolation phase* – the logic level present at *D* is frozen at *Q*, which remains in that state until *CLK* returns to its transparent phase. *D*-latches are categorized as being 'positive' or 'negative', depending upon the logic level of the transparent phase.

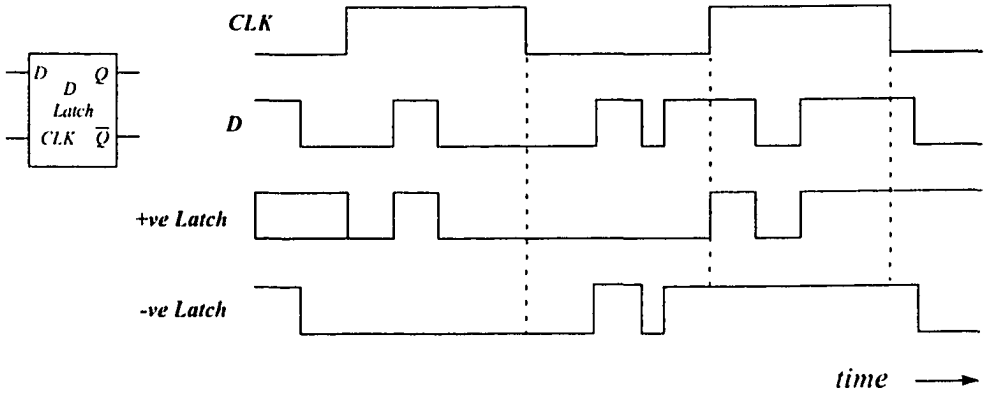


Figure 2.1: Ideal D-Latch Behavior

2.3.2 *The Master-Slave Latch and the D-Flip-Flop*

Transparency in latches can be responsible for instability, glitches and race conditions. These problems can be done away with by using an arrangement of two latches which are clocked successively with two non-overlapping clock phases. The first latch serves as a 'master' which receives data input and passes it on to a 'slave' latch, as in Figure 2.2(a). The non-overlapping nature of the *CLK* phases ensures that there is no transparency between the input and the output; most often the other phase of the clock is achieved by locally inverting the main clock.

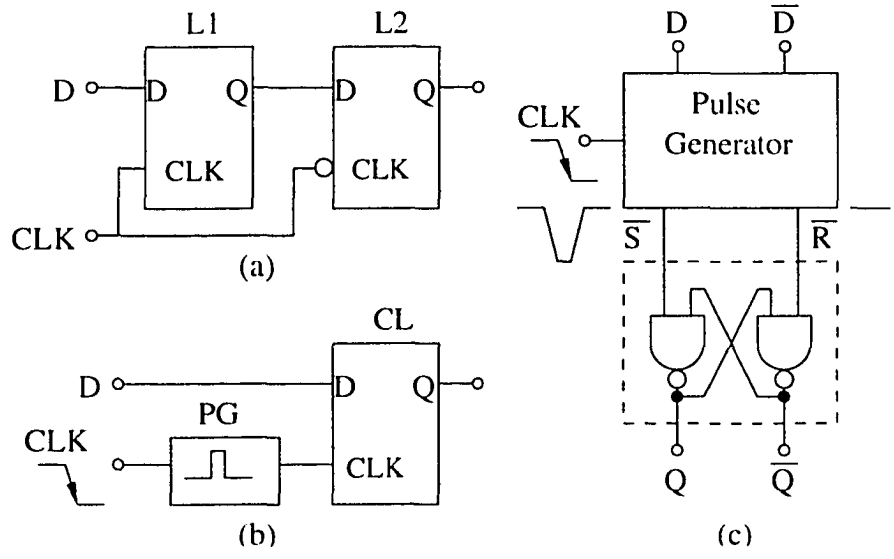


Figure 2.2: CSE Structures (a) MS Latch, (b) Pulsed Clock Latch, (c) Flip-Flop.

"This 'MSL' latch arrangement is not to be confused with the flip-flop, something which many of today's practitioners seem to do" [2]. The two devices have fundamentally differing operational characteristics, in that the latch is level-sensitive, something that makes its transparent mode possible, while the flip-flop is edge sensitive in that the data present at the time of the active clock edge is frozen at the output until the next active edge

(it is non-transparent). Thus, the two are suited to different sets of requirements and will also be characterized by inherently different circuit topologies.

The general structure of a D-Flip-Flop (DFF) is shown in Figure 2.2(b & c). The device consists of two stages: (a) a pulse generator (PG) and (b), a capturing latch (CL).

In case of pulsed clock latch Figure 2.2(b), the PG generates a short pulse on the arrival of the clock edge. During the pulse width time, the CL is transparent and the input data is transferred to the output where it is held until the next clock pulse. In the case of the structure shown in Figure 2.2(c) there is no period of transparency between the input and the output. Before the active clock edge, the data is stored in an intermediate node, and is then transferred to the output during a short pulse generated by the PG, after the active clock edge. The pulse duration can be as long as half a clock period or as short as a single inverter delay.

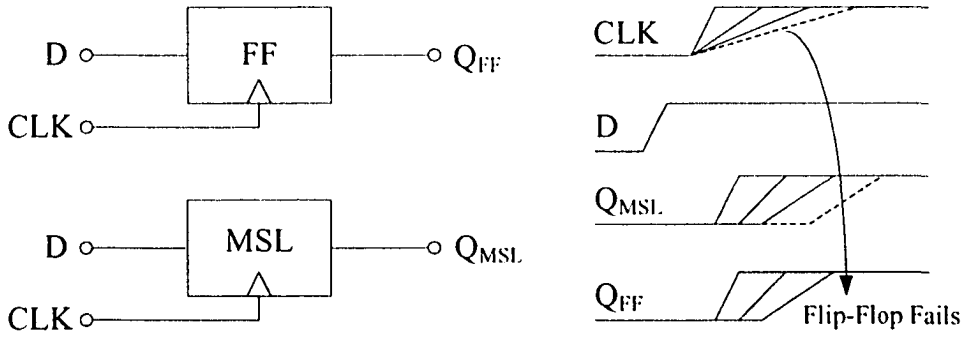


Figure 2.3: Behavior of MSL and FF

In spite of the different topologies for the FF and MSL, it may seem that the two behave identically. Figure 2.3 demonstrates the difference between the two, if the rise/fall time of the active clock edge increases, there will be a time at which the flip-flop will fail

to capture the data before the MSL would fail, because the capturing mechanism of both Master and Slave latches is related to the clock level, not to the rate of change. There are several reasons why the flip-flop may fail [2]:

1. Clock edge degradation (larger transition time) can diminish the level and duration of the internally produced pulse that switches the CL to transparent mode.

2. Any spurious clock signal glitch can cause erroneous triggering of the FF.

3. This sensitivity of the flip-flop to the rate of the triggering edge makes the flip-flop potentially hazardous for the noisy environment.

2.4 CSE Timing Parameters

CSE timing parameters are defined with respect to the active clock edges. A similar set of timing parameters can be defined for both latch and FF/MSL devices, but, because of different operating principles these parameters are defined differently in the two cases – see Figure 2.4 and 2.5.

2.4.1 D-Latch Timing Parameters

Latch parameters are defined relative to leading and trailing clock edges. The clock's isolation-to-transparent phase transition ($I \rightarrow T$) will be referred to as the triggering edge while the $T \rightarrow I$ transition will be called the isolation edge. This terminology is independent of physical voltage levels and can be used equally well in discussions involving either positive or negative latches (although positive logic will be used for illustrations). It will be further assumed that the D signal may change at arbitrary times, but of course setup and hold time requirements must be satisfied if successful data transfers are to take place. The timing parameters are illustrated in Figure 2.4.

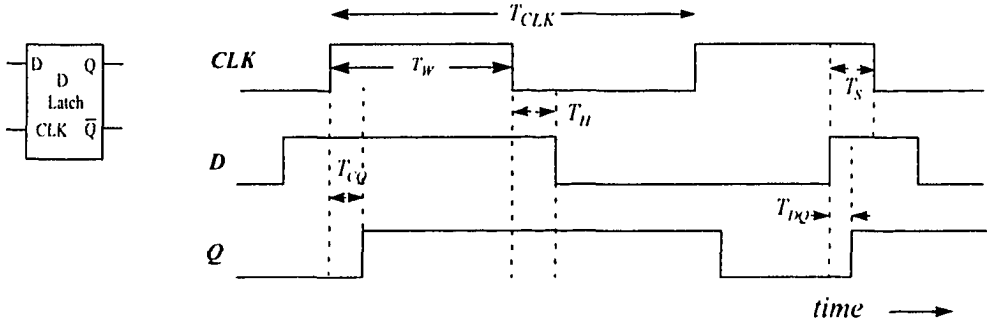


Figure 2.4: D-Latch Timing Parameters

2.4.2 MS Latch/Flip-Flop Timing Parameters

The edge-triggered D-flip-flop (ETDFF) (or master-slave latch – MSL) has the same input and output signals as does a D-latch; however, its edge-sensitive design means that it responds to changes at the *D* input at only the 'active' clock edge. But while the output is not affected by the other, inactive edge, changes do occur in the FF's internal circuitry. Similar timing parameters as those for a *D*-latch may also be defined for the *D*-flip-flop. Positive logic is assumed in Figure 2.5. The other edge of the clock, which was designated as the isolating edge for the latch, is inactive so far as the output *Q* is concerned.

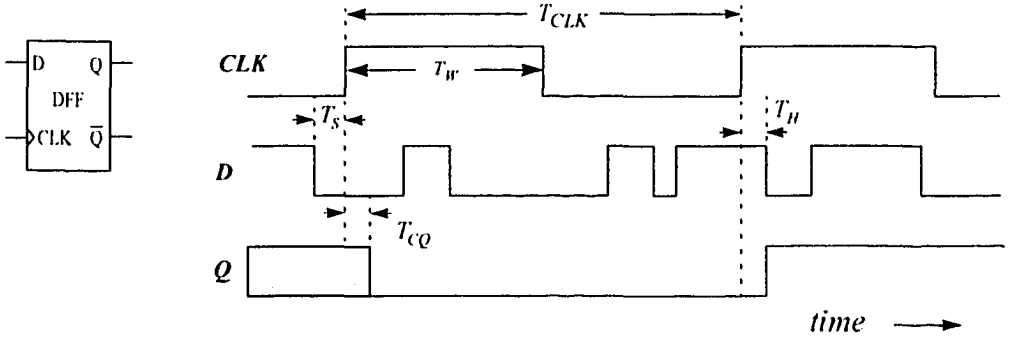


Figure 2.5: D Flip-Flop/MSL Timing Parameters

The **Minimum Clock Pulse-Width,** T_w is that which is necessary for proper latch operation. Any further increase in this pulse-width will be assumed not to affect any other timing parameters such as the setup or hold times. This statement is true also for the *D*-flip-flop/MSL.

The **Clock-to-Q Delay,** T_{CQ}, is the $CLK \rightarrow Q$ propagation delay. Its minimum value $T_{CQ(Stable)}$ is achieved for a *D* signal that has been stable prior to the triggering *CLK* edge.

The **D-to-Q Delay,** T_{DQ}, is the $D \rightarrow Q$ propagation time required for the level at *D* to appear at *Q* once *CLK*'s $1 \rightarrow T$ transition has occurred. In case of a latch this time is minimum during the transparent phase, denoted $T_{DQ(Stable)}$. However, for FF/MSL T_{DQ} always depends on relative position of *D* and *CLK* signals, as the *Q* output only changes after the clock edge.

The **Set-up Time,** T_S, and the **Hold Time,** T_H, can not be defined without considering the metastable behavior of the latches and flip-flops, which is described below.

2.4.3 Metastability in Latches and Flip-Flops

Uncertainties in the CSE delays exist if the *D* input changes in the vicinity of the triggering *CLK* edge. The clock-to-output delay T_{CQ} may be plotted as a function of the data-to-clock time T_{DC} (time between the last change in the *D* input before *CLK's* triggering edge), and regions of stability, metastability and failure may be defined as shown in Figure 2.6. The stable region is the region of the T_{DC} where T_{CQ} is constant and independent of T_{DC}. The next region is the metastable one, at some point in which T_{CQ} delay starts to rise in a monotonic fashion towards infinity, which of course marks the beginning

of the failure region. The metastable region is formally defined as the region of unstable T_{CQ} delay, where the parameter increases rapidly. In the failure zone, $D \rightarrow Q$ transfers will never be successful.

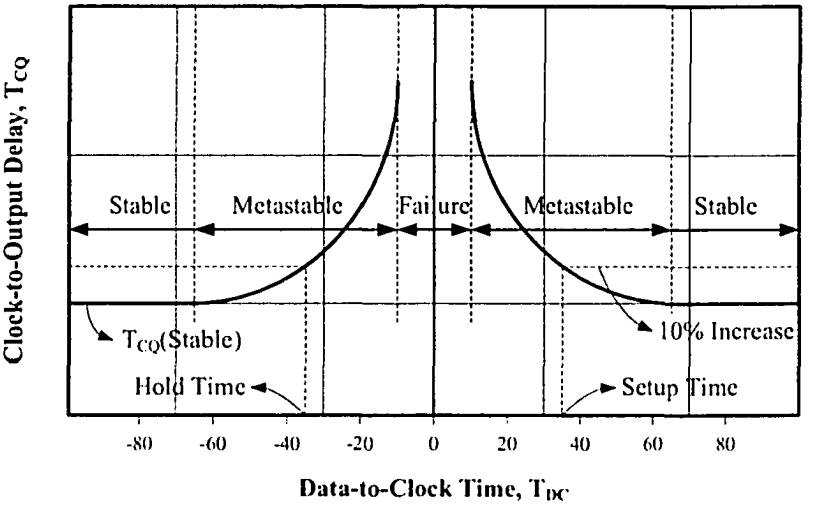


Figure 2.6: Regions of Stability in Flip-flops

An examination of Figure 2.6 suggests that setup and hold violations do not occur abruptly, but it is the probability of failure that increases as $|T_{DC}|$ becomes less and less in the two cases [11]. A precise definition of T_S and T_H values is therefore impossible, and a probabilistic one must be used – the setup and hold times can be defined as the T_{DC} time where the T_{CQ} delay increases by an arbitrary amount (usually 5%-10%), from its stable value [2], as shown in Figure 2.6.

Because of the higher gain of some logic styles, like complementary CMOS latches, the metastable region is very limited and a rapid change in the delay (steeper curve) appears before the failure region. So the time difference between the two boundaries of the metastable region is too small that further time probing is not considered necessary. The classical definitions of setup and hold times in [9], refers to the minimum time

T_{DC} that the input data can change before or after the active clock edge, without affecting the output delay T_{DQ}. In fact this is the beginning of the metastable region, and for some logic styles, like CML, metastable region is much wider like one shown in Figure 2.6. Following are the definitions of setup and hold times used in this thesis.

The **Set-up Time,** T_S, is the minimum time between a D signal change and the active edge of the clock which must be observed if the D level is to be accurately transferred to the Q output, without increasing the delay by more than 10% from its stable value $T_{CQ(Stable)}$. Nonobservance of this condition leads to a *setup time violation.*

The **Hold Time,** T_H, is the minimum time for which the D signal must remain constant or stable after the triggering clock edge, without increasing the delay by more than 10% from its stable value $T_{CQ(Stable)}$. The value of T_H can be zero or even negative for some flip-flops. Failure to observe this condition results in a *hold time violation.*

It is also common in the literature [6], to define the setup and hold times as the T_{DC} time just before the failure, $T_{DC(min)}$, without considering its adverse effects on the delay, which in turn affects the performance of the system.

2.5 CSE Classification

There are a number of CMOS latch/flip-flop structures to choose from in the modern VLSI design environment, the choice being a result of considering the signalling and clocking schemes and any other constraints which may result from the requirements of a particular system. A selection will be made from devices in the following categories.

2.5.1 Static and Dynamic Structures

Static storage devices retain their logic states in the absence of clock signals, so long as the power supply is maintained. This type of approach to temporary storage is probably the one in widest use. And it is a mandatory one when data is to be saved once clock signals have been gated off, as in a piece of apparatus having a 'power-saving' mode.

Dynamic flip-flops represent another class of storage elements, one which has become popular in the design of high speed CMOS digital systems. In this type of device, logic states are represented by the electric charge on capacitive elements, elements which usually are the parasitic gate capacitances of the MOS transistors used in the storage elements. But over a period of time, the charge will leak away for various reasons, and so must be 'topped up' (refreshed) periodically. This means that a two-phase (ones labelled precharge and evaluation) clock can never be stopped.

The choice between these options is not automatic, and must be made with project goals in mind.

2.5.2 Single-ended and Differential Designs

Due to the cross-coupled inverter structure of most storage elements, complementary outputs will be available. But this fact alone is not a sufficient reason to classify a device as being 'differential'. The true differential storage element provides complementary (differential) outputs and also requires complementary data ($D, \overline{D}$) and clock signals. Latches that need only a single-ended data signal are themselves defined as being single-ended devices.

There is now a growing number of both analog and digital electronic applications that make use of differential circuit techniques and a variety of differential latches and flip-flops have been made available to engineers. Unfortunately, differential circuits will be affected by non equal rising and falling delays, ones which cause glitches that affect succeeding stages, and also by short-circuit power consumption, which makes them less desirable for low-power applications at lower frequencies.

2.5.3 Clocking Styles

Latches and flip-flops can be further classified according to the number of clock phases required for their operation. The following paragraphs briefly describe the different types of clocking schemes available to the designer.

Single-Phase Clocks

This is the simplest form of clocking scheme – only one clock signal is used to trigger the flip-flops and latches in the system. Flip-flops are typically operated with complementary clock signals, where the second of the two phases may be generated within the flip-flop itself.

Two-Phase Clocks

In this scheme two non-overlapping clock signals are used. In a properly-operating circuit or system. Clock skew problems may lead to the violation of non-overlapping condition [9] however, but the problems one faces in a two-phase system are always less severe than in a single-phase scheme.

Multi-Phase Clocks

Some high-performance VLSI systems make use of more than two non-overlapping clock signals so that more actions may be accomplished in a given period of time.

2.6 Energy Considerations

The energy consumed in a clocked storage element is approximately

$$E(t) = \int_{t}^{t+T} V_{DD} \cdot i_{V_{DD}}(\tau) \cdot d\tau \tag{2.1}$$

where T is the time-interval during which all relevant transitions occur: the arrival of new data, the clock pulse and the output transition. This energy can be further subdivided:

$$E = E_{switching} + E_{shortcircuit} + E_{leakage} + E_{static} \tag{2.2}$$

2.6.1 Switching Energy (Dynamic)

The switching component of the energy is defined as

$$E_{switching} = \sum_{i=1}^{N} \alpha_{0\to 1}(i) \cdot C_i \cdot \Delta V(i) \cdot V_{DD} \tag{2.3}$$

where N is the number of circuit nodes, C_i the capacitance of node-i, $\Delta V(i)$ its voltage swing, V_{DD} the supply voltage and $\alpha_{0\to 1}(i)$ is the probability of an energy-consuming transition occurring at node-i.

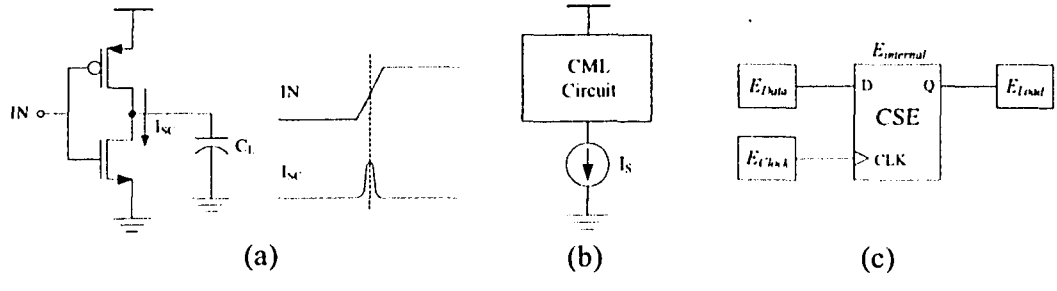


Figure 2.7: (a) Short Circuit Energy, (b) Static Energy, (c) Energy Breakdown

The switching component of the energy consumption is the main contributor (after the static energy consumption, if it exists) to the overall energy consumption when the switching activity is high.

2.6.2 Short Circuit Energy

The short circuit component of energy arises from the short circuit (crowbar) current which flows when both of the pull-up and pull-down paths of a CMOS device conduct simultaneously (see Figure 2.7(a)). The short circuit energy component is typically less than 10% of the total energy [3]. However it can be much greater than this when the slope of the input signal is much larger than the slope of the output signal.

2.6.3 Leakage Energy

The leakage component has two contributors: (a) reverse-bias diode leakage at the drain-bulk junction of the transistor which is given by $I_{leakage} = I_{sat} \cdot (e^{V/Vt} - 1)$, and (b) subthreshold leakage in the channel of an 'off' device, and which is due to carrier diffusion between the source and drain and whose level is exponentially proportional to the gate-to-source override

$$I_{subthreshold} \propto e^{(V_{GS} - V_{TH})/(Vt)} \cdot (1 - e^{(-V_{DS}/Vt)}) \qquad (2.4)$$

where V_{TH} is the threshold voltage, V_t is the thermal voltage and V_{GS} and V_{DS} are gate to source and drain to source voltages respectively. The proportion of energy consumption due to leakage currents is increasing as VLSI device densities scale upwards, and so leakage power will soon become a significant portion of the total power consumption in modern digital designs [3].

2.6.4 Static Energy

This component of energy appears in circuits with DC current biasing (e.g., CML circuits as shown in Figure 2.7(b)). When it exists, this term dominates the energy consumption.

2.6.5 Energy Dissipation Breakdown in CSEs

An understanding of where energy is consumed in a clocked storage element is the key to an energy-efficient design. The three most-important energy consumers in a latch or a flip-flop (shown in Figure 2.7(c)) are: (a) the internal energy consumption of the latch itself, with the exclusion of the energy used for driving its output loads, (b) the local clock buffer driving the latch/FF clock input (local clock energy) and (c), the logic stage driving the data input of the latch (local data energy).

Because of the possible trade-offs among the three, all of the energy loss contributors (Sections 2.8.3, 2.8.4 and 2.8.5) must be taken into account if misleading impressions are to be avoided.

2.7 CSE Circuit Structures

A wide variety of CSE circuits has been reported in the literature [1, 4, 7, 8-23, 26] – the behavior and timing parameters of CSEs has already been presented in Section 2.3 - 2.5. In this section, a selection of static and dynamic CMOS D-flip-flops and latches will be presented in order to show the multitude of device choices available, and then factors to be used in the selection of a device topology that is suitable for one's design. The main points of interest are simplicity of design, power consumption, frequency of operation and bandwidth.

2.7.1 Complementary CMOS Logic Latch

The gate structure of a conventional static CMOS latch is shown in Figure 2.8(a). The form shown here is based on a Set-Reset (SR) latch made of cross-coupled NOR gates (analogous implementations involving JK latches or cross-coupled NAND gates are also realizable). When *CLK* is high the AND gates are enabled and *Q* follows changes in *D* (transparent mode). But when *CLK* goes low, the current state of *D* is frozen at the *Q* output, which is then not affected by further changes in *D*. An inverter between the *S* and *R* latch inputs prevents disallowed states. This latch uses a single clock, but as one can see, the device count is still high. The circuit complexity and number of propagation delays makes this structure unsuitable for high speed applications.

Another realization (symbolic and circuit forms in Figure 2.8(b)) makes use of a 2:1 multiplexer. The *CLK* signal is used as the multiplexor's 'select' signal and its output is fed back to one of the inputs. The data bit to be stored is applied to the other input. The latch will be in its transparent mode when *CLK* is high, and the data will be locked when *CLK* goes low. This latch has a lower device count than the previous structure, but it suffers from instability – locally inverted *CLK* signal may be the cause of a glitch, which in turn may be latched.

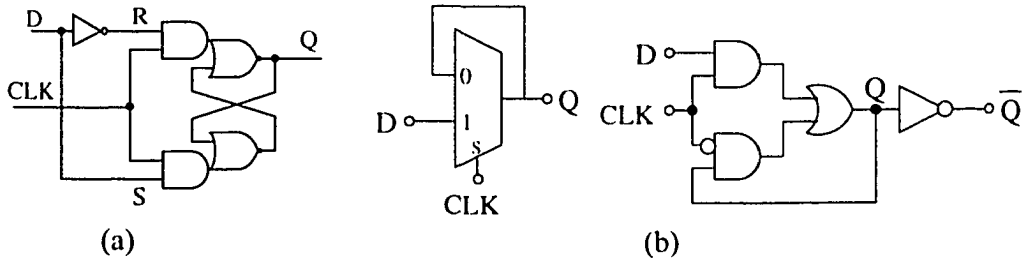


Figure 2.8: Static D-Latches Using: (a) SR Latch (b) Mux

2.7.2 *Dynamic Latches*

A completely different means of realizing a latch involves representation of data as the charge (voltage) of a capacitor [3][4]. An example of such a device is the simple transmission-gate-based one shown in Figure 2.9(a). The capacitor is used to store the input value at high *CLK* phase just before *CLK* goes low and transmission gate turns off. The capacitor is not explicitly included, but is the parasitic input capacitance of the inverter and of the transmission gate. The dynamic latch must be refreshed periodically, otherwise its value can be corrupted due to the leakage currents of the transmission gate junction. This impose minimum frequency on the clock signal. For this reason, dynamic latches are used only when it is known a priori that they will always be clocked.

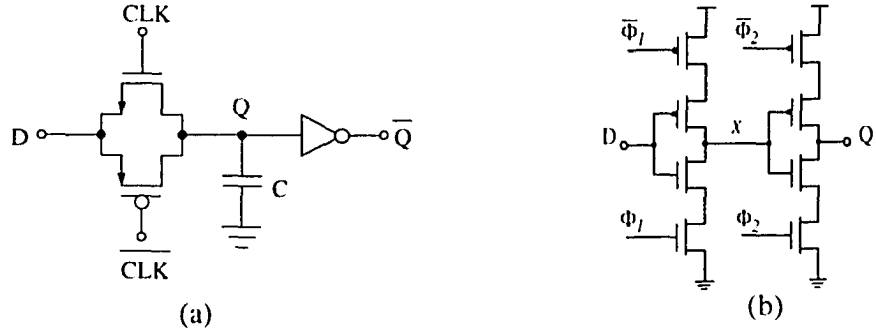


Figure 2.9: Dynamic Latches: (a) Transmission Gate, (b) Clocked Inverter

Other CMOS dynamic latches and flip-flops can be found in [10-13, 22]. Another dynamic master-slave latch, is shown in Figure 2.9(b), it uses a two phase clock to function. It operates as follows. The clock signals Φ_1 and Φ_2 are non-overlapping. With Φ_1 high, $\overline{D}$ is transferred to X but Q is not affected by any change to X. When $\Phi_1 \rightarrow 0$ (and $\Phi_2 \rightarrow 1$), node X is isolated from input D and the inverse of X (true value of D) is transferred to Q and latched.

2.7.3 Transmission-Gate Latches

A static master-slave D-latch based on the transmission gate is often used for digital storage in registers or pipelined circuits. The operation of this overall non-inverting latch is fairly straightforward. The master section inverts the polarity of the applied data and the following slave performs another inversion to restore the correct polarity (see Figure 2.10). With *CLK* high, *TG1* (transmission-gate #1) is on and *TG2* off, making the master latch transparent and causing X to take the value $\overline{D}$. Then, when *CLK* goes low, *TG1* is 'opened', so that X is isolated from the input data. At this time *TG2* will now be closed so that the two inverters are connected in a positive feedback loop which preserves the value of X. Furthermore, the slave latch will now be transparent and $\overline{X}$ (the true value of D) will appear at its output. In other words, Q has become the value of D at the time that *CLK* went low – D will have been latched. This is a classical structure and often used in full swing digital designs. Two disadvantages of this structure are a large clock load and the clock feedthrough characteristic of transmission gates.

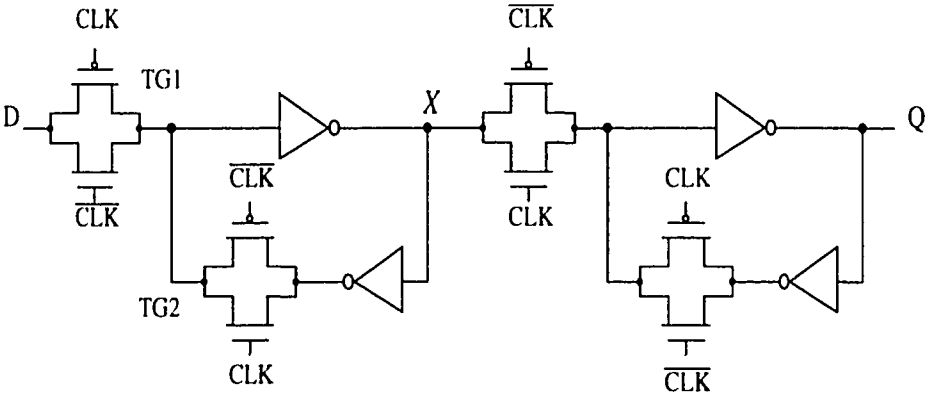


Figure 2.10: A Transmission Gate Master-Slave Latch

2.7.4 Cascode Voltage Switch Logic Latch

A master-slave latch based on 'cascode voltage switch logic' [6] is shown in Figure 2.11. This circuit uses a single clock but has poor noise margin and the use of a regenerative transistor pair in each latch mandates careful design. Its small size and the absence of output to input feedback gives it a potential for very fast operation. But differential latches implemented with this logic style suffer from unequal rise and fall times which can result in short-circuit power dissipation and in glitches which affect succeeding logic stages [1].

In the case of a positive latch, when *CLK* is high the bottom transistors will be conducting and the state of the middle transistors will depend on the data. depending on the data anyone of the middle transistors will be on which will pull the output node to ground which will turn the other PMOS transistor ON and the other output node will be charged to a high voltage level. During the hold mode the cross-coupled transistor pair keeps the outputs in the same state. In the sampling phase the clock and data transistors have to fight against the cross coupled pair to change the stored data in case of any transition. For this reason these transistors need to be small which makes them slower.

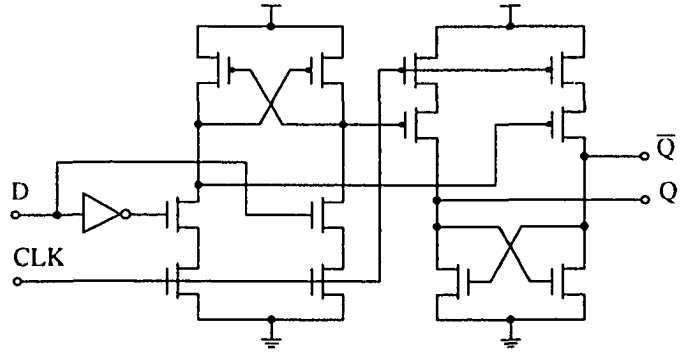


Figure 2.11: CVSL Master-Slave Latch

2.7.5 *Pseudo-nMOS Logic Latches*

In complementary CMOS latches (see Section 2.7.1), the state change of one output forces the other one to change after one inverter delay. This timing skew means that the outputs are not perfect complements. It is possible to eliminate the inverter delay, at the expense of increased power dissipation, if 'pseudo-NMOS' loads are used [4] and differential inputs and clock signals are available.

Referring to Figure 2.12, when *CLK* is high, the latch will be in its tracking (transparent) mode, with its output following its input. If *D* is high there is a conducting path between $\overline{Q}$ and ground, which begins to pull $\overline{Q}$ low. At the same time, since $\overline{D}$ is low, there is high impedance path between *Q* and ground and this node is charged to a high voltage level, through the p-channel transistor. Then when *CLK* is low - in the hold (latch) mode, no current can flow through the data transistors and the circuit becomes effectively a set of cross-coupled 'pseudo-nMOS' inverters which stores the data present at *D* when *CLK* went low.

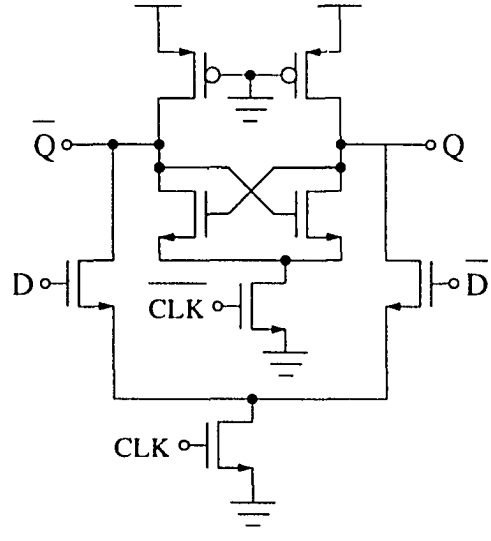


Figure 2.12: Pseudo-NMOS Logic Latch

2.7.6 *Pass-Transistor Logic Latch*

A fully differential pass transistor logic latch [7] is shown in Figure 2.13. This latch combines elements of pseudo-nMOS and pass transistor logic, and unlike the pseudo-nMOS latch it does not dissipate any DC power. It is a true differential design with buffered outputs; it is very useful in differential applications.

In the sampling (transparent) mode a high *CLK* signal allows the data inputs to pass through the bottom transistors. In the mean time the middle cross-coupled transistors driven by $\overline{CLK}$ are non-conducting so their presence does not affect the output state. The CMOS inverter and the PMOS transistor at the top make up a positive feedback loop to latch the data when *CLK* goes low. In this hold (latch) mode with *CLK* low, the output nodes are isolated from any data changes.

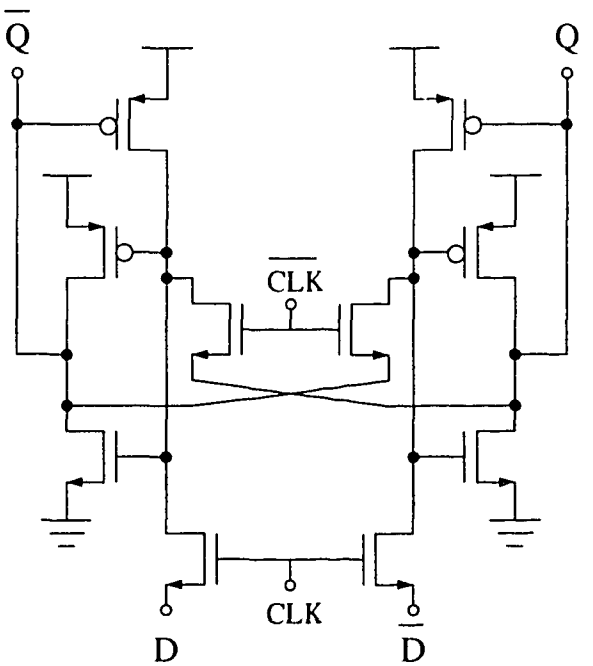


Figure 2.13: Pass Transistor Logic Latch

2.7.7 *Clocked CMOS Latch*

A clocked CMOS latch [4] is based on a clocked inverter structure (basically a three-state inverter) which can be used as a dynamic latch. When *CLK* is low, both clocked transistors are off and the output is in a high impedance state (floating), and the output value will be the inverse of the input value immediately before *CLK* went low. This output value is stored on the combined parasitic junction and next-stage input capacitances.

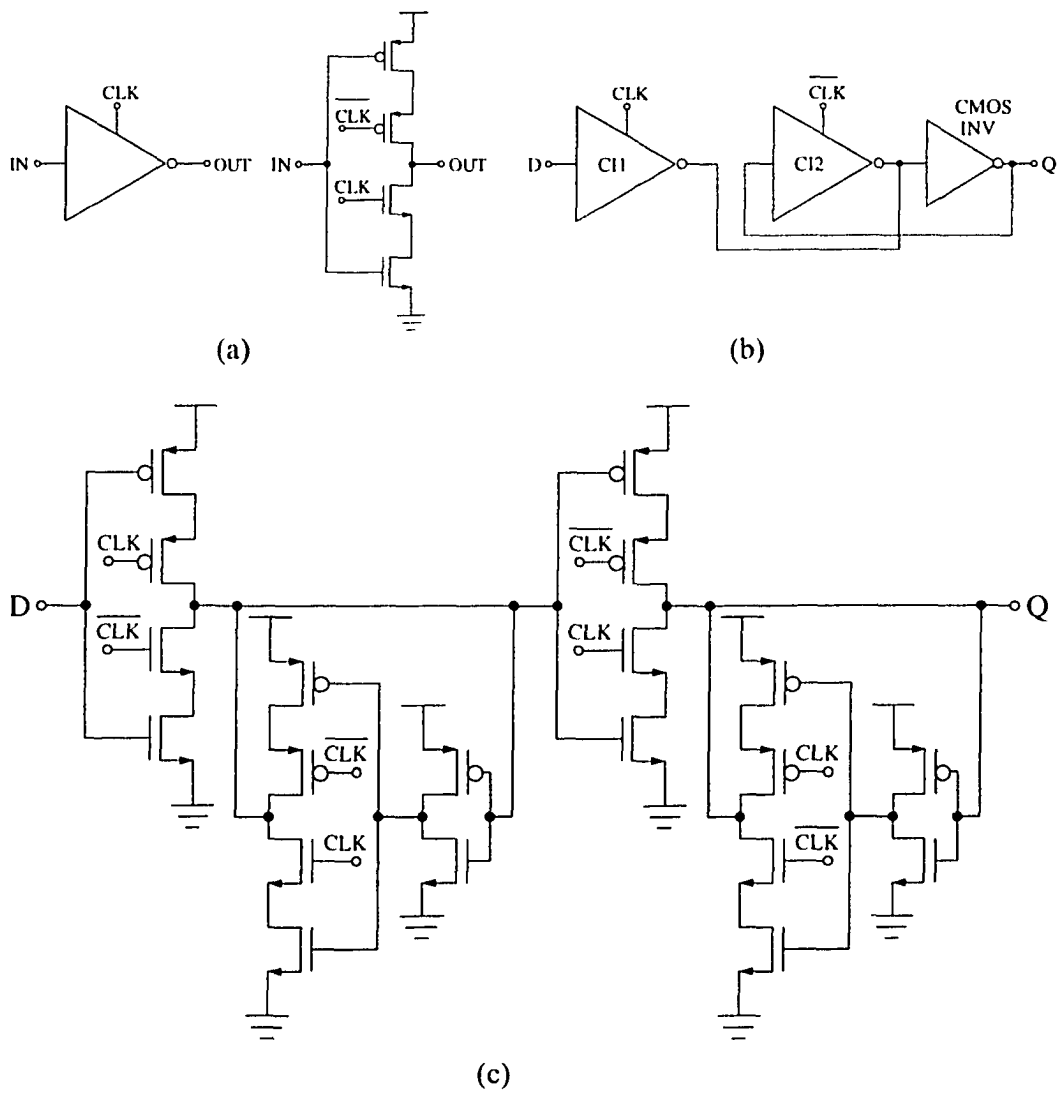


Figure 2.14: (a) Clocked CMOS Inverter (b) Latch Block Diagram (c) MS Latch

The fully-static C^2MOS D-latch combines two oppositely-phased clocked inverters along with a static CMOS inverter as shown in Figure 2.14(b). When *CLK* is high *CI1* (clocked-inverter #1) inverts the data which is then buffered by the CMOS inverter. When *CLK* is low *CI2* and the CMOS inverter form a positive feedback loop which latches the previous state. The C^2MOS master-slave latch has the advantages of low power consumption, presents a low clock load, and has low-power feedback.

PowerPC 603 Latch

The master-slave latch used in the PowerPC microprocessor [19] combines the previously-described transmission gate and clocked inverter structures. It is one of the fastest classical structures. Its main advantages are a short direct path and low power feedback. But it also presents a large clock load, something which greatly influences the total power consumption on-chip.

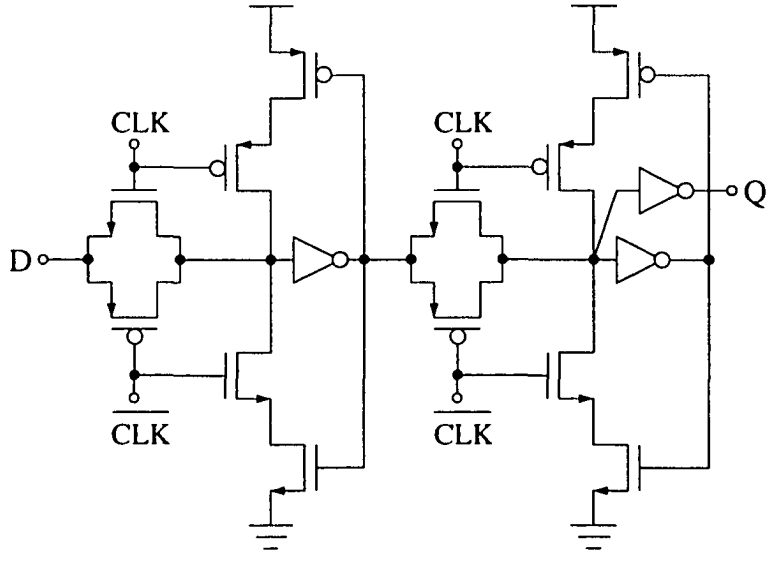


Figure 2.15: PowerPC Master-slave Latch.

2.7.8 Hybrid Latch Flip-Flop

The 'hybrid-latch flip-flop' (HLFF) (see Figure 2.16), presented in [17], is one of the fastest digital storage devices. The main idea of the hybrid design technique is one of greatly shortening the latch's transparency period. The operation of hybrid structures can be easily understood if they are thought of as classical transparent latches with this shortened transparency period. When $CLK = 0$, *N1* and *N4* are off and *N3*, *N6* and *P1* are conducting. Node X is precharged to V_{DD} and node Q holds the previous data. As $CLK \rightarrow 1$ the rising edge of the clock, *N1* and *N4* turn on while *N3* and *N6* remain on for a period determined by the inverter delay chain. During this period that the circuit is transparent and the data at D is sampled into the latch. After some further delay node X is decoupled from D and is either held or begins to precharge to V_{DD} via *P3*. Then, as $CLK \rightarrow 0$, *P1* fully precharges or holds X at V_{DD} so long as the clock remains low.

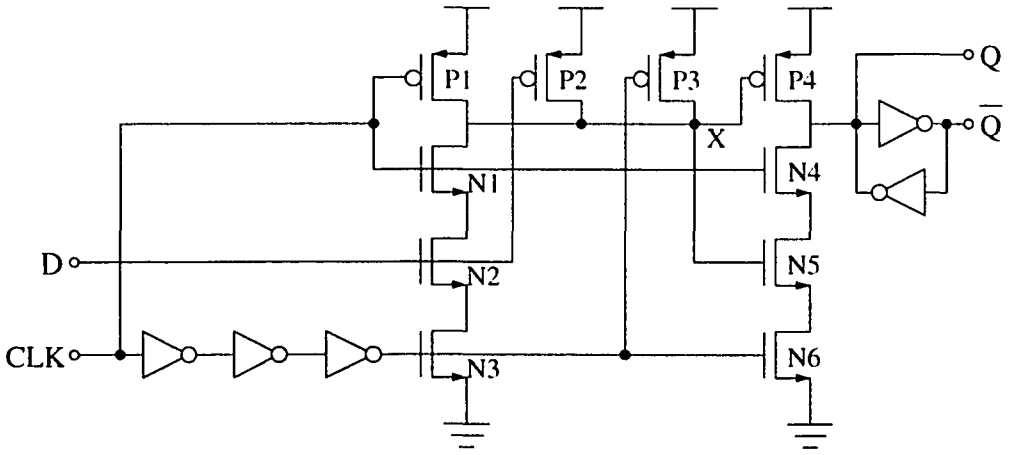


Figure 2.16: Hybrid Latch Flip-Flop

As it is the case with all precharging dynamic structures, their power dissipation depends upon the input data patterns – more energy is expended in the case of '1s' rather than '0s'.

2.7.9 *Semi-Dynamic Flip-Flop*

Another type of flip-flop is the semi-dynamic one, the SDFF [12] (Figure 2.17). The name comes from the fact that the device is a combination of a dynamic front-end and a static back-end. The circuit operates as follows: as $CLK \rightarrow 0$ the flop enters a precharge wherein node X is brought to a high level and node Q is isolated from the input stage. The static latch (cross-coupled inverters *IN3, IN4)* retains the previous value of Q. Since *CKD* is also low during the precharge period, node S remains high and keeps transistor *N1* on. The evaluation phase begins when $CLK \rightarrow 1$. If D is low at this time, (i.e., the flop is latching a zero) node X will remain high, through charge stored on the node capacitance. Node Q would then either remain low or else be discharged through transistors *N4* and *N5*, driving $\overline{Q}$ high. Three gate delays after $CLK \rightarrow 1$, node S will be driven low, turning transistor *N1* off. This shut-off operation will prevent a subsequent low-to-high transition of D from discharging node X. This feature provides the flip-flop its edge-triggered nature.

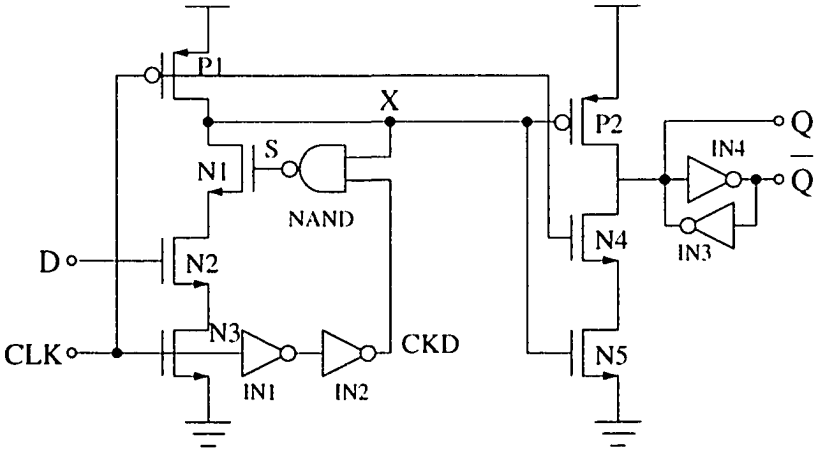


Figure 2.17: Semi Dynamic Flip-Flop

A significant advantage of the SDFF is that there is very little performance penalty when they are used for embedded logic functions. But the larger clock load and a larger

effective precharge capacitance means that there will be increased power consumption when input data contains more '1s' than '0s'.

2.7.10 Sense Amplifier Flip-Flop

A sense amplifier flip-flop (SAFF) uses a sense amplifier (SA) in its first (master) stage and a set-reset (SR) latch in its second stage [10] (see Figure 2.18). The SA stage produces smooth $0 \leftrightarrow 1$ output transitions at clock edges.

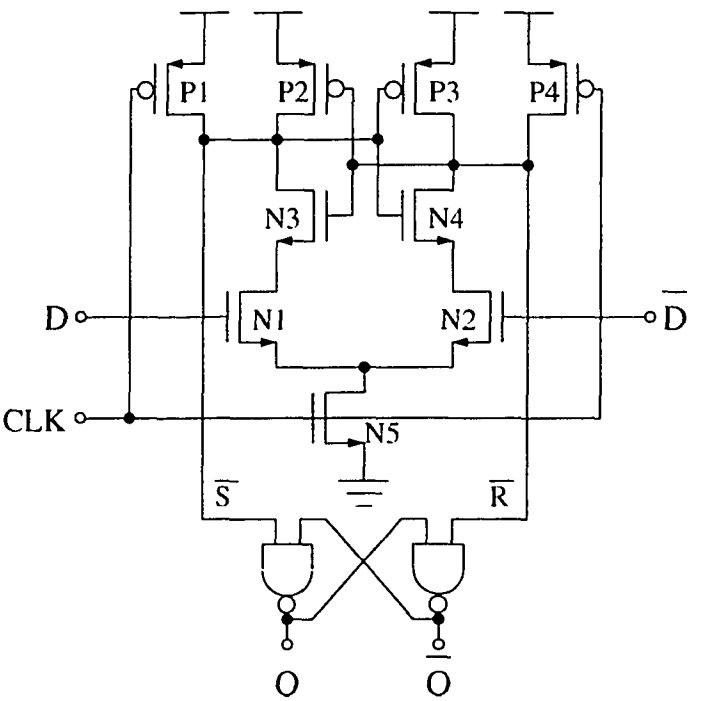


Figure 2.18: Sense Amplifier Flip-Flop

When *CLK* is low, *P1* and *P4* conduct to precharge the $\overline{S}$ and $\overline{R}$ nodes. *P1* and *P2* should be sized as small as possible – the lower limit being determined by their capability to precharge the nodes during half a clock period. During the high state of $\overline{S}$ and $\overline{R}$, *N3* and *N4* conduct, such that their sources are charged up to a high voltage level (because there is

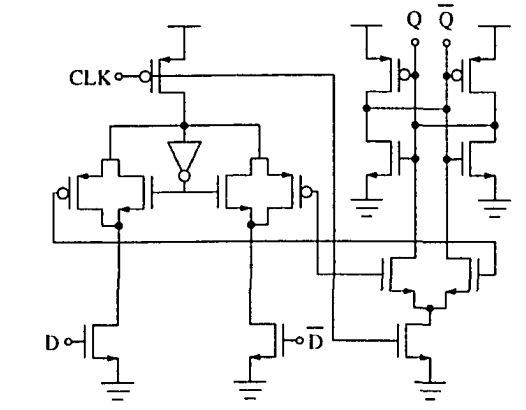
no path to ground due to the off state of the clocked transistor *N5)*. Since one of *N1* or *N2* must be conducting, the common node of *N1*, *N2* and *N5* will also be precharged. Therefore, prior to the leading clock edge, all the capacitances in the differential tree will have been precharged.

The SA stage is triggered on the leading edge of the clock. If *D* is high, node $\overline{S}$ is discharged through the *N3,N1,N5* path, and *N4* will be turned off and *P3* on. On the other hand, when $\overline{D}$ is high (*D* low), node $\overline{R}$ will be discharged through the *N4,N2,N5* path so that *N3* will be turned off and *P2* on. Further data transitions subsequent to these initial changes will not affect the $\overline{S}$ and $\overline{R}$ states. The inputs are decoupled from the outputs of the SA forming the base for the flip-flop operation of the circuit.

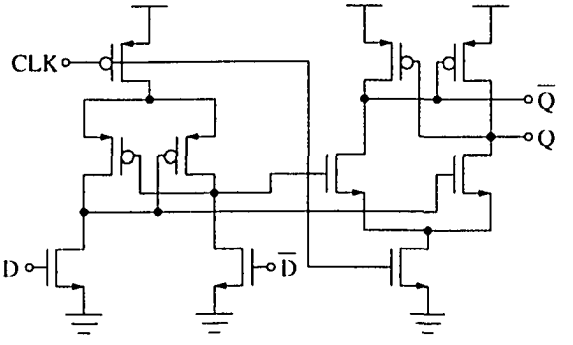
Although the precharged sense-amplifier stage is very fast, the set-reset latch almost doubles the delay [1] because of its asymmetric rise and fall times. This not only degrades speed but also causes glitches which affect succeeding logic stages. This issue is discussed in [11] and a symmetric second stage latch is proposed.

2.7.11 Single Clocked Transistor Latches

TSPC logic is suitable for high speed VLSI circuit operation. Significant advantages are simple clock distribution architectures and so no clock overlap problems [16]. This technique is mainly used in dynamic CMOS circuits where it helps to simplify designs. The true single phase clocking strategy has advantages of a simple and compact clock distribution, high speed and logic design flexibility.



(a)



(b)

Figure 2.19: Single Clocked Transistor Latches (a) Static, (b) Dynamic

2.7.12 Current Mode Logic Latch

Current Mode Logic is a low voltage-swing differential logic style. It employs a constant current source, pull-up loads and a pull-down network. At any given time, all of the current is passing through one of two circuit branches. A detailed analysis of CML operation, timing and power dissipation characteristics will be presented in Chapter 3.

A conventional current mode logic latch [23] consists of a sample stage and a hold stage (Figure 2.20). Which one is conducting is controlled by complementary clock sig-

nals. When the sample pair (a CML buffer) is activated, the input data is continually mirrored at the differential output. This is known as the sampling mode of the latch. On the next clock phase (the CML latch's hold mode) the hold pair becomes active where the cross-coupled latching transistors form a regenerative positive feedback structure which freezes the output data and isolates it from further activity at the *D* input.

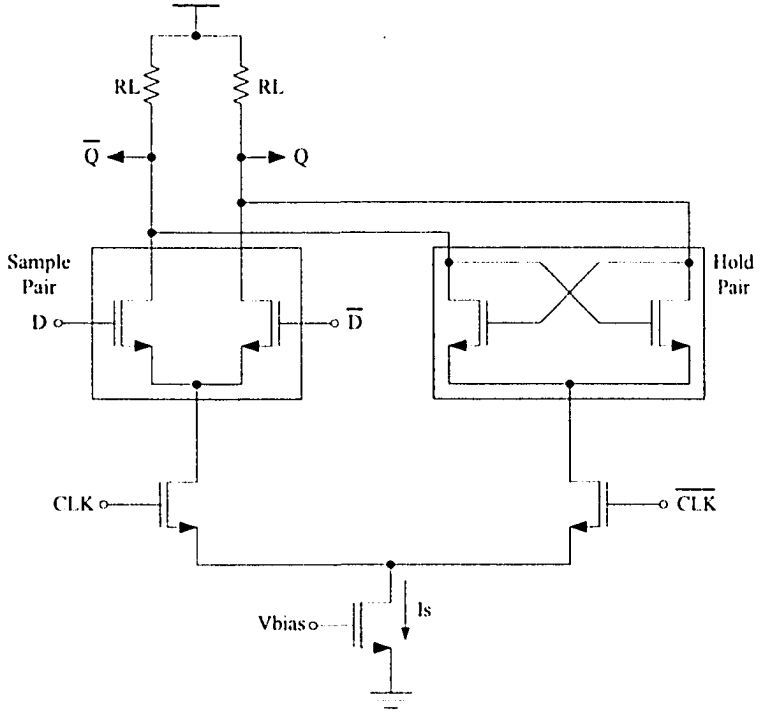


Figure 2.20: Current Mode Logic Latch

2.8 Comparison of Presented Structures

Many latch and flip-flop structures are now only of historical interest and so the emphasis of this thesis will be upon contemporary, state-of-the-art techniques which find use in modern microprocessors and VLSI integrated circuits. For more information please see [10-24].

As was mentioned in Section 2.1, a comparison of selected latches and flip-flops was made using the results of simulation (0.18μm CMOS technology being assumed). To ensure some sort of fairness in the process, the circuits being compared were optimized for speed and power consumption over the frequencies of interest, and then consistent simulation conditions were used when doing the performance evaluations. Only a limited number of latch/FF structures were chosen for comparison. It is felt that the most important issues were addressed. The actual simulation environment and 'test benches' will be discussed in Chapter 5. A master-slave configuration was assumed when the latches were simulated, so that all parameters derived are valid for both FFs and MSLs. The results are summarized in Table 2.1. Furthermore, rising and falling switching delays are not generally equal (so that, for example, T_S for a high level at D will not be the same as T_S for a low level at the same input), and this contingency will be dealt with by always selecting the 'worst-case' value of the two. Comparative plots of average powers and propagation delays of the simulated structures is shown in Figure 2.21.

TABLE 2.1: Latch Timing Parameters

FF/ MSL	T_{CQ} Stable [ps]	T_{DQ} (min.) [ps]	Setup Time [ps]	Hold Time [ps]	$P_{Dissp.}$ [uW]
CMOS	354	305	198	-25	315.72
PowerPC	362	357	312	-45	134.4
HLFF	205	213	34	-6	157.6
TSPC	335	711.6	175	342.7	476.4
PTL	560	960	-200	333.3	288.4
SAFF	298	293	188.6	-40.26	205.1
CML	103	176	45.75	85.1	252.1
Clock frequency = 500MHz, Clock/data rise/fall times = 200ps, Output fanout = 2					

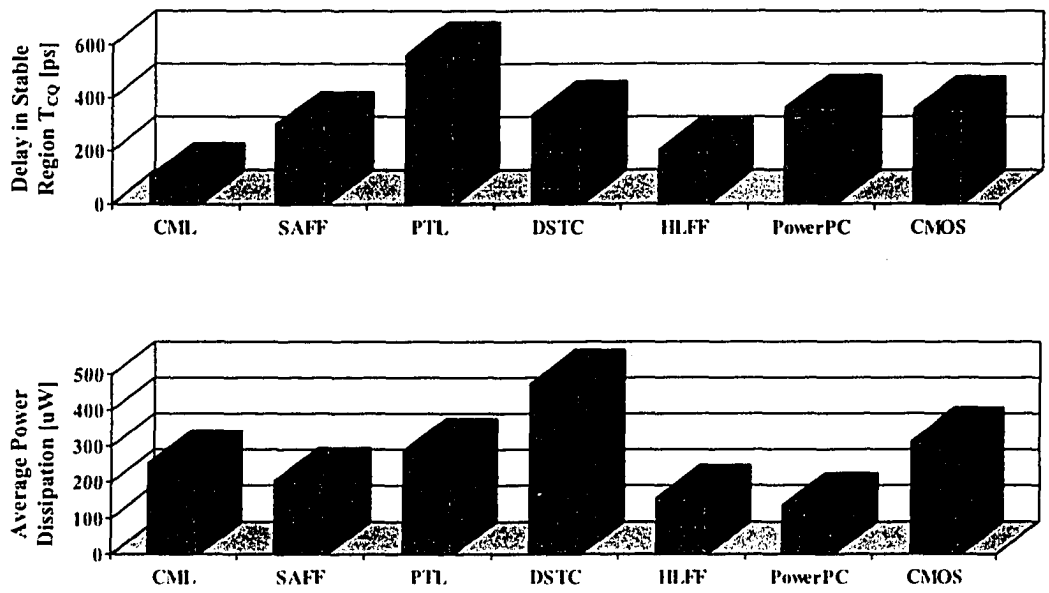


Figure 2.21: Power and Delay Comparison

2.9 Conclusion

The simulation results suggest that in 0.18μm CMOS technology, current mode logic latch offers the smallest propagation delay in the stable region. The power dissipated at the characterization frequency places however in the middle of the simulated structures.

Because of its constant supply current, the power dissipation of the CML latch is almost independent of the operating frequency, something not true of other CMOS structures. The conclusion of the simulation results is that CML latches could exhibit performance levels superior to those of other contemporary clocked storage elements at higher frequencies.

2.10 Chapter Summary

This chapter discusses latch and flip-flop characteristics that are important when the devices are used in synchronous digital systems. The most important structures were described including their operating principles and timing behavior. Simulation was used in an attempt at a fair comparison of the various arrangements, bearing in mind the clocking schemes used and the power availability. The simulation results suggested that the CML latch offers the most favorable time delay and power-consumption figures at very high frequencies.

In the rest of this document, most of the discussion will therefore be concerned with CML latches. A detailed analysis of current mode logic circuit operation and other design considerations is to be presented in Chapter 3.

CHAPTER 3

Design Considerations and CMOS Current Mode Logic

3.1 Chapter Overview

Comparison by simulation of the high speed CMOS clocked storage elements of the last chapter indicated that current mode logic latches are the fastest of all those considered. This architecture has therefore been singled out for a more-detailed study. A detailed analysis of current mode logic style is provided in this chapter, which will lead to a better understanding of the operation and design issues relevant to the CML latches. In addition to the basic timing parameters of clocked storage elements described in the last chapter, additional design constraints must be dealt with when these latches and flip-flops are incorporated into digital systems. This chapter deals with the effects of such factors on the performance and reliability of the system.

3.2 Design Constraints

The more important issues that must be dealt with when designing with CSEs include (principally) latch and flip-flop metastability (see section 2.5), and clock instability (jitter, skew). The origins and effects of these will be described.

3.2.1 Clock Jitter

Jitter is defined as the short-term fluctuations of a clock's period. A parameter 'Δt'

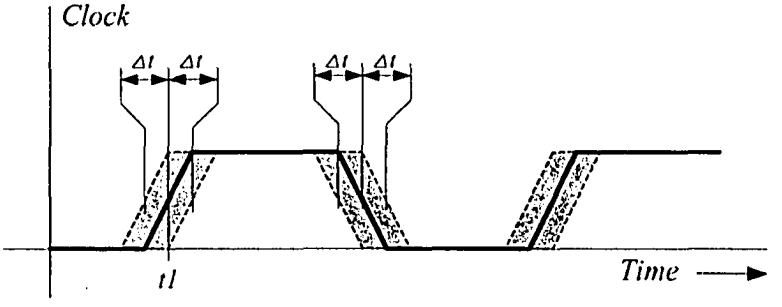


Figure 3.1: Clock Edge Deviation

is defined as the worst case clock edge deviation (see Figure 3.1). If the nominal time of a clock's active transition is t_l, one defines an interval of tolerance around t_l such that the clock edge will occur anywhere between t_l-Δt and t_l+Δt. The tolerance interval $2\Delta t$ is taken to include different types of clock uncertainties – jitter, skew, phase noise, etc.

3.2.2 Minimum Data Pulse Width

The minimum width of the data pulse is the minimum time during which data is required to be stable to ensure correct operation of the latch or flip-flop. It defines a sam-

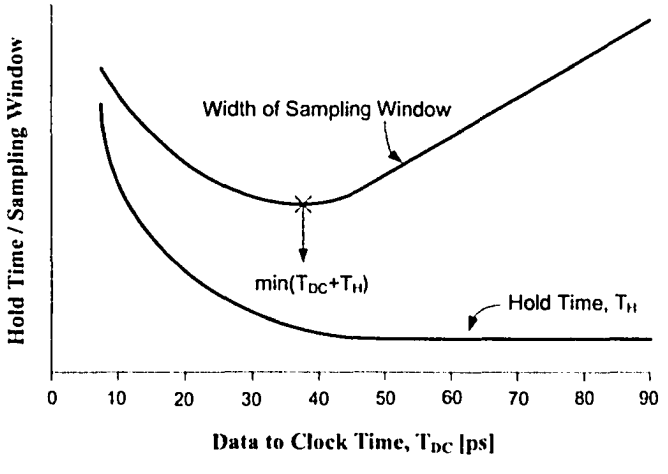


Figure 3.2: Hold Time and Width of Sampling Window as a function of T_{DC}

pling window surrounding the triggering edge of the clock, a time period during which the clocked storage element samples the input and the data must be stable. It is approximately equal to the sum of the setup and hold times (metastable latch and flip-flop behavior, as defined in Chapter 2, causes setup and hold times to vary).

The width of the sampling window as a function of T_{DC} can be obtained by adding T_{DC} to the corresponding hold time T_H, as shown in Figure 3.2. As the latest valid data time gets closer to the active clock edge, the width of the sampling window shrinks to an optimal value, a minimum which is seen to lie in the metastable region.

3.2.3 Minimum Clock Period

CSEs are commonly incorporated in synchronous finite state machine (FSM), having the general structure of Figure 3.3, the flip-flops are in the feedback path of the system. It is important to take into account the minimum and maximum delays associated with the combinational logic blocks. The maximum delay in a logic path $T_{L(max)}$ (the 'long path delay') determines the maximum clocking speed of the system and depends upon the number of logic stages in the signal path. On the other hand, some of the logic signal paths

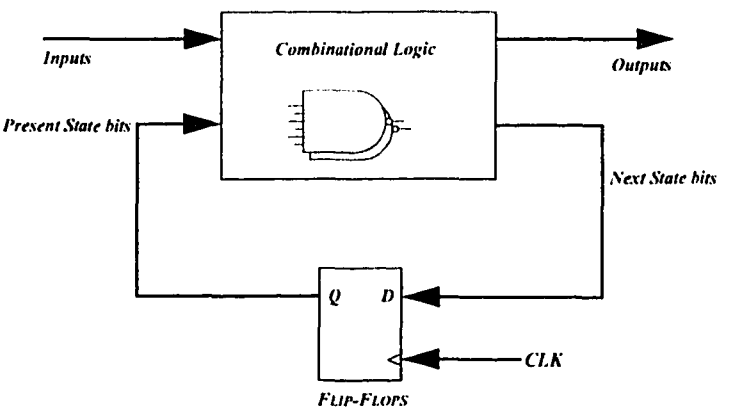


Figure 3.3: Finite State Machine Block Diagram

might have small delays and $T_{L(min)}$, the short path delay, becomes critical in determining the proper functioning of the flip-flops. This is because some D signals may change rapidly enough that hold-time violations occur. These can give rise to glitches and false signals. Therefore, short path delays are often deliberately increased to make them nearly equal to the larger delays in the system [6].

The minimum clock period (maximum clock frequency) at which a particular flip-flop can function properly can be estimated using the above mentioned timing parameters. If the D signal is assumed to arrive on time for the first clock cycle then the latest time of arrival of the D signals (T_{arr}) for the next cycle must satisfy

$$T_{arr} \leq T_{CLK} - (\Delta t + T_S) \tag{3.1}$$

where T_S is the setup time, T_{CLK} the clock period and Δt is the period uncertainty introduced in Section 3.2.1. The latest time at which the D signal would arrive is

$$T_{arr} = \Delta t + T_{CQ} + T_{L(max)} \tag{3.2}$$

The combination of these last two gives

$$T_{CLK} \geq 2 \cdot \Delta t + T_{CQ} + T_S + T_{L(max)} \tag{3.3}$$

To ensure that there will be no hold-time violations, D must remain stable for a time $\Delta t + T_H$ after the active clock edge. In terms of short path delays, it is clear that D must not change faster than once every $T_{L(min)}$, where

$$T_{L(min)} \geq 2 \cdot \Delta t + T_H - T_{CQ(min)} \tag{3.4}$$

Any logic path delay less than the one given by Equation (3.4), will cause a hold time violation.

3.2.4 Optimum Setup Time

In order to make optimal use of the clock cycle time, one must consider how closely should data be allowed to change with respect to the clocking event. Here, there are two opposing requirements [2]: (a) T_{DC} should be kept well out of the failure region, to ensure design reliability. But (b), it should be as small as possible, in order to increase the time available for logic operations. This is an obvious dilemma. From Figure 3.4 we can see that in spite of an increasing T_{CQ}, advantage is still being gained because the time taken from the cycle is reduced – the increase in delay from the storage element (T_{CQ}) is still smaller than the amount of delay introduced to the cycle (T_{DQ}), so that there will be more time left for intended logic operations of FSM combinational block. T_{DC} corresponding to the $T_{DQ(min)}$ is, therefore, considered to be the optimum setup time.

Interestingly the optimum setup time also corresponds to the point of minimum width of the sampling window (see Figure 3.2). That is, data needs to be stable in the same state for a minimum period, if it changes at the optimum setup time.

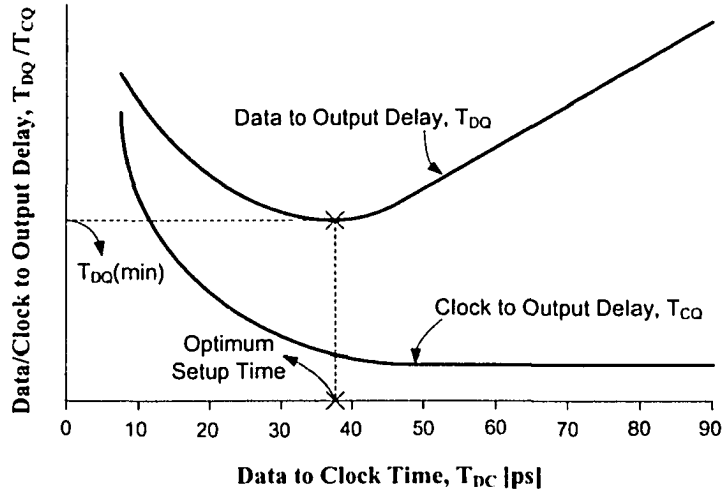


Figure 3.4: $T_{DQ(min)}$ and Optimum Setup Time

3.3 Current Mode Logic

Current mode logic (CML) is one of the most widely used logic styles for high speed digital circuits. It was initially developed for bipolar transistors, but as MOS technology improved and device-sizes scale down, MOS implementations became practical and attractive (The logic family is sometimes referred to as MOS Current Mode logic or MCML.) In this thesis the terms CML and MCML will be used interchangeably, unless otherwise specified.

The general CML circuit consists of three main components (see Figure 3.5): a pull-up load, a pull-down network (PDN) and a constant current source [26]. CML is a completely differential and static logic style and because of this differential nature, it is highly immune to common mode noise. The less than rail-to-rail output swing of a CML device means that the output settling times will be reduced, with the result of faster device operation. It has almost flat power curve over a wide range of frequency as opposed to other logic styles where power consumption increases directly with frequency. At very

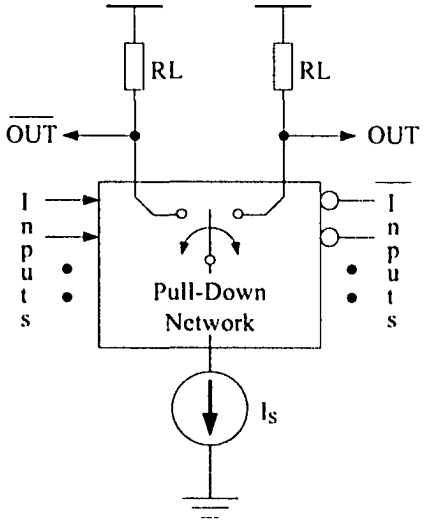


Figure 3.5: General CML Circuit Structure

high frequencies (multi-gigahertz) its power consumption is comparable or even lower than that of other logic styles.

3.3.1 CML Circuit Operation

The principle of operation of current mode logic circuits can be understood in terms of current steering (see Figure 3.6). The gate branch into which the source current (I_S) is directed depends upon the input combination and the logic implemented by the pull-down network. The voltage at the output of branch which carries no current reaches V_{DD}, but in the other branch the voltage drop across R_L causes the output voltage to be limited to $V_{DD} - I_S R_L$. The output voltage swing is therefore $\Delta V = I_S R_L$.

3.4 CML Circuit Analysis

The CML inverter/buffer circuit shown in Figure 3.6 is an example of a 'single level' CML gate. I_S, the bias current is set by the voltage V_{bias} applied to transistor M_S, and the drain voltage of M_S is V_X.

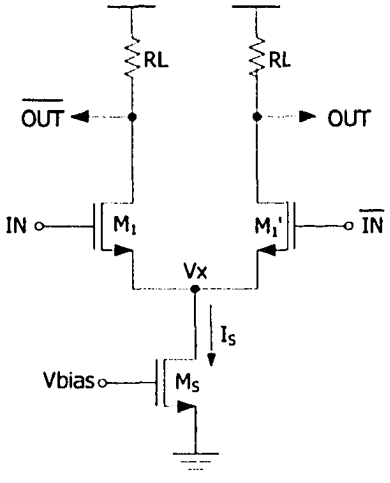


Figure 3.6: CML Inverter/Buffer

3.4.1 Minimum Supply Voltage

Lowering the supply voltage is the most effective technique for reducing the power consumption of an integrated circuit [27]. In the case of CML, the minimum supply voltage $V_{DD(min)}$ is that for which all the transistors in the circuit may be simultaneously in saturation, including the current source and the differential pairs of all levels. For the circuit of Figure 3.6,

$$V_{DD(min)} = V_{DS(SAT)} + V_{GS2} + \Delta V \tag{3.5}$$

where $V_{DS(SAT)}$, V_{GS2} and ΔV are respectively the drain-source saturation voltage of M_S, the gate-source voltage of M_1 and the output voltage swing.

The drain-source saturation voltage can be written as

$$V_{DS(SAT)} = V_{GS} - V_{TH} \tag{3.6}$$

And the saturation region value of V_{GS} is

$$V_{GS} = \alpha\sqrt{\frac{I}{K}} + V_{TH} \tag{3.7}$$

where α was introduced as a modification in the Shockley's square law [25], V_{TH} is the device's threshold voltage and I is the channel current and $K = \frac{1}{2}\mu_0 C_{OX}\left(\frac{W}{L}\right)$. The symbols μ_0, C_{OX}, W and L represent the electron mobility, gate oxide capacitance, transistor width and transistor length, respectively.

On substituting these into Equation (3.5) (and assuming that all the current flows through the conducting branch i.e. $I_S = I_1$), one finds

$$V_{DD(min)} = \alpha\sqrt{\frac{I_S}{K_S}} + \alpha\sqrt{\frac{I_1}{K_1}} + V_{T1} + \Delta V \tag{3.8}$$

And if it also assumed that $K_S \approx K_1$,.

$$V_{DD(min)} \approx \sqrt{K(V_{bias} - V_{TS})^{\alpha}}\left(\frac{2}{\alpha\sqrt{K}}\right) + V_{T1} + \Delta V \tag{3.9}$$

where V_{bias} is the current-source bias voltage and V_{TS} and V_{T1} are the threshold voltages of the M_S and M_1 transistors, respectively. Note that V_{TS} and V_{T1} are different because of the body effect.

Equation (3.9) gives us the minimum value of the supply voltage that will ensure correct functionality and adequate performance of the circuit.

3.4.2 DC Biasing of CML gates

If both inputs of the buffer are at mid-swing voltage (i.e. $V_M = V_{DD} - \Delta V/2$, where V_{DD} is the supply voltage and ΔV is the output voltage swing), the currents in the two branches will be equal to $I_S/2$ and the output voltages will be

$$V_o = V_{DD} - \frac{I_S}{2} \times R_L = V_{DD} - \frac{\Delta V}{2} = V_M \tag{3.10}$$

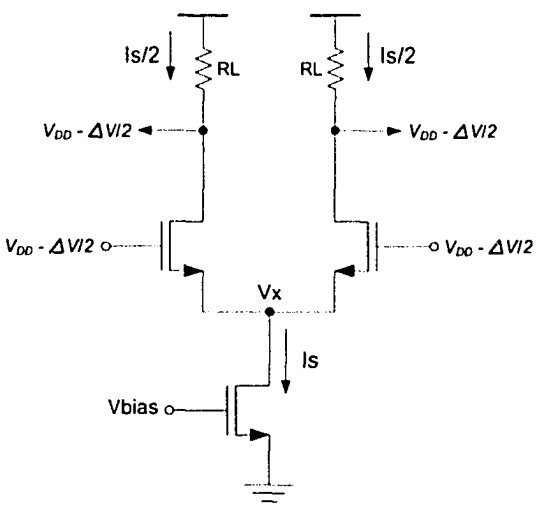


Figure 3.7: CML Inverter DC Bias

Since transistors M_1 and M_2 have identical drain and gate voltages, both will be in saturation with each carrying a current given by

$$\frac{I_S}{2} = \frac{\mu_0 C_{OX}}{2}\left(\frac{W}{L}\right)(V_{GS} - V_{T1})^{\alpha} \tag{3.11}$$

3.4.3 Output Voltage Swing Range

The output of a digital CML buffer can take one of the two values – either V_{DD} or V_{DD} - ΔV. The cascading of CML cells requires that the input and output swings, both in common mode and differential, be equal. An expression for the permissible range of ΔV is given in [27]. For the input transistors to be in saturation

$$(V_{DD} - \Delta V/2 - V_X) \geq V_{T1} \tag{3.12}$$

where V_{T1} is the threshold voltage of transistor M_1 and V_X is voltage at the drain of the current source, as shown in Figure 3.7. Actually ΔV can not exceed V_{DD}, therefore

$$\Delta V \leq min[2(V_{DD} - V_{T1} - V_X), V_{DD}] \tag{3.13}$$

For proper switching, the voltage V_{DD} - ΔV must be low enough to switch off the transistor of the next stage.

$$(V_{DD} - \Delta V - V_X) \leq V_{T1}$$

$$\therefore \Delta V \geq (V_{DD} - V_{T1} - V_X) \tag{3.14}$$

On combining Equation (3.13) with Equation (3.14), it is found that ΔV must satisfy

$$min[2(V_{DD} - V_{T1} - V_X), V_{DD}] \geq \Delta V \geq (V_{DD} - V_{T1} - V_X) \tag{3.15}$$

But this only places upper and lower bounds on ΔV – the actual value that is used will depend upon system requirements.

3.4.4 Large Signal Transient Behavior

When a large signal is applied to a CMOS transistor gate, the resulting switching process goes through three phases:

1. Input charging to threshold
2. Channel formation and device turning 'on' after a $1/f_T$ delay
3. Output charging

In the first step the input capacitance is charged to the device threshold voltage by the input signal. This time, usually very small, is governed by the input slew rate and the gate capacitance. Once the gate voltage reaches threshold, channel formation commences and the device turns on after a delay of $1/f_T$. This delay is technology dependent and is proportional to the channel length. The sum of the time taken by first two phases is known as the intrinsic delay, denoted T_i. After this delay, current begins to flow through the device and begins charging the output capacitances. While this is occurring, the input is fully charged and the device will enter its saturation region. Output charging is usually the dominant of the three steps.

3.4.5 CML Circuit Delay

Delay of a CML gate τ, is the time it takes to charge/discharge the outputs to the mid-swing voltage V_M, following any input transition. It can be expressed as

$$\tau = (\Delta V/2)\frac{C_L}{Is} + T_i \qquad (3.16)$$

where ΔV is the voltage swing, C_L is the total output load capacitance, and T_i is the intrinsic transistor delay, as described in Section 3.4.4.

On substituting the value of I_S from Equation (3.11), one finds

$$\tau = \frac{(\Delta V/2)}{\mu_0} \frac{C_L}{C_{OX}\left(\frac{W}{L}\right)(V_{GS} - V_{T1})^{\alpha}} + T_i \tag{3.17}$$

If it is assumed that the load is a next-stage CML gate, i.e. $C_L = C_{OX}WL$,

$$\tau = \frac{\Delta V}{2\mu_0} \frac{L^2}{(V_{GS} - V_{T1})^{\alpha}} + T_i \tag{3.18}$$

minimum value of ΔV from Equation (3.15) is,

$$\Delta V_{min} = V_{DD} - V_{T1} - V_X$$

and, from Figure 3.7

$$V_{GS} - V_{T1} = V_{DD} - \Delta V/2 - V_X - V_{T1} = \frac{(V_{DD} - V_X - V_{T1})}{2}$$

Finally, substitution in Equation (3.18) yields

$$\tau = \frac{V_{DD} - V_X - V_{T1}}{2\mu_0} \frac{L^2}{\left(\frac{V_{DD} - V_X - V_{T1}}{2}\right)^{\alpha}} + T_i$$

$$\tau = \frac{2L^2}{\mu_0 (V_{DD} - V_X - V_{T1})^{\alpha - 1}} + T_i \tag{3.19}$$

The only readily-adjustable variable in this expression for τ is V_X, as all the other quantities are technology dependant. Because of the differential nature of CML, the inter-

nal voltage V_X should almost be constant even during switching. However, due to the overlap capacitance C_{GS} of the differential pair transistors, data feedthrough effects can be seen at this node. It is clear that V_X should be kept as low as possible to achieve high switching speed, or in other words (V_{GS}-V_{TI}) should be kept as large as possible. Actually, reducing the value of V_X decreases V_{TI} (due to the body effect) and so increases (V_{GS}-V_{TI}) further [27]. A common practice to minimize the node voltage V_X, is to increase the aspect ratio (W/L) of the current biasing transistor; however, the negative effect of this approach is increase of capacitance at node X.

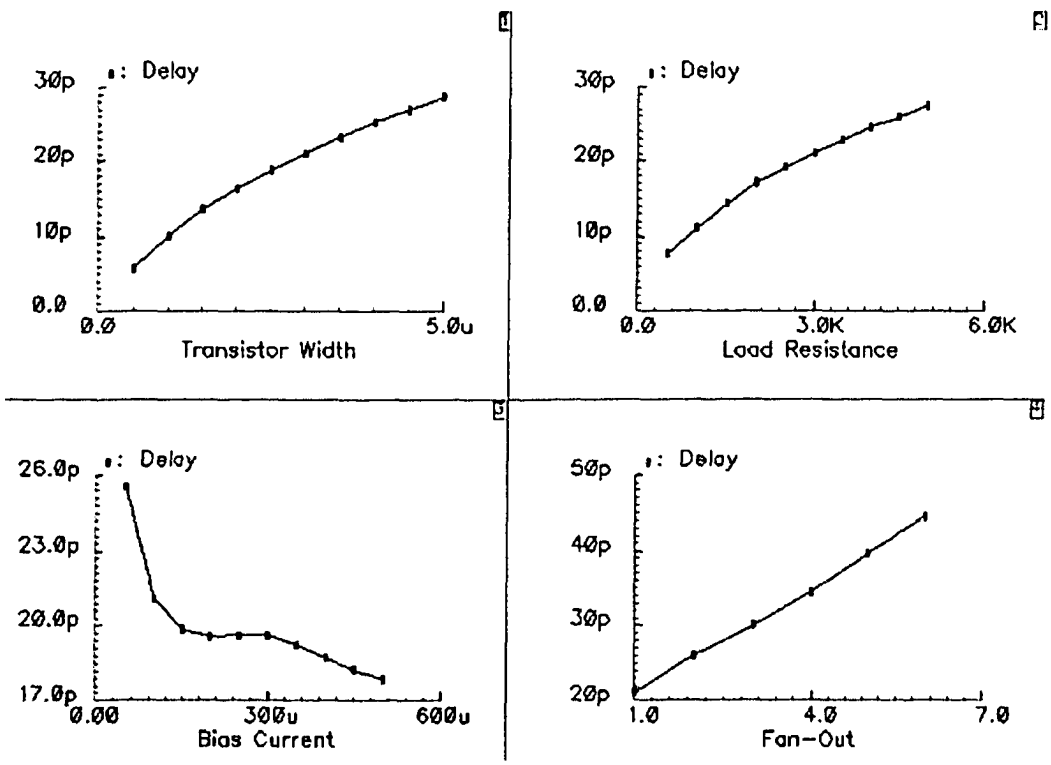


Figure 3.8: CML inverter delay versus (i) Transistor Width, (ii) Load Resistance, (iii) Bias Current and (iv) Fan-out

Figure 3.8 shows the simulated effect of varying certain parameters on the delay of a CML inverter. It can be seen that the CML inverter's delay is directly proportional to the load resistance value, output loading and also to the transistor width, due to a resulting increase in the capacitance. A larger bias current results in smaller delay. The observed non linearity in the delay is a result of changing output voltage levels (because the output voltage swing is a function of current through the load resistor).

3.4.6 Voltage Swing Ratio

Voltage swing ratio (VSR) is defined as the ratio of output and input voltage swings in a CML gate. Ideally all the bias current flows in the *ON* branch. In that case the output and input voltage swings are equal (*VSR=1*). But in reality, some finite amount of current flows in the *OFF* branch as well, so that *VSR<1*. The output voltage swing might be recovered through adjusting the biasing current I_S, and the load resistor R_L, however, a common mode offset voltage will be introduced.

3.4.7 Constant Current Source

A current mirror (see Figure 3.9) can be used to supply the constant current needed by a CML gate.

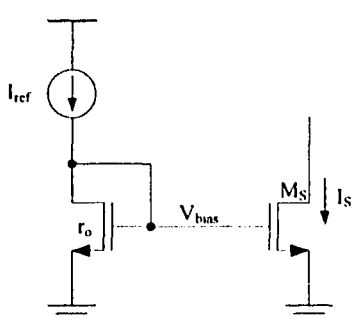


Figure 3.9: NMOS Current Mirror

The output impedance of a MOS transistor is given by

$$r_o = \frac{1}{\lambda I} = \frac{1}{\lambda K(V_{bias} - V_{TS})^{\alpha}} \tag{3.20}$$

where λ is the output impedance constant and V_{bias} and V_{TS} are the biasing and threshold voltages of the current source respectively.

$$\frac{I_S}{I_{ref}} = \frac{1 + \lambda V_{DS}}{1 + \lambda V_{DSref}} \tag{3.21}$$

With a high output impedance, the actual current flowing through the current source would be very close to the reference current source.

In mixed signal environments, a steady current in the V_{DD} supply is beneficial. There will be some current change during switching due to non-idealities such as partial current conduction and current peaking due to large biasing transistor, but *dI/dt* effects are negligible in comparison to other logic styles. The circuits are also significantly more robust against power supply noise due to their inherent common mode rejection.

3.4.8 Common Mode Rejection Ratio

The common mode rejection ratio (CMRR) here measures the ability of a CML gate to reject common mode signals (noise) at its inputs, so as to not corrupt the output. A high CMRR means that smaller voltage swings and correspondingly higher speeds may be realized, which consequently enhances speed. Furthermore, it will reduce the effect of differential-pair threshold voltage mismatch on the CML output amplitude [30].

3.4.9 CML Circuit Gain

The dc differential gain of the CML circuit is approximately:

$$G(0) = G(0)_{ideal}\left(\frac{r_{o1}R_L}{r_{o1}+R_L}\right) \tag{3.22}$$

where $G(0)_{ideal} = gmR_L$ is the ideal dc differential voltage gain ($r_o = r_{o1} = \infty$) and R_L the load resistance. The resistances r_o and r_{o1} in the above equation are the output impedances of the current source and the top level differential pair respectively.

A CML latch can perform its function without the need for high gains in the transistors of its differential pairs – the inherent ability to reject common-mode noise means that a CML latch can work with low signal levels and low gains, a situation that is attractive because the undesired effects of process variations or transistor or resistive load mismatches will not be excessively amplified. A gain of just over unity is in fact sufficient to achieve regeneration and bi-stability as well as immunity against process, voltage and mismatching conditions.

3.4.10 Signal Slope Ratio

In a CML gate, the *RC* time constant of the pull-up load determines the rise time, while it is the transconductance of the NMOS transistors that determines the fall time. Ideally, they can be closely matched. But this is prevented in actuality by the fact that real circuits are only approximately linear. It is possible, however, to make one of the two times substantially shorter than the other and gain an effective reduction in the circuit propagation delay.

Clearly a trade-off between rise/fall time T_r and propagation delay T_p exists. The

signal slope ratio is therefore defined as the ratio of *Tr* and *Tp*. Normally it achieves a value between 2 and 10, but a small value is preferred.

$$SSR = T_r / T_p \tag{3.23}$$

3.4.11 Power Dissipation

The power consumption of a non-CML circuit strongly depends on its structure and on the statistics of the applied data. But CML devices, with their constant current structures, are to a large extent immune to data-pattern differences. In fact, CML has a flat power spectrum over a wide range of frequencies., given by

$$P = I_S V_{DD} \tag{3.24}$$

where I_S is the biasing current and supply voltage is V_{DD}.

3.5 Multi-Level CML Gates

The analysis of CML circuits in the last sections was facilitated with the example of a CML inverter, which is a single level CML gate. However, multi-level circuits (series-stacked NMOS devices) are often employed for complex logic functions in CML. By way of example the CML D-Latch is frequently used in the design of multiplexers, demultiplexers and frequency dividers for high-speed optical communication circuits. Most common CML gates like AND, OR, NAND, NOR and so forth have two such levels.

But series-connected MOSFETs utilizing the same input voltage swings cannot be operated in their saturation region [28]. This point will now be examined.

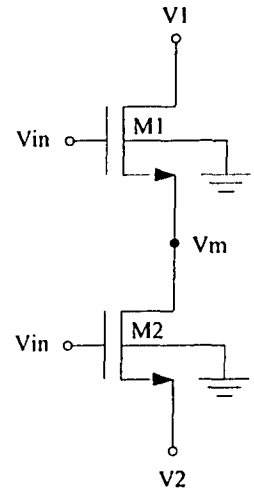


Figure 3.10: Series Connected MOSFETS

Figure 3.10 shows two series connected NMOS transistors. V_{in} is the common input voltage and V_m is the middle node voltage. Let V_{T1} and V_{T2} be the threshold voltages of *M1* and *M2* respectively. The essential conditions for an NMOS transistor to be operated in saturation are

$$V_{GS} \geq V_T \tag{3.25}$$

and $$V_{DS} > V_{GS} - V_T \tag{3.26}$$

For the upper transistor, *M1*, to be in saturation,

$$V_{GS1} \geq V_{T1}$$

$$V_{in} - V_m \geq V_{T1} \Rightarrow V_{in} \geq V_m + V_{T1} \tag{3.27}$$

And for the lower one,

$$V_{DS2} > V_{GS2} - V_{T2}$$

By combining Equation (3.27) and Equation (3.28), we can get the input voltage

$$V_m - V_2 > V_{in} - V_2 - V_{T2} \Rightarrow V_{in} < V_m + V_{T2} \tag{3.28}$$

that is required to operate both of these transistors in saturation

$$V_m + V_{T1} \leq V_{in} < V_m + V_{T2} \tag{3.29}$$

Clearly if V_{T1} and V_{T2} are equal then there is no possible value of the input voltage for which both transistors might be in saturation region. Equation 3.30 can however be satisfied if $V_{T1} < V_{T2}$. The effect of substrate bias in this situation will now be considered. The threshold voltage change due to the body effect is given by [5, pp. 69-71]

$$V_T = V_0 + \gamma(\sqrt{V_{SB} + |2\Phi_F|} - \sqrt{|2\Phi_F|}) \tag{3.30}$$

where V_0 is the zero bias threshold voltage, V_{SB} is the source-bulk voltage, γ is called the body-effect constant and Φ_F is the Fermi potential of substrate.

It can be seen that V_T is proportional to V_{SB}, and V_{T1} will actually be higher than V_{T2}, which results in input voltage levels for which both devices are not in saturation. Voltage level shifters have been employed in order to solve this problem [28] by reducing the input voltage swing entering the lower-level transistors. These level shifters contribute to greatly-increased power consumption in the CML circuits for which they are used.

The use of multi-threshold devices for the various levels of multi-level CML can eliminate the need for level shifters with a common input voltage swing being used to operate all of the transistors in their saturation regions. However, the implementation of this technique requires special fabrication methods.

3.6 Swing Control in CML Circuits

The maximum operating frequency and the required operating power of a CML gate can be controlled dynamically with gate bias adjustments. This mechanism enables performance vs. power compromises to be made during the circuit operation. The load resistors can also be replaced by active PMOS loads and a bias control circuit is utilized in stabilizing the output swing by controlling the active load and the current source biasing [49], as shown in Figure 3.11. The problem of output amplitude drop-off at high frequencies (due to slew limiting) can also be remedied with this approach.

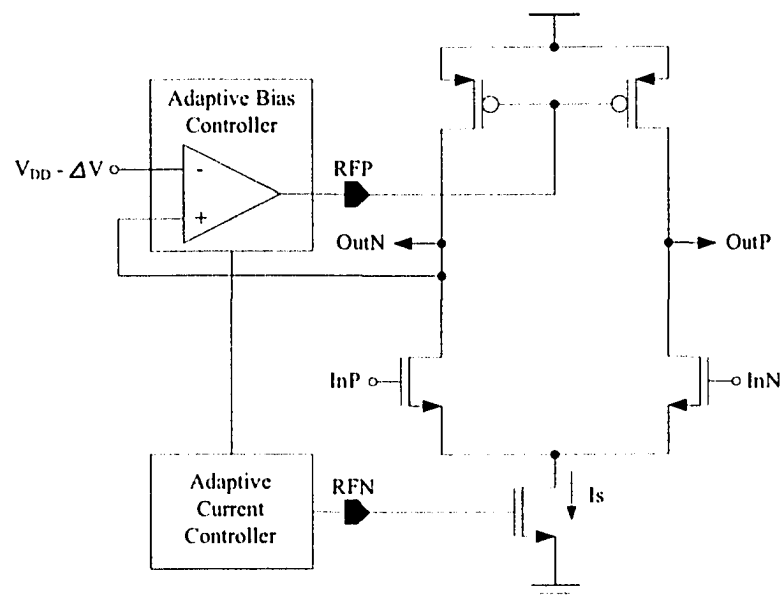


Figure 3.11: Adaptive Bias Control for CML gates

3.7 Chapter Summary

This chapter addressed the design considerations for an efficient and reliable system employing clocked storage elements. In addition, a detailed analysis of current mode logic circuits laid the foundations for the next chapter's closer look at CML latch operating principles and at the design challenges which are encountered.

CHAPTER 4

Current Mode Logic Latches and Prescaler Design

4.1 Chapter Overview

The previous chapter described the principles of current mode logic circuit operation. In this chapter these ideas will be extended to a study of the operation of a conventional CML latch. The effects of clock transition time on the characteristic parameters of a CML latch will be discussed. Some performance-limiting factors and the latch modifications to deal with them are also discussed. A modified CML latch structure is presented, one which effectively reduces setup and hold times. Finally, some new dual modulus frequency prescaler design techniques are reported.

4.2 The Conventional CML Latch

A conventional current mode logic latch consists of a sample and a hold stage, as shown in Figures 2.18 and 4.1 [26]. Current switching between transistor pairs is controlled by complementary clock signals. The sampling pair works as a CML buffer and when it is activated by the clock signal, it tracks the input data and transfers it to the outputs. This is known as the sampling mode of the latch. The hold pair becomes active when the clock polarity changes. The cross-coupled transistors in the hold pair form a regenerative positive feedback structure which retains the output data at the current state.

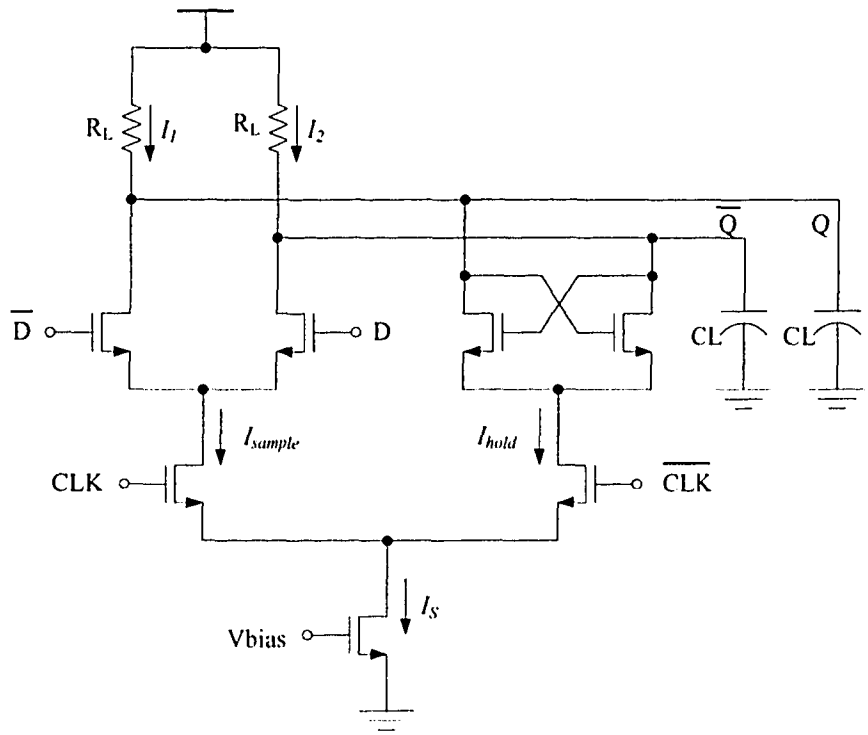


Figure 4.1: A Conventional current mode logic latch

In a properly-biased CML circuit, all of the biasing current I_S flows through either one of the two branches. As explained in Section 3.3.1, the low output voltage takes a value $V_L = V_{DD} - I_S R_L$, and the other output of the branch with no current remains at the high level $V_H = V_{DD}$. The output voltage swing ΔV is therefore $V_H - V_L = I_S R_L$. Ideally all the input and output signals have the same voltage swing ΔV with a common mode voltage $V_M = V_{DD} - \Delta V/2$.

Let I_1 and I_2 be the currents flowing through the two loads, and I_{sample} and I_{hold} be the currents flowing through the sample and the hold pairs respectively. The total capacitance at the output of the latch is given by

$$C_o = C_L + C_j + C_{Hold} \tag{4.1}$$

where C_L is the load capacitance, C_j is the drain to bulk junction capacitance and C_{Hold} is the parasitic capacitance at the drain of the cross-coupled hold pair. It is interesting to note that the output capacitances during the sample and the hold modes are not equal because of the change in the operating region of the active devices [5]. These unequal output capacitances result in unequal rise and fall delays. Contributions to the total output capacitance in both modes of latch operation are enumerated in Appendix-A. It will be assumed that the CML latch is driving an identical CML latch or buffer. It should be observed that the load capacitance C_L will vary as a function of the following stage's biasing conditions.

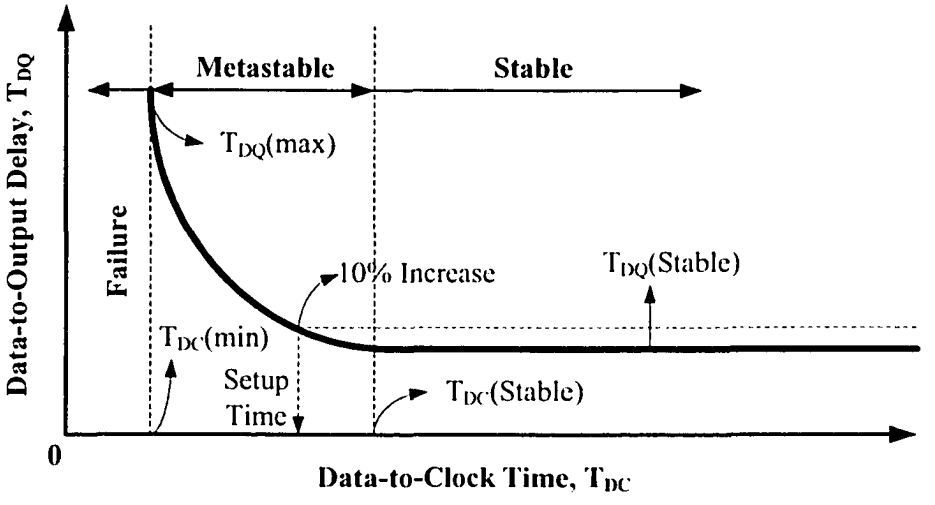


Figure 4.2: CML latch delay in different stability regions

For smaller T_{DC} near the clock edge, the latch propagation delay T_{DQ} increases due to a finite current transition time and could causes device metastability. The following section presents a detailed analysis of CML latch delay and the dependence of its characteristic parameters on the input signal slew rate.

4.3 Analysis of CML Latch Delay

As described in Section 3.4.4, any change in a signal with a finite slew rate will take some time to begin affecting the voltage and current levels in the device. This delay, denoted *Ti*, depends on the size and biasing conditions of the device. After this internal turn-on delay the current flowing through the device and the charging or discharging of the output capacitance starts. The T_i delay is usually small in comparison to the output charging time.

Different clock and data transition times will have different effects on CML latch propagation delay. In the following analysis data and clock rise and fall times will be assumed equal and be denoted T_r. At multi-gigahertz frequencies these rise/fall times are a significant fraction of the clock period. The waveform often resembles a sinusoidal wave, so entering the metastable region is unavoidable. Terminologies used in the analysis are illustrated in Figure 4.3.

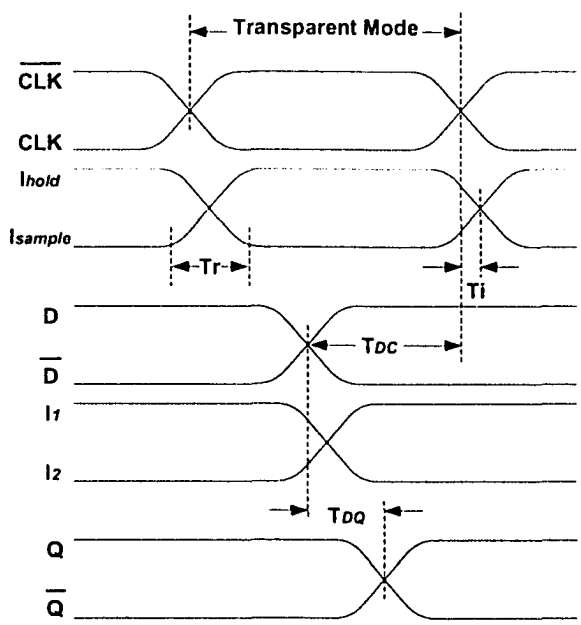


Figure 4.3: Latch delays and current switching times

4.3.1 Propagation Delay in the Stable Region

If the most recent change in the data was made during the transparent mode of the latch, well before the active edge of the clock, the output will change accordingly after a delay $T_{DQ(Stable)}$. If the data changes from a low to a high voltage ($V_L \rightarrow V_H$) in a time T_r, after an interval T_i the flow of current will switch from branch I_1 to I_2 in time T_r. Still all the current is still flowing through the sample pair, because there is no change in the clock signal. When the current transition starts, the output will start charging, eventually attaining a final value V_0 at the end of the transition period:.

$$V_0 = V_L + \frac{1}{C_O}\int_{-T_r/2}^{T_r/2} I_S dt = V_L + \frac{1}{2}\frac{I_S T_r}{C_O} \tag{4.2}$$

At this point the current will have reached a stable value, I_S, but the charging process continues. The time required to charge the output to the mid-swing voltage level V_M is given by

$$T_M = \left(V_M - V_L - \frac{1}{2}\frac{I_S T_r}{C_O}\right)\frac{C_O}{I_S} = \frac{1}{2}\frac{C_O}{I_S}\Delta V - \frac{1}{2}T_r \tag{4.3}$$

so the propagation delay T_{DQ} in the stable region is given by

$$T_{DQ(Stable)} = T_i + \frac{1}{2}T_r + T_M = T_i + \frac{1}{2}\frac{C_O}{I_S}\Delta V \tag{4.4}$$

Note that the delay is taken as the time between the input reaching a 50% level to the output reaching its 50% level.

4.3.2 T_{DC} Limit of the Stable Region

The limit of the stable region is $T_{DC(Stable)}$, beyond which the latch delay does not get higher than its stable value $T_{DQ(Stable)}$. This is only possible if the outputs are already charged to V_M, just before the current flow starts to switch from the sample to the hold pair. Current transition starts at a time $(T_r/2 - T_i)$ earlier than the clock edge:

$$T_{DC(Stable)} = T_{DQ(Stable)} + \frac{1}{2}T_r - T_i = \frac{1}{2}\frac{C_O}{I_S}\Delta V + \frac{1}{2}T_r \qquad (4.5)$$

Although the total bias current will split between I_{sample} and I_{hold}, all of the current will remain flowing in the same branch $(I_1 \text{ or } I_2)$. But there will be some change in the output rise time due to the decrease in the output capacitance, as the hold pair is now in active region (see Section 4.2). It is clear from Equation (4.5) that the setup time increases with T_r.

4.3.3 Delay in the Metastable Region

If the data changes after $T_{DC(Stable)}$, the output will not be charged to V_M before the current switching starts. I_{sample} will decrease gradually and I_{hold} will increase at the same time. The hold pair will try to regenerate the data, opposing the sampling pair. During the first half $(T_r/2)$ of the current transition, the current flowing in the sampling section is larger than that in the hold pair. The change in the output voltage during $T_r/2$ will be related by

$$Output\ Charging = Charging_{(Sample)} - Discharging_{(Hold)} \qquad (4.6)$$

Depending upon the level to which the output was previously charged, it is possible that the output will become charged to V_M during the time $T_r/2$. The hold pair could then regenerate the output correctly but with longer delay and rise times. This is known as the metastable region, during which the latch delay T_{DQ} increases exponentially with decreasing T_{DC}.

4.3.4 *Limit of the Metastable/Failure Region*

If the output fails to charge to V_M during the first half of the current transition $T_r/2$, the hold pair will regenerate the output to an incorrect value and latch operation will fail. The metastable region is limited by the value $T_{DC(min)}$ for which the output is charged to V_M just before the current through the hold pair exceeds from that of the sample pair. Using Equation (4.6), the output charging to V_M during the half current transition is;

$$\frac{3}{8}\frac{I_S T_r}{C_O} - \frac{1}{8}\frac{I_S T_r}{C_O} = \frac{1}{4}\frac{I_S T_r}{C_O}$$

and the initial charging during the data transition, from Equation (4.2), is

$$V_0 = V_L + \frac{1}{2}\frac{I_S T_r}{C_O}$$

so the time used for charging to V_M with stable current I_S, is

$$T_M = \left(V_M - V_0 - \frac{1}{4}\frac{I_S T_r}{C_O}\right)\frac{C_O}{I_S} = \frac{1}{2}\frac{C_O}{I_S}\Delta V - \frac{3}{4}T_r \qquad (4.7)$$

and the total time taken for output charging to V_M, is given by

$$T_{DQ(max)} = T_i + \frac{1}{2}T_r + \frac{1}{2}\frac{C_O}{I_S}\Delta V - \frac{3}{4}T_r + \frac{1}{2}T_r = T_i + \frac{1}{2}\frac{C_O}{I_S}\Delta V + \frac{1}{4}T_r \qquad (4.8)$$

Since the current switching takes place T_i delay after the clock edge (see Figure 4.3), the corresponding $T_{DC(min)}$ can be obtained as follows

$$T_{DC(min)} = T_{DQ(max)} - T_i = \frac{1}{2}\frac{C_O}{I_S}\Delta V + \frac{1}{4(2)}T_r \qquad (4.9)$$

Any change in the data after this time will not be captured by the latch. And the hold pair will retain the captured data at the output. Equation (4.5) and Equation (4.9) define the boundaries of the metastable region, which is clearly dependent on T_r.

The analysis presented here is based on the idealized assumption that the biasing current I_S remains constant while the data and clock signals are switching. However, in reality, as it could easily be observed in simulation, the current I_S varies during switching. The first effect of this is that during the current commutation between the sampling and holding branches the instantaneous conductance of both branches can be low, causing the total current to drop. This can be prevented by careful selection of DC biasing levels for the clock and data signals. The second effect is caused by the current sourcing transistor's C_{DS} parasitic capacitance. This effect is difficult to avoid, especially in low-voltage designs wherein the V_{DS} voltage drop is minimized by increasing the aspect ratio W/L of the current biasing transistor.

The boundaries of the metastable region are determined by the current switching time. Hence the rise/fall times of the clock signal can have a strong effect on the performance of a latch/flip-flop. Figure 4.4 shows the simulated latch delay in the metastable region for different clock rise and fall times. It can be seen that, in the stable region, the delay does not depend upon the data to clock time, as predicted by Equation (4.4). As the clock transition time increases, the setup time also increases. The latch delay before latch

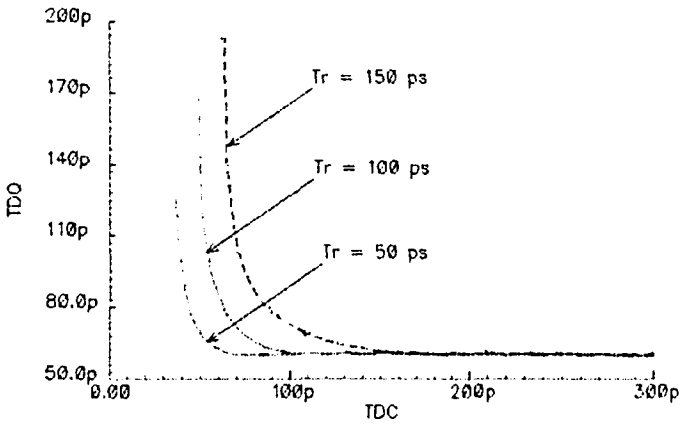


Figure 4.4: CML latch delay with different rise/fall times

failure $T_{DQ(max)}$ is found to be much higher in simulation than what was estimated by Equation (4.8). This is due to the drop in total bias current during the clock and data switching, as explained earlier.

4.4 CML Latch Performance Limiting Factors

Current mode logic is the most popular logic style for high speed and low power integrated circuit design. CML latches are employed for data sampling and storage elements as well as for sequential logic and divider applications. Analysis of signal slew rate effects on the timing parameters of CML latch was presented in the last section. There are other factors which affect the performance of the CML latch, resulting in lower operating frequency. The following sections will briefly describe those factors.

4.4.1 Clock and Data Feedthrough

Due to device overlap capacitance C_{GD}, the signal applied to the gate of an input transistor results in unwanted charge being injected into the circuit. This is commonly known as clock feedthrough. Since CML is a low voltage swing logic, this is a more seri-

ous concern than in the case of other logic styles. For the CML latch, clock and data feedthrough during the hold mode may corrupt the stored data and cause latch failure. Figure 4.5 shows the equivalent Miller's capacitance introduced by C_{GD}.

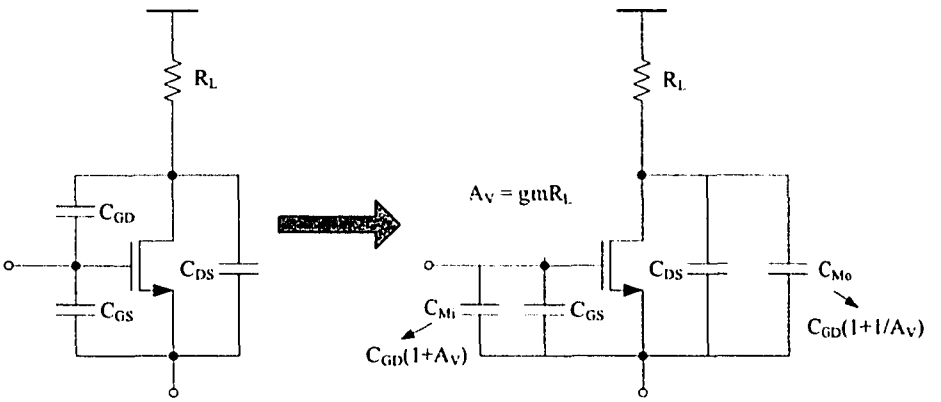


Figure 4.5: Miller's Equivalent Capacitance

4.4.2 Device Threshold Variations

Due to process variations affecting, for example, gate oxide thickness and gate length, there might be a threshold voltage V_{TH} mismatch between the differential pair transistors of a CML gate, and the output waveform could become unbalanced. An offset bias voltage ΔV_B at the output exists, given by

$$\Delta V_B = G(0)\Delta V_{TH} \tag{4.10}$$

where ΔV_{TH} is the variation in the threshold voltage of the device and $G(0) = g_m R_L$ is the CML gate's DC gain. From the above equation it can be seen that ΔV_B is proportional to $G(0)$, so a small dc gain is preferable.

4.5 Modified CML Latches

Several modifications in the CML latch structure have been proposed in the recent literature. Some worthy of note structures are briefly described in the following section. A comparison of conventional and modified CML latches is presented in [26].

4.5.1 Dual Current Source CML Latch

Because of the parasitic capacitance of the transistors of sample circuit, the tail current must be sufficiently high to achieve a wider range of linearity and a larger transconductance. On the other hand the hold circuit does not need a large bias current. These conflicting requirements can not be reconciled in conventional CML latch design because they have only a single constant current source. In reference [29], the regenerative latch is modified so that the sample circuit and the hold circuit use two distinct tail currents, as shown in Figure 4.6. The use of this technique results in significant speed improvement, but at a cost in increased static power consumption and circuit complexity.

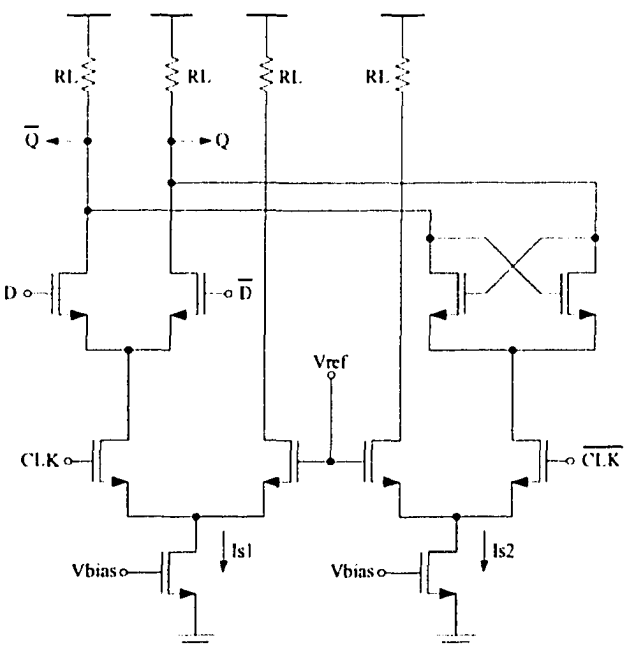


Figure 4.6: CML latch with dual current source [29]

4.5.2 Feedback CML Latch

As discussed in the last section, the maximum operating frequency of CML circuits is reduced by threshold voltage variations. A 'feedback' CML scheme which has improved immunity to V_{TH} variations has been proposed in [30]. Feedback transistors are connected between the input and the output as shown in Figure 4.7. In the always-ON configuration they work as feedback resistances. The effect of these is a wider operation bandwidth, or at same frequency, improved rejection of threshold voltage variation. However this technique is not particularly suited for use in CML latches. Since feedback transistors are connected between data inputs and outputs of the latch, a change in the input data will directly affect the output state when the latch is in its hold mode. Since CML output voltage swing is relatively small, these fluctuations in the output may result in a false state and metastability in the master slave configuration.

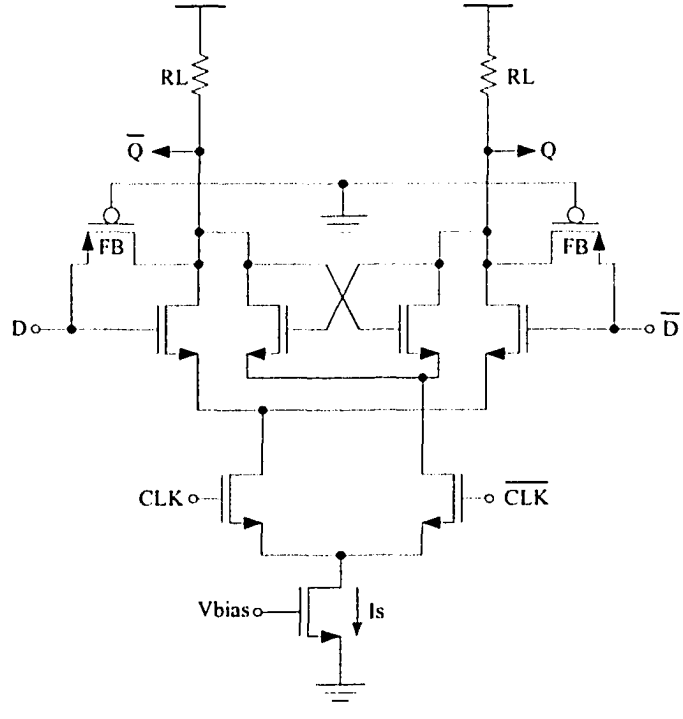


Figure 4.7: CML latch with feedback transistors [30]

4.6 Proposed Clock Feedback CML Latch

The CML latch is one of the fastest contemporary clocked storage elements. In addition to small delays, a CSE should also exhibit low data feedthrough. But CML suffers from input-output coupling and clock feedthrough due to device overlap capacitances which also introduce Miller capacitance effects through the gain of the CML gate (see Section 4.4.1). To do away with this problem, a cross-coupled pair of capacitors between the input and the output terminals of a CML gate can be used [29], as shown in Figure 4.8(a). However, it is realized that PMOS devices - with their gates tied to the ground (Figure 4.8(b)) - can provide enough capacitance necessary to compensate the Miller capacitance, and at the same time, because of their resistive behavior, establish a positive feedback path between the input and output terminals.

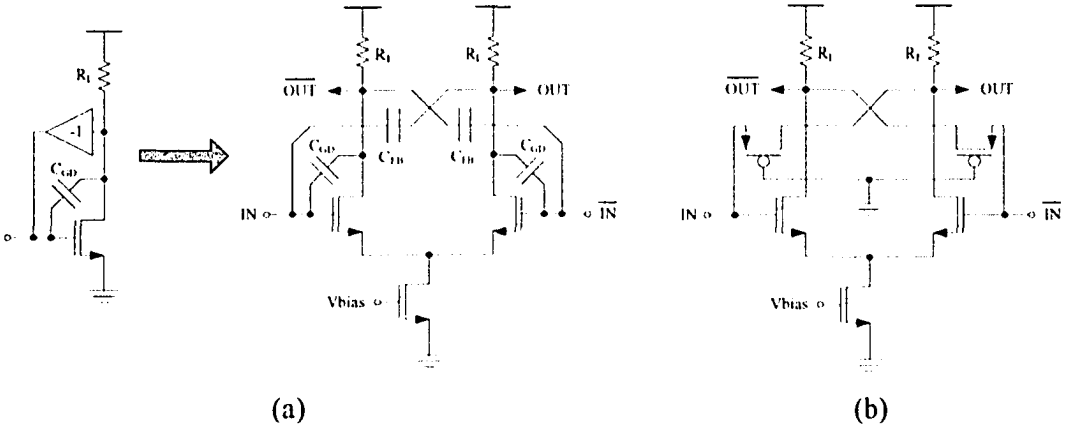


Figure 4.8:(a) Cross-Capacitive-Coupling, (b) Cross-Coupled PMOS

Positive feedback in CML inverters and buffers is beneficial because it leads to reduced propagation delay. But such feedback will degrade a CML latch's performance because a high degree of isolation is required during the device's hold mode. It should therefore be more effective to use cross-coupled PMOS transistors across the clock tran-

sistor pair only (see Figure 4.9) – this will result in faster current switching between the sample and the hold pairs. Rapid current transitions have effects similar to reduced rise and fall times, and so will directly affect latch setup and hold times, as described in Section 4.3.

A modified 'clock feedback' CML latch structure, is herein proposed. Cross-coupled PMOS devices are connected between the clock terminals of the latch, as shown in Figure 4.9.

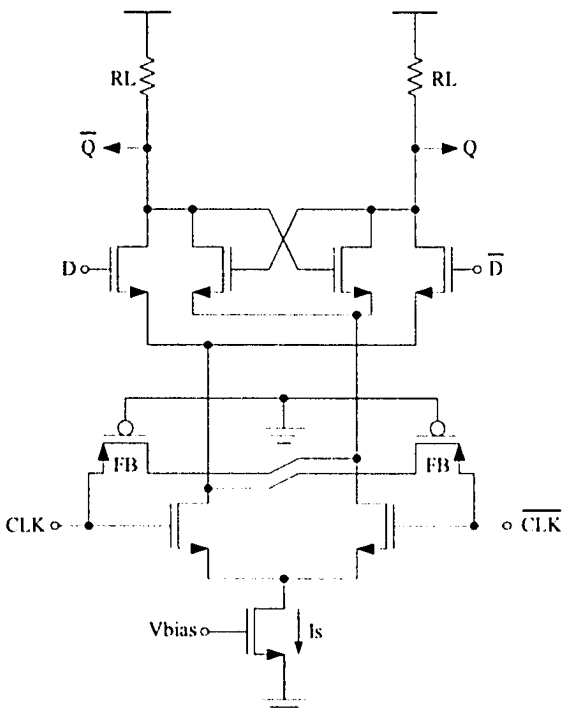


Figure 4.9: Clock Feedback CML Latch

In the proposed configuration, the feedback transistor gates are tied to ground and the voltage levels between the clock transistor gates and drains are sufficient to keep the feedback transistors in saturation at all times during latch operation. Since the operating regions of the feedback PMOS devices do not change, they exhibit a fairly constant capacitance which neutralizes the effect of Miller capacitance.

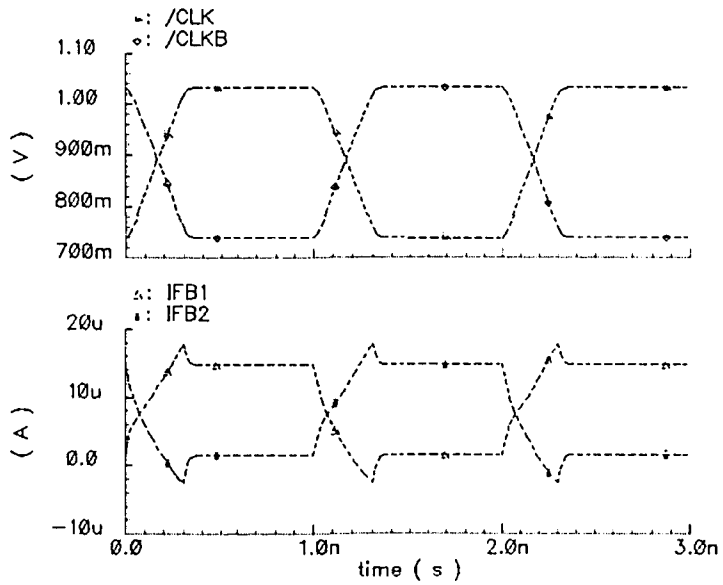


Figure 4.10: Current Peaking through Feedback Transistors

A small amount of current flows through the feedback transistors (Figure 4.10), current that will be subtracted from that flowing through the 'on' branch because of the constant tail current source. As a result, output voltage swing is reduced. The effects of this constant current flow on output voltage swing reduction may be ignored, since the current is much smaller than the total biasing current. However because of current peaking during clock transitions, a direct effect on the output can be seen in the form of voltage level fluctuations. These fluctuations at the output may be suppressed to a large extent through feedback transistor sizing. It should be noted that the output which is held at the high voltage level remains very stable.

Due to reduction in the current flowing through the 'on' branch and the additional capacitance of the feedback network, the delay of clock feedback latch is higher than the conventional one. However, with a small power penalty same propagation delay can be achieved, with smaller setup and hold times, as shown in Figure 4.11.

T_{CQ} and T_{DQ} delays versus T_{DC} for conventional and clock feedback latches in master-slave configuration are shown in Figure 4.11. Latch delays in the stable region $T_{CQ(Stable)}$ are deliberately made equal by increasing the biasing current of the clock feedback latch. It can be seen that the clock feedback latch has smaller-than-conventional setup time and $T_{DQ(min)}$.

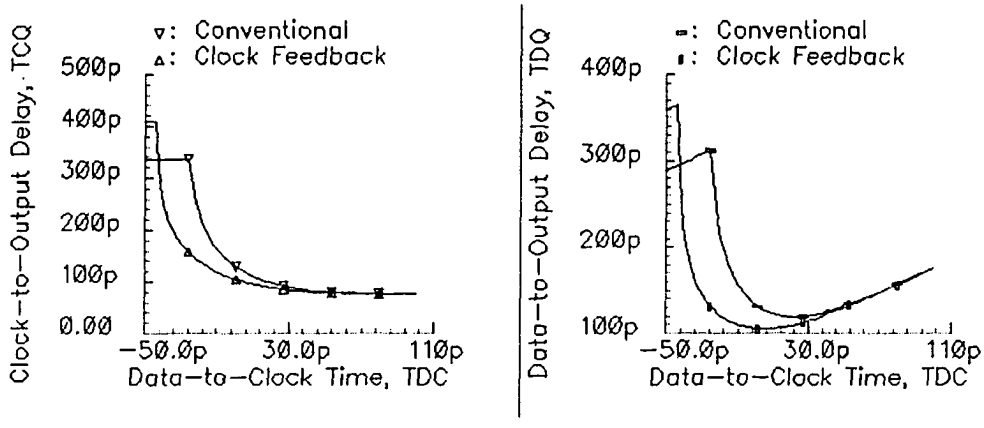


Figure 4.11: T_{CQ} and T_{DQ} vs. T_{DC}

So that the current flowing through the feedback transistors will be limited, they should have small transconductances. And furthermore, the capacitance required for clock feedthrough cancellation is also very small. Therefore, the devices must be sized very carefully – a minimal transistor width is sufficient for required capacitance, but the length of the feedback transistors should be 2-3 times the minimum feature size.

Because of the PMOS device resistance and other parasitic and Miller capacitances, an RC time constant exists at the clock terminals. If the rise and fall times of the clock signal are shorter than this time constant, then the feedback network will not act properly. Simulation results for two cases with different clock transition times are plotted in Figure 4.12.

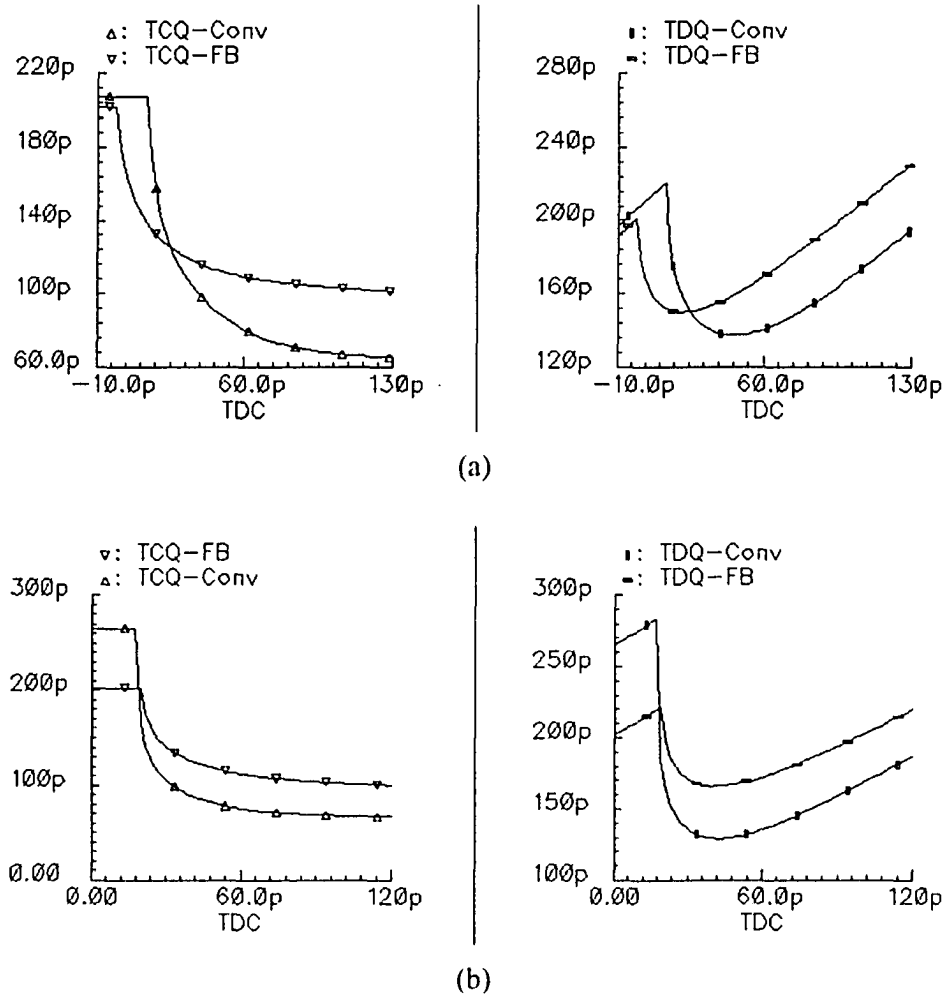


Figure 4.12: MS-Latch delays at same power consumption (a) 30% rise time, (b) 5% rise time

More simulation results will be presented in Chapter 5.

A study of the maximum toggle frequency of a divider will cover most of the important issues, and will be described in Section 4.7.2. In the next sections, the design and implementation of high speed dual modulus frequency prescalers will be presented.

4.7 Frequency Prescalers

The frequency divider is a key component in PLL frequency synthesizers. There are many types of circuits that can perform frequency division, and some care must be exercised in selecting the right one for a particular design – there is no 'universal' divider. Some of the basic requirements are [6]:

1. high operating frequency,

2. wide tuning range or bandwidth,

3. high division ratio,

4. variable and controllable, manually or electronically, division ratio,

5. no RF signal in the absence of input signal,

6. low cost

and so forth

Digital frequency dividers are the most popular divider structures in use today. High frequencies are possible: a regenerative CML divider (0.18μm CMOS) with inductive loads has been reported to operate at 40 GHz [40]. Digital frequency dividers also offer the flexibility of programmability, high division ratios and simple digital control [6].

The fundamental element of a digital frequency divider is a flip-flop, or a master-slave arrangement of two level-sensitive latches. The basic principle behind their operation is that of the finite state machine. Their basic operation is conceptually simple – they just count clock pulses. The terms *divider* and *prescaler* will be used interchangeably in this text and their division ratio being fixed or variable will be clear from the context.

4.7.1 Synchronous and Asynchronous Dividers

Digital frequency dividers can be classified into two types, synchronous and asynchronous [6]. In the former case, series-connected ($\rightarrow Q \rightarrow D \rightarrow Q \rightarrow$) flip-flops are driven from a common clock signal. With each active clock transition, the output of one stage propagates through to the output of the next. Asynchronous dividers also employ a series connection, except that a 'ripple' clocking method is used. Synchronous dividers are inherently faster since the state changes occur almost simultaneously on the same clock edge but the division ratio is relatively low. As all the CSEs are driven from common signal, they exhibit a fairly large clock load. Asynchronous dividers provide higher division ratios but are slower because of the propagation delay from one stage to the next.

4.7.2 Maximum Operating Frequency as a Divider

A master-slave latch or flip-flop can be configured as a divide by 2 circuit as shown in Figure 4.13. This circuit operates well so long as the output changes (at Q) are rapid enough to satisfy the FF setup time (at D) requirement. Hence the minimum clock period is the sum of clock-to-output delay T_{CQ} and the setup time T_S.

$$T_{CLK} = T_{CQ} + T_{DC} \pm \Delta t$$

$$\therefore T_{CLK(min)} = (T_{CQ} + T_S)_{min} + \Delta t = T_{DQ(min)} + \Delta t \qquad (4.11)$$

where Δt is the clock edge deviation as defined in Section 3.2.1. Another condition that must be satisfied is for the delay T_{CQ} to be larger than the hold time T_H of the latch, otherwise it will create glitches or unstable output. However in known clocked storage elements this is not a serious concern because normally T_H is much smaller than T_{CQ}.

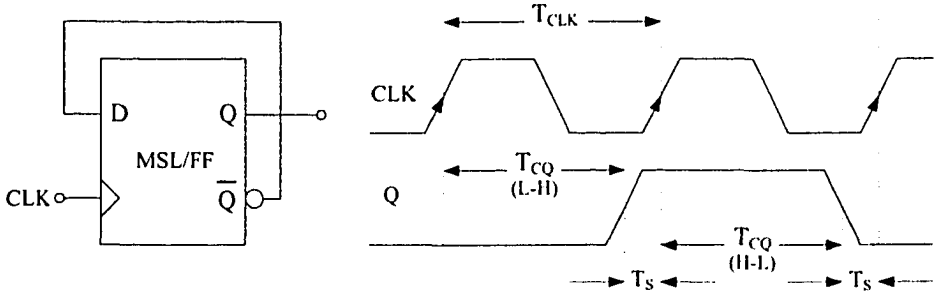


Figure 4.13: (a) Clock Divider (div. by 2), (b) Minimum Clock Period

It is interesting to note that $T_{CLK(min)}$ also corresponds to the optimum setup time, as described in Section 3.2.4.

4.7.3 D-Latch as a Divider

Instead of a flip-flop or master-slave latch, a single-stage latch can also be used as a stage [35] in a high speed and low power divider. Unfortunately this approach leads to additional constraints being placed on the clock period, such as an upper bound on the maximum clock pulse width. The method is suitable only for division in a narrow frequency range. The mechanism of operation is shown in Figure 4.14 – during the isolation phase the latch is holding a certain state – either high or low, and the inverted output is fed to the data input. When the latch enters the transparent phase the output changes after a delay T_{CQ}. The change in the output must be a setup time T_S earlier than the isolation edge of the clock. Equation (4.12) defines the condition for the minimum clock pulse width.

$$T_W \geq T_{CQ} + T_S + \Delta t \tag{4.12}$$

Furthermore, if the clock pulse width is wide enough, then during the transparent phase an output change will propagates through the latch again, and cause a race hazard. This places a condition on the maximum clock pulse width, expresses as:

$$T_W < T_{CQ} + T_{DQ} + T_S - \Delta t \tag{4.13}$$

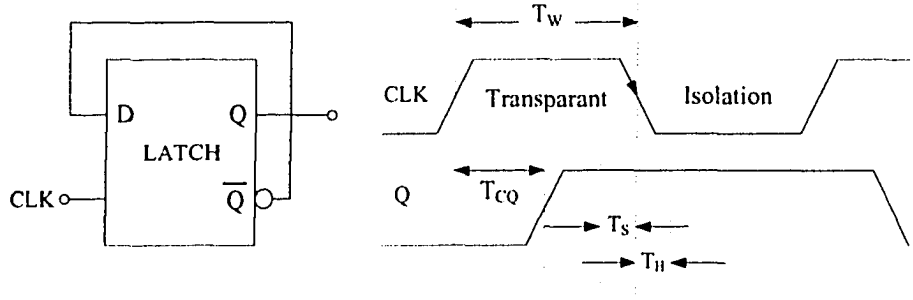


Figure 4.14: (a) Latch as a divider, (b) Clock pulse width

4.8 Dual Modulus Divider Techniques

Dual modulus frequency dividers are used in fractional-division phase-locked loop synthesizers. These dividers are used to greatly extend the frequency resolution of programmable prescalers, effectively using a rational number instead of an integer for the division ratio [45]. The usual approach when a PLL synthesizer is to be built is the 'dual modulus' method, where two division ratios differing by one *(N-1 and N)* are desirable. The general structure of a programmable prescaler is shown in Figure 4.15 [6] – it uses a

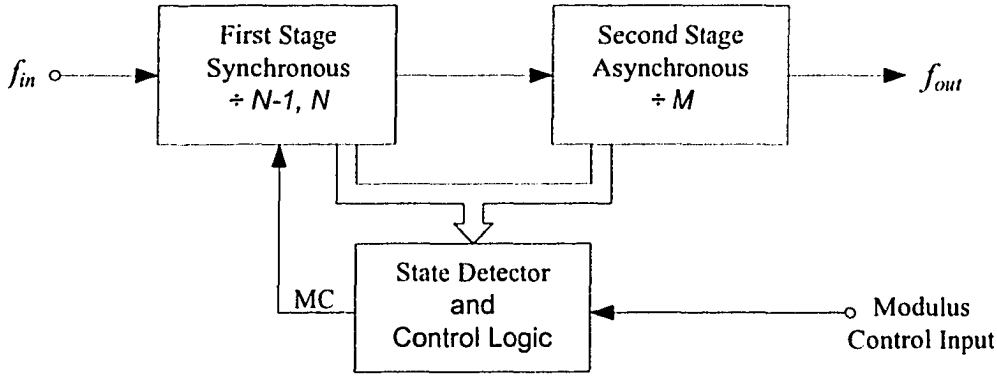


Figure 4.15:General structure for Dual-Modulus Prescaler

dual-modulus prescaler as a first stage divider followed by a modulo-*M* asynchronous counter (the whole thing would be placed in a PLL's feedback loop). Control logic detects the states of both dividers, and depending on the logic state of modulus control input, it generates a modulus switch signal *MC*. When *MC=0*, the first stage divides by *(N-1)* and when *MC=1* it divides by *N*. A range of effective divisors is produced by altering the duty cycle of *MC*. (A certain amount of phase noise cannot be avoided with the dual-modulus method.) The *MC* signal is generated only when the modulus control input is logic high and both dividers have reached a particular state. Since the second stage always cycles through all of its states and each state is unique, the control logic can use any state to remove one clock cycle by generating the *MC* signal. During normal operation when the modulus control input is in a logic low state the overall division ratio is $N \cdot M$, and when the modulus control input is logic high it divides by $N \cdot M - 1$.

$$f_{in} = \begin{cases} N \cdot M \cdot f_{out} & MCI = 0 \\ (N \cdot M - 1) \cdot f_{out} & MCI = 1 \end{cases} \tag{4.14}$$

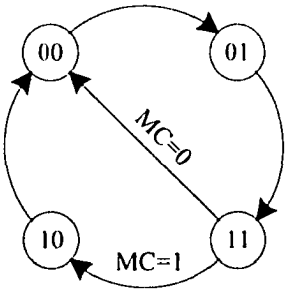
Various dual modulus prescalers can be found in recent literature [42-46]. A 17 GHz dual modulus prescaler in 120nm CMOS is reported in [45]. The following sections describe the design of both stages of a dual modulus frequency divider.

4.9 First Stage Synchronous Divider

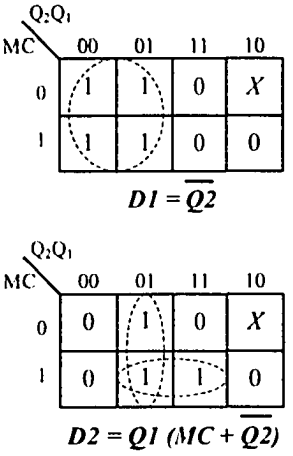
The VCO and the frequency divider operate at the maximum frequency seen in a PLL frequency synthesizer application. The divider therefore to a large extent determines the speed of the system and is a large contributor towards power consumption. (A synchronous divider is the best choice for high frequency dividers). The first stage divider

must present a small capacitive load to the VCO in order to achieve high frequency and lower power consumption. So the number of flip-flop stages should be a minimum. For this reason a 3/4 dual modulus structure was chosen – it has only two flip-flop stages, and one of the divisors, 4, utilizes the 2-stage design to its maximum extent. Figure 4.16 describes the design steps and procedure for the synchronous control logic. The control logic can be expressed as follows,

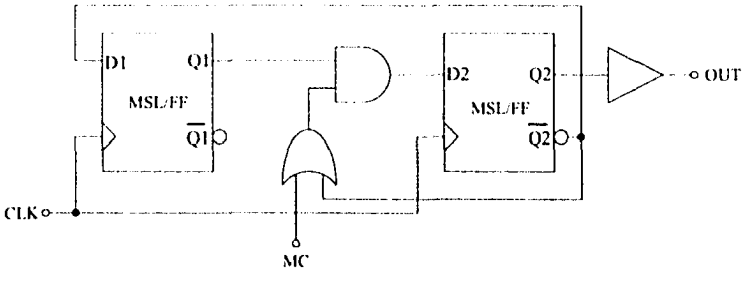
$$D1 = \overline{Q2}$$
$$D2 = Q1(MC + \overline{Q2}) \qquad (4.15)$$



Present State			Next State	
MC	*Q2*	*Q1*	*D2*	*D1*
0	0	0	0	1
0	0	1	1	1
0	1	0	*X*	*X*
0	1	1	0	0
1	0	0	0	1
1	0	1	1	1
1	1	0	0	0
1	1	1	1	0



(a)



(b)

Figure 4.16:3/4 Dual Modulus: (a) Logic Design, (b) Divider Schematic

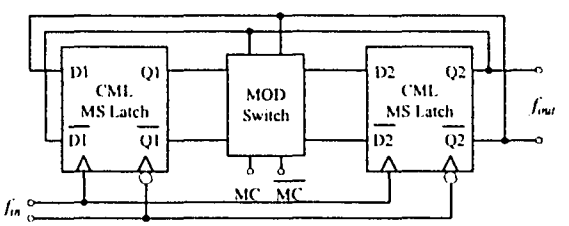
A CML divider employs two level-sensitive CML latches in master-slave configuration. In the following sections analysis and design of two different implementations of a 3/4 dual modulus divider are presented.

4.9.1 Modulus Switch Circuit in CML

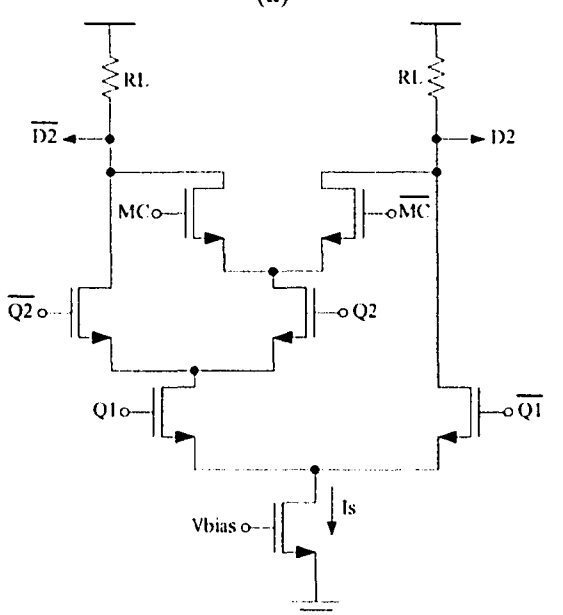
A CML implementation of the first stage of a synchronous dual modulus divider is shown in Figure 4.17. It consists of two CML master-slave latches and the modulus control circuit. The control logic delay time, T_{MC}, must satisfy the following relation in order to work properly at the frequency of interest.

$$T_{MC} \leq T_{CLK} - T_{CQ} - T_S - \Delta t = T_{CLK} - T_{DQ(min)} - \Delta t \qquad (4.16)$$

Due to the asymmetrical circuit structure, the T_{MC} delay varies depending on the logic states and modulus control input. This can be prevented by transistor width optimization or by cascode transistors in the respective data paths.



(a)



(b)

Figure 4.17: 3/4 Dual Modulus Switch: (a) Block Diagram, (b) CML Implementation

4.9.2 CML Embedded Logic Latch

The current mode logic style is advantageous in that additional control logic may be 'embedded' within the latch, incurring only a very small performance penalty in doing so [45]. One gate delay is eliminated. The modulus control switch can be merged within the latch, as shown in Figure 4.18. Due to the multi-stacked structure, transistors biasing is critical, especially in the case of low voltage circuits. This structure shown suffers from unbalanced output voltage swing which can be successfully re-symmetrized by the slave latch.

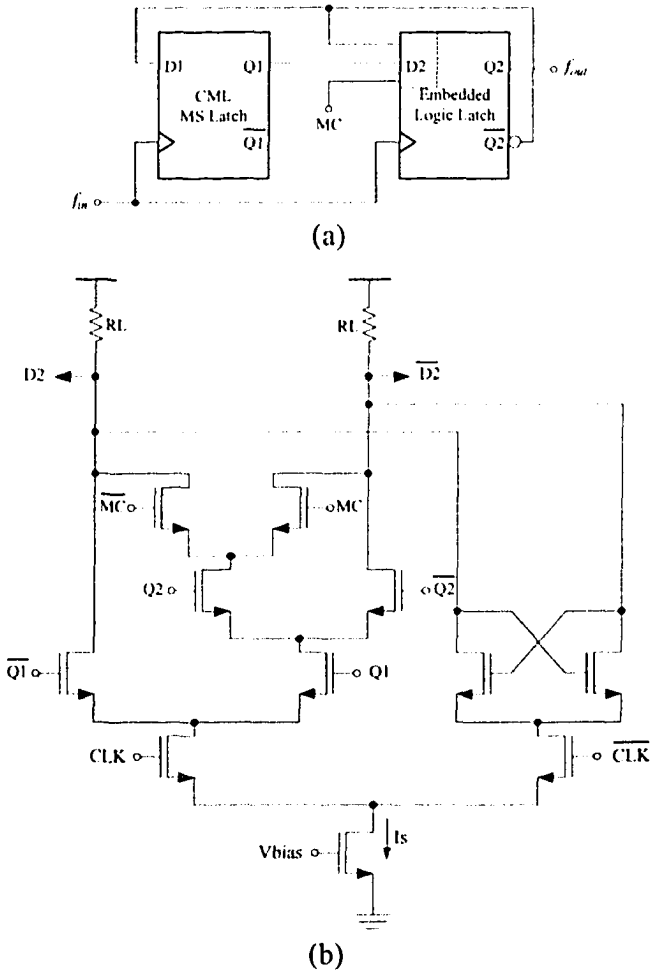


Figure 4.18: 3/4 Dual Modulus circuit with Embedded Logic Latch (a) Block Diagram, (b) Schematic of the Master Latch (Slave is conventional)

Although the individual latch delay is higher with this approach, the omission of the additional control logic gate results in higher operating frequency. Simulation results are presented in Chapter 5.

4.10 Second Stage Asynchronous Divider

After the first stage divider, the VCO frequency has been divided down to a frequency range where asynchronous dividers can be operated successfully. Asynchronous dividers are simple in operation and provide higher division ratios of the form 2^n, where n is the number of flip-flop stages. A conventional asynchronous divider can be realized using current mode logic, by cascading CML latches in a master-slave configuration, as shown in Figure 4.19. However, a new technique is proposed in the next section to reduce the area and power consumption of the CML divider.

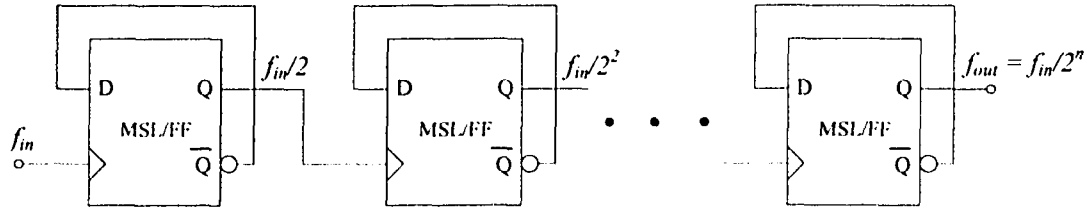


Figure 4.19: Asynchronous Frequency Divider

4.10.1 Master-Slave Combined CML Latch

Conventionally for a divider application two identical CML latches are used in a master-slave configuration. It is possible to simplify the usual CML latch clocking structure by employing a single clock transistor pair to switch the current between the sample and hold pair of the master and slave latches [34]. This new configuration uses a single bias current source for both latches.

As described in Section 4.5.1, different bias currents are used for the hold and sample differential pairs. In a conventional CML latch having a single current source this is not possible, so a dual current source CML latch was suggested [29]. In the proposed master-slave combined latch technique [34], the current difference is accomplished by using smaller transistor sizes for the hold pairs of both latches. This can be used to make most of the current flow through the sample pairs and so eliminates the requirement for two independent current sources. Due to the lower current through hold pair the width of the current source does not need to be doubled – a 1.5 times transistor width for the current source is sufficient for successful operation at the same operating frequency. This reduces the overall static power dissipation.

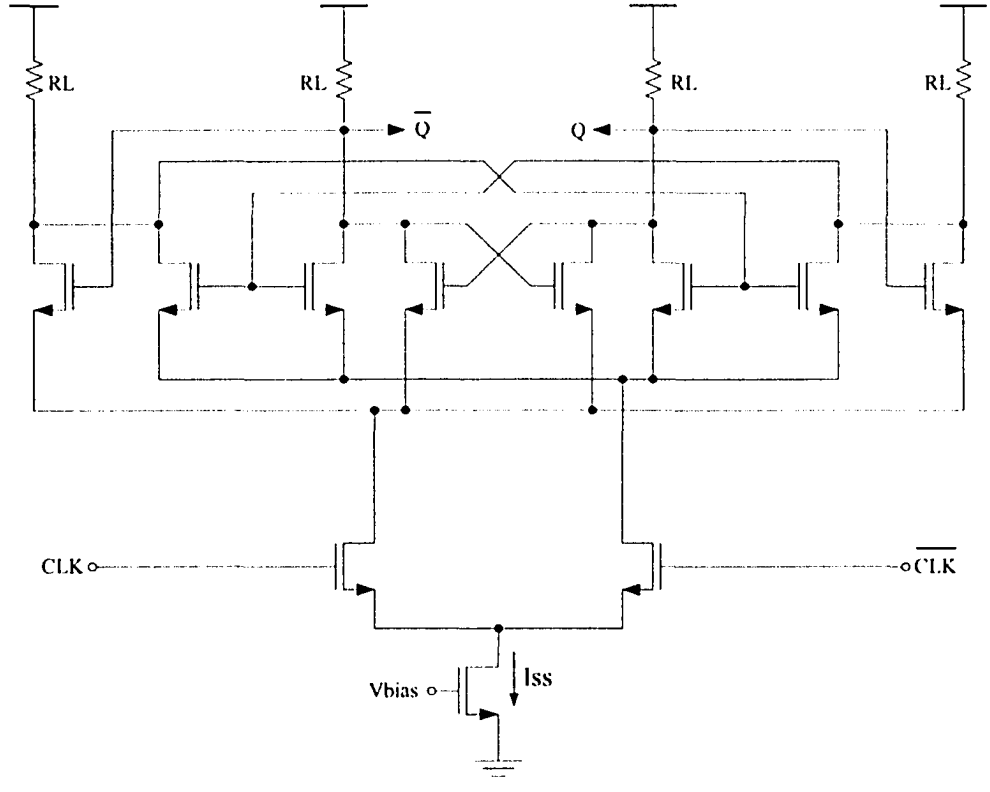


Figure 4.20: Asynchronous CML divider with Master-Slave Combined Latches

This technique is also area efficient, because the current source is the dominant area-occupying component (if active loads are used). Using single current source and clock transistors can save up to 20% of the layout area. Clock feedback transistors can minimize the setup time as can be seen in Figure 4.11. This reduces the minimum required clock period and allows signal division at higher input frequencies. Figure 4.20 shows a schematic of a divide by 2 prescaler with combined master and slave latches.

4.11 Chapter Summary

This chapter deals with the design and implementation of current mode logic latches, and their application in frequency prescalers. The operation of a conventional CML latch is analyzed. A detailed analysis of metastability in CML latches due to the rise and fall time of the clock is presented. Other performance limiting factors were also mentioned. After briefly describing some modified CML latch structures from the literature, a clock feedback CML latch was proposed. Addition of feedback transistors cross-coupled between the clock terminals improves the performance of the CML latch in terms of smaller setup and hold times.

This chapter also presented the design of a dual modulus frequency divider using CML latches. Two different implementations of a 3/4 dual modulus synchronous divider were presented, one with a separate control logic block for the modulus control and another with an embedded one. An asynchronous CML divider is also proposed, one having combined master and slave latches with a common current source, and a single pair of clock transistors. This technique effectively reduces power consumption and chip area. Simulation results along with design implementation techniques are presented in the next chapter.

CHAPTER 5

Simulation Results and Design Implementation

5.1 Chapter Overview

This chapter describes the simulation results for the circuit arrangements presented in the last chapter (0.18μm CMOS technology). Descriptions of the simulation environment and the test setups are included. Design implementation and issues encountered for the measurement are also discussed.

5.2 Simulation Environment

All simulation results reported in this thesis were obtained using the Cadence Analog Design Environment, with 'SpectreS' 0.18μm CMOS models, under nominal conditions. Table 5.1 briefly describes the simulation conditions and environment. At multi-gigahertz frequencies, signal rise and fall times become a significant fraction of the clock period, and the test waveforms are usually sinusoidal wave. This fact was recognized by setting all of the high frequency input signals' rise and fall times in the simulations to 30% of the minimum clock period.

An ideal voltage input would be able to provide an infinite amount of current, and make the input charging time infinitesimal. But in reality a finite amount of time is required for that process. In order to realize this, resistances are placed in series with simulated inputs, as shown in Figure 5.1.

TABLE 5.1: Simulation Environment

Permeates	Value
Simulator	SpectreS
Technology	0.18μm CMOS
Process Corner	Typical
Temperature	27 °C
Supply Voltage	1.2 V

5.3 Comparison of CML Latches

Master-slave latch timing parameters were evaluated using the circuit configuration of Figure 5.1. A similar circumstance was used for the comparison of the CSEs described in Chapter 2. Device sizes and testing conditions are summarized in Table 5.2.

TABLE 5.2: Device sizes used for latch comparison

Testing Conditions		Device Sizes	
Supply Voltage	1.2 V	PMOS Load	1.2/0.18 μm
Biasing Current	100 μA	Input Transistors	1/0.18 μm
Clock Frequency	3.3 GHz	Clock Transistors	2/0.18 μm
Input Rise/Fall Time	100 ps	Current Source	25/0.36 μm
Output Fan-out	2	Feedback Transistors	1/0.45 μm

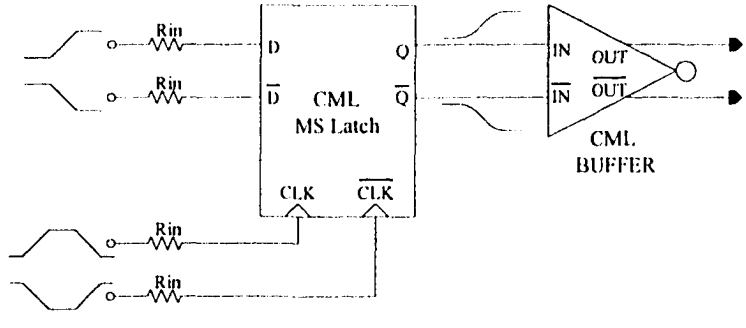


Figure 5.1: Simulation Test bench for CML MSL Timing Parameters

Comparative timing results for master-slave CML latches are presented in the next table:

TABLE 5.3: Latch Timing Parameters in Master-Slave Configuration

Latch Type & Parameters		Conventional CML Latch	Clock Feedback CML Latch
Setup Time [ps]	L-H	23	15
	H-L	31	19
Hold Time [ps]	L-H	35	27
	H-L	34	29
$T_{CQ(Stable)}$ [ps]	L-H	75	78
	H-L	81	79
$T_{DQ(min)}$ [ps]		120	105
Average Current [μA]		174	189

A transient analysis of falling edge master-slave configured conventional and clock feedback latches is shown in Figure 5.2 (circles are drawn to elaborate the respective transitions). It can be seen that the clock feedback latch can capture the data very near to a triggering clock edge, where conventional latch would fail.

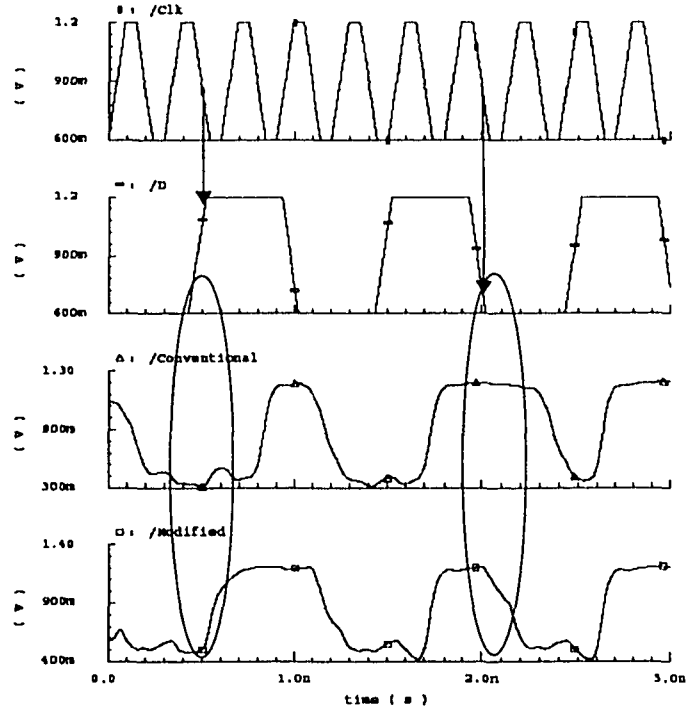


Figure 5.2: Transient Waveforms of Conventional and Clock feedback MSLs

Table 5.4 presents a comparison of divider-configured CML latches:.

TABLE 5.4: Comparison of CML Latches in Divider configuration

Parameters	Conventional	Clock Feedback
Max. Frequency	9.25 GHz	10.5 GHz
Av. Current	312.5 μA	350 μA
Input Sensitivity	5mV@7.8GHz	10mV@9.4GHz

The divider input sensitivity is an important parameter characterizing RF frequency range of prescalers. Input sensitivity of the divider is the minimum amplitude of the clock signal necessary for proper operation as a function of frequency. A set of curves depicting the input sensitivity of the two divider circuits are shown in Figure 5.3(b).

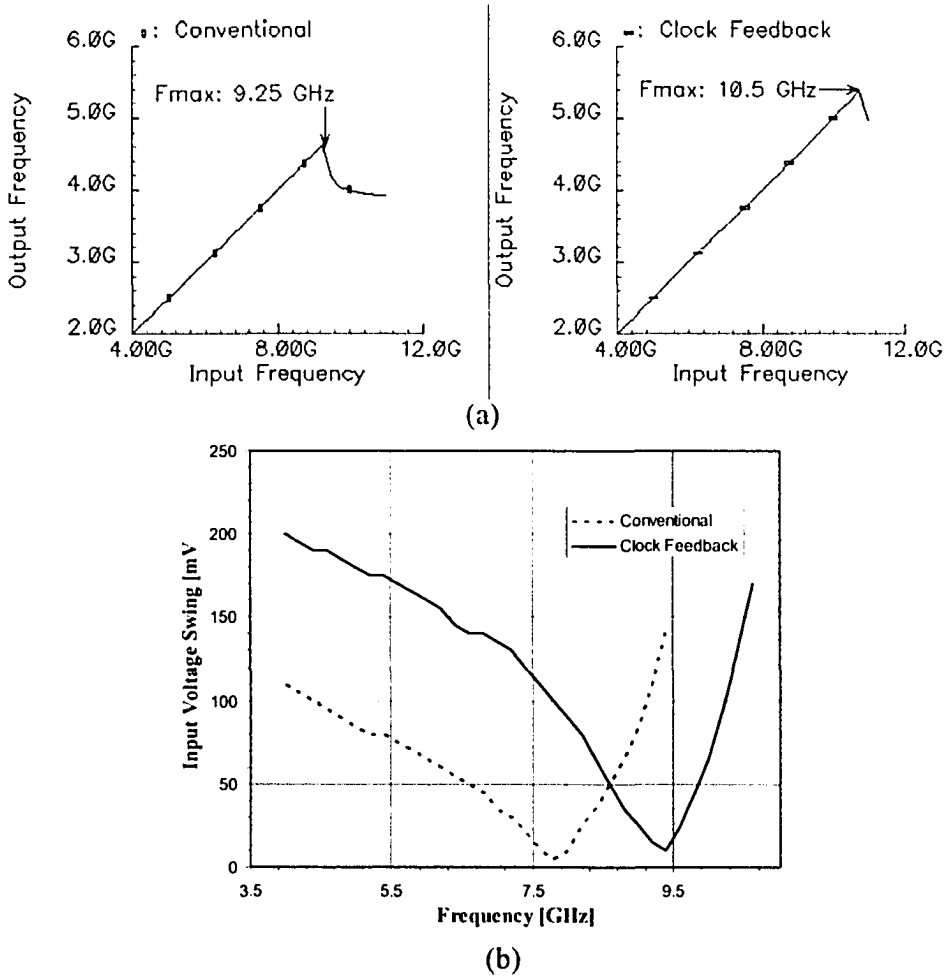


Figure 5.3: Comparison of Conventional and Clock Feedback CML dividers: (a) Maximum Frequency, (b) Input Sensitivity

5.4 Dual-Modulus Dividers

Two approaches to a 3/4 dual-modulus divider were presented in Section 4.9.1 and in Section 4.9.2, and the corresponding simulation results are shown here. The critical waveforms of the two dividers are shown in Figure 5.4 and Figure 5.5. It can be seen that the divide-by-three division output waveform has a distorted duty cycle, as would be expected.

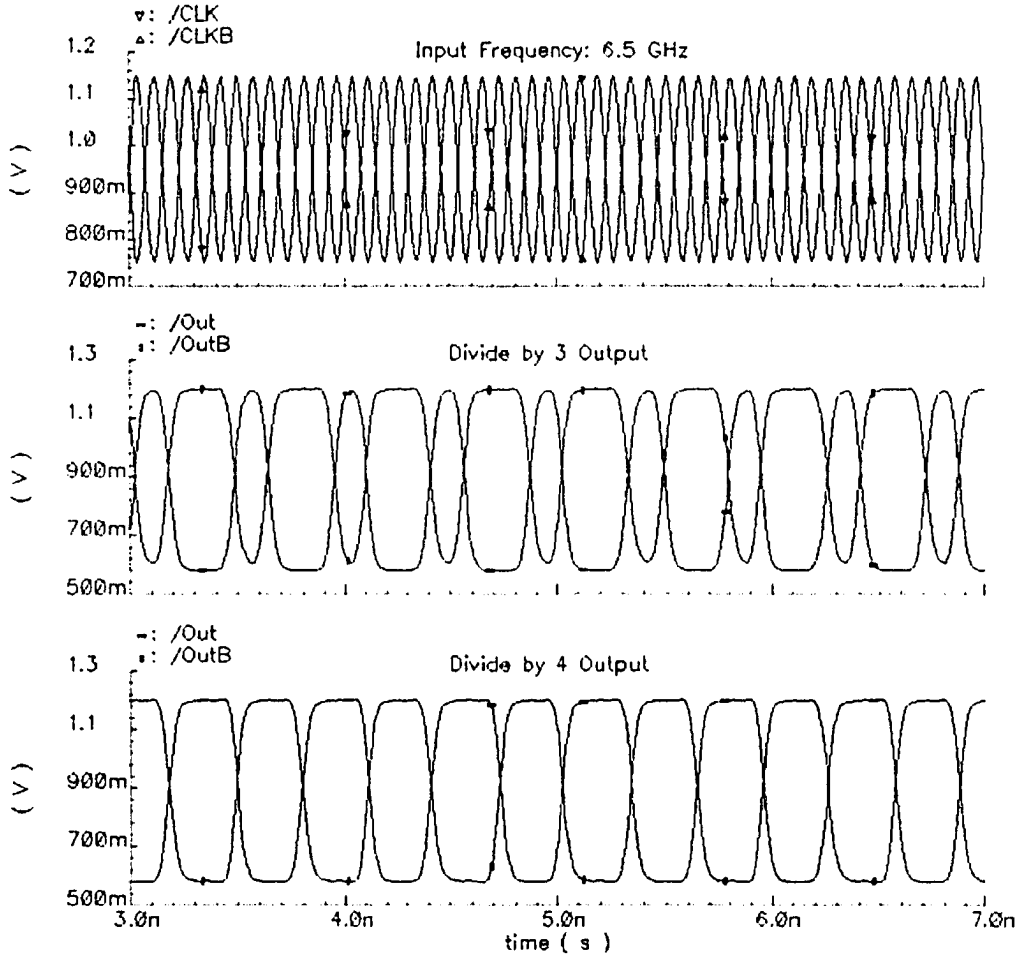


Figure 5.4: Waveforms of a Dual Modulus (3/4) CML Divider (Non-Embedded)

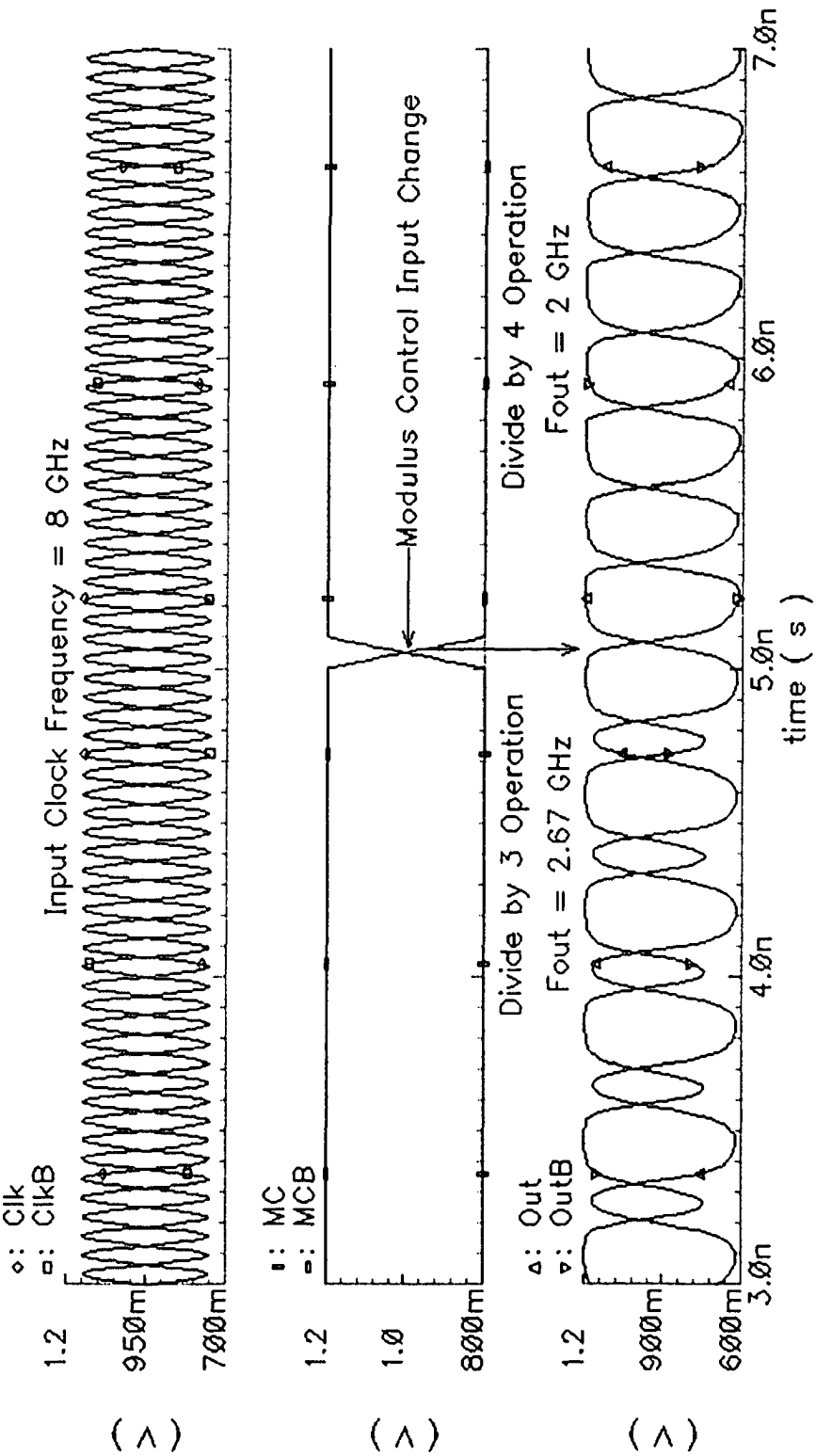
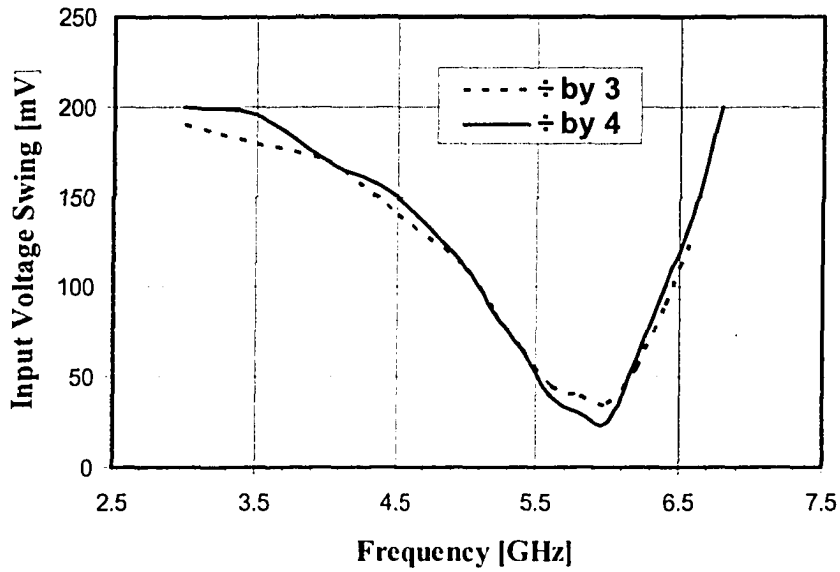
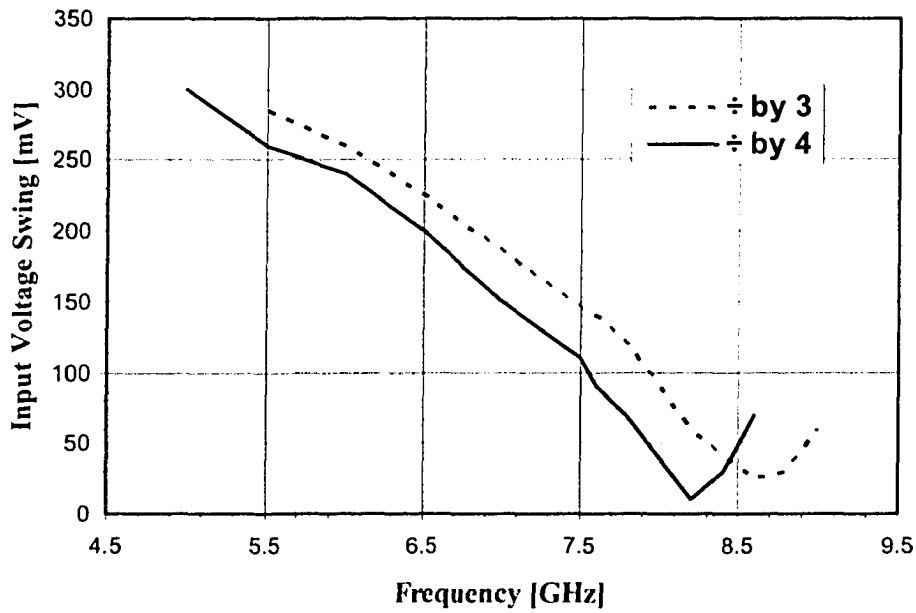


Figure 5.5: Waveforms of a Dual Modulus (3/4) CML Divider (Embedded Control)

Sensitivity curves for both of the dual modulus dividers are shown in Figure 5.6:



(a)



(b)

Figure 5.6: Input Sensitivity Curves for 3/4 Dual Modulus Dividers: (a) Separate Control (b) Embedded Control

Table 5.5 presents a comparative summary of the simulation results:

TABLE 5.5: Simulation Results for 3/4 Dual Modulus Frequency Dividers

Divider Type & Parameters	Separate Control Logic		Embedded Control Logic	
	div. by 3	div. by 4	div. by 3	div. by 4
Max. Frequency	6.6 GHz	6.8 GHz	9 GHz	8.6 GHz
First MSL Current	620 μA	631.2 μA	615.6 μA	605.8 μA
Second MSL Current	620.5 μA	624.4 μA	804.8 μA	793.2 μA
Control Logic Current	146.5 μA	155.7 μA	NA	NA
Input Sensitivity	35mV@6GHz	25mV@6GHz	25mV@8.6GHz	10mV@8.2GHz

5.5 Master-Slave Combined Latches

The idea of master-slave combined latches [34] was described in Section 4.10.1. Simulation results for the comparison of conventional and proposed schemes in asynchronous divider configuration are provided in Table 5.6.

TABLE 5.6: Master-Slave combined CML Latches in Divider

Parameters / Sizes	Conventional MS Latches	Master-Slave Combined Latches
Supply Voltage	1.2 V	1.2 V
Biasing Current (Ref.)	200μA	200μA
Sample Transistor Width	3μm	3μm
Hold Transistor Width	3μm	2μm
Clock Transistor Width	5μm	6μm
Biasing Transistor Width	30μm	45μm
Load Resistor	3KΩ	3KΩ
Maximum Frequency	9.25 GHz	9.4 GHz
Power Dissipation	0.4 mW	0.32 mW
Layout Area*	2 x (12 x 16) μm^2	(12 x 24) μm^2
		** active area (excluding load resistors)*

5.6 Comparison with other Published Results

The performance of presented work is compared with other results published in the recent literature, summarized in Table 5.7.

TABLE 5.7: Frequency dividers compared with other published results

References	CMOS Technology	Maximum Frequency	Power Dissipation	Input Sensitivity	Division Ratio	FOM GHz/mW
	Fixed Ratio Dividers					
[36]	0.18μm	7.6 GHz	6.84 mW	0 dBm	2	1.1
[37]	0.18μm	10 GHz	8.6 mW	NA	2	1.2
[38]	0.18μm	10 GHz	1.3 mW	NA	2	7.7
[39]	120nm	8.25 GHz	0.12 mW	-15 dBm	2	68.8
[40]*	0.18μm	40 GHz	31 mW	-1 dBm	2	1.3
This Work	0.18μm	10.5 GHz	0.42 mW	-27 dBm	2	25
	Dual Modulus Dividers					
[42]	0.35μm	2.4 GHz	4.8 mW	15 dBm	127/128	0.5
[43]	0.25μm	2.3 GHz	12 mW	NA	128/129	0.2
[44]	0.18μm	2.9 GHz	5.5 mW	NA	8/9	0.53
[45]	120nm	17 GHz	71 mW	-27 dBm	4/5	0.24
This Work (Separate)	0.18μm	6.6 GHz	1.5 mW	-16 dBm	3/4	4.4
This Work (Embedded)	0.18μm	8.6 GHz	1.7 mW	-19 dBm	3/4	5.1

* *with Inductive peaking*

A commonly used figure of merit (FOM) for the dividers is the maximum frequency per milliwatts, which is in favour of the presented research work. Few exceptions exist due to different fabrication technologies that is difficult to compare.

5.7 Design Implementation

Two test chips were fabricated to test the ideas involved in CML latches and dual-modulus divider design. Identification numbers, chip areas, chip package types and test-fixture names are listed in Table 5.8. More detail is provided in Appendix-B.

TABLE 5.8: Test chip details

Design Name	Technology	Area	Package	Test Fixture
ICFCUMU1	CMOSP18	1.2mm * 0.7mm	FCP24	PCB-TF2
ICFCUMU2	CMOSP18	1.2mm * 0.8mm	Loose Dies	Analytical Prorbe Station (APS)

5.7.1 Test Chip-1: ICFCUMU1

This first chip was not readily testable for a number of reasons. It was produced to gain experience with the fabrication of CML latches for comparison.

Any attempts at direct testing of the on-chip CSEs would be thwarted by the fact that picosecond time differences would be absorbed by input/output buffers, signal skew phenomena, and other numerous factors. A direct off-chip measurement of the delay between the waveforms could be used to validate the simulation results. However the results of doing this could well be misleading because the on-chip delays of the clocked storage elements are typically much smaller than that of the circuitry connecting the ports to the measuring instruments. The measured quantity would be comparable to the measurement errors incurred by this circuitry. Most often, the measured timing published in the literature, when such measurements have been attempted, only show the highest achieved toggle frequency of the CSEs [50].

Due to a limited number of pins available on the package, on-chip differential converters were employed for data and clock inputs. The signals were overlapping, something which degraded chip performance.

On a more practical note, chip testing was also prevented by some bonding issues.

5.7.2 Test Chip-2: ICFCUMU2

This chip is a combination of separately-testable components compatible with the APS-mounted 8-pin probe assembly. Only frequency dividers were fabricated, as their

measurement is inherently precise. Two 3/4 dual modulus CML dividers were laid out on the chip, one with a separate control logic system and another using an embedded scheme. Experience with the previous chip inspired the use of direct differential input signals instead of creating these using on-chip differential conversion. Chip schematics and lay-outs are provided in Appendix-B.

Figure 5.7 shows the test setup for the measurement of the dual modulus frequency prescaler characteristic parameters.

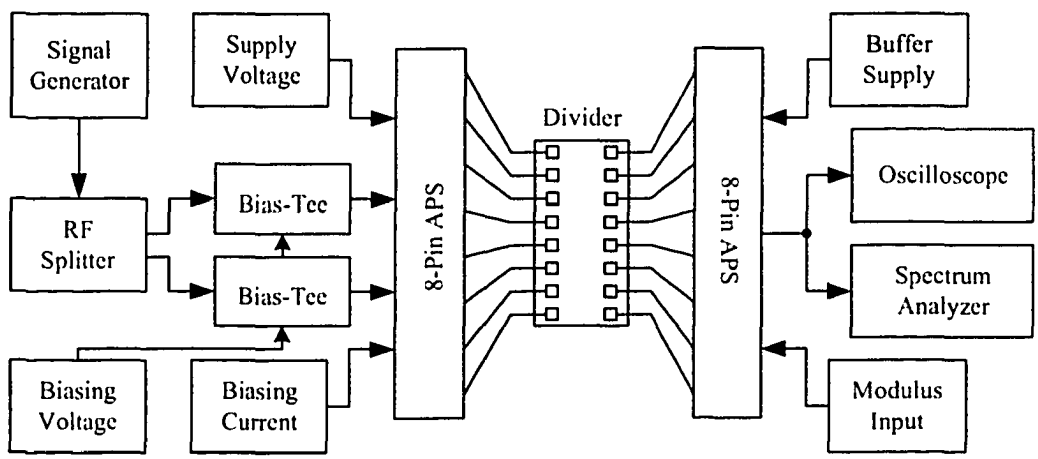


Figure 5.7: Measurement setup for ICFCUMU2

5.8 Design Considerations

This section briefly describes some design considerations and issues encountered during the design implementation.

5.8.1 Device Matching

Device matching in CML gates is important if a symmetrical transfer function is to be had. Matching layout techniques such as interdigitation and common centroid structures were used for the differential pair transistors.

5.8.2 Off-chip Measurement

If a high-frequency signal is to be monitored off-chip, it must be conditioned with an on-chip buffer. On-chip division of high-frequency signals before they are transferred off-chip is also a preferred practice.

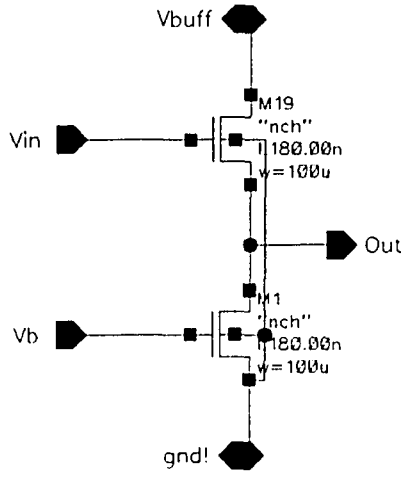


Figure 5.8: Source-follower as an on-chip output buffer

An NMOS source-follower circuit with its own power supply and biasing provisions was used for the buffering function. Chip and package parasitics were considered in the buffer design process: typical values of bond-pad capacitance are in the range of 1.5 pF-3 pF, the bond wire inductance (which depends upon length) was typically 1.5 nH, and FCP24 package pin capacitance is around 1 pF. The inductance of the PCB track depends on the thickness of the copper traces used on the PCB [48].

5.8.3 Resistor Layout

In the first test chip PMOS devices were used as active loads. Although they occupy small layout area, they suffer from non linearity problems like ones which lead to unequal rise and fall times.

The second test chip employed passive loads, in the form of actual resistances, to eliminate the non linearity difficulties of active loads. Poly-silicon resistors were used, as this material has higher sheet resistance than other ones available. However, due to process variations, this approach will result in approximately 30% resistance tolerance, something which can seriously affect CML delay and output voltage swing, and can be a reason for chip malfunction (if the resistance deviations are unbalanced).

Laser trimming can be used for post-fabrication matching of the on-chip resistors. The strategy for doing this is illustrated in Figure 5.9. All the resistors on the chip are initially segmented into small symmetrical pieces. Resistance is lowered by using a metal structure in the top-most layer to by-pass some of the segments. Resistance is adjusted upwards by cutting away appropriate parts of a top metal layer.

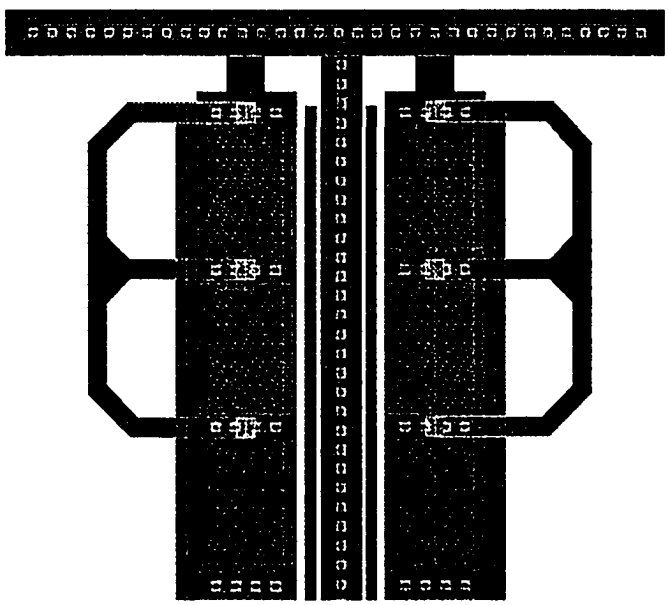


Figure 5.9: Layout technique for Post-Fabrication Resistor Tuning

This technique amounts to a coarse but useable resistance trimming method.

5.9 Chapter Summary

In Chapter-5 was presented the details of the test environment and the resulting circuit simulation findings. Two test chips were built using a standard 0.18μm CMOS process. A number of diagrams and tables summarizing both simulation and physical results were presented.

On comparing the simulation results of presented work with the recently published figures in Table 5.7, one finds that a circuit designed using the new methodology will display competitive bandwidth while consuming significantly less power (the power-delay product is superior).

CHAPTER 6

Conclusions and Future Work

6.1 Thesis Review

The purpose of this chapter is one of recapitulating the content of the thesis, one which in the space allowed brought together a summary of the state of the art of high-speed digital storage device design, introduced some new ideas which extended that state, and provided the setting for still more developmental work.

In Chapter 2 of this document were described the timing parameters common to all clocked storage elements, and also ones peculiar to specific devices, namely the latch, the master-slave latch and the flip-flop. A number of contemporary high-performance CMOS latch and flip-flop architectures presented in the recent literature were described. A comparative analysis of the presented structures was performed using the standard methods of circuit simulation. The results of this effort showed current mode logic (CML) latches to be the fastest of all and the architecture to be a suitable choice for high-speed and low-power CMOS VLSI design. The discussion was therefore restricted to this class of device for the remainder of the thesis.

In Chapter 3, a comprehensive study of CMOS current mode logic design methods was undertaken. A detailed description of circuit operation and an analysis of time delay

provided made it possible to understand the origins of the design challenges and issues faced by the CML designer, ones to be taken up in the remainder of the work. This included the timing constraints that must be considered in practical applications.

The actual design and implementation of a CML latch was studied in Chapter-4 – frequency prescaler design was thought to have covered most of the important issues, and was therefore used as a practical example. The operation of a conventional CML latch was analyzed in this context, an examination which included the effects on latch metastability of clock-signal rise and fall times, and other performance-limiting phenomena.

A perusal of some modified CML latch structures described in the literature led to a proposal for a novel 'clock feedback' CML latch. In this device, timing parameters are favourably modified on adding cross-coupled feedback transistors between the clock terminals.

The design of dual modulus frequency dividers which use CML latches provided a second case study for Chapter-4. Two different implementations of a 3/4 dual-modulus synchronous divider were presented, one having a separate (explicit) control block for the modulus control, and another with the control logic embedded within the latch structure. An asynchronous CML divider for use in the prescaler was also proposed, one making use of combined master and slave latches sharing a common current source and employing a single pair of clock transistors. This technique turned out to be effective at reducing power consumption and chip area.

Simulation environment and test designs are described in Chapter 5. Also portrayed in this chapter are the steps taken, from initial design, through to the simulation, to design implementation. The setups for measuring functionality and physical parameters of

the two test-chips fabricated are described. A comparison of presented work with other recently published results reveal that the new methodologies exhibit better performance.

6.2 Summary of Contributions

- A modified CMOS CML latch has been proposed, one which uses a clock feedback scheme to realize smaller setup and hold times. It follows a known capacitive cross-coupling idea but PMOS device usage is novel.
- A 10 GHz static frequency divider in CMOS 0.18μm process, consuming about 0.5mW power.
- An 8 GHz dual-modulus (3/4) prescaler employing a CML embedded logic latch was developed (0.18μm CMOS design rules).
- It was found that both power and area savings of some 20% can be achieved for asynchronous CML dividers if master and slave latches share a common current source and use a single pair of clock transistors.

6.3 Potential for Future Research

The work described in this document may be extended in a number of directions. For example:

- The effect of technology scaling on the choice of clock feedback techniques should be explored.
- Multi-Modulus and Fractional-N dividers using embedded logic CML latches.
- Use of clock feedback latches in the multi Gigahertz phase/frequency detector (PFD) applications.
- etc.

Appendix A

MOSFET Capacitance

A.1 MOSFET Device Capacitance

Figure A.1 shows a typical cross-sectional view of the MOSFET device and the capacitances associated with each terminal. The actual capacitance value varies with the size and operating region of the device. Detailed information about MOSFET capacitance can be found in [5]. Table A.1 summarizes the capacitances in different operating regions.

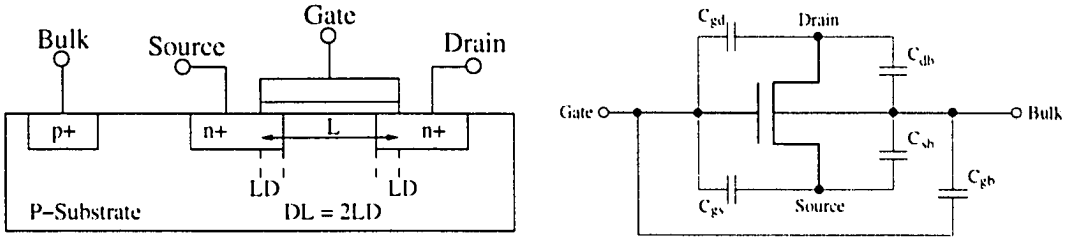


Figure A.1: MOSFET Cross-section and Capacitances

TABLE A.1: MOSFET Capacitance in different Operating Regions

Capacitance	Cut-Off	Triode	Saturation
C_{gd}	C_{ox}*LD*W	C_{ox}/2*W*L+C_{ox}*W*LD	C_{ox}*LD*W
C_{db}	C_j	Cj	Cj
C_{gb}	C_{ox}*W*L+Cox*DW*L	C_{ox}*DW*L	Cox*DW*L
C_{gs}	C_{ox}*LD*W	C_{ox}/2*W*L+C_{ox}*W*LD	2C_{ox}/3*W*L+C_{ox}*W*LD
C_{sb}	Cj	Cj	Cj
$C_{ox} = \varepsilon_{ox}/T_{ox}$, L = length, W = width , LD = Lateral-Diffusion , $DW = 2 \cdot LD$			

A.2 CML Latch Output Capacitance

The total capacitance at the output nodes of the CML latch is given by

$$C_o = C_L + C_{Hold} + C_j \tag{A.1}$$

Where C_L is the load capacitance, Cj is the drain to bulk junction depletion capacitance and C_{Hold} is the parasitic capacitance of the cross-coupled hold pair. It is interesting to note that both outputs see different output capacitances during the sample and the hold mode, as mentioned in the last section. These unequal output capacitances result in unequal rise and fall delays. It is assumed that the CML latch is driving a same size CML latch or buffer. The load capacitance C_L will also vary depending on the biasing conditions of the following stage. Let C_S^+, C_S^-, C_H^+ and C_H^- be the output capacitances of the positive and negative outputs during the sampling and the holding modes respectively.

A.2.1 +ve Node Capacitance during Sampling Mode

During the sampling mode hold pair transistors are in cut-off region, as well as the transistor whose drain voltage is high. Whereas the positive output will drive the next stage transistor into saturation. Therefore the total output node capacitance C_S^+ can be estimated using Equation A.1 as follows.

$$\begin{aligned} C_S+ &= (C_{gd} + C_{gs} + C_{gb})_{Sat} + (C_{db} + C_{gd} + C_{gs} + C_{gb})_{Off} + (C_{db})_{Off} \\ &= \frac{5}{3}C_{ox} \cdot W \cdot L + 4C_{ox} \cdot W \cdot LD + 2C_{ox} \cdot DW \cdot L + 2C_j \end{aligned} \tag{A.2}$$

A.2.2 -ve Node Capacitance during Sampling Mode

In this case the respective transistor of the sample pair is in saturation region, while the next stage transistor and the hold pair transistors are in cut-off state. Again, the total output node capacitance C_S^- can be estimated using Equation A.1.

$$C_{S^-} = (C_{gd} + C_{gs} + C_{gb})_{Off} + (C_{db} + C_{gd} + C_{gs} + C_{gb})_{Off} + (C_{db})_{Sat}$$

$$= 2C_{ox} \cdot W \cdot L + 4C_{ox} \cdot W \cdot LD + 2C_{ox} \cdot DW \cdot L + 2C_j \quad \text{(A.3)}$$

A.2.3 +ve Node Capacitance during Holding Mode

In this case one of the holding pair transistors is in the saturation region while the other transistor, as well as the transistors of the sample pair are in cut-off. The next stage transistor will be in saturation. The output capacitance C_H^+ can be found by Equation A.1.

$$C_{H^+} = (C_{gd} + C_{gs} + C_{gb})_{Sat} + (C_{db})_{Off} + (C_{gd} + C_{gs} + C_{gb})_{Sat} + (C_{db})_{Off}$$

$$= \frac{4}{3}C_{ox} \cdot W \cdot L + 4C_{ox} \cdot W \cdot LD + 2C_{ox} \cdot DW \cdot L + 2C_j \quad \text{(A.4)}$$

A.2.4 -ve Node Capacitance during Holding Mode

In this case the respective transistor of the holding pair is in saturation region, while the next stage transistor and the sampling pair transistors are in cut-off state. Again, the total output node capacitance C_H^- can be estimated using Equation A.1.

$$C_{H^-} = (C_{gd} + C_{gs} + C_{gb})_{Off} + (C_{db})_{Off} + (C_{gd} + C_{gs} + C_{gb})_{Off} + (C_{db})_{Sat}$$

$$= 2C_{ox} \cdot W \cdot L + 4C_{ox} \cdot W \cdot LD + 2C_{ox} \cdot DW \cdot L + 2C_j \quad \text{(A.5)}$$

Output node capacitances from Equations A.2 - A.5 are summarized in Table A.2.

TABLE A.2: CML Latch output node Capacitances

Sampling Mode	C_S^+	$(5/3)C_{ox}*W*L + C_M$
	C_S^-	$(4)\ C_{ox}*W*L + C_M$
Holding Mode	C_H^+	$(4/3)C_{ox}*W*L + C_M$
	C_H^-	$(4)\ C_{ox}*W*L + C_M$
$C_M=4C_{ox}*W*LD + 2C_{ox}*DW*L + 2C_j$		

It should be noted that the positive output node capacitance is always smaller than the negative output node capacitance. This results in unequal rise/fall times and switching point shifts from the mid-swing voltage.

Appendix B

Chip Schematics and Layouts

B.1 ICFCUMU1

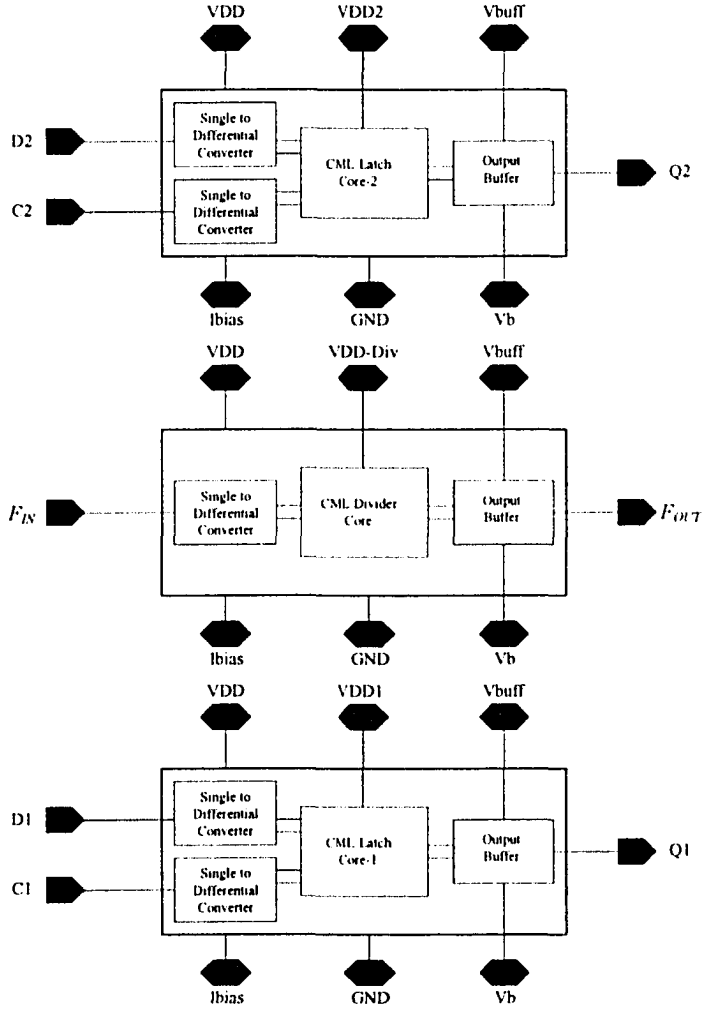


Figure B.2: Block Level Schematic of ICFCUMU1

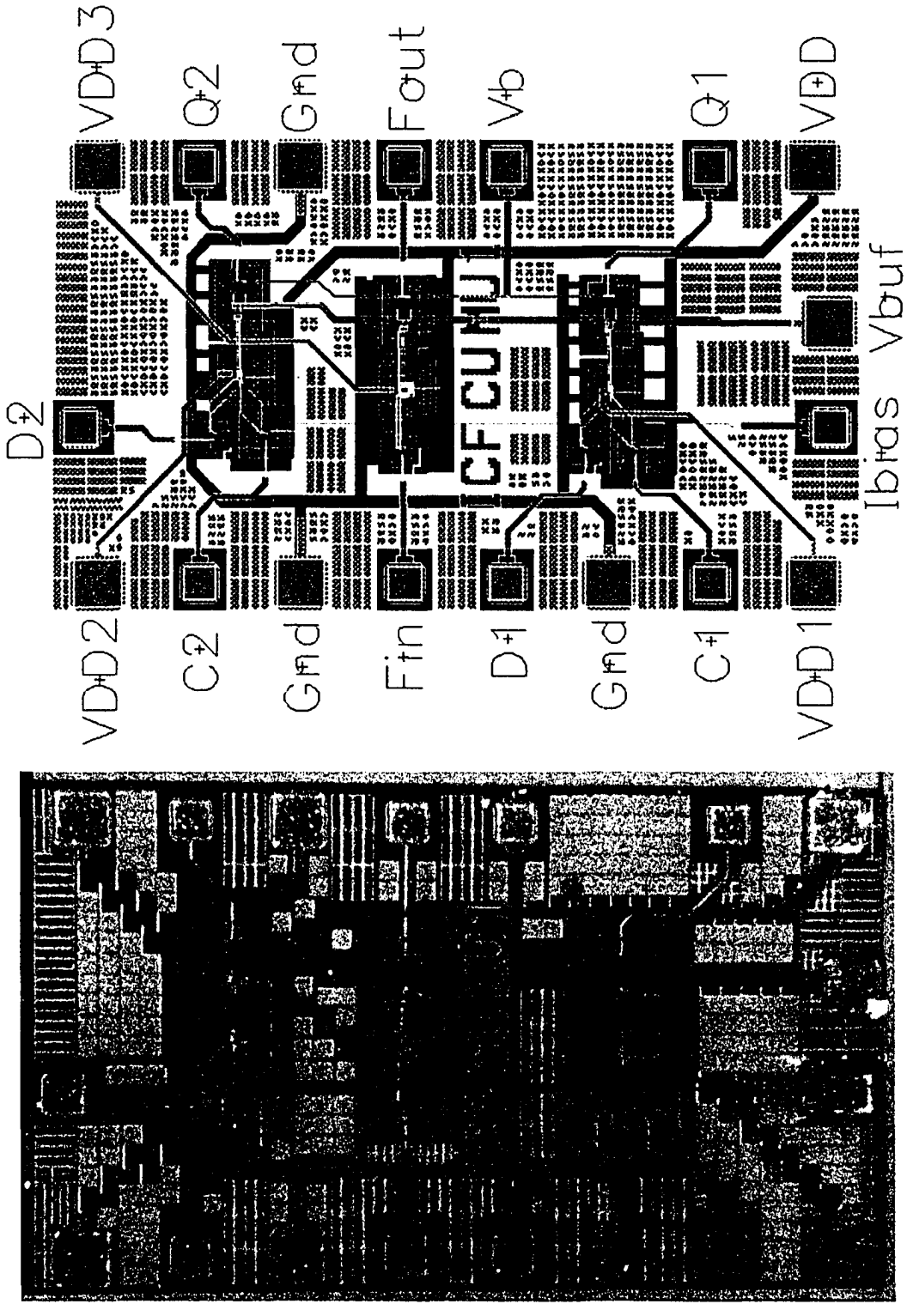


Figure B.3: ICFCUMU1: Layout and Chip Photograph

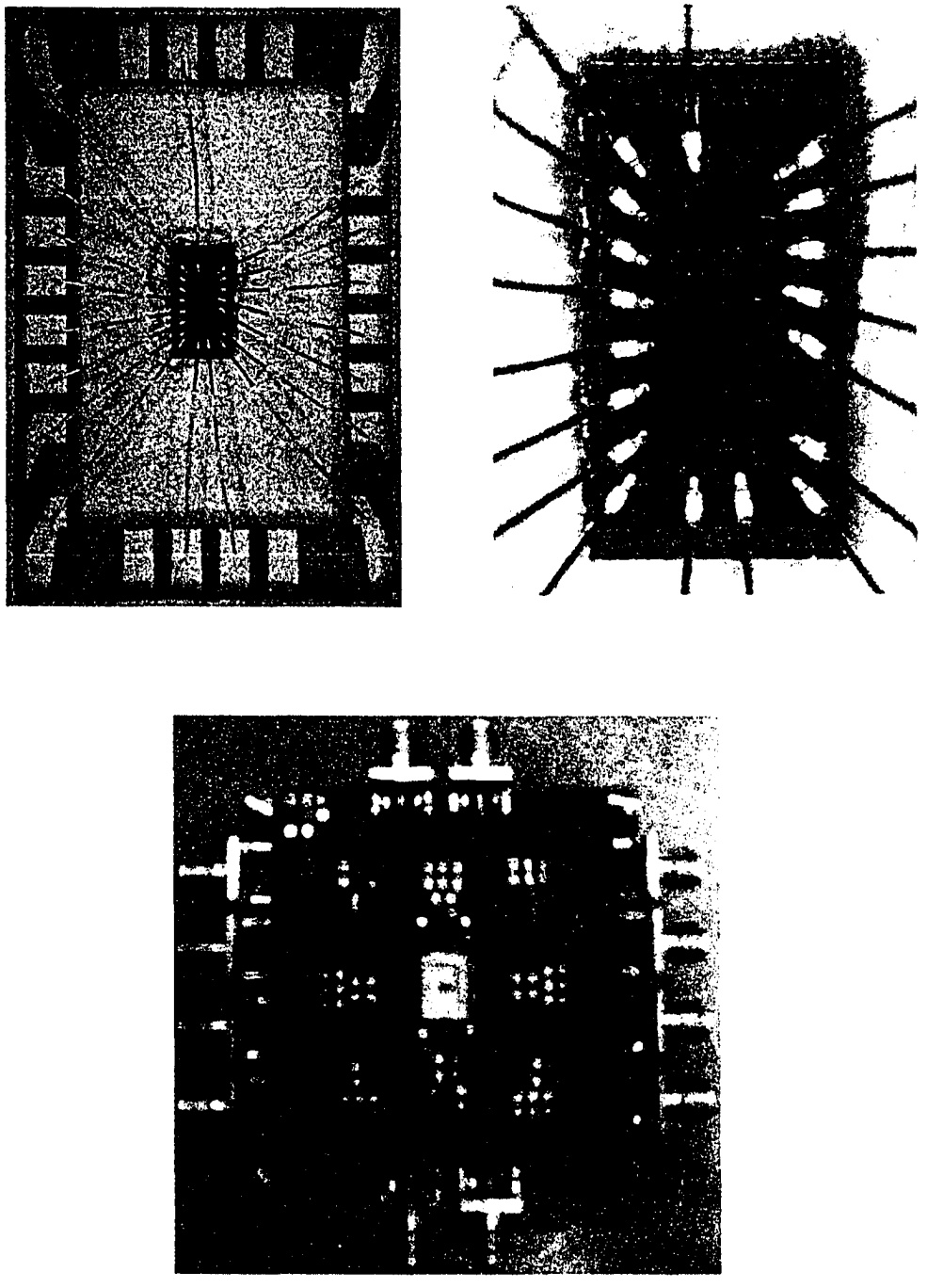


Figure B.4: Package, Bond wires and Test Fixture for ICFCUMU1

B.2 ICFCUMU2

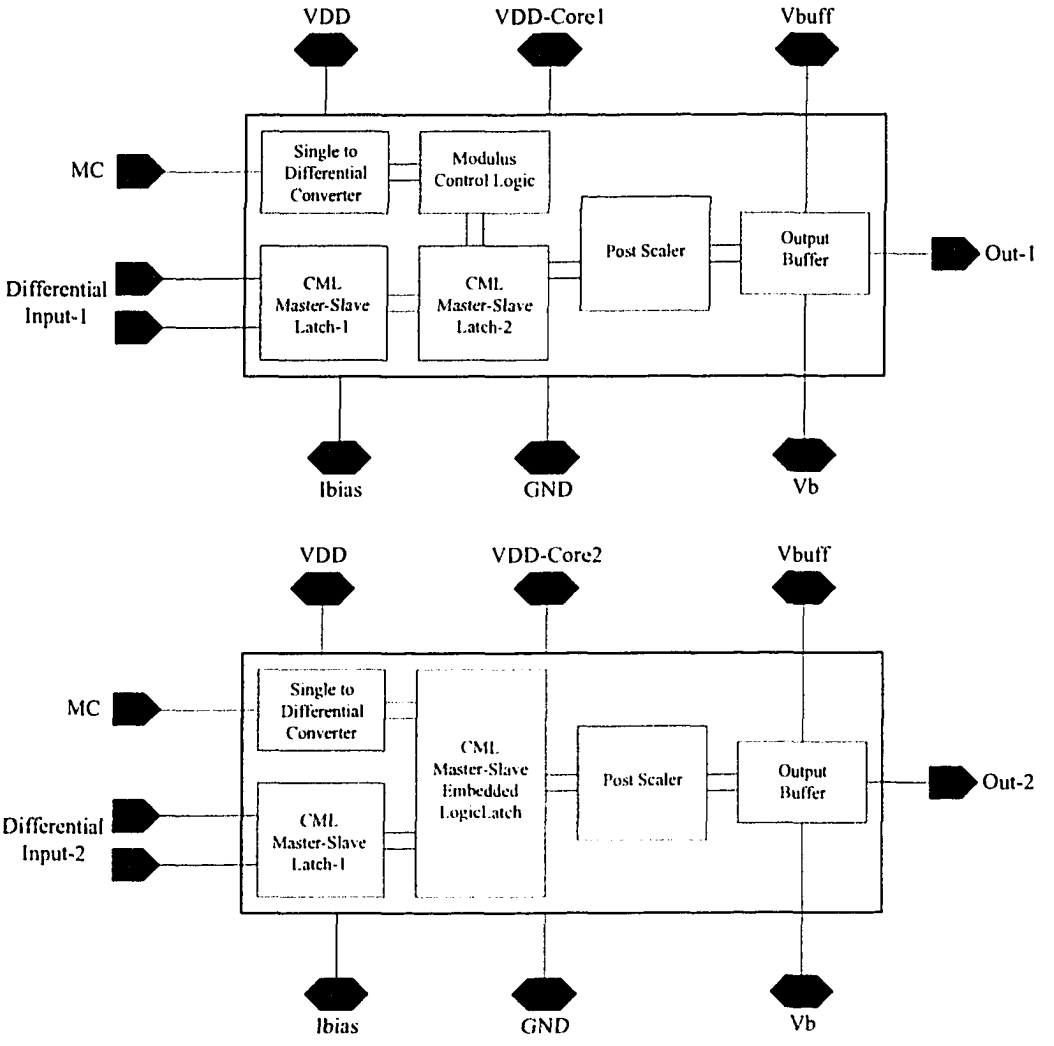


Figure B.5: Block Level Schematics of ICFCUMU2

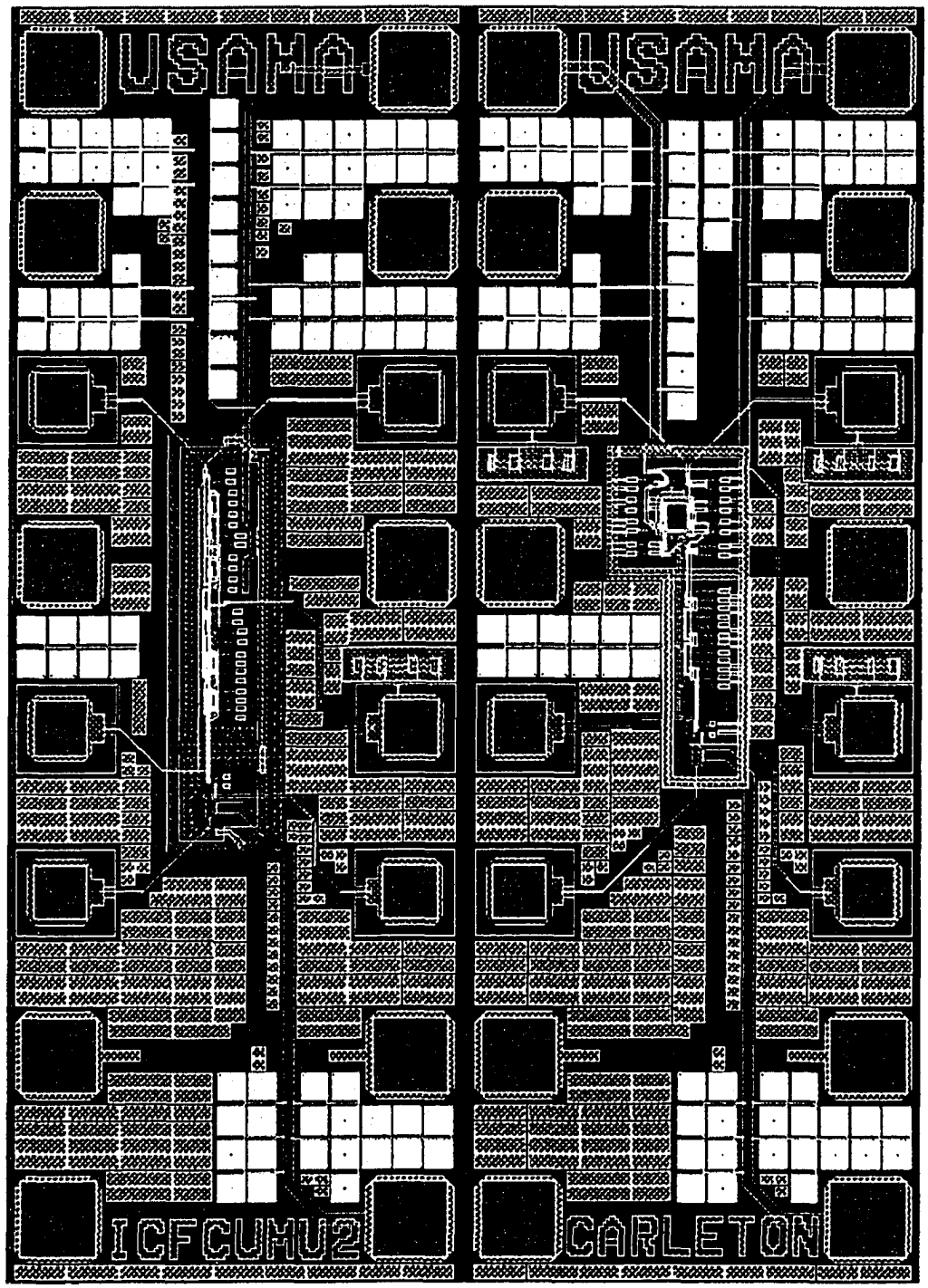


Figure B.6: Chip Layout of ICFCUMU2

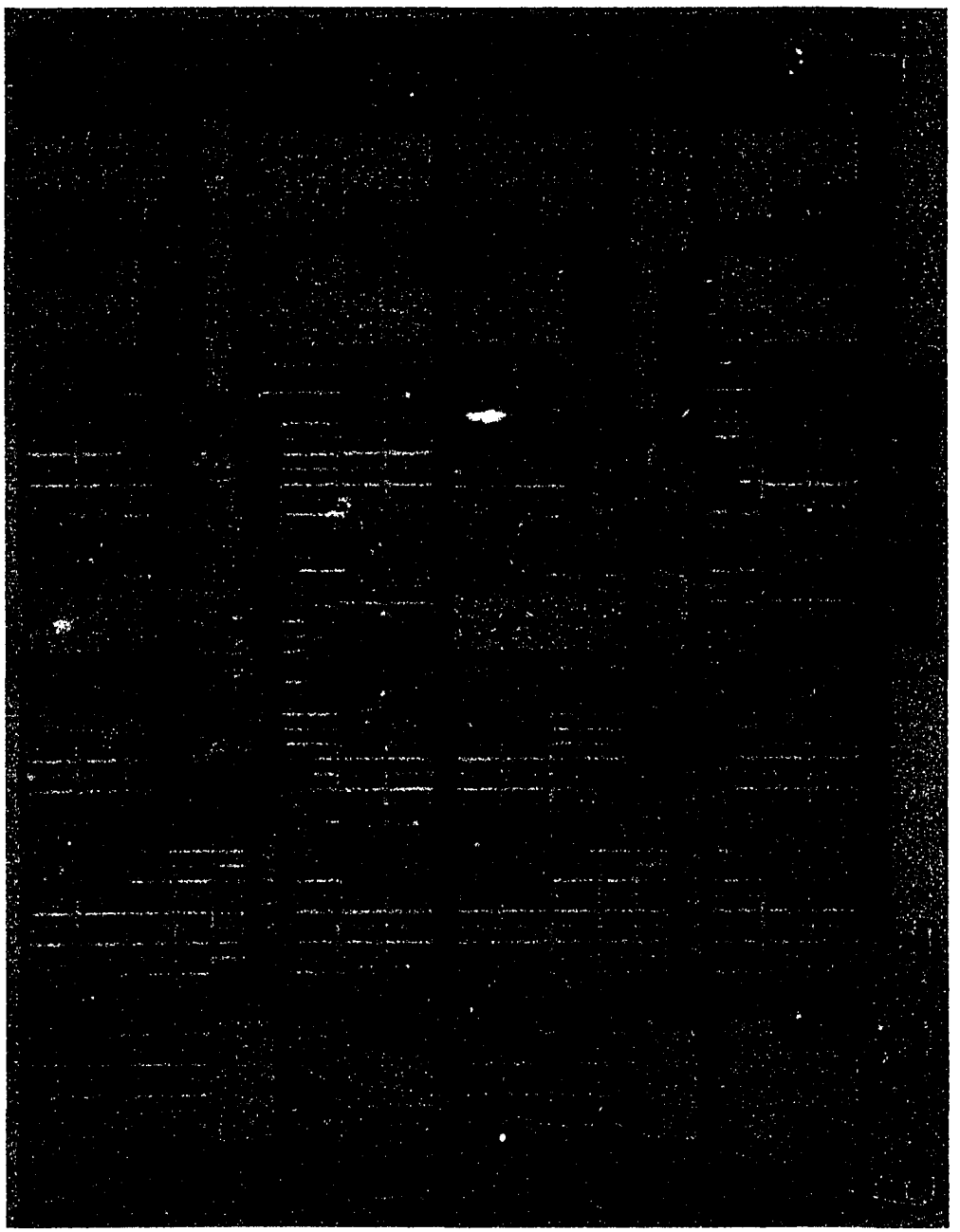


Figure B.7: Chip Photograph of ICFCUMU2

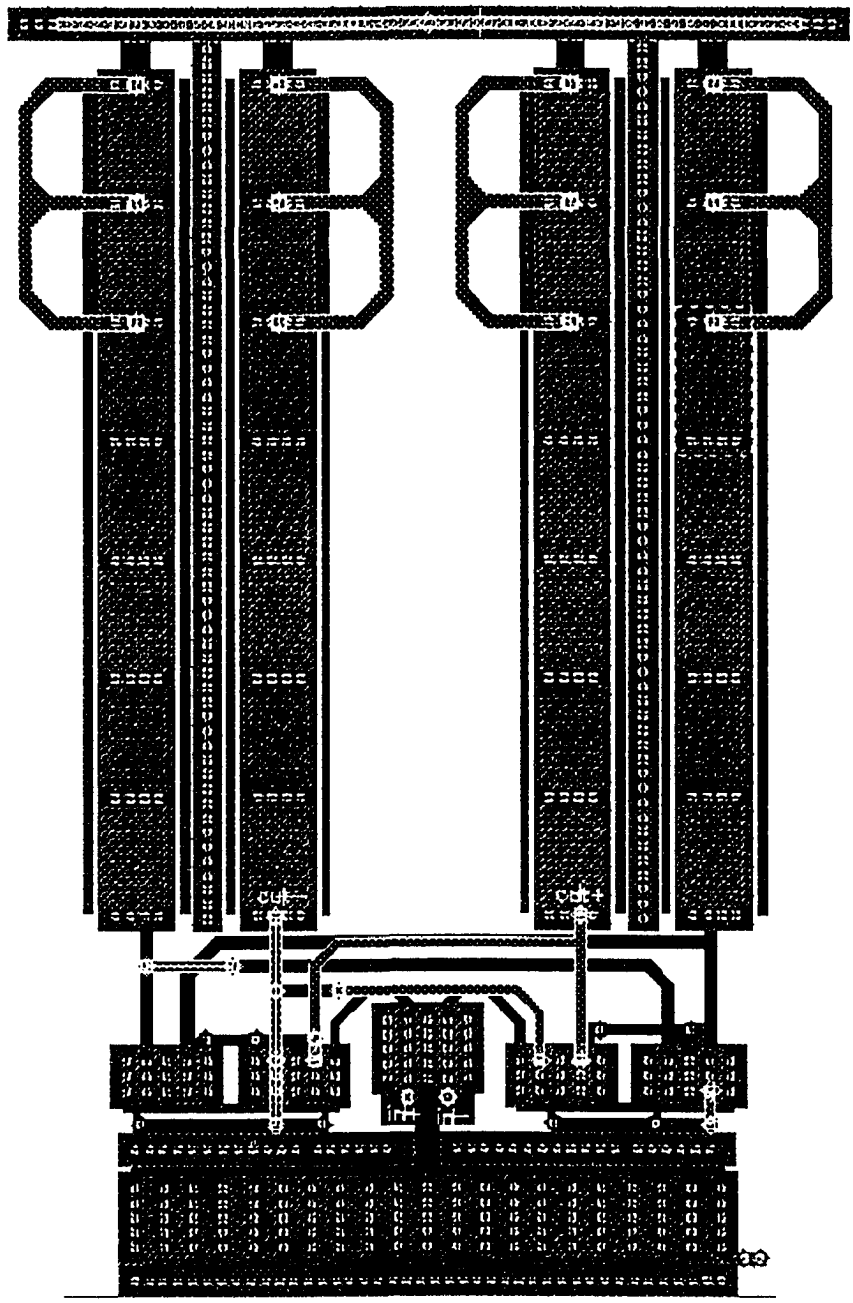


Figure B.8: Layout of Master-Slave Combined CML Latch

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