

A Variable Gain Low-Noise Amplifier for Use in an Integrated Television Tuner

by

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Abstract

The prohibitive cost and size of traditional television tuners are preventing the spread of television to poorer areas and mobile applications. Fully integrated television tuners could reduce the size and cost but currently face issues with noise and linearity which are both strongly dependant on the corresponding specifications of the low-noise amplifier (LNA). Noise and linearity face a trade-off in the LNA which can be dynamically adjusted depending on the input signal level.

In this thesis, a variable gain common-source amplifier is proposed to function as the front-end LNA in a television receiver system-on-chip (SoC). The amplifier employs bias adjustment in order to effect a continuously variable gain which the post-layout simulation results show to range from 9.4 dB to 14.5 dB. Noise figure ranges from 4 dB to 2.6 dB over this gain range while IIP_3 ranges from 1.8 dBm to 8 dBm. Measurements that correlate well to simulations have not been successfully made.

Unfortunately, the proposed variable-gain common-source LNA employing resistive feedback input matching does not meet the requirements determined by a system study. The system specifications are likely overly ambitious to be feasible with the current technology. Nevertheless, a charge-sampling architecture and corresponding low-noise transconductance amplifier is suggested to meet the system requirements.

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Nomenclature

ADC analog-to-digital converter

AGC automatic gain control

ATSC Advanced Television Systems Committee

BER bit error rate

BEOL back-end-of-line

CMC Canadian Microelectronics Corporation

CMFB common-mode feedback

CMFF common-mode feed-forward

CMOS complimentary metal-oxide-silicon

CNR carrier-to-noise ratio

CSO composite second-order beat

CTB composite triple-order beat

DC direct current

DOCSIS Data Over Cable Service Interface Specification

DSP digital signal processing

DTV digital television

DVB-T Digital Video Broadcasting — Terrestrial

ESD electro-static discharge

FIR finite impulse response

FEOL front-end-of-line

g_m transconductance

g_m - C transconductor-capacitor

IF intermediate frequency

IIR infinite impulse response

LO local oscillator

LNA low-noise amplifier

LNTA low-noise transconducting amplifier

MOSFET metal-oxide-silicon field effect transistor

NEF noise excess factor

NF noise figure

opamp operational amplifier

PER packet error rate

PVT process, supply voltage and temperature

RF radio frequency

SNR signal-to-noise ratio

RC resistor-capacitor

sinc sinus cardinalis

SoC system-on-chip

UHF ultra-high frequency (300–900 MHz)

VGA variable-gain amplifier

VNA vector network analyzer

Chapter 1

Introduction

This thesis describes the design of a variable gain low noise amplifier for use in a fully-integrated television tuner microchip. The design was achieved by researching current designs for low noise amplifiers and television tuners, simulating and implementing using the Cadence Design Suite and having the new design fabricated in IBM's 0.13 μm CMOS process and, finally, testing it. The goal of the thesis is to improve on current designs to assist with the ease of integration of television tuners.

1.1 Motivation

Our communication networks allow information to travel the globe at astonishing rates, allowing a shared global culture and knowledge. The broadcast radio and television networks seem to be the oldest and most connected of these networks sharing this global culture while also encouraging an individual, local culture—as evidenced in public broadcasting, such as the Canadian Broadcasting Corporation, and the multitude of local news stations—due to the limited broadcast area a transmitter can service. However, much of the world population is not able to share in the benefits of these networks, due mainly to prohibitive cost in poorer areas and limited portability.

The vast majority of current television tuner designs use lumped components and passive, off-chip filters primarily for their low distortion and high out-of-band attenuation. These benefits come at the cost of a large amount of variability in the parts, which requires manual tuning, and a large area and volume which prevents adoption of television tuners in mobile applications. For it to be useful, a fully integrated television tuner should be able to overcome these difficulties while having comparable out-of-band attenuation and low distortion relative to current designs.

Addressing these issues in an integrated receiver would be a step towards driving down costs and increasing integration with other electronics. This could catalyze an expansion of the communication networks, allowing more people to share in the benefits and opening up new markets to communications businesses.

1.2 Organization of thesis

This chapter gives an overview and introduction to the thesis including the motivation and background.

The rest of this thesis covers the design of the low noise amplifier. Chapter 2 describes the necessary background information and theory to design low-noise amplifiers. A hypothetical integrated tuner is described in Chapter 3. The design and simulation of the low noise amplifier is described in Chapter 4 and the implementation notes of the low-noise amplifier (LNA) can be found in Chapter 5. The testing, results and discussion of the fabricated circuit can be found in Chapter 6. A description of a possible future system intended to address the issues encountered with this design can be found in Chapter 7. Finally, Chapter 8 contains a summary of the results, conclusions drawn, and a discussion of possible future work.

Chapter 2

Background on Low-Noise Amplifiers and Variable Gain

There are a multitude of ways to design a broadband low-noise amplifier and also to vary the gain of an amplifier. Some of these methods will be discussed in this chapter.

2.1 Discussion of low-noise amplifiers

The low-noise amplifier is often the first component in a receiver chain. A full study of the receiver chain can be found in Chapter 3. There are generally two methods used to obtain a broadband input match. The first is a resistive negative feedback amplifier which uses a resistor in a negative feedback path to match the input impedance. This presents a direct trade-off between the input match and noise performance. The second method involves using a common-gate amplifier which has an input impedance of $Z_{in} = \frac{1}{g_m}$ where g_m is the transconductance of the input device. The larger the required input impedance is, the lower the transconductance of the device needs to be and thus, the lower the gain will be. These two methods can be combined and implemented in various ways to address specific drawbacks.

Along with the obtaining a broadband match, the signalling method also needs to be addressed. A differential circuit offers immunity to even-ordered distortion as the even-ordered distortion products tend to cancel and will be filtered out with the use of common-mode feedback (CMFB) and common-mode feed-forward (CMFF) circuits designed to remove common-mode signals from the differential signals. These circuits can also remove much of the common-mode noise, to the benefit of the amplifier's noise figure. This comes at the expense of increased on-chip area. Also, in television

systems, the cable used is single-ended with the outer sheath grounded so an off-chip balun is required to convert the single-ended signal to a differential signal for the front-end input in a differential system. This introduces loss and noise in the front-end and the cost of another part.

Some of the benefits of differential signalling can be obtained with a single-ended input and differential output circuit but this method tends to have a relatively large noise figure.

Following is a summary of published amplifiers employing some of the previously discussed techniques.

2.1.1 Amplifiers employing common-gate input matching

The low-noise amplifier (LNA) described in [1] is a two-stage single-ended to differential programmable-gain amplifier designed to achieve high linearity intended for use in the front-end of a mobile digital television (DTV) receiver. The first stage, shown in Figure 2.1, is a single-ended to differential converter that employs the opposite gain of common-gate and common-source amplifiers to perform the conversion without the use of a transformer. The common-gate amplifier provides the input matching and the gain of the amplifiers are matched to ensure a balanced differential signal. The gains are matched by using matched transistors biased from the same source and using matched load resistors. The second stage is shown in Figure 2.2 and employs two differential pairs with opposite second-order transconductance derivatives to cancel higher-order distortion. Programmable gain in the first stage is accomplished by switching in parallel output resistors, as shown in Figure 2.3, and the gain of the second stage is programmed using variable current sources. The overall IIP_3 is 10 dBm, noise figure is 5.7 dB, gain is 10 dB and power consumption is 5.2 mW and the chip is implemented in a 0.18 μm CMOS process.

Another paper [2] describes an LNA intended for use in digital terrestrial and cable TV tuners. This amplifier is single-ended and designed to cancel second-order distortion. It is based on a previous circuit, described in [3], that is fully-differential and employs noise cancelling of common-gate and common-source amplifiers, as shown in Figure 2.4. The new amplifier, however, uses a complementary CMOS parallel push-pull circuit instead of the differential circuit in order to remove the need for a lossy

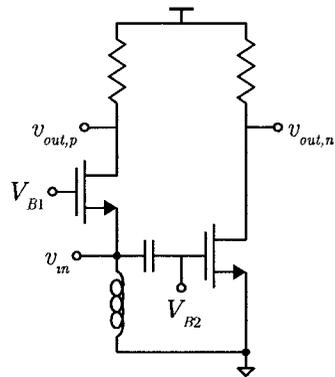


Figure 2.1: Schematic of input stage amplifier used in [1]

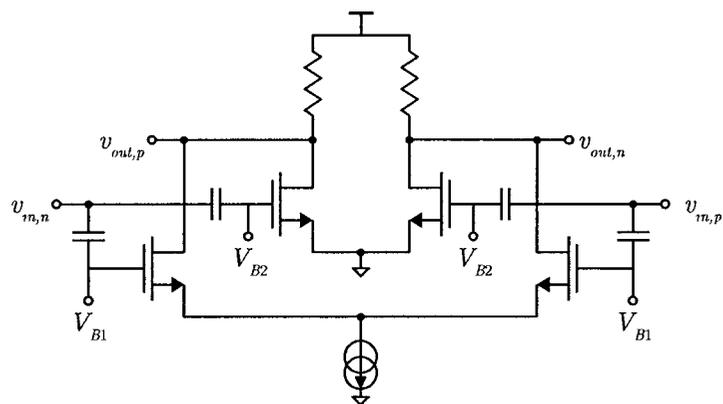


Figure 2.2: Schematic of second-stage amplifier used in [1]

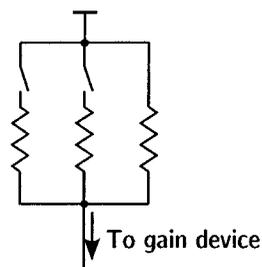


Figure 2.3: Schematic showing programmable gain load described in [1]

balun and decrease noise figure. The amplifier is able to achieve an IIP_3 of 3 dBm, an IIP_2 of 44 dBm, a power gain of 14 dB and a noise figure of 3 dB at a power consumption of 34.76 mW with 2.2 V rails.

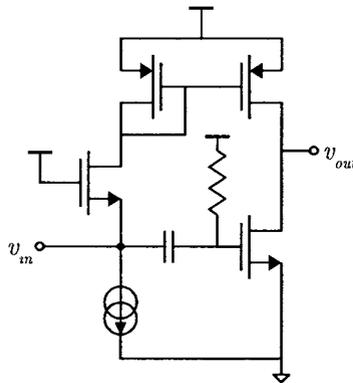


Figure 2.4: Schematic showing noise cancelling common-gate and common-source amplifiers used in [2]

The LNA proposed in [4], also intended for use in DTV tuners, uses a similar noise cancelling scheme but is implemented with positive current feedback to increase gain. The amplifier has an IIP_3 of 2.7 dBm, an IIP_2 of 43 dBm, a power gain of 20.5 dB and a noise figure of 3.3 dB with a power consumption of 32.4 mW on 1.8 V rails.

2.1.2 Amplifiers employing negative-feedback matching

Two papers [5, 6] describe an LNA intended for use in a terrestrial DTV receiver. This amplifier aims to decouple the noise and impedance matching trade-off by exploiting the inverted signal gain and non-inverted noise of a negative-feedback matched common-source transistor. A noise-cancelling technique is thus described. The analysis in [6] adds to that of [5] by considering linearity, a load impedance and lower power consumption. Overall, the circuit has been shown to have a gain of about 13.5 dB at a power consumption of between 30 mW and 35 mW for [6] and [5], respectively, both from 2.2 V rails. The circuit is able to achieve a noise figure less than 2.2 dB and an IIP_3 of 0 dBm. However, this circuit is able to trade off increased noise for increased linearity and can achieve a noise figure less than 3.5 dB and an IIP_3 of 3.3 dBm.

A DTV LNA that employs negative feedback for input power matching is described in [7]. This amplifier is intended for use in cable tuners and amplifies frequencies in the range 54–880 MHz. Instead of using a resistor in negative feedback, the input

impedance is set by a source-follower in feed back at the input, as shown in Figure 2.5. This amplifier uses a combination of current steering and negative transconductance (g_m) to effect variable gain with a suitable trade-off between linearity and bandwidth. In all, this amplifier is able to achieve an IIP₃ of between 5 and -21 dBm, a return loss greater than 8.2 dB, a noise figure between 2.8 and 6 dB, variable gain between 11 dB and 22.5 dB at a power consumption of 41.4 mW from a 1.8 V rail.

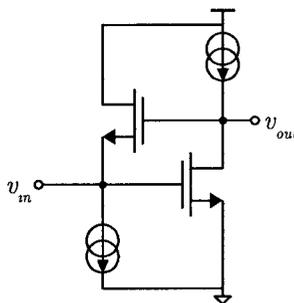


Figure 2.5: Schematic showing the active feedback input matching employed in [7]

Another DTV LNA utilising negative feedback input matching is found in [8] but it is only intended for use in the UHF television band (470–870 MHz). This amplifier is designed to have a near-constant output signal-to-noise ratio (SNR) and, to achieve this, includes a stepped attenuator followed by a variable-gain cascode amplifier. The negative feedback path is made to have constant gain, regardless of the cascode gain, in order to achieve an input match across gain levels. At higher levels of pre-attenuation, the input matching is switched to a resistive shunt at the input equal to the source impedance (75Ω) to save power. This amplifier is able to achieve a gain range of 16 dB to -17 dB, a noise figure between 4.3 dB and 35 dB, an input return loss greater than 11 dB across all gain settings and frequencies of interest, and an IIP₃ of between -1.5 dBm and 27 dBm, all at a power consumption of 22 mW from a 1.8 V rail.

2.1.3 Effect of power matching on noise

For the most common input power matching circuits, the theoretical minimum noise factor that can be obtained is $1 + \text{NEF}$, in which the noise excess factor (NEF) is $\gamma \frac{g_{d0}}{g_m}$ in a MOSFET [5]. In a sub-micron CMOS process, γ and $\frac{g_{d0}}{g_m}$ are both greater than one, which results in a minimum noise figure of greater than 3 dB. In fact, a power

match and a noise match are quite different unless special attention is paid to obtain a simultaneous noise and power match [9]. However, the technique described in [9] requires on-chip inductors and is therefore only useful for high-frequency, narrow-band applications. In addition to the separate noise and power match points, the theoretical minimum noise figure is highly dependant on the gain of the amplifier in most cases, with the 3 dB minimum only achievable at very high gain settings. An amplifier is presented [10] that is able to achieve a theoretical minimum noise figure of $1 + \text{NEF}$ independent of gain by employing a noise cancelling technique. Pursuing this further, [5] presents an amplifier which manages to achieve a sub-3 dB noise figure using noise cancellation. It seems that in order to achieve a power match and a sub-3 dB noise figure for wideband, relatively low-frequency applications where on-chip inductors are infeasible, noise cancelling techniques must be used.

2.2 Discussion of variable gain

Variable gain is desirable in a low-noise amplifier because it can be used to vary the trade-off between noise figure and linearity. At low input signal levels, linearity is not much of an issue as distortion products are usually much lower than the desired; indeed, they are likely below the noise floor. At low signal levels, the dominant source of signal degradation is noise. To minimize the overall noise figure of a system, it is desirable to have an amplifier with low noise and high gain at the front of the signal chain as noise contributions of signal blocks afterwards are reduced by a factor of the preceding gain, as per Friis equation. However, as signal strength increases, the noise becomes less of an issue while distortion becomes more of one. The noise level remains constant but the signal level increases thus the SNR increases. While the signal level increases, the distortion products increase at higher rate (2 dB/dB for second-order, 3 dB/dB for third-order, and so on). If the gain of the LNA can be adjusted, then the gain can be set to optimize the balance between noise and linearity for a given input signal level.

In general, the voltage gain of a MOSFET amplifier can be calculated as $g_{m,\text{eq}}R_{L,\text{eq}}$, where $g_{m,\text{eq}}$ is the equivalent transconductance and $R_{L,\text{eq}}$ is the equivalent load resistance. Thus, the gain of a MOSFET amplifier can be varied by either varying the device transconductance or the load resistance. The method of varying gain depends on the desired values of gain. Some methods are better suited to discrete gain steps

while others are better suited to continuous gain controlled by a continuous feedback signal.

There are two basic methods to control gain by controlling load resistance: switched resistors and bias-controlled load MOSFETs. When using switched resistors, resistors are placed in series with MOSFET switches, which are placed in parallel with other resistor-switch combinations. The total load resistance is then equal to the equivalent resistance of the connected resistors in parallel, as in [1]. This should have a minimal effect on linearity, as long as the on-resistance of the switches is much lower than the value of the series resistor and the off-resistance of the switches is much greater than the rest of the connected parallel resistors. That being said, special consideration must be paid to ensure that the output node does not stray too close to a DC node and thus begin clipping.

Instead of resistors, MOSFETs can be used as loads, usually in the active-region, as a current source, or in the triode-mode, as a voltage-controlled resistor. A triode-mode MOSFET has an output impedance dependent on the gate-source voltage which can be controlled continually over a certain range. This type bias-controlled MOSFET is not used very frequently as linearity is a problem due to the relationship between v_{ds} and current being non-linear, as opposed to an ideal resistor.

As a current source, the MOSFET will usually have more of an effect on the transconductance of the active element as opposed to the load resistance. However, active-mode MOSFETs can be exploited in a current steering topology. In this case, the bias on two MOSFETs is controlled to direct current from the gain device to either an output load resistance or a dummy load. This topology is used in [8] where the amplifier is, in effect, a variable-gain cascode amplifier. The paper goes further to describe a circuit for digitally controlling the gain in linear-dB steps using master-slave amplifiers and feedback.

The transconductance of a MOSFET is approximated by the square-law equation (2.1). The factor μC_{ox} is constant for a given process, so to vary the transconductance of a MOSFET either the $\frac{W}{L}$ ratio or the bias current must be varied. Usually, the length of a transistor cannot be easily changed once the transistor has been fabricated but the width can be varied to some extent. Because MOSFETs are fabricated as blocks of small transistors, or fingers, connected in parallel, all with equal widths and lengths, the effective width of a transistor can be changed by switching on more of these fingers. An example schematic of this can be found in Figure 2.6. In this case,

when S is high, the total width is $W_1 + W_2$, while when S is low, the total width is W_1 . Depending on how such a transistor is biased, this can also have the effect of increasing the bias current, I_{DS} .

$$g_m = \sqrt{2\mu C_{ox} \frac{W}{L} I_{DS}} \quad (2.1)$$

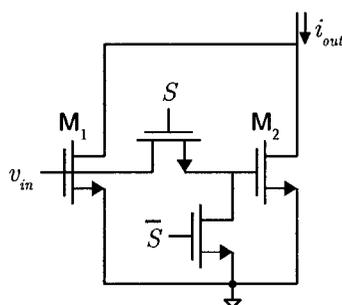


Figure 2.6: A schematic showing an example of a variable width transistor

The bias current of a MOSFET can also be adjusted independently of the width, in order to vary the transconductance. The gate to source bias voltage can be used in this regard to directly affect the bias current. Such a system could use a fully analog control loop to effect a continuous change in transconductance of the gain device. Alternatively, the gain device could be self-biased such that the drain-source and gate-source voltages are related at DC but independent at the desired frequency of operation. In such a scheme, the transconductance of the gain device is controlled by a separate current source.

For the purposes of an integrated television tuner, a continuous variable gain has been recommended as opposed to discrete gain steps. This is intended to reduce modulation and distortion caused by dithering the gain steps to achieve a fractional gain step.

2.2.1 Automatic gain feedback loop

Automatic gain control is a feedback loop and follows the same analysis as generic feedback loops. The goal of the automatic gain loop is to ensure that the signal-to-noise-and-distortion level remains relatively constant, regardless of the input power level. In other words, the loop ensures that the signal level is high enough above the

noise level but not so high that the distortion in the signal chain does not allow the signal to be correctly demodulated. The automatic gain loop consists of the signal chain from the variable gain amplifier to the power detector, the power detector, a low-pass filter, and a difference amplifier for comparing the measured power to a desired power level. Some of this loop can be implemented by digital signal processing (DSP), depending on the desired complexity of the loop and the ease of implementation. Since automatic gain involves a feedback loop, loop instability is an issue that must be paid close attention to. Additionally, the automatic gain control (AGC) loop should not add distortion to, or otherwise modulate the signal, so the loop bandwidth should be kept to a minimum. Decreasing the loop bandwidth too much will cause the loop to react too slowly to input power changes and increase the delay for the tuner to tune to a new channel.

The power detector is circuit used to measure the average power of the signal and can be as simple as a diode. A more advanced power detector is described in [11] and includes the power comparator and low-pass filter.

2.3 Conclusion

In general, input power matching, low noise and high linearity are divergent requirements and often require a trade-off to achieve optimal set of figures to meet the system requirements. It is likely possible to dynamically assign the trade-off for a given input signal level by employing variable gain in the amplifier. Additionally, it is clear that sub-3 dB in a sub-micron CMOS process can only be attained by employing noise-cancelling techniques. Unfortunately, variable gain techniques do not lend themselves well to noise-cancelling or indeed low-noise. It will make an interesting exercise to attempt to achieve a low noise figure whilst providing variable gain in an amplifier.

Chapter 3

Integrated Television Tuner System Design

In this chapter, we will investigate the design of integrated digital television (DTV) receivers and develop a system design using the specifications given by the three of the most widely deployed DTV and digital cable standards. These system specifications are then used to determine the specifications for the low-noise amplifier (LNA) design discussed in Chapter 4.

A television receiver, as with most receivers, front-end generally consists of a LNA, a radio frequency (RF) filter, an RF to intermediate frequency (IF) mixer, an IF filter, an IF amplifier, an IF to baseband mixer, a baseband filter, a baseband amplifier and an analog-to-digital converter (ADC) [12]. An example UHF-band television receiver block diagram can be found in Figure 3.1. Note that traditional television tuners use discrete components that need to be manually tuned and tested when produced. A fully integrated solution could reduce the costs associated with manufacturing television tuners by eliminating the cost associated with manually testing and tuning the components.

Due to the large bandwidth (roughly 50 MHz–800 MHz) that a tuner must be able to tune to and the variability in signal strength and distance, the major difficulties with designing television tuners are linearity and dynamic range. Common techniques to increase linearity include using different signal chains to handle different sub-bands and using high quality factor, high-order analog filters. To address the dynamic range, various variable gain amplifiers are generally used in the baseband and IF chains as part of an automatic gain control (AGC) system. Also, to reduce non-recoverable engineering costs, the tuner should be designed to receive as many of the competing

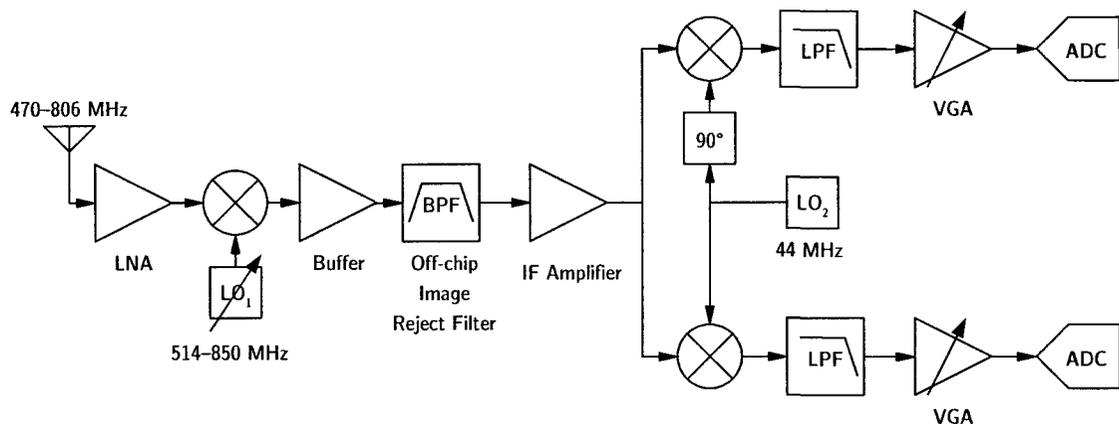


Figure 3.1: Block diagram of a typical UHF-band television receiver

standards as possible, with [13, 14] being the most prolific. The standards being targeted with this receiver system are ATSC [13], DVB-T [14] and DOCSIS [15].

3.1 Receiver Requirements

Tables 3.1, 3.2 and 3.3 summarize the specifications from [13–16]. An explanation of these specifications follows in this chapter. The receiver should have a $75\ \Omega$ input impedance. The standards also specify differing modulation schemes. The modulation scheme used by the ATSC specification is an eight-level vestigial side-band amplitude modulation (8VSB). The scheme used by the DVB-T specification is a quadrature-amplitude modulation with up to 64 levels (64QAM). The DOCSIS specification also uses a quadrature-amplitude modulation but this time with up to 256 levels (256QAM). The modulation type and minimum required bit error rate (BER) for a desired quasi-error free bit stream are used to determine a minimum signal-to-noise ratio (SNR) or carrier-to-noise ratio (CNR) at the ADC.

The specifications from Tables 3.1, 3.2 and 3.3 can be transformed into common specifications using the worst-case specification where there are conflicts. This has been done and the overall system specification can be found in Table 3.4.

Some important transformations to highlight are the transformations of composite second-order (CSO) and composite triple-beat (CTB) to IIP_2 and IIP_3 , respectively, and

Table 3.1: Summary of DOCSIS 3.0 specifications [15]

Parameter	Value Unit
Channel spacing	6 MHz
Minimum carrier-to-noise	35 dB
Minimum composite triple beat	41 dBc
Minimum composite second order	41 dBc
Maximum amplitude ripple	3 dB
Maximum carrier level	17 dBmV
Maximum number of carriers	121
Input frequency range	54–1002 MHz

Table 3.2: Summary of ATSC specifications [13] and best practises [16]

Parameter	Value Unit
Minimum carrier level	−83 dBm
Maximum carrier level	−8 dBm
Minimum bit error rate	3×10^{-6}
Minimum signal-to-noise ratio	18 dB
Typical antenna gain	12 dBi
Minimum analog-to-digital converter SNR	10 bit
Adjacent channel rejection for −68 dBm desired	40 dBc
Adjacent channel rejection for −53 dBm desired	35 dBc
Adjacent channel rejection for −28 dBm desired	26 dBc
Next adjacent channel rejection for −68 dBm desired	44 dBc
Next adjacent channel rejection for −53 dBm desired	40 dBc
Next adjacent channel rejection for −28 dBm desired	30 dBc
Nominal peak-to-average ratio	6.3 dB

Table 3.3: Summary of DVB-T specifications [14]

Parameter	Value Unit
Maximum packet error rate (PER)	1×10^{-7}
Minimum SNR for given PER [17]	28 dB
Channel spacing	6, 7 & 8 MHz
Nominal peak-to-average ratio [18]	7.5 dB

Table 3.4: System specifications derived to meet or exceed DOCSIS, ATSC and DVB-T specifications

Input Level	Parameter	Value Unit	Origin
—	Nominal input impedance	75 Ω	—
Minimum	RMS input voltage	19.4 μV	ATSC
	RMS noise voltage density	1.15 $\text{nV}/\sqrt{\text{Hz}}$	ATSC
	Adjacent channel rejection	40 dBc	ATSC
	Next adjacent channel rejection	44 dBc	ATSC
	Input referred second-order intercept point	8.25 V_{RMS}	—
	Input referred third-order intercept point	908 mV_{RMS}	—
Moderate	RMS input voltage	7.08 mV	DOCSIS
	RMS noise voltage density	17.4 $\text{nV}/\sqrt{\text{Hz}}$	DOCSIS
	Adjacent channel rejection	40 dBc	DOCSIS
	Next adjacent channel rejection	44 dBc	DOCSIS
	Input referred second-order intercept point	8.25 V_{RMS}	DOCSIS
	Input referred third-order intercept point	908 mV_{RMS}	DOCSIS
Maximum	RMS input voltage	109 mV_{RMS}	ATSC
	RMS noise voltage density	24.6 $\text{nV}/\sqrt{\text{Hz}}$	—
	Adjacent channel rejection	40 dBc	—
	Next adjacent channel rejection	44 dBc	—
	Input referred second-order intercept point	8.25 V_{RMS}	—
	Input referred third-order intercept point	908 mV_{RMS}	—

minimum carrier level to input-referred noise voltage density.

The maximum measured CTB, measured at the centre channel, can be calculated from (3.1), where P_{in} is the input power for the other channels and N is the maximum number of carriers. This equation can be re-arranged, as in (3.2), to obtain a target IIP₃ point for a given CTB specification.

$$\text{CTB [dB]} = 2 (\text{IIP}_3 - P_{\text{in}}) - 6 - 10 \log \left(\frac{3}{8} (N - 1)^2 \right) \quad (3.1)$$

$$\text{IIP}_3 = P_{\text{in}} + \frac{1}{2} \left(\text{CTB} + 6 + 10 \log \left(\frac{3}{8} (N - 1)^2 \right) \right) \quad (3.2)$$

Similarly, (3.3) and (3.4) can be used to derive a required IIP₂ for a given CSO specification. In this case, N_B is the number of beats next to a low carrier. This value is roughly twice as large for lower channels as for higher channels and can be calculated using (3.5) where f_L is the lowest frequency of the desired band, f_H is the highest frequency and d is the difference between the carrier frequency and multiples of the channel separation. In the case of digital television, the value of d is 1.31 MHz.

$$\text{CSO [dB]} = \text{IIP}_2 - P_{\text{in}} - 10 \log N_B \quad (3.3)$$

$$\text{IIP}_2 = \text{CSO} + P_{\text{in}} + 10 \log N_B \quad (3.4)$$

$$N_B = (N - 1) \left(1 - \frac{f_L - d}{f_H - f_L} \right) \quad (3.5)$$

For noise calculations, the required noise figure (NF) can be calculated from the minimum detectable signal using (3.6), where B is the channel bandwidth. The noise figure can be converted to a noise voltage density, with units of $\text{V}/\sqrt{\text{Hz}}$, using (3.7), where k is Boltzmann's constant and T is temperature, the product of which is roughly 4.11×10^{-21} J at room temperature.

$$\text{NF} = P_{\text{min}} - 10 \log B \quad (3.6)$$

$$v_{ni} = \sqrt{\left(10^{\frac{\text{NF}}{10}} - 1 \right) 2kTZ_{\text{in}}} \quad (3.7)$$

A complete set of specifications can be calculated using assumptions based on the given specifications. For this exercise, the IIP₂ and IIP₃ calculated for the moderate input level will be assumed to be the minimum IIP₂ and IIP₃ at all input levels. Using

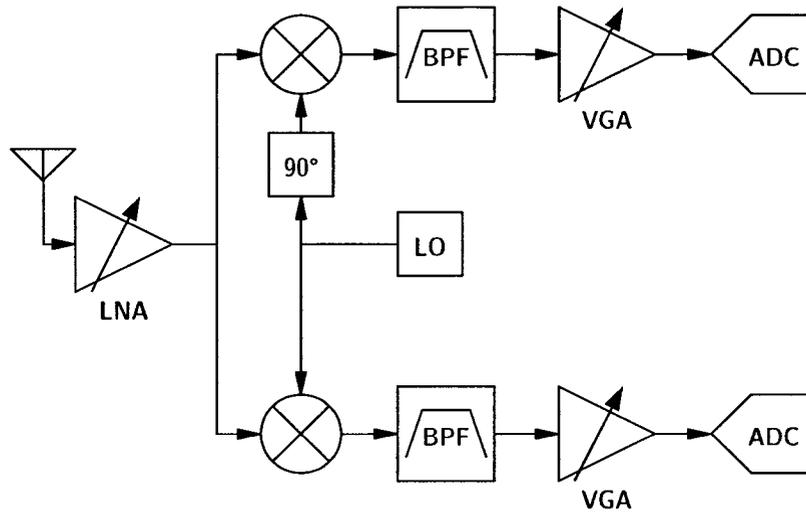


Figure 3.2: System-level block diagram of television receiver

this assumption, maximum second-order and third-order blockers at the minimum input level are $2.16 \text{ mV}_{\text{RMS}}$ and $7.77 \text{ mV}_{\text{RMS}}$, respectively. The 1 dB compression point, as a result of the specified IIP_3 , will be $298 \text{ mV}_{\text{RMS}}$ or $844 \text{ mV}_{\text{P-P}}$. To prevent clipping from limiting the 1 dB compression point, attention must be paid to the rail voltage of each block. Similarity, the noise and channel rejection specifications can be extrapolated to the maximum input level setting.

3.2 Receiver Signal Chain

The receiver architecture is based on [19] and the system-level schematic can be found in Figure 3.2. The receiver consists of a variable-gain low-noise amplifier, followed by an in-phase and quadrature-phase (I/Q) mixer which mixes the desired channel to a low IF of 5.38 MHz. Each I/Q path contains a fixed band-pass filter and a variable-gain amplifier for AGC, followed by an ADC. The system uses a low IF of 5.38 MHz and low-side injection, so to tune to all of the required frequencies, the local oscillator (LO) must be able to tune from 50 MHz to 992 MHz in steps of, at most, 1 MHz, to account for the varying channel sizes. The specifications for each component can be found in Tables 3.5–3.8 and the methods for determining these specifications are

Table 3.5: Specifications for LNA block

Input Level	Parameter	Value Unit
—	Input impedance	75 Ω
Minimum	Voltage gain	12 dB
	Input-referred noise density	0.874 nV/ $\sqrt{\text{Hz}}$
	Input third-order intercept point	1.09 V
	Input second-order intercept point	13.8 V
Moderate	Voltage gain	9 dB
	Input-referred noise density	0.966 nV/ $\sqrt{\text{Hz}}$
	Input third-order intercept point	1.38 V
	Input second-order intercept point	21.8 V
Maximum	Voltage gain	6 dB
	Input-referred noise density	1.06 nV/ $\sqrt{\text{Hz}}$
	Input third-order intercept point	1.73 V
	Input second-order intercept point	27.4 V

Table 3.6: Specifications for mixer and LO block

Parameter	Value Unit
Voltage gain	5 dB
Input-referred noise density	1.93 nV/ $\sqrt{\text{Hz}}$
Input third-order intercept point	7.08 V
Input second-order intercept point	89.1 V
Maximum phase noise at 6 MHz offset	-108 dBc /Hz

Table 3.7: Specifications for IF filter block

Parameter	Value Unit
Voltage gain	0 dB
Input-referred noise density	3.55 nV/ $\sqrt{\text{Hz}}$
Input third-order intercept point	22.4 V
Input second-order intercept point	224 V
Amplitude mismatch (between paths)	0.03 dB
Phase mismatch (between paths)	0.5 °
Centre frequency	5.38 MHz
Minimum channel bandwidth	5.38 MHz
Maximum channel bandwidth	8 MHz
Stop-band attenuation at one bandwidth away from centre	30 dB

explained in the remainder of this chapter.

3.3 System Noise Calculations

In a matched system, Friis formula can be used to calculate the cascaded noise figure of the system. However, integrated circuits often are not matched systems as they tend to transform voltage signals as opposed to power signals and the input and output impedance for each circuit is difficult to determine ahead of time. This makes the use of Friis equation inadequate to determine cascaded noise characteristics. For this reason, we will specify the noise characteristics of each circuit as a input-referred noise voltages. Note that input-referred noise voltages can be cascaded similarly to noise factors, as shown in (3.8), where v_{ni} is input-referred noise voltage and A_V is voltage gain.

$$v_{ni(\text{total})}^2 = v_{ni,1}^2 + \left(\frac{v_{ni,2}}{A_{V,1}}\right)^2 + \left(\frac{v_{ni,3}}{A_{V,1}A_{V,2}}\right)^2 + \dots \quad (3.8)$$

As shown in (3.8), the input-referred noise voltage of the first component in the signal chain has the greatest effect on the total noise of the system, assuming that

Table 3.8: Specifications for VGA block

Input Level	Parameter	Value Unit
Minimum	Voltage gain	70 dB
	Input-referred noise density	2.17 nV/ $\sqrt{\text{Hz}}$
	Input third-order intercept point	58.7 mV
	Input second-order intercept point	846 mV
Moderate	Voltage gain	21 dB
	Input-referred noise density	370 nV/ $\sqrt{\text{Hz}}$
	Input third-order intercept point	41.0 mV
	Input second-order intercept point	237 mV
Maximum	Voltage gain	0.5 dB
	Input-referred noise density	371 nV/ $\sqrt{\text{Hz}}$
	Input third-order intercept point	38.7 mV
	Input second-order intercept point	351 mV
—	Amplitude mismatch (between paths)	0.03 dB
	Phase mismatch (between paths)	0.5 °

each component has a voltage gain greater than one. Also, the noise contribution of a component is inversely scaled by the voltage gain preceding it. This can be rearranged to estimate the noise budget of a component, as in (3.10).

$$v_{ni,(total)}^2 = v_{ni,comp}^2 + \left(\frac{v_{ni,(other)}}{A_{V,comp}} \right)^2 \quad (3.9)$$

$$v_{ni,(other)} = A_{V,comp} \cdot \sqrt{v_{ni,(total)}^2 - v_{ni,comp}^2} \quad (3.10)$$

It should be noted that there are two degrees of freedom given in (3.10), as voltage gain and input noise voltage for a given active component can be adjusted independently of each other. A simple approach to balancing this equation would involve attempting to maximize gain early in the signal chain in order to relax requirements on other components. However, this would result in difficult to achieve linearity requirements, as described in Section 3.4.

3.4 System Intermodulation Calculations

The cascaded third-order input intermodulation voltage points can be calculated using (3.11), where iip_3 is an input third-order intermodulation voltage point, A_V is a linear voltage gain and S_V a selectivity measurement, i.e. the voltage attenuation of out of band signals. For the purpose of these equations, selectivity is the ratio between pass-band voltage gain and stop-band voltage gain of a filter. A more selective filter allows the use of components with lower input intermodulation points after the filter.

$$\frac{1}{iip_{3,(total)}^2} = \frac{1}{iip_{3,1}^2} + \frac{A_{V,1}^2}{S_{V,1}^3 iip_{3,2}^2} + \frac{(A_{V,1}A_{V,2})^2}{(S_{V,1}S_{V,2})^3 \cdot iip_{3,3}^2} + \dots \quad (3.11)$$

Similar to how the noise budget of each block is estimated in Section 3.3, (3.11) is re-arranged to (3.12) in order to estimate the third-order intermodulation budget of each component.

$$iip_{3,(other)} = \frac{A_{V,comp}}{S_{V,comp}^3 \cdot \sqrt{iip_{3,(total)}^{-2} - iip_{3,comp}^{-2}}} \quad (3.12)$$

Cascaded second-order input intermodulation voltage points can be calculated and estimated similarly, by using (3.13) and (3.14), respectively.

$$\frac{1}{\text{iip}_{2,(\text{total})}} = \frac{1}{\text{iip}_{2,1}} + \frac{A_{V,1}}{S_{V,1}^2 \text{iip}_{2,2}} + \frac{A_{V,1}A_{V,2}}{(S_{V,1}S_{V,2})^2 \cdot \text{iip}_{2,3}} + \dots \quad (3.13)$$

$$\text{iip}_{2,(\text{other})} = \frac{A_{V,\text{comp}}}{S_{V,\text{comp}}^2 \cdot (\text{iip}_{2,(\text{total})}^{-1} - \text{iip}_{2,\text{comp}}^{-1})} \quad (3.14)$$

3.5 Automatic Gain Control Specifications

In order to be able to handle the wide range of input signal levels, the receiver must be able to tune the gain of the signal chain so that the signal amplitude at the input of the ADC is fixed. This ensures that the ADC is running at optimal efficiency and accuracy is not wasted when the signal is small.

The signal amplitude at the input of the ADC is determined by the voltage rail of the ADC and the expected peak-to-average power ratio of the signal. The input signal is expected to range from 19.4 μV to 109 mV from the antenna. If the ADC is differential and has 1.5 V rails and we assume an 80 percent usable range, then the maximum peak-to-peak voltage is 2.4 V. The RMS voltage of such a full-swing signal would be 849 mV and with an expected peak-to-average power ratio of 6.3 dB (for the case of an ATSC signal), the RMS signal level at the input of the ADC would be 411 mV. This means that the receiver requires a gain between 11 dB and 87 dB.

3.6 Signal Interference Specifications

The signal can be interfered with in the signal chain by a few sources other than thermal noise and intermodulation products—namely LO noise and spurs mixing adjacent channels on top of the desired channel and mismatch between I/Q channels allowing the image channel to leak through.

Local oscillator interference The phase noise and any spurs of the LO can mix interfering signals onto the intermediate frequency, f_{IF} , as long as the difference in frequency between the oscillator noise and the interfering signals is equal to f_{IF} .

Near in oscillator phase noise has a natural roll-off of 30 dB/dec until flicker noise is no longer a factor, then roll-off becomes 20 dB/dec until the phase noise reaches a thermal noise floor [20]. Because of this roll-off, the primary source of interference comes from adjacent channels. Thus, the maximum allowable phase noise can be

calculated from the adjacent channel rejection specification. To achieve the adjacent channel specification, the phase noise at a 6 MHz phase offset must be 40 dB below the centre frequency and 68 dB below that to account for the phase noise integrated over the 6 MHz channel bandwidth. This gives a maximum phase noise requirement of -108 dBc/Hz at a 6 MHz offset.

I and Q mismatch interference Due to the low IF, the image frequency lies in the lower next-adjacent channel, so the next adjacent channel rejection requirement will be most useful for determining I/Q mismatch specifications. Using [12] as a reference, to achieve an image rejection of at least 45 dB, the amplitude and phase imbalance of the I/Q paths must be less than 0.03 dB and 0.5° , respectively.

3.7 Performance consequences on DVB-T

Since the DVB-T specifications have little detail on the requirements of a receiver, the performance of the receiver must be calculated after designing it. A summary of the expected performance of the receiver in DVB-T mode can be found in Table 3.9. Second- and third-order intermodulation performance will be similar to that of the expected ATSC and DOCSIS performance.

Table 3.9: Expected performance of receiver in DVB-T mode

Input Level	Parameter	Value Unit
Minimum	RMS input voltage	3.16 mV
	Voltage gain	41 dB
Maximum	RMS input voltage	95.0 mV
	Voltage gain	11.5 dB

3.8 Conclusion

The proposed method of simultaneously decreasing noise and linearity requirements by varying the gain of the LNA appears to have succeeded. Examining the block

specifications shows that as input signal level increases, both intermodulation and noise requirements decrease whereas normally, while the noise requirements decrease, intermodulation requirements would remain constant, if not worsen.

3.8.1 Low-noise amplifier conclusions

Since the LNA has a known input impedance, the performance figures can be transformed into power figures to make it easier to simulate and test. A summary of the modified figures can be found in Table 3.10.

Table 3.10: Specifications for LNA block using power units

Input Level	Parameter	Value Unit
—	Input impedance	75 Ω
Minimum	Power gain	12 dB
	Noise figure	3.5 dB
	Input third-order intercept point	12 dBm
	Input second-order intercept point	34 dBm
Moderate	Voltage gain	9 dB
	Noise figure	4.0 dB
	Input third-order intercept point	14 dBm
	Input second-order intercept point	38 dBm
Maximum	Voltage gain	6 dB
	Noise figure	4.5 dB
	Input third-order intercept point	16 dBm
	Input second-order intercept point	40 dBm

Chapter 4

LNA Design and Simulation

In this chapter, the design specified in Chapter 3 for a variable-gain low-noise amplifier is discussed. The basic architecture for the amplifier can be found in [20] with that design modified for the desired frequency range, distortion and variable gain. The schematic for this design can be found in Figure 4.1. Noise-cancelling could be employed similar to [5] and that discussed in Chapter 2 but it was decided that this would negatively affect the intended method of varying the gain.

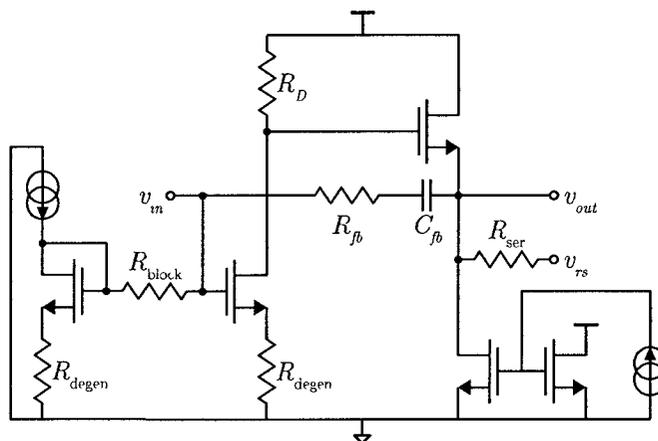


Figure 4.1: Device-level schematic for this circuit

To help achieve the desired linearity, a 3.3 V rail voltage was chosen at the cost of power consumption. Because of the high rail voltage, a thick-oxide transistor must be used so the IBM `nfet33_rf` model was chosen for all of the transistors in this design. This model allows a voltage across the gate oxide of up to 3.6 V before the oxide breaks down and the transistor is destroyed. The radio frequency (RF) model was used as it models the effects of a substrate ring and metal interconnects to the

transistor which the standard model does not include. The use of this model should allow a better correlation between the pre- and post-layout simulations.

The design of the amplifier was split into steps. To begin, the transistor was characterized to determine the optimum current density for low-noise operation. The transistor was then scaled to provide sufficient gain and low-distortion and the resistor sizes were calculated from the scaled quiescent current. After finding a theoretical solution, parametric analysis was performed on all parts in order to achieve maximum linearity and sufficient gain and noise figure. The output buffer was designed entirely using parametric analysis. What follows is a discussion of these design steps.

4.1 Transistor characterization and sizing

A characterization circuit was devised to determine the current density at which the minimum noise figure can be achieved. This was determined to be $J_{opt} = 32.5 \mu\text{A}/\mu\text{m}$ using a minimum length transistor. The width of the transistor was scaled to a width of $W = 250 \mu\text{m}$, which makes the required bias current, I_{bias} , 8 mA. Also, the transconductance of the transistor is estimated at this stage to be 25 mA/V.

4.2 Resistor sizing

There are three RF resistors in the circuit: the drain resistor, R_D , between the positive power rail and the drain of the gain transistor; the source-degeneration resistor, R_{degen} , between the source of the gain transistor and the negative power rail; and, the feedback resistor, R_{fb} , between the output buffer and the input. The rest of the resistors in the circuit are used for biasing and so should be made as large as feasible.

The drain resistor determines the voltage of the gain stage, along with the transconductance of the gain transistor. It also determines the bias voltage on the gain transistor's drain and the buffer transistor's gate based on the bias current in the gain transistor. To allow for a maximum voltage swing of $\pm 1.5 \text{ V}$ on the gain transistor's drain, the drain resistor should be set such that $R_D = \frac{1.5 \text{ V}}{8 \text{ mA}} = 187.5 \Omega$.

The source-degeneration resistor is used to limit the gain of the amplifier and prevent instability. This resistor presents a direct trade-off between high-gain and high-stability. To strike a balance between gain and stability, this resistance is set at $R_{\text{degen}} = 10 \Omega$.

The feedback resistor is used to provide a broad-band input power match for a $[75]\Omega$ input impedance. A small-signal analysis of the circuit can be used to determine the input impedance of the amplifier, as in (4.1).

$$R_{\text{IN}} \approx \frac{R_{fb}}{g_m R_D} \quad (4.1)$$

Note that $g_m R_D$ is the approximate voltage gain of the amplifier. Since the input impedance should be matched to the source impedance of $R_S = 75 \Omega$, (4.2) shows the rearranged equation to solve for R_{fb} . This gives $R_{fb} = 337.5 \Omega$.

$$R_{fb} = 75 \Omega \cdot 24 \text{ mS} \cdot 187.5 \Omega \quad (4.2)$$

4.3 Simulation results

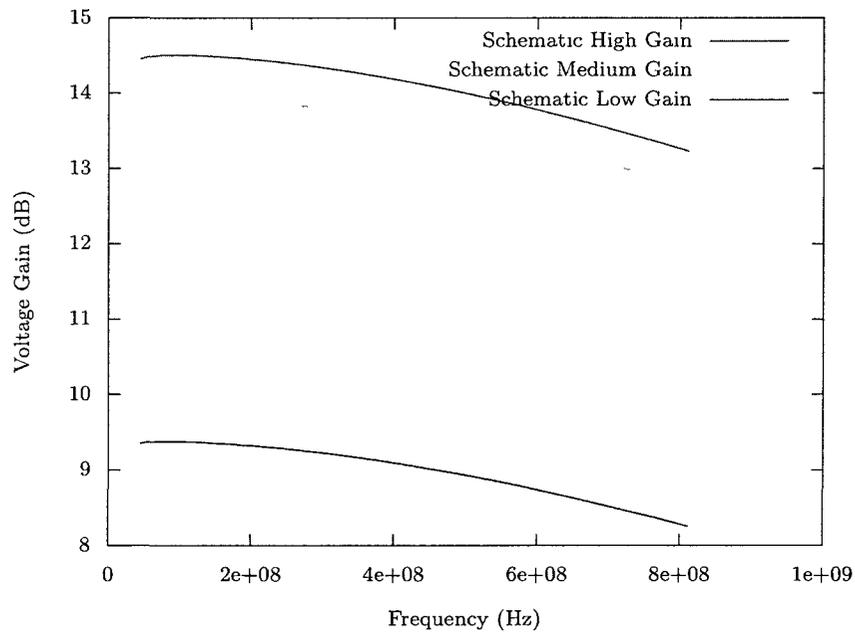
Parametric analysis was performed to find the correct balance between power consumption, linearity, noise figure and gain. The final sizing can be found in Table 4.1.

For all simulations, the ATSC specifications were specifically targeted so frequency sweeps were performed over the 44–812 MHz range. The simulated voltage gain can be found in Figure 4.2. At the high-gain setting, the maximum gain is 14.5 dB and the minimum gain is 13.2 dB and the variation in gain is 1.3 dB. At the low-gain setting, the maximum gain is 9.4 dB, the minimum gain is 8.3 dB and the gain variation is 1.1 dB. This gives a 5.1 dB difference in gain between the high-gain setting and the low-gain setting.

The simulated noise figure plots can be found in Figure 4.3. At the high-gain setting, the noise figure remains below 3.4 dB and reaches a minimum of 2.8 dB. Similarly for the low-gain setting, the noise figure remains below 4.3 dB and reaches a minimum of 3.9 dB.

Table 4.1: Parameter sizing for simulated circuit

Parameter	Theoretical Value	Simulated Value	Unit
Gain transistor width	250	600	μm
Gain transistor length	130	400	nm
Gain transistor number of fingers	50	120	
Buffer transistors width	—	300	μm
Buffer transistors length	—	400	nm
Buffer transistors number of fingers	—	60	
Drain resistor	187.5	186.94	Ω
Source-degeneration resistor	10	10.1	Ω
Feedback resistor	337.5	374.51	Ω

**Figure 4.2:** Voltage gain of simulated schematic

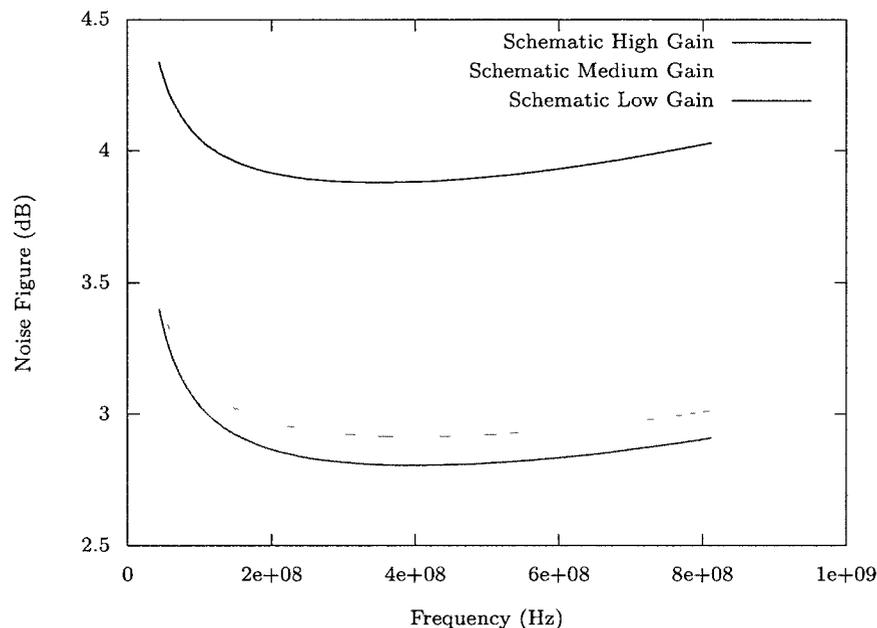


Figure 4.3: Noise figure of simulated schematic

The input matching can be observed in Figure 4.4. For the input matching, the return loss is greater than 15 dB for most of the range with only the low-gain setting reaching below this to a minimum of 14.7 dB. This represents a fairly good input matching.

As for the output match, the output impedance should be kept much smaller than the load impedance to minimize distortion, as described in [20]. With a simulated output load representing the input of an on-chip mixer of 500Ω , the output impedance of the buffer should be kept much smaller than 500Ω . The plots of the simulated output impedance can be found in Figure 4.5. They show that for all gain settings, the impedance never reaches more than 13.5Ω .

A summary of the distortion measurements can be found in Table 4.2. This table shows the input and output third-order intermodulation points for high, medium and low gain settings. The high-gain setting has the best linearity with an IIP_3 of 8.0137 dBm and the low-gain setting has the worst linearity with an IIP_3 of 1.7765 dBm. Similarly, the IIP_2 points are recorded in Table 4.3 which shows an IIP_2 of 16.003 dBm at maximum gain and an IIP_2 of 2.0794 dBm at the minimum gain setting. Note that these results do not match the specifications from Table 3.10,

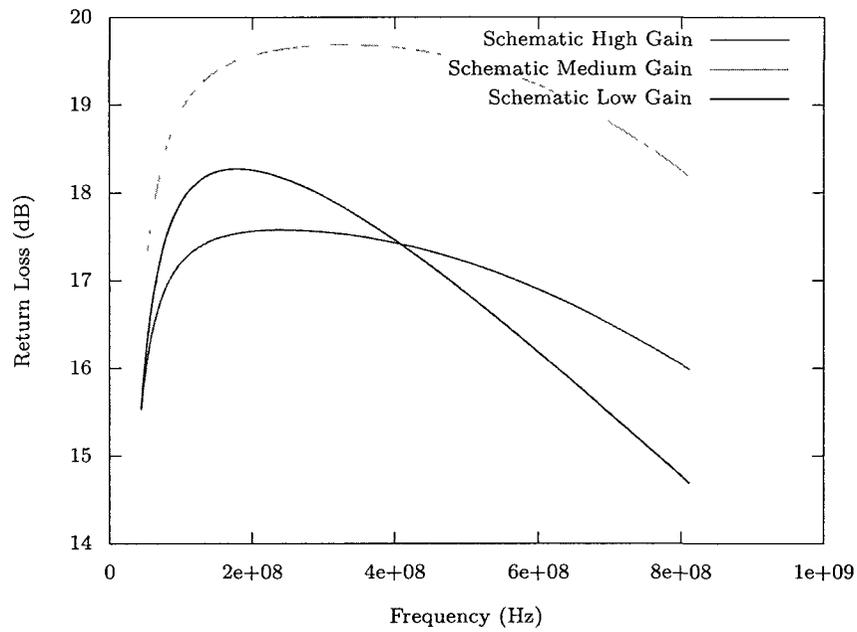


Figure 4.4: Return loss of simulated schematic

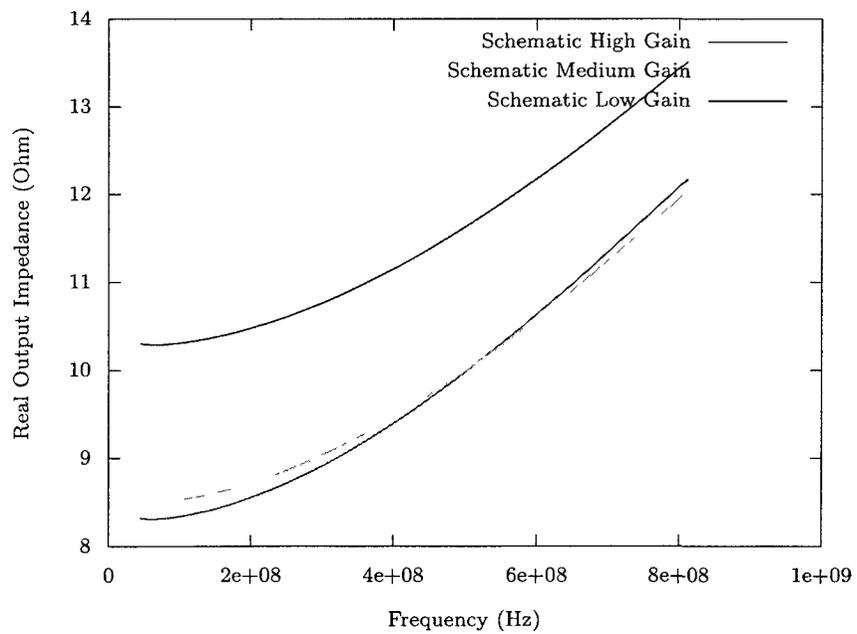


Figure 4.5: Real output impedance of simulated schematic

so the system will need to be redesigned in order to use this design. This is addressed in Chapter 7.

Table 4.2: IP_3 points of simulated schematic

Gain Setting	Input (dBm)	Output (dBm)
High	8.0137	12.653
Medium	7.6125	12.0408
Low	1.7765	3.4100

Table 4.3: IP_2 points of simulated schematic

Gain Setting	Input (dBm)	Output (dBm)
High	16.003	20.643
Medium	21.856	26.284
Low	2.0794	3.7128

4.4 Conclusion

The simulation results show that this design provides a broad-band match, a variable gain between roughly 8 dB and 13 dB and a noise figure between 4.3 dB and 2.8 dB. The linearity of this amplifier, as measured by the input third-order intercept point, varies between 1.8 dBm at low gain, and 8.0 dBm at high gain.

Note that this linearity does not meet the requirements discussed in Chapter 3. With the current linearity, the maximum number of simultaneous channels the receiver can receive in DOCSIS mode is 63. To meet the specifications, either the low-noise amplifier (LNA) will need to be tuned to a small portion of the bandwidth and replicated to fill the band, or a new design will need to be used that meets the full linearity requirements.

If the proposed LNA was duplicated and tuned to two separate bands, then the required IIP_3 for the DOCSIS specification would become 7.4 dBm, which is within the

capabilities of this LNA.

Chapter 5

Implementation

The low-noise amplifier was implemented using a $0.13\ \mu\text{m}$ CMOS process from IBM using the Cadence Design Suite and Layout XL. The chip layout can be seen in Figure 5.1 and the layout for just the LNA can be found in Figure 5.2

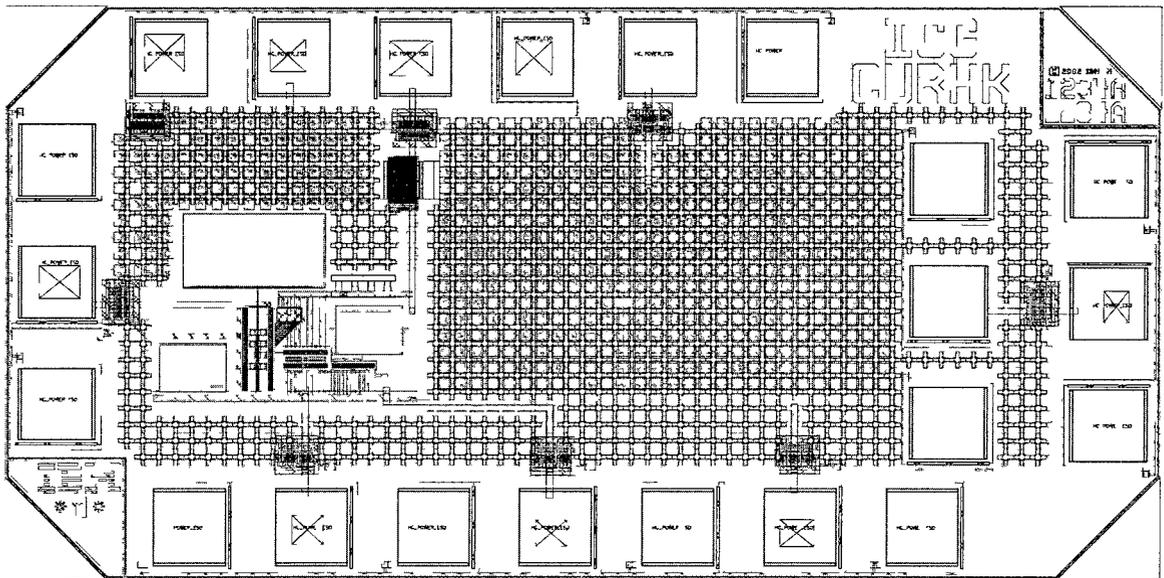


Figure 5.1: Layout of LNA test chip measuring $0.7 \times 1.4\ \text{mm}$

5.1 Layout Concerns

There were a few issues that required special attention during layout. Special attention was given to resistor model choice, output de-embedding, DC current handling,

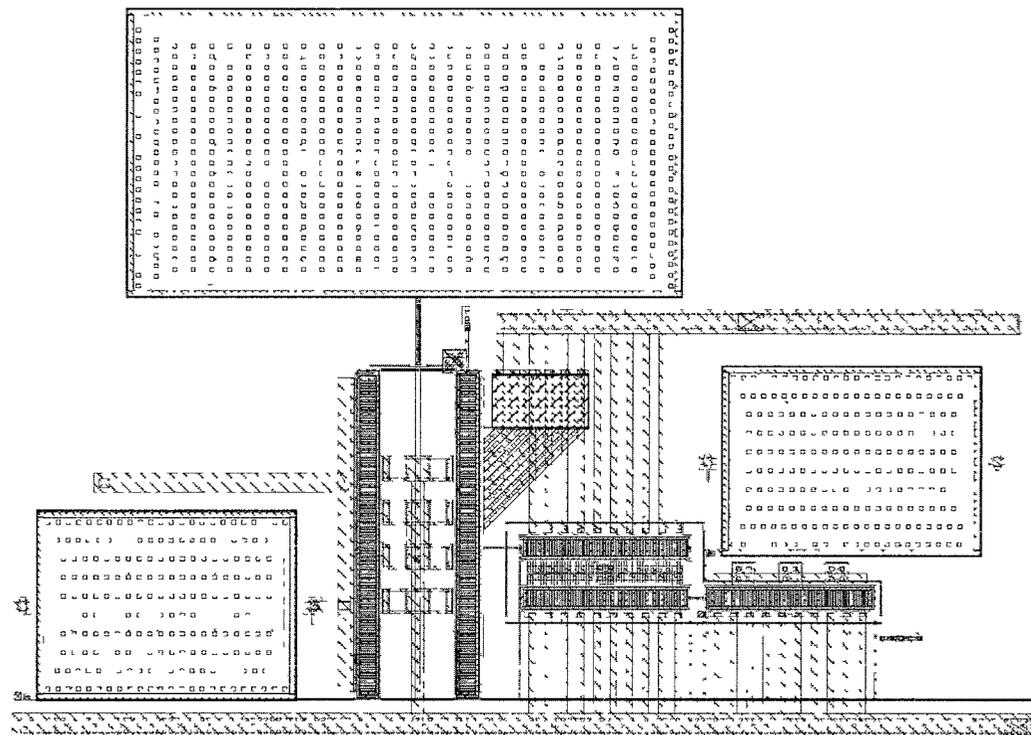


Figure 5.2: Layout of the LNA circuit

metal fill, electro-static discharge protection and antenna effect.

5.1.1 Resistor model choice

The technology provides up to seven different kinds of resistors with varying sheet resistance, absolute and relative tolerances, with only six kinds of resistors available for any single chip. There are five types of front end of line (FEOL) resistors and two types of back end of line (BEOL) resistors, only one of which can be used for a single chip.

There are six resistors present in the schematic for the low-noise amplifier. They are degeneration resistors on the sources of both the current mirror and primary gain transistor, a feedback resistor for input matching, a DC isolation resistor, a drain resistor and a series output resistor for load matching.

The degeneration resistors use the `kxres` model. A `kxres` is a BEOL thin-film resistor that is on a layer slightly above the top most thin metal (M3). This model was chosen due to the fact that the degeneration resistance is relatively small

(10 Ω) and the `kxres` has the smallest sheet resistance and fairly good absolute and relative tolerances compared to the other available resistors. The relative tolerance is important as the two resistors should be well matched to keep the current through the current source and the gain transistor well matched.

Since the required resistance is so small, four resistors are placed in parallel for each degeneration resistor, for a total of eight resistors. These eight resistors were placed in a common centroid layout to improve matching and tolerance.

The feedback resistor uses the `oprppres` resistor model. The feedback resistor sets the input matching based on the gain of the amplifier. As the input match quality is strongly dependant on the value of the feedback resistor, it should have a high certainty in the absolute value of the resistance in order to achieve the best input matching. For this reason, the resistor type chosen for use as the feedback resistor has the most accurate absolute value across process and temperature variations of the available resistor types.

The drain resistor needs to be able to handle a 10 mA DC current and, since the gain, matching and linearity of the amplifier is dependant on the absolute value of the resistance, it should also have a high absolute tolerance. The `oprppres` has the highest absolute resistance tolerance, and because of the current requirement, a large one was used.

The series output resistor also uses the `oprppres` model. It is required to provide a 500 Ω load on the output of the amplifier and still be able to measure the output with a 50 Ω probe. Again, a good absolute tolerance is required so the best model to use is the `oprppres` model.

The DC feed resistor is a fairly large resistor to isolate the DC bias of the gain transistor from the AC input signal. Since the resistor is large but tolerance is not an issue, the resistor model with the highest sheet resistance was chosen, `oprppres`.

5.1.2 Output de-embedding

Since the output of the amplifier is meant to feed the input of another on-chip component, test results should allow for the effects of the output pad and probe to be

negated. To allow this, extra pads were added to the chip to simulate a short, open and through circuit. The simulated circuits all have the same electro-static discharge (ESD) protection that the output pad has.

5.1.3 DC current handling

As the circuit requires relatively high power for the process, attention was required to ensure that the back end of line traces could withstand the expected current. The width of lines expecting DC current were checked against the design manual's Table 215: Current Limits to ensure that the lines could withstand the expected DC current plus roughly 25%.

5.1.4 Metal fill

In the process used for this chip, there are a total of eight metal layers, split into three types: thin, thick and RF in order of nearest to the substrate to furthest. The thin metals consist of M1, M2 and M3. Next, the thick metals are MQ and MG. Finally, the top-most metal layers are LY, E1 and MA.

Metal fill is required by CMC on the three top-metal layers: MA, E1, LY, in order from top-most to bottom-most. To achieve the required fill, to help with DC current handling, and to help with power line decoupling, a layout cell with MA and LY connected and E1 sandwiched between them was created so that VDD could connect to MA/LY and VSS could connect to E1. Arrays of this cell were spread across the chip where needed.

5.1.5 Electro-static discharge protection

To protect against ESD, all input and output pads, not including VDD or VSS, were connected to a `doublediode` cell that meets the requirements for the human body model (HBM). Smaller diodes that meet the charged-device model (CDM) requirements could have been used but the design would not have passed the design rule check.

Also, VDD and VSS were connected with a clamping circuit to prevent power line spikes from damaging the devices.

5.1.6 Antenna effect

During processing of the metal layers, charge can be accumulated on any piece of floating metal. The charge build-up can be enough to destroy device gates or the metal-insulator-metal capacitors. This is called the antenna effect for which antenna rules were developed to help mitigate.

Since the power lines consist of a large mesh, antenna effect damaging the devices during processing of the top metal layers was a concern. To prevent damage, the power rails connected to any front end of line devices were routed to MA, then down to E1 before being connected to the power line mesh.

5.2 Post-layout Simulations

After the layout was complete, parasitic resistors and capacitors were extracted in order to simulate how layout would affect circuit operation. The extracted view was used to run the post-layout simulations and these post-layout simulations were plotted along with the schematic (pre-layout) simulations to compare changes.

The voltage gain simulation results can be found in Figure 5.3. As can be seen, the post-layout simulations match the pre-layout simulations fairly well with the exceptions of slightly higher low-frequency gain and slightly lower high-frequency gain than the pre-layout simulations. This results in a maximum pass-band variation of about 1.7 dB.

The post-layout noise figure simulations show an improvement over the pre-layout simulations, particularly at low frequencies. This can be seen in Figure 5.4. The result is that the noise figure remains below 4 dB and reaches a minimum below 2 dB.

The input matching of the post-layout simulation can be found in Figure 5.5. It can be seen that the input matching quality has been degraded from the schematic simulation with the return loss being as low as 0.25 dB and only reaching as high 9 dB. This degradation is caused by the addition of the parasitic resistance and capacitance and a significant portion of the degradation is caused by the parasitics in the feedback path, due to the Miller effect increasing impedance in proportion to the amplification across it. This has been confirmed in simulations by adding series resistance and capacitance to ground in the pre-layout schematic with results more

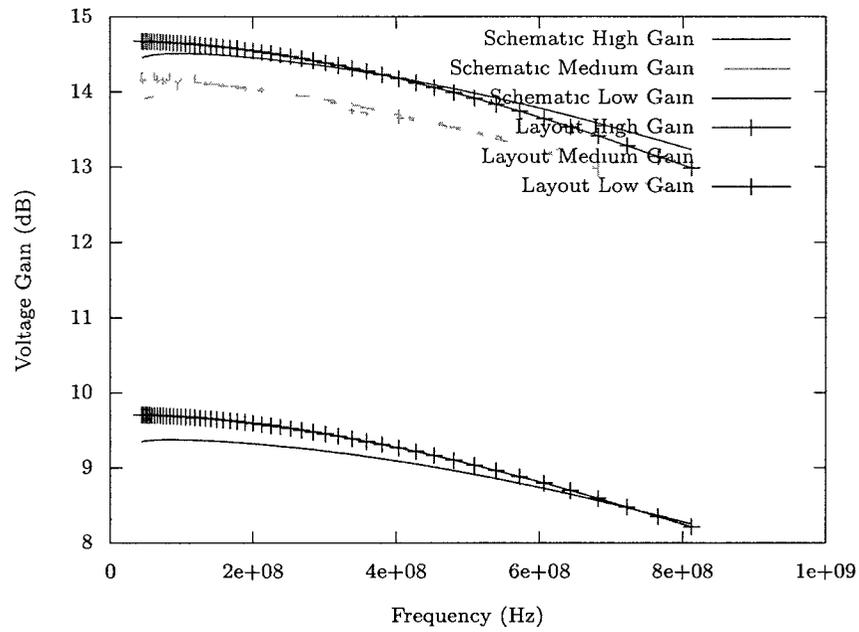


Figure 5.3: Voltage gain of simulated schematic and layout

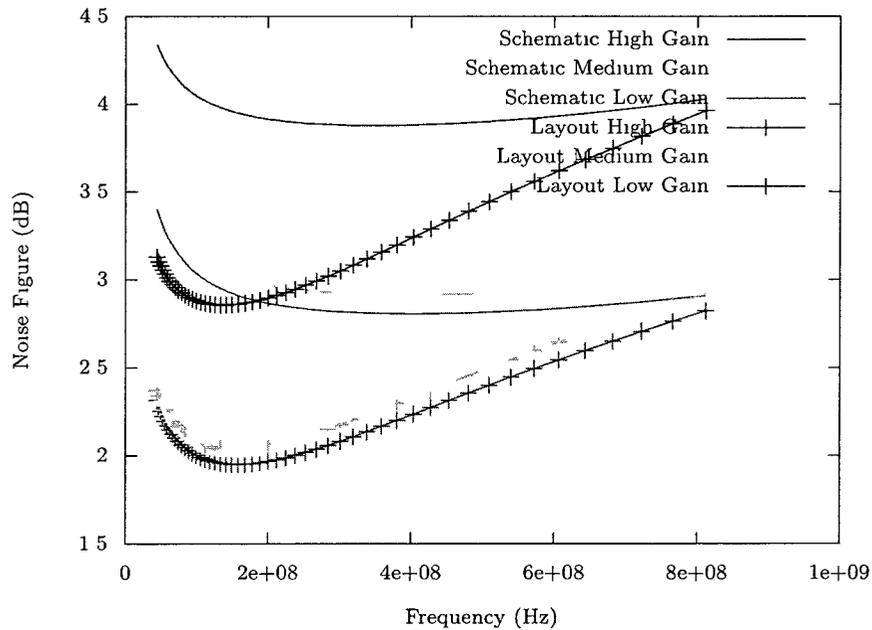


Figure 5.4: Noise figure of simulated schematic and layout

closely matching the post-layout simulations.

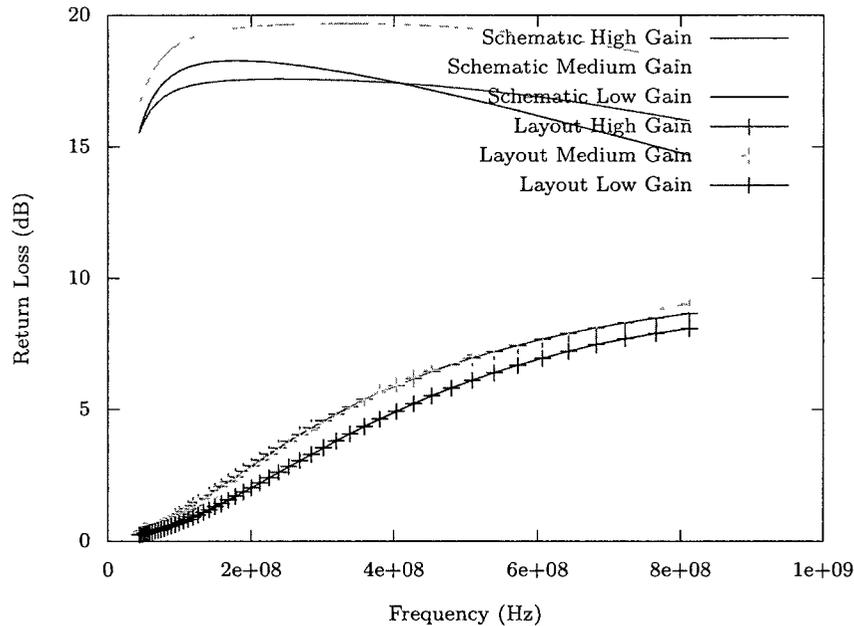


Figure 5.5: Return loss of simulated schematic and layout

A comparison of the pre- and post-layout output impedance simulations can be found in Figure 5.6. The post-layout output impedance is higher than the pre-layout output impedance, with a maximum of 16.8Ω and a minimum of 12.6Ω . Although the output impedance is higher than originally intended, it is still much lower than the intended load impedance so should pose minimal negative performance effects.

The linearity of the pre- and post-layout simulations is measured with third-order intercept points, the values of which can be found in Table 5.1. In general, the OIP_3 points for the post-layout simulations are very near those of the pre-layout simulations but the IIP_3 points are about 2 dB lower. This suggests that the power gain of the layout circuit is higher than that of the schematic circuit.

5.3 Conclusion

Based on the pre- and post-layout simulation results, the layout was successful. The input power matching has deteriorated to the point that input is no longer matched

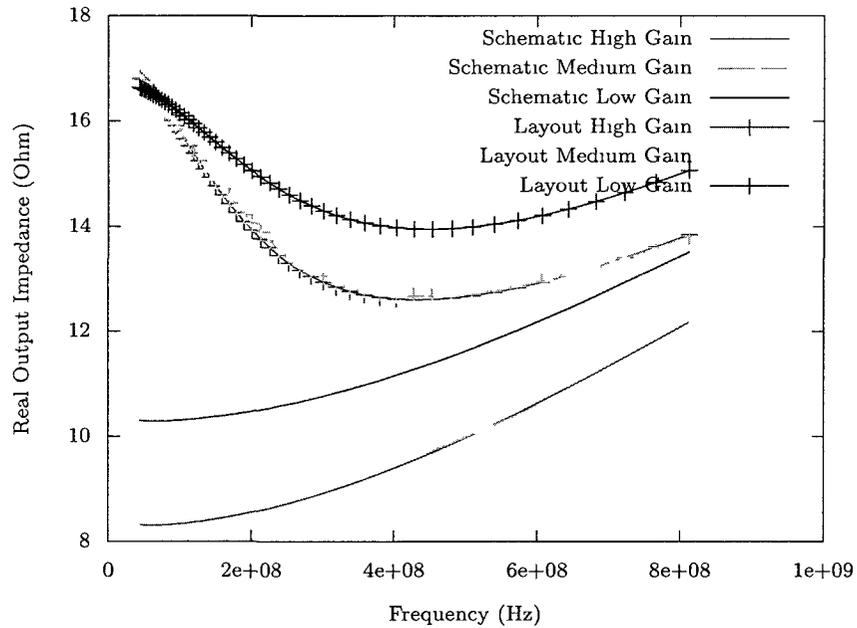


Figure 5.6: Real output impedance of simulated schematic

Table 5.1: IP_3 points of simulated schematic and layout

Gain Setting	Schematic		Layout	
	Input (dBm)	Output (dBm)	Input (dBm)	Output (dBm)
High	8.0137	12.653	6.7114	12.3397
Medium	7.6125	12.0408	6.5529	12.0931
Low	1.7765	3.4100	2.8182	5.5622

to $75\ \Omega$. This was discovered after the design was sent for fabrication but could be fixed by reducing the value of the feedback resistor in order to account for parasitic resistance in the feedback path. The pass-band gain variation has also deteriorated and increased from 1.3 dB in pre-layout simulations to 1.7 dB in the post-layout simulations. There is also a slight deterioration in the linearity, as measured by the input third-order intercept point, which dropped by roughly 2 dBm to a maximum of 6.7 dBm. Noise figure, on the other hand has improved so that maximum noise figure is below 4 dBm and, at high gain, is below 2.8 dBm.

Chapter 6

Testing

The testing was performed on the fabricated chip. A micrograph of the chip can be found in Figure 6.1. The low-impedance output on the micrograph is a pin directly connected to the output of the buffer stage. The high-impedance output pin is connected to a $450\ \Omega$ resistor in series with the output of the buffer stage. This allows linearity to be measured with a $500\ \Omega$ load while leaving the option to accurately measure the buffer stage output impedance. Only one output is measured at a time while the other output pin is left disconnected.

6.1 Equipment used

The following equipment was used for testing:

- HP 8975A Noise Figure Meter (10 MHz–26.5 GHz)
- HP 8722ES S-Parameter Network Analyzer w/Time Domain (50 MHz–40 GHz)
- HP 8595A Spectrum Analyzer (9 kHz–6.5 GHz)
- HP 83640B Frequency Synthesizer (10 MHz–40 GHz)
- Rohde & Schwarz Signal Generator SME06 (5 kHz–6.06 GHz)

6.2 Test setup

The testing of the chip was performed in the Faraday cage at Carleton University using the equipment provided. The measurement setups and results are described

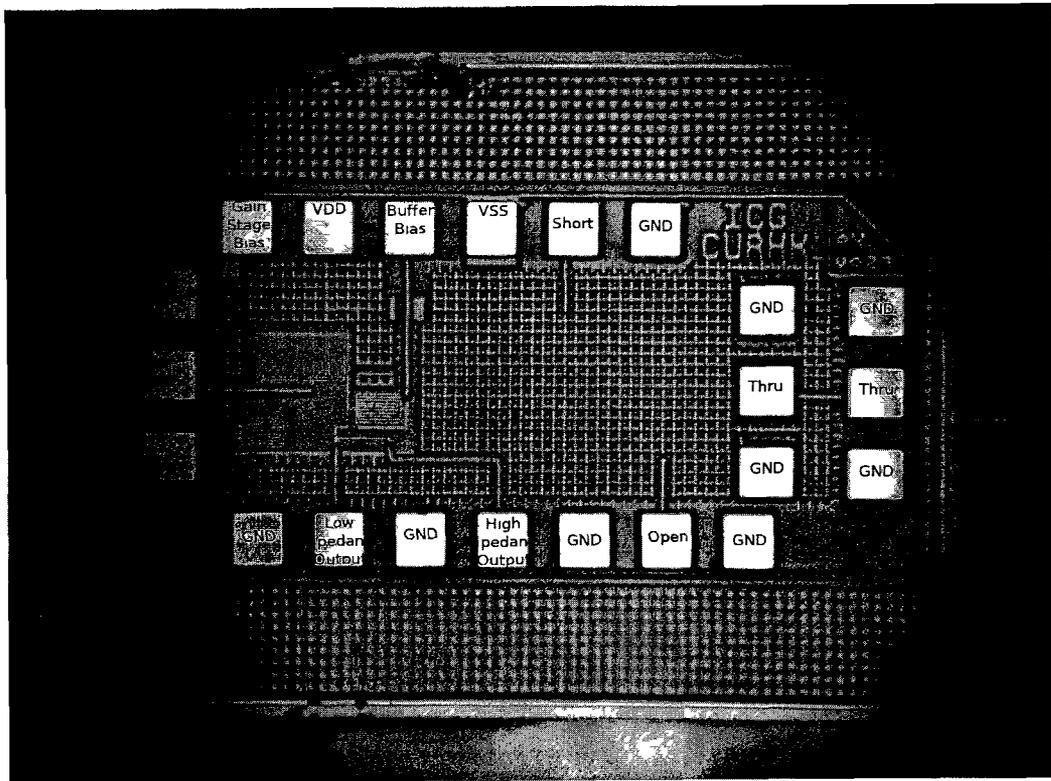


Figure 6.1: Micrograph of fabricated LNA measuring 0.7×1.4 mm

in the following section and compared against simulated results. The simulations were setup in such a way as to mimic the test environment as closely as possible; the simulations used $50\ \Omega$ ports, for example, but did not simulate the probes or cables.

6.2.1 Gain and noise figure

The noise figure and gain were measured using the HP 8957A at high, medium and low gain. The power consumption for each of these gain modes was also measured, a summary of which can be found in Table 6.1. Also, noise figure and gain were both measured using a $50\ \Omega$ load attached sequentially to the low-impedance and high-impedance outputs of the low-noise amplifier (LNA). The noise figure for the low-impedance output can be found in Figure 6.2 and the noise figure for the high-impedance output can be found in Figure 6.3. The measured gain for the low-impedance and high-impedance outputs can be found in Figures 6.4 and 6.5, respectively. The $50\ \Omega$ outputs are measured from the output of the LNA buffer whereas the $500\ \Omega$ outputs are measured with an on-chip $450\ \Omega$ resistor placed in series with the LNA buffer. It should be noted that all of the measurements are compared to post-layout simulations that use $50\ \Omega$ probes to simulate the measurement environment and to ensure a fair comparison between the two.

Table 6.1: Summary of measured power consumption

Gain setting	Measured power (mW)
High	62.0
Medium	44.6
Low	41.8

From the figures, it can be seen that the gain measurements match the simulations fairly well, but have an erratic frequency response, as opposed to the smooth frequency response of the simulations. The noise figure also displays this erratic frequency response but matches the simulation poorly, with the closest matching still having a difference of about 6 dB.

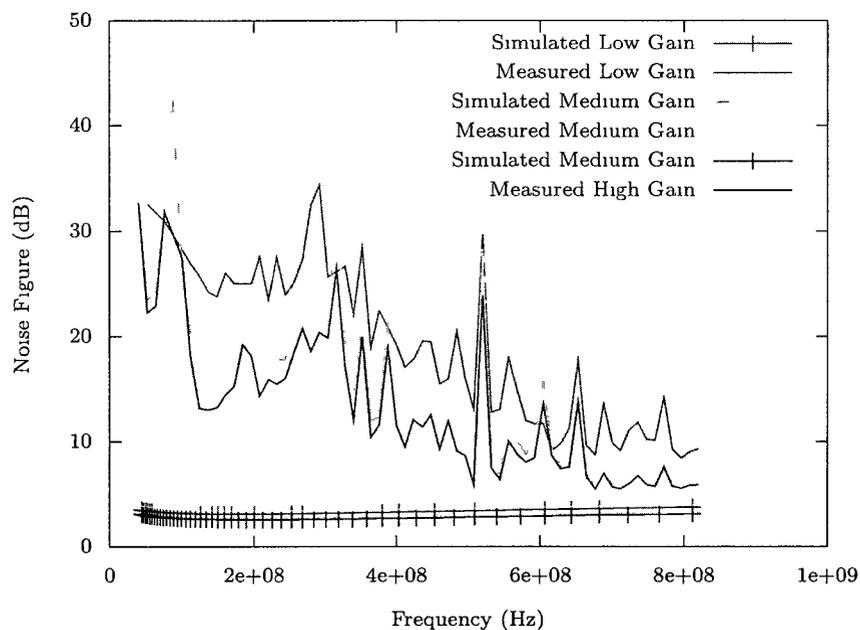


Figure 6.2: Measured and simulated noise figures with $50\ \Omega$ load for low, medium and high gain modes

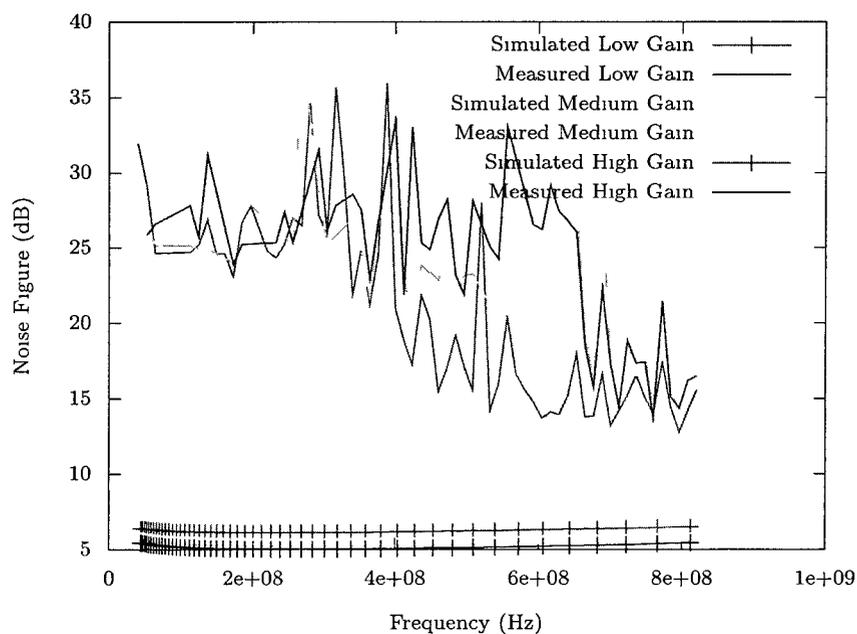


Figure 6.3: Measured and simulated noise figures with $500\ \Omega$ load for low, medium and high gain modes

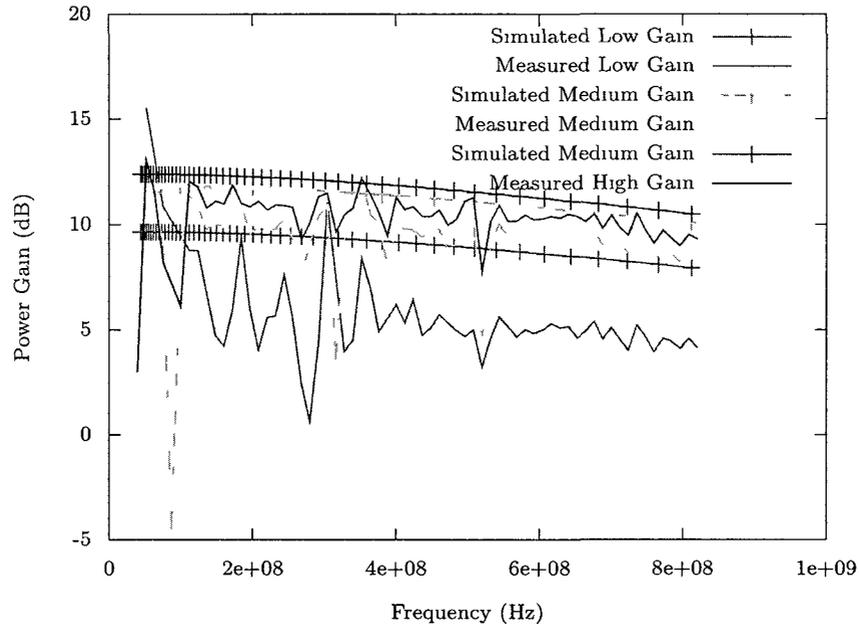


Figure 6.4: Measured and simulated gains with 50Ω load for low, medium and high gain modes

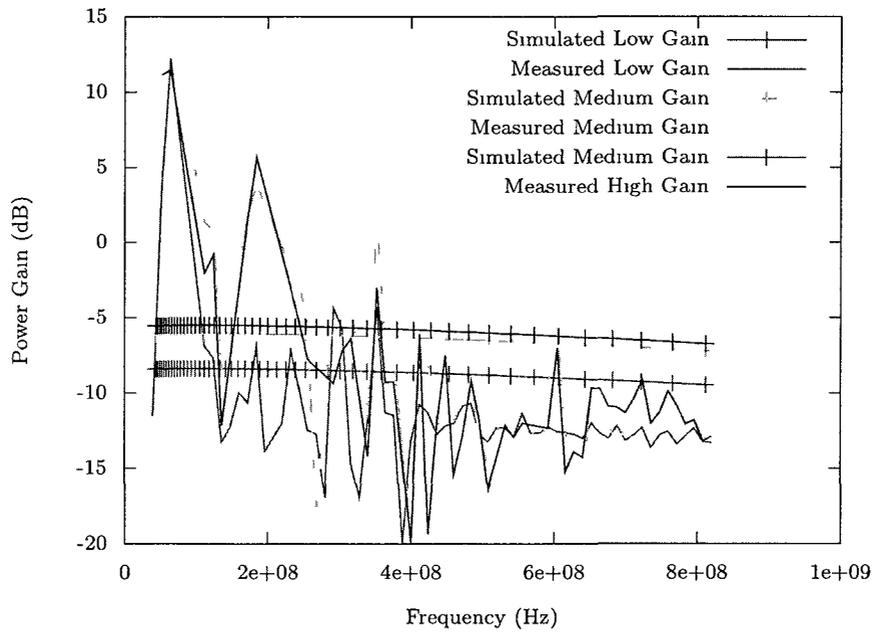


Figure 6.5: Measured and simulated gains with 500Ω load for low, medium and high gain modes

6.2.2 Scattering parameters

The scattering parameters were measured using the vector network analyzer (VNA). The VNA was calibrated using the supplied 3.5 mm calibration kit and not the substrate calibration kit as calibration using the substrate kit produced results that were untrustworthy, potentially due to the substrate kit seeming to be damaged. The measured plot of the input matching can be found in Figure 6.6 and the measured power gain is plotted in Figure 6.7. The measured output impedance and reverse isolation can be found in Figures 6.8 and 6.9, respectively.

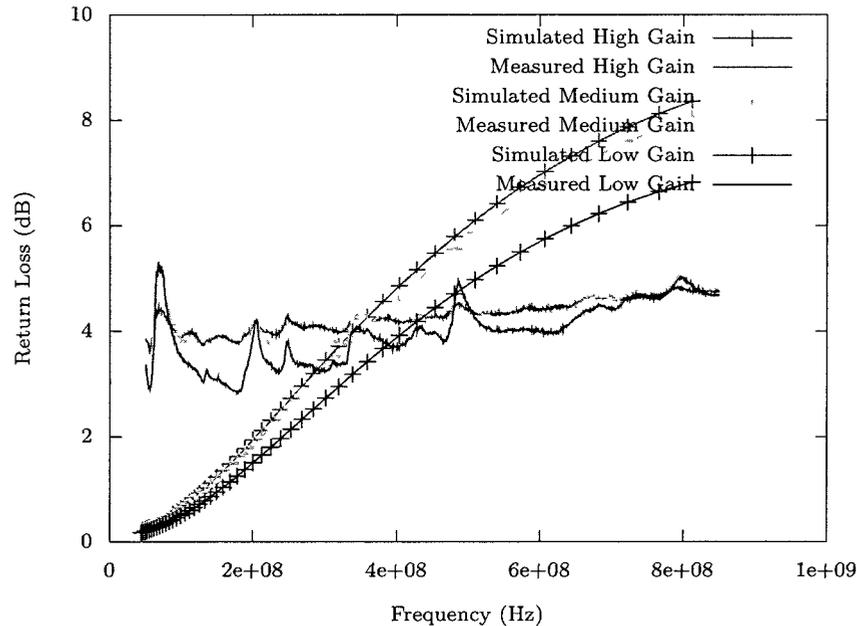


Figure 6.6: Measured and simulated results for input return loss for low, medium and high gain modes

As seen in the figures, the VNA measurements have very little resemblance to the simulated results. These differences are probably the result of the RF probes' impedances not being included in either the simulations or the VNA calibration. The RF probes probably have a measurable resistance and inductance that would change the apparent input and output impedances of the LNA, as measured by the VNA. This would result in the VNA not making accurate measurements of the LNA if they were

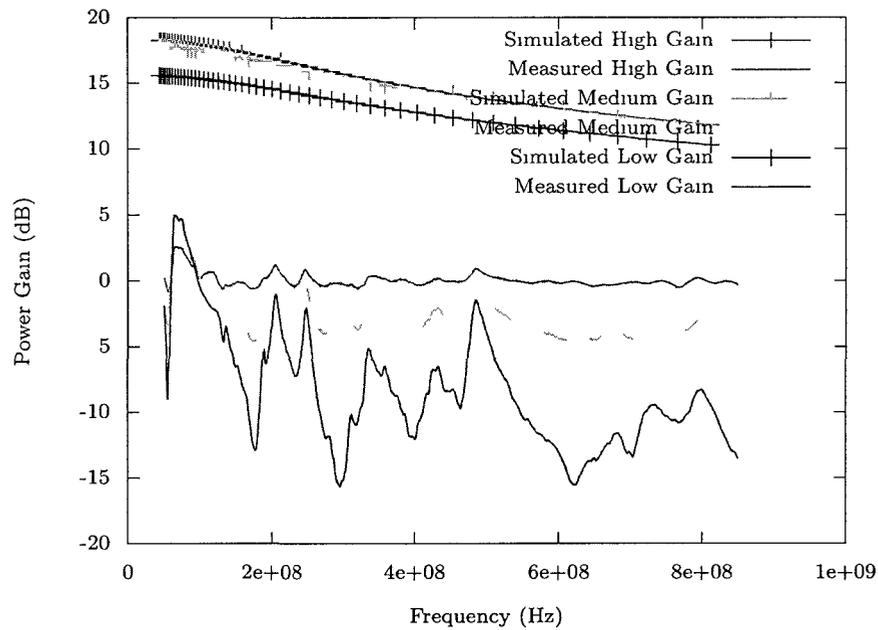


Figure 6.7: Measured and simulated results for forward power gain for low, medium and high gain modes

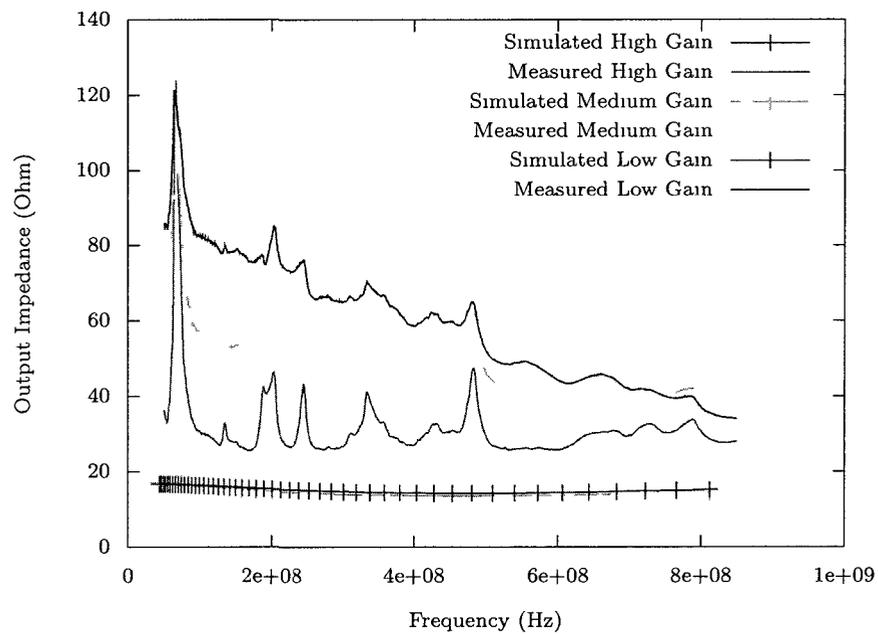


Figure 6.8: Measured and simulated results for output resistance for low, medium and high gain modes

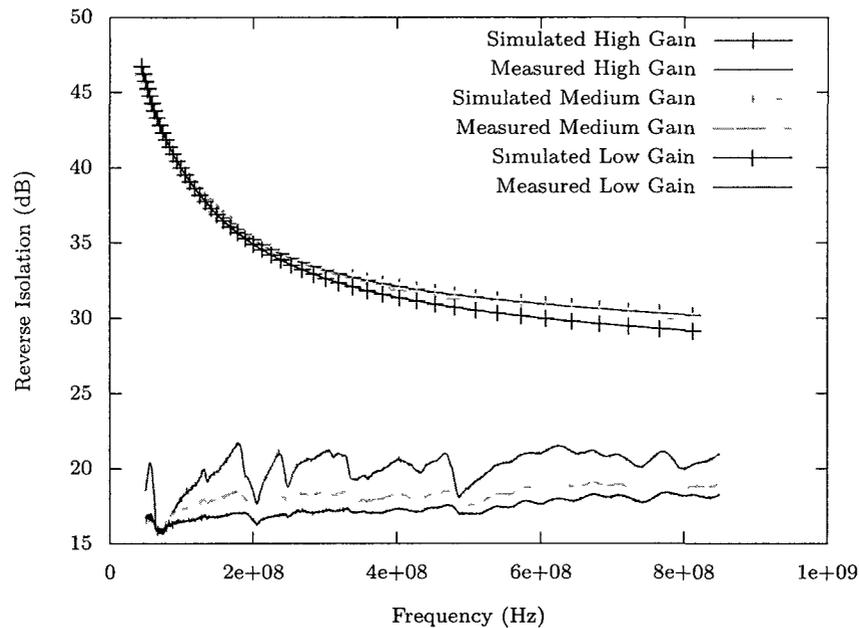


Figure 6.9: Measured and simulated results for reverse isolation for low, medium and high gain modes

not calibrated for.

6.2.3 Intermodulation points

The input intermodulation points were measured using two signal generators, power-splitter, and spectrum analyzer. The second signal generator was used to generate the second tone required for intermodulation tests. The tone pair was set to represent adjacent channels and were 500 MHz and 506 MHz. The output power for first- and third-order components were measured for various input power levels at high gain, medium gain and low gain which were plotted in Figure 6.10, Figure 6.11 and Figure 6.12, respectively. The IIP_3 points were measured from these plots and can be found in Table 6.2, compared against the simulated points.

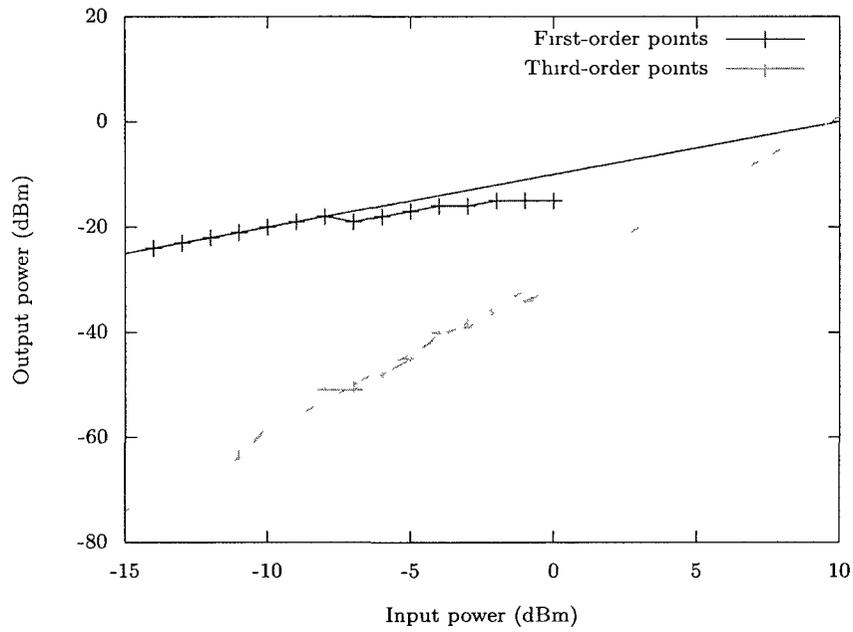


Figure 6.10: Measured third-order intermodulation curve for high-gain setting

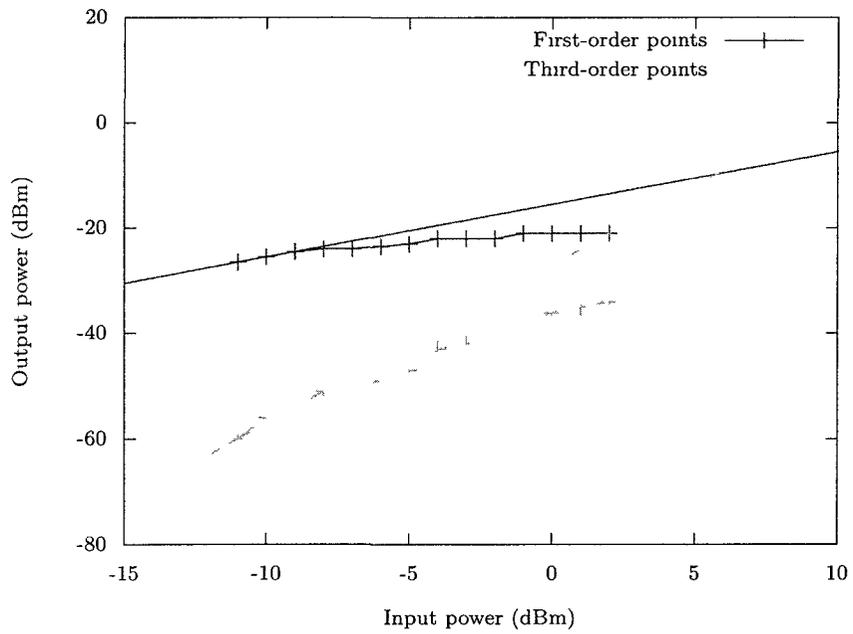


Figure 6.11: Measured third-order intermodulation curve for medium-gain setting

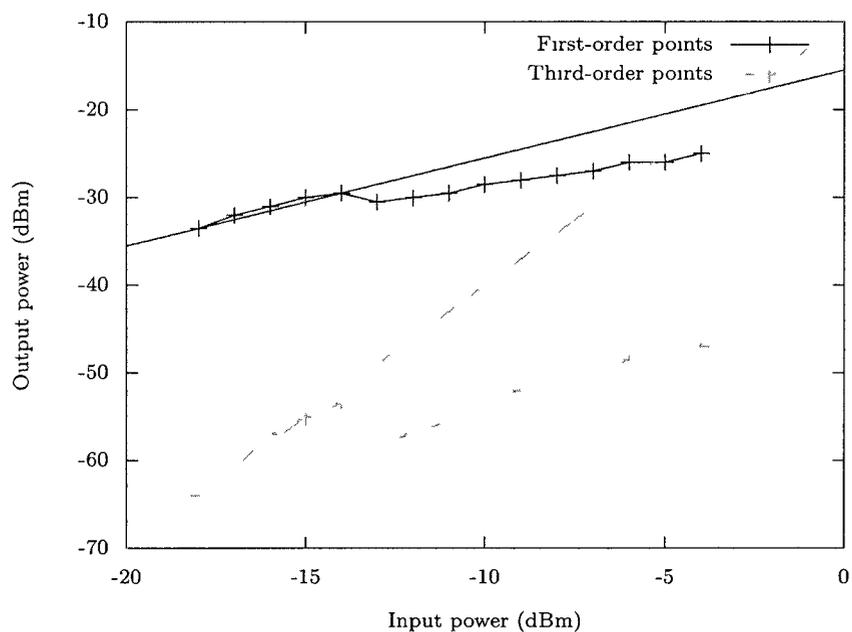


Figure 6.12: Measured third-order intermodulation curve for low-gain setting

Table 6.2: Simulated and measured third-order input intercept points

Gain stage current (mA)	Simulated IIP_3 (dBm)	Measured IIP_3 (dBm)
8.0	7.744941	9.5
5.0	7.281352	5.75
2.0	4.239876	-2.75

6.3 Testing conclusions

As shown in the previous sections, the LNA measurements do not perfectly match the simulations but this is not entirely unexpected. The simulations do take into account many parasitics in the layout and test setup but are missing many more sources of error related to the test setup such as cable loss and probe resistance and inductance, which were not accounted for by the VNA due to calibrating without using a substrate calibration kit.

Simulations were performed after testing in order to try to account for some of the discrepancies. Possible causes that were investigated include oscillation, process variations, parasitics in the radio frequency (RF) probes and parasitics in the DC probes. The simulations and results for each investigation are described in the following paragraphs.

Oscillation simulations were performed to determine whether the circuit might be oscillating and under what conditions it might oscillate. The simulations showed that the amplifier is stable across process corners for expected load conditions. The amplifier is potentially unstable for very large ($> 1 \mu\text{H}$) source and load inductances or very large ($> 1 \text{k}\Omega$) source and load resistances around 1 MHz. These conditions are not expected to have occurred during testing so it is unlikely that oscillations were the cause of the discrepancies in results between testing and simulation.

The circuit was also simulated across process corners. While process corners did affect the performance of the circuit, the effects were not significant enough to be deemed a primary factor in the discrepancies between the simulations and measurements. Process variations also do not significantly affect the stability of the circuit.

Parasitics in the RF probes were modelled as a resistance and inductance in series with the source and load. The values for each were varied in order to attempt to match simulations to the measurements. Series resistances up to 10Ω and series inductances up to 10nH were simulated but did not produce results that were comparable to the measurements. These maximum values were chosen as they should be well above the range of normally operating probes and therefore present an indication of the maximum degradation that may be caused.

Parasitics in the DC probes were modelled similarly to the RF ones with series resistance and inductance. Again, simulations for multiple values of resistance and inductance were run but none show the characteristics of the measured results.

Based on these simulation results, it would be difficult to attribute any discrepancies to oscillations, process variations or parasitics in the probes. Given this, the most likely conclusion that can be drawn is that the measurement setup was flawed in some way. It is possible that one of the cables used to make the measurements was damaged and presented undue noise or signal loss.

Chapter 7

Future Work

As discussed in Chapter 4, the proposed low-noise amplifier (LNA) does not meet the requirements defined in Chapter 3. A number of issues must be addressed in order to successfully design and implement a complete television tuner on a chip. These include linearity, noise, and filtering. The following sections will outline methods that can be employed to address these issues.

7.1 Addressing linearity

For starters, a single wideband amplifier that is able to cover the entire input range with a low noise figure is likely not feasible at this technology node as the linearity required is difficult to achieve without the use of passive attenuators before the LNA. Passive pre-attenuation would increase the linearity at the expense of noise figure. Another method to address the low-linearity of the LNA is to split the input band into multiple sub-bands with off-chip filters.

7.1.1 Pre-attenuation to increase linearity

Pre-attenuation can be used to increase the input-referred linearity of the amplifier as the signal power level at the input of the amplifier is reduced by the value of the attenuation. Assuming that the attenuator is perfectly linear, which is not far from reality if fairly linear passive components are used, the overall output-referred linearity will remain constant for all values of pre-attenuations. The net effect is that the input-referred linearity increases as the overall gain decreases. According to (3.11) and (3.13), the IIP_2 will increase by the attenuation, in dB and the IIP_3 will increase

by twice the attenuation, in dB.

The drawback of this technique is that noise figure of the receiver increases due to Friis formula. In fact, the noise figure of the receiver increases by the value of the attenuation.

The increase in noise figure can be mitigated somewhat by using a variable attenuator. The attenuation can be set to minimum when the signal is low and noise figure must be low to ensure proper demodulation of the signal. As the signal increases, the attenuation can increase so as to maintain the signal above a minimum level, determined by the noise floor, but below a maximum level, determined by the level of the distortion products.

7.1.2 Band-splitting to decrease linearity requirements

The receiver described in [21] uses a technique to split a wide input bandwidth into smaller sub-bands and employs two off-chip inductors feeding two, separate on-chip amplifiers. The on-chip amplifiers are tuned to the desired band with shunt capacitors. Four bands can be selected for each amplifier as there are two parallel shunt capacitors for each that can be activated by on-chip switches. This splits the 300–800 MHz input range into eight separate, selectable bands. However, this receiver does not employ input matching, which is required for a cable receiver.

Increasing the number of bands increases the number of off-chip components and the number pins required for the chip, so it drives up the cost of the system. Therefore, there is a trade-off between the number of sub-bands and required linearity of the input amplifiers that can be optimized to reduce cost. On-chip band splitting is possible but requires the use of very large inductors due to the relatively low frequency of operation which is prohibitively expensive. Thus, the band splitting will require some use of off-chip components.

The composite second-order (CSO) and composite triple-beat (CTB) can be calculated from (3.4) and (3.2), respectively. From these equations and (3.5), we can see that the CTB is dependant on the number of channels whereas the CSO is dependant on both the number of channels and the frequency of the channels. It can be shown that $0 < N_B < N - 1$. For a large number of channels and a low ratio between the lower band-edge and the channel bandwidth, N_B is closer to $N - 1$. Conversely, for a small number of signals or a high ratio between the lower band-edge and the channel bandwidth, N_B approaches zero. The equation for N_B can be re-arranged as in (7.1)

to better reflect these approximations.

$$N_B = (N - 1) \left(1 - \frac{f_L}{NB} \right) \quad (7.1)$$

Based on the equations for CSO and CTB, we can see that to minimize IIP₂ and IIP₃ requirements, the input frequency band should be split into sub-bands of equal number of channels. This will result in having slightly relaxed IIP₂ requirements for the higher sub-band front-ends but the required IIP₃ will be constant for each sub-band front-end. The required IIP₂ and IIP₃ by the system specification given in Chapter 3 for different numbers of sub-bands is tabulated in Table 7.1. As can be seen, each doubling of sub-bands, or halving of the number of carriers, reduces the required IIP₃ by 3 dBm. The relationship between IIP₂ and the number of carriers is not as simple but the trend is a reduction in IIP₂ requirement with a corresponding increase in the number of sub-bands.

Number of sub-bands	Number of carriers	IIP ₂ (dBm)	IIP ₃ (dBm)
2	61	26.3	7.4
3	41	24.2	5.6
4	31	22.5	4.4
6	21	19.8	2.6
8	16	17.4	1.4

Table 7.1: Required IIP₂ and IIP₃ for different numbers of sub-bands

7.2 Addressing filtering

Filtering is an issue that can greatly affect the linearity but has heretofore mostly been ignored as on-chip filtering could comprise an entire research project on its own. The three most common methods of implementing on-chip, analog filtering are active resistor–capacitor (R – C), transconductor–capacitor (g_m – C) and switched capacitors.

Active R – C filters employ resistors, capacitors and operational amplifiers (opamp) in order to make integrators and differentiators using feedback that can implement arbitrary transfer functions. With the use of highly linear passive components in the

feedback path, these filters can achieve high linearity. The pole locations are set by R - C ratios, which can vary greatly on-chip. This can be mitigated somewhat by using tunable components and self-tuning circuits, which negatively affect the linearity and power consumption. Additionally, the frequencies over which these filters can be used is limited by the gain-bandwidth product of the opamps.

The g_m - C filters are based around the use of a combination of transconductors and capacitors to form either integrator-based loops or gyrators, to approximate high- Q inductors. Integrator-based g_m - C loops are similar to active R - C filters except that the integrators use transconductors as opposed to opamps. Gyrators and capacitors can be used to approximate L - C ladder filters. Transconductors are known for their high frequency of operation. In fact, transconductors can operate at frequencies up to the unity transconductance frequency. In both filter-types, the pole locations are set by g_m - C ratios which vary greatly with process, supply voltage and temperature (PVT) variations. Pole locations can be tuned relatively easily by adjusting the transconductance of the transconductance (g_m) elements, but these automatic tuning circuits require additional power and chip area. Additionally, transconductors have fairly low linearity and special attention must be paid to increase the linearity.

Switched-capacitors filters address the lack of precision in pole locations of both the active R - C and g_m - C filter types by using precisely-timed switches and capacitors to approximate a resistor. These synthesized resistors are used in active R - C networks to replace the resistors. This way, pole locations are set by ratios of capacitors, the values of which are strongly correlated, and frequencies, which can be set quite accurately by crystal oscillators and phased-locked loops. Switched-capacitor filters, however, suffer from the limited bandwidth of the opamps used.

7.2.1 Charge-sampling architecture

Recently, a new technique has been introduced [22–25] which aims to address the issues of low frequency of operation of switched-capacitor filters and imprecision of g_m - C filters by, effectively, combining the two techniques. Charge-sampling filters employ transconductors followed by precisely clocked switches to integrate charge onto a capacitor. The transconductors can be implemented as passive resistors at low frequencies to achieve high linearity or can be implemented as transconducting amplifiers to achieve a high frequency of operation. A very brief overview of these receivers follows but much detail is omitted as it could consist of a thesis in and of

itself. Indeed, charge-sampling architectures have already been the subject of at least one PhD thesis [26].

In a charge-sampling filter, an input voltage signal is converted into a current signal which is integrated onto a load capacitor selected by a network of switches. After the integration is complete and the load capacitor is sampled, the capacitor can be reset, in the case of a finite impulse response (FIR) filter, or connected to another sampling capacitor, in the case of an infinite impulse response (IIR) filter. In either case, there are two responses present at the output: a discrete-time response, determined by the sampling rate of the switches and the ratio of the sampling capacitor values; and a continuous-time sinus cardinalis (sinc) response with zeros at integer multiples the sampling frequency. This continuous-time sinc response acts as a built-in anti-aliasing filter and clock rejection filter as multiples of the clock frequency fall on zeros of the frequency response. In addition to the filtering function, these charge-sampling architectures can also perform frequency conversion by decimating (down-conversion) or interpolating (up-conversion). It is important to note that filtering can be performed prior to or during the down-conversion, thus greatly reducing the linearity requirements of the “mixer” and sampler.

The bulk of the research into such charge-sampling architectures so far has focused on direct-conversion reconfigurable receivers [21, 23, 27, 28]. In these receivers, the input signal sampled at a multiple of the carrier frequency and then decimated, usually by a power of two, by the next set of switches and capacitors which are clocked at a frequency which is an integer divisor of the input sampling frequency. The signal passes through multiple such stages until the frequency response of the receiver matches the required frequency mask and only the desired channel remains, centred at DC. These receivers face many of the same issues as commonly associated with direct-conversion architectures, namely, static DC offset, $1/f$ noise and dynamic DC offsets caused by even-order distortion and self-mixing.

To address the issues associated with direct-conversion architectures, research has started to move into low intermediate frequency (IF) architectures [24, 29]. In these cases, the input sampling frequency is chosen so that when the input signal is decimated, it will not down-sample to DC but to a frequency slightly offset to avoid the bulk of the $1/f$ noise and allow DC offset problems to be eliminated with capacitive coupling. This all comes at a cost, however, as an image frequency is now present and must be filtered out prior to down-conversion or cancelled by using image-rejection

techniques, such as in-phase and quadrature-phase (I/Q) mixing.

Image rejections becomes less of an issue as the intermediate frequency increases and the separation between the desired signal and the image signal increases. As the separation between the desired signal and the image increases, filtering the image signal becomes much easier. Such an architecture is similar to the classic super-heterodyne radio and has been described in a number of publications [26,30,31]. The ability to choose multiple intermediate frequencies gives the system architect a great flexibility by allowing successively lower intermediate frequencies to be chosen so that the image frequency for the following down-conversion is relatively easy to filter. All of this flexibility comes at a cost as each IF adds to the potential mixing products and must be chosen carefully to ensure that the effects of mixing products do not overwhelm the desired signal.

It is clear the charge-sampling radios can offer some important benefits to a fully-integrated television receiver and also offer an interesting research area. For this reason, it is recommended to focus on a charge-sampling architecture and, specifically, a transconducting amplifier to perform the low-noise amplification.

7.3 Addressing noise

As discussed in Section 2.1.3, noise cancelling techniques must be investigated in order to achieve a sub-3 dB noise figure and an input power match. Additionally, in order to capitalize on the use of the charge-sampling receiver, the first amplifier in the receiver chain should be a low-noise transconducting amplifier (LNTA). Two potential LNTAs are discussed in the following section: the gain-boosted common-gate amplifier and the common-gate-common-source active balun.

7.3.1 Gain-boosted common-gate amplifier

An example schematic of the gain-boosted common-gate amplifier can be found in Figure 7.1. Note that in an actual implementation, M_1 and M_2 would likely be cascoded MOSFETs in order to increase the gain-bandwidth product and increase linearity. The input impedance is calculated in (7.2). The transconductance gain of the amplifier is calculated in (7.3). Based on the previous calculations and assuming a matched input and large loop gain, the minimum noise factor can be estimated in (7.4) to be

greater than $1 + \frac{1}{2}\text{NEF}$, or roughly 1.8 dB for a noise excess factor (NEF) of 1, which is a fairly liberal estimate for sub-micron CMOS technologies.

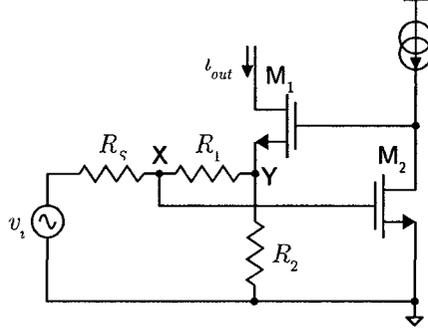


Figure 7.1: Example schematic of a gain-boosted common-gate transconducting amplifier

$$\begin{aligned}
 g_{m,\text{eqv}} &= -g_{m1}g_{m2}r_{o2} \\
 i_{\text{out}} &= g_{m,\text{eqv}}v_X \\
 \frac{i_{\text{in}}}{v_X} &= \frac{1 - R_2g_{m,\text{eqv}}}{\left(1 + \frac{R_2}{R_1}\right)R_1} \\
 Z_{\text{in}} &= \frac{v_X}{i_{\text{in}}} = R_S \\
 &= \frac{R_1 + R_2}{1 + g_{m1}g_{m2}r_{o2}R_2} \\
 &\approx \frac{R_1 + R_2}{g_{m1}g_{m2}r_{o2}R_2}
 \end{aligned} \tag{7.2}$$

$$\begin{aligned}
 i_{\text{out}} &= -v_Xg_{m1}g_{m2}r_{o2} \\
 v_X &= \frac{1}{2}v_i \\
 G_m &= \frac{-1}{2}g_{m1}g_{m2}r_{o2}
 \end{aligned} \tag{7.3}$$

$$\begin{aligned}
i_{n,\text{out}} &= G_m v_{n,S} + i_{n,R1} + i_{n,R2} + i_{n,M1} - i_{n,M1} \frac{R_2 R_S}{R_1 + R_S + R_2} g_{m1} g_{m2} r_{o2} + i_{n,M2} r_{o2} g_{m1} \\
&\approx G_m v_{n,S} + i_{n,M1} \left(1 - \frac{g_{m1} g_{m2} r_{o2} R_2}{2g_{m1} g_{m2} r_{o2} R_2 + 2} \right) \\
F &> 1 + \frac{\text{NEF}}{2}
\end{aligned} \tag{7.4}$$

It appears that this topology for a LNTA can achieve a fairly low noise figure and may prove useful in a charge-sampling receiver. A theoretical linearity analysis should be completed for this circuit to determine if there are any opportunities for distortion cancelling with this circuit. Additionally, while this circuit can implement variable gain by steering the output current, there is no obvious method to directly trade-off noise with linearity while maintaining a proper input match.

7.3.2 Common-gate–common-source active balun

This amplifier is described with noise and distortion cancelling in [32–34]. An example schematic of this circuit can be found in Figure 7.2. A full analysis of the noise and distortion cancelling can be found in [32]. Each branch has equal but opposite voltage gain but the common-source branch is admittance scaled in order to achieve the desired noise figure. The theoretical minimum noise figure appears to be well below 2 dB. Once the transistors have been sized to achieve the desired input match and noise figure, the gate bias can be chosen to minimize distortion. This design is extended by [33, 34] to include an I/Q current-mode switching mixer, modelled in the schematic by the cascode transistors. This current-mode switching mixer acts in a similar way to the switches in a charge-sampling filter act which switch the current from a transconductance device between various loads, albeit, capacitive loads.

This circuit could be directly applied in a charge sampling receiver by adding capacitors across the differential output and more switches to reset the capacitors after sampling, however the output impedance of the transconductors would be somewhat low for this application. To increase the output impedance of the transconductors, the resistive loads could be replaced by current sources or current mirrors. The key

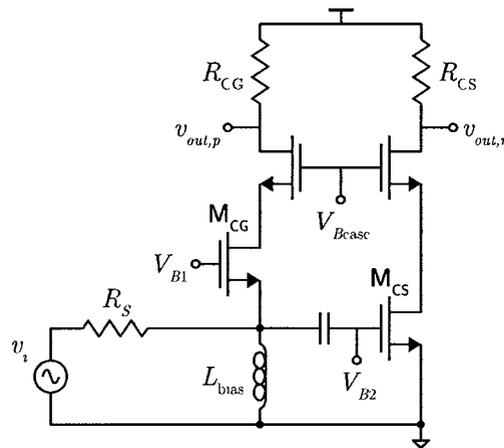


Figure 7.2: An example schematic of a common-gate–common-source active balun

to the input matching and the noise and distortion cancelling is keeping the admittance scaling constant and the output balanced. Indeed, the transconductors can be split into unit transconductors to provide multiple tap coefficient values without any adverse affect to the input matching, or noise and distortion cancellation as long as dummy loads are provided for the unused unit taps.

7.4 Conclusion

It seems that the way forward in investigating fully-integrated television tuners is with a charge-sampling architecture, most likely with at least one IF before a programmable low-pass or band-pass channel-select filter.

The receiver should probably use a common-gate–common-source active balun as the LNTA, in order to reduce the number of pins, reduce the noise figure and increase linearity. An investigation of common-mode feedback (CMFB) and common-mode feed-forward (CMFF) with this amplifier would also be apt as a properly designed CMFB and CMFF circuit should increase the even-order linearity and possibly assist with noise and distortion cancellation, as they are cancelled by being common-mode signals.

The linearity of the active balun LNTA will still likely not be high enough to meet the linearity requirements defined in Chapter 3. To further increase the linearity of the amplifier, the input band should be split into two or three sub-bands with off-chip filters. Further, the linearity at higher input power levels could be increased by

implementing a stepped attenuator before the LNTA.

Further research in this area could potentially lead to publications or patents on highly-linear LNTAs and charge-sampled filters, theoretical noise and linearity calculations of charge-sampled filters which are currently ill-defined, and charge-sampled architecture innovations. A commercial product is also likely, given more investment. With significant design and analysis effort, a highly-integrated digital television (DTV) receiver could be produced.

Chapter 8

Summary and Conclusion

This thesis began as an investigation into spreading our modern communications networks and the information and ideas they carry to an ever wider audience. The hope was to aid in decreasing the cost of television tuners by reducing the linearity requirements of the low-noise amplifier (LNA) and the following components of the tuner.

The issues of noise, power matching and variable gain in wideband LNAs were investigated in Chapter 2. The noise figure of a input power matched sub-micron CMOS LNA is limited to a minimum of about 3 dB without the use of noise cancelling techniques to achieve a simultaneous noise and power match. However, variable gain techniques do not lend themselves to noise cancellation.

The proposed low-noise amplifier (LNA) did not meet the specifications required for the multi-system television receiver outlined in Chapter 3 but it is possible to build a receiver using a combination of the proposed LNA and band pre-filters that will meet the requirements.

Further, a charge-sampling architecture and corresponding transconducting active balun are recommended to be investigated in order to meet the system requirements. Even this is unlikely to meet the system requirements, so the use of band-splitting off-chip filters and stepped attenuators are recommended.

8.1 Original contributions

The main contributions of this thesis are:

- Design of a fully-integrated digital television (DTV) receiver front-end

- Design, simulation and measurement of a variable-gain LNA

8.2 Conclusions drawn

The system specifications appear to be overly ambitious by requiring a single, highly-linear LNA to amplify the entire input band. Instead, the input band should likely be split into two or three sub-bands which can be amplified individually, which will reduce the linearity requirements of the receiver.

The goal of increasing the spread of global communications networks and the information and ideas carried upon them is still achievable through this avenue of research. With additional research and investment in fully-integrated DTV tuners and the suggested areas, a global community of consumers can be reached.

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