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COMPARISON OF OVERSAMPLED SIGMA DELTA MODULATORS
FOR ANALOG TO DIGITAL CONVERSION IN
DIGITAL SUBSCRIBER LOOPS

by

JANET M. DAVIS, B. ENG.

A thesis submitted to the
Faculty of Graduate Studies and Research
in partial fulfilment of the requirements
for the degree of
Master of Engineering

Ottawa-Carleton Institute for Electrical Engineering
Faculty of Engineering
Department of Systems and Computer Engineering
Carleton University

September 1987

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for Analog to Digital Conversion in
Digital Subscriber Loops"

submitted by JANET M. DAVIS, B.Eng., in partial fulfilment
of the requirements for the degree of Master of Engineering

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ABSTRACT

A comparison of simulation results for several oversampled sigma delta modulators is presented. The modulators provide a practical, area efficient solution for fabrication of high performance analog to digital (A/D) converters. The demand for high performance A/D converters has developed with advances in the Integrated Digital Services Network (ISDN) where high speed and accuracy are required for 160 kilobit subscriber loop transmission.

Several variations of oversampled sigma delta modulators are evaluated: those that require multiple integration loops and those that cascade single stage sigma delta modulators to achieve the desired signal to noise ratios.

The simulation results show that for the ideal situation the triple integration sigma delta modulator has the best SNR characteristics, but it was plagued by circuit impairments while the three stage cascaded noise shaping modulator exhibited slightly worse results, but it was far more tolerant of the circuit impairments applied in the simulations.

TABLE OF CONTENTS

1.0	Introduction	1
2.0	Sigma Delta Modulation	5
2.1	Op Amp Realization Considerations	8
3.0	Results of Ideal Case Simulations	12
3.1	MASH-1	12
3.2	SISDM With Four Level Quantization	20
3.3	MASH-2	24
3.4	DISDM	29
3.5	MASH-3	34
3.6	MASH-3 Longo.	41
3.7	TISDM	45
3.8	Summary of Ideal Case Results	51
4.0	Results of Simulations with Impairments	55
4.1	Operational Amplifier Offset	56
4.2	Operational Amplifier Saturation	86
4.3	Limited Op Amp Bandwidth	102
4.4	Feedback Gain Variation	111
4.5	Comparator Input Offset	127
4.6	Comparator Dead Zone	134
5.0	Conclusions and Suggestions for Future Work	142
	Appendix A. The FFT Algorithm	147
	Appendix B. The Blackman-Harris Windowing Function	148
	References	150

LIST OF ILLUSTRATIONS

Figure 1.	Echo Cancellation - Block Diagram	3
Figure 2.	Sigma Delta Modulator (MASH-1)	6
Figure 3.	Model of Operational Amplifier	10
Figure 4.	Obtaining the Specified Values from the Plots	13
Figure 5.	MASH-1 - Circuit Structure	14
Figure 6.	MASH-1 - Power Spectrum	16
Figure 7.	MASH-1 - SNR' Curve	18
Figure 8.	SISDM With Four Level Quantization - Circuit Structure	21
Figure 9.	SISDM With Four Level Quantization - Power Spectrum	22
Figure 10.	SISDM With Four Level Quantization - SNR' Curve	23
Figure 11.	MASH-2 - Circuit Structure	25
Figure 12.	MASH-2 - Power Spectrum	27
Figure 13.	MASH-2 - SNR' Curve	29
Figure 14.	DISDM - Circuit Structure	31
Figure 15.	DISDM - Power Spectrum	32
Figure 16.	DISDM - SNR' Curve	33
Figure 17.	MASH-3 - Circuit Structure	35
Figure 18.	MASH-3 - Power Spectrum	38
Figure 19.	MASH-3 - SNR' Curve	39
Figure 20.	MASH-3 Longo - Circuit Structure	42
Figure 21.	MASH-3 Longo - Power Spectrum	43
Figure 22.	MASH-3 Longo - SNR' Curve	44
Figure 23.	TISDM - Circuit Structure	46
Figure 24.	TISDM - Power Spectrum	48
Figure 25.	TISDM - SNR' Curve	49
Figure 26.	MASH-1 - Power Spectrum with Op Amp Offset at 0.01	63
Figure 27.	MASH-1 - SNR' Curve with Op Amp Offset at 0.01	63
Figure 28.	MASH-1 - Power Spectrum with Op Amp Offset at 0.25	64
Figure 29.	MASH-1 - SNR' Curve with Op Amp Offset at 0.25	64
Figure 30.	MASH-1 - Power Spectrum with Op Amp Offset at 0.5	65
Figure 31.	MASH-1 - SNR' Curve with Op Amp Offset at 0.5	65
Figure 32.	MASH-1 - Power Spectrum with Op Amp Offset at 0.75	66
Figure 33.	MASH-1 - SNR' Curve with Op Amp Offset at 0.75	66
Figure 34.	SISDM 4 Level Quantizer - Power Spectrum with Op Amp Offset at 0.01	67
Figure 35.	SISDM 4 Level Quantizer - SNR' Curve with Op Amp Offset at 0.01	67
Figure 36.	SISDM 4 Level Quantizer - Power Spectrum with Op Amp Offset at 0.25	68
Figure 37.	SISDM 4 Level Quantizer - SNR' Curve with Op Amp Offset at 0.25	68
Figure 38.	SISDM 4 Level Quantizer - Power Spectrum with Op Amp Offset at 0.5	69

Figure 39.	SISDM 4 Level Quantizer - SNR' Curve with Op Amp Offset at 0.5	69
Figure 40.	SISDM 4 Level Quantizer - Power Spectrum with Op Amp Offset at 0.75	70
Figure 41.	SISDM 4 Level Quantizer - SNR' Curve with Op Amp Offset at 0.75	70
Figure 42.	MASH-2 - Power Spectrum with Op Amp Offset at 0.01	71
Figure 43.	MASH-2 - SNR' Curve with Op Amp Offset at 0.01	71
Figure 44.	MASH-2 - Power Spectrum with Op Amp Offset at 0.25	72
Figure 45.	MASH-2 - SNR' Curve with Op Amp Offset at 0.25	72
Figure 46.	MASH-2 - Power Spectrum with Op Amp Offset at 0.5	73
Figure 47.	MASH-2 - SNR' Curve with Op Amp Offset at 0.5	73
Figure 48.	MASH-2 - Power Spectrum with Op Amp Offset at 0.75	74
Figure 49.	MASH-2 - SNR' Curve with Op Amp Offset at 0.75	74
Figure 50.	DISDM - Power Spectrum with Op Amp Offset at 0.01	75
Figure 51.	DISDM - SNR' Curve with Op Amp Offset at 0.01	75
Figure 52.	DISDM - Power Spectrum with Op Amp Offset at 0.25	76
Figure 53.	DISDM - SNR' Curve with Op Amp Offset at 0.25	76
Figure 54.	MASH-3 - Power Spectrum with Op Amp Offset at 0.01	77
Figure 55.	MASH-3 - SNR' Curve with Op Amp Offset at 0.01	77
Figure 56.	MASH-3 - Power Spectrum with Op Amp Offset at 0.25	78
Figure 57.	MASH-3 - SNR' Curve with Op Amp Offset at 0.25	78
Figure 58.	MASH-3 - Power Spectrum with Op Amp Offset at 0.5	79
Figure 59.	MASH-3 - SNR' Curve with Op Amp Offset at 0.5	79
Figure 60.	MASH-3 - Power Spectrum with Op Amp Offset at 0.75	80
Figure 61.	MASH-3 - SNR' Curve with Op Amp Offset at 0.75	80
Figure 62.	MASH-3 Longo - Power Spectrum with Op Amp Offset at 0.01	81
Figure 63.	MASH-3 Longo - SNR' Curve with Op Amp Offset at 0.01	81
Figure 64.	MASH-3 Longo - Power Spectrum with Op Amp Offset at 0.25	82
Figure 65.	MASH-3 Longo - SNR' Curve with Op Amp Offset at 0.25	82
Figure 66.	MASH-3 Longo - Power Spectrum with Op Amp Offset at 0.5	83
Figure 67.	MASH-3 Longo - SNR' Curve with Op Amp Offset at 0.5	83
Figure 68.	MASH-3 Longo - Power Spectrum with Op Amp Offset at 0.75	84
Figure 69.	MASH-3 Longo - SNR' Curve with Op Amp Offset at 0.75	84
Figure 70.	TISDM - Power Spectrum with Op Amp Offset at 0.01	85

Figure 71.	TISDM - SNR' Curve with Op Amp Offset at 0.01	85
Figure 72.	MASH-3 Longo - Op Amp Offset at 0.75 with Input Amplitude at 0.1	86
Figure 73.	MASH-1 - Histogram of Op Amp Outputs	90
Figure 74.	SISDM 4 Level Quantizer - Histogram of Op Amp Outputs	90
Figure 75.	MASH-2 - Histogram of Op Amp Outputs	91
Figure 76.	DISDM - Histogram of Op Amp Outputs	91
Figure 77.	MASH-3 - Histogram of Op Amp Outputs	92
Figure 78.	MASH-3 Longo - Histogram of Op Amp Outputs	92
Figure 79.	TISDM - Histogram of Op Amp Outputs	93
Figure 80.	MASH-1 - Power Spectrum with Op Amp Saturation	95
Figure 81.	MASH-1 - SNR' Curve with Op Amp Saturation	95
Figure 82.	SISDM 4 Level Quantizer - Power Spectrum with Op Amp Saturation	96
Figure 83.	SISDM 4 Level Quantizer - SNR' Curve with Op Amp Saturation	96
Figure 84.	MASH-2 - Power Spectrum with Op Amp Saturation	97
Figure 85.	MASH-2 - SNR' Curve with Op Amp Saturation	97
Figure 86.	DISDM - Power Spectrum with Op Amp Saturation	98
Figure 87.	DISDM - SNR' Curve with Op Amp Saturation	98
Figure 88.	MASH-3 - Power Spectrum with Op Amp Saturation	99
Figure 89.	MASH-3 - SNR' Curve with Op Amp Saturation	99
Figure 90.	MASH-3 Longo - Power Spectrum with Op Amp Saturation	100
Figure 91.	MASH-3 Longo - SNR' Curve with Op Amp Saturation	100
Figure 92.	TISDM - Power Spectrum with Op Amp Saturation	101
Figure 93.	TISDM - SNR' Curve with Op Amp Saturation	101
Figure 94.	MASH-1 - Power Spectrum with Limited Op Amp Bandwidth	105
Figure 95.	MASH-1 - SNR' Curve with Limited Op Amp Bandwidth	105
Figure 96.	MASH-2 - Power Spectrum with Limited Op Amp Bandwidth	106
Figure 97.	MASH-2 - SNR' Curve with Limited Op Amp Bandwidth	106
Figure 98.	DISDM - Power Spectrum with Limited Op Amp Bandwidth	107
Figure 99.	DISDM - SNR' Curve with Limited Op Amp Bandwidth	107
Figure 100.	MASH-3 - Power Spectrum with Limited Op Amp Bandwidth	108
Figure 101.	MASH-3 - SNR' Curve with Limited Op Amp Bandwidth	108
Figure 102.	MASH-3 Longo - Power Spectrum with Limited Op Amp Bandwidth	109
Figure 103.	MASH-3 Longo - SNR' Curve with Limited Op Amp Bandwidth	109
Figure 104.	TISDM - Power Spectrum with Limited Op Amp Bandwidth	110
Figure 105.	TISDM - SNR' Curve with Limited Op Amp Bandwidth	110
Figure 106.	MASH-1 - Power Spectrum with Feedback Gain	

	Variation At 0.25	115
Figure 107.	MASH-1 - SNR' Curve with Feedback Gain Variation At 0.25	115
Figure 108.	SISDM 4 Level Quantizer - Power Spectrum with Feedback Gain Variation At 0.25	116
Figure 109.	SISDM 4 Level Quantizer - SNR' Curve with Feedback Gain Variation At 0.25	116
Figure 110.	MASH-2 - Power Spectrum with Feedback Gain Variation At 0.25	117
Figure 111.	MASH-2 - SNR' Curve with Feedback Gain Variation At 0.25	117
Figure 112.	DISDM - Power Spectrum with Feedback Gain Variation At 0.25	118
Figure 113.	DISDM - SNR' Curve with Feedback Gain Variation At 0.25	118
Figure 114.	MASH-3 - Power Spectrum with Feedback Gain Variation At 0.25	119
Figure 115.	MASH-3 - SNR' Curve with Feedback Gain Variation At 0.25	119
Figure 116.	MASH-3 Longo - Power Spectrum with Feedback Gain Variation At 0.25	120
Figure 117.	MASH-3 Longo - SNR' Curve with Feedback Gain Variation At 0.25	120
Figure 118.	MASH-1 - Power Spectrum with Feedback Gain Variation At 0.5	121
Figure 119.	MASH-1 - SNR' Curve with Feedback Gain Variation At 0.5	121
Figure 120.	SISDM 4 Level Quantizer - Power Spectrum with Feedback Gain Variation At 0.5	122
Figure 121.	SISDM 4 Level Quantizer - SNR' Curve with Feedback Gain Variation At 0.5	122
Figure 122.	MASH-2 - Power Spectrum with Feedback Gain Variation At 0.5	123
Figure 123.	MASH-2 - SNR' Curve with Feedback Gain Variation At 0.5	123
Figure 124.	DISDM - Power Spectrum with Feedback Gain Variation At 1	124
Figure 125.	DISDM - SNR' Curve with Feedback Gain Variation At 1	124
Figure 126.	MASH-3 - Power Spectrum with Feedback Gain Variation At 0.5	125
Figure 127.	MASH-3 - SNR' Curve with Feedback Gain Variation At 0.5	125
Figure 128.	MASH-3 Longo - Power Spectrum with Feedback Gain Variation At 0.5	126
Figure 129.	MASH-3 Longo - SNR' Curve with Feedback Gain Variation At 0.5	126
Figure 130.	MASH-2 - Power Spectrum with Comparator Input Offset At 0.5	129
Figure 131.	MASH-2 - SNR' Curve with Comparator Input Offset At 0.5	129
Figure 132.	DISDM - Power Spectrum with Comparator Input Offset At 0.5	130
Figure 133.	DISDM - SNR' Curve with Comparator Input	

2.0 SIGMA DELTA MODULATION

Sigma delta modulation, because of its simplicity and its robustness - against circuit imperfections, has recently gained favour for use in ADC in the ISDN environment. Delta sigma modulators use oversampling and one bit quantization to achieve the required high resolution ADC at a lower rate. This modulation scheme is described, as it is the foundation for all the sigma delta structures compared in this thesis.

The basic sigma delta modulator, denoted by MASH-1 in future plots and tables, is a delta modulator which has been modified by preceding it with an integrator. Thus, in effect, the integral of the input signal is delta modulated to form the output of the sigma delta modulator. This modulator structure is further simplified by combining the preceding integrator and the one in the delta modulator into a single integrator which takes the integral of the difference between the input signal and the output signal, that is,

$$\int_0^T x(t)dt - \int_0^T y(t)dt = \int_0^T e(t)dt$$

The integral of the error signal, $e(t)$, is then passed through a comparator to obtain the required single bit digital output. Figure 2 depicts the structure which comprises three components: an integrator, a comparator and a one bit digital to analog converter. In the simulations a model is used for the components that make up the circuit. Figure 2b is a model of the circuit depicted in figure 2a. This

1.0 INTRODUCTION

Oversampled delta sigma modulation techniques in recent years have, with advances in technology, become more desirable for use in developing high accuracy linear analog to digital convertors (ADC). The demand for area efficient, high performance devices has grown out of a need for full duplex transmission of digital data at a rate of 160 kbits/sec over standard two wire lines for the Integrated Digital Services Network (ISDN).

The standard two wire subscriber loops are generally terminated by a two wire to four wire hybrid. The hybrid is used to isolate the transmitted signal from the received signal, but this is impossible and transmission of echo from the near end transmitted signal into the receiver occurs. Advances in echo cancellation circuitry have recently improved the feasibility of hybrids for full duplex transmission for ISDN, but the echo canceller requires the use of a high accuracy ADC. The ADC requirements are defined by the characteristics of the signal combined with the echo. The transmitted signal echo can be far stronger, as much as 50 dB greater than the actual received signal [1,11]. The echo cancellation circuitry is designed to remove this stronger unwanted signal, but the digital output of the ADC must have enough resolution and linearity that the very small received signal is not lost in the conversion process. Figure 1

shows a simple block diagram of a fully digital receiver/transmitter circuit which can be used in the full duplex line card for ISDN applications. As shown in figure 1 the ADC must be able to accurately convert the signal, noise and echo without concealing the very small signal component. The specifications defined for the ADC for ISDN, given by Koch et al. [5], require that the SNR be greater than 72 dB and the baseband width be between 3 and 120 kHz.

This paper studies various oversampled sigma delta modulators used for analog to digital conversion, so that, in combination with the echo canceller, the signal can be accurately recovered. The modulators studied incorporate switched capacitor techniques which allows a resistor free implementation for improved area efficiency and accuracy in the CMOS fabrication process. The modulators are all based on the basic sigma delta modulator with variations as described by several authors; Candy, Hayashi et al., Richie, Koch et al., and Matsuya et al. [2-6]. Single, double and triple integration techniques are simulated and compared. The comparisons are based on the output power spectrum and the signal to noise ratio (SNR) with respect to varying input voltages on a sine wave. All the simulations are done at a sampling frequency of 10 MHz and a baseband frequency of 39.0625 kHz unless otherwise specified, thus maintaining a constant oversampling ratio of 256 for all cases studied. The common techniques used in all the cases studied, that is

the FFT algorithm, and the Blackman-Harris windowing function [7] are described in the appendices.

All the cases studied are based on the sigma delta modulator. Therefore, a brief introduction to basic sigma delta modulation and its usefulness in analog to digital conversion is provided in chapter 2.

Chapters 3 and 4 present, in detail, simulation results for the ideal cases studied as well as cases including various circuit impairments. The simplest techniques studied are the single integration sigma delta modulator (MASH-1), and the single integration sigma delta modulator with four levels of quantization (SISDM - 4 level) which is shown to be only slightly better than the single integration modulator with the expense of a more complicated quantizer. The two stage multistage noise shaping modulator (MASH-2) [3] and the double integration sigma delta modulator (DISDM) [2] are also evaluated. The results show improved SNR for these modulators thus providing the added bits of resolution required for the ADC. The most promising results for SNR or bits of resolution appears in the triple integration and triple stage modulators [4,6,8]. The penalty for using these modulators is the added size and complexity of the circuitry.

Chapter 5 provides a summary and conclusion based on the results presented in the scope of this work. The thesis concludes with suggestions for future study.

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structure provides some improvements over the delta modulator with respect to slope overload and signal to noise ratio (SNR). By oversampling the slope overload is minimized and improved performance is achieved. The overload characteristic and SNR are independent of the frequency of the input signal which makes the modulator suitable for a wide variety of applications [9], including telephony.

The sigma delta modulator, thus, provides a suitable basis from which to build enhanced structures to meet the requirements of ADC's for ISDN. The model in figure 2b is used to generate the equations used in the simulations. The equations provide a gross approximation to the actual circuit. The e_i term is approximated as a source of added noise independent of the comparator input signals. This assumption for e_i is used in this and all later cases for evaluation of the modulator structures. For a more exact analytical treatment reference can be made to the papers by Gray [12] and Ardalan and Paulos [13]. The simulations performed use the approximations to obtain the following algorithm for the basic sigma delta modulator as the core for each of the stages in the multistage noise shaping modulators. Referring to figure 2b for the structure used, the following set of equations is obtained:

$$w_i = x - yz^{-1}$$

$$v_i = w_i / (1 - z^{-1})$$

$$y = v_i + e_i$$

Noting $y = \text{sign}(v_i)$ is used for the above equation. This simulates the comparator required in the circuit structures. Substituting:

$$y = x + (1 - z^{-1})e_i$$

where, for a sinusoidal input signal

$$x = 0.5 \sin(2\pi(n-1)f/fs)$$

$$n = \text{sample} = 1, 2, 3, \dots, 16384$$

$$f = \text{baseband signal frequency} = 39.0625 \text{ kHz}$$

$$fs = \text{sampling frequency} = 10 \text{ MHz}$$

$$fs/f = \text{oversampling ratio} = 256$$

The sinusoidal input was chosen to provide an integral number of sine waves to simplify analysis and calculation of the fast fourier transform (FFT). This waveform was used as the input for all cases studied unless otherwise specified.

2.1 OP AMP REALIZATION CONSIDERATIONS

Together the integrator and comparator form the sigma delta structures described. These components both contain operational amplifiers (op amps), which largely determine the circuit performance. In an ideal simulation the op amps do not cause impairments, but in an actual circuit realization the op amp can never be ideal and can generate many impairments. This section describes the op amp and the impairments which may affect its operation.

The op amp ideally, is a voltage controlled voltage source with infinite voltage gain and with zero input admittance as well as zero output impedance. It is free of frequency dependence, distortion and noise. Practical realizations of the the op amp, however, can only approximate the ideal device. There are several non linear effects introduced by the op amp realization which must be understood so that they can be minimized in the design process. The major performance affecting impairment is the generation of harmonics due to saturation of the op amp.

Saturation occurs when the input signal causes a change of the output voltage that exceeds the supply voltages of the output transistors. Since the output in reality cannot exceed the supply voltages, the signal is truncated introducing non-linearities or harmonics. Avoiding these harmonics can be achieved by raising the supply voltages which generally is not an acceptable solution since supply voltages are typically fixed at 0 and +5V. Thus, another method must be used to reduce the harmonics. They can be reduced by scaling down the input voltage level and at the same time by the same factor the fed back quantizer voltages. There is a limit, however, for scaling down the voltage which depends on the internal noise sources of the op amp. Figure 3 depicts a simple model in which op amp noise is represented as a noise source at the input. The noise source is comprised of two components: $1/f$ noise and thermal white noise. The

Figure 3. Model of Operational Amplifier

thermal white noise is caused by the two resistors or in a switched capacitor implementation the equivalent switches' thermal noise and by the transistors constituting the op amp. The device SNR can be determined for a signal amplitude of 0 dB, assuming a frequency range of 10 kHz to 100 kHz using the following equation:

$$\text{SNR} = -10\log(100\text{kHz}-10\text{kHz}) + e \text{ dB}$$

where e is the amplitude $\text{dB}/\sqrt{\text{Hz}}$ of the noise floor which, for simplification, is assumed to be white noise.

For $e = 100 \text{ dB}$ the SNR equals 80 dB . If the signal is then decreased by 20 dB the SNR will be decrease to 60 dB . Thus scaling down the input voltage ensures lower harmonics, but the SNR will also decrease due to internal device noise sources.

Saturation is not the only source of noise and harmonics. Dynamic operation factors such as op amp bandwidth and slew rate also cause harmonics and noise. The bandwidth is related by the op amp settling time which is usually taken to be the time taken to reach 99% of the final steady state value. The slew rate reflects the fastest allowable change of output voltages. If the slew rate is not considered in the design the voltage used as the output of the op amp may not be very accurate because the op amp has not been given enough time to reach its final output level.

These known op amp impairments have been included in the simulations with impairments described in chapter four. The ideal simulations assume that the op amps are ideal and the effects described do not influence the results.

3.0 RESULTS OF IDEAL CASE SIMULATIONS

Beginning with the sigma delta modulator (MASH-1), all the structures simulated and their simulation results will be presented in the sections of this chapter. The ideal case results will then be used as a basis for comparison and to determine the effects of the various impairments applied to the structures. The impairments will be presented in chapter four.

Several values have been taken from the two types of plots generated in the simulations, power spectrum and SNR'. (The definition of SNR' is given in the following section.) Figure 4 depicts how the values used for comparison were obtained from the plots.

3.1 MASH-1

MASH-1 is the term used for the multistage noise shaping modulator with a single stage which simply is the sigma delta modulator described in chapter 2. The details of its structure, therefore, are not repeated here. Just, the simulation results are presented.

One detail not previously mentioned, however, is the comparator used in the simulations for the modulator structure. Referring to figure 5, the comparator used in the

Figure 4. Obtaining the Specified Values from the Plots

simulations is a circuit which tests the sign of the output of the integrator. If the integrator output is zero or positive the comparator will output a +1V, otherwise a -1V will be output. In a real circuit, however, the comparator will have supply voltages 0 and +5V denoted by V_{dd} and V_{ss} respectively, which would replace the +1V and -1V used in the simulations. For numerical simplicity, +1V and -1V will be used throughout this paper to represent the supply voltages.

Thus, the output of the MASH-1 is a high frequency one bit digital signal with values ± 1 V which contains the analog input as its mean value. The fact that this modulator has only two output values implies that the decimation filter required at the output will have binary information as its input. Therefore, it can be relatively simple. The type of decimation filter required by each circuit structure has not

been included in the scope of this work. It is sufficient to note that decimation filters are required and that the greater the number of levels output, the more elaborate the required decimation filter must be which implies an increase in the size of the filter. The decimation filter is required to provide two major functions: decimation which is lowering of the sampling rate and lowpass filtering which eliminates the quantization noise and the higher order harmonics. The lowpass filtering is provided by the decimation filter, since it does not have an ideal cut off causes some of the high frequency noise to be included in the baseband.

The power spectrum of the bit stream output is obtained by calculating the FFT and determining the power of each sample of the sine wave. The power of the each sample was obtained using the following formula:

$$P = 20 \log (\sqrt{x^2 + y^2}) \text{ dB}$$

where x and y are the complex coefficients output from the FFT routine.

The resulting plot of power spectrum is shown in figure 6. The plot shows that the noise level is approximately -39 dB at low frequencies. At the higher frequencies, the harmonics of the signal are dominant and raise the noise level to approximately 20 dB. This shows the need to lowpass filter

Figure 6. MASH-1 - Power Spectrum

the output of the modulator to remove the effects of the noise and harmonics at the higher frequencies. Thus, before calculating the signal to average noise floor (SNR') for this modulator a lowpass filter is introduced with a cutoff frequency slightly greater than the Nyquist frequency of the baseband input signal, that is, greater than twice its bandwidth which in the simulations performed is greater than 80

kHz. This prevents any impairments due to aliasing of the signal to impact the SNR' calculations.

The SNR' plot in figure 7 depicts the variation of SNR' with respect to the input voltage of the sine wave. The SNR' curve is generated in much the same way as the power spectrum. The FFT of the output of the modulator is calculated and used to determine the signal power which is divided by the value for the average noise floor to obtain the SNR'. The formula used to calculate SNR' is given by:

$$\text{SNR}' = \text{Signal power} / \text{Average noise floor}$$

$$\text{SNR}' = \frac{\sum_{m=1}^M a_m^2}{\left(\sum_{n=1}^N a_n^2 / N \right)}$$

where $a_m = \sqrt{x_m^2 + y_m^2}$ the complex coefficients generated for the signal,

$a_n = \sqrt{x_n^2 + y_n^2}$ the complex coefficients generated for the noise,

M = Number of points generated for the signal = 7,

N = Number of points for noise in decimator bandwidth = 122.

This process is repeated over the amplitude range of the sine wave which determines the dynamic range of the

Figure 7. MASH-1 - SNR' Curve

modulator. The amplitude range of the sine wave was chosen to be -60 dB up to 0 dB where 0 dB is relative to 1 volt. The values for maximum and minimum SNR in the tables presented throughout this thesis, therefore, are 20 dB less than those shown on the SNR' curves. They are obtained by the following equation:

$$\text{SNR} = \text{SNR}' - 10 \log 122 = \text{SNR}' - 20.8 \text{ dB.}$$

where the -20.8 dB term removes the division by N in the SNR' equation. This implies that the SNR is obtained by integrating the power of the signal and noise.

One of the parameters obtained from the plot is the maximum input voltage as shown previously in figure 4. Although throughout this paper numerical results are given, the resulting number for maximum voltage is an approximation since it was obtained from the plots. The results are subjective and could vary as much as ± 2 dB from the values given. They also carry an error due to the random nature of the signals analyzed and the finite number of samples taken.

The MASH-1 SNR results show that the maximum sine wave input voltage is -1.5 dB and the difference between the maximum and minimum SNR's is 72 dB over the dynamic range of the modulator. The large difference implies that the modulator cannot be expected to work well over the entire range of the inputs. Thus, if the amplitude of the input signal can vary greatly, the lower amplitude signals will most likely be impossible to recover, as they may be only 10 to 20 dB above the noise floor. Since the received far end signal in the line card circuit, mentioned in the introduction, can be as much as 50 dB below the echo from the transmitter, the MASH-1 modulator would not be able to provide the accuracy required by the ADC in the fully digital implementation of this circuit for the frequencies used in the simulations.

Thus, other variations of this structure have been developed to meet the requirements of the line card circuit for ISDN.

3.2 SISDM WITH FOUR LEVEL QUANTIZATION

The basic sigma delta modulator has been modified by replacing the comparator with a four level quantizer to obtain the single integration sigma delta modulator (SISDM) with four level quantization. This is similar to the approach proposed by Paulos et al. [14] for tri-level coding. The four level quantizer is a more complex circuit than the original quantizer. It also results in an output signal of four possible values, therefore, a larger silicon area implementation of a decimation filter.

The algorithm for the structure shown in figure 8 is much the same as that for the sigma delta modulator. The $\pm 1V$ comparator has been replaced with a four level quantizer whose outputs take on the values $\pm 1/3V$ and $\pm 1V$. The equation of the output is still given by:

$$\dot{y} = x + (1 - z^{-1})e,$$

which is the same as that for the sigma delta modulator with the value of the error, e , being reduced because the quantization error will be smaller due to the extra quantization levels.

The power spectrum shown in figure 9 verifies this, as the lowest noise for the modulator is -45 dB which is 6 dB lower than the standard sigma delta modulator. The harmonic content in the modulator with four levels of quantization, however, is quite similar to the basic structure with the value of the second harmonic, which cannot be filtered out, slightly larger by about 2 dB. Thus, when the SNR' curve is

Figure 9. SISDM With Four Level Quantization - Power Spectrum

generated, refer to figure 10, the results are similar to those obtained in the MASH-1 simulation. The maximum input voltage of the sine wave is approximately -0.2 dB with the change in SNR over the dynamic range being 71 dB which is slightly better than that obtained for the MASH-1 case.

Figure 10. SISDM With Four Level Quantization - SNR' Curve

These results, in general, do not justify the use of multi-level quantization to improve the performance of the ADC. The added circuit size and complexity cannot be justified by the amount of improvement gained. If, however, the application is such that the input signal's dynamic range is more restricted and lies in the SNR region where the modulator works well it could be considered as a viable option. This

structure for the same reasons as the standard sigma delta structure is not suitable to meet the specifications required by ISDN.

3.3 MASH-2

The multistage noise shaping sigma delta modulator is made up of two cascaded single integration sigma delta modulators, hence MASH-2. This structure, proposed by Hayashi et al. is advantageous for circuit stability since feedback of the output signal is no longer required and noise reduction since the noise shaping characteristic is quadratic [3]. The input signal is larger which provides an improved dynamic range. It also provides the added resolution required for the ADC in the ISDN application.

Figure 11 shows the structure used in the simulations. It is made up of two sigma delta modulators whose outputs are combined to form the total digital four level outputs. The output of the integrator in the first stage is used as the input of the second stage, thus passing forward the integral of the error generated in the first stage, that is,

$$\int_0^T x(t)dt - \int_0^T w_1(t)dt = v_1(t)$$

The value of v_1 is used as input to the comparator for the first stage which will produce a bit stream of +/- 1V's. In

a similar fashion, the second modulator obtains another bit stream of ± 1 's. These two bit streams are then combined to form the final digital output which can take on the values ± 1 and ± 3 formed using two bits of digital information. The algorithm based on this structure is derived using the following set of equations, noting that x is the sine wave described previously. (Refer to figure 11 for the

location of the variables used with respect to the circuit structure.) The first stage output is given by:

$$v_1 = x - w_1 z^{-1} + v_1 z^{-1}$$

$$w_1 = v_1 + e_1 \text{ (} w_1 = \text{sign}(v_1) \text{ was used in the simulations.)}$$

Substituting

$$w_1 = x + e_1(1 - z^{-1})$$

Similarly, the second stage output is:

$$v_2 = v_1 - w_2 z^{-1} + v_2 z^{-1}$$

$$w_2 = v_2 + e_2 \text{ (} w_2 = \text{sign}(v_2) \text{ was used in the simulations.)}$$

Substituting

$$w_2 = v_2 + e_2(1 - z^{-1})$$

The final digital output, y , is obtained by combining the outputs of the first and second stage as follows:

$$y = z^{-1} w_1 + w_2(1 - z^{-1})$$

After substitution

Figure 12. MASH-2 - Power Spectrum

$$y = x + e_2(1 - z^{-1})^2$$

Note that the noise from the first stage, e_1 , does not appear in the final output and the effective error after decimation of the second stage is smaller due to the affect

of the $(1 - z^{-1})$ factor which moves the quantization noise toward higher frequencies.

Using these equations in the simulation program, the plots in figures 12 and 13 are obtained for the power spectrum and the SNR' respectively. The power spectrum shows that the noise floor has decreased to -47 dB and the highest noise level has increased to 30 dB. The highest noise level, however, is at high frequencies which will be filtered out by the lowpass filter. From figure 12, it can be seen that the effect of the harmonics is greatly reduced in the MASH-2 modulator. The harmonics can just be seen as small peaks in the noise level. This reduction in the amplitude of the harmonics is a definite advantage to using this type of structure because the second harmonic which cannot be removed is nearly negligible and does not impact circuit performance.

The SNR' curve of figure 13 shows that this structure is more appropriate for the ISDN application. It does not have as great a variation, 57 dB, in the SNR over the dynamic range of the modulator. Its maximum input voltage is -1 dB with a maximum SNR' of approximately 94 dB. This is a great improvement over both the single stage modulators described.

Figure 13. MASH-2 - SNR' Curve

3.4 DISDM

Double integration sigma delta modulation (DISDM) is another alternative for use in the ADC. This method, denoted in the plots by Richie two stage sigma delta modulator, is described by Richie [4] and Candy [2] as a technique which em-

employs feedback and integration as a means of moving the quantization error out of baseband.

The structure is made up of two integrators and a single comparator, thereby, producing an output bit stream of +/- 1 V's. This output requires a simpler decimation filter than the MASH-2 structure. Referring to figure 14, it should be noted that there are two gain components specified for this structure. The gains in the cases reviewed thus far have been chosen as one, therefore, they have not been included in the structures. The DISDM structure, however, is highly sensitive to the values of the gains. Theoretically, when deriving the algorithms if unity gains are chosen then the resulting equations for the output, y , is obtained as follows:

$$o_1 = o_1 z^{-1} + kx - k_1 y z^{-1}$$

$$o_2 = o_2 z^{-1} + o_1 - y z^{-1}$$

$$y = o_2 + e, \text{ (} y = \text{sign}(o_2) \text{ was used in the simulations.)}$$

Substituting

$$y(1 - z^{-1} + k_1 z^{-1}) = kx + e_1(1 - z^{-1})$$

If $k = 1$ and $k_1 = 1$ then

$$y = x + e_1 (1 - z^{-1})^2$$

which is the same result as that obtained for the MASH-2 modulator. In the simulations, however, the values of the gains, k and k_1 , were chosen to be 0.5 to obtain results comparable to the MASH-2 modulator. With unity gains the DISDM

Figure 15. DISDM - Power Spectrum

seemed unstable due to harmonics and did not produce the required results. Thus, any gains used in the DISDM must be optimized to ensure adequate performance of the modulator.

The simulation results show that with the values of gain equal to 0.5, the DISDM operated in a comparable manner to that observed for the MASH-2 modulator. The power spectrum

Figure 16. DISDM - SNR' Curve

plot in figure 15 shows a lowest noise level of -47 dB, the same as for the MASH-2 and a highest noise level of 28 dB slightly better than the MASH-2. Over the dynamic range of the modulator the SNR delta is 55 dB which is a slight improvement over that for the MASH-2 modulator. The maximum input voltage is -0.9 dB with a maximum SNR' value of 92 dB as shown in figure 16.

The DISDM and MASH-2 comparison when evaluated under ideal conditions without any consideration for circuit impairments shows that the DISDM performance is slightly better than the MASH-2. It also should be noted that the DISDM structure requires less area physically since two sigma delta modulators are not required and since only two output levels are obtained the decimation filter is smaller.

3.5 MASH-3

The modulators described in this and the following section are based on the multistage noise shaping modulator. Both structures yield similar results with very different approaches to the same problem.

The three stage, multistage noise shaping modulator, MASH-3, is a slight misnomer, as it is really made up of four single integration sigma delta modulators. This structure is similar to that presented by Matsuya et al. [6]. The four sigma delta modulators are arranged to obtain the same results as cascading three modulators (presented later) as far as the algorithm is concerned. The first two sigma delta modulators are used in parallel both having the sine wave as inputs. The results of the two modulators are combined and used as an input to the third modulator whose output is cascaded to the fourth modulator as in the two stage structure. This modulator, physically, is the largest of the structures

Figure 17. MASH-3 - Circuit Structure

simulated. It also requires a very large decimation filter since there are 4 bits at the final output of the circuit. Figure 17 depicts this complicated structure which at first glance seems unreasonable since the same results can be obtained with much less hardware. There is, however, some advantage to this approach as it in effect reduces the common mode noise in the first stage.

The technique of combining the first two modulators in parallel with reversed polarity is a trick to reduce noise by reducing the common mode noise in the operational amplifiers. This, in effect, improves the performance of the first stage. By combining half the magnitudes of the two outputs the required values are obtained for input to the next stage. This technique, however, does not have an appreciable effect on the simulation performed because mathematically the two integrators are the same. It should provide a more noticeable affect in an actual circuit where the structures can never be identical.

The algorithm used to simulate this structure allows the quantization noise to be shifted even further out of the baseband frequency range. Once out of the baseband range, however, the error is much greater which is of little concern since it will be filtered out. The algorithm used negates the input sine wave in one of the first stage modulators to account for the reversed polarity of the op amp in this stage, therefore, the difference between the two first stage modulators is fed forward and at the output the difference between half w_1 and half w_2 is required. This structure was presented by Matsuya et al at ISSCC '87 [6], although their equation for the summing logic is slightly different from the one presented here.

The derivation of the algorithm used in the simulations of this structure is obtained as follows, referring to figure 17 for the circuit position of the various parameters used.

For the first stage:

$$v_1 = x - w_1 z^{-1} + v_1 z^{-1}$$

$$w_1 = v_1 + e_1 \text{ (} w_1 = \text{sign}(v_1) \text{ was used in the simulations.)}$$

$$w_1 = x + e_1 (1 - z^{-1})$$

Similarly

$$v_2 = -x - w_2 z^{-1} + v_2 z^{-1}$$

$$w_2 = v_2 + e_2 \text{ (} w_2 = \text{sign}(v_2) \text{ was used in the simulations.)}$$

$$w_2 = -x + e_2 (1 - z^{-1})$$

Combining these two halves of the first stage the value to be passed to the input of the second stage, D, is obtained:

$$D = 0.5(e_1 - e_2)$$

where e_1 and e_2 are the quantization errors of the two first stage comparators.

Figure 18. MASH-3 - Power Spectrum

The second stage output is given by:

$$v_3 = D - w_3 z^{-1} + v_3 z^{-1}$$

$w_3 = v_3 + e_3$ ($w_3 = \text{sign}(v_3)$ was used in the simulations.)

Figure 19. MASH-3 - SNR' Curve

$$w_3 = 0.5(e_1 - e_2) + e_3(1 - z^{-1})$$

and the third stage output is:

$$v_4 = e_3 - w_4 z^{-1} + v_4 z^{-1}$$

$$w_4 = v_4 + e_4 \text{ (} w_4 = \text{sign}(v_4) \text{ was used in the simulations.)}$$

$$w_4 = e_3 + e_4(1 - z^{-1})$$

Combining the output of each of the stages to form the final output, y , the following is obtained:

$$y = 0.5(w_1 - w_2) - w_3(1 - z^{-1}) + w_4(1 - z^{-1})^2$$

$$y = x + e_4(1 - z^{-1})^3$$

The output, y , shows that the quantization noise is again shifted even further out of baseband than in the two stage and double integration modulators. The lowest noise level from the plot of power spectrum in figure 18, is about -47 dB while the highest is around 40 dB. The highest noise level is increased over the two stage structures since the noise shaping is a cubic function and rises more rapidly once out of the baseband region. The maximum input voltage is reduced to -4 dB where 0 dB is 1V. Over the dynamic range of the modulator the delta in SNR is 44 dB, a substantial improvement over the MASH-2 and DISDM modulators. Figure 19 shows the plot of the SNR curves for this structure.

This structure shows promising results for the ISDN application provided the added size of the circuit is tolerable, noting that in effect, four sigma delta modulators are re-

quired as well as a decimation filter to handle the 15 possible output values of the final output stage.

3.6 MASH-3 LONGO

Another modification of the multistage noise shaping modulator is being proposed by Longo [8]. This structure produces similar results to the MASH-3 modulator described in the previous section without the need of the fourth sigma delta modulator. Also, a slightly smaller decimation filter is required since only eight values are output in the final stage rather than 15.

This structure proposed by Longo, is a three stage cascaded modulator with the quantization error being the input to the following stage rather than the just the integrator output as in the MASH-2 modulator. Figure 20 depicts the structure from which the algorithm used in the simulations is obtained. It should be noted that three one bit comparators are used in this structure which results in a digital output that can take on one of eight possible output values. In this simulation the values are ± 1 , ± 3 , ± 5 , ± 7 .

This structure yields the same results for the output, y , as the previous MASH-3 result even though the intermediate steps are different. The algorithm is derived as follows:

First stage

$$v_1 = x - w_1 z^{-1} + v_1 z^{-1}$$

$$w_1 = v_1 + e_1 \text{ (} w_1 = \text{sign}(v_1) \text{ was used in the simulations.)}$$

$$w_1 = x + e_1 (1 - z^{-1})$$

Second stage

$$v_2 = e_1 - w_2 z^{-1} + v_2 z^{-1}$$

$$w_2 = v_2 + e_2 \text{ (} w_2 = \text{sign}(v_2) \text{ was used in the simulations.)}$$

Figure 22. MASH-3 Longo - SNR' Curve

$$w_2 = e_1 + e_2(1 - z^{-1})$$

Third stage

$$v_3 = e_2 - w_3 z^{-1} + v_3 z^{-1}$$

$$w_3 = v_3 + e_3 \text{ (} w_3 = \text{sign}(v_3) \text{ was used in the simulations.)}$$

$$w_3 = e_2 + e_3(1 - z^{-1})$$

Combining the outputs of the three stages:

$$y = w_1 - w_2(1 - z^{-1}) + w_3(1 - z^{-1})^2$$

$$y = x + e_3(1 - z^{-1})^3$$

The MASH-3 Longo structure actually displays slightly better results than the MASH-3. The power spectrum in figure 21 shows the lowest noise level to be the same, -47 dB, as the MASH-3, but the highest noise is lower by approximately 5 dB. The SNR' curve in figure 22 shows the same results for the maximum input voltage, -4 dB and a maximum SNR' of 105 dB. The SNR delta over the dynamic range is, however, improved, with a value of 41 dB. Thus, if the surface area of the circuit is of great importance the Longo approach can provide the results required with a smaller physical area.

3.7 TISDM

Triple integration sigma delta modulation (TISDM) has by far the best simulation results for the ideal case. It should be noted, however, that optimized gain coefficients were used for evaluating this structure [10].

Figure 23. TISDM - Circuit Structure

The TISDM is a simple extension of the DISDM structure described in section 3.4. It includes three integrators, three feedback loops from the output and a single comparator at the output as shown in figure 23. The comparator outputs a bit stream of + and - 1 V's, therefore, area requirements for the decimation filter are much more relaxed than for the three stage modulators described in the previous two

sections. This structure, because of the multiple levels of integration and feedback, can become unstable [2,4] and considerations must be made to ensure that the unstable conditions do not arise. Due to the effects of instability when unity gains were used, this structure was simulated using optimized gain coefficients and the amplitude of the sine wave was reduced to 0.09 rather than 0.5 as in the other simulations. The gain coefficients used are labeled in figure 23.

The algorithm used for this structure will be derived using gains of one and also using the optimum gain coefficients to see the effects of changing the gains on the algorithm.

The following algorithm is obtained with variable values for the gains:

$$o_1 = kx + o_1 z^{-1} - k_1 y z^{-1}$$

$$o_2 = k_2 o_1 + o_2 z^{-1} - k_3 y z^{-1}$$

$$o_3 = k_4 o_2 + o_3 z^{-1} - k_5 y z^{-1}$$

$$y = o_3 + e_3 \text{ (} y = \text{sign}(o_3) \text{ was used in the simulations.)}$$

Substituting

Figure 24. TISDM - Power Spectrum

$$y((1 - z^{-1})^3 + k_4 k_2 k_1 z^{-1} + k_4 k_3 z^{-1} (1 - z^{-1}) + k_5 z^{-1} (1 - z^{-1})^2) \\ = k_4 k_2 k_1 x + e_3 (1 - z^{-1})$$

For $k_1 = k_2 = k_3 = k_4 = k_5 = 1$ the equation reduces to:

$$y = x + e_3 (1 - z^{-1})^3$$

Figure 25. TISDM - SNR' Curve

which is the same result as obtained for the two MASH-3 algorithms.

Using the optimized values, obtained from a paper by Keyes et al. [10], for gain the equation for y changes to the one given below:

For $k = 0.09$, $k_1 = 0.25$, $k_2 = 0.4$,

$$k_3 = 0.3, k_4 = 0.6, k_5 = 0.7$$

$$y = (0.0216x + e_3(1 - z^{-1})^3)/(1 - 2.06z^{-1} + 1.42z^{-2} - 0.3z^{-3})$$

This optimal result is obtained by minimizing the saturation voltages at each node which results in minimal harmonics. It is this result that is used in the simulations. The plot of power spectrum in figure 24 shows a slightly lower noise level of -49 dB as well as a lower highest noise level of 30 dB. Since the input amplitude of the sine wave is smaller due to the change in gain coefficients the value of the signal is also slightly lower. The maximum input voltage is -13 dB which is also due to the reduced amplitude of the input sine wave. The SNR delta, from figure 25, over the frequency range, however, is 24 dB which shows that this structure maintains good results for SNR over the operating frequency range of the circuit.

If the potential instability caused by feedback can be overcome in the actual implementation of this circuit, it can be considered a good choice for the ADC in the ISDN line echo cancellation circuit for a 160 kbit/s subscriber loop.

3.8 SUMMARY OF IDEAL CASE RESULTS

Much data has been presented thus far for the ideal case simulations. It is useful to pause and summarize the ideal case results. Table 1 provides a quick reference to the results obtained from the various plots for the ideal case simulations.

Under ideal conditions, the MASH-1 or basic sigma delta modulator displayed the worst results. This is mainly due to the harmonics and the lack of noise shaping. This type of modulator, as expected, does not provide adequate resolution for consideration as an ADC for the line card circuit. It was included in the comparisons mainly as a reference to see the improvements gained by both multistage noise shaping sigma delta modulators and multiple integration sigma delta modulators.

The SISDM with four quantization levels, also did not yield adequate results when considering the added complexity of the quantizer and the four levels of output.

The MASH-2 and DISDM structures which provided results in the same range with respect to each other were a great improvement over the single stage structures. Each of the two stage circuits has advantages in its favour. The MASH-2 modulator is more stable and does not require feedback while

IDEAL CASE SIMULATION							
	MASH-1	SISDM 4 LEVEL	MASH-2 HAYASHI	DISDM	MASH-3	MASH-3 LONGO	TISDM
LEVELS AT OUTPUT	2	4	4	2	15	8	2
MAX. SIGNAL (dB)	63	63	63	63	63	63	60
HIGH NOISE LEVEL (dB)	20	20	30	28	40	35	30
LOW NOISE LEVEL (dB)	-39	-45	-47	-47	-47	-47	-49
SNR DELTA (dB)	72	71	57	55	44	41	24
MAX. INPUT VOLTS (dB)	-1	-0.2	-1	-1	-4	-4	-13
MAX. SNR (dB)	63	59	74	72	85	85	82
MIN. SNR (dB)	-10	-12	16	16	37	40	45

Table 1 - Summary of Ideal Case Results

the DISDM structure is more compact, therefore requiring less physical area. The DISDM structure has another advan-

tage described by Candy in that the quantization is uniform which allows the encoder to accept the sum of several independent signals without having interaction between them [2].

The three stage modulators, MASH-3 and MASH-3 Longo, and the triple integration sigma delta modulator show the most promising results for use in the analog to digital conversion process. They all shift the noise out of the baseband range and reduce the values of the harmonics. They provide good resolution over the dynamic range of the modulator. Again, each of these cases has its advantages.

The TISDM structure aside from having the best simulation results, mostly due to the use of optimum gain coefficients, has advantages with respect to its simplicity. Since, it has a two level output bit stream the decimation filter required is less complex. The overall size of the structure is also smaller since only one comparator is required. The major disadvantage is the instability caused by the feedback loops. This structure has a tendency to latch into noisy modes of operation because the properties of the modulation are modified [2].

The MASH-3 and MASH-3 Longo structures also provide acceptable simulation results to justify use in the ADC. Their results are basically equivalent, although there are advantages to each of the structures. The Longo structure

is the simpler of the two and requires less circuitry and a smaller decimation filter since it has eight output levels as opposed to 15. The MASH-3 modulator with 15 levels of output and an extra sigma delta modulator requires more area. If area is not a major concern this structure provides the advantage of reducing the common mode noise in the first stage op amps. Both these structures have a major advantage over the TIDSM structure because they do not exhibit the instability caused by feedback, therefore, they require less precision in the fabrication process.

The decision to use any one of the structures must be based not only on the ideal results presented here, but on the impairments. The impairments being a departure from the ideal properties inherent in any practical realization. Therefore, chapter four continues with further evaluation of these structures to determine the affects of various impairments introduced to the ideal algorithms.

4.0 RESULTS OF SIMULATIONS WITH IMPAIRMENTS

The accuracy of individual components and the fabrication process used in constructing the various types of oversampled ADC's can play a major role in the decision to use one type of modulator structure over another. This chapter describes the introduction of various impairments to the structures set forth in the previous chapter. The effects of the impairments are reviewed and an observation is made regarding which of the structures is most affected by the particular impairment. These results combined with those for the ideal cases should provide enough information upon which a decision can be made regarding the most feasible of the structures for implementation.

The impairments applied to the structure are listed below:

- op amp offset
- op amp saturation
- limited op amp bandwidth
- feedback gain variation
- comparator input offset

- comparator dead zone

The results for each type of impairment are provided in the appropriate sections of this chapter.

4.1 OPERATIONAL AMPLIFIER OFFSET

Of major concern in the sigma delta structures described are the parameters of the operational amplifier. One of these parameters is input offset voltage. This voltage offset at the input of the operational amplifier cannot be avoided, although with high precision fabrication process and careful design it can be minimized. Voltage offset is caused by asymmetry of op amp transistor pairs, mainly by area mismatches and silicon impurities. Also differences in the bias currents applied to the input transistors yields the input offset voltage. This section deals with the effect of op amp input offset on the sigma delta structures described in chapter 3.

To simulate op amp offset, a constant voltage was added to the input of each integrator in the structure. Four possible values were chosen for the offset: 0.01 V, 0.25 V, 0.5 V, and 0.75 V. The simulation programs were then executed with the added impairment and the results tabulated. Table 2, at the end of this section, summarizes the actual results obtained. Also at the end of this section, figures 26

through 72 provide the power spectrums and SNR' curves obtained for this impairment.

The op amp offset did adversely affect all the circuits. The circuits that were most severely affected were the double and triple integration sigma delta modulators. Once the offset was larger than the input amplitude of the sine wave, these two circuits became unstable and the results useless. This was particularly noticeable in the TISDM structure where the gains were crucial to begin with for stability and the gain at the input was 0.09. This, however, is not the case for the single, double or triple stage modulators which can tolerate the offset even if it is larger than the input voltage of the sine wave. It should be noted, however, that as the offset increased the dynamic range of the modulator was decreasing. The maximum input voltage became smaller.

Another observation that was made is that adding the op amp offset also creates a large dc component which is depicted in the plots of power spectrum. This is expected as the op amp offset can be seen as an applied dc value in the transfer functions for the structures. This is not of major concern since dc will not be passed through the following circuitry.

Finally, it was observed that as the offset is increased the maximum value of SNR' is decreased. This is due both to a

very small decrease in the signal and an increase in the harmonic content. As the offset is increased the harmonics get larger. These harmonics can, however, be minimized by reducing the input signal amplitude as discussed in section 2.1. Figure 68 for an op amp offset of 0.75 using the Longo structure can be compared with figure 72 which has a reduced signal amplitude, shows a marked decrease in the harmonics. This can be extended to any of the plots which show high harmonics at the input amplitude used in the simulations. There is, however, a tradeoff required when reducing the input amplitude as discussed in section 2.1.

Thus, the multistage modulators show the least amount of degradation due to op amp offset and the op amp offset should be minimized so that the harmonics do not degrade the SNR to an unacceptable level.

SIMULATIONS WITH OP AMP OFFSET AT 0.01							
	MASH-1	SISDM 4 LEVEL	MASH-2 HAYASHI	DISDM	MASH-3	MASH-3 LONGO	TISDM
MAX. SIGNAL (dB)	63	63	63	63	63	63	60
HIGH NOISE LEVEL (dB)	35	35	35	40	35	35	47
LOW NOISE LEVEL (dB)	-20	-20	-47	-47	-47	-47	-49
SNR DELTA (dB)	57	75.5	55	51	41	44	27
MAX. INPUT VOLTS (dB)	-1	-0.5	-1	-1	-4	-4	-14
MAX. SNR (dB)	54	56	71	71	85	85	80
MIN. SNR (dB)	-4	-20	15	19	40	37	39

Table 2A - Op Amp Offset at 0.01

SIMULATIONS WITH OP AMP OFFSET AT 0.25						
	MASH-1	SISDM 4 LEVEL	MASH-2 HAYASHI	DISDM	MASH-3	MASH-3 LONGO
MAX. SIGNAL (dB)	63	63	63	63	63	63
HIGH NOISE LEVEL (dB)	63	63	63	69	63	63
LOW NOISE LEVEL (dB)	-70	-31	-46	-45	-47	-47
SNR DELTA (dB)	48	68	35	32	41	41
MAX. INPUT VOLTS (dB)	-2	-2	-7	-10	-7	-7
MAX. SNR (dB)	43	50	64	58	84	83
MIN. SNR (dB)	-7	-20	22	16	36	35

Table 2B - Op Amp Offset at 0.25

SIMULATIONS WITH OP AMP OFFSET AT 0.5					
	MASH-1	SSDM 4 LEVEL	MASH-2 HAYASHI	MASH-3	MASH-3 LONGO
MAX. SIGNAL (dB)	63	63	63	63	63
HIGH NOISE LEVEL (dB)	69	69	69	69	69
LOW NOISE LEVEL (dB)	-70	-42	-88	-47	-47
SNR DELTA (dB)	55	54	33	26	20
MAX. INPUT VOLTS (dB)	-5	-9	-7	-11	-12
MAX. SNR (dB)	40	48	53	69	67
MIN. SNR (dB)	-20	-15	13	32	35

Table 2C - Op Amp Offset at 0.5

SIMULATIONS WITH OP AMP OFFSET AT 0.75					
	MASH-1	SISDM 4 LEVEL	MASH-2 HAYASHI	MASH-3	MASH-3 LONGO
MAX. SIGNAL (dB)	60	61	61	60	60
HIGH NOISE LEVEL (dB)	72	72	72	72	72
LOW NOISE LEVEL (dB)	-88	-75	-85	-85	-80
SNR DELTA (dB)	38	49	53	17	13
MAX. INPUT VOLTS (dB)	-12	-11	-12	-13	-13
MAX. SNR (dB)	30	40	45	47	49
MIN. SNR (dB)	-20	-20	-20	17	23

Table 2D - Op Amp Offset at 0.75

Figure 26. MASH-1 - Power Spectrum with Op Amp Offset at 0.01

Figure 27. MASH-1 - SNR' Curve with Op Amp Offset at 0.01

Figure 28. MASH-1 - Power Spectrum with Op Amp Offset at 0.25

Figure 29. MASH-1 - SNR' Curve with Op Amp Offset at 0.25

Figure 30. MASH-1 - Power Spectrum with Op Amp Offset at 0.5

Figure 31. MASH-1 - SNR' Curve with Op Amp Offset at 0.5

Figure 32. MASH-1 - Power Spectrum with Op Amp Offset at 0.75

Figure 33. MASH-1 - SNR' Curve with Op Amp Offset at 0.75

Figure 34. SISDM 4 Level Quantizer - Power Spectrum with Op Amp Offset at 0.01

Figure 35. SISDM 4 Level Quantizer - SNR' Curve with Op Amp Offset at 0.01

Figure 36. SISDM 4 Level Quantizer - Power Spectrum with Op Amp Offset at 0.25

Figure 37. SISDM 4 Level Quantizer - SNR' Curve with Op Amp Offset at 0.25

Figure 38. SISDM 4 Level Quantizer - Power Spectrum with Op Amp Offset at 0.5

Figure 39. SISDM 4 Level Quantizer - SNR' Curve with Op Amp Offset at 0.5

Figure 40. SISDM 4 Level Quantizer - Power Spectrum with Op Amp Offset at 0.75

Figure 41. SISDM 4 Level Quantizer - SNR' Curve with Op Amp Offset at 0.75

Figure 42. MASH-2 - Power Spectrum with Op Amp Offset at 0.01

Figure 43. MASH-2 - SNR' Curve with Op Amp Offset at 0.01

Figure 44. MASH-2 - Power Spectrum with Op Amp Offset at 0.25

Figure 45. MASH-2 - SNR' Curve with Op Amp Offset at 0.25

Figure 46. MASH-2 - Power Spectrum with Op Amp Offset at 0.5

Figure 47. MASH-2 - SNR' Curve with Op Amp Offset at 0.5

Figure 48. MASH-2 - Power Spectrum with Op Amp Offset at 0.75

Figure 49. MASH-2 - SNR' Curve with Op Amp Offset at 0.75

Figure 50. DISDM - Power Spectrum with Op Amp Offset at 0.01

Figure 51. DISDM - SNR' Curve with Op Amp Offset at 0.01

Figure 52. DISDM - Power Spectrum with Op Amp Offset at 0.25

Figure 53. DISDM - SNR' Curve with Op Amp Offset at 0.25

Figure 54. MASH-3 - Power Spectrum with Op Amp Offset at 0.01

Figure 55. MASH-3 - SNR' Curve with Op Amp Offset at 0.01

Figure 56. MASH-3 - Power Spectrum with Op Amp Offset at 0.25

Figure 57. MASH-3 - SNR' Curve with Op Amp Offset at 0.25

Figure 58. MASH-3 - Power Spectrum with Op Amp Offset at 0.5

Figure 59. MASH-3 - SNR' Curve with Op Amp Offset at 0.5

Figure 60. MASH-3 - Power Spectrum with Op Amp Offset at 0.75

Figure 61. MASH-3 - SNR' Curve with Op Amp Offset at 0.75

Figure 62. MASH-3 Longo - Power Spectrum with Op Amp Offset at 0.01

Figure 63. MASH-3 Longo - SNR' Curve with Op Amp Offset at 0.01

Figure 64. MASH-3 Longo - Power Spectrum with Op Amp Offset at 0.25

Figure 65. MASH-3 Longo - SNR' Curve with Op Amp Offset at 0.25

Figure 66. MASH-3 Longo - Power Spectrum' with Op Amp Offset at 0.5

Figure 67. MASH-3 Longo - SNR' Curve with Op Amp Offset at 0.5

Figure 68. MASH-3 Longo - Power Spectrum with Op Amp Offset at 0.75

Figure 69. MASH-3 Longo - SNR' Curve with Op Amp Offset at 0.75

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Figure 72. MASH-3 Longo - Op Amp Offset at 0.75 with Input Amplitude at 0.1

4.2 OPERATIONAL AMPLIFIER SATURATION

Another op amp impairment which can greatly affect the operation of the ADC is op amp saturation. This occurs when increases in the op amp input no longer generate increases in the output as previously discussed in section 2.1.

An evaluation of the op amp outputs was performed without considering the saturation. The results were useful for determining how the saturation affected the circuit performance. The op amp outputs for each structure are plotted using histograms which are included in figures 73 through 79. The saturation levels were chosen to be the comparator output levels of ± 1 V. The saturation was applied to the

op amp output using an IF statement. If the output was greater than 1 V then the output was changed to 1 V. If it was less than -1 V, it was changed to -1 V.

Figure 73 for the ideal structure op amp outputs showed the MASH-1 structure had only 62% of its outputs in the range ± 1 V which implies that the remaining 38% of the output would be over the saturation limits. Under these conditions, it was observed that the circuit no longer functioned because too much information was lost. Therefore, the saturation level was increased to ± 2 V's which permitted the modulator to operate over the dynamic range. The same situation arose for the SISDM with four levels of quantization which has a higher percentage, 79% of its values in the ± 1 V range. Even with this number of its outputs below saturation, it could not operate over the dynamic range. The two types of MASH-3 structures also experience similar problems with op amp saturation. The percentage of outputs in the ± 1 V range for each of the three op amps in the circuit were: first stage 63%, second stage 52%, and third stage 43%. These values are the same for both structures. Neither of these structures appeared to operate with the saturation limit set to ± 1 V. Thus, there appears to be a relation between the number of outputs over the saturation limits and the ability of the circuit to cope with the saturation. If greater than 20% of the op amp output is over the saturation limit, the circuit performance becomes unac-

ceptable. Another approach which will provide acceptable results is scaling down the input voltage, since normally the supply voltages are fixed.

Thus, for all four of these structures which exhibit problems with the ± 1 V saturation levels, the saturation limit on the op amp was increased to ± 2 V, leaving the comparator limits still at ± 1 V. Under this condition the circuits performed the required modulation, although not as effectively as in the ideal case. Table 3 at the end of this section summarizes the results of the plots obtained.

In general, op amp saturation caused the maximum allowable input voltage to decrease considerably, therefore, reducing the dynamic range of the modulators. Another observation is that the MASH-2, DISDM, and TISDM structures did not experience the problems with saturation that were seen in the previously mentioned structures. In the TISDM case, this is most likely due to the gain on the input signal which effectively makes the peak to peak voltage of the sine wave very small, 0.18 V. Thus, almost all the op amp outputs are well within the saturation limits, as can be seen from the histogram in figure 79. Similarly, for the MASH-2 and DISDM structures the outputs are mostly confined to the ± 1 V range. Thus, an important consideration to be made is the level of the op amp saturation versus the voltage levels to be output by the op amp.

The set of plots for op amp saturation are included in figures 80 through 93 at the end of this section. From these plots, it can be seen that the lowest noise is greatly reduced but the harmonics are magnified. The decrease in maximum SNR' and decrease in dynamic range can also be observed in these plots. The effects of saturation on the delta sigma structures appears to be the worst of the impairments applied to the structure, therefore, careful consideration must be made to ensure that the saturation limits are maximized with respect to the op amp output levels. Also, the input voltages should be scaled using the appropriate gains to minimize the number of output levels that are beyond the saturation limits.

Figure 73. MASH-1 - Histogram of Op Amp Outputs

Figure 74. SISDM 4 Level Quantizer - Histogram of Op Amp Outputs

Figure 75. MASH-2 - Histogram of Op Amp Outputs

Figure 76. DISDM - Histogram of Op Amp Outputs

Figure 77. MASH-3 - Histogram of Op Amp Outputs

Figure 78. MASH-3 Longo - Histogram of Op Amp Outputs

Figure 79. TISDM - Histogram of Op Amp Outputs

SIMULATIONS WITH OP AMP SATURATION							
	MASH-1	SISDM 4 LEVEL	MASH-2 HAYASHI	DISDM	MASH-3	MASH-3 LONGO	TISDM
MAX. SIGNAL (dB)	57	62	61	63	57	57	60
HIGH NOISE LEVEL (dB)	-78	25	-60	30	30	30	30
LOW NOISE LEVEL (dB)	-80	-45	-95	-5	-90	-85	-49
SNR DELTA (dB)	52	63	50	34	36	36	12
MAX. INPUT VOLTS (dB)	-1	-2	-10	-10	-14	-14	-17
MAX. SNR (dB)	44	53	40	52	40	40	64
MIN. SNR (dB)	-9	-12	-20	8	-10	-10	35
OP AMP OUTPUT VS. +1 & -1 (%)	62	79	1 2 87 70	1 2 97 86	1 2 63 51 3 43	1 2 63 51 3 43	1 2 100 100 3 95

Table 3 - Op Amp Saturation

Figure 80. MASH-1 - Power Spectrum with Op Amp Saturation

Figure 81. MASH-1 - SNR' Curve with Op Amp Saturation

Figure 82. SISDM 4 Level Quantizer - Power Spectrum with Op Amp Saturation

Figure 83x SISDM 4 Level Quantizer - SNR' Curve with Op Amp Saturation

Figure 84. MASH-2 - Power Spectrum with Op Amp Saturation

Figure 85. MASH-2 - SNR' Curve with Op Amp Saturation

Figure 86. DISDM - Power Spectrum with Op Amp Saturation

Figure 87. DISDM - SNR' Curve with Op Amp Saturation

Figure 88. MASH-3 - Power Spectrum with Op Amp Saturation

Figure 89. MASH-3 - SNR' Curve with Op Amp Saturation

Figure 90. MASH-3 Longo - Power Spectrum with Op Amp Saturation

Figure 91. MASH-3 Longo - SNR' Curve with Op Amp Saturation

Figure 92. TISDM - Power Spectrum with Op Amp Saturation

Figure 93. TISDM - SNR' Curve with Op Amp Saturation

4.3 LIMITED OP AMP BANDWIDTH

Harmonics and noise can be generated by another op amp impairment referred to as limited bandwidth. This implies that the op amp has not had time to settle at its final output value by the time the next value is sampled at the output. This is a function of the settling time and the slew rate. The simulations assume that the slew rate is fast enough to allow the output voltage to change for the next sample. The op amp, however, is bandwidth limited such that it reaches 98% of its final steady state value in the simulations performed. Table 4 presents the results obtained and figures 94 through 105 at the end of this section contain the plots obtained for this impairment.

The results show that the SISDM with four levels of quantization is most severely affected by this impairment. This is expected since the quantizer step size is smaller and integrator errors caused because the op amp has not settled can not be tolerated by the quantizer. Large harmonics are generated for the power spectrum plot and the SNR' curve is not stable. The DISDM and TISDM are the next structures which are greatly affected by this impairment, although not as much as the SISDM structure. In all these cases, the harmonic content was greatly increased relative to the ideal cases. The MASH-1, MASH-2, and both MASH-3 structures show

no changes from the ideal case. They are insensitive to this impairment.

SIMULATIONS WITH LIMITED BANDWIDTH						
	MASH-1	MASH-2 HAYASHI	DISDM	MASH-3	MASH-3 LONGO	TISDM
MAX. SIGNAL (dB)	63	63	63	63	63	60
HIGH NOISE LEVEL (dB)	20	30	26	40	35	27
LOW NOISE LEVEL (dB)	-39	-47	-46	-47	-47	-50
SNR DELTA (dB)	72	57	64	44	41	28
MAX. INPUT VOLTS (dB)	-1	-1	-1	-4	-4	-13
MAX. SNR (dB)	63	74	74	85	85	80
MIN. SNR (dB)	-10	16	9	37	40	39

Table 4 - Limited Bandwidth

Figure 94. MASH-1 - Power Spectrum with Limited Op Amp Bandwidth

Figure 95. MASH-1 - SNR' Curve with Limited Op Amp Bandwidth

Figure 96.. MASH-2 - Power Spectrum with Limited Op Amp Bandwidth

Figure 97. MASH-2 - SNR' Curve with Limited Op Amp Bandwidth

Figure 98. DISDM - Power Spectrum with Limited Op Amp Bandwidth

Figure 99. DISDM - SNR' Curve with Limited Op Amp Bandwidth

Figure 100. MASH-3 - Power Spectrum with Limited Op Amp Bandwidth

Figure 101. MASH-3 - SNR' Curve with Limited Op Amp Bandwidth

Figure 102. MASH-3 Longo - Power Spectrum with Limited Op Amp Bandwidth

Figure 103. MASH-3 Longo - SNR' Curve with Limited Op Amp Bandwidth

Figure 104. TISDM - Power Spectrum with Limited Op Amp Bandwidth

Figure 105. TISDM - SNR' Curve with Limited Op Amp Bandwidth

4.4 FEEDBACK GAIN VARIATION

Feedback gain variation is another parameter that was varied for the sigma delta structures evaluated. The results from the simulations performed are included at the end of this section in figures 106 through 129. Some of these plots have a highly unstable region after the drop in SNR' at the maximum input voltage.

These structures are all sensitive to the value of gain applied to the feedback loop. The impairment was applied in the simulations by multiplying the value being fed back to the summing node at the input by a constant gain coefficient. The values chosen for this were 0.25 and 0.5. These results were then compared to the results obtained for the ideal case where the gain was 1. The DISDM structure was different in that 0.5 was used for the ideal case and 0.25 and 1 were used for the impairment. The TISDM structure due to its extreme sensitivity to gain variation was not simulated with this impairment since any changes to the ideal gain coefficients used caused the structure to become unstable.

Table 5 summarized the results obtained from the plots. The results show that the MASH-2 and MASH-3 modulators are the least sensitive to feedback gain variations as far as maximum and minimum SNR values are concerned. All the cases,

however, show a significant decrease in the maximum input voltage. This is expected due to the reduced value of the gains. The DISDM structure is more sensitive to the variation of gain, although not nearly as much as the TISDM.

The MASH-3 modulators provide the best results with this impairment, therefore, if there is a known problem with obtaining precise values of feedback gain, one of these structures would be the appropriate choice for implementation.

SIMULATIONS WITH FEEDBACK GAIN VARIATION AT 0.25						
	MASH-1	SISDM 4 LEVEL	MASH-2 HAYASHI	DISDM	MASH-3	MASH-3 LONGO
MAX. SIGNAL (dB)	71	71	71	63	71	71
HIGH NOISE LEVEL (dB)	-51	-51	18	28	18	20
LOW NOISE LEVEL (dB)	-52	-75	-44	-47	-49	-43
SNR DELTA (dB)	47	66	31	56	7	6
MAX. INPUT VOLTS (dB)	-13	-13	-13	-1	-26	-26
MAX. SNR (dB)	53	67	73	73	75	74
MIN. SNR (dB)	-7	-12	29	16	42	42

Table 5A - Feedback Gain Variation

SIMULATIONS WITH FEEDBACK GAIN VARIATION AT 0.5						
	MASH-1	SISDM 4 LEVEL	MASH-2 HAYASHI	DISDM AT 1	MASH-3	MASH-3 LONGO
MAX. SIGNAL (dB)	69	69	69	66	69	69
HIGH NOISE LEVEL (dB)	-50	15	30	25	30	28
LOW NOISE LEVEL (dB)	-98	-29	-41	-48	-41	-40
SNR DELTA (dB)	55	65	46	39	35	35
MAX. INPUT VOLTS (dB)	-7	-6	-6	-7	-7	-7
MAX. SNR (dB)	56	59	73	36	85	85
MIN. SNR (dB)	-6	-12	21	-10	43	43

Table 5B - Feedback Gain Variation

Figure 106. MASH-1 - Power Spectrum with Feedback Gain Variation At 0.25

Figure 107. MASH-1 - SNR' Curve with Feedback Gain Variation At 0.25

Figure 108. SISDM 4 Level Quantizer - Power Spectrum, with Feedback Gain Variation At 0.25

Figure 109. SISDM 4 Level Quantizer - SNR' Curve with Feedback Gain Variation At 0.25

Figure 110. MASH-2 - Power Spectrum with Feedback Gain Variation At 0.25

Figure 111. MASH-2 - SNR' Curve with Feedback Gain Variation At 0.25

Figure 112. DISDM - Power Spectrum with Feedback Gain Variation At 0.25

Figure 113. DISDM - SNR' Curve with Feedback Gain Variation At 0.25

Figure 114. MASH-3 - Power Spectrum with Feedback Gain Variation At 0.25

Figure 115. MASH-3 - SNR' Curve with Feedback Gain Variation At 0.25

Figure 116. MASH-3 Longo - Power Spectrum with Feedback Gain Variation At 0.25

Figure 117. MASH-3 Longo - SNR' Curve with Feedback Gain Variation At 0.25

Figure 118. MASH-1 - Power Spectrum with Feedback Gain Variation At 0.5

Figure 119. MASH-1 - SNR' Curve with Feedback Gain Variation At 0.5

Figure 120. SISDM 4 Level Quantizer - Power Spectrum with Feedback Gain Variation At 0.5

Figure 121. SISDM 4 Level Quantizer - SNR' Curve with Feedback Gain Variation At 0.5

Figure 122. MASH-2 - Power Spectrum with Feedback Gain Variation At 0.5

Figure 123. MASH-2 - SNR' Curve with Feedback Gain Variation At 0.5

Figure 124. DISDM - Power Spectrum with Feedback Gain Variation At 1

Figure 125. DISDM - SNR' Curve with Feedback Gain Variation At 1

Figure 126. MASH-3 - Power Spectrum with Feedback Gain Variation At 0.5

Figure 127. MASH-3 - SNR' Curve with Feedback Gain Variation At 0.5

Figure 128. MASH-3 Longo - Power Spectrum with Feedback Gain Variation At 0.5

Figure 129. MASH-3 Longo - SNR' Curve with Feedback Gain Variation. At 0.5

4.5 COMPARATOR INPUT OFFSET

This section covers another type of impairment which does not pertain to the op amp as those that have been described thus far. The impairment described is the comparator input offset.

Comparator input offset is a constant dc voltage difference at the comparator input. This is simulated by adding a small dc value to the comparator input before deciding whether the output is a + or - 1 V.

In general, comparator offset does not degrade the circuit performance. The values used for the simulations with comparator offset were 0.01, 0.25, and 0.5. With these values, the changes from the ideal case are not significant. Table 6 summarizes the results. The single stage modulators results have been omitted since the structures are not suitable for the ADC structures desired and also since their results did not differ much from ideal.

Also only one set of comparator offset plots have been included. Figures 130 through 139 are the plots for an offset of 0.5, the other values have not been included because they are redundant.

SIMULATIONS WITH COMPARATOR INPUT OFFSET AT 0.5					
	MASH-2 HAYASHI	DISDM	MASH-3	MASH-3 LONGO	TISDM
MAX. SIGNAL (dB)	63	63	63	63	60
HIGH NOISE LEVEL (dB)	30	28	40	35	30
LOW NOISE LEVEL (dB)	-47	-47	-47	-46	-49
SNR DELTA (dB)	43	53	40	42	26
MAX. INPUT VOLTS (dB)	-9	-5	-4	-4	-13
MAX. SNR (dB)	68	74	83	84	83
MIN. SNR (dB)	16	16	39	38	44

Table 6 - Comparator Input Offset

Figure 130. MASH-2 - Power Spectrum with Comparator Input Offset At 0.5

Figure 131. MASH-2 - SNR' Curve with Comparator Input Offset At 0.5

Figure 132. DISDM - Power Spectrum with Comparator Input Offset At 0.5

Figure 133. DISDM - SNR' Curve with Comparator Input Offset At 0.5

Figure 134. MASH-3 - Power Spectrum with Comparator Input Offset At 0.5

Figure 135. MASH-3 - SNR' Curve with Comparator Input Offset At 0.5

Figure 136. MASH-3 Longo - Power Spectrum with Comparator Input Offset At 0.5

Figure 137. MASH-3 Longo - SNR' Curve with Comparator Input Offset At 0.5

Figure 138. TISDM - Power Spectrum with Comparator Input Offset At 0.5

Figure 139. TISDM - SNR' Curve with Comparator Input Offset At 0.5

4.6 COMPARATOR DEAD ZONE

A comparator dead zone is the final impairment applied to the ideal simulations. A dead zone of 40% was used in the simulations. All the comparators in the circuit were replaced with an IF statement such that if the comparator input was greater than 0.4 V the comparator would function and produce the required 1 V output. If the value was less than 0.4 V but greater than -0.4 V then no new comparator output would be generated and the previous value would be used. If the value was less than -0.4 V then the comparator would function and a -1 V would be generated at its output.

With this comparator in place the dead zone simulation was performed. The results are tabulated in Table 7 and the plots are included in figures 140 through 151 at the end of this section. In most of the structures the maximum input voltage was reduced. This, however, was not the case for the MASH-2 comparator offset simulation where the maximum input voltage remained the same. The offset really had no effect on the MASH-2 simulation. The only difference was 1 dB in the maximum SNR. The remaining structures all had a lower value for the maximum SNR. In general, this impairment did not cause any severe problems with the circuits.

SIMULATION RESULTS FOR COMPARATOR DEAD ZONE						
	MASH-1	MASH-2 HAYASHI	DISDM	MASH-3	MASH-3 LONGO	TISDM
MAX. SIGNAL (dB)	63	63	63	63	63	60
HIGH NOISE LEVEL (dB)	-75	30	28	38	32	30
LOW NOISE LEVEL (dB)	-90	-47	-47	-47	-47	-49
SNR . DELTA (dB)	70	56	50	27	26	24
MAX. INPUT VOLTS (dB)	-1	-1	-5	-10	-10	-17
MAX. SNR (dB)	59	73	64	79	78	75
MIN. SNR (dB)	-12	16	9	42	42	36

Table 7 - Simulation with Comparator Dead Zone

Figure 140. MASH-1 - Power Spectrum with Comparator Dead Zone

Figure 141. MASH-1 - SNR' Curve with Comparator Dead Zone

Figure 142. MASH-2 - Power Spectrum with Comparator Dead Zone

Figure 143. MASH-2 - SNR' Curve with Comparator Dead Zone

Figure 144. DISDM - Power Spectrum with Comparator Dead Zone

Figure 145. DISDM - SNR' Curve with Comparator Dead Zone

Figure 146. MASH-3 - Power Spectrum with Comparator Dead Zone

Figure 147. MASH-3 - 'SNR' Curve with Comparator Dead Zone

Figure 148. MASH-3 Longo - Power Spectrum with Comparator Dead Zone

Figure 149. MASH-3 Longo - SNR' Curve with Comparator Dead Zone

Figure 150.. TISDM - Power Spectrum with Comparator Dead Zone

Figure 151. TISDM - SNR' Curve with Comparator Dead Zone

5.0 CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

Oversampled sigma delta modulator structures have been simulated and compared in the scope of this thesis. It has been stated that the basic single stage modulators MASH-1 and SISDM with four levels of quantization are not suitable for ADC's in the ISDN environment since they cannot obtain the required resolution to recover the far end signal in an environment where the near end echo is 50 dB greater. They can be useful in alternative applications where the specifications are less strict.

The two stage, MASH-2 modulator and the double integration, DISDM modulator provide much better results. They each have impairments that affect their operation which must be considered when choosing between the two of them. The DISDM structure is very sensitive to op amp offset while the MASH-2 structure is more sensitive to op amp saturation. Another impairment that affected the structures differently was limited bandwidth which affected the DISDM structure but had no affect on the MASH-2. The remaining impairments affect the performance of both circuits in a similar manner, as tabulated in chapter 4. Generally, the SNR is reduced and the maximum input voltage tolerated is lowered. These structures could be used in the ISDN environment although their performance may not always meet all the requirements.

The best results were obtained from the three stage and triple integration sigma delta modulators. These structures meet the required specifications for the ISDN environment and should be able to convert the desired signal plus echo without losing the signal. The TISDM provided the best results under ideal conditions but became unstable when certain impairments were introduced. The op amp offset and gain variations created the worst problems for this circuit since the values of the gains were crucial to its stability. The impairment which had the least adverse affects on this circuit was the op amp saturation, which is due to the fact that the input gain was very small, 0.09. This implied that the inputs stayed within the saturation limits almost all the time. The limited bandwidth impairment also had a small adverse affect on this structure.

The two three stage modulators, MASH-3 and MASH-3 Longo, have similar results with respect to each other. The results are slightly worse than those obtained for the ideal TISDM. The effect of the impairments on these multiple stage modulators, however, is far less severe. They are least effected by op amp offset and gain, opposite to the TISDM case, and most effected by saturation. As long as the saturation level can be appropriately chosen, these circuits are far more stable for use in the ADC. The multiple stage modulators are far more tolerant of circuit imperfections and mismatching of components, therefore, they are much eas-

ier to implement. They do not have a natural tendency to lock into an unstable operating region as does the TISDM due to multiple levels of feedback. The TISDM structure has one good advantage in that there are only two output levels, therefore, the decimation filter circuitry is much smaller in size and simpler in complexity. The other impairments do not really favour one implementation over the other. The comparator input offset had little effect on any of the structures simulated and the comparator dead zone reduced the dynamic range and maximum SNR in all the cases.

The choice between which of the three stage modulators or the TISDM must finally be based on the fabrication technology available. If access to extremely high precision tools are available and optimum values for the gain coefficients can be arrived at, the TISDM structure would be a suitable choice, remembering its tendency to lock into unstable modes of operation and taking the appropriate actions to avoid such states. This tendency can only be overcome with extreme care to the construction of the circuit. TISDM will provide the best performance results given that all the circuit impairments are minimized and are as close to ideal as possible.

On the other hand, the MASH-3 and MASH-3 Longo structures provide nearly as good results without the added care and expense required in the fabrication process. These struc-

ture, however, require a larger surface area because there are physically more components. They also require a more complicated decimation filter. These structures, however, are far more tolerant of imperfections in the fabrication process which gives them a great advantage over the TISDM structure. Deciding between the two MASH-3 structures, requires only deciding whether the added physical size of the MASH-3 modulator is worth the gains obtained by eliminating the common mode noise, the effects of which are not covered in the scope of this work.

It appears from this study that the final choice should be made dependent on the application specifications and the fabrication technology available to meet the specifications. Each of the structures has advantages in its favour. Given an adequate fabrication process and not too great a size restriction, the MASH-3 Longo would be the most promising candidate for fabrication.

Future work could involve a more detailed study into the effects of gain variation which was briefly looked into in the scope of this work. It may be possible to optimize the gains so as to improve circuit performance as in the TISDM case. This perhaps could be tried for the multiple stage modulators. Other work could involve evaluating higher order structures to analyze their behaviour in ideal simulations as well as with circuit impairments. Another

possible project would be to fabricate the structures simulated to see whether they actually behave as predicted by the simulations performed.

APPENDIX A. THE FFT ALGORITHM

The FFT algorithm used in the simulations was the standard IMSL routine FFTRC whose function is to perform the fast fourier transform of a real valued sequence. The routine is double precision and calculates half of the transform coefficients. The following formula is used to compute the FFT of x:

$$x(k+1) = \sum_{j=0}^{n-1} a(j+1) * \text{cexp}((0.0, (2.0 * \pi * j * k) / n))$$

where a is the sampled output signal and

for $k = 0, 1, \dots, n/2$ and $\pi = 3.1415\dots$

APPENDIX B. THE BLACKMAN-HARRIS WINDOWING FUNCTION

The windowing function was applied in the simulations to overcome the effects of spectral leakage associated with a finite observation interval [7]. Eventhough even multiples of the sine wave were used so that the sine wave boundary would be zero, it was found that the calculated value was not exactly zero. Applying the window ensured that the boundary value was zero and the data continuous.

The window chosen for these simulations is called the Blackman-Harris window. The particular window used was the minimum four term window which could achieve a sidelobe level of -92 dB. Therefore, no sidelobes caused by the windowing appear in the simulations. This window as stated in [7] is suprisingly good for the small number of terms in its trigonometric series. The series used is given by the following equation:

$$w(n) = a_0 - a_1 \cos(2\pi n/N) + a_2 \cos(4\pi n/N) - a_3 \cos(6\pi n/N)$$

where $n = 0, 1, \dots, N-1$

and the coefficients are:

$$a_0 = 0.35875$$

$$a_1 = 0.48829$$

$$a_2 = 0.14128$$

$$a_3 = 0.01168$$

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