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A WIDEBAND PARALLEL
SAMPLING SYSTEM

by

Paul Langner, B.Eng., P.Eng.

A thesis submitted to
the Faculty of Graduate Studies and Research
in partial fulfilment of
the requirements for the degree of

Master of Engineering

Department of Electronics

Carleton University
Ottawa, Ontario
March, 1990

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"A WIDEBAND PARALLEL
SAMPLING SYSTEM"

submitted by Paul Langner B.Eng., P.Eng.
in partial fulfilment of the requirements for
the degree of Master of Engineering

Thesis Supervisor

Chair, Department of Electronics

Carleton University
March, 1990

ABSTRACT

The operational bandwidth of contemporary flash ADCs is limited by the response time of a critical component: the comparator. As well, difficulties in incorporating a fast track and hold amplifier into the front end of an ADC also limits performance. In order to overcome this limitation it is possible to operate several ADCs in parallel.

In this thesis, the theory and design of a parallel sampled data system are presented and a prototype constructed. As well, a numerical analysis of the overall system is developed and a program presented which incorporates this analysis. In addition, a novel bipolar impulse generator used in the system is described. Finally, the practical results obtained from the prototype are presented and compared with theory and good agreement is demonstrated.

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LIST OF SYMBOLS

a_{mn}	matrix variables
A	amplitude
A, B, C, D	parameters in an $ABCD$ matrix
A_n	an amplifier
$\bar{B}$	normalized susceptance
c	the speed of light in free space $\approx 3 \times 10^8$ m/s
C	capacitance
C_g	gate-to-channel capacitance in a FET
C_j	junction capacitance of a diode
C_{j0}	zero bias junction capacitance of a diode
C_n	a capacitor
C_p	parasitic package capacitance
C_o	distributed capacitance of a transmission line
C_v	capacitance of a varactor diode
C_{VR}	reverse bias capacitance of a varactor diode
d	indicates a derivative or a distance
d_m	spacing between taps on the meander line
D_n	a diode
e	base of the natural logarithm ≈ 2.71828
f	frequency
$f_n(\cdot)$	a function
f_s	sampling frequency
f_{si}	sampling frequency of individual tap
$f(t)$	time domain signal
F_n	a filter
$F(\omega)$	frequency domain signal equivalent to $f(t)$

LIST OF SYMBOLS (cont'd)

$F\{ \cdot \}$	indicates a Fourier transform
i	current or an integer
i_b	bias current
I_n	the current at the nth node in a periodic structure
I_s	diode reverse leakage current
j	the square root of -1: an imaginary number
J	the Jacobian of a matrix
k	Boltzmann's constant $\approx 1.38 \times 10^{-23}$ J/°K or an integer
k_0	free space propagation constant
K_n	a parameter in a numerical algorithm
l	length
l	an integer
L	inductance
L_n	an inductor
L_0	distributed inductance of a transmission line
L_p	parasitic package inductance
m	an integer
n	a diode ideality constant or an integer
Q_n	a transistor
$\text{rect}(t)$	a periodic aperture function: $\text{rect}(t \leq 1) = 1$ $\text{rect}(t > 1) = 0$
R	resistance
R_n	a resistor
R_s	real part of a source impedance or a series resistance
R_{Term}	termination resistance
$s(t)$	a positive-going, periodic sampling spike
$s^*(t)$	a negative-going, periodic sampling spike
$s_i(t)$	a time shifted version of $s(t)$

LIST OF SYMBOLS (cont'd)

$Sa(x)$	function equivalent to $\frac{\sin(x)}{x}$ or $\text{sinc}(x)$
S_n	Fourier series spectral amplitudes of $s(t)$
SNR	signal to noise ratio
$S(\omega)$	frequency domain signal equivalent to $s(t)$
t	time
t_d	the time between taps on the firing line
t_m	the time between taps on the meander line
T	period of a periodic signal or temperature
T_0	time between samples in the overall system
T_w	pulse width
v	time varying voltage
v_g	group velocity
V	DC voltage
$V_{A,B,C,D}$	voltages at specific points on a diode bridge
$V_{A,B,C,D}^i$	voltages at specific points on a diode bridge at time i (indicating the present)
V_b	bias voltage
V_{br}	diode reverse breakdown voltage
V_l	the amplitude of a voltage spike causing loss
V_m	a voltage margin
V_n	the voltage at the n th node in a periodic structure
V_r	a reverse bias voltage
V_T	diode voltage drop at 1 mA forward current
x	a variable
Y_{in}	input admittance
$\bar{Y}_0$	normalized characteristic admittance
Z	impedance

LIST OF SYMBOLS (cont'd)

Z_f	characteristic impedance of a firing line
Z_{in}	input impedance
Z_0	characteristic impedance
α	attenuation constant in nepers/m
β	propagation constant of structure
γ	complex propagation constant = $\alpha + j\beta$
$\delta(t)$	Dirac delta function: $\delta(t=0) = 1$, $\delta(t \neq 0) = 0$
ϵ	an arbitrary small number
ϵ_r	relative dielectric constant
θ	electrical length in radians
λ	wavelength
λ_0	free space wavelength
Λ	diode constant = $\frac{q}{nKT} = 0.0259$ at $T = 25^\circ\text{C}$
π	pi ≈ 3.14159
Σ	indicates a summation
τ	length of delay in a delay line or aperture time
ϕ	signal phase
ϕ_n	clock phase
ω	radian frequency
ω_0	radian frequency of a periodic signal
ω_p	radian sampling frequency of individual tap
Δ	indicates a difference
Δt	a time step in a numerical simulation
∂	indicates a partial derivative
∞	infinity
$\int$	indicates an integration

CHAPTER 1: INTRODUCTION

1.1 Introduction

One method of achieving ultra-high-speed analogue to digital conversion (where ultra-high-speed is defined as having a conversion rate in excess of 1 Gigasamples/second) is to use a parallel sampling scheme. Parallel sampling involves sharing the sampling burden amongst a number of identical slower analogue-to-digital converters (ADCs). In order to accomplish this sharing it is necessary to equip each ADC with an ultra high speed sample and hold (S/H) circuit at its input and synchronize the timing between the individual ADCs. Thus each S/H circuit samples the incoming waveform at the correct point on the waveform and holds it long enough for the slower ADC to perform the conversion upon the signal.

There are several problems associated with the construction of such a parallel sampling circuit. Some of the most critical ones are:

- a) The synchronization in time of individual S/H circuits.

- b) The need to match the performance of each channel to that of all the other channels.
- c) The leakage of the firing signal through the sampling gates.
- d) The slew rate limitations of the sampling gates and the hold amplifiers.
- e) The voltage droop of the S/H amplifiers during the hold period.
- f) The DC response of the hold amplifiers. (Sometimes there are relatively large DC offsets associated with hold amplifiers).
- g) The dispersive properties of periodically loaded structures. (This will be explained later.)

In this thesis, these problems and others not listed are addressed and a practical solution is explored.

In Section 1.2, the background and objective of the thesis is presented in greater detail, while the thesis organization is outlined in Section 1.3. Finally in Section 1.4 a statement of originality is given.

1.2 Background and Objective

The first attempts to develop an ultra-high-speed sampler occurred in the 1950s and were a result of efforts to create a sampling oscilloscope that would be able to sample microwave signals¹. These early approaches all utilized some sort of silicon diode sampling gate approach, but the physical implementation of the techniques were such that they could not be easily utilized in a parallel sampling scheme. The first ultra-high-speed parallel sampling scheme that operated reasonably well was designed by Conway², and was constructed using six-diode bridges that were placed along what was termed a meander line. This work was part of a continuing effort by electronic warfare organizations to develop a digital radio frequency memory (DRFM). A DRFM is a device which performs analogue-to-digital conversion upon a radar signal, stores the result in memory, and then is capable of recreating an exact but delayed copy of the original signal by means of an ultra-high-speed digital to analogue converter (DAC). DRFMs are one of the main driving forces behind attempts to create ultra high speed ADCs.

The objective of this thesis is to present the background theory and development of a 1.2 Giga-sample/second parallel sampling system for use with 100 MHz,

4-bit ADCs. The sampling system was intended to meet the following target specifications:

1) Input frequency -	50 - 550 MHz
2) Input impedance -	50 Ω
3) Number of bits of quantization -	4
4) Input power for full scale -	+10 dBm

From these specifications it can be seen that the choice of 1.2 Gs/sec system was made so that the input could be equipped with a realizable anti-aliasing filter. If 100 MHz ADCs were selected, a 12-channel parallel sampling system would have been required.

1.3 Thesis Organization

Chapter 2 of this thesis discusses possible approaches to the problem, while Chapter 3 presents the theory behind the approaches introduced in Chapter 2. In Chapter 4, the implementation of the prototype parallel sampling system is presented, and in Chapter 5 measurements on the system are compared with theory. Finally, Chapter 6 contains conclusions and a summary of the results, plus recommendations for future work.

1.4 Statement of Contribution

Unless otherwise stated, all of the material dealing with parallel sampling systems that is presented in this thesis is the result of original work performed by the author over the period 1986 to 1990.

CHAPTER 2: METHOD

2.1 Introduction

Parallel sampled data schemes have never enjoyed much popularity. Perhaps one of the reasons for this is the inevitable complexity involved and the fact that in order to fabricate such a system an ultra-high-speed S/H is required together with the circuitry capable of driving such a device. As mentioned previously, the first full-scale parallel sampling system appears to be the one designed by Conway. This was a prototype that was designed solely to demonstrate the feasibility of such a system. The first commercial parallel sampling system that was constructed and actually incorporated into a product (as far as the author is aware) was a 10-channel board designed and constructed by Cloutier³ in 1985 at Telemus Electronic Systems Inc. This board utilized NEC NE710 GaAs FETs as the sampling gates in the S/H circuit and utilized a meander-line structure to provide the correct timing to the sampling gates.

2.2 Parallel Sampling Schemes

2.2.1 Two Approaches

All parallel sampling schemes rely on some means of sharing the sampling burden amongst several S/H circuits. There are two approaches to this sharing. The first approach is a dual-rank scheme (the rank of a system defines the number of S/H operations that are performed upon a sample before it is digitized by an ADC). It involves having a single ultra-high-speed S/H performing all of the sampling on the incoming signal as shown in Figure 1. Its output is fed into a hold amplifier which then fans out to drive several slower parallel S/H amplifiers. These amplifiers in turn drive the parallel ADCs. The system operates from a two phase clock. The first phase of the clock, ϕ_1 , drives the first rank S/H circuit. The second phase of the clock is distributed to the parallel channels by a Johnson type encoder (see the timing diagram in Figure 1) and lags ϕ_1 by 90° . The result of this is that channel A will be "handed" the first sample, channel B will be handed the second sample and so forth.

The second method of performing parallel sampling is a single-rank method. This is shown in its simplest form in Figure 2. Basically, each channel is fed from a common input

$$\phi_1 = J \sum_{n=a}^b \phi_{2n}$$

Note that sampling occurs on falling edge.

Figure 1: A dual rank parallel sampling scheme.

amplifier (a normal high drive-current amplifier, not a hold amplifier), and each channel individually samples the incoming amplified RF signal. The requirement of this method is that each channel's S/H circuit must be capable of directly sampling the input signal.

2.2.2 Comparison of Two Approaches

The two approaches both have certain merits and drawbacks. Theoretically they are identical, but in reality the dual rank method can produce a better performing sampling system than the single rank system. The reason for this is that the dual rank system is almost immune to timing skew problems because only one sampler running from one clock at the overall sampling frequency is performing the sampling, whereas the single rank method relies on each channel to perform its own sampling. This means that each channel's sampler has to be synchronized to within picoseconds of the other samplers.

Unfortunately a dual rank sampler is technically more difficult to build than the single rank sampling system. This is due to the requirement in the dual rank sampler of a single ultra-high-speed S/H circuit. The actual sampler (as will be seen later) is not difficult to construct, but the hold amplifier that is required to buffer the output of the

Note that sampling occurs on falling edge.

Figure 2: A single rank parallel sampling scheme.

first sampler is. As a matter of fact, at the time that this work was being undertaken this amplifier (for the system being designed) was impossible to realize. Thus the second approach was chosen.

2.2.3 Variations on Single Rank Parallel Samplers

As suggested before when it was said that Figure 2 demonstrated the single rank sampler in its simplest form, there are several different ways to realize a single rank sampler. The first and most obvious way is to have all of the parallel channels sampling the incoming RF signal at a single point in space. The parallel sampling is achieved by using the Johnson phasing of the sampling clock to correctly time each channel. (This refers to the phasing of the clocks as seen in the timing diagram in Figure 2. This sort of timing would be typically generated in a Johnson counter.)

The first variation on the architecture of Figure 2 is to realize the correct timing of the parallel channels by attaching all of the channels to the first phase of the sampling clock (ϕ_{1a}) and serially feeding this phase to each of the other channels via delay lines with a delay of τ , the sampling interval. This is shown in Figure 3.

Note that sampling occurs on falling edge.

Figure 3: A single rank parallel sampling scheme with delayed sampling clock.

By looking at Figures 2 and 3, it may not be obvious how to find new variations on these two sampling architectures. The first clue to seeing how other architectures are possible is to realize that the input signal is not just present at one point in space, but like all electromagnetic radiation is a wave function with both a temporal and a spatial component. Thus if we wish to sample the RF signal at some sampling interval T , and we wait at the input of a single rank sampling system, every T seconds the sampling point on the RF waveform will arrive. However, if we could "look back" down the input signal line, we would "see" all of the points that will be sampled in the near future travelling towards us at the velocity of the wave in the medium. This is the key to producing variations on the single rank sampling architecture.

The second variation uses this principle and has each parallel sampler (hereafter referred to as "taps") attached to a different place on the incoming signal line. Each tap is fed from the same sampling clock with a parallel, equal-length feed, and samples the incoming signal at the same time. The timing between channels is done by spacing each tap on the incoming signal line exactly T seconds apart. This is shown in Figure 4 and produces exactly the same sampling results as Figures 2 and 3.

Note that sampling occurs on falling edge.

Figure 4: A single rank parallel sampling scheme and series input feed.

By combining the serial clock feed concept from Figure 3 with the spatially separated taps of Figure 4, one obtains a structure that can be termed a "meander line". A meander line is just a special case of a generic spatially-separated parallel sampler. An example of this structure is shown in Figure 5. The equation in this figure relating the length of the delays will be explained in the next chapter.

2.2.4 Spatially-Distributed Samplers

Spatially-distributed samplers can best be visualized by imagining the situation that occurs when you are travelling down a highway in an automobile and you meet a train made up of boxcars on tracks beside the highway. In this analogy the train is the RF signal, the boxcar doors are the desired sampling points on the signal, and you in your car are one edge of the sampling clock. Every time that you pass a boxcar door a sample should be taken. In a spatially-distributed sampler the distance between the taps would be the distance along the highway between your samples. For a train and a car, a proper sampling scheme can be arrived at for all possible velocity combinations of car and train (whether they are travelling in the same direction or in opposite directions) except when the car and train are travelling in the same direction and at the same speed.

Note that sampling occurs on falling edge and that f_s is the overall sampling frequency of the system. This is also the frequency of ϕ_1 .

Figure 5: A single rank parallel sampling scheme with delayed sample clock and series input feed.

For TEM electromagnetic signals, the velocity of the signal is determined by the dielectric constant of the medium that it is propagating in. If the RF signal line and the sampling clock signal line coexist in the same dielectric medium and are parallel to each other (as in the highway/railway track scenario), then there is only one possible tap-spacing solution to this problem, and this only occurs when the signals are travelling in opposite directions. In order to arbitrarily set the tap spacing along the lines, it is necessary (for physical realizability) to alter the velocities of the two signals with respect to each other. This can be achieved by making the path lengths between the taps different for the sampling clock and the RF signal. Thus one of the lines will meander between the taps and the other will travel in a straight line (it is possible for both to meander, but little is gained by this). Another method is to slow one of the signals down by altering the dielectric constant of the medium in which it is travelling.

Before we begin discussing the advantages and disadvantages of the various approaches, let us examine one last possible approach to constructing a spatial sampler. This approach is shown in Figure 6. It utilizes a combination of temporally and spatially separated clocks. In this example, four Johnson-phased clocks are generated from a master clock running at half of the desired sampling

Note that sampling occurs on falling edge.

Figure 6: Cobweb sampler.

rate. These four clocks each in turn drive two sampling gates (taps), spatially separated along an input line. The most convenient physical realization of this structure leads to what is referred to as a "cobweb" sampler. Again, the theory covering this particular structure will be dealt with in the next chapter.

2.2.5 Selection of Single Rank Samplers

As was mentioned in Chapter 1, the desired sampling rate of the entire system was 1.2 Gsample/sec and the ADCs that were selected for each of the parallel channels operated at 100 MHz. The implication of this was that 12 parallel S/H channels were required. The first sampler to be considered was the single point (non-spatially distributed) Johnson-phased sampler (Figure 2). In order to use this sampler, a broadband 12-way RF power divider would have been required that would in turn have fed each channel through a matched length of line. For any type of planar PC board structure, this implied that some sort of "spoked wheel" arrangement would be required. This on its own was overly onerous, but what became a problem was the generation and distribution of the twelve Johnson-phased clock signals. This would have required a 1.2 GHz Johnson counter and in 1986 this meant that GaAs flip flops would have to have been used. At the

time these devices were new and difficult to work with. Thus the single point sampler was discarded.

The next sampler investigated was the single-point, serially-fed sampler shown in Figure 3. In terms of physical realizability, this sampler was similar to the Johnson-phased single point sampler of Figure 2. The only difference was that in this circuit the sampling clock pulses could have been generated from a lower frequency clock, and the distribution of the clock pulses could have been done via a series of timed-length lines connected to each of the taps in series. A sketch of this is shown in Figure 7. Because of the "spoked wheel" requirement for the layout, this approach was also abandoned as the spatially-distributed approaches yielded a more favourable component layout.

The next structure considered was the one shown in Figure 4. In this sampler, the taps were spatially distributed, but the sampling clock would have to have been power split amongst the parallel channels and distributed along matched-length lines. The problem with this was that a broad-band power divider circuit with a bandwidth that extended from 100 MHz to over 10 GHz would have been required in order to handle the narrow sampling pulses of the clock. This implied that a resistive divider would have been

Figure 7: Spoked sampler.

needed and the losses inherent in resistive dividers were intolerable. Because of this, this method was also abandoned.

The next structure that was considered was a fully spatially-distributed sampler as shown in Figure 5. This sampler could have been realized as two parallel lines with opposing signals on the same substrate, or two parallel lines with opposing or non-opposing signals on different substrates, or as a meander line with opposing or non-opposing signals on the same substrate. The multiple substrate approach was discarded due to the difficulty of fabricating a multilayer board with different substrates. In addition, to achieve any significant delay differences, a high dielectric constant substrate (such as barium tetratitanate) would have been required as one of the substrates. The biggest problem with using this sort of substrate was that the line widths for a 50 Ω line became extremely small when compared with a similar thickness, low dielectric constant substrate. For instance, for a .020" thick substrate with an ϵ_r of 70, the line width for a 50 Ω line would have been 42 μ inches. This would have been far too small to work with. (It can be seen that the propagation velocity of a substrate varies with the square root of the dielectric constant, but the line width for a 50 Ω line varies directly with the dielectric constant). After

discarding these two ideas. the only remaining candidate structures were the parallel lines or meander line approach on similar substrates. The parallel lines idea would have been physically too large to fabricate, so the meander line was the only remaining possibility. For the meander line with both of the signals travelling in the same direction, the structure was still too large. so the meander line with opposing signals was the structure chosen.

The only other structure that had not been abandoned was the cobweb structure shown in Figure 6. This was discarded because it was found that the structure required the use of a multilayer board with vias. This created a problem as the transit-time through the vias was not sufficiently well characterized to allow the structure to be implemented. As well, there were anticipated difficulties in controlling the timing jitter between the Johnson-phased channels. This jitter would have led to a degradation in performance.

Hence the spatially distributed meander line sampler was chosen as the best way to implement the 12 channel, 1.2 Gsample/sec parallel sampling system.

2.3 Sample and Hold Circuits

A sample and hold circuit is a circuit that ideally will sample a waveform at a given point in time and hold the sampled value for as long as desired. The term "sampling window" describes the length of time that the sampling gate is open. Ideally this time is zero. Thus an ideal sampling gate would be driven by a delta function. An example of an ideal circuit is shown in Figure 8. In this circuit, the input signal is buffered by amplifier A_1 . The purpose of this buffer is to drive an infinite amount of current through the sampling gate, S_1 during the infinitely short period of time during which it is open. This current will flow through the switch for as long as the voltage at the output of A_1 is different from the voltage across the capacitor. Thus when the switch closes, the voltage across the capacitor will be equal to the voltage present at the input when the sample was taken. This voltage will remain across the capacitor until the sampling gate reopens. In order that the charge on the capacitor does not leak out through the output of the circuit, a second buffer amplifier, A_2 with infinite input impedance is used to buffer the voltage across C_1 . For the parallel sampler, and indeed in most sampling systems, the sampling is done on a periodic basis. Thus for this S/H circuit, the signal controlling the sampling gate would be a series of impulse functions. This is shown in Figure 8 as

$$s(t) = \sum_{n=-\infty}^{\infty} \delta(t-nT)$$

$T = \text{period}$

Figure 8: Generic sample and hold circuit.

the signal $s(t)$. An important characteristic of this ideal circuit is that the signal $s(t)$ is only used to open and close the sampling gate and none of this signal will leak through the sampling gate and corrupt the sampled voltage.

The circuit described in the previous paragraph is obviously unrealizable, but it is the perfect ideal of a S/H circuit. Thus the real-world circuit that is chosen should approximate this circuit as closely as possible.

For the parallel sampling system that was being constructed, there were three possible sampling circuits available, and only one buffer amplifier circuit available. These availability considerations will be explained shortly.

The fastest sampling circuit (not shown) available today is the one used by Hypres in their high frequency oscilloscopes. This sampler operates by measuring the polarization rotation of a reflected laser pulse fired into a crystal substrate (such as GaAs) in the vicinity of a microstrip line conducting the signal of interest⁴. This circuit is an excellent sampler, but it is large and could only be used as the first sampling gate in a dual rank sampling scheme. However the cost and complexity of this circuit prevented it from being considered as a practical alternative.

The second fastest sampling circuit available today is an electro-optic sampler⁵. This sampling circuit (also not shown) relies on electro-optic principles and requires a mode locked Nd:YAG laser to open the sampling gate. The sampling gate in this case would be a photoconductor: typically irradiated intrinsic silicon or chromium doped silicon. The circuit would operate by having the laser photo-electrically generate hole/electron pairs in the silicon. The purpose of the chromium doping and/or irradiation of the silicon is to produce as many crystal defects as possible, and hence a large number of generation sites for hole/electron pairs. A mode-locked laser is a laser that through piezoelectric modulation of its lasing cavity at a frequency equal to the difference between its possible operating frequencies produces a very intense burst of optical energy at the piezoelectric modulation frequency (this principle is similar to how a microscan receiver operates). The intense energy is required in order to produce a sufficient number of hole-electron pairs in the photoconductor to carry the required conduction current. This method, though capable of producing extremely short samples (e.g. several picoseconds long) is very expensive and bulky because of the Nd:YAG laser requirement. As a result it was also discarded as impractical.

Turning to more conventional sampling circuits, there are FET circuits and diode circuits that can be used. The major problem with a FET based circuit is that for very high speed operation there are no viable p-channel GaAs FETs, due to the lack of ballistic hole transport in GaAs. This means that a complementary, balanced FET sampler is impossible to construct. The result of this is that due to the unbalanced nature of the circuit there will be a high degree of sampling-pulse feedthrough and this will corrupt the sample. An example of this type of circuit is shown in Figure 9. Because of the finite gate-to-channel capacitance (C_g) of the FET, the short sampling pulses of $s(t)$ will travel almost unchanged through the GaAs FET and into the hold capacitor (the feedthrough into A_1 is not as important).

One method of overcoming this feedthrough problem to some degree is to construct a multiple gate FET⁶. The purpose of the multiple gates is to attempt to limit the feedthrough signal by providing a capacitive bypass to ground on either side of the central gate (which is where the firing signal is applied). An example of this circuit is shown in Figure 10. Although this circuit appeared to show some promise, the practicality of fabricating three-gate FET devices was out of the question at the time that this work was being done due to financial considerations.

Figure 9: FET-based sample and hold circuit.

Figure 10: Triple-gate based FET sample and hold circuit.

Another method of dealing with the feedthrough problem was to eliminate the hold capacitor and second buffer and replace them with a low pass filter and amplifier as shown in Figure 11. This circuit operates in the following manner: a narrow sample pulse is obtained from Q_1 , the sampling FET, and this pulse has a fixed amount of offset added to it due to the sampling pulse feedthrough via the C_g of Q_1 . This pulse then travels through the lowpass filter and amplifier combination F_1/A_2 , where it is spread out in time and amplified. Thus the pulse arriving at the ADC is stretched out and flattened. With the proper timing between the sampling signal $s(t)$ and the ADC clock, the ADC will sample the signal at the broad peak of the stretched signal. Because the lowpass filter is a linear system, the output of the ADC will directly correspond to the amplitude of the sampled signal. This technique was investigated by Cloutier in 1985⁷, but difficulty was experienced in trying to synchronize the ADC sampling point with the sampling signal $s(t)$. In addition the low peak amplitude of the signals produced by the F_1/A_2 combination significantly reduced the noise immunity of the sampling process. Thus while this method could be pursued, it was felt that a diode sampler would offer better performance.

There are two types of diode samplers available: the four-diode sampler and the six-diode sampler. These are

$$s(t) = \sum_{n=-\infty}^{\infty} \delta(t-nT)$$

T = period

Figure 11: Pulse stretching sampler.

shown in Figures 12 and 13 respectively. Both of these samplers operate in a similar fashion. When the bipolar pulses $s(t)$ and $s^*(t)$ arrive at the diode bridge in Figure 12, they momentarily turn on the bridge. This forces the voltage across C_1 to be equal to the voltage at the output of A_1 while the bridge is turned on. Essentially, the bridge is a current mirror and when a pulse is applied, either diodes D_1 and D_3 are on or diodes D_2 and D_4 are on. Since the bridge diodes are matched, the current mirror configuration forces the input and output voltages to be equal. This process will be covered in depth in the next chapter. The problem with this circuit is that the current used to charge the hold capacitor C_1 is supplied by one of the pulses $s(t)$ or $s^*(t)$. This means that one of the pulses will be reduced in amplitude by a variable amount each time the sampling bridge is fired. While this is acceptable if only one sampling bridge is being used, it is unacceptable for more than one bridge. This would cause the bridges down the line from the first bridge to see unbalanced firing signals and this would degrade performance.

In order to avoid this problem, the circuit shown in Figure 13 can be used. It is essentially the same circuit as Fig. 12, but the difference is that the sampling pulses $s(t)$ and $s^*(t)$ are being used to switch the currents i_1 and i_2 . When the bridge is off, these currents flow through the

$$s(t) = \sum_{n=-\infty}^{\infty} \delta(t-nT)$$

$T = \text{period}$

$$s^*(t) = -\sum_{n=-\infty}^{\infty} \delta(t-nT)$$

Note that the positive sampling pulse $s(t)$ is equal to the inverse of the negative sampling pulse $s^*(t)$.
(i.e. $s(t) = -s^*(t)$)

Figure 12: Four-diode sample and hold circuit.

resistors and on to the sampling pulse lines. When the pulses arrive they reverse bias the diodes D_5 and D_6 . This causes the current to flow through the sampling bridge instead of into the sampling pulse lines. This activates the current-mirroring action mentioned above and the capacitor C_1 is either charged or discharged so that the voltage across it is equal to the voltage at the output of A_1 . This is the circuit that was chosen as the switch for the 12 channel, 1.2 Gsample/sec parallel sampling circuit.

In retrospect, this may not have been the best possible choice as there is a subtle problem associated with this circuit. Basically, when the firing pulses shut off the diodes D_5 and D_6 , the current flowing into the firing lines (the sampling pulse lines) ceases and a pulse is generated in each line that travels in both directions from the sampling bridge. This pulse is opposite in polarity to the sampling pulses, and the half of the pulse that travels in the same direction as the sampling pulse subtracts from that pulse and reduces its amplitude.

To avoid this problem, the diodes D_5 and D_6 could have been replaced by FETs as shown in Figure 14. These FETs would have served the same purpose as the diodes in Figure 13, but the difference is that the current being switched would not have been travelling into the firing lines. Thus

Figure 14: FET switched bridge sample and hold circuit.

the signal would not have been degraded. The other difference between this circuit and that of Figure 13 was that the sampling pulses would have been both negative-going. This was due to the requirement that only n-channel FETs be used.

2.4 Pulse Generation Circuits

To this point we have discussed parallel sampling technology and sample and hold technology. In both of these discussions we have assumed that either unipolar or bipolar sampling pulses of very narrow width were readily available. Unfortunately, as is the case with most real-world circuits, this is easier said than done, especially with bipolar pulse generators.

For the six-diode sample and hold circuit that was chosen for this problem, bipolar firing pulses (or spikes as they are usually called) were required. These spikes had to be very short in duration (i.e. < 600 psec), and had to have an amplitude of around 8 V. There was only one possible sort of circuit that was capable of generating these sort of pulses and this circuit used a step recovery diode (SRD). The theory of operation of an SRD circuit is covered in the next chapter.

In order to produce bipolar spikes with an SRD it is necessary to have the SRD in a balanced environment. The circuit that was settled upon is shown in Figure 15. This circuit operates by using a 100 MHz balun to transform the amplified 100 MHz clock into a balanced signal. The SRD and its matching capacitors are connected across the outputs of the balun transformer. When the SRD fires, bipolar spikes are produced. These spikes then traveled through blocking capacitors and out on to the biased firing lines.

The use of a balanced circuit is probably the only viable way to produce perfectly symmetrical bipolar spikes. Any other method would have relied on two separate SRD circuits, one producing a negative spike and the other producing a positive spike. In order to synchronize these two circuits, some sort of feedback loop would have been required, and the complexity of the circuit would have been too great.

2.5 Summary of Method

After exploring all of the possible options to choose from in constructing a 12 channel, 1.2 Gsample/sec parallel sampling system, it was decided that 12 six-diode sampling gates (with their respective hold circuitry), spatially distributed along a meander line would be used. Each of

Figure 15: Bipolar spike generator.

these sampling gates would then be fired by signals generated by a bipolar spike generator.

CHAPTER 3: THEORY

3.1 Introduction

In this chapter, the various components of the parallel sampling system will be explored and the theory describing them developed. The theory will deal only with the architecture that was selected in Chapter 2 due to the amount of material that has to be covered. The items to be covered include the six-diode sampling switch, the bipolar spike generator, the parallel sampling architecture, and finally the physical layout problems.

3.2 The Six-Diode Sampling Bridge

The six-diode sampling gate (or bilateral Lewis-type diode gate⁸) is shown in Figure 16. As was briefly discussed before, the gate consists of a diode bridge (diodes D_1 through D_4), two switching diodes, (D_5 and D_6) and two bias resistors (R_1 and R_2). In normal operation, one side of the diode bridge (the junction of D_1 and D_2) is connected to the input and the other side of the bridge (the junction of D_3 and D_4) is connected to the output.

The first point in the analysis of this structure is to determine the anti-symmetrical bias voltages, $\pm V_b$. This can

Figure 16: Six-diode sampling gate.

be done by observing that in the OFF state, diodes D_5 and D_6 must be forward biased by the bias voltages $\pm V_b$. These voltages must then be chosen so that all the diodes in the bridge are reverse biased for all possible input voltages. Thus (referring to Figure 16) we can write:

$$V_{BMAX} - V_D \leq -V_r \quad (1)$$

where V_r is defined as a sufficient reverse bias voltage to ensure that the diodes are never forward biased. V_D is the voltage at point D, and V_{BMAX} is the maximum voltage that will be seen at the input (point B). As well we must ensure that we never cause any of the diodes in the bridge to go into reverse breakdown. Defining V_m as the allowed voltage margin, V_{BMIN} as the minimum voltage that will be seen at point B, and V_{br} as the diode breakdown voltage we can write:

$$V_{BMIN} - V_D \geq V_{br} + V_m \quad (2)$$

Now when D_5 and D_6 are forward biased, we have:

$$V_D = V_b - V_T \quad (3)$$

where V_T is the diode voltage drop. Combining (1) - (3) we can then write:

$$(V_{BMAX} + V_T + V_r) \leq V_b \leq (V_{BMIN} + V_T - V_{br} - V_m) \quad (4)$$

With (4) we can now determine what the allowed bias voltages on the firing spike lines are. For our situation $V_r = 0.5$ Volts and $V_m = 1.0$ Volt is a good assumption.

The next parameter that must be chosen is the amplitude of the firing spikes. These bipolar spikes (represented in Figure 16 as $s(t)$ and $s^*(t)$) must be selected so that when they are present at D_5 and D_6 they will reverse bias these diodes and force the bridge to turn on. The minimum condition for this to occur can be written as:

$$s(t) - V_b = -s^*(t) + V_b \geq V_{BMAX} \quad (5)$$

This now leads us to the requirement for the charging voltages, $\pm V$. In order for (5) to be true, we must have:

$$V \geq s(t) - V_b \quad (6)$$

The final item that must be chosen is the value of the charging resistors, R_1 and R_2 . So far the requirements for the parameters of the sampling gate have been easily derived. However, the resistor value is a more complex problem. Basically, the choice of the resistance is a tradeoff between how much current the output requires and how much current the firing spike lines can handle. We will deal with the second issue first.

In the architecture selected for the parallel sampling system, all of the parallel taps were connected in series along the bipolar firing lines. These lines were biased so that the DC voltage on the line was either $+V_b$ or $-V_b$, depending on which line was being observed. A simplified version of one tap of the positive firing line circuit is shown in Figure 17. The exact same situation applies to the

Figure 17: Equivalent circuit of the upper half of the six diode sampling gate in the OFF state.

negative firing line but in reverse. What is happening in this circuit (as will be discussed in more detail later) is as follows. The taps are all connected together in series along the firing line which has an impedance of Z_f . The DC bias circuit is attached to the firing line through an RF choke, L_1 . Its RF termination and source resistors, R_{f1} and R_{f2} , are isolated by the DC blocking capacitors C_1 and C_2 . These capacitors are chosen so that they appear transparent to the firing spike $s(t)$. Thus in the steady state, there is a current flowing from the tap into the bias sink such that:

$$i_b = \frac{V - V_T + V_b}{R_1} \quad (7)$$

When the firing spike turns on the bridge, the diode D_5 is reversed biased and the current i_b ceases to flow for the duration of the pulse. The effect of this is that a negative-going voltage spike with an amplitude of:

$$V_1 = -Z_f \cdot \frac{V - V_T + V_b}{2R_1} \quad (8)$$

is generated with half of the spike travelling towards the termination and half of the spike travelling towards the source. The mechanics of (8) can be seen by realizing that rapidly stopping the steady-state flow of current i_b into the transmission line (with an impedance of Z_f) is equivalent to presenting a negative current spike of magnitude i_b to the line. This then produces a negative voltage spike of magnitude $Z_f \times i_b$ for the duration the steady-state current

ceases to flow. The fact that there is a DC voltage on the transmission line has nothing to do with this problem. The result of this is that every time a firing spike passes a tap on the firing line its amplitude is reduced by V_1 . (The negative going spikes propagate in both directions and have the same voltage but half of the current). Thus R_1 and R_2 must be chosen so that amplitudes of the firing spikes, $s(t)$ and $s^*(t)$ are sufficient to meet condition (5). (This is the problem that was mentioned in Section 2.3. along with a possible solution as shown in Figure 14).

The other trade-off that must be made in choosing the value of R_1 and R_2 is (as was mentioned before) the amount of current that must be sourced or sunk by the diode bridge. In the application for which the bridge is intended, we are attempting to charge a capacitor up to the value of the input voltage within a certain aperture time, τ . (Assuming that the rise and fall time of the spikes is very short, the aperture time is in reality roughly equal to the width of the firing spikes). In order to optimize the values of R_1 and R_2 we must determine the relationship between the slew rate of the capacitor and the values of these resistances. This can be found by solving the circuit equations for the diode bridge in the ON state. Figure 18 shows the equivalent electrical circuit of the sampling gate in the ON state. The sense of the currents is drawn such that the voltage at V_B is

Figure 18: Six-diode sampling gate in ON state.

greater than the initial voltage on V_C . Using Kirchhoff's first law we can say that the sum of currents into any node is equal to zero. Thus:

$$i_1 = i_6 + i_7 \quad (9)$$

$$i_3 + i_7 = i_4 + i_8 \quad (10)$$

$$i_6 = i_5 + i_9 \quad (11)$$

$$i_8 + i_9 = i_2 \quad (12)$$

$$i_5 = C \cdot \frac{dV_C}{dt} \quad (13)$$

Rewriting these equations in terms of the node voltages, we have:

$$\frac{V - V_A}{R} = I_s [e^{\Lambda(V_A - V_C)} - 1] + I_s [e^{\Lambda(V_A - V_B)} - 1] \quad (14)$$

$$\frac{V_i - V_B}{R_s} - I_s [e^{\Lambda(V_A - V_B)} - 1] = \frac{V_B}{R_s} + I_s [e^{\Lambda(V_B - V_D)} - 1] \quad (15)$$

$$I_s [e^{\Lambda(V_A - V_C)} - 1] = C \cdot \frac{dV_C}{dt} + I_s [e^{\Lambda(V_C - V_D)} - 1] \quad (16)$$

$$I_s [e^{\Lambda(V_B - V_D)} - 1] + I_s [e^{\Lambda(V_C - V_D)} - 1] = \frac{V_D - (-V)}{R} \quad (17)$$

where $\Lambda = \frac{q}{nkT}$ is the diode constant.

Equations (14) - (17) describe the behaviour of the circuit. As can be seen there are three transcendental equations and one transcendental first order differential equation. Unfortunately, there is no closed form solution for V_C^* .

* There is one interesting result that can be obtained from (9) - (17). This is:

$$\frac{i_6 + I_s}{i_7 + I_s} = \frac{i_8 + I_s}{i_9 + I_s}$$

Thus we must either approximate the solution or turn to numerical methods in order to solve for V_C . As an approximation (and it is a useful one) we may observe that when V_B is greater than V_C only two of the diodes (D_3 and D_2) are really conducting current. Thus the initial current flowing into the capacitor C is:

$$i_5 = \frac{V - V_T - V_C}{R} \quad (18)$$

Thus a crude estimate of the final voltage V_C on the capacitor can be obtained by solving (18) for V_C . The solution is:

$$V_C = (V - V_T) - (V - V_T - V_{C0})e^{(-t/RC)} \quad (19)$$

where V_{C0} is the initial charge on the capacitor. The reason that this solution is only a crude estimate is that as V_C begins to approach V_B , the other two diodes, D_1 and D_4 begin to conduct too. Thus for a proper solution, numerical methods must be employed.

For this problem, it is desired to know the voltage on the capacitor, V_C after a certain period of time for a given input signal. Thus starting with an initial voltage on the capacitor of V_{C0} it is possible to find the instantaneous current flowing into the capacitor. From (13), we know that:

$$\frac{dV_C}{dt} = \frac{i_5}{C} \quad (20)$$

$$\frac{dV_C}{dt} = \frac{i_5}{C} \quad (20)$$

Then using the instantaneous current i_5 , numerical methods to solve differential equations can be used to find V_C after a certain time τ . In order to accurately simulate the parallel sampling system, several FORTRAN programs were written. One of these programs solved the system of equations (14) - (17). It did so in two parts. The first part called DSWTCHNR determined the instantaneous current i_5 flowing into the capacitor for a given V_i and V_C . The second part, called IC performed a numerical differential equation solution on (20). A complete description of the numerical routines that were used and their derivation is given in Appendix C.

3.3 The Bipolar Spike Generator

The impulse generator that was settled upon is shown (as mentioned before) in Figure 15. This circuit generates bipolar firing spikes that are almost perfectly aligned and have negligible amounts of ringing. In order to analyse this circuit, it is important to realize that in any balanced circuit there is a virtual ground running down the center of the circuit. This means, that in an analysis only half of the circuit need be analyzed. An idealized circuit and its equivalent half-section terminated by a virtual ground is shown in Figure 19. Here the circuit consists of a matching capacitor, C_1 , followed by a section of transmission line of

Equivalent
 $\frac{1}{2}$ Circuit $\downarrow$

Figure 19: Idealized bipolar spike circuit and equivalent half-circuit.

length ℓ , and finally a tuning capacitor and the SRD with its parasitic package inductance shown as L_D (remember that in order to split capacitors in half, two series capacitors with $2\times$ the capacitance must be created). In this circuit the termination resistance stays as R_{Term} since each arm of the full circuit was terminated in R_{Term} . Thus the balanced resistance is actually $2\times R_{Term}$.

For a shunt SRD impulse generator, the circuit produces half sine wave pulses of duration⁹:

$$T_w = \pi(L_1 \cdot 2C_{VR})^{\frac{1}{2}} \quad (21)$$

where:

$$L_1 \approx 10 \times \ell \sqrt{\epsilon_r} \text{ nH/cm} \quad (22)$$

and ℓ is in centimeters, and C_{VR} is defined as the reverse junction capacitance of the SRD at the negative swing voltage (the factor of $1/2$ occurs in the equation because of the balanced nature of the circuit). The formula that converts the transmission line length ℓ into an equivalent inductance L_1 is a rough approximation if ℓ is a small fraction of the wavelength of the signal passing through it, but for the purposes of our calculation it is more than adequate.

In order to design a bipolar spike generator of the type selected here, the desired pulse width, T_w is first chosen. Then an SRD is selected and its C_{VR} determined (typically from the manufacturer's catalogue). Then the required

inductance L_1 can be determined from (22), and hence the required length of transmission line, l . Next the tuning capacitor C_2 is determined using the following equation:

$$C_2 = \frac{T_w^2}{2L_p\pi^2} \quad (23)$$

This equation, which is essentially the same as (21) gives the tuning capacitance C_2 required to tune out the parasitic inductance of the SRD at the frequency equivalent to a half-sine output spike. Finally, C_1 is selected so as to tune out the series inductance and shunt capacitance that the SRD tank circuit presents to the input. With (21) through (23) it is possible to design a bipolar impulse generator. While this circuit may not be the most elegant, it is effective and simple. Because these equations are approximations, it is recommended that variable tuning capacitors be used for C_1 and C_2 .

3.4 Parallel Sampling Systems

In a parallel sampled data system perhaps the first item that needs to be addressed in theory is the question: "Is data obtained from a parallel sampled system the same as if it had been obtained from a single point sampler?". While a verbal description of the problem was given in Section 2.2.4, a mathematical analysis is now given.

3.4.1 The Equivalence of Single Point and Parallel Sampled Systems

Consider the waveform shown in Figure 20. It represents an idealized sampling signal with an aperture width τ , and a period T . It can be described as:

$$s(t) = A \cdot \sum_{n=-\infty}^{\infty} \text{rect}\left(\frac{\tau - nT}{\tau}\right) \quad (24)$$

Representing this function as a weighted sum of the orthogonal function set $e^{jn\omega t}$, we can find the exponential Fourier series by means of the Fourier transform. For a periodic waveform[†]:

$$s(t) = \sum_{n=-\infty}^{\infty} S_n e^{jn\omega t} \quad (25)$$

[†] It is interesting to note that T is the interval over which the integration was performed. In deriving the idea of representing a function as an infinite sum of weighted orthogonal functions, it is assumed that the integration interval T is the period of the time domain function that is being represented. The orthogonal functions themselves were chosen because they are orthogonal over the interval T . Thus the series representation of the function will be periodic over the interval T whether the actual function really was or not. If it wasn't, and the interval chosen was not the period of the function, then the series representation of the function will not be correct. This is a problem known as "windowing", and must be carefully considered whenever a discrete Fourier transform is performed.

$$s(t) = A \sum_{n=-\infty}^{\infty} \text{rect}\left(\frac{t-nT}{\tau}\right)$$

T = period

Figure 20: Sampling signal with finite width.

where:

$$\omega_0 = \frac{2\pi}{T} \quad (26)$$

$$S_n = \frac{1}{T} \cdot S(n\omega_0) \quad (27)$$

and:

$$S(\omega) = \int_{-T/2}^{T/2} s(t) e^{-j\omega t} dt \quad (28)$$

For our function:

$$\begin{aligned} S(\omega) &= \int_{-T/2}^{T/2} A \cdot \sum_{n=-\infty}^{\infty} \text{rect}\left(\frac{t-nT}{\tau}\right) e^{-j\omega t} dt \\ &= A \cdot \int_{-\tau/2}^{\tau/2} e^{-j\omega t} dt \\ &= \frac{-A}{j\omega} \cdot e^{-j\omega t} \Big|_{-\tau/2}^{\tau/2} \\ &= A\tau \text{Sa}\left(\frac{\omega\tau}{2}\right) \end{aligned} \quad (29)$$

where:

$$\text{Sa}(x) = \frac{\sin(x)}{x}$$

and:

$$\lim_{x \rightarrow 0} \text{Sa}(x) = 1$$

therefore:

$$s(t) = \frac{A\tau}{T} \cdot \sum_{n=-\infty}^{\infty} \text{Sa}\left(\frac{n\omega_0\tau}{2}\right) e^{jn\omega_0 t} \quad (30)$$

Now assume that this function is gating (sampling) another function $f(t)$. Then the sampled signal $f_s(t)$ will be:

$$\begin{aligned} f_s(t) &= f(t) \cdot s(t) \\ &= f(t) \cdot \frac{A\tau}{T} \cdot \sum_{n=-\infty}^{\infty} \text{Sa}\left(\frac{n\omega_0\tau}{2}\right) e^{jn\omega_0 t} \end{aligned} \quad (31)$$

Equation (31) describes the output of a perfect sampler where one signal, $s(t)$, is sampling another signal, $f(t)$. Now let us show that parallel sampling is the same as single point sampling. This can be done by showing that the spectra of the single point sampled signal and the summed parallel sampled signal are the same[†]. To do this, let:

$$\begin{aligned}\omega_0 &= \text{sampling rate of the single point sampler} \\ &= \frac{2\pi}{T_0}\end{aligned}$$

Now the complex spectrum of $f_s(t)$ for a single point sampler is found by taking the Fourier transform (which is symbolized by $F\{\cdot\}$) of (31). Thus:

$$F\{f_s(t)\} = F\left\{f(t) \cdot \frac{A\tau}{T_0} \sum_{n=-\infty}^{\infty} \text{Sa}\left(\frac{n\omega_0\tau}{2}\right) e^{jn\omega_0 t}\right\}$$

Because the Fourier transform is a linear operator, we can write:

$$F\{f_s(t)\} = \frac{A\tau}{T_0} \sum_{n=-\infty}^{\infty} \text{Sa}\left(\frac{n\omega_0\tau}{2}\right) F\{f(t)e^{jn\omega_0 t}\} \quad (32)$$

Now:

$$\begin{aligned}F\{f(t)e^{jn\omega_0 t}\} &= \int_{-\infty}^{\infty} f(t)e^{jn\omega_0 t} e^{-j\omega t} dt \\ &= \int_{-\infty}^{\infty} f(t)e^{j(\omega - n\omega_0)t} dt \\ &= F(\omega - n\omega_0)\end{aligned} \quad (33)$$

where $F\{f(t)\} = F(\omega)$.

[†] The term "summed parallel sampled signal" refers to the signal obtained by summing the outputs of all the parallel taps together.

Substituting this into (32) we get:

$$F\{f_s(t)\} = \frac{A\tau}{T_0} \sum_{n=-\infty}^{\infty} \text{Sa}\left(\frac{n\omega_0\tau}{2}\right) F(\omega - n\omega_0) \quad (34)$$

This is just the familiar aliased spectrum of $f(t)$ with $\text{Sa}(x)$ scaling imposed upon the aliases. Now for the parallel sampled case with m parallel taps sampling at the same effective rate as the single point sampler, let:

$$\begin{aligned} \omega_p &= \text{sampling rate of a tap in the parallel sampler} \\ &= \frac{2\pi}{T_p} \end{aligned}$$

Therefore:

$$\omega_p = \frac{\omega_0}{m} \quad (35)$$

$$T_p = mT_0 \quad (36)$$

Now each tap is designed so that ideally it will sample the signal $f(t)$ T_p/m seconds further ahead in time than the previous tap. Thus from (36), the output of the i^{th} tap (referenced to the time at the first tap, where $i = 0$) is:

$$f_{si}(t) = f(t)s_i(t)$$

where:

$$s_i(t) = s(t - iT_0)$$

Now the complex spectrum of the signal $f_{si}(t)$ is found to be:

$$F\{f_{si}(t)\} = F\{f(t)s_i(t)\} \quad (37)$$

In order to find (37), let us use the Fourier representation of $s_i(t)$.

From (25) - (28) we have:

$$F\{s_i(t)\} = \int_{-\infty}^{\infty} s(t-iT_0)e^{-j\omega t} dt$$

Performing a change of variable, let $x = t-iT_0$. Then $dx = dt$ and the limits of integration stay unchanged. Thus we have:

$$\begin{aligned} S_i(\omega) &= \int_{-\infty}^{\infty} s(x)e^{-j\omega(x+iT_0)} dx \\ &= e^{-j\omega iT_0} \int_{-\infty}^{\infty} s(x)e^{-j\omega x} dx \\ &= e^{-j\omega iT_0} S(\omega) \end{aligned}$$

Therefore:

$$S_{ni} = \frac{1}{T_p} S_i(\omega) \Big|_{\omega=k\omega_p}$$

From (30), we have:

$$S_{ni} = \frac{1}{T_p} e^{-jk\omega_p iT_0} A\tau \text{Sa}\left(\frac{k\omega_p \tau}{2}\right)$$

Therefore:

$$s_i(t) = \sum_{k=-\infty}^{\infty} \frac{A\tau}{T_p} e^{-jk\omega_p iT_0} \text{Sa}\left(\frac{k\omega_p \tau}{2}\right) e^{jk\omega_p t}$$

Now:

$$\begin{aligned} F\{f_{si}(t)\} &= \int_{-\infty}^{\infty} f(t) \sum_{k=-\infty}^{\infty} \frac{A\tau}{T_p} e^{-jk\omega_p iT_0} \text{Sa}\left(\frac{k\omega_p \tau}{2}\right) e^{jk\omega_p t} dt \\ &= \frac{A}{T_p} \sum_{k=-\infty}^{\infty} \text{Sa}\left(\frac{k\omega_p \tau}{2}\right) e^{-jk\omega_p iT_0} \int_{-\infty}^{\infty} f(t) e^{jk\omega_p t} e^{-j\omega t} dt \end{aligned}$$

$$= \frac{A}{T_p} \cdot \sum_{k=-\infty}^{\infty} \text{Sa}\left(\frac{k\omega_p \tau}{2}\right) e^{-jk\omega_p iT_0} F(\omega - k\omega_p) \quad (38)$$

We will now prove what we set out to do, namely that:

$$F\{f_s(t)\} = F\left\{\sum_{i=-\infty}^{m-1} f_{si}(t)\right\}$$

$$F\{f_s(t)\} = \sum_{i=-\infty}^{m-1} F\{f_{si}(t)\}$$

Now:

$$\sum_{i=0}^{m-1} F\{f_{si}(t)\} = \sum_{i=0}^{m-1} \frac{A}{T_p} \cdot \sum_{k=-\infty}^{\infty} \text{Sa}\left(\frac{k\omega_p \tau}{2}\right) e^{-jk\omega_p iT_0} F(\omega - k\omega_p) \quad (39)$$

From (35) and (36) we have:

$$k\omega_p iT_0 = k \times \frac{\omega_0}{m} \times i \times \frac{2\pi}{\omega_0} = \frac{2\pi ki}{m} \quad (40)$$

Interchanging the summations and substituting (40) into (39) we obtain:

$$\sum_{i=0}^{m-1} F\{f_{si}(t)\} = \frac{A}{T_p} \cdot \sum_{k=-\infty}^{\infty} \text{Sa}\left(\frac{k\omega_p \tau}{2}\right) F(\omega - k\omega_p) \sum_{i=0}^{m-1} e^{-j\frac{2\pi ki}{m}} \quad (41)$$

Now the summation $\sum_{i=0}^{m-1} e^{-j\frac{2\pi ki}{m}}$ acts as a filter[†] on k such that:

$$\begin{aligned} \sum_{i=0}^{m-1} e^{-j\frac{2\pi ki}{m}} &= m \quad \text{for } k = lm \\ &= 0 \quad \text{for } k \neq lm \\ &\quad \text{where } l \text{ is an integer} \end{aligned}$$

Thus the spectra of all m taps add together such that only every m^{th} frequency survives. Thus performing a change of

[†] This is a Kronecker delta function.

variable on (41) in order to take account of this decimation, we have:

$$n = \frac{k}{m} \quad \text{where } n \text{ is an integer}$$

we now have:

$$\sum_{i=0}^{m-1} F\{f_{si}(t)\} = \frac{mA\tau}{T_p} \sum_{n=-\infty}^{\infty} \text{Sa}\left(\frac{n\omega_p \tau}{2}\right) F(\omega - n\omega_p)$$

Using (35) and (36):

$$\begin{aligned} \sum_{i=0}^{m-1} F\{f_{si}(t)\} &= \frac{A\tau}{T_0} \sum_{n=-\infty}^{\infty} \text{Sa}\left(\frac{n\omega_0 \tau}{2}\right) F(\omega - n\omega_0) \\ &= F\{f_s(t)\} \end{aligned} \quad (81)$$

Thus the summed spectra of a parallel sampled system is equal to the spectrum of a the equivalent single point sampled system. This proves (if there was any doubt in the first place) that an ideal parallel sampled data system is identical to a single point sampled data system.

What can be seen here is that only if all the taps in the parallel sampled system are identical do the harmonics at ω_p cancel. Thus in an imperfect real world system, there will be sampling clock harmonics at ω_p . As mentioned before in a previous footnote (see page 57, all of the calculations for the output line spectrum must be done over a period common to both $f(t)$ and $s(t)$ or $s_i(t)$. This period will be referred to as the shortest common period. For calculation

convenience, it is useful to choose the input frequency so that the shortest common period is small.

3.4.2 Periodic Structure Considerations

Because a parallel sampled data system utilizes parallel taps all fed from common lines, the system inevitably becomes a periodically loaded structure as each connection point to a tap presents a shunt impedance to ground. In a periodically loaded structure, we make the assumption for the sake of easy analysis that the structure is infinitely long. This allows us to ignore the discontinuities that occur at the beginning and end of the structure. Let us assume that we have a periodic structure that consists of shunt loaded transmission line sections of the type shown in Figure 21. For this section the *ABCD* matrix is¹⁰:

$$\begin{bmatrix} V_n \\ I_n \end{bmatrix} = \begin{bmatrix} \cos(\frac{\theta}{2}) & j\sin(\frac{\theta}{2}) \\ j\sin(\frac{\theta}{2}) & \cos(\frac{\theta}{2}) \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\bar{B} & 1 \end{bmatrix} \begin{bmatrix} \cos(\frac{\theta}{2}) & j\sin(\frac{\theta}{2}) \\ j\sin(\frac{\theta}{2}) & \cos(\frac{\theta}{2}) \end{bmatrix} \begin{bmatrix} V_{n+1} \\ I_{n+1} \end{bmatrix}$$

where:

$\bar{B}$ = the normalized susceptance of the shunt load

θ = the electrical length of the section

Figure 21: Shunt loaded transmission line section.

$$= \begin{bmatrix} \cos(\theta) - \frac{\bar{B}}{2}\sin(\theta) & j(\frac{\bar{B}}{2}\cos(\theta) + \sin(\theta) + \frac{\bar{B}}{2}) \\ j(\frac{\bar{B}}{2}\cos(\theta) + \sin(\theta) + \frac{\bar{B}}{2}) & \cos(\theta) - \frac{\bar{B}}{2}\sin(\theta) \end{bmatrix} \begin{bmatrix} V_{n+1} \\ I_{n+1} \end{bmatrix} \quad (43)$$

Now for a propagating wave, we know that:

$$V_{n+1} = e^{-\gamma d} V_n$$

and:

$$I_{n+1} = e^{-\gamma d} I_n$$

where:

$\gamma = \alpha + j\beta$ is the propagation constant

d = distance between nodes.

Therefore:

$$\begin{bmatrix} V_n \\ I_n \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_{n+1} \\ I_{n+1} \end{bmatrix} = e^{\gamma d} \begin{bmatrix} V_{n+1} \\ I_{n+1} \end{bmatrix}$$

or

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} - \begin{bmatrix} e^{\gamma d} & 0 \\ 0 & e^{\gamma d} \end{bmatrix} \begin{bmatrix} V_{n+1} \\ I_{n+1} \end{bmatrix} = 0$$

This system of equations has a nontrivial solution only if the determinant of the system equals zero. Thus:

$$\begin{vmatrix} A - e^{\gamma d} & B \\ C & D - e^{\gamma d} \end{vmatrix} = AD - BC + e^{2\gamma d} - e^{\gamma d}(A + D) = 0 \quad (44)$$

For a reciprocal network the determinant $AD - BC$ of the transmission matrix equals unity.

Thus (44) becomes:

$$\begin{aligned}\cosh(\gamma d) &= \frac{A + D}{2} \\ &= \cos(\theta) - \frac{\bar{B}}{2}\sin(\theta)\end{aligned}\quad (45)$$

For the propagating case $|\cos(\theta) - \frac{\bar{B}}{2}\sin(\theta)| < 1$, we must have:

$$\gamma = j\beta \text{ and } \alpha = 0$$

Thus (45) becomes:

$$\cos(\beta d) = \cos(\theta) - \frac{\bar{B}}{2}\sin(\theta) \quad (46)$$

For the non-propagating case $\cos(\theta) - \frac{\bar{B}}{2}\sin(\theta) > 1$, we must have:

$$\gamma = \alpha \text{ and } \beta = 0$$

For the other non-propagating case $\cos(\theta) - \frac{\bar{B}}{2}\sin(\theta) < -1$, we must have:

$$\gamma d = \alpha + j\pi$$

From this it can be seen that, depending on the spacing of the shunt loads their susceptance, there will be a repeating passband/stopband type of behaviour that will be a function of frequency. In our case, the parallel sampling system had to be designed so that none of the signal distribution lines exhibited a cutoff behaviour. As well, the signal had to pass through the distribution lines with as little dispersion as possible. This was especially important for the firing

lines as they were intended to transmit positive and negative impulses to the sampling gates. These impulses were very rich in harmonics, and any degradation in the higher harmonics would have resulted in a broadening of the impulses. This would have meant that the taps closest to the spike generator would have seen very narrow pulses, and the taps furthest away would have seen broad pulses. This would also have created a clock skewing effect due to the differing shut-off times of each of the taps. A second problem that also had to be dealt with in the initial design was that the periodic loading changed the impedance and group velocity of the transmission structure. Thus an equation had to be derived for the group velocity v_g of a periodically loaded structure so that it was possible to space the taps correctly.

In microwave structures, group velocity is approximated¹¹ (quite accurately) as:

$$v_g = \frac{d\omega}{d\beta} \quad (47)$$

Now:

$$\omega = 2\pi f = \frac{2\pi c}{\sqrt{\epsilon_r} \lambda} = \frac{ck_0}{\sqrt{\epsilon_r}}$$

where:

$$k_0 = \frac{2\pi}{\lambda_0} \quad \text{and} \quad \lambda_0 = \text{free space wavelength.}$$

Thus from (47):

$$v_g = \frac{c}{\sqrt{\epsilon_r}} \cdot \frac{dk_0}{d\beta} = \frac{c}{\sqrt{\epsilon_r}} \cdot \frac{d(k_0 d)}{d(\beta d)} \quad (48)$$

where d is the physical length of the section. Now putting (46) in terms of $k_0 d$ and βd we have for a capacitive load, C :

$$\begin{aligned} \bar{B} &= \omega C Z_0 \\ &= \frac{c k_0}{\sqrt{\epsilon_r}} C Z_0 \\ &= \frac{c C Z_0}{d \sqrt{\epsilon_r}} k_0 d \end{aligned} \quad (49)$$

Therefore (46) becomes:

$$\cos(\beta d) = \cos(k_0 d) - \frac{c C Z_0}{2 d \sqrt{\epsilon_r}} k_0 d \sin(k_0 d) \quad (50)$$

Differentiating (50) implicitly we have:

$$-\sin(\beta d) =$$

$$-\sin(k_0 d) \frac{d(k_0 d)}{d(\beta d)} - \left[\frac{c C Z_0}{2 d \sqrt{\epsilon_r}} \sin(k_0 d) + \frac{c C Z_0}{2 d \sqrt{\epsilon_r}} k_0 d \cos(k_0 d) \right] \frac{d(k_0 d)}{d(\beta d)}$$

Thus from (50), we have:

$$\frac{d(k_0 d)}{d(\beta d)} = \frac{\sin(\beta d)}{\left(\frac{\bar{B}}{2 k_0 d} + 1 \right) \sin(k_0 d) + \frac{\bar{B}}{2} \cos(k_0 d)}$$

From (48) we now have:

$$v_g = \frac{\frac{c}{\sqrt{\epsilon_r}} \sin(\beta d)}{\left(\frac{\bar{B}}{2 k_0 d} + 1 \right) \sin(k_0 d) + \frac{\bar{B}}{2} \cos(k_0 d)} \quad (51)$$

There are several important things to be learned from (51). The first is that when $\beta d = 0$ the group velocity at this point is also equal to zero. This makes sense, since when βd is equal to zero, all of the shunt loads are spaced $\lambda/2$ apart which means that they present zero admittance to the source. Thus at the passband edges of the structure, the group velocity goes to zero. What this meant in practice was that the parallel sampling system had to be designed so that all of the frequencies used in the system lay as far from the passband edges as possible. This implied placing the periodic loads (i.e. the taps) as close together as possible.

In the limit when $k_0 d \rightarrow 0$ in (51) we obtain the familiar equation from ECL design handbooks¹²:

$$v_g = \frac{1}{\sqrt{L_0(C_0 + \frac{C}{d})}} \quad (52)$$

where L_0 and C_0 are the distributed inductance and capacitance per unit length of the transmission line that is connecting the periodic capacitance, C spaced " d " units apart. This shows that when the spacing is small compared with the wavelength, what appears to happen in a periodically loaded structure is that the periodic capacitance "smears" itself along the transmission line and become a distributed capacitance per unit length equal to C/d . Thus the new distributed capacitance per unit length of the transmission line becomes the sum of C/d and C_0 .

3.4.3 Meander Line Structure Considerations

In order to design the chosen parallel sampling structure (see Figure 5), an equation was required that would relate the spacing between taps along the meander line structure of the input signal. For the case of opposing signal propagation (the input signal travelling towards the sampling pulses), at a sampling rate of f_s , we can write:

$$t_m = \frac{1}{f_s} - t_d \quad (53)$$

where t_m is the time between taps on the meander line, t_d is the spacing between taps on the firing line, and f_s is the sampling frequency. In Figure 5, $t_m = \tau_1$ and $t_d = \tau_2$. This formula can be derived by realizing that in the time t_d that it takes the firing signal to travel between taps on the firing line, the input signal has travelled toward the firing signal for a duration of t_m . Thus the sum of these two times must equal the desired sampling interval, $1/f_s$, which is what (53) says. Thus with this equation and the others presented in this chapter, it was possible to physically implement the ideal structure of Figure 5.

CHAPTER 4: IMPLEMENTATION

4.1 Introduction

In the previous sections an approach was chosen and all of the theory applicable to the design of the parallel sampling system was developed. In this section the actual implementation will be discussed as well as the justification for this route. As with the previous sections the presentation of the material will proceed along the same lines that were followed in the actual prototype development.

4.2 The Six-Diode Sampling Gate

After having selected the six-diode sampling gate as the switch to use for the chosen parallel sampling system, the first problem was to determine how this was going to be physically realized. Referring to the circuit shown in Figure 22 (which is the same as the circuit in Figure 13), it can be seen that circuit consists of five separate parts. This first part is the input amplifier. The purpose of this amplifier is to provide a low impedance drive to the switch so that the sourcing or sinking of current that occurs when the switch opens has little or no effect on the voltage that the amplifier presents to the switch. Ideally this is a high drive-current operational amplifier or buffer. For the

parallel sampled system that was being constructed, the input frequency was targeted as being from DC to 550 MHz. In 1986/87 it was impossible to obtain an amplifier that could operate over this frequency range and provide a high drive-current. Thus it was decided to not put an input amplifier in at all. This was actually a reasonable compromise as the input line impedance was 50 Ω , which is a fairly low impedance. Another problem, which was circumvented by not having this buffer amplifier in the circuit, was the problem of matching the time delays through all of the buffer amplifiers in each of the taps. If this was not done, timing errors in the sampling process would have occurred and the performance of the system would have been degraded. This would have led to the appearance of clock spur harmonics as was discussed in the theory.

The second part of the sampling circuit in Figure 22 is the six-diode bridge. To reduce the parts count and to create a bridge with reasonably well matched diodes it was decided (after much discussion with various diode manufacturers) that the bridge would be implemented in two parts: a common-cathode triple and a common-anode triple. These two parts are shown in Figures 23 and 24. They were both packaged in 70 mil ceramic X-packs and were custom manufactured by SDI Inc. in Boston. The diodes that were chosen to implement the gate were low barrier Schottky

Figure 22: Six-diode sample and hold circuit.

Figure 23: Common anode triple.

Figure 24: Common cathode triple.

diodes. These were chosen because of their superior switching performance (due to their lower junction capacitance) as compared to standard p-n junction diodes. Because of the relatively low volume of diode triples that were being ordered, it was decided to have the triples fabricated from matched beam-lead diodes mounted in a lead frame as opposed to spending roughly \$12K US to have two monolithic diode-triple masks made up. In the diode industry this procedure is common practice so there were no great costs involved.

The diode electrical parameters were chosen to so as to meet the criteria specified in equation (4) as well as to have the lowest possible junction capacitance and ON resistance. The actual diode parameters were:

$$V_T = 0.4 \text{ V @ } 1 \text{ mA of forward current}$$

$$R_s = 4 \text{ } \Omega$$

$$L_p = 0.16 \text{ nH}$$

$$C_{j0} = 0.15 \text{ pF}$$

$$V_{BR} = -5 \text{ V}$$

$$C_p = .07 \text{ pF}$$

The third item that had to be dealt with was the hold capacitor. In the ideal limiting case its value should

approach zero as the input resistance to the hold amplifier and the OFF resistance of the switch both approach infinity. This would allow the charging of the hold capacitor to be instantaneous. In the S/H circuit, the worst-case maximum change in voltage due to the leakage through the switch can be estimated to be the change in voltage due to twice the leakage current flowing out of the hold capacitor multiplied by the time interval (one clock period or $1/100 \text{ MHz} = 10 \text{ nsec}$) divided by the hold capacitance. In order to calculate this voltage droop, the reverse bias leakage current, I_s , through the diodes must be calculated. Starting with the diode equation:

$$I = I_s [e^{\Lambda V} - 1] \quad (54)$$

$$\text{and } \Lambda = \frac{q}{KT} = \frac{1}{.0259}$$

at 25°C (298°K)

the value of I_s for our diodes was found to be:

$$I_s = \frac{1 \times 10^{-3}}{e^{(0.4/.0259)} - 1}$$

$$= .196 \text{ nA}$$

Thus the maximum change in voltage over 10 nsec would have been:

$$\Delta V_{\text{MAX}} = \frac{.196 \times 10^{-9} \times 10 \times 10^{-9}}{1 \times 10^{-12}}$$

$$= 1.96 \text{ } \mu\text{V/pF}$$

This is a very small change in voltage especially as 4-bit ADCs were selected. For a 1 V digitizing range, (which corresponds to the peak voltage on a 50 Ω line with a +10 dBm signal on it) the LSB in a 4-bit ADC represents:

$$1 \text{ LSB} = \frac{1\text{V}}{2^4} = 62.5 \text{ mV}$$

Thus the voltage droop would not have been a problem with up to roughly 15 nF of hold capacitance (the capacitance required to cause a voltage droop greater than 1/2 LSB).

The fourth item to be considered in the design of the sampling gate is the hold amplifier. Because the voltage droop due to leakage through the diode gate was so small it was decided to select a hold amplifier with a FET based input and a small, constant input capacitance. The idea arrived at was to use the capacitance associated with the input of the hold amplifier as the hold capacitance. This resulted in one less component in the sampling gate, and avoided the problem of having to find a low loss, non-inductive chip capacitor.

The hold amplifier that was selected was an Elantec EL2005 high performance buffer (almost every part that is ever produced is "high performance" at its introduction but at the time this genuinely was a high performance part). The specifications for this part can be found in Appendix D. With a 1 G Ω input impedance, there was no worry about leakage from the hold capacitance into the amplifier, so the 3 pF

input capacitance was not a concern. In terms of bandwidth and drive capability, the part was adequate in both of these areas as well.

The fifth and final components that had to be chosen were the bias resistors. The parts selected were 120 mil x 60 mil thin film chip resistors. These parts could operate satisfactorily up to 18 GHz and had 1/4 W power handling capability.

In order to select the optimum value for these bias resistors it was necessary to know the voltages that would be used to bias and fire the sampling gate. These voltages were determined from equation (4) and from the input signal level specifications. As was mentioned before, the peak input voltage level corresponded to a +10 dBm input signal level on the 50 Ω input line. This corresponded to 1 V as is shown in the following calculation:

$$10 \log \left(\frac{V_{Brms}^2}{Z_{in}} \right) + 30 = P \quad [\text{dBm}]$$

or:

$$10 \log \left(\frac{V_{Bpk}^2}{2 \times 50} \right) + 30 = 10 \quad [\text{dBm}]$$

therefore:

$$V_{Bpk} = 1 \text{ V}$$

Now from (4) we have:

$$1 + 0.4 + 0.5 \leq V_b \leq -1 + 0.5 - (-5) - 1$$

or:

$$1.9 \leq V_b \leq 2.5$$

Thus V_b was chosen to be 2.0 Volts. The next parameter that had to be chosen was the charging voltage, V . Since in the rough estimate, (19), the hold capacitor is charged as an RC circuit with V as its driving voltage, the larger V is, the faster the capacitor will charge. Hence V was chosen to be +15 V, which was the largest convenient regulated supply voltage available. Now with the assumption that the voltage spikes $s(t)$ and $s^*(t)$ were large enough in amplitude to turn on the sampling gate, it became possible to determine the value of the bias resistor.

4.2.1 The Selection of the Diode Switch Bias Resistor

As was mentioned, the choice of the bias resistor value depended upon the results of several computer simulations and upon some experimental work. The simulations were done first and hence they will be discussed first.

2

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4.2.1.1 SPICE Simulations

The first simulations were done using SPICE¹³. The diode switch was modelled as the circuit shown in Figure 25. The SPICE circuit file that was used can be found in Table 1 of Appendix A. Table 2 of Appendix A gives the component values that were used in the simulations. These component values were arrived at by considering the physical implementation of the selected sampling gate. For instance, all of the signal generators had to have 50 Ω source impedances, and the firing lines had to have 50 Ω terminations. The values for the hold resistance and capacitance were determined from the data sheet of the hold amplifier (see Appendix D). Finally, the diode equivalent circuit was determined from the manufacturer's information. This left only the bias resistance to be determined.

In order to determine the optimal bias resistance, a scenario was devised by which the sampling gate's performance could be evaluated. This scenario assumed that the sampling gate was sampling a 331 MHz signal at a 2 GHz sampling rate. The 2 GHz sampling rate was chosen as it was definitely a "worst case" situation, and the 331 MHz signal was chosen since it was not harmonically related to the sampling frequency. The amplitudes of the firing signals were

DIODE PARAMETERS

VF=0.4V

RS=4 Ω

CJO=0.12 pF

IS=196.22E-12

VBR=-5V

Figure 25: Six diode sampling gate SPICE simulation network.

chosen so that the sampling gates would be turned fully ON and fully OFF by these signals. The widths of the signals were initially chosen to be 200 psec because this was the width of the spikes that were being generated by the first prototypes of the bipolar spikes generator (more will be said about this later).

The first simulation that was done used a bias resistance of 3.9 K Ω , which was arbitrarily chosen. The results of this simulation are shown in Figure 26. As will be seen upon inspection of the other results, this resistance was too large. In order to judge the size of resistor that was needed better, a figure of merit, which was termed a "scaled time constant" was developed. Basically, what was done was to determine the RC time constant of the bias resistor and the hold capacitor and then divide this value by the ratio of final target voltage on the hold capacitor (1 V) to the charging voltage (15 V). Thus the 3.9 K Ω and the 3 pF intrinsic hold capacitance produced a scaled RC time constant of 780 psec. As expected with a 200 psec aperture, the results were poor. One thing that should be noticed from Figure 26 is that there is poor tracking of the output waveform because every time the switch is opened, the capacitor attempts to charge towards where the input voltage is at that moment. Sometimes the voltage on the capacitor is far away from the input voltage and hence the capacitance

v[5] - input sine wave
v[7] - output hold voltage
v[2] - input firing spike

Figure 26: Sampling gate with 3900 Ohms bias resistance.

voltage changes, while other times it happens to be close to its target. The result of this is that spectral spreading occurs. This will also be discussed later.

The next simulation used a $390\ \Omega$ resistance (again arbitrarily chosen), with a corresponding scaled RC time constant of 78 psec. The resulting plot is shown in Figure 27. What occurs here is not overly desirable either. In this plot, the resistance is too low and as a result the current flowing into (or from) the $50\ \Omega$ input drags down the input voltage too much. Thus while the hold capacitor quickly charges up to the input voltage, the input voltage itself is distorted.

The third plot, shown in Figure 28 again uses a $390\ \Omega$ bias resistor except that here the impedance of the driving circuit has been reduced to $1\ \Omega$ (as well the input voltage was cut by half to account for the fact that there was no voltage divider at the input). In this circuit, it can be seen that the output capacitor charges up to the required voltage and that the input is not skewed. However this is not a realizable circuit and was only simulated in order to demonstrate the effect of a low driving impedance. An interesting consequence of the low source impedance is that there is a slight droop on the capacitor hold voltage on the first sample. This is due to the fact that the low bias

v[5] - input sine wave
v[7] - output hold voltage
v[2] - input firing spike

Figure 27: Sampling gate with 390 Ohms bias resistance.

v[5] - input sine wave
v[7] - output hold voltage
v[2] - input firing spike

Figure 28: Sampling gate with 390 Ohms bias resistance
and 1 Ohm driver impedance.

resistance has caused the spike voltages to be dragged towards the bias voltages. This resulted in the diode bridge not being turned fully off and leakage occurring. In the actual circuit this would not happen because the biasing on the firing lines is not done through a $50\ \Omega$ resistor (see Figure 15) but through a bias choke. This bias choke was not simulated because of the unnecessary complexity this would have added.

As a compromise between the $390\ \Omega$ and $3900\ \Omega$ resistors it was found that a $1100\ \Omega$ resistor produced the best results. The plot of the sampling gate with an $1100\ \Omega$ resistor and a $50\ \Omega$ source impedance is shown in Figure 29.

The final SPICE simulation that was done involved widening the pulse width on the sampling gate with the $1100\ \Omega$ resistor in order to investigate the effect of longer charge time on the output voltage. The pulse width used was 600 psec. The result of this longer charge time is shown in Figure 30. As can be seen, the final output voltage is very close to the desired voltage. The reasoning behind doing this was that observation showed that there was no advantage in having a very narrow sampling window. In reality, all that mattered was that the turn-off of the sampling gate had to be sharp, as the final voltage on the hold capacitor would be equal to the input voltage at the shut-off of the sampling

v[5] - input sine wave
 v[7] - output hold voltage
 v[2] - input firing spike

Figure 29: Sampling gate with 1100 Ohms bias resistance.

v[5] - input sine wave
v[7] - output hold voltage
v[2] - input firing spike

Figure 30: Sampling gate with 1100 Ohms bias resistance and wider pulse.

gate. The only assumption made here was that the voltage on the hold capacitor had to be able to slew as fast as the input signal. This idea is not new as this is the principle behind the track-and-hold sampling gate. As can be seen from the results of Figure 30, this was the best approach.

4.2.1.2 Non-linear Switch Simulations

After the SPICE simulations were completed, a FORTRAN program was written to calculate the exact output voltage of the sampling gate for a fixed input voltage and a fixed ON time. The program (as mentioned in the Chapter 3) solves equations (13) - (16) and (20) in order to determine the final output voltage on the capacitor. The program, called SW is described in detail in Appendix C, where a listing of the program is given.

The program was compiled using the optimum values obtained from the SPICE simulations, namely a bias resistance of $R = 1100 \Omega$ and a sampling pulse width of 600 nsec. This program was written in order to determine in detail what effect the pulse width would have had on the hold capacitor's output voltage, and on its slew rate. While SPICE could have been used for this purpose, it was also realised that in order to simulate the entire sampling system (which was one of the goals in this work) a program such as this would have

to be written in order to accurately simulate the sampling gates.

The program was run for four different cases of input voltage and initial capacitor voltage. The four runs are shown in Figures 31 to 34. The purpose of including these runs is to demonstrate the effects of high slew rate on the final output voltage. The first run (Figure 31) shows the case of slewing over half of the input signal's range. As can be seen, after 600 psec the final voltage of .952 V is close to the desired value of 1 V. For a 4-bit ADC operating over a ± 1 V range, 1 bit corresponds to .125 V. Thus .937 V is within 1/2 LSB of the desired voltage, and for a 4-bit system, no degradation of the digitized data would be detected[†]. The second plot (Figure 32) shows the case of a full range slew in output voltage. In this simulation the start voltage on the capacitor is -1 V and the desired final voltage is 1 V ($V_I = 2$ V). As can be seen the slew rate is just fast enough, as the final output voltage is .932 V after 600 psec. This still corresponds to a $\frac{1}{2}$ -bit error after

[†] A .125 V LSB may seem like a coarse resolution, but at the time that this work was done, a 4-bit 100 Msample/sec ADC was state-of-the-art. As well, even if higher resolution ADCs had been available it is doubtful whether they could have been used as the 4-bit 12-channel parallel sampled system alone produced a 4.8 Gbit/second data stream. This "flood" of data was actually one of the limiting factors in the entire system design as state-of-the-art memory management techniques were required in order to even be able to store this data.

Figure 31: Switch slew rate test #1.

Figure 32: Switch slew rate test *2.

Figure 33: Switch slew rate test *3.

Figure 34: Switch slew rate test #4.

quantization. The next plot (Figure 33) is essentially the same as that of Figure 32 except that the voltages are inverted. This figure was included to demonstrate that the switch is indeed a symmetrical device.

The final plot (Figure 34) demonstrates the effect of reducing the input signal's full range swing and correspondingly reducing the quantization range. This figure shows the results of a full range slew when the full range is .4 V ($V_I = .8$ V), which corresponds to an input power of +2 dBm into 50 Ω . As can be seen, the final value of the voltage on the hold capacitor voltage is .380 V which is .020 V away from where it was supposed to be. This again corresponds to a $\frac{1}{2}$ -bit quantization error (1 LSB = 50 mV). While it is tempting to suggest that reducing the input signal's voltage range might be one way of improving the performance of the sampling gate, this reduced signal amplitude would have made the sampling system much less immune to noise. This approach was therefore avoided.

4.2.1.3 Hardware Prototype Testing

The final stage in deciding upon the correct parameters to use was to construct a prototype of the diode switch and through experiment confirm the predictions of the simulations. Because the switch was such an electrically

complicated device (in terms of connecting all of the required signals), it was decided to not construct a single switch prototype but to construct the entire parallel sampling board and then use it partially assembled as the test bed in order to determine what the correct value for the bias resistor should be. Thus the design methodology for the layout of the board will now be presented.

The actual layout decided upon for the sampling gate is shown in Figure 35. As can be seen the pair of diode-triples were mounted in a diamond-fashion so as to align the input and output of the sampling bridge. The Elantec buffer was mounted on the opposite side of the board from the diodes so as to reduce the distance between the output of the switch and the input of the buffer. In terms of signal feeds to the bridge, both the input signal to the sampling gate and the bipolar spike lines were fed via stripline to the bridge. More about this will be discussed when the overall board construction is discussed. The final components on the board were the bias resistors. They were mounted on the surface along with charge storage capacitors capable of absorbing the current transients that would occur during switching. 1000 pF chip capacitors were chosen for this.

From the diagram of the sampling gate layout, it is apparent that there was a problem with the connections from

Figure 35: Sampling gate layout.

the bipolar firing lines to the sampling gate. This was because the signals from the bipolar spike generator had to arrive at the sampling gate at the same time. However the inputs to the switches were spatially separated. This problem was dealt with by making the positive spike line (the upper one in Figure 35) longer than the negative spike line in order to compensate for the difference in length.

After the remainder of the board was designed (the details of which will be discussed later), the board was fabricated, and sampling gate testing was begun. Using the results of the sampling gate simulations as a guideline, various bias resistor values were tested. What was found was that 1100 Ω bias resistors did indeed produce the best results. Photographs of the output signal from the buffer amplifier of the third tap are shown for two different input signal frequencies. The first photograph (Figure 36) shows the output of the buffer amplifier for a 50 MHz input signal and a 93 MHz clock (the reason for the choice of 93 MHz will be discussed in Section 5.2). In order to properly interpret the photograph of the output, it should be realized that the sources driving the bipolar spike generator and the input test signal were both free running and were not phase locked together. The result of this is that there was blurring throughout the traces as the oscilloscope visually averaged all of the different sampled voltages together on the

display. This blurring was especially noticable at the beat frequency zero-crossing points.

The second photograph (Figure 37) shows the same buffer with an 88 MHz input signal and again a 93 MHz clock. As can be seen there is a bit of peaking at the low frequency. This was possibly due to the termination that was used for the buffer amplifier. It consisted of a 4" length of wire terminated with a 1 K Ω load and a shunt 33 pF capacitance. This was done so as to simulate the input of the ADCs that were being used.

In terms of high frequency performance, the sampling gate had no difficulty in sampling input signals up to 2 GHz. (Note that because this gate is designed for use in a parallel sampled data system, each gate must be capable of sampling signals far above the gate's actual Nyquist frequency.) This can be seen from the next three photographs which show the performance of the sampling gate for three other input frequencies with +10 dBm input power and a 100 MHz sampling frequency. These were taken using a high impedance oscilloscope probe. The first photograph in Figure 38 shows the sampling gate output for a 46 MHz input signal. The second (Figure 39) shows the output for a 631 MHz input signal, and the third (Figure 40) shows a 930 MHz input signal. As can be seen, there are no real amplitude

Figure 36: Sampling gate sampling 50 MHz signal with 93 MHz clock.

Figure 37: Sampling gate sampling 88 MHz signal with 93 MHz clock.

Figure 38: Sampling gate sampling 46 MHz signal with 100 MHz clock.

Figure 39: Sampling gate sampling 631 MHz signal with 100 MHz clock.

Figure 40: Sampling gate sampling 930 MHz signal
with 100 MHz clock.

differences apparent between the signals except in the case of the 46 MHz signal. This was due to the fact that the signal generator that was used did not have a constant output power versus frequency, and at 46 MHz the output power was higher.

It is interesting to observe these waveforms, as they are essentially the output of a sampling mixer. A sampling mixer's output is similar to a normal mixer's output except that in a sampling mixer, the hold capacitor smooths out the chopped waveform that is produced by a normal mixer. The result is that most of the energy in the output waveform is concentrated at the sampled output frequency, which is always less than or equal to $f_s/2$. Thus if the input signal was DC, the output of the sampling gate would be DC as the peaks produced by the mixing circuit (the sampling gate) would be joined together. Without the hold circuit, the output would (in the ideal case) be a square wave with a frequency of f_s . Increasing the input signal's frequency from DC, the sampling points would begin to fall at points all along the input sine wave. Because the input signal's frequency would be low compared to sampling signal's frequency, the distance between samples on the input sine wave would not be very far apart in terms of angular change of the input signal. Increasing the frequency further, the angular distance between sampling points on adjacent samples would begin to be farther and

farther apart. This would mean that the change in voltage would begin to be greater. What would have previously appeared to be a "staircase" of sampled voltages for an input signal close to DC would now begin to be a sine wave of frequency $f_s/2$ with an amplitude modulated envelope equal in frequency to $|f_{in} - f_s/2|$ MHz. This would occur because the angular distance between samples would begin to approach 180° as the frequency of the input signal became close to the Nyquist frequency ($f_s/2$). This would imply that sometimes the sampling would be occurring at the input signal's zero crossing points and other times it would be occurring at its peaks (where each sample would fall on the opposite peak of the sample before it, which would result in envelope being filled by the frequency $f_s/2$). The result of this would be that as the frequency of the input signal became equal to one half of the sampling frequency, there would be relatively long intervals of time where the output of the sampling mixer would be close to zero volts, and other equally long intervals where the output would be equal to $f_s/2$.

Increasing the input signal's frequency past $f_s/2$, we would begin to see the effect known as aliasing. The output signal of the sampling gate would still be an amplitude modulated sine wave with a frequency of $f_s/2$, but the frequency of the envelope would begin to increase again. What would be noticed is that if the input signal were Δf MHz

greater than $f_s/2$, the output signal would appear identical to the output for an input signal Δf MHz less than $f_s/2$. This would occur because the absolute angular distance between samples would be identical. (i.e. if the angular distance between samples was 190° for an input signal, its output would appear to match the output from a signal whose angular distance between samples was 170° . What would be different between them, but not noticable from the visually averaged oscilloscope output is that 190° sampling points would appear to be advancing along the input sine wave, whereas the 170° sampling points would appear to be retreating. This is the same effect that makes cart wheels in movies appear to be going backwards.)

If the input signal's frequency were increased further, the envelope and the $f_s/2$ filling frequency would become indistinguishable and the "staircased" sine wave would begin to emerge. As the input signal's frequency began to approach the sampling frequency, the angular distance between samples would now be close to 360° . This would mean that the sampling points on the sine wave would begin to be almost the same from sample to sample. The result of this would be that the output signal frequency would become DC as the input signal's frequency reached the sampling frequency. Increasing the input signal's frequency past the sampling frequency would repeat the entire process all over again.

Returning now to the experimental results obtained from the sampling gate, it can be seen from its performance as seen in the preceding figures, that the choice of 1100 Ω as the bias resistance was a good one.

4.3 The Bipolar Spike Generator

From the results of the sampling gate simulations, it was decided that the spike generator should produce spikes 600 psec wide at their base. Thus using equations (21)-(23) it was possible to determine the values for the components used in the bipolar spike generator. The calculations used to determine these values are shown in Appendix B. The schematic of the bipolar spike generator is shown in Figure 41.

The first consideration that had to be made in designing the actual bipolar spike generator around the values obtained from the calculations in Appendix B, was that in order for the parallel sampling system to be able to properly interface with the 12 ADCs, it was necessary to synchronize the parallel sampling board's sampling signal with the ADC's clock signal. To do this it was necessary to derive the two signals from a common source. The source used was a 100 MHz ECL clock oscillator that was located external to the parallel sampling board. A typical ECL clock signal (both

Figure 41: Bipolar spike generator.

10K or 100K ECL logic swings are very similar) is a square wave which roughly swings between -0.8 V and -1.8V and is terminated in 50 Ω to -2 V. In order to use this signal a capacitively coupled tap connected to the ECL clock line was used (see Figure 41). This tap consisted of a 1000 pF capacitor and an Elantec EL2005 buffer amplifier (the same one that was used as the buffer amplifier in the sampling gates). Because the buffer amplifier was used to drive a 50 Ω load, the amplifier had a significant amount of loss. However, because of the band-limited buffering characteristics of the buffer, it filtered out the higher order harmonics of the ECL square-wave. Thus the output signal was a relatively pure .11 V peak sine wave (-9 dBm into 50 Ω). In order to amplify this signal, an amplifier was used to boost the signal from -9 dBm to +20 dBm. This signal was then fed into a 16 dB chip attenuator which reduced the power to +4 dBm. This signal then fed to the next amplifier in the chain. The output signal from this amplifier was +23 dBm and this was the maximum saturated output power that could be obtained from this type of amplifier. The requirement for this power level was dependent upon the power requirement of the bipolar spike generator, and this value was arrived at through experimentation. The next component in the circuit was a balun transformer which split the +23 dBm amplified signal into two balanced, anti-phase components. Up to this point

in the circuit, all of the connections were made in stripline. (Stripline was used on the input to the spike generator for convenience as the actual firing lines that connected the spike generator to all of the parallel sampling gates were in stripline. Thus the spike generator circuit was placed on the same board layer as the firing lines.) After the balun transformer, the connections were made using twin microstrip lines (formed by exposing the buried stripline layer) spaced 0.2" apart. This was done so that it was possible to mount the SRD directly across the balanced signal lines, without having the inductance of vias added to the SRD's parasitic package inductance. (The coupling between these lines was negligible as the microstrip height was .010"). After the balun transformer, 1000 pF blocking capacitors were used in conjunction with 1.0 μ H chip inductors for the biasing and DC offsets required in the circuit. In order to tune the spike generator, variable capacitors with a 10 pF to 120 pF capacitance range were employed. The final component in this circuit was an SRD.

Using these values the circuit was constructed. After assembling the prototype circuit, it was found that +23 dBm of input power and around .45 V of forward bias produced the best bipolar spikes. The output of this spike generator is shown in Figure 42. Here the positive- and negative-going spikes that comprise the bipolar pair are shown. The time

Figure 42: Bipolar spike generator output into 50 Ohm load.

Figure 43: Bipolar spike generator output at end of 24 taps.

skew on the two channels was adjusted so that the spikes were offset from each other for easy viewing. As can be seen from the photograph, the spikes are roughly 10 V in amplitude and have a pulse width at their base of roughly 600 psec. The spike generator was run at 93 MHz for this picture.

After assembling the remainder of the taps, it was found that when the spikes travelled down the loaded periodic structure, dispersion and filtering occurred which resulted in the output spikes being roughly 1200 psec wide at the base of the pulse. As well the amplitude of the signal was reduced due to the effect of halting the current flow on the lines (see Section 3.2). From equation (8) we have the voltage loss of a spike through each tap as being:

$$V_1 = -50 \times \frac{15 - .5 + .2}{2 \times 100} \\ = .375 \text{ V}$$

A photograph of the spikes after they had travelled down the periodically loaded structure is shown in Figure 43. Here the spikes had a amplitude of about 2.2 V. This picture was taken after the bipolar spikes had travelled down a line loaded with 24 taps. The reason for using 24 taps will be discussed in the next section. For 24 taps, one would have expected the voltage on the spikes to drop by $.375 \times 24 = 9 \text{ V}$. However the voltage only dropped by 8 V. This was possibly due to the fact that the switch diodes have a parasitic package inductance that was not taken into account in the

spike loss calculation. As well, the vias present an additional series inductance. This inductance would result in the switch not turning off instantly. Correspondingly this would reduce the amount by which the spike was decreased by as it passed each tap.

This concludes the discussion of the bipolar spike generator.

4.4 The Parallel Sampling Board

After deciding upon the architectures for the sampling gate and the bipolar spike generator, the design of the overall parallel sampling system was begun. The first major consideration was that it was deemed necessary to be able to perform real-time testing on the parallel sampling system.

In order to accomplish this, it was decided that a complementary parallel digital-to-analogue conversion (DAC) process would be required so that the digitized signal could be re-created in real time and the results viewed on a spectrum analyzer. The amount of work required to implement this process was actually not great, as most of the considerations were the same as those for the parallel ADC process. What this implied for the parallel sampling board, was that a structure had to be designed that could take the

signals from twelve parallel 100 MHz DACs and recombine them into a 1200 MHz signal. In order to do this, the exact same architecture as the for parallel sampling system was used, except that no hold amplifier was required on the sampling gates, since the DAC signal provided the hold voltage. Thus the signals from the DACs were routed to an additional set of twelve sampling gates (with no hold amplifiers) which were fired in the same fashion as the input parallel sampling gates. When these output gates opened, the signals from the DACs appeared on an output meander line (structurally the same as the input meander line) and proceeded to travel in both directions. At one end of the output meander line there was a resistive termination, and at the other end there was an amplifier and lowpass filter. The signal that arrived at the output amplifier consisted of the sum of the output pulses from the twelve output sampling gates. This signal, after filtering, was the re-creation of the input signal with a 4-bit quantization imposed upon it. A block diagram of the overall system is shown in Figure 44.

Physically, it was decided to implement the output recombination system on the same board as the input parallel sampling system. This would enable the two sets of sampling gates to use the same firing lines, and would simplify the timing synchronization with the ADCs and DACs.

Figure 44: Overall system.

Thus the parallel sampling board consisted of 12 input sampling gates with hold amplifiers, 12 output sampling gates, a bipolar spike generator, and the required bias circuitry for all of the sampling gates and the spike generator. The bias circuitry consisted of two Op-Amp/power MOSFET source follower circuits to provide the ± 2 V bias for the sampling gates, and a temperature compensated OP-Amp/NPN-transistor emitter follower, adjustable voltage source for the SRD biasing. The temperature compensation was required because it was found that the optimal bias voltage on the bipolar spike generator changed with temperature.

After deciding what components were needed on the parallel sampling board, the board itself was designed. Because of all of the relatively high-frequency signals, and to avoid the inherent dispersion problems of non-TEM transmission lines, it was decided that most of the signal lines on the board should be implemented in stripline. The result of this was that the board design used nine layers. The material chosen for the board was .010" thick Rogers RO2800 .010" thick laminate. A data sheet on this material can be found in Appendix D. This material was selected as it had a low loss tangent and was physically very stable over temperature (i.e. it had a low thermal co-efficient of expansion or TCE), as opposed to PTFE based substrates which

have a much higher TCE. The layering structure chosen for the board is as follows:

Layer 1:	Microstrip	(outer component tracks and DAC sampling gates)
Layer 2:	Ground	
Layer 3:	Stripline	(output meander line)
Layer 4:	Ground	
Layer 5:	Stripline	(bipolar spike lines)
Layer 6:	Ground	
Layer 7:	Stripline	(input meander line)
Layer 8:	Ground	
Layer 9:	Microstrip	(outer component tracks and ADC sampling gates)

A photograph of the bare board is shown in Figures 45 and 46. Figure 45 is the front (layer 1) and Figure 46 is the back (layer 9). Additional photographs of the populated board are shown in Figures 42 and 43. (These pictures are of a second revision, so some of the component positions have been changed).

In order to connect the sampling board to the parallel ADCs and DACs, SMB variant slide-on jacks and plugs were used so that all twelve channels could be fed in and out of the

Figure 45: Side one of unpopulated parallel sampling board: Rev. 1.

Figure 46: Side two of unpopulated parallel
sampling board: Rev. 1.

Figure 47: Side one of populated parallel sampling board: Rev. 2.

Figure 48: Side two of populated parallel sampling board: Rev. 2.

board. Thus the entire board plugged into the rest of the system. These plugs can be seen in the photographs.

In laying out the board, the first consideration was the bandpass characteristics of the periodic structures. The periodic structure seen by the bipolar spike generator on the firing lines was the most critical, as there were twenty four closely spaced capacitive vias attached to the firing lines[†]. The spacing that was decided upon for these vias was 0.35", with every second via going to the output DAC sampling gates. The choice of .35" was physically the closest spacing that could be obtained for the taps on the firing lines. This was done in order to obtain as high a possible first cut-off frequency in the periodic structure of the firing line so as to minimize the dispersion in the firing lines.

The calculations for this periodic structure were done using (51) and (52). Perhaps the most difficult thing to estimate in these calculations was the capacitive loading of each tap. Using the quoted value of $C_{j0} = .15$ pF and the parasitic case capacitance of .07 pF, it was felt that the best estimate that could be made for the capacitive loading of the periodic structure was .22 pF per tap. This ignored

[†] The vias appeared capacitive rather than inductive because the pads on either end of the via were the significant feature, as opposed to the via's length which was quite short.

any contribution to the capacitance made by the pads of the via, but it was felt that the capacitance presented by the vias was small and would not significantly change the overall estimate. The reason an estimate had to be made for the tap capacitance was that it was not financially possible to fabricate a test board in order to verify the tap capacitance. As it turned out the estimated value was in error by 7%. This will be discussed in the next chapter. Thus using .22 pF in (51) and (52), the propagation velocity of the spikes at their fundamental frequency of 100 MHz was calculated. From the exact equation (51) this value was found to be 1.595×10^8 m/s and from the dispersion-less approximation equation (52), the value was found to be 1.597×10^8 m/s. As can be seen, the value from (52) is very close to the correct value, as the frequency of 100 MHz was still significantly below the first cutoff point of the periodic structure. However, because of dispersion, each higher harmonic in the 100 MHz spike would travel more slowly through the structure than harmonic before it, until at the cut-off point in the periodic structure, there would be no propagation at all. The effects of this are not very pronounced as can be seen in Figure 43. Here the leading edge of the spike at the output of the line appears to have close to the same rise time as the spike at the input to the line (Figure 42). However the trailing edge of the spike is quite degraded. This appears to be due to charge storage in the sampling gate diodes. As

well, the presence of the 100 MHz signal can be seen in the ripple that the spikes are riding on. Because of this dispersion effect, it was not possible to truly calculate the propagation velocity of the spikes on the firing lines, since they were made up of frequency components all travelling at different velocities. Fortunately, as can be seen from the calculation of (52), the effects of dispersion were quite small at the fundamental and continued to be so until the cut-off frequency was approached.

From (45), the cut-off frequency in the firing lines occurred when $k_0 d = \pi$. This corresponded to spacing the tap capacitances $\lambda/2$ wavelengths apart. Thus for a spacing of .35", cutoff would occur at:

$$\frac{2\pi f \sqrt{2.9}}{3 \times 10^8} \times .35 \times .0254 = \pi$$

or:

$$f = 9.91 \text{ GHz}$$

This meant that the first 99 harmonics of the 100 MHz spikes could propagate through the firing lines. Thus for the calculations it was reasonable to assume that the propagation velocity of the fundamental was equal to the propagation velocity of the spikes.

Dispersion also occurred on the meander lines, except here it was more of a problem because the taps were spaced farther apart which meant that the cutoff frequency would be

lower. Using (53) to calculate the time t_m required between taps on the input meander line (and remembering that every other tap on the firing line was connected to the output meander line) it was found that:

$$t_m = \frac{1}{1.2 \times 10^9} - \frac{2 \times .35 \times .0254}{1.595 \times 10^8}$$

$$= 721.9 \text{ psec}$$

Thus from (52) it was possible to say that the required spacing d_m between taps on the input meander line was :

$$d_m = \sqrt{\frac{721.9 \times 10^{-12}}{283.8 \times 10^{-9} \left(113.5 \times 10^{-12} + \frac{2 \times 0.22 \times 10^{-12}}{d_m} \right)}}$$

$$d_m = .1253 \text{ m} = 4.932''$$

This corresponded to an approximated v_g of $1.735 \times 10^8 \text{ m/s}^\dagger$. In the above, (52) was used for ease of calculation. Next this velocity was checked with (51) (at $f = 550 \text{ MHz}$) in order to determine what the magnitude of the error was. Using (51) and a tap spacing of $.1253 \text{ m}$, a velocity of $v_g = 1.730 \times 10^8 \text{ m/s}$ was found (see Appendix B for the calculations). Over the distance of $.1253 \text{ m}$ this corresponded to a difference of 2 psec or at 550 MHz an angular distance of 0.4° . After a distance of 12 taps at 550 MHz , the total angular error would have been 4.8° . This corresponded to a 1 LSB worst case error at the zero crossing of the 550 MHz sine wave.

[†] The factor of 2 in the calculation was due to the fact that two diodes were connected to each tap on the meander line, thus presenting double the capacitance of a tap on the firing lines.

Next checking the group velocity from (51) at the low frequency of 50 MHz we find that $v_g = 1.735 \times 10^8$ m/s. which corresponds to the approximated value of v_g . This showed that at the upper operating frequencies of the parallel sampling system, there would be a slight signal degradation due to the dispersion. The solution to this was to use the velocity of the signal at 550 MHz to determine the tap spacing. This would still result in a 2 psec/tap timing error, but in this case the error would be at 50 MHz where it would only produce an angular error of $.036^\circ$, which over twelve taps amounted to a total angular error of $.432^\circ$. In theory, this eliminated the quantization error. Thus the spacing between taps on the input (and output) meander lines was chosen to be:

$$\begin{aligned} d_m &= 721.9 \cdot 10^{-12} \cdot 1.730 \cdot 10^8 \\ &= .1249 \text{ m} = 4.917'' \end{aligned}$$

This spacing was the optimal tap spacing when the taps presented a periodic capacitive load of .22 pF on the firing lines, and .44 pF on the meander lines. Obviously this value was not exact, and as a result there would be spacing errors. However it was the best estimate available. The boards were fabricated using this tap spacing and then were evaluated afterwards so that a better second iteration could be made.

4.4.1 Board Simulation Program

Because of the complexity of the 12 channel parallel sampling system, in order to understand it better, a program was written to simulate it. The program was called PARSIM and a compiled copy of the program can be found in Appendix C. An in-depth explanation of this program also supplied in Appendix C. Thus only a brief overview will be given here. Basically the program has an two input files: PSIM.DAT which contains the overall system simulation parameters (such as the intended sampling frequency of the system) and PSKEW.DAT which contains the individual sampling gate parameters (such as the timing skew associated with each tap). Listings of the two files for a typical simulation are given in Tables 3 and 4 of Appendix A. By observing these files, it can be seen that the data input is fairly self explanatory: for instance, the PSKEW.DAT file contains the parameters for a 4 tap simulation.

When executed, the program reads these two input files and then proceeds with the simulation. The program then outputs two files. One is called PDATA.PTS and this contains data representing analog voltages that correspond to the sampled data obtained in the simulation. Also stored with this data is an integer number representing the number of the point (with 0 being the first point). This output data file

was produced so that other data manipulation programs could be used to analyze the data. The second output file is called PSPEC.PTS and this file contains a listing of the line spectra of the waveform that the data in PDATA.PTS represents.

The final information provided by the program is the number of effective bits for the simulation. This is the equivalent number of bits an ADC would need in order to produce the same S/N ratio as the simulation did. It is used as a measure of the accuracy of the simulated parallel ADC process. The number is determined by fitting a sine wave to the sampled data and then determining the RMS error between the fitted sine wave and the actual sine wave. This error is then used to determine the equivalent number of bits of the theoretical ADC. More about how this works can be found in the program listing in Appendix C.

This program will now be used to demonstrate some of the effects that occur in a parallel sampled system. (To facilitate understanding, the output data file PSPEC.PTS was plotted for all of the examples). The first plot in this set of examples is shown in Figure 49. For this plot the PSIM.DAT file shown in Table 3 of Appendix A was used. This file set the sampling aperture of in the simulation to be 1000 psec and the quantization to be 16 bits. In conjunction

Effective bits = 12.47

SNR = 79.83 dB

Figure 49: A perfect 16-bit system.

with this file, a twelve-tap version of "PSKEW.DAT" that was set to have no timing or voltage skews was used. As can be seen from the plot of the spectrum in Figure 49, the spectrum has one line at 460 MHz (which can be seen to be the input signal frequency from the PSIM.DAT file) and a low power level line at 180 MHz. The presence of this line at 180 MHz was unexpected and resulted from the slew rate limitations of the six-diode switch when sampling the 460 MHz signal at 1200 Msamples/sec. This line corresponds to the $3f_{in} - f_s$ intermodulation product, and being only -78 dB down causes the effective bits of the system to go to 12.47.

In the next simulation, shown in Figure 50, the number of bits of quantization in the simulation was reduced to 4. This resulted in the appearance of more spectral lines. These lines were generated by the 4-bit quantization errors. It should be noted here that these spectral lines could be at any frequency, as they are purely a function of the input signal frequency[†].

In the next simulation, which is shown in Figure 51, the aperture of the 4-bit system was reduced to 200 psec in order

[†] As explained more clearly in Appendix C, this program avoided windowing errors on the digitized data by imposing periodicity upon data. This was done by rounding the input signal frequency and the clock frequency to the closest 10 MHz. This ensured periodicity over a 100 nsec interval.

Effective bits = 3.96

SNR = 28.62 dB

Figure 50: A perfect 4-bit system.

Effective bits = 3.35

SNR = 24.96

Figure 51: A perfect 4-bit system with
slew rate limitations.

to demonstrate the effect of slew rate problems. As can be seen, the effective number of bits drops by .6 and spectral lines appear at all of the 10 MHz harmonics indicating the presence of events that occur only once during the 100 nsec interval. It can also be seen that stronger spectral lines appear at the same frequencies that they occurred at in Figure 50.

The next simulation (Figure 52) is the same as the previous one except that the aperture width was set to 600 psec in order to simulate the actual aperture width used. As can be seen, and as was predicted in the switch simulations, the 600 psec aperture does not cause any quantization errors for a 4-bit system. Thus the spectrum shown in Figure 52 is identical to that in Figure 50 and represents an essentially perfect 4-bit sampling system.

The next four cases will demonstrate the effects of various errors that can occur in a parallel sampling system. The first error is one tap failing to operate. This was simulated by setting the gain of Tap #12 to zero. The results are shown in Figure 53. As would be expected, there are strong spectral lines at 100 MHz and its harmonics, but there are even stronger intermodulation lines at 140 MHz and 160 MHz which are caused by mixing of the quantization spectral lines with the 100 MHz spectral line and its

Effective bits = 3.96

SNR = 28.62 dB

Figure 52: A 4-bit system with a 600 psec aperture.

Effective bits = 1.41

SNR = 13.25 dB

Figure 53: A 4-bit system with one tap missing.

harmonics. As can also be seen, there is less energy in the fundamental than previously.

The next error case which is shown (Figure 54) demonstrates the effect of a designed-in timing skew. For this case a timing skew of 36 psec/tap was used (arbitrarily chosen). As can be seen, there are no 100 MHz spectral lines present. As well, there are some very strong interference lines present. One frequency of especial interest is the line at 480 MHz. This was caused by the fact that the system has actually sampled the 460 MHz signal further along in time each sample than it should have. For the example above, the timing skew caused a doppler shift on the input data causing the system to appear that was actually sampling a 480 MHz signal (the average $d\phi/dt = 20$ MHz). However this condition persisted for only twelve samples. After the last tap had sampled the data, the bipolar spike generator fired again and the timing skew was temporarily corrected. The result of this was that the sampled spectrum appeared to be a 480 MHz signal which was periodically phase shifted down by 20 MHz at 100 MHz intervals. At these shift intervals, the rate of change of the sampled signal changed by far less than it should have. For instance, on the twelfth tap the sample was taken $36 \times 11 = 396$ psec further ahead on the signal than it should have been. Thus for the 1200 MHz desired sampling period of 833 psec, the first tap would have sampled the

Effective bits = 1.10

SNR = 11.40 dB

Figure 54: A 4-bit system with timing skew.

signal only 437 psec later than the last tap. Thus as well as creating a doppler-shifted remainder signal 20 MHz higher in frequency, every 100 nsec there was an amplitude change on the sampled signal. This was what caused the AM sidebands at 360 MHz and 560 MHz on the 460 MHz signal, as well as the smaller signals at 260 MHz, 160 MHz and 60 MHz.

The final error case is shown in Figure 55. Here the twelfth tap was given a fixed 200 mV DC offset. As expected, strong spectral lines were produced at the clock frequency and its harmonics. It should be noted that these lines were stronger than the clock harmonics produced by the missing tap in Table 13. Furthermore, the intermodulation products were fewer.

With these simulations, the operation of the parallel sampling system can be better understood.

Effective bits = 1.88
SNR = 16.09 dB

Figure 55: A 4-bit system with a one tap DC offset.

CHAPTER 5: MEASUREMENTS

5.1 Introduction

This chapter is concerned with the measured performance of the prototype parallel sampling system. Only the results of the overall system are given here as the data for the subsystems were presented in Chapter 4.

5.2 Parallel Sampling System Results

After the parallel sampling board was fabricated, it was used as a "test bed" for the diode switch and the bipolar spike generator. Once these subsystems were up and running, the remainder of the board was assembled. The first thing to be measured was the input meander line's transmission characteristic. This measurement was done using a scalar network analyzer. The results are shown in Figure 56. As can be seen there was a 5 dB dip in the transmission characteristic at 630 MHz, but this is safely away from the maximum input signal frequency of 550 MHz. As well, the loss slope of .58 dB/100 MHz was quite reasonable and did not cause any major problems.

The next test was to determine the parallel sampling alignment of all of the taps on the board. This test

Figure 56: Transmission characteristic of the loaded input meander line.

consisted of presenting a constant DC voltage to all of the output DAC recombination sampling gates. The signal out of the output meander line would then display the tap alignment for all of the taps. In order to observe this combined output signal, the output filter and amplifier were bypassed. A photograph of the results of this test is shown in Figure 57. The upper trace is the combination of all of the gated DC voltages put out onto the meander line from each tap. In this photograph the input signal frequency to the bipolar spike generator was adjusted so that the output spikes from each tap were perfectly aligned. What this means is that there was a designed-in tap-spacing error in this prototype (due to the uncertainty of the actual capacitive periodic loading on the firing lines and the meander lines). Thus the interval between taps along the meander line was incorrect. In order to correct for this spacing error, the frequency of the bipolar spike generator had to be adjusted so that the period of the bipolar spike generator was equal to twelve times the time between the output pulses from the sampling gates. As can be seen this occurred when the frequency of the signal driving the bipolar spike generator was equal to 93 MHz. Thus the sampling frequency of this parallel sampling board was $93 \times 12 = 1116$ Ms/sec. This resulted in a Nyquist frequency of 558 MHz. In order to correct this problem and increase the sampling frequency to the desired 1200 Ms/sec, the meander line had to be shortened by roughly

Figure 57: Output signal for a constant DC input on the output meander line.

7%. However, this could not be done without refabricating the board. Thus in order to properly test this board, the parallel sampling system was run at 93 MHz. This is the reason why many of the photographs were taken using a clock frequency of 93 MHz instead of 100 MHz.

Next, a series of "back-to-back" tests were run. In these tests, the output of the input sampling gates were directly connected to the input of the output sampling gates. In this way it was possible to determine the upper performance limit of the parallel sampling system operating as a digital delay device. (i.e. capturing the data, digitizing it, and then reproducing it). This was because the process of analogue-to-digital conversion and then digital-to-analogue conversion could only serve to degrade the signal quality. Four plots of the output signal spectrum for this test are shown in Figures 58 to 61. Three of these plots were made using a pulsed RF signal. The duty cycle of this test signal was chosen to be 1% and output blanking was used so that the noise generated by the sampling system was not seen on the spectrum analyzer during the 99% off-time of the signal. The first plot (Figure 58) shows the output for a pulsed 490 MHz input signal and a 93 MHz clock. The second plot (Figure 59) shows a 260 MHz pulsed signal and a 93 MHz clock. The next plot (Figure 60) shows a 270 MHz CW signal

Figure 58: "Back-to-back" test of the system with $f = 490$ MHz and a 93 MHz clock.

Figure 59: "Back-to-back" test of the system with $f = 260$ MHz and a 93 MHz clock.

Figure 60: "Back-to-back" test of the system with $f = 270$ MHz and a 100 MHz clock.

Figure 61: "Back-to-back" test of the system with $f = 460$ MHz and a 100 MHz clock.

and a 100 MHz sample clock. The final plot (Figure 61) shows a 460 MHz pulsed signal and a 100 MHz sample clock.

It is purely by coincidence that the sampling frequency came out to the value of 1116 Ms/sec. When the original tests were run, it was found that running the board with a 100 MHz input signal produced roughly the same results as running the board with a 93 MHz signal. This was due to the fact that with a 100 MHz clock the sample taken by the last tap almost exactly overlapped the signal taken by the first tap, effectively creating an 1100 Ms/sec system when operated in the "back to back" mode[†]. This situation was different from the doppler modulation simulation of a designed-in timing skew (Figure 54), as the signal sampling points in this scenario were exactly recreated on the output meander line in the same places that they were taken. Thus the output of the system using a 100 MHz clock was virtually the same as that for a 93 MHz clock. The only difference was that the twelfth tap in the 100 MHz case became redundant.

As can be seen from these four photographs, the desired signal is about +10 dB greater than the highest spurs for all cases. This rather limited the effectiveness of having a 4

[†] The "back-to-back" testing at 100 MHz was the first view of the overall system that was obtained. Thus the appearance of the Nyquist frequency at 550 MHz instead of at 600 MHz caused quite a bit of confusion initially.

bit quantization scheme, but the results were still deemed successful, especially considering the complexity of the system. One point that should be noted is that in all four plots, the output signal amplitude at all frequencies across the band of interest was displayed. Even though the Nyquist frequency in all of the cases was 550 MHz, the plots were continued up to this frequency anyway. An item of interest is that in the 100 MHz clock cases, the peak output signal amplitude is reduced every 100 MHz beginning at 50 MHz. This was due to problems with the buffer amplifiers at 50 MHz, and this problem was resolved before the clock frequency was dropped to 93 MHz.

In order to help understand what the main causes of the spurious signals were on the parallel sampling board, it was decided that it would be worthwhile to attempt to match the performance of the parallel sampling system to the theoretically predicted performance of a simulation using the PARSIM program (see Section 4.4.1). The plot in Figure 61 was chosen as the one for which matching would be attempted.

A clue to a problem in the parallel sampling board was gained by studying the photograph shown in Figure 57. From this picture, it can be seen that the fifth and seventh taps on the output meander line had relatively significant DC offsets. Figure 61 showed that at 100 MHz and its harmonics

there were significant clock spurs. Thus it was decided that the most probable cause of the spurious signals in Figure 61 was these DC offsets. After several attempts, and some inverse Fourier transform work it was found that the following PARSIM simulation produced results very close to the spectrum of Figure 61. A plot of the simulated spectrum is shown in Figure 62. As can be seen, the 100 MHz harmonics match quite well, however some of the intermodulation product amplitudes are not correct. The simulation file can be found in Table 5 in Appendix A.

This simulation was done using 11 taps as this was the effective sampling rate of the system. It was very difficult to exactly match the output spectrum of any of the back-to-back tests as there were far too many variables that affected the output spectrum. Had an exact spectral simulation match been desired, much more stringent control over all of the parallel sampling board parameters would have been required. For a prototype of this nature, this was impossible.

From the above, it can be seen that most of the problems in this parallel sampling board appear to be due to DC offsets caused by mismatching of components and misalignments in the placement of the sampling gates on the bipolar spike lines.

Effective bits = 1.66

SNR = 14.79 dB

Figure 62: Spectrum of 460 MHz simulation of the spectrum shown in Figure 61.

After these tests were done, the parallel sampling board was integrated with the ADCs and the DACs. However this work concerned the overall system and was outside the scope of this thesis.

As can be seen, the parallel sampling system operated well considering that this was the first prototype, and that there was only a minor error in the estimated periodic capacitance on the signal lines.

This concludes the presentation of the results.

CHAPTER 6: SUMMARY

6.1 Summary

In this thesis the development of a parallel sampling system for use with twelve 100 MHz ADCs was discussed. All of the theory used to design the system has been developed (including the equivalence of single-point and parallel sampling systems), and an extensive numerical simulation program presented that was used to compare the theoretical predictions of the system's performance to the actual results obtained from measurement. This program was also used to demonstrate the spectral degradation that arose from errors in the parallel sampling system. With this it was shown that good agreement exists between theory and practice for this parallel sampling system. In addition, all of the techniques used to construct this board and the novel bipolar impulse generator have been discussed, as well as their associated problems and their resolution.

6.2 Recommendations for Future Work

The major recommendation for improving the parallel sampling board would be redesign the layout of the meander lines again to correct the sampling frequency. In terms of

more far-reaching work. research is needed in the following areas:

- (a) Sampling Gate: As was mentioned Section 2.3. the sampling gates that were used did not incorporate input buffer amplifiers. and employed diodes to switch the bridge current. With the advent of reliable GaAs monolithic processes. it should be possible to develop a monolithic sampling gate with a single input clock. a continuously variable voltage controlled phase shifter for timing skew adjustment. a high impedance signal input and a low impedance ADC driver output. Even if such a gate were spread over several devices and implemented as a hybrid. it would still be superior to the sampling gate that was used for this iteration.

- (b) Feedback Skew Adjustment: Accurate tap placement is impossible with any sort of assembly process. not to mention skew effects caused by thermal expansion. In order to overcome this. some sort of self-calibration circuit is required. This circuit would adjust the clock skew lines of the monolithic sampling gate described in (a) so that the sampling of the input signal would occur at exactly the correct instant on the input waveform. There are

several possible routes that could be followed to achieve this.

With the development of the two circuits described above in (a) and (b), it should then become possible to construct a parallel sampling system that is self-calibrating and good for at least 8-bits of ADC performance. All that is required to achieve this is time, money, and a significant amount of effort.

APPENDIX A

A.1 Simulation Files and Listings

In this section, listings and files used in the various simulations are presented.

SWITCH

```

VPP 1 0 TRAN=PULSE(-4 12 .5N .1N .1N 1P 1N)
RPP 1 2 50
RPPT 2 0 50
VBP 4 0 DC 15V
RBP 4 3 1100
VSIG 6 0 TRAN=SIN(0 2 331MEG 0 0 0)
RSIG 6 5 50
RSIGT 5 0 50
VBN 9 0 DC -15V
RBN 9 8 1100
VPN 11 0 TRAN=PULSE(12 -4 .5N .1N .1N 1P 1N)
RPN 11 10 50
RPNT 10 0 50
X1 3 2 DIODE
X2 3 5 DIODE
X3 3 7 DIODE
X4 5 8 DIODE
X5 7 8 DIODE
X6 10 8 DIODE
RHOLD 7 0 1G
CHOLD 7 0 3P

*DIODE MODEL

.SUBCKT DIODE 1 2
L1 2 3 .16N
D1 1 3 DMOD
.MODEL DMOD D(IS=196.22E-12 RS=4 CJO=.12P BV=-5)
.ENDS DIODE

.OPTIONS LIMPTS=1001
.TRAN 50P 4N
.FILE TRAN V(2), V(3), V(5), V(7)
.END

```

Table 1: Typical SPICE simulation file

SPICE Simulation Component Values

CHOLD = 3 pF

RBP = RBN = VARIABLE

RHOLD = 1 G Ω

RPN = RPNT = 50 Ω

RPP = RPPT = 50 Ω

RSIG = RSIGT = 50 Ω

VBP = -VBN = +15 V

VPP = -VPN = DC OFFSET TRIANGULAR PULSE TRAIN

VLOW = -4 V (this translates after the
VHIGH = +12 V divider into -2 V -> +6 V)

PRF = 2 GHz

RISE TIME = FALL TIME = 100 psec

PULSE WIDTH (at base of triangle) = 200 psec

VSIG = SINE WAVE

PEAK AMPLITUDE = 2 V (1 V after the divider)

FREQUENCY = 331 MHz

SPICE Simulation Cases

CASE #1 (Figure 26): RBP = RBN = 3900 Ω

CASE #2 (Figure 27): RBP = RBN = 390 Ω

CASE #3 (Figure 28): RBP = RBN = 390 Ω

VSIG = 1 Ω

VSIGT = O/C (∞ Ω)

VSIG PEAK AMP = 1 V (no divider)

CASE #4 (Figure 29): RBP = RBN = 1100 Ω

CASE #5 (Figure 30): RBP = RBN = 1100 Ω

RISE TIME = FALL TIME = 300 psec

PULSE WIDTH = 600 psec

Table 2: SPICE simulation summary

SIMULATION DATA

*integer sampling frequency of individual tap in MHz:
100.0
*peak amplitude of input sine wave into the load in volts:
.4
*DC offset of input sine wave in volts:
0.0
*frequency of the input sine wave in MHz:
460
*start phase of input sine wave in degrees:
0.0
*number of bits of quantization of A/Ds:
16
*lower voltage reference levels of the A/Ds in volts:
-.4
*upper voltage reference levels of the A/Ds in volts:
.4
*the aperture width of all the taps in picoseconds:
1000
*the diode switch bias resistor value in ohms:
1100
*the hold capacitor value in pF:
3
*the diode switch bias voltage in volts:
15
*the 1 mA forward conduction voltage of the bridge diodes in
volts
.5
*the source and termination impedance of the diode bridge
driver in ohms:
50
*the designed in tap spacing error in picoseconds:
0

Table 3: Typical PSIM.DAT file

SKEW PARAMETERS

*Tap #1

*timing skew in picoseconds:

0

*gain (loss) multiplier of the hold amplifier

1

*DC offset of the sampling circuit in millivolts:

0

*lower reference skew in millivolts:

0

*upper reference skew in millivolts:

0

*Tap #2

*timing skew in picoseconds:

0

*gain (loss) multiplier of the hold amplifier

1

*DC offset of the sampling circuit in millivolts:

0

*lower reference skew in millivolts:

0

*upper reference skew in millivolts:

0

*Tap #3

*timing skew in picoseconds:

0

*gain (loss) multiplier of the hold amplifier

1

*DC offset of the sampling circuit in millivolts:

0

*lower reference skew in millivolts:

0

*upper reference skew in millivolts:

0

*Tap #4

*timing skew in picoseconds:

0

*gain (loss) multiplier of the hold amplifier

1

*DC offset of the sampling circuit in millivolts:

0

*lower reference skew in millivolts:

0

*upper reference skew in millivolts:

0

Table 4: Typical PSKEW.DAT file

SKEW PARAMETERS

*Tap #1

*timing skew in picoseconds:

0

*gain (loss) multiplier of the hold amplifier

1

*DC offset of the sampling circuit in millivolts:

-30

*lower reference skew in millivolts:

0

*upper reference skew in millivolts:

0

*Tap #2

*timing skew in picoseconds:

0

*gain (loss) multiplier of the hold amplifier

1

*DC offset of the sampling circuit in millivolts:

27

*lower reference skew in millivolts:

0

*upper reference skew in millivolts:

0

*Tap #3

*timing skew in picoseconds:

0

*gain (loss) multiplier of the hold amplifier

1

*DC offset of the sampling circuit in millivolts:

-37

*lower reference skew in millivolts:

0

*upper reference skew in millivolts:

0

*Tap #4

*timing skew in picoseconds:

0

*gain (loss) multiplier of the hold amplifier

1

*DC offset of the sampling circuit in millivolts:

-31

*lower reference skew in millivolts:

0

*upper reference skew in millivolts:

0

Table 5: PSKEW.DAT file used to match the output spectrum shown in Figure 61

```

*Tap #5
*timing skew in picoseconds:
0
*gain (loss) multiplier of the hold amplifier
1
*DC offset of the sampling circuit in millivolts:
200
*lower reference skew in millivolts:
0
*upper reference skew in millivolts:
0

*Tap #6
*timing skew in picoseconds:
0
*gain (loss) multiplier of the hold amplifier
1
*DC offset of the sampling circuit in millivolts:
-31
*lower reference skew in millivolts:
0
*upper reference skew in millivolts:
0

*Tap #7
*timing skew in picoseconds:
0
*gain (loss) multiplier of the hold amplifier
1
*DC offset of the sampling circuit in millivolts:
-37
*lower reference skew in millivolts:
0
*upper reference skew in millivolts:
0

*Tap #8
*timing skew in picoseconds:
0
*gain (loss) multiplier of the hold amplifier
1
*DC offset of the sampling circuit in millivolts:
27
*lower reference skew in millivolts:
0
*upper reference skew in millivolts:
0

```

(Table 5: cont'd)

```

*Tap #9
*timing skew in picoseconds:
0
*gain (loss) multiplier of the hold amplifier
1
*DC offset of the sampling circuit in millivolts:
-30
*lower reference skew in millivolts:
0
*upper reference skew in millivolts:
0

*Tap #10
*timing skew in picoseconds:
0
*gain (loss) multiplier of the hold amplifier
1
*DC offset of the sampling circuit in millivolts:
-30
*lower reference skew in millivolts:
0
*upper reference skew in millivolts:
0

*Tap #11
*timing skew in picoseconds:
0
*gain (loss) multiplier of the hold amplifier
1
*DC offset of the sampling circuit in millivolts:
-30
*lower reference skew in millivolts:
0
*upper reference skew in millivolts:
0

```

APPENDIX B

B.1 Bipolar Spike Generator Calculations

This section presents the calculations used to obtain the values of the components shown in Figure 41. First the value of the inductor was determined. This was found from (21) as follows: we know from the data sheet of the varactor (Appendix D) that $C_j(-6 \text{ V}) = 0.5 \text{ pF}$ and the parasitic case capacitance of case style 17 is 0.17 pF . Thus the total capacitance at -6 V is 0.67 pF . From (21) we have:

$$600 \times 10^{-12} = \pi(L_1 \cdot 2 \times 0.67 \times 10^{-12})^{\frac{1}{2}}$$

$$L_1 = 27.2 \text{ nH}$$

From (22) and with $\epsilon_r = 2.9$ for the R02800 substrate (see Appendix D) we have:

$$27.2 \times 10^{-9} = 10 \times 10^{-9} \times \ell \sqrt{2.9}$$

$$\ell = 1.60 \text{ cm} = .63''$$

The next item to be selected was the parallel resonance capacitor C_2 . Using (23) we have:

$$C_2 = \frac{(600 \times 10^{-12})^2}{2 \times 0.36 \times 10^{-9} \times \pi^2}$$

$$C_2 = 50.7 \text{ pF}$$

Finally the matching capacitor C_1 was selected. Calculating the input impedance looking into the half section of the

circuit (see Figure 19) for a frequency of $f_{in} = 100$ MHz we have:

$$\begin{aligned}
 Z_{in} &= j\omega_{in}L_1 + R_{Term} \left[\frac{1}{j\omega_{in}2C_2} + (j\omega_{in} \frac{L_p}{2} + \frac{1}{j\omega_{in}2C_V}) \right] \\
 &\approx j2\pi \times 100 \times 10^6 \times 27.2 \times 10^{-9} + 50 \left[\frac{-j}{4\pi \times 100 \times 10^6 \times 50.7 \times 10^{-12}} \right. \\
 &\quad \left. + (j\pi \times 100 \times 10^6 \times 0.36 \times 10^{-9} + \frac{-j}{4\pi \times 100 \times 10^6 \times 2 \times 10^{-12}}) \right]
 \end{aligned}$$

Here we have made the approximation that $C_V = 2$ pF is roughly equal to the average diode capacitance that the input frequency f_{in} will see. Thus:

$$Z_{in} \approx 4.18 - j13.84 \, \Omega$$

or:

$$Y_{in} \approx 20 + j66.2 \, \text{mS}$$

Thus we should choose $2 \times C_1$ so that its admittance at f_{in} is equal to 66.2 mS. This will give us an overall Z_{in} on each arm of $1/0.02 = 50 \, \Omega$ which is what we desire. Thus:

$$2\pi \times 100 \times 10^6 \times 2C_1 = 66.2 \times 10^{-3}$$

$$C_1 = 52.7 \, \text{pF}$$

This completes the calculation of the bipolar spike generator component values.

B.2 Signal Line Propagation Calculations

The calculations for the propagation velocity down the signal lines are now shown. The first case is for the firing lines with the taps spaced at 0.35" intervals. Thus:

$$C = 0.22 \text{ pF}$$

$$d = .35 \times .0254 = 0.0089 \text{ m}$$

From (49) we have:

$$\begin{aligned} \frac{\bar{B}}{2} &= \frac{\omega C Z_0}{2} \\ &= \frac{2\pi \times 100 \times 10^6 \times 0.22 \times 10^{-12} \times 50}{2} \\ &= 3.46 \text{ mS} \end{aligned}$$

$$\begin{aligned} k_0 \cdot d &= \frac{2\pi f d \sqrt{\epsilon_r}}{c} \\ &= \frac{2\pi \times 100 \times 10^6 \times 0.0089 \times \sqrt{2.9}}{3 \times 10^8} \\ &= 0.032 \text{ radians} \end{aligned}$$

From (46) we have:

$$\begin{aligned} \beta \cdot d &= \arccos(\cos(0.032) - 3.46 \times 10^{-3} \times \sin(0.032)) \\ &= 0.035 \text{ radians} \end{aligned}$$

Thus from (51):

$$\begin{aligned} v_g &= \frac{\frac{3 \times 10^8}{\sqrt{2.9}} \sin(0.035)}{(3.46 \times 10^{-3} + 1) \sin(0.032) + 3.46 \times 10^{-3} \times \cos(0.032)} \\ &= 1.595 \times 10^8 \text{ m/s} \end{aligned}$$

In order to compare this with (52) we must calculate the distributed capacitance and inductance for a 50 Ω line.

Thus:

$$\begin{aligned} C_0 &= \frac{\sqrt{\epsilon_r}}{c Z_0} \\ &= \frac{\sqrt{2.9}}{3 \times 10^8 \times 50} \\ &= 113.5 \text{ pF/m} \end{aligned}$$

Now:

$$Z_0 = \left(\frac{L_0}{C_0} \right)^{\frac{1}{2}}$$

Thus:

$$\begin{aligned} L_0 &= Z_0^2 C_0 \\ &= 50^2 \times 113.5 \times 10^{-12} \\ &= 283.8 \text{ nH/m} \end{aligned}$$

Now from (52) we find:

$$\begin{aligned} v_g &= \frac{1}{\sqrt{283.8 \times 10^{-9} (113.5 \times 10^{-12} + \frac{0.22 \times 10^{-12}}{0.35 \times 0.0254})}} \\ &= 1.597 \times 10^8 \text{ m/s} \end{aligned}$$

The next case is for the input meander line with the tap spacing of .1253 m:

$$C = 0.44 \text{ pF}$$

$$d = 0.1253 \text{ m}$$

$$\bar{B} = \frac{\omega C Z_0}{2}$$

$$= \frac{2\pi \times 550 \times 10^6 \times 0.44 \times 10^{-12} \times 50}{2}$$

$$= 38.01 \text{ mS}$$

$$k_c \cdot d = \frac{2\pi f d \sqrt{\epsilon_r}}{c}$$

$$= \frac{2\pi \times 550 \times 10^6 \times 0.1253 \times \sqrt{2.9}}{3 \times 10^8}$$

$$= 2.4579 \text{ radians}$$

From (46) we have:

$$\beta \cdot d = \arccos(\cos(2.4574) - 38.01 \times 10^{-3} \times \sin(2.4574))$$

$$= 2.4969 \text{ radians}$$

Thus from (51):

$$v_g = \frac{\frac{3 \times 10^8}{\sqrt{2.9}} \sin(2.4969)}{(38.01 \times 10^{-3} + 1) \sin(2.4579) + 38.01 \times 10^{-3} \times \cos(2.4579)}$$

$$= 1.730 \times 10^8 \text{ m/s}$$

Comparing this with the results from (52) we get:

$$v_g = \frac{1}{\sqrt{283.8 \times 10^{-9} (113.5 \times 10^{-12} + \frac{0.44 \times 10^{-12}}{0.1253})}}$$

$$= 1.735 \times 10^8 \text{ m/s}$$

The final calculations are the check on the propagation velocity of the above spacing from (51) at 50 MHz:

$$C = 0.44 \text{ pF}$$

$$d = 0.1253 \text{ m}$$

$$\bar{B} = \frac{\omega C Z_0}{2}$$

$$= \frac{2\pi \times 50 \times 10^6 \times 0.44 \times 10^{-12} \times 50}{2}$$

$$= 3.46 \text{ mS}$$

$$k_0 \cdot d = \frac{2\pi f d \sqrt{\epsilon_r}}{c}$$

$$= \frac{2\pi \times 50 \times 10^6 \times 0.1253 \times \sqrt{2.9}}{3 \times 10^8}$$

$$= 0.2235 \text{ radians}$$

From (46) we have:

$$\beta \cdot d = \arccos(\cos(0.2235) - 3.46 \times 10^{-3} \times \sin(0.2235))$$

$$= 0.2269 \text{ radians}$$

Thus from (51):

$$v_g = \frac{\frac{3 \times 10^8}{\sqrt{2.9}} - \sin(0.2269)}{\left(\frac{3.46 \times 10^{-3}}{0.2235} + 1 \right) \sin(0.2235) + 3.46 \times 10^{-3} \times \cos(0.2235)}$$

$$= 1.735 \times 10^8 \text{ m/s}$$

APPENDIX C

C.1 Numerical Solution to Diode Bridge

As was mentioned previously it was desired to write a computer program that could accurately simulate the overall parallel sampling system. In order to do this, it was first necessary to write a routine that could determine what the output voltage on the sampling gate would be for a given input waveform, with the gate held open for a certain duration of time. The solution to this problem was attacked by writing a routine that would solve the differential equation in (13). This equation related the current flowing into the hold capacitor to its final output voltage. Thus a routine that determined what the instantaneous value of i_5 was for a given V_i was required.

The numerical solution of i_5 for a given V_C and V_i requires (14), (15), and (17). The technique that was used was a three dimensional Newton-Raphson iterative routine¹⁴, where V_A , V_B , and V_D were the unknowns. This method is guaranteed to converge if there is only one solution to the set of equations and all of the equations are monotonic and differentiable at all points in the search area. Thus we can write (14), (15), and (17) as:

$$f_1 = I_s R [e^{\Lambda(V_A - V_C)} + e^{\Lambda(V_A - V_B)} - 2] + V_A - V = 0 \quad (55)$$

$$f_2 = I_S R_S [e^{\Lambda(V_B - V_D)} - e^{\Lambda(V_A - V_B)}] + 2V_B - V_i = 0 \quad (56)$$

$$f_3 = I_S R_S [e^{\Lambda(V_B - V_D)} - e^{\Lambda(V_C - V_D)}] - 2V_D - V = 0 \quad (57)$$

With this technique, the functions that we wish to find the solutions for are expressed as Taylor series. Hence, for the three functions $f_1(V_A, V_B)$, $f_2(V_A, V_B, V_D)$, and $f_3(V_B, V_D)$ we can express the functions at a new point in terms of an old point. For instance:

$$f_1(V_A^{i+1}, V_B^{i+1}) = f(V_A^i, V_B^i) + \frac{\partial f_1}{\partial V_A}(V_A^{i+1} - V_A^i) + \frac{\partial f_1}{\partial V_B}(V_B^{i+1} - V_B^i) + \dots \quad (58)$$

for f_1 , and similarly for f_2 and f_3 . Now if the point is close to the actual root (V_A^*, V_B^*, V_D^*) , we can approximate and say:

$$\frac{\partial f_1}{\partial V_A} \cdot \Delta V_A + \frac{\partial f_1}{\partial V_B} \cdot \Delta V_B = -f_1(V_A^i, V_B^i) \quad (59)$$

$$\frac{\partial f_2}{\partial V_A} \cdot \Delta V_A + \frac{\partial f_2}{\partial V_B} \cdot \Delta V_B + \frac{\partial f_2}{\partial V_D} \cdot \Delta V_D = -f_2(V_A^i, V_B^i, V_D^i) \quad (60)$$

$$\frac{\partial f_3}{\partial V_B} \cdot \Delta V_B + \frac{\partial f_3}{\partial V_D} \cdot \Delta V_D = -f_3(V_B^i, V_D^i) \quad (61)$$

Thus by the use of cofactor matrices we can solve for ΔV_A , ΔV_B , and ΔV_D which will describe the change in V_A , V_B , and V_D needed to take us toward the solution. Hence we need to find the partial derivatives of (55) - (57). Thus for $f_1(V_A, V_B)$:

$$a_{11} = \frac{\partial f_1}{\partial V_A} = \Delta I_s R [e^{\Lambda(V_A - V_C)} + e^{\Lambda(V_A - V_B)}] - 1 \quad (62)$$

$$a_{12} = \frac{\partial f_1}{\partial V_B} = -\Delta I_s R e^{\Lambda(V_A - V_B)} \quad (63)$$

$$a_{13} = \frac{\partial f_1}{\partial V_D} = 0 \quad (64)$$

For $f_2(V_A, V_B, V_D)$:

$$a_{21} = \frac{\partial f_2}{\partial V_A} = -\Delta I_s R_s e^{\Lambda(V_A - V_B)} \quad (65)$$

$$a_{22} = \frac{\partial f_2}{\partial V_B} = \Delta I_s R_s [e^{\Lambda(V_B - V_D)} + e^{\Lambda(V_A - V_B)}] + 2 \quad (66)$$

$$a_{23} = \frac{\partial f_2}{\partial V_D} = -\Delta I_s R_s e^{\Lambda(V_B - V_D)} \quad (67)$$

For $f_3(V_B, V_D)$:

$$a_{31} = \frac{\partial f_3}{\partial V_A} = 0 \quad (68)$$

$$a_{32} = \frac{\partial f_3}{\partial V_B} = \Delta I_s R e^{\Lambda(V_B - V_A)} \quad (69)$$

$$a_{33} = \frac{\partial f_3}{\partial V_D} = -\Delta I_s R [e^{\Lambda(V_B - V_D)} + e^{\Lambda(V_C - V_D)}] - 1 \quad (70)$$

We can now implement an iterative procedure to use the following equations:

$$V_A^{i+1} = V_A^i + \Delta V_A \quad (71)$$

$$V_B^{i+1} = V_B^i + \Delta V_B \quad (72)$$

$$V_D^{i+1} = V_D^i + \Delta V_D \quad (73)$$

where:

$$\Delta V_A = \begin{bmatrix} -f_1(V_A^i, V_B^i) & a_{12} & 0 \\ -f_2(V_A^i, V_B^i, V_D^i) & a_{22} & a_{23} \\ -f_3(V_B^i, V_D^i) & a_{32} & a_{33} \end{bmatrix} \quad (74)$$

J

$$\Delta V_B = \begin{bmatrix} a_{11} & -f_1(V_A^i, V_B^i) & 0 \\ a_{21} & -f_2(V_A^i, V_B^i, V_D^i) & a_{23} \\ 0 & -f_3(V_B^i, V_D^i) & a_{33} \end{bmatrix} \quad (75)$$

J

$$\Delta V_D = \begin{bmatrix} a_{11} & a_{12} & -f_1(V_A^i, V_B^i) \\ a_{21} & a_{22} & -f_2(V_A^i, V_B^i, V_D^i) \\ 0 & a_{32} & -f_3(V_B^i, V_D^i) \end{bmatrix} \quad (76)$$

J

and:

$$J = \begin{bmatrix} a_{11} & a_{12} & 0 \\ a_{21} & a_{22} & a_{23} \\ 0 & a_{32} & a_{33} \end{bmatrix} \quad (77)$$

where J is the Jacobian of the system of equations. Expanded this is:

$$J = a_{11}a_{22}a_{33} - a_{11}a_{23}a_{32} - a_{12}a_{21}a_{33} \quad (78)$$

In order for this iteration to always work, J must never go to zero for any point within the search area. It can be shown by expanding (78) that for all real values of V_A , V_B , and V_D , J is always negative. This expansion is not shown as it is very long and it is enough to know that J never goes to zero. Thus through the use of (55) - (57) and (62) - (76)

the iteration can be set up and the solution obtained. The iteration is terminated when:

$$[\Delta V_A^2 + \Delta V_B^2 + \Delta V_D^2]^{\frac{1}{2}} < \epsilon \quad (79)$$

and ϵ is an arbitrarily chosen small number.

These equations were incorporated into a routine called IC (for capacitor current or I_C) that accepted as its inputs the voltage on the capacitor V_C and the switch input voltage V . This routine would then solve for the instantaneous current into the the capacitor i_5 by using (16). Thus we can write (where the routine IC returns i_5):

$$\frac{dV_C}{dt} = \frac{1}{C} \cdot IC(V_i(t), V_C) \quad (80)$$

With this routine it was then possible to write a program that performed a numerical solution of the differential equation in (20). The method chosen was an Adams-Bashforth/Adams-Moulton predictor/corrector algorithm. This is a fourth-order multi-point[†] technique which means that it is fast and accurate. As well, the technique gives a measure of the error at each point. Unfortunately it is not self-starting, as it requires four points to start. Thus, a Runge-Kutta routine is used to start the predictor/corrector

[†] When we speak of points, what is being referred to is the time increment that the algorithm is operating on. Basically, we wish to know what the value of a variable expressed as a differential equation is after a certain amount of time. In order to solve this, the interval of time is broken into increments, and each increment is referred to as a point.

algorithm, as Runge-Kutta techniques are self starting and are also fourth order. The Runge-Kutta algorithm is as follows:

$$V_C^{i+1} = V_C^i + \frac{\Delta t}{6} \cdot [K_1 + 2K_2 + 2K_3 + K_4] \quad (81)$$

where:

$$K_1 = IC(V_i(t), V_C^i) \quad (82)$$

$$K_2 = IC(V_i(t + \frac{\Delta t}{2}), V_C^i + \frac{K_1}{2}) \quad (83)$$

$$K_3 = IC(V_i(t + \frac{\Delta t}{2}), V_C^i + \frac{K_2}{2}) \quad (84)$$

$$K_4 = IC(V_i(t + \Delta t), V_C^i + K_3) \quad (85)$$

and Δt is the time increment. With this technique, the next three points are obtained (i.e. V_C at $t = 0, \Delta t, 2\Delta t, 3\Delta t$). Once these points have been obtained it is possible to switch over to the Adams-Bashforth/Adams-Moulton algorithm. This algorithm first predicts what the next point will be, and then using the predicted value corrects itself, thus giving an idea of how much in error a given point is. If the error is considered too large, then the step size can be reduced. Thus the step size can be tailored to fit the problem. The algorithm is in two parts. The Adams-Bashforth predictor is (where the "bar" indicates a predicted value):

$$\bar{V}_C^{i+1} = V_C^i + \frac{\Delta t}{24} \cdot [55K_2 - 59K_3 + 37K_4 - 9K_5] \quad (86)$$

and the Adams-Moulton corrector is:

$$V_C^{i+1} = V_C^i + \frac{\Delta t}{24} \cdot (9K_1 + 19K_2 - 5K_3 + K_4) \quad (87)$$

where:

$$K_1 = IC(V_i(t+\Delta t), V_C^{i+1}) \quad (88)$$

$$K_2 = IC(V_i(t), V_C^i) \quad (89)$$

$$K_3 = IC(V_i(t-\Delta t), V_C^{i-1}) \quad (90)$$

$$K_4 = IC(V_i(t-2\Delta t), V_C^{i-2}) \quad (91)$$

$$K_5 = IC(V_i(t-3\Delta t), V_C^{i-3}) \quad (92)$$

These equations were incorporated into a routine called DSWTCHNR (for diode switch Newton-Raphson). Thus the two routines, IC and DSWTCHNR could be used together to determine the final hold voltage on the sampling capacitor for a given input voltage $V_i(\cdot)$. In order to test these two routines, a program called SW was written which basically exercised these two functions. A listing of this program is given in section C.3.

C.2 System Simulation Program

After the diode sampling gate simulation was dealt with, a program was written called PARSIM (for parallel simulation) which could simulate the overall parallel sampling system. What it did was read the simulation parameters from one file (PSIM.DAT) and the tap parameters from another file

(PSKEW.DAT). With this information, the program would simulate the parallel sampling system over a period of time. The interval over which the program ran was arbitrarily set to 100 nsec which was also the shortest common period. This was an interval in time over which both the sampling clock and the input test waveform could be guaranteed to be periodic. In order to ensure that this was so, it was decided to round the input signal frequency and the sampling clock frequency to the nearest 10 MHz. The reason that this was done was to avoid windowing problems when a discrete Fourier transform was done on the sampled data points.

After reading in the simulation data, all of the input variables (such as timing skew, etc.) are normalized to the system sampling frequency in order to simplify the program. Then the program proceeds to simulate the parallel sampling system over the 100 nsec interval by collecting the sampled voltages from all of the taps as they sampled the input waveform. This data is then quantized to simulate the effect of the ADCs, and finally a discrete Fourier transform is performed upon the sampled data so that the spectral composition can be determined. As well, the number of effective bits of the simulation is calculated. With this program it was possible to investigate the effects that various system parameters had on the integrity of the sampled

* PARALLEL TAPS. THE FORMAT OF THIS FILE IS AS FOLLOWS (AND AGAIN
 * THIS FORMAT MUST BE ADHERED TO!!):
 *

LINE NUMBER	DESCRIPTION	
1	comment line	
2	comment line	
3	comment line	
4	timing skew in picoseconds	
5	comment line	Skew
6	gain (loss) multiplier of channel	Parameters
7	comment line	for
8	DC offset of the channel in millivolts	Tap #1
9	comment line	
10	lower reference skew in millivolts	
11	comment line	
12	upper reference skew in millivolts	
13		
14	comment line	
15	comment line	
16	timing skew in picoseconds	
17	comment line	Skew
18	gain (loss) multiplier of channel	Parameters
19	comment line	for
20	DC offset of the channel in millivolts	Tap #2
21	comment line	
22	lower reference skew in millivolts	
23	comment line	
24	upper reference skew in millivolts	
25		
26	comment line	
27	comment line	
28	timing skew in picoseconds	
29	comment line	Skew
30	gain (loss) multiplier of channel	Parameters
31	comment line	for
32	DC offset of the channel in millivolts	Tap #3
33	comment line	
34	lower reference skew in millivolts	
35	comment line	
36	upper reference skew in millivolts	
37		
38	comment line	
39	comment line	
40	timing skew in picoseconds	
41	comment line	Skew
42	gain (loss) multiplier of channel	Parameters
43	comment line	for
44	DC offset of the channel in millivolts	Tap #4
45	comment line	
46	lower reference skew in millivolts	
47	comment line	
48	upper reference skew in millivolts	

data. A complete listing of this program is given in section C.4.

In the listing of this program, a very detailed explanation of the operation of the program is given, as well as references used in writing it. If more information on the program is required, the reader is directed to the program listing.

C.3 Program Listing of SW

In this section, a compiled listing of the FORTRAN program SW is given. The program has very detailed comments which make it easy to read.

*

* TITLE: DIODE SWITCH NEWTON-RAPHSON SOLUTION

* AUTHOR: PAUL LANGNER

* DATE: JULY 21, 1989

* DESCRIPTION: THIS PROGRAM DETERMINES THE OUTPUT VOLTAGE OF A
 * SIX DIODE SWITCH DRIVING A HOLD CAPACITOR. THE DC INPUT
 * VOLTAGE AND THE CAPACITOR START VOLTAGE ARE ENTERED BY THE
 * USER AT THE START OF THE PROGRAM. THE PROGRAM THEN CALCULATES
 * THE OUTPUT VOLTAGE AND CURRENT AT THE CAPACITOR OVER SEVERAL
 * POINTS OF THE SAMPLING INTERVAL. THE SAMPLING INTERVAL IS
 * GIVEN AS A CONSTANT IN THE PROGRAM. AS WELL AS THE NUMBER OF
 * INTERVALS.

*

* THE VOLTAGE THAT IS ON THE HOLD CAPACITOR AFTER THE CHARGING IS
 * DONE IS FOUND THROUGH NUMERICAL METHODS. THE DESCRIPTION OF
 * METHODS IS FAR TOO COMPLICATED TO BE WRITTEN HERE, BUT A BRIEF
 * OVERVIEW WILL BE ATTEMPTED. BASICALLY, THE SIX DIODE SWITCH WHEN
 * TURNED ON IS MODELLED AS A FOUR DIODE BRIDGE WITH PULL UP AND PULL
 * DOWN RESISTORS ON THE TOP AND BOTTOM OF THE BRIDGE. THE INPUT
 * SIGNAL IS APPLIED TO THE BRIDGE THROUGH A SOURCE RESISTOR, RS AND
 * AN IDENTICAL TERMINATION RESISTOR, RS. THE HOLD CAPACITOR SITS
 * ON THE OTHER SIDE OF THE BRIDGE. AT THE BEGINNING OF THE SAMPLE,
 * WHICH IS EQUIVALENT TO TIME $T=T_0$, THE CAPACITOR HAS A VOLTAGE OF
 * V_{C0} . A FUNCTION CALLED IC IS THEN CALLED TO DETERMINE THE
 * INSTANTANEOUS CURRENT THAT IS FLOWING INTO THE CAPACITOR. THIS
 * FUNCTION USES A 3 DIMENSIONAL NEWTON-RAPHSON ALGORITHM TO
 * DETERMINE THE VOLTAGES AND CURRENTS AT THE OTHER THREE NODES IN
 * THE CIRCUIT. ONCE WE HAVE THE INSTANTANEOUS CURRENT, WE KNOW
 * THAT:

*

$$dV/dT = I/C \quad (1)$$

*

* WITH THIS, A NUMERICAL ROUTINE IS USED TO FIND VC AT $T=TAU$. THIS
 * ROUTINE IS A COMBINATION OF ROUTINES. THE TIME TAU IS ARBITRARILY
 * DIVIDED INTO 16 INCREMENTS. VC IS DETERMINED AT THE FIRST FOUR
 * INCREMENTS USING A RUNGE-KUTTA ROUTINE. AFTER FOUR POINTS HAVE
 * BEEN FOUND, THE POINTS ARE TURNED OVER TO AN ADAMS-BASHFORTH/
 * ADAMS-MOULTON PREDICTOR/CORRECTOR ALGORITHM. THIS THEN CALCULATES
 * THE REMAINDER OF THE POINTS IN THE INTERVAL TAU. IT CAN BE SHOWN
 * THAT THIS SET OF EQUATIONS WILL ALWAYS CONVERGE FOR ANY SET OF
 * REAL VALUES. THE VARIABLES IN THE TWO FUNCTIONS ARE AS FOLLOWS:

*

* TAU = NORMALIZED SAMPLING APERATURE WIDTH
 * C = NORMALIZED CAPACITANCE IN 1/OHMS
 * V = CHARGE VOLTAGE APPLIED TO THE RC NETWORK IN VOLTS
 * VC = THE INITIAL VOLTAGE ON THE HOLD CAPACITOR
 * R = BIAS RESISTOR THAT VCH IS BEING APPLIED THROUGH
 * RS = PARALLEL INPUT IMPEDANCE OF THE SIGNAL SOURCE
 * AND TERMINATION

*

* REFERENCES:


```

*
*      (1) P.STARK, "INTRODUCTION TO NUMERICAL METHODS".
*          NEW YORK: THE MACMILLAN CO.. 1970. PAGES 123-272.
*
*      (2)   E.KREYSZIG, "ADVANCED ENGINEERING MATHEMATICS".
*          NEW YORK: JOHN WILEY AND SONS, 1983.  PAGES 830-842.
*
*****
*
*
*
*****
*
*START OF MAIN PROGRAM
*
*****
*
*
*
      PROGRAM DSWTCHNR
*
*PARAMETER DEFINITIONS
*
      IMPLICIT DOUBLE PRECISION (A-Z)
      INTEGER NUMPTS
      PARAMETER(NUMPTS = 16)
*
*TYPE DEFINITIONS
*
      INTEGER J,J1,J2,J3,J4
      DOUBLE PRECISION C,TAU,DT,TP,VP,VI
      DOUBLE PRECISION K1,K2,K3,K4,K5
      DOUBLE PRECISION V(NUMPTS + 1),I(NUMPTS + 1)
*
*PARAMETERS
*
*define the hold capacitor value
      C = 3.0D-12
*
*define the aperature width
      TAU = 600.0D-12
*
*INITIALIZATION
*
*write prompt
      PRINT *, 'INPUT VALUES FOR VI AND VC: '
*
*read answers
      READ *, VI,V(1)
*
*calculate the time step width
      DT = TAU/NUMPTS

```

```

*
*calculate the first four starting points via Runge-Kutta
DO 10, J = 1, 3
    I(J) = IC(VI,V(J))/C
    K1 = I(J)*DT
    TP = TP + DT/2.0
    VP = V(J) + K1/2.0
    K2 = IC(VI,VP)*DT/C
    VP = V(J) + K2/2.0
    K3 = IC(VI,VP)*DT/C
    TP = J*DT
    VP = V(J) + K3
    K4 = IC(VI,VP)*DT/C
*
*calculate the next V
    V(J + 1) = V(J) + (K1 + 2.0*K2 + 2.0*K3 + K4)/6.0
10  CONTINUE
*
*calculate the current corresponding to V(4)
    I(4) = IC(VI,V(4))/C
*
*calculate the remaining points via the
*Adams-Bashforth/Adams-Moulton predictor/corrector method

DO 20, J = 5, NUMPTS + 1
    J1 = J - 1
    J2 = J - 2
    J3 = J - 3
    J4 = J - 4
*
*calculate the predictor voltage
    VP = V(J1) + DT*(55.0*I(J1) - 59.0*I(J2)
    + 37.0*I(J3) - 9.0*I(J4))/24.0
*
*calculate the next point in time
    TP = TP + DT
    K1 = IC(VI,VP)/C
*
*calculate the corrector voltage
    V(J) = V(J1) + DT*(9.0*K1 + 19.0*I(J1)
    + 5.0*I(J2) + I(J3))/24.0
*
*calculate the current at the new point
    I(J) = IC(VI,V(J))/C
20  CONTINUE
*
*OUTPUT AND PROGRAM WRAP-UP
*
*print answer
    WRITE (UNIT = *, FMT = 100) VI,V(1)
100  FORMAT(' THE INITIAL VOLTAGES WERE: VI = ',F7.3,' V'/

```

```

VC = '.F7.3.' V'//)
WRITE (UNIT = *, FMT = 200)
200  FORMAT('      TIME',8X,'CAPACITOR CURRENT'.6X,
        'CAPACITOR VOLTAGE')
DO 30, J = 1, NUMPTS + 1
    WRITE (UNIT = *, FMT = 300) DBLE(DT*(J-1)*1.0D12),
        I(J)*1.0D3*C.V(J)
30  CONTINUE
300  FORMAT(' ',F7.3,' psec ',.6X,F7.3,' mA ',.11X,F7.3,' V')
*
*halt program
STOP
END

*****
*
*END OF MAIN PROGRAM
*
*****
*
*
*
*
*****
*
*START OF FUNCTION DEFINITIONS
*
*****
*
*
*
DOUBLE PRECISION FUNCTION IC(VI,VC)
*
*TYPE DEFINITIONS
*
INTEGER J
DOUBLE PRECISION GAMMA,IS,ERR,VI,VA,VB,VC,VD
DOUBLE PRECISION DA,DB,DD,JAC,SIGMA,AB,AC,BD,CD
DOUBLE PRECISION VT,R,RS,V,FA,FB,FD,ISR,ISRS
DOUBLE PRECISION FAA,FAB,FBA,FBB,FBD,FDB,FDC
DOUBLE PRECISION GISR,GISRS
*
*PARAMETERS
*
*define the threshold voltage for 1 mA forward conduction in
*the diodes as well as the bias resistor value in ohms, the
*input's source and termination impedance in ohms, the bias
*voltage on the switch in volts
VT = 0.5
R = 1100
RS = 50
V = 15

```

```

*
*CONSTANTS
*
  GAMMA = 1/.0259
  IS = 1.0D-3/(DEXP(GAMMA*VT) -1.0)
  ERR = 1.0D-10
  ISR = IS*R
  ISRS = IS*RS
  GISR = GAMMA*ISR
  GISRS = GAMMA*ISRS
*
*BEGIN
*
*decide which case the simulation falls into
  IF (VI.GE.VC) THEN
*
*assign start points
    VA = VC + VT
    VB = (R*VI - RS*(V - VT))/(RS + 2.0*R)
    VD = VB - VT
  ELSE
*
*assign start points
    VD = VC - VT
    VB = (R*VI + RS*(V - VT))/(RS + 2.0*R)
    VA = VB + VT
  ENDIF
*
*perform iteration until DC operating point is solved
10  CONTINUE
*
*calculate the exponentials used throughout the solution
  AB = DEXP(GAMMA*(VA - VB))
  AC = DEXP(GAMMA*(VA - VC))
  BD = DEXP(GAMMA*(VB - VD))
  CD = DEXP(GAMMA*(VC - VD))
*
*calculate the values of the three current functions
*and their non zero partial derivatives with respect
*to each other
  FA = ISR*(AC + AB - 2.0) + VA - V
  FB = ISRS*(BD - AB) + 2.0*VB - VI
  FD = ISR*(BD + CD - 2.0) - VD - V
  FAA = GISR*(AC + AB) + 1.0
  FAB = -GISR*AB
  FBA = -GISRS*AP
  FBB = GISRS*(I., + AB) + 2.0
  FBD = -GISRS*BD
  FDB = GISR*BD
  FDD = -GISR*(BD + CD) - 1.0
*
*compute the Jacobian matrix of the partial derivatives

```

```

      JAC = FAA*FBB*FDD - FAA*FBD*FDB - FAB*FBA*FDD
*
*halt if Jacobian is equal to zero
      IF (JAC.EQ.0.000) THEN
          PRINT *, 'JACOBIAN EQUALS ZERO!!'
          STOP
      ENDIF
*
*compute the cofactors
      DA = (-FA*FBB*FDD + FA*FBD*FDB
            -FAB*FBD*FD + FAB*FB*FDD)/JAC
      DB = (-FAA*FB*FDD + FAA*FBD*FD + FA*FBA*FDD)/JAC
      DD = (-FAA*FBB*FD + FAA*FB*FDB
            +FA*FBA*FDB + FAB*FBA*FD)/JAC
*
*calculate the next guess at the answer
      VA = VA + DA
      VB = VB + DB
      VD = VD + DD
*
*determine if the solution is close enough to the answer
      SIGMA = DSQRT(DA*DA + DB*DB + DD*DD)
*
*branch if the error on the variables is too large
      IF (SIGMA.GE.ERR) GOTO 10
*
*WRAP-UP AND RETURN
*
      IC = IS*(DEXP(GAMMA*(VA - VC)) - DEXP(GAMMA*(VC - VD)))
      RETURN
      END
*
*
*
*****
*
*END OF FUNCTION DEFINITIONS
*
*****

```

C.4 Program Listing of PARSIM

In this section, a compiled listing of the FORTRAN program PARSIM is given. The program has very detailed comments which make it easy to read in order to learn what it is doing.

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* TITLE: PARALLEL SAMPLING SPECTRAL COMPOSITION PROGRAM

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* DATE: JULY 16, 1989

* DESCRIPTION: THIS PROGRAM IS WRITTEN TO SIMULATE THE EFFECTS
 * OF TAP PLACEMENT ERROR, AMPLITUDE HOLD ERROR AND QUANTIZATION
 * ON THE SPECTUM OF A SAMPLED SINUSOID. THE PROGRAM OPERATES IN
 * CONJUNCTION WITH TWO OTHER FILES: "PSIM.DAT" AND "TAP.DAT".
 * BOTH OF THESE FILES SHOULD RESIDE IN THE SAME DIRECTORY AS THIS
 * PROGRAM. THE FILE "PSIM.DAT" CONTAINS ALL OF THE PARAMETERS
 * NECESSARY TO DESCRIBE THE PARALLEL SAMPLED DATA SYSTEM THAT IS
 * SAMPLING AN INCOMING SINUSOID. THE FORMAT OF THE FILE
 * "PSIM.DAT" IS AS FOLLOWS (AND THIS FORMAT MUST BE ADHERED TO!!):

*

LINE NUMBER	DESCRIPTION
1	comment line
2	comment line
3	integer sampling frequency of individual tap in MHz
4	comment line
5	peak amplitude of input sine wave into the load in volts
6	comment line
7	DC offset of input signal in volts
8	comment line
9	integer frequency of the input signal in MHz
10	comment line
11	start phase of input signal in degrees
12	comment line
13	number of bits of quantization of A/Ds
14	comment line
15	lower voltage reference levels of the A/Ds in volts
16	comment line
17	upper voltage reference levels of the A/Ds in volts
18	comment line
19	aperture width of the tap in picoseconds
20	comment line
21	diode switch bias resistor value in ohms
22	comment line
23	hold capacitor value in pF
24	comment line
25	diode switch bias voltage in volts
26	comment line
27	1 mA forward conduction voltage of bridge diodes
28	comment line
29	source and termination impedance in ohms
30	comment line
31	tap spacing error in picoseconds

*

* THUS THE DATA MUST BE ON LINES 3, 5, 7, 9, 11, 13, 15, 17, 19,
 * 21, AND 23 AND IT CAN BE ENTERED IN ANY FORMAT. THE OTHER FILE
 * "PSKEW.DAT" CONTAINS ALL OF THE INFORMATION DESCRIBING TIMING,
 * AMPLITUDE, AND VOLTAGE REFERENCE SKEW ERRORS IN EACH OF THE

* PARALLEL TAPS. THE FORMAT OF THIS FILE IS AS FOLLOWS (AND AGAIN
 * THIS FORMAT MUST BE ADHERED TO!!):
 *

LINE NUMBER	DESCRIPTION	
1	comment line	
2	comment line	
3	comment line	
4	timing skew in picoseconds	
5	comment line	Skew
6	gain (loss) multiplier of channel	Parameters
7	comment line	for
8	DC offset of the channel in millivolts	Tap #1
9	comment line	
10	lower reference skew in millivolts	
11	comment line	
12	upper reference skew in millivolts	
13		
14	comment line	
15	comment line	
16	timing skew in picoseconds	
17	comment line	Skew
18	gain (loss) multiplier of channel	Parameters
19	comment line	for
20	DC offset of the channel in millivolts	Tap #2
21	comment line	
22	lower reference skew in millivolts	
23	comment line	
24	upper reference skew in millivolts	
25		
26	comment line	
27	comment line	
28	timing skew in picoseconds	
29	comment line	Skew
30	gain (loss) multiplier of channel	Parameters
31	comment line	for
32	DC offset of the channel in millivolts	Tap #3
33	comment line	
34	lower reference skew in millivolts	
35	comment line	
36	upper reference skew in millivolts	
37		
38	comment line	
39	comment line	
40	timing skew in picoseconds	
41	comment line	Skew
42	gain (loss) multiplier of channel	Parameters
43	comment line	for
44	DC offset of the channel in millivolts	Tap #4
45	comment line	
46	lower reference skew in millivolts	
47	comment line	
48	upper reference skew in millivolts	

THE PARAMETERS IN THIS FILE CAN BE REPEATED AS MANY TIMES AS DESIRED. THE ABOVE EXAMPLE SHOWS THE PARAMETER FILE CONTAINING THE PARAMETERS FOR FOUR PARALLEL TAPS. THIS IS BY NO MEANS ARBITRARY. AS THE NUMBER OF TAPS DEFINED IN THIS FILE DEFINES THE NUMBER OF TAPS THAT WILL BE USED IN THE SIMULATION. THUS IF SIX TAPS WERE DESIRED, THE PARAMETERS FOR SIX TAPS WOULD BE DEFINED. ALL THAT IS REQUIRED IS THAT THE ABOVE FORMAT BE COPIED (ie. THERE SHOULD BE A BLANK LINE BETWEEN TAPS. EACH TAP DEFINITION SHOULD START WITH TWO COMMENT LINES, FOLLOWED BY THE TIMING SKEW, A COMMENT LINE, THE LINEAR GAIN (OR LOSS) OF THE TAP, THE DC OFFSET OF THE TAP, THE LOWER REFERENCE SKEW, ANOTHER COMMENT LINE, AND FINALLY THE UPPER REFERENCE SKEW). THE LAST LINE OF THE FILE SHOULD BE THE UPPER REFERENCE SKEW OF THE LAST TAP.

UPON START UP, THE SIMULATION PROGRAM "PARSIM.FOR" INITIALIZES ALL OF THE VARIABLES THAT WILL BE USED IN THE SIMULATION. SOME OF THESE VARIABLES ARE ARRAYS THAT MUST BE DEFINED BEFORE PROGRAM EXECUTION OCCURS. THIS IS DONE USING THE "PARAMETER" STATEMENT. THERE IS ONE PARAMETER THAT IS DEFINED: "MAXTAP". THIS PARAMETER DESCRIBES THE MAXIMUM NUMBER OF TAPS THAT CAN BE DEFINED FOR A SIMULATION. IT CAN BE SET TO ANY VALUE.

AFTER THE INITIALIZATION HAS BEEN DONE, THE INPUT DATA FILES ARE READ. THEN A FILE FOR OUTPUT IS OPENED. IT RESIDES IN THE SAME DIRECTORY AS THIS PROGRAM, AND IT WILL CONTAIN A LIST OF ALL OF THE POINTS THAT WERE SAMPLED, AND WHAT THEIR D/A'd VALUE WOULD BE. THE FILE IS CALLED "PDATA.PTS" AND IT IS STRUCTURED SO THAT EACH LINE CONTAINS THE SAMPLE NUMBER FOLLOWED BY A COMMA, AND THEN THE D/A'd DATA VALUE. ONCE THE SIMULATION HAS STARTED, EACH POINT AND ITS SAMPLE NUMBER ARE WRITTEN INTO THIS FILE. THE POINTS ARE OBTAINED BY THREE EXTERNAL FUNCTIONS. THE FIRST IS CALLED "SAMPLE" AND IT IS USED TO SAMPLE THE INCOMING SINUSOID, WITH THE CORRECT CLOCK SKEW FOR EACH TAP. THE SECOND IS CALLED "QUANTIZE" AND QUANTIZES THE VALUE OBTAINED THROUGH "SAMPLE" TO THE CORRECT NUMBER OF BITS AND WITH THE CORRECT REFERENCE SKEWS. FINALLY, THE FUNCTION "DTOA" IS CALLED, AND THIS CONVERTS THE OFFSET BINARY NUMBER RETURNED FROM "QUANTIZE" INTO AN EQUIVALENT D/A'd VOLTAGE.

EACH TIME THE THREE FUNCTIONS ARE CALLED, THEY ARE REFERRING TO A DIFFERENT TAP. THE TAP THEY ARE REFERRING TO IS INDICATED BY THE VARIABLE "TAPNUM". THIS VARIABLE IS COUNTER MODULO THE NUMBER OF TAPS IN THE SIMULATION, AND IS INCREMENTED EACH TIME A NEW DATA POINT IS REQUIRED. AFTER A POINT HAS BEEN OBTAINED AND WRITTEN TO THE OUTPUT FILE, SEVERAL ARRAYS THAT ARE REQUIRED TO DETERMINE THE EFFECTIVE NUMBER OF BITS IN THE SIMULATION ARE UPDATED. AS WELL, THE SPECTRAL LINE WEIGHT DATA ARE SUMMED IN I AND Q. AFTER THE DESIRED NUMBER OF POINTS HAVE BEEN OBTAINED, THE PROGRAM CALCULATES THE EFFECTIVE NUMBER OF BITS. THIS IS DONE USING A METHOD DERIVED BY HEWLETT-PACKARD. IT PERFORMS A

LEAST SQUARES SINUSOIDAL CURVE FIT TO THE SAMPLED DATA POINTS, AND DETERMINES THE LEAST SQUARED ERROR OF THE FIT. THIS CAN THEN BE USED TO DETERMINE THE EFFECTIVE NUMBER OF BITS. THIS METHOD ASSUMES THAT THE FREQUENCY OF THE INCOMING SIGNAL IS KNOWN AND THUS IT IS GREATLY SIMPLER THAN THE EQUIVALENT LEAST SQUARES FIT TO A SERIES OF POINTS THAT HAVE AN UNKNOWN FREQUENCY. IT IS AS FOLLOWS:

A SINE WAVE CONSISTING OF:

$$X_n = A \cos(wt_n) + B \sin(wt_n) + C \quad (1)$$

IS FIT TO THE INCOMING DATA. THIS IS DONE BY MINIMISING THE SQUARED ERROR WHICH IS:

$$e = \text{Sum from } k = 1 \text{ to } M \text{ of } (y_k - x_k)^2 \quad (2)$$

where: y_k = sampled data
 x_k = fit data
 M = #points

TAKING THE PARTIAL DERIVATIVES OF e WITH RESPECT TO A , B , AND C , WE OBTAIN THREE EQUATIONS IN THREE UNKNOWNNS. DUE TO THE DIFFICULTY IN WRITING THE EQUATIONS WITHOUT SPECIAL CHARACTERS, THE REMAINDER OF THE EQUATIONS WILL NOT BE SHOWN HERE, BUT THEY CAN BE FOUND IN THEIR ENTIRETY IN THE FIRST REFERENCE. AFTER ALL OF THE LEAST SQUARED ERROR VARIABLES HAVE BEEN SUMMED IN THE SIMULATION, THE THREE EQUATIONS IN THREE UNKNOWNNS ARE SOLVED FOR. THE 3x3 COEFFICIENT MATRIX IS CALLED "U" AND THE AUGMENTED PORTION OF THE MATRIX "U" IS CALLED Y. THE SOLUTION TO A , B , AND C IS FOUND USING CRAMER'S RULE. CRAMER'S RULE STATES THAT THE SOLUTION VECTOR TO THE SYSTEM CAN BE FOUND BY CALCULATING THE DETERMINANTS OF "U" AND "U" WITH THE VECTOR "Y" SUBSTITUTED FOR ITS FIRST, SECOND, AND THIRD COLUMNS. THESE DETERMINANTS ARE CALLED D , D_1 , D_2 , AND D_3 RESPECTIVELY. THUS:

$$A = D_1/D \quad (3)$$

$$B = D_2/D \quad (4)$$

$$C = D_3/D \quad (5)$$

AFTER THIS IS DONE, THE LEAST SQUARED ERROR VOLTAGE CAN BE FOUND BY SUBSTITUTING #1 INTO #2, EXPANDING, SUBSTITUTING THE VALUES OF A , B , AND C IN AND SOLVING. THEN THE RMS ERROR IS FOUND BY:

$$E_{rms} = \sqrt{e/M} \quad (6)$$

AFTER THIS IS FOUND, THE SNR IS DETERMINED BY USING THE FORMULA:

$$SNR = 20 \cdot \log_{10}(\sqrt{A^2 + B^2}/E_{rms}) \quad (7)$$

FINALLY THE NUMBER OF EFFECTIVE BITS IS FOUND USING THE EQUATION:

$$EB = \text{LOG}_2(\text{SQRT}(A^{**2} + B^{**2})/(\text{SQRT}(3)*\text{Erms})) \quad (8)$$

where: EB = EFFECTIVE NUMBER OF BITS
 FSCALE = FULL SCALE VOLTAGE OF A/D
 Erms = RMS ERROR OF SYSTEM

BOTH OF THESE VALUE ARE THEN PRINTED. AFTER THIS THE PROGRAM CALCULATES THE AMPLITUDES OF THE SPECTRAL LINE WEIGHTS IN dB RELATIVE TO THE AMPLITUDE OF THE INPUT SINE WAVE'S AMPLITUDE. THESE SPECTRAL POINTS ARE ONLY CALCULATED UP TO THE NYQUIST SAMPLING FREQUENCY BECAUSE AFTER THIS POINT THE VALUES REPEAT. THESE VALUES ARE WRITTEN INTO A FILE CALLED "PSPEC.PTS". THE FORMAT IS THE FREQUENCY OF THE SPECTRAL LINE IN MHz, A COMMA, AND THE AMPLITUDE OF THE SIGNAL IN dB. THE EQUATION USED TO CALCULATE THE SPECTRAL DATA IS THE STANDARD FOURIER TRANSFORM INTEGRATED OVER ONE PERIOD OF THE SHORTEST COMMON PERIOD OF THE SAMPLING SIGNAL AND THE INPUT SIGNAL. THIS SHORTEST COMMON PERIOD IS FOUND BY VIRTUE OF THE FACT THAT BOTH THE SAMPLING FREQUENCY AND THE INPUT SIGNAL FREQUENCY ARE CONVERTED TO INTEGER MULTIPLES OF 10 MHz. THUS THE WORST CASE SHORTEST COMMON PERIOD IS EQUAL TO 10 MHz. THUS THE NUMBER OF POINTS THAT ARE OBSERVED OF THE NORMALIZED SIGNAL IS THE INTEGER MULTIPLE OF 10 MHz OF THE SAMPLING FREQUENCY. (ie. IF FS = 1200 MHz. THEN THE NUMBER OF POINTS THAT MUST BE OBSERVED IS 120.)

THE SPECTRAL WEIGHTS ARE THUS:

$$FN = 1/\text{LEN} * \text{INTEGRAL}(ZK * \text{EXP}(-jN\omega t) dt) \quad (9)$$

TAKEN FROM $t = 1$ TO LEN

WHERE: ZK = EQUIVALENT D/A'd VALUE OF THE SAMPLE
 LEN = NUMBER OF SAMPLE POINTS IN THE COMMON PERIOD
 N = THE SPECTRAL LINE NUMBER ($-\text{LEN}/2 \rightarrow \text{LEN}/2$)
 ω = COMMON PERIOD FREQUENCY = $2\pi/\text{LEN}$

THIS INTEGRAL SIMPLIFIES TO BE A SUM BECAUSE THE SAMPLED POINT VALUE, ZK, CORRESPONDS TO A WEIGHTED DELTA FUNCTION TAKEN AT THE SAMPLE TIME, T. THUS:

$$FN = 1/\text{LEN} * \text{SUM}(ZK(i) * \text{EXP}(-jN\omega T)) \quad (10)$$

TAKEN FROM $i = 1$ TO LEN

IN THE PROGRAM, THE EQUATION IS WRITTEN IN TERMS OF THE REAL AND IMAGINARY COMPONENTS SO THAT:

$$FNI = \text{SUM}(ZK(i) * \text{COS}(N\omega T)) \quad (11)$$

TAKEN FROM $i = 1$ TO LEN

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*
*      FNQ = SUM(ZK(i)*-SIN(NWOT))
*          TAKEN FROM i = 1 TO LEN
*
*      AFTER THESE VALUES ARE CALCULATED (NOTICING THAT THE 1/LEN FACTOR
*      HAS BEEN LEFT OUT UNTIL LATER). THE MAGNITUDE OF THE REAL
*      FREQUENCIES ARE CALCULATED WITH RESPECT TO THE AMPLITUDE USING:
*
*      FNDB = 20*LOG(FMAG/AMP)                                (12)
*
*      WHERE: FMAG = 1/LEN * SQRT(FNI**2 + FNQ**2)            (13)
*              AMP = AMPLITUDE OF THE INPUT SINE WAVE
*
*      AFTER THESE VALUES ARE PRINTED THE PROGRAM ENDS.
*
*      REFERENCES:
*
*      (1)  B.J.FROHRING, B.E.PEETZ, M.A.UNKRICH, S.C.BIRD,
*           "WAVEFROM RECORDER DESIGN FOR DYANMIC PERFORMANCE".
*           HEWLETT-PACKARD JOURNAL, FEBRUARY, 1988. PALO ALTO,
*           CALIFORNIA: HEWLETT-PACKARD CCMPANY. PAGE 48.
*
*      (2)  E.KREYSZIG, "ADVANCED ENGINEERING MATHEMATICS".
*           NEW YORK: JOHN WILEY AND SONS, 1983. PAGES 320-321.
*
*      (3)  Y.C.JENQ, "ASYNCHRONOUS DYNAMIC TESTING OF A/D CONVERTERS".
*           HANDSHAKE MAGAZINE. SUMMER 1988. BEAVERTON, OREGON:
*           TEKTRONIX, INC. PAGE 5.
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*****
*
*
*
*****
*
*START' OF MAIN PROGRAM
*
*****
*
*
*
*      PROGRAM PARSIM
*      IMPLICIT DOUBLE PRECISION (A-Z)
*
*      *TYPE DEFINITIONS
*
*      INTEGER MAXTAP, FSMAX
*
*      *define the maximum number of taps permitted in the
*      *simulation, and the maximum sampling frequency that is allowed (in
*      *10s of MHz).

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        PARAMETER (MAXTAP = 20, FS MAX = 200)
*
*declare the remaining variables
        INTEGER BITS, LEN, TAPNUM, NUMTAP, I, J, T, QK
        DOUBLE PRECISION OFFSET, PHI, AMP, FREQ, FS, PI, W, WO, RADANG, RADPHI
        DOUBLE PRECISION LREF, UREF, SNR, TAU, CAP, SPERR, MAG, V, R, RS, VT
        DOUBLE PRECISION FNI(FS MAX), FNQ(FS MAX), FNDB(FS MAX), CHOLD
        DOUBLE PRECISION SK, ZK, AK, BK, EO, E, A, B, C, D, D1, D2, D3, ERMS, EBITS
        DOUBLE PRECISION TSKEW(MAXTAP), GAIN(MAXTAP), DCSHIFT(MAXTAP)
        DOUBLE PRECISION LRSKEW(MAXTAP), URSKEW(MAXTAP), VCAP(MAXTAP)
        DOUBLE PRECISION Y(3), U(3,3)
*
*declare common variables
        COMMON W, RADPHI, AMP, OFFSET, BITS, LREF, UREF, TAU, CAP, R, RS, V, VT
*
*CONSTANTS
*
        PI = 4.0*DATAN(1.0D0)
*
*load simulation parameters from "PSIM.DAT"
*
*open input data file "PSIM.DAT"
        OPEN (UNIT = 8, ACCESS = 'SEQUENTIAL', FORM = 'FORMATTED'
        , FILE = 'PSIM.DAT')
*
*read the data
*
*skip the first two comment records
        READ (UNIT = 8, FMT = *, ERR = 2, END = 2)
        READ (UNIT = 8, FMT = *, ERR = 2, END = 2)
*
*read the sampling frequency
        READ (UNIT = 8, FMT = *, ERR = 2, END = 2) FS
*
*skip the next comment record
        READ (UNIT = 8, FMT = *, ERR = 2, END = 2)
*
*read the amplitude
        READ (UNIT = 8, FMT = *, ERR = 2, END = 2) AMP
*
*skip the next comment record
        READ (UNIT = 8, FMT = *, ERR = 2, END = 2)
*
*read the offset
        READ (UNIT = 8, FMT = *, ERR = 2, END = 2) OFFSET
*
*skip the next comment record
        READ (UNIT = 8, FMT = *, ERR = 2, END = 2)
*
*read the input signal frequency
        READ (UNIT = 8, FMT = *, ERR = 2, END = 2) FREQ
*

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*skip the next comment record
  READ (UNIT = 8, FMT = *, ERR = 2, END = 2)
*
*read the start phase
  READ (UNIT = 8, FMT = *, ERR = 2, END = 2) PHI
*
*skip the next comment record
  READ (UNIT = 8, FMT = *, ERR = 2, END = 2)
*
*read the number of bits
  READ (UNIT = 8, FMT = *, ERR = 2, END = 2) BITS
*
*skip the next comment record
  READ (UNIT = 8, FMT = *, ERR = 2, END = 2)
*
*read the lower reference value
  READ (UNIT = 8, FMT = *, ERR = 2, END = 2) LREF
*
*skip the next comment record
  READ (UNIT = 8, FMT = *, ERR = 2, END = 2)
*
*read the upper reference value
  READ (UNIT = 8, FMT = *, ERR = 2, END = 2) UREF
*
*skip the next comment record
  READ (UNIT = 8, FMT = *, ERR = 2, END = 2)
*
*read the aperature width of the tap
  READ (UNIT = 8, FMT = *, ERR = 2, END = 2) TAU
*
*skip the next comment record
  READ (UNIT = 8, FMT = *, ERR = 2, END = 2)
*
*read the diode switch bias resistor value in ohms
  READ (UNIT = 8, FMT = *, ERR = 2, END = 2) R
*
*skip the next comment record
  READ (UNIT = 8, FMT = *, ERR = 2, END = 2)
*
*read the hold capacitor value in pF
  READ (UNIT = 8, FMT = *, ERR = 2, END = 2) CHOLD
*
*skip the next comment record
  READ (UNIT = 8, FMT = *, ERR = 2, END = 2)
*
*read the diode switch bias voltage in volts
  READ (UNIT = 8, FMT = *, ERR = 2, END = 2) V
*
*skip the next comment record
  READ (UNIT = 8, FMT = *, ERR = 2, END = 2)
*
*read the diode threshold voltage in volts

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      READ (UNIT = 8, FMT = *, ERR = 2, END = 2) VT
*
*skip the next comment record
      READ (UNIT = 8, FMT = *, ERR = 2, END = 2)
*
*read the source and termination impedance in ohms
      READ (UNIT = 8, FMT = *, ERR = 2, END = 2) RS
*
*skip the next comment record
      READ (UNIT = 8, FMT = *, ERR = 2, END = 2)
*
*read the tap spacing error
      READ (UNIT = 8, FMT = *, ERR = 2, END = 2) SPERR
*
*close the file "PSIM.DAT"
      CLOSE (8)
*
*open input data file "PSKEW.DAT"
      OPEN (UNIT = 8, ACCESS = 'SEQUENTIAL', FORM = 'FORMATTED'
           , FILE = 'PSKEW.DAT')
*
*skip the first record in the data file
      READ (UNIT = 8, FMT = *, ERR = 7)
*
*read the skew variables for all of the taps until the EOF
*condition occurs
      DO 4, I = 1, 20
*
*skip the two comment records
          READ (UNIT = 8, FMT = *, ERR = 7, END = 9)
          READ (UNIT = 8, FMT = *, ERR = 7, END = 9)
*
*read the timing skew
          READ (UNIT = 8, FMT = *, ERR = 7) TSKEW(I)
*
*skip the next comment record
          READ (UNIT = 8, FMT = *, ERR = 7)
*
*read the gain (or loss) of the tap
          READ (UNIT = 8, FMT = *, ERR = 7) GAIN(I)
*
*skip the next comment record
          READ (UNIT = 8, FMT = *, ERR = 7)
*
*read the DC offset of the tap
          READ (UNIT = 8, FMT = *, ERR = 7) DCSHIFT(I)
*
*skip the next comment record
          READ (UNIT = 8, FMT = *, ERR = 7)
*
*read the lower reference skew
          READ (UNIT = 8, FMT = *, ERR = 7) LRSKEW(I)

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*
*skip the next comment record
      READ (UNIT = 8, FMT = *, ERR = 7)
*
*read the upper reference skew
      READ (UNIT = 8, FMT = *, ERR = 7) URSKEW(I)
*
*convert DCSHIFT(I), LRSKEW(I) and URSKEW(I) into volts from millivolts
      DCSHIFT(I) = DCSHIFT(I)*1.0E-3
      LRSKEW(I) = LRSKEW(I)*1.0E-3
      URSKEW(I) = URSKEW(I)*1.0E-3
*
*attempt to read the last blank record
      READ (UNIT = 8, FMT = *, END = 6)
4      CONTINUE
      NUMTAP = MAXTAP
      GOTO 8
*
*escape for EOF marker next comment record read attempt
9      NUMTAP = I - 1
      GOTO 8
*
*escape for EOF marker last blank record read attempt
6      NUMTAP = I
8      CONTINUE
*
*close the input data file "PSKEW.DAT"
      CLOSE (8)
*
*PERFORM INITIALIZATIONS
*
*calculate combined sampling frequency
      FS = FS*NUMTAP
*
*round input frequency and sampling frequency to closest 10 MHz
      FREQ = 10.0*ANINT(FREQ/10.0)
      FS = 10.0*ANINT(FS/10.0)
*
*set length equal to FS/10 which will produce the shortest common
*period between FREQ and FS
      LEN = AINT(FS/10.0)
*
*compute the unnormalized and normalized radian frequency,
*radian phase, normalized aperture width, normalized capacitance
*in units of 1/Ohms, and normalized corrected tap spacing.
      W = 2.0*PI*FREQ/FS
      RADPHI = PHI*PI/180.0
      TAU = TAU*FS*1.0E-6
      CAP = CHOLD*FS*1.0E-6
      SPERR = SPERR*FS*1.0E-6
*
*(the factor of 1.0E-6 arises from the fact that the values are in
* picoseconds and the sampling frequency FS is in MHz)

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*
*normalize TSKEW(I) with respect to the sampling period
  DO 5, I = 1, NUMTAP
    TSKEW(I) = TSKEW(I)*FS*1.0E-6
5    CONTINUE
*
*compute the normalized radian frequency of the common period
  WO = 2.0*PI/LEN
*
*zero E0
  E0 = 0.0
*
*zero the two least squared error fit arrays, Y and U
  DO 10, I = 1, 3
    Y(I) = 0.0
    DO 20, J = 1, 3
      U(I,J) = 0.0
20    CONTINUE
10    CONTINUE
*
*zero the real and imaginary spectral weighting values
  DO 21, I = 1, LEN
    FNI(I) = 0.0
    FNQ(I) = 0.0
21    CONTINUE
*
*zero the hold capacitor voltages, VCAP(i)
  DO 22, I = 1, MAXTAP
    VCAP(I) = 0
22    CONTINUE
*
*adjust the values of TSKEW(i) to take into account the designed in
*timing error between taps, SPERR
  DO 23, I = 1, NUMTAP
    TSKEW(I) = TSKEW(I) + I*SPERR
23    CONTINUE
*
*set the tap pointer to point to the first tap
  TAPNUM = 1
*
*open data file
  OPEN (UNIT = 7, FORM = 'FORMATTED', FILE = 'PDATA.PTS')
*
*BEGIN SIMULATION
*
  DO 30, T = 0, (LEN - 1)
*
*obtain the A/D'd value
  SK = SAMPLE(T,DCSHIFT(TAPNUM),TSKEW(TAPNUM),
    VCAP(TAPNUM),GAIN(TAPNUM))
*
*save the hold capacitor voltage from the sample

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      VCAP(TAPNUM) = SK
*
*quantize the sampled voltage
      QK = QUANTIZE(SK,LRSKEW(TAPNUM),URSKEW(TAPNUM))
      ZK = DTOA(QK)
*
*write the data point into the data file
      WRITE (UNIT = 7, FMT = 100) T,ZK
100    FORMAT (I3.3,' ',F11.8)
*
*sum all of the spectral line weights
      DO 31, I = 0, LEN/2
          FNI(I + 1) = FNI(I + 1) + ZK*DCOS(DBLE(I*T*WO))
          FNQ(I + 1) = FNQ(I + 1) - ZK*DSIN(DBLE(I*T*WO))
31    CONTINUE
*
*calculate the sine and cosine of the radian angle
      RADANG = W * T
      AK = DCOS(RADANG)
      BK = DSIN(RADANG)
*
*sum least squared error fit variables
      Y(1) = Y(1) + ZK*AK
      Y(2) = Y(2) + ZK*BK
      Y(3) = Y(3) + ZK
      EO = EO + ZK*ZK
      U(1,1) = U(1,1) + AK*AK
      U(1,2) = U(1,2) + AK*BK
      U(1,3) = U(1,3) + AK
      U(2,2) = U(2,2) + BK*BK
      U(2,3) = U(2,3) + BK
*
*set up TAPNUM to point at the next tap
      TAPNUM = MOD(TAPNUM,NUMTAP) + 1
30    CONTINUE
*
*set remaining least squared error fit variables
      U(2,1) = U(1,2)
      U(3,1) = U(1,3)
      U(3,2) = U(2,3)
      U(3,3) = LEN
*
*calculate the determinants of the matrices U and Y
      D = U(1,1)*U(2,2)*U(3,3) - U(1,1)*U(3,2)*U(2,3)
      + U(2,1)*U(3,2)*U(1,3) - U(2,1)*U(1,2)*U(3,3)
      + U(3,1)*U(1,2)*U(2,3) - U(3,1)*U(2,2)*U(1,3)
*
      D1 = Y(1)*U(2,2)*U(3,3) - Y(1)*U(3,2)*U(2,3)
      + Y(2)*U(3,2)*U(1,3) - Y(2)*U(1,2)*U(3,3)
      + Y(3)*U(1,2)*U(2,3) - Y(3)*U(2,2)*U(1,3)
*
      D2 = U(1,1)*Y(2)*U(3,3) - U(1,1)*Y(3)*U(2,3)

```

```

      + U(2,1)*Y(3)*U(1,3) - U(2,1)*Y(1)*U(3,3)
      + U(3,1)*Y(1)*U(2,3) - U(3,1)*Y(2)*U(1,3)
*
      D3 = U(1,1)*U(2,2)*Y(3) - U(1,1)*U(3,2)*Y(2)
      + U(2,1)*U(3,2)*Y(1) - U(2,1)*U(1,2)*Y(3)
      + U(3,1)*U(1,2)*Y(2) - U(3,1)*U(2,2)*Y(1)
*
*calculate the fit parameters
      A = D1/D
      B = D2/D
      C = D3/D
*
*calculate the total residue error: the absolute value is
*taken so that computer round off error doesn't cause problems
      E = DABS(E0 - 2.0*A*Y(1) - 2.0*B*Y(2) - 2.0*C*Y(3)
      + A*A*U(1,1) + 2.0*A*B*U(1,2) + 2.0*A*C*U(1,3)
      + B*B*U(2,2) + 2.0*B*C*U(2,3) + LEN*C*C)
*
*calculate the RMS error
      ERMS = DSQRT(E/LEN)
*
*calculate the SNR
      SNR = 20.0*DLOG10(DSQRT(A*A + B*B)/ERMS)
*
*calculate the effective number of bits
      EBITS = DLOG(DSQRT(A*A + B*B)/(DSQRT(3.0D0)*ERMS))/DLOG(2.0D0)
*
*open data file
      OPEN (UNIT = 8, FORM = 'FORMATTED', FILE = 'PSPEC.PTS')
*
*output the effective number of bits
      WRITE (UNIT = 8, FMT = 200) EBITS
*
*output the SNR
      WRITE (UNIT = 8, FMT = 300) SNR
*
*calculate the spectral weights in dB relative to the input amplitude
      DO 41, I = 1, LEN/2
        MAG = 2.0*DSQRT(FNI(I + 1)*FNI(I + 1)
        + FNQ(I + 1)*FNQ(I + 1))/LEN
        IF (MAG.EQ.0.0) THEN
          MAG = 1.0D-33
        ENDIF
        FNDB(I + 1) = 20.0*DLOG10(MAG/AMP)
*
*write the data point into the data file
      WRITE (UNIT = 8, FMT = 600) (10*I), FNDB(I + 1)
600      FORMAT (I4.0, ' MHz, ', F6.2, ' dB')
41      CONTINUE
*
*output the effective number of bits
      WRITE (UNIT = *, FMT = 200) EBITS

```

```

200  FORMAT (' THE EFFECTIVE BITS FOR THIS SIMUALTION IS: '.F5.2)
*
*output the SNR
  WRITE (UNIT = *, FMT = 300) SNR
300  FORMAT (' AND THE SNR IS: '.F6.2.' dB')
*
*close the output data files
  CLOSE (8)
  CLOSE (7)
  STOP
*
*ERROR MESSAGES
*
*incorrect amount of input data
2    WRITE (UNIT = *, FMT = *) 'ERROR READING DATA IN FILE "PSIM.DAT"'
  STOP
*
*incorrect amount of input data
7    WRITE (UNIT = *, FMT = *) 'ERROR READING DATA IN FILE "PSKEW.DAT"'
  STOP
  END
*
*
*
*****
*
*END OF MAIN PROGRAM
*
*****
*
*
*
*****
*
*START OF SUBROUTINE DEFINITIONS
*
*****
*
*
*
*****
*
*END OF SUBROUTINE DEFINITIONS
*
*****
*
*
*
*****

```

```

*
*START OF FUNCTION DEFINITIONS
*
*****
*
*
*
*
*****
*
*   TITLE: SAMPLING FUNCTION
*   AUTHOR: PAUL LANGNER
*   DATE: JULY 21, 1989
*   DESCRIPTION: THIS FUNCTION WILL SAMPLE A POINT ON A
*                SINE WAVE THAT IS DESCRIBED BY THE PARAMETERS AMP,
*                OFFSET, W, AND RADPHI.  THE SINEWAVE EQUATION IS:
*
*                
$$VSINE = AMP * SIN(W * T + RADPHI) + OFFSET \quad (1)$$

*
*   WHERE:      AMP = AMPLITUDE (Volts)
*                W  = NORMALIZED RADIAN FREQUENCY
*                OFFSET = DC OFFSET OF INPUT SIGNAL (Volts)
*                RADPHI = RADIAN START PHASE
*                T  = NORMALIZED SAMPLING TIME
*                VSINE = INSTANTANEOUS SINEWAVE VOLTAGE (Volts)
*
*   NOW THIS FUNCTION IS SAMPLING THE SIGNAL VSINE WITH A CERTAIN
*   TIMING SKEW, TSKEW ASSOCIATED WITH THE TAP, AND THE
*   DURATION OF THE SAMPLING APERTURE IS GIVEN AS TAU.  WHEN
*   THE APERTURE IS OPEN, THE SIX DIODE GATE ATTEMPTS TO CHARGE
*   THE HOLDING CAPACITOR ASSOCIATED WITH THE TAP UP TO THE VOLTAGE
*   OF THE INPUT SIGNAL VSINE.  THIS CHARGING IS DONE THROUGH A
*   RESISTOR, THE RC TIME CONSTANT OF THE SYSTEM IS GIVEN AS RC,
*   AND THE CHARGING VOLTAGE IS GIVEN AS VCH.  THE VOLTAGE ON THE
*   CAPACITOR IS ASSUMED TO BE THE VOLTAGE FROM THE PREVIOUS
*   SAMPLE AND THIS VOLTAGE IS STORED IN THE VARIABLE VCAP.
*
*   THE VOLTAGE THAT IS ON THE HOLD CAPACITOR AFTER THE CHARGING IS
*   DONE IS FOUND THROUGH NUMERICAL METHODS.  THE DESCRIPTION OF
*   METHODS IS FAR TOO COMPLICATED TO BE WRITTEN HERE, BUT A BRIEF
*   OVERVIEW WILL BE ATTEMPTED.  BASICALLY, THE SIX DIODE SWITCH WHEN
*   TURNED ON IS MODELLED AS A FOUR DIODE BRIDGE WITH PULL UP AND PULL
*   DOWN RESISTORS ON THE TOP AND BOTTOM OF THE BRIDGE.  THE INPUT
*   SIGNAL IS APPLIED TO THE BRIDGE THROUGH A SOURCE RESISTOR, RS AND
*   AN IDENTICAL TERMINATION RESISTOR, RS.  THE HOLD CAPACITOR SITS
*   ON THE OTHER SIDE OF THE BRIDGE.  AT THE BEGINNING OF THE SAMPLE,
*   WHICH IS EQUIVALENT TO TIME T=To, THE CAPACITOR HAS A VOLTAGE OF
*   VCo.  A FUNCTION CALLED IC IS THEN CALLED TO DETERMINE THE
*   INSTANTANEOUS CURRENT THAT IS FLOWING INTO THE CAPACITOR.  THIS
*   FUNCTION USES A 3 DIMENSIONAL NEWTON-RAPHSON ALGORITHM TO
*   DETERMINE THE VOLTAGES AND CURRENTS AT THE OTHER THREE NODES IN
*   THE CIRCUIT.  ONCE WE HAVE THE INSTANTANEOUS CURRENT, WE KNOW

```

THAT:

$$dV/dT = I/C \quad (2)$$

WITH THIS, A NUMERICAL ROUTINE IS USED TO FIND VC AT T=TAU. THIS ROUTINE IS A COMBINATION OF ROUTINES. THE TIME TAU IS ARBITRARILY DIVIDED INTO 16 INCREMENTS. VC IS DETERMINED AT THE FIRST FOUR INCREMENTS USING A RUNGE-KUTTA ROUTINE. AFTER FOUR POINTS HAVE BEEN FOUND, THE POINTS ARE TURNED OVER TO AN ADAMS-BASHFORTH/ADAMS-MOULTON PREDICTOR/CORRECTOR ALGORITHM. THIS THEN CALCULATES THE REMAINDER OF THE POINTS IN THE INTERVAL TAU. IT CAN BE SHOWN THAT THIS SET OF EQUATIONS WILL ALWAYS CONVERGE FOR ANY SET OF REAL VALUES. THE VARIABLES IN THE TWO FUNCTIONS ARE AS FOLLOWS:

TAU = NORMALIZED SAMPLING PERIOD WIDTH
 TSKEW = NORMALIZED TIMING DUE TO TAP PLACEMENT ERROR
 CAP = NORMALIZED CAPACITANCE IN 1/OHMS
 V = CHARGE VOLTAGE APPLIED TO THE RC NETWORK IN VOLTS
 DCSHIFT = DCSHIFT OF THE SAMPLING GATE IN mV
 VC = THE INITIAL VOLTAGE ON THE HOLD CAPACITOR
 R = BIAS RESISTOR THAT VCH IS BEING APPLIED THROUGH
 RS = PARALLEL INPUT IMPEDANCE OF THE SIGNAL SOURCE
 AND TERMINATION

ALL OF THE PARAMETERS ARE PASSED TO THE FUNCTION THROUGH THE COMMON BLOCK. THE ONLY PARAMETERS THAT ARE PASSED TO THE FUNCTION AS ARGUMENTS ARE T, TSKEW, DCSHIFT, AND VCAP RESPECTIVELY.

REFERENCES:

- (1) P. STARK, "INTRODUCTION TO NUMERICAL METHODS".
NEW YORK: THE MACMILLAN CO., 1970. PAGES 123-272.
- (2) E. KREYSZIG, "ADVANCED ENGINEERING MATHEMATICS".
NEW YORK: JOHN WILEY AND SONS, 1983. PAGES 830-842.

*START OF FUNCTION DEFINITIONS FOR SAMPLE

DOUBLE PRECISION FUNCTION IC(VI,VC)
 IMPLICIT DOUBLE PRECISION (A-Z)

*TYPE DEFINITIONS

*

INTEGER BITS

DOUBLE PRECISION GAMMA,IS,ERR,VI,VA,VB,VC,VD

DOUBLE PRECISION DA,DB,DD,JAC,SIGMA,AB,AC,BD,CD

DOUBLE PRECISION VT,R,RS,V,FA,FB,FD,ISR,ISRS

DOUBLE PRECISION FAA,FAB,FBA,FBB,FBD,FDB,FDD

DOUBLE PRECISION GISR,GISRS,CAP

DOUBLE PRECISION W,RADPHI,AMP,OFFSET,LREF,UREF,TAU

*

*declare common variables

COMMON W,RADPHI,AMP,OFFSET,BITS,LREF,UREF,TAU,CAP,R,RS,V,VT

*

*CONSTANTS

*

GAMMA = 1/.0259

IS = 1.0D-3/(DEXP(GAMMA*VT) -1.0)

ERR = 1.0D-10

ISR = IS*R

ISRS = IS*RS

GISR = GAMMA*ISR

GISRS = GAMMA*ISRS

*

*BEGIN

*

*decide which case the simulation falls into

IF (VI.GE.VC) THEN

*

*assign start points

VA = VC + VT

VB = (R*VI - RS*(V - VT))/(RS + 2.0*R)

VD = VB - VT

ELSE

*

*assign start points

VD = VC - VT

VB = (R*VI + RS*(V - VT))/(RS + 2.0*R)

VA = VB + VT

ENDIF

*

*perform iteration until DC operating point is solved

10 CONTINUE

*

*calculate the exponentials used throughout the solution

AB = DEXP(GAMMA*(VA - VB))

AC = DEXP(GAMMA*(VA - VC))

BD = DEXP(GAMMA*(VB - VD))

CD = DEXP(GAMMA*(VC - VD))

*

*calculate the values of the three current functions

*and their non zero partial derivatives with respect

*to each other

```

FA = ISR*(AC + AB - 2.0) + VA - V
FB = ISRS*(BD - AB) + 2.0*VB - VI
FD = ISR*(BD + CD - 2.0) - VD - V
FAA = GISR*(AC + AB) + 1.0
FAB = -GISR*AB
FBA = -GISRS*AB
FBB = GISRS*(BD + AB) + 2.0
FBD = -GISRS*BD
FDB = GISR*BD
FDD = -GISR*(BD + CD) - 1.0
*
*compute the Jacobian matrix of the partial derivatives
JAC = FAA*FBB*FDD - FAA*FBD*FDB - FAB*FBA*FDD
*
*halt if Jacobian is equal to zero
IF (JAC.EQ.0.000) THEN
    PRINT *, 'JACOBIAN EQUALS ZERO!!'
    STOP
ENDIF
*
*compute the cofactors
DA = (-FA*FBB*FDD + FA*FBD*FDB
      -FAB*FBD*FD + FAB*FB*FDD)/JAC
DB = (-FAA*FB*FDD + FAA*FBD*FD + FA*FBA*FDD)/JAC
DD = (-FAA*FBB*FD + FAA*FB*FDB
      +FA*FBA*FDB + FAB*FBA*FD)/JAC
*
*calculate the next guess at the answer
VA = VA + DA
VB = VB + DB
VD = VD + DD
*
*determine if the solution is close enough to the answer
SIGMA = DSQRT(DA*DA + DB*DB + DD*DD)
*
*branch if the error on the variables is too large
IF (SIGMA.GE.ERR) GOTO 10
*
*WRAP-UP AND RETURN
*
IC = IS*(DEXP(GAMMA*(VA - VC)) - DEXP(GAMMA*(VC - VD)))
RETURN
END
*
*
*
DOUBLE PRECISION FUNCTION VIN(T1)
IMPLICIT DOUBLE PRECISION (A-Z)
*
*TYPE DEFINITIONS
*
DOUBLE PRECISION OFFSET,AMP,W,RADPH1,T1

```



```

COMMON W,RADPHI,AMP,OFFSET
*
*determine the value of the input signal at end of aperature
*the amplitude is multiplied by two as there is a voltage divider
*at the input of the sampling gate consisting of Rs and Rs.
  VIN = 2.0*AMP*DSIN(W*T1 + RADPHI) + OFFSET
*
*WRAP-UP AND RETURN
*
  RETURN
  END
*
*
*
*****
*
*END OF FUNCTION DEFINITIONS FOR SAMPLE
*
*****
*
*
*
  DOUBLE PRECISION FUNCTION SAMPLE(T,DCSHIFT,TSKEW,VCAP,
  |                               GAIN)
  IMPLICIT DOUBLE PRECISION (A-Z)
*
*PARAMETER DEFINITIONS
*
  INTEGER NUMPTS
  PARAMETER(NUMPTS = 16)
*
*TYPE DEFINITIONS
*
  INTEGER J,J1,J2,J3,J4,T,BITS
  DOUBLE PRECISION CAP,DT,TP,VP,VI,TABS
  DOUBLE PRECISION K1,K2,K3,K4,K5
  DOUBLE PRECISION V(NUMPTS + 1),I(NUMPTS + 1)
  DOUBLE PRECISION OFFSET,AMP,W,RADPHI,LREF,UREF,VCAP
  DOUBLE PRECISION DCSHIFT,TSKEW,TAU,VIN,GAIN
  COMMON W,RADPHI,AMP,OFFSET,BITS,LREF,UREF,TAU,CAP
*
*INITIALIZATION
*
*calculate the time step width
  DT = TAU/NUMPTS
*
*calculate the absolute time
  TABS = T + TSKEW
*
*start the Runge-Kutta routine at zero time
  TP = 0.0
*

```

```

*save the starting capacitor voltage
  V(1) = VCAP
*
*find the starting input voltage
  VI = VIN(TP + TABS)*GAIN
*
*calculate the next three points via Runge-Kutta
*
*!!!NOTE!!!
*The FORTRAN matrices must start at 1, thus V(1)
*corresponds to voltage at time T=0, etc.
*
  DO 10, J = 1, 3
*
*find the current/capacitance (dV/dT) at this point
  I(J) = IC(VI,V(J))/CAP
*
*calculate the first Runge-Kutta weighting factor
  K1 = I(J)*DT
*
*increment the time point by half of the step size
  TP = TP + DT/2.0
*
*add half of the first RK weight to the capacitor voltage
  VP = V(J) + K1/2.0
*
*find the input voltage at this new point in time
  VI = VIN(TP + TABS)*GAIN
*
*calculate the second RK weight
  K2 = IC(VI,VP)*DT/CAP
*
*add half of the second RK weight to the capacitor voltage
  VP = V(J) + K2/2.0
*
*calculate the third RK weight (the point in time doesn't
*change: hence VI is still the same as well)
  K3 = IC(VI,VP)*DT/CAP
*
*increment the time point by half of the step size
*(the previous point was (J-1)*DT + DT/2)
  TP = J*DT
*
*add half of the third RK weight to the capacitor voltage
  VP = V(J) + K3
*
*find the input voltage at this new point in time
  VI = VIN(TP + TABS)*GAIN
*
*calculate the fourth RK weight
  K4 = IC(VI,VP)*DT/CAP
*

```

```

*calculate the next capacitor voltage, V
      V(J + 1) = V(J) + (K1 + 2.0*K2 + 2.0*K3 + K4)/6.0
10    CONTINUE
*
*calculate the current corresponding to V(4)
      I(4) = IC(VI,V(4))/CAP
*
*calculate the remaining points via the
*Adams-Bashforth/Adams-Moulton predictor/corrector method
      DO 20, J = 5, NUMPTS + 1
*
*initialize pointers
      J1 = J - 1
      J2 = J - 2
      J3 = J - 3
      J4 = J - 4
*
*predict the next voltage using the last four voltages
*via the Adams-Bashforth algorithm (J is pointing to
*the next voltage)
      VP = V(J1) + DT*(55.0*I(J1) - 59.0*I(J2)
        + 37.0*I(J3) - 9.0*I(J4))/24.0
*
*calculate the next point in time
      TP = TP + DT
*
*find the voltage at this point in time
      VI = VIN(TP + TABS)*GAIN
*
*calculate the first Adams-Moulton weighting factor
      K1 = IC(VI,VP)/CAP
*
*calculate the corrected voltage via Adams-Moulton
      V(J) = V(J1) + DT*(9.0*K1 + 19.0*I(J1)
        - 5.0*I(J2) + I(J3))/24.0
*
*find the current/capacitance (dV/dT) at this point
      I(J) = IC(VI,V(J))/CAP
20    CONTINUE
*
*WRAP-UP AND RETURN
*
*assign the answer to the function variable
      SAMPLE = V(NUMPTS + 1) + DCSHIFT
*
*return
      RETURN
      END
*
*
*****

```

```

*
* TITLE: A/D QUANTIZATION FUNCTION
* AUTHOR: PAUL LANGNER
* DATE: JUNE 16, 1988
* DESCRIPTION: THIS FUNCTION HAS SIX INPUTS: THE SAMPLED
*             VOLTAGE, V, THE NUMBER OF BITS OF QUANTIZATION,
*             BITS, THE LOWER REFERENCE LEVEL, LREF, THE UPPER
*             REFERENCE LEVEL, UREF, THE SKEW ON THE LOWER REFERENCE
*             LEVEL, LRSKEW, AND THE SKEW ON THE UPPER REFERENCE
*             LEVEL, URSKEW. THE ROUTINE RETURNS A NUMBER IN OFFSET
*             BINARY WITH 0 BEING AT THE SKEWED LOWER REFERENCE
*             LEVEL, AND ALL ONES BEING AT THE SKEWED UPPER REFERENCE
*             LEVEL.
*
* REFERENCE: F.G. STREMLER, "INTRODUCTION TO COMMUNICATION
*             SYSTEMS". READING, MASSACHUSETTS: ADDISON-WESLEY, 1982.
*             PAGE 510
*
*****
*
*
*
* INTEGER FUNCTION QUANTIZE(V,LRSKEW,URSKEW)
* IMPLICIT DOUBLE PRECISION (A-Z)
*
* TYPE DEFINITIONS
*
* DOUBLE PRECISION V,LRSKEW,URSKEW
* DOUBLE PRECISION W,RADPHI,AMP,OFFSET,LREF,UREF
* DOUBLE PRECISION VINC,SLREF,SUREF
* INTEGER BITS
* COMMON W,RADPHI,AMP,OFFSET,BITS,LREF,UREF
*
* calculate the skewed references
*   SLREF = LREF + LRSKEW
*   SUREF = UREF + URSKEW
* prepare for quantization
*   VINC = (SUREF - SLREF)/2**BITS
*
* quantize voltage
*   QUANTIZE = IDINT((V - SLREF)/VINC)
*   RETURN
*   END
*
*
*
*****
*
* TITLE: D/A FUNCTION
* AUTHOR: PAUL LANGNER
* DATE: FEBRUARY 6, 1989
* DESCRIPTION: THIS FUNCTION HAS FOUR INPUTS: THE BINARY WORD

```

```

*      TO BE INPUT TO THE D/A. Q. THE NUMBER OF BITS OF
*      QUANTIZATION, BITS. THE LOWER REFERENCE LEVEL, LREF.
*      AND THE UPPER REFERENCE LEVEL, UREF. THE ROUTINE
*      RETURNS A VOLTAGE CORRESPONDING TO NUMBER BIN. WHICH IS
*      IN OFFSET BINARY WITH 0 BEING AT THE LOWER REFERENCE
*      LEVEL, AND ALL ONES BEING AT THE UPPER REFERENCE LEVEL.
*      ALL OF THE PARAMETERS ARE PASSED USING THE COMMON BLOCK
*      EXCEPT FOR THE BINARY NUMBER. D.

```

```

*      REFERENCE: F.G. STREMLER. INTRODUCTION TO COMMUNICATION
*      SYSTEMS. READING, MASSACHUSETTS: ADDISON-WESLEY, 1982.
*      PAGE 510

```

```

*****

```

```

*
*
*

```

```

      DOUBLE PRECISION FUNCTION DTOA(D)
      IMPLICIT DOUBLE PRECISION (A-Z)

```

```

*
*TYPE DEFINITIONS

```

```

      DOUBLE PRECISION W,RADPHI,AMP,OFFSET,LREF,UREF
      DOUBLE PRECISION VINC
      INTEGER BITS,D
      COMMON W,RADPHI,AMP,OFFSET,BITS,LREF,UREF

```

```

*

```

```

*prepare for D/A
      VINC = (UREF - LREF)/2**BITS

```

```

*

```

```

*offset and scale binary number so that the number is real and
*lies between the upper and lower reference levels and is
*centered about zero

```

```

      DTOA = D*VINC + LREF + VINC/2.0
      RETURN
      END

```

```

*
*
*

```

```

*****

```

```

*END OF FUNCTION DEFINITIONS

```

```

*

```

```

*****

```

APPENDIX D

D.1 Key Component Data Sheets

In this section, a collection of the data sheets of all of the key components used to construct the parallel sampling system is given.

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2005/EL2005C

High Accuracy Fast Buffer

Features

- Low input current — 50 pA
- Low offset & drift — 2 mV/25 μ V/°C
- High slew rate — 1500 V/ μ s
- Fast rise & fall time — 2.5 ns
- High input resistance — 1000 G Ω
- Bandwidth — 140 MHz
- Pin compatible with ELH0033
- MIL-STD-883 Revision C devices manufactured in U.S.A.

Advantages

- No input loading
- Input current independent of input voltage
- Eliminates offset adjustments
- Drives cables directly

Ordering Information

Part No.	Temp. Range	Pin	Outline
EL2005C	-25 to +85°C	TO-8	MDF0002
EL2005C/8+	-25 to +85°C	TO-8	MDF0002
EL2005C	-55 to +125°C	TO-8	MDF0002
EL2005C/883B	-55 to +125°C	TO-8	MDF0002

General Description

The EL2005 is a high-speed, FET input buffer similar to ELH0033 and EL2004 but with input specifications significantly improved over the previous types. The input stage employs a cascode configuration to maintain constant input characteristics over the full ± 10 V input range. The input looks like a 3 pF capacitor to ground in almost all cases since the DC bias current is constant with input voltage. In sample and hold circuits this results in an order of magnitude improvement in hold characteristics. Input offset voltage and offset voltage drift are also improved a factor of two over previous types.

These excellent DC characteristics are complemented by a wide 140 MHz bandwidth while the 1500 V/ μ s slew rate and excellent phase linearity of the ELH0033 family are preserved allowing direct plug-in replacement for upgraded performance. (For even faster operation see EL2004).

The EL2005 is specified for operation over the -55°C to +125°C military temperature range. The EL2005C is specified for operation over the -25°C to +85°C temperature range. Available packages include the TO-8 metal can, and Leadless Chip Carriers (LCCs) by special order.

Elantec facilities comply with MIL-I-45208A and are MIL-STD-1772 certified. Elantec's Military devices comply with MIL-STD-883B Revision C and are manufactured in our rigidly controlled, ultra-clean facilities in Milpitas, California. For additional information on Elantec's Quality and Reliability Assurance Policy and procedures request brochure QRA-1.

Connection Diagram

Simplified Schematic

EL2005/EL2005C

High Accuracy Fast Buffer

Absolute Maximum Ratings (25°C)

V_S	Supply Voltage ($V^+ - V^-$)	40 V	T_A	Operating Temperature Range:	
V_{IN}	Input Voltage	40 V		EL2005	-55°C to +125°C
P_D	Power Dissipation (See curves)	1.5 W		EL2005C	-25°C to +85°C
I_{OC}	Continuous Output Current	±100 mA	T_J	Operating Junction Temperature	175°C
I_{CP}	Peak Output Current	±250 mA	T_{ST}	Storage Temperature	-65°C to +150°C
				Lead Temperature	
				(soldering, 10 seconds)	300°C

Important Note: All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Elantec performs most electrical tests using modern high speed automatic test equipment, specifically the LTX 77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level Test Procedure

- I 100% production tested and QA sample tested per QA test plan QCX0002
- II 100% production tested at $T_A = 25^\circ\text{C}$, and QA sample tested at $T_A = 25^\circ\text{C}$, T_{MAX} and T_{MIN} per QA test plan QCX0002
- III QA sample tested per QA test plan QCX0002
- IV Parameter is guaranteed (but not tested) by Design and Characterization Data
- V Parameter is typical value for information purposes only

DC Electrical Characteristics $V_S = \pm 15\text{V}$, $V_{IN} = 0\text{V}$, $T_{MIN} \leq T_A \leq T_{MAX}$

Parameter	Test Conditions	EL2005				EL2005C				Units
		Min.	Typ.	Max.	Test Level	Min.	Typ.	Max.	Test Level	
V_{OS} Output Offset Voltage	$R_S = 100\text{ k}\Omega$, $T_J = 25^\circ\text{C}$ (Note 1)	2	5	1		3	10	1		mV
	$R_S \leq 100\text{ k}\Omega$			10	I			15	III	mV
$\Delta V_{OS}/\Delta T$ Average Temperature Coefficient of Offset Voltage	$R_S = 100\Omega$	25		V		25		V		$\mu\text{V}/^\circ\text{C}$
PSRR Supply Rejection	$\pm 10\text{V} \leq V_S \leq \pm 20\text{V}$	65	75		I	60	75		II	dB
I_B Input Bias Current	$T_J = 25^\circ\text{C}$ (Notes 1 and 3)	2	50	1		5	100	1		pA
	$T_A = 25^\circ\text{C}$ (Notes 2 and 3)	50	500	IV		100	1000	IV		pA
	$T_J = T_A = T_{MAX}$	2	5	1		0.5	5	III		nA
A_V Voltage Gain	$R_S = 100\Omega$, $R_L = 1\text{ k}\Omega$, $V_{IN} = \pm 10\text{V}$	0.97	0.98	1.00	I	0.96	0.98	1.00	II	V/V
	$R_S = 100\Omega$, $R_L = 100\Omega$, $V_{IN} = \pm 10\text{V}$	0.88	0.95	0.98	I	0.88	0.95	0.99	II	V/V
R_{IN} Input Impedance	$R_L = 1\text{ k}\Omega$, $-10\text{V} \leq V_{IN} \leq \pm 10\text{V}$	2×10^9	10^{12}		I	2×10^9	10^{12}		IV	Ω
	$T_J = 25^\circ\text{C}$ (Note 1), $R_L = 1\text{ k}\Omega$	10^{10}	10^{12}		I	10^{10}	10^{12}		I	Ω
R_O Output Impedance	$R_L = 1\text{ k}\Omega$, $V_{IN} = \pm 1\text{V}$	4	8	1		4	9	II		Ω
V_O Output Voltage Swing	$V_{IN} = \pm 14\text{V}$, $R_L = 1\text{ k}\Omega$	±12	±12.5		I	±12	±12.5		II	V
	$V_{IN} = \pm 10.5\text{V}$, $R_L = 100\Omega$, $T_A = 25^\circ\text{C}$	±9	±9.8		I	±9	±9.8		I	V
I_S Supply Current		19	22	1		19	24	II		mA
Power Consumption		570	660	1		570	720	II		mW

(See Notes on next page)

EL2005/EL2005C

High Accuracy Fast Buffer

AC Electrical Characteristics $T_C=25^\circ\text{C}$, $V_S=\pm 15\text{V}$, $R_S=50\Omega$, $R_L=1\text{k}\Omega$

Parameter	Test Conditions	EL2005				EL2005C				Units
		Min.	Typ.	Max.	Test Level	Min.	Typ.	Max.	Test Level	
S_R Slew Rate	$V_{IN}=\pm 10\text{V}$, $V_{OUT}=\pm 5\text{V}$	1000	1500		III	1000	1500		III	$\text{V}/\mu\text{s}$
BW Bandwidth	$V_{IN}=1\text{V}_{\text{rms}}$		140		V		140		V	MHz
Phase Non-Linearity	BW=1 to 20 MHz		2		V		2		V	Degree
t_r Rise Time	$\Delta V_{IN}=0.5\text{V}$		2.5		V		2.5		V	ns
t_p Propagation Delay	$\Delta V_{IN}=0.5\text{V}$		10		V		10		V	ns
HD Harmonic Distortion	$f>1\text{kHz}$		<0.1		V		<0.1		V	%
A_v Voltage Gain	$R_S=100\Omega$, $V_{IN}=1\text{V}_{\text{rms}}$, $f=1\text{kHz}$	0.97	0.99	1.00	I	0.96	0.99	1.00	II	V/V
R_O Output Impedance	$V_{IN}=1\text{V}_{\text{rms}}$, $f=1\text{kHz}$		4	8	I		4	9	II	Ω

Note 1: Specification is at 25°C junction temperature due to requirements of high-speed automatic testing. Actual values at operating temperatures will exceed the value at $T_J=25^\circ\text{C}$. When supply voltages are $\pm 15\text{V}$, no-load operating junction temperatures may rise 40°C to 80°C above ambient and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_Q will change significantly during warm-up. Refer to I_Q vs. Temperature graph for expected values.

Note 2: Measured in still air seven minutes after application of power

Note 3: Input bias current is guaranteed over the input range of $-10\text{V} < V_{IN} < +10\text{V}$

Typical Performance Curves

EL2005/EL2005C

High Accuracy Fast Buffer

Typical Performance Curves—Continued

Typical Applications

APPLICATIONS

The GC3200 series of harmonic generator varactors uses a single epitaxial silicon die. Strict material and process controls result in high reproducibility. A unique silicon dioxide passivation process assures greater stability, reliability and low leakage currents at high temperatures.

This series of diodes is available in a wide selection of capacitance values, breakdown voltages, transition times and cutoff frequencies for optimum circuit design. These devices have the best efficiencies and thermal dissipation available in single chip multiplier varactors.

The GC3200 series multiplier varactors can be used for all orders of multiplication from X2 through X20. They are used primarily in low harmonic order, high efficiency, high power applications. They are used in narrow and wide bandwidth frequency generator chains for all multiplication stages. Other applications include voltage controlled oscillators, frequency synthesizers and up converters.

ELECTRICAL SPECIFICATIONS

 $T_A = 25^\circ\text{C}$

MODEL NUMBER	TYP OUTPUT FREQ RANGE (GHz)	TYP OUTPUT POWER		JUNCT CAPACITANCE ¹ (AT -6V, 1 MHz) C _J (pF)	MINIMUM BREAKDOWN VOLTAGE (AT 10 μ A MAX) V _B (V)	MINIMUM ² CUTOFF FREQ (AT -6V) F _C (GHz)	MINIMUM ³ CARRIER LIFETIME (I _R = 6 mA, I _F = 10 mA) T _L (ns)	MAXIMUM ⁴ TRANSITION TIME T _T (ps)	MAXIMUM THERMAL RESISTANCE θ_{JC} °C/W
		W	MULT						
GC 3202	0.15 - 0.50	24.0	X3	18 - 25	180	20	8000		5
GC 3203	0.5 - 1.2	20.0	X3	8 - 12	80	60	200	1000	11
GC 3204	1.2 - 2.5	6.0	X4	3 - 6	60	110	200	650	20
GC 3205	2.5 - 5.0	2.5	X5	1.5 - 3.0	45	140	70	300	30
GC 3206	5.0 - 8.0	1.5	X2	1 - 2	40	150	35	150	40
GC 3207	8.0 - 12.0	1.0	X2	0.5 - 1.0	35	175	30	120	50
GC 3208	12.0 - 18.0	0.5	X2	0.3 - 0.6	25	200	15	100	75

NOTES

NOTES
1 JUNCTION CAPACITANCE IS MEASURED AT 1 MHz.

2 CUTOFF FREQUENCY IS CALCULATED FROM $f_{c0} = \frac{159}{C_1 R_{S6}}$

3 CARRIER LIFETIME IS MEASURED USING TEST CIRCUIT SHOWN IN FIGURE 1

4. TRANSITION TIME (SNAP TIME) IS MEASURED USING TEST CIRCUIT SHOWN IN FIGURE 2

5. THERMAL RESISTANCE IS MEASURED USING PULSED CONDITIONS WHILE MEASURING FORWARD VOLTAGE DROP ACROSS THE DIODE MOUNTED IN AN INFINITE HEAT SINK

Unless otherwise specified, capacitance will be within the range shown for each type. A capacitance tolerance of $\pm 10\%$ is available at an additional charge. Diodes can be optimized for custom electrical or mechanical specifications. Custom parameters for capacitance, voltage, transition time, cutoff frequency, etc. are available upon request.

All specifications shown above are based on the style 30 package, except for GC3202 and GC3203, which are based on the style 20 package. These latter two devices are available only in case styles 20, 25 or 55 due to dice size.

A complete list of case styles available along with dimensions and package parasitics are shown at the rear of this catalog. The cathode is the heat sink end of each package.

Diode chips, alone or mounted on carriers with gold wire ribbon leads, are also available.

Operating and Storage Temperature -65°C to +200°C

RO2800 Laminate Data Sheet

RO2800 Laminates for Digital Applications

RO2800™ low ϵ_r circuit laminates are fluoropolymer composite printed wiring board (PWB) materials for high speed digital applications. RO2800 PWB materials solve both electrical and mechanical problems associated with high speed digital systems.

By combining a low dielectric constant and low dissipation factor, RO2800 offers improved electrical performance over other PWB materials. The result—short propagation delays, low cross-talk levels and low degradation of rise time—makes RO2800 ideally suited for applications involving high speed ECL or GaAs.

The Z-direction Coefficient of Thermal Expansion (CTE) of RO2800 is the closest match of any available PWB material to that of copper, enabling plated thru-holes to survive thermal cycling and thermal shock. A low modulus and XY-directions coefficient of thermal expansion afford reliable surface mounting of even high I/O leadless ceramic chip carriers.

RO2800 is one of the new ROHSI™ family of materials and products from Rogers (ROHSI is an acronym for

Rogers High Speed Interconnections). For additional information about RO2800 or any of the other ROHSI products call a member of the ROHSI team at 800 528-8246.

Processing Features

- RO2800 multilayer boards are processed conventionally, except for lamination temperature and drilled-hole preparation prior to electroless plating.
- High temperature fusion bonding with RO2800 bondply results in a homogeneous construction and very low Z-axis CTE.
- Biaxial dimensional change combined with 4-slot tooling and high temperature fusion bonding result in excellent layer-to-layer registration.

RO2800 laminates have Underwriters Laboratories* recognition under classification 94V-0 (Vertical Flammability Test).

Table 1 RO2800 Features and Benefits

Product Features	Benefits	Comments/References
Low dielectric constant (DK)	Reduction in propagation delay Reduction in crosstalk at given impedance and line width/spacing	25% less than polyimide glass, 30% less than epoxy glass 60% less than polyimide glass and 63% less than epoxy glass at 5 mil spaces. See Figure 1.
Low dissipation factor (DF), even at high frequencies.	Reduction in rise time degradation Low dielectric loss	Dissipation factor of .0012 through 10 GHz 40% less than polyimide glass, 55% less than epoxy glass. See Figure 2. Dielectric attenuation less than 0.1 dB per inch at 10 GHz.
Coefficient of thermal expansion (CTE) in Z-direction is a close match to copper	Excellent plated thru-hole reliability	Typ. aspect ratio plated thru-holes subjected to MIL-P-55110 thermal shock and thermal cycling without failure.
Combination of low modulus and X-Y-direction coefficient of thermal expansion (CTE)	Affords surface mount reliability	Preliminary thermal cycling test results are available on request.

Table 2 Selected Properties of PWB Materials

PWB Material	Dielectric Constant	Dissipation Factor	CTE ² (PPM/°C)		Tensile Modulus ⁴ (MPSI)
			X-Y Axis	Z Axis	
PTFE	2.1 ¹	0.0004 ¹	224	224	0.05
PTFE/Microfiber	2.2 ¹	0.0008 ¹	24	261	0.14
RO2800	2.9 ¹	0.0012 ¹	16	24	0.12
Polyimide/Quartz	3.35 ¹	0.005 ¹	6-8	34	---
Polyimide/KEVLAR	3.6 ¹	0.008 ¹	3.4-6.7	83	4.0
Polyimide/Glass	4.5 ¹	0.010 ¹	11.7-14.2	60	2.8
Epoxy/Glass	4.8 ¹	0.022 ¹	12.8-16	189	2.5

¹measured at room temperature ²measured from 0 to +125°C ³measured at 1 MHz ⁴measured at 10 GHz

Rogers Corporation
ROHSI Products Department
Box 790 Chandler AZ 85244
800 528 8246

Table 3 RO2800
Laminate Data

Property	Test Method	Condition	Units (1)	Direction	Typical Value
Dielectric Constant	ASTM D3380	10 GHz, 23°C		Z	2.9
Dissipation Factor	ASTM D3380	10 GHz, 23°C		Z	0.0012 typ 0.0016 max
Volume Resistivity	ASTM D257	A	ohm-cm	Z	10
Surface Resistivity	ASTM D257	A	ohm	X Y	10
Dimensional Stability	IPC-TM-650	After etch + E-1, 150°C	%	X Y	0.05
Tensile Modulus	ASTM D638	A, 23°C	MPa (Kpsi)	X Y	828 (120)
Ultimate Stress	ASTM D638	A, 23°C	MPa (Kpsi)	X Y	6.9 (1.0)
Ultimate Strain	ASTM D638	A, 23°C	%	X Y	7.3
Copper Peel Strength	MIL-P-13949	After 260°C Solder Float	Kg/m (lbs./in.)	---	89 (5)
Water Absorption	ASTM D570	D 48/50	%	---	0.13 max
Thermal Conductivity	Rogers TR 2721	100°C	W/m·K (BTU/in ft·hr/°F)	Z	0.44 (3.0)
Specific Heat	Calculated	100°C	J/g·K (BTU/lb·°F)	Z	0.93 (0.22)
Coefficient of Thermal Expansion	ASTM D3386	10 K/min	(parts/part)·°C	X Y	16 · 10 ⁻⁶
Coefficient of Thermal Expansion	ASTM D3386	10 K/min	(parts/part)·°C	Z	24 · 10 ⁻⁶
Specific Gravity	ASTM D792	23°C			2.1

(1) SI units given first with other frequently used units in parenthesis

Fig. 1 Backward Crosstalk
vs. Line Spacing

Fig. 2 Substrate Effect on
Rise-Time Degradation

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