10 GHz LC VCOs For High-Speed Serial Data Communication ICs

by

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Abstract

As both wireless and optical communications systems move towards high-data-rate applications, high-frequency low-phase-noise oscillators are important building blocks in the transmit and receive channels. With scaling, CMOS technology proves to be a viable option for designing low power and low cost front-end circuitry for high-speed optical communication systems.

This thesis presents the design methodology and implementation of monolithic GHz range voltage controlled oscillators for high-speed serial data communication ICs in submicron CMOS technology. The design methodology illustrated, provides an efficient and practical approach by using a simulator-based design strategy with appropriate reference to the existing VCO noise model and theory. There are three LC VCO presented in this thesis. The first ($f_0=2\text{GHz}$) and the second ($f_0=10\text{GHz}$) oscillators use a complementary negative transconductance topology while the third oscillator ($f_0=10\text{GHz}$) works on self-switched inductor concept. On-chip broadband and high Q inductors are designed and optimized using dedicated software and 2.5D electromagnetic simulator. The design of PN-junction based and an “accumulation-mode” MOS tuning varactors are presented. Practical issues pertaining to CMOS LC VCO design, layout and testing are also discussed. The characterization of the VCO and the integrated passive components are presented. Best performance is achieved for the second VCO with phase noise of -100dBc/Hz at 1MHz offset from a center frequency of 10.24GHz . The tuning range is 860MHz . The circuit consumes 2.4mA from a 1.2V supply and has met the SONET OC192 jitter / phase noise requirement with fair

margin of 10dBc. The comparison of designed LC VCOs with the recent literature shows significant improvement with respect to phase noise and power consumption. Finally, several recommendations for further improvement in VCO performance and issues need to be addressed in future work are discussed.

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LIST OF ABBREVIATIONS

AC	Alternating Current
ADC	Analog to Digital Converter
ADS	Advance Design System
AM	Amplitude Modulation
C	Capacitor
CAD	Computer Aided Design
CICC	Custom IC Conference
CMOS	Complementary MOS
CDR	Clock and Data Recovery
CML	Current Mode Logic
CMU	Clock Multiplier Unit
DC	Direct Current
DFF	D type Flip-Flop
DUT	Device Under Test
FFT	Fast Fourier Transformation
FM	Frequency Modulation
FOM	Figure of Merit
FPGA	Field Programmable Gate Array
HSPICE	High speed Simulation Programming with IC Emphasis
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
ISF	Impulse Sensitivity Function
ISI	Inter Symbol Interference

L	represent inductance
LAN	Local Area Network
LNA	Low Noise Amplifier
LTi	Linear Time Invariant
LTV	Linear Time Variant
MIM	Metal-insulator-Metal
MOS	Metal Oxide Semiconductor
NRZ	Non Return to Zero
OC	Optical Channel
PD	Phase Detector
PFD	Phase Frequency Detector
PLD	Programmable Logic Device
PLL	Phase-Locked Loop
RF	Radio Frequency
SDH	Synchronous digital hierarchy
SERDES	Serializer / Deserializer
SONET	Synchronous Optical NETwork
SPDV	Single Poly Dual Voltage
STM	Synchronous Transport Module
UI	Unit Interval
VCO	Voltage Controlled Oscillator
VLSI	Very Large Scale Integration
WAN	Wide Area Network
WDM	Wavelength Division Multiplexing

1 Introduction

1.1 Motivation

With the growing demands for faster data rates of LANs (Local Area Networks) and SONET (Synchronous Optical Network), gigabit ethernet and high-speed optic fiber networks are becoming more popular because of their high throughputs. Paralleling this demand is a booming market for high data rate transceivers.

SONET and SDH (synchronous digital hierarchy) are the most widely used optical wide area networks (WAN) for today's long-distance telephone service and the Internet backbone. To meet the increasing demand for bandwidth, optical communication systems have been consistently upgraded to higher speeds through a combination of increasing line rates (TDM - time division multiplexing) and transmitting multiple wavelengths in a single fiber (WDM - wavelength division multiplexing). OC-192/STM-64 (10Gbit/s) networks are starting to be deployed and OC-768/STM-256 is on the horizon. Table 1-1 outlines the SONET/SDH signal hierarchies and data rates.

The building of networks to handle voice, data, and Internet Protocol (IP) traffic has created a large need for integrated circuits (ICs) that can transmit and receive large amounts of information at serial data rate as given in Table 1-1. Existing applications require the transmission and reception of point-to-point non-return-to-zero (NRZ) data for a few tens of centimeters on a printed circuit board or backplane for chip-to-chip communications or up

to hundreds of kilometers over fiber for long-haul transport of SONET frames. Longer distance mean tighter jitter specs, which mean more expensive components and more difficult to design [1]. Ethernet is the most widely used local area networks (LAN) and has been continuously evolving to handle ever-higher network speeds.

Table 1-1. SONET/SDH signal hierarchies

SONET Signal	SDH Signal	Bit Rate (Mbit/s)
STS-1, OC-1	STM-0	51.840
STS-3, OC-3	STM-1	155.520
STS-12, OC-12	STM-4	622.080
STS-48, OC-48	STM-16	2488.320
STS-192, OC-192	STM-64	9953.280
STS-768, OC-768	STM-256	39813.12

With the IEEE P802.3ae [2] 10 Gigabit Ethernet (10GbE) standard being released, LAN and WAN will converge at 10Gbit/s and merge into metro area networks (MAN). The transmission of information requires serialization of data bits with precise timing control and with stringent timing recovery. These applications thus necessitate the use of precision oscillators and clock/data recovery (CDR) circuits [3]. Therefore, serializer / deserializer (SERDES) physical layer devices are becoming an important function for high-speed serial data communications.

Any physical layer device at 10GHz will need to address the SONET/SDH jitter specification [4, 5]. An excessive amount of jitter and wander induced in the SONET/SDH synchronous network will cause degradation in transmission quality, bit errors, and data loss. Phase-locked loops (PLLs) typically used for clock recovery are sensitive to jitter (phase variation at a rate $\geq 10\text{Hz}$). The standard specifies three types of jitter related

requirements: jitter generation, jitter tolerance and jitter transfer. These jitter types will be discussed in detail in Chapter 2.

A 10G SERDES must perform the physical layer serializer/deserializer functions while operating at 9.953 Gbit/s (OC-192/STM-64/10GbE WAN PHY applications), 10.3125 Gbit/s (10GbE LAN PHY applications), or 10.709 Gbit/s (G.709 applications). A typical implementation to realize these functions is shown in block form in Figure 1-1

Figure 1-1. A generic architecture of high speed SERDES

The transmitter path / serializer, consists of a clock multiplier unit (CMU), a parallel-in-serial-out unit (PISO) and an output buffer (Tx), while the receiver path / deserializer, consists of an input buffer (Rx), a clock recovery unit (CRU) and a serial-in-parallel-out unit (SIPO).

Although wireless communication, or radio frequency ICs (RFIC), and wired communication ICs (SERDES) share some common building blocks such as a VCO and an ADC, there

are unique performance requirements that make SERDES design quite different from RFIC design. From a bandwidth requirement, RFIC circuits are narrowband while SERDES circuits are broadband. The high demand on bandwidth often pushes SERDES circuits into working close to the technology speed limit.

1.2 Thesis Objective

Significant eye closure and stringent SONET/SDH jitter requirements make clock and data recovery (CDR) a challenging task that requires thoughtful design of CDR building blocks. More so, a high-speed low jitter clock is required to perform the serialization in the CMU / transmit channel. Voltage Controlled Oscillator (VCO) is a critical building block in both the CMU of the serializer and the CDR on the receive side. The inherent jitter, or equivalently phase noise, of the VCO in the PLL is the fundamental limitation to performance in the transmitter or receiver, so its design is critical. The VCO phase noise performance determines the overall phase noise / jitter performance and the loop bandwidth trade-off. Here, low phase noise and large tuning range are the two main design objectives.

In this thesis, the Author has undertaken to research and develop 10GHz VCO that serves the above design objectives to meet difficult SONET jitter specification for OC-192 system, in standard sub-micron CMOS technology.

1.3 Thesis Outline

Chapter 2 of this thesis will give an overview of the design challenges of high speed SERDES with study of available topology options with respect to two of the most critical blocks in high speed PLL that is voltage-controlled oscillator and phase/frequency detector.

Chapter 3 will discuss the fundamentals of LC tank VCO. Chapter 4 will describe the design methodology of passive components. Chapter 5 will review the existing phase noise models, VCO critical design considerations and the design/implementation of three LC tank VCOs. Chapter 6 will present the measurement results and correlation to simulation results. Chapter 7 will summarize the thesis with recommendations to further improve the VCO design and things need to be done as future work.

2 Design Challenges of High-Speed SERDES

2.1 Introduction

This chapter describes the challenges in the design of CDR and CMU circuits used in high-speed SERDES. Both CDR and CMU are critical phase-locked loop (PLL) functions in high-speed transceivers. Such transceivers serve in many applications, including optical communications, backplane routing and chip-to-chip interconnects. Operation at 10G and 40G frequency is typically the realm of expensive SiGe, GaAs [6] or InP technologies due to their fundamental device competence (high mobility and transconductance). However, mainstream CMOS technology has competitive advantages in terms of cost, level of integration and performance as the technology scaling enables both increased functionality and speed (frequency) of chips [7-10]. With scaling, CMOS technology proves to be a viable option for designing front-end circuitry for high-speed optical communication systems [11].

Phase-locked loops (PLL) can be used to maintain a well define phase, and hence frequency, relation between two independent signal sources. Due to their versatility, PLLs are usually preferred over other methods of maintaining phase lock, such as injection locking [12]. Monolithic phase-locked loops have been used for clock-and-data recovery (CDR) in data communication systems [13], clock generation and distribution in micro-

processors [14], and frequency synthesis in wireless applications [15].

Frequency synthesizers, also called a clock multiplier unit, CMU, are used in Radio Frequency (RF) transceivers and applications requiring multiplication of periodic signals. It provides precise definition of the output frequency and is one of the challenging tasks in RF systems as it must meet very stringent requirements. The oscillators used in RF transceivers are usually embedded in a synthesizer environment so as to achieve a precise definition of the output frequency.

The phase-locked loop plays an important role in keeping parts of our world orderly.

2.2 CMOS Scaling

The speed of electronic circuit is limited mainly by the cut-off frequency of transistors. Typically, the current gain cut-off frequency, f_T , and the maximum oscillation frequency, f_{max} , are commonly used figure-of-merits of an IC technology. The f_T is a good indicator of the switching speed of logic circuits while the f_{max} is a good measure of analog circuits. In order to choose a proper IC technology to provide fast enough switching speed and proper system margins, a transistor technology with f_T and f_{max} better than four times of the bit rate is preferred to implement high speed ASICs [16]. Deep sub-micron CMOS technology, now-a-days, is providing f_T of greater than 65 GHz. Since CMOS technology offers higher level of integration and lower cost over the exotic technologies e.g. GaAs, INP, SiGe. Low supply voltage (less than 1.8V), however, makes design of the analog front-end very challenging.

2.3 Design Issues of High-Speed SERDES

2.3.1 Jitter Requirements

To preserve data integrity, rigorous jitter characteristics are required by SONET specifications [17]. The Bellcore jitter requirements center around the amplitude, rise and fall time, jitter, and bit timing of the clock and data signals on the line interfaces. Timing jitter is the short-term variation of a digital signal's significant instant from the signal's ideal positions in time. [10].

SONET has three jitter specifications: jitter tolerance, jitter generation, and jitter transfer. To be considered Bellcore compliant, any piece of SONET equipment must meet all three specifications.

Jitter tolerance (also known as jitter accommodation) is the maximum amplitude of sinusoidal jitter at a given jitter frequency. This measurement identifies how much jitter a deserializer / CDR path can accept and still recover data within the bit error ratio (BER) limits of the link. On the receiver side, the jitter tolerance must have a sufficient margin above the SONET mask which covers a wide frequency range from 10Hz to 80MHz [4].

Jitter generation is the amount of jitter that a serializer can add to a data stream, assuming a stable reference clock. On the transmitter side, the maximum allowable jitter generation is $0.1 U_{Ipp}$ (unit interval, peak-to-peak) over a bandwidth of 50KHz - 80MHz [5]. At OC-192, with its 100-picoseconds (ps) cycle time, the overall system must generate less than 10 ps of jitter, which means, timing in the transceivers must be extremely accurate.

Jitter transfer is the specification that describes how the spectral characteristics of jitter are modified as a signal passes through the equipment. It is defined as the ratio of the output

jitter of a network element to the applied input jitter, as a function of jitter frequency, expressed in decibels. This transfer function, $H(f)$, is given by:

$$H(f) = 20 \cdot \log_{10} \left[\frac{\text{Output_jitter}(f)}{\text{Input_jitter}(f)} \right] \quad \text{Eq(2.1)}$$

2.3.2 Eye Opening

When an analog signal is transmitted through an optical link, signal degradation occurs due to attenuation, dispersion and non-linearity of the link. To correctly recover the digital information being transmitted from the received degraded signal, a receiver needs to perform reshaping, retiming and regeneration (3R) functions. Reshaping and regeneration restore the integrity of the signal, while retiming ensures that the potential impact of jitter is minimized. The overall system performance depends on the received signal quality, the sensitivity of the optical receiver, and the jitter tolerance of clock and data recovery circuit.

Figure 2-1, below shows the Eye opening which determines probability of bit errors.

Figure 2-1. Eye mask

The traditional eye diagram intuitively illustrates a signal's quality, such as its rise and fall times, its overshoots and undershoots, and its ringing, noise and jitter. This is shown in above Figure. A wider vertical opening indicates more tolerance to noise, while a wider horizontal opening indicates more tolerance to jitter. To maximize performance, a receiver must decide whether a received bit is high or low at the optimum decision point, which is normally halfway between edge crossings and halfway between high and low signal levels. The wider the opening, the more tolerance the system will have to variations in the decision threshold or the timing of the recovered clock. The eye mask specifies a minimum requirement on eye opening to ensure a certain BER performance.

2.4 CDR / CMU Building Blocks:

In addition to high speed, the properties of random non-return-to-zero (NRZ) data, jitter requirement and loop bandwidth specifications of optical standards create many design and simulation issues at both circuit and architecture levels. Significant eye closure and stringent SONET/SDH jitter requirements make CDR and CMU, a challenging task, that requires thoughtful design of the building blocks.

Figure 2-2 illustrates a generic CDR architecture, where a voltage-controlled oscillator (VCO) is phase-locked to the input data by means of a phase detector (PD) and a low-pass filter (LPF). The recovered clock generated by the VCO then samples and retimes the data, thereby reducing the jitter and ISI and providing timing coherency with subsequent operations.

Figure 2-2. Generic CDR circuit [18]

In the following sections two of the most critical blocks of high speed SERDES that is VCO and phase / frequency detector are discussed.

2.4.1 VCO

The Voltage Controlled Oscillator (VCO) is one of the key building blocks for the clock recovery PLL, which determines the overall phase noise (jitter) performance and the loop bandwidth trade-off. Here, low phase noise and large tuning range are the two main design objectives.

2.4.1.1 Oscillator Classification

Oscillators come in a variety of different types. Two major classifications for the oscillators are based on the output waveform that is sinusoidal output and non-sinusoidal output (square or triangular wave output). Figure 2-3 shows tree formation of oscillators as classified. Sinusoidal-output oscillators employ a positive feedback loop consisting of an amplifier and a frequency-selective resonator, such as cavity, crystal or LC tank. The

amplitude of the generated sine wave is limited, or set, using a nonlinear mechanism, implemented either with a separate circuit or using the nonlinearities of the amplifying device itself [19]. Circuits that generate square, triangular, pulse waveforms are called non-sinusoidal output oscillators. They usually require only one type of energy storage element (e.g. capacitor), and rely on the threshold switching characteristics of the circuit rather than on a frequency-selective element to define an oscillatory waveform.

Figure 2-3. Classification of oscillators.

2.4.2 Choice of Oscillator

For a monolithic implementation in several Giga Hertz range, there are two main types of oscillators that can be used: a ring oscillator, using several delay stages, and a LC oscillator,

using an inductor and varactor. Ring-oscillator-based VCOs generally exhibit higher jitter than LC resonators because there are no high Q circuits to attenuate the thermal and flicker noise of the transistors. In contrast, LC-based oscillators have better jitter performance that improves with increasing resonator Q. LC oscillators have high Q factor by the nature of its design: a good quality inductor and a minimal number of active components. LC oscillators have a Q factor that is typically four times the Q factor of a relaxation oscillator [20].

2.4.2.1 Ring Oscillator

Ring oscillators have been popular in all-digital phase-locked loops due to their simplicity and ease of integration with other digital circuits. As technology scaling continues to drive faster, higher performance, digital circuits, ring oscillators also benefit and begin to become a viable choice for frequencies needed for wireless and high-speed data communication. Ring oscillators are superior to the LC-based oscillators in several respect. Since ring oscillators consist of only transistors and no bulky inductors, the area required by ring oscillator is significantly smaller. Controlling the frequency can be achieved by varying the current used to charge and discharge the load capacitance. This method can allow a tuning range of 2:1, which is easily enough to compensate for variations due to processing, temperature and age. When a differential inverter is used, an even number of delay stages can be used in the ring. By using an even number, the ring inherently provides quadrature outputs by tapping the signals at different points, as illustrated in Figure 2-4 [21].

Figure 2-4. Differential 4-stage ring oscillator with quadrature output.

While ring oscillators provide the numerous benefits listed above, they have seen only limited use in multi-gigabit data communication for one important reason: poor phase noise. As discussed in section 2.3, the SONET stringent jitter requirement calls for a very low oscillator phase noise. It can be shown that ring oscillators have an equivalent Q of 1-1.5 [35], and, using Leeson's Equation shown in 4.27, the phase noise of the ring oscillator is about 6-10dB worse than that of a comparable LC tuned oscillator.

2.4.2.2 LC based Oscillator

A typical LC based oscillator is made up of three distinct blocks as shown in Figure 2-8. The amplifier supplies energy to maintain oscillation in the circuit during the intervals between pulses of excitation energy. The LC tank circuit alternately stores energy in the inductor and the capacitor. A portion of the output of the LC network is fed back to the input of the amplifier through the regenerative-feedback network. This regenerative-feedback helps to sustain oscillation by overcoming the effect of damping caused by the LC tank's internal and load resistance. As such, a greater than unity gain needed to sustain oscillation is achieved. The operating or center frequency of the oscillator is fixed by the resonant frequency of the LC tank circuit, which is defined by the equation:

$$f_{\text{res}} = \frac{1}{2\pi\sqrt{LC}} \quad \text{Eq.(2.2)}$$

There exists two basic types of controlled oscillators: voltage controlled oscillators (VCO) with a voltage control signal, and current controlled oscillators (ICO) with a current control signal. Of the two, the VCO is more often used in IC design.

2.4.3 LC Oscillator Topologies

There are several different topologies for LC oscillators. Classical LC oscillator designs were based on simple single-ended configurations. The four classical LC oscillator configurations are: Armstrong oscillator, Hartley oscillator, Colpitts oscillator and Clapp oscillator. Each of the four are distinguished by their method of coupling the feedback signal from the LC tank. The more recently introduced differential-pair oscillator has also been gaining popularity and usage. Newer LC oscillator circuit designs currently being introduced are often based on the basic configurations of the classical single-ended LC oscillators. Both the Armstrong and the Hartley oscillators are inductively coupled. The Armstrong oscillator (Figure 2-5(a)) uses a transformer to sample its feedback signal from the inductor of the resonant circuit. In the Hartley oscillator (Figure 2-5(b)), the feedback signal is directly tapped from the inductor. This eliminates the need for another coil.

Figure 2-5. (a) A simple Armstrong Oscillator, (b) A simple Hartley Oscillator

The Colpitts and Clapp oscillators are capacitively coupled. Specifically, the Colpitts oscillator (Figure 2-6(a)) taps its feedback signal from between two capacitors in series within the LC tank. Note the similarity between the Hartley and the Colpitts oscillator. The Hartley oscillator taps the inductor, while the Colpitts oscillator taps the capacitor. The Clapp oscillator (Figure 2-6(b)) is just a variation of the Colpitts oscillator, in that the inductor in the LC tank is replaced with an inductor in series with a capacitor. This allows frequency to be tuned via L_1 and C_3 . For a given inductor value, the Clapp configuration has a higher loaded Q than that of the Colpitts oscillator [22].

Figure 2-6. (a) A simple Colpitts oscillator, (b) A simple Clapp oscillator

In applications such as CDR or CMU, a tunable with differential or quadrature output is

often required. The differential-pair oscillator provides such complementary outputs, while additionally maximizing the rejection of common mode disturbances. Figure 2-7 shows the schematic of a differential-pair oscillator first introduced by Nguyen and Meyer in 1992 [23]. The oscillator contains two LC tank circuits with different resonant frequencies. Loop feedback is applied to each tuned circuit in a classical Colpitts configuration. The loop transmission applied to each resonator is varied by voltages V_+ and V_- . As such, the oscillation frequency can be varied continuously from the resonant frequency of the left resonator when Q_1 is on and Q_4 is off, to the resonant frequency of the right resonator when Q_1 is off and Q_4 is on.

Figure 2-7. Schematic of differential LC VCO design [22]

All above LC VCOs are described in Bipolar technology can also be realized in Standard CMOS technology. Modern differential LC VCO in CMOS technology is much simpler and utilizes only two cross-coupled transconductors (FETs) to produce a negative resistance to sustain oscillation. Such topology is called a “negative- g_m oscillator” and can be implemented in either NMOS only or PMOS only or combination of both that is complementary, as shown in Figure 2-8 [24, 25, 26] and Figure 2-9 [44]

Figure 2-8. LC VCO -Gm Oscillator architectures in NMOS and PMOS implementation.

Figure 2-9. LC VCO -Gm Oscillator in complementary implementation

2.4.4 VCO Phase Noise Requirements and Design Issues

The GR-253-CORE for SONET OC-192 systems specifies rms jitter generation to be less than 0.01U.I. (unit interval). In a closed loop system, the VCO timing jitter increases with square root of time but it reaches a saturation level for time greater than the loop time constant [27]. The feedback loop tracks the timing uncertainties which are slower than the loop bandwidth. For an rms timing jitter of 1ps (0.01 U.I), the open-loop VCO phase noise requirement is calculated to be -90 dBc/Hz @ 1MHz offset from the carrier frequency of 10 GHz, considering a loop bandwidth of 10 MHz [11]. This puts a hard specification to meet at 10GHz carrier frequency and also emphasizes special and accurate design methodology for inductor, varactors and optimization of the VCO core. Differential and symmetric structure VCO will be a good choice because such structures have already shown superior phase noise performance as compared to other LC counterparts.

2.4.5 Phase and Frequency Detector (PD or PFD)

Different parameters of phase-locked systems like tracking range, acquisition range, loop gain, and transient response make use of the properties of the phase and frequency detectors employed in such systems. Phase and frequency detector is used to compare the phase and frequency difference between the input signal and the oscillator's output signal and to convert this difference to a voltage output. That output is fed to the input of the Loop Filter, LF, as error voltage. The ideal characteristic of a PD or PFD is a linear ramp, as shown in Figure 2-10, and can be expressed by Eq. (2.3)

$$\overline{V_{out}} = K_{PD} \Delta\phi \quad \text{Eq.(2.3)}$$

where K_{PD} is the “gain” of the phase detector and $\Delta\phi$ is the input phase difference.

Figure 2-10. Phase detector and its characteristic curve

The output of the phase detector contains a desired dc component and an undesired superimposed ac component. A low pass filter is used at the PD output to cancel this ac component.

Eq. (2.3) can be modified for the case of linearized PLL model as:

$$v_d = K_d \times e \quad \text{Eq.(2.4)}$$

Phase frequency detectors (PFDs) produce two outputs that are not complementary. To convert the output to dc one approach is to sense the difference between the two outputs by means of a differential amplifier and apply the result to a low-pass filter or the outputs can drive a three-state “charge pump”.

Detection range, operating frequency, linearity, dead-zone, power consumption, cost are the main performance criteria for a phase detector to be used in a PLL [28]. There are number of PD and PFD structures, both analog and digital, currently in use [29]

- Four - Quadrant Multiplier
- Gilbert Multiplier
- Double Balanced Multiplier
- Exclusive-OR (XOR) Phase Detector
- Three - State Phase Detector
- Z - State Phase Detector
- Sample and Hold Phase Detector
- Hogge Phase Detector
- Alexander / Bang-bang Phase Detector

All the conventional PDs can only detect the phase difference between two input signals. They can be modified to detect the frequency difference also by adding frequency discriminators to them and form phase frequency detectors (PFD). A phase and frequency detector [30, 31] with no dead-zone and 2π detection range is derived from XOR PD, as shown in Figure 2-11. In such PFD, frequency detection is done prior to phase detection whenever the input signal differ in frequency with voltage-controlled oscillator (VCO) output frequency. It helps to pull the VCO output frequency back to a stable locked condition and

reduces the lock in time.

Figure 2-11. PFD with no dead zone

Since the spectrum of NRZ data contains no impulse at a frequency equal to the bit rate, the phase detector in high speed CDR application, must generate such a component. This can be achieved by either edge detection and full-wave rectification or a PD topology in which the edges of data sample the VCO output. PDs for random data must provide two essential functions [32]:

- Phase difference detection
- Data transition detection

Among PLL based clock recovery applications, the Hogge phase detector, Figure 2-12, is considered to be a very good choice [33]. Hogge type phase detector is unique in a sense that it does not need any data conversion circuitry to convert non-return-to-zero (NRZ) data to return-to-zero (RZ) data. In closed loop, the clock signal will be forced to the cen-

ter of the data eye and is inherently self correcting.

Figure 2-12. Hogge phase detector and its waveform

Although, Hogge type PD has linear characteristic, it entails a number of issues. First, the finite delay through FF1 introduces a phase offset in the locked condition [33], degrading the clock phase margin. Second, as shown in Figure 2-12, the re-timing delay through FF2

leads to a half-period skew between the pulses at V_{out1} and those at V_{out2} . As a result, even in locked condition, control line of the VCO experiences a “sawtooth”, as shown in Figure 2-13, with a positive net area [34, 35], disturbing the VCO on every data transition.

Figure 2-13. Problem of sawtooth waveform in Hogge PD

Thus, the timing skew and speed of linear phase detector circuits then became the limiting factor for aggressive designs [36].

Another type of NRZ PD is “bang-bang” PD [37] (similar to Alexander PD [38]) and is gaining popularity in high speed CDR designs [39, 40, 41]. A bang-bang PD in its simplest form can be a simple master-slave D flipflop if its clock input is driven by the data stream and its D input senses the VCO output. This topology exhibits a very nonlinear characteristic, as shown in Figure 2-14.

Figure 2-14. Simplified bang-bang PD and its non-linear characteristic

The Alexander PD is a bang-bang system, exhibiting a very high gain in the vicinity of $\Delta\phi = 0$ [32]. It employs four flipflops to realize a three-point sampling scheme and two XOR gates to compare the samples, as shown in the Figure 2-15.

Figure 2-15. (a) Alexander phase detector, (b) Three point of sampling of data by clock,
 (c) internal waveforms of Alexander phase detector

Alexander PD works on the principle of “early-late” detection method. By making use of three data sample taken by three consecutive clock edges, as shown in Figure 2-15(b), the PD can determine whether a data transition is present, and whether clock leads or lags the data. If there is no data transitions, samples S_1 , S_2 , S_3 will be equal, and no action will be taken.

Alexander PD offers two critical advantages over a simple DFF PD or to the linear type PD counterpart:

- It retimes the data automatically, producing a valid data waveform at the output of FF1 and FF2, as shown in above Figure 2-15(a).

- In the absence of data transitions, it generates a zero dc output, leaving the oscillator control undisturbed. As a result, for long data runs, the VCO frequency drifts only due to device electronic noise rather than due to high or low level on the control line.

However, the disadvantages of the non-linear type of PD are the PD gain, which is not a constant value (gain increases as loop getting closer to loop locking range) and the large number of flipflop states switching creates ripple that deteriorates the jitter performance of the loop.

2.5 Summary

In this chapter, issues and challenges in designing high speed SERDES have been reviewed. While aggressive CMOS scaling, resulting from the competition to follow Moore's law has improved the intrinsic speed of MOSFETs by more than three orders of magnitude, it also become increasingly difficult to maintain an optimum sampling phase alignment between the recovered clock and the data over process, temperature, data-rate, and voltage variation in the high speed CDR design. Two of the most critical PLL blocks; VCO and PD circuit structure options have been reviewed along with their merits and demerits. As optical standards impose severe restriction on the jitter in the transmitted and recovered data, mandating low-noise VCOs in both the transmit and the receive path of a high speed SERDES, rest of the chapters in this thesis have been dedicated to the research and design of LC tank based VCO meeting the jitter requirement of SONET OC-192 systems.

3 Fundamentals of CMOS Voltage-Controlled LC-Tank Oscillators

In the previous chapter an overview of design challenges of high speed PLL based serializer and de-serializer has been presented. Both these applications use voltage controlled oscillator as an integral part of the design with different specifications required. As the focus of this thesis is voltage controlled oscillator, this chapter begins with an introduction of oscillator theory with emphasis on inductor on chip non-relaxation type positive feedback, negative resistance voltage-controlled oscillator.

3.1 Introduction

In a CDR and CMU, of all the PLL components, design of a good VCO is very critical as this component operate at the highest frequencies within the PLL and also need to work with low power and phase noise. The designers of analog and mix-mode IC designs are facing many issues in high speed PLL applications as discussed in the previous chapter. With increase in dependency on computer simulation with increase in technology advancement, accurate device modeling is very important. For example, a VCO designed with specs of center frequency of 900 MHz and tuning range of 10%, an error of 10% will bring centre frequency to 800 MHz or above 1 GHz. In practice, an error of 10% is considered to be tolerable if VCO has good tuning range, which clearly is not the case here. Hence,

designers are now left with making several design iterations and fabrications to meet the specs. Obviously, quite undesirable in fast competitive IC industry environment, where companies go head to head to bring better and cheaper product to market as early as possible.

3.2 Basic Principles of Oscillation

A basic oscillatory system is a closed-loop system with positive feedback. Figure 3-2 shows a structure of a sinusoidal oscillator consisting of an amplifier and a feedback network.

Figure 3-1. A basic oscillatory system consisting of an amplifier and a feedback network

Using a nodal analysis, the closed-loop transfer function can be shown to be

$$\frac{A(\omega)\beta(\omega)}{1 - A(\omega)\beta(\omega)} \quad \text{Eq. (3.1)}$$

where $A(\omega)$ is the gain of the amplifier and $\beta(\omega)$ is the gain of the feedback network.

Note that both $A(\omega)$ and $\beta(\omega)$ are frequency-dependent. By Barkhausen criterion [42], the denominator must be zero for oscillation to occur. Equating this, we have

$1 - A(\omega_o)\beta(\omega_o) = 0$, known as the characteristic equation, where ω_o is the resonant frequency of the network. It follows that $A(\omega_o)\beta(\omega_o) = 1$ and $\angle A(\omega_o)\beta(\omega_o) = 2\pi \cdot n$

(or $\text{Im}\{A(\omega_o)\beta(\omega_o)\} = 0$ where n is an integer. The closed-loop transfer function has two poles at $j\omega_o$ and $-j\omega_o$, and the system oscillates at ω_o .

Figure 3-2. A conceptual implementation of the oscillator feedback loop.

An intuitive explanation [42] for the oscillation is that for the system to sustain the output x_o (Figure 3-1) without an input signal, $x_f (= \beta(\omega_o) x_o)$ must be sufficiently large so that $x_f A(\omega_o)$ equals to x_o . This again results in $A(\omega_o) \beta(\omega_o) = 1$.

A conceptual implementation of the oscillator feedback loop is shown in Figure 3-2. The transconductor is assumed to be ideal, whose input impedance is infinite and output series impedance is zero. The corresponding open-loop voltage gain $A(\omega) = G_m Z_{RLC}(\omega)$ and feedback network gain $\beta(\omega) = 1$ where G_m is positive and real, and $Z_{RLC}(\omega) = \frac{j\omega LR}{R - \omega^2 LCR + j\omega L}$ is the total impedance of the RLC network. The characteristic equation becomes $G_m Z_{RLC}(\omega) = 1$. The resonant frequency $\omega_o = \frac{1}{\sqrt{LC}}$ can be derived by solving $\text{Im}\{A(\omega_o)\beta(\omega_o)\} = 0$. The resulting $Z_{RLC}(\omega_o) = R$ and the characteristic equation is reduced to $G_m R = 1$. The G_m satisfying this relation is the minimum transconductance required for oscillation to occur (critical oscillation), denoted as $G_{m,c}$. Another view point is that the amplifier generates current i (Figure 3-2) due to the input voltage V_{in} with a transconductance G_m (i.e. $G_m V_{in} = i$), the corresponding resistance looking into the output of the amplifier is $\frac{V_o}{-i} = \frac{V_{in}}{-i} = \frac{-1}{G_m}$ which is negative. The

magnitude of the parallel negative resistance $-1/G_m$ is equal to R and cancels the loss in RLC network. Hence, there would be no damping in the oscillatory system and the oscillation can be sustained.

For wireless and serial data communication, an RF VCO is typically required to have low noise performance. Thus, the number of devices which is also the number of noise sources is usually kept as low as possible. A differential structure is also desired to have better noise immunity. An example of a popular realization is shown in Figure 3-3(a). The transistors M_1 and M_2 are cross-coupled to form a positive feedback network. Due to symmetry, the loop gain $A(\omega)\beta(\omega)$ is $(G_m Z_{net})^2$ (Figure 3-3(b)) where G_m is the effective transconductance of M_1 and M_2 , and Z_{net} is the total impedance of the network consisting of an inductor, a varactor, and the parasitics associated with the transistors and passive components (not shown in Figure 3-3(a)).

Figure 3-3. (a): An example of a popular realization of the differential negative-resistance LC-oscillator.

(b): A simplified model of (a), (c): A simplified model of (b) at resonance [49].

At resonant frequency, $(G_m Z_{net})^2$ must become unity. Thus, $G_m Z_{net} = -1$ (common source amplifier). Substituting the upper half of the circuit in Figure 3-3(b) by -1 , the

model in Figure 3-3(b) can be further simplified as shown in Figure 3-3(c). Using the simplified model, the loop gain $A(\omega)\beta(\omega)$ can be expressed as $-G_m Z_{\text{net}} \cdot (-1) = G_m R_{\text{net}} = 1$ where R_{net} is the real part of Z_{net} . This means that G_m must be equal to $G_{m,c}$ so that the product of G_m and the real loss in the network is unity. In a real CMOS oscillator, the voltage swing is typically large and the amplifiers are not ideal. The transistors actually act as loss components instead of amplifiers in some position of a cycle as the active devices are not ideal. Effective G_m which may be different from the transconductance at the quiescent bias point as well as effective R , C , and loaded Q will be discussed in section 3.3.2.

3.3 Power Consumption of LC-Oscillators

3.3.1 Useful Transformation

The parasitic resistances of an inductor and a capacitor used in an LC-oscillator are generally in series with the reactive components. This may complicate the analyses and prevent designers from having intuitive ideas of the circuits. A transformation from series to parallel connections helps to alleviate this. The parallel forms of an inductor and a capacitor with their parasitic resistances will also be used for oscillator analyses in section 3.3.2

Figure 3-4. The transformation between series and parallel connections.

Illustrated in Figure 3-4 are the desired transformations. The derivation is straight forward. By equating the total impedances of the networks, L_2 and R_L' can be expressed in terms of L_1 and R_1 as

$$L_2 = L_1 + \frac{R_1^2}{\omega^2 L_1} = L_1 \cdot \left(1 + \frac{1}{Q_L^2(\omega)} \right) \quad \text{Eq. (3.2)}$$

and

$$R_L' = \frac{\omega^2 L_1^2 + R_1^2}{R_1} = R_1 \cdot (1 + Q_L^2(\omega)) \quad \text{Eq. (3.3)}$$

where $Q_L = \omega L_1 / R_1 = R_L' / \omega L_2$ is the quality factor of the inductor with its parasitic

resistance. Similarly, C_2 and R_C' can be expressed in terms of C_1 and R_3

$$C_2 = \frac{C_1}{1 + \omega^2 R_3^2 C_1^2} = \frac{C_1}{1 + \frac{1}{Q_C^2(\omega)}} \quad \text{Eq. (3.4)}$$

$$R_C' = R_3 + \frac{1}{\omega^2 R_3 C_1^2} = R_3 \cdot (1 + Q_C^2(\omega)) \quad \text{Eq. (3.5)}$$

where $Q_C = 1 / \omega C_1 R_3 = \omega C_2 R_C'$ is the quality factor of the capacitor with its parasitic resistance. The LC network (Figure 3-5) used in a VCO typically consists of series parasitic resistances associated with the inductor and varactor. From Eq.(3.3) and Eq.(3.5), the equivalent parallel parasitic resistances are proportional to Q^2 and the resonance frequency of the RLC network can be obtained using Eq.(3.2) and Eq.(3.4).

Figure 3-5. Transformation of a typical lossy LC-network to its equivalent parallel RLC network.

$$\omega_o = \frac{1}{\sqrt{L_1 \cdot \left(1 + \frac{1}{Q_L^2(\omega)}\right) \cdot \frac{Q_C^2(\omega) \cdot C_1}{Q_C^2(\omega) + 1}}} \bigg|_{\omega = \omega_o} = \sqrt{\frac{L_1 - C_1 R_1^2}{C_1 L_1^2 - R_3^2 C_1^2 L_1}}$$

When R_1 and R_3 are zero, ω_o is reduced to $1/(\sqrt{L_1 C_1})$. The resistances of R_1 and R_3 typically have a minor effect on the resonant frequency ω_o .

3.3.2 Power Consumption versus C/L Ratio

Using the LC-oscillator model shown in Figure 3-2, relations between power consumption and capacitance/inductance ratio can be found. First, if one considers an LC network of a VCO with the parasitic series resistances associated with L_1 and C_1 , the equivalent parallel RLC circuit model can be immediately derived using the transformations shown in the previous section (Figure 3-5). Typically, Q of the network in a monolithic VCO is dominated by that of the inductor. Thus, $R = R_C' \parallel R_L'$ may be approximated by R_L' . In addition, two other approximations $L_1 = L'$ and $C_1 = C'$ can be made with less than ~8% errors between 1GHz and 20 GHz since Q_L^2 and Q_C^2 are typically larger than 12.

To simplify the derivation, let $L_1/R_1 = k$ where k is a constant for a given technology (this is true only for some types of inductors such as bondwires at low to moderate frequencies, and not strictly true for spiral inductors). Using Eq.(3.3), R at oscillation frequency ω_o can be expressed as:

$$R = \text{Re}(Z_{\text{net}}) = R_1 + \omega_o^2 k L_1 \quad \text{Eq. (3.6)}$$

Since $G_m \text{Re}(Z_{\text{net}}) = 1$ at ω_o and R_1 is typically $\ll \omega_o^2 k L_1$, the required G_m is inversely proportional to L_1 . Hence, a larger L_1 or a smaller C_1/L_1 ratio for a given ω_o requires smaller G_m and a lower power consumption. Since $R_1 = L_1/k$, Eq. (3.6) can be rewritten in terms of C_1

$$R = \frac{L_1}{k} + \frac{k}{C_1} = \frac{1}{C_1} \cdot \left(\frac{1}{\omega_o^2 k} + k \right) \quad \text{Eq. (3.7)}$$

It follows that the required G_m is proportional to C_1 . A larger C_1/L_1 ratio for the same ω_o needs more bias current to sustain the oscillation.

For a practical LC-oscillator, the total capacitance “C” consists of varactor capacitance where $0 < \alpha < 1$, and the parasitic capacitances ($C(1-\alpha)$) associated with the inductor and active devices, which are assumed to be constant. Assuming that the total inductance is L , C/L ratio is r , the equivalent parallel tank resistance is R and the tail current is $2I$ (Figure 3-3(a)), the tank amplitude V_{amp} is proportional to IR [43], [44]. If the varactor capacitance can be tuned between $\chi\alpha C$ and αC where $\chi(0 < \chi < 1)$ is the capacitance ratio between minimum and maximum capacitances of a varactor for a given bias voltage range, the frequency tuning range can be expressed as

$$\frac{1}{\sqrt{L(C(1-\alpha)) + \chi\alpha C}} - \frac{1}{\sqrt{LC}} = \omega_o \left(\frac{1}{\sqrt{1 - (1-\chi)\alpha}} - 1 \right) \quad \text{Eq. (3.8)}$$

Now if the total capacitance is changed to $\beta C (\beta > (1-\alpha))$ by increasing / decreasing the varactor capacitance while keeping the same ω_o (the corresponding total inductance should be redesigned to be L/β), the equivalent tank resistance becomes R/β according to Equation 3.9 if Q_C and R_C' are once again assumed to be much larger than Q_L and

R_L . The corresponding current to have the same tank amplitude is βI . The resulting frequency tuning range is:

$$\frac{1}{\sqrt{\frac{L}{\beta}} \cdot (C(1 - \alpha)) + \chi(\beta C - C(1 - \alpha))} - \frac{1}{\sqrt{\frac{L}{\beta}} \cdot \beta C} \quad \text{Eq. (3.9)}$$

$$= \omega_o \left[\frac{1}{\sqrt{\chi + \frac{(1 - \chi)(1 - \alpha)}{\beta}}} - 1 \right] \quad \text{Eq. (3.10)}$$

Hence, in order to increase the frequency tuning range, β must be increased so that the expression inside the square root decreases, resulting in larger power consumption. In addition, if the varactor capacitance is much larger than the total parasitic capacitance ($\alpha \rightarrow 1$), both Eq. (3.9) and (3.10) are equal to $\omega_o \left(\frac{1}{\sqrt{\chi}} - 1 \right)$. That is, the frequency tuning range for a given ω_o is independent of the C/L ratio, and only depends on the varactor characteristics. The upper limit of the frequency range is $\omega_o \left(\frac{1}{\sqrt{\chi}} - 1 \right)$ when the total parasitic capacitance is negligible relative to the varactor capacitance. Therefore, decreasing C does not sacrifice the tuning range while decreasing the power consumption if the varactor capacitance is much larger than the total parasitic capacitance.

3.3.3 Noise Performance of an Oscillator

A figure of merit for the noise performance of an oscillator is phase noise which measures the short-term frequency stability of an oscillator. It is defined as $10 \cdot \log \frac{P_{\text{sideband}}(\omega_o + \Delta\omega)/\text{Hz}}{P_{\text{carrier}}}$ where P_{carrier} is the carrier power and $P_{\text{sideband}}(\omega_o + \Delta\omega)/\text{Hz}$ is the total power in a 1-Hz bandwidth at an offset of $\Delta\omega$ from ω_o . The unit is dBc/Hz where dBc indicates a measurement in dB relative to the carrier power. Figure 3-6 illustrates the phase noise definition.

Figure 3-6. An illustration of definition of phase noise.

The phase noise generated by a VCO is determined by:

- (a) Q factor of the resonator
- (b) Q factor of the varactor
- (c) the active device used for the oscillating transistor
- (d) power supply noise
- (e) external tuning voltage supply noise

The noise contribution made by (d) and (e) can be minimized by careful choice of the power supplies. Good, low noise power supplies, ideally, DC batteries for both supply (V_{cc}) and

tuning (V_{tune}) voltages will provide the best overall performance. The phase noise of the VCO is therefore determined primarily by the overall Q of the circuit. In order to achieve a circuit high Q , the tuning bandwidth must be made small. Therefore, a VCO designed for low phase noise performance will have a smaller tuning range.

3.4 Q of LC Oscillator

3.4.1 Q of an Ideal LC Oscillator

From Barkhausen criterion, the oscillation frequency ω_o is determined by the condition $\angle Z_{\text{net}} = 0$. Due to noise present in the oscillator, the criterion may not hold all the time. The characteristic of how the phase of the circuit changes with respect to the change of oscillation frequency ($d\Phi/d\omega$) becomes one of the ways to measure the performance of an oscillator [42]. If ($d\Phi/d\omega$) is large, then a small change, $\Delta\omega$, results in significant change of phase, $\Delta\Phi$. This change in phase makes the VCO violate the Barkhausen criterion and in turn prevents the VCO from oscillating at $\omega_o + \Delta\omega$. Larger ($d\Phi/d\omega$) results in better concentration of energy at ω_o and lower phase noise. This behavior represents the short-term frequency stability of an oscillator. Let the impedance of the LC-network shown in Figure 3-2 be $H(\omega)$. Differentiating $\Phi = \angle H(\omega)$ with respect to ω and evaluating at ω_o , we have $\frac{S_F}{\omega_o} = \frac{d\angle H(\omega)}{d\omega} \Big|_{\omega = \omega_o} = \frac{d\Phi}{d\omega} \Big|_{\omega = \omega_o}$ where S_F is the frequency stability factor. And the Q of the oscillator (also known as stability Q) can be defined as $\frac{S_F}{2}$ [45], [46], [47].

Since an LC-network is a band pass filter (BPF), another way to define the Q of an oscillator is to use the 3-dB bandwidth [46]. It is defined as the ratio of the center frequency to the

two-sided-3-dB bandwidth, $\Delta\omega = \omega_1 + \omega_2$, where $\omega_0 - \omega_1$ and $\omega_0 + \omega_2$ are the frequencies at which the magnitudes of $H(\omega)$ are $\frac{1}{\sqrt{2}}$ of that at ω_0 . If Q is high, there will be large attenuation on the skirt of the oscillator output spectrum resulting in lower phase noise.

3.4.2 Q of a Nonideal LC Oscillator

The above two Q definitions can be easily applied to any ideal oscillator whose active device(s) has (have) infinite output resistance and the capacitances and resistances present in the LC tank have no voltage dependence. However, a real oscillator fabricated using semiconductor devices typically has finite output resistance from the active device(s) and the varactor capacitances typically have strong voltage dependence as well. The non-ideality of the elements introduces nonlinearity to the LC tank making it difficult to estimate the loaded Q using the definitions mentioned previously. Moreover, due to a large signal swing, the active devices in an oscillator, for example Figure 3-3(a), act as an energy provider for approximately a half period ($T/2$ where T is the inverse of the oscillation frequency f_0) while act as a resistor or open for the other $T/2$ as illustrated in Figure 3-7. That is, the output resistances of the transistors are also voltage dependent. Hence, the loaded Q , effective G_m and effective tank resistance and capacitance could be significantly different from those at quiescent bias condition.

Figure 3-7. An illustration of the bias conditions of active devices in an oscillator [49].

3.5 Noise Sources in CMOS Oscillator

3.5.1 Flicker ($1/f$) Noise

In MOS transistors, the mobility and carrier number fluctuations result in high flicker ($1/f$) noise [48], which poses problems for attaining low close-in phase noise in CMOS VCO's. Figure 3-8 shows the normalized (to $1\text{ }\mu\text{m}$ width) input-referred $1/f$ noise spectra for NMOS and buried channel PMOS transistors from the $0.8\text{ }\mu\text{m}$ CMOS process at $|V_{GS}|$ and $|V_{DS}|$ of 1.0 and 2.0V (in saturation region of operation), respectively [49].

Figure 3-8. Noise spectra of a PMOS and a NMOS transistor at $|V_{GS}|=1.0\text{V}$ and $|V_{DS}|=2.0\text{V}$.

The input-referred $1/f$ noise S_{vg} is calculated by dividing measured output (current) noise S_{Id} by g_m^2 . The PMOS flicker noise is around one order of magnitude lower than the noise of the NMOS transistor with a surface channel. If the dc bias current were kept the same for the transistors by adjusting the widths, the difference would have been even greater. Using the simple theory [50],

$$S_{vg} = \frac{K_f}{W \times L \times C_{ox} \times f^{A_f}} \quad \text{Eq. (3.11)}$$

the extracted K_f parameters for the NMOS and PMOS transistors are 3.8×10^{-24} and $4.2 \times 10^{-25} \text{ V}^2\text{F}$, respectively.

For a deep submicron CMOS process, both NMOS and PMOS transistors are surface channel devices, and concern is that PMOS may have the same poor $1/f$ noise performance as NMOS transistors. However, measurements show that the PMOS $1/f$ noise is ~8-10 times smaller at 100kHz for the same transistor dimension and gate over drive ($V_{GT} = V_{GS} - V_T$) when the V_{GT} is smaller than ~0.3V [49]. In addition, when compar-

ing NMOS and PMOS transistors for oscillator applications, the LC-tank, G_m and I_D should be kept the same. The required channel width of a PMOS transistor is larger than that of an NMOS transistor due to the mobility difference. Hence, PMOS transistors still have the advantage of attaining low close-in phase noise in oscillator applications. As the devices are scaled down below $\sim 0.5 \mu\text{m}$, Eq. 3.12 does not hold. The dependence of L and C_{ox} becomes stronger, and thus, $1/f$ noise is higher for shorter channel devices [48], [49], which is an additional concern for VCO built using these technologies.

3.5.2 Channel Thermal Noise

Thermal noise in a MOS transistors originates from the resistive channel. It is white and may be expressed as $\overline{i^2} = \gamma 4kTg_m \Delta f$ where γ is a constant, k is the Boltzmann's constant and T is the temperature. The constant γ is $2/3$ for long channel devices and is typically significantly greater than $2/3$ (increases as $\frac{1}{L_{eff}^a}$ where L_{eff} is the effective channel length and "a" may be between 2 and 3) for short channel devices due to the hot electron effect [50]. Unlike the phase noise in $1/f^3$ region (contributed from $1/f$ noise) which may be reduced by a PLL (Figure 2-2), the phase noise converted from the thermal noise in $1/f^2$ region is typically outside the loop bandwidth and will not be suppressed by the PLL. According to [51], the hot electron effect for a PMOS transistor is smaller than that of an NMOS transistor because the impact ionization rate of electrons is 1-2 orders of magnitude higher than that of holes. Thus, PMOS is once again should be the preferred device for oscillators.

3.5.3 Noise from Power Lines and Substrate Coupling

When noise exists in the power and ground connections, the phase noise of an oscillator tends to be degraded even if the oscillator has a differential structure. There are two sources responsible for this [52]. One is the voltage-dependent drain-to-body capacitance, C_{db} , which senses the noise in power and ground lines, and translates it to FM noise and thus phase noise. The other is the insufficient common mode rejection ratio (CMRR) and power supply rejection ratio (PSRR) of the amplifier. The noise in the substrate is coupled in the same way as the supply noise. To reduce the noise coupled from supply and substrate, large bypass capacitors for dc lines and lots of substrate contacts surrounding the oscillator are needed to provide low-impedance grounding paths. The sensitivity of the oscillatory frequency to the supply voltage is called frequency pushing, and is expressed in Hz/Volt.

3.5.4 Noise/Effects from the Load

If an oscillator is not buffered, the noise in the load or subsequent circuit block which may be much larger than that of a buffer for the VCO can contribute significant noise back to the oscillator core. Another more serious problem is the injection locking. This happens when there is a strong signal at ω_s injected into the output port of the oscillator. The oscillator signal will tend to change frequency and will eventually lock onto ω_s if ω_s is within the pull-in range of the oscillator [53]. The last effect from the load is the frequency pulling which is due to a non-ideal load. That is, the oscillation frequency can be changed if the load changes its impedance from time to time or periodically. Hence, adding a buffer can improve the isolation although the buffer also adds noise.

3.5.5 Noise from the Bias Circuit

The bias current of an oscillator is typically controlled by a current source as shown in Figure 3-3(a). The noise from this current source can vary the g_m of the cross-coupled transistors and cause AM noise which may be converted into phase noise [54], [55]. Since the noise is common mode in nature, it may also vary the voltage across the tuning device resulting in FM noise and thus phase noise. In addition, the reference current generator and current mirror typically consist of many devices. Its output noise can directly modulate the output of the current source, and can further increase the phase noise.

It has been shown that the noise due to a bias circuit can contribute as high as 15% to the oscillator phase noise [55].

3.6 Phase Noise Measurement

Phase noise can be measured in different ways. Batteries are typically used as power supply of the device under test (DUT). The simplest method is to measure using a spectrum analyzer. However, there are limitations associated with the dynamic range and the fact that the input signal from a free running VCO may not be stable. The details as well as measurement using more sophisticated systems are described in this section.

3.6.1 Spectrum Analyzer

The simplest way to measure phase noise of an oscillator is to directly connect the DUT to a spectrum analyzer. This measures the short-term frequency stability of an oscillator. A spectrum analyzer measures the total power (P) in a frequency band referred to as the res-

olution bandwidth (RBW) which can be changed by users. The unit of the spectral density displayed on a spectrum analyzer is thus typically dBm/(RBW Hz). To compute the phase noise, the relative power level, P_r , at an offset frequency from the carrier is measured relative to the carrier power. It is then normalized to dBc/Hz by subtracting $10 \times \log(\text{RBW})$ from P_r . An assumption is that the power spectral density over the RBW is flat (white). The first limitation with this method is that the noise floor of the measurement system is limited by the LO of the spectrum analyzer. With a synthesized LO, a modern spectrum analyzer such as HP8563E has a sensitivity of ~ -149 dBm at 1 GHz. The second limitation is the measurable phase noise which is limited by the dynamic range of the spectrum analyzer. The dynamic range comes from the maximum allowed input power to the mixer (p_{max}) in a spectrum analyzer and the sensitivity of a spectrum analyzer. This limitation can be improved by the methods described in the following sections.

3.6.2 Phase-Locked Loop

To improve the dynamic range limit discussed above, a phase noise measurement setup with an external low noise source and a comparator can be used. A simplified configuration is shown in Figure 3-9. The basic principle of this method is to down convert the DUT output to baseband using a PLL formed by a low noise reference source, a phase detector and a narrow band low pass filter so that the strong carrier power is rejected, thus eliminates the dynamic range limitation due to a large carrier power. The measurable phase noise will then be limited by the sensitivity of the spectrum analyzer. The bandwidth of the narrow band filter (which is programmable in some measurement systems) must be

narrow enough (typically less than 100 Hz) so that the measured sideband represents the true oscillator sideband instead of the PLL sideband

Figure 3-9. A simplified configuration of phase noise measurement setup with an external low-noise reference source and a comparator.

The phase noise of the reference source obviously needs to be much lower than that of DUT. The amplifiers are necessary to avoid injection locking between the two sources. This configuration still suffers the limitation of system noise floor which is due to phase noise of the reference source and LO of the spectrum analyzer.

3.6.3 Frequency Discriminator

A phase noise measurement setup using a discriminator could give a better noise floor because there is no reference source needed in the system. Similar to the set-up using an external low noise reference source, the dynamic range limit can be improved. Figure 3-10 shows the setup. This method is also referred to as the autocorrelation method since the signal at the output of the double balanced mixer has the form of $E[x(t)x(t + \tau_d)]$ [56] which represents the power spectral density of the random process after being converted to frequency domain. A disadvantage is that the noise floor tends to be degraded for low

offset frequencies [57].

Figure 3-10. A phase noise measurement setup using a frequency discriminator.

3.7 Summary

In this chapter, basic principles of LC-oscillators were discussed. The relationship between power consumption and C/L ratio of an LC-tank which also directly influences the tuning range of a VCO was derived. This gives a guideline for choosing inductance and capacitance values when designing a VCO. A major factor in an oscillator design is the quality factor of the LC-tank. The effect of Q on oscillator power consumption was discussed. To better understand the contributions of phase noise in an oscillator, the noise sources in CMOS oscillators were identified. Finally, phase noise measurement setups were briefly presented. These discussions provide basic guidelines to improve the design and measurements of VCOs.

4 Passive Components Design Methodology

4.1 Inductor Design

4.1.1 Background

An important quantity in the characterization of resonant tank circuits is the quality factor (Q), which is defined as:

$$Q = 2\pi \frac{\text{maximum energy stored}}{\text{energy dissipated per cycle}} \quad \text{Eq. (4.1)}$$

The resonator Q will strongly influence both the phase noise and the power consumption of an oscillator. The inductor in an LC oscillator is usually the most critical circuit element in the design—typically, the Q of the inductor dominates the total Q of the tank circuit. In addition, the tuning range of a VCO is strongly affected by the self-resonant frequency (f_{sr}) of an inductor. The self resonant frequency is that frequency at which capacitive parasitics result in a zero net reactance; beyond this frequency the inductor becomes capacitive.

Traditionally, inductors have been incorporated as discrete components located off-chip (often as small surface mount parts). While off-chip inductors can have extremely good performance, it is desirable to eliminate as many discrete components as possible. This

reduces the board-level complexity and component count, which in turn leads to a direct reduction in cost. As an alternative to off-chip inductors, some RF integrated circuits have utilized bonding wires as hybrid inductors [58], [59]. While bonding wires can have a relatively high Q (on the order of 50), they can also suffer from large variations in inductance value since wire bonding is a mechanical process that cannot be as tightly controlled as photolithographic processes.

Monolithic inductors fabricated as simple planar spirals are now widely used on GaAs substrates with Q 's in the range of 10-20. The inductance of a monolithic inductor is defined solely by its geometry. Modern photolithographic processes provide extremely tight geometric tolerances in the range of $\pm 1\%$. For this reason monolithic inductors have very small variations in their performance.

Unlike standard Si technologies, GaAs processes are more conducive to the fabrication of monolithic inductors since the GaAs substrate is a nearly perfect insulator ($\rho \cong 10^8 \Omega \cdot \text{cm}$) and the metallization used is often thick electroplated gold ($\sigma \cong 4.1 \times 10^7 \text{ S/m}$). Silicon substrates have a resistivity that varies from 10 -100 $\Omega \cdot \text{cm}$, for Bipolar and BiCMOS to as low as 0.01 $\Omega \cdot \text{cm}$ on some digital CMOS processes. Furthermore, the metallization has traditionally been aluminum which has a low thin-film conductivity (although copper has appeared recently as an alternative interconnect metal [60], [61]). Monolithic inductors are becoming popular for BiCMOS technologies, especially the newer SiGe processes which are tailored for RF design [62]. However, these processes are still more costly than the standard digital CMOS process. The

dream of many RFIC designers is to be able to leverage the same economies of scale that have supported Moore's law for nearly two and a half decades for the realization of RF systems. For this reason, much recent effort has been focused on the problem of fabricating RF inductors in CMOS processes. In this chapter monolithic inductor design in a generic¹ digital CMOS process is explored.

(¹generic = low-resistivity substrate, single layer of poly, strict adherence to DRC rules, and no extra post-processing steps.)

Figure 4-1. Spiral inductor geometries: (a) circular spiral, (b) octagonal spiral, (c) square spiral.

4.1.2 Inductor Geometries

There are many ways to layout a planar spiral inductor. The optimum structure is a circular spiral. This structure [Figure 4-1(a)] places the largest amount of conductor in the smallest possible area, reducing the series resistance (R_s) of the spiral. This structure, however, is not often used because it is not supported by many mask generation systems. Many of these systems are only able to generate layouts style which contain structures with 90

degree angles (and possibly 45 angles as well). While the curved metal traces can be approximated in a step-wise fashion, a simpler solution is to approximate the circle with a polygon. Figure 4-1(b) shows an octagonal spiral that only requires the mask maker to generate 45 degree angles in addition to the standard 90 degree geometries. This structure has a Q that is slightly lower than the circular structure, but is much easier to layout. For the CMOS process used in this thesis only square and octagonal shapes are allowed. The square spiral structure does not have the best performance but it is one of the easiest structures to model, simulate and layout. For this reason the standard square spiral structure of Figure 4-1(c) was chosen.

Figure 4-2. Parameters for Equation (4.2)

The square spiral inductor has been studied extensively in [61], [63], [64]. The following recently published expression has demonstrated good accuracy for predicting the inductance of a square spiral [65]:

$$L = \frac{2\mu_0 n^2 d_{avg}}{\pi} \left[\ln\left(\frac{2.067}{\rho}\right) + 0.178\rho + 0.125\rho^2 \right] \quad \text{Eq.(4.2)}$$

where n is the number of turns in the spiral, and the parameters d_{avg} , and ρ are defined in Figure 4-2. μ_0 is the permeability of free space, d_{avg} represents the average diameter of the spiral, and ρ represents the percentage of the inductor area that is filled by turns. Equation (4.2), is based on a current sheet approximation of the spiral structure, and is valid only for square spirals. Predicting parameters such as inductor Q and self resonant frequency f_{sr} , generally cannot be done with a simple formula. These parameters are usually obtained through EM simulations.

4.1.3 Losses in spiral inductors

There are several sources of loss in a spiral inductor. The most obvious loss mechanism is the series winding resistance, R_s . The interconnect metals used in most CMOS processes are aluminum and copper. Depending on the metallization thickness and particular alloy used, the sheet resistivity can be anywhere from 30-70 (m Ω)/(sq). The DC resistance of the spiral is easily calculated as the product of this sheet resistance and the number of squares in the spiral. However, at higher frequencies the resistance of the spiral increases due to the skin effect and current crowding at the corners of the spiral.

As mentioned above, the introduction of copper metallization and thick upper-level inter-

connect have yielded improvements in the maximum inductor Q_s that have been reported in CMOS [61]. In addition, multiple levels of metallization may be strapped together to create a spiral with a lower DC winding resistance [66]. However, substrate losses ultimately remain the limiting factor even when the conductivity of the spiral windings is no longer an issue. Since the silicon substrate is neither a perfect conductor nor insulator there are resulting losses in the reactive fields that surround the windings of the spiral. Figure 4-3, shows the loss mechanism in integrated inductor.

Figure 4-3. Losses in integrated inductor [79].

At very low frequencies the bulk resistance of the metal and the resistance of inter-level vias will dominate the quality factor. The Q will be directly proportional to frequency since resistance is constant $Q \propto f$, and inductive reactance is proportional to frequency. At higher frequencies (typically $>1\text{GHz}$), the skin effect causes the resistance to rise at the square root of frequency, hence Q is proportional to square root of frequency $Q \propto \sqrt{f}$.

However, with silicon substrate there is capacitive coupling from the metal through the oxide layer into the lossy substrate. This results in Q having an inverse square relationship with frequency $Q \propto f^{-2}$. As a result Q peaks at a frequency in the transition between skin effect dominated and substrate loss dominated regions.

In a CMOS process the windings of the spiral are separated from the substrate by a thin layer of silicon dioxide (SiO_2). This creates a capacitance between the spiral and the surface of the substrate. In most digital CMOS processes, this substrate is heavily doped p+ material and is tied to ground potential. Thus, the substrate appears as a grounded resistor in series with this capacitance. This substrate capacitance has two detrimental effects in a circuit:

- (1) it allows RF currents to interact with the substrate, lowering the Q of the circuit;
- (2) it increases parasitic capacitances, reducing the self resonant frequency (f_{sr}).

This capacitance can be reduced by decreasing the area occupied by the inductor traces, but this in turn will increase the series resistance of the inductor. This is an important trade-off, since wide traces are generally used in inductors on silicon to overcome the low thin-film conductivity of the metallization. This also limits the feasibility of creating arbitrarily large valued inductances

Figure 4-4. Eddy currents due to magnetic field

Figure 4-4, shows the losses due to the magnetic field in the inductor structure. The magnetic field $\vec{B}(t)$ extends around the windings of the spiral and into the substrate. Faraday's Law states that this time-varying magnetic field will induce an electric field in the substrate. This field will force an *image* current to flow in the substrate in the opposite direction of the current in the winding directly above it. These image currents can account for 50 percent or more of the losses in a CMOS inductor [58].

This effect can also be thought of as a parasitic transformer, where the substrate represents an unwanted secondary winding. Larger inductors will have magnetic fields that penetrate deeper into the substrate, and will therefore suffer from higher substrate losses. This effect is in opposition to the goal of limiting series resistance with wide spiral traces. The substrate effects could be avoided by utilizing a post processing step to etch the substrate away under the inductor [67], however for this research no non-standard processing steps are used.

The magnetic field will not only penetrate into the substrate but also into the other wind-

ings of the coil, further increasing the loss [58]. Figure 4-4, shows the eddy currents that are generated in the center of a winding. This effect causes the inner turns of the inductor to contribute much more loss to the inductor while having a minimal impact on the actual inductance. This phenomenon is sometimes referred to as “current crowding” [68], [69]. In [68] a 9 turn inductor was simulated using a finite-element field solver. It was found that the resistance of the outer turn at 2 GHz was 18% higher than its DC value; however, the resistance of the inner turn at 2 GHz increased by 480% over its DC value. For this reason spiral inductors on silicon typically utilize “hollow” centers in order to increase their Q [58].

4.1.4 Inductor Circuit Models

A circuit model for a monolithic inductor on a low-resistivity substrate is shown in Figure 4-5 [70].

Figure 4-5. Spiral inductor lumped circuit model

This model includes circuit elements that model the loss mechanisms that were discussed

in Section 4.1.3. This circuit accurately models inductors on low resistivity silicon substrates since it includes the effect of the magnetic eddy currents. The magnetic substrate loss is represented in this model as an ideal transformer coupled to the resistor, $R_{\text{sub (m)}}$. Some confusion exists in the literature regarding how the quality factor (Q) and inductance (L) of a monolithic inductor should be defined, particularly with regard to differential (balanced) versus single-ended (unbalanced) implementations. Typically, the inductance of a monolithic inductor is calculated by converting measured or simulated S-parameters into Y-parameters. These Y-parameters are then used to extract the value of L and Q. In cases where one side of the inductor is grounded (i.e. single-ended or unbalanced), L is often defined as:

$$L = 2\pi \left(\frac{1/Y_{11}}{2\pi f} \right) \quad \text{Eq. (4.3)}$$

In other cases where the inductor is used differentially (i.e. balanced), L is often defined as [70],[71]:

$$L = \text{Im} \left(\frac{1/Y_{12}}{2\pi f} \right) \quad \text{Eq. (4.4)}$$

Depending upon the inductor application either of these expressions may be acceptable. To understand the difference between the above definitions it is helpful to look at the π equivalent of a two-port network (Figure 4-6). This circuit model expresses the two-port Y-parameters as admittances in a π network. For a passive reciprocal network, $Y_{12} = Y_{21}$. If the network is symmetric, $Y_{11} = Y_{22}$. To define inductance and quality

factor, this π model must be reduced to a single element (i.e. an inductance in series or parallel with a resistance). For the case of a simple series element $R + jX$:

$$L = \frac{X}{(2\pi f)} \quad \text{Eq. (4.5)}$$

Figure 4-6. : π equivalent circuit for a two-port network.

Figure 4-7. Two methods of reducing π -network.

and

$$Q = \frac{X}{R} \quad \text{Eq. (4.6)}$$

There are two simple methods of reducing the π -circuit to the series element, $R+jX$ (Figure 4-7). If port 2 of the π -circuit is grounded, the $Y_{22} = Y_{12}$ element is bypassed and the circuit looking into port 1 reduces to the admittance Y_{11} connected to ground

(since admittances in parallel add, Y_{12} is eliminated). Converting admittance to impedance, $R + jX$ becomes:

$$R + jX = \frac{1}{Y_{11}} \quad \text{Eq. (4.7)}$$

If this assumption is valid, then L and Q may be defined using:

$$L = \text{Im}\left(\frac{1/Y_{11}}{2\pi f}\right) \quad \text{Eq. (4.8)}$$

and

$$Q = \frac{\text{Im}(1/Y_{11})}{\text{Re}(1/Y_{11})} \quad \text{Eq. (4.9)}$$

This method is valid if the inductor will be used in a circuit where one terminal of the inductor is connected to AC ground. This is often the case in many RF circuits, particularly in LNAs and mixers, where inductors are used for degeneration or loading. This method is also equivalent to taking one-port S-parameter measurements with one terminal of the inductor grounded, and converting the measured reflection coefficient, Γ , into an input impedance. Using this approach with port 2 grounded yields:

$$\Gamma_1 = S_{11} - \frac{S_{12}S_{21}}{1 + S_{22}} \quad \text{Eq. (4.10)}$$

The series impedance is then given by:

$$R + jX = Z_{\text{in}} = Z_0 \frac{1 + \Gamma_1}{1 - \Gamma_1} \quad \text{Eq. (4.11)}$$

which is equivalent to Equation (4.7).

On the other hand, if the inductor will be used in a differential configuration (i.e. neither port is at AC ground potential) a different approach is required. The floating impedance, $R + jX$, seen between ports 1 and 2 of the π -network is

$$R + jX = \left(-\frac{1}{Y_{12}} \right) \parallel \left(\frac{1}{Y_{11} + Y_{12}} + \frac{1}{Y_{22} + Y_{12}} \right) = \frac{Y_{11} + Y_{22} + 2Y_{12}}{Y_{11}Y_{22} - Y_{12}^2} \text{ Eq.(4.12)}$$

Since in this case, the shunt elements $Y_{11} + Y_{12}$ and $Y_{22} + Y_{12}$ of the π network are the parasitic capacitances to ground (perhaps in series with a substrate resistance, see Figure 4-5), they are often ignored (particularly in technologies using insulating substrates) and L is calculated using Eq. (4.4) [70], [37]. The impedance calculated in Eq. (4.12) is referred to as floating since it ignores the ground connection in the equivalent circuit. This is valid, since if the inductor is connected in this manner, the ground as represented in Figure 4-6 is no longer explicit and exists only as virtual ground. Inductors connected in this manner are often referred to as floating or differential and L and Q can be defined as:

$$L = \text{Im} \left(\frac{1/Y_{12}}{2\pi f} \right) \quad \text{Eq. (4.13)}$$

$$Q = \frac{\text{Im}(1/Y_{12})}{\text{Re}(1/Y_{12})} \quad \text{Eq. (4.14)}$$

In most cases the differential Q measured using this method will be slightly higher (3-5 percent) than in the grounded one port case. If the shunt elements $Y_{11} + Y_{12}$ and $Y_{22} + Y_{12}$ are not negligible (as is the case in standard CMOS) it is more accurate to use

Eq. (4.12) in conjunction with Equations (4.5) and (4.6) to calculate L and Q rather than Equations (4.13) and (4.14).

In this thesis both methods of reporting L and Q are used. Although the total tank inductance is floating, it will actually be implemented as two identical inductors in series. While, the total tank inductance uses the differential inductor definitions, each individual inductor is considered using the simplified one port approach. Where not explicitly stated, subsequent references to L and Q in this thesis should be considered to follow this convention.

4.2 Inductor Layout Issues

Off-chip inductors are usually realized as a solenoidal coil or toroid. The magnetic energy is stored mostly in the inner core of each winding. The inductance is largely a function of the area of the loop and the number of turns in the winding typically resulting in an N^2 dependence.

4.2.1 Planar Structures:

Since on-chip inductors are constrained to be planar, the typical solution is to form a circular spiral. Such a structure is optimal given this constraint. However, since some IC processes constrain all angles to be 45 or 90 degrees, square or octagonal approximations are used as reasonable facsimiles.

In designing integrated circuits, it is sometimes convenient to tap an inductor at some arbitrary point. While this is certainly possible, as more than one metal layer is present, it is sometimes necessary to tap a spiral in the centre, especially for differential circuits. In a

spiral it is difficult to find such a symmetric centre point since the electric fields on the outer turns tend to fringe and thus the “inductive” centre does not correspond to the “capacitive” centre. Also, the “inductive” centre does not correspond to the “resistive” centre due to the non-uniform mutual magnetic coupling. To solve this problem, some researchers have proposed symmetric structures, such as that shown in Figure 4-8.

Note that each turn involves a metal-level interchange, a process that requires vias. A different centre-tapped structure proposed by [72] requires only one metal interchange. These structures have a natural geometric centre which coincides with the electrical centre point. This is needed in differential circuits as such points can be connected to an AC ground without disturbing the differential signal.

Since modern standard CMOS processes offer multi-metal layers, two simple approach in taking advantage of these extra metal layers are to connect multiple spiral inductors in series or in shunt. While N spirals in series increase the series resistance by a factor due to the mutual magnetic coupling. At low frequencies where the current flowing through each series connected spiral is equal, the effective inductance of N series connected coupled inductors is:

$$L_{\text{series}} = \sum_{i=1}^N L_i + 2 \sum_{i=1}^N \sum_{i \neq j} M_{ij} \quad \text{Eq. (4.15)}$$

where M_{ij} is the mutual coupling between each series connected spiral i and j.

Thus, the series connection approaches an N^2 increase in inductance and the Q factor can potentially increase by a factor of N for the case of perfectly coupled spirals ($k = 1$).

Alternatively, in the shunt connection, the series resistance drops by a factor of N (assuming equal resistivity in each metal layer and uniform current distribution among the coils) whereas the inductance of mutually coupled inductors to [73]:

$$L_{\text{shunt}} = \frac{1}{\sum_{i=1, j=1}^N K_{ij}} \quad \text{Eq. (4.16)}$$

In practice, both the series and shunt topologies offer a Q improvement close to the theoretical limit due to the tight coupling available in the on-chip environment. These benefits, though, occur only at low frequencies where the above assumptions hold.

At high frequencies, both approaches are liable to reduce the Q factor over the case of a single layer coil due to the capacitive and substrate effects. The series connection suffers from high interwinding capacitance which lowers the self-resonance frequency, lowering the maximum operating frequency of the device. The shunt connection moves the devices closer to the substrate where capacitive current injection may dominate the loss of the device.

4.2.1.1 Shielding Structures

A shield with lower metal layers or polysilicon layers underneath the spiral inductor helps in blocking electromagnetic energy from coupling to the substrate [74]. While electrostatic shielding works well for capacitors and RF pads, especially at low frequencies, the shield must be patterned in the case of inductors so as to avoid or reduce the effects of Eddy currents. Due to the close proximity of the device and the shield, using solid metallization would allow “image” Eddy currents to flow which would produce an opposing magnetic field. This would reduce the device magnetic energy storage and hence the Q factor. A pat-

terned shield only allows shield currents to flow perpendicular to the conductive paths of a spiral inductor, thereby preventing the majority of eddy currents which flow parallel to the device.

At first glance, a patterned ground shield seems like an unalloyed good thing for improving the device Q . However, there are many other problems associated with such shields, such as dramatically reduced self-resonant frequency due to the capacitive nature of the structure. There are some second-order problems as well. Figure 4-8 shows the patterned ground shield realization to improve inductor Q .

Figure 4-8. Spiral inductor with patterned ground shield

4.3 Inductor Modeling Programs

There are some programs available in the market which do electromagnetic simulation to characterize a spiral. Other programs use a lumped element model to do the same. This section will provide a brief overview of some of them and shows how an accurate inductor model can be developed using these programs.

4.3.1 ASITIC

This is a program that is freely available from the University of California, Berkley website. In the words of the author, “ASITIC” [75] is a CAD tool that aids RF/microwave engineers to analyze, model, and optimize passive metal structures residing on a lossy conductive substrate”. This includes inductors, transformers, capacitors, transmission lines, interconnects and substrate coupling analysis.

ASITIC is an Unix based graphical program which runs under the X windows environment. Typing *asitic* on the shell prompt brings out a layout screen where the user can specify the geometry of the object under test. It supports different kinds of geometries like the square and even non-traditional shapes like the polygon. There are a series of simple commands that help the user layout the spiral and help one manipulate it.

The next important step is editing the technology file, which specifies the IC process. In the technology file, specifying the size of the FFT specifies the resolution of the analysis. Different kinds of simulations can be done and the relevant parameters like inductance, quality factor and self-resonant frequency determined at a particular frequency. The program is relatively fast and simple which gives a good first cut for the different design

parameters.

4.3.2 Agilent ADS

This is a complete suit from Agilent, which does different types of simulations. Momentum RF is a 2.5D electromagnetic simulator. It uses “method-of-moments” to break problem down into discrete elements using meshing. Inductor modeling is achieved by creating discrete elements that take account of the substrate properties [76]. The technology file for the process can be input and solved one time and reused with different geometries. This saves a lot of time when testing different geometries under a single process.

The spiral can be either specified by selecting from a large collection of standard geometries or the user can draw the spiral using traces. With this option the user has considerable room to test a wide variety of spirals and is not limited by the ones available in the library. The results can be observed either as Smith charts or any of the other standard formats. Animations of currents and charges help the user to interpret the results better. For example, effects such as current crowding can be observed visually and better understood.

The small disadvantage with this program seems to be the long simulation time depending on the resolution of the mesh used for analysis.

4.3.3 Lumped Model Simulators

There are a number of lumped element models that have been previously published [63,77,78]. Some of them model on a turn-by-turn basis while others do a segment-by-segment analysis. To the best of author’s knowledge, there is no commercial or released programs which use these models for simulations.

4.4 Inductor Design Methodology

In this section, a methodology to design and model an accurate and optimized inductor is described. The following steps are taken:

1. Run ASITIC to generate preliminary inductor layout, S-parameters, and a simple simulation model i.e. inductor subcircuit with parasitic. It also gives first approximation of inductor Q, inductance L and series resistance, R_s .
2. Simple lumped model from ASITIC is only good for a single frequency. For a large tuning range on-chip inductor based VCO designs, inductor model needs to be optimized to provide constant inductance, higher Q and minimum series resistance for a wide range of frequencies. This is achieved by using HPEESOF ADS tools which uses the simple model from ASITIC and develops a new and accurate wide-band model for the inductor.
3. HPEESOF ADS method of moments is used to obtain equivalent S-parameter matrix for the inductor. Momentum modeling is initiated by entering the substrate details such as shown in Figure 4-9 into the Momentum substrate model. Substrate model provides a link between layout editor with physical properties of the substrate. The S-parameter result from Momentum should be compared with those obtained from ASITIC for verification.
4. In many simulators, it is an advantage in terms of speed if a lumped element representation of the inductor is used.

5. Figure 4-9 shows such a lumped element representation based on physical effects [79].

A more universal solution is obtained by forming the lumped element equivalent circuit by using ADS optimizer to find correct values for each element. Advantage is that the lumped elements have physical meaning.

Figure 4-9. Spiral inductor lumped circuit model.

Some important design guidelines are:

- **Width of the metal conductor:** Wide metal conductors of an inductor with a fixed area results in a smaller inductance, as the inner turns contribute less to the inductance. The spiral traces should be as wide as possible until the skin effect becomes significant. The increase of the metal width results in a rise of Q because the resistance of the inductor decreases and the inductance remains the same.
- **Skin effect:** It causes non-uniform current flow in the inductor and center of the wide conductor is not used. High frequency resistance increase.

- **Minimum spacing between adjacent conductors:** The spacing between the metal lines should be as small as possible. It maximizes the positive mutual inductance and allows for the largest center hole. Increasing the spacing decreases mutual inductance. It also increases the series resistance and also the total area.
- **Hollow coil:** Due to the generation of eddy currents at high frequencies, the innermost turns of the coil suffer from an enormous increase in resistance and also deteriorates the overall quality factor of the coil. Therefore, it is necessary to use a hollow coil. From the analysis of several spirals designs extracted from [61] and [80], a good inner radius is approximately equal to the 25 to 40 percent of the outer radius.
- **Coil area:** At high frequencies, the magnetic field generated by the inductor induces currents in the high doping substrate which cause extra resistive loss and decrease in inductance value. Hence, limiting the size of the coil decreases magnetic field penetration into the substrate and cause less loss. For the case of low doping substrate, this effect is generally negligible.
- **Stack metal:** Reducing the resistance per length of inductor trace increases inductor Q. The task can be accomplished using a thicker track. In standard CMOS processes, inductor metal lines can be thickened by shunting metal layers. As the number of layers shunted becomes higher, the inductor resistance becomes smaller and the quality factor rises. The number of metal layers used to make a spiral depends on the CMOS process. It is recommended not to use the closest metal layer to the substrate, which reduces the inductor resonant frequency.

Following Table 4-1, summarizes the design guidelines for a planar spiral inductor as discussed above.

Table 4-1. Inductor design guidelines

			Q_{max}	L	f_{res}
Conductor thickness (t)	↑	⇒	↗	—	—
Conductor sheet resistance (R_{sh})	↑	⇒	↘	—	—
Insulator thickness (h)	↑	⇒	↗	—	↗
Substrate resistivity (ρ)	↑	⇒	↘↗	—	↗
Area	↑	⇒	↘	↗	↘
Number of turns (n)	↑	⇒	↘	↗	↘
Track width (w)	↑	⇒	↗	↘	↘
Multi-layer inductor, extra layer	↑	⇒	↘	↗	↘
↗: increase, ↘: decrease, —: almost constant, ↘↗: exhibits minimum					

4.5 Final inductor design

During the inductor design, the trade-off between inductor size and oscillator current drain also served as a guideline. Large valued inductors will reduce current drain in the oscillator. This happens because larger inductors have larger equivalent parallel resistances, R_{eq} . Larger values of R_{eq} are desirable because the active portion of the circuit will be required to generate less negative resistance to sustain oscillation and thus consume less current. However, as L is increased, its self-resonant frequency decreases because its parasitic capacitances also increase. Larger inductances will also decrease the oscillator tuning range. This occurs because a smaller tank capacitance is required to achieve the desired

oscillation frequency. As the tank capacitance becomes smaller, it gets swamped out by the parasitic capacitances. As was discussed earlier, larger area inductors will also have an increased substrate loss, since their magnetic fields penetrate deeper into the substrate. All these factors must be considered when designing the inductor. The feasibility of using a larger inductor is limited by the parasitics that will be associated with the active circuitry and the varactor tuning element.

First LC VCO has a target frequency of 2GHz and uses higher value of inductor (5nH) for its resonant circuit. The design and optimization of this inductor (5nH) is mainly based on empirical equations given in [58] and uses 0.25um CMOS-1P5M SPDV technology parameter. For 5nH inductor having dimensions of 230um*230um, metal width of 10um and spacing of 1.3um, series inductance, L_s , is found to be 5.63nH, series resistance of $14\ \Omega$ (see Appendix-A). This gives Q of 5.05 at 2GHz center frequency.

Other LC VCOs reported in this thesis have target frequency of 10GHz. The inductor used in these 10GHz VCOs has a smaller value (0.9nH). It is designed and optimized using the design methodology as given above. Figure 4-10, shows simulated broadband inductance curve against frequency and gives almost constant value of 0.9nH between 5GHz to 20GHz.

Figure 4-10. Simulated Inductor characteristic for VCO#2

Figure 4-11, shows the 0.9nH inductor Q value against frequency. It has peak of 10.5 at around 12GHz

Figure 4-11. Inductor Q plot versus frequency for VCO#2.

4.6 Varactor Design

4.6.1 Background

The term varactor is coined from a voltage-controlled capacitor or variable reactor and is a key component extensively used in microwave applications, which include bandpass filter [81], phase shifter [82], voltage-controlled oscillator (VCO) [83], mixer, non-linear transmission line, and frequency multiplier. A varactor is generally used as an element in an LC resonant tank so that the resonance frequency can be varied inversely proportional to the square root of the capacitance value. In the VCO applications, the applied bias voltage to the varactors determines the oscillation frequency through capacitance variation.

4.6.2 Performance Parameters

Like other components, varactors are characterized by a number of performance parameters. In this section, seven different performance parameters are presented and discussed. These parameters are: (i) capacitance tuning ratio (C_{max}/C_{min} -ratio), (ii) quality factor (Q), (iii) absolute capacitance value (C_{min} or C_{max}), (iv) CV-characteristic, (v) self resonance frequency (f_{SR}), (vi) flicker noise, and finally (vii) silicon area efficiency. Among these parameters, the C_{max}/C_{min} -ratio and Q are the most important. Other parameters of interest are the absolute capacitance value, the CV-characteristic, and the self resonance frequency, while flicker noise and silicon area efficiency is considered to be of less importance.

4.6.2.1 Capacitance Tuning Ratio (C_{max}/C_{min} -ratio)

Perhaps the most important performance parameter is the capacitance tuning ratio, as it is directly related to the functionality of the varactor. The capacitance tuning ratio is usually designated by the C_{max}/C_{min} -ratio, where C_{min} and C_{max} are the minimum and maximum capacitance, respectively. The capacitances C_{min} and C_{max} are measured at the lower and upper limit of the tuning voltage. Usually, the maximum capacitance C_{max} is obtained at the lower limit of the tuning voltage, while C_{min} is measured at the upper limit. Obviously, a large C_{max}/C_{min} -ratio is desired, as this results in a large frequency tuning range.

4.6.2.2 Quality Factor (Q)

Another very important performance parameter is the quality factor (Q). This is defined for varactors and other passive components as [74]:

$$Q = 2\pi \cdot \frac{|\text{maximum stored capacitive energy} - \text{maximum stored inductive energy}|}{\text{energy dissipated per cycle}}$$

Eq. (4.17)

where a sinusoidal excitation (voltage or current) is assumed to be applied to the component.

From Eq. (4.17) it is seen, that Q is a relative measure of the inherent losses, which must be as small as possible. As the inherent losses are included in the denominator, a large Q is desirable.

The inherent losses are schematically represented by resistors. As indicated by the simplified equivalent circuits in Figure 4-12, the resistors are connected with an ideal varactor (tunable capacitor) in either parallel or series, or alternatively as a combination of both.

Figure 4-12. Simplified equivalent circuits for a varactor including resistors representing inherent losses.
 (a) Parallel equivalent. (b) Series equivalent. (c) Combined parallel and series equivalent.

For a capacitor operated far below the self resonance frequency, the stored inductive energy is negligible, and Eq. (4.17) then reduces to:

$$Q \approx 2\pi \cdot \frac{\text{maximum stored capacitive energy}}{\text{energy dissipated per cycle}} = 2\pi \cdot \frac{E_{C, \max}}{E_{\text{dis}}} \quad \text{Eq. (4.18)}$$

The maximum energy stored in a capacitor, $E_{C, \max}$ is given by:

$$E_{C, \max} = \frac{1}{2} \cdot C \cdot V_{\text{peak}}^2 \quad \text{Eq. (4.19)}$$

where V_{peak} is the peak voltage over the capacitor.

For the parallel equivalent circuit shown in Figure 4-12(a), the energy dissipated per cycle

$$\text{is:} \quad E_{\text{dis}} = \frac{V_{\text{peak}}^2}{2 \cdot R_p} \cdot T = \frac{V_{\text{peak}}^2}{2 \cdot R_p} \cdot \frac{1}{f} \quad \text{Eq. (4.20)}$$

where T is the period time, and $f = 1/T$ is the frequency of the applied signal.

Thus, by inserting Eq. (4.19) and Eq. (4.20) into Eq. (4.18), Q of the circuit in Figure 4-12(a) is found to be:

$$Q_p = 2\pi \cdot \frac{E_{C, \max}}{E_{\text{dis}}} = 2\pi \cdot \frac{\frac{1}{2} \cdot C \cdot V_{\text{peak}}^2}{\frac{V_{\text{peak}}^2}{2 \cdot R_p} \cdot \frac{1}{f}} = R_p \cdot \omega \cdot C_p \quad \text{Eq.(4.21)}$$

where the suffix “p” refers to parallel resonance, and $\omega = 2\pi \cdot f$ is the angular frequency.

As indicated in Figure 4-12(a), Q_p can also be determined from Y_{in} by using the expression:

$$Q_p = \frac{|\text{Im}(Y_{\text{in}})|}{\text{Re}(Y_{\text{in}})} = \frac{\omega \cdot C_p}{G_p} = R_p \cdot \omega \cdot C_p \quad \text{Eq. (4.22)}$$

which gives the same result as Eq. (4.21). By taking the absolute value of the imaginary term, the first part of the expression also applies to inductors.

For the series equivalent circuit shown in Figure 4-12(b), the maximum stored energy and dissipated energy per cycle are:

$$E_{C, \max} = \frac{1}{2} \cdot C_s \cdot V_{\text{peak}}^2 = \frac{1}{2} \cdot C_s \cdot \left(\frac{1}{\omega \cdot C_s} \cdot I_{\text{peak}} \right)^2 \quad \text{Eq. (4.23)}$$

$$E_{\text{dis}} = R_s \cdot \frac{I_{\text{peak}}^2}{2} \cdot T = R_s \cdot \frac{I_{\text{peak}}^2}{2} \cdot \frac{1}{f} \quad \text{Eq. (4.24)}$$

Thus, by inserting Eq. (4.23) and Eq. (4.24) into Eq. (4.18), Q for the circuit in Figure 4-12(b) is found to be:

$$Q_s = 2\pi \cdot \frac{E_{C, \max}}{E_{\text{dis}}} = 2\pi \cdot \frac{\frac{1}{2} \cdot C_s \cdot \left(\frac{1}{\omega \cdot C_s} \cdot I_{\text{peak}} \right)^2}{R_s \cdot \frac{I_{\text{peak}}^2}{2} \cdot \frac{1}{f}} = \frac{1}{R_s \cdot \omega \cdot C_s} \quad \text{Eq. (4.25)}$$

where the suffix “s” refers to series resonance.

As indicated in Figure 4-12(b), Q_s can also be determined from Z_{in} by using the expres-

sion:

$$Q_s = \frac{|\text{Im}(Z_{in})|}{\text{Re}(Z_{in})} = \frac{|(-1)/(\omega \cdot C_s)|}{R_s} = \frac{1}{R_s \cdot \omega \cdot C_s} \quad \text{Eq. (4.26)}$$

which gives the same result as Eq. (4.25).

The equivalent circuits in Figure 4-12(a) and (b) are sufficient for determination of Q based on measurement of Y_{in} or Z_{in} , but they can not be used as general models. In reality, the measured loss consists of series losses as well as parallel losses. The series losses account for substrate losses and losses in interconnecting metal layers, while the parallel losses account for dielectric losses. Hence, the equivalent circuit in Figure 4-12(c) is a better model of a real varactor, but not necessarily an exact model.

The total Q , Q_{tot} for the equivalent circuit in Figure 4-12(c) can be determined from the total series impedance Z_{tot} , which is given by:

$$Z_{tot} = R_{tot} + j \cdot X_{tot} = \frac{R_s(1 + \omega^2 \cdot C^2 \cdot R_p^2) + R_p}{1 + \omega^2 \cdot C^2 \cdot R_p^2} - j \frac{\omega \cdot C \cdot R_p^2}{1 + \omega^2 \cdot C^2 \cdot R_p^2} \quad \text{Eq. (4.27)}$$

By inserting the expression for R_{tot} and X_{tot} into Eq. (4.26), the following expression for Q_{tot} is obtained:

$$Q_{tot} = \frac{\omega \cdot C \cdot R_p^2}{R_s(1 + \omega^2 \cdot C^2 \cdot R_p^2) + R_p} \quad \text{Eq. (4.28)}$$

Assuming $Q_p = R_p \cdot \omega \cdot C \gg 1$, Eq. (4.28), simplifies to:

$$\frac{1}{Q_{tot}} = R_s \cdot \omega \cdot C + \frac{1}{R_p \cdot \omega \cdot C} = \frac{1}{Q_s} + \frac{1}{Q_p} \quad \text{Eq. (4.29)}$$

Eq. (4.29) expresses that the total Q is calculated in approximately the same method as the

total resistance of two resistors in parallel. Hence, if one of the quality Q_s or Q_p is much smaller than the other, it dominates the total Q . Eq. (4.29), is an important tool for design of varactors, where series losses must be weighed up against parallel losses.

4.6.2.3 CV-characteristic

For varactors used to tune the VCO frequency in PLL frequency synthesizers, the capacitance versus tuning voltage characteristic (CV-characteristic) is important. Ideally, the VCO frequency tuning must be a linear function of the tuning voltage, as indicated in Figure 4-13. With a linear frequency tuning, a constant VCO gain (K_{vco}) is obtained. This is important to ease the loop design and to obtain a stable loop with constant loop performances irrespective of the output frequency.

Figure 4-13. Ideal frequency tuning.

To find a way to evaluate the CV-characteristic of a given varactor, the lossless parallel LC-resonance circuit in Figure 4-14 is used. The capacitor C_p in Figure 4-14 represents fixed parasitic capacitances, which cannot be avoided in a real LC-tank. C_p is unwanted, as it reduces the C_{max}/C_{min} - ratio available from the varactor.

Figure 4-14. Parallel LC-tank

The resonance frequency f_o of the LC-tank, shown in Figure 4-14, is given by:

$$f_o = \frac{1}{2\pi\sqrt{L(C_p + C_v(V_t))}} \quad \text{Eq. (4.30)}$$

where $C_v(V_t)$ is the varactor capacitance as a function of tuning voltage V_t . To obtain linear frequency tuning, the VCO output frequency must fulfill the requirement:

$$f_o = f_{\min} + K_{\text{vco}}(V_t - V_{\min}) \quad \text{Eq. (4.31)}$$

Combining Equations (4.30) and (4.31),

$$\frac{1}{2\pi\sqrt{L(C_p + C_v(V_t))}} = f_{\min} + K_{\text{vco}}(V_t - V_{\min}) \quad \text{Eq. (4.32)}$$

Maximum varactor capacitance ($C_{\max}$) is used to remove C_p , Eq. (4.32) thus becomes:

$$\frac{1}{2\pi\sqrt{L(C_p + C_{\max} + C_v(V_t) - C_{\max})}} = f_{\min} + K_{\text{vco}}(V_t - V_{\min})$$

or

$$L(C_p + C_{\max} + C_v(V_t) - C_{\max}) = \frac{1}{4\pi^2(f_{\min} + K_{\text{vco}}(V_t - V_{\min}))^2} \quad \text{Eq. (4.33)}$$

Also, from Eq. (4.30)

$$L(C_p + C_{\max}) = \frac{1}{4\pi^2 \cdot f_{\min}^2} \quad \text{Eq. (4.34)}$$

Using Eq. (4.34) in Eq. (4.33) and re-arranging we get:

$$C_v(V_t) = C_{\max} - \frac{K_{\text{vco}}^2(V_t - V_{\min})^2 + 2 \cdot K_{\text{vco}} \cdot f_{\min}(V_t - V_{\min})}{4\pi^2 \cdot L \cdot f_{\min}^2(K_{\text{vco}}^2(V_t - V_{\min})^2 + 2 \cdot K_{\text{vco}} \cdot f_{\min}(V_t - V_{\min}) + f_{\min}^2)} \quad \text{Eq. (4.35)}$$

Above Eq. (4.35), provides CV characteristics of a MOS varactor in terms of $C_{\max}$ and $f_{\min}$.

4.6.2.4 Self Resonance Frequency

Figure 4-12(c) which shows equivalent model for varactor does not hold true on GHz frequency range. A series inductor, L , should be included as shown in Figure 4-15, to account for the interconnects used at gate, source and drain terminals within the varactor layout.

Such high frequency interconnect parasitic inductance, L , is expected to be a small value, however, it provides series resonance with tunable capacitor and determines the self-resonance frequency, f_{SR} , of the varactor. It is desirable to keep f_{SR} as high as possible to prevent it from interfering with varactor function. As the capacitance C is tunable, f_{SR} is a function of tuning voltage.

Figure 4-15. Varactor Model including the series inductor, L

4.6.3 Varactor Types

In CMOS technology, different options exist for the implementation of varactors [84, 85, 86]. There are two main types of varactors available in CMOS technology. These types are the PN-junction and the MOS Capacitance. In the following two subsections, both the junction type and the MOS type are briefly described.

4.6.3.1 PN-Junctions

The PN-junction is well known from discrete circuit design, where it apparently is the only varactor type available. In the discrete case, the PN-junction is better known as capacitance diode or varactor diode. In standard CMOS technology, the PN-junction includes a number of subtypes among which the p⁺-to-n-well junction has the highest Q. In Figure 4-16, the cross-section of the PN-Junction varactor is shown.

Figure 4-16. Cross-section of PN-Junction varactor with equivalent circuit model.

The resistor in series in the above equivalent model represent the series losses associated with the signal path through the silicon, and hence represents the main contribution to the inherent loss. The varactor function is achieved by applying a variable reverse bias voltage (V_R) across the anode (A) and cathode (C) terminals.

The p⁺-to-n-well junction utilizes the capacitance associated with the depletion region between the p⁺ -implementation and the n-well. The main contribution to losses, is the signal path through the n-well, where the majority carriers are electrons and hence, this subtype is expected to have a relatively high Q. This type can easily implementable in standard

CMOS and does not impose any constraints on the process. Further, both the anode and cathode terminals can be used for application of bias voltages.

One disadvantage of junction varactors is that they can become forward biased by large amplitude voltage swings.

4.6.3.2 MOS Capacitor Types

MOS capacitor is well known and has wide use among integrated circuit designers. Its most common use is in de-coupling in analog applications at low frequencies. This type of capacitor provides higher capacitance density (i.e. capacitance per area) as compared to MIM types. One drawback is the voltage dependency, which makes the MOS capacitor less useful for large signal operation. However, such voltage dependency is useful in the varactor applications. In Figure 4-17, the cross-section of four different MOS subtypes are shown. The resistors represent the main losses associated with the signal path through the silicon. In contrast to the junction subtypes, none of the MOS subtypes have grounded terminals and hence any constraints with respect to application of bias voltages. For all four MOS subtypes, the varactor function is achieved by applying a variable bias voltage across the gate terminal (G) and the combined drain/source terminal. Depending on the specific MOS type, the mode of operation is changed between depletion and strong inversion or between depletion and deep accumulation. In depletion mode only bound charges are present in the silicon just beneath the gate, while free carriers totally dominate in both strong inversion and deep accumulation mode. In both modes of operation, the capacitance between the gate and drain/source terminal reaches the maximum value C_{max} . This capacitance is approximately equal to the gate oxide capacitance C_{ox} of the MOS transistor.

Figure 4-17. Cross-section for different subtypes of the MOS capacitance.

(a) Standard Mode NMOS.

(b) Standard Mode PMOS.

(c) Accumulation Mode NMOS.

(d) Accumulation Mode PMOS.

The first MOS subtype is the Standard Mode NMOS. The main contribution to losses, is the signal path through the inversion layer (channel), where the majority carriers are electrons. Hence, this subtype is expected to have a relatively high Q . Only one publication is found on the Standard Mode NMOS varactor [87].

The second MOS subtype is the Standard Mode PMOS. The main contribution to losses, is the signal path through the inversion layer (channel), where the majority carriers are holes. Hence, this subtype is expected to show lower Q -values than its n-channel counter part. This type of MOS varactor has been treated in three papers [84, 88, 89].

The third MOS subtype is the Accumulation Mode NMOS varactor. This type of MOS varactor has attracted a great deal of attention and is treated in number of publications [90, 91, 92]. The Accumulation Mode NMOS structure is similar to an n-channel MOSFET with the exception of being fabricated in an n-well instead of the normal p-substrate. The Accumulation Mode NMOS varactor has advantage compared to the standard mode NMOS varactor. This advantage comes from n-well, which provides a good isolation against noise and interfering signals induced into the substrate by neighboring digital fast switching circuits. Also n-well eliminates the parasitic pn-junction capacitances at source and drain that would otherwise limit the tuning range.

The fourth MOS subtype is the Accumulation Mode PMOS. It is an alternative structure using p-channel MOSFET in a p-well/substrate has inferior quality due to lower mobility of holes. Accumulation Mode PMOS is only available in a twin well process [90].

4.6.4 Varactor Design Methodology and Layout

Since in this thesis, there are three LC tank VCOs have been implemented, which are:

1. VCO#1: 2GHz Complementary VCO with junction varactor in 0.25um standard digital CMOS technology
2. VCO#2: 10GHz Complementary VCO with Accumulation Mode MOS varactor in deep sub-micron CMOS technology.
3. VCO#3: 10GHz wide-tuning Inductor-switched VCO in deep sub-micron CMOS technology.

VCO#1 and VCO#2 uses varactors for fine tuning. VCO#3 uses inductor-switching for tuning purpose and does not contain any varactor. Implementation of both types of varac-

tors i.e. junction and MOS varactor for large Cmax to Cmin ratio, low series resistance and hence, high Q are discussed below:

4.6.4.1 PN-Junction Varactor Implementation

In Figure 4-16, model for p+-to-nwell junction varactor is shown. A snapshot of its layout is shown in Figure 4-18, where p+ diffusion is surrounded by n-well and all such tiny junction varactors are connected in parallel.

Figure 4-18. Snapshot of p+-to-n-well junction varactor layout

The capacitance is from the bottom side walls of the p+-to-n-well junction and side walls. Parasitic series resistance is from the n-well resistance between p+ and n+ diffusions as well as contact and metal series resistance. The series resistance, R_{var} , can be approximated as [93, 94]:

$$R_{var} = R_{nw, sheet} \left(\frac{L}{W} \times \frac{1}{2} + \frac{1}{L \times 28.6} \right) \times \frac{1}{N} \quad \text{Eq. (4.36)}$$

where W is the spacing between p+ and n+ diffusions, L is the length of p+ diffusion, N is the number of unit junction varactor cells, and $R_{nw, sheet}$ is the sheet resistance of n-well $R_{nw, sheet} \sim 580 \Omega/\square$. [95])

In order to reduce the series resistance and maximizing the varactor Q, N should be as large as possible for a given capacitance resulting in W to be as small as possible. Q of this varactor is given as:

$$Q_{\text{var}} = \frac{1}{\omega R_{\text{var}} C_{\text{var}}} \quad \text{Eq. (4.37)}$$

From Appendix-A (b), change in total capacitance C_{var} is estimated to be 0.83pF and from the varactor layout dimension of $L=5\mu\text{m}$, $W=1\mu\text{m}$, estimated R_{var} from Eq. (4.36), is 3.48Ω . This will give, Q_{var} , from Eq. (4.37), to be 27.55 at 2GHz.

Figure 4-19. Inter-digitized layout scheme for PN junction varactors

Inter-digitized layout scheme for two back-to-back PN junction varactors in the differential LC tank VCO will further reduce series resistance from p+ to n+ diffusion area and hence, will improve its Q.

4.6.4.2 MOS Varactor Implementation

The MOS varactor design in the 10GHz LC-Tank VCO (VCO#2) in this thesis is tightly associated with the overall LC tank circuit. The starting point for this design is a tank circuit with $L = 1\text{nH}$ and $C = 250\text{fF}$ which resonates near 10GHz. The total tank capacitance is formed by the combination of the variable tuning capacitance (varactor) and parasitic (fixed) capacitances associated with the circuit layout, including the inductors.

The varactors in the LC-Tank VCO is implemented in a differential fashion by connecting two identical Accumulation Mode (Accumulation Mode) NMOS varactors back-to-back in series as shown in the Figure 4-20. The common-node “vg” on a properly balanced circuit provides a virtual ground where a tuning voltage can be applied through a resistor or a RF choke.

Figure 4-20. Accumulation-Mode NMOS Varactors implementation.

The accumulation-mode varactor has higher capacitance per unit area, higher quality factor and high tuning range (increases with technology scaling) compared to reverse-biased PN junction and MOS depletion/inversion varactors [11]. The basic trade-off is between tuning range and quality factor. Shorter gate lengths improves quality factor by reducing n-well series resistance but decreases the tuning by increasing the ratio of fixed overlap capacitance to the variable capacitance.

Figure 4-21. A top view, a cross section and an equivalent circuit of the Accumulation mode NMOS varactor structure.

Figure 4-21, shows a top view, a cross section and an equivalent circuit model of an Accumulation mode NMOS varactor test structure. Top and bottom plates of the varactor are formed with silicided polysilicon and n-well, and are separated by a gate oxide (SiO_2) layer. C_{pad} and R_{psub} represent parasitic capacitance and resistance associated with probe pads of the test structure. Since the gate oxide layer is very thin (thickness of ~ 17 nm in a typical standard CMOS process), the capacitor has a high intrinsic capacitance/area especially if it is biased in the accumulation region. Because of this, the structure can also have a high ratio between capacitance and parasitic capacitance associated with the n-well-to-substrate junction. If the capacitor is not biased in the accumulation, the capacitance will decrease by a factor of around two due to formation of a depletion region under the gate oxide [99].

During the initial design of the oscillator it was assumed that the Accumulation Mode NMOS varactor would have a quality factor of approximately 30. The varactor was actually designed while the oscillator circuit was laid out. The layout geometry of the varactor determines its Q. The Q of a MOS varactor with a series resistance is defined as:

$$Q = \frac{1}{\omega_0 R_s C} \quad \text{Eq. (4.38)}$$

When the MOS gate and channel are considered as an RC transmission line, and the gate is contacted on both ends of the channel, the intrinsic gate resistance is given by [97]:

$$R_g = \frac{1}{12} \frac{W}{L} R_{\text{poly}, \square}. \quad \text{Eq. (4.39)}$$

This expression is valid only for the polysilicon over the active region of a device. The series resistance (R_s) originates from resistances of the silicided polysilicon gate, n-well, vias, contacts (R_{cont}) and metal lines. Excluding the via, metal and contact resistances, and gate-bias dependence of the n-well resistance [93], the series resistance of the varactors can be approximated as [98]:

$$R_s = \frac{1}{12} \times \frac{1}{N} \times \left(R_{\text{nw}, \square} \times \frac{L}{W} + R_{\text{poly}, \square} \times \frac{W}{L} \right) \quad \text{Eq. (4.40)}$$

where N is the number of gate fingers, L and W are the length and width of the fingers as shown in the Figure 4-21, and $R_{\text{nw}, \square}$, $R_{\text{poly}, \square}$ are the sheet resistance of the n-well and silicided polysilicon gate layers, respectively. For a required variable capacitance and thus an MOS varactor area A, N is equal to $A/(L \times W)$, putting this into Eq. (4.40), R_s can be expressed as a function of L and W:

$$R_s = \frac{1}{12 \times A} \times (R_{\text{nw}, \square} \times L^2 + R_{\text{poly}, \square} \times W^2) \quad \text{Eq. (4.41)}$$

Since $R_{\text{nw}, \square}$ is much larger compared to $R_{\text{poly}, \square}$, the $R_{\text{nw}, \square} \times L^2$ term typically dominates the total series resistance. When W/L ratio is large, $R_{\text{nw}, \square} \times L^2$ could become

comparable to $R_{\text{poly}, \square} \times W^2$. To minimize R_s , both L and W need to be as small as possible. Using Eq. (4.38), quality factor of the MOS varactor can be expressed as

$$Q = \frac{1}{\omega_0 R_s C} = \frac{12}{\omega \times c_{\text{unit}} \times (R_{\text{nw}, \square} \times L^2 + R_{\text{poly}, \square} \times W^2)} \quad \text{Eq. (4.42)}$$

where ω is the frequency and c_{unit} is the intrinsic capacitance divided by area. When the minimum dimensions of L and W are used, Q is maximum. However, penalties are larger overall required area and n-well to substrate parasitic capacitance because of an increased number of contacts. As stated, the contact resistance are not included in the analysis since they are typically small ($=R_{\text{contact}} / N_c$, where R_{contact} is the resistance of a single contact and N_c is the number of contacts). Since small devices can only support a single contact rather than the preferred larger array of contacts [99], the series resistance will be dominated by the contact resistances.

During the tank circuit design phase, Eq. (4.40) was simply used as a guideline. The gate resistance was estimated to ensure that the design led to a reasonable Q . To make an optimum layout of the Accumulation mode NMOS varactor, three parameters must be considered. These are (i) gate length, (ii) width of gate finger, and (iii) resistance associated with unit cell interconnection. The varactors used in the VCO design were realized using the minimum gate length allowed in the process technology. The width of each gate finger was chosen to be 5 μm , which represents a compromise between quality factor, varactor size, and parasitics. Each of the two series varactors consists of 2 parallel devices with 10 fingers each.

Figure 4-22, shows the layout of the varactor along with a detailed view of the gate and contact arrangement. Notice that the gate polysilicon is contacted on each end of the device. Also notice that in order to reduce the resistance of the polysilicon contacts two rows of

contacts are used. The contacts are placed at minimum distance allowed under the process technology rules. The entire structure is placed in a common n-well.

Figure 4-22. A high-Q accumulation mode varactor layout

The relevant contact and sheet resistances necessary to calculate the Q of this structure are given in the process technology design rules. By using Eq. (4.41) for each varactor, R_s was calculated to be 2.8Ω . From Figure 4-23, the varactor capacitance varies from 120fF to 240fF. If the tuning range extends from 10GHz to 11GHz (as was expected from simulation), Eq. (4.42) predicts that the Q of the varactor will vary from 25 to 40, respectively. Figure 4-23 shows a plot of the simulated total varactor capacitance versus the control voltage. This C-V curve was generated using a transient simulation in HSpice.

Figure 4-23. CV characteristic of the designed Varactor.

4.7 Summary

In this chapter, the design methodology for both passive components of the VCO resonant tank circuit is presented. Different inductor geometry with loss mechanism are discussed. It has been demonstrated that the inductors can be designed using empirical equations and more accurately by using state-of-the-art tools. Comparison between PN-junction varactor and MOS varactors are made. Based on the methodology and guideline both inductor and varactors have been designed and optimized for maximum Q for the VCOs.

5 Design and Implementation of Monolithic LC-Tank Oscillators

5.1 Introduction

In the previous chapter the design and methodology of both a monolithic inductor and varactor are presented. This chapter begins with a concise review of existing phase noise models for the oscillator. And based on these models and in the light of the oscillator theory presented in chapter 3, three LC tank VCOs (briefly described in section 4.6.4), each utilizing different types of tuning method, have been designed. All three VCOs have been implemented in sub-micron standard CMOS technology ($f_t > 30$ GHz) using HSpice simulator in Cadence environment. This chapter includes simulation, measurement and layout issues of the LC-tank VCO. Layouts of the design is done using Cadence IC design tool *Virtuoso* and design is fabricated by Taiwan Semiconductor Manufacturing Company (TSMC) through Canadian Microelectronics Corporation (CMC). As packaging models for RFICs were not available at frequencies above 1.5 GHz through CMC, hence direct wafer probing technique was employed.

The design of monolithic VCOs in standard CMOS processes has been the subject of several recent research efforts. Phase noise and frequency tuning range are key performance parameters of high-frequency voltage-controlled oscillators (VCOs). An LC VCO is the

architecture of choice in high-speed SERDES design since its center frequency is mainly set by the values of the LC tank as opposed to a ring-VCO, which relies on the transistor delay properties to set its speed. In addition to the speed advantage, an LC VCO also exhibits its lower intrinsic phase noise because of higher Q provided by the resonance load, which is desirable since the VCO phase noise reduces the jitter tolerance margin of the CDR and increases the jitter generation in the serial output of the transmitter [17].

5.2 Review of Existing Phase Noise Models

It is possible to analyze phase noise in the frequency domain or in the time domain. Both analysis are equivalent due to the duality between the frequency and time domains. For ring oscillators, VCO designers like to use a time domain analysis. Hence, the notion of phase noise is translated into jitter and is common to represent the jitter in a histogram. However, for LC oscillators, the frequency domain analysis is more intuitive. Indeed, for ring oscillators, the frequency of oscillation is not obvious as for LC oscillators. Besides, VCO designers like to refer to ring oscillators as delay cells, which implies a time constant rather than a frequency.

The modeling of frequency instabilities has been the subject of numerous studies in different disciplines. Phase noise in oscillators has been studied extensively [100,101,102,103,104]. Effects such as nonlinearity and periodic variation of the circuit parameters make the analysis of phase noise quite difficult. More rigorous analysis of oscillators is still a topic of active research [110]. This section starts with a brief review of some of the previous work used to analyze the effect of the noise sources present in the oscillator. There are two major approaches have been considered for tuned tank oscillator phase noise

analysis: LTI (linear time invariant) and LTV (linear time variant). Both approaches have their merits and de-merits and are reviewed below:

5.2.1 Groszkowski's Reactive Balance Model:

Groszkowski, perhaps, the first person who did extensive analysis on oscillators. In 1934, he observed that the steady-state oscillation frequency and the natural resonator frequency, which tunes the oscillator, do not match very often [106]. He found that the discrepancy arises because the active device in the oscillator drives the resonator with a harmonic-rich waveform. The harmonics will flow into the lower impedance capacitor Figure 5-1 and upset the exact reactive power balance between the L and the C required for steady state. Now the frequency of oscillation must shift down until the reactive power in the capacitor due to the fundamental and all harmonics.

Figure 5-1. Reactive power balance phenomenon for steady state oscillation

The shift, $\Delta\omega$, is given by:

$$\frac{\Delta\omega}{\omega_0} = \frac{1}{2Q^2} \cdot \sum_{n=2}^{\infty} \frac{n^2(1-n^2)}{(1-n^2)^2 + \frac{n^2}{Q^2}} \cdot m_n^2 \quad \text{Eq. (5.1)}$$

where m_n is the normalized level of the n^{th} harmonic, $\Delta\omega$ is the sum of all negative terms, which means that oscillation frequency slows down with more harmonic content.

Groszkowski also describes a method of reactive power balance of harmonics [107], in which the reactive components in the active devices are captured by measuring the area “ k ” enclosed by hysteresis in the dynamic negative resistance curve, Figure 5-2.

$$\frac{\Delta\omega}{\omega_0} = \frac{-k}{2Q^2\omega_0L} + \frac{1}{2Q^2} \sum_{n=2}^{\infty} \frac{n^2(1-n^2)}{(1-n^2)^2 + n^2/Q^2} \cdot m_n^2 \quad \text{Eq. (5.2)}$$

Figure 5-2. Negative resistance curve hysteresis

This technique is the basis of “harmonic balance” techniques used in modern state-of-the-art tool, HPEESOF -ADS, to predict phase noise of an oscillator.

5.2.2 Leeson's Model:

By far, the most well-known model for a linear feedback oscillator is presented by Leeson and is based on LTI approach. He showed that the basic requirement on an oscillator noise model is that it depicts clearly the relationship of the spectrum of the phase $S_{\phi}(\omega_m)$ to the known or expected noise and signal levels and resonator characteristics of the oscillator [108]. Assume a single resonator feedback network of fractional bandwidth $\frac{2B}{\omega_0} = \frac{1}{Q}$, where Q is the operating, or loaded, quality factor. For small phase deviations within the feedback half-bandwidth $\frac{\omega_0}{2Q}$, a phase error at the oscillator input due to noise or parameter variations results in a frequency error determined by the phase-frequency relationship of the feedback network, $\Delta\theta = \frac{2Q\dot{\phi}}{\omega_0}$. Thus, for modulation rates less than the half-bandwidth of the feedback loop, the spectrum of the frequency $S_{\dot{\phi}}(\omega)$ is identical to the spectrum of the spectrum of the uncertainty of the oscillator input phase due to noise and parameter variations. This uncertainty will be denoted $\Delta\theta(t)$, and its two-sided power spectral density $S_{\Delta\theta}(\omega_m)$. He further described that for a physical oscillator the spectrum $S_{\Delta\theta}(\omega_m)$ of the input phase uncertainty $\Delta\theta(t)$ will have two principal components: phase uncertainties resulting from additive white noise at frequencies around the oscillator frequency and noise at other frequencies mixed into the pass band of interest by nonlinearities. The second component is due to variations at RF frequencies which affect the phase such as variations in the phase shift of a transistor due to carrier density fluctuations in the base resistance. For a feedback oscillator with an effective noise figure F , the two-sided power spectral density $S_{\Delta\theta}(\omega_m) = \frac{2FkT}{P_s}$ where P_s is the signal level at oscillator active element input.

Leeson gave a composite expression which describes the total power spectral density of oscillator input phase error as:

$$S_{\phi}(\omega_m) = \frac{2FKT}{P_s} \left[1 + \left(\frac{\omega_o}{2Q\omega_m} \right)^2 \right] \quad \text{Eq. (5.3)}$$

Figure 5-3. The spectrum of the phase noise.

5.2.3 Razavi's extension to Leeson's Model:

Further insight into the Leeson model is obtained by modeling oscillator as a two port linear system [109]. To analyze phase noise, an oscillator is considered as a feedback system and each noise source as an input, as shown in Figure 5-4.

Figure 5-4. Simplified two-port model of an oscillator.

The phase noise observed at the output is a function of:

- sources of noise in the circuit, and
- how much the feedback system rejects various noise components.

Noise power spectral density for such linear system is shaped by Eq. (5.4) [110] and is shown in Figure 5-5:

$$\left| \frac{Y}{X} [j(\omega_o + \Delta\omega)] \right|^2 = \frac{1}{(\Delta\omega)^2 \left| \frac{dH}{d\omega} \right|^2} \quad \text{Eq. (5.4)}$$

Figure 5-5. Noise shaping in oscillator.

If $H(j\omega) = A(\omega) \exp[j\Phi(\omega)]$ then $\frac{dH}{d\omega} = \left(\frac{dA}{d\omega} + jA \frac{d\Phi}{d\omega} \right) \exp(j\Phi)$ Eq. (5.5)

since at $\omega \approx \omega_o$, $A \approx 1$, and $\left. \frac{dA}{d\omega} \right|_{\omega_o} \approx 0$.

Combining Eq. (5.4) and Eq. (5.5), will give similar form of Leeson's equation [108] as:

$$\left| \frac{Y}{X} [j(\omega_o + \Delta\omega)] \right|^2 = \frac{1}{4Q^2} \left(\frac{\omega_o}{\Delta\omega} \right)^2 \quad \text{Eq. (5.6)}$$

Eq. (5.6), includes the effect of noise on both the amplitude and the phase of the carrier.

This expression also shows the dependence of the output noise upon the Q of the tank, the center frequency, and the offset frequency.

5.2.4 Craninckx-Steyaert Model:

Phase noise aspects of LC-tuned oscillators are further analyzed in [111]. A general formula based on LTI approach has been developed. Concept of effective resistance and capacitance has been introduced which provide more physical meaning to the oscillator phase noise analysis.

An LC-tuned oscillator is modeled as linear feedback circuit as shown in Figure 5-6:

Figure 5-6. Basic LC-tuned oscillator model with parallel resistor R_p .

The LC-tank of the above model includes all parasitic resistances, for example, R_c is representing series resistance associated with capacitor C , R_l series resistance of inductor L and output resistance of the transconductor is modeled as R_p .

Since the model is linear, which means the amplitude of the oscillation is assumed limited such that the amplifier operates in its linear region and low frequency noise does not contribute to the phase noise. However, in a nonlinear circuit, low frequency noise can be upconverted to the oscillation frequency due to the nonlinear effects.

All the parasitic resistances can be reduced to one equivalent resistance R_{eff} , and the above equations are summarized as:

$$R_{\text{eff}} = R_c + R_l + \frac{1}{R_p \cdot (\omega_o C)^2} \quad \text{Eq. (5.7)}$$

Effective noise density at frequencies very close to the center frequency is given by:

$$dV_{\text{out},R}^2\{\Delta\omega\} = kT \cdot R_{\text{eff}} \cdot \left(\frac{\omega_o}{\Delta\omega}\right)^2 \cdot df \quad \text{Eq. (5.8)}$$

The Q-factor of the LC-tank can also be expressed as a function of this effective resistance

and is given as:
$$Q = \frac{1}{R_{\text{eff}}(\omega_o C)} \quad \text{Eq. (5.9)}$$

The active element in the oscillator also introduces noise and is modeled by an output current source $di_{G_M}^2$ as:

$$di_{G_M}^2 = 4kT \cdot F_{G_M} \cdot G_M \cdot df \quad \text{Eq. (5.10)}$$

where G_M is given by $G_M = R_{\text{eff}} \cdot (\omega_o C)^2$ Eq. (5.11)

and F_{G_M} is the noise factor of the amplifier used.

The output noise due to the active element is given as:

$$dV_{\text{out},G_m}^2\{\Delta\omega\} = kT \cdot R_{\text{eff}} \cdot F_{G_M} \cdot \left(\frac{\omega_o}{\Delta\omega}\right)^2 \cdot df \quad \text{Eq. (5.12)}$$

As in the real circuit only a part of the output signal is fed back into the amplifier, so the transconductance needed must be higher to make enough negative resistance. This is represented in equation by an excess noise factor, α , and is defined by A, where $A = \alpha \cdot F_{G_M}$.

Thus Eq. (5.12) is concluded as:

$$dV_{\text{out}}^2\{\Delta\omega\} = kT \cdot R_{\text{eff}} \cdot [1 + A] \cdot \left(\frac{\omega_o}{\Delta\omega}\right)^2 \cdot df \quad \text{Eq. (5.13)}$$

The phase noise given by Eq. (5.13) can be divided into two parts: first part with $R_{\text{eff}} \cdot 1$, which shows the contribution of the resistances of the LC-tank and second part with $R_{\text{eff}} \cdot A$, is due to the active element used. Power needed to maintain the oscillating is determined by this effective resistance R_{eff} . Factor “A” is usually taken equal or larger than 1. Finally, single sided spectral noise density for the given oscillator is evaluated as:

$$L\{\Delta f\} = \frac{\int_{(f_o + \Delta f - 1/2)}^{(f_o + \Delta f + 1/2)} dV_{\text{out}}^2}{\text{output power}} = \frac{kT \cdot R_{\text{eff}} \cdot [1 + A] \cdot \left(\frac{\omega_o}{\Delta\omega}\right)^2}{\left[\frac{V_{\text{amplitude}}^2}{2}\right]} \quad \text{Eq. (5.14)}$$

Eq. (5.14) depicts that the phase noise of an oscillator has inverse relation with oscillation amplitude, thus making the signal larger than the noise will reduce phase noise. The most important parameter in the design of an LC tank oscillator is its effective resistance R_{eff} , which determines the phase noise of the oscillator and power needed to maintain the oscillation.

While this approach is valuable in identifying the relative contribution of each noise sources but it is based on an unsupported implicit assumption of no amplitude limiting and also utilizes empirical fitting parameter “A” in the phase noise prediction. It is still not clear how to calculate “A” from circuit parameters [112].

5.2.5 Hajimiri - Lee Phase Noise Model:

As any oscillator is a periodically time-varying system, a general linear time-varying (LTV) phase noise model is presented in [113]. The model explains quantitatively the mechanism by which noise sources of all types convert to phase noise. It identifies the importance of symmetry in suppressing the upconversion of $\frac{1}{f}$ noise into close-in phase noise, and accommodates cyclostationary noise sources, leading to additional important design insights.

The LTV method introduces a special function called impulse sensitivity function (ISF or Γ) to consider the effects of nonlinearity, time-variance and cyclostationary noise. Γ is a dimensionless, frequency and amplitude independent function periodic in 2π and describes how much phase shift results from applying a unit impulse at any point in time, such that phase shift response to a unit impulse is expressed as:

$$h_{\Phi}(t, \tau) = \frac{\Gamma(\omega_o \tau)}{q_{\max}} u(t - \tau) \quad \text{Eq. (5.15)}$$

where $\Gamma(\omega_o \tau)$ is the ISF function of the output waveform and $q_{\max}$ is the maximum charge offset across the capacitor.

This current-to-phase transfer function is linear for small injected charge, although the active elements in any system have nonlinear voltage-current behavior. It is noted that the linearity and time-variance of a system depends on both the characteristics of the system and its input and output variables. The output excess phase, $\Phi(t)$, is calculated for small charge injections using the superposition integral:

$$\Phi(t) = \int_{-\infty}^{\infty} h_{\Phi}(t, \tau) i(\tau) d\tau = \int_{-\infty}^t \frac{\Gamma(\omega_o \tau)}{q_{\max}} i(\tau) d\tau \quad \text{Eq. (5.16)}$$

where $i(\tau)$ represents the input noise current injected into the node of interest.

Using phase modulation approach to convert phase to voltage and then the sideband power density is given as:

$$L\{\Delta\omega\} = 10 \cdot \log \left[\frac{\frac{\overline{i_n^2}}{\Delta f} \sum_{n=0}^{\infty} c_n^2}{8q_{\max}^2 \Delta\omega^2} \right] \quad \text{Eq. (5.17)}$$

where $\overline{i_n^2}/\Delta f$ is the power spectral density of input noise current, c_n is the coefficient of Fourier transform of ISF function, $\Delta\omega$ is the frequency shift from carrier frequency.

Although ISF is a good and comprehensive way of modeling phase noise, it has some practical difficulties. One major drawback for accurate ISF simulations is the long transient simulation time. In order to compute the ISF for a circuit node at time t , small time steps have to be taken to ensure accuracy and a long time is needed to allow the circuit to settle to its steady state after the impulse is injected. As the circuit complexity grows, the complete computation for all the ISFs becomes so time-consuming that it eventually becomes impossible. Moreover, Hajimiri's simulation-based LTV model does not trace the phase noise to its original sources and does not provide a direction of how to minimize phase noise by optimizing the circuit topologies [114].

5.3 VCO Design Considerations

The specification for a practical VCO depend on applications. General performance criteria required for VCO can be summarized by the following basic features:

- Low jitter or phase noise;
- Wide tuning range with linear frequency control characteristics within the desired range of operating frequency;
- Spectral purity
- Absence of harmonic content
- Supply and substrate noise rejection;
- Pulling and pushing sensitivity;
- Insensitive to aging or temperature effects
- testability, preserving signal integrity at the output pad;
- Low power consumption;
- Low cost;

In this section some of these features will be discussed along with design trade-offs and guidelines leading to an optimum VCO design within the limitations of the available technology.

5.3.1 Jitter or Phase noise

As described in section 3.3.3, phase noise and jitter are metrics that quantify the frequency stability of a periodic signal. Practically, due to device noise, the oscillator output spectrum exhibits noise power around the fundamental frequency.

Figure 5-7. Output spectrum (a) ideal (b) with phase noise

Jitter metrics quantify the time domain uncertainty in the oscillator period. Ideally, edges of the oscillator signal occur at identical intervals in time as shown by the voltage waveform in Figure#. In practical circuits, the edges of the signal deviate from the ideal position in time by some amount each cycle.

Figure 5-8. Time domain VCO output (a) ideal (b) with jitter

The three most commonly employed timing jitter metrics for autonomous oscillators include long-term, period and cycle-to-cycle jitter. All three metrics quantify the uncertainty in the oscillator period. The period jitter is of most interest in the design of oscillators as it characterizes the short-term variation in each period from the mean.

As carrier frequency increases, it is more difficult to achieve good phase noise or jitter. In a PLL, VCO phase noise components within the loop bandwidth can be greatly suppressed by the loop filter correction. However, at large offset frequencies which lie outside the loop bandwidth, phase noise of the PLL is largely the component introduced by its oscillator. Thus, it is essential that the oscillator's phase noise be kept as low as possible. Figure 5-9 shows the distribution of phase noise energy in a VCO phase noise plot.

Figure 5-9. Typical phase noise distribution

5.3.2 Frequency control characteristics

Frequency control characteristics of the VCO have the following main requirements:

- linearity of the VCO output frequency versus control voltage,

- wide tuning range,
- large gain factor
- capability of accepting wide band modulation.

The modulation bandwidth can be increased by reducing the time constant associated with the tuning port of the VCO. A high modulation/tuning bandwidth is required for fast tuning VCOs.

A compromise is needed between above conflicting requirements depending on the intended application.

5.3.3 Supply and substrate noise rejection

LC-Tank Oscillators are quite sensitive to power supply fluctuations, such as current spikes and ground bounce of common on-chip V_{dd} and gnd rails, as well as noise induced from adjacent on-chip circuitry. In order to reduce the VCO sensitivity to such noise sources, several layout optimization techniques must be employed :

- keeping power supply pads for the VCO circuit will reduce the sensitivity of the oscillator to changes in supply voltage levels of the common on-chip power rails,
- using on-chip decoupling capacitors between power supply and ground lines will filter the power supply high frequency noise, and

- separating the sensitive VCO circuit from adjacent fast switching digital circuitry to avoid substrate noise. Large number of substrate contacts within N and P wells and using double guard rings of n+ and p+ connected to a stable V_{dd} and gnd rails placed around the VCO circuit will reduce substrate noise to the VCO. Also use of deep N-well.

5.3.4 Sensitivity to injection pulling and supply pushing

VCOs show an interesting phenomenon that is if a external noise component is injected close to the carrier frequency and has a comparable magnitude, with the increase in noise magnitude, the VCO center or carrier frequency will shift toward the noise frequency ω_n and finally “lock” to that frequency. This VCO behavior is called “injection pulling” and is shown in Figure 5-10.

Figure 5-10. Carrier locking to noise frequency.

LC VCOs, in general, show poor supply rejection. As shown in Figure 5-11, reverse voltage across the varactor and hence, the oscillation frequency will vary with the variation in supply voltage. This undesirable feature of VCOs sensitivity to the supply voltages in VCO design is called “supply pushing” and is expressed in MHz per volt

Figure 5-11. Supply pushing in LC VCO

5.3.5 Spectral Purity (FM or AM noise)

FM noise or phase noise refers to the short term random frequency fluctuation of a signal which is the rate of change of phase deviation. AM refers to the amplitude fluctuations of the signal and is caused by bias noise fluctuations and supply voltage variations. The most common source of spurious amplitude modulation is the power supply. Thus, the supply voltage noise should be kept to a minimum. The AM noise component is usually 20dB lower than the FM or phase noise component. The AM noise component is therefore, small and can be neglected.

5.4 LC-Tank VCO Implementation

In chapter 3, the design of both a monolithic inductor and an accumulation-mode varactor are presented. In this section, these components are integrated into the overall design of the LC-tank VCOs. Section 4.5.4 briefly describes three types of VCOs to be designed. Among them VCO#1 and VCO#2 are negative-gm, positive feedback, complementary and fully differential LC-tank VCOs, whereas VCO#3 is a switch LC-tank VCO. Design, implementa-

tion circuit optimization and layout issues are described below. Prediction of phase noise based on LTI model is made.

All three VCOs were fabricated on the project test chip. These VCOs will be discussed in detail in the following sections.

5.4.1 VCO#1 and VCO#2 Design and Implementation:

Both VCOs are multi-gigahertz, low noise, moderate power consuming, complementary structures and incorporate resonant tank to achieve stable frequency output. VCO#1 has target frequency of 2GHz and same structure (VCO#2) is optimized and enhanced in speed to run upto 11GHz. A simplified structure representing both VCOs is shown in Figure 5-12.

As mentioned earlier, VCO#1 utilizes empirical equations in [58] to realize its inductor and relies on PN-junction varactor (Section #) for fine tuning.

VCO#2 utilizes state-of-the-art tools (ASITIC and HPEESOF ADS, Section 4.3) to obtain broadband, high Q inductor and varactor models. Both passive component designs are discussed in previous chapter along with optimum layout techniques. VCO#2 is designed and optimized to satisfy tuning range and jitter requirement of SONET OC192 high-speed SERDES system (Section 2.4.4).

- Symmetrical balanced in nature, gives advantage over other structures in -gm VCO family. Symmetry helps in lowering $\frac{1}{f}$ corner noise frequency which is important for low close-in phase noise performance [112].

To startup the oscillation and sustain a stable steady state oscillation, the negative resistance of active devices ($\frac{1}{g_m}$) must be greater than the loss resistance of the LC-tank. A low value of $V_{\text{effective}}$ i.e. $V_{gs} - V_t$ of the amplifying transistors gives a good transconductance-to-current ratio. This will translate into low power consumption, but larger transistor sizes and smaller tuning range. In order to have more control over the bias point of the oscillator, a tail current control device M5 is added. This tail current control device is implemented as a simple NMOS current mirror. This tail current device can alter the voltage swing across the tank circuit of the oscillator. Since the negative resistance presented to the LC tank circuit can be varied by changing this current, the actual equivalent parallel resistance (R_p) of the resonator can be experimentally determined by finding the lowest bias current at which the circuit will oscillate. At this bias point $R_{\text{negative}} = R_p$.

5.4.2 VCO#1: 2GHz LCVCO Implementation

The MOS devices in VCO#1, are implemented using the minimum gate length allowed in the process (0.25 μm). Since " g_m " is proportional to W/L , using the smallest allowable gate length (L) implies that a small device width (W) can be utilized. This helps in minimizing the total gate area ($W*L$) and hence the gate capacitance. In order to keep " $g_{m,\text{pmos}} = g_{m,\text{nmos}}$ ", PMOS devices will be twice the size of NMOS devices. This can be taken as a drawback for complementary structure LC VCOs because PMOS device will take double

the area as compared to NMOS device and also slows down the maximum achievable speed of the VCO due to higher device parasitic capacitance associated with it.

For VCO#1, NMOS transistors, M1 and M2 in Figure 5-12, are chosen to be 72 μm wide and the PMOS transistors, M3 and M4, are twice larger which will give same “ g_m ” for both type of devices. The tail transistor, M5, has W/L ratio is chosen to be large (200/1) so that it provides a high output impedance. Moreover, it is important to keep M5 in saturation region ($V_{on}=V_{gs}-V_{th}=200\text{mV}$) to avoid any noise at the gate to get amplified and modulated into the close-in phase noise of the carrier. In this particular design, $V_{\text{effective}}$ has been chosen to be 0.4 to get the best trade-off between power consumption and tuning range. This combination gives a single-ended oscillation of 1.2Vpp from a 2.5V supply.

The frequency at which resonance occurs in LC-tank circuit is given as:

$$\omega = 2\pi f = \frac{1}{\sqrt{LC}} \quad \text{Eq. (5.18)}$$

Therefore, for desired center frequency of 2GHz, taking inductor value, L, of 5nH and by using above equation, value of capacitance, C, calculated to be:

$$C = \frac{1}{L \times (2\pi f)^2} = \frac{1}{(5 \cdot 10^{-9}) \times (2 \cdot \pi \cdot 2 \cdot 10^9)^2} = 1.26\text{pF} \quad \text{Eq. (5.19)}$$

The capacitor of the LC-tank is formed by the inductor's parasitic capacitance to the substrate, the drain-bulk, gate-drain and gate-source capacitances of the active transistors and tunable p+-to-n-well junction capacitor, varactor. In order to achieve a large tuning range, this last contribution must be as large as possible.

The tunable junction capacitor, varactor, is made as a p+ active area in an n-well. Its capacitance can be tuned with the control voltage, VCON, which controls the bias voltage of the n-well. Since, this n-well is a common node, its parasitic capacitance to the substrate is not

important. Layout of this junction capacitor must be done carefully to limit its series resistance by using inter-digitated layout scheme (see section 4.5.4.1 for details).

Passive on-chip inductors are mostly realized using a spiral-shaped metal connection, routed in one or more of the standard available routing levels on the silicon substrate. The quality factor, Q , of the inductor is limited by the series resistance of the metal tracks (see section 4.4. for details).

Simplified tank circuit is shown in Figure 5-12. Simulation of this VCO is done in HSpice transient analysis in Cadence IC design environment and for accuracy p+-to-n-well junction diode model (section 4.5.4) and the spiral inductor π -circuit model (Appendix-A (a)) have been used. In order to simulate oscillator circuits, the tank circuit must be perturbed by a small transient. In reality noise that is present in the circuit should be sufficient to ensure oscillator startup. The maximum transient time step used was 0.01nsec. The maximum time step must be much less than the oscillator signal period to ensure valid simulation results.

Figure 5-13, shows the steady state outputs of the oscillator VCO#1.

Figure 5-13. VCO#1 simulation output waveform

Figure 5-14, shows the simulated post-layout tuning curve of the oscillator.

Figure 5-14. Simulated tuning curve for VCO#1

The predicted tuning range is 140MHz (6%). The amplitude of the oscillations does not change significantly over the tuning range. The VCO core draws 12mA at a supply voltage of 2.5V.

While these transient simulations are useful for evaluating key oscillator parameters, they tell the designer very little about the phase noise performance of the circuit. As discussed in phase noise model review (Section 5.2), the phase noise predictions are always difficult. Accurate simulations ultimately depend on accurate models. In this case, adequate noise models for the devices were not available at the time of VCO#1 design. To accurately simulate the phase noise of the oscillator, both the thermal noise and flicker ($\frac{1}{f}$) noise of the MOSFETs would need to be correctly modeled. A major disadvantage to using digital CMOS to achieve RF functionality is the lack of noise models for the MOS devices.

In order to have some idea of the expected phase noise of the VCO#1, the linear phase noise model (LTI) of [58] is employed. LTI model is commonly used among VCO designers and gives a good approximation of the expected phase noise. Using Eq. (5.14), the phase noise of the oscillator can be predicted. For single-ended output of $1.2V_{pp}$ at $f_o=2\text{GHz}$, Q of the inductor at this frequency is 5.05 (Appendix-A (a)). The varactor Q is estimated to be 27.55 (Section 4.6.4.1). The total tank circuit quality factor can therefore be computed as:

$$Q_{\text{tank}} = 1 / \left(\frac{1}{Q_{\text{varactor}}} + \frac{1}{Q_{\text{inductor}}} \right) = 1 / \left(\frac{1}{27.55} + \frac{1}{5.05} \right) = 4.26 \quad \text{Eq. (5.20)}$$

Thus, R_{eff} can be calculated from Eq. (5.9),

$$R_{\text{eff}} = \frac{1}{Q_{\text{tank}}(2\pi f_o C)} = \frac{1}{4.26 \times 2\pi(2 \times 10^9)(0.83 \times 10^{-12})} = 22.51 \Omega \quad \text{Eq. (5.21)}$$

The excess noise factor “A” in Eq. (5.14) is typically set equal to the oscillator startup safety factor and can be calculated as the ratio of the equivalent parallel resistance, R_{eq} , to the negative resistance generated by the circuit, R_{eq} is given by:

$$R_{\text{eq}} = Q_{\text{tank}} 2\pi f_o L = (4.26)(2\pi)(2 \times 10^9)(5.63 \times 10^{-9}) = 301.4 \Omega \quad \text{Eq. (5.22)}$$

From simulations the generated negative resistance is -112.7Ω , therefore, “A” is found to be 2.67. Now, using Eq. (5.14), the expected phase noise can be predicted as:

$$L\{1\text{MHz}\} = \frac{(1.38 \times 10^{-23})(297)(22.51)[1 + 2.67] \left(\frac{2 \times 10^9}{1 \times 10^6} \right)^2}{(1.2)^2 / 2} = -117.25 \text{dBc/Hz} \quad \text{Eq. (5.23)}$$

5.4.3 VCO#2: 10GHz LCVCO Implementation

As described earlier that VCO#2 uses same complementary “- g_m ” structure as shown in Figure 5-12, having the same general characteristics. The main features of this VCO are:

- designed and optimized to satisfy jitter/phase noise requirement SONET OC192 SER-DES systems.
- wide tuning range, target range 10GHz ~11GHz, to cover process, temperature and voltage variations.
- utilizes state-of-the-art tools ASITIC, and HPEESOF-ADS to obtain broadband inductor and Accumulation Mode MOS varactor models for the tank circuit.
- phase noise optimization using Cadence-ADS dynamic link
- layout optimization to reduce parasitic capacitance of the devices and routing.
- incorporate techniques to maximize power supply and substrate noise rejection.
- implemented in deep sub-micron CMOS technology with 1.2V supply.
- low power consumption of 6mW ($5mA \cdot 1.2V$)

MOS devices in VCO#2 are implemented with minimum gate length and P-channel transistors (M3-M4, in Figure 5-12) are kept twice the size of N-channel transistors (M1-M2, in Figure 5-12) so that “ $g_{m,pmos} = g_{m,nmos}$ ”. The tail transistor, M5, is kept in weak inversion region to reduce flicker (1/f) noise up-conversion [115]. This combination gives a single-ended oscillation of 1V_{pp} from a 1.2V supply.

For the desired center frequency of 10GHz, using inductor value of 0.9nH, required value of capacitance is found to be:

$$C = \frac{1}{L \times (2\pi f)^2} = \frac{1}{(0.9 \cdot 10^{-9}) \times (2 \cdot \pi \cdot 10 \cdot 10^9)^2} = 281.4 \text{fF} \quad \text{Eq. (5.24)}$$

Again, the total capacitance in the LC tank is formed by the inductor's parasitic capacitance to the substrate, the drain-bulk, gate-drain, and gate-source capacitance of the active devices and tunable Accumulation Mode capacitance of the varactor. It is desirable to have the maximum capacitance contribution should come from the varactor in order to achieve wide tuning range.

Passive devices of the tank circuit in this VCO are carefully modeled and optimized (see Sections 4.5 and 4.6.4.2) to achieve higher Q_{tank} . Figure 5-15 shows the post-layout tuning range curve of the oscillator.

Figure 5-15. Simulated tuning curve for VCO#2

The curve has a drooping characteristic at VCO control voltage, $V_{CTL} > 0.8V$. This is caused by the inaccurate HSpice model of the Accumulation Mode varactor available at the time of design of this VCO. This is confirmed at the measurement stage where VCO tuning curve does not show any drooping (Figure 6-12). From simulation predicted tuning range is from 10.25GHz to 10.89GHz (640MHz) and VCO gain of 1.26GHz/V. The VCO core draws 2.4mA at a supply voltage of 1.2V.

The expected phase noise is calculated using same equations as used in for VCO#1. For single-ended output of 1Vpp at $f_o = 10.25GHz$, total tank Q is found to be:

$$Q_{\text{tank}} = 1 / \left(\frac{1}{Q_{\text{varactor}}} + \frac{1}{Q_{\text{inductor}}} \right) = 1 / \left(\frac{1}{30} + \frac{1}{10.5} \right) = 7.78 \quad \text{Eq. (5.25)}$$

$$R_{\text{eff}} = \frac{1}{Q_{\text{tank}}(2\pi f_o C)} = \frac{1}{7.78 \times 2\pi(10 \times 10^9)(0.253 \times 10^{-12})} = 8.08 \Omega \quad \text{Eq. (5.26)}$$

Again, the excess noise factor “A” in Eq. (5.14) is calculated as the ratio of the equivalent parallel resistance, R_{eq} , to the negative resistance generated by the circuit, R_{eq} is given by:

$$R_{\text{eq}} = Q_{\text{tank}} 2\pi f_o L = (7.78)(2\pi)(10 \times 10^9)(1 \times 10^{-9}) = 488.83 \Omega \quad \text{Eq. (5.27)}$$

From simulations the generated negative resistance is -173Ω , therefore, “A” is found to be 2.82. Now, using Eq. (5.14), the expected phase noise can be predicted as:

$$L\{1\text{MHz}\} = \frac{(1.38 \times 10^{-23})(297)(8.08)[1 + 2.82] \left(\frac{10 \times 10^9}{1 \times 10^6} \right)^2}{(1.0)^2 / 2} = -105.96 \text{dBc/Hz} \quad \text{Eq. (5.28)}$$

From ADS phase noise optimization analysis, the predicted phase noise is between -96.83dBc/Hz to -118dBc/Hz at 1MHz offset from carrier frequency of 10GHz as shown in Figure 5-16.

Figure 5-16. ADS phase noise prediction for VCO#2

It is worth mentioning here that these phase noise predictions are based on standard digital CMOS technology and no RF model noise numbers (AF, KF and EF) were available for the devices at the time of design of this VCO. Hence, it was expected that in measurement the actual phase noise would be approximately 10dB less and should fall between “pn, fm” and “pn, mx” phase noise predictions by HPEESOF-ADS.

The dynamic link between Cadence and HPEESOF-ADS provides a fast and an efficient tool that builds confidence in designing optimum VCO. This link brings back-and-forth Cadence-schematic into ADS environment where harmonic balance is used to optimize VCO phase noise. Phase noise optimization procedure is critical to achieve low noise VCO

5.4.4 VCO#3: 10GHz Inductor-switched LCVCO Implementation

This type of LCVCO was first reported in [116] and is characterized by a very wide tuning range but moderate phase noise performance. This VCO has been included in this thesis for its performance study for 10GHz SONET OC 192 application. The general architecture of this VCO is shown in Figure 5-18.

The main features of this VCO are:

- very wide frequency tuning range, couple of GHz. Can compete with ring oscillators in terms of tuning range with better Q.
- utilizes soft switching of LC-tank.
- varactor less, uses fix metal-to-metal or MOS capacitor in the resonator circuit.
- NMOS only, negative g_m , positive feed back, differential structure.
- high gain (K_{vco}) that increases VCO sensitivity from any noise on the control path (VCON).
- large layout area due to second pair of inductor needed
- low power consumption, takes 5mA from 1.2V supply.

Figure 5-18. Generic structure of switched-inductor LCVCO.

The post-layout simulated tuning range is shown in Figure 5-19, below:

Figure 5-19. Simulated tuning range for VCO#3

This VCO shows an exceptionally wide tuning range from 6.5GHz to 11.3GHz (4.86GHz) which covers all the standards for SONET OC 192 applications. The tuning curve also highlights one important issue here which is its very high gain ($K_{vco}=4.7\text{GHz/V}$). Such large VCO gain is not feasible for PLL in CDR or CMU as even small “mV” of ripple on the control path from charge-pump output and loop-filter will get large magnification and easily modulates VCO carrier frequency.

ADS phase noise using same dynamic link method shows that the predicted phase noise falls between -82.99dBc/Hz to -110dBc/Hz at 1MHz offset from carrier frequency of 10GHz.

Figure 5-20. Expected phase noise prediction for VCO#3

Since VCO is varactor-less, it relies on soft-switching of inductor pair to obtain tuning range, as VCON is swept from 0V to 1.2V. The overall tank Q depends on the inductor Q.

and since values of inductor Q are normally not high enough, in this case 10.1 at 10GHz, therefore, this VCO has less ability for carrier frequency selectivity. This explains why the phase noise performance for this VCO are not as promising as its complementary counterpart.

A modified version of the above VCO is reported in [117] which shows very low VCO jitter of 130fs in a 10 MHz-bandwidth PLL.

5.5 Layout Optimization

In this section, layout related design considerations associated with speed improvement, noise and circuit partitioning are presented.

One of the crucial factors in achieving top speed in a CMOS design is the optimization of the circuit layout. For keeping post-layout extraction simulation results close to that of pre-layout, VCOs should be laid out full-custom with incorporating all optimization techniques previously described for passive components (Chapter 4). In addition to that, following layout guidelines have been considered in order to achieve optimum low power and low noise the high-speed VCOs.

- detailed layout floor-planning is an integral part of VCO circuit design. It must be captured at the schematic level, with the greatest possible rigor and concern for details.
- minimize parasitic capacitance, the core VCO layouts are made as compact as possible. Minimal metal lengths are used by using diagonal or 45° metal lines where possible. VCO high-speed outputs (OUTP / OUTN) are routed differential in nature, symmetrical and of equal length.

- power and ground lines are laid out as 20 μm wide metal lines. Power buses are wide enough to handle maximum current drawn by the VCO core and associated circuitry. Also there should be minimum IR (voltage) drop to avoid any headroom problem especially in 1.2V supply case.
- star-ground techniques are employed to prevent ground loops and power rail ripples. This results in lower current spikes and ground bounce which can cause VCO phase noise degradation.
- double guard ring around each VCO to prevent noise coupling from adjacent circuits. The p+ connections to ground help to keep a low-impedance path between the substrate and ground and avoid noise from propagating through the resistive substrate.
- generous use of on-chip de-coupling capacitors between power supply (Vdd) and ground (Gnd) in un-used layout space to filter high frequency noise on the power supply.
- special high-speed input-output (I/O) pads are used instead of standard digital pads provided in the technology standard cell library. This is to avoid any signal integrity issues i.e. signal attenuation or distortion, at the output. Separate power supply pin is used for the VCO core circuit to avoid any large current spikes from the buffer or output driver circuit.
- optimization in device sizes and layout are critical, symmetry in layout plays an important role to achieve best phase noise performance. Matching devices by interdigitating and adding dummies. The dummy element does nothing electrically but is simply added to ensure that the matched devices see the same adjacent structure. Shared

source/drain to minimize devices parasitic capacitance. Differential pairs have a common centroid to minimize the effect of process gradient. The gates of the active devices are connected on both sides to minimize excess poly resistance.

- use of deep N-well where technology permits (e.g in VCO#2 and VCO#3) helps in isolating VCO core from the rest of the circuit substrate. That greatly reduce risk of substrate noise pick up by the noise sensitive circuit. The use of N-well increases the resistive impedance between the isolated regions due to the PN-junction depletion region, which also acts as bypass capacitor to help lower the noise on Vdd [118]. Coupled noise in the substrate of the oscillator, causes device capacitances in the oscillator to vary, which in turn causes the output clock frequency to vary, introducing jitter.
- use of metal shielding on critical nets is important. Nets like VCO control input (VCON) and high-speed outputs (OUTP / OUTN) are properly shielded to avoid any noise coupling from adjacent nets.

All three VCOs have been laid out for probing.

5.6 VCO Output Driver Circuit

5.6.1 Output Driver for VCO#1

VCO#1, uses a differential-to-single-ended converter circuit (D2S) and a common-source amplifier (50 ohm driver circuit) to take the high-speed VCO signal off-chip. D2S provides an interface between the VCO differential outputs and the output 50 ohm driver circuit. It boosts the input signal so that a standard CMOS gate can be used for further amplification. The structure of this block is a basic single operational amplifier with PMOS transistors active loads as shown in Figure 5-21. To simplify the structure, the block does not have any

current limiting current sink. The input signals are large swing signals ($>1\text{V}$ in amplitude), thus the linearity of this operational amplifier is not a concern (i.e. short input channel lengths). But the dimensions of the differential pair and the active loads will limit the actual switch current. The peak current drawn from V_{dd} is 2mA and it occurs everytime the inputs commute.

Figure 5-21. Differential-to-single converter schematic

Common-source amplifier is used as a final circuit before which signal can be taken out of chip. Using single NMOS at the output has its advantages as no requirement of inverter switching at the output and VCO output signal can be taken out even if its swing is quite low.

Figure 5-22. Common source amplifier with off-chip test circuit.

5.6.2 Output Driver for VCO#2 and VCO#3

Both 10GHz VCOs utilize current mode logic (CML) output buffer chain to take signal off-chip. Since these VCOs are running at very high-speed, differential-to-single converter cannot be used here to switch fast enough and cause VCO output signal distortion. A differential pair with resistive loads is often used as an output buffer. Such a current mode logic (CML) output buffer is power-efficient and fast [9]. A generic CML structure is shown in Figure 5-23, below:

Figure 5-23. A generic CML structure.

Ideally, the load resistors, R , should be equal to the characteristic impedance of the transmission medium to eliminate reflections.

5.7 Summary

In this chapter, existing phase noise model for the VCO has been reviewed. Both merits and de-merits of LTI and LTV models are studied. LC VCO design considerations are highlighted and based on these three LC VCOs are designed and implemented. Since LTI approach is commonly used to predict phase noise in a VCO, therefore, same method has been employed to estimate the phase noise of the designed LC VCOs and comparison is made from values obtained from ADS harmonic balance simulator. It is shown in simulation that both 10GHz VCOs have sufficient tuning range to cover all SONET standards and have good phase noise to meet stringent jitter specification with fair margin.

6 Measured Results

This chapter presents the characterization of passive components and the VCOs on the fabricated CMOS die. First, the performance of the passive test structures are discussed; then the detailed oscillator measurements are presented.

The test chip for VCO#1 was received from CMC (Canadian Microelectronic Corporation) as loose unpackaged die. A photograph of the fabricated VCO#1 test along with inductor test structure is shown in Figure 6-1.

Figure 6-1. Test chip for VCO#1

VCO#2 and VCO#3 were on sponsoring company's wafer fabricated through TSMC. Fabricated VCO#2 test structures are shown in Figure 6-2

Figure 6-2. VCO#2 test structure

VCO#3 test structure is shown in Figure 6-3.

Figure 6-3. VCO#3 test structure

6.1 Test Setup

The test setup consists of a 40GHz Microtech probe station, GGB customized RF/microwave probes, Agilent E5500 phase noise measurement system, spectrum analyzer (40GHz HP 8561A), network analyzer (40GHz Wiltron 360), oscilloscope, multi-meter and several power supplies. Each probe head has two GSG (ground-signal-ground) RF probes and six DC probes, and the probing pad features a $50\text{ }\mu\text{m} \times 50\text{ }\mu\text{m}$ size and $75\text{ }\mu\text{m}$ pitch. The E5500 phase noise measurement system consists of a PLL-based phase noise test set, a low noise RF reference source, a downconverter and a spectrum analyzer. A simplified phase noise measurement diagram is shown in Figure 6-4. If the signal power of the oscillator under test is too small, an external low noise amplifier is required.

Figure 6-4. A simplified phase noise measurement setup

The measurement was performed at a government laboratory (CRC). Firstly, the testing results of passive components will be given. Secondly, the measurements of the VCO

tuning range and phase noise will be presented along with correlation to the simulated results.

6.2 Passive components Testing

The impedance of the passive components is extracted using the network analyzer (40GHz Wiltron 360) and a high-speed ground-signal-ground (GSG) picoprobe. Before the extraction of accurate S-parameters, it is necessary to perform the proper multi-step de-embedding (calibration). A two-step de-embedding procedure is performed that first moves the reference plane to the probe tips after removing all parasitics in the cables and connectors. This first de-embedding / calibration is accomplished with a picoprobe GGB industries calibration kit which consists of impedance standard substrate (ISS). It relies on open-short-load-thru (OSLT) calibration procedure to calculate 12-term correction coefficients at the network analyzer. The OSLT calibration result is shown in Figure 6-5. Since the CMOS substrate is much more lossy than the calibration substrate, the effect of the CMOS bond pad (PAD) must be de-embedded. Hence, the device-under-test's (DUT) S-parameters are then measured followed by on-chip de-embedding on open and short test structures. Both measurements containing DUT data and PAD data are stored as “ *.spi ” files for further process in software.

The second de-embedding step is performed in software, through the use of a “de-embedding data item” within ADS. Here, the PAD data are subtracted out of DUT data. Once this is accomplished, actual S-parameter data that reflects just the DUT without the effects of pad parasitics are thus obtained. Final S-parameters are then converted to Y-parameters in ADS to plot extracted DUT parameters versus frequency.

Figure 6-5. OSLT calibration result

6.2.1 Planar Inductor

Planar inductor test structures, used in VCO#1, are shown in Figure 6-6. Single-port open and short de-embedding structures are also fabricated for calibration purpose as explained earlier.

Figure 6-6. Test structures for VCO#1

Equations derived in Section 4.1.4, are then used to extract series inductance (L_s), series resistance (R_s) and inductor Q from the measurement data.

The symmetrical differential inductor layout used in VCO#2 is shown in Figure 6-7, and its extracted parameters are shown in Figure 6-8.

Figure 6-7. Fabricated 0.9nH inductor for VCO#2

The extracted parameters, L_s and Q for 0.9nH inductor are shown in Figure 6-8. At 10GHz the measured inductance and quality factor of the inductor are 0.868nH and 9.11.

Figure 6-8. Measured inductance versus frequency for the inductor in VCO#2

Comparing the measured result in Figure 6-8, to the simulated result in Figure 4-10, both the inductance and Q matches with simulated result very closely between the band of frequency of interest (9GHz to 11GHz). The series resistance is found to be 8.64Ω at 10GHz. The inductance plot also shows that the inductor self-resonance occurs at around 22GHz which is at lower frequency compared to the simulated result. This can be attributed to the use of pattern-ground shield which lowers self-resonance frequency of the inductor more than expected.

6.2.2 Varactor Measurement

S11 versus frequency of the tank circuit varactor test structure are also measured using a similar one-port test configuration as mentioned for the inductor case. Measured CV-curve for Accumulation Mode MOS varactor used in VCO#2 is shown in Figure 6-9. It is vital to compare measured CV-curve with that obtained in simulation, Figure 4-23. HSpice simulated CV-curve predicts that this Accumulation Mode varactor has all three regions of operations: inversion, depletion and accumulation, but measured CV-curve and VCO#2 tuning curve both show monotonic behavior, Figure 5-15.

Figure 6-9. Measured CV-curve for Accumulation Mode MOS Varactor.

It was later found that Level 49 SPICE model for the Accumulation Mode MOS varactor used in VCO#2 design was inadequate as Level 49 SPICE model does not support frequency-dependent capacitance. TSMC has published a document detailing some experimental varactor measurement result for frequencies between 300MHz and 10GHz. This data confirms that the Accumulation Mode MOS varactor device does not have a significant inversion mode capacitance at high frequencies.

6.2.3 VCO Measurement

Measured phase noise for VCO#1 is shown in Figure 6-10, shows single-sideband phase noise of -99.77dBc/Hz at 1MHz offset for carrier frequency of 2GHz.

Figure 6-10. Measured spectrum of VCO#1

Figure 6-11. Measured tuning range for VCO#1

Measured tuning range for VCO#2 is shown in Figure 6-12, which shows a monotonic accumulation mode tuning only and conforms with the measured CV-curve for the Accumulation Mode varactor (Figure 6-9).

Figure 6-12. Measured tuning range for VCO#2

Maximum VCO gain, K_{VCO} is 1.35GHz/V.

Measured phase noise for VCO#2 is shown in Figure 6-13, which shows single-sideband phase noise of -100dBc/Hz at 1MHz offset for carrier frequency of 10.244GHz.

Figure 6-13. Measured phase noise graph of VCO#2

Measured phase noise for VCO#3 is shown in Figure 6-14, which shows single-sideband phase noise of -94.5dBc/Hz at 1MHz offset for carrier frequency of 10GHz. Maximum VCO gain is 5.37GHz/V.

Figure 6-14. Measured phase noise graph of VCO#3

6.3 Summary

This chapter concludes with presenting characterization of Accumulation Mode MOS varactor, inductor, measured tuning range and phase noise plot for each designed VCO. CV-curve of Accumulation Mode MOS varactor showed monotonic behavior and is verified by the measured tuning curve of the VCO#2, which clearly indicates that the HSpice model used in simulation for this varactor is incorrect. Inductor modeling for 0.9nH inductor using ASITIC and ADS gives a good match with measured data between 5GHz to 15GHz and at 10GHz the difference is just 3.5% from the simulated value. VCO measurements shows that the tuning range and phase noise obtained are close to simulated values.

7 Conclusion and Future Work

This chapter concludes the research work presented in this thesis. The goal of this research was to design the most challenging and sensitive circuit with respect to jitter / phase noise requirements in high-speed SERDES. SERDESeS are now popular in broadband, high-speed serial data communication chips and now have emerged as important feature among PLDs and FPGAs solutions. Among other IC standards e.g. XAUI, INFNIBAND, etc., SONET OC applications have the most stringent jitter requirements to meet that emphasis the need of low-power and low-noise VCOs.

7.1 Conclusions

In this thesis, it has been demonstrated that with proper design methodology and optimization for the passive components of the LC-tank and VCO core circuit, an LCVCO can simultaneously run up to its maximum speed possible under a given technology f_T along with meeting the jitter / phase noise requirement while consumes minimum power.

The lowest phase noise for the VCOs presented in this thesis is achieved with the Accumulation Mode MOS varactor VCO (VCO#2); -100dBc/Hz at 1MHz offset at an output frequency of 10.24GHz. At this operating point the VCO (not including output buffers) draws 2.4mA from a 1.2V supply (2.88 mW). A widely used figure of merit (FOM) for VCO performance is defined as [119]:

$$\text{FOM} = L\{\Delta f\} - 20\log\left(\frac{f_c}{\Delta f}\right) + 10\log\left(\frac{P_{dc}}{1\text{mW}}\right) \quad \text{Eq. (7.1)}$$

For the conditions as mentioned above, this becomes:

$$\text{FOM} = -100 - 20\log\left(\frac{10.24 \times 10^9}{1 \times 10^6}\right) + 10\log(2.88) = -175.61 \quad \text{Eq. (7.2)}$$

This work can be compared to other LC-tank VCOs. Table 7-1, shows the phase noise of this VCO compared with recently reported 10GHz VCOs.

Table 7-1. 10GHz VCO comparison table

Reference	Tech (μm)	f_o (GHz)	Phase Noise (dBc/Hz)	Tuning Range (GHz)	Power (mW)	Supply (V)	FOM (dBc/Hz)
Mostafa [120]	0.35 CMOS	10.5	-84.4 @ 100KHz	10.25~10.55 =0.3	28	3.5	-170.35
Mukerjee [11]	0.13 CMOS	10	-99 @ 1MHz	3.7	3.6	1.2	-173.44
This Work [VCO#2]	*	10.24	-100 @ 1MHz	10.2~11.1 = 0.86	2.88	1.2	-175.61
This Work [VCO#3]	*	10	-94.5 @ 1MHz	6.5~11.0 = 4.5	5.76	1.2	-166.8
De Cock [121]	0.25 CMOS	10	-127 @ 3MHz	2.8	50	2.5	-180.46
Wu [122]	0.35 BiCMOS	10.2	-114 @ 1MHz	9.3~10.5 =1.2	35	2.5	-178.73
Yang [123]	0.18 CMOS	10	-117 @ 3MHz	9.76~10.45 = 0.69	8.82	1.8	-178
Liu [124]	0.25 CMOS	10.2	-106 @ 1MHz	9.76~11.0 = 1.24	45	1.5	-169.64

* since this research work has been sponsored by the sponsoring company, and under agreement CMOS technology used for the design cannot be disclosed without permission.

Table 7-1, shows that the present work is quite competitive with other 10GHz VCO solutions and surpass others with respect to power consumption performance. As it can be noted that higher phase noise performance is achieved by burning more current (see Table 7-1, [121,122,124]), which is not a power efficient solution for the design of overall high-speed SERDES. And especially these days when IC companies are competing bitterly with each other to provide low power and low cost solutions to their customers and to grasp most of the market share.

Only [11] with larger tuning range and with little higher power consumption, has phase noise performance close to VCO#2. As mentioned earlier, VCO#2 was designed with a goal to achieve SONET OC192 rms timing jitter requirement of 1ps (0.01UI) that translates to open-loop VCO phase noise requirement of -90 dBc/Hz @ 1MHz offset from the carrier frequency of 10GHz. VCO#2 meets that stringent requirement by fair margin of 10 dBc and with wide tuning range extending from 10.2GHz to 11.1GHz (860Mhz). Similarly, VCO#3 also meets this phase noise requirement by 4.5dBc but considering process, voltage and temperature variations, such margin would not be sufficient. However, VCO#3 showed maximum tuning range from 6.5GHz to 11GHz (4.5GHz) which is itself a record among LC based VCOs, and the author has not seen any publication on LC based VCO that has reported such a large tuning range yet.

VCO#1 has provided a launching pad for the development of 10GHz VCO#2. At somewhat lower speed (2GHz) and having same VCO topology (complementary), several high-speed design issues were studied to minimize noise contribution of the active devices, flicker noise up-conversion mechanism from bias (tail) transistor and power reduction while still maintaining maximum output signal amplitude and phase noise performance.

VCO#1 results also pin-point the necessity of proper broadband modeling of inductor and varactor in order to obtain maximum tank Q, a major factor to achieve lowest possible VCO phase noise.

7.2 Future Work

During the course of this work a number of unresolved questions regarding design issues were raised. Addressing these concerns is a possible area for future work.

- the discrepancy appeared in between Accumulation Mode varactor HSpice model and its measured CV-curve can be investigated further in detail and more accurate model for the varactor either in HSpice or in ADS should be generated so that VCO tuning range prediction in simulation can be made close to measured data. A detailed characterization of PN-junction varactor and MOS varactor at different regions of operation is itself a good research area and based on the results an optimum LC VCO with respect to phase noise / jitter, speed, linearity and power can be designed.
- the overall tank Q of an LC VCO is much dictated by the inductor Q. Further study is still needed to explore more on inductor geometry that can raise its on-chip Q. Octagonal, circular and horseshoe inductors [125] have shown excellent results in achieving inductor $Q > 10$. Such new inductor geometries can further be analyzed in ADS to obtain broadband models for 10GHz or beyond work. Deep sub-micron process is beneficial for inductor design as top metals can be used to realize inductor while reduction in its self-resonance frequency is achieved due to increase in spacing between top metal to metal 1 shielding underneath.

- tail / bias transistor in existing complementary VCOs can be a source of flicker noise upconversion and low frequency modulation. Filtering techniques as given in [126] can be implemented to suppress such noise and improve phase noise. Moreover, as supply voltage is reducing with technology scaling the tail transistor suffers from headroom problem, it is hard to keep it in deep saturation region ($V_{ON} = V_{GS} - V_T$), a desirable region of operation for the tail transistor. And because of that tail transistor (NMOS or PMOS) its DC operating point can move to soft-saturation or even in linear region where it can start act as an amplifier for any noise / ripple at its gate. Performance of the given VCOs in this thesis can further be studied without using any tail transistor.
- 10GHz VCOs (VCO#2 and VCO#3) showed large gain (K_{VCO}) which is often not a desirable feature for a VCO in a closed-loop system. Any small ripple / noise on the control path can get magnified and modulate carrier frequency. A multi-band or multi-gear coarse tuning scheme can be deployed either by switching fix binary-weighted capacitors [127] or by switched tuning inductors [128] to reduce VCO gain, improve linearity and to cover wide tuning range along with fine tuning scheme by varactors.
- quadrature phase VCO is much needed in CMU block of the high-speed SERDES in order to provide four phase clocking system, VCOs reported in this thesis can also be extended to achieve that goal while maintaining basic features of low noise and low power.
- low voltage and area-efficient approach utilizing differential transformer-like coupled tank [129] can be employed to overcome supply scaling and headroom issues in latest CMOS technologies.

- new exotic approach like distributed VCO [127] can further be explored to obtain best phase noise performance as it does not use any active device for oscillation. Frequency of a distributed oscillator is controlled by the time delay of its transmission line, layout of such VCO is very critical.
- it is from author's experience in ADS harmonic balance that the accuracy in VCO phase noise prediction in simulation is within $\pm 4\text{dB}$ of that from measurement provided that the RF noise models available in a particular process. If noise models are not available, as in the case for the designed VCOs in this thesis, this prediction can increase to $\pm 10\text{dB}$. As a future work same VCOs can be re-simulated in ADS harmonic balance with real noise numbers to verify and confirm above argument.
- phase noise of the VCOs in this thesis is also predicted using LTI model and showed quite close result compared to measurement. Since oscillators are inherently non-linear and time-variant system. The accuracy of the noise prediction increases if the time varying nature of the circuit is taken into account. It would be worth doing to use LTV model proposed in [112] to calculate VCO phase noise and compare result with that from LTI model, ADS harmonic balance, and measurement.
- accurate measurement of VCO phase noise is another important issue. Phase noise measurements on a free running oscillator are tricky because the carrier frequency can drift while the power at the desired offset is being measured. Since the entire oscillator spectrum drifts with the carrier this can lead to incorrect result. Accurate measurement of the phase noise of a free running VCO can be obtained using a dedicated phase noise measurement system, such as Agilent 3048A or E5500.

- RF interference coupled into the test setup was a significant problem, especially the upconversion of local FM 105MHz broadcast and the refresh signals of nearby computer monitors. Since all the designed VCOs in this thesis are microprobed and dies are exposed to noisy lab environment, a packaged VCO test chips can be a future work provided that proper package modeling has been done at higher frequencies ($f_o \geq 10\text{GHz}$) and incorporated in simulation.
- some on-chip bias and power supply decoupling should be considered to clean up the power supply and bias lines. Simple capacitor connected NMOS transistors could be used. A very low frequency pass filter ($3\text{dB } f_{\text{cutoff}} < 100\text{KHz}$) on the gate of bias / tail transistor can help in suppressing the low frequency modulation.

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Appendix - A

(a) Inductor Calculations for VCO#1:

Using the inductor lumped model based on extensive simulation and measurement results obtained for various spiral and octagonal coils using 3-D electromagnetic simulator, the required inductance for the VCO is calculated as follows

:

Figure: Pi model for inductor.

Inductor design empirical equations are given as:

$$L = K_l \cdot \frac{A_r^{1.5}}{\omega^2} \cdot \eta_{ar}^{1.67} \cdot \eta_w^\alpha$$

$$R_s = \frac{\rho_{metal}}{t_{metal}} \cdot \frac{A_r}{w} \cdot \left(\frac{1}{w} + \frac{1}{\delta} \right) \cdot \eta_{ar}$$

where

$$\delta = \left(\frac{\rho_{metal}}{t_{metal}} \cdot \frac{K_r}{\omega_c} \right)^2 = \text{skin effect}$$

$$C_p = \frac{\epsilon_{ox}}{t_{ox}} \cdot A_r \cdot \eta_{ar}$$

$$R_c = R_{sheet_{sub}} \cdot \frac{t_{sub}^2}{t_{sub}^2 + A_r}$$

• **Parameter descriptions are:**

$$A_r = \text{Area of inductor} = s \times s$$

$$\eta_{ar} = \text{Area efficiency} = \frac{(\text{Area covered by metal}) A_{r, metal}}{(\text{Total area}) A_r}$$

$$\eta_w = \text{Line efficiency} = \frac{(\text{Area covered by metal}) A_{r, metal}}{(\text{Total area}) A_r}$$

$$K_l = \text{Inductor constant} = 1.3 \times 10^{-7} \quad (\text{H/m})$$

$$K_r = \text{Resistor constant} = 3.6 \times 10^9 \quad (\sqrt{m}). \text{Hz}/\Omega$$

$$\rho_{metal} = \text{Resistivity of metal layer}$$

$$t_{metal} = \text{Thickness of metal layer}$$

$$t_{ox} = \text{Oxide thickness between metal layer and substrate}$$

$$t_{sub} = \text{Thickness of substrate}$$

$$\epsilon_{ox} = \text{Oxide dielectric constant} = 3.4 \times 10^{-11} \quad (\text{F/m})$$

$$\omega_c = \text{Operating frequency} \quad (\text{rad/sec.})$$

$$R_{sheet_{sub}} = \text{Sheet resistance of the substrate} \quad (\Omega / \text{box})$$

- **0.25um CMOS-1P5M SPDV technology parameter for Typical case:**

1. Substrate type: Low doping, high resistivity substrate, $\rho_{\text{sub}} = 8 \sim 12 \text{ } \Omega \cdot \text{cm}$

2. Substrate thickness: $t_{\text{sub}} = 500 \text{ } \mu\text{m}$

3. Substrate sheet resistance:

$$\begin{aligned} R_{\text{sheet}_{\text{sub}}} &= \frac{\text{substrate resistivity}}{\text{substrate thickness}} = \frac{10}{500} \frac{\Omega \cdot \text{cm}}{\mu\text{m}} \\ &= 200 \quad (\Omega / \text{box}) \end{aligned}$$

4. Oxide thickness: $t_{\text{ox}} = 55698 \text{ } \text{\AA}$ (for metal 4)

$= 70009 \text{ } \text{\AA}$ (for metal 5)

5. Metal thickness: $t_{\text{metal}} = 0.57 \text{ } \mu\text{m}$ (for metal 4)

$= 0.92 \text{ } \mu\text{m}$ (for metal 5)

6. Metal resistivity: ρ_{metal}

$= \text{metal sheet resistance} * \text{metal layer thickness}$

$$\rho_{\text{metal4}} = 0.076 * 0.57 = 0.04332 \quad \Omega \cdot \mu\text{m}$$

$$\rho_{\text{metal5}} = 0.044 * 0.92 = 0.04048 \quad \Omega \cdot \mu\text{m}$$

- **Spiral Inductor layout parameters :**

1. Number of turns $n = 3$

2. Width of each line segment $w = 10 \text{ } \mu\text{m}$

3. Spacing between each line $sp = 1.3 \text{ } \mu\text{m}$

4. Inductor area $A_r = 230 \text{ } \mu\text{m} * 230 \text{ } \mu\text{m} = 52900 \text{ } \mu\text{m}^2$

5. Area efficiency $\eta_{\text{ar}} = 0.548$

6. Line efficiency $\eta_w = 0.885$
7. Top metal used = metal 4 and metal 5 with large number of VIA (4-5) in shunt

Figure: Spiral inductor layout.

Now, applying above inductor equations to calculate inductance and parasitics for the inductor lumped model to be used in the VCO design are given as :

1. Inductance

$$L = K_l \cdot \frac{A_r^{1.5}}{\omega^2} \cdot \eta_{ar}^{1.67} \cdot \eta_w^\alpha = 5.63 \text{ nH}$$

2. Series resistance

$$R_s = \frac{\rho_{\text{metal}}}{t_{\text{metal}}} \cdot \frac{A_r}{w} \cdot \left(\frac{1}{w} + \frac{1}{\delta} \right) \cdot \eta_{ar}$$

where

$$\text{skin effect} = \delta = \left(\frac{\rho_{\text{metal}}}{t_{\text{metal}}} \cdot \frac{K_r}{\omega_c} \right)^2 = 1.017 \times 10^{-4}$$

therefore,

$$R_s = 14 \, \Omega$$

Since, metal 4 has been used in shunt with metal 5 with lot of vias in the inductor layout design, its series resistance will further be reduced.

2. Parasitic capacitance

$$C_p = \frac{\epsilon_{\text{ox}}}{t_{\text{ox}}} \cdot A_r \cdot \eta_{\text{ar}} = 140.8 \, \text{fF}$$

3. Substrate resistance

$$R_c = R_{\text{sheet}_{\text{sub}}} \cdot \frac{t_{\text{sub}}^2}{t_{\text{sub}}^2 + A_r} = 165 \, \Omega$$

4. Inductor Q

Using equation $Q = \frac{\omega L}{R_s}$, inductor Q at 2GHz= 5.05

(b) p+-to-n-well (PN) Junction Varactor Calculations for VCO#1:

Total junction capacitance (C_J) as a function of the reverse voltage (V_R) is given by [98, HSpice Manual]:

$$C_J = C_{JA} \cdot A + C_{JP} \cdot P \quad \text{Eq. (1A)}$$

where

C_{JA} = area junction capacitance / unit area

A = total junction area

C_{JP} = perimeter junction capacitance / unit junction periphery

P = total junction perimeter ($PJ = PJ_{\text{eff}}$)

C_{JA} and C_{JP} are given as :

$$C_{JA} = C_J \left[1 + \frac{V_R}{PB} \right]^{-MJ} \quad \text{Eq. (2A)}$$

where

C_J = zero-bias junction capacitance / unit junction bottom well area

PB = area junction contact potential (typical value = 0.8V)

V_R = applied reverse voltage

MJ = area junction grading coefficient (typical value = 0.5)

$$C_{JP} = C_{JSW} \left[1 + \frac{V_R}{PBSW} \right]^{-MJSW} \quad \text{Eq. (3A)}$$

where

C_{JSW} = zero-bias junction capacitance / unit junction periphery (PJ)

$PBSW$ = $PB = 0.8V$

MJSW = periphery junction grading coefficient (typical value = 0.33)

Using BSIM3(v3.1) HSpice Model for P+ / NW diode (PDIO) in TSMC 0.25um CMOS technology, post-layout extraction for a single diode gives:

$$\text{PDIO : Area} = 1.7944\text{e-}12, \quad \text{PJ} = 3.52\text{e-}6 \quad \text{Eq. (4A)}$$

$$\text{NWDIO: Area} = 8.291\text{e-}9, \quad \text{PJ} = 318.4\text{e-}6$$

From Eq.2A and Eq.3A, when $V_R = 0\text{V}$,

$$C_{JA} = C_J = 1.931\text{e-}3 \text{ and } C_{JP} = C_{JSW} = 2.232\text{e-}10,$$

- **Case 1: (when $V_R = 0\text{V}$)**

From Eq.1A and Eq.4A, unit cell PN junction diode capacitance is :

$$C_J = (1.931 \times 10^{-3}) \cdot (1.7944 \times 10^{-12}) + (2.232 \times 10^{-10}) \cdot (3.52 \times 10^{-6})$$

$$C_J = 4.25\text{fF}$$

Total number of PN junction varactor diode (from layout extraction netlist) = $N = 416$

Therefore, total capacitance of PN junction varactor at zero_bias = $416 \times 4.25 \times 10^{-15} = 1.77\text{pF}$

- **Case 2: (when $V_R = 2.5\text{V}$)**

From Eq. 2A,

$$C_{JA} = (1.931 \times 10^{-3}) \left[1 + \frac{2.5}{0.8} \right]^{-0.4812} = 0.98 \times 10^{-3}$$

From Eq. 3A,

$$C_{JP} = (2.232 \times 10^{-10}) \left[1 + \frac{2.5}{0.8} \right]^{-0.324} = 1.41 \times 10^{-10}$$

Therefore, from Eq.1A and Eq.4A, unit cell PN junction diode capacitance is :

$$C_J = (0.98 \times 10^{-3}) \cdot (1.7944 \times 10^{-12}) + (1.41 \times 10^{-10}) \cdot (3.52 \times 10^{-6})$$

$$C_J = 2.25 \text{fF}$$

Therefore, total capacitance of PN junction varactor at 2.5V bias = $416 \times 2.25 \times 10^{-15} = 0.94 \text{pF}$

Hence, total capacitance variation from $V_R=0\text{V}$ to $V_R=2.5\text{V}$ is :

$$C_{\text{var}} = (1.77 - 0.94) \text{ pF} = 0.83 \text{pF}$$

(c) VCO#1 layout