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NOISE AND TRANSIENT ANALYSIS OF A FRACTIONAL-N PHASE-LOCKED
LOOP FREQUENCY SYNTHESIZER

by

WINSTON L. SORFLEET, B.ENG.

A thesis submitted to
the Faculty of Graduate Studies and Research
in partial fulfilment of
the requirements for the degree of
Master of Engineering

Ottawa-Carleton Institute for Electrical Engineering
Department of Electronics
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April, 1991

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PHASE-LOCKED LOOP FREQUENCY SYNTHESIZER"

submitted by Winston L. Sorfleet, B. Eng.

in partial fulfilment of the requirements for the degree of
Master of Engineering

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ABSTRACT

This thesis explores the implementation of a new fractional-N phase-locked loop frequency synthesis method. A sigma-delta modulator is used to control a dual modulus divider, thereby achieving fractional modulus division. This divider is placed in the feedback path of a phase-locked loop frequency synthesizer; hence, fractional-N frequency synthesis is achieved.

In the course of this study, a fractional-N phase-locked loop frequency synthesizer prototype was designed, built, and tested. This thesis examines the synthesizer's phase noise performance and transient response. By comparing the measured results to the ones predicted by simulation, the synthesis method and its model are validated.

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CHAPTER 1

INTRODUCTION

A frequency synthesizer is used to produce an output frequency or set of output frequencies on the basis of a stable reference frequency. A phase-locked loop (PLL) synthesizer system with a frequency divider in the feedback path is shown in Figure 1.1. The feedback action of the loop acts to keep the feedback phase ϕ_{BACK} matched to the reference phase ϕ_{REF} when in lock, and changes in the reference are matched by changes in the feedback signal. Hence the feedback frequency F_{BACK} and reference frequency F_{REF} are equal in steady state. Since F_{BACK} is simply the output frequency F_{OUT} divided by N , then after transients have settled F_{OUT} equals $N \cdot F_{\text{REF}}$.

It would be desirable to be able to tune the synthesized output frequency by changing the divider count, since F_{REF} is typically a high-stability fixed frequency source. However, the divider would only be able to be changed by fixed steps (say from N to $N+1$ to $N+2$), and none of the in-between frequencies could be synthesized. A fractional division scheme would be required.

Consider the case when a dual modulus (N or $N+1$) divider is used. Many such dividers are commercially available. By varying the divide count from N to $N+1$ and back in some fashion, it is possible to achieve a time averaged divide count somewhere in between; since the loop cannot respond

Figure 1.1 PLL frequency synthesis using feedback divider.

instantaneously to changes in the divider count, it must also settle on some intermediate value. What is needed is (1) a modulus switching scheme and (2) a proper choice of loop filter to control the PLL's response. Existing methods that implement the fractional division scheme include pulse swallowing, phase interpolation, and Wheatly random jittering.

Recently, a new method has been proposed at Carleton University by Riley et al. [1] which uses a second or higher order sigma-delta modulator (sometimes known as an oversampled analog to digital converter or OSA/D) to modulate the bit stream that controls the division ratio of the divider. This system is shown in Figure 1.2.

It is well known that a phase-locked loop's instantaneous frequency output is low-pass to the reference input; that is, the loop can track slow variations in the reference but does not respond to high frequency phase jitter. The loop's transient and frequency responses are determined primarily by the loop filter. It has been shown in various sources such as Rohde [2] that a step change in the divider count is equivalent to a corresponding change in the reference. Then, with good design, the loop will filter out any high-frequency jitter caused by the changing value of the divider, while passing the low-frequency average division ratio.

The second order sigma-delta modulator, as first proposed by Candy [3], takes a band-limited analog signal as input and produces a bit stream whose average value is proportional to

the input. In addition, due to the second order sigma-delta modulator's structure, the quantization noise is shaped in the frequency domain so that it is concentrated at half the sampling frequency but rolls off at approximately 40 dB per decade towards D.C. This noise is caused by the error in quantizing the output of the modulator into two discrete levels. The bit stream as viewed by a spectrum analyzer would contain both the analog input signal and quantization noise, but the noise would be shifted to high frequency. When this bit stream is used to control the dual modulus divider, the phase-locked loop will track the slowly varying analog input signal controlling the division modulus, while the high frequency quantization noise will be suppressed. Hence, a fractional division ratio with low phase jitter will be maintained.

In the course of preparing this thesis a prototype frequency synthesizer using a second order OSA/D to control the division ratio was designed, built, and tested. PLL frequency synthesis in general has been explored in Rohde [2] and Egan [13]. The primary goal of this work was to validate this fractional-N synthesis method experimentally and to characterize its transient and noise behaviour under sigma-delta modulus variation. Although some predictions had already been done on the sigma-delta frequency synthesizer architecture, certain questions still arose about the possibility of unpredicted behaviour which might only be

observed in an experimental verification, for example, possible effects of time delays from the sigma-delta modulator. Additionally, comprehensive closed loop measurements had never been conducted to verify the expected performance in fractional-N frequency synthesis mode. In summary, the central purpose of this thesis was to resolve some of the uncertainties through measurement and analysis.

A classic Candy double-integration sigma-delta modulator was used to control the divider because it has been well characterized both through work done at Carleton [5, 11] and in the published literature [3]. There are certain deficiencies in its performance which came to light (particularly undesired spectral impulses) during the course of this thesis. These are no reflection on the basic method of sigma-delta modulated fractional-N frequency synthesis since various techniques can be used to reduce such effects, for example higher order sigma-delta modulators. Such work, however, is outside the scope of this thesis.

Chapter 2 of this thesis discusses the structure and operation of this sigma-delta modulator when it is used as a bit stream generator. Chapter 3 presents the results observed in the transient response of the synthesizer and compares them to the theoretical predictions. Chapter 4 examines the noise measurements and compares them to levels predicted by theory. Finally, chapter 5 presents the conclusions and provides suggestions for areas of future study.

CHAPTER 2

OVERSAMPLED ANALOG TO DIGITAL CONVERTER

In order to achieve fractional-N division, a scheme to switch back and forth between divide moduli N and $N+1$, based on some input value, is required. Since there are only two divide values, one may look at the switching controller as an analog to digital converter of some sort. The mechanism used in this work is the sigma-delta modulator, sometimes known as the oversampled analog to digital converter.

2.1 DELTA MODULATION

In order to understand how the sigma-delta modulator works, it is helpful to examine its predecessor, the delta modulator. A basic linear delta-modulated transmitter and the corresponding receiver as given by Shanmugan [4] is shown in Figure 2.1. The transmitter consists of a quantizer (a hard limiter in this case) in the forward loop and an integrator in the feedback loop. The system is sampled-data, with the successive samples separated in time by the sampling period and held in-between. The feedback is arranged so that the output of the integrator approximates the input. The difference is fed to the quantizer. If the difference is positive, the feedback approximation of the input signal is too low, and the quantizer output is positive so the integrator output will rise to attempt to match the input

Figure 2.1 Delta modulation transmitter and receiver.

level. The reverse is true if the difference is negative. Thus the output $y(n)$ will consist of a stream of positive and negative pulses which indicate if the input signal $x(n)$ is increasing or decreasing. This can be easily represented by binary ones and zeroes. At the receiver, the $y(n)$ bit stream is integrated to form the approximate waveform. This in turn is passed through a low-pass filter, so that the signal $x'(n)$ is a good approximation of $x(n)$.

2.2 SIGMA-DELTA MODULATION

Sigma-delta modulation is a modified delta-modulation system where the input signal is integrated before being fed to the modulator. Since both the input and feedback signals are now integrated, the two integrators may be removed and replaced with a single integrator in the feedforward loop, as shown in Figure 2.2(a). Now the output of the modulator tracks the input $x(n)$ with some error introduced by the quantizer. The receiver of the sigma-delta modulated signal must now differentiate first, and since they are complementary operators, the differentiator and integrator cancel out, leaving only the low pass filter. In this work, the low pass filtering is part of the function of the phase-locked loop itself. Perhaps the greatest advantage of sigma-delta modulation systems is their ability to shift the quantization noise out of baseband, as will be shown.

The discrete-time version of the basic single-integration

(a) Sigma-delta Modulation

(b) Single-Integration Sigma-delta Modulator

(c) Candy's Quantizer Error Model

Figure 2.2 Single-integration sigma-delta modulation.

sigma delta modulator is shown in Figure 2.2(b). The integrator is realized using positive feedback of a delayed output signal V_1 . The negative feedback is accomplished with a single delay element, so the system should be well within the limits of stability as long as the sampling rate is much higher than the Nyquist rate of the input (hence the name "oversampled" analog to digital modulation). The delay in the feedback loop must be inserted because neither computer software nor hardware can evaluate instantaneous loops and because of the need to allow for realistic response time of the quantizer. The quantizer does introduce gross nonlinear distortions into the system. In order to calculate the transfer function for this (and other) sigma-delta modulators, the model shown in Figure 2.2(c) is used, where it is assumed that the quantizer noise can be modelled as a summation with a zero-mean error signal whose power spectral density is white. It is also assumed that the gain of the quantizer is unity. This is the model used in Candy's analysis [3]. Derivation of the transfer function is as follows:

$$\begin{aligned} y(n) &= V_1(n) + e \quad (y(n) = \text{sign}(V_1(n))) \\ V_1(n) &= x(n) - y(n-1) + V_1(n-1) \end{aligned} \quad (2.1)$$

Therefore, making use of the z transform,

$$\begin{aligned}
 V_1 &= \frac{x - yz^{-1}}{1 - z^{-1}} \\
 y &= \frac{x}{1 - z^{-1}} + e - \frac{yz^{-1}}{1 - z^{-1}} \\
 &= x + e(1 - z^{-1})
 \end{aligned}
 \tag{2.2}$$

Clearly, then, y/x is allpass, while y/e has a zero at $z=1$ and is therefore highpass, with a rolloff of 20 dB per decade from half the sampling frequency towards D.C.. If the sampling frequency is high enough then the quantization noise will be greatly attenuated in the baseband.

2.3 DOUBLE-INTEGRATION SIGMA-DELTA MODULATION

2.3.1 Operation

The quantization noise in baseband can be further reduced by multiple integration feedback loops. Figure 2.3 shows the sigma-delta modulator with two feedback loops as proposed by Candy [3]. The gains K_1 and K_2 are normally unity but may be scaled as desired. The net delay around the outer feedback loops is still one and inverting as in the single-integration sigma-delta modulator, so with oversampling, the system should remain stable. As before, the quantizer is assumed to introduce a noise source e for derivation of the transfer functions. Then

Figure 2.3 Double-integration sigma delta modulator.

$$\begin{aligned}
 V_1 &= x - yz^{-1} + V_1z^{-1} \\
 &= \frac{x-yz^{-1}}{1-z^{-1}} \\
 V_2 &= \frac{V_1 - yz^{-1}}{1-z^{-1}} \\
 y &= V_2 + e
 \end{aligned}
 \tag{2.3}$$

It is easy to show that

$$y = x + (1-z^{-1})^2 e \tag{2.4}$$

The transfer function y/x is still allpass. The transfer function to the error now has two zeroes at D.C., so the high-pass action will be an improvement over the single-integration sigma-delta modulation case (rolling off at 40 dB per decade instead of 20). Therefore the signal-to-noise ratio in baseband is increased. Though even higher orders are possible, only the double-integration sigma-delta modulator is used to control the divider in this work.

It is re-emphasized that the output of the modulator is directly proportional to the input. The lowest value allowed on the input is -1, corresponding to a bit stream sequence of all zeroes, while an input of +1 would correspond to all ones and an input of 0 would correspond to an equal amount of ones and zeroes.

2.3.2 Noise

Using Candy's assumptions, the noise caused by the quantizer can be derived. Assuming a uniform distribution of the error caused by the quantizer, the variance is

$$\sigma_e^2 = \frac{1}{12} q_i^2 \quad (2.5)$$

where q_i is the stepsize of the quantizer. Assuming this noise is white, the power is distributed uniformly from D.C. to half the sampling frequency of the sigma-delta modulator. Then the power spectral density (with a one ohm load) is

$$S_{\phi_e}(f) = \frac{1}{6f_s} q_i^2 \left[\frac{W}{Hz} \right] \quad (2.6)$$

and with the noise shaping function, assuming unity gain in the quantizer,

$$S_{\phi_{out}}(f) = |(1-z^{-1})^2|^2 S_{\phi_e}(f) \quad (2.7)$$

2.3.3 Operating Limitations

Due to the nature of the double-integration sigma-delta modulator, there are specific regions at the input where the modulator will not act properly. In a real

circuit, the integrators must not be forced to saturate or else the noise shaping action will break down. Saturation occurs in an analog circuit when the integrators try to assume output values in excess of the power supply rails, and in a digital circuit when the accumulator registers exceed their wordlengths. Empirical data shows that to avoid saturation it is sufficient to assure that (1) V_1 and V_2 are capable of assuming absolute values 2.5 times greater than K_1 and K_2 , and (2) the absolute value at the input $x(n)$ is never greater than $1/2$ [5]. This means that the frequency synthesizer's frequency output is limited to being in between $(N+0.25) \cdot F_{REF}$ and $(N+0.75) \cdot F_{REF}$ when in fractional division mode.

The noise shaping is also affected by finite sequence length effects when D.C. levels are applied as inputs. Consider the case when an exact value of zero (midrange) is applied as a D.C. input. The sigma-delta modulator will settle on a condition where the output is toggling high and low. The repetitive sequence length is only two. In the frequency spectrum, only two impulses will be seen: one at d.c (the fractional value of $1/2$) and one at $f_s/2$, rather than a continuous noise spectrum. Assuming no other sources of phase noise, the frequency synthesizer would output the desired fractional frequency $(N+0.5) \cdot F_{REF}$, plus large, undesired spectral impulses at

$N \cdot F_{REF}$ and $(N+1) \cdot F_{REF}$ as per frequency modulation theory. Similar cases will happen if an input level of $+1/2$ ($3/4$ range) is applied, except that there will be four evenly spaced impulses instead of two (corresponding to a sequence length of four instead of two). A finite sequence length will always be present if the input value and the initial integrator values are rational numbers and there is no external source of noise in the modulator. However, finite sequence length effects may be ameliorated by avoiding integer submultiples of one-half as input levels (e.g. 0, $+1/2$, $-1/2$, $+1/4$, $-1/4$, etc.) [5]. The longer the sequence length is, the more the collection of impulses in the frequency domain will resemble the desired continuous spectrum.

2.3.4 Implementation

The sigma-delta modulation used to control the dual modulus divider in this work was achieved by use of a computer and a bit stream circuit card. The bit stream card is capable of storing 2^{20} bits and outputting them as desired, in this case synchronized to the reference source (one bit per clock cycle). A computer program simulates the second-order sigma-delta modulator, storing the output data in an auxiliary file. After the simulation, the second program transfers the contents of the auxiliary file to the bit stream card. Because the

card can only store 2^{20} bits, the maximum sequence length will also be no more than 2^{20} . It is desirable to ensure that the sequence length for any particular input is an integer submultiple of this (i.e. a power of 2) or there will be a "rollover glitch", a discontinuity in modulation between the value of the last bit in the card and the first bit in the card, leading to an increasing phase and frequency error with time. Fortunately, this is relatively easy to achieve with a good choice of the input level. Because the dual modulus dividers used in this work divide by N when the control line is high and by $N+1$ when the control line is low, this simulated sigma-delta modulator inverts the bit stream output to compensate. Also, because it was desired to simulate a real sigma-delta modulator, the input levels used were always kept low enough to avoid the saturation of the integrators which could occur in a real circuit.

CHAPTER 3

TRANSIENT BEHAVIOUR OF THE FRACTIONAL-N FREQUENCY SYNTHESIZER

3.1 IMPLEMENTATION OF THE PHASE-LOCKED LOOP

In order to test the performance of the sigma-delta modulated fractional-N frequency synthesizer, a phase-locked loop was built. Design procedures for a PLL frequency synthesizer may be found in sources such as Rohde [2] and Egan [13]. This prototype system needed to have a minimal circuit complexity and commercially available components (to reduce the construction time). In addition, the system required good immunity to outside sources of noise to accurately correlate measurement with theory.

The complete circuit diagram is shown in Figure 3.1 and the simplified block diagram in Figure 3.2. In discussing the implementation and characterization of the loop it is useful to split up the system into three functional blocks: charge-pump phase detector and loop filter, voltage controlled oscillator, and divider. The charge-pump unit generates a control voltage V_c in proportion to the phase error between ϕ_{REF} and ϕ_{BACK} . The VCO adjusts the output frequency F_{OUT} and phase ϕ_{OUT} to follow the control voltage. The divider counts the zero crossings of the output signal and switches the state of the feedback signal ϕ_{BACK} every N cycles.

Figure 3.1 PLL frequency synthesizer circuit diagram.

3.1.1 Charge-pump phase detector

Because the reference signal and feedback signal from the divider are digital waveforms, a digital phase detector is required. Two choices were considered: a sample and hold phase detector and a sequential phase/frequency detector. The first choice was discarded because it required a separate high-frequency clock to generate a ramp voltage, and this violated the guideline of minimal circuit complexity. The phase/frequency detector was used instead because it includes a wide phase tracking range (the range that the phase error may assume without losing lock) and frequency-aided acquisition, as will be discussed. In addition, a commercial MC4044 PFD chip was readily available. This chip uses TTL-level inputs.

In the configuration used for this prototype, the 4044 has two inputs, reference phase ϕ_{REF} and feedback phase ϕ_{BACK} , and two outputs, PUMP UP and PUMP DOWN. As described by Gardner [6], either one or the other or neither of the outputs will be active depending on whether the feedback phase lags the reference, leads the reference, or is in perfect synchronization with the reference respectively. Both outputs will never be active at the same time.

Assume the first case, that the feedback phase lags the reference. The phase error is positive. On the

negative edge of ϕ_{REF} , the PUMP UP pulse (+0.75 volts nominal) will go active and remain active until the negative edge of ϕ_{BACK} . This signifies that the voltage-controlled oscillator must raise the output frequency so that the divided-down feedback phase can catch up to the reference.

In the second case the feedback phase leads the reference phase. The phase error is negative. On the negative edge of ϕ_{BACK} , PUMP DOWN (+2.25 volts nominal) goes active until the subsequent negative edge of ϕ_{REF} , when it disconnects. The voltage-controlled oscillator must lower the output frequency so that the divided-down feedback phase approaches the lagging reference.

If the feedback signal and reference are exactly in phase, the phase error is zero and both PUMP UP and PUMP DOWN are inactive (open circuit).

The above discussion applies when the loop is in lock and the phase error is small. Now consider the case when this is false and the reference frequency and feedback frequency are substantially different. Due to the internal logic of the PFD, either the PUMP UP or PUMP DOWN signals (depending on the sign of the frequency difference) will be periodically active, driving the VCO in the direction required to match the frequencies and bring the loop into lock. Hence the phase/frequency detector provides frequency acquisition when power is

first applied to the loop and it is initially out of lock. Details of the logic states internal to the PFD may be found in the various literature. It suffices here to mention that because of the internal memory, the sequential phase detector may theoretically maintain phase-lock within a relatively wide phase error window of -2π to $+2\pi$.

A charge pump follows the phase detector to convert the digital pulses to an analog control voltage for the VCO. The simplest charge-pump device is an integrating capacitor, corresponding to a loop filter with frequency-independent gain only, where the gain is in volts per time interval. Referring to Figure 3.3(a) [6], the PUMP UP signal may be used to switch a positive current source into the capacitor, resulting in a positive step in the control voltage. A PUMP DOWN signal switches a negative current source into the capacitor, resulting in a negative step in the control voltage. Naturally, the longer the pulse (i.e. the greater the phase error), the larger the step is in the control voltage. Typically, however, a somewhat more sophisticated loop filter is used, because it is not desirable to have unfiltered steps applied to the VCO (the reference clock feedthrough would be unacceptable).

For this prototype circuit, the voltage levels of the phase detector PUMP UP and PUMP DOWN pulses are used

Figure 3.3 Charge-pumps and loop filters.

directly to pump current into and out of an integrating feedback network as seen by examining Figure 3.1. This type of charge-pump configuration was chosen because a previous prototype using current sources and CMOS switches was found to have poor performance. Ignoring the Phase Offset control resistor for the moment, the phase detector and loop filter can be reduced to the simplified form shown in Figure 3.2. If a PUMP DOWN pulse is issued, a current of $+0.75/R_1$ is transferred into the feedback network, while an equal but opposite current is developed across the input resistor for a PUMP UP pulse. The output of the op-amp, which controls the VCO, slews downwards or upwards accordingly. The feedback network incorporates a high frequency pole, to reduce reference feedthrough pulses, and a stabilizing zero, which will result in a third-order Type II loop according to the terminology used by Gardner [7].

When testing the phase detector open-loop (by applying inputs with a controlled phase difference), several problems were encountered which required the addition of new circuitry. The first problem was caused by parasitic capacitances on the phase detector outputs. These outputs would turn on fast when active but would go to an open-collector condition when turning off. Hence there was a considerable tail added on to the pump pulse, yielding phase detector non-linearity. Resistors R_2 and

R_1 , were added to drag the outputs quickly to the neutral voltage (1.5 volts) when the outputs went inactive. This reduced the tail significantly.

The second problem discovered was that of the phase detector deadzone. Though not mentioned in most of the literature, this serious problem is inherent to the design of the phase/frequency detector and charge pump.

The deadzone is encountered when a phase error approaching zero is applied. Due to unavoidable delays such as logic propagation in the chip, the phase/frequency detector has difficulty in determining whether the phase difference is positive or negative, and this results in very narrow, non-linear pump pulses yielding high phase jitter. This effect can be reduced with good circuit design (such as elimination of pulse tails as described above) and is not that significant when the transient phase error is passing rapidly through the zero point. However, in steady state, the loop tries to track the phase error to zero, which is in the nonlinear deadzone region. In order to counter this problem, a Phase Offset control resistor R_2 was added. In every cycle of the reference a constant amount of current is drained off or injected into the summing point at the inverting input of the op-amp. In order to keep equilibrium, the loop must maintain a non-zero phase error whose average current input exactly compensates for

the effect of the Phase Offset resistor. Adjustment of the Phase Offset control can set the steady-state phase error to any value within the $+2\pi$ to -2π phase window, though in practice it is kept fairly close to zero to maximize the allowable phase error transient peak. The Phase Offset control also allows the average output voltage of the phase detector to be measured for known, stable phase errors when the loop is closed. This is necessary for accurate measurement of the phase detector characteristic.

As a final implementation note, the op-amp used for the prototype circuit, the OP27, is a low-noise device with internal offset compensation and a slew rate sufficient to drive the VCO and the feedback network.

3.1.2 Voltage-controlled oscillator

The core of the voltage-controlled oscillator (VCO) is the MC1648 oscillator chip, which oscillates at the resonant frequency of the network at its input. This network consists of a hand-wound coil and two back-to-back varactor diodes. A varactor diode is a device whose capacitance is an approximately linear function of the voltage across it. As capacitors, the two diodes form a series pair in parallel with the coil. This produces a resonant frequency:

$$\omega_{VCO} = \frac{1}{\sqrt{LC}} \quad (3.1)$$

$$C = C_0 - kV_C$$

The intended range of frequency for this VCO is 50 MHz to 55 MHz; although higher frequencies are possible if the control voltage is large, the VCO gain becomes less linear.

Resistors R_7 and R_8 form a voltage divider whose purpose is to ensure that the varactor diodes can never be forward-biased, which would prevent the VCO from operating properly. Transistor Q_1 is used to isolate the VCO chip output from the BNC output of the synthesizer so that line reflections do not feed back and cause the frequency divider to misinterpret the true VCO phase. As well, it protects the main circuit from accidents such as short-circuiting of the output to ground.

3.1.3 Frequency divider

The frequency divider chip used in this synthesizer is the SP8789 dual modulus divider, which divides by 20 when the control input is high and by 21 when the control input is low. When used with a reference frequency of 2.5 MHz, the output frequency range is 50 MHz to 52.5 MHz, which is within the range that the VCO is designed for.

The SP8789 divides the fundamental frequency at its

input, F_{OUT} from the VCO, by counting the positive-going zero crossings and cycling its output, F_{BACK} , every 20 (or 21) VCO cycles. The output is a TTL-compatible digital signal fed to the MC4044 phase/frequency detector. The input signal amplitude is controlled by voltage divider resistors R_9 and R_{10} and is A.C. coupled to meet the specifications of the divider chip. When used as a fractional divider, the OSA/D drives the modulus control with a bit stream clocked by the reference frequency.

3.1.4 Other implementation details

This prototype frequency synthesizer was built using mostly wire-wrapped components. This was done to allow circuit modifications to be made easily. The disadvantage of wire-wrap is that it is more prone to noise and parasitics which go up with frequency. Because of this, the choice of reference frequency and output frequency (2.5 MHz and 50 - 52.5 MHz) was kept low. Future versions of this synthesizer design could have a higher choice of frequencies if the system were implemented on a printed circuit board.

Additionally, the circuit layout was designed to minimize crosstalk and parasitic effects where possible. Certain key paths, including the high frequency connection from the voltage-controlled oscillator to the frequency divider and the longer paths to the external

system inputs and outputs, were done using shielded coaxial cable instead of the more vulnerable wire-wrap. The VCO coil was surrounded by a copper shield to prevent it from picking up extraneous signals. The frequency synthesizer circuit board made use of a ground plane and was enclosed by a steel box.

The MC4044 phase/frequency detector, the MC1648 VCO chip, and the SP8789 frequency divider all used separate +5 volt regulated supplies to eliminate crosstalk between components along the power rails. Decoupling capacitors were used wherever a stable D.C. level had to be established and on all the power supplies. In order to eliminate 60 Hz noise on the power supplies, a battery was first used; however it was found that most batteries could not drive the 50 MHz output into a 50 ohm load for very long. Instead, a second stage of regulation was introduced between the +5 volt regulators and the external A.C. powered supply. This was sufficient to suppress the 60 Hz ripple.

3.2 CHARACTERIZATION OF SUBCIRCUITS

In order to assemble the fractional-N frequency synthesizer transfer functions, it is convenient to first individually characterize the subsystems mentioned in the previous section. This is done by matching Laplace domain transfer functions to the sub-blocks' models.

3.2.1 Charge-pump

As explained previously, the PUMP UP and PUMP DOWN pulses from the MC4044 phase/frequency detector generate a voltage difference V_p across the input resistor R_i . A corresponding current I_p is fed into the feedback path of the op-amp. The feedback device for a pure charge pump would be a single capacitor, so that the current input would be integrated to raise or lower the output level of the op-amp. Since the phase difference is sampled data (one pulse every period of the reference signal), however, this would result in unacceptable reference feedthrough into the VCO, not to mention practical problems such as slew rate limiting. Therefore a different feedback topology is used, one which incorporates both a high frequency pole to reduce feedthrough and a stabilizing zero.

The PUMP UP/DOWN pulses are applied for a time t_p equal to the time difference between ϕ_{REF} and ϕ_{BACK} . Then the average error current pumped in one cycle is

$$i_d = -I_p \frac{t_p}{T_{REF}} = -I_p \frac{\phi_{ERROR}}{2\pi} \quad (3.2)$$

It is easy to show that the combined transfer function of the phase detector and loop filter is then

$$\begin{aligned}
 F(s) &= \frac{V_C(s)}{\phi_{\text{ERROR}}(s)} = \frac{-I_d(s)Z_f(s)}{\phi_{\text{ERROR}}(s)} = \frac{I_p}{2\pi} \times Z_f(s) \\
 &= \frac{1}{2\pi} \frac{V_p}{R_f} \frac{sC_1R_3+1}{s(C_1+C_2) \left(s \frac{C_1C_2}{C_1+C_2} R_3+1\right)} \quad (3.3)
 \end{aligned}$$

with the essential underlying assumption being that the sampled-data nature of the phase detector can be approximated with a continuous time model.

The measured phase detector characteristic is shown in Figure 3.4. Actual phase hold-in range is slightly less than ± 340 degrees. The true phase detector gain is about $V_p = 0.504$ volts per $\phi_{\text{ERROR}} = 2\pi$ radians for positive phase errors and 0.645 volts per 2π radians for negative phase errors. The capacitor values were measured in-circuit as accurately as possible at 2.5 MHz (the reference frequency), with an estimated error of about $\pm 3\%$, based on variation of measured values with different test equipment. It is assumed in deriving the transfer function that the op-amp gain is infinite and that the delays caused by logic propagation in the phase detector and parasitic capacitances are negligible.

Using the measured values, there is a pole at zero frequency, a stabilizing zero at 8151 Hz, and another pole at 105 KHz to help suppress reference feedthrough and OSA/D quantization noise. With a division ratio of 20.5 and an assumed VCO gain of 5.4 MHz / Volt, HSPICE simulation shows the unity-gain frequency of the open

Figure 3.4 Phase detector characteristic.

Table I Charge-pump parameter values

Parameter	Selected Value	Measured Value
C_1	10 nf	8.875 nf
C_2	820 pf	749 pf
R_1	2.7 K	2.7 K
R_3	2.2 K	2.2 K
V_p	0.75 V	0.504 / 0.645 V

loop is about 17 KHz, with a phase margin of about 56 degrees, as shown in Figure 3.5 and Figure 3.6. The open-loop HSPICE simulation model uses voltages to represent all signals, with a perfect integrator for the VCO as shown in Figure 3.7. Subsequent tests show errors in using this model, but for stability calculation purposes it is sufficient.

3.2.2 Voltage-controlled oscillator

The frequency vs. voltage gain of the voltage-controlled oscillator was found, by applying an adjustable voltage source to the input and using a spectrum analyzer to measure the output frequency. In the desired VCO tuning range of 50 MHz to 55 MHz this gain is approximately linear (approximately 5.38 MHz per volt at 51.25 MHz), as shown by the slope of the graph contained in Figure 3.8. Nevertheless, it has been

Figure 3.5 Open-loop gain of phase-locked loop.

Figure 3.6 Open-loop phase of phase-locked loop.

Figure 3.7 HSPICE open-loop frequency response model.

Figure 3.8 VCO frequency vs. voltage characteristic.

found, in the course of measurement of the transient response to a step change, that the VCO gain should be re-calculated in the locality of the target frequency (assuming a fast settling time). This is because small differences in this gain lead to a noticeable increase in error between the predicted transient response and that determined experimentally. With this in mind, the transfer function of output phase to input control voltage is expressed as

$$\frac{\phi_{out}(s)}{V_c(s)} = \frac{K_v(f)}{s} \quad (3.4)$$

where K_v is the frequency-dependent voltage-controlled oscillator gain. The resistor-varactor diode combination at the input of the VCO does create a pole, but its corner frequency is high enough to be ignored.

3.2.3 Frequency divider

Whether the frequency divider divides by 20 or 21 depends on the control input (which for fractional division is driven by the sigma-delta modulator). The divider counts the positive-going zero crossings of the input signal from the voltage-controlled oscillator and switches state on the output every 20 (or 21) VCO cycles. There is however a delay between the information presented to the divider and the phase detector. If a

change occurring in F_{OUT} is passed through the divider's internal logic just before the phase detector samples, then there is no delay. On the other hand, if this change is still propagating through the divider when the phase detector samples, then there is a delay of one reference period in the divider. On average, the delay is one half of one reference period. Then the transfer function is

$$\frac{\phi_{BACK}(s)}{\phi_{OUT}(s)} = \frac{e^{-s\frac{T}{2}}}{N} \quad (3.5)$$

where N is the current division ratio and T is the period of the reference frequency. Subsequent MATLAB simulations show that this effect does not affect the synthesizer response significantly, but the term is included for accuracy.

3.3 DERIVATION OF SYNTHESIZER TRANSFER FUNCTIONS

Now that the transfer functions of the sub-blocks have been derived, an overall transfer function from the input reference phase $\phi_{REF}(s)$ to either the instantaneous frequency output $F_{OUT}(s)$ or the phase error $\phi_{ERROR}(s)$ may be formed. Knowledge of the instantaneous frequency output for a given input is of course the primary goal of this analysis, while knowledge of the phase error as a function of time is necessary in order to assure that the phase detector does not

lose lock.

Actually, the transient input to the loop is applied to the divider rather than to the phase reference input. However, Rohde [2] has shown that a step change in the divider count from N_1 to N_2 is equivalent to a step change in the input frequency of value $(N_2 - N_1)/N_2$ times the constant frequency reference F_{REF} . A step change was used to determine the transient response as it can easily be applied to the input and included in a Laplace domain model (as a $1/s$ term). Furthermore, response to a step change is a commonly accepted method of characterizing a system.

When switching the divider from the old modulus N_1 to the new modulus N_2 , the output phase can be seen to be

$$\phi_{OUT}(s) = \frac{K_V}{s} \cdot F(s) \phi_{ERROR}(s) \quad (3.6)$$

and the phase error term is

$$\begin{aligned} \phi_{ERROR}(s) &= \phi_{REF}(s) - \phi_{BACK}(s) \\ &= \phi_{REF}(s) - \frac{e^{-s\frac{T}{2}}}{N_2} \phi_{OUT}(s). \end{aligned} \quad (3.7)$$

Substituting equation (3.6) into (3.7), the phase error is

$$\phi_{ERROR}(s) = \frac{\phi_{REF}(s)}{1 + \frac{K_V}{s} F(s) \frac{e^{-s\frac{T}{2}}}{N_2}} \quad (3.8)$$

The equivalent phase input at the reference for a step change in the divider modulus from N_1 to N_2 is

$$\phi_{REF}(s) = \frac{1}{s} \cdot \frac{(N_2 - N_1)}{N_2} \cdot \frac{F_{REF}}{s} \quad (3.9)$$

where F_{REF} is the constant frequency reference. Incorporating this and equation (3.3) into (3.8), then

$$\phi_{ERROR}(s) = \frac{\frac{(N_2 - N_1)}{N_2} F_{REF}}{s^2 + \frac{K_V}{2\pi} \frac{V_P}{R_I} \frac{e^{-s\frac{T}{2}}}{N_2} \frac{sC_1R_3 + 1}{(C_1 + C_2) \left(s \frac{C_1C_2}{C_1 + C_2} R_3 + 1 \right)}} \quad (3.10)$$

from which the transient phase error response to a divider change can be derived by taking the inverse Laplace transform.

The Final Value Theorem confirms that the transient phase error settles to zero as expected:

$$\lim_{t \rightarrow \infty} \phi_{ERROR}(t) = \lim_{s \rightarrow 0} s \phi_{ERROR}(s) = 0 \cdot \frac{\frac{N_2 - N_1}{N_2} F_{REF}}{\frac{K_V}{2\pi} \frac{V_P}{R_I} \frac{e^{-s\frac{T}{2}}}{N_2}} \quad (3.11)$$

By multiplying the phase error through the charge-pump and voltage-controlled oscillator transfer functions, the output frequency of the loop is found to be

$$F_{OUT}(s) = s \cdot \Phi_{OUT}(s) = K_V F(s) \Phi_{ERROR}(s)$$

$$= \frac{\frac{K_V}{2\pi} \frac{V_P}{R_I} \frac{sC_1R_3+1}{s(C_1+C_2) \left(s - \frac{C_1C_2}{C_1+C_2} R_3 + 1 \right)} \frac{(N_2-N_1)}{N_2} F_{REF}}{s^2 + \frac{K_V}{2\pi} \frac{V_P}{R_I} \frac{e^{-sT}}{N_2} \frac{sC_1R_3+1}{(C_1+C_2) \left(s - \frac{C_1C_2}{C_1+C_2} R_3 + 1 \right)}} \quad (3.12)$$

The Final Value Theorem may be applied to equation (3.12) as well, yielding

$$\begin{aligned} \lim_{t \rightarrow \infty} F_{OUT}(t) &= \lim_{s \rightarrow 0} s F_{OUT}(s) = F_{OUT}(t=0) \\ &= (N_2-N_1) F_{REF} + N_1 F_{REF} \\ &= N_2 F_{REF} \end{aligned} \quad (3.13)$$

as expected.

3.4 EVALUATION OF LAPLACE DOMAIN MODEL

MATLAB numerical methods procedures were used to calculate the theoretical transient response of phase error and instantaneous frequency output. The MATLAB inverse Laplace Transform routine was written by Richard J. Griffith of Carleton University, and its accuracy for this application was confirmed using an HSPICE equation model.

Originally, an HSPICE model which closely approximated the actual system topology, as shown in Figure 3.9, was used to simulate the phase transient response. Gain constraints on the amplifiers and node termination resistors were necessary to achieve convergence. However the HSPICE response did not match that predicted by the inverse Laplace Transform routine. A new HSPICE model, shown in Figure 3.10, was used to confirm the accuracy of the MATLAB prediction. Node termination resistors are left out for simplicity here. The output signal of this model is

$$\phi_{\text{ERROR}}(s) = \frac{A}{sC_1R_1+1} \frac{sC_2R_2+1}{s^2C_3L+sC_3R_3+1} \frac{B}{sC_4R_4} \quad (3.14)$$

which yields one real pole and two complex poles, a zero, and another pole for the integration from frequency to phase. Then with proper values for the variables, (3.14) will be equal to (3.10). The appropriate component values for the measured loop parameters may be calculated using the formula for solutions of a third-order equation.

The three responses to a 20 to 21 divider step are shown in Figure 3.11. The original HSPICE model was discarded because the relaxation of constraints necessary to obtain convergence resulted in a significant error. The equation-based HSPICE model and the MATLAB routine were in reasonable agreement with each other. However, the MATLAB routine was used for all subsequent simulations as it did not require

Figure 3.10 HSPICE Laplace equation model.

Figure 3.11 Comparison of transient response predictions.

lengthy manual calculations and could easily incorporate the exponential delay term in the divider, which the HSPICE equation model could not. Furthermore, it was judged to be somewhat more accurate than the HSPICE equation model because of the latter's gain constraints and termination resistors.

3.5 COMPARISON OF MEASURED AND THEORETICAL TRANSIENT RESULTS

Measurement of the experimental transient response was done using the HP5372A Time Interval Analyzer. This device is capable of directly measuring the instantaneous frequency of a signal or the phase error between two signals. The HP5372A determines "edges" of an input signal as defined by a trigger level. These edges are counted with a 150 ps rms timing error (that is, the rated uncertainty jitter for the HP5372A is 150 ps rms). An internal time counter is used to keep track of the time elapsed since the last sample interval. At the next sample interval, the number of counted edges (events) can be compared to the time counter to find the average period or frequency. Likewise, the phase difference between two signals can be calculated. It is important to note that many events may occur within a sample interval. If the interval is small, then the uncertainty (caused by the 150 ps rms phase jitter) proportional to the interval length is larger. Therefore, a practical limitation exists in that the accuracy of the measurements goes down as the interval between samples is decreased. However the sample interval should not be made too

large or else there will be insufficient data on rapidly changing instantaneous signal frequencies or phases. For this particular study, sample intervals of 0.4 microseconds for phase error and 1 microsecond for frequency error were used. Since the reference frequency is 2.5 MHz, the phase error sampling rate is maximum. This sampling interval was chosen so that all pulses at the phase detector could be observed (the time interval analyzer was synchronized to the reference frequency). Uncertainty in the measured jitter caused by the time interval analyzer was acceptably low for this choice. For the frequency measurement, however, a smaller sampling interval than one microsecond resulted in unacceptable random jitter in the measurements, while larger intervals would result in less time resolution.

3.5.1 Integer Step: N to N+1

Before proceeding to fractional division, the accuracy of the transient model was confirmed. This was be done by comparing the predicted transient response to a step from 20 to 21 (and 21 to 20) with the experimental response obtained by toggling the control input to the divider. No OSA/D effects were introduced as yet. The time interval analyzer was synchronized to the reference frequency. After the divider was switched to the new modulus, the phase difference between ϕ_{REF} and ϕ_{BACK} was measured. The time interval analyzer inputs were set to

trigger at the 50% points of these signals. The predicted and measured transient phase errors resulting from a 20 to 21 step are shown together in Figure 3.12. The solid line represents the predicted response based on the theoretical model and the dashed line represents the experimentally measured response. Because it is impossible to take the inverse Laplace transform of a transfer function with nonlinear gain, the theoretical result was based on what the phase detector gain was going to be during most of the phase error excursion as predicted by an approximate simulation. With this in mind, the Phase Offset Control resistor was set to maximize the linear range; however, with the maximum phase error being so close to 360° , there was little room to manoeuvre without exceeding the phase detector limit and cycle-slipping.

The predicted and experimentally measured transient phase error to a step change in the divider from 21 to 20 is shown in Figure 3.14, obtained in a similar fashion as described above.

Transient instantaneous frequency was measured with the time interval analyzer as well. The trigger level was the 50% point as before. The response to a 20 to 21 step is shown in Figure 3.13, and to a 21 to 20 step in Figure 3.15. Note that the very slight jitter in the measured curve was caused by the time interval analyzer

Figure 3.12 Theo. and experimental phase error, 20 to 21 step.

Figure 3.13 Theo. and expt. o/p frequency, 20 to 21 step.

Figure 3.14 Theo. and experimental phase error, 21 to 20 step.

Figure 3.15 Theo. and expt. o/p frequency, 21 to 20 step.

frequency measurement system rather than the phase-locked loop itself. This conclusion was justified by the fact that no corresponding jitter is observed in the transient phase error, which is directly correlated to the transient instantaneous frequency.

Taking into account the variation in loop gain caused by the phase detector and voltage-controlled oscillator nonlinearities, the measured transient phase error and instantaneous frequency responses compared very well to the predicted ones. This validated the phase-locked loop model derived above.

3.5.2 Fractional Step: N_1 to N_2

The phase-locked loop equations derived above may also be applied to a fractional change in the divider. Here, the sigma-delta modulator input is resting at one value corresponding to divider count N_1 , and it is stepped up (or down) to a new value corresponding to divider count N_2 . The density of ones, in the modulator output bit stream controlling the divider, corresponds to the input value. Hence the average value of the bit stream is stepped. Assuming that the quantization noise in the sigma-delta modulator is filtered out, the transient response to the fractional step may be evaluated in exactly the same manner as the integer step.

Keeping the input levels of the sigma-delta

modulator such that N_1 and N_2 are confined to the range $N+0.25$ and $N+0.75$ guarantees that the modulator will not saturate. As well, the standard second-order sigma-delta modulator does not perform well on integer submultiples of 2, so the $N+0.5$, $N+0.25$ and $N+0.75$ levels should be avoided, as explained in Chapter 2. To test the fractional division, two sets of values were used: $N+0.41$ to $N+0.63$ and $N+0.2501$ to $N+0.7499$. The first pair can be used to represent a fairly typical step, while the second pair approaches the defined saturation limits.

Figure 3.16 shows the theoretically predicted and actual transient phase error for the $N_1 = 20.41$ to $N_2 = 20.63$ step. The quantization noise is quite evident and fairly large as the divider is driven from 20 to 21 and back in rapid succession. However, the loop could not instantaneously track changes in the divider, and the average measured phase error matched that predicted for a true fractional divider step. The quantization noise was greatly suppressed by the loop filter before passing on to the voltage-controlled oscillator, as the transient instantaneous frequency response shows in Figure 3.17.

Figure 3.18 shows the predicted and measured phase error for the 20.2501 to 20.7499 step. Compared to the smaller 20.41 to 20.63 step, there was a much higher degree of correlation in the quantization noise, making it appear as though there was a distinct beat note. This

Figure 3.16 Phase error, 20.41 to 20.63 fractional step.

Figure 3.17 Instantaneous frequency, 20.41 to 20.63 step.

Figure 3.18 Phase error, 20.2501 to 20.7499 fractional step.

is because the limits are very close to integer submultiples of two (0.25 and 0.75). The instantaneous frequency response is shown in Figure 3.19.

The transient phase error and frequency responses to steps in the opposite direction ($N_1 = 20.63$ to $N_2 = 20.41$ and 20.7499 to 20.2501 , respectively) are shown in Figure 3.20 through Figure 3.23. They are very similar to the equivalent positive steps save that the sizes of the peaks are smaller, due to the higher phase detector gain (0.687 volts per 2π radians as opposed to 0.453).

As an observation, the phase error response to a fractional step from 20.25 to 20.75, using pulse swallowing, is shown in Figure 3.24. The density of ones in the divider bit stream is forced from three in four to one in four at the time of the step. Sigma-delta randomization is removed. A clear beat-note at one fourth of the reference frequency is now present showing one of the deficiencies of this method.

As a result of the transient measurements, it may be concluded that the models used to predict the transient response are accurate. For fractional steps, it is seen that the average measured phase error at the phase/frequency detector matched the prediction with additional noise introduced by the sigma-delta modulator. This quantization noise is removed from the instantaneous frequency output by the loop filter.

Figure 3.19 Instantaneous frequency, 20.2501 to 20.7499 step.

Figure 3.20 Phase error, 20.63 to 20.41 fractional step.

Figure 3.21 Instantaneous frequency, 20.63 to 20.41 step.

Figure 3.22 Phase error, 20.7499 to 20.2501 fractional step.

Figure 3.23 Instantaneous frequency, 20.7499 to 20.2501 step.

Figure 3.24 Phase error, pulse swallowing 20.25 to 20.75 step.

CHAPTER 4

NOISE PERFORMANCE OF THE FRACTIONAL-N FREQUENCY SYNTHESIZER

4.1 DEFINITION OF PHASE NOISE

In this frequency synthesizer, as in any real circuit, there are sources of noise. The various noise sources create a fluctuation on the instantaneous frequency output of the voltage-controlled oscillator. For a frequency synthesizer, phase noise may be defined as that random noise on the output additional to the ideal signal. The term "phase" noise is used to describe the phase fluctuation in the output frequency. The output signal in terms of voltage is

$$V(t) = A \sin(\omega_c t + \theta_e(t)) \\ = A \sin(\omega_c t) \cos(\theta_e(t)) + A \cos(\omega_c t) \sin(\theta_e(t)) \quad (4.1)$$

where, in phase, $\omega_c t$ is the desired carrier term and $\theta_e(t)$ is the phase error term. Equation (4.1) assumes that there is no amplitude noise present in the output signal. The usual assumption for a frequency synthesizer is that phase noise effects are greater than amplitude noise effects [8]. For illustrative purposes, consider first the simple case where the phase error term is itself a sinusoid at frequency ω_n so that

$$\theta_e(t) = \theta_n \sin(\omega_n t) \quad (4.2)$$

Now if the amplitude of this phase error is small,

$$\begin{aligned} \text{if } \theta_e < 1 \\ \cos(\theta_e(t)) &= 1 \\ \sin(\theta_e(t)) &= \theta_e(t) = \theta_e \sin(\omega_e t) \end{aligned} \quad (4.3)$$

then the output signal is

$$V(t) = A \sin(\omega_c t) + A \cos(\omega_c t) \cdot \theta_e \sin(\omega_e t) \quad (4.4)$$

The first term in (4.4) is the ideal output signal at the synthesized carrier frequency, while the second term is caused by phase error. The second term would place one spur of amplitude $\frac{1}{2}\theta_e A$ offset by ω_e radians on either side of the carrier in the voltage spectrum. Phase error (and phase noise) effects are always symmetric about the carrier.

Similar arguments apply if the phase error is a noise spectrum instead of a discrete frequency. In this case, there will be a continuous noise spectrum on both sides of the carrier instead of a spur. This spectrum, expressed in terms of power spectral density, would be in units of Watts per Hertz. This is defined as the two-sided power spectral density. Some texts add the frequency components on the left side of the carrier to the right side, effectively doubling the power. All the phase noise is then considered to be contained in only one sideband. This is defined as the one-sided power spectral density.

For a frequency source, the practice is to express the ratio of power in the sideband caused by phase noise to the power in the carrier, rather than expressing the phase noise in terms of absolute power. The units would then be radians² / Hz. The definition of phase noise used in this thesis is the phase noise spectrum $\mathcal{L}(f)$ used by Hewlett-Packard [8]. This spectrum is equal to one half of the one-sided power spectral density, or one sideband of the two-sided power spectral density, measured in decibels relative to the power in the carrier (dBc / Hz). This is a convenient definition as it allows $\mathcal{L}(f)$ to be measured directly on a spectrum analyzer as long as the small angle criterion discussed above is met. A commonly accepted limit is that the total standard deviation from the mean of the instantaneous phase, integrated up to some offset from the carrier, must be less than 0.2 radians [9]. Then, at 1 Hz from the carrier, the $\mathcal{L}(f)$ measured by the spectrum analyzer is a valid representation of the true $\mathcal{L}(f)$ only if

$$\mathcal{L}(f) \leq 10 \log_{10} \left(\frac{0.2 \text{ rad}}{2\pi \text{ rad}} \right) = -30 \text{ dBc} \quad (4.5)$$

At larger offsets from the carrier, the limit of valid measurement will decrease by 10 dB per decade, because the total phase standard deviation integrated up to the offset must be less than 0.2 radians. An example from Hewlett-Packard [8] is shown in Figure 4.1. Above the line, the true

Figure 4.1 $L(f)$ limit of validity using spectrum analyzer.

$\epsilon(f)$ cannot be measured by the spectrum analyzer. Instead, a phase noise measurement must be made with a system such as the HP3048A or HP537A.

4.2 MEASUREMENT OF PHASE NOISE

Three phase noise measurement methods were used in this thesis: measurement by the HP4195 Network Analyzer, measurement by the HP5732A Time Interval Analyzer, and measurement by the HP3048 Phase Noise Measurement System. Each method had its advantages as summarized below, and each was used when appropriate to the type of measurement.

4.2.1 HP4195 Network Analyzer

The HP4195 Network Analyzer may act as a high-frequency (up to 500 MHz) spectrum analyzer. By sweeping from the frequency synthesizer's nominal output frequency to the highest frequency of interest, and normalizing by the resolution bandwidth (RBW), the power spectral density of the phase noise may be observed. The normalization is necessary to convert from what power the spectrum analyzer observes in a resolution bandwidth window [dBm] to what is really a power spectrum distributed across this bandwidth [dBm / Hz]. With narrow enough resolution bandwidths, a white noise distribution can be assumed within the RBW of the spectrum analyzer. By subtracting from this the value of

the power measured in the carrier, the phase spectrum may be derived (except when very close to the carrier, where the measured $f(f)$ exceeds the limit imposed by the small angle criterion). This method has great advantage in its simplicity. An additional attraction is that the 4195 is fully programmable, allowing programmed sweeps according to a measurement point set table. One disadvantage of the HP4195 is that it has a relatively poor noise floor, only about -130 dBm. With the measured power in this frequency synthesizer's carrier approximately equal to -5 dBm, this translates to a noise floor of -125 dBc. The other disadvantage is that it cannot measure $f(f)$ above the (-30 dBc minus 10 dB per decade) limit described in Section 4.1.

4.2.2 HP5372A Time Interval Analyzer

The HP5372A time interval analyzer may be controlled by a Phase Noise and Jitter program provided by Data Physics Corporation so as to measure phase noise up to a specified frequency. The HP5372A counts the zero crossings of the VCO output signal and stores the corresponding time of crossings. After a batch of measurements are complete (the maximum being 8192 measurements), the PNJ program extrapolates the average rate of change of phase (one zero crossing corresponding to 2π radians) versus time. Then, the deviations of the

individual measurements may be compared to the average slope. Taking an 8192-point FFT of the deviations will yield the phase noise spectrum.

There is a noise floor caused by the 150 ps rms jitter of the time interval analyzer. The jitter relative to the true period of the measured wavetform will cause a phase variance:

$$\sigma^2_{\pi} = \frac{150\text{ps}}{T_{\text{signal}}} \cdot 2\pi \text{ [radians}^2\text{]} \quad (4.6)$$

It is also known that the variance is equal to the power in the spectrum:

$$\sigma^2 = \int_0^{BW} N_1 df \quad (4.7)$$

Assuming that the measurement noise floor is white, then its value may be calculated from equations (4.6) and (4.7):

$$N_1 = \frac{\sigma^2}{BW} \quad (4.8)$$

The bandwidth of measurement is equal to one-half the sampling frequency specified by the PNJ program. The lowest noise floor would occur with a maximum (10 MHz) sampling frequency; however, with only 8192 samples to work with, this would yield rather large (10 MHz / 8192)

spacings between frequency measurements. Hence, the sampling frequency should be chosen to accommodate the desired measurement range.

Although the noise floor of the HP5372A is rather high (that is, poor), the PNJ system has one very attractive advantage: measurements are taken very quickly compared to other methods. This allows phase noise measurements of drifting sources (such as an open-loop VCO); since the total measurement time is so short, the sources will not have time to drift significantly. Furthermore, what little drift there is may be detected by the HP5372A and removed mathematically.

4.2.3 HP3048A Phase Noise Measurement System

The HP3048A is actually a large software program provided by Hewlett-Packard and run on an HP Basic microcomputer. Using the General Purpose Interface Board bus, it can control an HP11848 phase detector, HP8863 frequency source, and HP3561 dynamic signal analyzer. The overall system is known as the HP3048A phase noise measurement system. The system configuration used in this work is shown in Figure 4.2. The Device Under Test (DUT) generates a frequency signal at frequency F_{out} . The HP8863A provides a synchronized signal at the same frequency. These two signals are mixed together sinusoidally by the 11848 phase detector, and the second-

Figure 4.2 HP3048A phase noise measurement system.

order terms are rejected. The baseband signal is fed to the HP3561 dynamic signal analyzer, which is essentially an all-digital spectrum analyzer. By mixing the output signal of the DUT down to baseband with a high-precision low-noise phase detector, $\phi(f)$ is extracted accurately.

Of the three phase noise measurement systems discussed, the HP3048A is by far the most precise and has the lowest noise floor (below -140 dBc). There are three disadvantages. First, the DUT and the frequency generator must be in perfect synchronization. Because the HP11848 uses a sinusoidal phase detector, its linear range is small and any beat-note will render it useless (the phase detector is designed to pick up very small fluctuations between two locked signals; large fluctuations such as a beat-note will exceed its range of linearity). Second, the HP11848A phase detector cannot measure signals below 5 MHz. Third, and most important, the HP3561 and HP3048A in combination try to differentiate between the "true" phase noise spectrum and what are perceived to be signal spurs (i.e. power signals). They can sometimes make erroneous assumptions in deciding which are which. A case in point is shown in Figure 4.3. Here, the sigma-delta modulator was used to allow fractional synthesis. Because there is a finite sequence length in the sigma-delta modulator bit stream, the phase "noise" is contained in evenly spaced spurs, as

Figure 4.3 HP3048A with fractional-N phase noise effects.

described in Chapter 2. The dynamic signal analyzer measured the total energy in each frequency window. Depending on the placement of the FFT measurement window, more spurs (and hence more energy) were present in some of the windows than in others. The system displayed the higher-energy windows as if they contained spurs and the lower-energy windows as if they contained true continuous phase noise. The only way to avoid this problem is to measure and display each spur individually, which the HP3048A could not be programmed to do. Therefore, this system cannot be used to measure the phase noise of the frequency synthesizer in fractional-N mode. It might however be usable if the sequence length were longer.

4.3 SOURCES OF PHASE NOISE

There are three primary contributions of phase noise in the prototype frequency synthesizer used in this work: noise from the frequency reference source, noise from the voltage-controlled oscillator, and noise caused by the sigma-delta modulator (fractional mode only). Compared to these, all other noise contributions (from the PLL circuit components) are assumed to be insignificantly small (this assumption was justified in the subsequent measurements). If a better (lower noise floor) frequency reference source were used, however, then close-in phase noise in the phase detector itself would be visible in comparison. Noise from the reference source and

VCO are truly random processes and are caused by electrical properties such as flicker, shot, and thermal noise phenomena [10]. Noise caused by the sigma-delta modulator is external to the loop and pseudo-random in nature; it may be completely predicted for a digital sigma-delta modulator when the initial conditions are known. Therefore the first two are dealt with separately before proceeding to the third.

4.3.1 Noise from Frequency Reference Source

The reference signal to the frequency synthesizer is provided by an HP3325 frequency generator. To measure its phase noise contribution to the prototype synthesizer, the HP3048A Phase Noise Measurement System was used for maximum accuracy. Although normally run at 2.5 MHz when acting as the reference source to the synthesizer, the generator frequency was increased to 5 MHz to meet the minimum requirements of the HP11848 phase detector as discussed previously. Test measurements by the HP4195 spectrum analyzer show that there is no noticeable difference between the phase noise when the generator is running at 5 MHz as opposed to 2.5 MHz. The result of the HP3048A measurement of the reference source is shown in Figure 4.4. The spurs in the figure are at multiples of 60 Hz.

Figure 4.5 shows the transfer function (in dB) from the phase noise at the reference input to the synthesizer

Figure 4.4 Phase noise from frequency reference source.

Figure 4.5 Transfer function to frequency reference.

output. Knowing in general that

$$S_{\phi_{out}}(f) = |H(f)|^2 S_{\phi_{in}}(f) \quad (4.9)$$

then the phase noise power at the reference input will be amplified at the synthesizer output by 26 dB up to the corner frequency of 30 KHz, after which it rolls off at 40 dB per decade.

4.3.2 Noise from Voltage Controlled Oscillator

Because the unlocked voltage-controlled oscillator's nominal frequency drifts rapidly (hundreds of hertz fluctuation every second), the phase noise and jitter analysis program with the HP5372A time interval analyzer must be used. Each measurement is limited to 8192 frequency windows (from an 8192 point FFT) as explained previously, and since these frequency windows should not be inappropriately large, a number of measurements had to be taken. These measurements are shown in Figure 4.6 through Figure 4.9, with their corresponding noise floors as specified by Hewlett-Packard (recalling that the noise floor of the HP5372A depends on the sampling frequency). The last of the measurements used the minimum noise floor (corresponding maximum sampling frequency of 10 MHz) which intersects $f(f)$ at about 80 KHz, so the VCO phase spectrum could not be measured accurately beyond this

Figure 4.6 VCO phase noise spectrum, 1 to 100 Hz.

Figure 4.7 VCO phase noise spectrum, 10 to 1000 Hz.

Figure 4.8 VCO phase noise spectrum, 100 to 10000 Hz.

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MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS
STANDARD REFERENCE MATERIAL 1010a
(ANSI and ISO TEST CHART No. 2)

Figure 4.9 VCO phase noise spectrum, 1 to 100 KHz.

Figure 4.10 Estimated VCO phase noise spectrum.

point. It was noted that the actual performance (noise floor) of the HP5372A at high frequency was about 18 dB better than HP's specifications. Figure 4.10 shows the VCO phase spectrum obtained from estimating and averaging the overlaps of the successive phase noise measurements. The transfer function (in dB) from the unlocked (open-loop) VCO to the closed-loop synthesizer output is shown in Figure 4.11.

Measurement of the phase noise spectrum of the synthesizer output (without sigma-delta modulation, fixed divide ratio = 21) was done using the HP3048A. The results are shown in Figure 4.12, together with the predicted effects of the reference source (neglecting the spurs at multiples of 60 Hz) and the voltage-controlled oscillator. Within about 3 dB, they are in close agreement.

4.3.3 Noise from Sigma-Delta Modulation

In measuring the phase noise caused by sigma-delta modulation, the reference frequency was chosen to be 2.62144 MHz, output frequency 53.7408 MHz, requiring divide ratio $20 + 0.50048828125$. This divide ratio was chosen because it allows the sigma-delta modulator to operate very close to the middle of its range (recalling that a divide ratio of $20 + 0.5$ exactly will cause the noise shaping action to break down for a second-order

Figure 4.11 Transfer function to VCO.

Figure 4.12 Unmodulated synthesizer phase noise spectrum.

modulator due to the short sequence length). Also, with this choice of divide modulus, the modulator output bit stream sequence length is 4096 (the average of the 4096 bits being 0.50048828125 exactly, and then the sequence repeats). This is useful when doing FFT analysis.

Assuming that the error caused by the quantizer is uniformly distributed and white, Candy provides an approximation to the shaped quantization error spectrum [3]:

$$Q(f) = q_I \sqrt{\frac{2}{3f_{REF}}} \left[1 - \cos\left(2\pi \frac{f}{f_{REF}}\right) \right] \quad (4.10)$$

where q_I is the quantization interval: 1 unit interval or 2π radians. This shaped spectrum is derived from the $(1 - z^{-1})^2$ term caused by feedback. Then the phase noise in the divider is given by [1]

$$S_\phi = \left[\frac{f_{REF}}{f} \frac{Q(f)}{N} \right]^2 \quad (4.11)$$

where N is the divide modulus, approximately 20.5. Equation (4.11) also takes into account the integration from frequency to phase in the frequency divider. It must be remembered that because of the non-infinite sequence length of the modulator bit stream, this noise is not a true continuous spectrum but rather a collection

of 4096 frequency impulses evenly spaced from 0 to f_m Hz away from the carrier. Therefore the theoretical phase noise should be shifted up by a factor of $2.62144e6/4096 = 640$ when compared to the measured level of the frequency impulses.

Unfortunately, it is now well known that Candy's assumptions of uniform distribution, white phase noise, and unity gain in the quantizer are incorrect [11]. The true power spectral density may be found by analyzing the output bit stream sequence. The 4096 bits of the sequence were captured and integrated over time (since the divider value is a function of previous bits integrated over time). The integrated bit stream is shown in Figure 4.13 with the D.C. component removed. Taking the FFT of the integrated bit stream, its power spectral density may be found:

$$\begin{aligned}
 S_f(f) &= \sum_{n=-\infty}^{\infty} |F_n|^2 \delta(f - nf_0) \\
 &= \sum_{n=-2048}^{2048} \left| \frac{X_n}{4096} \right|^2 \delta(f - nf_0)
 \end{aligned}
 \tag{4.12}$$

where the X_n are the discrete Fourier series coefficients of the integrated bit stream and f_0 is the fundamental frequency of 640 Hz. This power spectral density is itself a repetitive sequence as per sampling theory.

Figure 4.13 Integrated sigma-delta modulator bit stream.

Figure 4.14 Phase noise spectrum in divider.

Then the phase noise spectrum in the divider is

$$S_{\phi}(f) = \left[\frac{f_{REF}}{f} \frac{2\pi}{N} \right]^2 S_f(f) \quad (4.13)$$

where the factor of 2π is to convert from unit intervals in the divider to radians. The phase noise spectrum in the divider was calculated and is compared to Candy's predictor in Figure 4.14. There is a significant difference between the two, although both of them have the predicted 20 dB/decade slope (40 dB per decade from the sigma-delta modulation minus 20 dB per decade caused by the integration from frequency to phase in the divider). Therefore Candy's predictor is discarded, and the spectrum as directly calculated by FFT is used henceforth.

In order to measure the effects of the sigma-delta modulation on the phase noise spectrum of the frequency synthesizer's output, the power relative to the carrier was measured at each of the 4096 frequency points using a 10 Hz resolution bandwidth on the HP4195 spectrum analyzer. This small bandwidth was necessary in order to ensure that the phase noise spectrum from other sources (namely the reference source and the voltage-controlled oscillator), which are true, continuous phase noise spectrums, did not contribute significantly to the power measured in the resolution bandwidth window. For

example, at 640 Hz, the phase noise caused by these other sources is approximately -90 dBc/Hz (referring back to Figure 4.12). Then the power contribution in a 10 Hz window would be -80 dBc. As long as the power in the corresponding phase noise spur caused by the sigma-delta modulator is well above this value, the measurement is valid.

The transfer function from the frequency synthesizer output to the phase noise in the divider is exactly the same as from the frequency reference source, barring a change in sign. The theoretically predicted levels of the phase noise spurs caused by the sigma-delta modulator were compared to those actually measured as described above. The results are presented in Figure 4.15 and Figure 4.16. This is of course a power spectrum as opposed to a power spectral density, since the effects of the finite sequence length sigma-delta modulator used here cause frequency spurs instead of a continuous spectrum as mentioned before. Within the 1.5 dB error range on the HP4195 spectrum analyzer, the theoretical predictions are in good agreement with the measurements for the majority of the higher-valued frequency spurs only. For the lower-valued spurs, the random phase noise caused by the voltage-controlled oscillator and the frequency reference source renders the measurement inaccurate. Another way of saying this is that the

Figure 4.15 Power spectrum of phase noise spurs (close-in).

Figure 4.16 Power spectrum of phase noise spurs from GSA/D.

values of the lower noise spurs from the sigma-delta modulator are below the noise floor of the other sources. The phase noise power spectral density caused by the VCO and frequency reference source is plotted together with the phase noise power spectrum caused by the sigma-delta modulator in Figure 4.17, and their respective contributions are

$$S_{\phi_{out}}(f) = \left| \frac{F(s) \frac{K_V}{s}}{1 + F(s) \frac{K_V}{s} \frac{e^{-s\frac{T}{2}}}{N}} \right|^2 (S_{\phi_{ref}}(f) + S_{\phi_{div}}(f)) + \left| \frac{1}{1 + F(s) \frac{K_V}{s} \frac{e^{-s\frac{T}{2}}}{N}} \right|^2 S_{\phi_{vco}}(f) \quad (4.14)$$

As a result of the phase noise measurements, it may be concluded that the noise caused by the quantizer error in the sigma-delta modulator is indeed shifted out of baseband and into the higher frequencies. This is translated to high frequency phase noise in the divider and is attenuated by the phase-locked loop in a predictable and controllable fashion.

Figure 4.17 Phase noise effects in PLL frequency synthesizer.

CHAPTER 5

CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE STUDY

In the course of this thesis, a prototype phase-locked loop frequency synthesizer using a second-order sigma-delta modulator to implement fractional division was designed, built, and tested. The model described in Chapter 3 was experimentally verified. It was seen that the sigma-delta modulator could indeed be used to implement a fractional division ratio in the dual modulus divider, and that a step change between fractional division ratios caused a corresponding step in the phase error and instantaneous frequency output as predicted by theory. The fractionally stepped phase error contained visible fluctuation caused by the noise in the sigma-delta modulator's quantizer; these fluctuations were removed by the loop filter leaving a smooth response in the instantaneous frequency output, as desired.

In Chapter 4, the noise sources in the frequency synthesizer were examined. There were two significant sources of phase noise ever present in the loop: noise from the frequency reference source, and noise from the voltage-controlled oscillator. Both sources' contribution to phase noise on the instantaneous frequency output were in agreement with the theoretical predictions. In addition, the error caused by quantization in the sigma-delta modulator also introduced noise into the phase-locked loop when the loop was

operating in fractional division mode. This noise contribution differed from what the theory predicted using Candy's formula; however, it was in agreement with the results expected after taking an FFT of the bit stream of the sigma-delta modulator. This noise was actually a power spectrum of impulses with shaped amplitudes rather than a continuous noise power spectral density, due to finite sequence length effects in the sigma-delta modulator bit stream.

Several observations can be made from this thesis. It was seen that the loop filter did indeed suppress the quantization noise from the oversampled analog to digital converter. A narrower bandwidth could be used to further reduce this noise, but this would mean that the phase noise contribution from the voltage-controlled oscillator would increase. Therefore when deciding the bandwidth of the closed-loop system, a balance of priorities must be made, taking into account the expected phase noise contributions from the voltage-controlled oscillator and the sigma-delta modulator. When in fractional division mode, this synthesizer's noise performance is poor, but it would improve if a better sigma-delta modulator and / or voltage-controlled oscillator were used.

When designing a frequency synthesizer like this one, it is important to choose the feedforward gain and divider ratio so that the phase excursions will not exceed the range of the phase detector and cause cycle-slipping. The phase detector

itself should not be allowed to settle in a non-linear region such as the deadzone of a charge-pump. A higher-order loop filter could be used to achieve sharper cutoff. This would greatly attenuate the quantization noise effects outside of the passband, though it has implications for the system's complexity and stability.

Given that this frequency synthesis method has been validated, there are many possibilities for future study. Closer examination of the sigma-delta modulator could certainly be productive. It would be desirable be able to have an expectation on the bounds of the quantization noise and the effects of finite sequence length without having to resort to empirical data, so that future designers will be able to calculate how much suppression is required. Higher-order sigma-delta modulators (using three or more feedback loops) could be experimented with to reduce the quantization noise in baseband even further. Multiple-modulus dividers driven by sigma-delta modulators with multiple-level quantization could be examined; several recent sigma-delta modulator designs using summed and cascaded modulators have higher-order rolloffs and therefore better noise shaping [12]. Modifications of the sigma-delta modulators so that the sequence length is longer (for instance, stages with gains that approach irrational numbers) should also be investigated to reduce the finite sequence length effect.

The demonstrated ability of the frequency synthesizer to

step from one output frequency to another raises the prospect of using the synthesizer to perform frequency-shift keying. Furthermore, because the oversampled analog to digital converter pushes the quantization noise into high frequency, low-frequency analog signals as well as pure D.C. levels may control the divider. This means that by applying a modulating waveform to the input of the OSA/D, frequency and phase modulation can be achieved. The maximum input frequency would only be limited by (1) the cutoff frequency of the phase-locked loop and (2) the maximum frequency where the quantization noise effects are deemed to be too large. If a higher reference (and therefore sampling) frequency is selected, this second limiting value will also become higher, and the loop filter could become wider (reducing the phase noise contribution from the voltage-controlled oscillator as well). This would allow the phase-locked loop frequency synthesizer to be used for wideband frequency modulation.

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