**Linearization Studies for Radio Frequency Power Amplifiers in SiGe
Technology for Wireless Infrastructure Applications.**

by

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A thesis submitted to the Faculty of Graduate Studies and Research
in partial fulfillment of the requirements for the degree of
Master of Applied Science.

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ABSTRACT

Two studies of linearization techniques, namely predistortion and transformer feedback, for radio frequency power amplifier in CDMA IS-95 wireless applications are studied. In the first study, a novel active and adjustable predistortion circuit is designed, simulated and fabricated in IBM 5HP SiGe technology. This is the first reported variable active predistortion circuit design in HBT SiGe technology with an adjustable positive gain expansion and positive phase expansion characteristic. The active predistortion circuit is a common emitter amplifier with Schottky diode degeneration. The nonlinear Schottky diode provides the expansion characteristics of the predistortion. By applying this active predistortion to a power amplifier, a reduction of 8dB in intermodulation distortion level has been achieved for a two-tone signal. In the second study, monolithic transformers are studied and characterized. A conceptual circuit using double-loop monolithic transformer feedback is proposed to linearize transistor amplifiers.

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1 Introduction

1.1 Tradeoffs in Power Amplifier Design

Amplifiers have always been central components of communications systems because of the need to compensate for the inherent losses suffered by signals during transmission. From a receiver standpoint, low noise amplifiers (LNAs) restore the signal amplitude or power to levels sufficiently above the noise levels that the receiver is able to accurately retrieve the data from received signals. From a transmitter standpoint, high power amplifiers (HPA) boost the signals to the required levels that allow the end receiver to be able to receive the transmitted signals with good fidelity after suffering from many communication channel losses. All amplifiers are inherently non-linear devices. A non-linear device is a device whose output signal is not a linear function of the input signal. This nonlinear behaviour of amplifiers causes the output signal to exhibit amplitude and phase distortions. In most modern modulation schemes, the signals are modulated in both amplitude and phase so any amplitude and/or phase distortions on the signals reduce the ability to decode these signals properly.

Today, system engineers prefer complex modulation schemes such as Quadrature Phase Shift Keying (QPSK)/ Offset Quadrature Phase Shift Keying (OQPSK) and $\pi/4$ -DQPSK because of their efficient use of bandwidth. However, a signal modulated using such schemes has a non-constant envelope [Appendix A] and hence is susceptible to

nonlinearities in the radio transmitting and receiving devices. For applications where bandwidth efficiency is not an issue, constant envelope modulation schemes such as FSK are used. Radio signals modulated using the constant envelope modulation schemes are the least susceptible to radio nonlinearities. As a result, the system's components can operate at or near their compression levels without affecting performance. At the other extreme, radio signals are affected the most by nonlinearities when they are modulated with Quadrature Amplitude Modulation (QAM).

Power amplifiers are potentially a large contributor to signal distortion in a radio transmitter chain. A challenge at hand is to design linear PA with low amplitude and low phase distortions to operate in wireless systems with very high linearity requirements. To design a linear PA, circuit designers face several problems. The first problem is power back-off. To meet the required linearity, it is typical that a PA is operated at power levels from 6-10dB below its 1dB compression point, hence "power back-off". This method is widely used but requires a more expensive higher power amplifier to compensate for the required power back off. In addition, more PA stages might be required in the transmit chain to achieve the output power level thereby increasing overall system cost.

Other problems are PA power efficiency and device bias requirements. These problems go hand in hand as PA efficiency and linearity depend greatly on the device bias point. A linear PA, such as a class-A amplifier, is generally very inefficient in its use of power. This in turn causes extra current drain on the power supply. Power added efficiency (PAE) is a common term used to characterize this PA efficiency and is defined as the following:

$$PAE = \frac{P_{RFout} - P_{RFin}}{P_{DC}} \quad (1.1)$$

where P_{RFout} is the fundamental RF output power, P_{RFin} is the RF input power, and P_{DC} is the DC power consumed by the PA.

A power amplifier biased in class-A configuration exhibits the best linearity but has the lowest PAE. In class-A, the transistor is biased at exactly in the middle of its active operating region. As long as the RF_{in} signal never drives the device into compression so that there is no clipping of the output voltage, the ideal class-A amplifier has perfect linearity. Other biasing configurations with higher PAE include class AB, class B, and class C. These classes obtain high PAE by biasing the transistor at a low quiescent point between the middle point (as in class-A) and cutoff. The RF_{in} signal then swings the device into conduction between a half to a full cycle. This causes the device to draw less current per cycle since it only conducts current when it is in the conduction period. Since these amplifiers are operated in a nonlinear region, harmonic filtering must be applied to their outputs to minimize distortion. Table 1.1 summarizes the efficiency and linearity characteristics of these amplifier classes.

Table 1-1: Efficiency and Linearity characteristic of class A, AB, B, and C PAs [3]

PA Class	Conduction Angle	Max Theory Efficiency	Linearity
A	360°	25% - 50% ¹	High
AB	180° – 360°	50% - 78.5%	Medium
B	180°	78.5%	Medium
C	0° – 180°	78.5% - 100%	Low

In wireless radio systems, PAs are used at both terminals of the system, i.e. base station and mobile terminal. In the mobile terminal, the efficiency is of much greater concern since the battery power must be minimized. Unlike the mobile terminals, the

¹ 25% efficiency is achieved with resistive load. 50% efficiency is achieved with a tuned LC tank.

efficiency in the base station is less important and high linearity is much more important due to the near-far effect in the radio systems [4]. The near-far effect arises when a mobile terminal receives both the desired signal from a base station, and one or more interference signals from other base stations. When the mobile terminal is closer to the interference base station than the desired base station, the strong interference signal can cause strong intermodulation distortion (IMD) signals next to the desired signal. Hence the base station transmitter must have outstanding linearity to keep IMD signals low enough so that the mobile terminal can detect and decode the transmitted signal correctly. In this thesis, a class-A PA is emphasized for CDMA IS-95 base station applications. Since a PA in a base station transmitter operates at much higher power level than that in a mobile terminal, lowering the PA nonlinearity distortions while preserving its efficiency is equivalent to reducing overall system cost.

1.2 Thesis Objectives

The objective of this research is to gain an understanding of the various linearization techniques available for PAs and to implement novel circuits to linearize transistor amplifiers to be used in a CDMA IS-95 wireless system. To achieve this objective, practical circuits from four linearization techniques will be studied. Novel circuits are proposed for predistortion and feedback techniques.

1.3 Thesis Contributions

The first major contribution the author made in this study is a novel variable active PRD circuit. To the best of the author's knowledge, this active PRD, which employs HBT transistors and Schottky diodes, has not yet been proposed in the literature. The second contribution is the proposal and study of a conceptual double-loop transformer feedback circuit to linearize a transistor amplifier.

1.4 Thesis Outline

The remaining chapters of the thesis are summarized as follows. Chapter 2 discusses common PA linearization techniques such as feedback, feedforward, predistortion (PRD), and postdistortion (POD). Chapter 3 presents three experimental class-A Darlington pair amplifiers and a design of a novel variable active PRD circuit. Chapter 4 is concerned with transformer feedback. Several transformers are designed on-chip and equivalent circuits are developed for them from simple measurements. Conceptual double loop transformer feedback circuits to linearize HBT transistor amplifiers are also described which will be further studied in the next level. Chapter 5 concludes this thesis with recommendations for future work.

2 Linearization Techniques

Many different power amplifier linearization techniques are available to circuit designers. These techniques can be classified into four categories: (1) feedback; (2) feedforward; (3) predistortion; and (4) postdistortion. Each of these categories contains several different methods, which are very unique on their own. These categories and methods are presented in the remaining sections of this chapter. Their advantages and disadvantages are also highlighted and summarized at the end of the chapter.

2.1 Feedback

Feedback is arguably the oldest amplifier linearization technique. Introduced in 1937 by H.S. Black [5], the first feedback circuit consisting of an amplifier and a resistor connected in a closed loop system. The feedback resistor samples a portion of the output signal and feeds this sampled signal back to the input. At the input, the sampled signal is subtracted from the input signal to create an error signal, which is the input to the amplifier. The gain and distortion of the amplifier with feedback are both lowered by the closed loop gain. This common circuit and its analysis are well known in literature so will not be discussed here. It is worth noting that the feedback network not only reduces

the amplifier's distortion but also stabilizes the amplifier over temperature and aging effects.

Over the last decades, many types of feedback topologies have been developed and they can be sorted into two different types: 1) feedback for a single transistor or a compound transistor amplifier and 2) feedback for a system's PA. The first type of feedback includes simple passive feedback and transformer feedback. The second type of feedback involves more complex circuits such as active feedback, envelope feedback, polar loop feedback, and Cartesian loop feedback. The feedback topologies from these two types as well as their recent designs in the literature are presented in the following sections.

2.1.1 Passive Feedback

Passive feedback involves only passive elements such as resistors, capacitors, and inductors in the feedback circuit. This feedback circuit either feeds back a sample voltage or current of the output to the input. Three most common passive feedback circuits are series feedback, shunt feedback, and a combination of series-shunt feedback. The circuit schematics of these feedback circuits around a single transistor are illustrated in Figure 2.1.

Figure 2.1: Types of passive feedback around a single transistor: a) series feedback (degeneration), b) shunt feedback, c) series-shunt feedback.

Consider a one-stage common emitter bipolar transistor amplifier with collector resistor R_c , emitter resistor R_E , and feedback resistor R_F . The transistor itself has transconductance g_m , small-signal input conductance between base and emitter g_π , and capacitor C_π . The voltage gains for resistive feedback circuits applied to a bipolar transistor have been derived in the literature [6] and are given here for reference:

$$\left(\frac{v_{out}}{v_{in}} \right)_{series_feedback} = \frac{-g_m R_c}{1 + \frac{g_m}{g_\pi + \frac{1}{R_E} + j\omega C_\pi}} \quad (2.1)$$

$$\left(\frac{v_{out}}{v_{in}} \right)_{shunt_feedback} = \frac{\frac{R_c}{R_F} - g_m R_c}{1 + \frac{R_c}{R_F}} \quad (2.2)$$

$$\left(\frac{v_{out}}{v_{in}} \right)_{series_shunt_feedback} = \frac{-g_m (R_c // R_F)}{1 + g_m R_E} \quad (2.3)$$

The feedback resistor has reduced the common emitter amplifier gain, $g_m R_c$ and introduced additional noise. However, the feedback resistor greatly improves the transistor linearity [3] and stabilizes transistor gain. Resistive feedback could be applied around two or more transistors to further improve linearity [6]. However, the gain and phase margin are greatly reduced by larger loop gain and phase shift around the loop. Instability will be an issue if phase margin becomes small. In all of these feedback circuits, the improvement in linearity is achieved by sacrificing the amplifier's gain. If the transistor's gain can be made large enough and additional noise does not exceed the design specifications then passive resistor feedback is a simple and effective method in reducing transistor nonlinearity. Also, common design techniques such as replacing the degeneration resistor with an inductor or adding a parallel capacitor with the degeneration resistor can reduce noise and improve gain at high frequency. Analyses of these frequency selective circuits are much more involved than purely resistive feedback; interested readers are encouraged to refer to references [3][7][8].

2.1.2 Transformer Feedback

Transformer feedback, also known as lossless feedback, was introduced and patented by David E. Norton in 1971 [9][10] as an alternative solution to resistive feedback. Compared with resistive feedback, lossless transformer feedback is completely noise-free and non-dissipative. Hence the noise figure of the transistor is preserved. The configuration of transformer feedback in a common-base amplifier is illustrated in Figure 2.2 [10]:

Figure 2.2: Transformer coupled common base amplifier.

Norton [9], [10] reported an improvement of 1.9dB in noise figure and 4dB in linearity using this transformer feedback amplifier. Trask [11] further employed this circuit with passive augmentation (also transformer feedback) and measured another 5dB in linearity improvement for a common base amplifier. In [14], Trask used transformer feedbacks in a double-balanced active mixer to enhance linearity and noise as shown in Figure 2.3. The author has used common-base configuration in this active mixer as an RF

(or IF) input stage to realize the feedback in [10] [11] and measured almost 15dB improvement in IIP3 in comparison with a simple Gilbert cell mixer.

Figure 2.3 Lossless feedback double-balanced active mixer.

Analyses of the common base amplifier transformer feedback have been presented in the literature [12] [13]. The transformer's performance and behavior are studied based on its S parameters. It is reported that S_{33} has the greatest impact on performance of a transformer feedback amplifier. A 5% change in S_{33} amplitude and phase (where port 3 is the collector terminal of the common-base transistor amplifier) causes 22% and 15.1% change in the amplifier's gain, respectively. Other S parameters either have no impact or little impact on the transformer feedback amplifier's

performance. In [12][13], transformer feedback offers good noise figure and good linearity; however, it only operates at low frequency range up to 570MHz [13]. This is mainly due to the presence of the transformer parasitic capacitance at high frequency. A drawback to this transformer feedback circuit is a strict requirement on reflection coefficient S_{33} . The tolerance in S_{33} (both amplitude and phase) must be less than 5% to achieve a small ripple in the amplifier's gain. This requirement can be very challenging since S_{33} varies largely with a change in the frequency.

In the past few years, transformer feedback topology has been used extensively in LNA designs [15], [16], [17], [18] in both bipolar and FET technology to achieve excellent noise figure, impedance match, gain and linearity. Long [18] proposed the first transformer feedback LNA design for use in a 1.9GHz narrow band receiver as shown in Figure 2.4, (complete bias network is not shown). The feedback is achieved by mutual inductive coupling from the transistor output at the collector of transistor Q_1 back to the emitter to improve transistor linearity and stabilize transistor gain against temperature and aging effects. The low frequency power gain of the transistor is proportional to square of the transformer turn ratio, which is more stable than transistor gain. The primary winding inductor of the transformer at the transistor emitter can be used to obtain a minimum noise figure and maximum power transfer at the input (matched input impedance) under certain conditions. The author measured a higher IP3 by at least 4dB with this design than LNAs fabricated using a GaAs process and biased under similar conditions [18]. In [15], Cassan reported a novel FET gate-drain capacitance neutralization method by using transformer feedback. The feedback design resulted in a cascode LNA designed for Wireless Local Area Networks (WLAN) at 5.75GHz with

measured IIP3 higher by 8dB than other LNAs designed using a different process and biased under similar conditions. In [17], an attempt was made to design a double-loop negative feedback LNA to provide inherent matched input impedance and to achieve good gain and noise performance. The authors presented an analysis of a LNA with two feedback loops, but only one comprises a monolithic transformer. While many efforts were done to characterize the impedance, noise figure and gain of the LNA, little analysis was presented for the intermodulation distortions of the LNA.

Figure 2.4: Transformer feedback LNA.

A novel concept of Transformer Feedback Degeneration (TFD) LNA has been recently introduced in [16]. The authors proposed a new input impedance model and an orthogonal input power matching condition (matched to both real and imaginary of the input impedance). The concept was validated in simulation, however, little comment on intermodulation distortions was made.

2.1.3 Active Feedback

Unlike passive feedback where a form of voltage division is employed, active feedback employs a small (auxiliary) amplifier in its feedback path. This auxiliary amplifier provides a small gain hence less output power is sampled through the feedback network. In addition, the auxiliary amplifier itself might generate some distortion, which is added with the input signal. If this distortion signal is properly adjusted in magnitude and phase, the amplifier's distortion could be further reduced. This extra distortion cancellation is somewhat similar to the predistortion method, which will be discussed in section 2.3.

Perez et. al. [19] designed an active feedback amplifier and reported a gain drop of 3.25dB while achieving linearity improvement of 12dB. A drawback to this active feedback circuit is the dependency of IMD3 cancellation on the input signal power. The auxiliary amplifier and coupler are adjusted at a particular condition to achieve the above improvement. However, at an input power other than the specified level, the improvement in IMD3 might be lower. Another drawback is the auxiliary amplifier's sensitivity to temperature and time since a small change in this amplifier's gain greatly affects the IMD3 cancellation. This can be fixed by adding an adaptive gain control circuit, but this will increase the size and cost of the overall amplifier. A system diagram of this active feedback is illustrated in Figure 2.5.

Figure 2.5: Active feedback circuit employing auxiliary amplifier.

2.1.4 Envelope Feedback

Envelope feedback detects and feeds back only a sample of the envelope of the output signal. This envelope feedback is most often used in AM transmission (such as AM radio power amplifiers), where amplitude distortion must be minimized. In digital modulation schemes such as QPSK, this technique is of little use since phase distortion is not being compensated. Phase distortion is present in all power amplifiers to some degree due to AM/PM conversion.

Nevertheless, some work has been done using envelope feedback to compensate for $\pi/4$ -shift QPSK modulation signal [20]. The proposed method achieves a high efficiency (50%) but little improvement in linearity. The envelope of this circuit is generated arithmetically using a special envelope generator, which is rather complicated. Moreover, the phase distortion is not compensated for in this circuit. As a result, the amplifier operates in backoff mode by 3.5dB from its saturated power to minimize the

output phase-shift caused by AM/PM conversion. The common circuit schematic for this envelope feedback is shown in Figure 2.6.

Figure 2.6: Block diagram envelope feedback circuit with a RF PA.

2.1.5 Polar Loop

Unlike envelope feedback, which does not compensate for phase distortion, polar loop feedback takes into account both envelope and phase distortion. The circuit diagram of a polar loop is plotted in Figure 2.7 [21] and its operation is explained as follows. The RF output signal is sampled and down converted to an IF signal, which is then resolved into amplitude and phase using a limiter and a demodulator. The demodulator-2 gets the output of the limiter-2 to detect unlimited input signal and performs coherent amplitude detection. The output of demodulator-2 is compared with the output of the demodulator1, which is similar to the output of the demodulator-2, by a differential amplifier. The

This polar loop resolves the phase problem encountered by envelope feedback. However, the required bandwidths of the amplitude feedback circuit and the phase feedback circuit are limitation which prohibit the use of the polar loop in practice. In most modulation schemes, the bandwidths of the amplitude feedback circuit and the phase feedback circuit are different. As the gain-bandwidth product is a constant for a particular loop, this limits the loop gain of amplifiers to either that of the amplitude or phase feedback loop. As a result, a compromise must be made in designing the loop gain

and bandwidth. If the amplitude feedback loop is optimized to reduce amplitude distortion, the phase distortion might get worse or vice versa.

In spite of the above limitation, Petrovic and Gosling [22] modified the polar loop and achieved an IMD level of -54dB for a narrow band (3kHz) SSB transmitter in simulation. The authors further improved the circuit and lowered the bandwidth from 200kHz to 50kHz to ensure stability. This circuit had an IMD level of -66dB relative to the peak envelope power (PEP).

2.1.6 Cartesian Feedback

Cartesian feedback, which was proposed in 1983 by Petrovic [23], has two major advantages over polar loop feedback: reducing the need for a PLL and eliminating the requirement of different feedback loop bandwidths. The circuit diagram of a Cartesian feedback circuit is shown in Figure 2.8.

Both polar loop feedback and Cartesian feedback are feasible linearization techniques for a complete transmitter rather than for a single transistor amplifier. The circuits shown in Figures 2.7 and 2.8 are complicated and very large in size including not just an amplifier but many other components such as local oscillators, phase shifters, modulators (mixers) and filters. Moreover, the costs of these components quickly increase the system's cost. High cost makes the polar loop feedback and Cartesian feedback less attractive.

Figure 2.8: Block diagram of Cartesian feedback loop.

2.2 Feedforward Linearization

Figure 2.9: Block diagram of a feedforward circuit.

A common feedforward circuit is illustrated in Figure 2.9. The feedforward technique is the subject of much active research as this technique can offer perfect distortion cancellation. The fundamental operation of the feedforward circuit is the combination of two signals: the error signal and the main RF signal. The RF input signal is split into half by a hybrid splitter. Half of the RF input signal is fed through a delay line, while the other half is fed to the main RF PA. The output signal from the PA, including distortion signal generated by the RF PA, is sampled by coupler 1, attenuated, and combined with the signal in the delay path. With an adjustable attenuator and a variable delay line, the sampled signal and delay signal have the same amplitude but 180° out of phase. As the result, the main signal will be cancelled out at the combiner and the RF PA distortion signals feed through the combiner to the highly linear class-A error amplifier. This error amplifier will amplify the error distortion signals to the same level of the distortion signals in the RF PA. The delay line 2 in the upper path adjusts the output signal from the RF PA such that it will arrive at the coupler 2's output 180° out of phase with the amplified error distortion signals. The combined signal at the coupler 2's output is an amplified, distortion-free RF signal.

The feedforward technique is also feasible for complete transmitter linearization rather than a single or compound transistor amplifier linearization. In the literature, however, there are some feedforward techniques, which are designed to linearize a single transistor amplifier. These feedforward techniques use only passive elements for matching or filtering and active elements for gain or error amplifications. These feedforward circuits are much simpler and compact than the circuit illustrated in Figure 2.9 and do not require precision delay lines, attenuator, couplers, and combiner.

The feedforward amplifier presented in [24] has a second harmonic feedforward configuration, in which the second harmonic ($f_2 - f_1$) at the gate is fed through a small and low frequency operational amplifier to the drain of a common source FET transistor amplifier. The circuit schematic is illustrated in Figure 2.10. The gain of the operational amplifier is related to the transistor amplifier components. The second harmonic voltage at the gate is amplified by the operational amplifier and subtracted from the drain voltage of the FET amplifier. The new drain voltage results in a nonlinear drain current, whose third-order coefficient can be made equal to zero [24]. This proposed circuit was tested by the author with a Sirenza SHF-0289 FET and showed 18dB IMD3 improvement with general two-tone test and more than 10dB ACPR improvement with a nine-channel forward-link CDMA signal test. This feedforward circuit is inherently stable and broadband since it employs a feedforward technique. A drawback to this circuit is the gain sensitivity of the operational amplifier (Op Amp) to temperature and time. The optimum value of Op Amp gain (β) is 147, however, a small deviation from this value might cause some reduction in the above IMD3 achievement.

Figure 2.10: Circuit of a FET amplifier with the second harmonic feedforward.

Another common type of wideband feedforward circuits is the “cascomp” (cascade compensator) circuit [6]. In the cascomp circuit, an error signal is fed forward by error amplifiers to the output drains of the cascade amplifier. At the output drains, the error currents add with the cascade amplifier’s currents and if the phase of the error currents are properly adjusted, cascade amplifier distortion could be reduced. The advantage of the cascomp circuit is that the error amplifier transconductance is independent of temperature, time and input signal power. The circuit was reported to have some improvement in amplitude distortion but degradation in phase distortion. [6]

2.3 Predistortion Linearization

A PRD circuit generates an inverse nonlinear transfer characteristic of the PA in both amplitude and phase so that the combined transfer characteristic of the combined PRD+PA is more linear. A general block diagram of a combined PRD+PA is illustrated in Figure 2.11.

A PRD circuit is an open loop system in nature. As a result, the transfer function of the PRD must be pre-calculated in advance for a given range of input power, at which the PA’s gain starts to compress. The gain expansion characteristic of a PRD is achieved by nonlinear components such as Schottky diodes or FET channel resistance. This nonlinear component also generates the required harmonic distortion to cancel the unwanted intermodulation distortion of the PA. A PRD circuit employing these nonlinear components forms the main discussions of this section. Adaptive PRD will be briefly introduced at the end of the section.

Figure 2.11: Typical block diagram of PRD and PA and their characteristics.

2.3.1 Anti-parallel and Parallel Diode Predistortion

The main circuit of an anti-parallel diode PRD consists of two diodes connected in anti-parallel configuration. A common type of this PRD found in the literature is illustrated in Figure 2.12 [25]. The advantage of this anti-parallel diode pair is that it only generates odd-order distortion, while even-order distortion is circulated within the diode loop [26]. A single diode, when driven with RF signals, generates both even-and odd-order distortion. This can be seen from the exponential nonlinearity of a diode. Depending on the RF signal level, the diode should be biased to generate sufficient distortion. Attention must be paid to biasing of anti-parallel diodes with regards to RF choking and maintaining diode balance. The signal in the upper path of the PRD circuit is phase shifted so that the original input signal and the distortion generated in the lower path are 180° out of phase. A delay line compensates for the delay of the distortion

generator and the attenuator in the lower path. The attenuator adjusts the distortion level to match that of the distortion generated by the PA. The output signal of the PRD consists of the RF signals plus distortion signals. When this signal is fed through the PA, the distortion signals cancel with the distortion generated in the PA [4]. To achieve maximum distortion cancellation, the phase shifter, delay line, attenuator, and distortion generator (the anti-parallel diode in this case) must be very well controlled.

Figure 2.12: Anti-parallel diode PRD circuit with a RF PA stage.

Despite the need for accurate control of the phase shifter, delay line, and attenuator, anti-parallel PRD circuits have shown good improvement in IMD3. In [27], the authors reported a 17dB improvement in IMD3. This improvement could be better if the PRD circuit was modeled to account for higher-order distortion (i.e fifth-order) in simulation. The distortion generator of this PRD is shown in Figure 2.13. This PRD circuit achieves a good IMD3 cancellation between output power ranges from 21dBm to 28dBm. Outside this range, little cancellation is observed.

Figure 2.13: Distortion generator circuit employing anti-parallel diode.

A parallel diode can also be used to create a distortion generator. In [28], the authors designed a diode linearizer for high power travelling wave tube and solid-state power amplifiers (TWTA and SSPA). The proposed linearizer consists of two PIN diodes and two Schottky diodes as shown in Figure 2.14.

Figure 2.14: Schematic of the diode linearizer employing parallel Schottky and PIN diodes.

The Schottky diode pairs in the lower path (nonlinear path) generate the required distortion. The PIN diodes in the upper path (linear path) serve as a variable attenuator. The output signal of the linearizer contains the original and distortion signals, which is again fed to the amplifier. The authors measured a 3.8dB and 8.7dB in IMD3 improvement at 1dB and 2dB output power back-off, respectively. At higher output power back-off, improvement in intermodulation is less than 4dB.

In yet another design [29], the authors used two distortion generators in parallel as shown in Figure 2.15. The upper path is optimized for phase to correct the AM/PM effect whereas the lower path is optimized for amplitude to correct the AM/AM effect of the amplifier. This circuit shows a measured improvement of 6dB in ACPR.

Figure 2.15: Block diagram of an independent controlled AM/AM and AM/PM predistortion linearizer circuit system and circuit schematic of a distortion generator.

Yamauchi et. al. [30][31] proposed the simplest parallel diode distortion generator to date. The circuit consists of a single Schottky diode and a bias resistor as shown in Figure 2.16. The buffer amplifier is needed to restore the loss in the PRD circuit. The nonlinear resistance of the Schottky diode causes the gain expansion and phase compression of this PRD circuit. Compared to the previous parallel diode PRD, this simple PRD gives a similar improvement in ACPR of 5dB in measurement.

Figure 2.16: Circuit diagram of parallel diode with bias feed resistance linearizer with variable gain buffer amplifier.

2.3.2 Series Diode and FET Predistortion

Another type of diode PRD is series diode PRD as shown in Figure 2.17 [32]. A series diode PRD is also compact and ideal for design in monolithic format. It requires only two coupling capacitors and two RF chokes for biasing.

Figure 2.17: Circuit diagram of a series diode PRD circuit with a RF PA and a diode equivalent circuit model.

The diode is forward biased at a quiescent point in its nonlinear I-V curve. In forward bias, the nonlinear C-V of the diode capacitance can be neglected. The nonlinear capacitance is approximated as a fixed capacitor with a value of $10C_{j0}$, where C_{j0} is the value of junction capacitance with 0V applied to the diode [33]. In this forward bias region, the diode functions as a nonlinear resistor R_j and a fixed capacitor C_j in parallel. The transfer characteristics of this network is given by:

$$S_{21} = \frac{2Z_0 Y}{1 + 2Z_0 Y} \quad Y = j\omega C_j + \frac{1}{R_j} \quad (2.4)$$

When the RF signal is applied, the diode rectifies the RF power and the quiescent point moves up the diode I-V curve with increasing RF input power. As the result, the diode resistance R_j decreases as forward bias voltage across the diode increases. This results in amplitude expansion and phase compression across the diode [32]. Haskins [32] reported a measured improvement of 5.9dB in upper ACPR but only 2.2dB in lower ACPR for QPSK modulation scheme. The asymmetrical improvement between upper and lower ACPR has not yet been resolved.

Hau [34] proposed a series FET PRD circuit. A HJFET is biased in a switch mode to operate as a nonlinear resistor. This PRD circuit can have gain expansion or compression characteristic by adjusting the bias voltage V_{bias} . This circuit is again very compact and ready to implement monolithically. The author reported a measured ACPR reduction of 5.4dB. The diagram of this series HJFET PRD is shown in Figure 2.18.

Figure 2.18: Schematic of a series HJFET PRD circuit and a FET common-source amplifier.

2.3.3 Active FET Predistortion

Combining two FETs in a “cascode” topology with the upper FET biased as a common source amplifier while the lower FET biased as a nonlinear element results in an active PRD circuit [1]. All of the PRD circuits discussed so far are passive and so have gain less than unity. Loss is the main disadvantage of passive PRD circuits. The signal level must be restored by adding a buffer amplifier when integrating a PRD circuit with a PA. In [1] the authors benchmarked the first active FET PRD with a small-signal

gain of 6.5dB. This active PRD achieves programmable gain and phase variation by adjusting the bias and size of the FET transistors. The author measured a reduction in ACPR as high as 10dB at 45dBm output power for a 30W High PA (HPA) for a CDMA base station. This is undoubtedly the highest ACPR improvement on a CDMA base station HPA reported to date with a simple PRD circuit. The schematic of this new active PRD is shown in Figure 2.19.

Figure 2.19: Circuit diagram of a new active PRD employing FET “cascode” structure [1].

2.3.4 Adaptive Predistortion

An adaptive PRD technique is often performed at baseband rather than at RF frequency. This PRD method essentially employs a Cartesian loop feedback with a Digital Signal Processing (DSP) circuit to distort the input signal. This type of PRD can

offer high distortion reduction for third- and higher-order intermodulation distortions. As simulated in [35], the distortions outside the band are all suppressed below -80dB . This suppression of distortion meets all of the power spectral requirements for most wireless standards. However due to its circuit complexity and large size, this PRD topology is not studied, even though it offers an excellent reduction in IMD.

2.4 Postdistortion Linearization

Similar to the predistortion topology, the RF PA can be linearized with a postdistortion (POD) circuit. The postdistortion circuit generates an inverse transfer characteristic function to that generated by the RF PA. The result is a linear transfer function as shown by the solid line in Figure 2.19.

Figure 2.19: Typical block diagram of POD and PA and their characteristics

One disadvantage of a POD circuit is the requirement for large power handling capability of all the POD circuit's passive or active elements at the output of the RF power amplifier. Another disadvantage of this topology is any loss in the POD circuit reduces the overall amplifier efficiency. These restrictions make the POD circuit less attractive in linearizing medium or high power amplifiers [4]. However it might be feasible to use a POD circuit to linearize low power amplifiers such as in a receiver. The POD circuit should be carefully designed so that no significant noise is introduced into the overall receiver.

2.5 Conclusions

Four different linearization techniques for transistor amplifiers and radio transmitters presented. It becomes clear that the size and complexity of linearization circuits have direct impact on the degree of intermodulation improvement of the amplifiers they linearize. Active feedback (envelope, polar, and Cartesian loop feedback) and feedforward are ideal to linearize a complete transmitter rather than a simple transistor amplifier. For a single transistor or compound transistor amplifier, methods such as transformer feedback and Schottky diode predistortion are more attractive. First, such circuits are less complex and ready for monolithic implementation. Second, the improvement in IP3 is very competitive considering the circuit size and power consumption. These two types of linearization techniques are selected for further study.

3 Predistortion Study

The study of linearization techniques in general relies heavily on well-characterized amplifiers. As the design goal of this study is to minimize the IMD3 of the amplifiers at a certain output power, the IMD behavior of the amplifiers must be thoroughly understood. To this end, three power amplifiers are designed, fabricated, and measured to characterize each amplifier's nonlinearity. The designs of three amplifiers using a Darlington pair topology are discussed in the first section of this chapter. In the second section, a novel variable active PRD circuit is proposed, designed and simulated. The chapter concludes with a new methodology for designing a linearized power amplifier using an active PRD.

3.1 Technology Available for Circuit Designs

Silicon Germanium (SiGe) is available for the amplifier and PRD designs in this study through Sirenza Microdevices Inc. and Canadian Microelectronics Corporation (CMC). CMC provides Canadian universities and research students with fabrication access to IBM5HP BiCMOS SiGe 0.5 μ m process. Due to the fact that the fabrication process parameters are strictly confidential, all other process parameters except those given above cannot be released.

The experimental amplifier 1 and amplifier 2 as well as the transformers, were designed using Sirenza's SiGe process. Unfortunately, this process became unavailable in late 2002. The IBM SiGe process was then selected to design the amplifier 3 and the PRD circuit.

3.2 Amplifier Designs

3.2.1 Darlington Pair Amplifier

The Darlington pair has become a very popular amplifier configuration in RF power amplifier design due to its high current gain, high input impedance, and large bandwidth. The circuit diagram of a typical Darlington pair amplifier is illustrated in Figure 3.1(a). The feedback resistor R_{f1} ensures a good DC bias, gain, and return loss over the large bandwidth. The degeneration emitter resistors are employed for DC operation, stabilization and series feedback. A typical application with external bias circuit components is shown in Figure 3.1(b). Only two DC-blocking capacitors, a bias resistor and a RF choke are required for biasing and operation at RF frequencies. Whereas the RF choke is an option, the series bias resistor is necessary as it provides negative feedback to stabilize the current to the Darlington pair amplifier over supply and output voltage fluctuation.

Figure 3.1(b) shows the application circuit of a Darlington pair medium power amplifier SGA-6489 from Sirenza Microdevices Inc. This commercial amplifier is used as a reference for all the designed amplifiers in this study. The important RF performance characteristic of the SGA-6489 at a frequency of 1.95GHz in a 50Ω system are shown in

Table 3.1, which will be used as specifications for designed amplifiers 1, 2 and 3. Since amplifier 2 will be used in transformer feedback design, its gain is higher than the specified gain shown in Table 3.1.

Figure 3.1: General topology of amplifier using Darlington pair. a) Schematic of a Darlington pair and b) Application schematic.

Table 3-1: Summary of the SGA-6489 operation specifications [36].

Symbol	Parameter	Unit	Value
G	Small Signal Gain	dB	17.5
OIP3	Output Third Order Intercept Point	dBm	32
P_{1dB}	Output Power at 1dB Compression	dBm	18
IRL	Input Return Loss	dB	14.4
ORL	Output Return Loss	dB	10.9
NF	Noise Figure	dB	3.0

Test Conditions: $V_s=8V$ $I_D=75mA$ Tone spacing=1MHz
 $R_{BIAS}=39\text{ Ohms}$ $T_L=25^{\circ}C$ Pout per tone = 0dBm

3.2.2 First Experimental Power Amplifier Design (Amplifier 1)

The first designed amplifier employs the Darlington pair topology as shown in Figure 3.1(a) with two minor modifications. The first modification is to replace the second common collector transistor by multiple transistors in parallel. This design technique is a common practice in power amplifier design to handle more power. The second modification is to add a small series resistor between transistor Q_1 and transistor Q_2 of the Darlington pair. This resistor degrades slightly the gain and noise of the amplifier, but is believed to stabilize the amplifier on-chip. Resistor values from 6Ω to 10Ω are simulated in Cadence to yield an unconditionally stable amplifier. In order to physically realize the above resistor values, five 30Ω resistors are laid out in parallel with the top metal level M3 fuse at each end. These fuses will be blown by a laser during testing if the amplifier becomes unstable to give a resistor with a value of 6, 7.5, 10, 15 or 30Ω . However, these resistors are first short circuited using top metal level M3 to measure the amplifier's response without the resistor present. The circuit schematic is shown in Figure 3.2 and its die photograph is shown in Figure 3.3.

Figure 3.2: Schematic of the first experimental amplifier (Amplifier 1).

Figure 3.3: Die photograph of the amplifier 1.

3.2.3 Second Experimental Power Amplifier Design (Amplifier 2)

In the first designed amplifier, the feedback resistor R_{f1} is used to set the DC bias level and to adjust the voltage gain, as well as the input and the output impedance at RF. This resistor should be carefully chosen to ensure the base collector junctions are not forward biased, to meet the required gain and to satisfy the return loss and stability requirement. Placing these design parameters on a single resistor gives the circuit designer little choice. Introducing an additional feedback resistor into this amplifier gives another degree of freedom to meet the required specifications. The result is a dual feedback amplifier, which has already been used in amplifier designs [37], [38]. The circuit schematic of this dual feedback amplifier is shown in Figure 3.4. This amplifier can be seen as a two stage direct-coupled amplifier. The first stage, a common emitter with degenerative inductor, consists of transistors Q_3 and inductor L_e . The second stage is the Darlington pair amplifier as seen in amplifier 1. The first feedback resistor R_{f1} couples the output signal RF_{out} to the input of the second stage amplifier. This resistor

sets the DC bias level, the output impedance and the amplifier's gain. The second feedback resistor R_{f2} couples the output signal of the first stage at the emitter of transistor Q_2 to the input signal RF_{in} . This resistor sets the DC bias level at the input of the first stage and the input impedance. This amplifier has been very well characterized and designed in the literature [39]. A degenerative inductor L_e is selected instead of a resistor or a resistor with a peaking capacitor as suggested in [37], [39]. This inductor with the second feedback resistor R_{f2} is designed and simulated to give a good input match and a lower noise figure than amplifier 1. The measured noise figure of amplifier 2 is approximately 1.2 dB lower than the measured noise figure of amplifier 1 as will be seen in the measurement section.

Figure 3.4: Schematic of the second experimental amplifier (Amplifier 2).

Figure 3.5: Die photograph of the amplifier 2.

3.2.4 Third Experimental Power Amplifier Design (Amplifier 3).

In both of the above amplifier designs, due to a high tolerance of resistors with small sheet resistance in the Sirenza's SiGe process, the small emitter resistors R_{e1} were realized by placing resistors with high sheet resistance in parallel. While it is practically feasible, putting resistors in parallel occupies additional chip area. Secondly, both amplifier1 and amplifier 2 employ large transistors ($1.2 \times 20\mu\text{m}^2$), which have low base resistance values. In the third experimental amplifier, the transistor Q_1 and high sheet resistance resistors R_{e1} are replaced by smaller size transistors ($0.5 \times 20\mu\text{m}^2$) and smaller sheet resistance resistors. These modifications have the following advantages. Firstly, small size transistors have bigger base resistances and so the additional resistor R_{b1} between transistor Q_2 and Q_1 can be removed while still keeping the amplifier stable. Secondly, because of the smaller size, ten small transistors (Q_1) are used to handle the same power instead of four in the previous amplifier designs. As a result, a larger

degeneration resistor R_{e1} can be used due to a smaller emitter current going through each transistor. The larger resistor value eliminates the need of placing multiple high sheet resistance resistors R_{e1} in parallel at the emitter. These modifications improve stability, free up additional chip area, and reduce layout complexity. Figures 3.6 and 3.7 show the schematic and layout in Cadence of the third experimental amplifier (Amplifier 3).

Figure 3.6: Schematic of the third experimental amplifier (amplifier 3).

Figure 3.7: Layout in Cadence of amplifier 3.

3.2.5 Measured and Simulated Results

The measured dice sizes of amplifier 1 and amplifier 2 are $800 \times 550 \mu\text{m}^2$ and $1100 \times 650 \mu\text{m}^2$, respectively. Both amplifier 1 and amplifier 2 were designed to have input matched to 25Ω and output matched to 12.5Ω . The ports are not matched to 50Ω because the amplifiers were initially designed to form a push-pull amplifier. As the result, when both amplifiers were tested in a 50Ω system, lower return losses were expected. Figure 3.8 and 3.9 show the S-parameter measurements of amplifier 1 and amplifier 2, respectively. As can be seen from the Smith chart, the input and output real impedances are reasonably matched to 25Ω and 12.5Ω . The imaginary impedances can be tuned out with inductive bondwires. In the amplifier 2 design, the first stage common emitter amplifier provides extra gain and prevents the output signal from going back to the input directly through the feedback resistor R_{f1} as seen in amplifier 1. The two shortest direct paths from the output to the input of amplifier 2 are through the feedback resistor R_{f1} and the transistor Q3 or through the transistor Q1 and the feedback resistor R_{f2} . Hence the isolation of amplifier 2 is always higher than the isolation of transistors Q1 or Q3. As a result, amplifier 2 has a higher gain (30dB) and a higher isolation (37dB) than amplifier 1. Adding the degenerative inductor L_e in amplifier 2 results in good impedance and noise match at the input port. The measured noise figure (1.69dB) of amplifier 2 is close to the minimum simulated noise figure ($NF_{\min}$) of 1.3dB. The noise figure of amplifier 2 is approximately 1.2dB better than that of amplifier 1 as can be seen from Figure 3.10 and Figure 3.11. While amplifier 2 has a clear advantage in noise performance over amplifier 1, it suffers a much smaller bandwidth due to gain roll off in

the common emitter gain stage. The increasing impedance of the degenerative inductor lowers the gain of amplifier 2 at high frequency.

Figure 3.8: Measured S-parameter response for amplifier 1.

Figure 3.9: Measured S-parameter response for amplifier 2.

Figure 3.10: Measured noise figure and gain vs. frequency for amplifier 1.

Figure 3.11: Measured noise figure and gain vs. frequency for amplifier 2.

Amplifier 3 was designed with similar specifications as set out in Table 3.1 for the commercial SGA-6489 amplifier. The simulated S-parameter, noise figure, and nonlinearity responses of amplifier 3 are shown in the next figures. Unlike amplifiers 1 and 2, amplifier 3 was designed to match to 50Ω impedance.

Figure 3.12: Simulated gain and return loss vs. frequency for amplifier 3.

Figure 3.13: Simulated noise figure vs. frequency for amplifier 3.

Figure 3.14: Simulated fundamental and IMD3 vs. input power for amplifier 3.

The amplifier 1 and amplifier 2 nonlinearities were characterized by applying two-tone signal at 1MHz apart. The output levels are observed while sweeping the input level from linear region to compression region. The IP3 points were calculated using equation A.5 in appendix A. The performances of amplifiers 1, 2, and 3 at 1.95GHz are summarized in Table 3.2 for easy comparison. Note that the tested and simulated DC bias conditions of each amplifier are different. The following equipment was used to do measurements.

- Picoprobe and Cascade Microtech GSG-150 micro probes (2).
- Picoprobe Calibration Substrate, Part # CS-5150 (1).
- Bausch&Lomb Micro Zoom Microscope (1).
- HP E3610A DC Power Supply (1)
- HP 34401 Digital Multimeters (2)

- HP 8722ES S-parameter Network Analyzer 50MHz-40GHz (1).
- Agilent N8974A NFA Series Noise Figure Analyzer 10MHz-6.7GHz (1).
- Agilent N4002A Smart Noise Source (SNS) 10MHz-26.5GHz (1).
- HP 8595A Spectrum Analyzer 9KHz-6.5GHz (1).
- HP 8564E Spectrum Analyzer 30Hz – 40GHz (1).
- Rohde&Schwarz Signal Generator 5KHz-6GHz (2).
- Cables, connectors, couplers, splitters.

Table 3-2: Performance summary of amplifiers 1, 2, and 3

Symbol	Parameter	Unit	Amplifier 1	Amplifier 2	Amplifier 3
G	Small Signal Gain	dB	18.1	30.2	19
OIP3	Output Third Order Intercept Point	dBm	25.4	25.5	31
P_{1dB}	Output Power at 1dB Compression	dBm	18	18	17.5
IRL	Input Return Loss	dB	<10	<10	12
ORL	Output Return Loss	dB	<10	<10	10
S₁₂	Reverse Isolation	dB	21.3	37.7	24
NF	Noise Figure	dB	2.83	1.69	2.8
PAE	Power Added Efficiency	%	17.5	16.5	17

Test Conditions

Amplifier 1	V _s =8.1V	I _D =62.5mA	Tone spacing = 1MHz
	R _{BIAS} = 49 Ohms	T _L =25 ⁰ C	Pout per tone = 0dBm
Amplifier 2	V _s =8V	I _D =75mA	Tone spacing = 1MHz
	R _{BIAS} = 39 Ohms	T _L =25 ⁰ C	Pout per tone = 0dBm
Amplifier 3	V _s =5V	I _D =70mA	Tone spacing = 1MHz
	R _{BIAS} = 25 Ohms	T _L =25 ⁰ C	Pout per tone = 0dBm

3.3 Predistortion Analysis

Figure 2.11 in chapter 2 illustrated a general diagram of a PRD circuit and a linear P_{in}/P_{out} characteristic of the amplifier when PRD is utilized. The combined PRD+PA is more linear than the amplifier alone since it has higher output P_{1dB} compression. This type of predistortion circuit only works in the situation when the amplifier is compressed due to the transistor's nonlinearity. When the amplifier is compressed due to clipping of the output voltage, the PRD circuit does not, generally, improve the output 1dB compression. Figure 3.15 illustrates the typical amplifier compressions with and without passive PRD.

In Figure 3.15, curve A represents the amplifier's compression without any applied predistortion. Curves B and C represent the amplifier's compression with predistortion. However, in curve B the amplifier compresses due to clipping of the output voltage, whereas in C, the amplifier compresses due to the transistor's nonlinearity. It should be noticed that in both cases, the small signal gain of the combined PRD+PA reduces due to loss in the passive PRD circuit. This loss can be compromised by adding a linear buffer amplifier in between the PRD and the amplifier. This buffer amplifier must be highly linear so that no distortions from this buffer amplifier will be introduced into the predistorted signal from the PRD output. A linear class-A amplifier is often used as the buffer amplifier. A linear class-A buffer amplifier will increase the circuit complexity, power consumption, and cost, however.

Figure 3.15: Typical amplifier's compressions. Curve A represents amplifier compression. Curve B represents a combined PRD+PA compression due to output voltage clipping. Curve C represents a combined PRD+PA compression due to transistor nonlinearity.

Class-A amplifiers, such as experimental power amplifiers 1, 2, and 3, often compress due to clipping of the output voltage. The use of PRD cannot improve the output P_{1dB} in this case but can reduce the amplifier's IMD3. The idea of PRD circuit is to create two signals, at the IMD3 frequencies, which have the same amplitudes but opposite phases than the IMD3 produced by the amplifier itself [40]. If the signals have the correct phases at the output, then in theory, IMD3 should be zero. It should be noted that PRD is an open loop system. As the result this cancellation in IMD3 occurs only at a particular input power. This will be seen in the next section of the thesis.

To see how the PRD can cancel the distortion levels, let us assume for a moment a third-degree amplifier and a third-degree PRD with only odd-power series coefficients (from equation A.3 in the Appendix A, only odd-degree coefficients generate the inband IMD3). This assumption is for a simple qualitative analysis. In practice, many higher-order terms are needed for accurate results. The combined PRD+PA output is given in the following form:

$$v_{out} = a_1 v_{pd} + a_3 v_{pd}^3 \quad (3.1)$$

where $v_{pd} = b_1 v_{in} + b_3 v_{in}^3$ is the output of the PRD. Substitute v_{pd} into the Equation 3.1, then

$$v_{out} = a_1 (b_1 v_{in} + b_3 v_{in}^3) + a_3 (b_1 v_{in} + b_3 v_{in}^3)^3 \quad (3.2)$$

$$v_{out} = a_1 b_1 v_{in} + (a_1 b_3 + a_3 b_1^3) v_{in}^3 + 3a_3 b_1^2 b_3 v_{in}^5 + 3a_3 b_1 b_3^2 v_{in}^7 + a_3 b_3^3 v_{in}^9 \quad (3.3)$$

$$v_{out} = k_1 v_{in} + k_3 v_{in}^3 + k_5 v_{in}^5 + k_7 v_{in}^7 + k_9 v_{in}^9 \quad (3.4)$$

where

$$k_1 = a_1 b_1 \quad k_3 = (a_1 b_3 + a_3 b_1^3) \quad k_5 = 3a_3 b_1^2 b_3 \quad k_7 = 3a_3 b_1 b_3^2 \quad k_9 = a_3 b_3^3$$

In Equation 3.4, k_1 represents the linear combined PRD+PA gain, while k_3 , k_5 , k_7 , and k_9 represent the odd-order nonlinearity of the combined PRD+PA, respectively. In most passive PRD circuits reported in the literature, the coefficient b_1 is less than unity and so the combined gain k_1 is less than the original amplifier's gain a_1 . It has already been illustrated in Figure 3.15. Also from equation 3.4, it can be noted that a third-order PRD combined with a third-order PA have produced up to a ninth-order nonlinearity at the output of the combined system. In the case of two-tone test, the contributions of these

nonlinearities to the desired signal as well as higher-order IP signals are summarized in Table 3.3. [25]

Table 3-3: Contributions of odd-order nonlinearity to the desired and intermodulation signals.

n	3	5	7	9
	$k_3 v^3$	$k_5 v^5$	$k_7 v^7$	$k_9 v^9$
Fund	$\frac{9}{4}$	$\frac{25}{4}$	$\frac{1225}{64}$	$\frac{3969}{64}$
IMD3	$\frac{3}{4}$	$\frac{25}{8}$	$\frac{735}{64}$	$\frac{1323}{64}$
IMD5	-	$\frac{5}{8}$	$\frac{245}{64}$	$\frac{567}{64}$
IMD7	-	-	$\frac{35}{64}$	$\frac{567}{256}$
IMD9	-	-	-	$\frac{3969}{256}$

Since only a third-order nonlinearity was assumed for both the PRD and the amplifier, only the third-order coefficient k_3 can be made equal to zero. The contributions of higher-order nonlinearity to the IMD3 are fixed and represent the limitation in distortion reduction when a third-order PRD is used. Assuming for the moment that the contributions of higher-order nonlinearities to IMD3 level are less significant compared with that from third-order, the IMD3 vanishes when k_3 in equation 3.4 equal to zero, or

$$a_1 b_3 + a_3 b_1^3 = 0 \quad (3.5)$$

$$b_3 = -\frac{b_1^3}{a_1} a_3 \quad (3.6)$$

The equation 3.6 gives a relationship between the third-order power series coefficient of the PRD transfer function and that of the amplifier. Since a_3 of the amplifier is a negative number (a cause of gain compression in power amplifiers), b_3 of the PRD must be a positive number in order for the above relationship to hold true. Because b_3 is the third-order power series coefficient of the PRD, the PRD must have a gain expansion characteristic. This is what is expected in all PRD circuits. The equation 3.6 does not, however, reveal any relationship in terms of the phase of the third-order power series coefficient between the PRD and the amplifier. In order to extract this phase relation, one must use the Volterra series, which is not within the scope of this study.

The above analysis represents the input as a single signal v_{in} , which in a two-tone analysis is a combination of two signals at two adjacent frequencies. The next section gives a more complete analysis on the behaviors of the combined PRD+PA when a two-tone signal is applied at the input.

3.3.1 Analysis of Predistortion with Two-Tone Input Signal.

Consider a two-tone signal as given in equation A.2 applied to the input of the combined PRD+PA. Figure 3.16 illustrates a combined PRD+PA and output signal in spectrum domain of each circuit block. Assuming a band limiting system, the output v_{pd} of the PRD circuit contains the fundamental tones and two IMD tones as given below:

Figure 3.16: Circuit blocks represent a combined PRD+PA.

$$v_{pd} = \left(b_1 A + \frac{9}{4} b_3 A^3 \right) \cos(\omega_1 t) + \left(b_1 A + \frac{9}{4} b_3 A^3 \right) \cos(\omega_2 t) + \frac{3}{4} b_3 A^3 \cos(2\omega_1 - \omega_2)t + \frac{3}{4} b_3 A^3 \cos(2\omega_2 - \omega_1)t \quad (3.7)$$

$$v_{pd} = M[\cos(\omega_1 t) + \cos(\omega_2 t)] + N[\cos(2\omega_1 - \omega_2)t + \cos(2\omega_2 - \omega_1)t] \quad (3.8)$$

where

$$M = \left(b_1 A + \frac{9}{4} b_3 A^3 \right) \quad N = \frac{3}{4} b_3 A^3 \quad (3.9)$$

The output signal of the PRD, v_{pd} is then applied to the third-order nonlinear power series representation of the amplifier.

$$v_{out} = a_1 \{ M[\cos \omega_1 t + \cos \omega_2 t] + N[\cos(2\omega_1 - \omega_2)t + \cos(2\omega_2 - \omega_1)t] \} + a_3 \{ M[\cos \omega_1 t + \cos \omega_2 t] + N[\cos(2\omega_1 - \omega_2)t + \cos(2\omega_2 - \omega_1)t] \}^3 \quad (3.10)$$

The derivation of this equation is a straightforward process which requires extensive uses of trigonometric identities. With assistance of mathematic software such as MatLab or MathCAD, this derivation can be simplified without any difficulties. Only the signals at the fundamental and the IP3 frequencies are of interest. These are given in the next equations.

$$v_{out, fund} = \left(a_1 M + \frac{9}{4} a_3 M^3 + \frac{9}{4} a_3 M^2 N + \frac{9}{2} a_3 M N^2 \right) (\cos \omega_1 t + \cos \omega_2 t) \quad (3.11)$$

$$v_{out, IMD3} = \left(a_1 N + \frac{3}{4} a_3 M^3 + \frac{9}{2} a_3 M^2 N + \frac{9}{4} a_3 N^3 \right) [\cos(2\omega_1 - \omega_2)t + \cos(2\omega_2 - \omega_1)t] \quad (3.12)$$

Let $\alpha = \frac{\frac{3}{4}b_3A^3}{b_1A}$ represent the ratio of the applied IMD3 signal to the fundamental signal

level at the input of the nonlinear amplifier. This ratio is always less than unity as the PRD's IMD3 signal amplitude is always less than the PRD's fundamental amplitude. The above M and N coefficients can be rewritten as

$$M = b_1A(1 + 3\alpha) \quad \text{and} \quad N = b_1A\alpha \quad (3.13)$$

Substituting M and N in the equation for $v_{out,fund}$ and $v_{out,IMD3}$ and neglecting the second- and higher powers of the α coefficient, we have:

$$v_{out,fund} = \left\{ a_1b_1A(1 + 3\alpha) + \frac{9}{4}a_3A^3[b_1^3(1 + 10\alpha)] \right\} (\cos\omega_1t + \cos\omega_2t) \quad (3.14)$$

$$v_{out,IMD3} = \frac{3}{4}a_3A^3 \left(b_1^3 + \frac{a_1b_3}{a_3} + \frac{45}{4}b_1^2b_3A^2 \right) [\cos(2\omega_1 - \omega_2)t + \cos(2\omega_2 - \omega_1)t] \quad (3.15)$$

Comparing the fundamental and IMD3 signals at the output of the combined PRD+PA with the signals at the output of the amplifier itself as given in equation A.3, the following observations can be made:

- The coefficient $k_1 = \left\{ a_1b_1A(1 + 3\alpha) + \frac{9}{4}a_3A^3[b_1^3(1 + 10\alpha)] \right\}$ of the combined

PRD+PA fundamental signal, which is used to calculate the compression, depends on the linear gain of the PRD and coefficient α , thus the input signal at 1dB compression can be solved as:

$$20 \log \left(\frac{a_1b_1A(1 + 3\alpha) + \frac{9}{4}a_3b_1^3A^3(1 + 10\alpha)}{a_1b_1A} \right) = -1dB$$

$$20 \log \left((1 + 3\alpha) + \frac{9 a_3 b_1^2 A^2 (1 + 10\alpha)}{4 a_1} \right) = -1 \text{ dB}$$

$$\Rightarrow A_{1\text{dB}} = 2 \sqrt{\frac{a_1}{3 a_3 b_1^2 (1 + 10\alpha)}} \sqrt{\alpha + \frac{1 - 10^{-\frac{1}{20}}}{3}} \quad (3.16)$$

Case 1: If $b_1 < 1$ or passive PRD

The combined PRD+PA has a lower gain than the original PA gain, however it has a higher input signal level at 1dB compression. Clearly, the combined PRD+PA has traded off its gain for linearity. Note that this is only true in the case where the PA is compressed due to transistor nonlinearity but not when it is compressed due to clipping of the output voltage. If the PA is compressed due to output voltage clipping then the output power at 1dB compression point cannot be improved even if the gain is reduced.

Case 2: If $b_1 > 1$ or active PRD

The combined PRD+PA has a larger gain but a smaller input signal at 1dB compression point. Gain and linearity are once again traded off for each other. In the case of signal compressed due to voltage clipping, the input compression point is reduced proportionally with the increase in gain.

- The coefficient $k_3 = \frac{3}{4} a_3 A^3 \left(b_1^3 + \frac{a_1 b_3}{a_3} + \frac{45}{4} b_1^2 b_3 A^2 \right)$ of the combined PRD+PA

can be made equal to zero regardless of b_1 being smaller or greater than unity because b_3 and a_3 are always opposite in sign. It is equal to zero when

$$b_1^3 + \frac{a_1 b_3}{a_3} + \frac{45}{4} b_1^2 b_3 A^2 = 0 \quad (3.17)$$

Equation 3.17 shows the cancellation of IP3 signals depending on input signal A, which was not presented in equation 3.6. Unless the PRD's linear and third-order coefficients b_1 and b_3 vary with input power A, equation 3.17 holds true only at a particular input power.

These observations indicate that the output 1dB compression point of the designed amplifiers cannot be improved with the active PRD if the amplifier is compressed due to output voltage clipping. However, if the designed PRD has the transfer characteristic that satisfies the equation 3.17, then the IMD3 of the designed amplifier can be null at a particular input power. In the vicinity of this particular input power, it is expected that some reduction in distortion can be achieved. The design of such active PRD is presented in the next section.

3.4 Novel Variable Active Predistortion Circuit

Until recently, most of the PRDs reported in the literature are passive devices which have insertion losses often higher than 3dB. These PRDs often utilize nonlinear devices such as Schottky diodes, FETs or other nonlinear resistive elements to generate the gain expansion characteristic of the PRDs [25]. Because of their inherent losses, buffer amplifiers are required after PRDs to restore the power before feeding it to the PAs, thereby increasing the overall system complexity and cost. An active FET PRD with positive gain ($b_1 > 1$) has recently been introduced [1]. In this design, the authors

have used two FETs in cascode topology, where the bottom FET is biased and used as a nonlinear element and the top FET is biased as an amplifier. This active PRD achieves a gain of 6.5dB and a reduction in ACPR of 10dB.

In this section, a novel active PRD with power gain of 13dB and adjustable gain expansion of 5dB is presented. The active PRD is composed of HBT transistors biased in common emitter configuration with Schottky diode degeneration. The transistor is biased to provide gain and the Schottky diodes act as nonlinear elements to generate the required gain expansion in the PRD circuit. A current mirror and a control voltage are added to the active PRD, which will adjust the gain expansion at different input powers.

3.4.1 Circuit Operation

The common emitter amplifier with resistive degeneration is a very well known circuit [7], [8]. This circuit has been earlier introduced in chapter 2 as a feedback circuit. Its small-signal equivalent circuit is shown in Figure 3.17.

Figure 3.17: Small-signal equivalent circuit of a common emitter amplifier with resistive degeneration.

Using Kirchoff's voltage law, the input voltage and output voltage can be expressed in term of v_π , the voltage across the base emitter junction [7].

$$RF_{out} = -g_m v_\pi R_L \quad (3.18)$$

$$RF_{in} = v_\pi + v_e = v_\pi + R_e (g_m v_\pi + v_\pi g_{r_\pi} + v_\pi g_{C_\pi}) = v_\pi [1 + R_e (g_m + g_{r_\pi} + g_{C_\pi})] \quad (3.19)$$

where $g_{r_\pi} = \frac{1}{r_\pi}$ and $g_{C_\pi} = j\omega C_\pi$

Thus, the voltage and power gain are

$$Voltage_gain = \frac{RF_{out}}{RF_{in}} = \frac{-g_m R_L}{1 + R_e (g_m + g_{r_\pi} + g_{C_\pi})} \quad (3.20)$$

$$Power_gain = \frac{P_{out}}{P_{in}} = \frac{(RF_{out})^2}{(RF_{in})^2} \frac{R_{in}}{R_L} = (Voltage_gain)^2 \frac{R_{in}}{R_L} \quad (3.21)$$

For a chosen DC bias point and a load resistance, the voltage and power gains are inversely proportional to the degeneration resistor R_e . In a variable gain amplifier, the value of R_e is adjusted to yield the desired gain over a large bandwidth and input power range. However, in an active PRD, it is desired to have a low and constant gain at low input power and an increasing gain when high input power is applied. This operation should be compared to a conventional passive PRD which has a high loss at low input power and a low loss at high input power [25]. The larger the gain expansion in a passive PRD, the bigger the loss at low input power and hence lower the combined PRD+PA gain. The common emitter amplifier with resistive degeneration can be designed to have low gain at low input power if R_e is high and to have high gain if R_e becomes low at high

input power. This nonlinear behavior of resistor R_e is realized by a Schottky diode, which is the topic of discussion in the following section.

3.4.2 The Schottky Diode's Nonlinear Resistance

The nonlinear characteristic of a Schottky diode has been used extensively in many RF circuit applications such as mixers, frequency multipliers, and harmonic oscillators. In passive predistortion circuits, a Schottky diode is the main component of the distortion generator [28], [30]. The distortion generator relies mainly on the nonlinear junction capacitance C_j and nonlinear resistance R_j of the diode, which are shown in the dashed box of Figure 3.18. Parasitic and embedding effects are modeled by series resistance R_s , series inductance L_s , and parallel capacitance C_p .

Figure 3.18: Small-signal equivalent circuit of a Schottky diode.

The Schottky diode is a majority carrier device, so its advantages over other type of diodes at high frequency are faster switching time due to high mobility of electrons and lower junction capacitance [26]. When the Schottky diode is forward-biased above the built-in junction voltage, the junction resistance R_j is the major nonlinear element. In

the forward-biased region, the junction capacitance C_j is approximated to $10C_{j0}$, where C_{j0} is the junction capacitance when applied voltage $V_d = 0V$ [33]. The parasitic capacitance C_p , package bond wire inductance L_s and resistance R_s are present to some extent in all discrete Schottky diode components. When implemented monolithically, they can be ignored and so the forward-biased Schottky diode can be approximated as an impedance Z_s , consisting of a variable resistor R_j and a capacitor of $10C_{j0}$. The approximate equivalent model of a monolithic Schottky diode is shown in Figure 3.19.

$$Z_s = R_j // C_j = \frac{R_j}{1 + j\omega R_j (10C_{j0})} = \frac{R_j}{1 + j\frac{\omega}{\omega_p}}$$

where $\omega_p = \frac{1}{10R_j C_{j0}}$

Figure 3.19: Approximate equivalent circuit model of a monolithic forward-biased Schottky diode.

The values of R_j and C_{j0} at various forward-biased voltage levels are shown in the Table 3.4 for a $5 \times 5 \mu m^2$ Schottky diode in the IBM5HP BiCMOS SiGe process.

Table 3-4: Equivalent R_j and C_{j0} of an Schottky diode at various forward-biased voltage.

$V_{\text{forward}} \text{ (V)}$	$R_j \text{ (}\Omega\text{)}$	$C_{j0} \text{ (fF)}$	$\omega_p \text{ (Grad/s)}$
0.45	28.30	22.50	157
0.5	19.60	22.97	222
0.55	14.79	23.35	290
0.6	11.80	24.00	353
0.65	9.77	27.20	376
0.7	8.31	46.70	257
0.75	7.23	169.50	81.6
0.8	6.39	945.03	16.56
0.85	5.47	5580.00	3.28

From Table 3.4, note that the resistance R_j reduces as the forward voltage, V_d increases. This can also be derived from the I-V curve of a Schottky diode [26].

$$I_d = f(V_d) = I_s \left(e^{\frac{q}{kT} V_d} - 1 \right) \quad (3.22)$$

The equivalent resistance R_j is the inverse of the slope of the I-V function, hence

$$R_j = \frac{1}{\frac{\partial I_d}{\partial V_d}} = \frac{kT}{qI_s} e^{-\frac{q}{kT} V_d} \quad (3.23)$$

Equation 3.23 validates the inverse relationship between the equivalent resistance R_j and forward-biased voltage V_d . Figure 3.20 shows the I-V characteristic of a $5 \times 5 \mu\text{m}^2$ Schottky diode used in this design.

Figure 3.20: A graph of I-V characteristic of a $5 \times 5 \mu\text{m}^2$ Schottky diode in IBM 5HP BiCMOS SiGe process.

From Table 3.4, the value of the junction capacitance is quite small; hence its impedance is large compared to the equivalent resistor R_j . So the equivalent impedance Z_s can be approximated to R_j to simplify the analysis. The presence of this junction capacitance will be discussed later in the instability discussion. An active PRD consisting of the nonlinear Schottky diode and the common emitter is presented next.

3.4.3 Active Predistortion Circuit

Figure 3.21 shows the small-signal equivalent circuit of a common emitter amplifier with Schottky diode degeneration.

Figure 3.21: Equivalent circuit of a common emitter amplifier with a Schottky diode degeneration.

The voltage gain of this circuit is similar to equation 3.20 with R_e replaced by Z_s .

$$\text{Voltage_gain} = \frac{RF_{out}}{RF_{in}} = \frac{-g_m R_L}{1 + Z_s (g_m + g_{r_\pi} + g_{C_\pi})} \quad (3.24)$$

Assume that the impedance of the diode $Z_s = R_j$ and that g_m is much greater than g_{r_π} .

Then the above voltage gain expression is reduced to

$$\text{Voltage_gain} = \frac{-g_m R_L}{1 + R_j (g_m + j\omega C_\pi)} \quad (3.25)$$

$$\text{Voltage_gain} = \left| \frac{g_m R_L}{\sqrt{(1 + R_j g_m)^2 + (\omega R_j C_\pi)^2}} \right| \angle \left\{ 180 - \tan^{-1} \left(\frac{\omega C_\pi}{\frac{1}{R_j} + g_m} \right) \right\} \quad (3.26)$$

From equation 3.26, we can find that the active predistortion achieves gain and phase expansion with the decrease of R_j . The reason R_j reduces with increasing input power is that the output current wave is clipped, which causes the rectified current to increase. At the new dynamic bias point, the voltage across the diode is higher, which reduces the effective resistance R_j according to equation 3.23. The voltage deviation across the

diode, when the common emitter with Schottky diode degeneration is excited with a two-tone signal is shown in Figure 3.20.

Figure 3.22: Voltage deviation across the Schottky diode when two-tone signal is applied.

A reduction in the effective resistance has increased the gain at high input power. The common emitter amplifier with Schottky diode degeneration is simulated with a simple resistor-biasing network [7]. The gain and phase simulation results with various values of R_b are shown in Figure 3.23 and the circuit schematic is illustrated in Figure 3.24.

Figure 3.23: Simulated gain and phase results of a common emitter amplifier with a Schottky diode degeneration.

Figure 3.24: Schematic of a common emitter amplifier with a Schottky diode degeneration.

From the preliminary simulation result in Figure 3.23, two observations can be made. Firstly, the gain is directly proportional to the bias resistor R_b , which is inversely proportional to the effective resistance of the diode. Secondly, the gain expands at higher input power with low bias resistor value R_b . While the second phenomenon is very interesting because it can be used to design an active predistorter with variable gain expansion point, the first phenomenon is not desirable since the gain fluctuates with the bias resistor R_b at low input power. Moreover, in a combined PRD+PA, the gain should be made constant at low input power.

It is worth noting that the circuit in Figure 3.24 is not thermally stable. As the temperature increases, the Schottky diode current will decrease, causing the transistor collector current to increase. This increasing current causes the gain to increase as well.

3.4.4 Variable Active Predistortion Circuit

The circuit in Figure 3.24 is modified by adding a current mirror and two control voltages to adjust the gain and gain expansion at different input powers. The new circuit is shown in Figure 3.25. In this circuit, the base bias voltage is controlled by a second voltage supply V_c instead of the bias resistor R_b . Tuning base bias voltage using V_c is much more flexible than changing resistor R_b once the circuit is implemented monolithically. A current mirror is added in parallel with the Schottky diode to keep a constant gain at different diode bias points. While it is desirable to have a constant DC current I_c going through the transistor to have a constant transconductance, it is less desirable to have the same constant DC current flowing through the diode. For the active PRD to expand at different input powers, the Schottky diode must be biased at different points in its I-V curve. This can be achieved by adjusting the third voltage supply V_i . By varying this control voltage, the Schottky diode can be biased independently of the transistor bias at zero DC current as the minimum and at I_c as the maximum.

Figure 3.25: Schematic of a variable active PRD circuit.

Unfortunately this new circuit was simulated in Cadence to be unstable. While stability was not an issue in passive PRD circuits, it becomes a problem in an active PRD. Recall the common emitter circuit with degeneration. Three types of passive elements could be used to form emitter degeneration: an inductor, a resistor or a capacitor. The first two elements have been used to optimize for noise figure, stability and linearity. Adding a capacitor in the emitter is the main source of oscillation in this configuration. The presence of the junction capacitance of the forward biased Schottky diode and the capacitance of the current mirror in the active PRD are the main reasons of instability. A small series resistor can be added at the base to improve stability of this circuit, at the cost of increased noise and somewhat reduced gain. However the noise figure (about 7dB) of the active PRD is mainly due to the nonlinear resistor of the diode, so a small series resistor adds very little noise. Also, the overall effect of the noise of this PRD will be reduced by the gain of the amplifier preceding it. A small series resistor to improve stability is therefore justified.

Another remedy to the stability problem is to cascade a common collector stage before the PRD. It effectively reduces the effect of the nonlinear junction capacitance and resistance on the input impedance as input power varies. The circuit is simulated with CMC 24CFP package model and CMC PCB-TF2 test fixture model. The simulation result shows unconditional stable PRD. This circuit is presented in Figure 3.26 and selected as the final configuration for the active PRD.

Figure 3.26: Schematic of the variable active PRD with a common collector input stage.

After this circuit was stabilized, it was simulated with a two-tone signal to obtain the gain response. In a combined PRD+PA, the output power of the PRD is the input to the amplifier. Hence, to meet the output power requirement, six transistors are placed in parallel to handle the required power. The final circuit of the novel variable active predistortion is shown in Figure 3.27.

Figure 3.27: Circuit schematic of the novel variable active PRD.

The collector current of each transistor is set at $I_c=4\text{mA}$. This is to ensure that the Schottky diode bias points are always in the linear region below the point A shown in Figure 3.20. In this region, the slope or the equivalent resistance of the diode is constant. As a result, the gain at low input power is the same for different diode bias points. Above this region, the diode current increases sharply with a small change in voltage. This rapid change in current causes the equivalent resistance to drop significantly. Hence, it is desired to bias the diodes in the region below point A so that when input power increases, the rectified current will move the diode bias point up to the region above point A. In this region, the gain expands as the resistance reduces. The input power level where the gain expands depends on the original Schottky diode bias point. In general, the lower the bias point, the higher the input power is required before the gain starts to expand. The simulated gain expansions of the variable active PRD are shown in Figure 3.28. The results are summarized in Table 3.5 for different control voltage V_i and V_c .

Table 3-5: Summary of simulation results of the novel active PRD circuit.

Condition	V_c (V)	V_i (V)	I_{diode} (mA)	I_{ref} (mA)	Gain (dB)	$P_{1db-expansion}$	OIP3 (dBm)
A	4.50	1.33	1.75	2.25	13.3	-7.7dBm	15.5
B	4.61	1.22	2.25	1.75	13.3	-11.4	15.8
C	4.71	1.11	2.75	1.25	13.3	-14	15.0
D	4.82	0.98	3.25	0.75	13.4	-17.8	5.9

Figure 3.28: Gain expansion of the variable active PRD with different bias conditions.

The variable active PRD was then direct coupled with the amplifier 3. Using equation 3.17, the PRD was adjusted to yield a cancellation in the IMD3 level of the combined PRD+PA. While equation 3.17 only provided approximate values, circuit optimization was used extensively to obtain the final values for the control voltage V_c and V_i . Figure 3.29 represents the output and IMD3 power of the amplifier 3 and the combined PRD and amplifier 3. At the output power of 8dBm (marker A), the IMD3

level (-34dBm) to output signal of the amplifier 3 is -42dBc, which has already exceeded the -50dBc limit. However, for the combined PRD+PA3, the IMD3 level is -42dBm (marker B), which results in -50dBc between IMD3 and output power. So for the same output power level, the simulated distortion level has been reduced close to 8dB. Moreover, the distortion of the combined PRD+PA3 stays fairly constant as input power increases by 2dB. As the result, the combined PRD+PA3 can operate at higher output power than amplifier 3 itself, while still maintains the required level of distortion. Note that 3dBm improvement is equivalent to double the output power in linear range. From Figure 3.29, it is clear that the combined PRD+PA3 can easily operate at twice the output power level comparing to amplifier 3. The complete chip layout with the amplifier 3 and the active PRD are shown in Figure 3.30.

Figure 3.29: Simulated fundamental output power and IMD3 vs. input power for amplifier 3 (lower curve) and combined PRD+PA3 (upper curve).

Figure 3.30: IBBCUPDA chip layout showing the amplifier 3 and the active PRD.

3.5 Conclusions

Three amplifiers were designed and characterized as sample amplifiers used in this study. All three amplifiers have the similar Darlington pair topology, however a few modifications were made to improve their stability, gain, noise figure or layout complexity. The measured results for amplifiers 1 and 2 agree well with the design specifications as summarized in Table 3.1 for the commercial SGA-6489 amplifier. The lower in measured OIP3 point is due to inappropriate DC coupling and deficiencies in the foundry models. All fabricated circuits in the same run had IP3 point lower by 2-4dB.

A novel variable active PRD circuit was proposed, designed and simulated. The predistorter topology is a common emitter amplifier with Schottky diode emitter degeneration. The common emitter amplifier provides a positive gain while the Schottky diode serves as a nonlinear element to generate the required gain expansion. The predistorter was direct coupled with the amplifier 3. The combined PRD+PA showed an improvement in IMD3 level by 8dB.

The novel variable active PRD provides flexibility to a power amplifier designer. The active PRD can be designed to be a drive amplifier at low input power and a true linearizer to the power amplifier at high input power. It can replace the first or second driver amplifier in the power amplifier chain. The second driver amplifier seems to be the best place as the active PRD will be able to directly linearize the high nonlinearity power amplifier. The traditional passive predistortion circuit to linearize a power amplifier and a new proposed power amplifier topology with the second driver amplifier replaced by an active predistorter are illustrated in Figure 3.31 and Figure 3.32, respectively.

Figure 3.31: Typical passive predistortion to linearize a power amplifier.

Figure 3.32: Proposed power amplifier with second driver amplifier replaced by active predistorter.

4 Transformer Feedback Study

The architectures of wireless radio systems (i.e. heterodyne, direct conversion, offset PLL) differ in the way that the transmitting/receiving signal is processed. However, all of these architectures require signal amplification in both the transmitter (PA) and receiver (LNA). Figure 4.1 illustrates the fundamental signal amplification block of a radio system.

Figure 4:1: Signal amplification block in a radio system.

In both LNA and PA designs, impedance matching to 50Ω is necessary to allow maximum power transfer from/to the antenna through the transmitting/receiving switch. In the case of an LNA, the design goals are to minimize the noise figure, to provide sufficient gain, and to meet the required linearity. On the other hand, PA design goals are

to supply enough output power, to meet the stringent linearity requirement, and to operate efficiently. The common six performance specifications in amplifier designs are: gain, output powers, IP3, input and output return loss, and noise figure. The standard procedure for designing an amplifier involves selecting transistor(s) to meet gain and power requirements, biasing the transistor(s) and matching the amplifier to system impedance. It is worth noting that transistor biasing has great impact on the amplifier linearity, efficiency, and noise. This procedure gives three variables to meet six design goals. In order to achieve the minimum requirements, other variables are needed.

Feedback has been a simple and effective method used in amplifier design. Lossless transformer feedback used in LNA designs [15], [18] has proven its superiority over common passive feedback in achieving excellent noise figure. While reducing noise figure is the central focus of these transformer feedback LNA designs, improvement in IP3 is the result of either negative feedback [18] or sufficient bias current [15]. The authors did not optimize the transformers to achieve distortion cancellation in either design. This author is not aware of any published research concerned with optimizing transformer feedback to reduce intermodulation distortion of an amplifier. Double loop resistive feedback (such as amplifier 2 in this study) [38][39] has allowed multiple design goals to be simultaneously achieved. In [17], the authors attempted to use double loop feedback, consisting of a resistive feedback loop and a transformer feedback loop, to reduce noise and distortion in a LNA design. It is expected, at least in theory that a double-loop feedback transformer can achieve minimum noise figure, impedance match, and IP3 cancellation in LNA or PA.

Transformers have been used extensively in audio applications, high frequency (HF) and ultra high frequency (UHF) applications since the early days of electronics. These applications take advantage of one of two superior properties of transformers: transforming impedance levels and transferring energy between two electrical nets. In these applications, transformers are used to match high impedance to low impedance and vice versa, to isolate two electrical nets, to create balanced and unbalanced outputs, and/or to generate a large AC voltage from a small voltage. At these low frequency ranges, the energy is coupled by flux linkages of the transformer's winding inductors. To confine the magnetic flux, the inductors are wound on a high permeability common core, such as laminated iron or ferrite [41]. In radio frequency and microwave integrated circuit applications, core losses and self-resonance frequency limit the use of coil off-chip transformers in circuit design.

There are advantages in integrated circuit design to have on-chip high frequency transformers available. Miniature transformers are realized by wrapping and interwinding metal lines into two spiral or circular inductors so their dimensions can be reduced, and their self-inductances and mutual inductances can be increased. On-chip planar transformers were introduced and further studied and characterized in [43], [41], [42]. A three-dimensional transformer has been fabricated recently in multiple metal layers fabrication process yielding a very high coupling ($k=0.96$ at C band) and a small transformer structure [44]. A similar structure can be used in other fabrication processes to achieve a transformer with tight coupling transformer, which can then be used in double-loop transformer feedback.

This chapter will continue with a discussion on conceptual double loop transformer feedback in a single transistor. Next, transformer designs, measurements, and models (extracted from measurements) are presented. An understanding of transformer behavior with different impedance terminations will facilitate the design of double-loop transformer feedback.

4.1 Double-Loop Transformer Feedback

Transformer feedback has an advantage over negative resistive feedback in that it has inherently lower loss. At the same time, there is DC isolation between input and output. The result is an ideal feedback network where low noise and no DC connection between output and input are desired. The two separate windings and the ability to couple both voltage and current makes a transformer well suited for any of the four feedback topologies, named according to the feedback connection in the input and output network: series-series, series-shunt, shunt-series, and shunt-shunt. The effects of these different feedback topologies on a transistor's impedances have been well studied and characterized. Table 4.1 summarizes the changes of a transistor's input-and output impedances when feedback is applied [8]. Readers are encouraged to refer to the reference for a complete analysis of these feedback circuits.

From Table 4.1, it can be noted that in either series or shunt connections, the impedance increases or decreases by approximately the closed loop gain. Applying the same connections at both the input and the output terminals (series-series or shunt-shunt) caused the input-and output impedances to move in the same direction. When opposite

connections are applied at the input and the output terminals (series-shunt, shunt-series), the input and output impedances move in opposite directions. Combinations of the two topologies, series-series with shunt-shunt or series-shunt with shunt-series promises an ultimate match in the input and output impedances. Such feedback connections provide the amplifier designer with additional design parameters.

Table 4-1: Summary of impedances of different feedback topologies.

<i>Input \ Output</i>	Series	Shunt
Series	$Z_i = (1 + ak)z_i$ $Z_o = (1 + ak)z_o$	$Z_i = (1 + ak)z_i$ $Z_o = \frac{z_o}{(1 + ak)}$
Shunt	$Z_i = \frac{z_i}{(1 + ak)}$ $Z_o = (1 + ak)z_o$	$Z_i = \frac{z_i}{(1 + ak)}$ $Z_o = \frac{z_o}{(1 + ak)}$

Where

- a is the open loop gain
- k is the feedback network transfer function.
- z_i, Z_i are input impedances before and after applied feedback
- z_o, Z_o are output impedances before and after applied feedback

A single SiGe transistor is selected for a preliminary amplifier design. A standard bias network with two power supply sources was used to ensure class-A operation. Each of the above four single negative feedback topologies was simulated with ideal transformers. Additional block capacitors were added in the shunt arms at the input and output ports to ensure proper DC operation. The following observations were noted from the simulations:

- The shunt-shunt topology does not yield a stable circuit, even though blocking capacitors were selected to have resonance frequency higher than the unity gain frequency of the transistor. The shunt-shunt feedback is not a candidate for this amplifier. It is best use for a current input amplifier such as common-base.
- The series-series topology yields a marginally stable amplifier (stability factor is just bigger than unity). It is expected that the amplifier can become unstable when using a real transformer due to coupling and interwinding capacitances.
- Both series-shunt and shunt-series topologies yield a stable amplifier. The input and output impedances move in opposite directions as expected.

From the preliminary simulation observations, series-shunt and shunt-series negative feedback are promising candidates to implement double loop transformer feedback. One can create a double loop feedback around a transistor or an amplifier using two monolithic spiral transformers [2]. Figure 4.2 illustrates a common emitter transistor with four inductors, which represent primary and secondary windings of two transformers. By coupling these four inductors in different combinations, the four different negative feedback topologies above can be realized. By re-arranging the order of the feedback around the transistor (series then shunt or shunt then series), four different types of configuration can be made. These configurations are shown in Figure 4.2(a), (b), (c), and (d), respectively. Table 4.2 summarizes the different combinations of these inductors.

Figure 4:2: Four different topologies to net two transformers to form negative feedback around a common emitter amplifier (Bias circuit is not shown). a) Input: series then shunt, Output: shunt then series, b) Input: shunt then series, Output: shunt then series, c) Input: series then shunt, Output: shunt then series, d) Input: shunt then series, Output: shunt then series.

Table 4-2: Summary of inductor coupling to form double-loop transformer feedback.

<i>Input</i> \ <i>Output</i>	Series	Shunt
Series	L ₁ and L ₄	L ₁ and L ₂
Shunt	L ₃ and L ₄	L ₃ and L ₂

From Table 4-2, it is clear that the combination of inductor couplings in either shaded or non-shaded cells will not share a common winding. Combination of a shaded and a non-shaded cell will result in a common winding between two transformers. This common winding between two transformers in double loop feedback can be realized by utilizing a trifilar balun as proposed in [41]. This will reduce the number of inductors in Figure 4.2 from four to three.

To properly utilize double loop feedback for linearizing HBT transistor amplifiers, detailed knowledge of the transformer and transistor nonlinearities are required. Study of the HBT transistor nonlinearities will be left for future work. However, the next section will present the design and modeling of a monolithic spiral transformer in a SiGe process.

4.2 Monolithic Transformer Designs

To gain an understanding of transformer properties, monolithic spiral transformers were designed, simulated in Advanced Design Systems (ADS), fabricated using SiGe process, and measured to validate their performance in the given technology. A symmetrical transformer layout topology introduced in [41] is selected as it can be easily converted to a Balance Unbalance (Balun) structure with minimum modification. Baluns will be needed to design push-pull amplifiers using amplifier 1 or amplifier 2. The transformers were designed using the criteria outlined in [41], [42]. To achieve maximum possible coupling, minimum conductor spacing and width were selected. As suggested in [41], the coupling saturates if the winding has more than 3 turns. Windings having 3 turns were selected for the fabricated transformers. The primary inductance was calculated using a formula given in [42] to achieve maximum coupling at frequency over operating frequency at 1.95GHz.

$$f_{peak} = \frac{R}{2\pi L_p \sqrt{1-k^2}} \quad (4.1)$$

where R is approximately equal to 50Ω and the coupling coefficient k is assumed to be 0.8. Next, Analysis and Simulation of Spiral Inductors and Transformers for ICs (ASITIC) Computer Aid Design (CAD) software was used to determine the required dimension to achieve the value of L_p calculated above. The outer dimensions of $400\mu\text{m}$ and $200\mu\text{m}$ were selected to achieve good response at 1.95GHz and 6.85GHz, respectively. The transformer operating at 6.85GHz is for other applications, however, its results will be discussed for comparison between design and measurement. The

transformers were laid out in top metal layers to reduce substrate coupling and to minimize conductor losses.

The designed transformers were first laid out and simulated in ADS Momentum. The layout of a 1:1 transformer with outer dimension of $200\mu\text{m}$ is shown in Figure 4.3. The simulated S-parameters of this transformer are shown in Figure 4.4.

Figure 4:3: Layout in ADS Momentum of a 1:1 transformer with outer dimension of $200\mu\text{m}$

Figure 4:4: Simulated Momentum S-parameter (S_{11} , S_{21}) of a 1:1 transformer with outer dimension of $200\mu\text{m}$.

The final layouts of the transformers in Cadence allow both inverting and non-inverting measurements. The transformers were fabricated with Sirenza's SiGe process. The dice photographs of the fabricated transformers are showed in Figure 4.5 and Figure 4.6 for transformers with 400 μ m and 200 μ m outer dimension, respectively.

Figure 4:5: Dice photographs of transformers with outer dimension of 400 μ m.

Figure 4:6: Die photograph of transformers with outer dimension of $200\mu\text{m}$.

4.3 Monolithic Transformer Measurements

Since most RF test equipment has system impedance of 50Ω , measuring a 1:1 on-chip transformer is a simple task of applying 50Ω wafer probes at both primary and secondary ports and saving the S-parameters from a S-parameter network analyzer. The measured S-parameters of the 1:1 transformer with $\text{OD}=200\mu\text{m}$ in non-inverting and inverting configuration are shown in Figure 4.7 and Figure 4.8, respectively. The measured S-parameters of the 1:1 transformer with $\text{OD}=400\mu\text{m}$ in inverting configuration is shown in Figure 4.9.

The measured S_{21} and S_{11} of the 1:1 transformer with outer dimension of $200\mu\text{m}$ in non-inverting agree very well (within 0.3dB) with the Momentum simulated S_{21} and S_{11} as shown previously in Figure 4.4. Similar results were obtained for the transformer having $\text{OD}=400\mu\text{m}$. This validates the transformer design steps above.

Figure 4:7: Measured S-parameters (magnitude only) vs. frequency of a 1:1 transformer in non-inverting configuration with OD=200 μ m.

Figure 4:8: Measured S-parameters (magnitude only) vs. frequency of a 1:1 transformer in inverting configuration with OD=200 μ m.

Figure 4:9: Measure S-parameters (magnitude only) vs. frequency of a 1:1 transformer with OD=400 μ m.

From Figure 4.7 and 4.8, note the lower coupling in non-inverting configuration due to reduction in magnetic coupling between windings as explained in [41], [44]. Similar observations were made with other transformers.

While measuring 1:1 transformers is very straightforward, measuring 1:2 or 3:2 transformers in a 50 Ω system requires some post processing of the data to obtain the true transformer response. Moreover, transformers used in double-loop feedback do not always have two out of four ports AC grounded as in [15] [18]. In double-loop feedback, one or more ports of the transformers can be terminated with unknown impedances. This results in the need for a simple transformer model to use in simulating the double-loop feedback.

4.4 Monolithic Transformer Model

Modeling monolithic transformers has been the focus of much research. Models of monolithic spiral transformers are available for different fabrication processes such as GaAs, SiGe, Si [41], [42], [43]. However, these models are dependent on both transformer topology and the fabrication process. The focus of research here is to develop a model for the specific transformer(s) fabricated which can be used to explore the use of monolithic transformer feedback in PA linearization. An understanding of the major characteristics and behavior of a monolithic transformer under different port impedances will assist in designing double loop transformer feedback PA. The model topology for the spiral symmetric transformers used in this study has already been proposed in [42]. A equivalent circuit for a spiral symmetric transformer, neglecting substrate coupling for simplicity, is shown in Figure 4.10.

Figure 4:10: Model of a spiral symmetric transformer.

In the equivalent circuit shown in Figure 4.10, the passive elements are:

L_{kp} and L_{ks} are the leakage inductance of the primary and secondary windings

r_p and r_s are the conductor losses of the primary and secondary windings

C_p and C_s are the parasitic capacitance of the primary and secondary windings

C_{int} is the interwinding capacitance between windings.

L_m is the mutual inductance between windings

n is the ratio of the voltage in the secondary winding to the voltage in the primary

The layout of the spiral symmetric transformers used in this study was previously shown in Figure 4.3 to 4.6. A drawing of this layout is shown again in Figure 4.11 to illustrate the transformer physical parameters, which will be used in the calculations.

Figure 4:11: Layout of a spiral symmetric transformer.

In Figure 4.11 the variables in the physical layout of the transformer are:

OD is the outer dimension of the transformer

s is the spacing between the primary and secondary winding's conductors

w is the width of the primary and secondary winding's conductors.

d is the opening gap for conductor crossing in the primary and secondary windings.

x is the length of the crossing section.

To obtain approximate values for the transformer model parameters, the following set of low and high frequency measurements were made.

- DC measurements to extract r_p and r_s
- Low and midband frequency measurements to extract the windings self-inductances L_p , L_s and mutual inductance L_m .
- High frequency measurements to extract the C_p and C_s

The transformer model parameters can then be optimized beginning with these extracted values so that the models S-parameters have good agreement with measured S-parameters. The model will be validated with Momentum simulated results and measurement results. This model will be adopted for future double-loop transformer feedback circuit simulations. After validating the S-parameters of this fabricated transformer from Momentum, physical measurement, and modeling, in the future transformer design, the frequency dependent parameters will be extracted from the

Momentum simulation and the DC losses (r_p and r_s) can be found using the developed formulas in the next section.

4.4.1 DC Measurements

The conductor losses in the primary and secondary windings are extracted by applying a small DC voltage across each winding and measuring a DC current flowing through each winding. The applied voltage should be small enough that it does not result in a current exceeding the rated current of the winding's conductor and causing permanent damage to the transformer. Using the calibration substrate's short circuit, the losses of cable, connectors and wafer probe tip can be determined. The conductor losses can then be extracted using the following equation:

$$Conductor_loss = \frac{V_{DC}}{I_{DC}} - (Cable_loss + Probe_loss + Connector_loss) \quad (4.2)$$

The spiral symmetric transformer in Figure 4.9 does not have the same conductor loss in the primary and secondary windings since its primary winding is always longer. The primary and secondary unwound lengths of the spiral transformer as shown in Figure 4.11 with an integer number of turns N is given by the following equations:

$$l_{primary} = 4N * OD - 8N(N-1)(s+w) - (2N-1)d + 2(N-1)x \quad (4.3)$$

$$l_{secondary} = 4N * OD - 8N^2(s+w) - (2N-1)d + 2(N-1)x \quad (4.4)$$

where $x = \sqrt{d^2 + 4(s+w)^2}$ is the length of the crossing section (4.5)

N is the number of turn in the primary and secondary windings

From equations 4.3 and 4.4, it can be noted that the difference between primary and secondary inductor unwound lengths is:

$$\Delta l = 8N(s + w) \quad (4.6)$$

This equation reveals one interesting fact that the difference in length between the primary and secondary winding is independent of the transformer dimension. It depends only on conductor width, conductor spacing and the number of turns. This equation becomes useful when designing a 1:1 transformer using a spiral symmetric transformer, as care should be exercised to ensure equal self-inductance in both primary and secondary windings. This equation explains the conductor losses and the self-inductances being unequal, which was the main cause of less than ideal unity transformer turn ratio in a 1:1 transformer. This is very consistent with the measured results.

The resistance loss of each winding can then be determined, given the conductor sheet resistivity and conductor width, as:

$$r_p = \frac{l_{primary}}{w} * Conductor_sheet_resistivity \quad (4.7)$$

$$r_s = \frac{l_{secondary}}{w} * Conductor_sheet_resistivity \quad (4.8)$$

Table 4.3 shows the calculated and measured resistances in the primary and secondary windings of the fabricated transformers.

Table 4-3: Calculated and measured resistances of fabricated transformers.

Fabricated Transformer n, OD	Calculated Resistances (Ω)		Measured resistances (Ω)	
	r_p	r_s	r_p	r_s
1, 400 μ m	4.55	4.3	4.651	4.414
2, 400 μ m	1.23	3.02	1.646	3.659
0.67, 400 μ m	4.55	3.02	4.681	3.615
1, 200 μ m	2.03	1.78	2.392	2.112
1, 200 μ m	0.4	1.34	0.852	1.669
0.67, 200 μ m	2.03	1.34	2.363	1.658

The calculated results are made with the line width of 7 μ m, spacing of 3 μ m, opening gap of 20 μ m and sheet resistance of 7.35m Ω /square. There is good agreement between the measured resistances calculated using equations 4.3 and 4.4.

4.4.2 Low and Midband Frequency Measurements

At low frequency (50MHz-100MHz) the contributions of parasitic and interwinding capacitance are minimal compared to that of the winding self-inductances. At this frequency, the unwound winding lengths of both primary and secondary are much less than the wavelength. So the impedance looking in each winding can be approximated as [42]:

$$Z_{in} = r + j\omega L \quad (4.9)$$

where r is the series resistance and L is the self-inductance of the winding.

The winding self-inductances and mutual inductance can then be extracted by measuring S-parameters at low and midband frequency, reading off the reactive value from the Smith Chart of the S-parameter network analyzer, or converting S-parameters to Z-parameters, and applying the following equations [3]

$$L_p = \frac{\text{Im}(Z_{11})}{j\omega} \quad (4.10)$$

$$L_s = \frac{\text{Im}(Z_{22})}{j\omega} \quad (4.11)$$

$$L_m = \frac{\text{Im}(Z_{21})}{j\omega} \quad (4.12)$$

The turns ratio of the transformer as shown in Figure 4.10 and coupling coefficient can be found by

$$n = \sqrt{\frac{L_s}{L_p}} \quad (4.13)$$

$$k = \frac{L_m}{\sqrt{L_p L_s}} \quad (4.14)$$

Table 4.4 shows the measured self-inductance in the primary and secondary windings and turns ratio of the fabricated transformer.

Table 4-4: Measured winding inductances, mutual inductance and calculated turns ratio and coupling coefficient of the fabricated transformers

Transformer n, OD	Self Inductance (nH)		Mutual Inductance L_m	Turn ratio n	Coupling k
	L_p	L_s			
1, 400 μ m	6.68	6.03	5.3	0.95	0.84
2, 400 μ m	1.19	3.85	1.61	1.79	0.76
0.67, 400 μ m	6.68	3.85	4.41	0.76	0.86
1, 200 μ m	1.96	1.53	1.39	0.88	0.81
2, 200 μ m	0.35	1.11	0.49	1.78	0.79
0.67, 200 μ m	1.95	0.89	1.02	0.68	0.78

4.4.3 High Frequency Measurements

At high frequency, the winding inductances will resonate with the parasitic capacitances as well as the substrate coupling capacitance and interwinding capacitance. As it is difficult to differentiate the effect of these capacitances, the parasitic capacitances are approximated from the self-resonance frequency of the winding inductances. The measured parasitic capacitances are summarized in Table 4.5.

Table 4-5: Measured parasitic C_p, C_s .

Transformer n, OD	Parasitic Cap (pF)	
	C_p	C_s
1, 400 μ m	0.61	0.59
2, 400 μ m	2.72	0.52
0.67, 400 μ m	0.61	0.51
1, 200 μ m	0.25	0.24
2, 200 μ m	0.95	0.31
0.67, 200 μ m	0.34	0.74

Table 4-6: Summary of extracted parameters of the fabricated transformers.

Transformer n, OD	Metal Loss		Inductance		L_m	Capacitance		n	k
	r_p	r_s	L_p	L_s		C_p	C_s		
1, 400 μ m	4.651	4.414	6.68	6.03	5.3	0.61	0.59	0.95	0.84
2, 400 μ m	1.646	3.659	1.19	3.85	1.61	2.72	0.52	1.79	0.76
0.67, 400 μ m	4.681	3.615	6.68	3.85	4.41	0.61	0.51	0.76	0.86
1, 200 μ m	2.392	2.112	1.96	1.53	1.39	0.25	0.24	0.88	0.81
2, 200 μ m	0.852	1.669	0.35	1.11	0.49	0.95	0.31	1.78	0.79
0.67, 200 μ m	2.363	1.658	1.95	0.89	1.02	0.34	0.74	0.68	0.78

Table 4.6 summarizes the fabricated transformer parameters. These parameters with the calculated self-inductances were used for circuit simulation in ADS. As an example, the equivalent model of a 1:1 transformer with outer dimension of 200 μ m is shown in Figure 4.12.

Figure 4:12: Equivalent model of a 1:1 transformer with OD=200 μ m in non-inverting configuration.

Figure 4:13: Simulated S parameters (magnitude only) of the equivalent circuit of a 1:1 transformer in non-inverting configuration with OD = 200 μ m as shown in Figure 4.12.

Figure 4:14: Simulated S parameters (magnitude only) of the equivalent circuit of a 1:1 transformer in non-inverting configuration with OD = 400μm.

The equivalent circuit in Figure 4.12 is simulated in ADS. The S parameter results are shown in Figure 4.13. There is a good agreement between the model simulated S-parameter results with simulated Momentum results and measurement results in Figures 4.4 and 4.7, respectively. Figure 4.14 shows the simulated S parameter of the equivalent circuit of a 1:1 transformer with outer dimension of 400μm. Comparing with Figure 4.9, the results are within 0.4dB of each other. Please note that these simulated S-parameters were obtained using the extracted parameters in Table 4.6. If these parameters were optimized, even better results may be observed. These parameters are not optimized to demonstrate the fact that this model can be used for initial circuit simulation where simulation time is weighted more than a high accuracy. To obtain a model with high accuracy, the substrate losses and coupling should also be included. The author is currently investigating the use of the available HP4155A Semiconductor parameter analyzer to model the substrate effects or applying a different model suggested in the literature [42].

4.5 Conclusions

The feasibility of using double-loop transformer feedback to linearize transistor amplifiers was discussed and conceptual double-loop transformer feedback circuits are proposed for a single HBT transistor. Preliminary results indicate the series-shunt with shunt-series is the best combination to loop two transformers. A detailed study of this configuration to linearize HBT transistor amplifier is left for future work.

However, a study of monolithic transformers was carried out. An experimental procedure to obtain a good transformer model for circuit simulation was realized. It will assist in future transformer designs for a double-loop feedback transformer. Attention must be paid when designing monolithic transformers to linearize power amplifiers that the DC current does not exceed the rating limit of the metal winding of the transformers.

5 Conclusion

5.1 Summary

The major goal in performing this research was to gain an understanding of the various linearization techniques available for transistor power amplifiers and to implement novel circuits to linearize amplifiers to be used in CDMA IS-95 wireless systems. To achieve this goal, practical circuits from four linearization techniques were studied. Amplifiers and transformers were designed, fabricated and measured to fully characterize them in practice.

The study of linearization techniques resulted in a selection of two promising methods to linearize amplifiers, namely predistortion and transformer feedback. The advantages of these techniques are low power requirement, low loss, large IP3 improvement, and monolithic implementation. The results of simulation studies are a novel variable PRD circuit with positive gain of 13dB and more than 5dB in gain expansion, a new method in designing a combined active PRD + PA to realize lower intermodulation distortion levels, and a conceptual design using double-loop feedback to linearize amplifiers.

Three Darlington pair amplifiers were designed, fabricated and measured. The measured results agreed well with the simulated results. These amplifiers were the targets

for the new variable active PRD developed subsequently. The PRD circuit has a clear advantage over conventional PRD as it can provide gain of 13dB and adjustable gain expansion of 5dB. The active predistortion circuit can be adjusted to linearize a wide range of amplifiers. The new PRD circuit reduced the intermodulation distortion simulated for one of the designed amplifier by 8dB and allowed the amplifier to operate at higher output power level.

Monolithic transformers were designed, fabricated and measured. A transformer model was developed based on a model reported in the literature. The model will allow a designer to investigate transformer feedback as a method to linearize transistor amplifiers.

5.2 Future Work

In future, first and foremost will be the measurement of the fabricated amplifier 3, the novel variable active PRD and the combined active PRD+PA. The test procedure should be very similar to that used for amplifiers 1 and 2. The results of this test will be used to optimize the design of the novel active PRD circuit.

A three-stage PA for handset applications (due to limitation of fabrication process available) used in CDMA IS-95 with specifications given in Table 5.1 will be designed with and without the active PRD in its second stage to experimentally verify the expected linearization improvement.

More work must be done to characterize SiGe HBT transistor nonlinearities. With such knowledge, transformer feedback circuits can be designed to linearize HBT transistors to use in LNA and PA designs. For RF circuit designers with limited access to

fabrication processes, circuit designs which improve the transistor amplifier linearity are always in great demand. Double- loop transformer feedback is a promising candidate, which will be investigated by the author.

Table 5-1: Proposed PA specifications

Specifications	Values
Frequency	1800MHz – 2400MHz
Gain	30dB
P_{1dB}	29dBm
Intermodulation level	-50dBc at 3-6dB PBO
Return Losses	12-15dB
Noise Figure	6-8dB
V_{dc}	5V
I_{dc}	350mA-400mA
PAE	45% max
Technology	SiGe HBT

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Appendix A: Characterization of Amplifier Nonlinearities

While the transistor causes the nonlinearity in all transistor PAs, it is the wireless system modulation scheme, which sets the linearity requirement of all PAs. In the CDMA IS-95 system, the information data is modulated using Quadrature Phase Shift Keying (QPSK) modulation scheme to superpose onto the RF carrier. PSK modulation itself is a constant envelope modulation scheme in nature. However, the band-limiting of IS-95 system results in envelope variation in QPSK which causes both phase (by nature) and amplitude (due to band limiting) modulations.

A non-constant envelope exhibits a peak envelope power (PEP) higher than the signal's average power of a continuous wave. When the PA operates in a strongly nonlinear region, this PEP must be considered so that the linearity requirement is not violated. The nonlinearity measures of PA in this region are AM/AM conversion, AM/PM conversion and Adjacent Channel Power Ratio (ACPR). In the case of IS-95 system, class-A PA often operates in a weakly nonlinear region (power-back off) where distortion levels are often less than -30dBc [25]. In this region, important measures of amplifier nonlinearities are 1dB compression point, Intermodulation distortion Products (IP), and distortion level. These amplifier nonlinear characteristics are discussed in the next sections.

A.1 Weakly Nonlinear- IP and 1dB Compression

An ideal amplifier has a linear response to an infinite range of input signal levels. However, a practical nonlinear amplifier has an output response described by a power series:

$$v_{out} = \sum_{n=0}^{\infty} a_n v_{in}^n = a_0 + a_1 v_{in} + a_2 v_{in}^2 + a_3 v_{in}^3 + \dots, \quad (\text{A.1})$$

where v_{in} is the RF input signal, v_{out} is the RF output of the amplifier, and a_n is a scalar coefficient of the power series. In most modern amplifiers, third-order approximation often gives acceptable accurate results in the weakly nonlinear region. Hence higher-order terms such as fifth-and seventh-order are neglected. This type of nonlinear input-output response always results in IP. A simple two-tone analysis shows how IP are formed for the above response. For two-tone analysis, the input signal consist of two equal amplitude RF signals closely spaced in frequency and in or near the desired frequency band of operation of amplifier:

$$v_{in} = A \cos(\omega_1 t) + A \cos(\omega_2 t) \quad (\text{A.2})$$

where A is the signal amplitude at each input tone. When Equation A.1 and A.2 are combined, the output, after using some common trigonometric identities, can be expressed as Equation A.3:

$$\begin{aligned}
v_{out} &= a_0 + a_2 A^2 && \text{DC term} \\
&+ \left(a_1 A + \frac{9}{4} a_3 A^3 \right) \cos(\omega_1 t) + \left(a_1 A + \frac{9}{4} a_3 A^3 \right) \cos(\omega_2 t) && \text{Fundamental terms} \\
&+ \frac{1}{2} a_2 A^2 \cos(2\omega_1 t) + \frac{1}{2} a_2 A^2 \cos(2\omega_2 t) \\
&+ a_2 A^2 \cos(\omega_1 - \omega_2)t + a_2 A^2 \cos(\omega_1 + \omega_2)t && \text{IP2} \\
&+ \frac{1}{4} a_3 A^3 \cos(3\omega_1 t) + \frac{1}{4} a_3 A^3 \cos(3\omega_2 t) && \text{Third order harmonic} \\
&+ \frac{3}{4} a_3 A^3 \cos(2\omega_1 - \omega_2)t + \frac{3}{4} a_3 A^3 \cos(2\omega_2 - \omega_1)t \\
&+ \frac{3}{4} a_3 A^3 \cos(2\omega_1 + \omega_2)t + \frac{3}{4} a_3 A^3 \cos(2\omega_2 + \omega_1)t && \text{IP3} \\
&+ \dots
\end{aligned}
\tag{A.3}$$

Higher-order terms have been neglected in equation A.3 for simplicity. The DC term is often negligible or canceled out by coupling capacitors. The second order harmonic and IP2 contains spectral components at $2\omega_1$, $2\omega_2$, $\omega_1 - \omega_2$, and $\omega_1 + \omega_2$, which increase twice as fast in amplitude as the RF input signal. Fortunately, these even-order IP are typically far enough out of the frequency band of operation to be of little concern or disregarded completely in differential or push-pull amplifier topologies. The third order IP3 are particularly troublesome in amplifier design because the signals at frequencies $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ fall within the pass band of the desired fundamental signals. For example, given two signals $\omega_1=1950\text{MHz}$ and $\omega_2=1951\text{MHz}$, the IP frequencies will be at $2\omega_1 - \omega_2 = 1949\text{MHz}$ (lower side IP3) and $2\omega_2 - \omega_1 = 1952\text{MHz}$ (upper side IP3). The IP3 products appear as sidebands to the desired signals at the same frequency spacing of the two fundamental signals. Moreover, these IP3 terms increase exponentially in magnitude by a power of 3 when compared to the desired fundamental

signal. Figure A.1 shows, up to third-order, the components at the output of a nonlinear amplifier.

Figure A: 1: Output components of a amplifier having third-order nonlinearity.

Intermodulation distortion is characterized by an intercept point. The intercept point is defined as the RF input signal power level at which an undesired IMD is equal to the desired fundamental output signal. Of particular interest to PA design engineers is the input third-order intercept point (IP3). From Equation A.3, the IP3 can be found by equating:

$$a_1 A = \frac{3}{4} a_3 A^3 \implies A_{IP3} = 2 \sqrt{\frac{a_1}{3a_3}} \quad (\text{A.4})$$

In general, the n^{th} -order intercept point could be found by equating the desired output signal to the n -order IMD products output signal. The n^{th} -order intercept point can be defined as:

$$IP_n = A + \frac{\Delta}{n-1} \quad (\text{A.5})$$

where A is the RF input signal in dBm and Δ is the difference in dB between the desired output signal level and undesired IP levels at the RF input signal A (dBm). This concept is illustrated in Figure A.2

Figure A: 2: Amplifier fundamental and n-order IMD transfer functions

The intercept point of an amplifier is a good indication of the amplifier's nonlinearity. However, it is fictional in that the amplifier will enter saturation with a signal level well before the IIP_n point. The 1-dB compression point (P_{1dB}) indicates this saturation region in an amplifier. The P_{1dB} is defined as the input signal power level at which the output signal power has decreased 1-dB from the linear gain level. From Equation A.3, the P_{1dB} can be found by equating:

$$20 \log \left(\frac{a_1 A + \frac{9}{4} a_3 A^3}{a_1 A} \right) = -1 \text{ dB} \Rightarrow A_{1 \text{ dB}} = 2 \sqrt{\frac{a_1}{3 a_3}} \sqrt{\frac{1 - 10^{-\frac{1}{20}}}{3}} = A_{IP3} \sqrt{\frac{1 - 10^{-\frac{1}{20}}}{3}} \quad (\text{A.6})$$

or in term of dB, we have $A_{1 \text{ dB}} = A_{IP3} - 14.4 \text{ dB}$ (A.7)

This relationship is a good rule-of-thumb for calculating IP3 from $P_{1 \text{ dB}}$ or vice versa in two-tone analysis. In practice it will not hold true due to high-order effects. Third-order intercept (IIP3) and $P_{1 \text{ dB}}$ points as given in A.3 and A.7 are good indications of an amplifier's nonlinearity in the weakly nonlinear region. Since the amplifier will not often operate at or above $A_{1 \text{ dB}}$ input level because of the presence of high distortions, it is beneficial to calculate the input level given Δ in dBc. Assume that third-order distortion is the strongest in this weakly nonlinear region, then from A.3 and A.7, the operation input power can be derived as follow:

$$A_{\text{operation}} = A_{1 \text{ dB}} + 14.4 \text{ dB} - \frac{\Delta}{2} \quad (\text{A.8})$$

For CDMA IS-95 system, Δ should be less than 50dBc. Then using equation A.8, the input level should be

$$A_{\text{operation}} = A_{1 \text{ dB}} - 10.6 \text{ dB} \quad (\text{A.9})$$

In this back off region, the amplifier is linear but very inefficient. What equation A.9 means is to transmit a 10dBm (10mW) signal, it is required, at the minimum, an amplifier which can safely transmit a 20dBm (100mW) signal.

A.2 Strongly Nonlinear - AM/AM, AM/PM & ACPR

AM/AM effect is the fundamental cause of signal compression, which is presented in the 1dB compression point (P_{1dB}) of the above analysis. AM/AM effect is the direct result of amplifier nonlinearity as can be seen in Equation A.1 or in equation A.3 when two-tone signal is applied. At high input level, the desired amplifier linear gain a_1 is reduced to $a_1 - \frac{9}{4}|a_3|A^2$. This deviation in the amplifier's gain is the AM/AM effect.

Unlike the AM/AM effect, AM/PM effect is harder to analyze based on the equation A.1 as this equation has assumed a memoryless system. To fully understand the AM/PM effect, a Volterra series analysis should be carried out, however it is not within the scope of this study. It is worth to note that the AM/PM effect is highly unpredictable as it's expansion and compression characteristic varies from amplifier to amplifier.

In the strongly nonlinear region, the presence of higher-order distortion such as fifth-and seventh cannot be ignored. The presence of third-fifth-seventh-and even higher-order IP needs a different method in measuring amplifier's nonlinearity. ACPR becomes the new figure-of-merit in defining an amplifier's nonlinearity in this region and in multicarrier wireless systems. ACPR is defined as the measured power in an adjacent channel of a specified bandwidth relative to the power in the main channel of specified bandwidth. There is an effort to relate the ACPR with IP3. Figure A.3 illustrates the ACPR at different offset frequencies in spectral domain.

Figure A: 3: ACPR in spectral domain