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A Fully Differential CMOS Charge Pump and VCO At High Frequency

By
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A Thesis submitted to
the Faculty of Graduate Studies and Research
in partial fulfillment of the requirements for the degree of
Master of Applied Science (Electrical)

Department of Electronics
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Abstract

This thesis is about the design of high frequency, low noise and low power oscillators. Phase noise, frequency and power consumption are some of the important factors in VCO design.

As part of this research, two chips were fabricated using IBM's CMOS 0.13 micron RF technology. The first chip consisted of two high-frequency negative transconductance VCOs designed for oscillation frequencies of 20 GHz and 30 GHz, while measured oscillation frequencies were 16 GHz and 23 GHz, respectively. Both VCOs have also been tested to have a 1 GHz tuning range and consume less than 4 mA of current each.

The second chip consisted of three VCOs, expected to operate at 17 GHz and have a tuning range of 1 GHz, however, these have not been tested. The first is an improvement of the VCOs from the first chip. The second is a fully differential (input and output) negative G_m VCO. The third is also fully differential, but uses a constant current source.

A fully differential charge pump, operating at 200 MHz with a charge pump current of 200 μ A, is also fabricated to complement the fully differential VCOs.

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Abbreviations

RFIC	Radio Frequency Integrated Circuits
RF	Radio Frequency
MIM	Metal Insulator Metal
PLL	Phase-Locked Loop
VCO	Voltage-Controlled Oscillator
CMOS	Complementary Metal Oxide Semiconductor
SOI	Silicon-on-Insulator
FM	Frequency Modulation or Frequency Modulated
AM	Amplitude Modulation or Amplitude Modulated
CP	Charge Pump
G_m	Transconductance
PFD	Phase Frequency Detector
CMFB	Common-Mode Feedback
IBM	International Business Machine
CMC	Canadian Microelectronics Corporation
ESD	Electro-Static Discharge
PCB	Printed Circuit Board
VHDL	VHSIC Hardware Description Language
RMS	Root Mean Squared
DSP	Digital Signal Processor
LNA	Low-Noise Amplifier
ISM	Industrial Scientific Medical
EM	Electro-Magnetic
DC	Direct Current
AC	Alternating Current
Q	Quality Factor

Chapter 1 Introduction

1.1 Motivation

Incoming transmission frequencies continue to increase due to increased bandwidth and speed of data communications. As lower bands are becoming increasingly congested, there is the also need to move to higher frequencies. To address higher incoming frequencies in radio architectures, engineers are faced with many challenges. One issue of importance is overcoming the effects of phase noise in phase-locked loop (PLL). A secondary issue of importance is the challenge to save power. Power supplies are getting smaller and current consumption is being reduced.

As incoming frequencies increase, many parts of the PLL also need to increase in frequency. The voltage-controlled oscillator (VCO) is forced to operate at higher frequencies to down-convert incoming signals. The charge pump also operates at higher frequency. Designing high frequency VCOs and charge pumps optimized for phase noise allows high frequency signals to be demodulated properly by the backend digital signal processor. However, at higher frequencies, phase noise tends to be worse, so research to reduce phase noise is also very important.

From a circuit point of view, poor phase noise can be attributed to bias noise from the current source, poor sizing of the transistors and inductors, improper placement of the varactors, noise from the supply and improper device selection, etc. Another way of reducing noise is through the use of differential signals at both the input and output.

From a layout point of view, phase noise can be attributed to improper selection of transistor fingers and/or multiplicity, improper selection of varactor fingers and/or multiplicity, improper distance of inductor substrate contacts, etc.

Although phase noise can be reduced, it cannot be eliminated. Even if the VCO and charge pump are fully optimized for minimum phase noise, there will still be noise from the passive and active components.

The motivation of this research is to investigate ways of reducing phase noise of the VCO and charge pump, while operating at a high frequency.

1.2 Contributions

There are three main contributions in this thesis

1. In this thesis, the design, fabrication and measurement of negative G_m complementary cross-coupled VCOs at high frequency is undertaken. VCOs are designed with the purpose of reducing phase noise, while maintaining a high frequency. Techniques to reduce phase noise included differential design and the use of fully differential varactors. A charge pump is also designed to complement the VCOs. Final measurements of frequency and tuning range were in close agreement with simulations demonstrating the quality of the models and verifying the design technique. Further simulations demonstrate that the VCO and charge pump are functional when combined in a full phase-locked loop.
2. A mechanism is proposed for a varactor structure that is shown to reduce $1/f$ noise substantially in oscillators by moving the $1/f$ noise corner to a lower frequency.
3. An open-loop technique based on varying pulse widths is used to measure charge pump linearity. This test can be done on a stand-alone charge pump, eliminating the need to design a complete loop for this test.

1.3 Thesis Overview

This thesis is organized as follows.

First a review of PLLs and phase noise is presented in Chapter 2. This review involves a discussion of the PLL as a frequency synthesizer and the individual components of the loop. Sources of noise for both the VCO and the Charge Pump are discussed in relation to phase noise of the loop. Existing VCO architectures and a differential Charge Pump for PLLs are also presented in Chapter 2.

In Chapter 3, variations of the same VCO are designed. Phase noise calculations are done for the general VCO. This chapter consists of two chips sent for fabrication. This first chip is an experimental design used to investigate the reliability of the process since the technology is new to the university. Unlike TSMC's CMOS 0.18 micron technology, the technology used does not have a standardized track record. The second chip has improvements over the first one, schematic-wise and layout-wise. A Charge Pump is also on this chip and is designed and analyzed as well in this chapter. This chapter also includes simulations. The VCO simulation results are compared and discussed. The charge pump is optimized and studied through the use of extensive simulations.

Chapter 4 holds the laboratory results of the first chip. Comparisons are made between post-layout simulation results and labs results. The second chip results are not included since the foundry has not shipped the chips to the department before the termination of this thesis. However, post-layout simulation results are still shown.

Chapter 5 focuses on simulations of a complete PLL based on the components proposed in Chapter 3.

Finally, conclusions are presented in Chapter 6.

Chapter 2 Background

This chapter covers the background theory of receivers in general, PLLs as frequency synthesizers, VCOs and charge pumps. It presents VCO and charge pump designs to be used in frequency synthesizers. Sources of noise for both designs and how they translate to phase noise are studied.

2.1 Receiver

In most wireless devices, there is a receiver. A typical receiver is shown below in Figure 1.

Figure 1 Typical Receiver

An incoming radio frequency (RF) signal is received by an antenna, as well as other signals. The signals are then amplified by a low-noise amplifier (LNA). The LNA raises the signals' power without raising the noise power. The Image Reject Filter removes the image associated with the operating frequency. The signal is then mixed down with a signal from the frequency synthesizer via the Mixer. The Intermediate Frequency Filter is a channel select filter to suppress unwanted channels. Finally, the backend processes the information.

Every component in a receiver is important, but the design of the PLL is vital. This is because it consists of many parts that interact with each other and many parameters to consider.

2.2 Phase-Locked Loops (PLL)

A PLL has many applications. It can be used for synchronization, frequency synthesis, or indirect frequency demodulation [1]. When a PLL is used as a frequency synthesizer, it acts to synthesize a required frequency needed to down-convert an incoming signal. A frequency synthesizer consists of many components as shown in Figure 2, two of which will be covered in this thesis. They are the voltage-controlled oscillator (VCO) and the charge pump (CP). The other components are the phase-frequency detector (PFD), loop filter and divider.

Figure 2 A Frequency Synthesizer

A PLL is essentially a negative feedback loop, meaning the feedback damps the amount of unwanted disturbances in the loop. The divided down VCO phase and frequency are driven such that they are locked to the input phase and frequency of the reference signal.

To ensure that the loop is locked, we need to understand the loop dynamics of the PLL by writing transfer functions in the Laplace domain. Transfer functions can be written for each component of the PLL. This is shown in Table 1.

Table 1 Transfer Functions for Each Component of the PLL

Type	Transfer Function
Phase Detector and Charge Pump	$i_d(s) = K_{phase} * [\theta_i(s) - \theta_o(s)]$
Low-Pass Filter	$V_c(s) = i_d(s) * F(s)$
VCO and Divider	$\theta_o(s) = V_c(s) * \frac{K_{vco}}{s} * \frac{1}{N}$

Therefore a closed loop gain transfer function can be written in terms of $\theta_o(s)/\theta_i(s)$ as

$$H(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{KF(s)}{s + KF(s)} \quad (1)$$

where $K = K_{vco}K_{phase}/N$.

This closed loop transfer function allows us to predict the behavior of the PLL. It allows us to extract two important parameters, ω_n and η . ω_n is the natural frequency which is the combined effect of the loop filter impedance, $F(s)$, and the natural filtering effect of the loop. η is the damping constant which gives a measure of the speed of the response of the loop.

A common type of loop filter impedance for $F(s)$ is the integrator with phase lead correction in (2).

$$F(s) = R + \frac{1}{sC} = \frac{sCR + 1}{sC} \quad (2)$$

If this loop filter is used, ω_n and η can be solved to be

$$\omega_n = \sqrt{\frac{K}{C}} \quad (3)$$

$$\eta = \frac{R}{2} \sqrt{KC} \quad (4)$$

We can also predict whether or not the loop will be stable by solving for ω when the open loop gain is 0dB and by ensuring sufficient phase margin ($\phi_m \geq 45^\circ$).

One very important aspect of writing transfer functions is that they allow us to determine noise shaping in the PLL. The noise of most concern in a PLL is phase noise.

2.3 Phase Noise of PLLs

Each component of the PLL contributes to the overall phase noise. In the frequency domain, phase noise is associated with the level of noise in the skirts, at a particular offset, with respect to the carrier. Phase noise is measured in dBc/Hz at some particular offset frequency. The “c” represents carrier or the amount of dBs down from the carrier. A diagram of the frequency domain phase noise is shown in Figure 3.

Figure 3 Single Tone with Skirts showing Phase Noise with respect to the carrier at an offset

Due to the filter, $F(s)$, and the natural filtering effect of the loop, noise sources from different parts of the loop are shaped differently to the node of interest. This is because noise sources from each component of the loop “see” a different transfer function [2].

The noise generated by the PFD, CP, loop filter, and divider is referred back to the input. The noise transfer function for them can be derived from the diagram below in Figure 4.

Figure 4 Diagram for the Noise Transfer Function of the PFD, CP, Loop Filter and Divider

The transfer function is shown below.

$$\frac{\theta_{noise out A}(s)}{\theta_{noise A}(s)} = \frac{N * KF(s)}{s + KF(s)} \quad (5)$$

where $K = K_{vco}K_{phase}/N$. Equation (5) is a low-pass filter, which means that all noise generated by the PFD, CP, loop filter, and divider will be low-pass filtered.

The VCO, however, “sees” a different transfer function. The noise generated by the VCO is referred to the output. The noise transfer function for the VCO can also be derived by looking at Figure 5.

Figure 5 Diagram for the Noise Transfer Function of the VCO

The transfer function for the VCO noise source is shown below.

$$\frac{\theta_{noise\ out\ B}(s)}{\theta_{noise\ B}(s)} = \frac{s}{s + KF(s)} \quad (6)$$

where $K = K_{vco}K_{phase}/N$. Equation (6) is a high-pass filter, which means that all noise from the VCO will be more dominant at higher frequencies.

Low-pass filtered noise generated by the PFD, CP, loop filter, and divider is combined with high-pass filtered noise generated by the VCO to achieve the overall phase noise and noting that noise adds in power. Both corner frequencies in (5) and (6) have the same natural frequency (loop bandwidth), ω_n . Therefore, optimization of ω_n is crucial in the

reduction of phase noise, however, reduction of the noise sources is always the designer's first obligation.

The next sections describe specific components of the loop and their respective noise sources.

2.4 Voltage-Controlled Oscillators (VCO)

A VCO is an oscillator that is tunable (frequency selective) based on a DC voltage. The VCO takes a DC voltage supplied by the charge pump and outputs a sine or square wave. This wave goes to both the mixer and the divider in a typical receiver.

Oscillators, not necessarily tunable, are broken up into two groups, ring oscillators and LC oscillators. Ring oscillators depend on the amount of time that it takes current to charge a capacitor, whereas LC oscillators depend on the resonance of both the inductor (L) and capacitor (C). Ring oscillators have poor phase noise, but can have excellent tuning range. LC oscillators have great phase noise, but often limited tuning range.

There are 3 main LC oscillators: the Hartley oscillator, the Colpitts oscillators and the negative G_m oscillators. This thesis focuses only on the negative G_m oscillator.

All oscillators have the same purpose of providing a single tone at a specific frequency. However, due to noise (phase noise), an oscillator exhibits a skirt around the tone. This was shown in Figure 3.

2.4.1 LC Resonance

In a negative G_m oscillator, both the inductor and capacitor act to transform energy. Energy is transferred back and forth between the magnetic field of the inductor and the electric field of the capacitor. All that is needed is energy to start the oscillations, usually noise. Oscillations continue because of the law of conservation of energy.

If losses were non-existent, the oscillations would continue indefinitely. Because of losses, a source of energy needs to exactly compensate for the losses. This source of energy can come from transistors. For a $-G_m$ VCO, the source of energy is the cross-coupled negative transconductance.

Losses can be modeled by a resistor and comes from losses in the inductor, capacitor and other parts of the circuit. The resistor dissipates the energy in the form of heat. An RLC model is shown below in Figure 6.

Figure 6 RLC model

The steady state frequency of oscillation is set by (7) below.

$$f_{osc} = \frac{1}{2\pi\sqrt{LC}} \quad (7)$$

This equation is derived from the RLC's system response to an impulse of current.

2.4.2 Linear Model of Oscillation

To make oscillations continue indefinitely, a source of energy is required to balance the energy lost by heat. Amplifier transistors provide feedback to replenish the lost energy. This can also be thought of as negative resistance because it negates the losses from the resistor.

A linear feedback system is usually shown in textbooks to show the conditions for oscillation. This is shown in Figure 7.

Figure 7 Linear Feedback Model of an Oscillator

The transfer function for this system is given in (8).

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{A(s)}{1 - A(s)B(s)} \quad (8)$$

From this equation, the closed loop gain approaches infinity when the open loop gain $|A(s)||B(s)| = 1$ at resonance and $\angle A(s)B(s) = 2n\pi$. These two conditions are also known as the Barkhausen criteria. Because the closed-loop gain is close to infinity, it is possible for a small input voltage to become a large output voltage.

In reality, however, the voltage amplitude is limited. The amplitude continues to grow until a limit is reached, usually the supply rails or a current limit. At this point the losses are just cancelled out by the negative resistance and the open loop gain is constant at one.

The process by which the oscillation grows is called positive feedback. This process is in contrast to the PLL, since the PLL is driven in a negative feedback.

2.4.3 Oscillator Tunability

The RLC model of Figure 6 oscillates at a particular frequency. To make the oscillator tunable, varactors are needed. A varactor is a variable capacitor that is voltage-controlled. A DC voltage is applied to select a desired capacitance. An accumulation MOS varactor also known as an AMOS varactor is described below.

An AMOS varactor is built using a MOS transistor-like structure in an N-well, with two n+ regions shorted as shown in Figure 8. The N-well provides isolation from the substrate so that the voltage of the well need not be the voltage of the substrate.

Figure 8 Cross-section of the AMOS Varactor

It can be seen that there are two capacitors in series from Figure 8. These two capacitors make up the three regions of operation of the varactor.

The first region is accumulation which is when a positive voltage is applied to the gate. Electrons are attracted to the surface. This action forms the second electrode of a capacitor. This capacitor is the oxide capacitance, C_{ox} , and is the largest capacitance the varactor can achieve.

The second region is depletion. Depletion is achieved when the voltage is decreased below the flatband voltage and a depletion region forms under the gate oxide (electrons are depleted). This depletion region has a decreasing capacitance that is dependent on the decreasing voltage. The depletion capacitance, C_{dep} , is in series with the oxide capacitance, C_{ox} , because the holes are electrically isolated from the two n+ regions. This means the total capacitance of the varactor is decreasing as the voltage is decreasing.

Eventually, the voltage at the gate becomes negative and the depletion region size is fixed and at its largest size. Inversion is achieved since there is a layer of holes at the surface

of the channel. This region has the smallest C_{dep} , which means the total varactor capacitance is at its minimum.

2.4.4 $-G_m$ VCO Configuration

The typical negative G_m VCO is shown below in Figure 9.

Figure 9 NMOS Negative G_m VCO

From Figure 9, it is apparent that this circuit has a differential output (V_{out-} and V_{out+}), but a single-ended input (V_{ctrl}). The tunable capacitors (varactors) and inductors are visible. The resistive losses are overcome by the negative transconductance of the transistors, which act like amplifiers.

2.4.5 Negative Transconductance for the $-G_m$ VCO

The amount of negative transconductance can be calculated with the use of a small signal model as shown in Figure 10.

Figure 10 Small Signal model for the Negative Resistance of the Negative G_m Oscillator

The small signal model above is drawn using the transistor T model.

Therefore using Kirchoff's current law,

$$I_{in} = \frac{V_{in}}{r_{e1} + r_{e2}} - g_{m1}V_{gs1} + g_{m2}V_{gs2} \quad (9)$$

It can also be noted that $V_{gs1} = -V_{gs2}$, since the output at each drain of Figure 9 is equal but opposite in polarity. Also $g_{m1} = g_{m2}$ and $r_{e1} = r_{e2}$, since the transistors are identical and biased the same way.

Simplifying,

$$Z_{in} \geq \frac{V_{in}}{I_{in}} = \frac{-2}{gm} \quad (10)$$

Equation (10) gives us the requirement for oscillation for the negative G_m oscillator. The negative resistance Z_{in} needs to be greater than $-2/gm$ [3].

2.4.6 $-G_m$ VCO Variations

There are many other $-G_m$ VCO variations, two of which are shown below.

Figure 11 PMOS Version of the $-G_m$ VCO

The PMOS version of the $-G_m$ VCO has positive and negative features compared to the NMOS version. The PMOS version has less flicker noise also known as in-band $1/f$ noise. For the same current, the PMOS transistors need to be larger which increases parasitic capacitances. The current source close to the rail also offers isolation from supply fluctuations. Lastly, the DC level is not affected by noise fluctuations from the current source since the output is referenced to ground (i.e. the varactors are not frequency modulated by noise).

The other version is the complementary $-G_m$ VCO which uses both PMOS and NMOS transistors, as shown in Figure 12.

Figure 12 Complementary $-G_m$ VCO

This complementary VCO uses half the startup current compared to an all NMOS or all PMOS version since there is twice the transconductance, half coming from the PMOS transistors and the other half coming from the NMOS transistors.

By matching the g_m s of the NMOS and PMOS transistors, this type of VCO also has superior phase noise over all NMOS or all PMOS designs. Matching the g_m s allow the rise and fall time to be matched. If the rise and fall time are matched, less noise can potentially be mixed to the fundamental [4]. This is because fewer harmonics are available from a balanced output voltage swing.

Another advantage of this VCO is that the output amplitude is twice as large as the all PMOS or all NMOS designs [5]. The swing in this case is given by

$$V_{\text{tank}} = \frac{4}{\pi} * I_{\text{bias}} * R_p \quad (11)$$

2.4.7 Differential Tuning Voltage

The VCOs presented so far all have a differential output, $V_{\text{out-}}$ and $V_{\text{out+}}$, but a differential input is also possible [6]. The configuration is shown in Figure 13.

Figure 13 Fully Differential Complementary $-G_m$ VCO

The voltage control tuning scheme is described with the use of a figure.

Figure 14 Varactor Sensitivity curves for the differential input VCO

As V_{ctrl+} increases from the common mode centre, the capacitance of the top varactors increases. V_{ctrl-} would decrease from the common mode centre and the capacitance of the bottom varactors would also increase.

As V_{ctrl+} decreases from the common mode centre, the capacitance of the top varactors decreases. V_{ctrl-} would increase from the common mode centre and the capacitance of the bottom varactors would also decrease. These two operations reinforce the differential input technique since the varactors should all increase or decrease when a change in frequency is needed.

However, if there is unwanted common mode noise from the charge pump, both V_{ctrl+} and V_{ctrl-} would increase or decrease together. The above varactor configuration would act to negate the change in capacitance (i.e. the bottom varactors would increase and the top varactors would decrease or vice versa).

Flicker noise has been proven to be greatly reduced using this differential input design [6]. This is because inductors are shorts at low frequency, so low frequency flicker noise acts like common-mode noise and appears equally on both positive and negative output terminals. The varactors are modulated since they are connected to the output terminals. The capacitance is not only dependent on the voltage control, but is more accurately de-

defined as the voltage difference across the varactor. The top and bottom pairs of varactors have a capacitance defined by

$$\text{Top Pair of Varactors} \quad C_{top} = \frac{C_0}{2} + \frac{k_{v_{top}}}{2} (V_{ctrl^+} - V_{ncm}) \quad (12)$$

$$\text{Bottom Pair of Varactors} \quad C_{bot} = \frac{C_0}{2} + \frac{k_{v_{bot}}}{2} (V_{ctrl^-} - V_{ncm}) \quad (13)$$

where C_0 is the zero bias capacitance, k_v is the varactor sensitivity and V_{ncm} is the common-mode noise voltage at the output terminal. Since the total capacitance is $C = C_{top} + C_{bot}$ and $k_{v_{top}} = -k_{v_{bot}}$ if the varactors are perfectly symmetrical, then

$$C = C_0 + k_v V_c \quad (14)$$

where $V_c = V_{ctrl^+} - V_{ctrl^-}$. Therefore, from (14) the common-mode noise voltage is rejected.

Unfortunately, there is a problem with the varactor configuration in Figure 13. The problem is that there is a depletion capacitance (parasitic diode) from the n-well to the substrate as shown in Figure 15.

Figure 15 AMOS Varactor Cross section Showing Parasitic Diode

This depletion capacitance is a reverse PN junction that behaves like a low Q (quality factor) voltage dependent varactor. A lower Q from the varactor results in worse phase noise. Figure 16 shows the impact on the schematic.

Figure 16 Varactor Configuration Showing Parasitic Diodes

From the above figure, the bottom varactors have two parasitic diodes at the centre. These diodes do not pose a problem because Vctrl- is an AC ground, which shorts out the two parasitic diodes at the centre.

The top varactors, however, are a different situation. Each varactor has a parasitic diode connected to the AC signal line. Therefore, the outer diodes are not shorted out and therefore lower the overall Q of the resonator.

This problem can be avoided if a silicon-on-insulator (SOI) CMOS process is used, instead of a bulk CMOS process. This is because the substrate capacitance of SOI is the buried oxide capacitance underneath the active area. This capacitance is a fixed high Q capacitor, instead of a low Q varactor.

In [6], a $-G_m$ VCO was built in SOI CMOS. For this differential tuning line LC VCO, all low frequency noise such as flicker noise was shown to be considered common mode noise. Differentially tuned varactors were used to suppress flicker noise from being up-converted to the carrier frequency.

Since the oscillators are designed in a bulk CMOS process and having the problem with the varactor configuration in Figure 13, there is an alternative varactor configuration as shown in Figure 17. In [7], the configuration uses PN-junction varactors instead of AMOS varactors, but the concept is similar. This varactor configuration uses fixed capacitors in series with the varactors and therefore isolating the DC node voltages of both terminals of each of the four varactors. Isolation of the nodes is necessary to be able to change the voltages of the terminals without affecting the outer AC signal lines. The VCO in Figure 17 is the main VCO proposed in this thesis.

Figure 17 Modified Fully Differential Complementary $-G_m$ VCO

From Figure 17, both top and bottom varactors have the parasitic diodes at the centre. Both V_{ctrl+} and V_{bias2} are considered AC grounds, hence all four parasitic diodes are shorted out. The bias resistors are necessary to prevent AC grounds.

The disadvantage of this VCO is that it requires more real estate (fixed capacitors and resistors) and more signal lines (bias lines). The mechanism to reduce $1/f$ noise is different from that of Figure 13 and was not explained in [7]. The fixed capacitors and bias resistors act as high-pass filters, so $1/f$ noise is attenuated at the varactor terminals. This technique could be done on a single-ended design, but a differential tuning line still has the advantage of rejecting common-mode signals from the tuning line. Other fully differential and low-voltage VCOs exist in [8] and [9]. In [8], not all of the parasitic diodes are shorted out, and therefore there will be a reduced Q . In [9], MOS varactors are used in-

stead of AMOS varactors. In IBM CMOSP13, MOS varactors have a horrible Q compared to AMOS varactors at high frequency.

For each of the $-G_m$ VCO configurations discussed so far (Figure 9, Figure 11, Figure 12, Figure 13 and Figure 17), the current sources could have been placed next to the rail, next to ground or the current source could have been omitted. This provides a large number of variations of VCOs. However, in any topology or variation used, sources of noise need to be considered since ultimately the phase noise is the parameter of interest.

2.4.8 Noise Sources

All sources of noise degrade the phase noise of an oscillator. However, there are two specific types of noise in any CMOS design. They are thermal noise and flicker noise. These sources of noise are random in nature due to electron movement and can get translated into phase noise.

1. Thermal noise in resistors is due to random electron motion generated by thermal agitation. The noise voltage function is given by (15).

$$V_n^2(f) = 4kTR\Delta f \quad (15)$$

where $kT = 4E-25$ Joules, R = resistor value and Δf is the noise bandwidth.

Thermal noise also exists in transistors called channel or drain noise. The noise current is given by

$$I_{nd}^2 = 4kT\left(\frac{2}{3}\right)\sqrt{2\mu C_{ox} \frac{W}{L} I_{DS}} \quad (16)$$

All thermal noise is flat across the frequency spectrum and is thus called white noise.

2. Flicker noise (1/f noise) is caused by the random trapping of charge such as the filling and emptying of traps at the oxide-silicon surface of a transistor. The input noise voltage at the gate of a MOSFET is given by

$$V_{ng}^2(f) = \frac{K}{WLC_{ox}f^\alpha} \quad (17)$$

K is a process dependent constant and α is close to 1, but not exactly 1. From (17), it is obvious that flicker noise is inversely proportional to frequency. It is also obvious that larger transistors exhibit less flicker noise. This is because their larger gate capacitance smoothes the fluctuations in channel charge [10]. If (17) is output referred, an output noise current can be written similarly to what was written in (16).

$$I_{ng}^2(f) = \frac{2K\mu}{L^2} I_{DS} f^\alpha \quad (18)$$

2.4.9 Phase Noise

The mechanisms that relate noise to phase noise will be examined. In the frequency domain, phase noise is responsible for the skirt as shown in Figure 3. This skirt is present because the perfect tone is sliding back and forth very quickly and randomly.

In the time domain, phase noise is referred to as jitter and is responsible for the amount of deviation of the zero crossings of a sine wave from the ideal position. The oscillation output, V_{out} , is mathematically written as

$$V_{out} = A \cos[\omega_o t + \phi_n(t)] \quad (19)$$

A is the amplitude, ω_o is the fundamental frequency and $\phi_n(t)$ is the amount of phase deviation. Amplitude noise is not included in (19).

The main type of phase noise mechanism is based on Leeson's formula. This type of phase noise is linear (additive). The formula associates all the losses in the VCO to a parallel resistance. The Q or quality factor is a parameter that quantifies the loss. A higher Q means less loss and the lower the phase noise skirts. Noise generated by the parallel resistance is shaped by the bandpass shape of the LC tank and is centered around the tone giving the "skirt" [11]. Leeson's formula is shown below in (20).

$$PN = \mathcal{L}(\Delta\omega) = \left[\frac{\omega_o}{(2Q\Delta\omega)} \right]^2 \left(\frac{kT}{2P_s} \right) \quad (20)$$

P_s is the signal power of the carrier, $\Delta\omega$ is the offset frequency and ω_o is the carrier frequency. This formula gives a phase noise estimate at a particular offset frequency. The formula only includes phase noise as opposed to amplitude noise as well so an extra factor of $\frac{1}{2}$ is present to account for half the noise. Usually amplitude noise is of less interest due to amplitude limiting.

Another type of mechanism is frequency modulation (FM). Frequency modulated phase noise is based on non-linearities. Any low frequency noise applied to the varactors will get modulated up to the carrier frequency. The effect is similar to narrowband frequency modulation. Any noise on the voltage control line is directly connected to the varactors. The varactors are voltage dependent and any change in voltage will modulate the frequency. This source of noise can come from the charge pump, the control line, the switching transistors of the VCO and the bias current source transistors. The sources of noise could be flicker noise, thermal noise and power supply noise. Equation (21) models this type of phase noise [3].

$$\mathcal{L}_{\text{fm}}(\Delta\omega) = \left(\frac{V_m K_{\text{VCO}}}{2\Delta\omega} \right)^2 \quad (21)$$

V_m is the FM noise voltage and K_{VCO} is the VCO tuning sensitivity.

A last type of mechanism is amplitude modulation (AM). AM phase noise is the least important factor of noise discussed so far and is therefore usually ignored. For this mechanism, the $-G_m$ VCO of Figure 17 is acting like a commutating mixer [12]. The switching transistors of this VCO act as the switching transistors of a mixer. When the LO of the mixer is small (i.e. the output amplitude of the VCO is small), the mixer is an analog multiplier. When the LO of the mixer is large (i.e. the output amplitude of the VCO is large), the mixer is a cascode amplifier. Flicker noise from the switching transistors and current source transistor can get multiplied up to the VCO carrier. Also, thermal noise around the harmonics of the output amplitude can mix down to the carrier. Lastly, thermal noise at two times the carrier frequency exists at the sources of the PMOS transistors and will mix down to the carrier. This noise exists because the tail current is pulled up each time one of the differential NMOS transistors turns on [13]. There is also noise at two times the carrier frequency between the two inductors, but inductors are open circuited at high frequency so there is no effect.

Now that all the types of phase noise mechanisms are presented, a typical phase noise curve is shown in Figure 18.

Figure 18 Typical Phase Noise Plot vs. Offset Frequency

From the figure, the flicker noise or $1/f$ noise dominates at low frequency offsets and rolls off at -30dB/decade . After a certain frequency offset (the $1/f$ corner), the VCO phase noise dominates and rolls off at -20dB/decade . The VCO phase noise is predicted by Leeson's Equation. Eventually the thermal noise floor is reached. Note that flicker noise is actually -10dB/decade but adds with Leeson's Equation to make it -30dB/decade at low frequency offsets.

Since the main VCO proposed in this thesis has a differential input, a differential output charge pump is necessary to make full use of the differential VCO. The charge pump presented in the next section is brief since this device is not the main focus of this thesis and is only an accessory to the VCO.

2.5 Charge Pumps

A charge pump is an analog device that places or removes charge onto a loop filter capacitor so that the VCO can be frequency tuned. Recall from the previous section that a DC voltage sets the frequency of oscillation of the VCO. The charge on the loop filter capacitor remains until a correction is needed to change the frequency of oscillation.

Charge may leak off the loop filter capacitor, but the negative feedback of the loop will provoke a correction.

A simplified charge pump is shown below in Figure 19.

Figure 19 Simplified Charge Pump

The loop filter is a capacitor, $C1$, which mimics an op-amp integrator with infinite DC gain. A resistor is necessary in series to allow for stability. The capacitor, $C2$, cleans up any reference feedthrough that could frequency modulate the VCO.

The charge pump is controlled by two signals from the phase frequency detector, pump up or pump down. The pump up signal is sent when the VCO is lagging and needs to be sped up. Charge is placed on the filter. The pump down signal is sent when the VCO is leading and needs to be slowed down. Charge is removed from the filter.

There are two main issues when dealing with charge pumps: the voltage headroom and the output impedance.

2.5.1 Voltage Headroom

Ideally, we would like to maximize the control line voltage range to the VCO. This would allow for a broader tuning range. The current source transistors can be designed to take as little headroom as possible. This is done by minimizing the saturation voltage in MOSFETs making up the charge pump. Equation (22) shows the saturation voltage.

$$V_{DS,Sat} = V_{GS} - V_t = \sqrt{\frac{2i_D}{\mu_n C_{ox}} \left(\frac{L}{W} \right)} \quad (22)$$

From (22), the saturation voltage can be decreased by reducing the current, decreasing the length of the transistors and making the width large. If a broad tuning range is necessary, then capacitors could be switched in and out of the VCO. This technique is known as bank switching and allows for a wide tuning range while maintaining a low K_{VCO} .

2.5.2 Output Impedance

Another issue with charge pumps is the output impedance of the current sources. Ideally, we would like the output impedance to be very large and the current to be constant at every voltage on the tuning line. If the current is not constant, then a mismatch between the UP and DOWN currents will occur, which in turn causes feedthrough. The output impedance of the current sources is given by

$$r_{DS} = \frac{1}{\lambda I_{DS}} = \frac{2}{\lambda \mu_n C_{ox} (V_{GS} - V_t)^2} \left(\frac{L}{W} \right) \quad (23)$$

To increase the output impedance, the current needs to be small which correlates with the saturation voltage. The length needs to be large and the width needs to be small, which are both at odds with the saturation voltage. This compromise is shown in Figure 20.

Figure 20 Current Source Current vs. Output Voltage Showing Compromise Between V_{sat} and r_{DS}

If a high output impedance is achieved, then a high saturation voltage reduces the tunable range. If a low saturation voltage is designed for, then a low output impedance is achieved. Ideally, the saturation voltage should be low to maximize the tunable range and the output impedance should be high to get a more constant current throughout the range. Making the charge pump current small would achieve both goals the best.

2.5.3 Differential Charge Pumps

Fully differential charge pumps also exist. The advantage of using fully differential designs is the rejection of common mode noise and the rejection of noise from the rails. An example of a fully differential charge pump is shown below in Figure 21 [14]. The PMOS transistors have circles around the transistors to clearly differentiate them from the NMOS transistors due to the large number of transistors present.

Figure 21 Fully Differential Charge Pump for use with the VCO

The above CMOS charge pump requires rail-to-rail input signals from the PFD. This circuit has three states as predefined by the phase-frequency detector.

When neither an UP or DOWN pulse is present, then M5 and M8 are on, but M6 and M7 are off. Current from M12 and M13 goes straight to M2 and M3. No current goes to the loop filter output (lout and lout_bar). This is the “locked” state of the PLL. The circuit requires static current flowing even when in the locked state, so it is considered power intensive and potentially noisy due to static current. This noise, if designed properly, could be offset by the noise rejection due to having differential outputs.

When an UP pulse is present only, then M6 and M8 are on, but M5 and M7 are off. Current from M12 and M13 goes entirely down the right branch, but M3 can only sink half of this current while the other half is sunk to the loop filter. M2 is also still expecting to sink current, but it is not being supplied with current from the rails, so it must take current

from the loop filter. This action describes the differential nature of the loop filter. If a DOWN pulse is present, instead of an UP pulse, something similar but opposite happens. The differential loop filter is shown below in Figure 22.

Figure 22 Differential Loop Filter

Another issue with the differential charge pump shown in Figure 21 is the use of common mode feedback (CMFB). CMFB is needed because there is nothing setting the common mode voltage at the output of the charge pump. The two resistors in Figure 21 monitor the average voltage between the two outputs. The resistors are large to prevent the loss of charge from the loop filter capacitor. The average voltage is then compared to V_{ref} . If it is below V_{ref} , then more current is pulled from M14. If it is above V_{ref} , then less current is pulled. The current from M14 is mirrored to the current sources M12 and M13, which supply the current sources for the charge pump.

Other fully differential and low voltage charge pumps exist in [15] - [17], but all require op-amps in the designs. Due to the amount of chip space and pins necessary, these designs were not chosen.

2.5.4 Noise Sources

In general, there are two main sources of noise for the charge pump. As discussed for the VCO in Section 2.4, they are flicker noise from the MOS transistors and thermal noise from the transistors or resistors. Charge pump noise is characterized as output noise cur-

rent and is measured in $\text{pA}/\sqrt{\text{Hz}}$. The charge pump output noise current is a function of how often and how wide current pulses are. For low noise operation, minimizing the amount of time the current sources are on would be the goal to achieve. At low frequencies, the flicker noise becomes more dominant than thermal noise.

The output noise current is divided by the phase frequency detector sensitivity, K_{phase} , to arrive at the input referred noise. The overall phase noise due to the charge pump and VCO can be found by output referring the respective noise with the use of (5) and (6) and then adding the noises in power. This technique was explained in Section 2.3.

2.6 Conclusions

This chapter started with the background of PLLs, followed by the background of VCOs and charge pumps. Noise sources in both the VCO and charge pump were examined and how these noise sources affect phase noise were presented. VCO designs were introduced with successive designs having advantages over the previous one, leading up to a VCO with a differential tuning voltage. A differential charge pump was also examined. Making the entire PLL differential, including the VCO and charge pump, is desirable because it becomes less prone to common-mode noise. The VCOs are designed and compared to each other in the following chapters. The single charge pump is also designed and discussed.

Chapter 3 Design and Layout

In this chapter, VCO and charge pump designs will be presented, based on some of the circuits discussed in the previous chapter. Both schematic and layout designs are examined and discussed.

3.1 Technology Overview

The technology used in the designs was IBM's 0.13-micron CMOS. This technology was supplied by MOSIS by way of the Canadian Microelectronics Corporation (CMC). It has eight layers of metal (3 thin, 2 thick and 3 thick RF top metals suitable for high-Q inductors), one layer of polysilicon, a 1.2 V core and a transit frequency of 120 GHz. It is possible to use transistors up to 3.3 V, but with non-minimum gate lengths. The threshold voltages for the NMOS and PMOS transistors are 0.333 V and -0.3 V, respectively. The transistor model is the BSIM3v3.2.

3.2 VCO Design

In total, five different $-G_m$ complementary VCOs were designed to operate at 20 GHz, but only two were fabricated. The other three have yet to be returned from the supplier at the time of this thesis. 20 GHz was chosen as the frequency of operation because at this frequency, the performance limits of the models (passive and active components) are being reached. The five descriptions of each VCO are below.

1. First Chip: $-G_m$ complementary VCO with no current source at 20 GHz.
 2. First Chip: $-G_m$ complementary VCO with no current source at 30 GHz. The inductors and varactors are made smaller. This VCO is a design to further push the performance limits of the models.
 3. Second Chip: $-G_m$ complementary VCO with no current source at 20 GHz. This design has improved layout over the first chip. It includes interleaving of transistors, better placement and layout of the inductors and varactors, increased contacts
-

between metals, increased substrate contacts across the design and is latchup-minded.

4. Second Chip: Fully differential $-G_m$ complementary VCO with no current source at 20 GHz.
5. Second Chip: Fully differential $-G_m$ complementary VCO with PMOS current source at 20 GHz.

This section goes through the design cycle of a typical VCO, including both the schematic design and the layout design.

3.2.1 Topology and Variation

Negative G_m VCOs were selected as the choice of VCOs due to their simple designs, which led to more designer control, and their minimal startup current [3]. The Colpitts and Hartley counterparts require impedance transformation for the loading of the transistors to the tank circuit [18].

The majority of the $-G_m$ VCOs were not designed with current sources. With a 1.2 V core, it is possible to have three transistors (including current source) stacked from top to bottom, but with reduced output voltage swing. At 20 GHz, it is necessary to have high output voltage swing to be able to drive a buffer. There is bound to be swing reduction due to the high operating frequency and therefore the parasitics are playing a big part. For the above reason, only two transistors are ever stacked with a 1.2 V supply. The gate oxide can handle up to 1.5 V for extra headroom, but at the cost of reliability. A single VCO was designed which included a PMOS current source with a supply voltage of 1.5 V. Inverters were used as buffers to help drive the output load of 50 Ω for all VCO designs.

All five VCOs were designed to have the same centre frequency (20GHz), same tuning characteristics, same biasing and same loading conditions.

3.2.2 Inductors

Fortunately, IBM has inductor models, which greatly aids the design of VCOs. Without models, a simulation tool like ASITIC would need to be used. This tool helps model the inductor by allowing the user to specify the different layers (metals, vias, substrate, nitride, oxide), the different parameters (resistivity, permittivity, thickness) and the distances between materials of the process being used. Given the operating frequency and inductance value, the tool can auto-generate the dimensions of the inductor that gives the best quality factor. An EM simulator like Momentum can also be used.

Since the IBM models include inductors, all that is needed is to specify the dimensions and the built-in models will auto-generate the inductance value and the peak quality factor frequency, Q_{peak} , for that inductance value, L . Then, the chosen model can be simulated and swept across frequency to determine Q and L across frequency. The models separate the technology processing issues from the circuit design issues. One very important advantage of having inductor models is that schematic and post-layout simulations are now possible. Without inductor models, there is less confidence in the designs. The IBM models greatly save design time and perhaps it will be commonplace sooner or later to have models for inductors from almost any foundry.

Two inductors are used for all VCO resonator designs. The IBM kit has three different types of inductors, but it lacks a completely differential inductor. A differential inductor saves chip area (subsidized cost of \$800/mm²) and it has been shown to have a higher Q at higher frequencies [3]. The differential inductor has fewer lossy paths to ground than two inductors in series. Losses in the inductor can be attributed to metal resistive losses and substrate losses due to eddy currents. The inductor with the overall highest Q at the required operating frequency of 20 GHz was chosen of the three. The highest Q gives the best phase noise.

Choosing the inductor size is also very important. If the output voltage amplitude is not maximized, then the VCO is considered current limited. Increasing the inductor size will

improve phase noise because the value of R_p increases, where R_p is the equivalent parallel resistance of the resonator. If the output voltage amplitude is maximized, then the VCO is considered voltage limited. Increasing the inductor size will then degrade the phase noise [3]. Voltage limited does not necessarily mean rail-limited.

Phase noise can be improved or degraded based on the value of R_p . From Leeson's equation in (20), $PN \propto 1/P_s$. In the voltage limited mode,

$$P_s = \frac{V_{\text{tank}}^2}{R_p} \quad \text{so} \quad P_s \propto \frac{1}{R_p} \quad (24)$$

From (11) $V_{\text{tank}} \propto R_p$ so in the current limited mode,

$$P_s = \frac{V_{\text{tank}}^2}{R_p} \propto \frac{R_p^2}{R_p} \quad \text{so} \quad P_s \propto R_p \quad (25)$$

Therefore, referring back to phase noise, $PN \propto R_p$, in the voltage limited mode or $PN \propto 1/R_p$, in the current limited mode. So given an inductor size and a capacitor size with an equivalent parallel resistance, R_p , there is an optimum value of R_p that gives the best phase noise. This value of R_p is where the voltage-limited regime meets the current limited regime. Phase noise can be improved even more by increasing the current.

The Q in (20) is considered the Q of the resonator. This Q includes the losses in the inductor, quantified by Q_L , and the losses in the capacitor, quantified by Q_C to be shown in the next section. It does not include transistor losses and other losses. The inductor quality factor, Q_L , is given by

$$Q_L = \frac{\omega L}{R_s} \quad \text{or} \quad Q_L = \frac{R_p}{\omega L} \quad (26)$$

From (26), less series resistive loss, R_s , from the inductor can lead to a higher quality factor. R_p is the equivalent parallel loss.

The IBM inductor chosen uses the top metal (Metal 8) for the spirals and the second top metal (Metal 7) for the underpass. The two top metals have the least amount of resistance (less loss), which is good for making inductors because of the higher Q . The spirals are made in an octagonal shape. The inductor also has a moat (trench) underneath that reduces parasitic capacitances to the substrate. Parasitic capacitances reduce the resonance frequency of the inductor and they also allow unwanted AC current to flow into the substrate. Finally, the inductor has a ground connection (substrate contacts) that is at least 50 μm away from the edge of the inductor. The ground connection terminates the magnetic field lines. Two series inductors meant to be used for 20 GHz and optimized for the highest possible Q at that frequency is shown below in Figure 23.

Figure 23 Layout of the Series Inductors Showing Detail

The dimensions (per inductor) are shown in Table 2.

Table 2 Inductor Dimensions

Parameter	Value
Outer Dimension	110 μm
Metal Width	5 μm
# of Turns	1
Underpass Width	15 μm
Space	5 μm

The chosen inductor was simulated and swept across frequency. The quality factor and inductance versus frequency are shown in Figure 24. This inductor was chosen for most designs.

Figure 24 Q and Inductance vs. Frequency for a Single Inductor

From Figure 24, the inductance is 220 pH and the Q is 20 at 20 GHz. It is safe to operate at some distance away from the peak Q frequency. If the designer operates too close to the peak Q frequency, any unaccounted for capacitance could push the operating frequency past the peak Q frequency and into the resonance frequency zone. In this zone, the inductor could behave like a capacitor.

3.2.3 Varactors

The IBM varactor model used in this process is an accumulation MOS varactor as described in Section 2.4.3. The varactor has a much higher quality factor, Q_C , than the inductor quality factor, Q_L . The definition of Q_C is shown below.

$$Q_C = \frac{1}{\omega C R_s} \quad \text{or} \quad Q_C = \omega C R_p \quad (27)$$

From (27), a smaller series resistance, R_s , can lead to a higher quality factor. The series resistance can be attributed to metal resistive losses. R_p is the equivalent parallel loss.

Varactors were placed as described in Section 2.4.7. They were placed so that the parasitic diodes would always be AC grounded, whether they were singled-ended or differential input varactors, depending on which variation of the VCO.

The model requires dimensions to be entered. The chosen varactor was simulated and swept across frequency. The quality factor and capacitance versus frequency are shown in Figure 25. If the capacitance is not the correct value to give the correct operating frequency, using (7), then another size is to be chosen. The operating frequency can be off due to parasitic capacitance. From Figure 25, the capacitance is 163 fF and the Q is 79 at 20 GHz. The control voltage, V_{ctrl} , is set to 0.6 V.

The typical dimensions (per varactor) are shown in Table 3.

Table 3 Varactor Dimensions

Parameter	Value
RX (active region) width	2 μm
PC (poly gate) length	240 nm
# of Gates	8
RX Repetition	8
Multiplicity	1

Figure 25 Q_c and Capacitance vs. Frequency for a Single Varactor

Choosing the varactor dimensions is not trivial. There is an optimum varactor dimensions that gives the best quality factor [19]. By keeping the varactor small, resistive losses are minimized. To achieve the required capacitance value, multiple varactors are placed side by side vertically and horizontally. This is done by increasing the number of gates and/or increasing the multiplicity of the cell.

3.2.4 Tuning Range

As the control voltage is tuned, the varactor capacitance changes and therefore the oscillation frequency changes. Figure 26 shows a typical plot of the capacitance, C , and quality factor, Q_c , versus the voltage control. The change in capacitance (parasitics need to be included) corresponds to a change in frequency from 19 GHz to 21 GHz, centered around 20 GHz.

Figure 26 Capacitance and Qc at 20 GHz vs. V_{ctrl}

3.2.5 Switching Transistors

At 20 GHz, both PMOS and NMOS transistors need to have minimum length gates or close to minimum length gates. This is because the speed of the technology is inversely proportional to the gate length squared in CMOS, $f \propto 1/L^2$. It was found by simulation that transistor lengths greater than $2 \cdot L_{min}$ would not operate at 20 GHz.

Another problem is parasitic capacitance becoming significant at 20 GHz. Having a large W/L ratio helps to increase the output voltage swing and possibly improving phase noise, but at the cost of parasitics affecting the operating frequency. The varactors could be re-sized, but up to a certain limit, the point where the varactors cannot get any smaller. Also, the more the oscillating frequency depends on the parasitics, the tuning range becomes smaller.

Having both a large W and a small L are at odds with any reduction in thermal or flicker noise. Thermal and flicker noise were covered in Section 2.4.8. The contribution of flicker noise from the switching transistors is small due to the switching action. Flicker noise is considered correlated noise and only exists in systems with memory. When the transistors are fully switched, all memory and therefore the flicker noise is removed [20].

The transistors were sized so that the DC voltage at the output was 0.6 V. For a 1.2 V rail, the midpoint voltage would be 0.6 V. Using the midpoint voltage maximizes the output voltage swing. A higher voltage swing, equates to a larger signal over the noise.

The transconductances (gms) of the NMOS and PMOS transistors were matched to match the rise and fall time of the output signal. By matching the rise and fall times, the signal levels of the harmonics of the output signal are reduced and therefore less noise can be mixed to the carrier frequency. Since the same current goes through the PMOS and the NMOS and since the output voltage DC midpoint is 0.6 V, the W/L ratio of the PMOS works out to be three times larger than the W/L ratio of the NMOS for matched gms.

Interleaving the transistors in layout is necessary for symmetrical designs. Symmetrical designs for all components (inductors, varactors, transistors, etc) are necessary for common-mode rejection, especially for designs without a current source.

The typical transistor sizes are shown below in Table 4.

Table 4 Switching Transistor Sizes

Parameter	NMOS Value	PMOS Value
Width	1 μm	3 μm
Length	120 nm	120 nm
# of Fingers	7	7
Multiplicity	1	1

3.2.6 Current Source Transistor (Biasing)

The current source transistor is known to upconvert flicker noise to the carrier. Because of this, the length of the biasing transistor is made larger than usual to minimize both thermal and flicker noise. From (23), having a large length also improves the output impedance. The width needs to be made large to minimize $V_{DS,Sat}$ as shown in Section 2.5.1. Having a small $V_{DS,Sat}$ allows the actual VCO core to have a larger output voltage swing.

In [21], it is shown that the dominant flicker noise is not from the biasing transistor but is actually from the switching transistors. Jerng and Sodini state that bias flicker noise is only amplified by improper sizing of the switching transistors and is therefore not the main culprit of flicker noise. By increasing the gate overdrive ($V_{GS} - V_T$) of the switching transistors, the linear range of the MOS differential pair is increased and therefore less upconversion gets to the carrier (less distortion for a given signal swing). The gate overdrive is increased by assuming the same bias current, but decreasing the width of the switching transistors.

In this thesis, only one VCO has a current source. The above technique was not applied since it was discovered after the design. The current source chosen was a PMOS current source since PMOS devices have less flicker noise than their NMOS counterparts. A PMOS current source also allows the midpoint voltage of the switching transistors to still be 0.6 V, because the midpoint voltage is referenced from ground and not from the sup-

ply. The current source mirror ratio was 1:1. A smaller ratio results in less noise being multiplied. The transistor sizes for both the mirror and the source are shown in Table 5.

Table 5 Bias Transistor Sizes

Parameter	PMOS Value
Width	8 μm
Length	2 μm
# of Fingers	20
Multiplicity	4
Current	1 mA

From Table 5, a current of 1 mA was selected based on voltage swing and power dissipation. For the VCOs without a current source, the current is determined by the size of the switching transistors, while still getting a desirable output voltage swing and keeping power dissipation in mind.

3.2.7 Buffer

The simplest buffer is an inverter as shown in Figure 27.

Figure 27 Inverter Buffer

The inverter does not require a DC level shift that a source follower would need. Looking at Figure 12, the complementary $-G_m$ VCO is just two back to back inverters, so using an inverter as a buffer would be very appropriate. The midpoint of the $-G_m$ VCO is at the exact DC input level for the inverter, so no biasing scheme is necessary since it is provided by the VCO. The ideal DC input level for the inverter is the midpoint because it allows maximum voltage swing, which is the same reason as for the switching transistors of the VCO.

There are two reasons for using a buffer. The first is that it provides more output AC current to drive the $50\ \Omega$ load. The second is that it isolates the load from the resonator. At 20 GHz, the buffer is used more for the isolation purpose. This is because there is attenuation from the input of the buffer to the loaded output, so output current is actually reduced and there is no point to have more than one inverter. The poles due to the parasitic capacitances cause too much attenuation at 20 GHz. The sizes of the buffer transistors are similar and should be no greater than the sizes of the switching transistors. Making the size of the buffer transistors too small would result in almost no signal at the output.

The $50\ \Omega$ load represents the probing pin. A DC blocking capacitor is connected at the output of the buffer before touching the probe. The same buffer is used for the negative output of the VCO.

3.2.8 Transmission Lines

Long metal lines greater than $100\ \mu\text{m}$ from the circuit to the bondpads and from the inductors to the switching transistors were modeled with transmission lines from the IBM CMOSP13 kit. This was done for the second chip. It was only done to the first chip after the chips came back from the foundry. The transmission lines have the same layers as the inductors. At 20 GHz, the natural wavelength is 1.5 cm, so it is important to model the high frequency paths to the bondpads.

3.2.9 Sample Phase Noise Calculation

By knowing the information about the inductors and varactors, given in this chapter, a phase noise estimate can be plotted by making a few assumptions. Leeson's phase noise equation can be used in (20), but with a modification that includes flicker noise. This is given as

$$\mathfrak{f}(\Delta\omega) = \left(\frac{\omega_o}{(2Q\Delta\omega)} \right)^2 \left(\frac{kT}{2Ps} \right) \left(1 + \frac{\omega_c}{\Delta\omega} \right) \quad (28)$$

The ω_c term is the estimated flicker noise corner of $2\pi \cdot 500$ kHz.

The Q in (28) is the resonator quality factor. To calculate the resonator Q, (29) can be used below.

$$Q = R_p \sqrt{\frac{C_{tot}}{L}} \quad (29)$$

The R_p here is the equivalent parallel resistance of the resonator (includes both the inductor and capacitor parallel resistance). The C_{tot} is the required capacitance (includes both varactor and parasitic capacitance) to oscillate at 20 GHz.

For the inductor at 20 GHz, $L = 220$ pH and $Q_L = 20$. Therefore, from (26) the equivalent parallel resistance for the inductor only is $R_p = \omega L Q_L = 553 \Omega$.

For the capacitor at 20 GHz, $C = 163$ fF and $Q_C = 79$. Therefore, from (27) the equivalent parallel resistance for the capacitor only is $R_p = Q_C / (\omega C) = 3857 \Omega$.

The total R_p of the resonator is just the two R_p s in parallel, which is 484Ω .

$C_{tot} = 288$ fF to oscillate at 20 GHz, so from (29) the Q of the resonator is 35.

The signal power of the carrier, P_s , is given by (30).

$$P_s = \frac{(V_{rms})^2}{R_p} = \frac{V_{peak}^2}{2R_p} \quad (30)$$

The singled-ended output of the oscillator can be estimated at 0.6 V_{peak} (1.2 V_{pp}) to be rail limited. So $P_s = 372 \mu W$.

Now that all of the unknowns are defined, (28) can be plotted against offset frequency as it is swept from 1 kHz to 100 MHz as shown in Figure 28.

Figure 28 Sample Plot of Phase Noise vs. Offset Frequency

From Figure 28, it can be seen that the phase noise rolls off at -30 dB/decade until about 500 kHz, where the phase noise starts to roll off at -20 dB/decade . A thermal noise floor was included so the phase noise would flatten out at -140 dBc/Hz .

3.3 Charge Pump Design

The charge pump of Figure 21 was designed for use with the differential VCOs. It consists of a charge pump current of 200 μA for the UP and DOWN currents. It has been simulated with reasonably matched currents at an operating frequency of 200 MHz. The charge pump was part of the second chip, so no experimental results are yet available. The following sections review some important design issues for the charge pump.

3.3.1 Current Source

The current sources in the charge pump were designed with large lengths and large widths. The large lengths minimize thermal and flicker noise. A large width helps to decrease $V_{\text{DS,Sat}}$ so that more headroom can be used for the charge pump. A small current for the charge pump current ensures high output impedance.

3.3.2 Switching Transistors

The switching transistors also have large lengths to minimize noise. Large widths are also used to keep the PMOS current sources saturated. If the widths are made too large, however, the large parasitic input capacitance from the transistors could load the input signal and prevent the transistors from switching completely. The switching transistors were interleaved in the layout to ensure the best possible match in UP and DOWN currents.

3.3.3 Common Mode Feedback (CMFB)

Attention should be made to the CMFB during the design of the charge pump. The CMFB is a negative feedback circuit, just as the entire PLL is also a negative feedback system. If the poles of the circuit are not accounted for, the loop can go unstable. For example: if the CMFB is correcting slower than the loop, then the loop can go unstable. This is because the loop should not “see” the change from the CMFB. This was tested by

performing a full loop simulation with a large loop bandwidth and ensuring the loop still locked. A large loop bandwidth has a short settling time for the loop and, therefore, gives the worst case scenario to see if the CMFB is still correcting faster than the loop. The capacitor in parallel with M14 in Figure 21 is responsible for the additional pole to make the loop go potentially unstable. It is needed to filter out transistor noise, but could potentially filter out the common-mode feedback so care must be taken when sizing this capacitor.

3.4 Chip Layouts

The layout for the first chip sent for fabrication is shown below in Figure 29. Notice the amount of space (~25%) the bondpads take in relation to the entire chip size (600 μm by 1200 μm). The size of bondpads makes it very difficult to put many circuits on a chip.

Figure 29 First Chip Design

The layout for the second chip sent for fabrication is shown in Figure 30. It has dimensions of 925 μm by 2700 μm .

Figure 30 Second Chip Design

3.5 Simulations and Comparisons

This section focuses on the VCO and charge pump simulations, separately. All five VCOs are compared in a table format. The simulation results are discussed and analyzed. The charge pump is also simulated and analyzed.

3.5.1 VCO Simulations and Analysis

Table 6 below shows the parameters of all VCOs and the simulation results achieved for each parameter. The VCO descriptions were presented in 3.2. For comparison purposes, only schematic simulations results without loading conditions are presented.

Table 6 VCO Parameters and Results

VCO #	VCO1	VCO2	VCO3	VCO4	VCO5
VDD (V)	1.2	1.2	1.2	1.2	1.5
Centre Frequency (GHz)	21.62	34.85	21.62	21.73	21.68
PMOS Current Source	No	No	No	No	Yes
Differential Input	No	No	No	Yes	Yes
Peak to Peak Diff. Output Voltage (V)	2.438	2.31	2.438	1.556	1.611
Tuning Range (GHz) & Voltage (V)	20.55 - 22.96	33.84 - 36.04	20.55 - 22.96	21.08 - 22.9	21 - 22.83
	0 - 1.2	0 - 1.2	0 - 1.2	0 - 1.2	0 - 1.2
Phase Noise (dBc/Hz) @ 0.6 V	10 kHz	-53	-43	-53	-63
	100 kHz	-82	-72	-82	-85
	1 MHz	-107	-98	-107	-105
DC Current (mA)	1.503	0.957	1.503	0.717	0.962

From Table 6, VCO1 and VCO3 have the same results. Schematic simulations will not show any difference if the layout has been changed. Recall that VCO3 has improved layout over VCO1.

A difference can be seen between VCO3 and VCO4. VCO3 has a single-ended input as shown in Figure 12, whereas VCO4 is the differential version as shown in Figure 17. VCO4 (and VCO5) has significantly lower inband phase noise than VCO3. A plot of phase noise versus offset frequency is shown below in Figure 31. VCO5 also has a differential input, but with a PMOS current source.

Figure 31 Phase Noise vs. Offset Frequency for VCO3 and VCO4

Figure 31 shows that from 1 kHz to 500 kHz, VCO4 has lower phase noise. After 500 kHz, VCO3 has lower phase noise. Having a differential input VCO clearly has advantages of reducing inband phase noise. The $1/f$ noise is suppressed by the highpass filters from being upconverted to the carrier frequency. The $1/f$ corner frequency for VCO4 is less than 10 kHz, whereas it is just below 1 MHz for VCO3.

The phase noise after 500 kHz, where thermal noise is more dominant than $1/f$ noise, is compromised in the differential design. The extra bias resistor noise and the extra parasitic resistor noise from the fixed capacitors dominate in this region. Phase noise after 500 kHz is usually less important than the inband phase noise because it can be filtered out by the loop filter in the PLL and it is also further away from the carrier.

One observation between VCO3 and VCO4 is that the peak to peak voltage amplitude of VCO4 is smaller than that of VCO3. The transistors of VCO4 are smaller than those of

VCO3, so less current would be used, which leads to a smaller amplitude. VCO4 has a differential input and therefore has more capacitance due to the increase in varactors and fixed capacitors. To oscillate at 20 GHz, the switching transistors need to be smaller so that parasitic capacitance plays less of a role in the oscillation frequency.

3.5.2 Charge Pump Simulations and Analysis

Table 7 below shows the parameters of the charge pump and the simulation results achieved for each parameter. Only the schematic simulation results are presented.

Table 7 Charge Pump Parameters and Results

Charge Pump Parameters		Value
VDD		1.5 V
Differential Input & Output		Yes
Maximum Frequency		200 MHz
Usable Tuning Range		0.3 V - 0.9V
Optimum Charge Pump Current & Percentage Variation		200 μ A +/- 15%
Output Noise Current (pA/ $\sqrt{\text{Hz}}$)	10 kHz	21.5 pA/ $\sqrt{\text{Hz}}$
	100 kHz	12.1 pA/ $\sqrt{\text{Hz}}$
	1 MHz	10.6 pA/ $\sqrt{\text{Hz}}$
DC Current		804 μ A

The output noise current is recorded when the charge pump is in the locked state. The locked state is important because the charge pump produces the least amount of noise in this state. The simulation is done by measuring the output noise voltage across a 1 Ω noiseless resistor. Therefore the output noise current can be extracted since $V = IR$. The plot of output noise current versus frequency offset is shown below in Figure 32.

Figure 32 Output Noise Current vs. Offset Frequency

Another design issue is the output resistance of the charge pump. As the charge pump output voltage gets closer to the rails, the UP and DOWN currents will become more and more mismatched causing increased feedthrough. This is because the transistor is going from saturation to triode.

The variation in the charge pump current was tested by sourcing current to the loop filter and sinking current from the loop filter, while sweeping the output voltage within the usable range (0.3 V to 0.9 V). Figure 33 shows the results.

Figure 33 Output Current vs. Tuning Voltage @ 200 MHz

From Figure 33, it can be seen that the charge pump current for both the UP and DOWN currents are close to $200\ \mu\text{A}$ when the output voltage is around $0.6\ \text{V}$. The charge pump current then deviates by 15% as the output voltage is veered away from $0.6\ \text{V}$. If an even more conservative match in the UP and DOWN currents is necessary, either the frequency can be lowered or the charge pump current reduced.

3.6 Conclusions

This chapter covered the schematic design, layout and simulations of the VCOs and the charge pump. Five VCOs and one charge pump were designed using the IBM CMOSP13 technology. The specifics of the designs were presented such as transistor sizing, passive characterization, feedback, etc. The chapter also compared the VCO simulations with respect to each other. It was shown that having a differential tuning line for the VCO

could greatly improve inband phase noise by about 10 dB at 10 kHz. This is because 1/f noise is being filtered by a high-pass filter before being upconverted. In simulation, the 1/f noise corner is moved from about 800 kHz for the single-ended control to about 8 kHz for the differential control. The negative aspects of the varactor structure are that it requires more components and signal lines. Also, out of band phase noise is slightly worse due to the parasitics of the extra components. Schematic simulations of the charge pump showed an optimum current of 200 μA $\pm$ 15% and a usable tuning voltage range of 0.3 V to 0.9 V. Post-layout simulations will be presented in the next chapter where they will be compared to laboratory measurements.

Chapter 4 Testing and Results

In this chapter, the testing procedure and the testing of loose dice will be discussed. The probing station in the lab at Carleton University was used. Since only the first chip was available for testing, only measurements from that chip are shown. While measurements could not be completed for the second test chip, test procedures will still be outlined.

Some bondpads are shared, but circuits are powered separately. The differential VCO and differential charge pump have the option of being tested separately or together. The VCOs are tested with 8-pin probes, but the charge pump requires a printed circuit board (PCB). For any off-chip input signals that are connected to the gates of transistors, electro-static discharge (ESD) protection circuitry are used. This is to avoid charge build up on the gate that could cause the oxide to break down and the transistor to be damaged.

4.1 First Chip Testing

The first chip consists of two $-G_m$ complementary LC VCOs, namely VCO1 and VCO2. The control voltage inputs to both VCOs are single-ended. The outputs of both VCOs are differential, but the 8-pin probing equipment can only measure a single-ended output. Phase noise is expected to be worse for a single-ended measurement since there are reflections back to the VCO core coming from the unused end. The VCOs are tested separately. The test setup is shown below in Figure 34 and the layout with pins labeled is shown in Figure 35.

Figure 34 Conceptual setup for testing a VCO

Figure 35 First Chip Showing Pin Names

VCO1 was set to a control voltage of 0.6 V and power supply voltage was set to 1.2 V, but the oscillator did not start up. The supply voltage was increased and it was found that 1.5 V is needed to produce an adequate signal that could be tuned. A supply voltage of greater than 1.5 V would destroy the gate oxide since the transistors have a breakdown voltage of 1.5 V for a 1.2 V transistor. VCO1 had an oscillation frequency of about 16.3 GHz. Figure 36 below shows the spectrum analyzer output for VCO1.

Figure 36 VCO1 Spectrum Analyzer Output

The exact same setup was used for VCO2 on the same loose die. VCO2 also needed a supply voltage of 1.5 V for an adequate signal that could be tuned. VCO2 had an oscillation frequency of about 22.8 GHz. Figure 37 below shows the spectrum analyzer output for VCO2 with a smaller span.

Figure 37 VCO2 Spectrum Analyzer Output

Both VCOs on the first chip were very sensitive to power supply changes. This observation is expected since the VCOs do not have a controlled current source. Another issue was the lighting of the room. Turning off the lights in the Faraday cage would shift the frequency by 5 MHz. At high frequency, the VCOs are very sensitive to photons.

The layout was analyzed to investigate the difference between the expected oscillation frequencies and the measured. One important factor in the inductor placement was observed. Inductors were connected to switching transistors through 100 μm metal lines and these should have been modeled by transmission lines. The transmission lines are a source of extra inductance that is unaccounted for. This is shown in Figure 38 below.

Figure 38 Metal Lines connecting the inductors to the switching transistors

Post-layout simulations were done with the metal lines modeled as transmission lines for both VCOs. A comparison of the post-layout simulation results including loading effects and parasitics versus the measured results is shown below in Table 8.

Table 8 Comparison Between Post-Layout Simulation Results and Measured Results

VCO #		VCO1 Post-Layout Simulation	VCO1 Measured	VCO2 Post-Layout Simulation	VCO2 Measured
VDD (V)		1.5	1.5	1.5	1.5
Centre Frequency (GHz)		16.27	16.3	22.67	22.96
PMOS Current Source		No	No	No	No
Differential Input		No	No	No	No
Peak to Peak Single-Ended Output Voltage (V)		0.473	0.141	0.440	0.090
Tuning Range (GHz) & Voltage (V)		15.76 - 17.05 0 - 1.2	15.7 - 17.3 0 - 1.2	22.36 - 23.14 0 - 1.2	22.73 - 23.75 0 - 1.2
Phase Noise (dBc/Hz) @ 0.6 V	10 kHz	-51	~	-41	~
	100 kHz	-80	-58	-70	-49
	1 MHz	-108	-80	-99	-70
DC Current (mA)		3.745	4	2.3	4

From Table 8, the frequency of oscillation of the post-layout simulation results agrees very well with the measured results. The single-ended output voltage and the phase noise, however, are quite different. The measured VCOs required 1.5 V, not 1.2 V, in order for them to oscillate. This means the VCOs were more lossy than initial simulations indicated, hence more current was required to sustain oscillations. The measured results show an increase in current consumption, which is directly related to the power supply increasing because of the lack of current sources. Note that the measured current consumption includes the current from the output buffers.

VCO1 and VCO2 did not have interleaved transistors, leading to mismatched transconductances. Gate connections were routed in polysilicon, which leads to paths of high resistance (Figure 39). Due to paths of high resistance, the output voltage swing would be reduced, as seen in the measured results, for a given current and therefore would have a smaller signal to noise ratio. Both higher resistance and lower output swing will result in higher phase noise for both VCOs. The above issues were fixed for the second chip.

Figure 39 Non-interleaved PMOS and NMOS transistors showing paths of high resistance

The improved layout in VCO3 from the second chip is shown below in Figure 40 to compare to Figure 39. Both PMOS and NMOS transistors are interleaved and gate connections are routed in metal.

Figure 40 Improved Layout with Interleaved PMOS and NMOS transistors

The measured tuning sensitivity, K_{VCO} , for both VCOs is plotted below in Figure 41.

Figure 41 Frequency vs. Tuning Voltage for VCO1 and VCO2

4.2 Second Chip Testing

The second chip consists of three $-G_m$ complementary LC VCOs. The outputs of all VCOs are measured single-endedly. The measurement results are not included, but post-layout simulation results are included in Table 9.

Table 9 Post-Layout Simulation Results including Transmission Line Models and Parasitics

VCO #		VCO3	VCO4	VCO5
VDD (V)		1.2	1.2	1.5
Centre Frequency (GHz)		17.02	16.99	16.87
PMOS Current Source		No	No	Yes
Differential Input		No	Yes	Yes
Peak to Peak Single-Ended Output Voltage (V)		0.140	0.115	0.134
Tuning Range (GHz) & Voltage (V)		16.31 - 17.92	16.58 - 17.67	16.48 - 17.55
		0 - 1.2	0 - 1.2	0 - 1.2
Phase Noise (dBc/Hz) @ 0.6 V	10 kHz	-48	-47	-51
	100 kHz	-78	-76	-79
	1 MHz	-105	-104	-105
DC Current (mA)		1.577	1.003	0.962

From Table 9, the VCOs on the second chip had similar transmission lines connecting the transistors to the inductors as the first chip. The metal lines were modeled as transmission lines, but lack of time prevented a redesign for 20 GHz since the first chip only arrived about the same time the second was taped out. Therefore, the oscillation frequencies are expected to be about 17 GHz as indicated by the post-layout simulations.

Another thing to note is that VCO4 and VCO5 do not have improved inband phase noise over VCO3 from the suppression of flicker noise as seen in the schematic simulations. There is one man factor. The VCOs are sensitive to the buffers. A well-designed buffer should separate any imbalances from the load or the buffer “seen” by the VCO. Also, a good buffer should not provide too much loss of voltage swing. At 20 GHz, the inverters provided a significant voltage loss from the input to the loaded output. A reduced signal to noise ratio can degrade the phase noise.

The charge pump is also on the second chip. To test the charge pump, a pulse generator will be used to apply square waves at different pulse widths. The average slope of the voltage transient on the capacitor depends on the width of the pulse. The difference in

average slope is proportional to the pulse width, thus allowing linearity of the charge pump to be determined. A longer pulse width translates to a steeper average slope over many pulses. The test setup is shown below in Figure 42 and the layout with pins labeled is shown in Figure 43.

Figure 42 Conceptual Charge Pump Test Setup

Figure 43 Second Chip Showing Pin Names

As shown in Figure 42, an oscilloscope measures the voltage on the capacitor. The bias circuitry is needed to predefine the differential voltage on the capacitor. The loose die is packaged in a 24-pin ceramic flat package provided by CMC. The package is then placed on a PCB. The large capacitor is on the PCB.

A schematic simulation of the capacitor charging with different input pulse widths is shown below in Figure 44. Since the frequency of operation is 200 MHz, the rising pulse edges will be 5 ns apart. By using the pulse width generator, three widths are selected: a) 1% of 5 ns, b) 5% of 5 ns and c) 25% of 5 ns.

Figure 44 Voltage vs. time for Varying Pulse Widths

From Figure 44, when the pulse width of b) is applied the output has a slope that is five times of that when the pulse width of a) is applied. Likewise, when the width of c) is applied, the output has a slope that is five times of that when the pulse width of b) is applied. Note that the voltage increases do not increase at the same time due to quantization error from Microsoft Excell.

From the above information, we can plot the linearity of the charge pump as shown below in Figure 45. The slope of Figure 45 is similar to K_{phase} . The above test will be done at various tuning voltages. The slopes should all be the same at all tuning voltages if linearity is preserved across the tuning range. Figure 45 has the tuning voltage set at 0.6 V.

Figure 45 Average $\Delta v/\Delta t$ vs. Phase with the Tuning Voltage at 0.6 V

If the graph of Figure 45 were not linear, then it would reflect the poor linearity of the charge pump. The graph can be converted to average output current by using (31).

$$\bar{I} = C \frac{\overline{\Delta V}}{\Delta t} \quad (31)$$

If the capacitor is assumed to charge linearly, then the average output current can be plotted against phase. The slope of this new curve is K_{phase} .

4.3 Conclusions

In this chapter, comparisons were made between the post-layout simulation results and the laboratory measurements of the first chip. After unaccounted inductance was included in post-layout simulations, the centre frequencies matched well with simulated numbers of 16.27 GHz and 22.67 GHz, while measured numbers were 16.3 GHz and 22.96 GHz for VCO1 and VCO2, respectively. Post-layout simulations were done for the

second chip as well and it showed that the oscillation frequencies of the VCOs are expected to be about 17 GHz. A novel way to test the linearity of the charge pump was explained at the end of the chapter. One final simulation to demonstrate the application of these components would be to include both the VCO and charge pump in a full PLL simulation to verify if the loop will lock. This is done in the next chapter.

Chapter 5 Full Loop PLL Simulations

This chapter focuses on the closed loop phase-locked loop simulations. Both VCO5 and the charge pump are combined in a loop to demonstrate operation. The other components of the loop are modeled using VHDL code.

5.1 Setup Parameters

A few parameters need to be calculated before the simulation can be done. Since the operating frequency of the VCO is 20 GHz and the operating frequency of the charge pump is 200 MHz, a divide ratio around $N = 100$ is needed.

The natural frequency, ω_n , is set to 500 kHz to filter out noise. The damping constant, η , is set to 0.707 for a fast response. The loop bandwidth is given by

$$\omega_{-3dB} = (1 + \eta\sqrt{2})\omega_n \quad (32)$$

Therefore from (32), $\omega_{-3dB} = 1$ MHz.

Given ω_n and η and the knowledge of (3) and (4), R and C of the filter in (2) can be derived explicitly. They are shown below in (33) and (34).

$$C = \frac{K}{\omega_n^2} \quad (33)$$

$$R = \frac{2\eta}{\sqrt{KC}} \quad (34)$$

The expression for $K = K_{vco}K_{phase}/N$.

An extra capacitor, C_2 , is usually placed in parallel with the loop filter to remove reference feedthrough. The value of C_2 is one tenth that of C .

The VCO tuning sensitivity, K_{vco} , is calculated as $(23 \text{ GHz} - 21 \text{ GHz})/(1.2 \text{ V}) = 1.67 \text{ GHz/V}$. The unknowns are provided from VCO5 in Table 6. Notice that the rail voltage for VCO5 is 1.5 V, but the tuning range is 1.2 V.

The phase detector sensitivity is $K_{phase} = I/(2\pi) = (200 \text{ } \mu\text{A})/(2\pi)$. The phase detector is assumed to be a three-state phase frequency detector with a linear region of $\pm 2\pi$. The current is the charge pump current of $200 \text{ } \mu\text{A}$.

Therefore, the value of $R = 1.33 \text{ k}\Omega$, $C = 338 \text{ pF}$ and $C_2 = 33.8 \text{ pF}$. These components are used in the diagram of the setup shown below in Figure 46.

Figure 46 Closed Loop PLL Setup

5.2 Simulation

The voltage on the tuning line, V_{ctrl} and V_{ctrl_bar} , is shown in Figure 47 when a $>300 \text{ MHz}$ frequency step is applied. The tuning line starts at 0.6 V (21.68 GHz) and ends at 0.78 V (21.98 GHz).

Figure 47 Tuning Voltage vs. time

From Figure 47, for large frequency steps, therefore giving large phase errors, the error stabilizes and the PLL loses lock. The VCO is free running. Due to the frequency detection of the PFD, the PLL goes into acquisition mode. The PFD is in the non-linear region known by the presence of successive “UP” or “DOWN” pulses at the PFD output. The spike on the tuning line represents a cycle slip in the acquisition mode.

Once the phase error remains less than $\pm 2\pi$, the PLL exits the non-linear region and enters the linear region. For small frequency steps, therefore giving small phase errors, the PLL tracks out the static phase error and the VCO tracks the input reference frequency. The PLL is in settling mode and the tuning line has the overshoot expected with a damping constant of 0.707 (labeled as “bump”) in Figure 47.

5.3 Conclusions

This chapter demonstrated the interaction between the VCO and the charge pump using a full loop simulation. The loop locked with a 1 MHz loop bandwidth. The simulation also proved that the loop locked with a large loop bandwidth, translating to a fast settling time, even with the presence of the CMFB of the charge pump.

Chapter 6 Conclusion

6.1 Conclusion

High frequency VCOs and a charge pump were designed for use in synthesizers. The goal was to investigate ways of reducing phase noise, while operating at high frequencies and considering reasonable current consumption.

The CMOSP13 technology was used to build high frequency $-G_m$ LC oscillators. They were designed for 20 GHz to challenge the performance limits of the models (passive and active components). The first chip produced two oscillators, one at 16 GHz and the other at 23 GHz, with each VCO having a tuning range of 1 GHz and each consuming less than 4 mA of current. The post-layout simulation results agreed well with the measured results in terms of frequency and tuning range. The output voltage and phase noise are quite different due to mismatched transistors and paths of high resistance.

A second chip was designed to make improvements over the first one. Schematic improvements involved variations such as having a differential control line and the use of a PMOS current source. Layout improvements involved interleaving of transistors, proper selection of varactor sizes, better routing of connections using higher level metals instead of using polysilicon and finally, proper modeling of metal lines as transmission lines. The oscillation frequencies of the VCOs on the second chip are expected to be 17 GHz with improved measured phase noise (greater than 20 dB) over the first chip VCOs and have a tuning range of 1 GHz.

In terms of phase noise, the differential input VCO has been shown in simulation to have a significant improvement over the single-ended input VCO because the $1/f$ corner frequency had been shifted down by two orders of magnitude (from 800 kHz to 8 kHz) through the use of filtering. High-pass filtering was proposed as the mechanism that reduces $1/f$ noise.

A fully differential charge pump was also designed on the second chip. It operates at 200 MHz and has a charge pump current of 200 μA . It has the option of being combined with the differential VCO. Having a fully differential VCO and fully differential charge pump gives a more robust design of the PLL since they provide suppression of common-mode signals.

A full loop simulation was done to ensure proper interaction between the differential VCO and the differential charge pump. The loop locked.

6.2 Future Work

Many improvements can be done to the designs. They are listed below.

1. Design and modeling of differential inductors. The designs only used predefined inductors in the IBM library. A differential inductor would mean less loss leading to improved quality factor and therefore improved phase noise.
2. The design of more sophisticated buffers. The buffers did not isolate the VCO core from the load very well. Also, a good buffer does not provide too much voltage loss from the input to the loaded output. At 20 GHz, this is very difficult to design.
3. Redesigning the center frequency to be 24 GHz, an ISM band, instead of 20 GHz. Designing for an ISM band would be more marketable. By taking the transmission lines and parasitic capacitance into account, the center frequency can be readjusted.
4. At frequencies approaching the performance limits or exceeding the performance limits of the inductor models, inductors should really be modeled with an EM simulator.

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5. Use of an off-chip balun (transformer) to measure differential results. Single-ended measurements were used to obtain all results. The difficulty is finding a balun that works at 20 GHz.
 6. Use of better equipment to measure phase noise. The E5500 phase noise kit will be used for the second chip VCOs. A spectrum analyzer was used for measuring the first chip VCOs. The drawback of using a spectrum analyzer is that the frequency drifts with slight changes in temperature, which makes it hard to make accurate phase noise readings. The E5500 phase noise kit puts a VCO under test into a loop, so the frequency is locked by the loop and is therefore more stable. Much more accurate phase noise measurements can then be done. At 20 GHz, the limits of the E5500 phase noise kit are being approached. The highest frequency the kit is qualified for is 26.5 GHz.
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