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Ground Noise Minimization in Integrated Circuit Packaging and Printed Circuit Packs

by

John M. Williamson, B.Sc., M.Sc.

This thesis is submitted to the Faculty of Graduate Studies and Research in partial
fulfillment of the requirements for the degree of

Doctor of Philosophy

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acceptance of the thesis.

**“Ground Noise Minimization in Integrated Circuit
Packaging and Printed Circuit Packs”**

submitted by

John M. Williamson, B.Sc., M.Sc.

in partial fulfillment of the requirements
for the degree of Doctor of Philosophy

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Abstract

Due to suboptimal assignment of pins to grounds and signals, the ground noise problem in integrated circuit (IC's) packages either persists or compromises the design by forcing too many pins to be wasted carrying ground reference. In addition, current IC placement rules do not, in general, account for the effects the relative IC positions have on ground noise at the PCB level. This document proposes a new CAD technique for optimizing pin assignment at the IC package and printed circuit board levels to minimize ground noise using simulated annealing. Optimization techniques are used in which the objective function is the ground noise as determined by simulation of the IC package leadframe and the board level track interconnect. However, modeling and simulation methods currently employed are prohibitively expensive in terms of CPU time.

For this reason, two circuit models of the total interconnect are developed and used concurrently: one to provide accuracy and the other to ensure fast execution. The first captures the leadframe at the IC level or the entire network of multi-connected PCB-level IC's. In the former case, the circuit elements used to describe the leadframe include resistors and inductors only. In the latter, the total interconnect is described in terms of resistive, inductive and capacitive parasitic elements. From these the signal path di/dt values are determined using a circuit simulator. These values are then provided to the second, entirely inductive model in which the noise voltages across the ground path inductances are calculated using a set of real, linear equations.

Results at the IC package and PCB levels indicate the usefulness of the method. Using simulated annealing with a ground noise cost function has provided an observed 26-fold reduction in ground noise in a 208-pin IC quad flat pack (QFP) from an admittedly poor initial configuration. However, the same process was able to produce a 2.2-fold improvement when an intelligent initial pin assignment was used. Furthermore, these

results came at a CPU cost of about 1200 seconds each on a SUN SPARC10 workstation. At the PCB level, a PCP containing 15 IC's was selected for ground noise optimization. Of the 15 IC's, five were singled out as targets for ground noise minimization. Of the five, one was a 64-pin QFP while the other four were 160-pin QFP's. Calculation of ground noise for this configuration involved 14 of the IC's on the PCB. A maximum ground noise threshold of 500mV was specified for the five target IC's. After about 5 hours (SPARC10), a solution configuration was found. The initial configuration produced a maximum PCB-level ground noise of over 900mV and after optimization, the maximum ground noise had dropped to below 700mV. However, for PCB-level optimization, the IC packages are invariant from iteration to iteration. Therefore, the optimization process is able to minimize that portion of the ground noise due to the PCB-level ground return path inductance. Prior to optimization this portion of the ground noise amounted to about 570mV. After optimization, this value dropped to just over 200mV. Ideally, such a board-level optimization would be conducted after each of the IC's of interest had been optimized at the IC-package level.

For my father, Kenneth who showed me the way

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Notation

A	Magnetic vector potential
$\tilde{A}$	System matrix
A_c	Companion matrix
A	Reciprocal of transfer function in ABCD matrix
B	Magnetic flux density
$\tilde{B}$	Initial condition matrix
C	Matrix of capacitances
C_m	Matrix of imaginary (reactive) circuit elements
C	Capacitance
C_{ij}	Capacitance between the i^{th} and j^{th} conductors
c	Speed of light in a vacuum
D	Electric flux density
D	Length of transmission line
di/dt	Change in current i with respect to time
$\partial\phi/\partial n$	Change in ϕ with respect to normal direction (Neumann condition)
∇	Operator $\partial/\partial u$ where u is any of the three directions x , y or z
E	Electric field intensity
e_{U_k}	Relative error in k^{th} objective function compared with upper bound
e_{L_k}	Relative error in k^{th} objective function compared with lower bound
ϵ	Permittivity
ϵ_0	Free space permittivity
ϵ_r	Relative permittivity
ϵ_{stop}	Maximum tolerable error

$F(\phi)$	Functional of variable ϕ
$F^e(\Phi_j)$	Error function vector
f	Objective function in optimization
f	General function
f	Frequency
ϕ	Scalar potential
Φ	Set of variables (pin assignment) of which objective function is a function
$G(r r')$	Green's function
G_m	Matrix of real (resistive) circuit elements
$\mathcal{G}$	Geometry of structure
γ	Set of variables (package position) of which objective function is a function
H	Magnetic field intensity
h	Time step size
I	Vector of currents
$i(t)$	Right-hand-side vector of sources
I_i	Current in i^{th} path
$I_{SN}, \dot{I}_{SN}$	Switching noise current and its derivative with respect to time
$I_{PS}, \dot{I}_{PS}$	Power supply surge current and its derivative with respect to time
$\mathbb{S}$	Set of integers
J	Current density (A/m^2)
J^*	Complex conjugate of J
K	Sheet current density (A/m)
K	Number of separate ground references within the same IC
k_i	i^{th} approximate residue
κ_1, κ_2	Scalar potential weighting factors
L	Matrix of inductances
L	Inductance
L_i^p	Partial inductance of i^{th} current path
L_{ij}	Mutual inductance between i^{th} and j^{th} current path
L_{ef}	Effective inductance
λ	Wavelength

Λ	Magnetic flux linkage
M	Mutual inductance matrix unless specified as a selector matrix
M_J	Jacobian matrix
m_r	r^{th} moment
μ	Permeability
N_{GRID}	Number of discrete locations on a PCB where a package may be located
N_G	Number of ground leads in a PCB-level ground noise estimation
N_L	Number of package level leads in a PCB-level ground noise estimation
N_R	Number of receivers in a PCB-level ground noise estimation
N_S	Number of signal leads in a PCB-level ground noise estimation
n_G	Number of discrete position in one row of the grid
n_{Gi}	Number of separate grounds in the i^{th} package
P	Probability
P_{E_i}	Probability that a state with energy E_i is the current state in simulated annealing
P_B	Number of PCB-level separate ground return paths
P_C	Number of packages in a PCB-level ground noise estimation
P_N, P_D	Numerator and denominator polynomials respectively in a rational function
p_i	i^{th} approximate pole
Ψ_{ij}	Magnetic flux linking current paths i and j
Q	Electric charge
R	Matrix of resistances
R	Resistance
R	Radius
$R(Y)$	Rank of matrix Y
$R_{M,N}$	Pade approximation
r	Distance from evaluation point to any other point in space
S_i	Number of signal leads in the i^{th} package leadframe
s	Laplacian frequency variable ($=j\omega$)
s	Surface
σ	Conductivity
T_{tl}	ABCD parameter matrix for a distributed transmission line

T_{LC}	ABCD parameter matrix for a lumped LC-section
t	Time
U	Unity matrix unless otherwise stated
V	Vector of voltages
V	Voltage
V_g, V_g	Ground noise voltage
$V_p^{(i)}$	Ground noise voltage in i^{th} package
V_{GB}	Ground noise due to PCB ground return path
V_{GD}	Ground noise due to driver package
V_{GR}	Ground noise due to receiver package
V_{GT}	Total ground noise voltage in a driver-to-receiver ground path
$v(t)$	Vector of unknown time-domain voltages and currents
$\dot{v}(t)$	Derivative with respect to time of $v(t)$
$\hat{v}(t)$	Approximation to $v(t)$
$\mathbf{v}$	Vandermonde matrix
$v_k(\Phi_j)$	k^{th} evaluation of the objective function
v	Volume
W	Energy
W_k	k^{th} weighting factor in objective function relative error
ω	Radian frequency ($=2\pi f$)
$\chi(t)$	Vector of non-linear voltages or currents
ξ_g	Fraction of total number of package pins assigned to ground
Y	Generic matrix
Y_A	General modified nodal admittance matrix
Y_R	Real part of Y_A
Y_I	Imaginary part of Y_A
Y	Transmission line quantity ($=G+j\omega C$)
Z	Complex impedance
Z_0	Characteristic impedance
Z	Transmission line quantity ($=R+j\omega L$)
ζ	Index set of non-zero error functions

Abbreviations

AWE	Asymptotic waveform evaluation
BEM	Boundary elements method
CFH	Complex frequency hopping
FEM	Finite elements method
FDTD	Finite differences time domain
IC	Integrated circuit
MNA	Modified nodal admittance
MOM	Method of moments
NILT	Numerical inversion of the Laplace transform
PCB	Printed circuit board
PCP	Printed circuit pack

Chapter 1

Introduction

1.1 Motivation

This thesis discusses a methodology by which ground noise due to integrated circuit packages and printed circuit boards can be estimated and minimized within a computer aided design (CAD) environment. To be successful, such a methodology must accomplish two things. First, it must provide characterization of electrical parasitics such as inductance and capacitance present in the interconnect from which active devices derive their ground reference. Second, it must use this characterization to quantify the expected ground noise via simulation. Furthermore, since it is desirable to have such a process work from within an interactive CAD system, the speed of the characterization and quantification processes must be maximized. With these capabilities in place we then use the ground noise estimation as the objective function to optimize both integrated circuit (IC) packages and their placement on a printed circuit board (PCB) via simulated annealing.

Ground noise, the transient shift of a reference potential away from its nominal value is a serious problem in high-speed printed circuit packs (PCP) because it often causes false switching in active circuits. Primarily, ground noise is due to parasitic inductance in the ground return path and the rate at which current through these parasitics is changing.

Currently, there exist numerous methods for the simulation of ground noise at the IC and PCP levels [SP94], [HHS92], [KTW93], [SNP93], [SC92], [MB92]. Reference [SP94] deals primarily with ground noise due to the simultaneous switching of CMOS devices. Great care is taken to accurately characterize the ground return structures and the CMOS drivers in order to predict the ground noise resulting from their interaction. The method discussed in [HHS92] shows how ground planes in IC packaging should be connected to the IC ground in order to make the ground plane current density uniform and thereby minimize the ground noise. In [KTW93] it was observed that increasing signal frequency and packaging complexity requires the use of 3D characterization techniques. To this end an efficient inductance extraction process is proposed. A common thread in all of the above is that accurate prediction of the ground noise waveform demands accurate characterization of the ground return path. This usually involves sophisticated numerical techniques for both characterization and simulation.

This thesis proposes a method for minimizing IC package-level ground noise by optimizing the signal/ground pin assignment and then extends the method to provide estimation of ground noise at the PCB level. Using this extension, the placement of chips on a pre-routed board is optimized for ground noise performance. To achieve these ends, ground noise as determined through simulation, is used as the objective function in an optimization process. For large IC packages with inputs/outputs (IO) exceeding 200 pins the number of function evaluations via simulation needed to reach an optimum pin assignment can easily be in the thousands. Furthermore, board level optimizations are even more evaluation intensive. Therefore, simulation CPU time is at a premium and precludes the highly accurate methods found in [SP94], [HHS92], [KTW93], [SNP93], [SC92], [MB92] which often take several hours for each evaluation. Instead, this thesis proposes an optimization formulation and a novel method for fast ground noise simulation.

Optimization using simulated annealing [KGV83], [Rut89] was chosen for its ability to proceed past local minima. The formulation consists of defining a real valued objective function, in this case ground noise, as a function of a set of integer variables, in this case the assignment of signals and ground to the package pins at the package level and, at the

PCB level, the assignment of packages to discrete locations on the board. Each time the optimizer calls for a different assignment of integer values, a different pin assignment or package placement occurs requiring a new simulation. To provide sufficiently short duration simulations, it is advisable to develop two modeling/simulation approaches. The first approach accounts for a linearized driver output resistance as well as the parasitic inductance and capacitance of the package leadframe. Package-level ground noise is then calculated in the time-domain by constructing a modified nodal admittance (MNA) matrix [HRB75] and solving it using numerical inversion of the Laplace transform (NILT) [VS83], [SVN76]. More importantly, a by-product of solving the MNA matrix equation is the set of rates-of-change of the source currents di/dt , in the leadframe. Subsequently, the di/dt values thus obtained are used in the second modeling/simulation approach. Since ground noise is predominantly due to the inductive parasitics (self and mutual), the second approach model consists only of the leadframe inductance matrix and simulation merely consists of solving a real-valued system of linear equations which relates peak ground noise to the di/dt 's, in the leadframe inductances. Subsequently, to determine the PCB-level contribution to the ground noise, the MNA matrix is augmented by the PCB-level parasitic inductance and capacitance in the first approach. In the second approach, it is the lead-frame inductance matrix alone which is augmented by the board-level parasitic inductances. Thus the board-level modifications affect only the modeling. The simulation processes in the two approaches are the same at board-level as they were at package-level. The simplifications made in the second approach make it hundreds of times faster than the first approach yet preserves sufficient accuracy due to the use of accurately determined di/dt 's. Thus employing the second approach to repeatedly evaluate the ground noise objective functions requires far less CPU time to achieve an optimum result. Comparisons of an accurate non-linear driver simulation with simulations obtained from the second approach indicate a several thousand fold increase in performance with the results in agreement within a few percent.

1.2 Definition of ground noise

The trend in the evolution of electronics has been one of extracting more performance from less material occupying a smaller space. In the early 1970's, IC's comprised of thousands of transistors were mounted on single-sided PCB's where coplanar signal and ground tracks constituted the interconnect for the active circuits. Today, the same piece of silicon houses millions of transistors and may be mounted on PCB's with twenty or more layers. One of the reasons for the greatly increased PCB complexity is the need to minimize the interconnect parasitic impedance for signals of ever increasing operating frequency. This is especially true for that part of the interconnect carrying the ground return path. Because of the increase in frequency, active circuits which in the past could be connected to ground via a single PCB track, now require entire solid metal planes in an attempt to keep the ground reference of the active circuits actually at ground potential. The occurrence of a non-ground voltage in the ground reference is referred to as ground noise. More formally, ground noise is the presence of non-nominal (usually non-zero) voltage in the ground reference of the active circuit. It is caused by the impedance due to resistive, inductive and capacitive parasitics in the return-current path with inductance being the major culprit. Inductance is the main factor because of the fact that where there is time-varying current flowing in an inductor, there is voltage across the inductor given by

$$V = L \frac{di}{dt} \quad (1.1)$$

Equation (1.1) has serious ramifications for digital electronics and it is these ramifications that this thesis will address and mitigate. Digital format is inherently susceptible to ground noise because the output is dependent on the difference between the input and the ground reference and therefore on any swings in the reference. Furthermore, upward pressure on data rates forces di/dt up and since digital trapezoidal waveforms are harmonically rich,

ground noise can occur at deceptively low data rates. As an example, consider Figure 1.1. Here, the signal waveform at the active receiver and the ground noise waveform at the quiet receiver are shown. On the falling edge of the active waveform, the ground reference of the quiet receiver bounces down to -0.8V. Since the input to the quiet receiver is 0V, the receiver detects a 0.8V signal at its input. For some digital technologies, TTL for example, such spurious inputs can cause false triggering.

Figure 1.1: Digital waveform with ground noise

In the early 1970's, a 1MHz trapezoidal waveform with 100ns risetime was typical. If drivers and receivers 10cm apart (see Figure 1.2) were connected to ground by a standard PCB trace, the inductance L of the trace would be of the order of 100nH. If the 1MHz signal produced a 10mA return current, the ground noise would be $100\text{nH} \times 10\text{mA}/100\text{ns} = 10\text{mV}$. If

the same circuit is used today at 100MHz and the return current is still 10mA, the ground noise voltage across L increases to 1.0V assuming the current now switches in 1ns. If in Figure 1.2 the active line makes a high-to-low transition, the ground potential at the receiver will drop 1.0V which may be interpreted by the receiver as a high state at its input since $V_{rec} = V_{in} - V_{ref} = 0 - (-1.0) = 1.0V$. A false state change will then occur at the output of the receiver.

Figure 1.2: Typical ground noise environment

Unfortunately, ground noise is not the only problem in digital electronics. Parameters such as thermal flux, power budget and crosstalk performance also play a role. In accounting for these other constraints, efficient digital layout on a PCB demands high chip density and large IC packages, resulting in placement of some chips far from absolute ground. These practices run counter to effective ground noise management. Furthermore, Figure 1.1 depicts but a single active driver and in reality, there may be dozens of active drivers simultaneously contributing ground noise to the same victim quiet line. Therefore (1.1) must really be modified to get a more accurate picture of what elements contribute to ground noise.

$$V_g \propto \sum_{k=1}^N L_k \frac{di_k}{dt} \quad (1.2)$$

Here, N represents the number of simultaneously switching drivers. It is because of the

many factors contributing to ground noise and its inextricability from other design issues that present board design practices are rapidly becoming obsolescent. However, these other signal quality degradation factors are beyond the scope of this thesis which is concerned with the ground noise problem. In order to properly address ground noise, we must have the means to estimate ground noise and drive the layout process based on minimizing the ground noise. In Chapters 3 through 5, just such an automated process is discussed.

1.3 Contribution

The ideas developed and implemented as reported in this thesis arose from a need in the early 1990's for a technique to characterize and simulate ground noise in IC packages and the PCB's on which they reside. From the beginning, the intent was to incorporate the ideas and lessons learned from many years in industry into a CAD environment such that, as far as possible, ground noise could be reduced along with the other deleterious phenomena typically analyzed during the CAD phase of product development. In looking to existing products available from computer aided engineering (CAE) vendors, it soon became apparent that they had all, to some degree, pursued electronic and electromagnetic phenomena with the intent of maximizing accuracy. There can be no doubt of the great value of techniques which have evolved pursuing a maximum accuracy philosophy. However, accuracy comes at the price of often prohibitive CPU time. Therefore, the maximum accuracy philosophy tends to find application in electronic structures with well defined topological boundaries, i.e. it is fairly straightforward to determine what structures are part of the circuit under test and those which are not. Furthermore, analysis is only carried out when such a structure has been isolated as likely to exhibit inadequate performance. The role such methods play is usually one of verification. That is, the designer has some idea of the required structure and proceeds to verify its performance by characterization and subsequent simulation. However, ground noise characterization at the PCB and even the IC package level does not lend itself well to specific structure analysis

because it is difficult to know what part of the ground structure significantly affects the performance of a given circuit net. This means that an entire PCB ground sheet will have to be characterized and simulated with the other more obviously defined circuit elements. Such a formidable task is virtually impossible using existing methods if the desire is to optimize the placement of IC's on the PCB such that the maximum ground noise is minimized. Such a method is precisely what is proposed in this document and forms the principal contribution to the general body of knowledge.

The subject of this thesis is the optimization of IC package signal-to-pin assignment and of the placement of IC packages on PCB's such that ground noise is minimized. In view of the fact that existing methods are incapable of performing such tasks in a reasonable amount of time, the principal contributions of this document are:

1. Significant simplification to the circuit simulation process by characterization of the ground return pathways as purely inductive. It has long been known that the dominant parasitic characteristic of package leadframes, PCB tracks and ground planes is inductive. By concentrating on this single parasitic element, an elegantly simple method for simulation of the maximum ground noise level emerges. Whereas in general a circuit characterization is simulated by formulation and solution of a set of complex linear differential equations, the approach in this document allows for solution of a set of real algebraic equations as long as the change with respect to time of all non-ground currents (di/dt) is known (di/dt determination is outlined in contribution 4). Since the objective is to minimize the peak value of the ground noise, the need for maintaining accurate ground noise wave-shape and phase information is obviated. So far comparisons of this method's ground noise estimates and those found by more conventional means indicate errors within 5%. On the other hand, the proposed method can be thousands of times faster making possible the signal-to-pin optimization of high IO count packages in under a half hour of CPU time. Furthermore, optimization of IC placement is also possible for the same reason.
2. Breakdown of board-level ground noise into one of two possible modes. The study of ground noise led to the realization that ground noise could occur in two ways. In

the first and far more predominant mode, worst-case ground noise often occurs when a driver makes a high-to-low state transition. The ground noise is caused by the current in the ground structures between the driver and receiver. In the second mode, a driver switches causing a momentary surge of current from the power supply through the driver in transition and back to the power supply ground. The two ground noise modes require very different treatment and both are described in this document.

3. Development of a special superposition technique (SST) to improve the speed of planar structure inductance characterization. Inductance characterization in planar structures is required in the analysis of ground noise arising from the second mode. In a planar structure with N inductive pathways, there will be N self and a further $N(N-1)/2$ mutual inductance characterizations. Normally this would involve a numerical technique such as FEM $N(N+1)/2$ times. However, using SST the number of separate characterizations drops to $N + 1$. On a PCB with a thousand inductive pathways (modern PCB's often have several thousand) use of SST would result in a 500-fold performance improvement.
4. Application of numerical inversion of the Laplace transform (NILT) [SVN76] to determine the required di/dt values. To evaluate the ground noise voltages properly it is necessary to have the maximum di/dt values for all drivers. This was made possible by making the process compatible with NILT. The advantage of using NILT was twofold. First it is often faster than SPICE-type simulators for this application due to its simplicity. Secondly, it was much easier to implement into the source code than a SPICE-type simulator.

1.4 Organization of the Thesis

In Chapter 2 we begin with a discussion of some of the methods others have used to approach the problem and why it is still important to develop the methodology specified in

this thesis. Chapters 3 and 4 cover the methods used to characterize and quantify ground noise at the package and board levels culminating in a fast method suitable for repetitive use in optimization. Furthermore, Chapter 4 expands on the methods of Chapter 3 through the development of more detailed models of the interconnect required at the PCB level and demonstration of their favorable comparison with the simpler, faster method. In Chapter 5 we show how discrete simulated annealing lends itself to optimization of the IC package pin configurations and of the packages' placement on a PCB. In Chapter 6 examples of the evaluation of ground noise at both package and PCB level are presented indicating the expected speed and accuracy of the methodology. Conclusions follow in Chapter 7.

Chapter 2

Previous work in ground noise analysis

Before proceeding with ground noise mitigation methods which constitute the subject of this thesis, it is necessary to discuss the work of others upon which this thesis is at least in part based. Any analysis of ground noise requires two areas of endeavor. First, the structure in which the ground noise occurs must be characterized. Secondly, the structure so characterized must be simulated to predict the ground noise. For this reason, the areas of the existing literature which are presented in this chapter are concerned with the characterization and simulation of interconnect structures for the purpose of predicting and/or minimizing ground noise.

2.1 Characterization of the interconnect

Because ground noise is a spurious voltage occurring in interconnect structures, it is logical to want to predict it as accurately as possible via simulation. To achieve this end, it is necessary to first characterize all the parasitic electrical elements which exist in the interconnect structure. Once complete, such a characterization would then be the input to a circuit simulator which would forecast the ground noise voltage. Consequently, this

section deals with existing characterization methods while the next section covers simulation.

Most of the work done in characterization and simulation resulting in an estimation of ground noise performance is similar to that found in [SP94], [HHS92], [KTW93], [SNP93], [SC92], [MB92] the common element being the emphasis on accuracy. The techniques proposed in such papers are suitable for CAD applications because they are quite general and as such form a high-accuracy counterpart to the high-performance methods proposed in this thesis. As mentioned in the introduction, accuracy of both characterization of the electrical structures leading to circuit parameter values and the simulations in which they are used is of paramount importance in the six references above. Given such emphasis, it is reasonable to expect that a premium is to be paid in both characterization and simulation CPU time. For example in [SP94] and [SNP93] accurate characterization of the ground structures is a prerequisite for the determination of ground noise in IC packages.

As pointed out in [SP94], the ground path through a modern electronic IC package may include, “signal traces, bond wires, metal planes, vias and pins”. Most difficult to characterize are planar structures where the current is free to spread out. The method described in [SP94] begins by considering the electric field due to the ground return current in a structure such as that shown in Figure 2.1.

Figure 2.1: Current paths in a planar interconnect structure

Obviously, there would be a small amount of current entering the ground plane at points a and b (sources) which would enter the PCB ground at points d and c (sinks) respectively. In general

$$\sum_{i=1}^N I_i = \sum_{j=1}^M I_j \quad (2.1)$$

where N is the total number of current source points and M is the total number of current sink points where the package ground pins connect to the PCB ground plane. The total currents in (2.1) give rise to an electric field inside the ground plane given by

$$\mathbf{E} = -\nabla\phi - j\omega\mathbf{A} \quad (2.2)$$

where $\mathbf{A}$ is the magnetic vector potential. For (2.2) to apply, the assumption that the current is not subject to significant variation in the z -direction must be made, i.e. the current varies only in the x and y directions since the ground plane is considered to be in the x - y plane. Due to Ohm's law (2.2) can be rewritten as

$$\mathbf{J} = -\sigma\nabla\phi - j\sigma\omega\mathbf{A} \quad (2.3)$$

where $\mathbf{J}$ is current density and σ is the conductivity of the ground plane. Inside the ground plane, magnetic diffusion effects are considered negligible giving an approximation for current density

$$\mathbf{J} = -\sigma\nabla\phi \quad (2.4)$$

Maxwell's equation from Gauss's law states that

$$\nabla \cdot \mathbf{D} = 0 \quad (2.5)$$

and therefore since

$$\mathbf{D} = \frac{\varepsilon}{\sigma} \mathbf{J} \quad (2.6)$$

it must also be the case that

$$\nabla \cdot \mathbf{J} = 0 \quad (2.7)$$

Substitution of (2.4) into (2.7) results in the well-known Laplace equation for electric potential, namely

$$\nabla^2 \phi = 0 \quad (2.8)$$

From calculus of variations [Sad92], it can be shown that solving (2.8) is equivalent to minimizing the functional defined by

$$F(\phi) = \frac{1}{2} \int_v (\nabla \phi)^2 dv \quad (2.9)$$

where the volume, v is reduced to a surface in the x - y plane. As a result, (2.8) can be solved numerically using the finite element method (FEM). In this case the following boundary conditions apply: 1) At plane boundaries the Neumann condition

$$\frac{\partial \phi}{\partial n} = 0, \quad (2.10)$$

2) At all sink points $\phi = 0$ and at source points ϕ is assigned an arbitrary non-zero value. Once ϕ has been determined, the total current entering each sink point can be calculated using

$$I_{total} = t \oint_C \mathbf{J} \cdot \mathbf{n} dl \quad (2.11)$$

where t is the thickness of the plane and the contour C is any closed path encircling a particular sink point. Using the current density determined in (2.4) in conjunction with the free-space Green's function $G(r|r')$, where

$$G(r|r') = \frac{1}{4\pi|r-r'|} \quad (2.12)$$

gives rise to an expression for the magnetic vector potential

$$\mathbf{A} = \mu \int_v \mathbf{J}(r') G(r|r') dv' \quad (2.13)$$

From (2.4) and (2.11), the resistance of the current path can be determined according to

$$R = \frac{1}{\sigma |I_{total}|^2} \int_v \mathbf{J} \cdot \mathbf{J}^* dv \quad (2.14)$$

where the asterisk denotes complex conjugation. More importantly, from (2.4), (2.11) and (2.13) the inductance of the current path can be determined using

$$L = \frac{1}{|I_{total}|^2} \int_v \mathbf{J}^* \cdot \mathbf{A} dv \quad (2.15)$$

Equations (2.2-2.15) represent the theoretical basis for the inductance calculation package called UALGRL(c). As an example, consider the partial plane in Figure 2.2. The shaded region represents the IC-package ground plane to which the IC is connected via two bondwires. These connection points represent the sources mentioned in (2.1). At the outside edge the ground plane connects to the PCB ground via three ground pins and these represent the sink points.

Figure 2.2: IC ground plane inductance

If the IC grounds are all assumed to be at the same potential, UALGRL will return a single effective value for the inductance of the plane given this source/sink pattern and another for the effective resistance. Table 2.1 shows the results as a function of the mesh pattern in terms of the number of nodes in the x and y directions respectively.

Table 2.1: UALGRL generated inductances

FEM pattern	Effective R(mΩ)	Effective L(nH)	CPU time (s)
4 x 14	0.304441	2.760354	2.4
8 x 28	0.375440	3.268950	26.7
12 x 42	0.332305	2.915504	131.6
16 x 56	0.362298	3.144270	413.6

The CPU times shown in Table 2.1 were observed on a SPARC10 workstation.

In [SNP93] the theme is similar except that the ground over which the high-speed signals travel is considered non-ideal. In standard transmission line theory for lossless conductors, the voltages and currents present in the conductors are given by the lossless telegrapher equations, namely

$$\frac{dV}{dz} = -L \frac{\partial I}{\partial t} \quad (2.16)$$

and

$$\frac{dI}{dz} = -C \frac{\partial V}{\partial t} \quad (2.17)$$

where, because there may be N conductors, V , I , L and C are matrices of rank N . In (2.16) and (2.17) it is assumed that each of the conductors is referred over its entire length to a perfect ground conductor. The authors point out that this is not the case and that the effect of the imperfect ground should be reflected in the above L and C matrices. In fact it can be shown that the effect of the parasitic ground inductance is accounted for in the i^{th} conductor according to

$$L_i^e = L_i^p + L_g^p - 2L_{ig}^p \quad (2.18)$$

where e denotes effective, p denotes partial and g refers to the ground conductor. The term L_{ig}^p is of course the mutual inductance between the signal and ground conductors and is negative because the ground current travels, by definition, in the opposite direction. To account for the ground inductance in a circuit simulator, the method used in [SNP93] proposes replacing the ideal distributed transmission line model of (2.16) and (2.17) with a non-ideal lumped parameter model based on the partial inductances of (2.18). According to [Rue72], partial inductance in general derives from the general definition of inductance given by

$$L_{ij} = \frac{\Psi_{ij}}{I_j}, \quad I_k = 0, \quad k \neq j \quad (2.19)$$

where Ψ_{ij} represents the magnetic flux in loop i due to a current I_j in loop j . The vector potential generated by a current I_j in loop j is given by

$$A_{ij} = \frac{\mu}{4\pi s_j} \oint \oint \frac{d\mathbf{l}_j ds_j}{r_{ij}} \quad (2.20)$$

where $r_{ij} = |\mathbf{r}_i - \mathbf{r}_j|$, $d\mathbf{l}_j$ is an element of conductor j with direction along the axis of the conductor and s_j is the cross sectional area of the conductor perpendicular to the current flow. Since the above magnetic flux is related to A_{ij} according to

$$\Psi_{ij} = \frac{1}{s_i} \oint \oint A_{ij} \cdot d\mathbf{l}_i ds_i, \quad (2.21)$$

combining (2.19-2.21) yields

$$L_{ij} = \frac{1}{s_i s_j} \frac{\mu}{4\pi} \oint \oint \oint \oint \frac{d\mathbf{l}_i \cdot d\mathbf{l}_j}{r_{ij}} ds_i ds_j \quad (2.22)$$

Thus with the method described in [SP94], L_i^e in (2.18) is known. Furthermore, L_i^p and L_g^p in (2.18) can be found using (2.22). Hence the partial mutual inductance between signal and ground is obtained by rewriting (2.18) as

$$L_{ig}^p = \frac{L_i^p + L_g^p - L_i^e}{2} \quad (2.23)$$

At this point the ground inductances can be incorporated into simulations yielding both ground noise and cross-talk.

In [HHS92], the inductance characterization, again of an IC package-level ground plane, is used to optimize the ground pin attachment points of the ground plane. Specifically, the authors present the diagram shown in Figure 2.3 representing a section of ground plane between IC bondwire connection (source) and ground pin attachment point (sink).

Figure 2.3: Section of ground plane between arbitrary source and ground

The authors of [HHS92] showed that the current density J on the $y = 0$ line in Figure 2.3 is given by

$$J(x, 0) = \frac{\sigma V_0 \lambda^2}{\left[x^2 + \left(\frac{\lambda}{2} \right)^2 \right]^{3/2}} \quad (2.24)$$

If the condition, $J(d/2, 0) = \frac{J(0, 0)}{2}$ where d is the maximum pin distance, is imposed so that the current density is uniform along the $y = 0$ line, then $d = 0.75\lambda$. Using this result leads to a superior ground pin positioning pattern in terms of ground noise. Since the current is more uniform, the maximum ground noise voltage is reduced. The conventional and optimal pin attachments are shown in Figure 2.4.

Figure 2.4: Current distribution in an IC package ground plane

A very different approach to interconnect characterization is given in [KTW93]. In this paper 3D structures are characterized using volume filaments. Furthermore, using a multi-pole accelerator, the required CPU time increases as almost order n rather than as order n^2 as would normally be expected. In this case, n represents the number of volume filaments describing the structure. In the method presented, each conductor is divided up into a set of

piecewise-straight sections. The volume of each section is then broken up into a collection of parallel thin filaments through which current is assumed to flow uniformly. Figure 2.5 shows schematically a single conductor which has been divided up into three sections each of which consists of four parallel current filaments.

Figure 2.5: Schematic of multi-section conductor

The b branch impedances relate the branch currents to branch voltages according to

$$\mathbf{Z}\mathbf{I}_b = \mathbf{V}_b \quad (2.25)$$

where $\mathbf{Z}$ is of rank b and

$$\mathbf{Z} = \mathbf{R} + j\omega\mathbf{L} \quad (2.26)$$

$\mathbf{R}$ is a diagonal matrix representing the DC resistance of each branch and $\mathbf{L}$ is a dense matrix of partial self and partial mutual inductances given by

$$L_{ij} = \frac{1}{s_i s_j} \frac{\mu}{4\pi} \oint_{ij} \frac{d\mathbf{l}_i \cdot d\mathbf{l}_j}{r_{ij}} \quad (2.27)$$

which is exactly the same as (2.22) if there is uniform current distribution in each of the filaments. Applying Kirchoff's voltage law around each of the meshes shown in Figure 2.5 results in

$$\mathbf{M}\mathbf{V}_b = \mathbf{V}_s \quad (2.28)$$

where $\mathbf{M}$ is a selector matrix of 1's and 0's. Furthermore, the mesh currents in each loop give rise to

$$\mathbf{M}^t \mathbf{I}_m = \mathbf{I}_b \quad (2.29)$$

where t denotes the transpose. Combining (2.28) and (2.29) yields

$$\mathbf{M}\mathbf{Z}\mathbf{M}^t \mathbf{I}_m = \mathbf{V}_s \quad (2.30)$$

The matrix $\mathbf{M}\mathbf{Z}\mathbf{M}^t$ in (2.30) is dense and time consuming to solve. It is here that the multipole technique can be applied. First, (2.30) is expanded according to (2.26) resulting in

$$\mathbf{M}\mathbf{Z}\mathbf{M}^t \mathbf{I}_m^k = \mathbf{M}\mathbf{R}\mathbf{M}^t \mathbf{I}_m^k + j\omega \mathbf{M}\mathbf{L}\mathbf{M}^t \mathbf{I}_m^k \quad (2.31)$$

The first term on the right-hand-side of (2.31) is sparse since $\mathbf{R}$ is diagonal. The second term, however, requires order m^2 operations to solve. By considering only $\mathbf{L}\mathbf{M}^t \mathbf{I}_m^k$ or equivalently $\mathbf{L}\mathbf{I}_b$, (2.27) can be used to rewrite $\mathbf{L}\mathbf{I}_b$ in terms of the vector potential, $\mathbf{A} \in \mathbb{C}^3$ (3D complex) which is given by

$$\mathbf{A} = \frac{\mu}{4\pi} \sum_j \frac{\mathbf{I}_{b_j}}{s_j} \int_{\text{filament}_j} \frac{d\mathbf{l}_j}{r_j} dv_j \quad (2.32)$$

Specifically, the i^{th} element in $\mathbf{LI}_b$ is the average over the filament cross section of the integral of the vector potential along filament i which can be represented by

$$(\mathbf{LI}_b)_i = \frac{1}{s_{i\text{filament}_i}} \int \mathbf{A}_i \bullet d\mathbf{l}_i dv_i \quad (2.33)$$

Each component of the vector potential in (2.32) can be identified with a scalar electrostatic potential due to a collection of filament charges. Hence, for $k \in \{1, 2, 3\}$ the k^{th} component of $\mathbf{A}$ denoted by $\psi_k \in C$ (C denotes complex) is a scalar potential given by

$$\psi_k = \frac{\mu}{4\pi} \sum_j \frac{\mathbf{I}_{b_j}}{s_j} \int_{\text{filament}_j} \frac{(d\mathbf{l}_j)_k}{r_j} dv_j \quad (2.34)$$

suggesting that $(\mathbf{I}_{b_j}/s_j) (d\mathbf{l}_j)_k$ can be interpreted as a charge density. It is the evaluation of these electrostatic potentials which can be accelerated by using the multipole technique. Conceptually, evaluating the electrostatic potentials at n_1 points due to n_2 point charges involves $n_1 \times n_2$ operations. The multipole method is able to reduce this due to the fact that the charge space details do not strongly affect the results in the evaluation space due to the fact that $r \gg R$ as shown in Figure 2.6.

Figure 2.6: Space concept in multipole acceleration

A synopsis of the performance results presented in [KTW93] are shown in Figure 2.7 .

Figure 2.7: Multipole performance

2.2 Simulation of the interconnect

The vast majority of circuit simulation methods in use today fall into one of three types: 1) SPICE-type, 2) Numerical inversion of the Laplace transform (NILT) or 3) Asymptotic Waveform Estimation (AWE). Interconnect topology is the same regardless of simulation method. Moreover, once an interconnect structure has been characterized in terms of electrical circuit parameters, the purpose of simulation is to predict voltages and currents anywhere in the structure or functions thereof upon applying some sort of stimulus to one or more nodes of the interconnect structure. It is convenient to determine unknown node voltages resulting from one or more known source currents. This is the basis for the modified nodal admittance (MNA) matrix approach. In general, to obtain the network node voltages, the following equation is solved

$$\mathbf{C}_m \dot{\mathbf{v}}(t) + \mathbf{G}_m \mathbf{v}(t) + \boldsymbol{\chi}(t) - \mathbf{i}(t) = \mathbf{0} \quad (2.35)$$

where $\mathbf{C}_m, \mathbf{G}_m \in \mathbb{R}^{N \times N}$ and represent lumped linear reactive and resistive components respectively,

$\mathbf{v}(t)$ is the vector of unknown voltages augmented by any independent voltage source currents and inductor currents,

$\boldsymbol{\chi}(t)$ is a vector of nonlinear current voltage relationships and

$\mathbf{i}(t)$ is the source current vector.

2.2.1 SPICE-type simulators

In this kind of simulator, (2.35) is solved using a numerical integration formula where the $\dot{\mathbf{v}}$ term at time t is defined in terms of $\mathbf{v}$ at time t and possibly previous values of both $\dot{\mathbf{v}}$ and $\mathbf{v}$. The Forward Euler (FE) and Backward Euler (BE) are examples of first order inte-

gration formulae and are given in (2.36) and (2.37) respectively.

$$\dot{v}_n = \frac{v_{n+1} - v_n}{h} \quad (2.36)$$

$$\dot{v}_{n+1} = \frac{v_{n+1} - v_n}{h} \quad (2.37)$$

The subscript n in (2.36) and (2.37) refers to the n^{th} point in time and h is the time step size. One other standard integration formula is the Trapezoidal Rule (TR) which is second order and given by

$$\dot{v}_{n+1} = -\dot{v}_n + \frac{2(v_{n+1} - v_n)}{h} \quad (2.38)$$

The BE and TR are examples of absolutely stable integration formulae and as such are widely used, however, there is a host of others.

In general, the simulator will solve (2.35) by first substituting the definition for $\dot{v}$ as defined by its integration formula into (2.35). For example, a BE formula simulator would in effect be solving

$$f(v) = \left[\frac{1}{h} C_m + G_m \right] v_{n+1} + \chi(v_{n+1}) - \frac{1}{h} C_m v_n - i(t_{n+1}) = 0 \quad (2.39)$$

The general solution to (2.39) must be determined iteratively using Newton iterations based on the fact that

$$f(x_0) \approx f'(x_0) [x_0 - x_1] \quad (2.40)$$

which is clearly illustrated in Figure 2.8.

Figure 2.8: Basis of Newton iterative root-finding process

In (2.35) C_m and G_m were defined to be of rank N which implies that, in general, (2.39) describes a system of N non-linear equations in terms of N unknown quantities. Each equation in the system can be expressed as a Taylor series expansion with the terms of order two and above assumed to be negligible or

$$f(x) \approx f(x_0) + f'(x_0) [x - x_0] = 0 \quad (2.41)$$

where x_0 represents the initial values of the vector x which corresponds to v in (2.39). Since each equation in the system in (2.39) can be represented as shown in (2.41), solution of (2.41) will require the partial derivatives of the N functions with respect to each of the N variables in x resulting in a Jacobian matrix, M_J [Per88]. Hence the Jacobian of the system in (2.39) is defined as

$$M_J = \frac{1}{h} C_m + G_m + \frac{\partial \chi}{\partial v} \quad (2.42)$$

based on use of the BE integration formula. Now (2.41) can be applied to (2.39) for an iter-

ative solution where the solution of each iteration appears as the vector of unknowns in

$$\mathbf{M}_J|_{\mathbf{v}_0} \Delta \mathbf{v} = -f(\mathbf{v}_0) \quad (2.43)$$

where

$$\Delta \mathbf{v} = \mathbf{v}_1 - \mathbf{v}_0 \quad (2.44)$$

with $\mathbf{v}_0$ being the initial (or old) values of $\mathbf{v}$,

$\mathbf{v}_1$ being the subsequent (or new) values of $\mathbf{v}$ and

$f(\mathbf{v}_0)$ being the evaluation of $f(\mathbf{v})$ in (2.41) at $\mathbf{v}_0$. Using (2.43) and (2.44), the iterations would continue until

$$\|\Delta \mathbf{v}\| = \sqrt{\sum_{i=1}^N (\Delta v_i)^2} < \epsilon_{stop} \quad (2.45)$$

where ϵ_{stop} is the maximum tolerable error. Some integration formulae such as the BE are stable for all values of the time-step value h . However, in highly non-linear circuits such as those containing bipolar transistors, accuracy may not be acceptable unless h is very small and this may severely slow down the simulation process. If the non-linear elements can be linearized, this constraint is removed since in that case (2.43) will reach $\Delta \mathbf{v} = \mathbf{0}$ after a single iteration. However, even in a linear circuit, the desired waveforms must be evaluated as functions of sequential time. The implication here is that once a sufficiently small h has been determined, the desired waveform value at $t = 10h$ cannot be found without finding those at $t = 9h$, $t = 8h$, etc. So although only one iteration is required for each new time point evaluation, there may still be a lot of such evaluations required. This disadvantage is not a characteristic of simulation using the NILT process.

2.2.2 NILT simulators

The Laplace transform is an indispensable tool in circuit analysis since it allows straightforward treatment of the interaction between linear time-invariant systems and any stimuli to such systems. This is due to the fact that convolution in the time domain is reduced to simple multiplication in the frequency domain. NILT-based simulation is therefore carried out first by consideration of the frequency domain equivalent of (2.35). One restriction of such considerations is that the $\chi(v)$ term in (2.35) must be zero since components whose voltages are non-linear functions of currents cannot be represented in the frequency domain. This is not a major disadvantage when CPU time is the critical factor and it is known that non-linear analysis can be prohibitively expensive in CPU-time. Linearization of (2.35) gives the frequency domain equivalent

$$sC_m V(s) + G_m V(s) - I(s) = 0 \quad (2.46)$$

where the Laplacian variable $s = j\omega$ where ω is the radian frequency and s is equivalent to the $\frac{d}{dt}$ operator in the time domain. Since solution of (2.46) results in a frequency domain representation of the unknown voltages and a time domain representation is desired, the inverse Laplace transform must be applied according to the formula [VS83]

$$v(t) = \frac{1}{2\pi j} \int_{c-j\infty}^{c+j\infty} V(s) e^{st} ds \quad (2.47)$$

Exact inversion is possible only if the poles of $V(s)$ are known which implies the CPU-intensive root-finding process. Instead of this, an approximation to the integrand is carried out by removing t according to the transformation

$$z = st. \quad (2.48)$$

Replacement of s in (2.47) according to (2.48) results in

$$v(t) = \frac{1}{2\pi jt} \int_{c'-j\infty}^{c'+j\infty} V(z/t) e^z dz \quad (2.49)$$

Next, e^z is approximated by a rational function (Pade approximation) $R_{M,N}(z)$ and equated to some terms of a series according to

$$R_{M,N}(z) = \frac{P_M(z)}{Q_N(z)} = \frac{\sum_{i=0}^M a_i z^i}{1 + \sum_{i=1}^N b_i z^i} = \sum_{i=0}^{M+N} c_i z^i + \sum_{i=M+N+1}^{\infty} c_i z^i \quad (2.50)$$

Here the Pade approximation is equal to the Taylor series expansion in the first $M+N+1$ terms.

The system of equations in (2.50) has a closed form solution given by

$$R_{M,N}(z) = \frac{\sum_{i=0}^M (M+N-i)! \binom{M}{i} z^i}{\sum_{i=0}^N (-1)^i (M+N-i)! \binom{N}{i} z^i} \quad (2.51)$$

Substitution of (2.50) into (2.49) yields the approximation $\hat{v}(t)$ to $v(t)$ given by

$$\hat{v}(t) = \frac{1}{2\pi jt} \int_{c'-j\infty}^{c'+j\infty} V(z/t) R_{M,N}(z) dz \quad (2.52)$$

If the path of integration is closed either to the right or the left, (2.52) may be evaluated using residue calculus. In order to ensure that the path along the infinite arc does not contribute to the integration, the stipulation that $N \geq M + 2$ is made. The approximation of e^z therefore has at least two more poles than zeros. After applying the residue theorem to (2.52) the integration can be carried out by summing the residues according to

$$\int_C V(z/t) R_{M,N}(z) dz = -2\pi j \sum_{i=1}^N r_i \quad (2.53)$$

where r_i represents the residues resulting from closing the path of integration in the right half plane. The right half plane is chosen because there, no poles of $V(z/t)$ exist. Since $M < N$,

$$R_{M,N}(z) = \sum_{i=1}^N \frac{K_i}{z - z_i} \quad (2.54)$$

where z_i are the poles of $R_{M,N}(z)$ and K_i are the corresponding residues. Note that the K_i residues can be found from a partial fraction expansion of $R_{M,N}(z)$ in (2.51); they are not the residues in (2.53) since the K_i residues are determined from $R_{M,N}(z)$ alone whereas to evaluate (2.53) requires the residues of $V(z/t)R_{M,N}(z)$. Hence from (2.52-2.54) the time domain waveform can be approximated by

$$\hat{v}(t) = -\frac{1}{t} \sum_{i=1}^N K_i V(z_i/t) \quad (2.55)$$

which is the basic inversion formula. Real time functions can exploit the fact that the poles z_i come in complex conjugate pairs reducing (2.55) to

$$\hat{v}(t) = -\frac{1}{t} \sum_{i=1}^{N'} \text{Re} \{ K'_i V(z_i/t) \} \quad (2.56)$$

where $N' = N/2$ and $K'_i = 2K_i$ when N is even and $N' = (N+1)/2$ when N is odd. Also, when N is odd $K'_i = K_i$ for the residue corresponding to the real pole.

At the end of Section 2.3.1, it was mentioned that in SPICE-type simulators the waveforms had to be evaluated sequentially at each time point. On the other hand NILT-based simulations do not. From (2.56) it is apparent that there are no restrictions on t and that $v(t)$ may be evaluated at any time t without a knowledge of the values of $v(t)$ at some previous time. Having said this, NILT is not without its disadvantages. Experience has shown that for lumped RLC-type circuits, at least five pole-pairs are required to approximate e^z with sufficient accuracy. This means that for every time point at which $v(t)$ is to be determined, (2.46) will have to be solved five times requiring five LU decompositions of the matrix $sC_m + G_m$. Another disadvantage is that the Taylor series expansion to which the Pade approximation is set equal is an expansion about $z = 0$. Consequently as t increases, so does z due to (2.48) implying that as time increases, the Pade approximation for e^z becomes less and less accurate.

2.2.3 AWE Simulators

Like SPICE-type and NILT-based simulation, AWE [Pil89], [CN94] solves the system of equations found in (2.35). Unlike NILT, AWE has been modified using complex frequency hopping (CFH) [Chi94] to be compatible with non-linear components. The advantage of AWE is that it models any given circuit based only on the dominant poles in the circuit. As a result, it is often at least two orders of magnitude faster than a SPICE-type simulator. Rearrangement of (2.35) results in expression of the system in terms of the well-known state-space formulation

$$\dot{\mathbf{x}} = \tilde{\mathbf{A}}\mathbf{x} + \tilde{\mathbf{B}}\mathbf{e} \quad (2.57)$$

where $\mathbf{e}$ is the excitation vector. The first step in solving (2.57) is to determine the homogeneous solution which can be found by solving

$$\dot{\mathbf{x}}_h = \tilde{\mathbf{A}}\mathbf{x}_h \quad (2.58)$$

Subsequent application of the Laplace transform to (2.58) gives rise to

$$\mathbf{X}_h(s) = [s\mathbf{U} - \tilde{\mathbf{A}}]^{-1} \mathbf{x}_h(0) \quad (2.59)$$

where $\mathbf{U}$ is the unit matrix of rank equal to $\text{rank}(\tilde{\mathbf{A}})$. If $\mathbf{X}_h(s)$ is expanded in a Maclaurin series the result is

$$\mathbf{X}_h(s) = -\tilde{\mathbf{A}}^{-1} \left(\sum_{n=0}^{\infty} \tilde{\mathbf{A}}^{-n} s^n \right) \mathbf{x}_h(0) \quad (2.60)$$

This means that for the j^{th} component of $\mathbf{X}_h(s)$, the moments in (2.60) can be expressed as

$$[m_r]_j = \left[-\tilde{\mathbf{A}}^{-(r+1)} \mathbf{x}_h(0) \right]_j \quad (2.61)$$

where the initial conditions specify that $[m_{-1}]_j = [-\mathbf{x}_h(0)]_j$.

If it is determined that the Maclaurin series representation in (2.60) yields sufficient accuracy when truncated after the first $2q-1$ terms (moments), then $[\mathbf{X}_h(s)]_j$ can be approximately represented by

$$\hat{X}_j(s) = \sum_{i=1}^q \frac{k_i}{s-p_i} = -\sum_{i=1}^q \frac{k_i/p_i}{1-s/p_i} \quad (2.62)$$

where p_i represents each of the q approximate poles and k_i represents each of the q approximate residues. The corresponding approximate time-domain function is given by

$$\hat{x}_j(t) = \sum_{i=1}^q k_i e^{p_i t} \quad (2.63)$$

If each of the terms in (2.62) is expanded in a series about the origin and then equated to the moments in (2.61), the result is the following set of non-linear equations

$$\begin{aligned} -\sum_{i=1}^q k_i &= [m_{-1}]_i \\ -\sum_{i=1}^q \frac{k_i}{p_i} &= [m_0]_i \\ -\sum_{i=1}^q \frac{k_i}{p_i^2} &= [m_1]_i \\ &\dots \\ -\sum_{i=1}^q \frac{k_i}{p_i^{2q-1}} &= [m_{2q-1}]_i \end{aligned} \quad (2.64)$$

Note that each of the equations in (2.64) has q non-zero terms and there are $2q$ equations. This is required because both k_i and p_i are unknown so there are in fact $2q$ equations in $2q$ unknowns.

The non-linear system in (2.64) could well be solved using an iterative process. However, there are disadvantages in terms of speed-of-convergence. Rather than attempting this, it is possible to transform (2.64) and find k_i and p_i directly. If (2.64) is considered to be two systems with one consisting of the first q equations and the second consisting of the remaining q equations, these can be written as

$$-\mathbf{v}\mathbf{k} = [\mathbf{m}_{low}]_j \quad (2.65)$$

and

$$-\mathbf{v}\Lambda^q\mathbf{k} = [\mathbf{m}_{high}]_j \quad (2.66)$$

where $\mathbf{v}$ is a Vandermonde matrix of the form

$$\mathbf{v} = \begin{bmatrix} 1 & 1 & \dots & 1 \\ \frac{1}{p_1} & \frac{1}{p_2} & \dots & \frac{1}{p_q} \\ \dots & \dots & \dots & \dots \\ \frac{1}{p_1^{q-1}} & \frac{1}{p_2^{q-1}} & \dots & \frac{1}{p_q^{q-1}} \end{bmatrix}, \quad (2.67)$$

$\mathbf{k}$ is the vector of q unknown residues, $\mathbf{m}_{low}$ represents the low-order moments, i.e. the moments $\mathbf{m}_{-1}$ through $\mathbf{m}_{q-2}$, $\mathbf{m}_{high}$ represents the high-order moments and Λ is a diagonal matrix given by

$$\Lambda = \begin{bmatrix} \frac{1}{p_1} & 0 & \dots & 0 \\ 0 & \frac{1}{p_2} & \dots & 0 \\ \dots & \dots & \dots & \dots \\ 0 & 0 & \dots & \frac{1}{p_q} \end{bmatrix} \quad (2.68)$$

Therefore, the substitution of $\mathbf{k} = -\mathbf{v}^{-1}\mathbf{m}_{low}$ from (2.65) into (2.66) yields

$$\mathbf{v} \Lambda^q \mathbf{v}^{-1} \mathbf{m}_{low} = \mathbf{m}_{high} \quad (2.69)$$

The Vandermonde matrix is the modal matrix for a companion form matrix and as such makes (2.69) equivalent to

$$\mathbf{A}_c^{-q} \mathbf{m}_{low} = \mathbf{m}_{high} \quad (2.70)$$

where

$$\mathbf{A}_c^{-1} = \begin{bmatrix} 0 & 1 & 0 & \dots & 0 \\ 0 & 0 & 1 & \dots & 0 \\ \dots & \dots & \dots & \dots & \dots \\ -a_0 & -a_1 & -a_2 & \dots & -a_{q-1} \end{bmatrix} \quad (2.71)$$

with the coefficients $a_0, a_1, \dots, a_{q-1}$ normalized such that $a_q = 1$. From (2.71), the following set of linear equations is derived

$$\begin{bmatrix} m_{-1} & m_0 & \dots & m_{q-2} \\ m_0 & m_1 & \dots & m_{q-1} \\ \dots & \dots & \dots & \dots \\ m_{q-2} & m_{q-1} & \dots & m_{2q-3} \end{bmatrix} \begin{bmatrix} -a_0 \\ -a_1 \\ \dots \\ -a_{2q-2} \end{bmatrix} = \begin{bmatrix} m_{q-1} \\ m_q \\ \dots \\ m_{2q-2} \end{bmatrix} \quad (2.72)$$

Now the characteristic polynomial equation

$$a_0 + a_1 p^{-1} + a_2 p^{-2} + \dots + a_{q-1} p^{-q+1} + p^{-q} = 0 \quad (2.73)$$

can be formed whose roots are the reciprocals of the desired poles. With this information, the q desired residues in k can be found by solving (2.65). It should be noted that due to the nature of (2.62), $\hat{X}_h(s)$ is assumed to have unique poles. If this is not the case, (2.62) can be rewritten to account for the repeated poles.

A serious problem can arise through the use of AWE as described since there is no way to predetermine the accuracy of the approximation. For example, if the generated moments are matched at $s = 0$, the frequency response will be accurate at DC but errors may grow unacceptably as $s \rightarrow \infty$. If matched at both $s = 0$ and $s = \infty$ accuracy will be good in those regions but unacceptable for some intermediate frequency band. To counter this problem an extension of AWE called complex frequency hopping (CFH) [Chi94], [CN94] can be used. In this method, as many complex frequency expansion points in the entire frequency band, $0 \leq s \leq \infty$, are used as necessary. Sufficient accuracy is deemed to have been realized when the same poles are found in adjoining neighborhoods. This process is illustrated in Figure 2.9.

Figure 2.9: Complex frequency hopping (CFH)

Fundamentally, the process captured in Figure 2.9, results from rewriting (2.59) such that the expansion is about the complex frequency $s = \alpha + j\beta$ rather than about $s = 0$ resulting in

$$X_h(s) = [(s - \alpha - j\beta)U - \tilde{A}]^{-1} x_h(0) \quad (2.74)$$

In this case the residues $\hat{k}$, from each hop are determined from

$$\begin{bmatrix} \hat{p}_1^{-L-2} & \hat{p}_2^{-L-2} & \dots & \hat{p}_q^{-L-2} \\ \hat{p}_1^{-L-3} & \hat{p}_2^{-L-3} & \dots & \hat{p}_q^{-L-3} \\ \dots & \dots & \dots & \dots \\ \hat{p}_1^{-L-M-1} & \hat{p}_1^{-L-M-1} & \dots & \hat{p}_1^{-L-M-1} \end{bmatrix} \begin{bmatrix} \hat{k}_1 \\ \hat{k}_2 \\ \dots \\ \hat{k}_q \end{bmatrix} = - \begin{bmatrix} m_{L+1} \\ m_{L+2} \\ \dots \\ m_{L+M} \end{bmatrix} \quad (2.75)$$

where the poles from each hop arise from

$$\lim_{L \rightarrow \infty} Q_{[L/M]}(s) \rightarrow \prod_{j=1}^M \left(1 - \frac{s}{p_j}\right) \quad (2.76)$$

and $Q_{[L/M]}(s)$ is the denominator polynomial of the Pade approximant.

2.3 Application-specific methods

In addition to the methodologies suitable for incorporation in CAD systems, there is another body of work which may be classified as specific solutions to the ground noise problem. In such methods [DeB87], [And89], [GV91], [DeF93], [DGK93], [KNS88] ground noise is reduced or eliminated within the scope of the specific application. In [And89], for example, ground noise is reduced at the silicon level by adjusting the response characteristics of various drivers with the result that the effective number of drivers switching simultaneously is reduced. In [KNS88] the CMOS output stage is divided into two parallel pairs of transistors; one large and one small. The small pair switches first to cause the initial transition in the output state. The larger pair having been delayed then switches thus spreading what would otherwise be a large simultaneous switching current over a longer period of time. Conversely, the method discussed in [GV91] uses a control algorithm to ensure that no more than a given number of output drivers in a given location switch simultaneously. In most of the application specific methods for reducing ground noise, it is the di/dt part of (1.2) which is reduced. Unfortunately, if the solution to the ground noise problem is to be general enough for incorporation into a CAD system, this kind of application specific solution cannot, by definition, be adequate.

Probably the greatest single piece of evidence that there is a need for a systematic optimization of ground noise at the PCB level is provided in [Col91]. This article tells the

story of a minicomputer company which did not properly address the ground noise problem with which it was afflicted. By the time the problem was recognized, it was so deeply imbedded that there was little that could be done. As a result the company sustained irretrievable financial loss and was forced out of business. At the very least the methods proposed in this thesis emphasize to the reader the likely magnitude of ground noise in PCB based electronic systems.

2.4 Comment on existing methods

In the introduction it was mentioned that ground noise is dependent on a number of factors. These factors are addressed in the literature to a lesser or greater extent, depending on the particular occurrence of ground noise. One aspect of the approaches taken which seems common to all is that characterization accuracy is of prime importance and no expense is to be spared to attain it. Certainly, the more accurate the ground structure characterization, the more accurate the subsequently simulated ground noise. The fact is that most commercially available software for R, L and C characterization is designed to maximize the characterization accuracy. To accomplish this, many innovative methods using finite differences time domain (FDTD), finite elements method (FEM), or method of moments (MOM) in 2 and 3D are available. However, such accuracy comes only at considerable cost. In fact in [Shi91], it is stated that to take full advantage of the (FDTD) techniques proposed in that paper, significant advances in computing technology would have to be made. At the time of writing, a super computer was considered essential for that method. While it is acknowledged that such limitations in no way cast doubt on the method or its usefulness, they do indicate that for objective function evaluation within an optimization process, another approach is required.

In Sections 2.1 and 2.2 current trends in characterization and simulation were discussed in terms of some specific examples. The work presented in [SP94], [SNP93], [KTW93] as well as many others represents state-of-the-art methods in interconnect characterization.

Some of these methods can characterize an entire PCB interconnect in terms of inductive and capacitive parasitics in several hundred CPU seconds. Such time may be justified if the objective is to accurately simulate ground noise in a structure which is now fixed. However, if the structure changes as it would in an optimization process, then this kind of time cost may still be prohibitive since it would still be of the order of several CPU weeks, if not months. In addition, the time cost of simulating a highly accurately characterized structure can also be very significant if SPICE-type or even NILT-based simulation is used. Significant gains can be made through the employment of AWE and in particular CFH. However, even here, large-scale interconnect may require tens or hundreds of CPU seconds. The process described in this thesis allows relaxation of accuracy of characterization so that optimization is possible. In fact two levels of optimization are proposed. The first is at the IC package level where the assignment of signals and grounds to leadframe tracks is optimized for ground noise performance. The second occurs at the board level where the placement of chips on the board is optimized to yield a placement configuration exhibiting a minimum of ground noise. At each level, an accurate simulation as would be provided by SPICE, NILT or CFH is still required to provide cost function evaluation. However, using the method developed in this thesis, this process would only have to be carried out once. In this case a NILT-based process was used due to its availability and relative ease of incorporation into the existing source-code. However, CFH would in all likelihood yield superior performance.

Chapter 3

Package-level ground noise estimation

In the introduction it was mentioned that the problem of optimizing a PCP for ground noise would be broken up into two parts: package and board level optimization which of course require their own specific modeling and simulation techniques. In any optimization process, the objective function of some variables $f(\Phi)$ changes as Φ , the set of variable values changes. In this case $f(\Phi)$ is the ground noise at the IC packaging and PCB levels and it will therefore be necessary to optimize at each of these levels. At the package level it is the pattern of signal and ground assignment to the physical pins which is being optimized; at the PCB level, the actual package placement is optimized. Hence, given the two optimization problems, it is necessary to set up two objective functions and the means for their evaluation. In both cases the function evaluations derive from circuit simulations which are specifically suited to estimating the values of voltage and current in circuits. Before any simulations can be carried out, the circuit in which the ground noise occurs must be characterized for the parasitic R, L, and C parameters mentioned in previous chapters. It is highly desirable if not crucial that the characterization and estimation processes be of as short a duration as possible. For this reason the notion of model/simulation approaches is introduced. The first approach accounts for parameters such as driver resistance and interconnect capacitance and is solvable by simultaneous linear differential equations. The second approach accounts for the inductance matrix L and simulations are carried out by

solving a real matrix equation closely related to (3.1).

As mentioned above, in order to obtain a ground noise estimate, characterization and simulation of the interconnect are required. In this chapter, these two topics are discussed with regard to the contribution IC-packaging makes to ground noise.

3.1 Characterization of IC-packaging interconnect

At the package level there can be significant interaction among lead frame traces due to a high degree of inductive coupling i.e. mutual inductance. In this way the voltage across any one inductance is dependent on currents in all the other inductances. Hence for an entire package (1.1) becomes a matrix equation.

$$[V] = [L] \frac{d}{dt}[i] \quad (3.1)$$

Initially, it was assumed that to determine the ground noise due to IC packages, they would have to be characterized in as much detail, and as accurately as possible. To be of maximum value, the methods described in this thesis should be applied as early in the design cycle as possible. Therefore, while the on-chip driver and package leadframe could be modeled in detail, the board level tracks, vias, connectors and ground planes, etc. could not be because they were not yet known. Therefore, the decision was made to ignore all but the driver and package and place ideal sources at the inputs to the package for the purpose of determining worst case ground noise performance. Figure 3.1 shows the initial circuit to be used for package level ground noise estimates and is referred to as the full model of the driver/package circuit. In Figure 3.1, CMOS transistors are shown but any active device could have been used. CMOS was chosen to exemplify the problem due to its widespread use and because ground noise in CMOS circuits is becoming a serious problem [SP94], [Ott88].

Figure 3.1: Full model

For the purpose of ground noise determination it is important to understand that the ideal sources represent the sources of current which would flow back toward the driver when the driver switched from high to low-state. Furthermore, it is the high-to-low transition which typically produces worst case ground noise due to the lower on-state resistance of N-channel devices employed as "pull-downs" in output drivers. As is pointed out in [DeF93], the down-line structures (board-level transmission lines, receivers, etc.) are not as important in determining the maximum rate-of-change of current as the dynamic impedance of the driver output transistors. However, as discussed in Chapter 2, there is a severe CPU time

cost to be paid during simulation if non-linear models must be employed. Therefore, the non-linear transistor models will be replaced by their minimum on-state impedance. This will ensure that maximum current will be drawn resulting in worst-case ground noise. By linearizing the drivers, we arrive at what will be henceforth referred to as the Approach 1 model of the IC package interconnect. This model is shown in Figure 3.2

Figure 3.2: Approach 1 model

Note that the power supply line is actually shorted to ground. This is because the power supply can be considered to be an ideal voltage source which is a short circuit as far as transient voltages are concerned. Furthermore, power line noise is usually reduced by the presence of large decoupling capacitors connected between power and ground. In Figure 3.1, the $1\mu\text{F}$ decoupling capacitor is effectively a short circuit for frequencies above a few megahertz.

The decision to use LCL T-sections to model the leadframe tracks was made primarily for

two reasons. First, fully distributed transmission lines often cause convergence problems during simulation leading to significantly increased CPU time when their lengths are as short as those found in IC packages. Secondly, the first resonance point (quarter wavelength frequency) is given by

$$f = \frac{c}{\lambda \sqrt{\epsilon_r}} \quad (3.2)$$

where c is the speed of light in a vacuum and λ is wavelength. Therefore, structures of approximately 2cm in length (typical of large IC packages) have first resonances of about 1GHz (assuming $\epsilon_r = 10$, typical of ceramic packages). Moreover, since any resonant harmonic higher than this is irrelevant for signals in this kind of packaging, a second order LCL T-section is sufficient to model the leadframe.

The model of the circuit to be simulated has already been shown in Figure 3.2. However, the major task of determining the R, L, and C values to be used in the simulation section remains. There are basically two kinds of characterization required, depending on whether the leadframe consists of purely filamentary tracks for signals and grounds alike or a combination of tracks for signals and planes for ground return. The two characterization methods are now dealt with in detail.

3.1.1 Filamentary leadframe

Most IC packaging consists of a set of coplanar leadframe tracks such as the quad flat pack (QFP) example shown in Figure 3.3.

Figure 3.3: Standard QFP leadframe

In such packages, signals and ground references are carried from the chip to the PCB on which the package is mounted via metal leadframe tracks. The tracks themselves range in length from several millimeters to a few centimeters. At the same time, the maximum cross-sectional areas (at the outside of the package) are of the order of 10^{-8}m^2 . Because the tracks are so much longer than each of their cross section dimensions they can be considered filaments. Most importantly, filaments exhibit negligible variation in current density over their cross sections and hence lend themselves to parasitic characterization using closed form expressions. In this thesis, the self inductance of each track and the mutual inductance between every pair of tracks is determined using such a closed form technique [Rai84]. Such an assembly of inductances is referred to as the leadframe inductance matrix L

$$L = \begin{bmatrix} L_{11} & L_{12} & \dots & L_{1N} \\ L_{21} & L_{22} & \dots & L_{2N} \\ \dots & \dots & \dots & \dots \\ L_{N1} & L_{N2} & \dots & L_{NN} \end{bmatrix} \quad (3.3)$$

The L matrix in (3.3) is the mathematical representation of the inductance in an N -pin package where each L_{ii} represents the self inductance of the i^{th} lead and each L_{ij} , $i \neq j$ represents the mutual inductance between the i^{th} and j^{th} leads in the leadframe. Details of the inductance calculations are given in Appendix A.

Independent of the method used to determine the inductance matrix, the capacitive parasitics are determined using (3.7) as will now be shown. In the vast majority of IC packages, the leadframe is surrounded by homogeneous packaging material such as plastic or ceramic, etc. Furthermore, these materials usually possess relative dielectric constants less than 10 making the inductive parasitics dominant. It is reasonable to treat the tracks as filaments in a homogeneous medium. Consequently, it is valid to apply the telegrapher's form of Maxwell's equations to solve for the transmission line properties of the leadframe; namely that from

$$\frac{d^2 V}{dx^2} = ZYV \quad (3.4a)$$

$$\frac{d^2 I}{dx^2} = ZYI \quad (3.4b)$$

the solution is

$$V = V_1 e^{j\omega t + x\sqrt{ZY}} + V_2 e^{j\omega t - x\sqrt{ZY}} \quad (3.5a)$$

$$I = V_1 \sqrt{\frac{Y}{Z}} e^{j\omega t + x\sqrt{ZY}} - V_2 \sqrt{\frac{Y}{Z}} e^{j\omega t - x\sqrt{ZY}} \quad (3.5b)$$

where $Z = R + sL$, $Y = G + sC$ and V_1 and V_2 are constants determined by the initial conditions. From (3.5) the phase velocity is given by

$$v = \frac{\omega}{\text{Im}(\sqrt{ZY})} = \frac{1}{\sqrt{LC}} \quad (3.6)$$

if $R \ll sL$ and $G \ll sC$ as would be the case for such structures. This means that if L and C are not single values but matrices then

$$LC = \frac{1}{c^2} I \quad (3.7)$$

where I is the unit matrix and c is the speed of light in a vacuum. The parasitic capacitance matrix C may be determined by inversion of (3.7) and the application of

$$C_r = \epsilon_r C \quad (3.8)$$

where ϵ_r is the relative dielectric constant and C_r is the matrix of capacitances which would occur given the dielectric medium. It is important to note that when (3.7) and (3.8) are solved, the values they yield are per unit length.

There is a one-to-one correspondence between the inductances of (3.3) and the inductors shown in Figures 3.1 and 3.2 and each self inductance makes a contribution to the system MNA matrix as shown in Figure 3.4

$$\begin{array}{c} \begin{array}{cc} i & j & I_{n+1} \end{array} \\ \begin{array}{c} i \\ j \\ I_{n+1} \end{array} \left[\begin{array}{ccc} & & \\ & & \\ & & \\ \hline 1 & -1 & -Ls \end{array} \right] \end{array}$$

Figure 3.4: The MNA matrix stamp for a single inductor

where i and j represent the nodes to which the inductor's terminals connect and I_{n+1} represents an augmentation of the system MNA by one row and one column (the current through the inductor becomes another matrix variable). Furthermore, due to (3.1), the inductances calculated will later be directly applied to the MNA matrix $Y_r + sY_i$ in (3.25) since the

stamp or contribution made to the MNA matrix by an inductor is given by the submatrix shown in Figure 3.4. The same is not true of the capacitances determined using (3.7) and (3.8). This is due to the process by which line-to-line capacitances must be determined. Consider Figure 3.5.

Figure 3.5: Line-to-line charge distribution and voltage

If the n conductors are considered filaments into the page then from the fact that for one conductor

$$Q = CV \quad (3.9)$$

it can be stated that for n conductors

$$Q_1 = C_{11}V_1 + C_{12}V_{12} + \dots + C_{1n}V_{1n}$$

$$Q_2 = C_{22}V_2 + C_{12}V_{21} + \dots + C_{2n}V_{2n} \quad (3.10)$$

...

$$Q_n = C_{nn}V_n + \dots + C_{2n}V_{n2} + C_{1n}V_{n1}$$

and since

$$V_{12} = V_1 - V_2$$

$$\begin{aligned} & \dots \\ V_{2n} &= V_2 - V_n \\ V_{1n} &= V_1 - V_n \end{aligned} \tag{3.11}$$

the substitutions can be made to yield

$$\begin{bmatrix} Q_1 \\ Q_2 \\ \dots \\ Q_n \end{bmatrix} = \begin{bmatrix} \sum_{i=1}^n C_{1i} & -C_{12} & \dots & -C_{1n} \\ -C_{21} & \sum_{i=1}^n C_{2i} & \dots & -C_{2n} \\ \dots & \dots & \dots & \dots \\ -C_{n1} & -C_{n2} & \dots & \sum_{i=1}^n C_{ni} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ \dots \\ V_n \end{bmatrix} \tag{3.12}$$

Once the C-matrix has been determined from (3.8) the circuit capacitances derive from (3.12) for C_{ij} according to

$$C_{ij} = -\hat{C}_{ij} \tag{3.13}$$

and from

$$C_{ii} = \hat{C}_{ii} - \sum_{k=1, k \neq i}^n \hat{C}_{ik} \tag{3.14}$$

for the diagonal (self) capacitances where $\hat{C}_{ij}$ refers to an element of the C-matrix given in (3.12).

Using (3.7) and (3.8) and the fact that the filamentary structures being considered support quasi-transverse electromagnetic (TEM) waveform propagation, the C-matrix can

be determined if the L-matrix is known. However, the quasi-TEM assumption provides a means by which the C-matrix can be calculated directly. Calculation of the capacitances in the C-matrix is possible using several numerical methods such as FEM, BEM and MOM. In this thesis, FEM is the method used to solve the Laplace equation

$$\nabla^2\phi = 0. \quad (3.15)$$

From this it is possible to determine the electric field E using

$$E = -\nabla\phi. \quad (3.16)$$

The quasi-TEM assumption also constrains the dielectric medium to have a constant relative dielectric value ϵ_r for the region in which the conductors are immersed (see Figure 3.5). The energy stored in a 2-D electric field is given by

$$W = \frac{1}{2} \epsilon_o \epsilon_r \int_S |E|^2 ds. \quad (3.17)$$

Furthermore, the energy stored in a capacitor is given by

$$W = \frac{1}{2} CV^2. \quad (3.18)$$

To calculate the self capacitance of each conductor in Figure 3.5, each conductor is in turn set to a nominal voltage and (3.17) and (3.18) are employed to determine C_{ii} . FEM can be utilized to calculate each C_{ii} by setting the voltage on the conductor in question to a nominal non-zero value, V_n . The Dirichlet boundary conditions dictate that any FEM nodes on the n^{th} conductor have the value V_n and the ground conductor has a Dirichlet value of 0.0V. This process would be carried out for each conductor. To determine the line-to-line capacitances, a similar process is used except that the Dirichlet values are

assigned to the two conductors for which the line-to-line capacitance is required. For example, to obtain C_{ij} , $i \neq j$, all FEM nodes connected to the i^{th} conductor would be set equal to V_i and all nodes connected to the j th conductor would carry a Dirichlet value of V_j with $V_i \neq V_j$. In Chapter 5 a similar approach is developed to determine the inductance matrix using FEM.

Using the previous development, filamentary leadframes can be characterized for L and C parasitics which can then be used in an MNA system of equations to solve for the ground noise. However if the ground return paths are not filaments, but entire planes, a different approach is necessary.

3.1.2 Planar interconnect

A recent development in high-speed packaging is an increase in the use of planes to carry the ground reference. Often, the package has two layers of metal interconnect; one the standard leadframe, as shown in Figure 3.3, to carry the signals and the other, a solid metal plane to carry ground.

Figure 3.6: Planar package ground

As shown in Figure 3.6, the chip's ground reference will be connected at many locations

on the chip to the plane at points referred to as current sources. When the IC is operating, current will then flow from sources to sinks and the current density profile across the plane may well be highly non-uniform and geometry dependent. At first glance, it appears that proper characterization of the source-to-sink pathways will require some fairly rigorous 2 or 3D numerical electromagnetic methods. However, this turns out to be unnecessary. As is shown in [Sco90] for signals with frequencies above 30MHz, there is tight coupling between signal and return path. In fact, the coupling is so tight that the filamentary signal track which would appear in the leadframe layer close above the plane shown in Figure 3.6, induces the return current to flow almost exactly beneath it in the plane. For this reason, the plane can be modelled as a leadframe identical to that carrying the signal currents. Structures in which the signal tracks reference ground from a single ground plane directly beneath the plane of signals are referred to as microstrips. If the package has more than one plane such that each signal layer is sandwiched between two planes, called a stripline structure, two identical leadframes are added to the signal leadframe model. If the package houses a microstrip then the inductance matrix appears as

$$L = \begin{bmatrix} L_s & M \\ M & L_s \end{bmatrix} \quad (3.19)$$

where L_s is the leadframe inductance matrix as calculated in Appendix A, and M is a matrix of mutual inductances which are calculated in a similar manner. If the package houses a stripline structure, the inductance matrix is given by

$$L = \begin{bmatrix} L_s & M_p & M_1 \\ M_p & L_s & M_2 \\ M_1 & M_2 & L_s \end{bmatrix} \quad (3.20)$$

where M_p is a matrix of mutual inductances between the “strips” of current induced into each plane and M_1 and M_2 are matrices of mutual inductances between the filaments in the

leadframe and the “strips” of current in the planes. If the filaments are located exactly halfway between two planes then $M_1 = M_2$.

Figure 3.7 shows how a package leadframe carrying only signals and a ground plane just below it can be modeled as two parallel leadframes.

Figure 3.7: Microstrip structure and equivalent circuit

The leadframe matrix (the signal tracks alone, not the ground return) for the equivalent circuit shown in Figure 3.7(b) would be given by

$$\mathbf{L}_s = \begin{bmatrix} L_{11} & L_{12} \\ L_{21} & L_{22} \end{bmatrix} \quad (3.21)$$

Due to the tight coupling between the leadframe and ground the ground return inductances are considered identical to the leadframe inductances so that the ground return inductance matrix is given by

$$\mathbf{L}_g = \begin{bmatrix} L_{33} & L_{34} \\ L_{43} & L_{44} \end{bmatrix} \quad (3.22)$$

In general there also exists mutual inductance between ground return inductance and signal track inductance giving rise to the matrix in (3.23) according to (3.19).

$$L = \begin{bmatrix} L_{11} & L_{12} & L_{13} & L_{14} \\ L_{21} & L_{22} & L_{23} & L_{24} \\ L_{31} & L_{32} & L_{33} & L_{34} \\ L_{41} & L_{42} & L_{43} & L_{44} \end{bmatrix} = \begin{bmatrix} L_s & M \\ M & L_g \end{bmatrix} \quad (3.23)$$

If the leadframe has a ground plane above *and* below, each signal track in the leadframe defines a stripline structure. The inductance model for a stripline structure is analogous to that for the microstrip and leads to the matrix representation given in (3.20).

3.2 Simulation of IC-packaging interconnect

As indicated in Figure 3.1, ground noise is developed across the LCL T-section connected to ground at the board. Additional ground T-sections would connect in parallel with the grounded one shown. Neglecting the impedance of the chip ground ring is not considered a problem since this kind of impedance tends to isolate different grounds, reducing the effective mutual inductance. Due to the small geometries, it is expected to play a small role. Using the full model, simulation amounts to solving a set of simultaneous non-linear differential equations of the form

$$Y_R v(t) + Y_I \frac{d}{dt} v(t) + \chi(t) = i(t) \quad (3.24)$$

where Y_R represents time-independent components, Y_I represents time-dependent compo-

nents and $\chi(t)$ is a vector of non-linear functions specified by the transistor models. Equation (3.24) is a MNA matrix [HRB75] representation.

Due to the non-linear nature of the driver models, too much CPU time would be required in the simulation to allow optimization of large packages (>200 IO). A comparative example is given later in this chapter which bears out this fact. In order to remove this impediment it was decided to replace the transistor models with the driver's minimum on-state resistance since maximum ground noise would occur when currents were maximized and hence when resistances were minimized. Figure 3.2 shows how the circuit to be simulated appears with the driver transistors replaced by their minimum on-state resistances. In going from the full model of Figure 3.1 to the Approach 1 model of Figure 3.2, it is expected that no significant errors in the peak value of the ground noise will result. An example showing the expected error level is presented at the end of this chapter.

Removal of the non-linear components translates into a simplification of (3.24). Now the system of equations relating to currents and voltages may be written in the frequency domain as the following MNA equation

$$[Y_R + sY_I] V(s) = I(s) \quad (3.25)$$

To formulate the nodal equations for each track circuit model as shown in Figure 3.2, consider the lumped element representation of a single leadframe track shown in Figure 3.8.

Figure 3.8: Generic leadframe track with source resistance

$$V_k - V_{k+1} - s \sum_{i=1}^N [L_{k(2i-1)} I_{2i-1} + L_{k(2i)} I_{2i}] = 0 \quad (3.26)$$

$$V_{k+1} - V_{k+2} - s \sum_{i=1}^N [L_{(k+1)(2i-1)} I_{2i-1} + L_{(k+1)(2i)} I_{2i}] = 0 \quad (3.27)$$

$$(V_{k+2} - V_{k+3}) G_k - I_{k+1} = 0 \quad (3.28)$$

$$I_{k+1} - I_k + V_{k+1} C_{kk} s + s \sum_{i=1}^N (V_{k+1} - V_{4i-2}) C_{ki} = 0 \quad (3.29)$$

$$\{V_k = 0 | k \in \text{groundnode}\} \quad (3.30)$$

$$\{I_k = I_{E_k}, V_k = V_{E_k} | k \in \text{sourcenode}\} \quad (3.31a,b)$$

where E indicates association with an ideal voltage source and

$$k = 4m - 3, m = 1, 2, \dots, N \quad (3.32)$$

where N is the number of pins. From these, a set of generalized frequency domain equations can be written in MNA form according to (3.24). In general, Y_R and Y_I are of order N_y and

$$N_y = 3N_s + 3N + K \quad (3.33)$$

where N_s is the number of signal tracks and K is the number of separate ground references in the package. Note that each signal pin will contribute (3.26 through 3.29 and 3.31a,b) for a total of six equations while each ground pin contributes (3.26, 3.27 and 3.29) to the

generalized MNA matrix in (3.24). The sum of these two quantities and the fact that the number of ground pins, $N_g = N - N_s$ gives rise to (3.33).

Substantial CPU time savings will be realized using (3.25) instead of (3.24) because of the elimination of the need to use iterative numerical techniques for the solution of non-linear differential equations. However, since the goal is to estimate the peak ground noise voltage in the time domain (3.25) must be converted to the time domain. In this case, the conversion will be accomplished using numerical inversion of the Laplace transform (NILT) [VS83], [SVN76]. In fact simulation in Approach 1 amounts to solving (3.25) in the time-domain via NILT the details of which were covered in Chapter 2. Equation (2.58) yields an approximation of the actual time domain waveform $v(t)$ and becomes more accurate as N' increases. For the purpose of this thesis, $N' = 5$ was found sufficient. However, this indicates that for an Approach 1 simulation with 10 time points, (3.25) must be solved 50 times. For large packages with upwards of 200 leadframe traces, the MNA will be of rank > 850 containing upwards of 160 000 self and mutual inductances and upwards of 40 000 self and coupling capacitances. Even though linear, it was found that the required CPU time will not be insignificant. Hence, for optimization, Approach 1 does not appear to be sufficiently fast, illuminating the need for a yet faster model/simulation approach [Wil96].

3.3 Simplified modeling and simulation

As indicated in Section 3.2, the Approach 1 simulations are still likely to be too CPU intensive to support the optimization of large packages. To further increase the speed of simulation, it was decided to reduce the circuit being simulated from that shown in Figure 3.2 to that given in Figure 3.9. This simplification is referred to as Approach 2 at the package level.

Figure 3.9: Approach 2 model

In going to this simpler circuit, there are two differences in the model. First, the interconnect capacitance has been neglected. Tests so far indicate that for $\epsilon_r < 10$, the inductive parasitics are strongly dominant so neglecting the capacitance has resulted in errors $< 5\%$ for peak ground noise voltage. Secondly, the source resistances have been replaced by short circuits. Such a move would render an MNA matrix approach unworkable since removing all resistance may lead to a singularity even in linear systems. In addition, simply removing the driver resistances would cause inaccuracies arising from the fact that the driver resistance plays a critical role in determining the rates-of-change of the currents flowing in the leadframe. Here then arises the need for developing the two approaches. From Approach 1, by-products of the more accurate ground noise simulation are the maximum di/dt values for the currents flowing from the ideal sources. By providing these values to Approach 2 the resistors may be ignored resulting in an inductance matrix equation the solution of which contains the peak ground noise values. Moreover, once Approach 1 has been invoked just a single time and the maximum di/dt values determined, the optimizer can be driven by a multitude of calls to the much faster Approach 2 ground noise simulation. For this reason, the full model approach to simulation is abandoned in favour of a simple method based on (3.1). If the voltage across every inductance in Figure 3.9 were known, then the equation

$$L\dot{I} = V \quad (3.34)$$

where $\dot{I} = \frac{d}{dt}I$ could be solved. However, the voltage across all the inductors to ground is precisely the value sought. Furthermore, the $\dot{I}$ values for conductors connected to sources are precisely the di/dt values obtained from Approach 1. Therefore, if KCL is invoked at the V_g node (see Figure 3.9) the additional equation

$$\sum_{k=1}^{Gr} \dot{I}_k = - \sum_{m=Gr+1}^N \dot{I}_m \quad (3.35)$$

becomes available. Through rearranging (3.34) such that only known quantities appear on the RHS, it is possible to write a new equation of the form of (3.34)

$$\begin{bmatrix} L_{11} & L_{12} & \dots & L_{1Gr} & -1 \\ L_{21} & L_{22} & \dots & L_{2Gr} & -1 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ L_{Gr1} & L_{Gr2} & \dots & L_{GrGr} & -1 \\ 1 & 1 & \dots & 1 & 0 \end{bmatrix} \begin{bmatrix} -\dot{I}_1 \\ -\dot{I}_2 \\ \vdots \\ -\dot{I}_{Gr} \\ V_g \end{bmatrix} = \begin{bmatrix} \sum_{i=Gr+1}^N L_{1i} \dot{I}_i \\ \sum_{i=Gr+1}^N L_{2i} \dot{I}_i \\ \vdots \\ \sum_{i=Gr+1}^N L_{Gri} \dot{I}_i \\ - \sum_{i=Gr+1}^N \dot{I}_i \end{bmatrix} \quad (3.36)$$

where each L_{ij} $1 \leq i, j \leq Gr$ represents a self or mutual inductance of ground conductors, N is the total number of leadframe tracks and Gr is the number of ground tracks.

It is often the case in modern highspeed packaging that more than a single ground reference is required. For example, in IC's with large output drivers, it may be advantageous to separate the ground reference of the output drivers from that of the internal logic. In such cases, the designer confines the ground noise from the output

drivers to a “dirty” ground reference enabling the logic ground to remain “clean”. In such a scheme, ground noise due to the self inductance of the leadframe for the dirty ground is isolated from the clean ground because there is no physical connection. However, there still exists mutual inductance which provides a route for the dirty ground noise to invade the clean ground. This effect is accounted for by making a simple modification to (3.36) which amounts to applying KCL at each separate ground reference node. In general (3.36) becomes

$$\begin{bmatrix} \mathbf{L} & -\mathbf{U} \\ \mathbf{U}^T & \mathbf{0} \end{bmatrix} \begin{bmatrix} \mathbf{I}_g \\ \mathbf{V}_g \end{bmatrix} = \begin{bmatrix} \sum \mathbf{LI} \\ \sum \mathbf{I} \end{bmatrix} \quad (3.37)$$

where, as before, $\mathbf{L}$ is the ground conductor inductance matrix. The matrix $\mathbf{U}$ is a binary selector matrix such that the appropriate ground reference $\mathbf{V}_g$ is selected and $\mathbf{U}^T$ is the transpose of $\mathbf{U}$ and as such accounts for KCL being carried out at each separate ground reference. Hence in general $\mathbf{U}$ and $\mathbf{U}^T$ are not square and $\mathbf{U}$ has a column order equal to the number of separate ground references. Finally, $\mathbf{0}$ represents a square matrix of 0's. As an example, we wish to estimate ground noise in a six pin package which had two separate grounds, one with two ground pins fed from two signals and the other with a single ground and signal pin, we would set up the following system of equations

$$\begin{bmatrix} L_{11} & L_{12} & L_{13} & -1 & 0 \\ L_{21} & L_{22} & L_{23} & -1 & 0 \\ L_{31} & L_{32} & L_{33} & 0 & -1 \\ 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ V_{g1} \\ V_{g2} \end{bmatrix} = \begin{bmatrix} \sum_{i=Gr+1}^N L_{1i} I_i \\ \sum_{i=Gr+1}^N L_{2i} I_i \\ \sum_{i=Gr+1}^N L_{3i} I_i \\ -s_1 \\ -s_2 \end{bmatrix} \quad (3.38)$$

where $Gr = 3$ since there are three ground pins and $s_1 = di_4/dt + di_5/dt$. In addition, the last term in the right-hand-side vector is given by $s_2 = di_4/dt$.

Thus, construction and solution of (3.36) replaces the netlister and simulator required in Approach 1. Furthermore, whereas solution of (3.25) involves a complex Y -matrix formulation where Y is of rank $3N_s + 3N + K$ and a subsequent time domain conversion via NILT, solution of (3.36) is a real algebraic process of the form $\tilde{A}\mathbf{x} = \mathbf{b}$ where $\tilde{A}$ is of rank $N - N_s + K$. The matrix of (3.25) is about 25% full as opposed to almost 100% full for $\tilde{A}$ in (3.36). However, for a 1:1 ratio of signal to ground pins, the rank of Y is about 7 times that of $\tilde{A}$. This factor increases roughly linearly with signal to ground pin ratio such that for a 4:1 ratio, the rank of Y is 27 times the rank of $\tilde{A}$. Furthermore, as mentioned previously, use of NILT to obtain the peak ground noise voltage requires that (3.25) be solved about 50 times.

Most of the gains made in performance in choosing Approach 2 over Approach 1 are due to the fact that because the interconnect model was simpler, the simulation could be made much simpler. However, even though extraction of R, L, and C parasitics has been reduced to L alone, there is nothing suggested by the method which simplifies the L extraction process. Approach 2 will use the methods outlined in Approach 1 for obtaining the actual L-matrix values.

3.4 Numerical results

Figures 3.1, 3.2 and 3.9 show the full model, Approach 1 model and Approach 2 model representations of the package shown in Figure 3.10. The full model driver models are from a Motorola 88K CMOS microprocessor chip. The driver resistors used in Approach 1 are 25Ω (the on-state resistance of the 88K output stage). The package is a 28mm body size QFP with eight pins. The leadframe tracks have an average spacing of 9.8mm and an average width of 0.254mm. The leadframe thickness is 0.127mm. In addition, the source waveform for the six signal pins is a step input with 0 to 100% risetime of 4ns. After the 4ns, the

input voltage remains constant at 3.5V. Pins 2 and 4 through 8 carry the signals while ground was connected to pins 1 and 3.

Figure 3.10: 8-pin quad package

Figure 3.11 shows the time-domain waveforms for the full model and for Approach 1 based on the package in Figure 3.10. Approach 2 gives only a peak value and this is indicated as the constant flat line. The closeness in value of the full model peak voltage, the Approach 1 peak voltage and the Approach 2 voltage indicates the validity of the simplifying assumptions resulting in the model being reduced from the full model to the Approach 2 model. On the other hand, Table 3.1 compares the relative cost to obtain each of the three curves in Figure 3.11. Approach 2 is 7000 times faster than simulation with the full non-linear model and nearly 200 times faster than Approach 1. Obviously Approach 2 is the method to use recursively in optimization.

In fact, the simplifying assumptions result in a loss of information concerning the higher harmonics in the ground noise waveform and of phase information. In a study of signal integrity in digital systems the shape and phase characteristics may be of supreme importance and in such cases the CPU intensive methods of [SP94], [HHS92], [KTW93], [SNP93], [SC92], [MB92] must be used. However, for ground noise optimization, consideration of only the peak value constitutes a safer approach. It is possible to design a digital system with the threat of ground noise controlled by ensuring that the data is clocked when the ground noise is at a minimum i.e. it is known where in time the ground noise occurs hence phase information is part of the ground noise evaluation. However, the sensitivity of

such designs to manufacturing and component tolerances make this approach quite risky, at least for the present.

Figure 3.11: Full model, Approach 1 and Approach 2 peak value comparison

Table 3.1: Full model comparison

	Full Model	Approach 1	Approach 2
Peak V_g (V)	0.82541	0.81722	0.79454
Error	-	-0.99%	-3.74%
CPU time(s)	152.3	3.8	<0.02

Chapter 4

Package level ground noise minimization

Up to this point the method for evaluating ground noise at the IC package level has been discussed. In this chapter, we look at how this evaluation can be used in an optimization process to provide IC package pin assignments which minimize the observed ground noise. Since there is little interaction between package and board level parasitics due to the relative distances involved, it is assumed that package optimization may take place first and independently of the board-level optimization.

4.1 Formulation of the optimization process

An objective function f to be minimized and a set of variables whose domain of values are mapped via f to a range of function values needs to be defined. In this case, f is defined to be a measure of the ground noise voltage V_g and is a function of the assignment of signals and grounds to the pins $\Phi_1, \Phi_2, \dots, \Phi_N$ where N is the number of pins in the package. An unconnected pin is considered a signal pin with the derivative with respect to time of the leadframe current, $di/dt = 0.0$. Once an assignment of signals and grounds to all pins has been made this assignment configuration is denoted Φ_j representing the j^{th} configuration

and is one of $(N-1)!$ possible assignment configurations. (It is $(N-1)!$ and not $N!$ because the pins are positioned around the periphery of a closed loop.) Symbolically, ground noise being a function of pin assignment is represented by

$$V_g = V_g(\Phi_j) \quad (4.1)$$

where $\Phi_j \in \mathcal{S}^N$, $\Phi_j(i) \in \{1, 2, \dots, N\}$, $\Phi_j(i) \neq \Phi_j(k)$ and $\Phi_j(i)$ defines the assigned location of the i^{th} pin. For the purpose of optimization it is useful to develop V_g as a function of pin configuration Φ_j . However, V_g is, in addition, a circuit theory parameter and as such is more directly a function of the self and mutual inductance, L_s and M , due to the package lead-frame tracks. Furthermore, the inductance is ultimately a function of the geometry, $\mathcal{G}$ of the lead-frame tracks. Therefore, although it is unimportant as far as optimization is concerned *per se*, the functional link between the circuit theory evaluation of the cost function and the optimization process can be related by

$$V_g = V_g(\Phi_j) = V_g(\Phi_j, L_s, M) = V_g(\Phi_j, L_s(\mathcal{G}), M(\mathcal{G})) \quad (4.2)$$

To formulate the ground noise cost function, an index set J_{total} is defined representing all possible assignments of signal and ground status to the leadframe tracks. In addition, there may be K multiple separate ground references in the package. For example a package with two ground references would have $K = 2$. In this case, V_g will be a vector of dimension K which contains the values of ground noise corresponding to each ground reference. For the k^{th} separate ground selected from this set, an upper ground noise specification, v_{u_k} , a lower ground noise specification v_{l_k} and a weighting factor w_k are defined respectively. Let $v_k(\Phi_j)$ be the ground noise voltage produced by the j^{th} configuration on the k^{th} separate ground. The normalized upper and lower error functions for the k^{th} separate ground are defined as [BZ88]:

$$e_{U_k}(\Phi_j) = w_k \left(\frac{v_k(\Phi_j) - v_{U_k}}{v_{U_k} - v_{L_k}} \right) \quad (4.3a)$$

$$e_{L_k}(\Phi_j) = w_k \left(\frac{v_k(\Phi_j) - v_{L_k}}{v_{U_k} - v_{L_k}} \right) \quad (4.3b)$$

where $j \in J_{total}$ and $v_{U_k} > v_{L_k}$. It is reasonable to want to assign the lower ground noise specification a zero value. However, this may not be realistic so (4.3) is left in its more general form. If the package in question has a single ground ($K = 1$) to which all signals are referenced (as is usually the case) then the optimization process is successful as soon as a configuration yielding a ground noise between the specification limits is found. However, if $K > 1$ we need to optimize an array of ground noise values; one for each separate ground reference. Let $F^e(\Phi_j)$ be defined as a vector combining the upper and lower error functions for the ground noise corresponding to assignment Φ_j :

$$F^e(\Phi_j) = \begin{bmatrix} e_{U_1} \\ e_{U_2} \\ \dots \\ e_{U_K} \\ -e_{L_1} \\ -e_{L_2} \\ \dots \\ -e_{L_K} \end{bmatrix} \quad (4.4)$$

The error functions violating their specifications are positive and since it is only these which we need to consider, we define the index set ζ by

$$\zeta = \{n | F_n^e > 0\} \quad (4.5)$$

where F_n^e represents each vector entry in (4.4). In general, the cost function is defined by an inner one-sided l_p formula given by

$$f = \left[\sum_{n \in \zeta} \left(F_n^e \right)^p \right]^{1/p} \quad (4.6)$$

By letting $p \rightarrow \infty$ in (4.6) the cost function value becomes the largest of the error functions. In other words the cost function value will be the ground reference noise value which violates its specification to the greatest extent. Hence, the optimization process becomes a minimax process.

Given an N pin package, there are $(N-1)!$ ways of assigning the signals and grounds to the pins. The implication is that with N variables and $(N-1)!$ possible states it will be virtually impossible to find the objective function minimum deterministically. This also implies that as the optimization process proceeds, it will be difficult to distinguish the desired global minimum value from incidental local minima. When the digital computer was still in its infancy, the similarity between statistical mechanics and combinatorial optimization was recognized. In particular, it was realized that the simulation of systems with many degrees of freedom, a system of interacting particles, for example, was now feasible [OG89]. In statistical mechanics, the problem was one of determining the state equation for models that could not be mathematically analyzed. Specifically, the energy of particles which interact by forces inversely proportional to their separation and constrained to some arbitrary boundary was sought. The simulation proceeded by selecting a particle at random and perturbing its current state at random. If the energy of this new state was lower than the current state, the perturbed new state was accepted. However, even if the new state had an energy higher by d joules than the current state, it would be accepted over the current state with probability

$$P = e^{-\frac{d}{kT}} \quad (4.7)$$

where T is temperature in degrees Kelvin and k is Boltzmann's constant. This perturbation, energy evaluation and comparison step is referred to as a *metropolis step* and continues until some arbitrary condition is met. Normally, several perturbations occur before T is allowed to decrease and such a collection of steps is called a *metropolis loop*. This method of generating current states led to a distribution of states in which the probability of a state with energy E_i being the current state is given by

$$P_{E_i} = \frac{e^{-E_i/kT}}{\sum_{j=1}^N e^{-E_j/kT}} \quad (4.8)$$

The probability function in (4.8) is known as the Boltzmann density. A useful characteristic of (4.8) is that at initially high temperature, each state has virtually the same chance as every other state of being the current state. As the temperature decreases in subsequent metropolis loops, only low energy states have a high probability of being the current state. It is this temperature dependence which allows simulated annealing to proceed past local minima.

Simulated annealing [KGV83], [Rut89] was chosen as the optimization engine because it lends itself well to situations where the cost function is a function of discrete valued variables due to its similarity to the laws governing statistical mechanics. During the optimization process a set of values for the N variables is selected at random. Let the cost function of this set of values be f_n and let the function of the previous set be f_{n-1} . If $f_n < f_{n-1}$ then the current set of variables will replace the previous set since it produces a better result. However, even if $f_n > f_{n-1}$, the current set may still be accepted. In this case a random number R between 0 and 1 is generated and compared with P where P is calculated from

$$P = P_0 e^{-D/T} \quad (4.9)$$

where P_0 is a constant, $D = |f_n - f_{n-1}|$ and T is a resolution parameter similar to temperature in real annealing [KGV83]. If $R < P$ then the current set of variable values is accepted even though it did not give rise to a lower cost function. As the optimization process continues the value of T is gradually reduced making the acceptance of an inferior result less and less likely. In this manner simulated annealing can progress beyond local minima.

4.2 Package-level optimization results

As a simple illustrative example, a 12 pin QFP is used to compare the ground noise determined using Approach 1 and that obtained when the di/dt 's from Approach 1 are used in Approach 2. Figure 4.1 shows the geometry and pin numbering of the 12-pin package to be optimized. In this case, the design is to consist of 8 signals and 4 grounds. Initially, the grounds are assigned to pins 9 through 12. After the initial assignment has been simulated and the signal di/dt 's and V_g calculated, the di/dt 's are used in Approach 2. Based on these di/dt values,

Figure 4.1: 12-pin quad package

Approach 2 is used to evaluate the cost function during the optimization process. Table 4.1 shows the ground noise arising from the initial and final (optimized) pin assignments as determined by both Approaches 1 and 2. The eight sources involved in simulation with Approach 1 were composed of 3.5V step inputs with a 4ns risetime.

Table 4.1: Approach 1 vs. Approach 2 for V_g

	Initial V_g (V)	Optimized V_g (V)
Approach 1	1.6888	1.3860
Approach 2	1.6358	1.3652
Error	-3.14%	-1.50%

Table 4.2 contains the di/dt data for the initial and optimized pin assignments. Figure 4.2 shows the ground noise waveforms arising from Approach 1 before and after optimization. A reoptimization of the optimized pin assignment produced no further changes in the optimum pin assignment.

Table 4.2: Initial vs. optimized pin assignment

Pin #	Initial di/dt (A/s)	Optimized di/dt (A/s)
1	8.00e+07	11.31e+07
2	7.40e+07	ground
3	7.14e+07	11.31e+07
4	6.69e+07	11.31e+07
5	6.70e+07	ground
6	6.93e+07	11.31e+07
7	8.67e+07	11.31e+07
8	9.95e+07	ground
9	ground	11.31e+07
10	ground	11.31e+07
11	ground	ground
12	ground	11.31e+07

Figure 4.2: Ground noise before and after optimization of 12-pin QFP

As mentioned in Chapter 3, an important aspect of the proposed method is the determination of the source di/dt values using Approach 1 and their subsequent use by Approach 2 in the optimization process. Table 4.2 shows the before- and after-optimization pin configurations for the 12-pin package seen in Figure 4.2. In addition, the di/dt values for the currents passing through each signal pin are given before and after optimization. From Table 4.2 it is apparent that the optimized pin configuration in addition to providing the minimum ground noise level has also resulted in uniform and higher di/dt values. The reason for this elevation in value is that the optimized configuration exhibits minimal inductive impedance due to the mutual inductive effects. As a result of lower impedance, the di/dt 's increase. Interestingly, if the initial di/dt values and optimized pin assignment are used in Approach 2, the ground noise value is about 0.95V which does not agree with the peak voltage value of about 1.38V observed in Figure 4.2. Agreement is obtained if the *optimized* di/dt values are used in Approach 2. This means that the initial di/dt values are accurate for the initial objective function evaluations but as optimization progresses, since the di/dt val-

ues are not up-dated, these evaluations become less and less accurate. However, since the optimized configuration depends only on the relative merit of a configuration these inaccuracies do not prevent the optimum configuration being found. Two facts support this conclusion. First, optimization tests with widely differing di/dt values with an order of magnitude separating the smallest from the largest did not prevent the optimizer from finding the optimum configuration. Secondly, reoptimization using the optimized di/dt 's and pin assignment resulted in either the same pin assignment or different ones with similar ground noise performance. A useful "sanity" check is to calculate the spread (standard deviation) of the optimized di/dt 's. The optimized values should have less spread than the initial values. Finally, to return an accurate value of the optimized ground noise once the optimized assignment is known, the Approach 1 should be rerun once more.

The 12-pin package was useful for illustrating the method, but is of little practical value. For this purpose a 208-pin QFP is selected. The 208-pin QFP to be optimized features 86 high-speed signals with $di/dt = 3.5e+06A/s$, 62 low-speed signals with $di/dt = 1.8e+06A/s$, 4 very high-speed clocks with $di/dt = 7.0e+06$ and 56 grounds. The initial pin assignment had pins 1-86 carrying the high-speed signals, pins 87-148 carrying the low-speed signals, pins 149-152 carrying the clocks and the remainder carrying ground.

Table 4.3: 208-pin QFP optimization results

Parameter	Value
Signal types	86 lines, $di/dt = 3.5e+06A/s$ 62 lines, $di/dt = 1.8e+06A/s$ 4 phase clk, $di/dt = 7.0e+06A/s$ 56 grounds
Initial V_g	1.16302V
Optimized V_g	0.043158V
Real CPU time (SPARC10)	1197.4sec
Factor by which ground noise has decreased	26.95
Re-optimized V_g	0.043158V

Table 4.3 displays the results of optimizing a 208-pin QFP using the proposed process and Table 4.4 shows the optimized pin assignment.

Table 4.4: Optimized pin assignment for 208-pin package

Signal type	Pin assignments
High-speed $di/dt=3.5e+06A/s$	2, 3, 6, 7, 9, 10, 11, 14, 16, 17, 19, 21-23, 26, 29, 30, 32, 33, 37, 38, 41, 42, 43, 47, 49, 56, 59-61, 63, 64, 66, 67, 70, 73, 74, 78, 79, 81, 84, 87, 93, 95, 98, 97, 105-107, 109, 114, 116, 118, 119, 124, 126, 128, 129, 132, 133, 136, 140, 141, 143, 144, 146, 149, 152, 155, 157, 160, 162, 164, 169, 170, 172, 178, 182, 185, 186, 189, 191, 198, 202, 204, 208
Lowspeed $di/dt=1.8e+06A/s$	4, 12, 13, 15, 25, 27, 28, 31, 35, 39, 45, 46, 50, 51-54, 62, 69, 71, 75, 80, 82, 88, 89, 90, 92, 99, 101, 102, 104, 110, 111, 120-123, 130, 134, 138, 139, 147, 148, 151, 156, 161, 165, 166, 171, 173, 174, 177, 179, 181, 183, 184, 188, 193, 194, 196, 197, 201
Clocks $di/dt=7.0e+06A/s$	85, 112, 135, 206
Grounds	1, 5, 8, 18, 20, 24, 34, 36, 40, 44, 48, 55, 57, 58, 65, 68, 72, 76, 77, 83, 86, 91, 94, 96, 100, 103, 108, 113, 115, 117, 125, 127, 131, 137, 142, 145, 150, 153, 154, 159, 158, 163, 167, 168, 175, 176, 180, 187, 190, 192, 195, 199, 200, 203, 205, 207

Admittedly, the initial configuration represents a poor choice of signal-to-pin assignment. A more informed initial configuration would assign grounds to the shorter pins so that self inductance is minimized and alternate the ground pins with signal pins to take advantage of the mutual inductance. Such an intelligent configuration is shown in Table 4.5 and the optimization results are shown in Tables 4.6 and 4.7 respectively.

Table 4.5: 208-pin QFP intelligent initial configuration

Signal type	Pin assignments
High-speed $di/dt=3.5e+06A/s$	9-13, 15, 17, 19, 21, 23, 25, 29, 31, 33, 35, 37, 39, 41-44, 60-65, 67, 69, 71, 73, 75, 77, 81, 83, 85, 87, 89, 91, 93-96, 113-116, 118, 120, 122, 124, 126, 128, 132, 134, 136, 138, 140, 142, 144-148, 164-168, 170, 172, 174, 176, 178, 180, 182, 184, 186, 188, 190, 192, 194, 196-200
Lowspeed $di/dt=1.8e+06A/s$	1-8, 45-59, 97-112, 149-163, 201-208
Clocks $di/dt=7.0e+06A/s$	27, 79, 130, 182
Grounds	14, 16, 18, 20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40, 66, 68, 70, 72, 74, 76, 78, 80, 82, 84, 86, 88, 90, 92, 117, 119, 121, 123, 125, 127, 129, 131, 133, 135, 137, 139, 141, 143, 169, 171, 173, 175, 177, 179, 181, 183, 185, 187, 189, 191, 193, 195

Table 4.6: 208-pin QFP optimization results given intelligent initial configuration

Parameter	Value
Signal types	86 lines, $di/dt = 3.5e+06A/s$ 62 lines, $di/dt = 1.8e+06A/s$ 4 phase clk, $di/dt = 7.0e+06A/s$ 56 grounds
Initial V_g	0.095786V
Optimized V_g	0.043418V
Real CPU time (SPARC10)	1275.4sec
Factor by which ground noise has decreased	2.206

Table 4.7: Optimized assignment for 208-pin QFP from intelligent initial config.

Signal type	Pin assignments
High-speed $di/dt=3.5e+06A/s$	3, 8-10, 13, 14, 17, 19, 20, 25, 27, 28, 31, 34, 41, 43-45, 47, 49, 55, 56, 61-63, 69, 72, 79-81, 83, 84, 87-92, 96, 98, 99, 103, 104, 107, 110, 111, 114, 115, 120, 129-131, 133, 134, 136, 138-141, 143-145, 147, 148, 151, 154, 156, 158-160, 166, 168-170, 173, 176, 177, 183, 185, 191, 195, 197, 198, 202-205
Lowspeed $di/dt=1.8e+06A/s$	2, 4, 5, 11, 12, 16, 23, 29, 30, 32, 35-39, 50, 51, 57-59, 65, 71, 75, 78, 85, 94, 95, 97, 101, 106, 109, 112, 116, 118, 119, 122, 124, 125, 127, 132, 135, 149, 152, 157, 162, 164, 165, 172, 175, 178, 180, 181, 186, 187, 189, 190, 194, 200, 201, 205, 207, 208
Clocks $di/dt=7.0e+06A/s$	21, 66, 121, 171
Grounds	1, 6, 7, 15, 18, 22, 24, 26, 33, 40, 42, 46, 48, 52-54, 60, 64, 67, 68, 70, 73, 74, 76, 77, 82, 86, 93, 100, 102, 105, 108, 113, 117, 123, 126, 128, 137, 142, 146, 150, 153, 155, 161, 163, 167, 174, 179, 182, 184, 188, 192, 193, 196, 199, 206

The results in Table 4.6 indicate that even with an informed initial pin assignment, the optimization process is able to find a pin assignment configuration with less than half the ground noise. Furthermore, this improvement does not derive from any obvious pattern, as indicated by the optimized configuration shown in Table 4.7.

Chapter 5

PCB-level ground noise estimation

5.1 Sources of ground noise in PCP's

In Chapter 3, methods for estimating ground noise due to the IC package were discussed. However, in practice, signals are driven through one IC package onto a PCB and through one or more receiver packages before the signal arrives at its destination IC(s). The entire circuit then consists of IC and PCB interconnect structures for both the signals themselves and the ground return currents shown in Figure 5.1. The switching noise current I_{SN} and the power supply surge current I_{PS} are important because they give rise to two different ways in which ground noise can occur. Furthermore, methods used to predict the ground noise resulting therefrom are necessarily very different. If the time derivative of I_{SN} denoted $\dot{I}_{SN}$ is dominant, as is usually the case, a voltage between points a and b, V_{ab} (see Figure 5.1) will be developed due largely to the inductance in the ground return portion of the loop carrying I_{SN} . While the switching driver would probably not suffer any deleterious effects from this voltage, a neighboring quiet driver in the same IC sharing essentially the same ground return could be induced to trigger falsely. This becomes increasingly likely the larger the number of drivers switching simultaneously.

Figure 5.1: Interconnect showing IC package and PCB components.

Using the CMOS illustration again, neighboring quiet drivers in the low-state have their N-channel pull-down transistors "on" in a low-impedance state. In this case V_{ab} could even propagate back down the quiet driver's interconnect and cause false inputs to any receivers which happen to be connected there. On the other hand, if I_{PS} is dominant, a voltage between points a and c, V_{ac} is likewise developed. Although developed due to a different set of circumstances, the resulting potential ground noise problem is the same as for ground noise due to I_{SN} . Hence the two different methods, depending on whether I_{SN} or I_{PS} is dominant, differ largely in how the inductance in the ground return pathway is determined. For I_{SN} that pathway is filamentary, for I_{PS} it is a plane. The ramifications of these two models were discussed in Chapter 3.

5.2 I_{SN} dominant

Most output drivers consist of a two-transistor totem pole output stage where the two different output states are achieved by mutually exclusively switching the two transistors. The examples cited will be of this configuration but the methods apply to active devices such as ECL since all that is required to produce I_{SN} induced ground noise is a charged interconnect (transmission line) connected to a low-impedance driver. In CMOS drivers, for example, the electron mobility is much higher than hole mobility so that in the on-state, the N-channel devices are much less resistive than their P-channel counterparts. Consequently, high-to-low state transitions result in higher current levels due to the lower device resistance in devices which have not been geometrically scaled to equalize this imbalance. Typically worst case ground noise occurs at high-to-low transitions. Therefore, to predict this worst-case ground noise, it is necessary to adequately characterize all ground return structures. In Chapter 3, the leadframe inductances, L_f (see Figure 5.1) were determined. The task now is to determine the inductances L_s and L_g in the PCB part of the signal and return paths respectively.

5.2.1 Characterization of PCB-level interconnect

At the package level, Approach 1 is based on the model shown in Figure 3.2. If the board-level parasitics are taken into account the resulting configuration is shown in Figure 5.2. Note that since the worst-case ground noise occurs during high-to-low transitions, only the N-channel transistor is on in the CMOS case, the P-channel is off and represents a virtually infinite impedance. Therefore, in Figure 5.2 the entire totem pole output stage of the driver is replaced by the N-channel on-state resistance. Non-CMOS devices would simply have their non-linear on-state impedance replaced by the minimum value for that technology. This is analogous to the process carried out for the package-level interconnect in which the full non-linear model was replaced by the linear Approach 1 model. In addition, although

not shown, each of the sections labelled either LEADFRAME or BOARD contain mutual inductance and coupling capacitance which mutually couple all paths internal to each respective section.

Figure 5.2: Approach 1 model when I_{SN} dominant

In Section 3.1.1, extraction of parasitic inductance from the filamentary leadframe was discussed. Then, in Section 3.1.2, planar interconnect was covered. This treatment of the IC package with leadframe above ground plane is substantially similar to tracks above a ground plane at the PCB level. For this reason, the track inductance will be similarly determined using the method discussed in Appendix A. In addition, since the tight coupling between signal track and ground is present at the PCB level also, the PCB ground will be thought of as filamentary current conduits. However, in Section 3.1.1, the package leadframe tracks were modeled as T-sections with two inductors and a capacitor and all the associated mutual inductances and coupling capacitances. At the PCB level,

this may be inadequate due to the much greater distances covered by the PCB tracks. Typically, to conduct a signal integrity analysis involving PCB tracks of more than a few centimetres in length, transmission line models are used. True transmission line models are not practical in this case because they involve either an absolute ground reference which does not exist (see Figure 5.3) or are necessarily very CPU time intensive to simulate. For this reason, lumped LC sections will be used to extend Approach 1 modelling and simulation to the PCB level. To do this amounts to appropriately adding the extra L and C components to the MNA matrix formulation. In fact, now $Y_r + Y_i$ will have to account for both driver and receiver package leadframes as well as the PCB track/ground LC sections.

(a) True T-line track model with ground reference

(b) Lumped element model with parasitic ground

Figure 5.3: True T-line and lumped element track models

After having made the decision to represent the interconnect at the PCB-level using the lumped model in Figure 5.3(b), the question of how many LC-sections to use in the model naturally arises. In signal integrity analysis there is usually a trade-off: more sections lead to better accuracy at the expense of CPU time and the risk of numerical non-convergence,

fewer sections simulate more quickly but with less accuracy. For the purpose of this thesis, the latter side of the trade-off is chosen. This is because speed of simulation is of primary importance. In addition, as mentioned in the introduction, the actual wave-shape is of little concern when the objective is to minimize the maximum occurring ground noise.

At the package-level the parasitic capacitance was ignored due to the dominance of the inductive parasitics. At the PCB-level, it is not obvious that this assumption is valid. If not, the worst case occurs if the capacitive effects would augment the estimated ground noise by causing the circuit to be under-damped. If that is the case, the interconnect structure is correctly modeled as a transmission-line. However, because the ground return path parasitics, in particular the inductance, are central to this thesis, the transmission-line model would have to include them. The usual perfect-ground-reference model as shown in Figure 5.3(a) is not sufficient. Furthermore, inclusion of an appropriate distributed transmission-line model with ground path parasitic impedances would add significantly to the CPU time required to estimate the ground noise. Therefore, the distributed transmission-line model will be replaced by an equivalent second order lumped model.

Figure 5.4: Distributed (a) and lumped inductive (b) interconnect models

In Figure 5.4(a) the inductors shown represent the effective signal and ground lead inductances for the receiver and driver packages. They are connected via a distributed transmission line model which assumes inductive and capacitive parasitics in both the signal and ground paths. In Figure 5.4(b) L_s represents the total inductance in the PCB-level signal path and L_g represents the total inductance in the PCB-level ground path. In both (a) and

(b) R represents the on-state driver output resistance. If the circuit in Figure 5.4(b) is to compensate for the transmission line effects in Figure 5.4(a) the time-domain equations governing voltage for each case will have to be found. An even simpler approach is to replace the transmission line in Figure 5.4(a) with the appropriate LC-section such that the peak ground noise value for the two circuits is the same. This intermediate circuit is shown in Figure 5.5.

Figure 5.5: Transmission-line-equivalent LC-section circuit

In general, the parameters in Figures 5.4(b) and 5.5 can be found by optimization such that their responses best approximate the original transmission line network model of Figure 5.4(a). Here a much simpler and faster analytical solution is derived effectively reducing the transmission line from a multi-pole to a two-pole model.

In order to make the peak ground noise in Figures 5.4(a) and 5.5 the same consider the ABCD parameter matrix, also called the T-matrix, representation for a distributed lossless transmission line

$$T_{tl} = \begin{bmatrix} \cos\left(\frac{\omega D \sqrt{\epsilon_r}}{c}\right) & jZ_0 \sin\left(\frac{\omega D \sqrt{\epsilon_r}}{c}\right) \\ \frac{j \sin\left(\frac{\omega D \sqrt{\epsilon_r}}{c}\right)}{Z_0} & \cos\left(\frac{\omega D \sqrt{\epsilon_r}}{c}\right) \end{bmatrix} \quad (5.1)$$

where ω is the radian frequency, D is the length in meters, ϵ_r is the relative dielectric constant, c is the speed of light in a vacuum and Z_0 is the characteristic impedance. A simple LC section of the form shown in Figure 5.6

Figure 5.6: Simple LC-section

has the following T-matrix.

$$\mathbf{T}_{LC} = \begin{bmatrix} LCs^2 + 1 & Ls \\ Cs & 1 \end{bmatrix} \quad (5.2)$$

The upper left, or A element in the transmission matrix is the reciprocal of the voltage transfer function. Resonance occurs if $A = 0$. Hence the transmission line in (5.1) resonates when

$$\frac{\omega D \sqrt{\epsilon_r}}{c} = \frac{(2k+1)\pi}{2} \quad (5.3)$$

where $k \in \mathfrak{I}$, $k \geq 0$. The resonant frequency is therefore given by

$$\omega = \frac{(2k+1)\pi c}{2D\sqrt{\epsilon_r}} \quad (5.4)$$

In addition, it is apparent from (5.2) that the resonant frequency of the LC section is given by

$$\omega = \frac{1}{\sqrt{LC}} \quad (5.5)$$

For a distributed lossless transmission line, Z_0 is defined as

$$Z_0 = \sqrt{\frac{L_p}{C_p}} \quad (5.6)$$

where L_p and C_p are the per unit length inductance and capacitance of the transmission line. This implies that L_p and C_p are related to the L and C in (5.2) and (5.5) according to

$$L = L_p D \quad (5.7a)$$

$$C = C_p D \quad (5.7b)$$

If this restriction is applied to the L and C in (5.2), then equating (5.4) and (5.5) fixes the L and C values in (5.2) according to

$$L = \frac{2Z_0 D \sqrt{\epsilon_r}}{(2k+1)\pi c} \quad (5.8)$$

and

$$C = \frac{2D \sqrt{\epsilon_r}}{(2k+1)Z_0 \pi c} \quad (5.9)$$

The use of (5.8) and (5.9) ensures that the transmission line and LC-section represented in (5.1) and (5.2) respectively have the same resonant frequency. However, no restriction is placed on the relative magnitudes of the voltage transfer functions at resonance. It is difficult to say what the relative magnitudes are because they are each infinite at resonance. Thus we have an indeterminate condition of the form ∞/∞ . The ratio of the A-terms from

(5.1) and (5.2) likewise results in a 0/0 indeterminate condition. This problem can be resolved using l'Hopital's rule. Specifically, let

$$\frac{P_N}{P_D} = \frac{\cos\left(\frac{\omega D \sqrt{\epsilon_r}}{c}\right)}{1 - LC\omega^2} = \frac{0}{0} \quad (5.10)$$

Applying l'Hopital's rule and setting the ratio to unity results in

$$\lim_{\omega \rightarrow \omega_r} \frac{\frac{\partial P_N}{\partial \omega}}{\frac{\partial P_D}{\partial \omega}} = \frac{-\frac{D \sqrt{\epsilon_r}}{c} \sin\left(\frac{\omega D \sqrt{\epsilon_r}}{c}\right)}{-2LC\omega} = 1 \quad (5.11)$$

where ω_r is the resonant frequency. The ratio is set to unity so that the A values for the distributed and lumped circuits approach resonance at the same rate. From (5.4) and (5.5) it is apparent that (5.11) reduces to

$$\frac{D \sqrt{\epsilon_r}}{c} = 2\sqrt{LC} \quad (5.12)$$

Using (5.12) in conjunction with (5.6) results in

$$L = \frac{Z_0 D \sqrt{\epsilon_r}}{2c} \quad (5.13)$$

and

$$C = \frac{D \sqrt{\epsilon_r}}{2Z_0 c} \quad (5.14)$$

Note that because L and C result now from (5.6) and (5.12) rather than from (5.6) and equating (5.4) and (5.5) the resonant frequencies of the transmission line and LC-section are no longer equal. This is unimportant since it is the maximum magnitude of the voltage transfer functions which is of prime importance and these are rendered equal by (5.13) and (5.14).

As an example of how this latter equivalence might be used, consider the circuit in Figures 5.7(a) and (b). In these circuits the 2.98nH inductors represent the effective signal and ground pin inductances of the receiver and driver packages and R represents the driver on-state output impedance.

(a)

(b)

Figure 5.7: Transmission line and equivalent LC-section PCB-level circuits

Figures 5.8 and 5.9 compare the ground noise of the circuits in Figures 5.7(a) and 5.7(b) for $R = 5\Omega$ and 100Ω respectively.

Figure 5.8: Transmission line/LC section comparison for $R = 5\Omega$

Figure 5.9: Transmission line/LC section comparison for $R = 100\Omega$

Figures 5.8 and 5.9 derive from greatly differing on-state output impedances yet the peak ground noise predicted using the LC-section circuit is within a few percent of that present in the transmission-line circuit. Since only the greatest peak value of the ground noise is of importance, it is valid to use a lumped representation of the distributed transmission line interconnect.

5.2.2 Simulation of PCB-level interconnect

In Chapter 3 it was demonstrated that the Approach 1 simulation of the interconnect amounted to MNA matrix formulation of the linearized interconnect network according to (3.25). Simulation at the PCB-level involving two or more IC packages connected by PCB-level tracks can be accomplished by augmenting the system Y matrix. The augmented MNA matrix accounting for board-level interconnect LC-sections would have the form

$$Y_A = \begin{bmatrix} Y_1 & C_{12} & \dots & C_{1P} & U_1 \\ C_{12} & Y_2 & \dots & C_{2P} & U_2 \\ \dots & \dots & \dots & \dots & \dots \\ C_{1P} & C_{2P} & \dots & Y_P & U_P \\ U_1^T & U_2^T & \dots & U_P^T & Y_B \end{bmatrix} \quad (5.15)$$

where Y_i represents the MNA submatrix from each package, C_{ij} contains any capacitance coupling board-level tracks between the i^{th} and j^{th} packages and each matrix U_i contains either 1's or -1's and forms the board-level links between the various packages. In other words the U_i , U_i^T and Y_B matrices form the inductance stamps (see Figure 3.4) for all the board-level inductances assembled in Y_B . Moreover, Approach 1 simulation at the PCB level is tantamount to solving

$$Y_A(s) V(s) = I(s) \quad (5.16)$$

where in the application of NILT, as discussed in Chapter 3, the Laplacian variable s is replaced by z/t .

Once (5.16) has been solved, a by-product is the set of di/dt values governing the current flowing in each signal track. Unlike at the package-level, where the di/dt values represented the time rate-of-change of the source current, at the PCB-level the di/dt values for all signal (non-ground) conductors is required. It is this broader set of di/dt values which will be provided to Approach 2 for the rapid and repetitive evaluations required to optimize the positioning of the IC packages on a PCB in terms of ground noise.

5.2.3 Simplified modeling and simulation

Due to the added complexity of the model it is even more imperative at the PCB-level to maximize the characterization and simulation speed. Therefore, extensive simplification is required for the PCB-level interconnect model. Conversely, the simplification can be thought of as an extension of the simplified IC package-level model. When considering board-level inductances, the model in Approach 2 involves a simple modification to that shown in Figure 3.9 and is shown in Figure 5.10.

Figure 5.10: Approach 2 model when I_{SN} dominant

Moreover, the basic formulation as given in (3.36) and (3.37) needs to be modified to account for multiple chips and the large number of parallel board-level inductances. The required modification involves creating a super L matrix which includes the L matrices from the leadframes of all IC's on the board being considered for ground noise analysis. The super matrix takes on the form shown in (5.17).

$$L_L = \begin{bmatrix} L_{11} & 0 & \dots & 0 \\ 0 & L_{22} & \dots & 0 \\ \dots & \dots & \dots & \dots \\ 0 & 0 & \dots & L_{PP} \end{bmatrix} \quad (5.17)$$

If it is assumed that there are P packages involved in the analysis on the board then each matrix denoted L_{ii} , $i = 1, 2, \dots, P$ contains the leadframe inductance for that package. The inter-package mutual inductances are assumed to be zero since package-to-package inductive coupling will be negligible due to the distances involved. The objective of this section is to explain how the package-level and board-level inductances can be assembled mathematically so that their ground noise contributions can be accounted for simultaneously. To do this (5.17) is augmented by one more L-submatrix, L_B representing the board-level

interconnect inductances of signal tracks and ground return paths resulting in L_{AI} .

$$L_{AI} = \begin{bmatrix} L_{11} & 0 & \dots & 0 & 0 \\ 0 & L_{22} & \dots & 0 & 0 \\ \dots & \dots & \dots & \dots & \dots \\ 0 & 0 & \dots & L_{pp} & 0 \\ 0 & 0 & \dots & 0 & L_B \end{bmatrix} \quad (5.18)$$

It is important to remember that if the board-level interconnect is microstrip then L_B has the form of (3.19) and if stripline then it appears as in (3.20). In the examples to be illustrated, L_B is considered to represent a microstrip interconnect but a stripline applies equally, simply requiring some extra bookkeeping.

Finally, at the package-level the geometries involved allowed for neglecting the capacitance in both Approaches 1 and 2 as long as the relative dielectric was reasonably low (< 10). At the PCB-level, it was shown how the transmission-line capacitance could be accounted for without actually using multi-pole transmission line models. However, as shown in Chapter 3, the PCB-level Approach 2 model may remain purely inductive since the effects of both resistance and now capacitance can be incorporated into the di/dt terms.

Modeling of the simplified PCB-level interconnect has been shown as an extension of that developed for the IC package model. For Approach 1 the additional board-level LC-sections would be added linking those representing the driver and receiver packages. The MNA matrix would have increased in size but the process by which the MNA matrix equations are solved would not have changed. Similarly, the PCB-level simulation derives from an extension of the IC package simulation and involve incorporation of L_{AI} of (5.18) into a modification of (3.36) and (3.37) to yield a ground noise solution based on both package and board-level inductances.

Now that the signal di/dt values are known, (5.18) must be revisited so that each submatrix L_i is reformulated as in (3.37). Once this has been accomplished the final matrix

equation to be solved is given in (5.19)

$$\begin{bmatrix}
 L_{G1} & -U_1 & 0 & 0 & \dots & 0 & 0 & 0 & 0 \\
 U_1^T & 0 & 0 & 0 & \dots & 0 & 0 & 0 & 0 \\
 0 & 0 & L_{G2} & -U_2 & \dots & 0 & 0 & 0 & 0 \\
 0 & 0 & U_2^T & 0 & \dots & 0 & 0 & 0 & 0 \\
 \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots \\
 0 & 0 & 0 & 0 & \dots & L_{GP} & -U_P & 0 & 0 \\
 0 & 0 & 0 & 0 & \dots & U_P^T & 0 & 0 & 0 \\
 0 & 0 & 0 & 0 & \dots & 0 & 0 & L_{GB} & -U_B \\
 0 & 0 & 0 & 0 & \dots & 0 & 0 & U_B^T & 0
 \end{bmatrix}
 \begin{bmatrix}
 I_{G1} \\
 V_{G1} \\
 I_{G2} \\
 V_{G2} \\
 \dots \\
 I_{GP} \\
 V_{GP} \\
 I_{GB} \\
 V_{GB}
 \end{bmatrix}
 =
 \begin{bmatrix}
 -\sum M_1 I_{S1} \\
 -\sum I_{S1} \\
 -\sum M_2 I_{S2} \\
 -\sum I_{S2} \\
 \dots \\
 -\sum M_P I_{SP} \\
 -\sum I_{SP} \\
 -\sum M_B I_{SB} \\
 -\sum I_{SB}
 \end{bmatrix}
 \quad (5.19)$$

where L_{G1} , L_{G2} , ..., L_{GP} represent matrices which consist of the ground lead self and mutual inductances (as in (5.18)) from each chip, U_1 , U_2 , ..., U_P represent column vectors of 1's and 0's and L_{GB} and U_B are the board-level equivalents. It is important to note that it is only the values in L_{GB} and M_B which will change during optimization since these values alone are affected by the changes in relative position of the IC's. As was the case in (3.37) each U_i is in general an $r_i \times n_{Gi}$ matrix where r_i is the rank of L_{Gi} and n_{Gi} is the number of separate ground references within the package as outlined in Section 3.3. Similarly, U_B is in general an $r_B \times n_{GB}$ matrix where r_B is the rank of matrix L_{GB} and n_{GB} is the number of different board-level inductive ground-return pathways there are, each of which supports a different ground potential difference (noise). Generally, the I_{Gi} terms represent $G_i \times 1$ column vectors where G_i is the number of ground leads in the i^{th} package. Furthermore, the V_{Gi} terms represent $n_{Gi} \times 1$ column vectors. The terms in the right-hand-side vector are exactly as they were defined in Section 3.3 except that the system matrix in (5.19) contains the additional board-level terms given by $\sum M_B I_{SB}$ and $\sum I_{SB}$ but their construction corresponds exactly to their package level counterparts. Solution of (5.19) produces the ground noise voltages across each of the package ground leads and the board-level ground

return pathways. The concept of total path ground noise will now be introduced. Each complete ground return path consists of the driver package ground leads, the receiver package ground leads and the board-level ground return path connecting them. The total ground noise, V_{GT} due to any driver must therefore be the sum of these three components or

$$V_{GT} = V_{GD} + V_{GR} + V_{GB} \quad (5.20)$$

where V_{GD} corresponds to the V_{Gi} in (5.19) representing the driver package, V_{GR} corresponds to the V_{Gi} representing the receiver package and V_{GB} corresponds to the appropriate element in V_B from (5.19).

5.2.4 Comparison of Approaches 1 and 2

At this point it is worth making a comparison of (5.16) and (5.19) in order to illustrate certain advantages incorporated in the process embodied in (5.19). Assuming all signals begin and end on the same PCB, the rank of the Y_A matrix in (5.16) is given by

$$R(Y_A) = \sum_{i=1}^{P_c} (2S_i + n_{Gi} + 1) + N_L + 2N_T + N_R \quad (5.21)$$

where P_c is the package count on the PCB, $2S_i + n_{Gi} + 1$ arises from the fact that for each of the S_i signal conductors in the i^{th} package leadframe there is a node at each end, n_{Gi} (usually 1) separate ground nodes and 1 board-level ground node. In addition, N_L represents the

total number of package-level leads on the PCB since each represents an inductor which in turn creates an extra MNA unknown current (see Figure 3.4), $2N_T$ represents the total number of board level tracks (both signal and ground) again each being an inductor and N_R is the total number of receivers on the board since each receiver represents a voltage source each of which also gives rise to an unknown current. If the real coefficient ξ_g is introduced and defined as the fraction of the total number of IC package pins assigned to ground then (5.21) can be rewritten as

$$R(Y_A) \approx 2(1 - \xi_g)N_L + N_L + (1 - \xi_g)N_L + \left(\frac{1 - \xi_g}{2}\right)N_L = \left[\frac{7}{2}(1 - \xi_g) + 1\right]N_L \quad (5.22)$$

The origin of the first two terms in (5.22) is straightforward while the third term arises because the number of board-level signal tracks will be roughly equal to half the total number of signal pins (one track for each driver/receiver pair). Moreover, since there is a board-level ground return path for every signal this number must be doubled. The last term arises if there are an equal number of drivers and receivers. If there are more receivers than drivers this number would actually be higher but for comparison purposes, the minimum value is used. On the other hand the rank of the matrix in (5.19) is given by

$$R(Y) = N_G + \sum_{i=1}^{P_c} n_{Gi} + N_T + P_B \quad (5.23)$$

where N_G is the total number of ground leads on the PCB, n_{Gi} is the number of separate grounds in the i^{th} package and P_B is the total number of PCB-level separate ground return paths. By definition

$$N_G = N_L - N_S \quad (5.24)$$

where N_S is the total number of signal leads on the PCB. By applying the factor ξ_g to (5.23) $R(Y)$ can be approximately reduced to

$$R(Y) \approx \xi_g N_L + \left(\frac{1 - \xi_g}{2} \right) N_L = \left(\frac{1 + \xi_g}{2} \right) N_L \quad (5.25)$$

Realistically, no more than half the pins on a PCB could be assigned to ground due to the enormous upward pressure in modern system designs on throughput. In addition, every IC must have at least one ground pin so that the valid range of values for ξ_g cannot be outside the interval $[0, 1/2]$. Given these limits it is apparent that

$$\lim_{\xi_g \rightarrow 0} \frac{R(Y_A)}{R(Y)} \approx 9 \quad (5.26)$$

and

$$\lim_{\xi_g \rightarrow \frac{1}{2}} \frac{R(Y_A)}{R(Y)} \approx \frac{11}{3} \quad (5.27)$$

More typical would be a high-speed PCB where a third of all pins would be assigned pwr/gnd. In this case the $R(Y_A)/R(Y)$ would be about 5. Therefore, in a typical case, we would expect the matrix of (5.16) to have at least 25 times the number of elements as the matrix in (5.19).

Another novel characteristic of (5.19) is that the unknowns are the currents through branches and voltages across branches rather than the branch currents and node voltages found in a MNA matrix. This fact and the fact that there is assumed to be negligible coupling between package leadframes and between package leadframes and PCB-level tracks result in uncoupled package submatrices, L_{Gi} in matrix Y . The importance of this characteristic is that each submatrix in Y can be solved in isolation from every other

submatrix thereby realizing a further reduction in the CPU time to do the calculations. However, the uncoupled nature of the submatrices would be incomplete if not for the fact that the board-level submatrix L_B appears mathematically to be no different than the submatrices representing packages. At the package level, the submatrices are individually solvable due to the invocation of KCL at the package ground reference node, at which the package ground noise would be measured. Mathematically, this is the role of U_i^T , $1 \leq i \leq P$. At the board-level this is accomplished by the implication of U_B and U_B^T . The equations encompassed by U_B^T imply that the sum of board-level signal currents must be equal and opposite to the ground currents in the return pathways directly beneath the signal tracks. From [Sco90], it is apparent that at frequencies above 1MHz this is a reasonable assumption. To account for the effects of closely spaced signals the structure of U_B^T does not insist that each signal current be identically equal in magnitude to the return current beneath but merely that the magnitude of the sum of the signal currents be equal to the magnitude of the sum of the ground return currents for each ground return pathway. In a typical high-speed PCB, each signal layer is very close to its reference plane, usually less than 1mm away. Table 5.1 shows the ratio of signal-to-ground mutual inductance to ground path self inductance as a function of signal-to-ground separation assuming a signal conductor width of 0.1524mm (6mil) and thickness of 0.03556mm (1.4mil).

Table 5.1: Mutual inductance as a percentage of self inductance

Signal to ground spacing (mm)	$\frac{Mutual}{Self} \times 100$ (%)
1.0 (39.4mil)	65.1
0.5 (19.7mil)	77.2
0.15 (6.0mil)	98.4

The importance of the trend shown in Table 5.1 is realized when the simple circuit shown in Figure 5.11 is considered.

Figure 5.11: Typical PCB circuit with inductively coupled signal and gnd return paths

In Figure 5.11 the voltage across the parasitic ground inductance is given by

$$V_g = sL_g I_r + sM I_s \quad (5.28)$$

and since $I_r = -I_s$ it follows that

$$V_g = (L_g - M) s I_s \quad (5.29)$$

Therefore the effective ground return path inductance, L_{ge} is given by

$$L_{ge} = L_g - M \quad (5.30)$$

Together Table 5.1 and (5.29) show the likelihood that the return pathway will be carrying the total signal current. The greater the mutual inductance, M the smaller the ground path effective inductance, L_{ge} and therefore the greater the tendency for the current to flow in this path. Consequently, in a conventional circuit simulator, the ground return current is constrained only by the level of mutual inductance as characterized by an electromagnetic field solver. By constraining the ground current by the mechanism embodied in U_B^T , we are

really invoking KCL as was done at the package level except that the currents being summed in this case enter a network and not simply a node.

5.2.5 Numerical Results

To illustrate the simplified simulation at the PCB level, consider the simple two-package system illustrated in Figure 5.12

Figure 5.12: Two-chip board-level example

In this case each chip has a single ground reference so that V_{Gi} will be a single number for each chip package leadframe. From knowledge of the geometry the equations in Appendix A are used to calculate the leadframe inductances of the two chips and the board-level

inductance matrix. For this example the particular matrix equation corresponding to (5.19) is given by

$$\begin{bmatrix} 7.83 \times 10^{-9} & -1.42 \times 10^{-10} & -1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\ -1.42 \times 10^{-10} & 7.83 \times 10^{-9} & -1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\ 1.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\ 0.0 & 0.0 & 0.0 & 4.04 \times 10^{-9} & 1.44 \times 10^{-10} & -1.0 & 0.0 & 0.0 & 0.0 \\ 0.0 & 0.0 & 0.0 & 1.44 \times 10^{-10} & 4.04 \times 10^{-9} & -1.0 & 0.0 & 0.0 & 0.0 \\ 0.0 & 0.0 & 0.0 & 1.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 \\ 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 5.79 \times 10^{-8} & 2.23 \times 10^{-8} & -1.0 & 0.0 \\ 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 2.23 \times 10^{-8} & 6.74 \times 10^{-8} & -1.0 & 0.0 \\ 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 1.0 & 0.0 \end{bmatrix} \begin{bmatrix} i_1^{(1)} \\ i_2^{(1)} \\ V_{G1} \\ i_1^{(2)} \\ i_2^{(2)} \\ V_{G2} \\ i_1^G \\ i_2^G \\ V_{GB} \end{bmatrix} = \begin{bmatrix} 1.53 \times 10^{-2} \\ 1.75 \times 10^{-2} \\ -1.19 \times 10^8 \\ -1.36 \times 10^{-2} \\ -1.31 \times 10^{-2} \\ 6.36 \times 10^7 \\ -2.32 \times 10^0 \\ -2.53 \times 10^0 \\ -7.73 \times 10^7 \end{bmatrix} \quad (5.31)$$

In order to calculate the signal di/dt values using Approach 1, the voltage swing V_{sw} and risetime t_r must be given. In this example $V_{sw} = 3.5V$ and $t_r = 2ns$. Solution of (5.31) is compared in Table 5.2 with the results of simulating the circuit of Figure 5.12 using a conventional simulator

Table 5.2: Comparison of conventional simulator, NILT and Approach 2 at PCB level

	$V_g(V)$	Error(%)	CPU time(s)
Conventional simulator	1.4370	-	2.90
NILT	1.4538	1.17	0.2
Approach 2	1.4691	2.23	0.002

Note that although there are two drivers and receivers producing two separate ground pathways, each of the three components in each pathway is in parallel with the other. In fact

there is but a single ground return path.

The results in Table 5.2 are also plotted graphically in Figure 5.13

Figure 5.13: Comparison of SPICE-type, NILT and Approach 2 simulations of Figure 5.12

As an illustration of the tight coupling between signal tracks and ground plane return paths discussed in the previous section, consider the network in Figure 5.14.

Figure 5.14: Three-chip board-level interconnected network

The small network in Figure 5.14 contains two separate ground return pathways. The first consists of the inductance of the parallel ground leads in IC1 represented by $L_{11}^{(1)}$ and $L_{22}^{(1)}$, the board-level inductances represented by L_{11}^g and L_{33}^g and the inductance of the parallel ground leads in IC3 represented by $L_{11}^{(2)}$ and $L_{22}^{(2)}$. The second pathway consists of the inductance of the ground leads in IC1, the board-level inductances L_{22}^g and L_{44}^g and the inductance of the ground lead in IC2. In general, the board-level ground return path has three stages, the driver package ground lead inductances, the board-level ground return path inductances and the receiver package ground-lead inductances. The total ground path noise voltage of the i^{th} path is therefore the sum of the voltages across each stage given by

$$V_{GT}^{(i)} = V_{GD}^{(i)} + V_{GB}^{(i)} - V_{GR}^{(i)} \quad (5.32)$$

which is exactly the same equation as (5.20) except that the receiver term is negated. The last term is subtracted because the package lead ground noise is calculated with the current oriented from the inside of the package to the outside. Calculation of the voltages across each of the stages of course includes the mutual inductances internal to each of the three stages.

Tables 5.3 and 5.4 compare the ground noise calculated by a conventional circuit simulator and by the proposed method for the two ground paths in Figure 5.14. Table 5.3 reflects a track-to-ground separation, z of 1.0mm while the separation used in Table 5.4 is 0.1524mm. In addition, in both tables the voltage drop across the ground lead inductance of any package is represented by $V_p^{(i)}$ regardless of whether the package houses the driver or receiver for the ground path in question.

Table 5.3: Comparison of conventional simulator and Approach 2 for $z = 1.0\text{mm}$.

	$V_p^{(1)}$ (V)	$V_p^{(2)}$ (V)	$V_p^{(3)}$ (V)	$V_b^{(1)}$ (V)	$V_b^{(2)}$ (V)	$V_T^{(1)}$ (V)	$V_T^{(2)}$ (V)
Conventional simulator	0.30751	0.08161	-0.21516	0.82877	-0.12722	1.35144	0.09868
Approach 2	0.31251	0.08590	-0.22046	0.85331	-0.134614	1.38627	0.09199

Table 5.4: Comparison of conventional simulator and Approach 2 for $z = 0.1524\text{mm}$.

	$V_p^{(1)}$ (V)	$V_p^{(2)}$ (V)	$V_p^{(3)}$ (V)	$V_b^{(1)}$ (V)	$V_b^{(2)}$ (V)	$V_T^{(1)}$ (V)	$V_T^{(2)}$ (V)
Conventional simulator	0.47775	0.22557	-0.36739	0.14653	-0.01872	0.99167	0.23346
Approach 2	0.48265	0.23253	-0.37395	0.15145	-0.01943	1.00805	0.23069

Apparently, there is good agreement between the conventional simulator and Approach 2 for a wide range of separation, z between signal and ground return pathways. From the conventional simulator, Table 5.5 compares the amount of signal di/dt to that in the corresponding ground return path as defined in Figure 5.14.

Table 5.5: Signal & return current directly beneath found by conventional simulator.

	$i(L_{11}^s) + i(L_{33}^s)$	$i(L_{11}^g) + i(L_{33}^g)$	$i(L_{22}^s) + i(L_{44}^s)$	$i(L_{22}^g) + i(L_{44}^g)$
$z = 1.0\text{mm}$	$9.1270 \times 10^7 \text{A/s}$	$-9.1271 \times 10^7 \text{A/s}$	$8.7310 \times 10^6 \text{A/s}$	$-8.7300 \times 10^6 \text{A/s}$
$z = 0.1524\text{mm}$	$1.5609 \times 10^8 \text{A/s}$	$-1.5616 \times 10^8 \text{A/s}$	$2.6430 \times 10^7 \text{A/s}$	$-2.6429 \times 10^7 \text{A/s}$

From Table 5.5 it is apparent that for the range of z values being considered, there is sufficient mutual inductance to indeed result in the return path currents being directly beneath the signals from whence they came. This in turn validates the uncoupled matrix structure of (5.19) which leads to significant performance improvement over conventional circuit simulators.

5.3 I_{PS} dominant

In IC technology the simplest structure is an inverter consisting of a P-type transistor above an N-type transistor in a totem pole configuration. The output of such a circuit is in either a stable high or low state if the input is stable. If the output is in a stable high state, the N-type device is off and presents a virtual open circuit while the P-type device is on and presents an impedance of a few tens of ohms or less. On the other hand, the reverse is true if the output is in a stable low state; the P-type device presents a very high impedance while the N-type is on and presents an impedance of only a few ohms. In CMOS technology, the NMOS devices usually have lower on-state impedances owing to the fact that electrons have higher mobility than holes. Whenever the input state changes, a change in the output occurs and during such transitions, both P- and N- type devices may present impedances somewhere between their on and off impedances. At such a time, both transistors are said to be partially on. The surge current I_{PS} can occur if the two totem pole output stage transistors are simultaneously at least partially on. It is interesting to note that technology such as ECL does not produce much surge current I_{PS} since it is continually drawing the same

current at a constant rate. For the transistors we have tested thus far, I_{PS} has never been as serious a problem as I_{SN} . However, it is not possible to determine the precise circumstances under which an I_{PS} derived ground noise may occur. For this reason, it is necessary to develop a process to handle this possibility.

5.3.1 Characterization and simulation of PCB-level interconnect

In Section 5.2 it was shown how the interconnect characterization at the PCB level could be derived by extension of the model shown in Figure 3.2. In this section, a similar approach is taken; the only difference being that since both totem pole transistors are partially on, there are two resistances which must be taken into account. In addition, there are the PCB-level parasitics. These are all shown in Figure 5.15.

Figure 5.15: Approach 1 model with composite driver resistors and PCB parasitics

In considering Figures 5.2, 5.15 and 5.16, it is important to realize that only two of many possible I/O drivers, two of many possible signals and two each of many possible power and ground pins are shown. In Figure 5.15, due to the large decoupling capacitors commonly used in modern packaging, for high speed transistors there is virtually no difference in potential between the IC side of the power and ground pins. For this reason, Figure 5.15 may be redrawn as shown in Figure 5.16.

Figure 5.16: Approach 1 model with simple driver resistors and board parasitics

Note that in Figure 5.16, the model is identical to that of Figure 3.2 except for the board-level inductances and capacitances. Mutual inductance and coupling capacitance is accounted for among package pins. In addition, mutual inductance at the board level is also considered. However, there is no mutual inductance between board and package pins due to the relatively large distances involved. As with the I_{SN} dominant case,

augmentation of the MNA matrix amounts to the addition of the board-level inductances and capacitances this time shown in Figure 5.16.

In order to build the circuit shown in Figure 5.16 it is necessary to characterize the PCB-level inductances which in this case are all planar. In Section 5.2, it was observed that for frequencies above 1 MHz, the signal track carrying the signal and the ground plane beneath carrying the return current are very tightly coupled. The coupling is so tight that the ground return path follows the signal track almost exactly, resulting in filamentary confinement of the current in the ground return path. On the other hand, no such filamentary restriction exists for I_{PS} since it is sourced to and drained from the active drivers via conductive planes as shown in Figure 5.17

Figure 5.17: I_{PS} flowing in planes

From Figure 5.17, it is obvious that I_{PS} will cause a voltage across L_{bg} such that point d will temporarily no longer be at ground potential. An idle driver grounded to this point may well falsely trigger. Therefore, it is necessary to calculate the inductance of the planar region between points d and G .

One way to solve for inductance is to observe its relationship in the equation relating energy W and current I , namely

$$L = \frac{2W}{I^2} \quad (5.33)$$

There are many numerical techniques available which can ultimately provide L via planar energy and current. The inductance extraction process need only be carried out once and therefore need not be particularly high performance. It was decided that due to the popularity of the method a FEM approach would be taken [Zie71], [CS80], [SF93]. This method begins by solving the Laplace equation as was done in (3.15) across the surface of the 2-D ground plane structure in Figure 5.17. From Maxwell's equations it is known that electric field E is related to potential ϕ according to (3.16) and that current density J is related to the electric field from Ohm's law according to

$$J = \sigma E \quad (5.34)$$

where σ is the conductivity of the medium over which the ϕ distribution was calculated. Figure 5.18 shows the ground plane of Figure 5.17 and indicates the lines of constant current density which would likely exist.

Figure 5.18: Current density distribution between Dirichlet points.

Points d and ground are of fixed potential and are therefore referred to as Dirichlet points. Since the total current I entering (or leaving) the plane is required in (5.33) to get L , we

observe that I may be determined by integrating the current density over either contour G or contour d . In this case the current is confined to a sheet so the sheet current density variable $\mathbf{K}$ is used in (5.35)

$$I = \oint_G \mathbf{K} dG \quad (5.35)$$

If (5.33) is to be used then the energy can be calculated from

$$W = \frac{1}{2} \mu \int_S |\mathbf{H}|^2 dS \quad (5.36)$$

where S is the 2-D planar surface in question and the magnetic field $\mathbf{H}$ is determined by

$$\mathbf{H} = \frac{1}{\mu} (\nabla \times \mathbf{A}) \quad (5.37)$$

Finally, $\mathbf{A}$, the magnetic vector potential and $\mathbf{J}$ are related by

$$\mathbf{A} = \frac{\mu}{4\pi} \int_v \frac{\mathbf{J}}{r} dv \quad (5.38)$$

where v is 3-D space in general but reduces to 2-D for this problem since the current density is confined to a plane. Note that it may be necessary to compute

$$\mathbf{A} = \frac{\mu}{4\pi} \int_v \frac{\mathbf{J}_0 e^{j\omega\left(t - \frac{r}{c}\right)}}{r} dv \quad (5.39)$$

in cases where the length of the pathway being characterized for inductance approaches the wavelength of the highest significant ground noise frequency component. In other words (5.39) accounts for retarded potential.

On the other hand, energy need not be considered directly. Instead of solving (5.33) it is somewhat shorter to proceed from the fact that

$$L \frac{dI}{dt} = \frac{d\Lambda}{dt} = \frac{d}{dt} \int \mathbf{B} \cdot d\mathbf{s} = \frac{d}{dt} \int (\nabla \times \mathbf{A}) \cdot d\mathbf{s} \quad (5.40)$$

Then applying Stokes' theorem, the inductance L can be somewhat more directly calculated using

$$L = \oint \frac{\mathbf{A} \cdot d\mathbf{l}}{I} \quad (5.41)$$

Proceeding according to (5.41) has the added advantage that (5.37) and its associated numerical errors are avoided. A FORTRAN program FINREDD written at the University of Ottawa [LC94] is capable of providing inductance using the aforementioned development.

With (5.41), the means is available to determine the inductance between any two points on the planar ground sheet. Practically, the board must therefore be overlaid with a grid whose intersection points constitute the only defined inductances as shown in Figure 5.19.

Figure 5.19: Ground grid with internode lumped inductances

However, for an $N \times N$ point grid, it would be necessary to calculate $2N(N-1)$ self inductances and $[2N(N-1) - 1]^2/2$ mutual inductances. As shown in Figure 5.17, only inductances between the driver reference ground and absolute ground need to be calculated. This involves N^2 self inductances and

$$K = \frac{N^2 (N^2 - 1)}{2} \quad (5.42)$$

mutual inductances (assuming a symmetric inductance matrix) which is about one eighth the task of calculating inductance between each adjacent pair of grid points. Figure 5.20 shows the grid point inductances to be calculated when each one represents the inductive path between a driver's reference ground and absolute ground at the edge connector.

Figure 5.20: Ground grid with point-to-ground inductances

The advantage of using a grid system is that once the matrix of inductances representing self and mutual inductance for every grid point is determined it does not change. This is important because the inductance characterization process requires significant CPU time. Therefore, a process which removes inductance characterization from the objective func-

tion evaluation during optimization is mandatory. Using a grid system, the placement of chips at different locations on the board simply requires accessing the board-level inductance value of the grid point closest to the ground reference of the chip in question. This means that to define a chip board-level inductance, the chip ground reference will have to be mapped to the nearest grid point and the appropriate inductance from the board-level grid inductance matrix accessed.

In choosing a grid structure to represent defined inductances, it then becomes necessary to decide the “granularity” of the grid. Obviously, there is a trade-off: if the grid is too widely spaced, there will be large errors when a chip is snapped to the grid and if the grid is too dense, its inductance matrix will take more time to calculate and more memory to store. At this point the belief is that a compromise can be reached by spacing the grid points such that the maximum difference in inductance between adjacent points is in the 2 - 5% range. Obviously, grid points nearest the absolute ground point will be most sensitive and this range may have to be relaxed for points in this vicinity.

Although the board level L-matrix extraction process is carried out only once, it is still preferable to make the process as fast as possible. As indicated by (5.42), an $N \times N$ point grid would involve calling the FEM analysis and the inductance calculator some $N^2(N^2-1)/2$ times. This means that for a board with a modest 10 x10 grid FINREDD would be called 4950 times. Each call could conceivably take 30 seconds or more requiring over 41 hours to provide the entire matrix. The following development shows how K in (5.42) can be significantly reduced.

After completing N^2 executions of FINREDD all the self inductances are known. This would seem to leave another $N^2 (N^2-1)/2$ executions to determine the mutual inductances. However, before investigating how K might be reduced it is first necessary to see how the mutual inductance L_M would be calculated using results from FINREDD. For mutual inductance, FINREDD would be run with two non-zero Dirichlet boundary nodes (A and B) as shown in Figure 5.21. These nodes must have the same Dirichlet potential so that the inductances between each node and ground are in parallel.

Figure 5.21: Example of mutual inductance calculation

Upon return, FINREDD would provide the effective inductance of the system of two parallel inductors shown in Figure 5.21 and mathematically represented by a 2 x 2 inductance matrix given by

$$\mathbf{L} = \begin{bmatrix} L_{11} & L_M \\ L_M & L_{22} \end{bmatrix} \quad (5.43)$$

From the L-matrix collapsing technique discussed in Appendix B it can be shown that the effective inductance L_{ef} of the 2 x 2 system represented in (5.43) can be calculated using

$$L_{ef} = \frac{1}{\sum_{i=1}^2 \sum_{j=1}^2 L'_{ij}} = \frac{L_{11}L_{22} - L_M^2}{L_{11} + L_{22} - 2L_M} \quad (5.44)$$

where L'_{ij} is an element of the inverse of $\mathbf{L}$ in (5.43). Working (5.44) in reverse to solve for L_M results in

$$L_M = L_{ef} - \sqrt{(L_{ef} - L_{11})(L_{ef} - L_{22})} \quad (5.45)$$

(See Appendix B.) This then would have to be carried out $N^2(N^2-1)/2$ times to get every

L_M . However, it turns out that if “snapshots” of the first N^2 (self inductance) solutions to ϕ in (3.15) are stored, the remaining solutions required for the mutual inductance calculations can be obtained by interpolation. This novel interpolation technique is referred to as the special superposition technique (SST).

Perhaps the best way to illustrate SST is by way of a simple example. Consider the small planar ground structure in Figure 5.22

Figure 5.22: Small planar ground example

Assuming there are only $N = 3$ self inductances to be determined, it would be necessary to solve (3.15) three times. However, it is desirable not to have to solve (3.15) a further $N(N-1)/2$ times to get the mutual inductances. To get the self inductances ϕ_1 , ϕ_2 and ϕ_3 are set in turn to 1V and the ground nodes are always 0V. For example, L_{11} is obtained by making ϕ_1 and the grounds Dirichlet points while ϕ_2 and ϕ_3 float. A similar approach is used to get L_{22} and L_{33} . It is necessary to obtain the mutual inductances L_{12} , L_{13} , and L_{23} without reassigning Dirichlet nodes, and thereby avoid having to redo the LU decomposition required to solve (3.15). In other words the same set of nodes are Dirichlet each time a mutual inductance is calculated. Only the values of the Dirichlet nodes change from one mutual inductance calculation to the next. Since FEM is essentially a linear algebraic formulation of the form $\mathbf{Ax} = \mathbf{b}$, changing the Dirichlet values amounts to changing the values in $\mathbf{b}$ while $\mathbf{A}$ is immutable. In Figure 5.22, this could be done if ϕ_1 , ϕ_2 and ϕ_3 were all fixed to some non-zero value (zero values would result in incorrect inductance). In solving for L_{12} , ϕ_3 is set

to the value it would have had if it had been allowed to float. In other words, what value should ϕ_3 have in the presence of $\phi_1 = \phi_2 = 1\text{ V}$ when all that is known are the ϕ_3 values when $\phi_1 = 1\text{ V}$ and $\phi_2 = 1\text{ V}$ individually? The answer is to use a special form of superposition.

Let $\phi_1^{(1)}$ and $\phi_2^{(1)}$ represent ϕ_1 and ϕ_2 when L_{11} was calculated i.e. $\phi_1 = 1\text{ V}$ (Dirichlet) and ϕ_2 is determined according to (3.15). Similarly, let $\phi_1^{(2)}$ and $\phi_2^{(2)}$ represent ϕ_1 and ϕ_2 when L_{22} was calculated. Since solution of (3.15) is a linear operation, it is valid to say that

$$\phi_2^{(1)} = \kappa_1 \phi_1^{(1)} \quad (5.46a)$$

$$\phi_1^{(2)} = \kappa_2 \phi_2^{(2)} \quad (5.46b)$$

After the two sets of ϕ -values are superposed, it should appear that the analysis had been done with $\phi_1 = \phi_2 = 1\text{ V}$ in the first place so there is the additional requirement that

$$\phi_1^{(1)} + \phi_1^{(2)} = 1 \quad (5.47a)$$

$$\phi_2^{(1)} + \phi_2^{(2)} = 1 \quad (5.47b)$$

Substitution of (5.46) into (5.47) results in the following matrix equation

$$\begin{bmatrix} 1 & \kappa_2 \\ \kappa_1 & 1 \end{bmatrix} \begin{bmatrix} \phi_1^{(1)} \\ \phi_2^{(2)} \end{bmatrix} = \begin{bmatrix} 1 \\ 1 \end{bmatrix} \quad (5.48)$$

The solution to (5.48) is

$$\begin{bmatrix} \phi_1^{(1)} \\ \phi_2^{(2)} \end{bmatrix} = \frac{1}{1 - \kappa_1 \kappa_2} \begin{bmatrix} 1 - \kappa_2 \\ 1 - \kappa_1 \end{bmatrix} \quad (5.49)$$

The values of $\phi_1^{(1)}$ and $\phi_2^{(2)}$ from (5.49) are the values that should have been used such that when the two sets of ϕ -values are superposed, the result is $\phi_1 = 1$ and $\phi_2 = 1$ simultaneously. At the outset, the objective of this exercise was to find the Dirichlet value that should be assigned to ϕ_3 . Since the values of $\phi_1^{(1)}$ and $\phi_2^{(2)}$ are now known, the value of ϕ_3 in the presence of the simultaneous condition of $\phi_1 = 1\text{V}$ and $\phi_2 = 1\text{V}$ can be calculated using

$$\phi_3 = \phi_1^{(1)} \phi_3^{(1)} + \phi_2^{(2)} \phi_3^{(2)} \quad (5.50)$$

In Figure 5.22, the Dirichlet points were at ϕ_1, ϕ_2, ϕ_3 and ground. All other nodes in the FEM grid used to solve (3.15) would float to some calculated values. By storing the values of ϕ_1, ϕ_2 , and ϕ_3 during their respective self inductance calculations, they would be available when (5.50) had to be used to calculate the mutual inductances. And because only Dirichlet values were being changed, the mutual inductances could be determined without additional LU decompositions to solve (3.15). Instead, (3.15) could be solved using only forward and backward substitution. However, for an N^{th} order matrix, N^2 multiplications/divisions are required to carry out forward and backward substitutions. If memory is not at a premium, instead of storing only ϕ_1, ϕ_2 , and ϕ_3 , we could store the entire ϕ distribution (all FEM grid node values) for each self inductance. Then the solution to (3.15) for each mutual inductance would require only $2N$ multiplications/divisions.

At this point the means exist to characterize all self and mutual inductances due to the power and ground planes resulting in an inductance matrix for each. However, the mutual inductance between the power and ground planes has been ignored. To rigorously determine interplane mutual inductance is not a simple task and requires numerical

techniques such as 3D FEM. Instead it may still be possible to estimate the mutual inductance in the following way. Consider the current pathways shown in Figure 5.23.

Figure 5.23: Mutually coupled planes showing inductive current pathways

Each line in the current pathways between P and s and between d and G represents a line of constant current density. Therefore each line can be thought of as a filamentary conduit of current. This is advantageous because the self and mutual inductance of filaments can be calculated using the two closed form equations shown in Appendix A. If the filament method were used to characterize the inductance of the system in Figure 5.23 and if there were N_{f1} and N_{f2} filaments in the power and ground pathways respectively, the following inductance matrix would result

$$\mathbf{L} = \begin{bmatrix} \mathbf{L}_P & -\mathbf{M} \\ -\mathbf{M} & \mathbf{L}_G \end{bmatrix} \quad (5.51)$$

where $\mathbf{L}_P$ is an $N_{f1} \times N_{f1}$ matrix representing the power plane self and mutual inductances, $\mathbf{L}_G$ is an $N_{f2} \times N_{f2}$ matrix representing the ground plane self and mutual inductances and $\mathbf{M}$ is a $N_{f1} \times N_{f2}$ matrix representing the mutual inductances between each of the N_{f1} power plane filaments and the N_{f2} ground plane filaments. $\mathbf{M}$ is negated in (5.51) because by def-

initiation, the currents in the power and ground planes will be oriented in opposite directions. The inductance matrix can then be reduced to a 2×2 matrix by employing the methods discussed in Appendix B. In fact, when L_P and L_G are reduced the resulting values will be precisely the inductance values returned by FINREDD for the paths between P_s and G_d (Figure 5.23) respectively, i.e. L_P and L_G . However, instead of actually doing this it would be more efficient to treat the L_P and L_G values as having come from single filaments and then use the mutual inductance equation from Appendix A to get the effective mutual inductance. For the purposes of this thesis, it is this simpler approach which is proposed.

Up to this point Section 5.3.1 has dealt solely with characterization of the PCB-level interconnect. Fortunately, although the parallel planar structures involved make the inductive pathway characterization when I_{PS} is dominant a fairly complex task, Approach 1 simulation is identical in procedure to that where I_{SN} is dominant. In this case Approach 1 simulation amounts to solving (5.16) and once again determining the di/dt values which will then be made available for evaluation by Approach 2.

5.3.2 Simplified modeling and simulation

When considering board-level characterization for I_{PS} dominance, the model in Approach 2 involves a simple modification to that shown in Figure 3.9 and is shown in Figure 5.24. The model of Figure 5.24 is essentially the same as that of Figure 5.10 except that there is no receiver package leadframe nor are there any board-level signal tracks. Again, the model is reduced to one of inductance such that the simulation can be based on the solution of a system of real, linear equations.

Figure 5.24: Approach 2 model with board-level inductance.

The supermatrix of (5.52) is constructed in a similar way with the package leadframe inductances on the main diagonal.

$$L_{A2} = \begin{bmatrix} L_{11} & L_{12} & \cdots & L_{1P} \\ L_{21} & L_{22} & \cdots & L_{2P} \\ \cdots & \cdots & \cdots & \cdots \\ L_{P1} & L_{P2} & \cdots & L_{PP} \end{bmatrix} \quad (5.52)$$

Notice that due to the formulation, the off-diagonal submatrices are not zero as they were in (5.17) but contain the board-level ground return path mutual inductances. On the other hand, the L_{ii} terms contain package-level mutual inductances and self inductances representing the sum of the leadframe and board-level self inductances.

Extension of the ground noise estimation process to the PCB level has significant ramifications for simulation. In particular, the L matrix given in (3.1) must still be modified to be of the form shown in (3.38) in order to use L to solve for ground noise at the board level. As is done in (3.38), it would be possible to take every row from L_{A2}

containing a ground self inductance, leave the ground self and mutual terms and move the signal/ground mutual inductances to the right hand side vector. However, it is not difficult to see that boards with a few very large packages would soon produce huge almost totally dense matrices which could take considerable CPU time to solve. To circumvent this problem, we employ the techniques described in Appendix B for collapsing inductance matrices. In the super matrix L_{A2} , the main diagonal submatrix representing each package leadframe will contain its ground inductances in the upper left corner. If there are G_i ground pins in a package, it will be possible to collapse the $G_i \times G_i$ ground pin submatrix to a $K \times K$ submatrix where K is the number of separate ground references in the package. From (5.52) it is evident that one package with G_i ground pins and another with G_j ground pins will give rise to a $G_i \times G_j$ mutual submatrix. If the former has K_1 separate grounds and the latter K_2 separate grounds, then the $G_i \times G_j$ mutual submatrix can be reduced to a $K_1 \times K_2$ mutual submatrix. In general this can be described by

$$L_r = \left[\begin{array}{cc|cc|c|cc} L_{g_1} & M_{g_1} & M_{12} & M & \dots & M_{1n} & M \\ M_{g_1} & L_{s_1} & M & M & \dots & M & M \\ \hline M_{12} & M & L_{g_2} & M_{g_2} & \dots & M_{2n} & M \\ M & M & M_{g_2} & L_{s_2} & \dots & M & M \\ \hline \dots & \dots & \dots & \dots & \dots & \dots & \dots \\ \hline M_{1n} & M & M_{2n} & M & \dots & L_{g_n} & M_{g_n} \\ M & M & M & M & \dots & M_{g_n} & L_{s_n} \end{array} \right] \quad (5.53)$$

where each L_g and L_s with the same subscript number indicate the ground and signal pin inductance from the same ground group, M appears in many places and refers to any mutual inductance matrix containing mutual inductances between non-ground pins. The M 's are not necessarily equal to one another. When the appropriate reductions on each of the L_g matrices has been made according to Appendix B, each L_g will be reduced to a single value L_g . Finally, it is still necessary to move the known di/dt's (signal di/dt's) and their signal/ground mutual inductance weighting factors to the right hand side vector. Assume the i^{th} package has K references, $G_1, G_2, \dots, G_k$ ground pins in each reference group and $S_1, S_2, \dots, S_k$

signal pins in each reference group. This will result in $S_1x(G_1 \times 1)$, $S_2x(G_2 \times 1) \dots S_kx(G_k \times 1)$ column vectors in the super matrix. Each of these column vectors is collapsed to a single entry in a way similar to the way the mutual inductance submatrix collapses. They are then moved to the right hand side vector in the same way that signal/ground mutual inductance terms populated the right hand side vector in (3.38). Applying the modifications called for by (3.35-3.37) results in an overall system equation given by

$$\begin{bmatrix} -L & -U \\ U & 0 \end{bmatrix} \begin{bmatrix} \dot{I}_g \\ V_g \end{bmatrix} = \begin{bmatrix} -\sum M \dot{I}_s \\ -\sum \dot{I}_s \end{bmatrix} \quad (5.54)$$

L is a matrix of the reduced now single L_g values, U is the unity matrix, 0 is a $K \times K$ zero matrix, $\dot{I}_g$ is the unknown vector of ground current rates-of-change and V_g is the unknown vector of ground noise voltages. $\dot{I}_s$ is the column vector of known di/dt values from the sources and M is a non-specific matrix of reduced mutual inductance column vectors (column vectors reduced to single effective mutual inductances as specified above). The most significant result of (5.54) is that the system of equations may be solved without inverting the matrix. By simple algebraic manipulation, it turns out that the solution to (5.54) is given by

$$\begin{bmatrix} \dot{I}_g \\ V_g \end{bmatrix} = \begin{bmatrix} 0 & U \\ -U & -L \end{bmatrix} \begin{bmatrix} -\sum M \dot{I}_s \\ -\sum \dot{I}_s \end{bmatrix} \quad (5.55)$$

As an example consider a board with ten 100 pin packages with 10 ground pins each, with each package having but one ground reference (1 separate ground). The super matrix L_{A2}

would be 1000 x 1000. Each of the packages' grounds would then be reduced to a single entry reducing L in (4.38) to a 10 x 10. However, in applying KCL there are 10 different ground references (one for each package) so L would gain 10 rows and columns. Thus solving for the ten ground noise values (V_g is a 10 x 1 vector) would involve a 20 x 20 matrix. But as indicated by (5.55) no LU decomposition is required.

5.4 Comparison of I_{SN} and I_{PS}

Although the theory to predict ground noise due to I_{SN} and I_{PS} has been developed, that for I_{PS} was not implemented once it was realized that for typical operating conditions of a digital PCP, the main source of ground noise is that due to I_{SN} . In the next chapter, results are presented for I_{SN} only. As justification for providing ground noise results for that due to I_{SN} only, two simulations were carried out on the circuit shown in Figure 5.1. In the first the driver and receiver are CMOS devices while in the second they are TTL. Figures 5.25 and 5.26 show the ground noise across the ground path $L_g + 2L_f$ due to I_{SN} and the ground noise developed across the ground path L_p due to I_{PS} respectively.

Figure 5.25: CMOS ground noise due to I_{SN}

Figure 5.26: CMOS ground noise due to I_{PS}

In this case, the ground noise due to I_{SN} is over 200 times greater than that due to I_{PS} . Similarly, Figures 5.27 and 5.28 show the ground noise waveforms corresponding to TTL devices.

Figure 5.27: TTL ground noise due to I_{SN}

Figure 5.28: TTL ground noise due to I_{PS}

Again the ground noise due to I_{PS} is insignificant compared with that due to I_{SN} . In this case the I_{SN} ground noise is well over 300 times larger in magnitude than that due to I_{PS} . It should be noted that no claim is being made regarding the relative merits of CMOS versus TTL devices. In short, it should not be inferred from Figures 5.25 through 5.28 that there tends to be less ground noise in using CMOS as opposed to TTL technology. However, in both technologies, the ground noise due to I_{PS} is insignificant when compared with that due to I_{SN} .

Chapter 6

PCB-level ground noise minimization

Now that the processes for evaluating ground noise at the PCB level are in place it is necessary to modify the optimization formulation discussed in Chapter 4 so that it can be used for PCB-level optimization.

6.1 PCB-level optimization

The basic formulation as discussed in Chapter 4 is still applicable at the board level. The only difference is in the domain of variables which give rise to the ground noise function evaluation. At the package level, the variables were Φ_j , the pin assignment as given by (4.1). For example, in an N pin package, the integers 1 to N are assigned to each pin. This means there are $(N-1)!$ different possible pin assignments.

At the PCB level, (4.2) still applies; ground noise is a function of the inductances at the IC-package level and now the PCB-level as well. In Section 5.3.1, a grid was laid over the PCB ground sheet and inductances were defined at each of these points. The grid also serves the purpose of defining a finite number of locations on the board at which to locate

IC packages. Therefore at the PCB level, the variables are now given by γ_j , the grid location of the package. The principal difference between γ_j and Φ_j is that Φ_j represents the assignment of package pins around the periphery of an IC package whereas γ_j represents the assignment of IC-packages to grid coordinates. Φ_j is by definition one-dimensional while γ_j becomes one-dimensional via the mapping given in (6.2). Hence, at the PCB level (4.2) becomes

$$V_g = V_g(\gamma_j) \quad (6.1)$$

where $\gamma_j \in \mathcal{S}$, $\gamma_j(i) \in \{1, 2, 3, \dots, N_{GRID}\}$, $\gamma_j(i) \neq \gamma_j(k)$ and $\gamma_j(i)$ defines the assigned location of the i^{th} IC package grid location.

In order to make use of the same simulated annealing algorithm used to optimize the pin assignment at the IC-package level, (6.1) translates the configuration variable γ_j back to one dimension. If there are N_{GRID} discrete grid locations then γ_j may have any integer value in the range 1 to N_{GRID} . Again, the γ_j value for each package is unique since only one package can be at any grid location at a given time. One further restriction on the γ_j values is caused by the fact that large packages may overlap more than one grid point. We arbitrarily define the location of a package to be the coordinates of its lower left corner. If the package overlaps other grid points, then they too are removed from the list of available positions for the next package. For example, if the grid is 10 x 10 then the first package for which a location is to be selected may occupy any of the defined grid points with values from 1 to 100.

Figure 6.1: Selection of γ_j a PCB-level location

If in addition the grid points are 1cm apart, the package is 1.5cm on a side and it is placed as shown in Figure 6.1 then γ_j has the value 56, and grid points 57, 66 and 67 are removed from the selection process for the next package. The selection γ_j can be broken into its x,y coordinates according to

$$\gamma_j = n_G y_s + x_s \quad (6.2)$$

where n_G is the number of grid points in each row and y_s and x_s are the x,y coordinates corresponding to γ_j and are given by

$$y_s = \frac{\gamma_j}{n_G} \quad (6.3)$$

where the division in (6.3) is integer division and

$$x_s = \text{mod}(\gamma_j, n_G) \quad (6.4)$$

After γ_j has been selected the additional grid point values which are no longer available are obtained by mapping each value in the range

$$x_s \leq x \leq x_s + P_r - 1 \quad (6.5a)$$

and

$$y_s \leq y \leq y_s + P_r - 1 \quad (6.5b)$$

according to (6.2) where P_r is the number of grid points spanned in the x and y directions by the given package. In the above example, $P_r = 2$ and since $\gamma_j = 56$, $n_G = 10$ we know that $x_s = 6$ and $y_s = 5$. This means that the x values removed according to (6.5a) are $x = 6, 7$ and the y values removed according to (6.5b) are $y = 5, 6$. These values map according to (6.2) into the γ_j values of 56, 57, 66 and 67. Experience so far has shown that better results are obtained if the largest packages are assigned positions first.

In addition to the cost function which naturally selects certain IC placements over others, there are also manufacturing constraints. Specifically, to be manufacturable, there is a minimum distance which must be maintained between all IC's. This buffer zone around between IC's is required to ensure correct autoinsertion, visual inspection and to facilitate the repair of field-returns should an IC prove to be faulty once its PCP has been installed at the customer's premises. For at least one major telecommunications products manufacturer in the Ottawa area the minimum spacings for IC's are given in Table 6.1.

Table 6.1: IC-to-IC minimum spacing

Package type	Minimum spacing (mm)
Through hole	2.54
Surface mount	1.02

An example of the above minimum spacing is shown in Figure 6.1 which is an actual product PCP.

Figure 6.2: IC-to-IC spacing on a section of production PCP

The yellow borders enclosing the IC packages in Figure 6.2 extend 1.27mm beyond the IC package outline on all sides. This indicates the area required by the IC-to-IC spacing rule given in Table 6.1. It is important to note that in an actual design a host of other rules gov-

erning the spacing of other components and PCB features such as via holes may be in force resulting in further restrictions on their placement.

6.2 PCB-level optimization results

To demonstrate the capabilities of board-level ground noise optimization the PCP shown in Figure 6.3 [Uni] is presented.

Figure 6.3: PCP initial configuration

In this example, it was required that IC's U10, U17, U18, U19 and U20 exhibit no more than 500mV of ground noise. After about 5 hours of optimization, the layout shown in Figure 6.4 was obtained.

Figure 6.4: PCP optimized configuration

Figure 6.5 shows the entire return path ground noise values for each of the five critical IC's before and after optimization.

Figure 6.5: IC package/board-level ground noise before and after placement optimization

It may appear from the results in Figure 6.5 that the optimization process has resulted in

fairly marginal improvement and that the optimization process stopped before satisfying the 500mV requirement. However, this is an unfair assessment. As was the case for package-level optimization, the optimal configuration is based on di/dt values calculated from the initial configuration. Based on the initial di/dt values, the optimal configuration returned ground noise values of between 405mV and 486mV which clearly satisfies the requirement. To obtain the actual ground noise values the estimation process must be run once more on the optimal configuration which returns higher di/dt values due to the now lower inductance. Hence, the actual ground noise values are higher than expected. Furthermore, during the optimization process, the IC placement continually changes and is reflected by the continual update of L_{GB} in (5.19). These changes affect only the PCB-level self and mutual inductances not the IC-package-level leadframe inductances. The ground noise due to the IC packages remains constant. To appreciate the real improvement which has occurred as a result of the optimization process, only the ground noise voltage developed across the board-level ground inductances should be compared before and after optimization. This information is shown in Figure 6.6. Finally, U18 returns no ground noise since, as it turns out, this device has no active connections.

Figure 6.6: Board-level ground return path noise before and after placement optimization

From Figure 6.6 it is apparent that significant improvement has occurred in that portion of the ground noise cost function over which the optimization process has control.

The results in Figure 6.6 suggest using the noise voltage due to the PCB-level ground return inductance alone as the optimization cost function since that due to the packages is constant. After just such an optimization, the configuration shown in Figure 6.7 was obtained. In this case the required threshold is set at 175mV which allows 325mV for the IC packages. The optimization process required about 4.2 hours to complete. The PCB-level ground noise results are shown in Figure 6.8.

Figure 6.7: Alternative PCP optimized configuration

Figure 6.8: Board-level ground return path noise as optimization cost function

Figure 6.8 shows that altering the cost function in this way results in a more successful optimization because the PCB-level ground noise contributions are more uniformly optimal. Again, the optimized result has apparently not satisfied the requirement of 175mV. In fact, the requirements are exceeded only after recalculation of the di/dt values using Approach 1 one last time. This was also the case in Figure 6.5. However, if the entire return path ground noise generated in the optimum configuration represented by Figures 6.6 and 6.8 are compared, as shown in Figure 6.9, the configuration shown in Figure 6.6 results are marginally favorable. It should be remembered that the IC packages have not been optimized according to the methods described in Chapter 4. Had this been done prior to PCB-level optimization there would likely be greater improvement observed as a result of the PCB-level optimization process.

Figure 6.9: Entire ground return path noise based on Figure 6.7 configuration

One final point of interest concerns the ground noise observed in U20. In each of the optimizations, U20 consistently exhibits less ground noise than the other active IC's. The main reason for this is likely due to the fact that U20 has both drivers and receivers which are assumed to be active simultaneously. As can be seen in Figures 5.12 and 5.14, the currents due to drivers and those due to receivers flow through the IC package ground pins in *opposite* directions. The net result is that there is a partial cancellation of the opposing currents resulting in lower ground noise due to that IC package. Hence the ground noise in U20 is lower than the others due to this partial cancellation of the ground current in the IC package. It would therefore seem advisable to package IC's with a balance of drivers and receivers whenever possible.

Chapter 7

Conclusion

A new method has been proposed for characterizing, evaluating and optimizing ground interconnect to minimize ground noise. This method provides for fast ground noise estimation at both the IC package and PCB levels.

The method proposed in this thesis applies both modeling and simulation to IC packages and PCB-level interconnection structures. At the package level, the first approach accurately determines the expected di/dt values due to the sources while the second uses the di/dt values to estimate peak ground noise at vastly reduced CPU time cost. The enormous CPU cost reduction is made possible by eliminating all but the package-level parasitic inductance which reduces the simulation to a system of real linear equations. At the board level, the parasitic capacitance can no longer be ignored. In this case, the di/dt values in all signal-path inductances (not just those due to the sources) are determined using Approach 1. As was the case at the package level, the di/dt values are then used in Approach 2 to determine the resulting noise voltages in the ground inductances, again using a system of real linear equations. Unlike the package level, the ground noise at the board level is the total noise voltage across the receiver package ground pin inductance, the board-level ground return inductance and the driver package ground pin inductance. Using this scheme, structures which could take weeks if not months of CPU time to optimize using conventional characterization and simulation

techniques can now be optimized in hours.

The results observed indicate that the method can indeed deliver optimized IC package pin assignments in a reasonably short CPU time. At the package level a 208 pin package took about 20 CPU minutes to be optimized from a “random” initial configuration and showed a 26 fold improvement in ground noise performance. Furthermore, even when an intelligent initial configuration was selected, the optimization process led to a configuration exhibiting a 2.2-fold reduction in ground noise.

At the board level, a PCP with 15 IC’s was optimized based on the requirement that five particular IC’s must exhibit no more than 500mV of ground noise. Initially, the maximum ground noise was over 900mV. The optimization process took about 5 hours on a SPARC10 workstation and resulted in a maximum ground noise of less than 700mV. The 240mV improvement is somewhat disappointing until it is realized that the entire improvement is due solely to reducing the effective inductance of the PCB-level ground return path. The ground noise due to the PCB-level ground path, in fact, exhibits better than two-fold improvement. Ideally, IC package-level optimization should be carried out to reduce the IC package induced ground noise to a minimum. Such a strategy would likely result in significantly lower ground noise over the entire ground return path between driver and receiver.

The ultimate success of the method described in this thesis is due to two facts. First, the errors observed in Approach 2 ground noise estimation are within a few percent of the values obtained via NILT. Secondly, and more importantly, the optimization process is quite insensitive to the absolute di/dt values calculated for the signal path inductances. For these two reasons, the method can deliver optimization of large interconnected PCB-level networks in several hours; an impossibility using current conventional high-accuracy characterization and simulation methods.

Appendix A

Inductance Modeling

In order to implement the proposed optimization, (3.36) must be solved which in turn requires knowledge of the lead-frame self and mutual inductance and the di/dt values entering each signal pin. To determine the lead-frame inductance matrix L , there are many techniques available [KTW93], [Rue72], [Gro46], [GOP90], [Rai84]. These range from empirically determined rules of thumb to 3D FEM. Since the lead-frames in question are comprised of filamentary tracks with very small cross-sectional current density variation, the closed form equations found in [Rai84] were chosen. We stress, however, that the estimation and optimization processes are in no way dependent on the means by which the lead-frame inductances are derived. Any convenient method could be substituted for the one used here. From [Rai84] the self L_{ii} , and mutual L_{ij} , lead-frame inductances are determined using

$$L_{ii} = \frac{\mu}{2\pi} l_i \left[\ln \left(\frac{2l_i}{r_i} \right) - 0.75 \right] H \quad (\text{A.1})$$

$$\hat{L}_{ij} = K \left[\ln \left(A + \sqrt{1 + A^2} \right) - \left(\sqrt{1 + \frac{1}{A^2}} \right) + \frac{1}{A} \right] H \quad (\text{A.2})$$

where $K = \mu l_{ij}/2\pi$, $A = l_{ij}/d_{ij}$, l_i is the length of the i th track, r_i is the cross-sectional radius of the i th track, d_{ij} is the average distance between the i th and j th tracks and l_{ij} is the effective parallel length of the i th and j th tracks given by

$$l_{ij} = \sqrt{l_i l_j} \quad (\text{A.3})$$

and l_i and l_j are defined below in Figure A.1.

Figure A.1: Lead orientation in a chip package

It has been found that better accuracy is achieved for the small mutual inductances resulting from widely separated leads by modifying (A.2) such that

$$L_{ij} = \hat{L}_{ij} \cos \alpha \quad (\text{A.4})$$

Using (A.4) results in $L_{ij} = \hat{L}_{ij}$ for parallel leads since $\alpha = 0$ and in $L_{ij} = 0$ for perpendicular leads as would be expected. Note that for leads on opposite sides of the package, L_{ij} should be negative and (A.4) accounts for this since $\cos \alpha < 0$ for $90^\circ < \alpha < 270^\circ$.

The L matrix calculated using (A.1-A.4) results in sufficiently accurate values as supported in the following comparison with L values determined from the commercially

available software package HENRY™ [OEA]. The data in Figure A.3 is based on the package shown in Figure A.2.

Figure A.2: 8-pin quad package

$$\begin{bmatrix} 8.400 & 0.507 & 0.000 & -0.334 & -0.397 & -0.265 & 0.000 & 0.912 \\ 0.507 & 8.400 & 0.912 & 0.000 & -0.265 & -0.397 & -0.334 & 0.000 \\ 0.000 & 0.912 & 8.400 & 0.507 & 0.000 & -0.334 & -0.397 & -0.265 \\ -0.334 & 0.000 & 0.507 & 8.400 & 0.912 & 0.000 & -0.265 & -0.397 \\ -0.397 & -0.265 & 0.000 & 0.912 & 8.400 & 0.507 & 0.000 & -0.334 \\ -0.265 & -0.397 & -0.334 & 0.000 & 0.507 & 8.400 & 0.912 & 0.000 \\ 0.000 & -0.334 & -0.397 & -0.265 & 0.000 & 0.912 & 8.400 & 0.507 \\ 0.912 & 0.000 & -0.265 & -0.397 & -0.334 & 0.000 & 0.507 & 8.400 \end{bmatrix}$$

a) Lead-frame inductances (nH) determined using (A.1-A.4)

$$\begin{bmatrix} 8.257 & 0.528 & 0.000 & -0.350 & -0.416 & -0.278 & 0.000 & 0.946 \\ 0.528 & 8.257 & 0.946 & 0.000 & -0.278 & -0.416 & -0.350 & 0.000 \\ 0.000 & 0.946 & 8.257 & 0.528 & 0.000 & -0.350 & -0.416 & -0.278 \\ -0.350 & 0.000 & 0.528 & 8.257 & 0.946 & 0.000 & -0.278 & -0.416 \\ -0.416 & -0.278 & 0.000 & 0.946 & 8.257 & 0.528 & 0.000 & -0.350 \\ -0.278 & -0.416 & -0.350 & 0.000 & 0.528 & 8.257 & 0.946 & 0.000 \\ 0.000 & -0.350 & -0.416 & -0.278 & 0.000 & 0.946 & 8.257 & 0.528 \\ 0.946 & 0.000 & -0.278 & -0.416 & -0.350 & 0.000 & 0.528 & 8.257 \end{bmatrix}$$

b) Lead-frame inductances (nH) determined using HENRY™

Figure A.3: Lead-frame inductance comparison

The lead-frame L matrices compared in Figure A.3 indicate a maximum error in using (A.1-A.4) of less than 5%.

Appendix B

Inductance Matrix Reduction

The pathways through which the ground return currents pass are important due to the parasitic inductance they possess. Often there are many parallel pathways each contributing to a matrix which must be LU decomposed to solve for the ground noise present. By reducing the number of pathways, the size of the matrix is reduced thereby increasing the speed of numerical processing. The following development shows how matrix reduction can be achieved while maintaining the relevant mutual inductances. Consider the network of parallel groups of parallel inductors shown in Figure B.1

Figure B.1: Parallel groups of parallel inductors

In Figure B.1 assume there are a total of N voltages. one across each of the N groups of parallel inductances. In each group there are $m_i - m_{i-1}$ branches where $i = 1, 2, \dots, N$ and $m_0 = 0$. Each branch contains an inductance L_{ij} . Since each voltage v_{gi} is due to the currents through self and mutual inductances, the following matrix equation can be written to describe the entire system

$$\begin{bmatrix} v_{g1} \\ \dots \\ v_{g1} \\ v_{g2} \\ \dots \\ v_{g2} \\ \dots \\ v_{gN} \\ \dots \\ v_{gN} \end{bmatrix} = \begin{bmatrix} L_{11} & L_{12} & \dots & L_{1N} \\ L_{21} & L_{22} & \dots & L_{2N} \\ \dots & \dots & \dots & \dots \\ L_{N1} & L_{N2} & \dots & L_{NN} \end{bmatrix} \begin{bmatrix} i_1 \\ \dots \\ i_{m_1} \\ i_{m_1+1} \\ \dots \\ i_{m_2} \\ \dots \\ i_{m_{N-1}+1} \\ \dots \\ i_{m_N} \end{bmatrix} \quad (\text{B.1})$$

where each element L_{ij} is a submatrix of column order $m_j - m_{j-1}$ and row order $m_i - m_{i-1}$. If we assume that each voltage v_{gi} is composed of N voltage components; one from each group then

$$v_{gi} = v_{gi}^{(1)} + v_{gi}^{(2)} + \dots + v_{gi}^{(N)} \quad (\text{B.2})$$

Furthermore, from (B.1) it is apparent that each voltage component is due to an inductance submatrix and a set of currents according to

$$\begin{bmatrix} v_{gi}^{(j)} \\ v_{gi}^{(j)} \\ \dots \\ v_{gi}^{(j)} \end{bmatrix} = L_{ij} \begin{bmatrix} i_{m_{j-1}+1} \\ i_{m_{j-1}+2} \\ \dots \\ i_{m_j} \end{bmatrix} \quad (\text{B.3})$$

If $i = j$ then L_{ij} can be inverted and (B.3) can be rewritten as

$$\begin{bmatrix} i_{m_{j-1}+1} \\ i_{m_{j-1}+2} \\ \dots \\ i_{m_j} \end{bmatrix} = L_{ij}^{-1} \begin{bmatrix} v_{gi}^{(j)} \\ v_{gi}^{(j)} \\ \dots \\ v_{gi}^{(j)} \end{bmatrix} \quad (\text{B.4})$$

Since the j^{th} group of inductances is being considered, let the total (equivalent) current in the j^{th} group be denoted I_j^e and therefore the sum of the terms in the right-hand-side vector in (B.4) is given by

$$I_j^e = \sum_{k=m_{j-1}}^{m_j} i_k \quad (\text{B.5})$$

Due to (B.4) the summation carried out in (B.5) can also be equated to the right-hand-side of (B.4). Since the right-hand-side vector contains only the term v_{gi} it can be factored out giving an alternate expression for I_j^e , namely

$$I_j^e = v_{gi}^{(j)} \sum_{n=m_{j-1}}^{m_j} \sum_{k=m_{j-1}}^{m_j} \hat{L}_{nk} \quad (\text{B.6})$$

where $\hat{L}_{nk}$ is an element of L_{ij}^{-1} . Note that since the submatrix being reduced is square, the limits on the summations in (B.6) are both m_j . Since inductance is defined to be the constant of proportion between voltage across an inductance and the rate of change with respect to time of the current through it, (B.6) gives rise to an expression for effective inductance L_{jj}^e , i.e.

$$L_{jj}^e = \frac{1}{\sum_{n=m_{j-1}}^{m_j} \sum_{k=m_{j-1}}^{m_j} \hat{L}_{nk}} \quad (\text{B.7})$$

Using (B.7) any of the submatrices L_{jj} in (B.1) can be reduced to a single effective inductance value.

To reduce all the submatrix elements of the L -matrix in (B.1) it is also necessary to reduce the off-diagonal mutual inductance submatrices L_{ij} , to single effective mutual inductance values. However, if it is assumed that $j > i$ and $m_j > m_i$ then L_{ij} is a non-square matrix with more columns than rows and hence in general L_{ij}^{-1} does not exist. Fortunately, such matrices do possess a *left*-inverse matrix which is a matrix satisfying the following conditions. Given a matrix A with column rank j and row rank i and $j > i$, there exists a square matrix $A^T A$ [Usm84] such that

$$(A^T A)^{-1} (A^T A) = I \quad (\text{B.8})$$

where I is the identity matrix. A^L is the left inverse of A if $A^L A = I$. From (B.8) it is obvious that the left inverse of A is given by

$$A^L = (A^T A)^{-1} A^T \quad (\text{B.9})$$

Therefore if $m_j > m_i$ (B.4) must be modified to appear as

$$\begin{bmatrix} \dot{I}_{m_{j-1}+1} \\ \dot{I}_{m_{j-1}+2} \\ \dots \\ \dot{I}_{m_j} \end{bmatrix} = L_{ij}^L \begin{bmatrix} v_{g^i}^{(j)} \\ v_{g^i}^{(j)} \\ \dots \\ v_{g^i}^{(j)} \end{bmatrix} \quad (\text{B.10})$$

Then in a manner similar to (B.5-B.7) the effective mutual inductance can be calculated from

$$L_{ij}^e = \frac{1}{\sum_{n=m_{i-1}}^{m_i} \sum_{k=m_{j-1}}^{m_j} \hat{L}_{nk}} \quad (\text{B.11})$$

where $\hat{L}_{nk}$ is an element of L_{ij}^L . For submatrices in (B.1) whose row rank is greater than their column rank, i.e. $m_j < m_i$ only a right-inverse exists. However, (B.4) arises from (B.3) by pre-multiplying both sides of (B.3) by the inverse of L_{ij} but matrices with right-inverses must be post-multiplied. Therefore it is not possible to find the effective mutual inductance of L_{ij} directly if $m_j < m_i$. Fortunately, the overall L-matrix in (B.1) is symmetric so any L_{ij} with $m_j < m_i$ gives rise to its own transpose which has the same effective mutual inductance value.

Experience has shown that any diagonally dominant matrix such as the self inductance submatrices in (B.1) can be accurately reduced to its effective inductance value according to (B.7). Unfortunately, this is not the case for the mutual inductance submatrices. Because they are not diagonally dominant in general, the method can lead to large errors in the effective mutual inductance. To circumvent this problem, the effective mutual inductance calculation can be reformulated using a diagonally dominant matrix. Given

any 2x2 self inductance matrix (B.7) leads to the fact that

$$L_{ef} = \frac{L_{11}L_{22} - L_{12}L_{21}}{L_{11} + L_{22} - L_{12} - L_{21}} \quad (\text{B.12})$$

where since $L_{12} = L_{21} = L_M$, (B.12) is really the same as equation (5.44). Working (B.12) backwards in terms of L_M yields

$$L_M = L_{ef} \pm \sqrt{(L_{ef} - L_{11})(L_{ef} - L_{22})} \quad (\text{B.13})$$

which is essentially (5.45). Note that in equation (5.45) only the '-' sign appears. This will be proved now. Let $L_{ef} = h_1 L_{11}$ and $L_{ef} = h_2 L_{22}$ where $0 < h_1 < h_2 < 1.0$ and $h_1, h_2 \in \mathfrak{R}$. This implies that $L_{11} < L_{22}$ but this is arbitrary. If the '+' sign had been used in (5.45) then with the above definitions (5.45) can be rewritten as

$$L_M = h_1 L_{11} \left[1 + \sqrt{\left(1 - \frac{1}{h_1}\right)\left(1 - \frac{1}{h_2}\right)} \right] \quad (\text{B.14})$$

Next it must be determined if $L_M > L_{11}$. This is done by setting up the following inequality.

$$h_1 L_{11} \left[1 + \sqrt{\left(1 - \frac{1}{h_1}\right)\left(1 - \frac{1}{h_2}\right)} \right] > L_{11} \quad (\text{B.15})$$

By way of some algebraic manipulation (B.15) reduces to

$$h_2 > h_1 \quad (\text{B.16})$$

which by the original definitions is known to be true. Hence $L_M > L_{II}$ however, a mutual inductance can never exceed either of the self inductances to which it is linked [JHJ78]. Therefore, in (5.45) only the '-' sign applies. Using a similar argument it can be shown that (5.45) so defined also leads to the condition that $L_M < L_{22}$ as required.

As an example of the matrix reduction process consider a set of two parallel groups of inductances with three inductances in the first group and two in the second. Assume that (B.1) is given by

$$\begin{bmatrix} v_{g1} \\ v_{g1} \\ v_{g1} \\ v_{g2} \\ v_{g2} \end{bmatrix} = \left[\begin{array}{ccc|cc} 12.0 & 8.2 & 5.8 & 0.6 & 0.5 \\ 8.2 & 13.5 & 8.9 & 0.7 & 0.6 \\ 5.8 & 8.9 & 14.8 & 1.0 & 0.6 \\ \hline 0.6 & 0.7 & 1.0 & 12.0 & 7.0 \\ 0.5 & 0.6 & 0.6 & 7.0 & 13.5 \end{array} \right] \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_5 \end{bmatrix} \quad (\text{B.17})$$

where all the inductance values are in nH. Using (B.7) L_{11}^e and L_{22}^e are calculated to be

$$L_{11}^e = 9.3082\text{nH}$$

$$L_{22}^e = 9.8261\text{nH}$$

and using (B.11)

$$L_{12}^e = L_{21}^e = 0.5427\text{nH}$$

However, by using (B.7) to collapse the entire L-matrix in (B.13) to a single effective value L^e , the result is $L^e = 5.1092\text{nH}$. Using this value and the values for L_{11}^e and L_{22}^e

above in equation (5.13) produces

$$L_{12}^e = L_{21}^e = 0.6588\text{nH}$$

The process of calculating L_{ij}^e can be accomplished without the use of (B.11) and is completely general. If the effective mutual inductance for a particular L_{ij} is required, L_{ii}^e , L_{jj}^e and L^e can be determined from (B.7). Then L_{ij}^e can be calculated using (5.45).

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IMAGE EVALUATION TEST TARGET (QA-3)

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