Ruggedized HMIC S-X Band Frequency Converter for Severe Weather Tracking Radar

By

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Abstract

As climate change progresses, the severity of weather events is expected to increase leading to an increased risk for personal injury and property damage. Climate change has presented a need for increased tracking of severe weather for the purpose prediction and early warning systems with regards to natural disasters.

This thesis presents the design of a hermetically sealed hybrid microwave integrated circuit (HMIC) up and down for use in an X-band severe tracking weather radar system would improve the environmental performance and reliability over the existing PCB (printed circuit board) based design. The design was verified through analysis and test with respect to RF performance, thermal performance, environmental survivability and reliability of the designed electronic assembly. As reliability is the most important outcome of the research, MTBF (mean time before failure) was considered a global figure of merit to compare the HMIC design against the existing PCB implementation. Analysis of the HMIC was shown to provide an MTBF of 4.3 million hours compared to 1.5 million hours for the PCB implementation or a 2.8 factor of improvement in reliability. It is worth noting that this number is a mean, and thereby reduces the chance of failure in a 10-year mission from 2% to 0.3%. The two main drivers for improved reliability (determined by analysis) are the hermeticity of the HMIC, as well as improved thermal conductance from die junction to ambient.

Due to the Covid-19 pandemic manufacturing was delayed, preventing production of hardware to validate the thesis through physical testing. For this reason, the thesis stands on analysis of the design alone. Once the manufacturer has restored is capacity, the design will be produced, and results verified through physical test.

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"If I have seen further than others, it is because I have stood on the shoulders of giants" – Isaac Newton

While this work does not presume to see further than others, it was only achievable in the fashion suggested by Sir Isaac Newton. The following are my giants.

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ABBREVIATIONS

COTS	Commercial off the shelf
dB	Decibel
dB_c	Decibel (power, referenced to carrier power)
dB_m	Decibel (power, referenced to 1 mW)
dBZ	Decibel (reflectivity).
DUT	Device under test
FET	Field effect transistor
FIT	Failures in time
GaAs	Gallium arsenide
HMIC	Hybrid microwave integrated circuit
IR	Image reject
MMIC	Monolithic microwave integrated circuit
MTBF	Mean-time between failure
OBW	Occupied bandwidth
UDC	Up-down converter
SMT	Surface mount technology
SMD	Surface mount device

SSPA	Solid-state power amplifier
STALO	Stable local oscillator
VCXO	Voltage controlled crystal oscillator
Z	Reflectivity

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1.0 INTRODUCTION

The thesis presented herein is that a hermetically sealed hybrid microwave integrated circuit (HMIC) will offer improved reliability and environmental hardening when compared to the PCB implementation of the same circuit. To demonstrate this, an HMIC implementation of an S-band to X-band frequency converter was designed in the Nanowave Technologies HMIC process to demonstrate improved reliability and environmental hardening compared to an existing PCB implementation of the subassembly. The following chapter provides a discussion on motivation for this work, system specifications, discussion on design challenges, and information on the specific contributions and organization of the thesis.

1.1 Motivation

There is a scientific consensus that anthropogenic climate change is occurring [1] [2] [3] [4] [5] [6] [7]. One effect of a changing climate is the increase in frequency of severe weather events [8] [9] [10]. For this reason, development of severe weather tracking sensors is imperative for prediction, detection, and early warning systems. Research was undertaken in collaboration with an industrial partner (Nanowave Technologies Inc.) to develop environmentally hardened componentry for weather sensing applications for the Asian market.

During the development of a ruggedized weather sensor by Nanowave Technologies Inc., it was observed that an S-X band up-down frequency converter subassembly (here-after referred to as a UDC) was sensitive to fault during

exposure to environmental extremes. Failure of a PCB (printed circuit board) was observed during extensive environmental testing of the initial severe weather tracking radar prototype. The current research was initiated to develop a ruggedized, high-reliability frequency converter capable of withstanding the extreme environmental conditions the radar would experience in practical deployment. The use of PCB technology was reviewed, with consideration given to other technologies.

1.1.1 Comparing Printed Circuit Board and Hybrid Microwave Integrated Circuit Technologies

Environmentally hardening a PCB has several challenges. Conformal coating of the RF substrates affects the characteristic impedance of transmission lines leading to increased loss and VSWR. For this reason, in the PCB implementation of the UDC, conformal coating was not used, and solder-mask was removed around RF traces. After 14 days of environmental testing over the full operating temperature range and at 95% relative humidity, the PCB was exhibiting signs of corrosion on RF traces and solder interconnects to various SMT packages.

Ceramic and plastic packaging used for active devices on PCBs also reduces heat transfer out of the top of the package; PCB dialectic slows thermal transfer out of the bottom. While this is not significant enough to cause a thermal failure (with proper PCB design), it does raise the operating temperature thereby lowering the lifetime (and in turn reliability) of the active component. Active components on PCBs are adhered using solder. This solder becomes part of the thermal relief path, exposing it to thermally induced mechanic stress in pulsed RF systems.

Contrasting with an HMIC design, all active devices are secured with a conductive thermal epoxy to a carrier with a matched coefficient of thermal expansion. This means the carrier will expand/contract equivalently to the die interface, ensuring minimal mechanical stress due to thermal variation. The carrier is then screwed into the housing, ensuring the die is mechanically secure. In the process used, the housing is aluminum. This allows a continuous metal path from die to ambient for maximum thermal transfer. The electrical interconnect between the die and transmission lines is not also the thermal relief path, and so the interconnect experiences less thermally induced mechanical stress. Interconnecting transmission lines are implemented on commercially available RF substrates similar to PCB implementations, but the HMIC provides a hermetic environment. The HMIC housing has all atmosphere evacuated, and then backfilled with nitrogen. As nitrogen is inert, there is no need for any protective coating. The chip and wire implementation also removes the need for solder mask.

Based on these observations, the research presented below was undertaken to produce an HMIC implementation of the UDC to improve reliability and environmental hardening.

1.2 UDC Subassembly Specifications

Tables 1 – 5 present the design specifications for the UDC subassembly. Table 1 gives the specifications in the transmitter or up-conversion path of the UDC subassembly, while table 2 presents the specifications for the receiver or down-converter path. Some of the key RF specifications are derived in section 3.1

Derivation of Key Specifications with the remaining specifications coming from interface requirements to the existing system. The interface specifications are from the Nanowave internal Interface Control Documents for the specific radar program to which the UDC HMIC will be interfaced.

Table 1: Specifications for up-conversion in the UDC HMIC subassembly.

Description	**Specification**	**Comment**
Operating Frequency (GHz)	Output (RF) Port: 9.3 – 9.5 GHz and 9.7 – 9.9 GHz	Based on allocated spectrum. [11]
	Input (IF) Port: 3.0 – 3.1 GHz	5 MHz channels, 100 MHz operating band [11]
	LO Port: 12.3 – 12.9 GHz	LO to move in steps of 100 MHz to integer mode operation of PLL [11]
Small signal gain (dB)	> 42.7 dB	Measured with IF P_{IN}= -20 $dB_{m.}$ See section 3.1.3.
Output P_{SAT} (dB_m)	>31.5 dB_m	See section 3.1.3.
Output Spurious (dB_c) (@fc ± 5 MHz)	< -50 dB_c	P_{IN}= +0.5 dBm See section 3.1.4.1.
Output Spurious (dB_c) otherwise	< -60 dB_c	P_{IN}= +0.5 dBm, measured out of channel
IF Return Loss (dB)	>15 dB	See section 3.1.4.2.
RF Return Loss (dB)	>13 dB	See section 3.1.4.2.

Table 2: Specifications for down-conversion in the UDC HMIC subassembly.

Description	**Specification**	**Comment**
Operating Frequency (GHz)	Input (RF) Port: 9.3 – 9.5 GHz and 9.7 – 9.9 GHz	Based on allocated spectrum. [11]
	Output (IF) Port: 3.0 – 3.1 GHz	5 MHz channels, 100 MHz operating band [11]
	LO Port: 12.3 – 12.9 GHz	LO to move in steps of 100 MHz to integer mode operation of PLL [11]
Small signal gain (dB)	> 26.6 dB	Measured with RF P_{IN}= -30 dB_m. See section 3.1.2.
Noise Figure	<3 dB	See section 3.1.1.
O_{P1dB} (dB_m)	> 5 dB_m	See section 3.1.2.
Output Spurious (dB_c)	< -50 dB_c	See section 3.1.4.1.
Input Return Loss (dB)	>15 dB	See section 3.1.4.2.
Output Return Loss (dB)	>15 dB	See section 3.1.4.2.

Table 3: Specification for DC bias/control PCB for HMIC subassembly.

Description	**Specification**	**Comment**
TX/RX Trigger Level	0 - +5 V TTL	Transmit is active high [11].
TX/RX Trigger Rise Time (ns)	< 100 ns	Based on system specification [11]
System STALO	Control PCB to include STALO	-
STALO Frequency (GHz)	12.4 – 12.9 GHz	Based on system specification [11]
STALO Output Power (dB_m)	-2 to +4 dB_m	-
STALO reference	PCB to lock to external Reference	Based on system specification [11]
STALO Ref Frequency (MHz)	50 MHz	50 MHz VCXO on PCB
Reference Absolute Pull Range (PPM)	± 20 after reflow, supply, temperature, and 10 years aging	Required to ensure system stability of ±20 ppm is achievable. Input reference has stability of ±17.05 ppm. [11]
RMS Jitter (fs)	500 fs	Allows a velocity measurement error of ±1 m/s in 99.7% of all velocity measurements. [11]
EXT Reference Input	10 MHz	Based on existing interface.
STALO Control Protocol	SPI	Based on existing interface.
DC Supply Voltage	+6 V_{DC}	Based on existing interface.
DC Supply Current	< 1.5 A	Based on existing interface.
DC Power Consumption	< 9 W	Based on existing interface.

Table 4: Mechanical specifications for UDC subassembly.

Description	**Specification**	**Comment**
RF Input Connector	SMA, Female	-
RF Output Connector	SMA, Female	-
IF Input Connector	SMA, Female	-
IF Output Connector	SMA, Female	-
EXT LO Input Connector	SMA, Female	-
EXT REF Input Connector	SMA, Female	-
Trigger Input Connector	SMA, Female	-
STALO Control Connector	12 lead rectangular connector	Must be shrouded and keyed.
Telemetry Data Connector	4 lead rectangular connector	Must be shrouded and keyed.
Mass	< 0.5 kg	Maximum mass; reduce as much as possible.
Maximum Dimensions (L x W x H, inch)	7” x 5“ x 1”	Maximum dimensions.

Table 5: Specifications regarding environmental conditions and reliability for UDC HMIC subassembly.

Description	Specification	Comment
Operating Temperature	-30ºC - +65ºC	-
Storage Temperature	-40ºC - +70ºC	-
Humidity	MIL-STD-202F, M103, Cond B [11]	-
Salt Fog	MIL-STD-202F, M101E, Cond C [11]	Unit to be deployed in a salt fog environment
Altitude	MIL-STD-202F, M105C, Cond B [11]	Unit to be shippable by air
Operating Life	10 Years	Continuous operation
MTBF	> 149,796 hours	Target system MTBF is 15 years. MTBF for UDC subassembly is calculated assuming when combined with MTBF of other subassemblies the system MTBF is greater than 15 years.

1.3 Context of UDC Subassembly in Terms of Radar System

The UDC subassembly is an intermediary subsystem between the IF and RF subassemblies. The IF interface of the UDC is connected to the DTX (digital transceiver) subassembly, which includes an SDR (software defined radio) and FPGA for received echo processing. The RF transmit interface is connected to the SSPA (solid-state power amplifier) and the RF receive interface is connected to the receiver port of the duplexer.

On transmission, the DTX unit outputs a 5 MHz channel in S-band, between 3.0 and 3.1 GHz. The DTX IF output is connected to the IF input of the UDC subassembly. The transmit IF signal is up-converted to X-band via mixing with a high-side STALO (stable local oscillator). The X-band RF output is connected to the SSPA via the RF output interface. The radar system is design to operate over a 100 MHz bandwidth, with the capability of re-banding the output in X-Band in 100 MHz steps between 9.3 – 9.5 GHz and 9.7 – 9.9 GHz through revision to other subassemblies. In order to minimize the component changes needed for re-banding the system, the UDC is to be able to meet its operating specification over all specified operating bands.

For the receiver, the returned echoes are transmitted from the antenna to the RF input port on the UDC. The signal is then amplified and down-converted from X-band to S-band. The UDC outputs 3.0 to 3.1 GHz from the IF output, back to the IF input on the DTX.

Figure 1: Radar system overview. (below) shows the connection on the UDC subassembly to the radar system. The figure is provided for context, but highly abstracted to maintain the confidentiality of system aspects not related to this thesis.

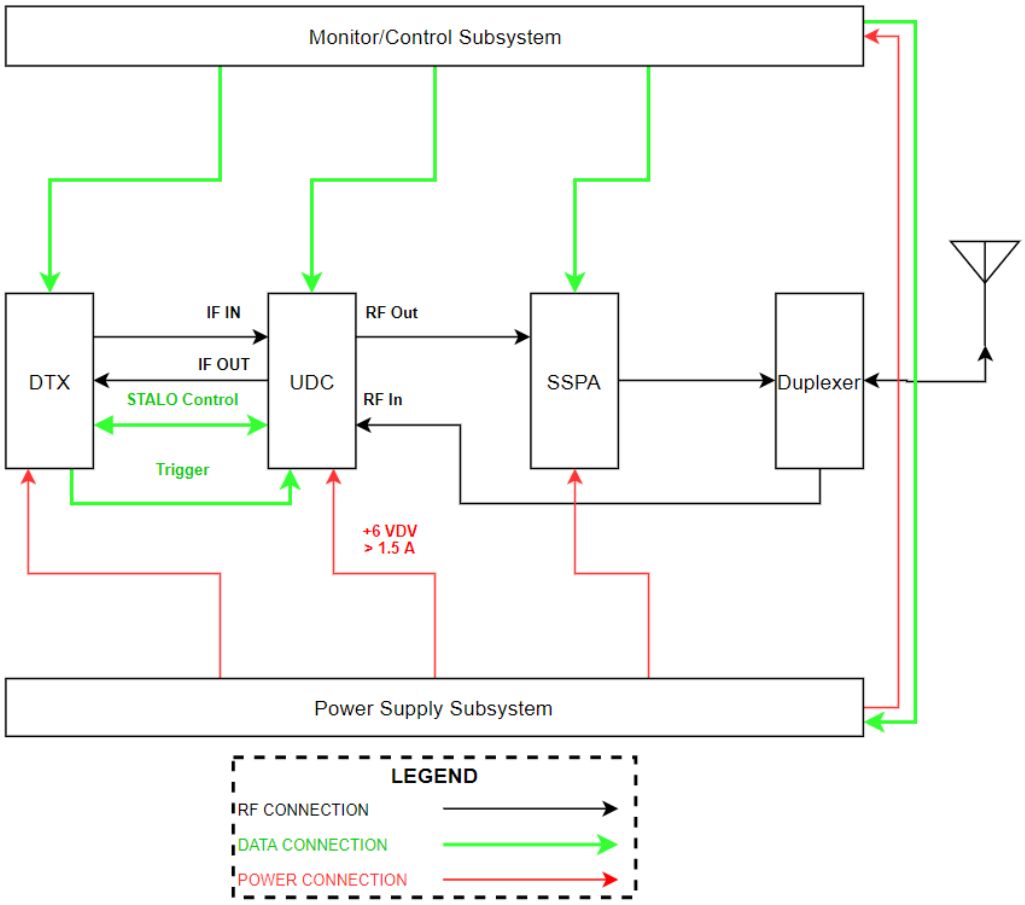


Figure 1: Radar system overview.

1.4 Challenges

The hardware developed for verification of the thesis faces four main challenges: wide storage and operating temperature ranges, long operating life, constraints on physical mass, and a need for economic viability. The following subsection discusses and contrasts these challenges with either an HMIC or PCB implementation of the UDC.

1.3.1 Operating/storage temperature range

The device overall radar system must operate from -30 ºC to +55º C without fault. However, due to the electronics enclosure existing in within a radome, it is expected that the actual operating environment would be approximately 10ºC warmer [12], meaning the UDC is expected to be subject to -20 ºC to +65ºC during operation. To ensure reliable operation, the operational temperature range of the HMIC increased the high temperature of the environmental range, while still allowing for operation at -30ºC to support a cold start. Thus, the specified operating range of the HMIC is -30 ºC to +65º C. In development of the PCB, the packaging of the die is handled by a third-party vendor. Consequently, the designer has less control the thermal interface from the die junction to ambient temperature. In the HMIC implementation, the thermal path from the die to the ambient temperature is tightly controlled. It is also worth noting that in the PCB implementation, SMT packages are mounted on a dielectric with poor thermal performance while in the HMIC implementation, there is a continuous metal path to ambient. While there are techniques to reduce the thermal resistance introduced by a PCB, a PCB based implementation will struggle to achieve the same thermal performance as an HMIC.

1.3.2 Radar operating life

The overall radar system is expected to operate continuously for 10 years. This means that the subassembly must function 10 years continuously without fault. A target MTBF of 15 years is used in the design, in order to provide margin on the reliability of the system. The reliability of the component is assessed with the

FIDES reliability analysis method, as MIL-HDBK-217 can be overly pessimistic in predicting device failures [13]. Based on the mission profile, the design should have a FIT (failures in time) value less than 6677 FIT, corresponding to an MTBF of 149,796 hours.

There were three main strategies to achieve this level of reliability.

- The RF components of the unit is hermetically sealed, with the interior atmosphere of the assembly replaced with an inert gas, thus ceasing any corrosion or degradation at a chemical or environmental level of the electronics. All DC bias and control electronics are on a PCB that is conformally coated. In a pure PCB implementation, there are significant hurdles to hermetically sealing the unit which are not present in the HMIC version.
- All passive devices will have all tolerances (voltage, current, or power) de-rated by 50%. This means that each device is treated as if maximum tolerance specified for the part were half the value given by the manufacturer.
- All capacitors will have a defined temperature rating of X5R or greater. This classification is a defined operating temperature where the first digit indicated the lowest operating temperature (X = -55ºC), the second digit represents the maximum temperature (5 = +85ºC) and the final character indicated % variance over temperature range (R = 15%) [15]. As thermal stress (applied temperature divided by rated temperature) is inversely related to MTBF or FIT, a capacitor less than X5R cannot be tolerated. X7R is preferred.

1.3.3 Mechanical Constraints

The mass of the overall system cannot exceed 40 kg. This is to ensure the ability of a 2-man installation in remote or hard to access areas. While the mass of the UDC has been constrained in the specification, the goal is to reduce the mass as much as possible below the specification to allow for margin on other subassemblies in the overall system design. The largest mass in this design is expected to be the mechanical housing, and so the main strategy to mitigate this challenge is to attempt to reduce the outer dimensions of the assembly as much as possible in the design.

1.3.4 Economic Constraints

In order to have the successful deployment and adoption of a distributed network of weather sensors, the systems must be designed to be economically viable. Producing a design for this subassembly within the existing Nanowave HMIC process provides economic advantages over PCB manufacture in several ways. The design will re-use as many existing Nanowave modules as possible. The benefit of this is two-fold; it reduces the manufacture cost by allowing for increased volume on existing product while also reducing engineering labour costs by reducing design time. This design also reduces future costs due to obsolescence mitigation, as if an individual die becomes obsolete only the individual module needs to be redesigned. In a PCB implementation, if there were no footprint compatible part it would force a redesign of the PCB to accommodate a new component.

1.5 Thesis Contributions

The following thesis contributions were the direct result from the research presented in this work:

- Derivation of effect of pulse compression radar on meteorological radar
- Demonstration of improved subassembly reliability of HMIC over PCB iteration based on analysis
- Design of an HMIC up-down converter for verification of environmental performance

1.6 Thesis Organization

The thesis is organized in the following manner. Chapter 2 contains theory required for the system analysis, including theory related to meteorological radar systems, cascaded RF systems, methods for reliability and environmental analysis, and an overview of the high reliability packaging methods to be used. Chapter 3 presents all the relevant system analysis done including derivation of key specifications from the theory presented in chapter 2, an RF analysis of the up converter stage, an RF analysis of the down converter stage, the thermal analysis of high powered components, and the reliability analysis of the system. Chapter 4 contains the specifics on the design of the subassembly. Chapter 5 contains the methodologies and results of all verification and testing on the design prototype. Chapter 6 draws conclusions on the sum of the work presented in all other chapters and discusses future work to be done.

2.0 BACKROUND INFORMATION

The fundamental purpose of a meteorological radar is to determine the rate of precipitation at a specific range. The figure of merit often used to compare meteorological radar systems is weather sensitivity. This value is the minimum resolvable reflectivity for a set distance. As the reflectivity is related to rate of precipitation, this is essentially the lowest precipitation rate that the radar can detect. Chapter 2 provides various theoretical information including a derivation of the meteorological radar equation, the theoretical effect of cascaded RF systems on noise and linearity, discussions on methods for reliability analysis, an overview of the HMIC process used for the design, and a discussion on verification of the results. The theory presented in this chapter is applied in Chapter 3 to determine the specifications for the UDC from the overall system specifications.

2.1 Weather radar Theory

Meteorological radar uses the same fundamental mechanisms as standard hard-target radar to observe a different phenomenon. The purpose of a hard target to observe reflections of the transmitted pulse off a large dominant scatterer in order to determine information about the scatterer such as range and velocity. In contrast, meteorological weather radar is used to observe the backscattered power of a multiple distributed targets within a defined volume of space in order to infer how much precipitation is falling within the region of measurement. Given the purpose of the weather radar is to measure precipitation, the key specification of a weather radar is the sensitivity; a requirement to be able to detect a minimum rainfall rate

at a specific range. To design a system with the required weather sensitivity, one must translate that sensitivity specification into key parameters of the RF hardware such as noise figure or linearity. To this end, a meteorological weather equation must be determined based on the standard radar equation for point targets, in order to equate rainfall rate to received RF power levels.

2.1.1 Revisions to the radar range equation for meteorological measurement

The following section provides a brief summary of work done in [14], which can be reviewed for more information on the topic. While this reference is less modern, it was selected due to the elegance and clarity demonstrated in presenting the material. It is worth noting, this is the classical work which has defined the field of point target and meteorological radar. Most work in the field since has focussed into digital signal processing and waveform design, and thus the hardware is not impacted. For that reason, this reference was chosen as the most appropriate to discuss the fundamentals of radar. The standard radar equation for power received off a point target is:

$$P_R = \frac{P_t G^2 \lambda^2 \sigma}{(4\pi)^3 R^4} \qquad (1)\ [14]$$

Where

$$P_R = power\ received$$

$$P_t = power\ transmitted$$

$$G = gain\ of\ antenna$$

$$\lambda = operating\ wavelength\ of\ radar$$

$$R = range\ to\ measurement\ \frac{cell}{target}$$

$$\sigma = cross - section\ of\ target$$

In order to adjust this equation for meteorological use, an adjustment must be made to the variable in the equation related to the cross section of the target. The target is no longer one dominant reflector, but instead a distributed target filling a volume. Therefore, the cross-section of the target can be redefined with (2).

$$\sigma = V \cdot \Sigma\sigma_i \quad (2)\ [14]$$

Where

$$V = the\ volume\ of\ measurement$$

$$\sigma_i = cross\ section\ of\ each\ independent\ scatterer\ in\ the\ volume\ of\ measurement$$

The volume of measurement (called the radar resolution cell) is defined in two dimensions by the cross section of main beam of the antenna, with the third dimension being the range resolution of the radar. Assuming a classical (non-pulse compression radar), the range resolution is given by (3), and the radar resolution cell is given by (4).

$$S_R = \frac{c\tau}{2} \quad (3)\ [14]$$

$$V \approx \frac{pi}{4}(R\theta_B)(R\phi_B)S_R \quad (4)\ [14]$$

Where

$$c = velocity\ of\ pulse\ propagation$$

$$\tau = duration\ of\ transmit\ pulse$$

$$\theta_B = horizontal\ beamwidth\ of\ the\ antenna$$

$$\phi_B = vertical\ beamwidth\ of\ the\ antenna$$

(4) includes a factor pi/4 to account for the elliptical shape of the antenna beam. A further correction is applied to this measurement, as the antenna pattern is applied to both the transmission and reception of the measurement pulse. Assuming a Gaussian-shaped antenna pattern and a resolution cell evenly distributed with precipitation, the resolution volume of the radar is given by (5).

$$V \approx 2ln2 \cdot \frac{pi}{4} \theta_B \phi_B R^2 S_R \quad (5)\ [14]$$

By combining (1), (2), and (5) and simplifying, the radar equation becomes:

$$P_{R_{AVG}} = \frac{P_t G^2 \lambda^2 \theta_B \phi_B c\tau}{2^{10} \cdot ln2 \cdot \pi^2 \cdot R^2} \cdot \Sigma\, \sigma_i \quad (6)\ [14]$$

Knowing that for a Gaussian beam shape:

$$G = \frac{\pi^2}{\theta_B \phi_B} \quad (7)\ [14]$$

The radar equation can be further refined by combining (6) and (7) into (8).

$$P_{R_{AVG}} = \frac{P_t G \lambda^2 c\tau}{2^{10} \cdot ln2 \cdot R^2} \cdot \Sigma\, \sigma_i \quad (8)\ [14]$$

2.1.2 Distributed cross-section of a Rayleigh scatterer

When an electromagnetic wave is moves through a region of objects with a diameter much less than the object, Rayleigh scattering occurs. This model for scattering is generally valid under the condition given in (9).

$$\frac{\lambda}{D} \gtrsim 10 \tag{9} [15]$$

Precipitation varies, but can be expected to be less than 4 mm [16], thus (9) is satisfied for most precipitation using meteorological radars operating at frequencies up to and including X-band, except during the heaviest precipitation [14]. Based on the back-scattered radiation from a Rayleigh scatterer, one can then define the cross section of a raindrop using (10).

$$\sigma_i = \frac{\pi^5 D_i^6}{\lambda^4} |k|^2 \tag{10} [14]$$

Where

$$D_i = diameter\ of\ rain\ drop$$

$$|k|^2 = \frac{E-1}{E+2}$$

$$E = dialectric\ constant\ for\ scatterer$$

We can now include this definition back into (8):

$$P_{R_{AVG}} = \frac{\pi^5 P_t G \lambda^2 c\tau}{2^{10} \cdot ln2 \cdot R^2} \cdot |k|^2 \Sigma\, D_i \tag{11} [14]$$

The result shown in (11) provides an interesting contrast between point targets and distributed targets; the receive power is inversely related to the square of the range in distributed targets as opposed to the 4th power of the range in the case of point targets.

2.1.3 Relating precipitation diameter and rainfall rate to radar sensitivity

Work done in [16] has allowed for an empirical relationship between the sum of the diameters of precipitation and the rainfall rate, defined before in (12).

$$Z = \Sigma D^6 = ar^b \qquad (12)\ [16]\ [14]$$

Where

$$Z = reflectivity\ of\ precipitation\ \left(\frac{mm^6}{m^3}\right)$$

$$r = rainfall\ fate\ \left(\frac{mm}{hr}\right)$$

$$a\ and\ b\ are\ determined\ empirically$$

While different values for a and b have been determined based on specific precipitation conditions [16], the generally accepted form of the equation is given by (13).

$$Z = 200r^{1.6} \qquad (13)\ [14]$$

Water has an approximate dielectric constant of $80\frac{F}{m}$, meaning $|k|^2 \sim 0.93$. Substituting this value and (13) into (11), there is now a relationship between received power and rainfall rate given in (14).

$$P_{R_{AVG}} = \frac{2.4 P_T G \tau r^{1.6}}{R^2 \lambda^2} \; x \; 10^{-8} \qquad (14)\ [14]$$

This equation now provides a direct link between rainfall rate, range, the radar system parameters, and the received power.

2.1.4 Attenuation by precipitation over measuring range

Over the range of particle sizes and frequencies where Raleigh scattering applies (see (9)) the attenuation due to absorption was approximated by Skolnik as shown in (15).

$$A = 0.434 \, \frac{\pi^2}{\lambda} \, \Sigma D^3 \; I_M(-k) \qquad (15)\ [14]$$

$$where\ the\ sum\ of\ particals\ is\ over\ 1\ m^3$$

$$D = partical\ diameter\ in\ cm$$

$$\lambda\ is\ wavelength\ in\ cm$$

$$k\ is\ the\ dielectric\ constant\ of\ water$$

2.1.5 Effect of pulse compression on meteorological radar range equation

Pulsed radar systems require a specific amount of energy reflected off a target for detection above the system noise floor. To accomplish this, often two parameters are traded against each-other during system design, pulse width and peak power.

Increasing the peak power or the pulse width will affect the total energy per a pulse, allowing for more energy to be reflected off a target for each transmitted pulse. The peak power is often limited by the design or technology, while the pulse width is limited by range resolution. In a radar not employing pulse compression, the range resolution is given by (3) in section 2.13.

Modern processing has allowed radars to decouple these two parameters using pulse compression techniques. By using a matched filter, a dispersive relationship between frequency and group delay can be created which compress the transmitted signal in time upon would receive. This allows for a wide pulse width on transmit, which can be compressed into a narrow pulse width on receive. As the energy in the pulse will remain the same, but the duration will decrease, the apparent power of the pulse will increase allowing for a higher returned power and a narrow duration (allowing for improved range resolution). The pulse width for a compressed pulsed is given below in (16).

$$S_{R_C} = \frac{c}{2B} \qquad (16)\ [14]$$

$$where\ B\ is\ the\ bandwidth\ of\ the\ transmitted\ pulse$$

The higher amplitude and narrower pulse also contribute to an improvement of SNR. The SNR is improved by the PCR (pulse compression ratio) given in (17).

$$PCR = \frac{S_R}{S_{R_C}} = \frac{\frac{c\tau}{2}}{\frac{c}{2B}} = \tau B \qquad (17)\ [14]$$

When a pulse compression radar is used as a weather radar, the meteorological weather equation must be updated accordingly. The range of the resolution cell is no longer defined by pulse width, but instead by the bandwidth of the transmitted pulse. Also, the improvement in SNR must be accounted for as discussed in [17]. The updated meteorological radar equation for a pulse compression is shown in (18). It is worth noting that pulse compression will provide a processing gain when compared to (14). (14) is the average power measured at the receiver. (18) is the detectible power after processing the received echo with a matched filter.

$$P_{R_{AVG}} = \frac{2.4PCR \cdot P_T Gr^{1.6}}{R^2 \lambda^2 B}\ x\ 10^{-8} \tag{18}$$

2.2 RF Systems Theory

Once the subassembly specifications have been derived from the weather radar theory given in section 2.1, the specification for each module can be determined by ensuring the cascaded equivalent of the blocks meets the specification. The effect of the cascaded gain is trivial; it is simply the sum of the logarithmic value of the gain of each block. The effects of non-linearity and noise are more consequential and need to be further examined.

2.2.1 Noise in RF systems

Noise creates the lower bound of dynamic range. Typically, it is not possible to recover signals below the noise floor. Every block in an RF system will contribute some noise, thus degrading the SNR of the system. For this reason, it is imperative

to understand sources of noise, and the effect of cascading RF blocks on the system noise floor.

2.2.1.1 Sources of noise

There are two main sources of noise in RF systems considered for this work. The first, and most common, is thermal noise. [18] As temperature is effectively particle motion, any electron in a system with temperature above absolute zero will undergo some random motion, producing a noise current. Across a fixed resistor, this will produce an average noise voltage according to (19) below.

$$N = \sqrt{4kTR} \tag{19}$$ [18]

$$where\ k\ is\ boltzmann's\ constant$$

The resultant units of (19) are $V/\sqrt{Hz}$. In order to determine the spectral power density, one can convert the result to power, and multiply by the finite bandwidth over which one intends to measure as shown in (20).

$$P_n = \frac{N^2}{R} \cdot B = \frac{\left(\sqrt{4kTR}\right)^2}{R} \cdot B = 4kTB \tag{20}$$

The result of (20) is the power spectral density of thermal noise in the system. This source of noise is considered important as it will drive the noise floor of the system and is a key parameter for understanding the weather sensitivity of the radar.

Another key source of noise in RF systems, especially relevant in a frequency converter, is phase noise from the STALO. An ideal STALO would only produce

energy in the desired tone. However, instantaneous variations in phase will exist due to external effects on the STALO causing some power to appear locally in the frequency domain surrounding the STALO. The effect of this is a spectral degradation of the signal, which can cause power in adjacent channels as well as instantaneous phase errors on transmitted/received signals. In the specific application, velocity measurements are made using the pulse-pair processing algorithm presented in [17]. This algorithm compares the returned phase in each sample of the measurement against the last measurement. If a detected target has not moved, the phase should be the same as the path length is the same. If the target has moved, even slightly, a phase shift will be observed between the current and previous measurement, which can be used to calculate the Doppler frequency and in turn the velocity. Any phase error generated by the STALO would cause a phase shift between each measurement, thus corrupting the velocity measured by the pulse-pair processing. The peak phase error of the STALO will determine the accuracy of velocity measurements in the radar.

2.2.1.2 Figures of merit for noise in RF systems

The effect of an RF block on the system noise floor is characterized by a parameter called the noise figure (or the logarithmic equivalent called noise factor). The noise figure is a measure of how much the SNR of the system was degraded by the RF block as shown in (21).

$$F = \frac{SNR_{OUT}}{SNR_{IN}} \quad (21)\ [18]$$

2.2.1.3 Cascaded noise figure

The effective noise figure of multiple cascaded RF blocks can be calculated using the noise figure and gain of each individual block using (22).

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 \cdot G_2} + \cdots + \frac{(F_n - 1)}{G_1 \cdot G_2 \cdot G_3 \ldots G_{n-1}} \quad (22)\ [19]$$

From this equation, one can see that the noise contribution of each block in a cascaded system is reduced by the gain of the preceding blocks. For this reason, the noise contribution of the first block is the most relevant in determining the system noise figure, provided it has sufficient gain.

2.2.2 Cascaded linearity in RF systems

As noise provided the minimum bounds for the system SNR, the linearity of the system provides the maximum bound. The figure of merit used in this work to characterise the linearity of the system is OIP3. The cascaded OIP3 can be calculated by assuming a truncated power series model for device non-linearity. With two cascaded devices with non-linearity, they will have voltage transfer functions given by (23) and (24) respectively:

$$vo_a = k_{a1} \cdot v_i + k_{a2} \cdot v_i^2 + k_{a3} \cdot v_i^3 \quad (23)\ [18]$$

$$vo_b = k_{b1} \cdot v_i + k_{b2} \cdot v_i^2 + k_{b3} \cdot v_i^3 \quad (24)\ [18]$$

Using (23) as an example (which is the same in (24) by symmetry), one can examine what happens when 2 tones are injected to the system.

$$Let\ v_i = v_1 cos\omega_1 t + v_2 cos\omega_2 t = X_1 + X_2 \quad (25)\ [18]$$

By substituting (25) into (23), it becomes apparent that the third order modulation terms is produced by expansion of the third term of the power series along with harmonic distortion:

$$k_{a3} \cdot v_i^3 = k_{a3}(X_1^3 + 3X_1^2 X_2 + 3X_1 X_2^2 + X_2^3) \quad (26)\ [18]$$

While X_1^3 and X_2^3 will produce other harmonics, they will not produce mixing terms. Therefore the third order terms are $3X_1^2 X_2$ and $3X_1 X_2^2$. This is apparent when X is substituted with a sinusoid:

$$\begin{aligned} 3(cos\omega_1 t)^2 \cos\omega_2 &= \frac{3}{2}(1 - cos2\omega_1 t)cos\omega_2 t \\ &= \frac{3}{2}cos\omega_2 t - \frac{3}{2}\cos\omega_2 t \cdot \cos2\omega_1 t \end{aligned} \quad (27)$$

The final term in (27) provides the mixing term which generates the third intermodulation distortion.

$$IM_3 = \frac{3}{2}(cos\omega_2 t \cdot cos2\omega_1 t) = \frac{3}{4}(\cos\omega_2 t \pm cos2\omega_1 t) \quad (28)$$

Thus, the amplitude of the third order intermodulation can be related to the input voltage and power series coefficients by (29):

$$v_{ip3} = \frac{3}{4}k_3 v_i^2 v_2 \quad (29)\ [18]$$

From this same expansion, one can conclude that the amplitude of the fundamental based on the terms contributing to the fundamental tone assuming $v_1 = v_2 = v_i$. This is given in (30).

$$v_\omega = k_1 v_i + \frac{9}{4} k_3 v_1^3 \quad (30)\ [18]$$

The linear component of the output is given by the first term, and the IM3 component by the second. At the third intercept point, the contribution to the output amplitude of these two components are equal. Therefore, v_{ip3} can be solved by setting these two terms equal to another and solving for v_i.

$$k_i v_i = \frac{9}{4} k_3 v_i^3 \quad (31)\ [18]$$

$$v_i = v_{IP3} = 2\sqrt{\frac{k_1}{3|k_3|}} \quad (32)\ [18]$$

We can now apply the result above to calculate the effective third order intercept point for multiple cascaded RF devices. Let us assume one has two devices; the output voltage of the series combination of these two devices would be given by (33):

$$v_o = k_{a1}k_{b1}v_i + (k_{a2}k_{b2} + k_{ai}^2 k_{b2})v_i^2 + (k_{b1}k_{a3} + 2k_{b2}k_{a1}k_{a2} + k_{b3}k_{ai}^3) + \cdots \quad (33)\ [18]$$

By taking the third term of (33), once can solve for the effective v_{iip3}:

$$v_{iip3} = 2\sqrt{\frac{k_{a1}k_{b1}}{3|k_{b1}k_{a3} + 2k_{b2}k_{a1}k_{a2} + k_{b3}k_{a1}^3|}} \quad (34)\ [18]$$

Inverting and squaring the above equation yields:

$$\frac{1}{v_{iip3}^2} = \frac{3}{4}\left(\frac{|k_{b1}k_{a3}|}{k_{a1}k_{b1}} + \frac{|2k_{b2}k_{a1}k_{a2}|}{k_{a1}k_{b1}} + \frac{|k_{b3}k_{a1}^3|}{k_{a1}k_{b1}}\right) \quad (35)\ [18]$$

This expression can be simplified using the following assumptions:

- k_{a2} and k_{b2} are small compared to the first order terms.
- All the blocks in the cascaded series have the same system impedance, and therefore the squared voltages can be interpreted as power.

This results in (33) which can be used to find the effective third order modulation point of the system:

$$\frac{1}{IIP3} = \frac{1}{IIP3_1} + \frac{G_1}{IIP3_2} + \frac{G_2}{IIP3_3} + \cdots \quad (36)\ [18]$$

2.3 Method for Reliability Analysis

In order to ensure the suitability of the design as a high-reliability mission-critical component, an analysis must be done during the design phase to predict the failure rate of the UDC. As previously stated, the selected method for reliability analysis is FIDES. FIDES analyzes the reliability of the system on two tiers. The first is contributions to the reliability based on manufacturing process. This includes

factors such as (but not limited to) the manufacturers expertise in assembling the product, the processes the manufacturer has in place for quality control, and the quality of suppliers used by the manufacturer for componentry. The second assessment is based on the strains applied to the assembly undergoing the analysis. This is further broken down into three categories; a mission profile, stress factors based on application, and strains on the specific components in the system. Different models are used by the software for SMD components in a PCB system as opposed to die components in hybrid chip and wire system.

The mission profile is set up to capture the life cycle of device being analyzed. This analysis breaks the operation of the device into smaller periodic cycles, capturing the ambient temperature, the temperature variation during each cycle, the on/off state during the cycle, and the exposure to humidity, vibration, and chemical pollution during each cycle. For this application, there is expected to be high humidity and saline pollution due to deployment in marine environments. The hermeticity of the HMIC process improves the reliability of the system by lowering the impact of humidity and chemical pollution exposure.

Stress factors based on application try to capture risks associated with how a component or subassembly is used. This includes factors such as whether the system is mobile or stationary, the exposure to human interaction, the level of disturbance expected on the power supply network, the qualification of the users that may interact with it and the protection from weather. As both possible UDC configurations are used in the same manner, there is little variation to be expected here.

Finally, the specific voltage and temperature strains of each component are considered based on the mission profile. This analysis considers each component, represented by a statistic model based on component type, and various information about the component. For example, if the component were a capacitor, it would consider the dielectric type, any thermal ratings (i.e., X7R, X5R), and the voltage-capacitance product. As the entire thermal path from die to ambient is controlled by the designer in the HMIC configuration, there should be reduced operating junction temperatures of the device resulting in a higher reliability system.

Based on the input data, the FIT for each component is calculated using various statistical models, and then summed to give the FIT for the system. As many statistical models are used for calculation of reliability of various components, the specific calculation for each component is considered to be outside the scope of this work. Information on the specific method for calculation of reliability at the component level can be found in [20]. FIT is defined in [20] as failures in 10^9 hours. This is converted to MTBF assuming all failures are spaced equally in time using (36).

$$MTBF = \frac{10^9\ hours}{FIT} \tag{36}$$ [20]

As a failure in any component is considered a failure for the system, the system MTBF can be derived as the sum of the FIT of each subassembly converted to MTBF using (36).

2.3.1 Methods for Improving reliability

Assuming the environmental conditions are fixed, there are two methods that can be used to improve reliability: reducing thermal strain or adding redundancy.

2.3.1.1 Use of redundancy to improve device reliability

As any failure in the system would correspond to a system failure, it can be observed that the sum of the failures in time for each component would be generate the expected failures in time for the system. In (36) is shown that MTBF and FIT are inversely proportional. Therefore while the FIT of a system will increase if the fit of multiple critical components is considered where any component failure constitutes a system failure. In terms of MTBF, the combination of the MTBF of critical components will result in the system MTBF given below in (37):

$$\frac{1}{MTBF_{SYSTEM}} = \sum_{n=1}^{n=m} \frac{1}{MTBF_{COMPONENT_n}} \tag{37}$$

In the case a component was introduced with the same expected FIT which provided redundancy to a critical component, it would now take 2 failures (failure of the primary, and failure of the redundant component) in order to cause a system failure, and so the number of failures of the system would be expected to be reduced by a factor of 2. Based on (36), a factor of 2 reduction in FIT corresponds to an increase in MTBF by a factor of 2. Thus, adding passively redundant componentry can improve the reliability of the subassembly. However, if an active circuit is required to handle a switch-over to the redundant component, the MTBF of the switch-over equipment will have to be included in the system analysis calculated

by (37), and so the benefit to the system MTBF will be proved, but not ideally halved for active redundancy.

2.3.1.2 Reducing component stresses

The reliability of components is proportional to the ratio of applied stress (such as voltage, operating temperature, power dissipation, etc) to the component rating for that stress [22]. Therefore, either reducing the stress across components or selecting components with higher ratings will improve the reliability of the device.

2.4 Ruggedized Packaging Methods

The presented thesis is that a chip and wire HMIC assembly will provide better environmental performance, and higher reliability over the life of the designed subassembly. The HMIC process to be used is a proprietary process developed by Nanowave Technologies. This process involves automated installation of RF die alongside internally fabricated thin film networks which are reflowed to the same continuous housing [21]. Die are attached using AuSn solder to copper carriers which are screwed down to the main housing and then wire bonded to adjacent thin film networks for connectivity. The housing is then laser sealed using a 500W YAG laser, fusing the lid and housing [22]. This creates a seal with a leak rate of less than $10^{-8}\ atm \cdot cm^3/sec$, exceeding the hermeticity requirements of MIL-STD-883 [23]. This makes the unit impervious to the effects of condensation and corrosion, allowing reliable operation in marine environments. This level of hermeticity will provide improved performance compared to the PCB implementation which is exposed directly to the operating environment. The atmosphere in the intended

operating environment is high in moisture and saline pollution, which are highly corrosive. Any material directly exposed, such as the SMD components and traces on the PCB implementation will suffer corrosion in the intended environment of operation. After a 14-day environmental test in a thermal chamber of the PCB version, corrosion was observed on RF transmission lines. It is worth noting that this environment did not include saline pollution, and this exposure is much less than the intended 10-year life of the system. Hermeticity will remove the impact of the environments atmosphere on the operation and health of the UDC, allowing an improved environmental performance compared to the PCB.

The packaging also provides thermal advantages, as the die is directly soldered to a metal carrier, which is in direct contact with the housing, allowing a low thermal resistance from junction to ambient. With proper thermal design, this allows for very high-performance systems.

The technology also improves EMI (electromagnetic interference) immunity and improved isolation between internal RF circuits as each circuit is implemented in a cavity inside a complete metal housing. Due to this, there is a high level of shielding between nearby circuits, and a high level of shielding preventing external interference.

All DC components are included on a bias PCB to which the HMIC is mounted and connected using hermetic feedthrough pins. As all RF components have been removed from this PCB and placed in the HMIC assembly, the PCB can now be conformally coated with urethane to protect from corrosion.

2.5 Methods for Verification

An acceptance test procedure for the UDC has been defined, based on the subassembly specification document in order to determine if the final product meets the original specifications discussed in section 1.2. All specifications are tested over temperature corners, using a compact thermal chamber. If the design passes the initial acceptance test, an accelerated life test will be performed over which the design will be subjected to diurnal temperature variation significantly exceeding what it is expected to withstand in standard operation. All key parameters will be monitored and verified after this testing.

3.0 SYSTEM ANALYSIS

In this chapter, the system level analysis is done to determine the specifications of the individual RF modules. In order to do this, relevant sub-assembly specifications are derived using the theory presented in section 2.1, and then a system level design is completed of the RF portion of the subassembly using the theory presented in section 2.2. Thermal analysis of all active device in the subassembly is provided, as well as reliability analysis based on the FIDES [24] methodology.

3.1 Derivation of Key Specifications

In this section, various specifications are derived from the existing radar system.

3.1.1 Minimum detectible signal and noise figure

In meteorological radar, the minimum detectible signal is calculated from the weather sensitivity specification. This is the theoretical reflectivity that could be detected above the noise floor at a specific distance. The specification for the weather sensitivity of the radar system is 23 dBZ @ 30 km range [25]. Rearranging (12), the rainfall rate corresponding to 23 dBZ can be calculated.

$$r = \left(\frac{10^{\frac{23}{10}}}{200} \right)^{\frac{1}{1.6}} = 0.9985\ mm/hr$$

From this value, one can then calculate the expected received power based on the range and rainfall rate using (16) and the specification for the weather radar.

$$P_r = \frac{2.4 \cdot PCR \cdot P_T \cdot G \cdot 0.9985^{1.6}}{R^2 \lambda^2 B} \; x\; 10^{-8} = 1.965x10^{-13}\; W = \; -97.8\; dB_m$$

As process, supply and environmental variation can degrade the noise figure of the solution, a minimum signal approximately 3 dB lower of -101 dB_m was selected for the design. Having this value, the required noise figure of the system can now be determined. This analysis makes the following assumptions:

- The minimum detectible signal is measured at the output port of the antenna. As such, the losses of cabling, limiter, and the duplexer must be considered.
- The maximum 99% OBW (occupied bandwidth) of the received signal falls within a 5 MHz bandwidth. This is assumed, as the final stage has a brick-wall FIR filter which will eliminate all frequency content out of the 5 MHz bandwidth.
- The UDC provides sufficient gain to make the noise contribution of the following digitizer negligible. Given the NF of the digitizer is 5 dB, and the gain of the UDC is > 26.6, this is a valid assumption.

Based on the preceding assumptions, the system noise floor can be calculated using (18).

$$P_n = kTB = 1.3807x10^{-23}\; JK^{-1} \cdot 293\; K \cdot 5MHz = 2.0227\; x\; 10^{-14}\; w$$
$$= \; -106.9\; dB_m$$

The attenuation of the duplexer, cabling loss, and limiter will reduce the available signal power from the antenna port to the receiver, effectively reducing the system SNR by the value of their attenuation. The loss associated with the duplexer, cabling and limiter are 1 dB, 0.5 dB, and 1.5 dB respectively. The remaining

difference between the noise floor (including the previously stated losses) and the required minimum detectible signal is the required noise figure of the receiver.

$$NF_{Receiver} = -106.9\ dB_m + 1.5\ db + 0.5\ db + 1\ dB - (-101\ dB_m) = 2.9\ dB$$
$$\approx 3.0\ dB$$

Given the earlier margin given to the minimum detectible signal, approximating the noise figure of the receiver to 3 dB is acceptable. As such, the design will target a maximum noise figure of 3 dB.

3.1.2 Receiver gain and linearity

The linearity of the receiver is limited by the digitizer subassembly, which has a maximum IIP3 of 14 dBm, corresponding to an input referenced 1 dB compression point of approximately 4 dBm. The output referenced 1 dB compression point of the UDC shall be set to 5 dBm to keep the UDC from limiting the linearity of the system.

Selecting the gain of the system is more complex. The goal would be to set the highest gain possible to achieve to maximize noise performance, without causing distortion or damage to components. This would be measured at the shortest range of the longest pulse. This is further complicated by the fact that at heavy rainfall rates, the size of hydrometers becomes comparable to a wavelength at X-band, which means that Ryleigh scattering is no longer a valid model for back-scattered power. As such, the linearity of the system will also be limited by the actual rainfall rate, as higher rainfall rates would be under-reported by the meteorological radar

[14]. For this, the gain is calculated on the receiver making the following assumptions:

- A moderate rainfall rate was selected to ensure the validity of Ryleigh scattering model used in the meteorological radar equation. According to the US geological survey, moderate rainfall is 3 mm/hr. [26]
- The radar is blinded during transmission due to the limiter in the receive path becoming active. The time the transmission takes to finish, as well as the time it takes the limiter recover will correspond to a close in distance from the transmitter over which the radar cannot receive an echo, known as the blind range. The blind range is calculated by the blind time, multiplied by the speed of propagation over 2. The blind range of the radar is the range corresponding to the pulse length plus 1 μs (to allow the limiter to fully recover), which would be 5.996 km.
- Cabling, duplexer, and limiter losses are combined 3 dB.
- The transmitted signal is using a hanning window, with a processing loss of 3.74 dB [27]
- The maximum pulse duration is 39 μs.
- Pulse compression will not be considered, as this is the linearity before processing in the matched filter.
- Path loss attenuation in the blind range will not be considered. While it is unlikely to have a moderate rainfall exactly at the edge of the blind range with no rainfall occurring in the blind range, it is possible and therefore represents the worst case for received power.

Based on these assumptions, the received power would be:

$$P_{R_{AVG}} = \frac{2.4 P_T G \tau r^{1.6}}{R^2 \lambda^2}\ x\ 10^{-8} = \ -6.796\ x\ 10^{-6} w = \ -21.677\ dBm$$

As this power represents the maximum linear received power before the rainfall rate limits the linearity of the measurement, the gain can be as such so that as this input power, the output power is the P1dB point of the UDC subassembly.

$$G = 5\ dB_m - (-21.68\ dB_m) = 26.68 dB$$

3.1.3 Transmitter gain and linearity

The linearity and gain of the transmitter section of the UDC is more straight forward to calculate. The power level required at the input of the SSPA is 31.5 dBm. Assuming cabling losses of 0.5 dB between the UDC and SSPA subassemblies, an output power of 31.5 dBm is required from the UDC. In order to maximize efficiency and provide stability over operating temperature, the final stage of the UDC should be operated in saturation. Assuming the device is to operate 3 dB into compression, the output referenced one dB compression point for the UDC can be set to 29 dBm.

Assuming the output is 3 dB into compression at 31.5 dBm with an input of -8.15 dBm, the small signal gain would have to be:

$$G = 32\ dB_m - (-8.15\ dB_m) + 3\ dB = 42.65\ dB$$

3.1.4 Other Specifications

The following other specifications have come from regulatory requirements or have been selected based on good practice.3.1.4.1 Spurious

3.1.4.1 Spurious

Based on the licensing available for the radar in its intended country of operation, a spurious of –50 dBc is allowed within the operating channel (fc±5 MHz), and -60 dBc otherwise. This specification was applied to the transmitter only. The receiver will have more generous -50 dBc spurious across the entire spectrum.

3.1.4.2 Return Loss

The return loss for the IF input/output ports was set to 13 dB, as these ports are relatively low power a lower return loss specification can be tolerated (as less VSWR would be expected). The RF input/output ports are specified to have better than 15 dB return loss. This is especially important on the RF output, which is higher power as significant VSWR could cause damage to the connected subassemblies. The RF input from the antenna is also set to 15 dB return loss, however a worse return loss may be tolerated if required for noise performance.

3.1.4.3 DC Power Consumption

A limit of 1.5 A at 6 VDC is available from the main power supply subassembly for this unit.

3.1.4.4 STALO Reference Frequency and System Frequency Stability

The STALO used in frequency conversion must accept a 10 MHz reference, as this reference is already available in the system. The STALO PCB may use the 10 MHz reference directly, or phase lock a secondary VCXO to the incoming reference as required. The overall frequency error at the output of the system cannot exceed 200

kHz or 20 ppm at the output operating frequency to comply with the frequency allocation; any VCXO must be selected considering this constraint.

3.1.4.5 STALO Jitter

The average velocity of the measured distributed target can be measured by comparing the phase change between the same samples on concurrent measurements. As this represents the change in phase over time, it allows the direct inference of the Doppler frequency as given in (37) with Δ_ϕ given in radians.

$$f_{doppler} = \frac{\Delta_\phi}{2\pi \cdot PRI} \tag{37}$$

This allows the calculation of the tangential velocity using (38).

$$v = \frac{f_{doppler} \cdot c}{2f_{transmtted}} \tag{38} [14]$$

Combining (37) and (38) we can now relate phase change between measurements to velocity.

$$v = \frac{\Delta_\phi \cdot c}{4\pi \cdot PRI \cdot f_{transmitted}} \tag{39}$$

If measuring a static object, such as ground clutter, Δ_ϕ should be zero. However, between concurrent pulses, the phase noise of the STALO is no longer uncorrelated. Between pulses one and two, Δ_ϕ may be as large as the phase change caused by the peak to peak jitter. The phase error can then be calculated using (40).

$$\phi_e = 2\pi \cdot \frac{jitter_{p-p}}{f_{transmitted}} \tag{40}$$

Substituting ϕ_e for Δ_ϕ in (40), v_e for v, and rearranging to solve for peak jitter, one comes to (41) which provides the jitter expected for a particular maximum velocity error, v_e.

$$jitter_{p-p} = \frac{2 \cdot v_e \cdot PRI}{c} \tag{41}$$

To now determine the peak to peak jitter tolerable from the STALO, one can substitute in an acceptable velocity error for a specific PRI. As a lower value of jitter is increasingly difficult to achieve technically, the worst case would be the shortest PRI of the system, in this case 500 µs. Therefore, for an acceptable error on the velocity measurement, of ±1 m/s, the system can tolerate a peak to peak jitter of 3.33 ps.

Assuming the peak jitter is half the peak to peak jitter, and the measurement error should be within 3 sigma (or within the specified error 99.7% of all measurements), the RMS jitter would need be one sixth the peak to peak jitter, or 555.56 fs. Therefore, the specification was set to 500 fs rms jitter to ensure a measurement error of ±1 m/s in 99.7% of all velocity measurements based on the phase error incurrent by the UDC.

It is also worth noting that phase noise from the STALO will be translated on to the transmitted signal. Thus, the phase noise from the STALO will spread into adjacent

spectrum and is a driving factor for adjacent channel power. As there is no regulatory requirement to address this, it was not seriously considered in the design.

3.2 RF System Overview

The design of the system was done using commercially available die, implemented in existing Nanowave HMIC modules when possible to minimize module level design. Modules are named using their existing Nanowave part numbers. Some modules contain COTS (commercial off the shelf) die as the active component. The part-numbers have been with-held as it is considered proprietary by Nanowave Technologies. The block diagram for the RF system is given below in figure 2. The selection of each module is justified in the following sections.

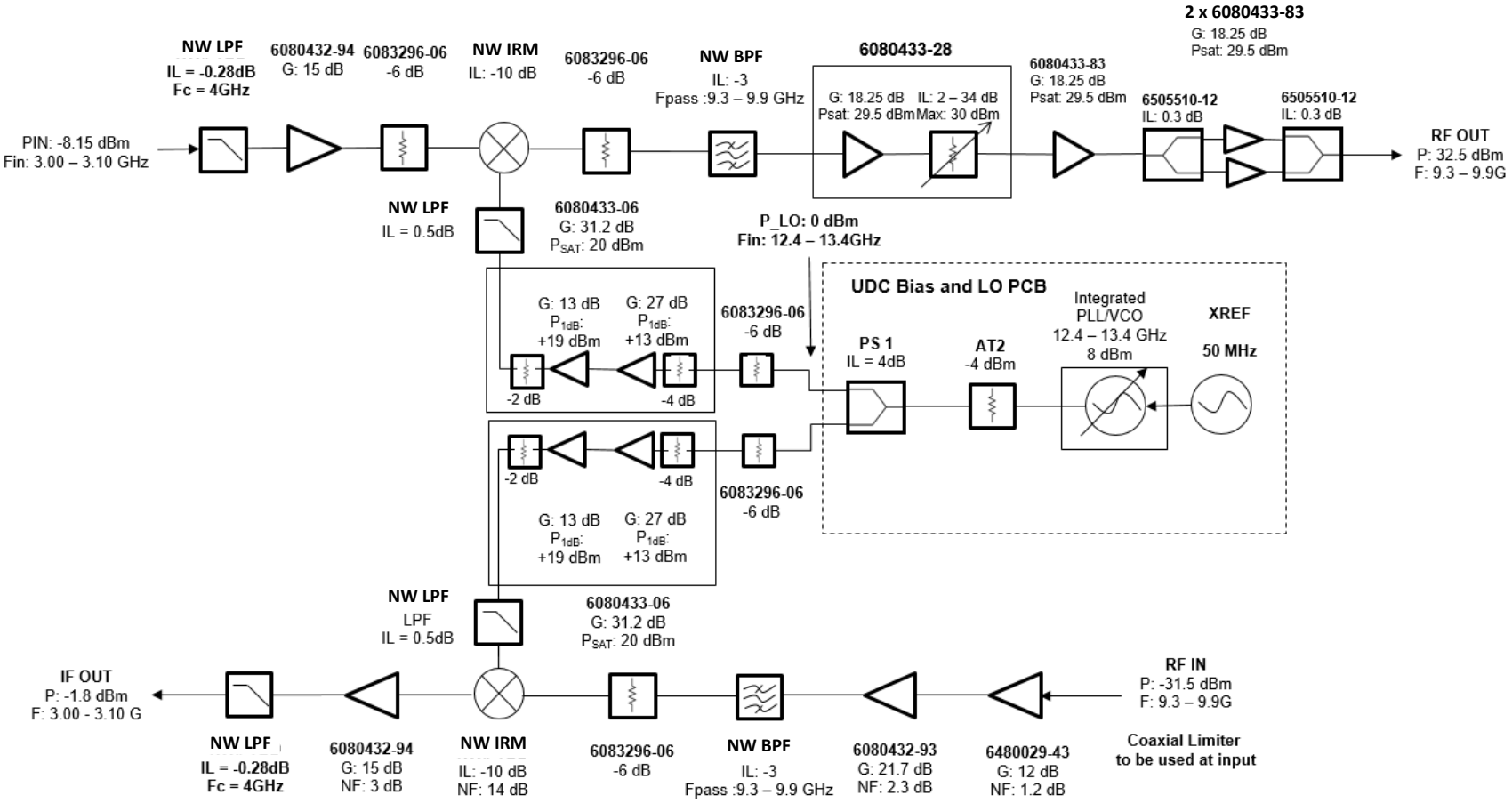


Figure 2: System block diagram.

3.2.1 Analysis of Down-Converter Stage

The justification for selection of components and RF budget for the down-converter stage is covered in detail in the following section.

3.2.1.1 Low noise amplifier selection

For the LNA stage of the up-converter, the 6080029-43 module was selected. The module is a single stage common drain amplifier using a COTS (commercial off the shelf) GaAs FET. The module uses a hybrid couple to feed two LNAs in parallel. These outputs are geometrically isolated with respect to the inputs, as the differential phase shift due to line length is always 180º. Thus any reflection off of the LNA due to poor matching will be out of phase at the antenna port, thus improving the apparent match and stability. This comes at the cost of the coupler losses directly degrading the noise figure. This module was selected as the FET can provide a typical noise figure of 0.5 dB. This module is then paired with 6080432-93, containing a COTS MMIC LNA. The latter module has a higher noise figure of 1.5 dB, but also a much higher gain of 24 dB. This LNA pair will ensure a low initial noise figure with high gain, thus significantly reducing the impact of all following RF stages on the system noise figure.

3.2.1.2 Band-select filter

A band select filter is required to reject signals in the image band from interfering with the operation of the radar. As the spurious specification for the receiver is -50

dB_c, and the mixers to be used provide a typical 25 dB of image rejection, the image reject filter should provide a minimum 25 dB of rejection in the image band. The specifications for the band select filter are given below in Table 6: Specifications of band-select filter.

Table 6: Specifications of band-select filter.

Specification	**Value**	**Comment**
Passband Frequency	9.3 – 9.9 GHz	Cover operational band of UDC
Passband Amplitude Variation	< 0.5 dB	
Image band rejection	> 30 dB	
Insertion Loss	< 3dB	
Return Loss	> 10 dB	
Characteristic Impedance	50 Ω	

As no existing Nanowave filter module is available meeting comparable specifications, this module had to be designed. See section 4.2 Band-Pass Filter Design for more information on the design.

3.2.1.3 RF attenuator

As the filter design assumes a wideband 50-ohm port, an RF attenuator was added between the filter and the mixer to ensure the transfer function of the filter behaves as designed. The selected attenuator is 6083296-06, which uses deposited thin-film resistors to generate a 6 dB pi-pad attenuator.

3.2.1.4 IR Mixer

A COTS MMIC (monolithic microwave integrated circuit) die was selected as the die is stocked by Nanowave and it meets the frequency requirements. No module

was available that allowed for an LO input at Ku band however, so a revision to an existing module was undertaken to revise the transmissions lines to support higher frequency. An image reject mixer was selected to reduce the amount of power transmitted in the image band, reducing the attenuation requirement of the band-select filter. The hybrid coupler requires the specification given in Table 7: Specifications of hybrid-coupler in order to meet the image rejection capable by the IR mixer.

Table 7: Specifications of hybrid-coupler

Specification	**Value**	**Comment**
Operating Frequency	3.00 – 3.10 GHz	IF frequency range.
Amplitude balance	$\lesssim 0.5$ dB	Based on recommendation from IR mixer datasheet.
Phase balance	$\lesssim 3.4^{\circ}$	Based on recommendation from IR mixer datasheet.
Loss	$\lesssim 0.3$ dB	
Port Isolation	≥ 20 dB	Based on recommendation from IR mixer datasheet.
Characteristic Impedance	50 Ω	

No Nanowave module was available to meet the above specifications, so a new module was designed for this project. More information regarding the design of the module is available in section 4.1 Hybrid Coupler Design.

3.2.1.5 IF Amplifier

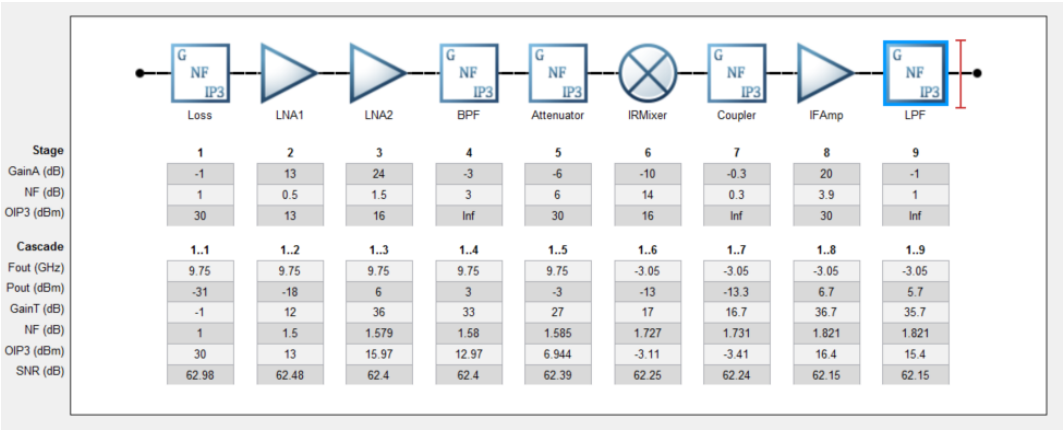
The IF amplifier was selected to make up the remainder of the gain required for the receiver. The Nanowave module number 6080432-94 was selected as it provided reasonable gain at the desired operating frequency.

3.2.1.6 IF Low pass filter

A low pass filter was included to eliminate any harmonics produced for the IR mixer. An existing Nanowave design with a 3 dB cut off frequency of 4 GHz and an insertion loss of < 1 dB was available.

3.2.1.7 RF budget for down converter

A cascade analysis was conducted using the theory presented in section 2.2 and the RF Budget Analyzer tool [28] in MATLAB with the results presented in Figure 3: Ideal RF Budget analysis of down-converter based on die specifications. The analysis includes a 1 dB loss for interconnect (connectors, transmission lines and wire bonds to die) in an attempt to give a more physical representation of the noise figure. The result predicts the system gain to be 35.7 dB, and the noise figure to be 1.82 dB. As this is based off the specification of the die, it is assumed that all the interconnect between them will degrade performance reducing gain and increasing noise figure.



Stage	1	2	3	4	5	6	7	8	9
GainA (dB)	-1	13	24	-3	-6	-10	-0.3	20	-1
NF (dB)	1	0.5	1.5	3	6	14	0.3	3.9	1
OIP3 (dBm)	30	13	16	Inf	30	16	Inf	30	Inf
Cascade	**1..1**	**1..2**	**1..3**	**1..4**	**1..5**	**1..6**	**1..7**	**1..8**	**1..9**
Fout (GHz)	9.75	9.75	9.75	9.75	9.75	-3.05	-3.05	-3.05	-3.05
Pout (dBm)	-31	-18	6	3	-3	-13	-13.3	6.7	5.7
GainT (dB)	-1	12	36	33	27	17	16.7	36.7	35.7
NF (dB)	1	1.5	1.579	1.58	1.585	1.727	1.731	1.821	1.821
OIP3 (dBm)	30	13	15.97	12.97	6.944	-3.11	-3.41	16.4	15.4
SNR (dB)	62.98	62.48	62.4	62.4	62.39	62.25	62.24	62.15	62.15

Figure 3: Ideal RF Budget analysis of down-converter based on die specifications.

3.2.2 Analysis of Up-Converter Stage

The justification for selection of components and RF budget for the up-converter stage is covered in detail in the following section.

3.2.2.1 IF Low Pass Filter

The purpose of the low pass filter is to prevent any harmonics from the preceding digital stage. The low-pass filter is to have the same characteristics as the low pass filter specified in section 3.2.1.6 IF Low pass filter

The IF amplifier was included to provide gain before various lossy components. The selected IF amplifier was 6080432-94 as it was suitable and maximized component re-use.

3.2.2.3 IF Attenuator

An IF attenuator in included at the input of the mixer to ensure a good VSWR at the IF input port. The selected attenuator is 6083296-06, which uses deposited thin-film resistors to generate a 6 dB pi-pad attenuator.

3.2.2.4 IR Mixer

The same IR mixer and coupler selected for the down-converter are to be used in the up-converter. See section 3.2.1.4 IR Mixer for details.

3.2.2.5 Band-select filter

The same band-select filter specified in section 3.2.1.2 Band-select filter to be used in the up-converter. Additionally, as the IR mixer only provides 39 dB isolation

between LO and RF ports, this filter must provide an additional >30 dB rejection of the LO to ensure compliance to the spurious specification.

3.2.2.6 RF Gain Stage 1

The first RF Gain stage chosen is 6080433-28. This existing Nanowave HMIC module combines two COTS MMICs. The first die is a driver for a high-powered amplifier, the second die is a voltage-controlled attenuator. This module was selected to provide some of the required gain, while also providing a method of tuning the gain of the system via the voltage-controlled attenuator. The voltage control was set with a potentiometer on the bias PCB, allowing adjustment of this value during test and tune. The PCB will also provision for a 2-resistor voltage divider to fix this control signal during standard manufacturing.

3.2.2.6 RF Gain Stage 2

The next gain stage selected was the 6080433-83, which was selected as a driver to the final PA stage. This was selected because of its high saturated output power (29.5 dB_m) and its ability to handle the higher powers experienced at this stage in the system. This module contains a COTS high-powered amplifier MMIC with a TTL control line to modulate the drain current (allowing pulsed operation for reduced thermal strain and power consumption).

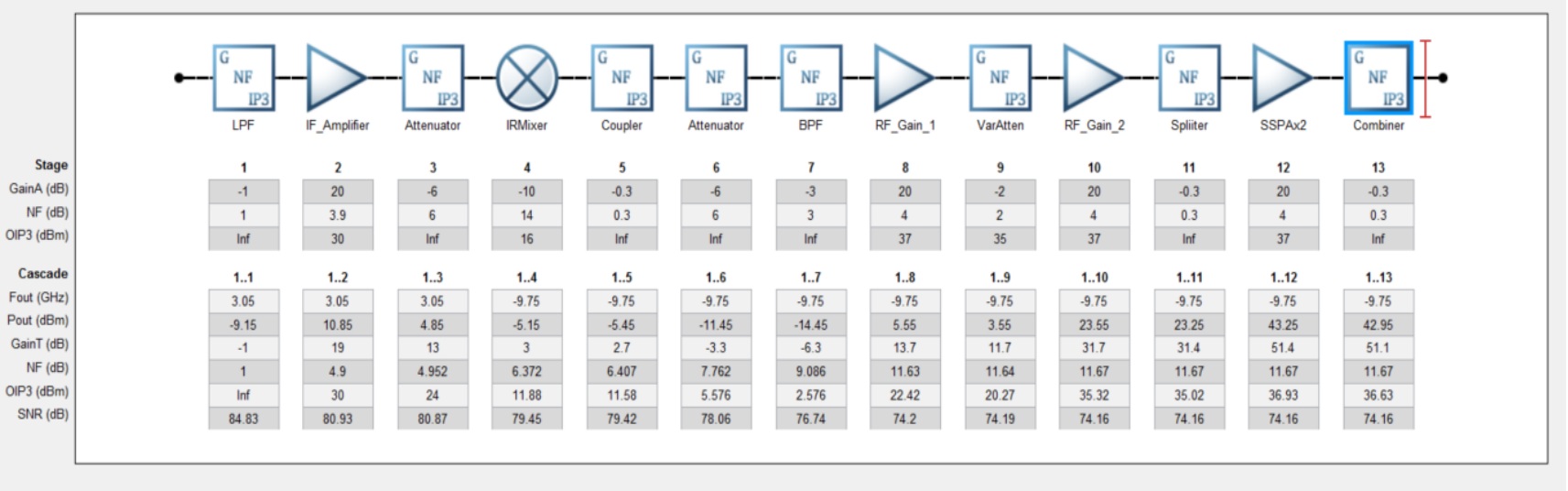
3.2.2.7 RF Gain Stage 3

The final gain stage is comprised of two 6080433-83 in parallel, with 6080433-83 hybrid couplers used to split and combine the signal. Each 6080433-83 amplifier

has a saturated output of 29.5 dB_m. When combined, the saturated output of this RF stage would be 32.5 dB_m, minus 0.3 dB combiner losses in the 6080433-83 hybrid coupler. This will exceed the required saturated output power for the system.

3.2.2.8 RF Budget Analysis for Down-Converter

The RF budget analysis for the down-converter was once again calculated using the RF Budget Analyzer Tool [28] in MATLAB, and is presented in Figure 4: RF Budget analysis for down-converter. The small signal gain is predicted to be 51.1 dB, which would likely push the final stage too far into compression and may damage the output amplifier. The gain is expected to be lower in the actual design, as these values are based on the datasheets for the COT die used in the design. If the gain is not sufficiently lowered due to interconnect losses between the die, then the gain can be lowered by adjusting the voltage variable attenuator during test.



Stage	1	2	3	4	5	6	7	8	9	10	11	12	13
GainA (dB)	-1	20	-6	-10	-0.3	-6	-3	20	-2	20	-0.3	20	-0.3
NF (dB)	1	3.9	6	14	0.3	6	3	4	2	4	0.3	4	0.3
OIP3 (dBm)	Inf	30	Inf	16	Inf	Inf	Inf	37	35	37	Inf	37	Inf

Cascade	1..1	1..2	1..3	1..4	1..5	1..6	1..7	1..8	1..9	1..10	1..11	1..12	1..13
Fout (GHz)	3.05	3.05	3.05	-9.75	-9.75	-9.75	-9.75	-9.75	-9.75	-9.75	-9.75	-9.75	-9.75
Pout (dBm)	-9.15	10.85	4.85	-5.15	-5.45	-11.45	-14.45	5.55	3.55	23.55	23.25	43.25	42.95
GainT (dB)	-1	19	13	3	2.7	-3.3	-6.3	13.7	11.7	31.7	31.4	51.4	51.1
NF (dB)	1	4.9	4.952	6.372	6.407	7.762	9.086	11.63	11.64	11.67	11.67	11.67	11.67
OIP3 (dBm)	Inf	30	24	11.88	11.58	5.576	2.576	22.42	20.27	35.32	35.02	36.93	36.63
SNR (dB)	84.83	80.93	80.87	79.45	79.42	78.06	76.74	74.2	74.19	74.16	74.16	74.16	74.16

Figure 4: RF Budget analysis for down-converter.

3.3 Thermal Analysis of High-Powered RF Components

Thermal analysis was done on critical active devices as the thermal performance of these devices directly impact the reliability of the component. The thermal analysis done with the following assumptions:

- Devices generating less than 100 mW of heat were not considered
- All thermal relief is through conduction to the outer housing, which is connected to a large enough metal plate to maintain ambient temperature at the interface to the housing despite thermal output from the unit
- The only path for conduction is directly below each die; any lateral conduction or radiative heat loss is not considered.
- The interior temperature of the Radome will exceed the environmental specification of 55º C by a further 10 degrees due to waste heat and solar loading on the radome.
- The maximum operating duty cycle for high-powered components is 20%, with supply modulation to turn off high-powered devices when not transmitting.
- Turn on and turn off time of the modulator is small compared to the 20% duty cycle and not significantly contributing to waste heat.
- All devices are heated by their average thermal output, and the system has reached steady state.

Using the above criteria, the only die to considered relevant with respect to the reliability are the RF amplifiers in the transmit chain of the UDC.

The thermal resistivity from junction to ambient can be calculated as a series or thermal resistances as shown in Figure 5: Thermal stack-up for the CHA5012 amplifier die.

Thickness		Area
N/A	CHA5012 DIE	17082 mil²
10 mil	PEDESTAL (Cu)	17082 mil²
25 mil	CARRIER(Cu)	17082 mil²
250 mil	HOUSING (AL)	17082 mil²

Figure 5: Thermal stack-up for the CHA5012 amplifier die.

(42) can be used to calculate the thermal conductivity of a single stage:

$$W = \frac{kA(T_2 - T_1)}{d} \qquad (42)\ [29]$$

$$where\ W = energy\ transfer\ in\ \frac{J}{s}$$

$$k = thermal\ conductivity\ constant\ of\ the\ barrier\ material$$

$$A = cross - sectional\ area\ of\ interface$$

$$d = thickness\ of\ the\ interface$$

The thermal conductivity for various materials can be found in [30]. From this reference, the thermal conductivity of copper is $385.0\frac{W}{m \cdot K}$ and the thermal conductivity of aluminum is $205.0\frac{W}{m \cdot K}$. From this, one can relate the temperature across each layer of the thermal interface to the power conducting through it with a proportionality constant θ with a value calculated by (43).

$$\theta_{L_1 to L_2} = \frac{d}{kA} \quad (43)\ [29]$$

Using this equation, the thermal resistivity of each layer in the thermal interface was calculated and is available below in Table 8.

Table 8: Thermal resistance of various thermal interface layers used in heat transfer analysis.

Layer	Material	Cross-section (m^2)	Thickness (m)	Thermal Resistance $\left(\frac{mK}{W}\right)$	$\theta\ (\frac{K}{W})$
1	Copper	1.102×10^{-5}	2.54×10^{-4}	385.0	0.599
2	Copper	1.102×10^{-5}	6.35×10^{-4}	385.0	0.150
3	Aluminum	1.102×10^{-5}	6.35×10^{-3}	205.0	2.811

These values can be summed with the thermal resistance from junction to back of die (45ºC/W available from CHA5012 datasheet [31]) to give the total thermal resistance of the heat conduction path.

$$\theta_{JtoA} = 45\frac{K}{W} + 0.599\frac{K}{W} + 0.150\frac{K}{W} + 2.811\frac{K}{W} = 48.021\frac{K}{W}$$

Knowing this value, one can now determine the temperature rise in the junction. Assuming the worst case power output operating at P_{SAT}, each device would have a maximum power output of 29.5 dBm or 0.8913 W. The worst case PAE at high temperature for this device is 30%. From this one` can calculate the waste heat:

$$PAE = \frac{P_{OUT} - P_{IN}}{P_{DC}}$$

$$\therefore P_{DC} = \frac{(P_{OUT} - P_{IN})}{P_{AE}} = \frac{0.8913W - 0.2113W}{0.3} = 2.267\ W$$

Assuming a 20% duty cycle with modulation of the DC supply:

$$P_{DISS} = P_{DC}(1 - PAE) \cdot Duty\ Cycle = 2.267W \cdot 0.70 \cdot 0.2 = 0.3096\ W.$$

$$\Delta T = \theta_{JtoA} \cdot P_{DISS} = 48.021 \frac{ºC}{W} \cdot 0.3096\ W = 14.87\ ºC$$

Therefore, the worst-case junction temperature experienced by any die in the system would be:

$$T_J = T_{AMB} + \Delta T = 65.00ºC + 14.87\ ºC = 79.87\ ºC$$

As the maximum junction temperature for the CHA5012 is 175ºC, all die are de-rated thermally by 54.36% which will ensure low thermal part stress and high reliability.

3.4 Reliability Analysis

The reliability analysis for the system was completed using FIDES as discussed in section 2.3 Method for Reliability Analysis.

The reliability analysis methodology, as discussed in section 2.3, was completed using the FIDES reliability analysis tool in the following steps:

1. Define mission profile
2. Define application specific risks
3. Define ruggedizing (manufacturing) standards
4. Define individual stresses on each component

To perform the analysis, a combination of qualitative statements about the mission profile, manufacturer, design methodology and component selection were given weights, and combined with the component stresses in each phase of the mission profile in order to generate a statistical model of the number of failures for all the

constituent components in the subassembly expected over 1 billion hours of operation. The FIT for the subassembly is the summation of the FIT of its components. The underlying statistical models used by the FIDES reliability analysis tool are considered beyond the scope of this document but is readily available in [20].

3.4.1 Determining MTBF/FIT Specification for UDC

The target MTBF for the overall system is 15 years. Using (36) we can determine the overall FIT for the system should not exceed 7610.40 FIT to ensure an MTBF of 15 years. Assuming no redundancy, a failure in any component will directly result in a system failure. For this reason, the FIT of the system can be calculated as the sum of its constituent subassemblies and components as expressed in (44).

$$FIT_{SYSTEM} = \sum_{n=1}^{n=m} FIT_{SUBASSEMBLY_n} \quad (44)\ [20]$$
$$where\ m = number\ of\ subassemblies\ in\ the\ system$$

The fit of all other components in the system was determined to be 5385.35 FIT [32]. As the remainder of the system will suffer 5385.35 FIT and can tolerate 7610.40 FIT, the UDC should not introduce more than 2225.05 FIT. For that reason, a maximum limit of 2225 FIT was deemed an acceptable specification for the reliability analysis.

3.4.2 Mission profile

The mission profile can be broken down into a series of sub-cycles which make up with overall life cycle of the system with the following parameters: on/off state,

ambient temperature, sub-cycle duration, number of sub-cycles (per annum), maximum temperature, relative humidity, vibration, saline pollution, environmental pollution, application pollution, and protection level from pollution.

As the system is to be operated as a stationary deployment in a marine environment and operate for 10 years continuously, the following assumptions are made for each cycle:

- Saline pollution is high due to salt-fog in marine environments
- Environmental and application pollution are considered low
- The on/off state is set to on for all cycles
- RMS vibration is classified as ground benign, as the system will be mounted on a building or fixed ground deployment.

Using these assumptions two mission profiles were then set up, an optimistic mission profile and a pessimistic profile. Each breaks up the life cycle into a series of 12 repeating sub-cycles, representing a month of operation.

The optimistic mission profile was set up using meteorological averages for Tokyo, Japan. It assumes each day in the month hits the historical high temperature for that month, and each day sees the average diurnal temperature swing for that month. It also assumes the humidity in each month is the historical average.

The pessimistic profile tries to accentuate the temperature extremes, and the diurnal temperature variation. It makes the following assumptions:

- All winter months will experience the minimum operating temperature of the system every day, with a 30ºC diurnal temperature swing every day.

- All spring/autumnal months will have an average temperature of 0ºC, with an extended diurnal temperature swing of 40ºC every day.
- All summer months will experience the maximum operating temperature of the system, with a 30ºC diurnal temperature swing each day.

While the former mission profile is more representative of the use-case, the end customer requested the analysis also be performed using the pessimistic case to ensure the reliability of the system.

The optimistic use case for the STALO PCB is summarized below in Table 9: Optimistic mission profile used for FIDES analysis of STALO PCB. and the pessimistic mission profile for the STALO PCB is summarized below in Table 10: Pessimistic mission profile used for FIDES analysis. The mission profile for the HMIC portion of the design is nearly identical, except that the device is considered hermetic in all phases.

Table 9: Optimistic mission profile used for FIDES analysis of STALO PCB. Note: protection level is set to hermetic for analysis of HMIC.

Definition			Temperature	Temperature cycling				Humidity	Mechanical	Chemical			
Phase name	On / Off	Calendar time (hours)	Ambient temperature (°C)	Δt (°C)	Cycle duration (hours)	Number of cycles (/phase)	Maximum temperature during cycling (°C)	Relative humidity (%)	Random vibrations (Grms)	Saline pollution	Environmental pollution	Application pollution	Protection level
Japan January	ON	730 h	5.00 °C	10.00 °C	24 h	30	10.00 °C	50	0.00 Grms	High	Low	Low	Non hermetic
Japan February	ON	730 h	5.00 °C	10.00 °C	24 h	30	10.00 °C	52	0.00 Grms	High	Low	Low	Non hermetic
Japan March	ON	730 h	8.00 °C	8.00 °C	24 h	30	12.00 °C	56	0.00 Grms	High	Low	Low	Non hermetic
Japan April	ON	730 h	14.00 °C	8.00 °C	24 h	30	18.00 °C	63	0.00 Grms	High	Low	Low	Non hermetic
Japan May	ON	730 h	18.00 °C	8.00 °C	24 h	30	22.00 °C	66	0.00 Grms	High	Low	Low	Non hermetic
Japan June	ON	730 h	21.50 °C	7.00 °C	24 h	30	25.00 °C	73	0.00 Grms	High	Low	Low	Non hermetic
Japan July	ON	730 h	25.00 °C	6.00 °C	24 h	30	28.00 °C	76	0.00 Grms	High	Low	Low	Non hermetic
Japan August	ON	730 h	27.00 °C	6.00 °C	24 h	30	30.00 °C	73	0.00 Grms	High	Low	Low	Non hermetic
Japan September	ON	730 h	23.00 °C	6.00 °C	24 h	30	26.00 °C	73	0.00 Grms	High	Low	Low	Non hermetic
Japan October	ON	730 h	17.50 °C	7.00 °C	24 h	30	21.00 °C	67	0.00 Grms	High	Low	Low	Non hermetic
Japan November	ON	730 h	12.00 °C	8.00 °C	24 h	30	16.00 °C	61	0.00 Grms	High	Low	Low	Non hermetic
Japan December	ON	730 h	7.50 °C	9.00 °C	24 h	30	12.00 °C	54	0.00 Grms	High	Low	Low	Non hermetic

Table 10: Pessimistic mission profile used for FIDES analysis. Note: protection level is set to hermetic for analysis of HMIC.

Definition			Temperature	Temperature cycling				Humidity	Mechanical	Chemical			
Phase name	On / Off	Calendar time (hours)	Ambient temperature (°C)	Δt (°C)	Cycle duration (hours)	Number of cycles (/phase)	Maximum temperature during cycling (°C)	Relative humidity (%)	Random vibrations (Grms)	Saline pollution	Environmental pollution	Application pollution	Protection level
Japan January	ON	730 h	-15.00 °C	30.00 °C	24 h	30	0.00 °C	95	0.00 Grms	High	Low	Low	Non hermetic
Japan February	ON	730 h	-15.00 °C	30.00 °C	24 h	30	0.00 °C	95	0.00 Grms	High	Low	Low	Non hermetic
Japan March	ON	730 h	0.00 °C	40.00 °C	24 h	30	20.00 °C	95	0.00 Grms	High	Low	Low	Non hermetic
Japan April	ON	730 h	0.00 °C	40.00 °C	24 h	30	20.00 °C	95	0.00 Grms	High	Low	Low	Non hermetic
Japan May	ON	730 h	0.00 °C	40.00 °C	24 h	30	20.00 °C	95	0.00 Grms	High	Low	Low	Non hermetic
Japan June	ON	730 h	40.00 °C	30.00 °C	24 h	30	55.00 °C	95	0.00 Grms	High	Low	Low	Non hermetic
Japan July	ON	730 h	40.00 °C	30.00 °C	24 h	30	55.00 °C	95	0.00 Grms	High	Low	Low	Non hermetic
Japan August	ON	730 h	40.00 °C	30.00 °C	24 h	30	55.00 °C	95	0.00 Grms	High	Low	Low	Non hermetic
Japan September	ON	730 h	0.00 °C	40.00 °C	24 h	30	20.00 °C	95	0.00 Grms	High	Low	Low	Non hermetic
Japan October	ON	730 h	0.00 °C	40.00 °C	24 h	30	20.00 °C	95	0.00 Grms	High	Low	Low	Non hermetic
Japan November	ON	730 h	0.00 °C	40.00 °C	24 h	30	20.00 °C	95	0.00 Grms	High	Low	Low	Non hermetic
Japan December	ON	730 h	-15.00 °C	30.00 °C	24 h	30	0.00 °C	95	0.00 Grms	High	Low	Low	Non hermetic

3.4.3 Application Factors for Reliability

FIDES adjusts 8 weighting factors based on the application of the device being analyzed. The application weights are qualitatively assigned based on a description of the operation of the system. These are applied to each operating phase of the system. As the system is to be operated continuously without intervention, the application factors were set the same for each cycle. The following weights were chosen:

- **User type in the phase considered** – this weighting represents the capacity of the user to respect the operating procedures of the device [20]. The lowest weight of 0 (or favourable) was selected, given it will be used by well trained, experienced operators.
- **User qualification level in the phase considered** – this weighting represents the level of control the user has regarding the operational context [20]. As the system is controllable remotely and to be operated by well trained and qualified individuals, the lowest weighting of 0 (or favourable) was selected.
- **System mobility** – this weighting represents the amount of disturbance the system will take from manipulation and relocation [20]. As the system is to be fixed during is life cycle, the lowest weighting of 0 (or few contingencies; fixed or stable environment) was selected.
- **Product manipulation** – this weighting represents the possibility of damage occurring from manipulation such as manipulation in unintended

ways, shocks or drops [20]. As this is a fixed deployment, the weighting was again set to the lowest value of 0 (or not manipulated).

- **Type of electrical network for the system** – this weighting represents the level of electrical disturbance expected on all electrical interfaces to the system (including power and signal lines) [20]. The weighting selected for this was a moderate rating of 1 (or slightly disturbed network). This is because the electrical power may be supplied from the power grid directly. As this is an established power grid in a developed nation, it is considered reliable, but it may experience some interruptions, transients, and surges.
- **Product exposure to human activity** – represents exposure to contingencies related to human activity such as shock or change in operation due to human exposure [20]. This weighting was selected to be the lowest value 0 (or uninhabitable zone) as the systems will be deployed in areas restricted to public access.
- **Product exposure to machine disturbances** – this weight represents disturbances due to the operation of machines, motors, actuators such as shock, overheating and electrical disturbances. This was selected as moderate or 1, as electric motors and actuators are included inside the same compartment (within the radome).
- **Product exposure to weather** – this weight represents exposure to rain, hail, frost, dust, and other weather phenomenon. All electronics are inside a non-hermetically sealed radome. As such, there is expected to be eventual

ingress of fog, humidity, and salt-fog. Thus, a moderate rating of 1 (or indirect exposure) was selected.

3.4.4 Ruggedizing Factors

The ruggedizing factors are a set of weights in the analysis common to all cycles based on the process of the manufacturer. It is an assessment of the compliance of the manufacturer to a set of recommendations for of high-reliability electronic assemblies. The weights for this were based on the compliance of Nanowave Technologies to these recommendations and are presented below in Table 11: Ruggedizing factors used for FIDES reliability analysis.

Table 11: Ruggedizing factors used for FIDES reliability analysis.

Recommendation	**Compliance Level**	**Comment**
Check that environmental specifications are complete.	N4 – Recommendation is fully applied	Environmental specifications are provided at the subassembly and system level.
Provide training and manage operation and maintenance for implementation and maintenance of the product.	N4 – Recommendation is fully applied	Manuals and training provided by Nanowave Technologies to end use. Nanowave to provide a 10-year maintenance contract for support of systems.
Check that procedures specific to the product and rules specific to businesses are respected by an appropriate monitoring system.	N4 – Recommendation is fully applied	Nanowave Technologies is an AS9100 RevD qualified manufacturer, with specific rules and procedures. These are monitored by AS9100 audits.
Design dependable electrical protection devices	N4 – Recommendation is fully applied	All designs manufactured by Nanowave Technologies have industry standard protections such as keyed

		connectors, over/reverse voltage protections, and surge/lightning protection when applicable.
Study and handle risks of the product under test being deteriorated by failures of its test or maintenance means.	N4 – Recommendation is fully applied	Nanowave Technologies uses a root cause analysis to assess such risks.
Identify and use appropriate prevention means of preventing reasonably predictable aggressions (related to the weather)	N4 – Recommendation is fully applied	System to be deployed in a sealed radome. PCBs are conformally coated in urethane to reduce impacts of weather, and HMIC is hermetic.
Use appropriate prevention means to identify and handle reasonably predictable abnormal uses (related to the weather)	N4 – Recommendation is fully applied	Certain subassemblies will shut down if thermal limits are exceeded. All subassemblies are monitored with respect to thermal state, and supply voltage and current. An external temperature sensor is included for additional telemetry.
Justify that environmental specifications are respected.	N4 – Recommendation is fully applied	Certain subassemblies will shut down if thermal limits are exceeded. All subassemblies are monitored with respect to thermal state, and supply voltage and current. An external temperature sensor is included for additional telemetry.
Carry out a product improvement process (for example highly accelerated stress tests) to limit the product sensitivity to environmental constraints (disturbances, environments, overstress)	N4 – Recommendation is fully applied	Qualification units of the overall system are subjected to a 14-day accelerated life test.

Perform an analysis of failure cases that could result in failure propagation.	N4 – Recommendation is fully applied	Subassemblies are designed to prevent failure at all interfaces, considering the possible inputs to the interface (including fail states of connecting subassemblies). For example, the system is intended to survive in the case there is a failure of the antenna cable, resulting in a total reflection of power back to the duplexer.
Carry out a process analysis of implementation and maintenance operations	N4 – Recommendation is fully applied	Nanowave Technologies to provide maintenance contract on system as stated above.
Write complete procedures for all product implementation and maintenance operations	N4 – Recommendation is fully applied	Nanowave Technologies includes product installation documentation, a product user guide, and a maintenance guide for the system.
Respect a standard dealing with conducted and radiated electromagnetic disturbances. This is equally applicable to the product and the system into which it is integrated.	N4 – Recommendation is fully applied	System is designed to be CE and UL compliant. Design considered PSE compliance (as a Japanese regulatory standard for safety, EMI and EMC) but was found to be considered outside the scope of that regulation and not required for import to Japan.
Respect a standard dealing with power supplies (standard that defines possible disturbances and possible EN2282 type variations). The standard must be respected both for electricity generation and for electricity consumption	N4 – Recommendation is fully applied	System is CE and UL compliant.

3.4.5 Part Stress Analysis

The simulation was set up with each component used on both the HMIC and STALO PCB design. For each component, the part stress was defined as a percent of the specification. For example, if a capacitor rated for 16 volts was used in a circuit with 4 volts applied, it would be considered to have a 0.25% voltage stress. The following assumptions were made in the analysis:

- For each component type, it was assumed the worst stress seen by one component would be experience by them all. This means that if there were 21 of the same type of capacitor, seeing 21 different stresses, the analysis would treat them as 21 capacitors seeing the worst-case stress.
- The stresses considered are power, voltage, current, thermal, duty cycle, and number of annual mating cycles (for connectors only).
- The stresses are assumed to be the same in every phase of the mission profile, as the device is continuously operating

Using the assumptions in this and all previous subsections, the analysis was completed using the reliability analysis tool provided by the FIDES group, with the results given in the next section.

3.4.6 Results of Reliability Analysis

Based on the reliability analysis completed in this section, the unit is expected to suffer 82.91 FIT based on expected environmental conditions, and 232.34 FIT based on worst-case operating conditions. This corresponds to 4,304,307.19 MTBF or approximately 491 years. This is in-line with other subassemblies produced in

the Nanowave HMIC process; the limiting factor in the system is typically the power supplies or associated mechanical assemblies.

Of these failures, 52% are due to predicted faults in the linear regulators, and 32% are due to predicted faults in ceramic capacitors. This makes sense, as the regulators are the highest power dissipating components in the design, and ceramic capacitors can undergo quite a bit of electromechanical force variation during standard operation. Higher reliability could be achieved by integrating the linear regulators into the HMIC design. Further results can be found in APPENDIX B: RELIABILITY ANALYSIS RESULTS.

3.4.7 Comparing HMIC reliability to PCB reliability

Analysis of the reliability of the PCB implementation of the HMIC was completed by Nanowave Technologies separately from this work using the FIDES reliability analysis tool. The worst-case reliability analysis of the PCB implementation was determined to be 1,593,498.52 MTBF [32], corresponding to 627.55 FIT. Based on analysis, the HMIC should reduce the number of failures by 2.7 times.

One might observe that the reliability of the PCB (achieving an MTBF approximately 1.6 million hours exceeds the specification significantly enough and the improvement is not warranted. It should be noted that this value is a mean, and as such there is still a chance a failure would occur within the anticipated life of the radar system (10 years or 87600 hours). With an MTBF of 1.6 million, there remains a 5.5% chance of observing a failure in 10 years of continuous operation. The HMIC would reduce this risk to 2% for the pessimistic analysis, or less than

0.3% for the realistic analysis. Thus moving from PCB to HMIC has increased the confidence that there will be no failure during the mission from 2 sigma to 3 sigma.

4.0 SYSTEM DESIGN

The following chapter discusses the design of various system components which were not available from existing Nanowave parts, including the design of a 90º hybrid coupler, an interdigital band-pass filter, and all connecting RF tracks in the hybrid. It then discusses the EM co-simulation of the various components used in the system before considering the overall simulation of the system against specifications. The final section discusses the mechanical layout of the HMIC and housing.

4.1 Hybrid Coupler Design

The hybrid coupler is used to combine the I and Q outputs of the IR mixer with a quadrature phase shift, while providing isolation between the I and Q ports on the mixer. The design was done based on the methodology presented in Pozar [33] on page 343. An ideal 90º hybrid coupler would achieve the following S matrix:

$$[S] = -\frac{1}{\sqrt{2}}\begin{bmatrix} 0 & j & 1 & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \\ 0 & 1 & j & 0 \end{bmatrix} \quad (45)\ [33]$$

The analysis presented by Pozar [33] provides the following solution shown below in Figure 6.

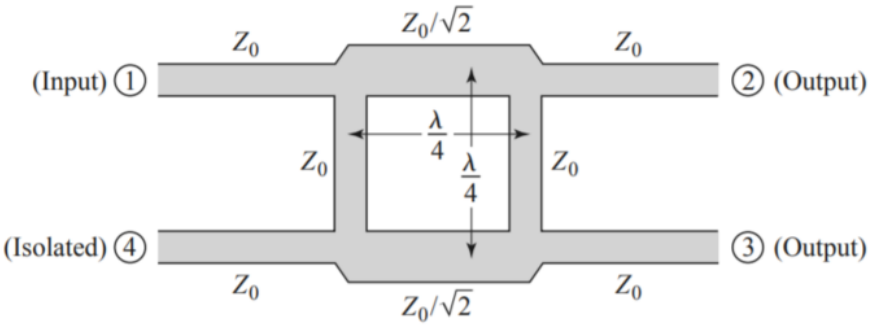


Figure 6: Geometric solution for 90º hybrid coupler realized with transmission lines presented by Pozar. [33]

The work presented by Pozar [33] makes the design of a single-stage branch-line coupler somewhat trivial; the issue with the design is the dependence on quarter-wave transformers which geometrically limit the bandwidth of the solution to approximately 10-20% [33]. As the current design required 100 MHz bandwidth at 3050 MHz, representing 3.27% bandwidth, a single-stage branch line coupler should be sufficient for the needs of the design.

4.1.1 Schematic Level Simulation of Hybrid Coupler Using Microstrip Models

An ideal transmission line model was initially designed to verify the theory presented in [33].Having determined that the single-stage branch-line coupler would be an appropriate topology for the design, a schematic level design was done using microstrip models to incorporate non-idealities of a real system. The selected substrate was 15 mil alumina, to keep the bond height and substrate material consistent between the hybrid coupler and IR mixer substrate.

Line widths and lengths were calculated to provide the impedances and electrical length of the ideal model. Values were calculated in mils and rounded to one tenth of a mil to be in line with the manufacturing capabilities of the Nanowave Thin

Film Deposition process. The initial schematic only includes the 4 interconnecting lines, neglecting transmission lines to feed the system and the width discontinuity between the lines. The schematic used for the initial microstrip simulation shown below in Figure 7. The design was then iterated, by adding in curved feeding transmission lines and models for line-width discontinuity before moving to layout.

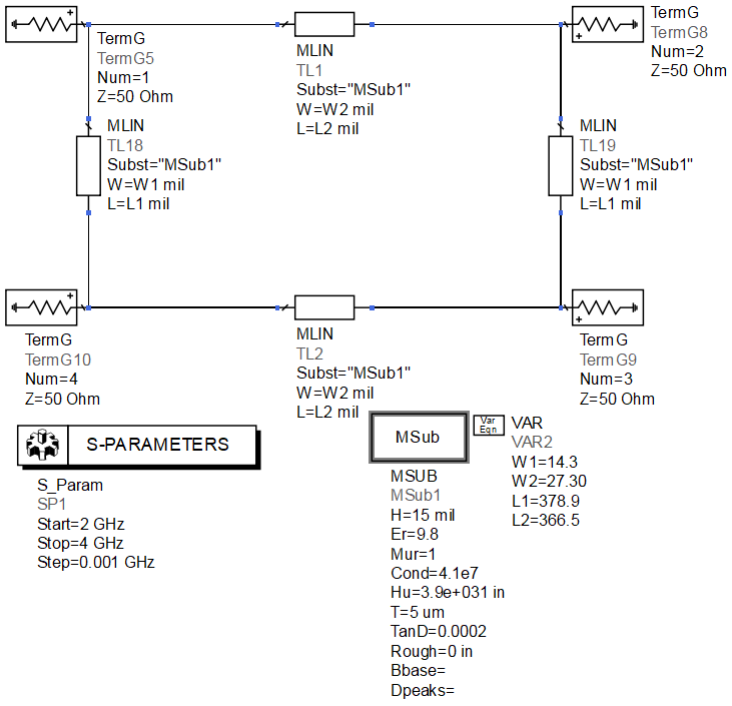


Figure 7: Schematic of microstrip model for hybrid coupler.

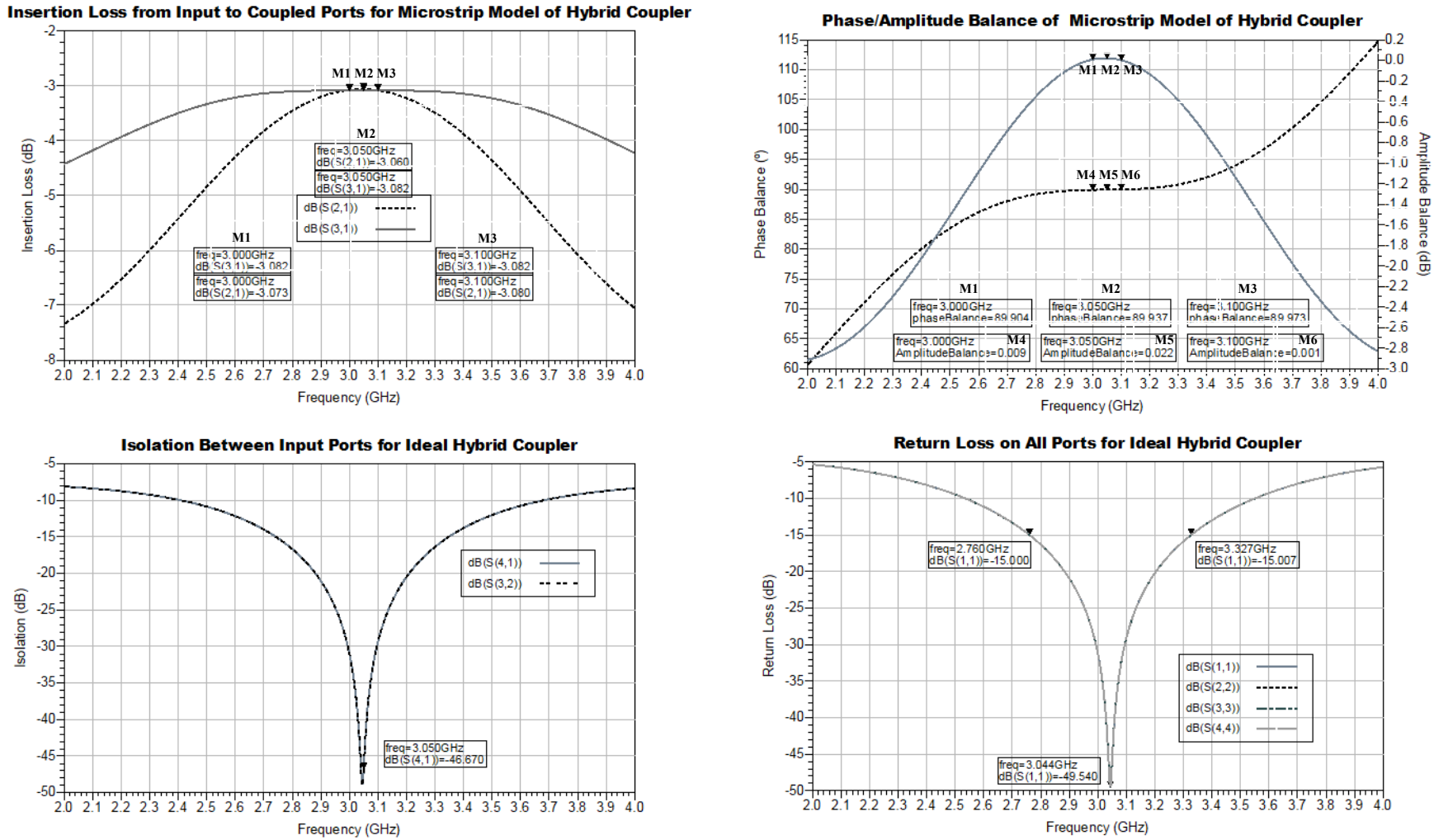


Figure 8: Results of schematic level microstrip model for hybrid coupler.

4.1.2 Layout of Hybrid Coupler

After iteration on the schematic level microstrip model, the design was taken to layout. As this substrate is to be integrated on an existing carrier design with a mixer substrate, the dimensions of the substrate are bounded by the geometry of the carrier. In order to fit the design, the microstrip lines had to be meandered to reduce the width and length while maintaining the physical length. Feeding RF lines were also added to connect the coupler to the substrate edge for wire bonding. Between the outputs, a strip of copper was placed with via's to ground to allow a 50 Ω resistor to be installed, thus allowing either output to be terminated when unused. Other manufacturing details were added, including fiducial marks in the corners of the substrate to allow automated assembly of the HMIC, and a placeholder for the part number. The final layout can be seen below in Figure 9.

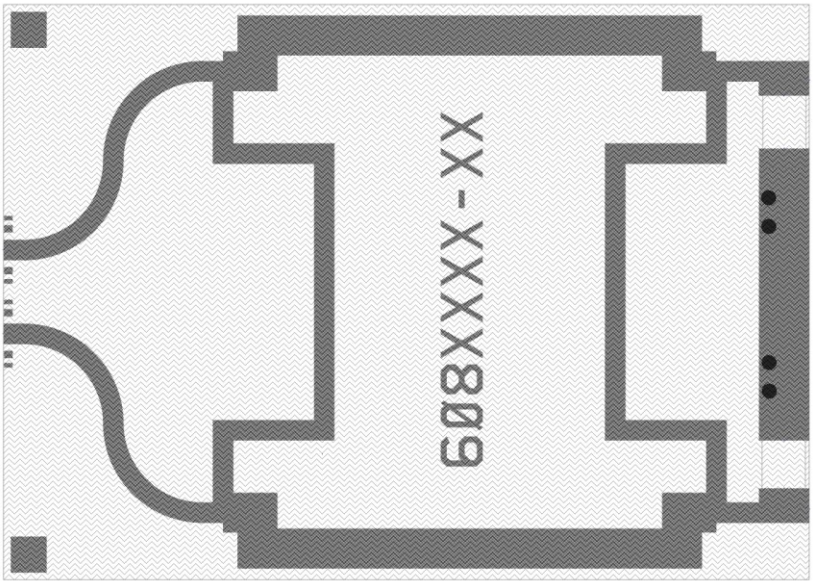


Figure 9: Layout of 90º Hybrid Coupler.

Once this layout was completed, it was simulated using the ADS method of moments EM simulator. An EM model was generated, and then incorporated back into the schematic simulation. The simulation results are presented below in Figure 10.

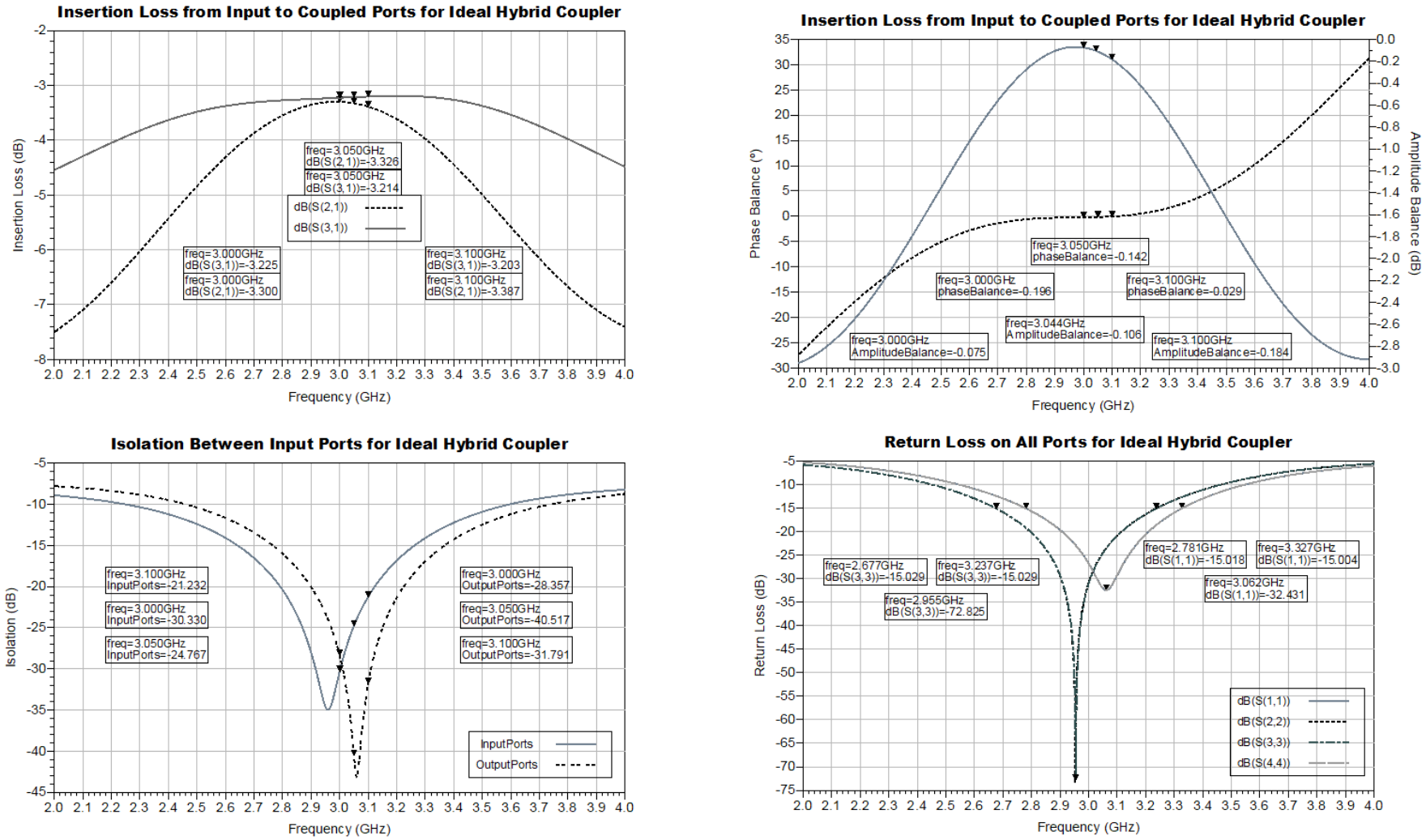


Figure 10: EM co-simulation results for layout of hybrid coupler design.

The results of each level of simulation have been captured in Table 12: Comparison of various simulation results against specification for hybrid coupler design. It can be seen that the design meets all criteria with the exception of the insertion loss, which is marginally higher than the specification. It was determined at this time to accept the higher loss, and address this at the system level. If the receiver failed to provide adequate gain, the additional loss could be addressed at that time.

Table 12: Comparison of various simulation results against specification for hybrid coupler design.

	Specification	**Ideal Simulation**	**Microstrip Model Simulation**	**Layout EM Simulation**
Match Bandwidth	3.27 %	18.59%	18.59%	17.83%
Amplitude balance	$\lesssim$ 0.5 dB	0 dB	0.022 dB	-0.184 dB
Phase balance	$\lesssim$ 3.4º	0º	0.096º	-0.196º
Insertion Loss	$\lesssim$ 0.3 dB	0.01 dB	0.08 dB	0.326 dB
Port Isolation	$\lesssim$ 20 dB	∞	46.67 dB	21.23 dB

4.1.3 Design analysis over manufacturing variation and operating temperature

There are two sources of variation that can be expected compared to the results from EM simulation presented in 4.1.2 Layout of Hybrid Coupler. The first source of variation would be due to manufacturing. The thin film process at Nanowave is accurate to ±700 ppm in trace dimension [21]. The other source of variation is thermal expansion of the substrate, and thermal variation of the dielectric of the substrate. For Rogers TMM10i, these values are captured in Table 13: Substrate variation over temperature. [34]

Table 13: Substrate variation over temperature.

Dimension	Variation
Variation in X dimension	19 ppm/ºC
Variation in Y dimension	19 ppm/ºC
Variation in Z dimension	20 ppm/ºC
Variation in dielectric	-43 ppm/ºC

The two corner cases combining these variations would be at hot with +700 ppm manufacturing variation and at cold with -700 ppm manufacturing variation. The design was simulated on these two corner cases to assess compliance over all possible variation with the results shown below in Figure 11.

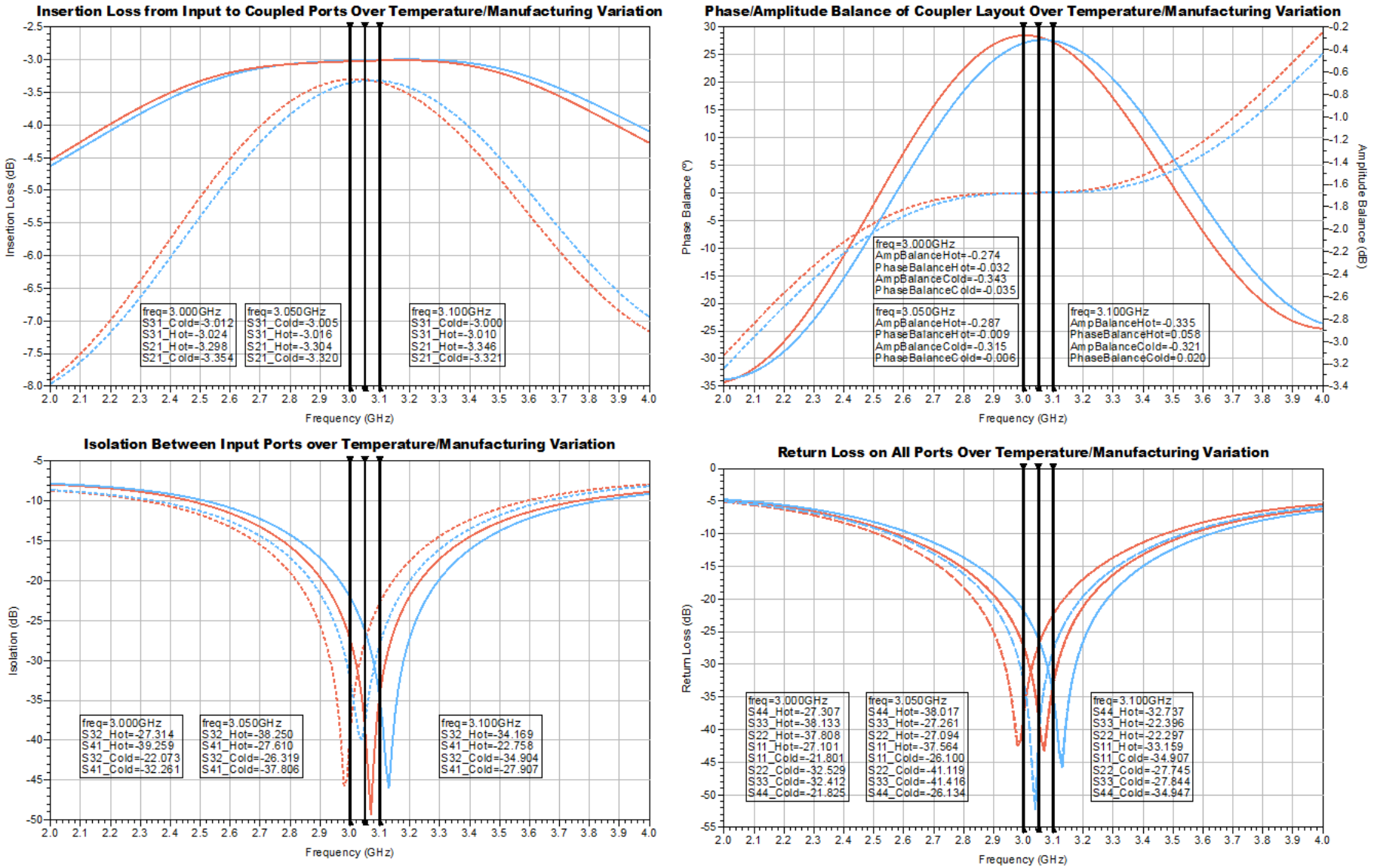


Figure 11: Hybrid coupler performance over temperature/manufacturing variation.

The worst case over each temperature range was selected and included below in Table 14. Based on these results, the design will work over all manufacturing and temperature variation, except that the loss is marginally higher than desired. This has been noted and is adjustable if the gain specification is failing at the system level.

Table 14: Worst performance of hybrid coupler over temperature/manufacturing variation.

	Specification	**-40 ºC**	**25 ºC**	**65 ºC**
Return Loss	$>$ 15 dB	21.8 dB	32.3 dB	22.2 dB
Amplitude balance	$\lesssim$ 0.5 dB	0.315 dB	0.184 dB	0.335 dB
Phase balance	$\lesssim 3.4º$	0.032º	0.196º	0.058 º
Insertion Loss	$\lesssim$ 0.3 dB	0.0354 dB	0.326 dB	0.346 dB
Port Isolation	$\lesssim$ 20 dB	27.61 dB	21.23 dB	22.76 dB

4.2 Band-Pass Filter Design

The band-pass filter was designed based on the criteria outlined in sections 3.2.1 and 3.2.2. The selected topology was an interdigital filter, in order to minimize the footprint of the design. The main risk associated with this filter type is periodic unwanted passbands emerging at higher harmonics of the center frequency [36]. This risk was mitigated by extending the simulation range to 2.5 times the center frequency and ensuring attenuation of specific known interferers. The normalized impedances required for a 5^{th} order filter with a Chebyshev response were calculated using the methods described in [33] and are as follows:

$$g_0 = 1.000$$

$$g_1 = 1.1468$$

$$g_2 = 1.3712$$

$$g_3 = 1.1486$$

$$g_4 = 1.3712$$

$$g_5 = 1.1468$$

$$g_6 = 1.000$$

These normalized impedances define the desired low-pass transfer function of the filter with g_0 and g_6 representing the interface to the system impedance. From these values, one can calculate the relative fringe capacitance between the coupled resonators as described in [36]. The relevant parameters required for the calculation provided in [36] are given below in Table 15 with the calculated relative fringe capacitance between elements given in Table 16.

Table 15: Parameters used in conjunction with normalized impedances to calculate required normalized fringe impedances of half-wave resonators for interdigital filter.

Parameter	Description	Value	Comment
ϵ_r	Relative dielectric constant	9.9	Rogers TMM10i datasheet
bw	Relative bandwidth	10.53%	
t	PCB laminate thickness	15 mil	
Y_A	System admittance	0.02 S	50-ohm system
f_c	Center frequency	9.6 GHz	Middle of band

Table 16: Normalized fringe capacitance between elements in filter.

Element Numbers	$\frac{\Delta C}{\epsilon}$
1 – 2	0.3618
2 – 3	0.2355
3 – 4	0.2355
4 – 5	0.3618

Using these values, the ratio between element spacing and substrate thickness was selected off of Getsinger's Curves for fringing capacitances in coupled microstrip lines available in [37]. The spacing was then calculated for a 15-mil substrate. These values are given below Table 17.

Table 17: Spacing of half-wave resonators for interdigital filter.

Element Numbers	$\frac{\Delta C}{\epsilon}$	$\frac{s}{h}$	**Element Spacing**
1 – 2	0.3618	1.20	18.0 mil
2 – 3	0.2355	2.10	31.5 mil
3 – 4	0.2355	2.10	31.5 mil
4 – 5	0.3618	1.20	18.0 mil

The electrical length of each resonator was then calculated as described in [36], shown below in equation (44).

$$\theta = \frac{\pi}{2}\left(1 - \frac{BW}{2}\right) \qquad (44)\ [33]$$

This value was calculated to be 160.52º, corresponding to 213.52 mil.

In order to achieve an optimal match between the 50-ohm line feeding transmission line and the first resonator, the imaginary contribution of the reflection from each

end of the resonator cancels. Therefore, the electrical length from closer side of the resonator would be given by (45):

$$\theta_{Feed} = \frac{\theta - 90º}{2} \quad (45)\ [33]$$

This corresponds to an electrical length of 35.26º from the closer end of the resonator, or 46.91 mil. Based on all the calculated values in this section, a filter layout was produced for simulation.

4.2.1 Layout of Interdigital Filter

As there are less behavioural models available for multiple coupled resonators, the design was implemented directly in layout for simulation.

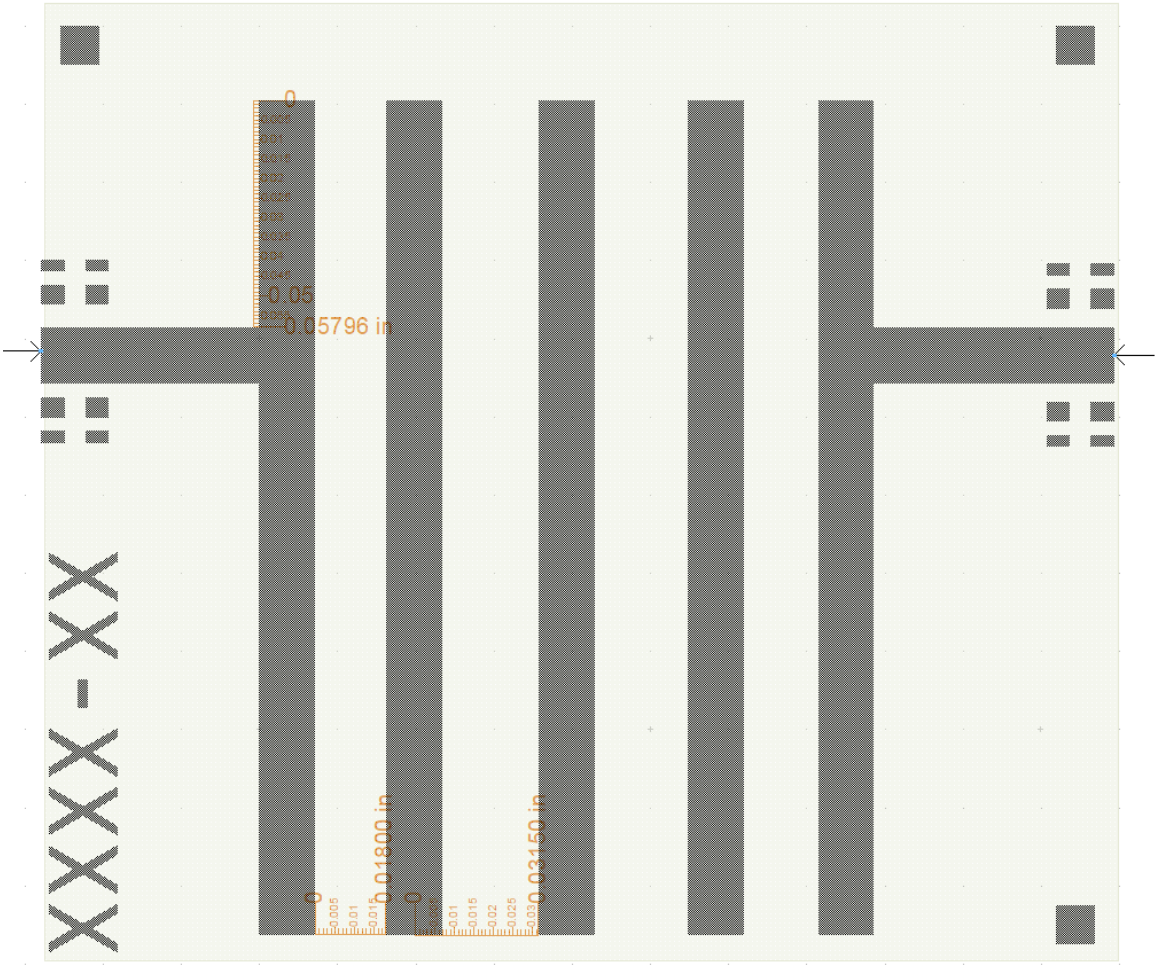


Figure 12: Initial layout of interdigital filter based on theoretical calculations.

The design was simulated using the method of moments EM simulator in Keysight ADS. The results of the EM simulation are shown below in Figure 13. One can see from these results that the filter center frequency is slightly higher than desired, and the bandwidth is slightly expanded.

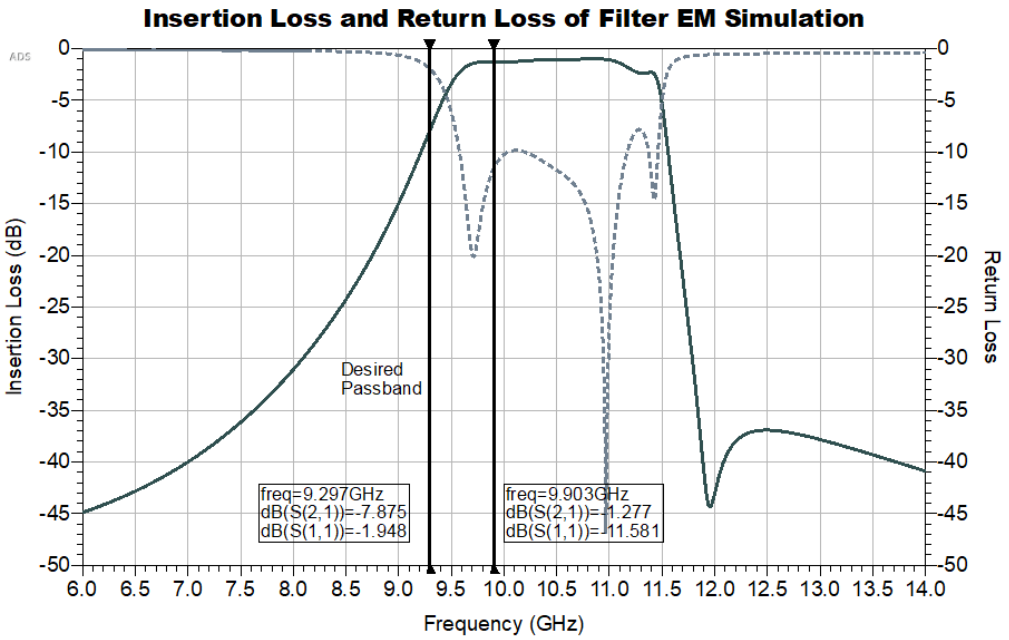


Figure 13: S-parameter simulation of filter design.

4.2.1 Iteration to Correct Frequency Response

Increasing the electrical length of each resonator will decrease the bandwidth, as can be seen by (44). The center frequency is set by element spacing as seen by [36]. To correct the response, the length of the resonators was incrementally increased, and the spacing incrementally increased until the bandwidth and center-frequency matched the design specification. The lengths of all elements were expanded to 213 mil, or 172.12º electrical length. The spacing between elements 1 and 2 (and by symmetry 4 and 5) expanded to 20.1 mil, and the spacing between elements 2 and 3 (and by symmetry 3 and 4) expanded to 35.3 mil. The results of the EM simulation are shown below in Figure 14. This figure shows an improved response in terms of insertion loss, but that return loss as suffered by the iteration. As the line length increased, the position of the transmission line feeding the first and last element needs to be readjusted according to (45). The position of this line was readjusted to

41.06º from one end as per (45), and then iteratively adjusted until the optimal insertion loss was found.

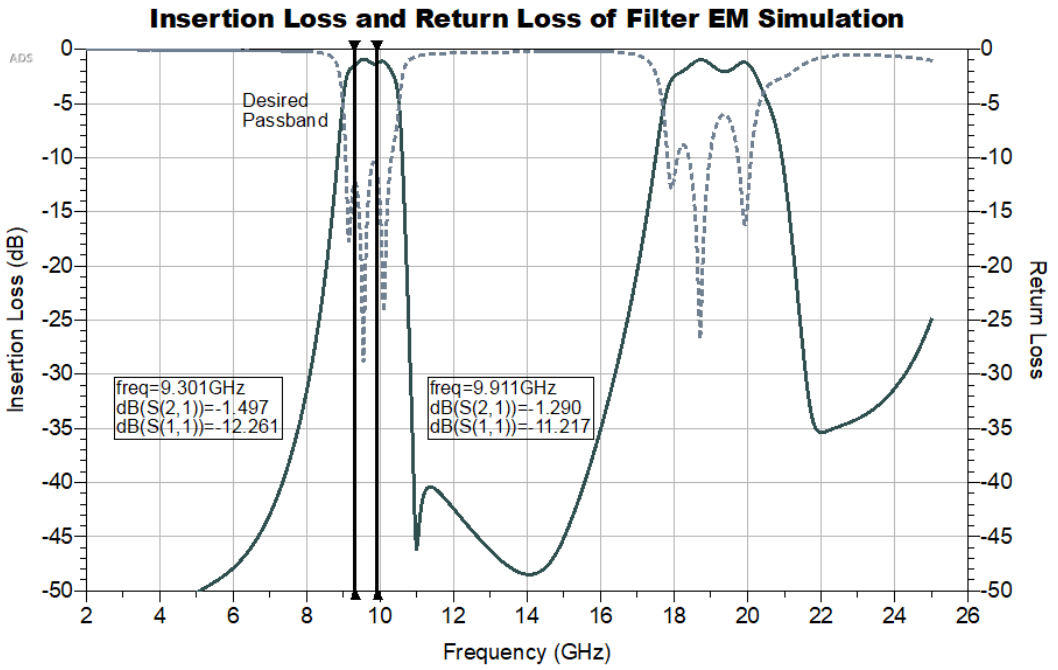


Figure 14: EM simulation of filter layout after iteratively adjusting resonator length and spacing to optimize bandwidth and center frequency.

The final layout is present below in Figure 15. The final position of the feeding line from the open end of the resonator was 68.50 mil. This improved the return loss of the filter, ensuring that the design achieved better than 15 dB return loss over the entire band of operation. The wideband plot (shown in Figure 16) has also been annotated to show the rejection of the image band as well as the LO. Figure 17 shows a better resolution plot of the filter passband. A comparison from these results to the specification for the filter is given below in Table 18: Comparing EM simulated results to specification.

Table 18: Comparing EM simulated results to specification.

	Specification	**EM Simulation**
Passband Frequency (0.5 dB equiripple)	9.3 – 9.9 GHz	9.254 – 10.19 GHz
Passband Amplitude Variation	<0.5 dB	0.5 dB
Image band rejection	> 30 dB	> 39.50 dB
Insertion Loss	< 3dB	< 1.3 dB
Return Loss	> 10 dB	> 18.5 dB

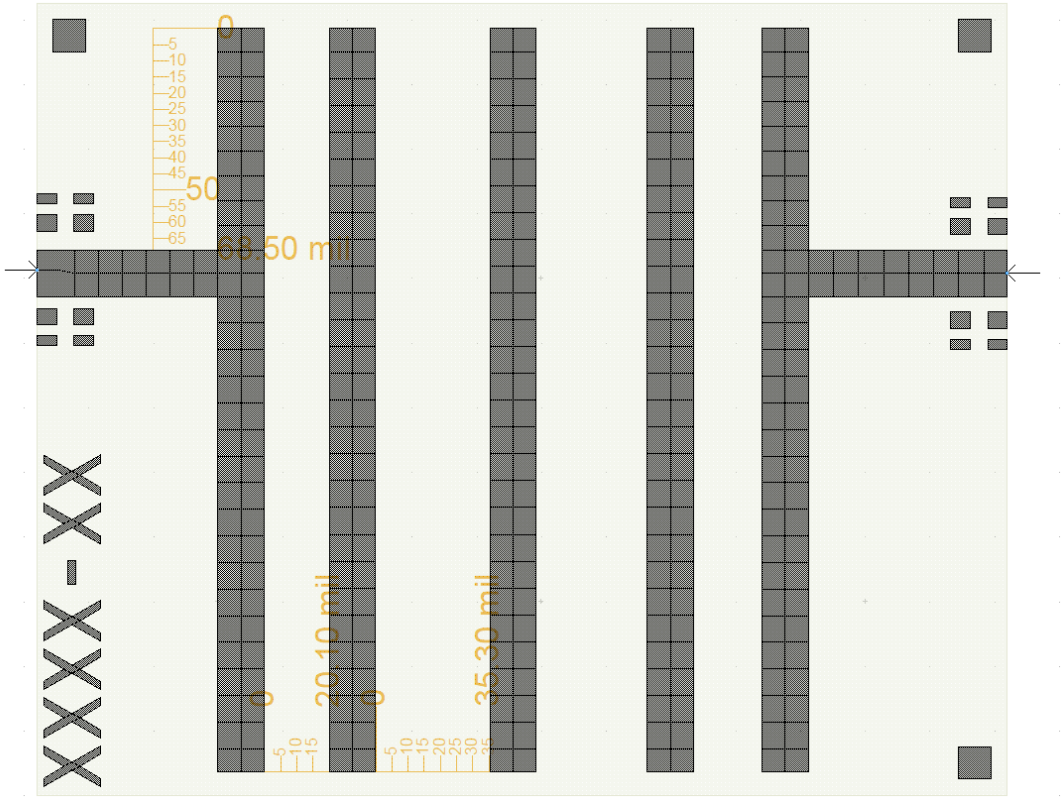


Figure 15: Final layout of interdigital filter after optimization.

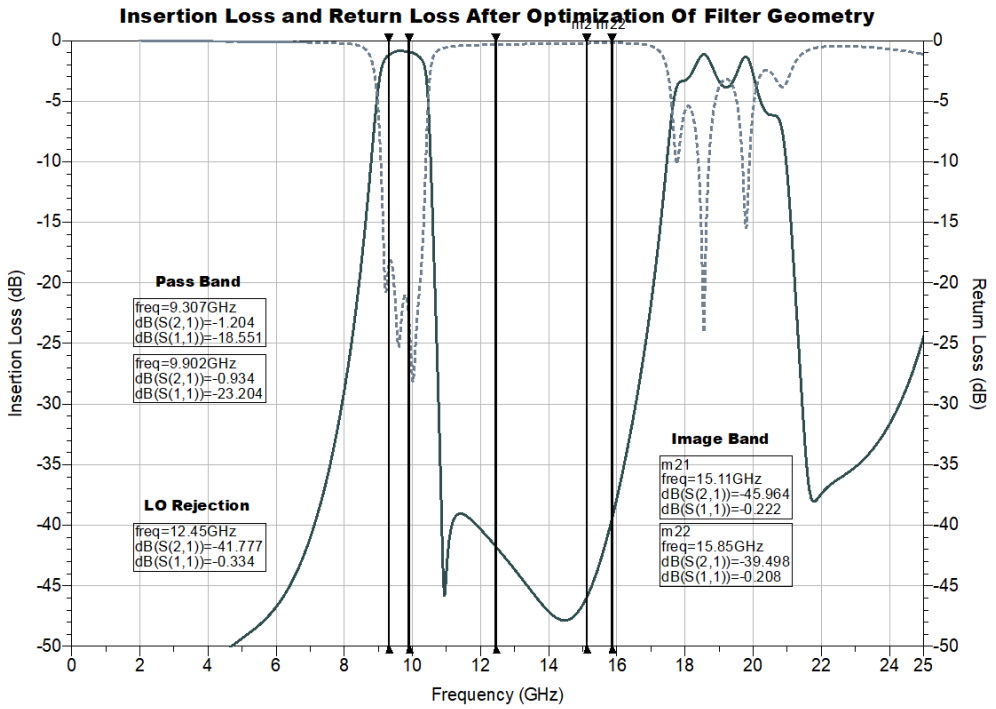


Figure 16: Wideband frequency response of interdigital filter.

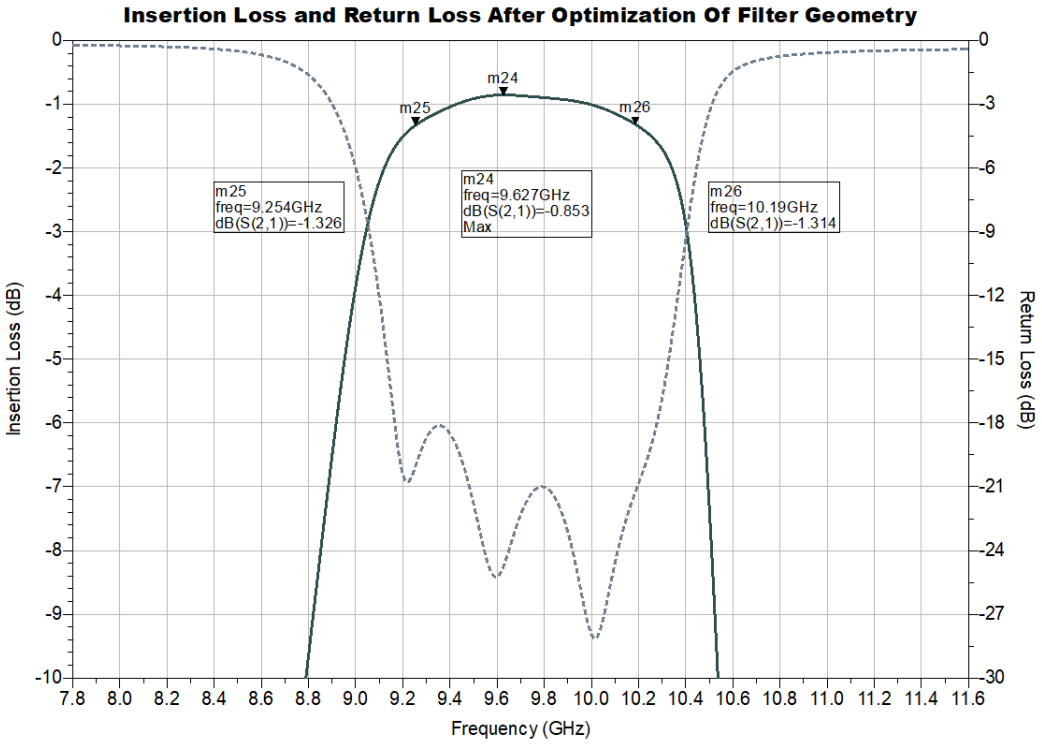


Figure 17: Insertion loss and return loss in filter passband.

4.2.3 Simulation over Manufacturing and Temperature Variance

The variance over manufacturing and temperature were simulated as discussed in 4.1.3 Design analysis over manufacturing variation and operating temperature. The results are shown below in Figure 18 and Figure 19. The results are compared in Table 19.

Table 19: Comparison of simulation over temperature and manufacturing variation to specifications.

	Specification	**EM Simulation**	**Simulation over Variation**
Passband Frequency (0.5 dB equiripple)	9.3 – 9.9 GHz	9.254 – 10.19 GHz	9.3 – 10.15 GHz
Passband Amplitude Variation	<0.5 dB	0.5 dB	0.5 dB
Image band rejection	> 30 dB	39.50 dB	36.49 dB
Insertion Loss	< 3dB	< 1.32 dB	< 1.32 dB
Return Loss	> 10 dB	> 18.50 dB	> 17.41 dB

Based on these results, the design can be considered suitable for the system.

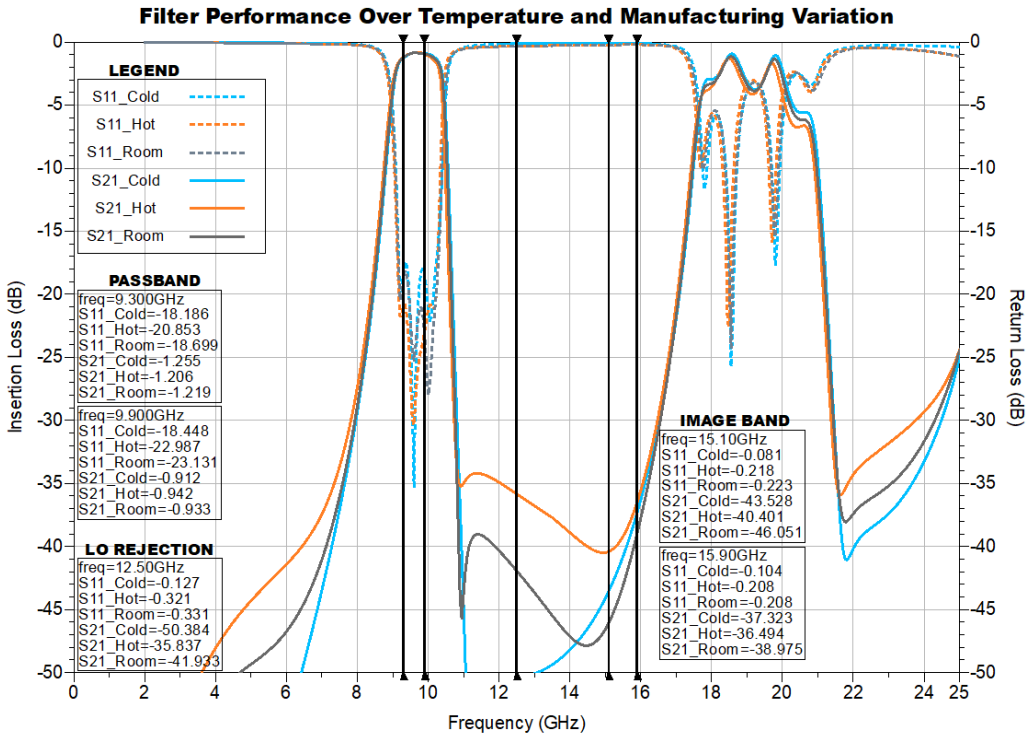


Figure 18: Filter performance over temperature and manufacturing variation.

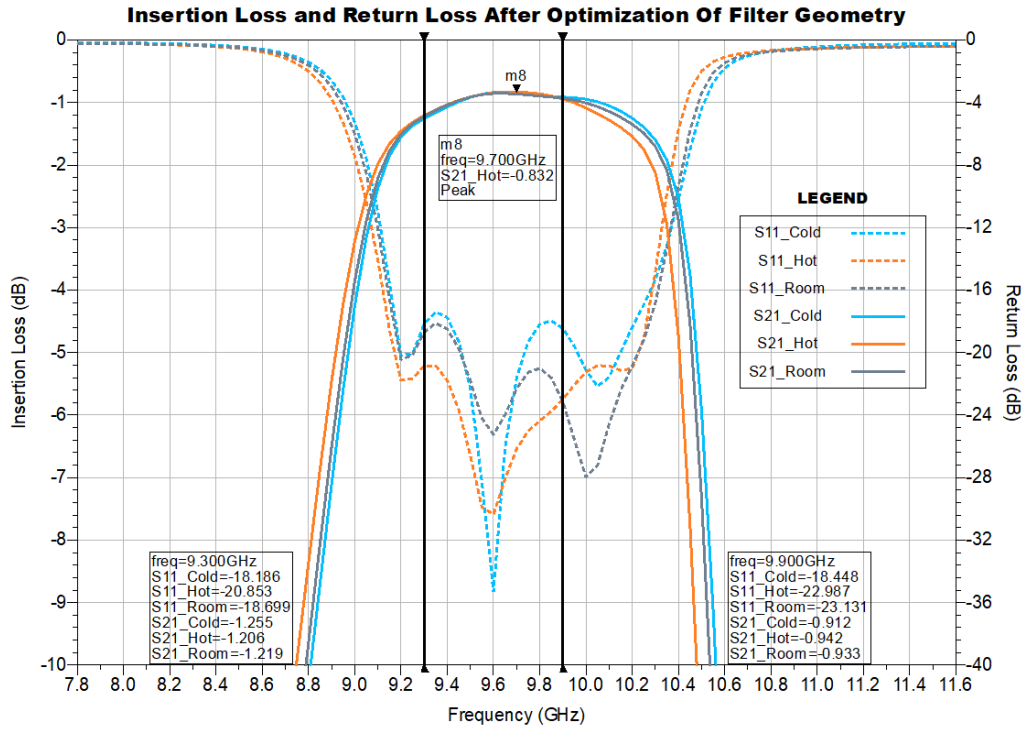


Figure 19: Filter passband over temperature and manufacturing variance.

4.3 RF Interconnects

All RF interconnects between modules are designed as microstrip lines on an intermediary substrate. The interconnecting substrates are reflow soldered onto the housing in between the die. The substrate selected for all RF interconnects is Rogers TMM10i. This substrate was selected as the dielectric constant for Rogers TMM10i is 9.8, which is very close to the alumina substrates used for dies. The advantage of this is that designs can move easily between alumina and TMM10i, allowing designs to move between modules and interconnect seamlessly if required. It will also keep the line widths between carriers and interconnect very similar. The width for a 50-ohm line was calculated using the LineCalc tool in Keysight ADS.

The disadvantage of using Rogers TMM10i as a substrate is a manufacturing difficulty; the bond strength between the conductor and substrate is low enough that during wire bonding the conductor can lift from the substrate. In order to mitigate this risk, ribbon bonds are to be used in manufacturing. The end on the ribbon bond connected to the Rogers TMM10i is to be gap soldered to prevent mechanical failure, while the end connected to the alumina substrate are ribbon bonded as shown in the manufacture instruction included in the drawing (shown below in Figure 20).

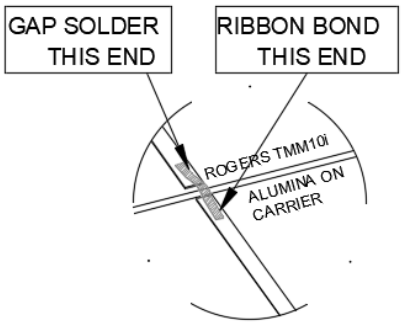


Figure 20: Interface assembly instruction for ribbon bond between Rogers TMM10i included on the manufacturing drawings.

4.4 STALO PCB Design

An external PCB was included in the design to provide the STALO for frequency conversion. The STALO is produced by a COTS fractional PLL with integrated VCO capable of synthesizing 12.4 – 13.4 GHz. The device was common to the UDC version of the design. It is imperative this component remains the same to allow the results of this research to be integrated into the system without revision to the STALO control software. A review of the part demonstrated an appropriate jitter and frequency range to be used in this design. The STALO PCB is required to meet the specifications outlined in Table 20 below.

Table 20: STALO PCB Specifications.

Description	**Specification**	**Comment**
Supply 1 Voltage	+6 VDC	
Supply 2 Voltage	+16 VDC	
Supply 1 Current	< 300 mA	
Supply 2 Current	< 50 mA	
STALO Frequency (GHz)	12.4 – 12.9 GHz	-
STALO Output Power (dB_m)	-2 to +4 dB_m	-
STALO reference	PCB to lock to external Reference	-
STALO Ref Frequency (MHz)	50 MHz	50 MHz VCXO on PCB
Reference Absolute Pull Range (PPM)	± 20 after reflow, supply, temperature, and 10 years aging	Selected VCXO on PCB achieves specification.
RMS Jitter (fs)	500 fs	Allows a velocity measurement error of ±1 m/s in 99.7% of all velocity measurements.
EXT Reference Input	10 MHz	
STALO Control Protocol	SPI	-

4.4.1 Loop Filter Design

As the COTs PLL contains an integrated VCO, the only required additional design for this synthesizer is the loop filter. The VCO tuning voltage range exceeds the charge-pump output voltage, and so an active filter was selected.

The PLL datasheet recommends 100 kHz loop bandwidth for optimal phase noise performance [38] which should in turn minimize the rms jitter. All selected design parameters are given below Table 21. The design methodology followed the active filter design presented by Banerjee in [39].

Table 21: Selected design parameters for PLL loop filter

Parameter	**Selected Value**	**Comment**
F_{OUT}	12.8 GHz	STALO required for RF output of 12.8 GHz (based on most common operating frequency for system).
F_{REF}	50 MHz	System reference generated on control PCB.
N	256	Divider ratio based on above parameters.
K_ϕ	2 mA	Based on PLL datasheet.
K_{VCO}	190 MHz/V	Based on PLL datasheet.
BW	100 kHz	Based on recommendation from PLL datasheet.
ϕ	45°	Selected to ensure stability.
ATTEN	10 dB	Recommended reference spurs attenuation from [39].

Based on these parameters, the time constants of the system were calculated, as described in [39].

$$T_3 = \frac{\sqrt{10^{\frac{ATTEN}{10}} - 1}}{2\pi \cdot F_{REF}} = 9.55\ ns \quad (46)\ [39]$$

$$T_1 = \frac{\sec\phi - \tan\phi}{2\pi BW} - T_3 = 649.69\ ns \quad (47)\ [39]$$

$$T_2 = \frac{1}{(2\pi BW)^2(T_1 + T_3)} = 3.84\ \mu s \quad (48)\ [39]$$

From these values, the component values can be calculated:

$$C_1 = \left(\frac{T_1}{T_2}\right)\left(\frac{K_\phi K_{VCO}}{(2\pi BW)^2 N}\right)\sqrt{\frac{1 + (2\pi BW\ T_2)^2}{(1 + (2\pi BW T_1)^2)(1 + (2\pi BW T_3)^2)}} = 1.54\ nF \quad (49)\ [39]$$

$$C_2 = C_1\left(\frac{T_2}{T_1} - 1\right) = 7.56\ nF \quad (50)\ [39]$$

$$C_3 = \frac{C1}{10} = 154\ pF \quad (51)\ [39]$$

$$R_1 = \frac{T_2}{C_2} = 508.36\ \Omega \quad (52)\ [39]$$

$$R_2 = \frac{T_3}{C_3} = 62.09\ \Omega \quad (53)\ [39]$$

These values were simulated using the ADIsimPLL simulator tool supplied by Analog Devices. The schematic used for simulation is shown below Figure 21. The results of the simulation showed a phase margin of 69.8º, and a loop bandwidth of 115 kHz. The rms jitter was simulated at 154 fs corresponding to a velocity measurement uncertainty of ±0.139 m/s. Although slightly expanded from the design values, the velocity uncertainty exceeds the specification, and so the design was considered acceptable. The component values were then moved to standard sizes found in a 403-package size. The updated values are given in Table 22.

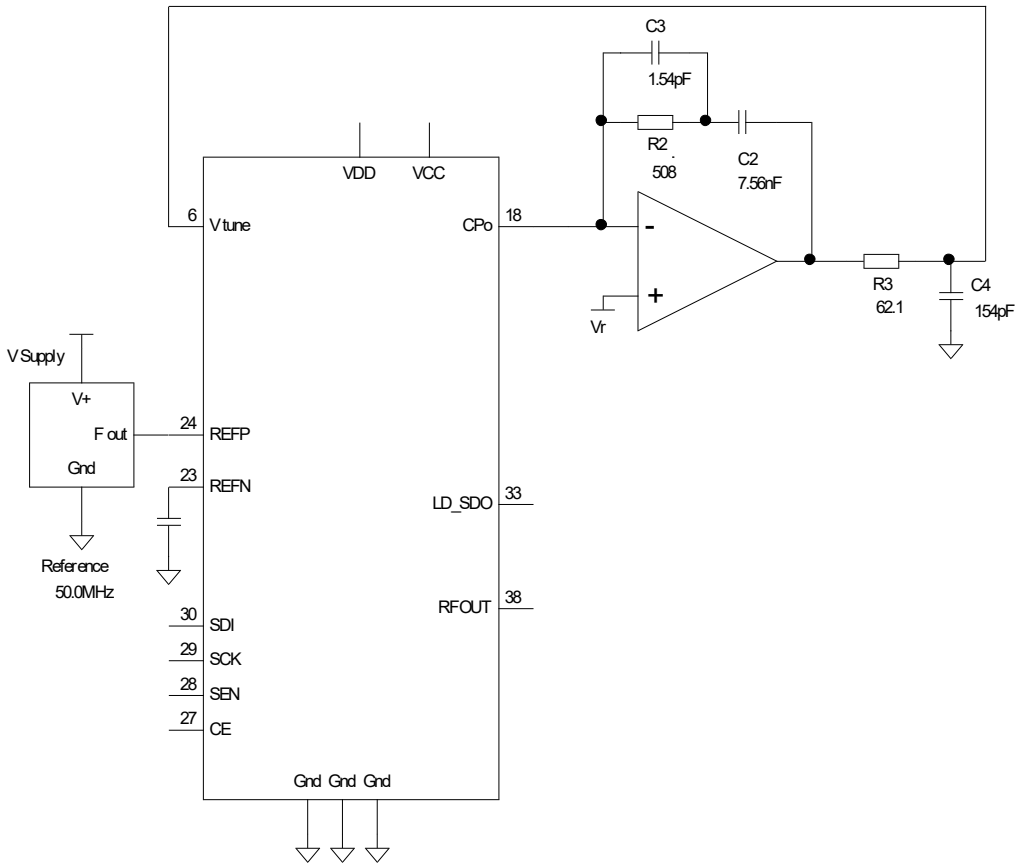


Figure 21: Simulation of loop filter in ADIpllSIM using calculated component values.

Table 22: Revised component selection based on standard capacitor/resistor sizes.

Component	**Calculated Value**	**Available Value**
C1	1.54 nF	1.5 nF
C2	7.56 nF	7.5 nF
C3	154 pF	150 pF
R1	508 Ω	510 Ω
R2	62.1 Ω	62 Ω

The simulation was re-run using standard capacitor/resistor values as indicated in Table 22. The revised simulation once again showed a phase margin of 69.8º and a loop bandwidth of 116 kHz; the small component changes did not significantly impact the loop performance. A full simulation report is available in APPENDIX

A: SIMULATION RESULTS OF STALO PLL. As the design met the stability and bandwidth requirement, it was accepted.

4.4.3 Block Diagram of STALO PCB

The STALO PCB must provide 2 outputs to the UDC, one for up-conversion and the other for down-conversion. The output of the PLL will go through a COTs band-pass filter provided by mini-circuits to reject any out-of-band spurs, and then be split using a Wilkinson. Both outputs of the splitter will then run through a 0 dB attenuator, before connecting to the UDC on an RF feedthrough pin. The 0 dB attenuator is included as a provision, to allow the installation of an attenuator during test if there is a return loss issue with the RF feedthrough pin.

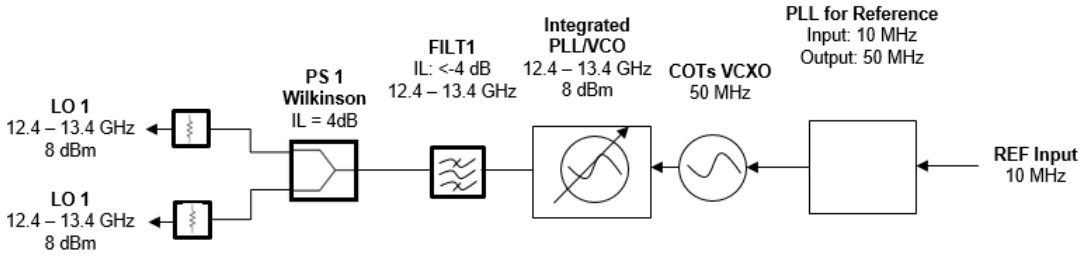


Figure 22: Block diagram of STALO PCB

4.4.3 Output Power Splitter Design

The power splitter was designed as a microstrip Wilkinson splitter to be implemented on the STALO PCB. The Wilkinson was designed in Keysight ADS, and then ported to Altium for integration into the full layout of the board. The full

analysis and design methodology for a Wilkinson divider is presented in [33]. The characteristic impedances of a Wilkinson divider are shown in Figure 23.

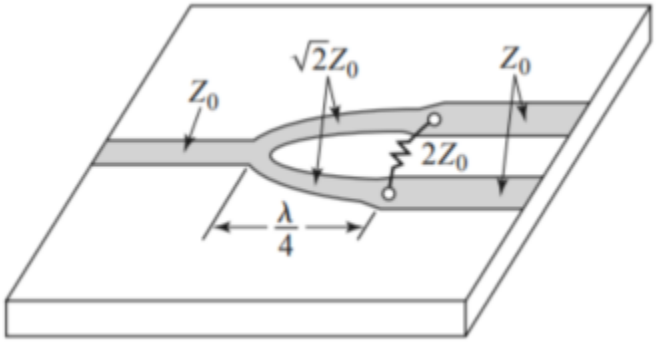


Figure 23: Characteristic impedance of a Wilkinson Splitter as determined by Pozar presented in [32] .

Based on this, an ideal schematic simulation was done in Keysight ADS to verify the theory. The schematic used is shown below in Figure 24.

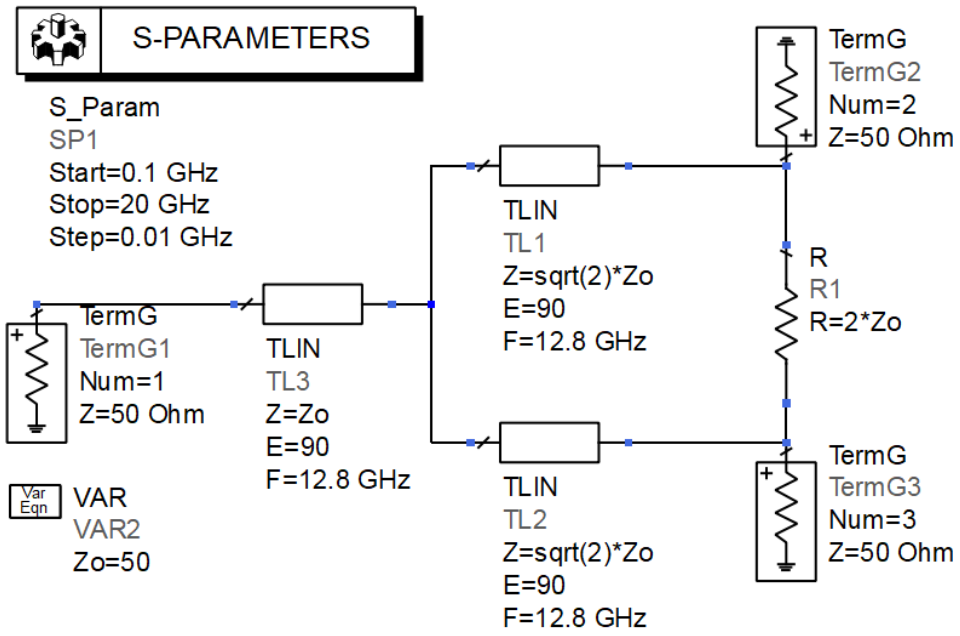
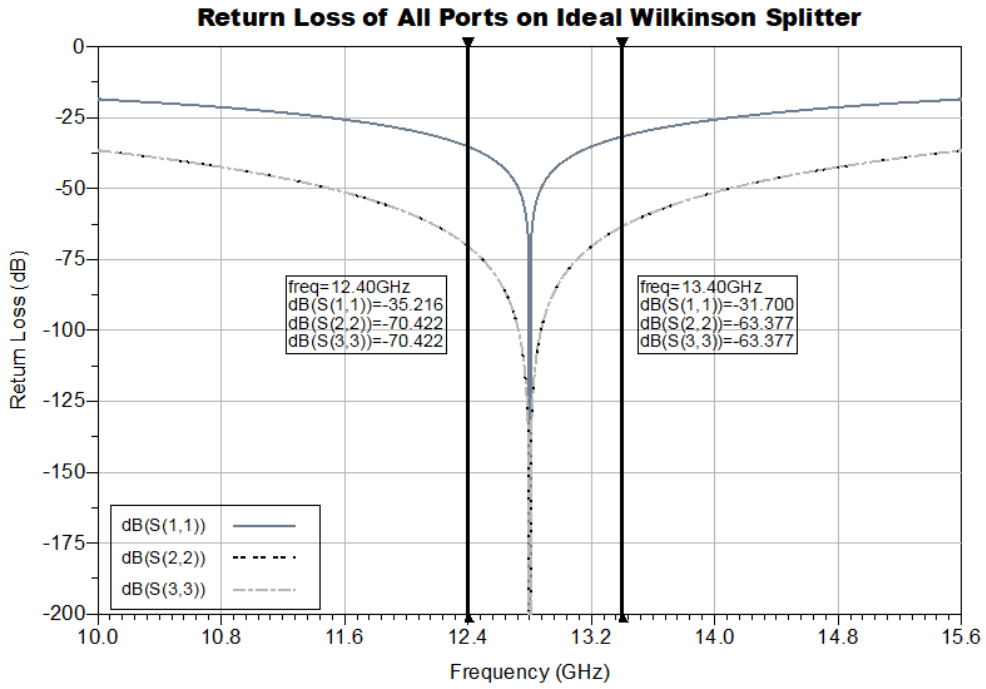


Figure 24: Schematic used to simulate Wilkinson splitter in Keysight ADS.

The results of the s-parameter simulation are given below in Figure 25. The ideal design shows better than 30 dB return loss on all ports, and no phase/amplitude imbalance as would be expected for an ideal design.



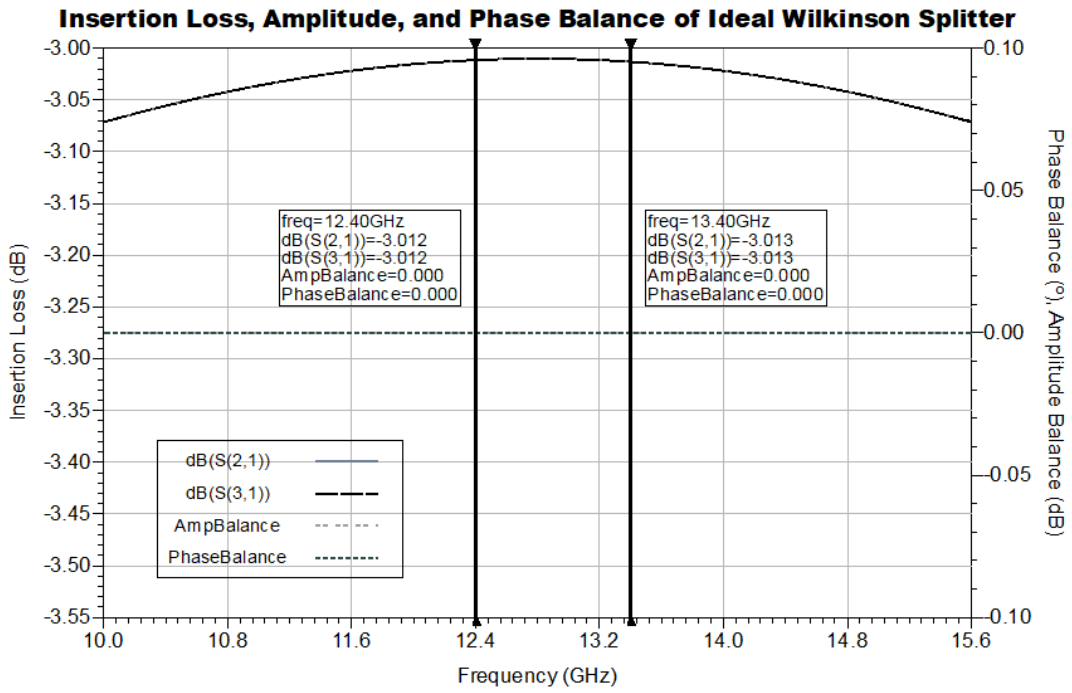


Figure 25: Simulated results of Ideal Wilkinson Splitter.

As the design is somewhat trivial, it was moved directly into layout without further behavioural modelling at the schematic level. A width of 44.74 mil was calculated for 50 Ω, and a width of 70.7 Ω was calculated as 25.85 mil. The layout was implemented as shown in Figure 26. The PCB utilizes co-planar waveguide transmission lines to reduce radiated RF and coupling between traces on the PCB. For the design of more complex shapes, such as the splitter, microstrip were used as discontinuities in the co-planar ground planes are difficult to design around. For this reason, the final EM simulation of the splitter ended each port with a transition to coplanar waveguide to allow the EM simulation to capture the effect of this discontinuity.

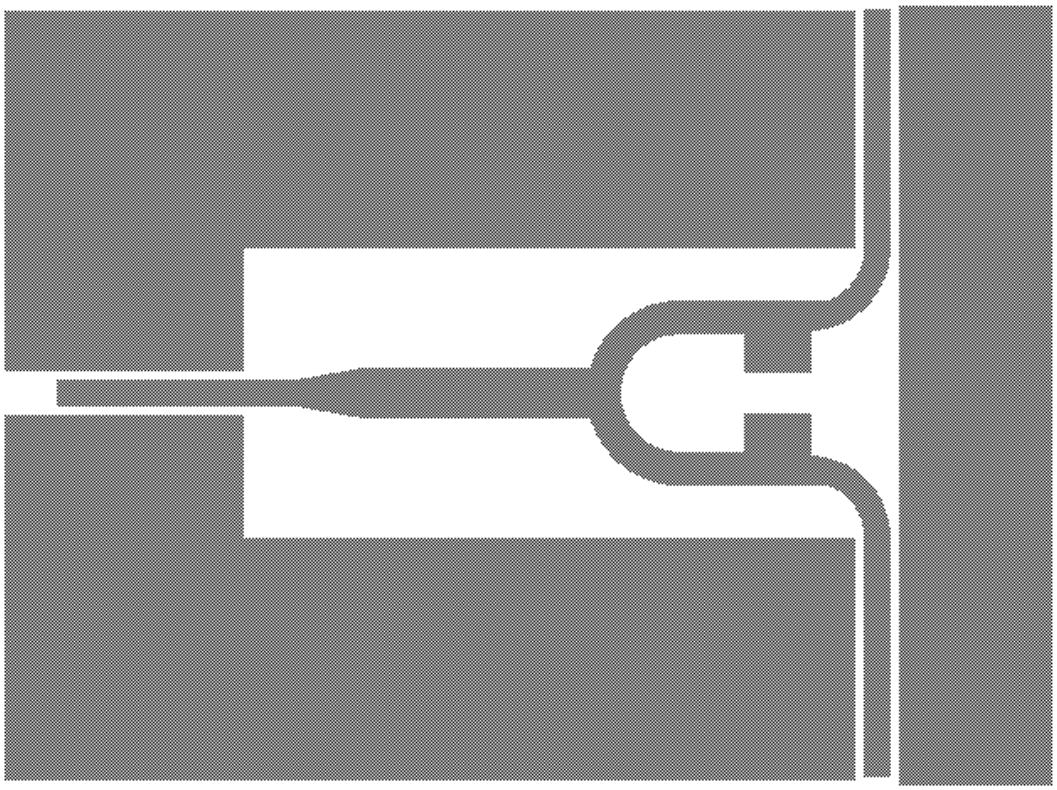


Figure 26: Layout of Wilkinson Splitter used for EM simulation

The design was simulated, including a 100 Ω behavioural model of a resistor, with the results shown below in Figure 27. It can be seen from these results that the return loss of each port is better than 20 dB and the insertion loss is less than 0.2 dB. This design was considered acceptable for use on the STALO PCB.

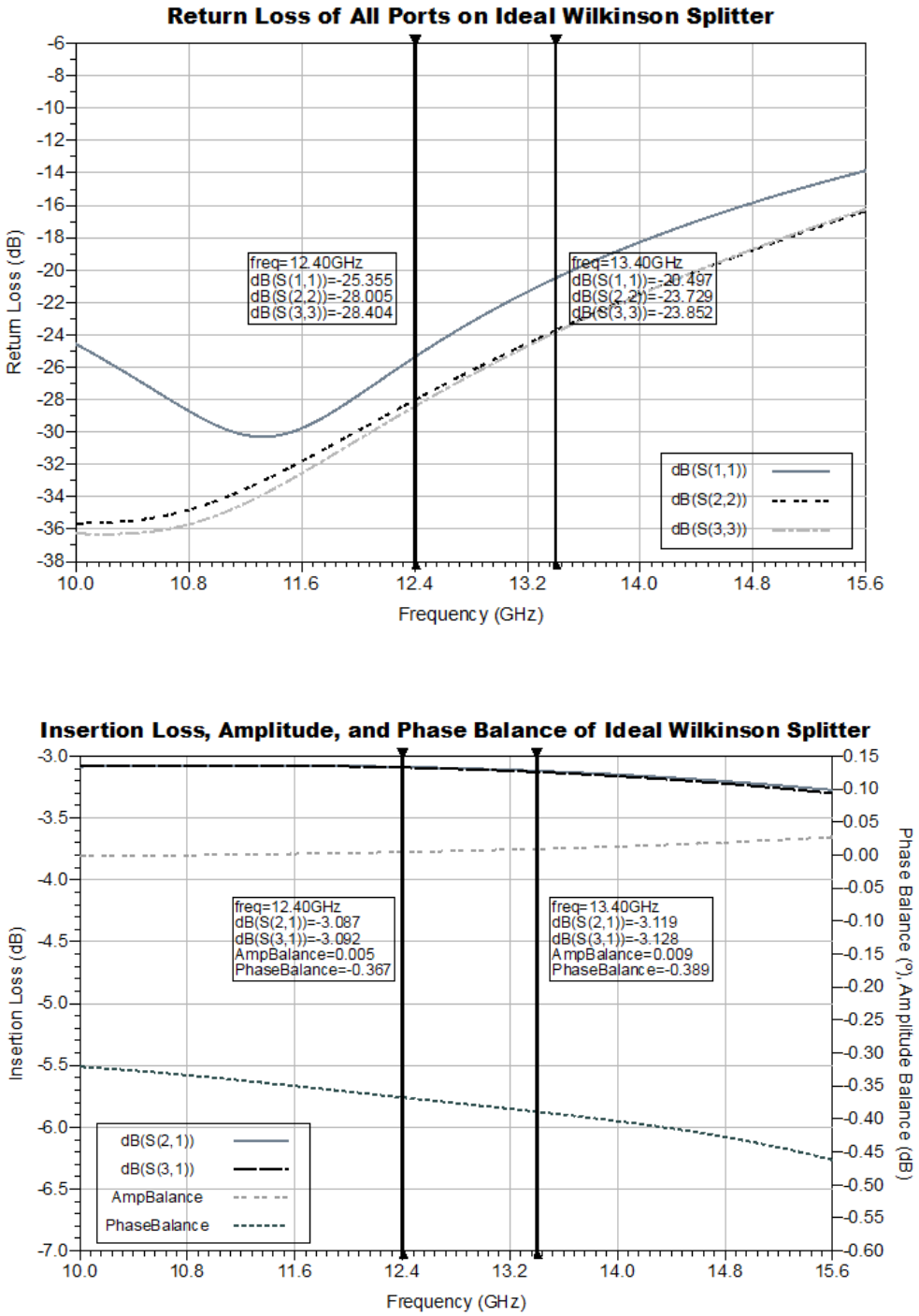


Figure 27: Results of EM simulation of Wilkinson splitter layout.

4.4.4 Layout of the STALO PCB

The layout of the STALO PCB was undertaken with the following considerations:

- The PCB was a 4-layer board, comprised of 2 15 mil ROGERS 4350B cores.
- All RF is run on the top board; internal layers are used for power and data routing only.
- Data lines (for STALO control) are isolated from RF with a continuous ground plane.
- The bottom layer will contact the HMIC housing and be reflow soldered on to the housing for good electrical contact. All solder-mask has been removed off the back layer, except for a small region of overhang containing connectors.
- All layers have a polygon pour connected to ground where no other routing elements are required.
- All ground planes/pours are via-stitched at $\frac{\lambda}{5}$ to ensure equal potential
- All RF traces are via-shielded at a spacing of $\frac{\lambda}{10}$ to ensure coplanar waveguide ground on top and bottom maintain equal potential
- All IC decoupling caps are located as close as possible.
- All DC lines are regulated with low noise, low drop-out linear regulators with ripple rejection at frequency > 1 MHz to reduce power supply noise.
- All RF components and traces are installed inside a shield, soldered on to a continuous ground pour.

- Solder mask is removed over any RF trace to reduce its effect on the characteristic impedance of that trace.
- A lid height of 8 mm was included in the EM model of the substrate to simulate the RF shield.

The layout of the PCB was completed in Altium Designer. The Wilkinson splitter was exported from ADS and imported into the Altium Design. A 3-D model of the final design is shown below in

Figure 28.

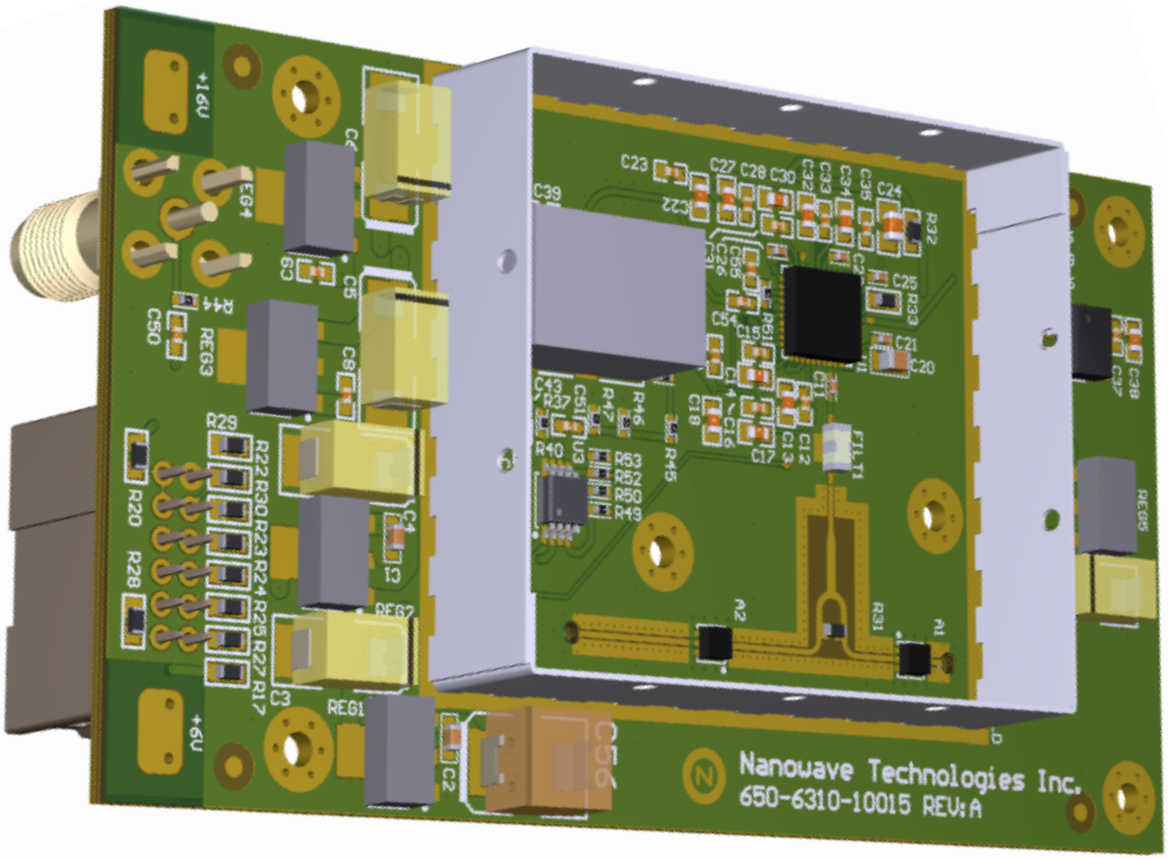


Figure 28: Three dimensional model of STALO PCB from Altium Designer.

4.5 RF Simulation of COTs Modules

For each COTs module supplied by Nanowave Technologies, an EM simulation was done in Keysight ADS. This served two purposes; the EM simulation allowed a verification of the specification for each module as provided by the manufacturer. It also allowed for generation of an EM model for each module to be used in an EM co-simulation of the entire system.

For each module, the layout was imported from AutoCAD into Keysight ADS, and an EM simulation of the layout generated. An example of an EM simulation generated from the layout of 6080432-94 shown below in Figure 29.

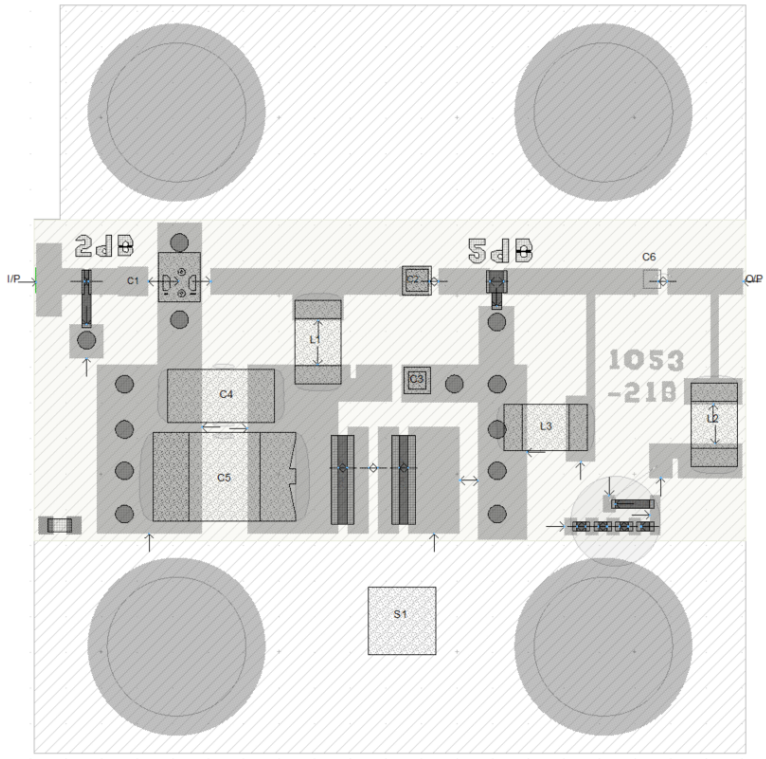


Figure 29: AutoCAD layout of 6080432-94 imported into Keysight ADS for EM simulation.

This was done for all modules used in the design, except for the output amplifier stage. The final gain stage comprises several modules working together in one pocket of the HMIC with high gain. This gain stage provides significant risk of instability if transmission lines on output modules couple to transmission lines on input modules. To assess this risk, a more complex multi-substrate simulation was generated as shown in Figure 30. This simulation nested all three types of substrates used into one region, bounded by a substrate layer for each type.

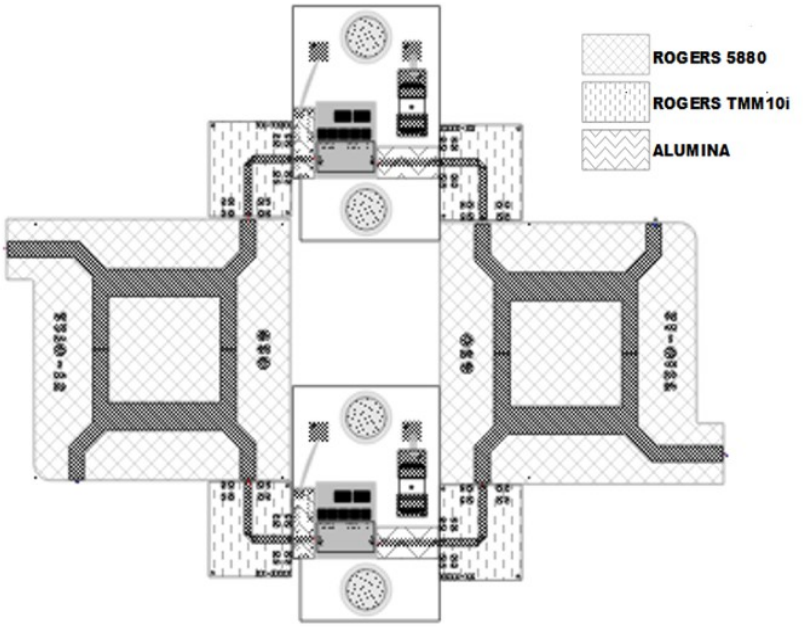


Figure 30: EM simulation of output amplifier stage using nested substrates.

Using this EM layout and S-parameter files of the output amplifier modules, the small-signal stability was assessed using the geometrically defined mu and mu-prime stability factor. These stability factors measure the distance from the center of the Smith chart to a region of instability for the source and load ports of a 2-port network. Having a value greater than 1 implies unconditional stability. These

stability criteria were assessed from DC to the highest frequency showing gain (20 GHz). The results, shown below in Figure 31, showed the output would be unconditionally stable.

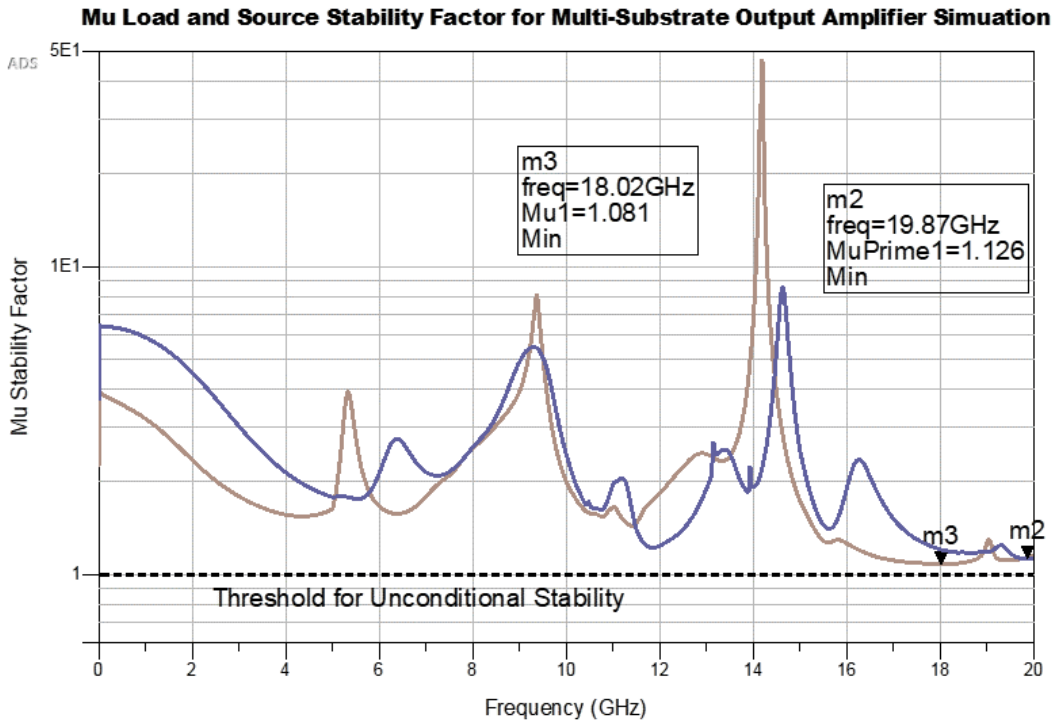


Figure 31: Stability of Output Amplifier Stage.

All other modules were simulated individually, with the EM models connected at the schematic level as mentioned above.

4.5.1 Configuration of EM simulation

In order to run an EM simulation, a substrate definition needs to be provided. This section provides the substrate configuration for each type of substrate used in the system.

4.5.1.1 Configuration of Rogers TMM10i substrate for EM simulation

The EM stack-up for the Rogers TMM10i substrate is given below in Figure 32. The conductor thickness for both top and bottom covering was set to 35 microns. The conductor material was set to copper, and its conductivity set for 5.6×10^7 S.

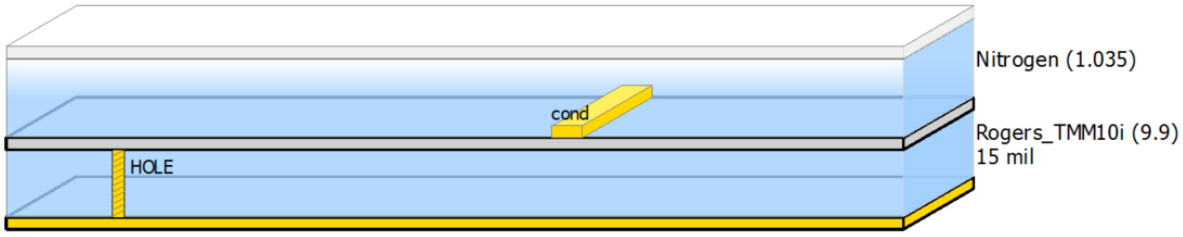


Figure 32: EM Stack-up for Rogers TMM10i substrate

4.5.1.2 Configuration of Alumina substrate for EM simulation

The EM stack-up for the Alumina substrate is given below in Figure 33. The conductor thickness for both top and bottom covering was set to 5 microns. The conductor material was set to copper, and its conductivity set for 4.1×10^7 S.

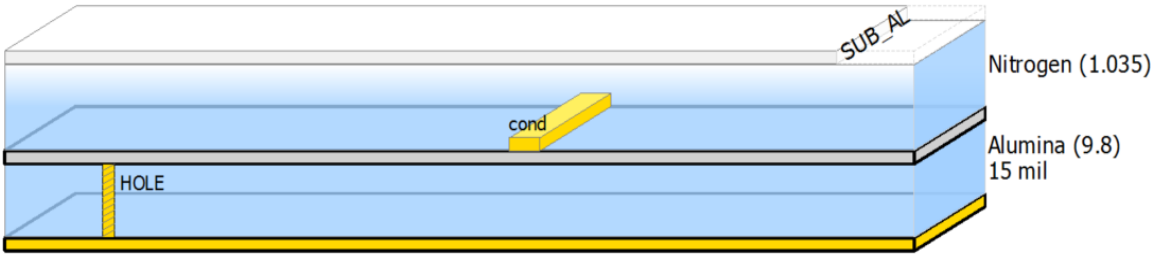


Figure 33: EM Stack-up for Alumina substrate.

4.5.1.3 Configuration of Rogers 5880 substrate for EM simulation

The EM stack-up for the Alumina substrate is given below in Figure 33. The conductor thickness for both top and bottom covering was set to 35 microns. The conductor material was set to copper, and its conductivity set for $5.6x10^7$ S.

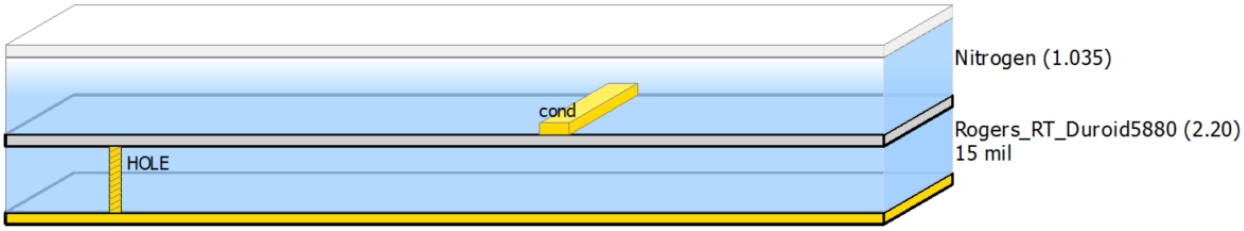


Figure 34: EM Stack-up for Rogers 5880 substrate.

4.6 System Simulation

A system simulation was generated using the EM models generated in section 4.5 for verification of the results. The following section discusses the methodology and results of these simulations.

4.6.1 Methodology of Simulation

For each COTs module, the EM model was paired with some sort of device model to allow for simulation. For small signal simulations, s-parameter files were used when available for all active and passive devices. A noteworthy exception to this is the image reject mixer, which did not have any behavioural model available. The modelling of this mixer is discussed further in section 4.6.1.1 Behavioural model Image Reject Mixer.

For large signal simulations, any s-parameter file used was replaced with an ADS device behavioural model configured based on the datasheet. Behavioural models

had all parameters modelled over temperature using a polynomial regression to assess variation over operating temperature. The system was verified over manufacturing and thermal variation as discussed in section 4.1.3 Design analysis over manufacturing variation and operating temperature.

4.6.1.1 Behavioural model Image Reject Mixer

The manufacturer of the IR mixer die was unable to provide a behavioural model of the mixer, and only had S1P files for each port. For this reason, the small signal parameters of the mixer were simulated using a behavioural model as shown below Figure 35. This behavioural model allowed for an I/Q output including phase and amplitude error, allowing the image rejection of the mixer and coupler to be properly assessed. The S1P files provided by the manufacturer were used for any return loss simulations (including at the system level).

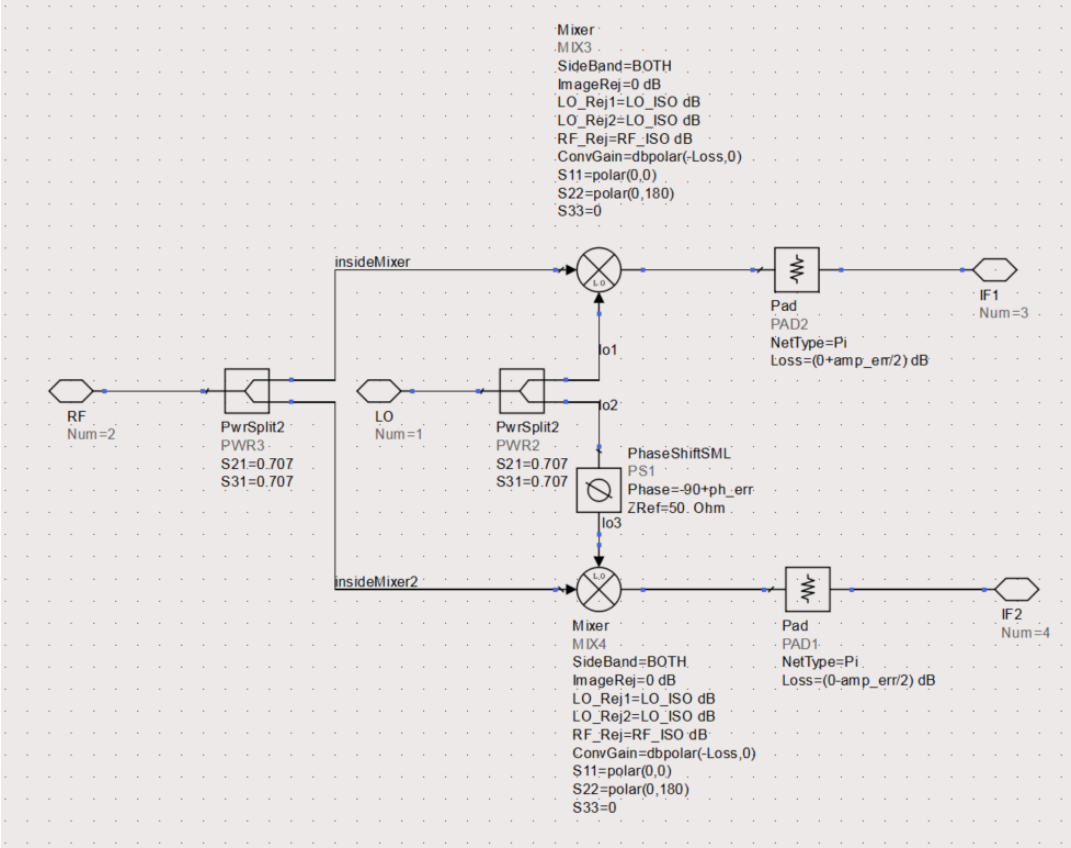


Figure 35: Behavioural model of IR mixer

4.6.2 Simulation of Up-Converter

The up-converter was simulated using the EM co-simulation as shown below in Figure 36. The results of the simulations were compared against the system specifications to verify the RF performance of the design.

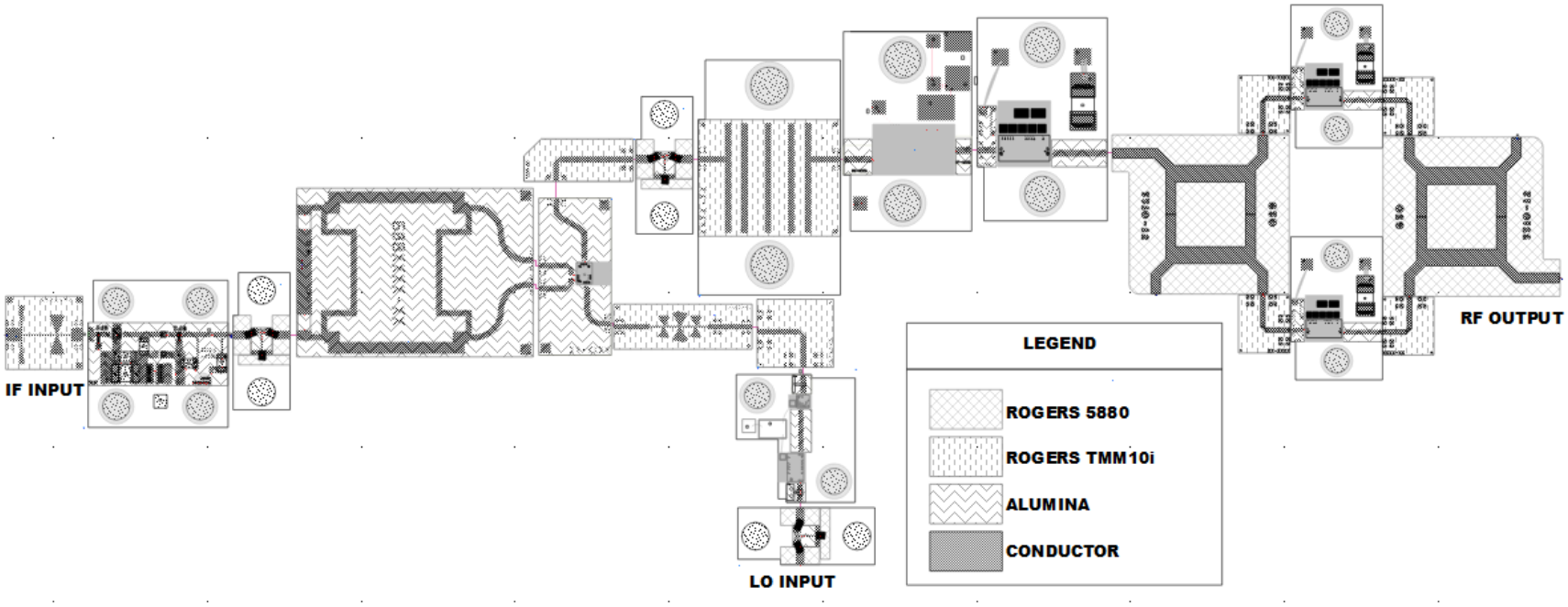


Figure 36: Schematic level EM co-simulation of the up-converter done using Keysight ADS.

4.6.2.1 Verification of Saturated Output Power

The output power was simulated using a harmonic balance simulation, sweeping the input power and plotting the output power. The temperature of the simulation was swept from -30 ºC to +65 ºC in steps of ten degrees (with a final step of 5). The operating frequency was swept from 9.3 GHz to 9.9 GHz in steps of 100 MHz by fixing the input at 3.10 GHz and moving the STALO frequency from 12.4 GHz to 13.0 GHz in steps of 100 MHz. Manufacturing variance was simulated over all other variation at the maximum, nominal, and minimum values of variation. The result of sweeping all these parameters is shown below in Figure 37: Effect of manufacturing, temperature, and operating frequency on saturated output power. It can be observed that over the range of possible variation, the design continues to meet the specified saturated output power, providing a minimum of +31.72 dB_m of saturated output power. It is also worth noting that the design is always into saturation at the specified operating point.

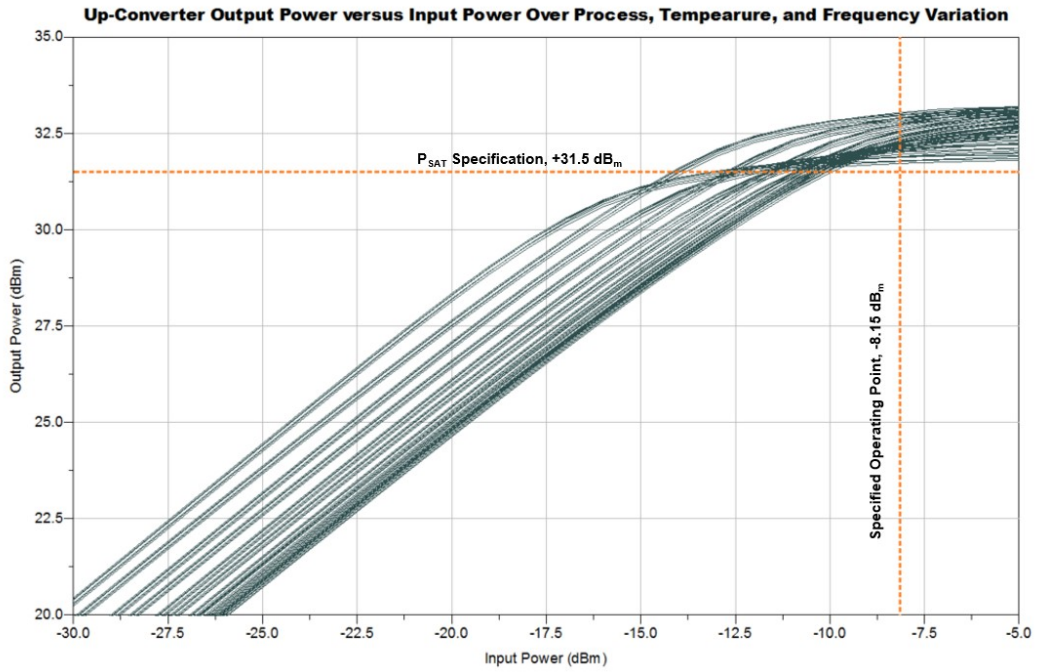


Figure 37: Effect of manufacturing, temperature, and operating frequency on saturated output power.

4.6.2.2 Verification of Conversion Gain

The conversion gain was simulated using a harmonic balance simulation, sweeping the input power and plotting the resultant conversion gain. The results shown in Figure 38 were generated in the same simulation as discussed in 4.6.2.1 Verification of Saturated Output Power, and thus subject to the same manufacturing, frequency, and temperature variations. Overall possible variation, it can be observed that the small signal conversion gain (the flat portion of the curve) does not fall below the specification. One might argue the performance is borderline in some cases. This was deemed acceptable as the output power (measured in the previous section) was well saturated in all cases at the desired operating point. The small signal gain was

specified to ensure saturation of the output amplifiers; as long as the output is saturated, variance in small-signal gain with respect to temperature can be tolerated.

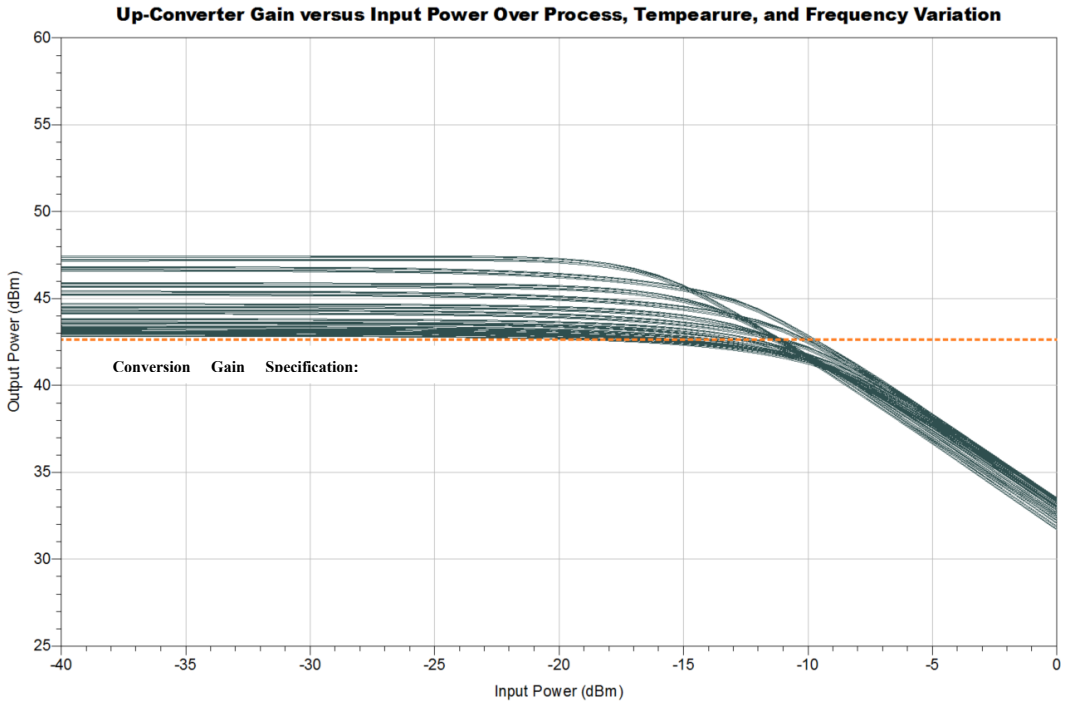


Figure 38: Effect of manufacturing, temperature, and operating frequency on conversion gain.

4.6.2.3 Verification of Output Spurious

The output spurious was simulated using a harmonic balance simulation with the input power to the up-converter fixed at +0.5 dB_m @ 3.00 GHz. The simulation was repeated over the same frequency, temperature and manufacturing variance as previous simulations. Figure 39 was generated at 9.7 GHz with maximum manufacturing variance over all three temperatures and shows the worst spur is -64.69 dB_c at a 600 MHz offset from the carrier, occurring at room temperature. No spur exceeded the maximum specification of -60 dB_c in any configuration.

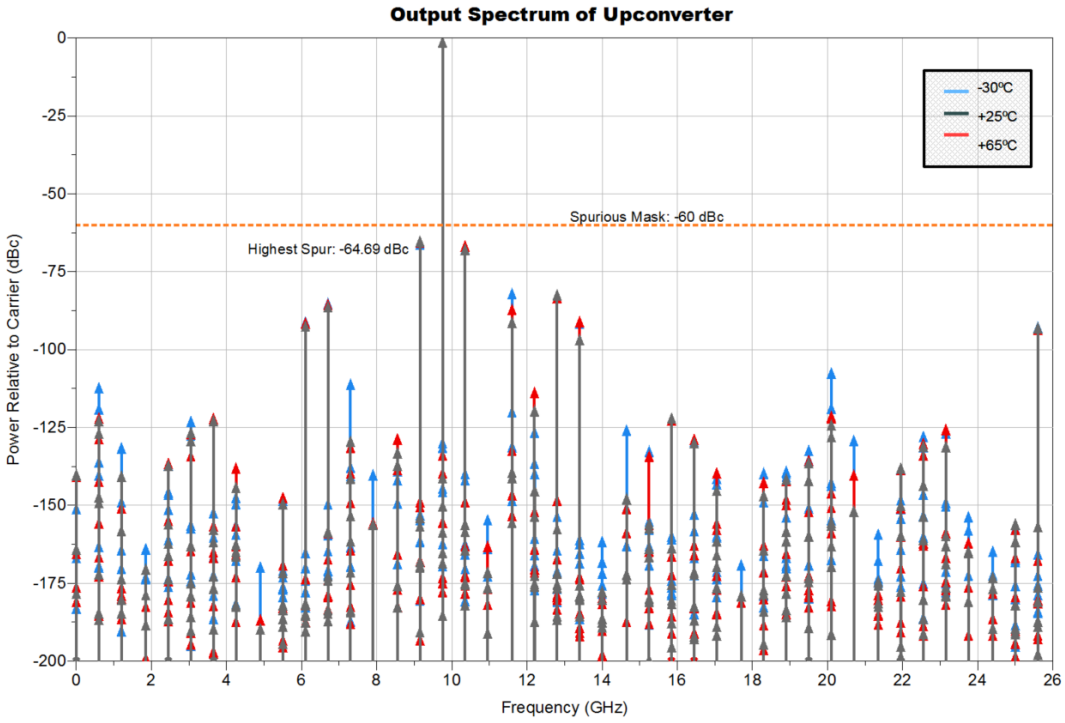


Figure 39: Normalized output spectrum of Up-Converter with nominal manufacturing values over temperature @9.70 GHz output frequency.

4.6.2.3 Verification of Return Loss

The return loss of both ports on the up-converter were assessed using an s-parameter simulation with small signal models present for all active devices. The simulation was run at the nominal operating temperature and manufacturing variation, as well as at hot with maximum manufacturing variation, and cold with minimum manufacturing variation. Over these corner cases, the input never exceeded -15.58 dB input return loss as shown in Figure 40. The output return loss never exceeded -20.48 dB over the entire operating band as shown in

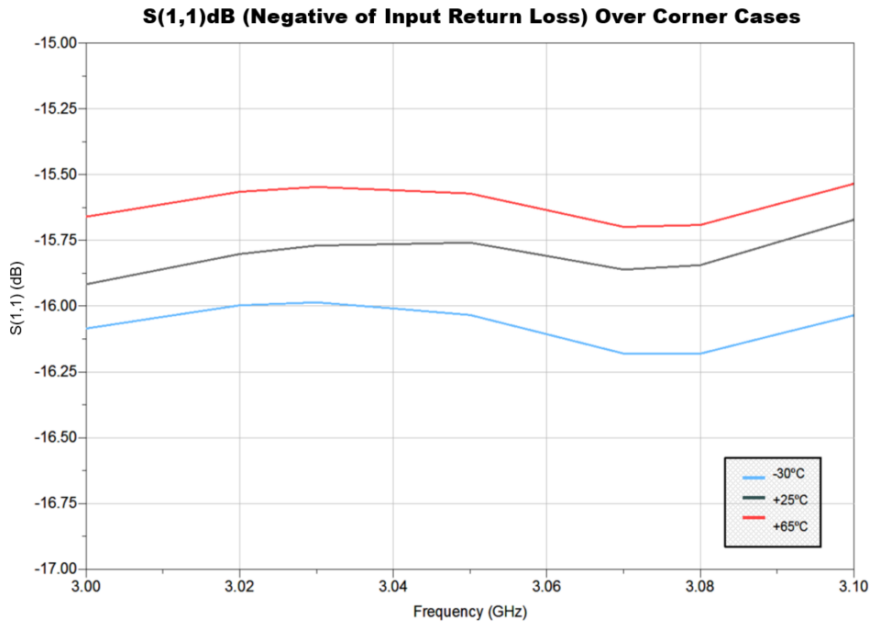


Figure 40: S(1,1) (inverse of input return loss) versus frequency of up-converter over temperature and manufacturing variation.

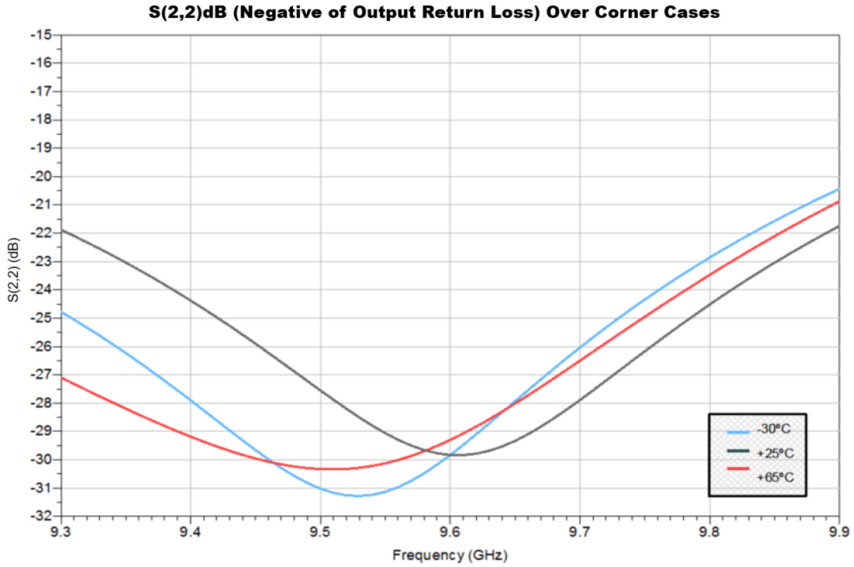


Figure 41: S(2,2) (Inverse of output return loss) versus frequency of up-converter over temperature and manufacturing variation.

4.6.3 Simulation of Down-Converter

The simulation of the down-converter was done in a similar fashion to the up-converter for the purpose of verifying the RF performance against the specification. An EM model of each module was generated from the CAD drawing, and all the EM modules were connected as shown below in Figure 42.

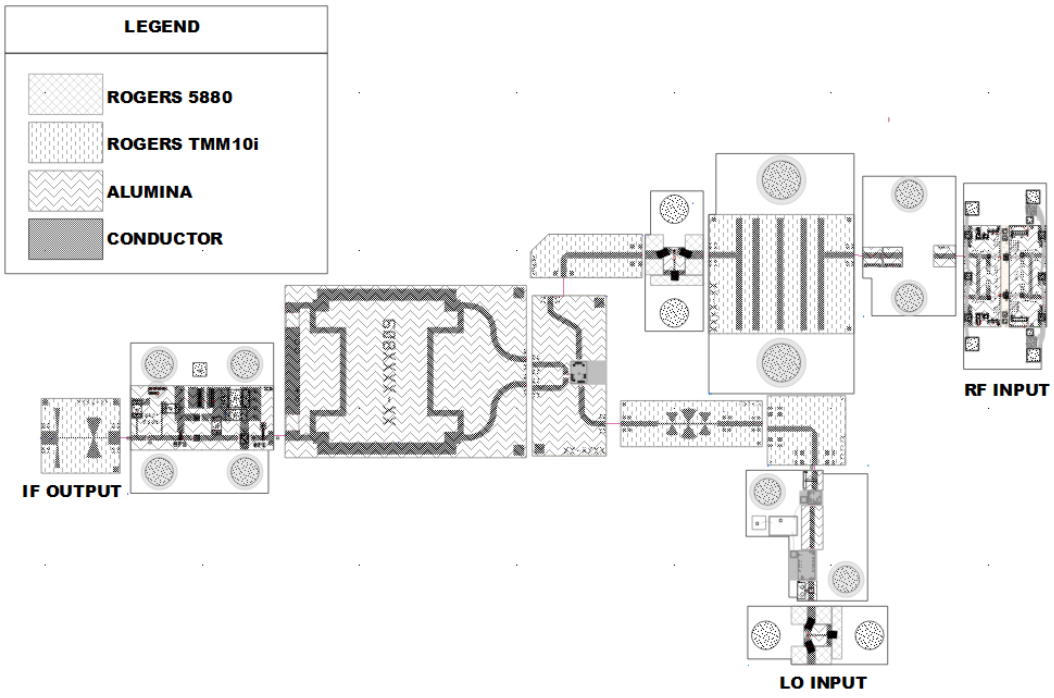


Figure 42: EM co-simulation of down-converter.

4.6.3.1 Verification of Output P_{1dB}

The output P_{1dB} of the up-converter was verified using a harmonic balance simulation on the EM model shown above. The RF Frequency was swept from 9.3 to 9.9 GHz, while updating the STALO frequency to ensure the IF frequency always landed between 3.0 and 3.1 GHz. The temperature was swept from -30 ºC

to +65 ºC in steps of ten degrees (with the last step being 5 degrees). All cases were simulated using minimum, nominal, and maximum manufacturing variance. The results of all cases were plotted in Figure 43. The worst case measured 1 dB compression point was +6.50 dBm. As such, the design will pass the specification at all operating conditions.

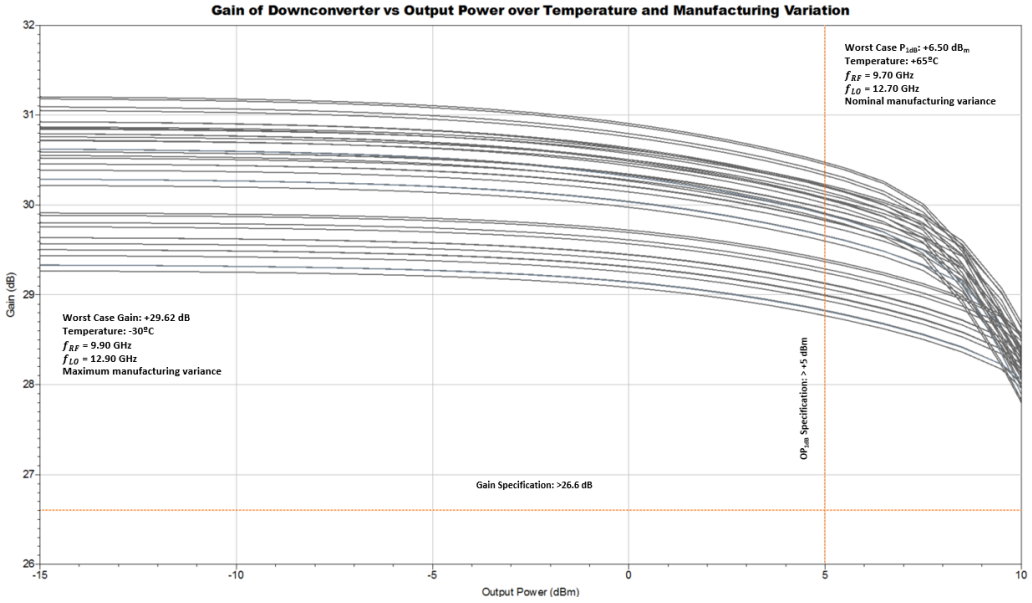


Figure 43: Results of harmonic balance simulation of down converter over all frequency, temperature, and manufacturing corners.

4.6.3.2 Verification of Gain

The small-signal gain was verified using the same simulation as the output 1 dB compression point. The small signal gain can be observed as the region of flat gain seen in Figure 43. The worst-case gain observed was 29.62 dB, which is compliant to specification. The observed gain was as high as 31.22 dB. The specification only

required the gain be higher than 26.6 dB, and so this was not address. If required, a coaxial attenuator can be included in the overall system to mitigate excess gain.

4.3.3.3 Verification of Output Spurious

The output spurious was measured using the same method to measure the conversion gain, except for a fixed input power level of -30 dBm. It was measured over all input RF and LO frequency combinations, as well as all temperature and manufacturing corners. The maximum observed spur was -55.71 dB_c at 12.7 GHz. This was measured at 9.7 GHz RF frequency, at the hot temperature with nominal manufacturing variance. This spur is due to STALO leakage in the mixer. It is within the specified -50 dBc, and so the design was considered sufficient to meet the spurious specification.

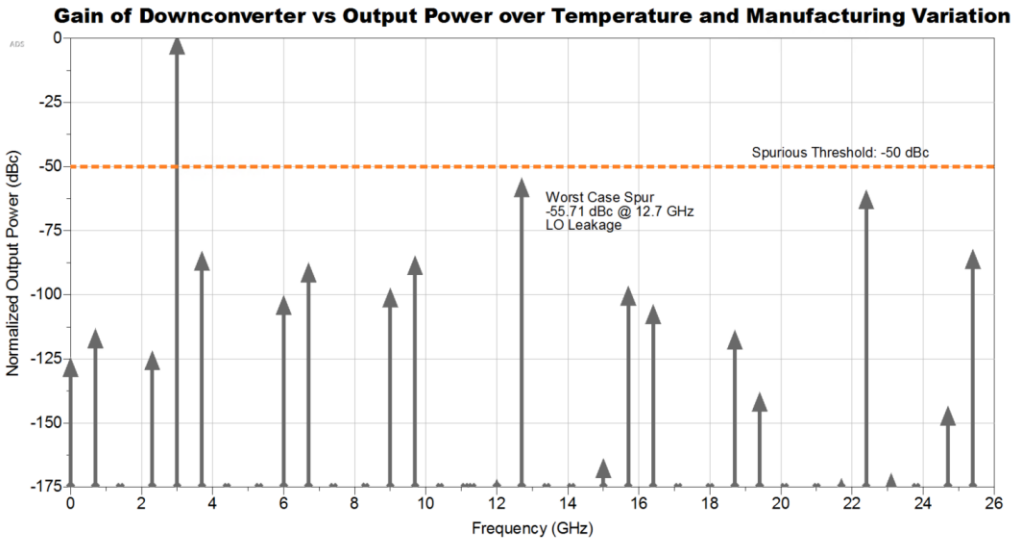


Figure 44: Worst case spurious measured at f_{RF} = 9.7 GHz, f_{LO} = 12.7 GHz, nominal manufacturing variance, and hot temperature.

4.6.3.4 Verification of Noise Figure

The noise figure for the system was measured over maximum temperature and manufacturing corners as has been done for previous simulations. The results are shown below in Figure 45. The worst case noise figure in the 9.3 to 9.9 GHz band is 2.69 dB which is compliant to the specification of less than 3 dB.

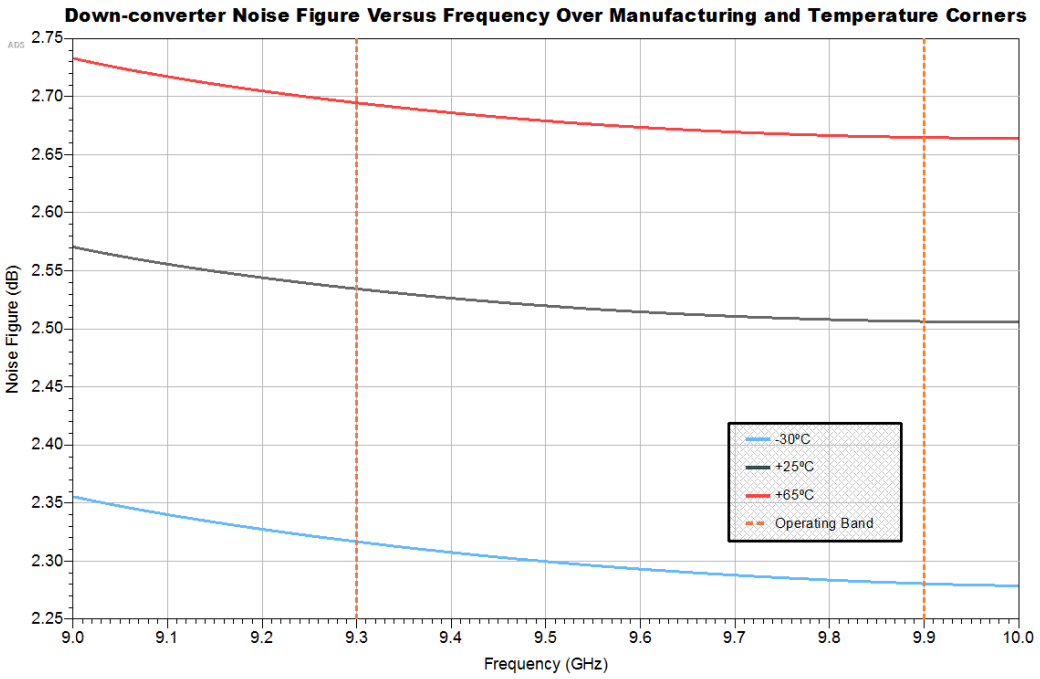


Figure 45: Downconverter noise figure versus frequency over manufacturing and temperature corners.

4.6.3.5 Verification of Return Loss

Verification of the return loss was done using a similar method as was presented in section 4.6.2.3 for verification of the up-converter. The input return loss marginally failed the specification on +65ºC temperature corner with maximum manufacturing variance with a value of -14.63 dB at 9.3 GHz. This was considered a tolerable

failure, as attempts to improve the input match would degrade the noise figure, and the noise figure is a more important parameter. The results are shown below in Figure 46.

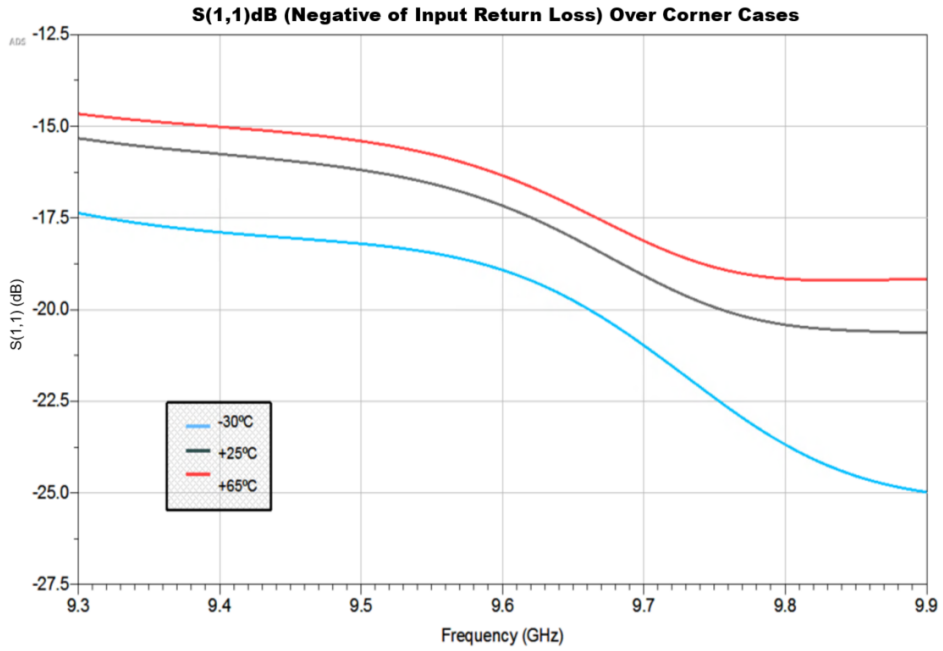


Figure 46: Up-converter S(1,1) (inverse of input return loss) over temperature and manufacturing variation.

Simulation results of the output return loss of the down converter are given below in Figure 47. The worst case return lost was observed was -15.64 dB.

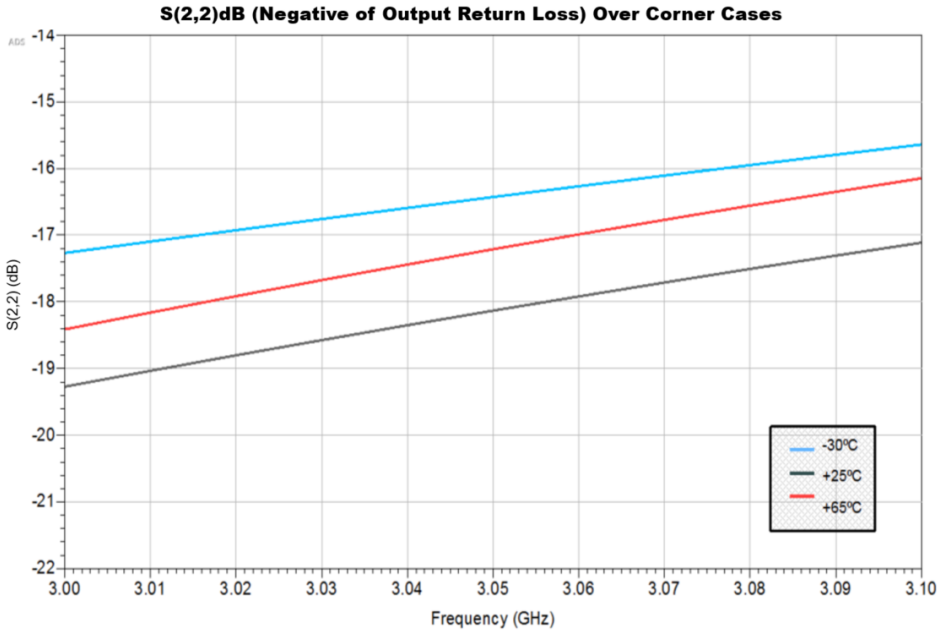


Figure 47: S(2,2) (inverse of output return loss) of down-converter simulated over temperature and manufacturing corners.

4.7 HMIC Layout and Mechanical Design

After verifying the design met the RF specifications and demonstrated improved reliability via the FIDES method of reliability analysis, the mechanical 2-D drawing of the housing was generated and is shown below in Figure 48. The mechanical layout was done with the following considerations:

- Each module and substrate sit in a pocket with a depth of 500 mil plus the height of the substrate and carriers. This allows for a consistent bond height between adjacent substrates, and a consistent lid height over the substrate of 500 mil.
- Inside corners have a minimum a minimum fillet of 63 mil, as the drill bit machining this housing is round.

- The design will have a sub-lid, which is screwed to the housing in multiple places to ensure a lid with good electrical contact to the housing. Sub-lid screw spacing must be at minimum $\frac{\lambda}{5}$ with a nominal value of $\frac{\lambda}{10}$ preferred to ensure consistent electrical potential between sub-lid and housing. A main lid in installed over the sub-lid and secured via laser welding to ensure hermeticity.
- DC power is fed through hermetic DC feedthrough pins supplied from underneath the housing. The STALO will also be supplied from underneath using hermetic RF feedthrough pins.
- RF inputs and outputs are fed through the side using hermetic RF feedthrough pins compatible with SMA connectors.
- A dedicated hermetic DC feedthrough must be present for grounding.
- Any space in the housing not used for RF shall have pockets installed to reduce unit mass as much as possible. All mass-reduction pockets must be separated from active RF pockets by at least one wavelength.

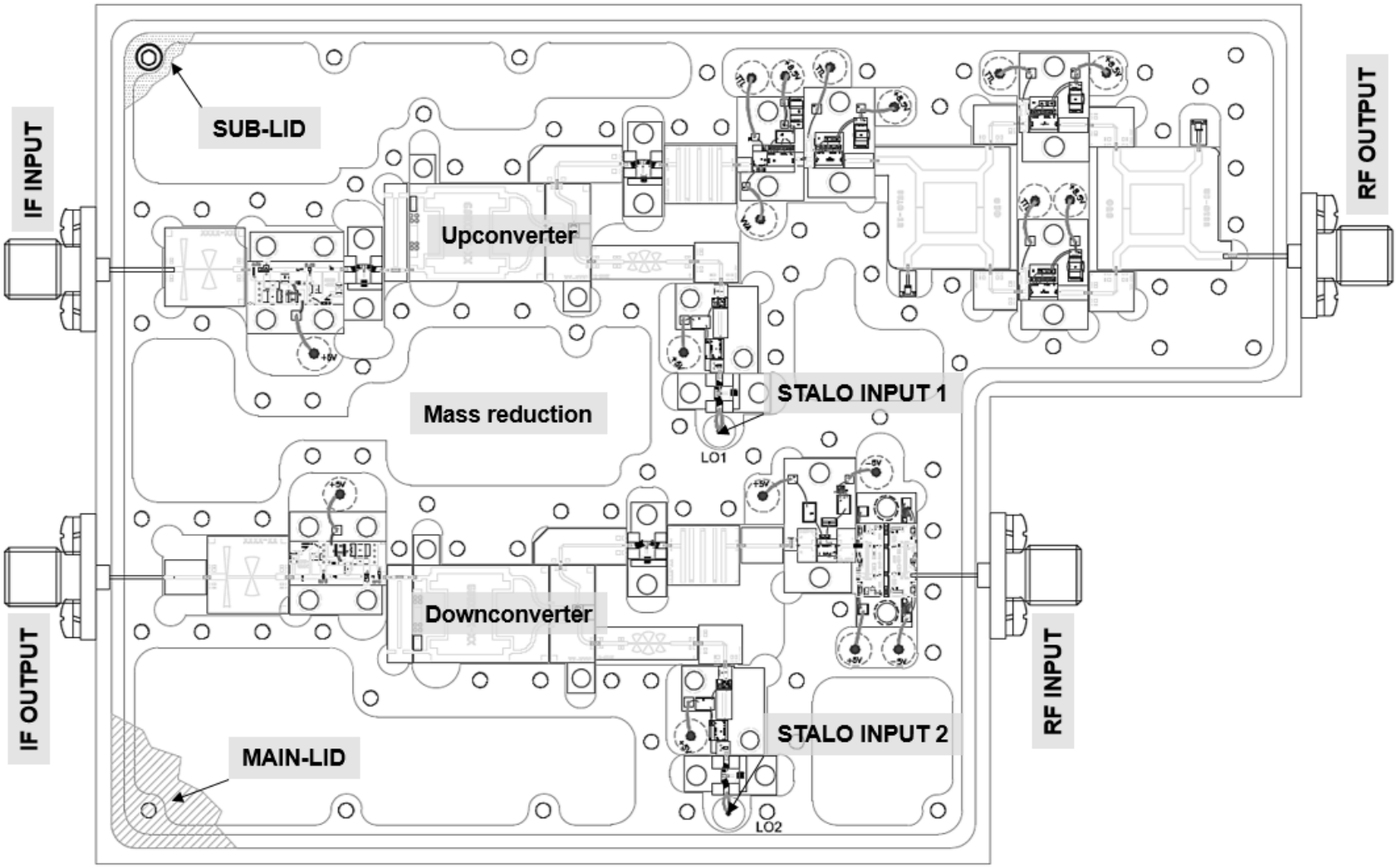


Figure 48: Mechanical layout of HMIC modules and housing

Figure 49: 3D Model of UDC HMIC Housing.

5.0 ENVIRONMENTAL TEST AND VERIFICATION

Due to the ongoing Covid-19 Pandemic, the manufacturer had to cease operation to maintain health and safety and no hardware was able to be returned. After the pandemic passes, the manufacturer will resume operation and the hardware will be assessed as discussed in this section. The device will be tested over temperature corners according to the acceptance test procedure outlined in section 5.1.

5.1 HMIC Acceptance Test Procedure

The following section outlines the required tests to accept the design as function and verified. It includes a list of the required test, equipment, environmental corners, and a final section with detailed instruction on each required test.

5.1.1 Test Procedure Matrix

A list of all required tests are presented below in Table 23: Test procedure matrix required for acceptance of unit verification. Each test included in the test matrix below are discussed in further detail in section 5.1.5 Detailed Test Description.

Table 23: Test procedure matrix required for acceptance of unit verification.

Subassembly Test	**Subassembly Specification**	**Procedure Overview**
5.1.5.1 Transmitter Gain Test	10 dB	Apply known input signal at IF and measure power at RF with power meter
5.1.5.2 Transmitter Spurious Test	< -50 dBc @ +0.5 dBm input power	Apply known input signal and measure harmonic content of output on spectrum analyzer
5.1.5.3 Receiver Gain Test	> 26.6 dB	Measure using power sweep on VNA.
5.1.5.4 Receiver OP1dB Test	> 5 dBm	Measure using power sweep on VNA.
5.1.5.5 Receiver Spurious Test	< -50 dBc	Apply known input signal and measure harmonic content of output on spectrum analyzer
5.1.5.6 Power Supply Consumption Test	< 1.5 A @ 6 VDC input	Record current from power supply during active transmit/receive at 10% transmit duty cycle.
To test the power consumption, the DUT will be connected as shown in the transmitter gain test (Figure 50: Test configuration for transmitter gain test. with one exception; the trigger signal will be connected to the trigger output of the digital baseband unit. The digital baseband will be configured to run a scan with a PRI of 500 µs and a pulse length of 39 µs. This corresponds to the longest pulse and highest duty cycle. While this scan is running, the average current drawn from the power supply will be recorded in all frequency combinations used in tests. It is important that it run at the maximum duty cycle, as the DC supply to the	> 15 dB	Measure with VNA, trigger held high.

high-powered amplifiers is modulated with the trigger signal. The highest duty cycle would represent the highest power consumption of the device. 5.1.5.7 TX-IN Return Loss Test		
5.1.5.8 RX-OUT Return Loss Test	> 15 dB	Measure with VNA, trigger held low.
5.1.5.9 TX-OUT Return Loss Test	> 13 dB	Measure with VNA, trigger held high.
5.1.5.10 RX-IN Return Loss Test	> 15 dB	Measure with VNA, trigger held low.
The RF RX-IN port return loss can be measured as describe above for other ports. The trigger will be held low, as the LNA will be turned on regardless of trigger state. 5.1.5.11 Receiver Noise Figure	< 4 dB	Measure using noise figure meter configured for frequency translation.

5.1.2 Environmental Conditions

The DUT is to be measured at all ambient and both temperature corners to ensure compliance against the design over the intended operational temperature range. The set of environmental criteria for the acceptance test are presented below in Table 24: Environmental conditions for DUT acceptance test.

Table 24: Environmental conditions for DUT acceptance test.

Temperature(ºC)	**Soak Time (before power applied)**	**Warm Up Time (Before starting test)**
-30 ºC ± 2ºC	> 10 minutes	> 10 minutes
+25 ºC ± 2ºC	> 10 minutes	> 10 minutes
+55 ºC ± 2ºC	> 10 minutes	> 10 minutes

5.1.3 Required Test Equipment

The required test equipment is listed below in Table 25: Test equipment matrix required for UDC acceptance test.

Table 25: Test equipment matrix required for UDC acceptance test.

Item	Equipment Name	Model	Manufacturer	Qty
1	Network Analyzer	ENA E5071C	Keysight	1
2	Spectrum Analyzer	MXA N9020B	Keysight	1
3	Series Noise Source	N4002A	Keysight	1
4	Power Supply	XEL 30-3p	Sorensen	3
5	Average Power Meter	N1913A	Keysight	1
6	Signal generator	E8752D	Keysight	1
7	20 dB Attenuator	PE7337-20	Pasternack	1
8	Digital Baseband Transceiver	650-8010-21	Nanowave Technologies	1

5.1.4 Required Calibration for Test Equipment

All equipment will be inspected to ensure a valid calibration sticker is present from the manufacture. This is to ensure the validity of measured data. The loss of all cables and interconnects must be measured on a VNA and recorded in order to de-embed test infrastructure from the required measurement.

5.1.5 Detailed Test Description

The following subsection details the specific procedure for each specification to be verified. A detailed test procedure is included in APPENDIX C: DETAILED TEST PROCEDURES.

As the UDC generates a STALO internally, the digital baseband unit will be required for all testing to supply the reference signal, and program the STALO to various frequencies during all tests.

Note that each test will be repeated over the three temperature corners as described in 5.1.2 Environmental Conditions.

5.1.5.1 Transmitter Gain Test

The standard way to measure transmitter gain would be to use a VNA configured for conversion gain. To run this test, the VNA requires the LO used for frequency conversation. However, the LO is internal to the frequency converter in this instance, and therefore unavailable to an external piece of test equipment. For this reason, and alternate method will be used. The transmitter gain test will be completed using the test configuration as shown below in Figure 50. A known IF signal will be input at the specified input power of -8.15 dB_m at 3.10 GHz. The STALO will be programmed to 12.4 GHz, and the output observed on both a spectrum analyzer and average power meter. A compliant output will be at 9.3 GHz, with a power greater than 31.5 dB_m. The following considerations will need to be taken during this test:

- All RF cables should be measured and de-embedded from the measurement. The injected test signal should be increased in power to account for the cable loss so that -8.15 dBm is present at the IF input port.
- The transmitter chain in the UDC is triggers by a 5V TTL active high signal. A DC bench supply can be used to hold this high during testing. The design

is thermally compliant for continuous operation, and only modulated to meet the power supply specifications.

- The measurement should be repeated for STALO frequencies from 9.3 – 9.9 GHz in steps of 100 MHz, at IF frequencies of 3.00 – 3.10 GHz in steps of 50 MHz.
- All unused RF ports should be terminated in a 50-ohm load.

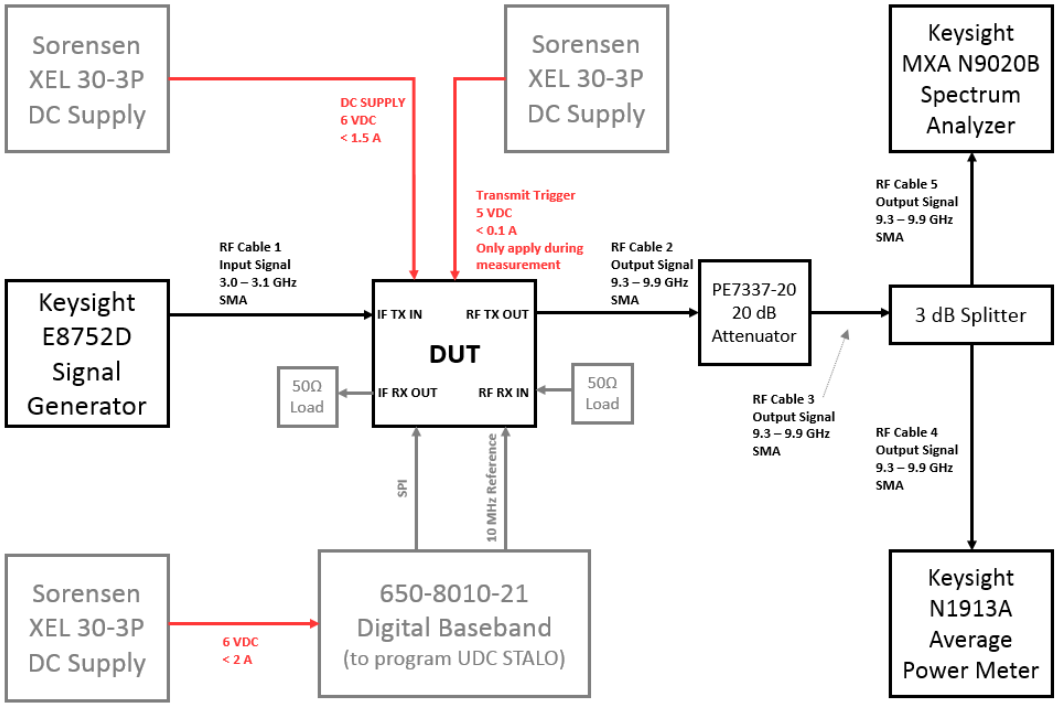


Figure 50: Test configuration for transmitter gain test.

In future revisions, it would be good to provision for a STALO output to SMA to allow for the STALO signal to be available to external test equipment. This would allow for the use of a VNA to check over the whole operating IF band for each STALO setting and reduce the number of measurements for this test by a factor of 3.

5.1.5.2 Transmitter Spurious Test

To measure the spurious of the transmitter, a similar test set up will be used as shown in Figure 62. The main differences are that the power of the input signal is increased to +0.5 dB_m and the power meter is removed from the test configuration. As the input signal is an LFM chirp, there is only considered to be one frequency instantaneously, thus a two-tone test was not considered appropriate for the spurious measurement. The spectrum analyzer must be configured with VBW/RBW (video bandwidth/resolution bandwidth) in order to achieve the peak resolution and DANL (dynamic average noise floor) required to resolve spurs at lease to -60 dBc. A noise floor of less than -70 dBc is preferable to ensure the spurs are well above the noise floor. The regulatory body which has produced the spurious mask has provided specific conditions for spurious measurements which include:

- VBW/RBW set to 1 kHz
- Trace set to maximum hold for a 5-minute sweep (to show the worst-case power level of any spur).
- Detector mode set to peak as opposed to average (again to show the worst-case spur).
- Measurement span set to ±100 MHz minimum. The minimum required span is used to reduce measurement time.

This measurement should be taken over all the IF and STALO frequency combinations as were used in the previous test.

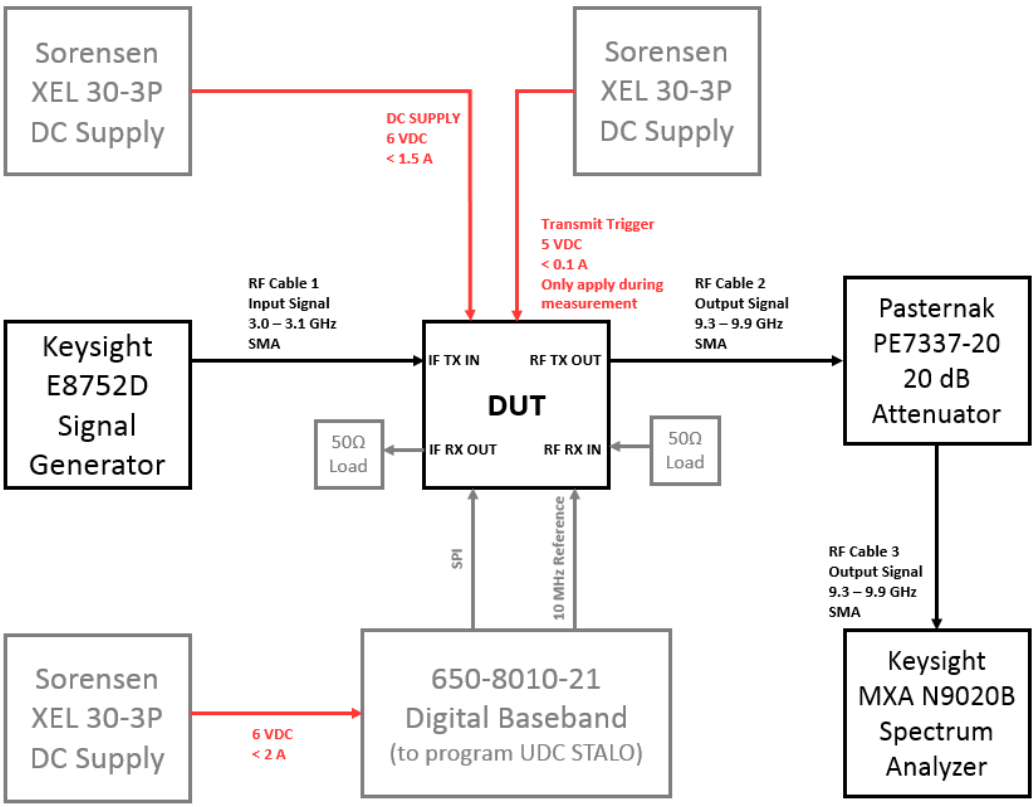


Figure 51: Test configuration for transmitter spurious test.

5.1.5.3 Receiver Gain Test

Given the similarity in measurement, the receiver gain will closely follow the methodology proposed for in section 5.1.5.1 Transmitter Gain Test, using the configuration shown below in Figure 52: Test configuration for receiver gain test. The following differences can be observed:

- Input will now be to the RF receiver input port, at a power level of -30 dB_m and a frequency of $f_{STALO} - 3.00\ GHz$, $f_{STALO} - 3.05\ GHz$, and $f_{STALO} - 3.10\ GHz$ for every STALO frequency used.
- The output power for each frequency combination should be higher than -3.4 dB_m to achieve compliance.

- Trigger signal will be held at GND (0 VDC) to ensure the receiver is turned on. A 50-ohm real load can be used as a pull down on the SMA port.

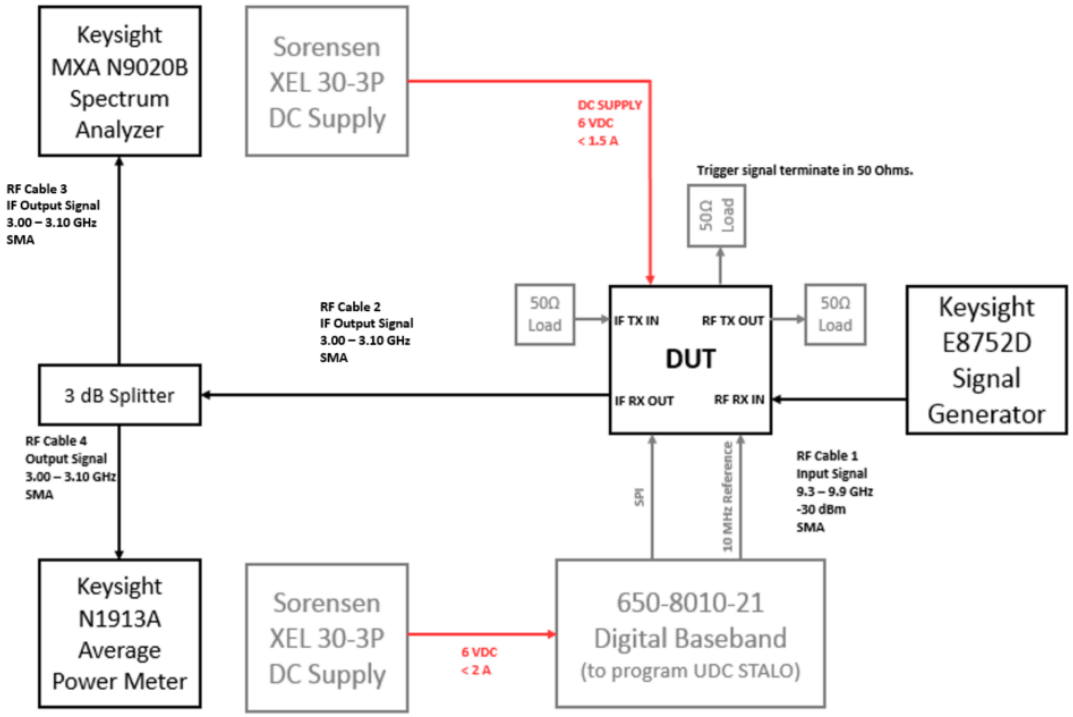


Figure 52: Test configuration for receiver gain test.

It is worth noting that an external output port for the STALO would also be useful to reducing the number of measurements required in this test, as then a VNA could be used in a frequency conversion measurement configuration.

5.1.5.4 Receiver OP1dB Test

The output referenced 1 dB compression point will be measured using the same test set up shown in Figure 52. The key difference in this test is that the input power will be lowered to -35 dB_m and increased in 1 dB steps to -15 dB_m. The output power will then be plotted against the input power, and the 1 dB compression point observed as the data point where the curve has deviated from the linear relationship

by 1 dB. This will have to be repeated for all frequency combinations included in the previous test.

Given the number of individual data points required for this test, it could be vastly improved by using a VNA configured for frequency conversion, as the Keysight ENA series VNAs are capable of P1dB measurements. Having an external STALO port on the UDC would allow a reduction in 20 measurement steps per frequency to be measured.

5.1.5.5 Receiver Spurious Test

The receiver spurious test is done using the test configuration shown in Figure 52. The RF input power will be set to -30 dBm. The spectrum analyzer will be set for the same settings as described for in section 5.1.5.2 Transmitter Spurious Test. The key change will be the center frequency of the measurement, which will target either 3.00, 3.05, or 3.10 GHz depending on the RF and LO frequencies at each stage of the test. The same range of LO and RF frequencies will be used as in previous receiver tests.

5.1.5.6 Power Supply Consumption Test

To test the power consumption, the DUT will be connected as shown in the transmitter gain test (Figure 50: Test configuration for transmitter gain test. with one exception; the trigger signal will be connected to the trigger output of the digital baseband unit. The digital baseband will be configured to run a scan with a PRI of 500 µs and a pulse length of 39 µs. This corresponds to the longest pulse and highest duty cycle. While this scan is running, the average current drawn from the power

supply will be recorded in all frequency combinations used in tests. It is important that it run at the maximum duty cycle, as the DC supply to the high-powered amplifiers is modulated with the trigger signal. The highest duty cycle would represent the highest power consumption of the device.

5.1.5.7 TX-IN Return Loss Test

The IF TX-IN return loss will be tested using a Keysight ENA series VNA (vector network analyzer). The analyzer can have each of its 2 ports connected to the two IF ports. Prior to use, the VNA must undergo a SOLT calibration to ensure measurement accuracy. The trigger signal can be held low for this measurement, as the IF amplifiers in both the transmitter and receiver will still be on regardless of the trigger level. The return loss can be measured by measuring S(1,1) (dB), and negating the value. The measurement configuration is shown below in Figure 64: Test configuration for IF return loss measurements.

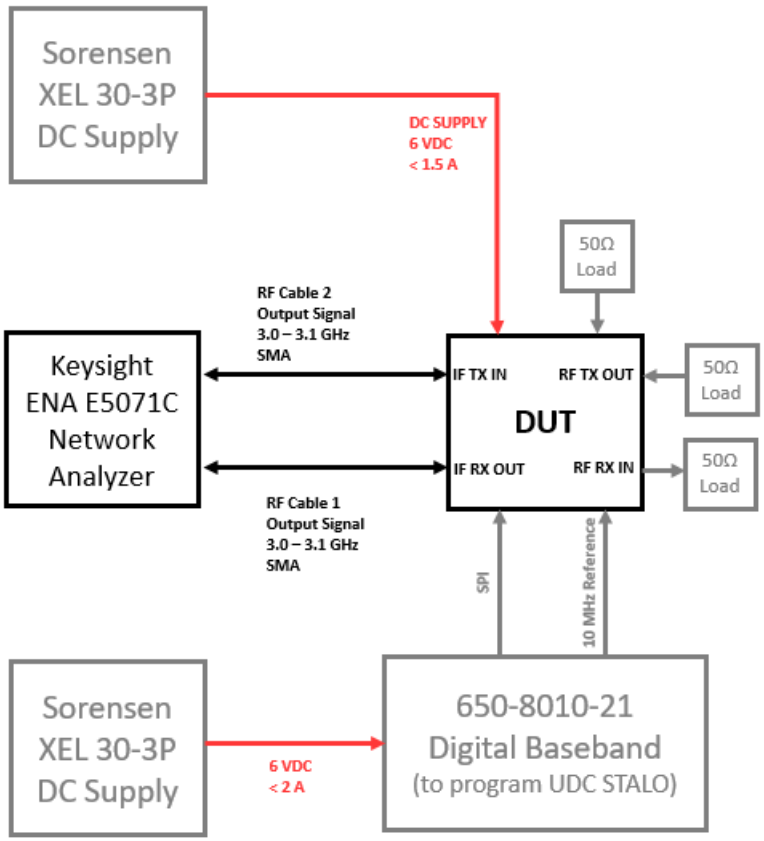


Figure 53: Test configuration for IF return loss measurements.

5.1.5.8 RX-OUT Return Loss Test

The IF RX-OUT return loss will be measured in the same fashion, but taking the measurement from the other VNA port (i.e. S(2,2) (dB)).

5.1.5.9 TX-OUT Return Loss Test

The RF TX-OUT port return loss can be measured in the same fashion as the IF port return loss, with one exception. The transmit trigger should be held high during the measurement to ensure the output amplifier is in steady state, as S-parameters are bias dependent. It is also imperative that the input be terminated in a 50-ohm

load so that no signal is applied to the transmitter chain. It should be noted the output power of the transmitter is sufficient to cause damage to the VNA. The measurement configuration is shown below in Figure 54.

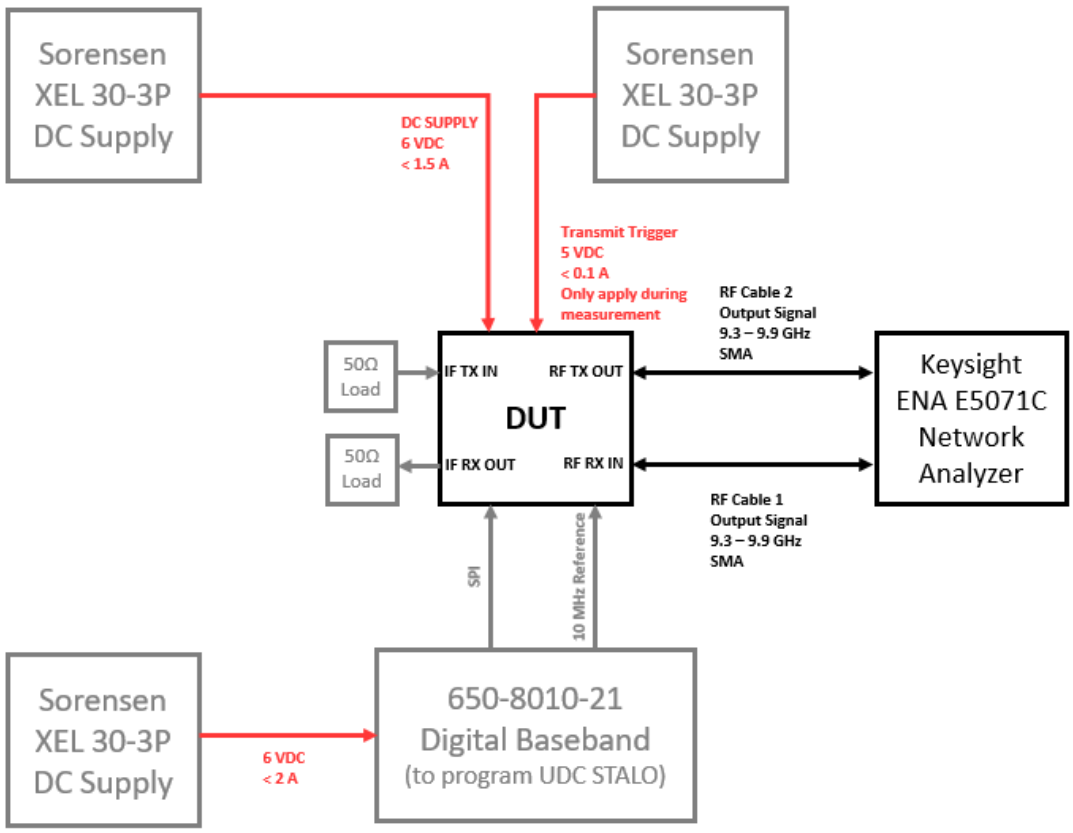


Figure 54: Configuration for return loss measurement of RF ports on UDC.

5.1.5.10 RX-IN Return Loss Test

The RF RX-IN port return loss can be measured as describe above for other ports. The trigger will be held low, as the LNA will be turned on regardless of trigger state.

5.1.5.11 Receiver Noise Figure Test

The receiver noise figure uses the Keysight MXA series spectrum analyzer with a wideband noise source (Keysight N4002A). The Keysight N4002A noise source is a broad band source from 10 MHz to 26.5 GHz. As this device is measuring the noise of a frequency converter, a proper set up and calibration is required. The MXA series spectrum analyzer allows for configuration of noise figure measurements with frequency conversion. Once configured as a frequency conversion measurement in noise figure mode, the measurement set up must be calibrated by connecting the noise source directly to the input of the spectrum analyzer. The calibration will then measure the noise in the RF band corresponding to the IF sweep range (which will be displayed on the screen) and use the calibrated values for the input noise to the system. The DUT will then be connected between the noise source and meter as shown below in Figure 55. Before taking the measurement, the losses of all cables should be added into the cable loss calibration table. The spectrum analyzer will then de-embed cable losses from the measurement. After this, the measurement can be taken across the entire IF range. The measurement will measure the noise floor at the output, as well as the gain of the DUT in order to determine the additive noise from the DUT. The display shows the noise figure and gain of the DUT across the IF band.

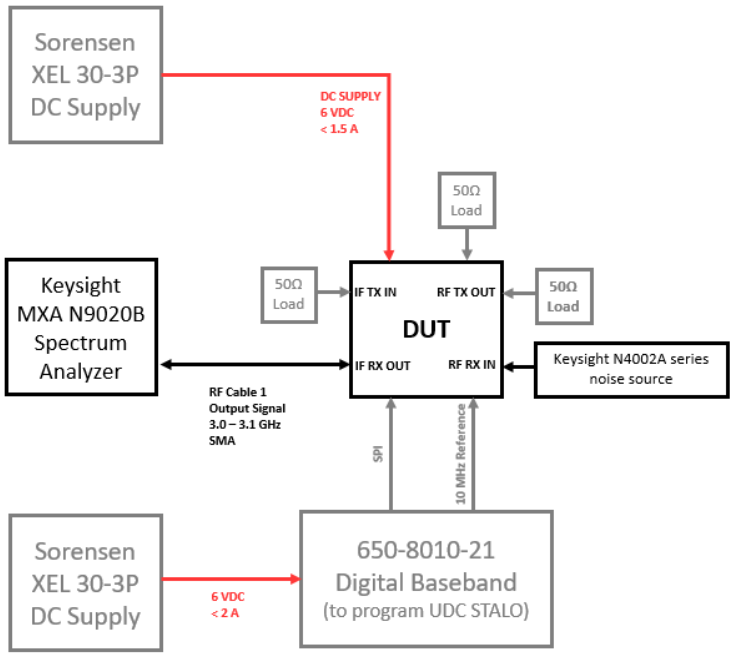


Figure 55: Test configuration for receiver noise figure measurement.

5.1.5.12 Highly Accelerated Thermal Stress Test

The end user has specified a highly accelerated thermal test for acceptance of all qualification units. It is worth noting that this acceptance test is where failure of the PCB implementation of the UDC produced a failure, raising concerns for the overall environmental durability of the design. The test is to exceed the specified system operating temperature by 5 degrees on either extreme, swinging the full operating temperature range on a diurnal cycle for 14 days consistently. The planned daily thermal cycle is shown below in Figure 56. During the testing, the humidity shall be set to the maximum relative value (at dew point). It can be observed that there will be a 105ºC variation in temperature over a three-hour period. This variation is far more extreme that will be realized in any deployment.

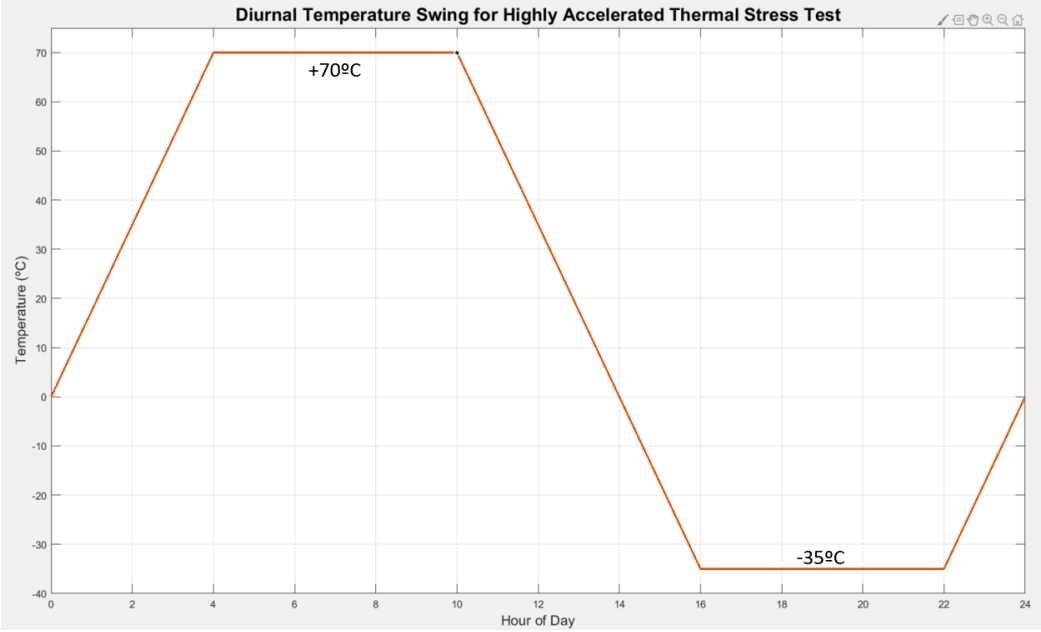


Figure 56: Diurnal temperature variation for accelerated thermal stress testing.

During the testing, the UDC will be placed in an environmental chamber to allow control of the subassembly. The device will be configured in RF loop back as shown below in Figure 57. The UDC will be connected to the digital baseband subassembly and configured to run an active scan at a pulse duration of 39 µs, with a repetition interval of 500 µs representing the maximum duty cycle of 7.8%. The output of the UDC will be monitored in software on the digital baseband unit to detect any changes in gain or distortion of the waveform. The test will be considered a success if no significant variation in output power or distortion is observed at the end of the 14-day period.

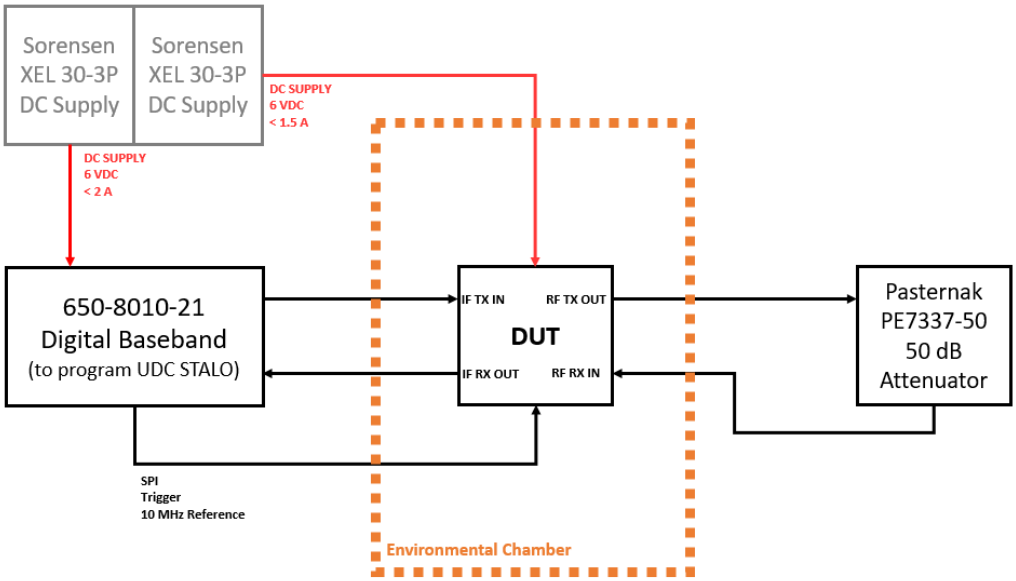


Figure 57: Test configuration for highly accelerated thermal stress test.

5.2 HMIC Acceptance Test Results

Due to manufacturing delays caused by the Covid-19 outbreak, the prototype could not be completed in time to support the conclusion that the HMIC unit will have improved environmental durability and increased reliability as shown through analysis. This research will be continued in the coming months in order to further support the development of environmentally hardened subassemblies for severe weather tracking.

5.3 PCB Acceptance Test Results

The PCB implementation of the UDC has 5 copies go through the acceptance tests 5.1.5.1 through 5.1.5.11. One copy of the PCB underwent a modified version of 5.1.5.12 to be discussed in section 5.3.1. The RF performance of the PCB was generally compliant to the specifications, with the following exceptions:

- As the PCB implementation was not able to withstand having the TX trigger held high (leaving the transmit amplifiers in the on-state) due to thermal reasons, the TX output port return loss was measured cold and measured non-compliant. This non-compliance was waived as stated above.
- The transmitter small signal conversion gain was measured at 39.71 dB, which would be non-compliant to the current specifications. However, during the small signal gain specification for the transmitter was compliant at the time, as this specification was later revised due to changes in the transmit waveform design
- The output referenced 1 dB compression point of the receiver was non-compliant at +0.5 dB_m. This non-compliance was accepted in the prototype, with the understanding that a revision would be made before production.

The conclusion can be drawn from these results that both technologies are capable in terms of RF performance. Either technology can implement similar RF circuits. The only critical failing of the PCB implementation can be observed during environmental testing, in which a fault was detected.

5.3.1 Nature of Fault during PCB Environmental Testing

The PCB underwent a highly accelerated thermal test similar to that described in section 5.1.5.12. The key difference is that the PCB UDC was integrated into a full radar system. The system completed 15 thermal cycles over a 23 day period, with some interruptions due to issues with the thermal chamber. The system was left in the chamber during this time, and operating continuously in an active scan. The

thermal chamber was configured to maintain the maximum possible humidity over the full test. The measured internal radome temperature is shown below in Figure 56. The device was subject to a maximum operating temperature 57.5ºC, and a minimum of -32.5ºC.

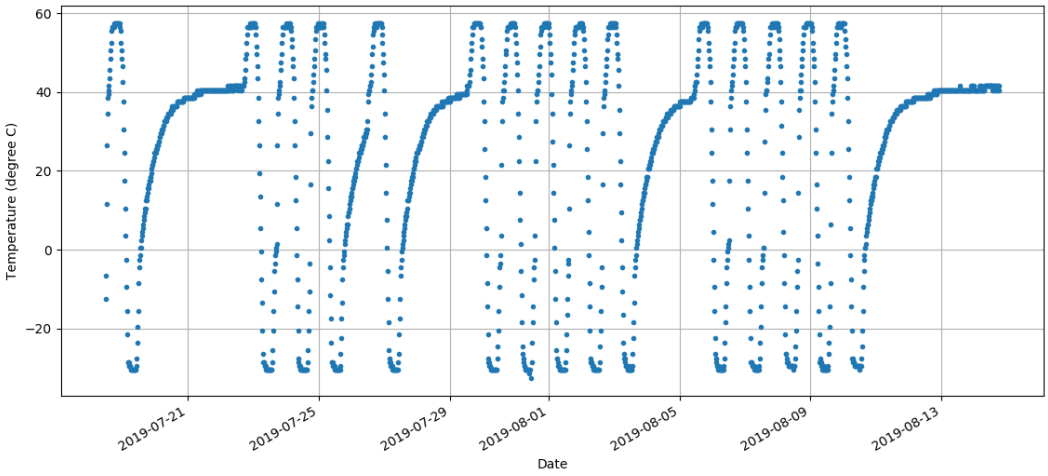


Figure 58: Internal radome temperature over radar system environmental testing. [40]

After completing the thermal cycles, the system was subject to an overall acceptance test. It was observed at this time that a fault had occurred in the receiver, preventing the detection of any received signals.

The UDC PCB was determined to be at fault. Corrosion was observed on several of the RF traces and on the pins of several SMD packages. This was not determined to be the cause of the fault, but is worth noting as the duration of the test is significantly less than the expected duration of the mission profile, and the thermal chamber did not expose the PCB to saline pollutants.

The determination of fault was due to a failed solder joint on one of the SMD packages. The fault is expected to have occurred during thermal expansion and contraction.

This is the principle reason that an HMIC technology was considered. The HMIC has all active devices held in place mechanically with screws. Each device, substrate, and carrier has careful matching of thermal expansion coefficients to reduce thermal stress. The electrical interface is a bond-wire and decoupled from the mechanical interface. Based on these results, an RF PCB is less suitable than an HMIC implementation of the UDC.

6.0 CONCLUSIONS AND FUTURE WORK

The thesis demonstrated through analysis that an HMIC implementation will have a higher MTBF as predicted using the FIDES reliability analysis method. These improvements are due to increased hermeticity, and increased control over thermal conduction from chip junction to system ambient temperature. Due to the covid-19 pandemic, delays in the manufacturing process have prevented a timely production of the prototype. Given the important nature of this work, the design will still be produced as soon as manufacturing bandwidth becomes available. This section discusses the further work to be undertaken once the prototype is available for test, and future work to further improve reliability of the design.

6.1 Verification and Comparison against PCB Implementation

A comparison of performance between the HMIC and PCB implementation of the UDC is available below in

Table 26. The data for the PCB was taken as the worst-case measurement from Nanowave Technologies test data sheets for serial numbers 1 through 5. The values for the HMIC were taken as the worst-case value presented through analysis or simulation over all manufacturing, temperature, and process corners. It can be observed that implementation in either technology did not present an improvement in RF related system parameters. The main noticeable difference between the two technologies is an increase in meantime before failure of 2.7 times. This increased reliability can be attributed to lower junction temperatures due to more flexible thermal design, as well as the hermeticity of the HMIC implementation. As soon as

hardware is available, the environmental durability of the HMIC will be compared against the PCB implementation in order to assess if HMIC technology is better able to withstand the environmental extremes presented in the highly accelerated thermal stress testing required for this application. It should be noted that an HMIC SSPA module was included in the system level testing and has survived the extremes of thermal testing, and so the UDC HMIC is expected to survive.

Table 26: Comparing performance of HMIC and PCB implementations of the UDC.

Description	**Specification**	**HMIC**	**PCB**	**Comment**
Operating Frequency (GHz)	RF Port: 9.3 – 9.5 GHz, 9.7 – 9.9 GHz	Used to determine simulation/measurement range at RF port.		-
	IF Port: 3.0 – 3.1 GHz	Used to determine simulation/measurement range at IF port.		-
MTBF (hours)	>149,796 hours	4,304,307.19 hours	1,593,498.52 hours	HMIC improved reliability by a factor of 2.7.
Environmental Test Results	Survivability	Pending manufacturing.	Device failed in testing.	PCB failed during testing. HMIC to be tested pending manufacturing.
Power Consumption	< 1.5A @ 6 VDC	1.38 A @ 6 VDC	1.05 A @ 6 VDC	HMIC power consumption based on DC budget presented in APPENDIX D: DC BUDGET
UPCONVERTER				
Small signal gain (dB)	> 42.65 dB	42.89 dB	39.71 dB	Specification for TX small signal gain was revised between phase II and phase III of radar program.
Output P_{SAT} (dB_m)	>31.5 dB_m	+31.72 dB_m	+34.11 dB_m	
Output Spurious	< -50 dB_c	-64.69 dB_c	-53.22 dB_c	

(dB_c) (@fc ± 5 MHz)				
Output Spurious (dB_c) otherwise	< -60 dB_c	-64.69 dB_c	-64.64 dB_c	
IF Return Loss (dB)	>13 dB	15.58 dB	15.07 dB	
RF Return Loss (dB)	>15 dB	20.48 dB	-3.37 dB	PCB implementation would not tolerate holding the trigger active long enough for a steady-state measurement of output return loss.
DOWNCONVERTER				
Small signal gain (dB)	>26.6 dB	29.62 dB	27.02 dB	
Noise Figure	< 3 dB	2.69 dB	2.61 dB	
O_{P1dB} (dB_m)	> +5 dB_m	+6.50 dB_m	+0.05 dB_m	PCB was non-compliant.
Output Spurious (dB_c)	< -50 dB_c	-55.71 dB_c	-66.53 dB_c	
RF Return Loss (dB)	>15 dB	14.63 dB	12.7 dB	Non-compliance accepted as matching favours noise performance of VSWR reduction.
IF Return Loss (dB)	>13 dB	15.64 dB	22.9 dB	

6.2 Qualification in Overall System

Once the verification of the design is complete, the HMIC implementation will be integrated into the overall system for qualification. The overall system will undergo verification for acceptance of the new subassembly. Pending a successful acceptance test, the qualification will be commissioned on site in the Asian market, and the design will be accepted for production.

6.3 Integration of STALO Components into HMIC Synthesizer for Improved Reliability

The current implementation of the UDC presented in this work has only moved RF components directly in the signal path into an HMIC implementation but has not addressed the STALO. The COTS IC PLL and VCO used in the PCB implementation were also used in the HMIC implementation for ease of integration as no software revision would be required. Nanowave Technologies has several advanced low-phase noise STALO technologies which could be migrated to HMIC, allowing for further improved reliability and improved jitter performance. By leveraging in-house technology, the manufacturing costs could be lowered while improving unit reliability. Such work would leave only DC regulators on an external PCB, which can be conformally coated providing pseudo-hermeticity and high reliability.

6.4 Integration of DC Regulators into HMIC for Improved Reliability

It can be observed that 52% of the failures predicted by the FIDES analysis came from the linear regulators which are left on the PCB. By moving these regulators inside the HMIC in a die version, the thermal conduction from the die to ambient temperature could be improved, thereby improving the reliability of these parts. The devices would also benefit from the hermetic environment of the HMIC.

6.5 Include STALO Output for Test

While there is no interface requirement for a STALO output in the system, it has become apparent that inclusion of the STALO output would improve test and be useful when moving the design into mass production to allow for faster verification of key parameters. If a STALO output were available a VNA could be used to measure the conversion gain across the entire IF band in one measurement, reducing the number of measurements required for these tests by a factor of 3. The VNA could also measure the 1dB compression point of the receiver by doing a power sweep, reducing the number of measurements in that test by a factor of 20. While this work would not support the academic research, it would provide convenience for the industrial partner supporting this research.

References

[1] J. Cook, "Consensus on consensus, a synthesis of consensus estimates on human-caused global warming," *Environmental Research Letters,* vol. 11, no. 4, 2016.

[2] J. Cook, "Quantifying the consensus on anthropogenic global warming in the scientific literature," *Environmental Research Letters,* vol. 8, no. 2, 2013.

[3] W. R. L. Anderegg, "Expert Credibility in Climate Change," *Proceedings of the National Academy of Sciences,* vol. 107, no. 27, 2010.

[4] P. T. D. &. M. K. Zimmerman, "Examining the Scientific Consensus on Climate Change," *Eos Transactions American Geophysical Union,* vol. 90, no. 3, 2009.

[5] N. Oreskes, "Beyond the Ivory Tower: The Scientific Consensus on Climate Change," *Science,* vol. 306, no. 5702, p. 1686, 2004.

[6] AAAS (American Association for the Advancement of Science), "AAAS Reaffirms Statements on Climate Change and Integrity," 4 December 2009. [Online]. Available: https://www.aaas.org/news/aaas-reaffirms-statements-climate-change-and-integrity. [Accessed 27 October 2019].

[7] Edenhofer, O., R. Pichs-Madruga, Y. Sokona, E. Farahani, S. Kadner, K. Seyboth, A. Adler, I. Baum, S. Brunner, P. Eickemeier, and B. Kriemann "IPCC, 2014: Summary for Policymakers. In: Climate Change 2014: Mitigation of Climate Change. Contribution of Working Group III to the Fifth Assessment Report of the Intergovernmental Panel on Climate Change," Cambridge University Press, Cambridge, United Kingdom, and New York, USA., 2014.

[8] Donald J. Wuebbles and Kenneth Kunkel, "Severe Weather in United States Under a Changing Climate," *EOS Transactions, American Geophysical Union,* vol. 95, no. 18, pp. 149-156, 2014.

[9] H. Brooks, "Severe Thunderstorms and Climate Change," *Atmospheric Research,* vol. 123, no. 1, pp. 129-138, 2013.

[10] Karoly, Patrick T. Marsh, Harold E. Brooks, and David J., "Assessment of the severe weather environment in North America simulated by a global climate model," *Atmospheric Science Letters,* vol. 8, pp. 100-106, 2007.

[11] Military Specifications and Standards (Author), *MIL-STD-202F: Test Method Standards for Electrical and Electronic Component Parts,* Military Specifications and Standards (Publisher), 1998.

[12] K. Pitre, "E671 Phase II Thermal Analysis," Nanowave Technologies Inc, Ottawa, Ontario, 2019.

[13] J. Marin and R. Pollard, "Experience report on the FIDES reliability prediction method," in *Annual Symposium on Reliability and Maintainability*, Alexandria, VA, USA, USA, Jan. 2005.

[14] M. I. Skolnik, Introduction to Radar Systems, Pennsylvania, USA: McGraw-Hill, 1962.

[15] D. W. Hahn, "Light Scattering Theory," Department of Mechanical and Aerospace Engineering, University of Florida, Gainesvilla, Florida, 2009.

[16] J. S. Marshall and W. M. Palmer, "The distribution of raindrops with size.," *Journal of Meteorology,* vol. 5, no. 4, pp. 165-166, 1948.

[17] R. J. Doviak and D. S. Zrnic, Doppler Radar and Weather Observations: Second Edition, Dover: Dover Books on Engineering, 2006.

[18] J. W. Rogers, C. Plett and I. Marsland, Radio Frequency System Architecutre and Design, Artech House, 2013.

[19] H. Friis, "Noise Figures of Radio receivers," *Proceedings of the IRE,* pp. 419-422, 1944.

[20] FIDES Group, Reliability Methodology for Electronic Systems, FIDES Guide Ed. A, France: FIDES Group, September 2010.

[21] Nanowave Technologies Inc, "Automated Hybrid Assembly," Nanowave Technologies, 2019. [Online]. Available: https://www.nanowavetech.com/capabilities/HMICAutomatedAssemblies.php. [Accessed 12 December 2019].

[22] Nanowave Technologies Inc, "Hermetic Sealing: Truly Hermetic for High Reliability," Nanowave Technologies Inc., 2019. [Online]. Available: https://www.nanowavetech.com/capabilities/HemanticSealing.php. [Accessed 12 December 2019].

[23] US Deparment of Defense, *Test Method Standard Microcircuits, MIL-STD-883L,* Columbus, OH, 2019.

[24] Institut pour la Maîtrise des Risques, "A methodology for components reliability," FIDES, [Online]. Available: https://www.fides-reliability.org/en/node/555. [Accessed 08 01 2020].

[25] Nanowave Technologies Inc, "E671 Compact X-Band Weather Radar Specification," Ottawa, Ontario, 2018.

[26] USGS, "Rainfall calculator, metric units.," US Geological Survey, [Online]. Available: https://water.usgs.gov/edu/activity-howmuchrain-metric.html. [Accessed 15 02 2020].

[27] A. Poulariskas., The Handbook of Formulas and Tables for Signal Processing., CRC Press LLC, 1999.

[28] MathWorks, "RF Budget Anayler," 2019. [Online]. Available: https://www.mathworks.com/help/rf/ug/rfbudgetanalyzer-app.html. [Accessed 1 March 2020].

[29] R. Nave, "Heat conduction and Heat Convection," Georgia State University, 2016. [Online]. Available: http://hyperphysics.phy-astr.gsu.edu/hbase/thermo/heatra.html#c2. [Accessed 23 02 2020].

[30] H. D. Young, University Physics, 7th Ed., Addison Wesly, 1992.

[31] United Monolithic Semiconductors, "CHA5012 X-Band Driver Amplifier GaAs Monolithic Microwave IC," UMS, Orsay, France, 2016.

[32] Nanowave Technologies Inc, "E671: Phase II Reliability Analysis," Nanowave Technologies, Ottawa, 2019.

[33] D. M. Pozar, Microwave Engineering, 4e., Wiley, 2012.

[34] Rogers Corporation, "TMM Thermoset Microwave Materials Datasheet," Advanced Connectivity Solutions, Chandler, AZ, 2019.

[35] N. Durga Indira, K. Nalini, and H. Khan, "Design of Interdigital Bandpass Filter," *International Journal of Engineering and Advanced Technology,* vol. 2, no. 4, pp. 592-596, 2013.

[36] G. Matthaei, "Interdigital Band-Pass Fitlers," *IRE Transactions on Microwave Theory and Techniques,* pp. 479-491, 1962.

[37] B. S. a. P. J. Dr. Shiela Prasad, "Aids in the design of microstrip components I: Gensinger's Chart," *IEE-IERE Proceedings - India,* vol. 13, no. 6, pp. 210-217, 1975.

[38] Analog Devices, "HMC807LP6CE FRACTIONAL-N PLL WITHINTEGRATED VCO, 12.4 - 13.4 GHz, V03.0411," Analog Devices, Inc., rwood, MA 02, 2018.

[39] D. Banerjee, PLL Performance, Simulation, and Design, National Semiconductor, 1998.

[40] Nanowave Technologies Inc., "E671 Thermal Testing Report," Nanowave Technologies Inc., Norman, Oklahoma, 2019.

[41] P. K. Atul Makrariya, "Microstrip Interdigital Bandpass Filters: Design analysis.," *International Journal of Scientific & Engineering Research,* vol. 7, no. 3, 2016.

APPENDIX A: SIMULATION RESULTS OF STALO PLL

The results from the ADIpllSIM tool are available in this appendix.

OVERVIEW OF RESULTS

Frequency Domain Analysis of PLL
Analysis at PLL output frequency of 12.8GHz

Phase Noise Table

Freq	Total	VCO	Ref	Chip	SDM	Filter
100	-81.81	-163.1	--	-81.81	--	-145.8
1.00k	-91.44	-143.1	--	-91.44	--	-127.0
10.0k	-98.08	-123.2	--	-98.66	--	-107.2
100k	-94.68	-111.7	--	-101.7	--	-95.75
1.00M	-113.2	-129.9	--	-121.0	--	-114.0

Reference Spurious
Noise and Jitter Calculations include the first 10 ref spurs
First three spurs: -173 dBc -185 dBc -193 dBc

Phase jitter using brick wall filter
From 1.00 kHz to 20.0MHz
Phase Jitter **154fs rms**

ACP - Channel 1
Channel 1 is centred 25.0 kHz from carrier with bandwidth 15.0 kHz
Power in channel = **-54.7dBc**

---- End of Frequency Domain Results ----

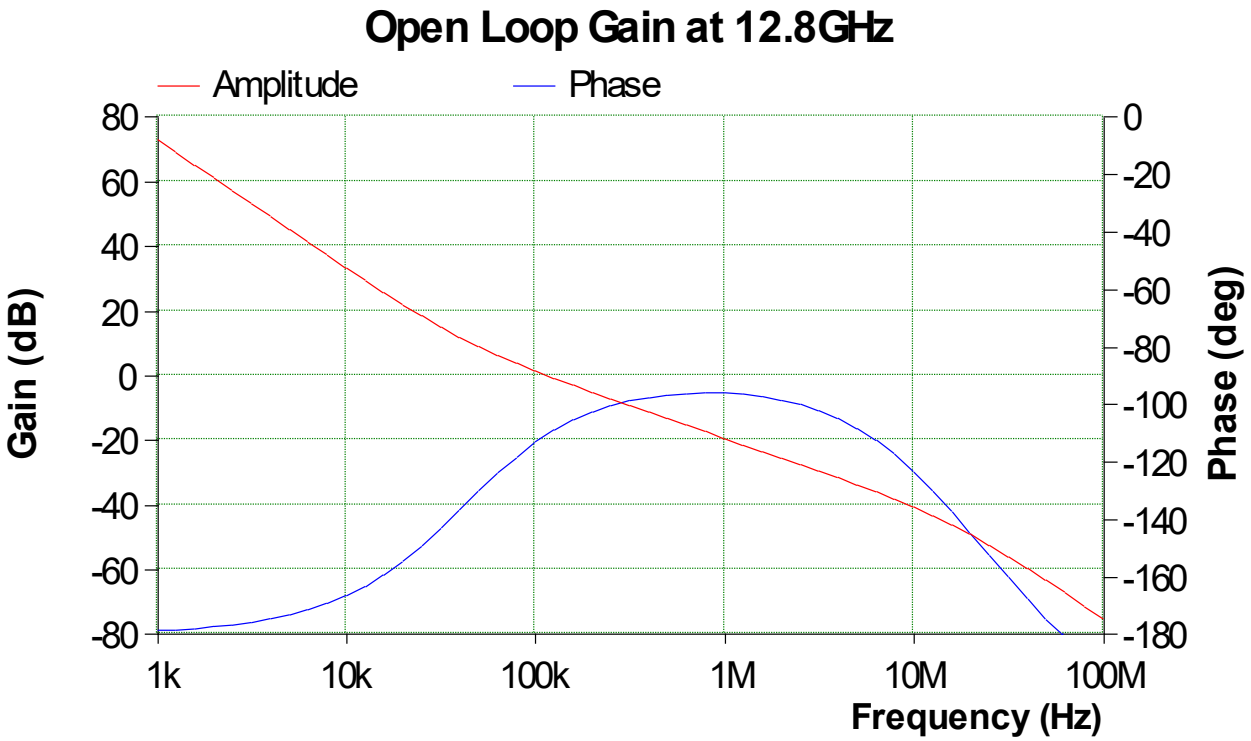
Transient Analysis of PLL
Power up transient to frequency of 12.8GHz
Simulation run for 147us Final Tuning voltage = 5.8547 V

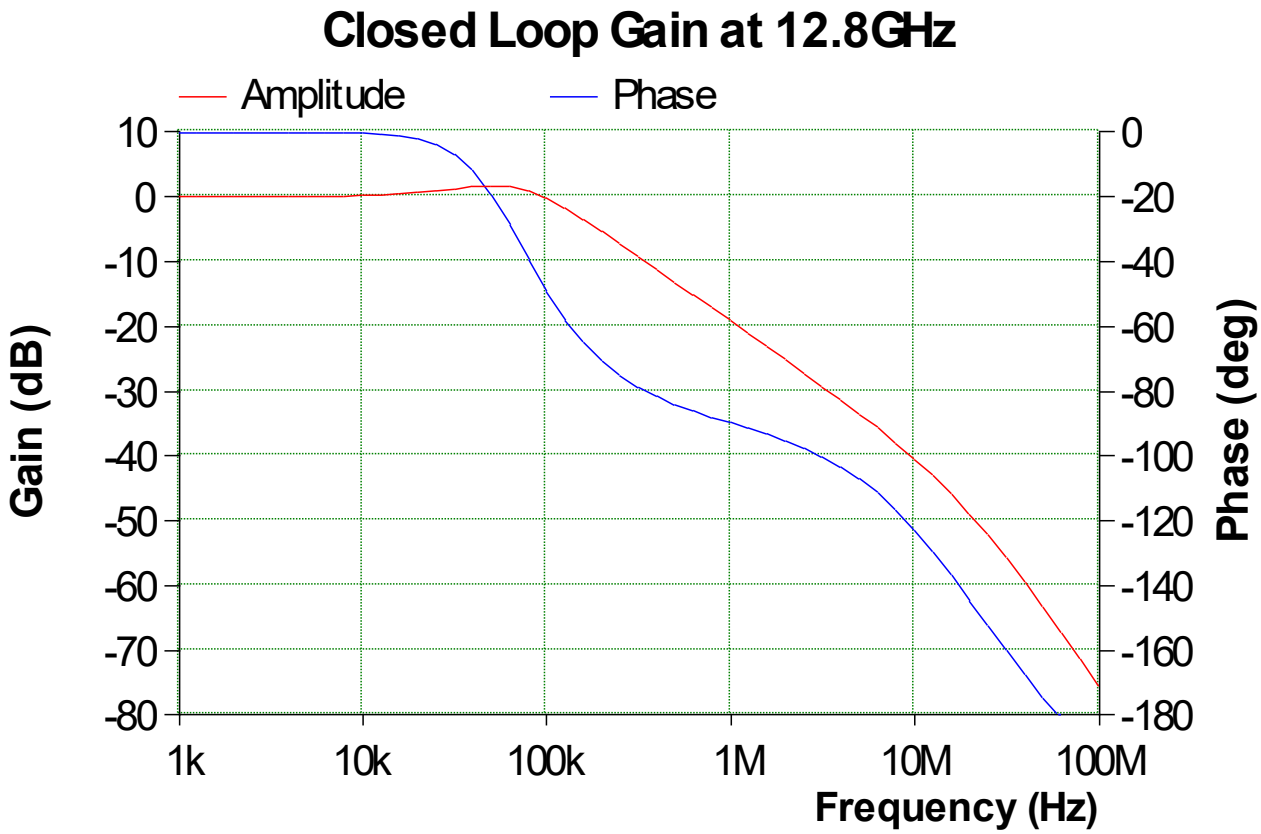
Frequency Locking
Time to lock to 1.00kHz is 78.8us
Time to lock to 10.0 Hz is 91.7us

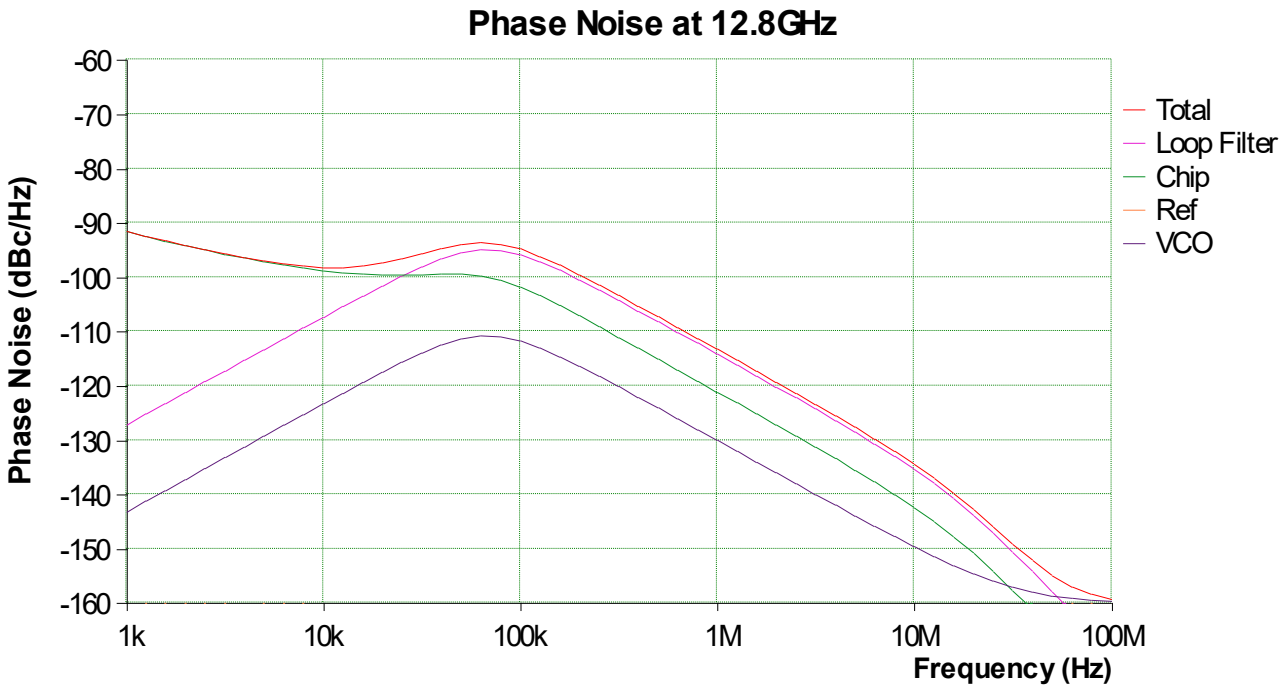
Phase Locking (VCO Output Phase)
Time to lock to 10.0 deg is 71.2us
Time to lock to 1.00 deg is 76.9us

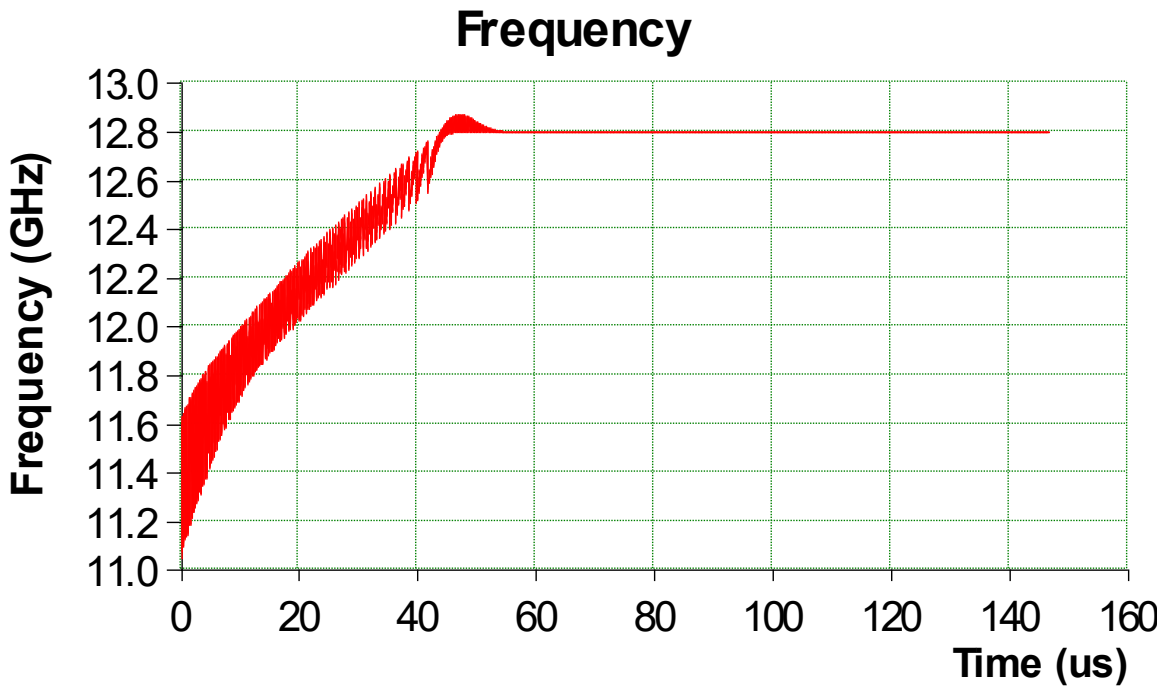
Lock Detect Threshold
Lock Detect output did not pass 2.50 V

---- End of Time Domain Results ----


Open Loop Gain at 12.8GHz
Amplitude
Phase
80
60
40
20
0
-20
-40
-60
-80
0
-20
-40
-60
-80
-100
-120
-140
-160
-180
1k
10k
100k
1M
10M
100M
Gain (dB)
Phase (deg)
Frequency (Hz)


Closed Loop Gain at 12.8GHz
Amplitude
Phase
10
0
-10
-20
-30
-40
-50
-60
-70
-80
0
-20
-40
-60
-80
-100
-120
-140
-160
-180
1k
10k
100k
1M
10M
100M
Gain (dB)
Phase (deg)
Frequency (Hz)


Phase Noise at 12.8GHz
Phase Noise (dBc/Hz)
-60
-70
-80
-90
-100
-110
-120
-130
-140
-150
-160
1k
10k
100k
1M
10M
100M
Frequency (Hz)
Total
Loop Filter
Chip
Ref
VCO


Frequency
Frequency (GHz)
13.0
12.8
12.6
12.4
12.2
12.0
11.8
11.6
11.4
11.2
11.0
0
20
40
60
80
100
120
140
160
Time (us)


|Freq Error|
Abs Frequency Error (Hz)
10G
1G
100M
10M
1M
100k
10k
1k
100
10
1
100m
0
20
40
60
80
100
120
140
160
Time (us)

APPENDIX B: RELIABILITY ANALYSIS RESULTS

λ Total	82.91 FIT

			Results			
Model	Component type	Component name	λ Total	Quantity	λ Unit.	%
ELECTRONIC COMPONENT	Ceramic capacitors [ECCC]	C1,C2	0.2	2	0.1	0%
ELECTRONIC COMPONENT	Ceramic capacitors [ECCC]	C11	0.0	1.000	0.0	0%
ELECTRONIC COMPONENT	Ceramic capacitors [ECCC]	C12, C15, C16, C19, C2	0.5	21.000	0.0	1%
ELECTRONIC COMPONENT	Ceramic capacitors [ECCC]	C13, C14, C17, C18, C2	0.0	1.000	0.0	0%
ELECTRONIC COMPONENT	Ceramic capacitors [ECCC]	C21, C25, C26	0.0	3.000	0.0	0%
ELECTRONIC COMPONENT	Ceramic capacitors [ECCC]	C29	0.0	1.000	0.0	0%
ELECTRONIC COMPONENT	Ceramic capacitors [ECCC]	C36	0.0	1.000	0.0	0%
ELECTRONIC COMPONENT	Ceramic capacitors [ECCC]	C8, C9, C10	0.0	3.000	0.0	0%
ELECTRONIC COMPONENT	Connectors [ECCO]	J1	0.2	1.00	0.2	0%
ELECTRONIC COMPONENT	Connectors [ECCO]	J2	0.1	1	0.1	0%
ELECTRONIC COMPONENT	Integrated Circuits [ECIC]	U1	0.6	1	0.6	1%
ELECTRONIC COMPONENT	Resistors [ECRE]	R17, R29, R30	0.0	3	0.0	0%
ELECTRONIC COMPONENT	Resistors [ECRE]	R35, R36, R37, R38, R4	0.0	15	0.0	0%
ELECTRONIC COMPONENT	Tantalum capacitors [ECTC]	C3, C4, C5, C6, C7	0.1	5	0.0	0%
HYBRID AND MULTICHIP MODULE	Case and substrate	Case	0.0	1	0.0	0%
HYBRID AND MULTICHIP MODULE	Ceramic capacitors	Cer Cap 215 pF	1.8	4	0.4	2%
HYBRID AND MULTICHIP MODULE	Ceramic capacitors	Cer Cap 30 pF	2.6	6	0.4	3%
HYBRID AND MULTICHIP MODULE	Ceramic capacitors	Cer Cap 40 pF	0.4	1	0.4	1%
HYBRID AND MULTICHIP MODULE	Ceramic capacitors	Cer Cap 50 pF	4.4	10	0.4	5%
HYBRID AND MULTICHIP MODULE	Ceramic capacitors	Cer Cap 1 nF	0.5	2	0.2	1%
HYBRID AND MULTICHIP MODULE	Ceramic capacitors	Cer Cap 1 uF	7.2	4	1.8	9%
HYBRID AND MULTICHIP MODULE	Ceramic capacitors	Cer Cap 12 pF	0.1	4	0.0	0%
HYBRID AND MULTICHIP MODULE	Ceramic capacitors	Cer Cap 120 pF	1.7	18	0.1	2%
HYBRID AND MULTICHIP MODULE	Ceramic capacitors	Cer Cap 7 pF	7.2	4	1.8	9%
HYBRID AND MULTICHIP MODULE	External Connection	Feedthrough	3.0	21	0.1	4%
HYBRID AND MULTICHIP MODULE	RF HF DS AsGa discrete semiconductor circui	AMM5618	1.0	2	0.5	1%
HYBRID AND MULTICHIP MODULE	RF HF DS AsGa discrete semiconductor circui	CHA5012	0.2	4	0.0	0%
HYBRID AND MULTICHIP MODULE	RF HF DS AsGa discrete semiconductor circui	FHX13X	0.5	1	0.5	1%
HYBRID AND MULTICHIP MODULE	RF HF DS AsGa discrete semiconductor circui	SBB5000	1.0	2	0.5	1%
HYBRID AND MULTICHIP MODULE	RF HF DS AsGa discrete semiconductor circui	TGA2512	0.5	1	0.5	1%
HYBRID AND MULTICHIP MODULE	RF HF IC AsGa integrated circuit [HMAG]	CHT4690	3.8	1	3.8	5%
HYBRID AND MULTICHIP MODULE	RF HF IC AsGa integrated circuit [HMAG]	HMC521A	2.1	2	1.0	3%
HYBRID AND MULTICHIP MODULE	Wiring	Bond Wire	0.0	56	0.0	0%
VARIOUS SUBASSEMBLIES	AC/DC and DC/DC voltage converters [VSAI	REG1, REG2, REG3, R	43.2	5	8.6	52%

Figure 59: Results of reliability analysis based on expected environmental conditions.

λ Total	234.24 FIT

			Results			
Model	Component type	Component name	λ Total	Quantity	λ Unit.	%
ELECTRONIC COMPONENT	Ceramic capacitors [ECCC]	C1,C2	0.2	2	0.1	0%
ELECTRONIC COMPONENT	Ceramic capacitors [ECCC]	C11	0.0	1.000	0.0	0%
ELECTRONIC COMPONENT	Ceramic capacitors [ECCC]	C12, C15, C16, C19, C2	0.7	21.000	0.0	0%
ELECTRONIC COMPONENT	Ceramic capacitors [ECCC]	C13, C14, C17, C18, C2	0.0	1.000	0.0	0%
ELECTRONIC COMPONENT	Ceramic capacitors [ECCC]	C21, C25, C26	0.0	3.000	0.0	0%
ELECTRONIC COMPONENT	Ceramic capacitors [ECCC]	C29	0.0	1.000	0.0	0%
ELECTRONIC COMPONENT	Ceramic capacitors [ECCC]	C36	0.0	1.000	0.0	0%
ELECTRONIC COMPONENT	Ceramic capacitors [ECCC]	C8, C9, C10	0.0	3.000	0.0	0%
ELECTRONIC COMPONENT	Connectors [ECCO]	J1	0.2	1.00	0.2	0%
ELECTRONIC COMPONENT	Connectors [ECCO]	J2	0.1	1	0.1	0%
ELECTRONIC COMPONENT	Integrated Circuits [ECIC]	U1	0.9	1	0.9	0%
ELECTRONIC COMPONENT	Resistors [ECRE]	R17, R29, R30	0.0	3	0.0	0%
ELECTRONIC COMPONENT	Resistors [ECRE]	R35, R36, R37, R38, R4	0.2	15	0.0	0%
ELECTRONIC COMPONENT	Tantalum capacitors [ECTC]	C3, C4, C5, C6, C7	0.6	5	0.1	0%
HYBRID AND MULTICHIP MODULE	Case and substrate	Case	0.0	1	0.0	0%
HYBRID AND MULTICHIP MODULE	Ceramic capacitors	Cer Cap 215 pF	3.9	4	1.0	2%
HYBRID AND MULTICHIP MODULE	Ceramic capacitors	Cer Cap 30 pF	5.8	6	1.0	2%
HYBRID AND MULTICHIP MODULE	Ceramic capacitors	Cer Cap 40 pF	1.0	1	1.0	0%
HYBRID AND MULTICHIP MODULE	Ceramic capacitors	Cer Cap 50 pF	9.7	10	1.0	4%
HYBRID AND MULTICHIP MODULE	Ceramic capacitors	Cer Cap 1 nF	1.0	2	0.5	0%
HYBRID AND MULTICHIP MODULE	Ceramic capacitors	Cer Cap 1 uF	8.8	4	2.2	4%
HYBRID AND MULTICHIP MODULE	Ceramic capacitors	Cer Cap 12 pF	0.5	4	0.1	0%
HYBRID AND MULTICHIP MODULE	Ceramic capacitors	Cer Cap 120 pF	3.6	18	0.2	2%
HYBRID AND MULTICHIP MODULE	Ceramic capacitors	Cer Cap 7 pF	8.8	4	2.2	4%
HYBRID AND MULTICHIP MODULE	External Connection	Feedthrough	58.1	21	2.8	25%
HYBRID AND MULTICHIP MODULE	RF HF DS AsGa discrete semiconductor circui	AMM5618	1.6	2	0.8	1%
HYBRID AND MULTICHIP MODULE	RF HF DS AsGa discrete semiconductor circui	CHA5012	0.3	4	0.1	0%
HYBRID AND MULTICHIP MODULE	RF HF DS AsGa discrete semiconductor circui	FHX13X	0.8	1	0.8	0%
HYBRID AND MULTICHIP MODULE	RF HF DS AsGa discrete semiconductor circui	SBB5000	1.6	2	0.8	1%
HYBRID AND MULTICHIP MODULE	RF HF DS AsGa discrete semiconductor circui	TGA2512	0.8	1	0.8	0%
HYBRID AND MULTICHIP MODULE	RF HF IC AsGa integrated circuit [HMAG]	CHT4690	6.1	1	6.1	3%
HYBRID AND MULTICHIP MODULE	RF HF IC AsGa integrated circuit [HMAG]	HMC521A	3.3	2	1.7	1%
HYBRID AND MULTICHIP MODULE	Wiring	Bond Wire	3.8	56	0.1	2%
VARIOUS SUBASSEMBLIES	AC/DC and DC/DC voltage converters [VSAI	REG1, REG2, REG3, RE	111.4	5	22.3	48%

Figure 60: Results of reliability analysis based on extreme environmental conditions.

APPENDIX C: DETAILED TEST PROCEDURES

The following appendix contains the test plan drafted to be provided to technicians for verification during qualification and production runs.

C.1 Transmitter Gain Test

The standard way to measure transmitter gain would be to use a VNA configured for conversion gain. This method will not work in this instance, as the VNA requires a copy of the LO operating in the system. However, the LO is internal to the frequency converter in this instance, and therefore unavailable for this measurement. For this reason, and alternate method was used as described below. The transmitter gain test will be completed using the test configuration as shown below in Figure 50 in the following manner:

1. DUT was placed in a thermally controlled chamber and allowed to soak at the specified test temperature for 30 minutes before beginning test. This test procedure was repeated for each temperature specified in Table 24: Environmental conditions for DUT acceptance test.
2. Digital baseband unit was used to configure STALO on UDC to 12.4 GHz.
3. RF cable 2 was disconnected from power meter. RF cable 1 was disconnected from the DUT and connected to input port of power meter. The signal generator output power was set to -8.15 dBm. The output power was measured at $3.00\ GHz$, $3.05\ GHz$, and $3.10\ GHz$ and adjusted to ensure -8.15 dBm was present at the output of RF Cable 1 for each frequency. The power setting on the signal generator required to achieve the

desired output power from RF Cable 1 at each frequency was recorded for use during the test.

4. RF cables were reconnected as shown in Figure 50.
5. The output power and frequency of RF Cable 2 was recorded for input frequencies of 3.00 GHz, 3.05 GHz, and 3.10 GHz.
6. Using measured losses in all RF connections, the interconnects were de-embedded in order to calculate the conversion gain for each input frequency.
7. The measurements were then repeated incrementing the LO frequency by 100 MHz until the LO frequency reached 12.9 GHz (with 12.9 GHz included in measurement set).

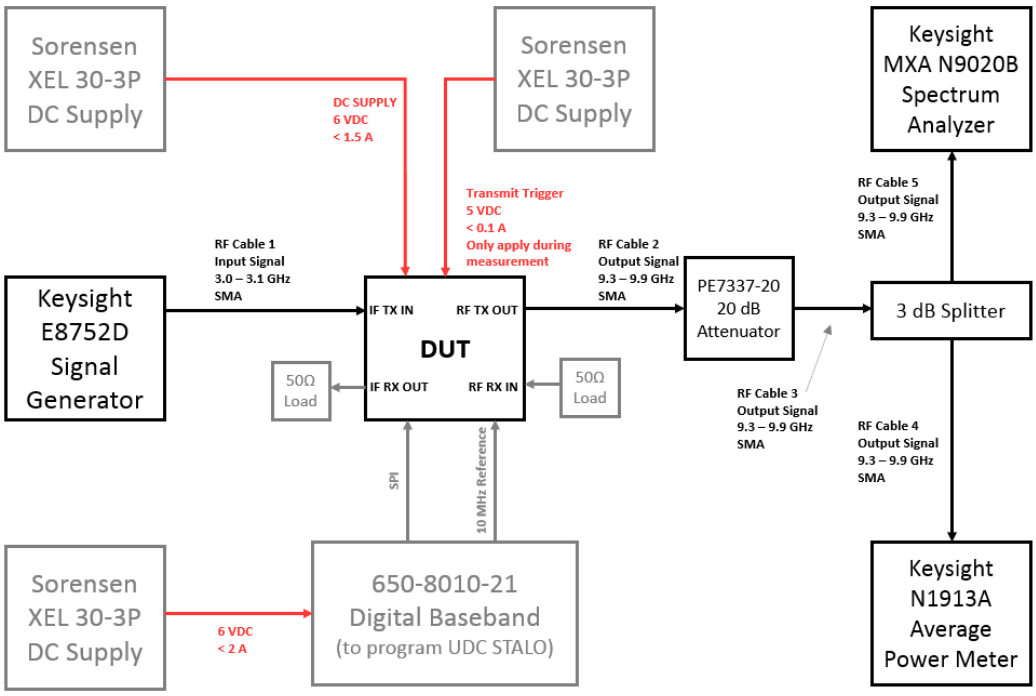


Figure 61: Test configuration for transmitter gain test.

C.2 Transmitter Spurious Test

The transmitter spurious test was completed using the diagram shown in Figure 51: Test configuration for transmitter spurious test. using the method described below:

1. DUT must be placed in a thermally controlled chamber and allowed to soak at the specified test temperature for 30 minutes before beginning test. This test procedure is to be repeated for each temperature specified in Table 24: Environmental conditions for DUT acceptance test.
2. Digital baseband unit was used to configure STALO on UDC to 12.4 GHz.
3. RF cable 2 was disconnected from power meter. RF cable 1 was disconnected from the DUT and connected to input port of power meter. The signal generator output power was set to +0.5 dBm. The output power was measured at $3.00\ GHz$, $3.05\ GHz$, and $3.10\ GHz$ and adjusted to ensure 0.5 dBm was present at the output of RF Cable 1 for each frequency. The power setting on the signal generator required to do this measurement was recorded for repeated use in this test.
4. RF cables were reconnected as shown in Figure 50.
5. For each input frequency, two measurements were recorded at each input frequency (3.00 GHz, 3.05 GHz, and 3.10 GHz). The power and frequency of the highest spur within ± 5 MHz of the center frequency of the spectrum analyzer, and the power and frequency of the highest spur in $f_c - 100MHz \geq f_{SPUR} \geq f_c - 5MHz$ and $f_c + 5MHz \leq f_{SPUR} \leq f_C + 100\ MHz$. The spectrum analyzer was configured with the following settings:

- Center Frequency: $f_{LO} - f_{INPUT}$
- Span: 200 MHz
- Points: >400
- Resolution bandwidth: 1 kHz
- Video Bandwidth: 1 kHz
- Detector: Positive Peak
- Trace: Maximum hold
- Measurement time: 5 minutes

6. The measurements were repeated incrementing the LO frequency by 100 MHz until the LO frequency reached 12.9 GHz (with 12.9 GHz included in measurement set).

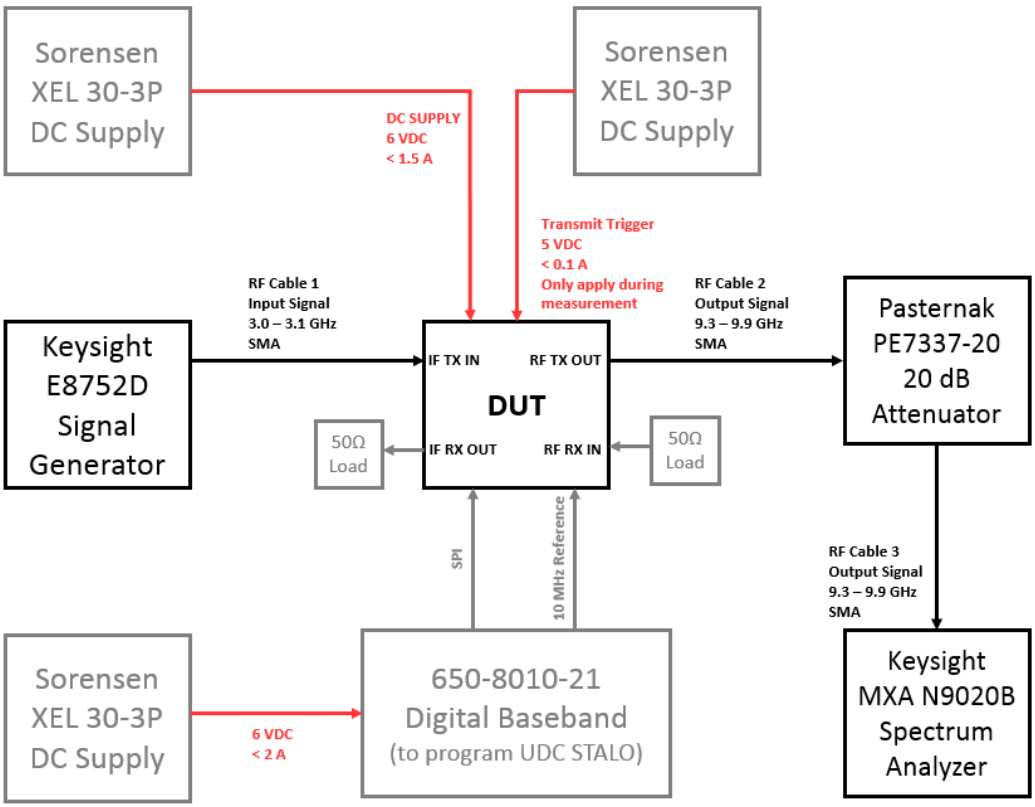


Figure 62: Test configuration for transmitter spurious test.

C.3 Receiver Gain Test

The receiver gain was verified using a similar approach to the transmitter gain. The test configuration is shown below in Figure 52. The test was conducted using the following procedure:

1. DUT must be placed in a thermally controlled chamber and allowed to soak at the specified test temperature for 30 minutes before beginning test. This test procedure is to be repeated for each temperature specified in Table 24: Environmental conditions for DUT acceptance test.
2. Digital baseband unit was used to configure STALO on UDC to 12.4 GHz.

3. RF cable 4 was disconnected from power meter. RF cable 1 was disconnected from the DUT and connected to input port of power meter. The signal generator output power was set to -40 dBm. The output power was measured from 9.3 GHz to 9.9 GHz in steps of 50 MHz and adjusted to ensure -40 dBm was present at the output of RF Cable 1 for each frequency. The power setting on the signal generator required to achieve the required power out of RF Cable 1 was recorded for use during the test.
4. RF cables were reconnected as shown in Figure 50.
5. The output power of the receiver was measured for the three following input frequencies: $f_{LO} - 3.00\ GHz, f_{LO} - 3.05\ GHz, and\ f_{LO} - 3.10\ GHz$.
6. Using measured losses in all RF connections, the interconnects were de-embedded in order to calculate the conversion gain for each input frequency.
7. The measurements were then repeated incrementing the LO frequency by 100 MHz until the LO frequency reached 12.9 GHz (with 12.9 GHz included in measurement set).

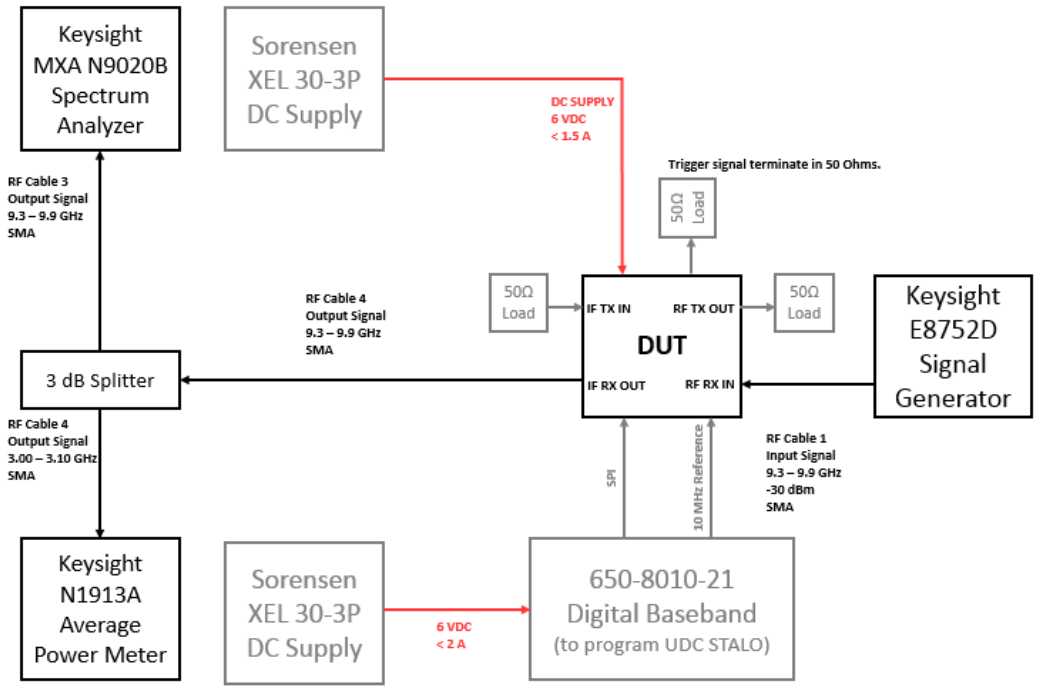


Figure 63: Test configuration for receiver gain test.

C.4 Receiver OP1dB Test

The receiver gain shall be measured using the same configuration as shown in Figure 52 using the following steps:

1. DUT must be placed in a thermally controlled chamber and allowed to soak at the specified test temperature for 30 minutes before beginning test. This test procedure is to be repeated for each temperature specified in Table 24: Environmental conditions for DUT acceptance test.
2. Using digital baseband unit to program STALO to 12.9 GHz.
3. Configure RF input signal to be $f_{STALO} - 3.00$ GHz at -40 dB_m following the cable de-embedding processes used in previous tests and record the output power.

4. Increase the input power in 1 dB_m increments to -15 dB_m. Plot and calculate P_{1dB}.
5. Repeat measurement over all temperature corners and for $f_{RF} = f_{STALO} -$ 3.00 GHz and $f_{RF} = f_{STALO} - 3.00$ GHz.
6. Repeat for $f_{STALO} = 12.4, 12.5, 12.6, 12.7, and\ 12.8\ GHz$ and record the worst-case output referenced 1dB compression point. This value must be greater than +5 dB_m.

C.5 Receiver Spurious Test

1. DUT must be placed in a thermally controlled chamber and allowed to soak at the specified test temperature for 30 minutes before beginning test. This test procedure is to be repeated for each temperature specified in Table 24: Environmental conditions for DUT acceptance test.
2. Use digital baseband to configure STALO on UDC to 12.4 GHz.
3. Losses of RF cables shall be de-embedded as done in previous tests. The input shall be set to $f_{LO} - 3.00\ GHz$ with a power of -30 dB_m.
4. For each input frequency, two measurements shall be recorded at the corresponding output frequency; the power and frequency of the highest spur within ± 5 MHz of the center frequency of the spectrum analyzer, and the power and frequency of the highest spur in $f_c - 100MHz \geq f_{SPUR} \geq f_c - 5MHz$ and $f_c + 5MHz \leq f_{SPUR} \leq f_C + 100\ MHz$. The spectrum analyzer will be configured with the following settings:
    - Center Frequency: $f_{LO} - f_{INPUT}$
    - Span: 200 MHz

- Points: >400
- Resolution bandwidth: 1 kHz
- Video Bandwidth: 1 kHz
- Detector: Positive Peak
- Trace: Maximum hold
- Measurement time: 5 minutes

5. The measurements shall be repeated for an input frequency of $f_{LO} - 3.05\ GHz$ and $f_{LO} - 3.10\ GHz$.
6. The measurements shall be repeated incrementing the LO frequency by 100 MHz until the LO frequency reached 12.9 GHz (with 12.9 GHz included in measurement set).

C.6 Power Supply Consumption Test

The power supply consumption test shall be completed using the test configuration shown in Figure 51 and shall be done using the following procedure:

1. DUT must be placed in a thermally controlled chamber and allowed to soak at the specified test temperature for 30 minutes before beginning test. This test procedure is to be repeated for each temperature specified in Table 24: Environmental conditions for DUT acceptance test.
2. Disconnect DC supply from trigger control port on UDC.
3. Connect trigger control from digital baseband unit to UDC. Ensure all SMA ports on the digital baseband and UDC which are un-used are terminated in 50-ohm loads.

4. Set the digital baseband unit into an active scan with maximum duty cycle (7.8%) and configure the STALO frequency to be 12.4 Apply an input signal of -8.15 dBm at 3.1 GHz following the cable de-embedding practices used in previous tests.
5. Observe the output signal in burst power mode on the E8752D signal generator to confirm the saturated output power is observed.
6. Record the current consumption from the DC power supply.
7. Repeat over all temperature corners, and for input signals of 3.00 and 3.05 GHz.
8. Adjust STALO frequency from 12.4 to 12.9 GHz in steps of 100 MHz. Repeat measurements.
9. The maximum current consumption for all input/STALO frequency shall not exceed 1.5 A_{RMS}.

C.7 TX-IN Return Loss Test

The IF TX input return loss shall be measured using the test configuration shown in Figure 53. The test shall observe the following procedure:

1. DUT must be placed in a thermally controlled chamber and allowed to soak at the specified test temperature for 30 minutes before beginning test. This test procedure is to be repeated for each temperature specified in Table 24: Environmental conditions for DUT acceptance test.

2. The TX trigger signal shall be held low, as all the active devices interfacing IF ports will always be powered on when the UDC is powered on (regardless of trigger signal). Only high-powered devices are modulated.
3. Before testing, a SOLT calibration must be done on the VNA over the frequency range of 3.0 to 3.1 GHz.
4. The return loss shall be measured over the specified band of 3.0 to 3.1 GHz and shall not exceed 15 dB.

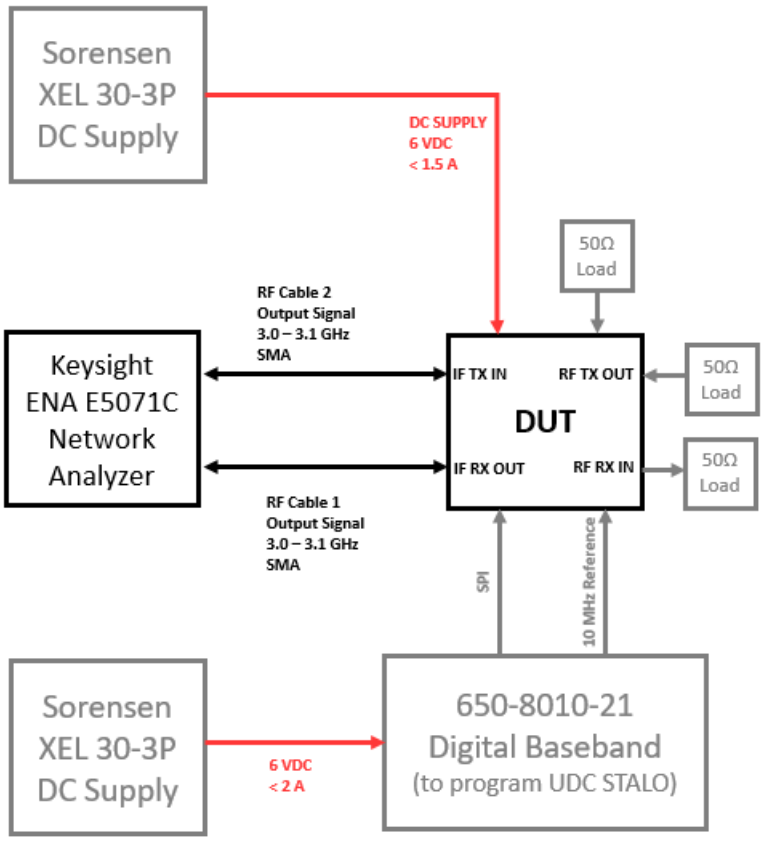


Figure 64: Test configuration for IF return loss measurements.

C.8 RX-OUT Return Loss Test

Measurement of the IF RX output return loss shall follow the procedure in section 5.1.5.8 for measuring the IF TX input return loss.

5.1.5.9 TX-OUT Return Loss Test

The output return loss of the RF TX output shall be completed using the test configuration shown in Figure 54. The test will use the following procedure:

1. DUT must be placed in a thermally controlled chamber and allowed to soak at the specified test temperature for 30 minutes before beginning test. This test procedure is to be repeated for each temperature specified in Table 24: Environmental conditions for DUT acceptance test.
2. Before testing, a SOLT calibration must be done on the VNA over the frequency range of 9.3 to 9.9 GHz.
3. The return loss should be measured with the amplifier turned on. While the TX path should withstand being powered on indefinitely without thermal failure, the trigger signal shall only be held high as long as required to take the measure to limit thermal stress.
4. The return loss shall be measured over the specified band of 9.3 to 9.9 GHz and shall not exceed 13 dB.

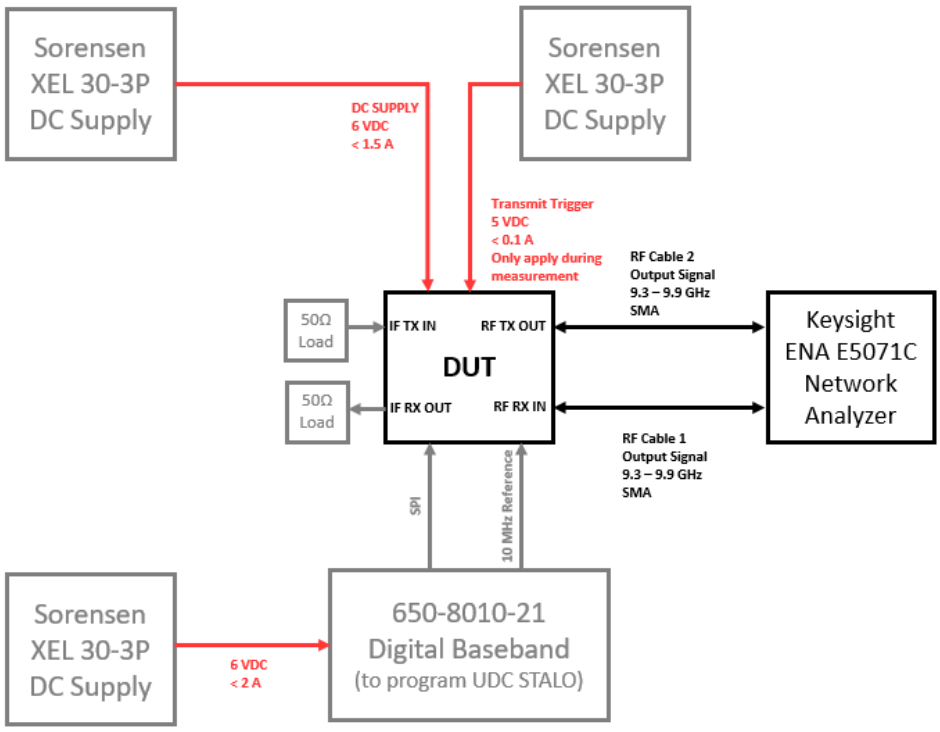


Figure 65: Configuration for return loss measurement of RF ports on UDC.

C.10 RX-IN Return Loss Test

The output return loss of the RF TX output shall be completed using the test configuration shown in Figure 54. The test will use the following procedure:

1. DUT must be placed in a thermally controlled chamber and allowed to soak at the specified test temperature for 30 minutes before beginning test. This test procedure is to be repeated for each temperature specified in Table 24: Environmental conditions for DUT acceptance test.
2. Before testing, a SOLT calibration must be done on the VNA over the frequency range of 9.3 to 9.9 GHz.

3. The transmit trigger shall be held low during this measurement, as the LNA is not modulated and it will reduce thermal stress on higher-powered devices.
4. The return loss shall be measured over the specified band of 9.3 to 9.9 GHz and shall not exceed 15 dB.

C.11 Receiver Noise Figure Test

The receiver noise figure test shall be completed using the configuration shown in Figure 55. The test will use the following procedure:

1. DUT must be placed in a thermally controlled chamber and allowed to soak at the specified test temperature for 30 minutes before beginning test. This test procedure is to be repeated for each temperature specified in Table 24: Environmental conditions for DUT acceptance test.
2. The MXA N9020B spectrum analyzer must be configured and calibrated for a noise figure measurement with frequency translation. The measurement shall be configured to be taken over an IF band of 3.0 to 3.1 GHz.
3. The digital baseband unit shall be used to configure the STALO frequency to 12.4 GHz.
4. The highest noise figure in the band for each temperature shall be recorded. The noise figure shall not exceed 3 dB.
5. The measurement shall be repeated while adjusting the STALO from 12.4 to 12.9 GHz in steps of 100 MHz.

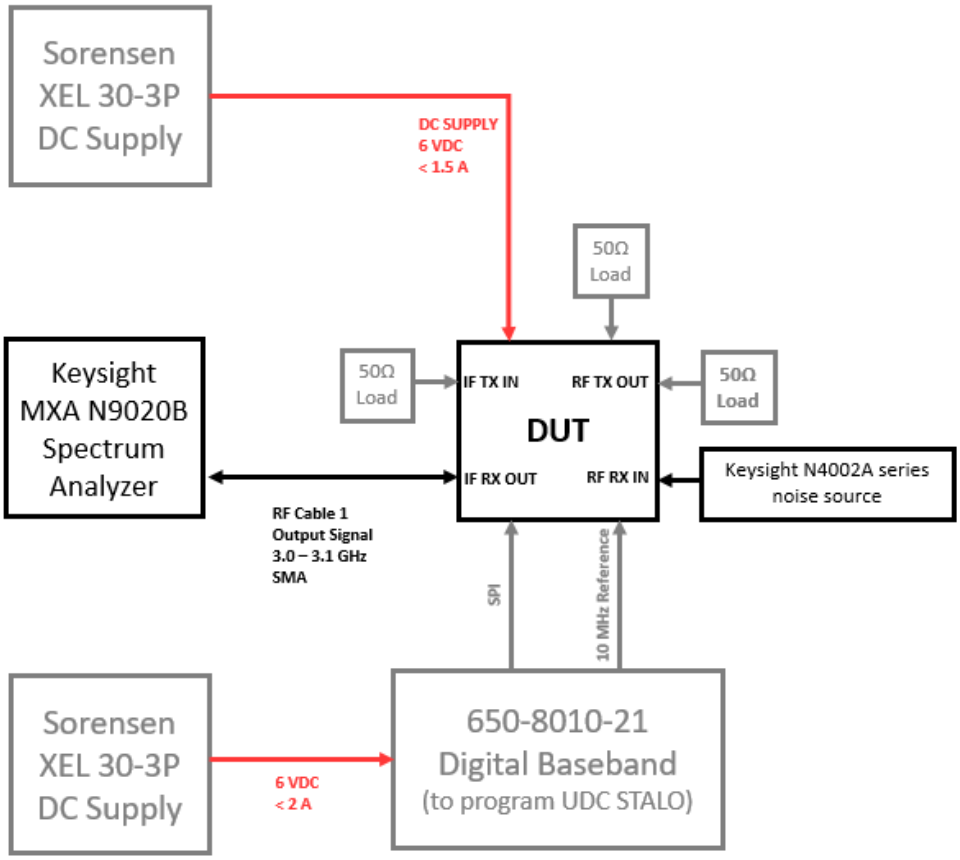


Figure 66: Test configuration for receiver noise figure measurement.

C.12 Highly Accelerated Thermal Stress Test

The end user has specified a highly accelerated thermal test for acceptance of all qualification units. It is worth noting that this acceptance test is where failure of the PCB implementation of the UDC produced a failure, raising concerns for the overall environmental durability of the design. The test is to exceed the specified system operating temperature by 5 degrees on either extreme, swinging the full operating temperature range on a diurnal cycle for 14 days consistently. The planned daily thermal cycle is shown below in Figure 56. During the testing, the

humidity shall be set to the maximum relative value (at dew point). It can be observed that there will be a 105ºC variation in temperature over a three-hour period. This variation is far more extreme that will be realized in any deployment.

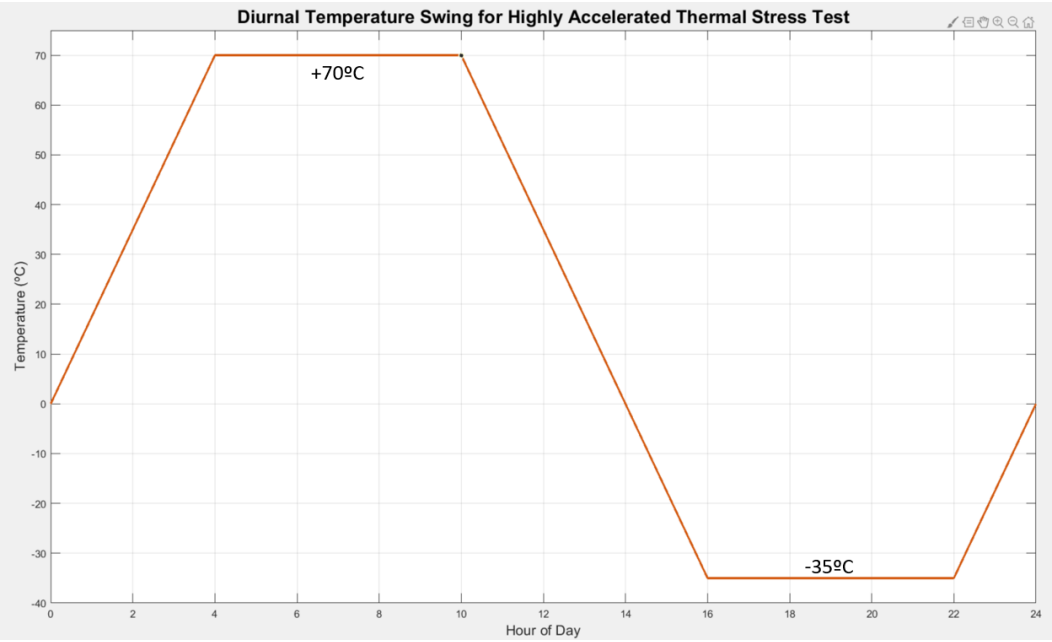


Figure 67: Diurnal temperature variation for accelerated thermal stress testing.

During the testing, the UDC will be placed in an environmental chamber to allow control of the subassembly. The device will be configured in RF loop back as shown below in Figure 57. The UDC will be connected to the digital baseband subassembly and configured to run an active scan at a pulse duration of 39 µs, with a repetition interval of 500 µs representing the maximum duty cycle of 7.8%. The output of the UDC will be monitored in software on the digital baseband unit to detect any changes in gain or distortion of the waveform. The test will be considered a success if no significant variation in output power or distortion is observed at the end of the 14-day period.

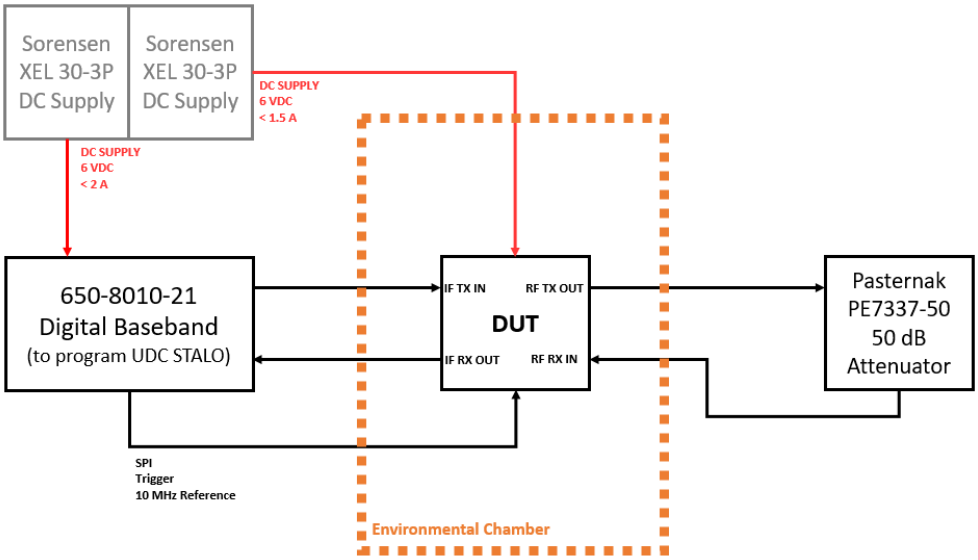


Figure 68: Test configuration for highly accelerated thermal stress test.

APPENDIX D: DC BUDGET

The DC budget is presented below. The analysis makes the following assumptions:

- 8.5 V rail was generated by a low-noise switching boost regulator from the 6V input rail with an output of 9 V, and then linearly regulated with low-noise LDO regulators back to 8.5 V. The analysis assumes the boost regulator achieves an efficiency of 90%.
- All voltages less than 6 V were generated using LDO regulators. The assumption is that current into the LDO regulator matches the current out, and any current losses in regulation are minimal.
- The expected power consumption for each device uses the maximum limit from the datasheet, to provide the worst-case view of power consumption.
- The calculated power consumption was increased by 20% to allow margin on the analysis.
- Analysis assumes the maximum duty cycle of 7.8%.

			TX			
Module	DC Consumption	DC Voltage	Modulated Consumption	QTY	Total	From 6 V
6080432-94	0.075	5	0.00585	1	0.00585	0.00585
6080432-83	0.26	8.5	0.02028	4	0.08112	0.1352
			TOTAL		**0.08697**	
			RX			
Module	DC Consumption	DC Voltage	Modulated Consumption	QTY	Total	
6080432-94	0.075	5	0.075	1	0.075	0.075
	0.09	5	0.09	1	0.09	0.09
	0.03	5	0.03	1	0.03	0.03
			TOTAL		**0.12**	
			LO			
Module	DC Consumption	DC Voltage	Modulated Consumption	QTY	Total	
	0.14	5	0.14	2	0.28	0.28
	0.09	5	0.09	2	0.18	0.18
			PCB			
Designator	DC Consumption	DC Voltage	Modulated Consumption	QTY	Total	
PLL/VCO	0.24	5	0.24	1	0.24	0.24
	0.12	3.5	0.12	1	0.12	0.12
			TOTAL		**0.36**	
Duty Cycle			**System Total @ 6V**		**1.15605**	
DC Efficiency			**DERATED 20%**		**1.38726**	