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CHARACTERIZATION OF MOS DEVICES FABRICATED ON LASER
CRYSTALLIZED POLYSILICON

by

Kamlesh Dutta Dwivedi

A thesis submitted to the Faculty of Graduate Studies
and Research in partial fulfilment of the
requirements for the degree of

Master of Engineering

Department of Electronics
Faculty of Engineering
Carleton University
Ottawa, Canada
July, 1981

The undersigned recommend to the Faculty of Graduate Studies and Research
the acceptance of the thesis:

"Characterization of MOS Devices fabricated on Laser Crystallized
Polysilicon"

submitted by Kamallesh Dutta Dwivedi in partial fulfillment of the requirements
for the degree of Master of Engineering.

Prof. R.E. Thomas
Thesis Supervisor

Prof. A.R. Boothroyd
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July, 1981

ABSTRACT

MOS transistors with channel length as short as 2.5 μ m and as long as 50 μ m have been fabricated in laser crystallized polysilicon layer. The results have been compared with those fabricated on single crystal silicon substrate. A modified expression for threshold voltage for polysilicon devices has been derived. A relatively smaller droop in channel conductance and gate to source transconductance at higher gate to source voltages for polysilicon devices has been reported and a need for a different modelling approach for laser crystallized polysilicon devices has been established.

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NOTE

This thesis was prepared with the aid of text editing facility available on VAX-11 computer. The digits following an alphabetic character denote a subscript throughout the thesis.

CHAPTER 1

INTRODUCTION

1.1 Overview Of Integrated Circuit Technology

The introduction of planar silicon technology in the late 1950's heralded the era of integrated circuits whereby the integration of an ever increasing number of circuit functions on the same chip became possible. Historically, the evolution of integrated circuits has progressed through small scale integration (SSI), medium scale integration (MSI) and large scale integration (LSI). SSI, introduced in the early 1960's, was characterized by an integration complexity of several logic gates per chip. With the development of a stable MOS process in the second half of the 1960's transition to the MSI phase occurred. The highest complexity MSI chip corresponded to about 100 logic gates or 256 bits of memory. The inception of large scale integration (LSI) is identified with the introduction in 1970 of the 1k-bit dynamic MOS RAM. LSI can be characterized by the development of proven silicon process technologies and outstanding progress in device and circuit development. One of the most advanced devices of the LSI era is the 16K-bit dynamic MOS RAM.

Development of 64K-bit dynamic MOS RAM's, 16K-bit static MOS RAM's, 16-bit microprocessors and logic arrays with about

10,000 logic gates marked the birth of the Very Large Scale Integration (VLSI) phase. This phase is characterized by extension of the technologies to achieve finer and finer dimensions and to refinement in device structures and introduction of new innovative circuit design ideas. It is possible to extrapolate the history of integrated circuit technology into the future and foresee a long continuation of the rapid progress shown by the famous Moore's curve[1]. However, the extrapolation implies certain changes in the intensive parameters of a system, such as increasing impurity concentrations and electric fields in semiconductor components and increasing power dissipation in large systems containing many components. In other words, one must consider the extrapolation of semiconductor technology to ever smaller dimensions in the light of known semiconductor phenomena and the laws of physics. Some of the phenomena that apparently are likely to limit the functioning of miniaturised, highly integrated semiconductor devices are: electromigration, hot electrons and breakdown, wiring complexity, ohmic resistance, interconnections and power dissipation. An extrapolation of the levels of integration of main memory and logic chips taking the aforementioned phenomena into account shows a saturating trend in both bits per chip and circuits per chip[2] as contrasted to the Moore's curve[1] which predicted the doubling of circuit complexity every year.

All these extrapolations of the level of integration have been done considering the 'in-plane' fabrication of semiconductor devices and taking into account improvement in the basic device technology such as electron-beam lithographic capability to define the sub-micron pattern linewidths and ion-implantation to accurately introduce the dopant impurities. Shrinkage in device dimensions following the 'scaling rules' is, however, ultimately limited by the laws of physics. So the question arises: where do we go from here?

Application of lasers to device fabrication domain provides part of the answer. The speed of logic circuits will be ultimately limited by the laws of physics but the density of circuits per chip can be approximately doubled if the 'in-plane' fabrication of devices is extended to the concept of 'multi-plane', 'high-rise' devices. One such 'high-rise' CMOS structure in which the the N-channel transistor, instead of lying by the side of the P-channel transistor, sits on the top of the P-channel device, has been recently shown feasible[3]. This feat has been achieved by using lasers to crystallize the polysilicon layer deposited on the top of an insulator such as silicon-dioxide. A brief review of the work done to-date on Laser-Assisted-Crystallization(LAC) is given in the next section.

1.2 Review Of Previous Work On Laser Assisted Crystallization:

Ever since the first Russian work [4] in 1974, the subject of laser annealing has become one of increasing international activity. This application of the laser was, however, designed to remove ion-implantation induced damage in silicon, whereas the idea of using lasers to crystallize a polysilicon layer is a recent one [5-13]. Workable semiconductor devices have been made and reported [5-12] on laser crystallized polysilicon with a performance comparable to those on silicon-on-sapphire (SOS) substrates.

The first attempt to fabricate MOS transistors on a polysilicon layer was made by T.I. Kamins [14] using high temperature polysilicon deposition followed by thermal annealing. The field-effect mobility obtained was very low (approx. 30 cm²/V-sec), so it was concluded that MOS transistors fabricated in polycrystalline silicon films would probably find limited practical application. The introduction of lasers to anneal the polysilicon film, however, changed the scene. A field-effect mobility of 300- 400 cm²/V-sec, calculated from the source-drain I-V characteristics of NMOS devices, fabricated on laser crystallized polysilicon, has been reported by K.F. Lee et al [15]. Reasonably good I-V characteristics for MOS devices have

also been obtained with the underlying substrates being silicon dioxide and silicon nitride[16-17].

1.3 Subject Of The Thesis:

Almost all the previous researchers have used ion-implantation as a means to introduce impurities into the polysilicon film. An alternate approach, which has been adopted in this thesis, is to dope the polysilicon film by introducing suitable dopants in the epitaxial reactor while the polysilicon film is growing. This eliminates the need of an ion-implanter and a complex process step in the fabrication schedule. Secondly, doping during growth gives large sized grains to start with and consequently lower power is required to crystallize the film. Using such a doped, chemical-vapour-deposited (CVD) polysilicon layer as the starting material and subsequent laser assisted crystallization, NMOS transistors were fabricated and characterized in detail for threshold voltage, channel conductance, gate transconductance and the field-effect mobility which has not been reported so far by any of the previous researchers. The threshold voltage is found to show a dependence on the defect levels in the semiconductor bulk. The channel conductance and the gate transconductance show the usual droop at higher gate voltages. But the percentage droop is much lower than that for MOS devices fabricated on

single crystal silicon. An electron field-effect mobility of $500 \text{ cm}^2/\text{V}\cdot\text{SEC}$ has been reported for the short channel devices which is higher than that reported by previous researchers..

1.4 Organisation Of The Thesis:

This thesis has been organised into six chapters. Chapter-1 introduces the phenomenon of laser-assisted crystallization in the perspective of VLSI and sets the scene for this research work. Chapter-2 deals with laser theory in brief. The physics of the laser action is dealt with, with an emphasis on the optics of the laser beam which is relevant to the semiconductor device process engineer. A mathematical expression for the spot-size of the laser beam has been derived. The chapter ends with a description of potential application areas for laser in device processing. Chapter-3 starts with a brief description of conventional crystal growing techniques used in semiconductor industry to allow comparison with laser assisted crystallization (LAC). The mechanisms of laser crystallization via either a solid phase or a liquid phase growth are highlighted and thermal crystallization via furnace annealing is compared with LAC. Laser-solid interactions are considered and the heat flow equation derived to allow the temperature profile normal to the silicon surface being crystallized to be plotted.

Finally, the spot size of the laser beam has been calculated and plotted after the theory developed in chapter-2.

Chapter-4 deals with the characterization of as-deposited and laser-crystallized polysilicon layers on different substrates by resistivity measurements and optical and scanning electron microscopic methods. Chapter-5 presents the characteristics of n-channel MOS transistors emphasizing the channel conductance, gate transconductance, threshold voltage and field-effect mobility. Theoretical I-V characteristics of sample devices have been obtained by finding V_t and X_j from SUPREM-III (a device process simulation program) and current and voltage characteristic from SPICE2F-1 (a circuit simulation program) and compared with the results obtained experimentally. Chapter-6 concludes this research work and suggests areas of further work in the application of lasers to device processing.

CHAPTER-2

LASER:ITS THEORY AND APPLICATION TO SEMICONDUCTOR DEVICE PROCESSING

2.1,Introduction:

The recent application[4-14] of lasers in to the fabrication of solid-state devices has opened up various possibilities in the area of very large scale integrated (VLSI) circuits. Though a complete knowledge of laser physics is not essential for a device processing engineer, a brief treatment of laser theory and laser optics is necessary for successful employment of this tool in device fabrication. This chapter deals with the principle of laser operation, laser optics and its applications to device processing.

2.2 Laser Theory:

2.2.1 Laser Action:

A laser (Light Amplification by Stimulated Emission of Radiation) works by the "stimulated emission" of radiation. When electrons excited to a higher energy level fall to lower energy states, there is an emission of radiation. Normally these processes occur randomly and, therefore, are

called 'spontaneous emission'. The rate at which electrons fall from a higher level of energy E_2 to a lower level of energy E_1 is at every instant proportional to the number of electrons remaining in E_2 , which is called the 'population' of E_2 . The electron population in E_2 , if allowed to decay follows an exponential rate of decay to a lower energy level with a mean decay time characterizing the process. The electrons in a higher energy level can, however, be 'stimulated' to fall to a lower energy level and emit photons in a time much shorter than the mean spontaneous decay time. This stimulus is provided by the presence of photons of the proper wavelength.

Assume that an electron in energy state E_2 is waiting to drop spontaneously to a lower level E_1 as shown in Fig. 2.1. If it does so, a photon of energy given by

$$h\nu = E_2 - E_1 \quad \dots (2.1)$$

will be emitted. Here, h is the Planck's constant and ν is the frequency associated with the wave properties of the emitted photon. Now assume that the electron in the energy state E_2 is immersed in an intense field of photons, each with an energy given by equation (2.1) above, and in phase with the other photons. The electron is thus induced to drop in energy from E_2 to E_1 , emitting a photon whose wave is in phase with the radiation field. If this process is con-

tinued and other electrons are stimulated to emit photons in the same way, a large radiation field can build up. Since each emitted photon has an energy of precisely $h\nu = E_2 - E_1$, this stimulated radiation will be 'monochromatic' and because all the emitted photons are in phase and reinforcing, it will be 'coherent'.

With the stimulating photon field, there will be some absorption of photons and electrons will find sufficient energy to jump to the higher energy level E_2 . For an emission to occur, the rate of emission must be higher than the rate of absorption. Let the instantaneous populations of E_2 and E_1 be n_2 and n_1 respectively. At thermal equilibrium, if the levels contain an equal number of available states, the relative population is given by

$$\frac{n_2}{n_1} = \text{EXP}(-\Delta E/KT) = \text{EXP}(-h\nu/KT) \quad \dots\dots (2.2)$$

Hence at equilibrium, $n_1 \gg n_2$, i.e. most of the electrons are in the lower energy level as expected. If the atoms exist in a radiation field of photons with energy $h\nu$ such that the energy density of the field is $p(\nu)$, then stimulated emission can occur along with absorption and spontaneous emission. The rate of stimulated emission is proportional to the instantaneous number of electrons in the upper energy

level, n_2 , and to the energy level of the stimulating field, $p(\nu)$, and is given by

$$\text{Rate Of Stimulated Emission} = B_{21} \cdot n_2 \cdot p(\nu) \quad (2.3)$$

where B_{21} is the proportionality constant. The rate at which photons are absorbed by the electrons in E_1 is proportional to $p(\nu)$ and to the electron population, n_1 , in E_1 and is given by

$$\text{Rate Of Photon Absorption} = B_{12} \cdot n_1 \cdot p(\nu) \quad (2.4)$$

Where B_{12} is another proportionality constant. The rate of spontaneous emission is proportional to the electron population in the upper energy level and can be described by

$$\text{Rate Of Spontaneous Emission} = A_{21} \cdot n_2 \quad (2.5)$$

where A_{21} is a proportionality factor for spontaneous emission. For steady state, the two emission rates must balance the rate of absorption to maintain the population n_1 and n_2 in E_1 and E_2 , respectively. So

$$B_{12} \cdot n_1 \cdot p(\nu) = A_{21} \cdot n_2 + B_{21} \cdot n_2 \cdot p(\nu) \quad (2.6)$$

FIG 2.1: Transition of electron from an upper state to a lower state, with accompanying photon emission.

FIG 2.2: Balance of absorption and emission in steady state (a) stimulated emission; (b) absorption; (c) spontaneous emission

These three processes are shown in Fig.2.2. The coefficients B_{12} , A_{21} and B_{21} are called Einstein's coefficients. At thermal equilibrium, the ratio of the stimulated emission rate to the spontaneous emission rate is generally very small, and the contribution of stimulated emission is negligible. The ratio is given by

$$\frac{\text{Stimulated Emission Rate}}{\text{Spontaneous Emission Rate}} = \frac{B_{21} \cdot n_2 \cdot p(\nu)}{A_{21} \cdot n_2} \dots (2.7)$$

As depicted by equation (2.7), to make the stimulated emission predominate over the spontaneous emission, a very large photon field density, $p(\nu)$, is required. In the laser, this is achieved by providing an optical resonant cavity in which the photon density can build up to a large value through multiple internal reflections at certain frequencies (Fig.2.3).

Similarly the ratio of stimulated emission rate to absorption rate is given by

$$\frac{\text{Stimulated Emission Rate}}{\text{Absorption Rate}} = \frac{B_{12} \cdot n_1 \cdot p(\nu)}{B_{12} \cdot n_1 \cdot p(\nu)} = \frac{B_{21} \cdot n_2}{B_{12} \cdot n_1} \dots (2.8)$$

Thus for stimulated emission to dominate over absorp-

FIG.2.3: Resonant Modes Within A Laser Cavity

tion of photons from the radiation field, $n_2 \gg n_1$, i.e. more electrons must be maintained in the upper energy level E_2 than in the lower energy level E_1 . This condition is unnatural, since equation (2.2) indicates that n_2/n_1 is less than unity for any equilibrium case. Because of this unusual nature, the condition $n_2 \gg n_1$ is called 'population inversion'. This is also referred to as a condition of negative temperature, because $n_2 \gg n_1$, if T in the exponent of equation (2.2) is negative. Thus to obtain laser action two conditions must be satisfied:

(1) A very large photon field density, and

(2) Population inversion, i.e., $n_2 \gg n_1$

2.3 Optics Of Laser Beams

2.3.1 Mathematical Representation Of Laser Beams:

Most well designed lasers emit an output beam that is very close to an ideal Gaussian spherical beam which can be represented mathematically as follows [18]:

$$\bar{u}(x,y) = \sqrt{\frac{2}{\pi}} \cdot \frac{1}{w} \cdot \text{EXP} \left[\frac{-j\pi(x^2+y^2)}{\lambda \cdot R} \right] \cdot \text{EXP} \left[\frac{-(x^2+y^2)}{w^2} \right] \quad \dots (2.9)$$

Combining the two separate exponents in the above equation, we may write the total exponent in the form

$$- \frac{j\pi(x^2+y^2)}{\lambda \cdot R} - \frac{x^2+y^2}{w^2} = \frac{-j\pi(x^2+y^2)}{\lambda \cdot \bar{q}} \quad \dots\dots\dots (2.10)$$

And the expression for $u(x,y)$ becomes

$$\bar{u}(x,y) = \sqrt{\frac{2}{\pi}} \cdot \frac{1}{w} \cdot \text{EXP} \left[-j\frac{\pi}{\lambda} \cdot \frac{x^2+y^2}{\bar{q}} \right] \quad \dots\dots\dots (2.11)$$

where $\bar{q}$, defined as complex radius of curvature, is given by

$$\frac{1}{\bar{q}} = \frac{1}{R} - j \frac{\lambda}{\pi w^2} \quad \dots\dots\dots (2.12)$$

The one complex number $\bar{q}$ contains both the radius of curvature, R , and the spot size, w , of the Gaussian spherical wave. The expression given by equation (2.12) will be used in the following section to find the spot size and radius of curvature at any given point in space, provided beam properties at some previous points are given.

2.3.2 Propagation Of Gaussian Spherical Wave

Assume a Gaussian plane wave at an input plane $z=0$, as shown in Fig. 2.4,

$$\bar{u}(x,y) = \sqrt{\frac{2}{\pi}} \cdot \frac{1}{w} \cdot \text{EXP} \left[-j \frac{k(x^2+y^2)}{2\bar{q}} \right] \quad \dots\dots\dots (2.13)$$

$$\text{where } \left\{ \begin{array}{l} k = \frac{2\pi}{\lambda} \\ \bar{q} = j \frac{\pi w^2}{\lambda} \end{array} \right. \quad \dots\dots\dots (2.14)$$

As the wave propagates, the radius of curvature R and

Fig 2.4 Outward Propagation Of a Gaussian Beam From a Waist, located at $Z=0$.

Fig 2.5 A Collimated Gaussian Beam.

the spot size w change with distance. By applying the simplified Huygens principle [18] $u(x,y)$ at a later plane z is given by,

$$u(x,y,z) = \sqrt{\frac{2}{\pi}} \cdot \frac{1}{w(z)} \cdot \text{EXP}[-j\{Kz - \psi(z)\}] \cdot \text{EXP}\left[-j \frac{k(x^2 + y^2)}{2 \tilde{q}(z)}\right] \quad (2.15)$$

where,

$$\begin{aligned} \tilde{q}(z) &= z + j \frac{\pi w^2}{\lambda} z^{1/2} \\ R(z) &= z \left[1 + \left(\frac{z_r}{z} \right)^2 \right]^{1/2} \\ W(z) &= W_0 \left[1 + \left(\frac{z}{z_r} \right)^2 \right]^{1/2} \\ \psi(z) &= \tan^{-1} \left(\frac{\lambda z}{\pi W_0^2} \right), \quad z_r = \frac{\pi W_0^2}{\lambda} \quad (2.16) \end{aligned}$$

The input plane where the beam wavefront is planar and the spot size is W_0 , is called the waist of the beam. The results expressed by the equation (2.16), show that a beam starting as a Gaussian plane wave at a waist will remain in the form of a Gaussian wave with complex curvature $\tilde{q}(z)$ at all later planes z , as shown in Fig. 2.5. The radius of curvature of this diverging wave as a function of distance from the waist is given by

$$\begin{aligned} R(z) &= z \left[1 + \left(\frac{z_r}{z} \right)^2 \right]^{1/2} \\ &= z; \text{ for } z \gg z_r \quad (2.17) \end{aligned}$$

Thus at sufficiently large distances from the waist, the wave has a spherical wavefront with its center of curvature located essentially at the waist. Furthermore, since the spot size of the beam as a function of distance from the waist is given by

$$W(z) = W_0 \left[1 + \left(\frac{z}{Z_r} \right)^2 \right]^{1/2}$$

$$= W_0 \cdot \left(\frac{z}{Z_r} \right); \text{ for } z \gg \frac{\pi W_0^2}{\lambda} \dots (2.18)$$

at large distances from the waist the beam diverges linearly with distance. Thus as a Gaussian wave propagates outward from a waist, its diameter or spot size at first stays nearly constant, then begins to diverge linearly with distance at large distances. What is required is a pencil laser beam which remains collimated to as small a diameter as possible for as long a distance as possible. A collimated laser beam is simply a particularly long Gaussian-beam waist, as shown in Fig. 2.5. The collimated region is defined as extending between the points where the spot size $W(z)$ has increased by $\sqrt{2}$ over the value $W(0)$ at the waist [18]. The distance Z_r from the beam waist to the $\sqrt{2} W(0)$ point is given by the equation

$$W(z) = W_0 \left[1 + \left(\frac{\lambda z}{\pi W_0^2} \right)^2 \right]^{1/2} = \sqrt{2} W_0$$

$$\text{or, } Z_r = \frac{\pi W_0^2}{\lambda} \dots (2.19)$$

The quantity z_r is called the Rayleigh range. The waist region extends for roughly one z_r on either side of the origin. From (2.19) it is obvious that the smaller the spot size of the beam, the more rapidly it diverges and smaller is the Rayleigh range, which is a measure of collimation of the laser beam.

2.3.3 Gaussian Beam Propagation Through An Optical Element:

The expressions for the laser beam spot size derived above apply to the beam travelling in free space. When beam modifying optical elements such as mirrors, lenses and dielectric interfaces are present, as is the case with laser-assisted-crystallization set-up, to be described in the next chapter, the beam properties are modified. Consider an arbitrary black-box optical system as shown in Fig.2.6. The optical system can be characterized by its $[A, B, C, D]$ parameters of the ray matrix [18]. The overall effects are summarized by

$$\begin{aligned} r_2 &= A \cdot r_1 + B \cdot r_1' \\ r_2' &= C \cdot r_1 + D \cdot r_1' \end{aligned} \quad \dots\dots\dots (2.20)$$

The wavefront curvature R and the ray parameters r and r' are related by

Fig 2.6 Evaluation Of Gaussian Beam Propagation through an arbitrary optical system..

$$r' = r/R \quad \text{or} \quad R = r/r' \quad \dots\dots\dots (2.21)$$

Therefore the input and output wavefront curvatures for the optical black box may be related by

$$R_2 = \frac{r_2}{r_1} = \frac{A \cdot R_1 + B}{C \cdot R_1 + D} \quad \dots\dots\dots (2.22)$$

Equation (2.22) has been shown to hold true for the wavefront radius R in geometrical optics, however, this relationship holds for any optical system if $\bar{q}$ is substituted for R in equation (2.22) [18]. These expressions will be used for finding the spot size of the laser beam in the next chapter.

2.4 Lasers In Semiconductor Device Processing

Although lasers have been used for sometime in hybrid circuit technology for trimming resistors, penetration by lasers into the solid state device fabrication domain is a recent phenomenon [4-15]. The flowchart given in Fig. 2.7 shows the important applications of lasers in integrated circuit (IC) technology [5]. Some of these applications are briefly outlined below.

Fig 2.7 Application of Lasers To Device Processing [5]

(a) Scribing:

Laser scribing is the oldest and most common laser application in device processing. Q-switched YAG lasers, which provide relatively high peak power at repetition rates ranging upto 50 kHz, have been employed for scribing. The laser light at 1.06 micron couples effectively into silicon and the absorption is sufficient to effect adequate material removal. Typically, laser kerfs of 25 micron have been obtained during routine production operation on commercial systems[5].

(b) Silicon Drilling:

Because of the interdigitation of beam leads in beam lead technology, laser scribing for chip separation cannot be employed. However, a laser is still employed in the process for drilling alignment holes required to achieve front to back alignment followed by subsequent etching to effect ultimate chip separation. The most suitable laser for achieving drilling of holes 25 micron in diameter to a depth of 175 micron, in a single shot is a pulsed YAG laser with sub-millisecond pulses[5].

(c) Connections:

Formation of connections for MOS structures is one of the first laser applications[5]. During the development phase of a design program, or when a small number of components is needed, it is more economical and requires a shorter

turnaround time if a laser is used to customise individual circuits for specific functional response. Such a step eliminates the need of additional masks and the steps associated with the particular mask level.

(d) Gettering:

Laser induced damage has proven to be an effective gettering mechanism in removing transitional metal contaminants from active areas in a preprocessing step whose effectiveness is not lost during subsequent device processing. Laser induced gettering has removed the shortcomings encountered in other gettering mechanisms such as mechanical damage, impurity diffusion and use of stress producing films and it is a basis for a clean, well controlled and effective gettering technique[5].

(e) Photo Induced Zone Migration (PIZM):

In photo induced zone migration (PIZM), a thin layer of a suitable metal, eg. Aluminium, is deposited on one surface of a silicon wafer. This metal film is then heated by transmission, through the wafer from the other side, using a high power CO laser. A molten zone of silicon rich Aluminium is thereby formed and this zone migrates through the silicon towards the light source. This process could possibly find application for deep junction isolation and in large area high power devices such as thyristors and triacs.

(f) Laser Induced Oxidation:

Since the surface of a silicon wafer can be heated to temperatures on the order of 1000 C during laser crystallization, if the surface is left in an oxidizing ambient, silicon dioxide can be expected to grow on the irradiated surface. The oxidation rates for laser oxidation in steam ambient are comparable to the furnace oxidation rates[6]. By repeated raster scanning of a silicon surface immersed in an oxidizing environment, it has been possible to grow 200A thick oxide layers having breakdown voltages of more than 20V[6].

(g) Laser Assisted Dopant Diffusion:

It has been recently shown by Narayan et al.[7] that lasers can be used to induce impurity diffusion in the substrates. The advantages of laser induced diffusion accrue from the fact that lasers provide a heat source at a localized spot, so all the wafer need not be subjected to high temperature and as a result, impurity contamination and minority carrier life time degradation are avoided.

(h) Graphoepitaxy:

Graphoepitaxy is a process of imposing long range order on the in-plane orientation of laser crystallized silicon grains by etching suitable grooves in the underlying insula-

tor substrate. Grooves of various shapes give different crystallographic orientation[10].

(i) Laser Assisted Crystallization Of Polysilicon Layer:

Polysilicon films formed by chemical vapour deposition (CVD) are a potentially important material for device fabrication. However, the relatively small grain size obtained under normal growth conditions makes device fabrication unfeasible since the grain boundaries usually determine the transport properties of the film. PN junction diodes fabricated on polysilicon exhibit a minority carrier life time on the order of 20psec[8] and MOS transistors fabricated on such films also exhibit poor electrical characteristics[9]. However, if the polysilicon layer is irradiated with high power laser light a tremendous improvement in the electrical characteristics of the polysilicon film is obtained[7-12]. As has been shown in the present work, an electron field effect mobility as high as 500 cm²/V-sec is possible in a laser crystallized polysilicon layer and MOS transistors with good characteristics can be fabricated.

2.5 Conclusion:

With the aforementioned applications of laser in the device processing, it is obvious that the importance of lasers to other areas of device fabrication steps has been increasing. Since this research work is concerned with the

laser assisted crystallization (LAC) and subsequent characterization of MOS transistors, fabricated on the crystallized polysilicon layer, the mechanism and parameters involved in LAC have been dealt with in detail in the next chapter.

CHAPTER-3

LASER ASSISTED CRYSTALLIZATION-MECHANISM AND EXPERIMENTAL SET-UP

3.1 Introduction

This chapter deals with the mechanism of laser assisted crystallization, the heat flow equation and the experimental set-up. A comparison of furnace annealing with laser annealing has been made and the advantages of the latter over the former have been pinpointed. Heat equation for the laser annealing has been solved and temperature-time and temperature-depth profile has been plotted. One of the critical parameters, the laser beam spot size, for laser crystallization has been plotted with respect to the distance of the focussing lens from the wafer being crystallized.

3.2 Laser-Assisted-Crystallization (LAC):

The common feature of all the conventional crystal growing techniques is that they all involve the need for a single crystal to start with--in Czochralski and Float zone techniques, the seed and in the vapour phase epitaxy, the single crystal substrate. On the contrary, laser assisted crystallization (LAC) starts without any need of a single crystal seed or a crystalline substrate. Substrates such as, silicon dioxide, quartz and graphite, can be used and the polycrystalline silicon deposited on these substrates is turned into single crystal silicon using laser beams.

Two distinct mechanisms have been identified for laser assisted crystallization of polycrystalline material. Liquid phase regrowth has been found to predominate for high power pulsed laser irradiation of very short duration (<1 microsec). Here the near surface layers of the substrate locally melt to a depth beyond the amorphous layer and recrystallization proceeds epitaxially on the underlying substrate during rapid refreezing. The second mechanism applies to low laser powers obtained from continuous wave (cw) lasers and lasting for relatively longer times (of the order of millisecond). This is called solid phase regrowth in which the laser beam raises the local surface temperature sufficiently to induce complete solid phase epitaxial regrowth of the amorphous layer in a manner analogous to furnace annealing. These two mechanisms of LAC examined in detail below.

3.2.1 Liquid Phase Regrowth-Pulsed Laser Annealing

After pulsed laser annealing of amorphous silicon, it has been found by Rutherford Backscattering Spectra (RBS) measurements [11] that there is a substantial dopant redistribution during recrystallization and the regrown surface morphology contains a prominent ripple structure [12]. Both these observations strongly suggest that the crystallization proceeds by a melt regime. The maximum growth rate in the silicon solid phase is about 10 Å/s just below the melting

point. For time intervals comparable with the laser pulse duration (20-100ns), the regrown film thickness would be only a few Angstroms as contrasted with the observed annealing of 5000A thick amorphous layers using pulsed lasers. Furthermore, assuming a solid phase diffusivity of 10^{-10} cm²/s, suggests that a broadening of the dopant profile of only about $1 \pm 1\text{\AA}$ [13] would occur, which is meaningless. Growth rates as high as 10 A /s are obtained in liquid phase epitaxy and the diffusion coefficients in liquid are of the order of 10^{-4} cm²/s or higher [13]. Hence these facts rule out the possibility of a solid phase regrowth during pulsed laser annealing.

In situ time resolved reflectivity measurements [19-20] have shown that just after a threshold energy, melting does indeed occur; the reflectivity is increased during the dwell time of the pulse, and the layer remains molten for about 1 microsecond following the pulse [21]. Fig 3.1 shows the change in reflectivity as a function of time for pulsed laser annealing. At time t_1 , a sharp transition in phase is evident by an increase in the reflectivity. This enhanced reflectivity remains constant until time t_2 at which it reduces again reaching a new steady state value at time t_3 . Reflectivities at time t_1 and t_3 are not same because of the different crystalline structure of the substrate at these times.

Fig 3.1 Change in reflectivity as a function of time [21].

Fig 3.2 Reflectivity as a function of laser annealing power for cw annealing [20].

The threshold energy density required for annealing via a phase transition from amorphous to liquid to crystalline has been found to be $2.5 \pm 0.2 \text{ J/cm}^2$ for silicon implanted silicon [22]. A similar threshold for annealing of arsenic implanted silicon has been found to be $2.7 \pm 0.2 \text{ J/cm}^2$. After the threshold energy has been reached, a complete defect free recrystallized layer appears.

3.2.2 Solid Phase Growth-cw Laser Annealing:

In contrast to the pulsed laser duration, the dwell time for cw laser annealing is normally of the order of several milliseconds, and even for a surface temperature of the order of 1000 C, normal diffusion broadening of the dopant profile is not expected and indeed not observed. By monitoring the reflectivity during annealing and examining the channeling spectra, Austen et al [20] have shown that for cw annealing, existence of a liquid layer is neither necessary for, nor detrimental to, good annealing. Their result of reflectivity vs laser power is shown in Fig 3.2. At point a, reflectivity goes through a peak suggesting constructive interference between the regrowth interface and the front surface of the crystal. Between point c and d a large increase in reflectivity is observed which shows the existence of a liquid layer. The continuous nature of the reflectivity increase between points c and d indicates that the liquid layer grows in thickness and in extent on the surface as the

laser power is increased.

The solid phase regrowth proceeds at a moving crystalline-amorphous interface and the rate of regrowth depends on the anneal temperature via a single stage activation process. The rate of regrowth can be represented as

$$V = V_0 \cdot \text{EXP} (-E_a/KT) \dots\dots\dots (3.1)$$

where, $V_0 = 10^7$ A/s and $E_a = 2.35\text{eV}$. Equation (3.1) can be used to calculate the temperature required to grow a particular layer of amorphous silicon for the dwell time of the cw laser beam spot on the substrate. It has been found that a temperature $> 900^\circ\text{C}$, is necessary to completely regrow an amorphous layer. This, of course, varies with the type of crystallinity of the layer to be grown.

3.2.3 Laser Annealing vs Furnace Annealing:

As explained in the previous section, cw laser annealing, like furnace annealing proceeds through solid phase epitaxy characterized by a single activation energy Arrhenius type growth as given by equation (3.1). For furnace annealing regrowth takes place at temperature $> 550^\circ\text{C}$ [5] and regrowth quality depends on time and temperature.

The parameters controlling cw laser annealing are power and dwell time, scanning speed and substrate temperature. No threshold energy is involved. In contrast, single crystal recovery occurs in pulsed laser annealing above a threshold energy, and the substrate retains its polycrystalline nature below the threshold. For both, furnace and cw annealing regrown quality has been observed to be dose dependent[5]. High doses regrow poorly whereas for low implant doses, the regrowth rate increases with dose. No dose dependence has been found for pulsed laser annealing. Similarly, cw laser and furnace annealing show an orientation dependence, with $\langle 111 \rangle$ silicon regrowing poorly with extended defects in the regrown layer. Best regrowth occurs for $\langle 100 \rangle$ silicon. Again pulsed laser annealing has not shown any orientation dependence[5]. Although cw laser annealing results in a lower dislocation density than furnace annealing, neither gives a defect free annealed layer, whereas for pulsed laser annealing an extended defect free layer appears. Below the solid solubility limit and for a temperature $< 850^\circ\text{C}$, no significant dopant redistribution has been found for furnace annealing, though normal diffusion occurs above 850°C . Above the solubility limit, grain boundary outdiffusion and "push-out" occurs. The same applies for cw laser annealing. Pulsed laser annealing, on the other hand, always shows dopant redistribution[19-21] within the melt.

Laser annealing as compared to furnace annealing provides a means of 'cold processing'. The main features of laser crystallization are--(1) heating and cooling can take place in microseconds rather than hours as in furnace annealing; (2) heating can be limited in depth to the active surface layers which are of interest in device fabrication and (3) heating can be localized to only those areas requiring thermal processing rather than over the entire wafer surface. The advantages accruing from the short time involved in laser annealing are--greatly reduced probability of contamination; reduced changes in dopant profile; no change in bulk properties and production of non-equilibrium structures. The feature of localized heating in laser annealing has several advantages--viz, heating itself has become a maskable operation in device processing; localized heating can remove the dependence of the process sequence on the temperature of the operation, and no significant distortion or warping of the wafer occurs due to the localized nature of heating.

3.3 Laser Solid Interaction And The Heat Flow Equation

The important parameters for laser crystallization of amorphous and polycrystalline silicon are the laser beam power and the spot dwell time, defined as the diameter of the beam divided by the scanning speed. Both of these par-

ameters combine to determine the temperature profile in the layer being crystallized. A calculation of the temperature profile with depth is important, because regrowth quality depends on the temperature achieved throughout the polysilicon layer.

3.3.1 The Heat Equation:

The thermal effects induced by the laser can be described by the usual heat flow equation with a source term to include light absorption. If the laser beam spot is large enough compared to the depth of the layer to be regrown, which is usually the case, and if the laser beam spot is uniform in the cross plane, the heat flow equation can be described by the well known one dimensional expression:

$$C \cdot \rho \cdot \frac{\partial T}{\partial t} = I(z,t) \cdot \alpha + K \frac{\partial^2 T}{\partial z^2} \quad \dots\dots\dots (3.2)$$

where, C is the heat capacity, ρ is the mass density, α is the absorption coefficient, k is the thermal conductivity and I is the laser light power density inside the specimen, which is a function of both time and depth. The steady state solution and the time dependent decay of temperature are derived below.

3.3.2 Steady State Solution:

For cw laser crystallization, since the dwell time is large compared to the time for heat diffusion, it can be assumed that as long as the laser beam spot remains at a particular place on the wafer, a steady state situation has been reached. Furthermore, assuming no phase change during regrowth, equation (3.2) can be rewritten as:

$$K \frac{d^2 T}{dz^2} = -\alpha \cdot I(z) \quad \dots\dots\dots (3.3)$$

and,

$$I(z) = (1-R) \cdot I_0 \cdot \text{EXP}(-\alpha z) \quad \dots\dots\dots (3.4)$$

where R is the reflectivity of the silicon surface I_0 is the incident laser power density. The boundary conditions are given by

$$T(a, t) = T_0 \quad \dots\dots\dots (3.4.a)$$

$$\frac{\partial T}{\partial z}(0, t) = 0 \quad \dots\dots\dots (3.4.b)$$

Condition (3.4.a) means that far from the surface at $z=a$ ($>10\mu\text{m}$), the substrate is unaffected [21-22] and the temperature remains at the ambient temperature, T_0 . The condition implies no loss from the surface. Integrating the equation (3.3) with the above boundary conditions, the temperature profile is given by:

$$T(z) - T_0 = \frac{(1-R) \cdot \alpha \cdot I_0}{K} + \frac{(1-R) \cdot I_0 \cdot \text{EXP}(-\alpha a)}{K} - \frac{(1-R) \cdot I_0}{K} \cdot z - \frac{(1-R) \cdot I_0 \cdot \text{EXP}(-\alpha z)}{\alpha K} \quad \dots\dots\dots (3.5)$$

and the surface temperature is given by

FIG.3.3 Temperature variation with depth,normal to the wafer
laser power density as a parameter.

$$T(0) - T_0 = \frac{(1-R) \cdot a \cdot I_0}{K} + \frac{(1-R) \cdot I_0}{K} [\text{EXP}(-\alpha a) - 1] \quad \text{.. (3.6)}$$

The steady state temperature distribution as given by equation (3.5) has been plotted in Fig.3.3. As is evident from the plot, for low laser power the temperature profile is almost flat. But as the power density is increased the steepness in the curves also increases as expected. For a laser power density of 0.1 MW/cm to 1.0 MW/cm the profile is almost flat till a distance of 0.5 micron. This observation is significant, because it ensures the uniformity of temperature throughout the polysilicon layer being crystallized. These results agree well with steady state solutions published elsewhere [19-22]. From the temperature profile, we can obtain the laser power density required to crystallize the polysilicon layer and depending on the available laser power the beam spot size can be decided. Furthermore, the curves also give the maximum thickness of polysilicon which can be crystallized for a given surface temperature and laser power density.

3.3.3 Temperature Decay:

When the source term in equation (3.2) is equated to zero and the same assumptions are made as in the previous section, the heat equation becomes

$$C \cdot \rho \cdot \frac{\partial T}{\partial t} = K \frac{\partial^2 T}{\partial z^2} \dots\dots\dots (3.7)$$

and the boundary conditions are

$$\left. \frac{\partial T}{\partial z} \right|_{z=0} = 0 \dots\dots\dots (3.7.a)$$

$$T = T_0, \text{ at } z = a \dots\dots\dots (3.7.b)$$

The initial condition is given by

$$T(z,0) = f(z) \dots\dots\dots (3.7.c)$$

where $f(z)$ is given by equation (3.5) derived in the previous section. The temperature variation with time is obtained as

$$T(z,t) - T_0 = \sum_{n=1}^{\infty} A_n \cdot \cos(\lambda_n z) \cdot \exp(-\lambda_n^2 \cdot D^2 \cdot t) \quad (3.8)$$

And the surface temperature decay is given by

$$T(0,t) - T_0 = \sum_{n=1}^{\infty} A_n \cdot \exp(-\lambda_n^2 \cdot D^2 \cdot t) \quad \dots\dots\dots (3.9)$$

Equation (3.9) clearly shows that the surface temperature decays exponentially with time as the laser beam is removed from a position on the wafer. As t the temperature tends to T_0 , which is the substrate temperature. From equation (3.9) the quenching rate can also be found by differentiating it. The maximum quenching rate which occurs at time $t=0$ and at $z=0$, is given by

FIG. 3.4 (a-b) Surface Temperature Decay With Time (a) ; Maximum Quenching Rate (b)

$$\left[\frac{dT}{dt} \right]_{\max} = - \sum_{n=1}^{\infty} A_n \cdot \lambda_n^2 \cdot D^2 \quad \dots\dots\dots (3.10)$$

The negative sign in front of equation (3.10) shows that the temperature is decaying with time. The temperature decay and the maximum quenching rate have been plotted in Fig.3.4(a-b). As the laser power density increases the decay is delayed but it is steeper as is evident from Fig.3.4a. Fig.3.4b shows that even for a laser power density of 1.0MW/cm the maximum quenching rate is about 10^{10} DEG k/sec. This tremendous cooling rate of the wafer was found to induce stress in the silicon wafer being crystallized. A combination of low laser power density and higher ambient temperature was found to alleviate this problem of cooling induced stress.

3.4 Laser Assisted Crystallization Set-Up and Calculation of Spot-size

3.4.1 Experimental Set-up

The laser annealing set-up used in this research work consists of the Coherent Model-18, cw Argon Ion laser, optical

FIG 3.5: Laser Crystallization Set-Up

elements such as mirrors to reflect the laser beam and lenses to focus the beam at a spot, and a microprocessor controlled X-Y driver stage for scanning the silicon wafer. The horizontal beam coming out of the laser aperture was reflected downwards by a mirror placed at 45 degrees with the horizontal. It then passed through a lens of focal length 50 mm and focussed to the silicon sample to be crystallized. A quartz plate was used to cover up the sample which was held on the sample holder on a vacuum chuck placed on a platform driven by X-Y motors. Fig.3.5 shows the optical arrangement. For controlling the X-Y motors, the MOSTEK 6502, microprocessor was used. A detailed description of the set-up can be found in Ref[23].

The software for the control, original to the author, has the feature of driving the X-motor for a fixed distance, then stopping for a few seconds before giving a shift to the Y-motor, and then reversing the direction - thus completing one scan period. The program parameters are the driving frequency, the Y-shift and the direction reversal, which can be used for suitable reverse multiple scanning. The block diagram of the system is shown in Fig.3.6.a. Fig.3.6.b shows the waveforms generated by the software. The flowchart depicted in Fig.3.7 shows the algorithm for the program, which is given in Appendix-A. Counter M1 counts the number of pulses given to the X or Y motors. M2 checks whether one

FIG.3.6(a):X-Y Control Unit for Scanning the Wafer

FIG 3.6(b): Waveforms Generated By The Software

Fig 3.7 Flowchart for the Microprocessor Program to control X-Y driver stage.

scan period (one forward and one reverse scanning) has been achieved or not. Counter M3 holds the total number of scan periods to be done, thus giving control over the width band scanned on the silicon wafer. After one scan period, the software starts all over again initializing the counters M1 and M2. A delay of 0.5 seconds for the mechanical relay to operate without fail was thought to be necessary and has been incorporated in the software.

In addition to the optical and control set up, there was additional facility provided to heat up the substrate to a desired temperature with the aid of a temperature controller. Heating the silicon sample to higher temperature helps to relieve the thermal shock received by the wafer during laser crystallization. The effect of laser annealing and subsequent device fabrication using the set up described above is described and discussed in the next chapters.

3.4.2 Calculation of Spot Size:

As shown in the section 2.3.3 chapter-2, if a Gaussian spherical wave with the complex radius of curvature q_1 , passes through a combination of optical elements, the complex radius of curvature of the emergent Gaussian wave is given by

$$q_2 = \frac{A \cdot q_1 + B}{C \cdot q_1 + D} \dots\dots\dots (3.11)$$

where A,B,C,D are the elements of the ray matrix. Hence the problem of finding the spot size and the radius of curvature boils down to finding one complex number, q_2 , which contains both the spot size and the radius of curvature. Taking an average wavelength of 0.5 micron in the laser beam and an average beam diameter of 1.8mm [24], the Rayleigh range as defined by equation (2.19), repeated here for convenience,

$$Z_r = \frac{\pi \cdot W_0^2}{\lambda} \dots\dots\dots (3.12)$$

turns out to be approximately 5 meters. Hence, the laser beam can be thought of as being collimated over the distance between the beam aperture and the silicon wafer, because this distance was less than 5 meters in the experimental set up. Thus instead of going through the rigorous approach, a good estimate of the spot size can be made by exploiting the fact of large Rayleigh range and using the equation [18]

$$d_0 = \frac{4 \cdot f \cdot \lambda}{\pi \cdot d} \dots\dots\dots (3.13)$$

where, d is the diameter of the incident beam. Finding d_0 from (3.13) and using equation (2.18), repeated here for convenience

$$W(z) = W_0 \cdot \left[1 + \left(\frac{z}{Z_r} \right)^2 \right]^{1/2} \dots\dots\dots (3.14)$$

gives for large Z , $W(z)$ Z as expected and explained in sec-

Fig 3.8 Sppt size of the laser beam vs vertical distance of the focussing lens from the wafer.

tion 2.3.2. A computer calculation using (3.13) and (3.14) is given in Appendix-B. The spot size is plotted in Fig.3.8. The plot shows the linear nature of the spot size at large distances and parabolic variation at shorter distances. Experimentally, the beam was completely focussed on the silicon wafer and a single line was scanned. The width of the line was measured to be 20.0 microns. The computer calculation shows that d_0 is equal to 17.69 microns which is in good agreement with experimental observation.

3.5 Conclusion:

The theoretical results obtained in this chapter and the laser crystallizing set up described as earlier will be used for arriving at an optimum set of crystallizing parameters used for crystallization of the polysilicon layers on different types of substrates.

CHAPTER-4

Laser Crystallization Of Polysilicon Layer

4.1 Introduction:

This chapter presents experimental results on laser crystallization of chemical vapour deposited (CVD) polysilicon layer. It starts with the characterization of the CVD polysilicon layers. The laser annealing parameters used in the annealing of the polysilicon are then discussed. The layers are characterized via etching techniques and diodes fabricated in the layers.

4.2 Characterization Of Deposited Polysilicon Layers:

Deposition of polysilicon on oxidized silicon wafers is an important process in the fabrication of silicon gate and shielded silicon gate MOSFET's, two phase CCD's, and dielectrically isolated circuits. The advent of the laser into the device processing areas opens the possibility of crystallizing the deposited polysilicon layer making it suitable for fabrication of useful devices. Among the various means by which the polysilicon can be deposited chemical vapour deposition is usually the choice. CVD via silane pyrolysis can be done either in a hydrogen or an inert gas atmosphere.

Furthermore, the polysilicon can be doped during deposition which provides an alternative to the ion-implantation used for the introduction of impurities[11]. This saves time and a step which is more complicated than doping during deposition of the polysilicon layer. The deposition conditions and the apparatus used are described below.

4.2.1 Deposition Of Polysilicon Layer:

A horizontal epitaxial reactor with an RF generator for substrate heating was used to deposit the layers for this study. The susceptor material was silicon carbide-coated graphite on a tilted quartz jig. The carrier gases used were hydrogen and nitrogen. The starting wafers were <100> p-type and n-type with resistivities in the range of 1.8-2.6 ohm-cm. A 1 micron thickness of silicon dioxide was grown at 1200 C by conventional thermal oxidation on five of the p-type wafers. Before the polysilicon deposition the standard wafer cleaning step was followed. The wafers were then introduced in the horizontal epitaxial reactor for polysilicon deposition. Before the gas flow was initiated, an HCL etch at 1150 C for 30 sec was performed in the epitaxial reactor to remove oxide layers, if any, from the unoxidized samples. This step is critical and it is thought to be essential for ensuring a uniform polysilicon layer thickness. After this etching step the gas flows were resumed with the

ratio of diborane to silane in the gas phase kept at 1.9×10^{-6} . The temperature of polysilicon deposition was 700 C and the rate of deposition .016 micron/min. Characterization of the polysilicon layer follows next.

4.2.2 Characterization Of As-deposited Polysilicon:

The thickness of the polysilicon layer was estimated to be 0.45-0.5 micron by counting the optical interference fringes on the back side of the oxidized silicon wafers. A countercheck was done by bevelling and properly staining (chromium oxide and HF) the p-type doped polylayer on the n-type substrate and counting the interference fringes. This method also indicated the polysilicon layer thickness to be in the range .48-.5 micron. Since no difference is found in the deposition rate of polysilicon on silicon and on silicon dioxide[25] in the temperature range of 680-750 C, the thickness of the poly-layer on both- the oxidized and unoxidized samples can be taken to be in the range .48-.5 micron. The total density of dopant atoms introduced in the growing polysilicon film was calculated by gas flow considerations to be 1.2×10^{16} . For a gas phase ratio of diborane to silane of 1.9×10^{-6} , at 680 C, the acceptor concentration has been reported [26] to be approximately 1×10^{16} . Hence the poly-layer can be assumed to be doped with a boron concentration of 1.2×10^{16} at the deposition temperature of 700 C. This value

Fig. 4.1 a. Optical photomicrograph of polysilicon on single crystal silicon showing crystallites connected to each other via a thin neck; X1000

Fig 4.1.b: Optical photomicrograph of polysilicon on single crystal silicon showing finger-like grains resulting from localized hot spots on the susceptor in epitaxial reactor; X1000

Fig.4.1c: SEM photomicrograph of the same area as shown in Fig.4.1.b;X2000.

of dopant concentration was taken for all the MOS characterization parameters reported in chapter-5.

The physical examination of the polysilicon layer showed a smooth and mirror-like surface on both the oxidized and unoxidized samples, though the polysilicon layer on the oxidized sample looked somewhat smoother due to smaller grain size as compared to that on the unoxidized silicon wafer. In order to determine more closely the grain structure of the polysilicon layers, both optical and scanning electron microscopic (SEM) examinations were conducted. To delineate the grain boundaries, a Secco etch (one part of potassium dichromate and two part of hydrofluoric acid) [27] was used. A small quantity of water was added to make the etch act faster. The optimum etching time was found to be 15-20 seconds. After etching the control samples, they were examined microscopically. Figs 4.1(a-c) show photomicrographs of polycrystalline silicon on single crystal silicon. As depicted in fig 4.1.a, there are crystallites seen all over the silicon wafer with no particular orientation in any preferred direction. It was difficult to establish the size of these crystallites, because they were not isolated, one being connected to the next via a thin neck. When the sample was scanned, some relatively large, finger-like grains were observed as shown in fig 4.1(b-c). Their density was quite low and they are thought to result from the presence of lo-

calized hot spots on the susceptor in the epitaxial reactor. The largest such structure had a dimension of 2.5×20 microns.

The polycrystalline structure observed on the oxidized samples had more interesting features as shown in Figs. 4.2(a-c). Instead of having bigger crystallites as in the case of poly on single crystal silicon, the poly on oxide had a dendritic structure. The small nucleation sites can be identified very clearly from where dendritic growth is initiated in all directions. Here again there is no preferred direction of growth. The average distance between nucleation sites is about 50 microns. This dendritic growth in the case of polysilicon on oxide is thought to be a result of low surface diffusivity of the nucleation centres on the oxide as compared to that on the single crystal silicon. Due to the low diffusivity, and relatively larger growth rate the nucleation process continues at and around the nucleation sites once formed initially and there is no further movement of these centers. Hence two or more dendritic structures do not coalesce to form bigger crystallites as in the case of polysilicon on single crystal silicon.

Fig. 4.3(a-b) show SEM photomicrograph of polysilicon on oxide-untreated with Secco etch 4.3.a and treated for 8secs as in 4.3.b. These photographs were taken in a slightly de-

Fig.4.2.a: Optical photomicrograph of polysilicon on silicon dioxide showing nucleating sites and dendritic growth X625

Fig.4.2.b: SEM photomicrograph of polysilicon on silicon dioxide; X400

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Fig. 4.2.c: SEM photomicrograph of polysilicon on silicon dioxide; X400 the glassy appearance in the background is due to the silicon dioxide.

Fig. 3.a: SEM photomicrograph of polysilicon on oxide, untreated with Secco etch; X10,000.

fectured area to show the few large Si grains protruding above the surface which were occasionally seen and which represent the only obvious defect on the surface. A water mark on the sample or an unclean wafer is thought to be the reason for the presence of these large Si grains. Similar protruding grains on boron doped polysilicon grown at 650 C on thermal silicon dioxide have been observed by Cowher, et al [26].

For electrical characterization, resistivity measurements were performed using the four point probe method. The resistivity of the poly layer on silicon dioxide was found to be difficult to measure using the four point probe. Hence spreading resistance was measured on the oxidized samples using a two probe technique. Spreading resistance was found to lie between 40-50 MegOhm which corresponds to a resistivity of 15-16 KOhm. On the other hand, the resistivity of the poly layer on the single crystal silicon as determined by the four point probe was found to be 120-125 Ohm-cm. This marked difference in the resistivities of the polysilicon layer on the two types of substrates is thought to be as a result of the difference in the crystalline structure of the layer and, in the case of polysilicon on single crystal silicon, sampling of the material by the four point probe underneath the polysilicon layer.

To see the effect of laser induced redistribution, if

Fig.4.3.b: SEM photomicrograph of polysilicon on oxide, etched for 8secs X10,000.

any, of impurities after laser crystallization, anodic oxidation [28,29] was used to profile the as deposited polysilicon layers. The electrolytic solution used was prepared by dissolving 2.02 gm of potassium nitrate in 500 cc of ethylene glycol to get a solution of strength 0.04N. 2%, by volume, DI water was added to speed up the oxidation. A constant voltage source was used to polarize the electrodes. A cycle of anodic oxidation, oxide thickness measurement, etching away the grown oxide and resistivity measurement showed an almost constant impurity profile throughout the polysilicon layer.

4.2.3 Crystallization of the Polysilicon layer:

Before crystallizing the polysilicon layer for final device fabrication, some control samples were chosen for characterization of the laser crystallization process and the quality of the crystallized layer. The laser crystallizing apparatus as described in section 3.4.1 was used for all the experiments. The parameters emphasized were the power density of the incident laser beam and the substrate temperature, which was controlled by the temperature controller. The power density was varied by defocussing the converging lens. The scanning speed was kept constant at 1cm/sec. The line-to-line overlap varied with the spot size. The number of steps in the Y-direction after one scanline in X-direction was kept at 2, which was equivalent

to 25 microns. The spot size was varied from 18 microns to 200 microns in increments of 20 microns. Several 6mm wide crystallized bands were formed on all three types of samples- polysilicon on P-type silicon, polysilicon on N-type silicon and polysilicon on silicon dioxide. After forming the bands, the samples were microscopically (optical and SEM). Since the polysilicon layer was doped P-type, a dotted (1mm dia) metallization pattern was formed on the N-type sample to study the change in the polysilicon-substrate diode characteristics as laser power density was varied.

4.2.4 Characterization of Crystallized Polysilicon Layers:

Figs.4.4(a-d) show the I-V characteristic of the crystallized P-type polysilicon layers on top of the N-type substrates. For comparison, the I-V characteristic of an uncrystallized polysilicon layer and the substrate is given in Fig.4.4.e. As can be seen from fig4.4.e--the current-voltage characteristic of this sample suggests that it behaves purely as a very high resistance. A marked difference in the reverse characteristics is seen as the spot size is varied from 74 to 180 microns, keeping the total laser power fixed at 14.5 Watts, Figs4.4(a-d). At higher power densities, (lower spot size) diode breakdown is characterized by a "soft" knee which is a result of the amorphosity

Fig.4.4(a-d): Forward and reverse i-V characteristics of P-type Polysilicon layer and N-type substrate; total laser power=14.5 Watts and varying spot size.

(a) SPOT-SIZE = 74 μm

(b) SPOT-SIZE = 109 μm

(c) SPOT-SIZE = 145um

(d) SPOT-SIZE = 180um

(e) Uncrystallized P-type Polysilicon on N-type substrate.

of the polylayer crystallized at high laser power density. Sharp breakdown (60 Volts) is observed at a spot size of 145 microns and a total laser power of 14.5 Watts. The same breakdown is observed at a spot size of 180 microns. From these observations, it can be concluded that a higher power density does not necessarily mean a good crystalline recovery. In fact as the optical and SEM microscopic examination will show later, at higher power densities, thermal etching of the material occurs and the polysilicon layer becomes even more amorphous than the as deposited layer.

For all cases there is an improvement in the reverse and forward characteristic as the spot size is increased from 74 to 180 microns. All that can be concluded from Figs 4.4 (a-c) is that the laser irradiation has brought about a marked decrease in the forward resistance as compared to that of the uncrystallized polysilicon (Fig 4.4.e). There is no "knee" voltage evident from the higher powers (lower spot size), however as can be seen from Fig 4.4.d, (180 micron spot size) the forward characteristic resembles that of a typical PN junction diode with a knee voltage of 0.7 volts. The reverse characteristic shows a sharp breakdown at 60 volts.

Results of microscopic examination of the crystallized polysilicon layers are shown in Fig. 4.5 (a-h). At higher power densities, the layer melts and evaporation also takes

place, as is evident from the spherical grain shape in Figs 4.5(a-b). In Fig. 4.5(b) where the spot size was 91 micron, grains are arranged in a longitudinal fashion whereas in Fig. 4.5(a) (spot size 109 microns) the grains are more random. This result (Fig. 4.5.b) is thought to be due to coalescence of two or more neighbouring grains when melting occurs followed by material flow. In Fig. 4.5(a) the grains retain their shape due to the lower power density, however, material removal through evaporation is still evident from the black areas in the centers of the grains. For highest power (18 micron spot size) a rectangular crack developed in the polysilicon layer, Fig. 4.5(c-d). Propagation of the heat wavefront is also visible due to a changed reflectivity and surface morphology. The scanned band, Fig. 4.5(c) shows warping and distortion of the surface due to material flow and thermal etching.

Figs 4.5(e-f) show the effect of crystallizing the polysilicon layer on single crystal silicon (lower band) and silicon dioxide (upper band). For the same power density, the polysilicon layer on silicon dioxide shows a greater warping of the surface (Fig. 4.5f). Microcracks are still visible on both types of samples, the density of these microcracks being much greater than that in Fig. 4.5(a-b). The difference in the surface morphology on the two types of samples is due to the different boundary conditions for the heat flow. The

Figs 4.5(a-h): Results of laser crystallization of polysilicon at laser power = 14.5 Watts and varying spot sizes.

(a) Polysilicon on single crystal silicon spot-size=91um X500

(b) Same as (a) spot-size=109um, X500

(c) Polysilicon on single crystal silicon spot-size=18um, SEM X800

(d) Edge View of (c) SEM X1000

(e) spot-size=40um X100 (f) same as (e) spot-size=25um
upper band: polysilicon on SiO₂; lower band: polysilicon on Si.

(g) Polysilicon on SiO₂,
spot-size=109um, X500

(h) Polysilicon on Silicon,
spot-size=180um, X1000

presence of the silicon dioxide layer between the polysilicon and the silicon substrate provides a reflecting boundary for the heat flow. Thus when the same power density is used for crystallizing the two types of samples, the one with the intermediate silicon dioxide layer is bound to show a different (and worse) surface morphology, since it retains the heat for a longer time. Fig 4.5(g) illustrates this point. The crystallizing parameters were the same for both 4.5(g) and 4.5(a), yet the average diameter of the spherical grains in the case of polysilicon on insulator is approx. 4 microns, whereas for the single crystal substrate it is approx. 10 microns. Furthermore, the crack propagation is much more severe in the former case than in the latter.

Fig 4.5(h) shows the surface of polysilicon on single crystal silicon after irradiating with laser beam at a spot size of 180 microns and treated with Secco etch. Long grains can be easily seen aligned in the direction of the scanlines. Except for the circular pits (delineated by the interference fringes) due to overetching by the Secco etch at some preferential sites such as water marks and other contaminants, the surface morphology is quite smooth and free from any structures as in previous Figs 4.5(a-f). The average size of such elongated grains is 3×30 microns. As was noted in section 4.2.2 in this chapter, the polysilicon layer deposited on silicon dioxide had a dendritic

structure(Figs4.2a-c)with no particular orientation. Even after crystallization, the crystalline recovery tends to form branch like structure as in Fig4.6(a). The tip-to-tip length of these branches is approx.40 microns (the spot size in this case was 200 microns). Fig4.6(b) shows the columnar growth of the polysilicon layer on silicon dioxide after laser irradiation,which emphasizes the fact that the growth occurs from the polysilicon silicon dioxide interface and proceeds upwards towards the surface. Crystallites extend through the whole thickness of the polysilicon layer.

To find the change in the dopant profile,if any,anodic oxidation was performed as described earlier(section4.2.2). The resistivity of the sample crystallized at a total laser power of 14.5 Watts and a spot size of 180 microns,which also gave the largest grain sizes,was measured by the four point probe. There was 80-85% reduction in resistivity from the as-deposited case. Furthermore, this experiment showed no redistribution of impurities after laser irradiation which is supported by other researchers[6-14]for the case of cw-laser crystallization.

4.3 Conclusion:

The parameters for laser crystallization found in this chapter have been used for crystallizing the polycrystalline

Fig 4.6 (a) SEM Photomicrograph of polysilicon on SiO₂,
spot-size=200um, X500.

Fig 4.6 (b) same as (a), X7000, edge view showing columnar
growth of crystals, spot-size 200um.

silicon layer deposited on various substrates. The characteristics of MOS transistors fabricated on laser crystallized polysilicon have been discussed in the next chapter.

CHAPTER-5

CHARACTERIZATION OF MOS TRANSISTORS FABRICATED ON
LASER CRYSTALLIZED POLYSILICON

5.1 Introduction:

With the aid of the laser crystallization procedure discussed in the previous chapter, metal-oxide-semiconductor transistors with channel length as short as 2.5 micron and as long as 50 micron were fabricated and successfully tested. The results obtained from the characteristics of MOS transistors fabricated on laser crystallized polysilicon layer on top of single crystal silicon and silicon dioxide and those fabricated on single crystal silicon substrates were compared. To explain the results, a theoretical I-V characteristic was obtained by a combination of process simulation using SUPREM-II and circuit simulation using SPICE2F.1. All these results are discussed in this chapter.

5.2 Fabrication Process Steps For MOST's:

The flowchart of the MOST fabrication process steps

FIG.5.1 Flowchart Of The MOST Fabrication Steps

starting from substrate preparation is given in Fig.5.1. As can be seen from the figure, there are two fundamental deviations from the normal MOST fabrication steps. The first one relates to the use of laser crystallized p-type polycrystalline silicon layer. Secondly, rather than thermally growing the field oxide, it has been deposited in order not to consume all the polysilicon layer during field oxide growth. After the device well is etched and gate oxidation done the polysilicon for the gate is deposited. Following this step, and using the mask described in ref[35] the standard Carleton University N-channel MOST process[30] was employed.

5.3 Testing and I-V Characteristics:

The MOS devices were probed and I-V curves plotted using the Tektronix Type 576 curve tracer. The output characteristics depicting the relationship between the source-drain current (I_{ds}) and the drain-source voltage (V_{ds}) for various gate source voltages (V_{gs}) are given in Fig 5.2(a-i). For each channel length, there are three sets of curves relating to devices fabricated on (1) laser crystallized polysilicon on single crystal silicon; (2) laser crystallized polysilicon on silicon dioxide; and (3) single crystal silicon. To show the effect of channel length on the output characteristics, devices were chosen with channel lengths of .50 microns (a-c); 7 microns (d-f) and 2.5

microns(g-i). For comparison, using a combination of SUPREM-II and SPICE2F.1, theoretical I-V characteristics were obtained. The computed curves are given in Fig.5.3(a-c). A detailed analysis of MOST parameters is given in the following sections.

5.4 Threshold Voltage:

The appearance of a useful conducting channel in a standard MOS transistor requires the formation of an inversion layer near the surface of the semiconductor. The formation of an inversion layer requires considerable distortion of the energy bands within the semiconductor by the field-effect voltage. It is accompanied by a depletion layer between the neutral bulk and the inversion layer. Once the inversion layer is formed, however, further increases in the magnitude of the field-effect voltage will induce more charge in the inversion layer but will have little effect on the depletion layer width. For this reason, the drain current gate voltage characteristic of an MOS transistor is linear once the inversion layer is formed, i.e., once the 'threshold voltage' (V_t) is surpassed. Therefore, the major influence of the semiconductor material will be reflected in the threshold voltage. The threshold voltage is given by [30]

Figs 5.2(a-i) Output characteristics of MOS transistors fabricated on various type of substrates

(a) polysilicon on single crystal silicon, $W=L=50\mu m$

(b) polysilicon on SiO_2 , $W=L=50\mu m$.

(c) single crystal silicon, $W=L=50\mu\text{m}$.

(d) polysilicon on single crystal silicon, $W=50\mu\text{m}$; $L=7\mu\text{m}$.

(e) polysilicon on SiO₂, W=50um; L=7um.

(f) single crystal silicon, W=50um; L=7um.

(g) polysilicon on single crystal silicon, $W=50\mu m$; $L=2.5\mu m$.

(h) polysilicon on SiO_2 , $W=50\mu m$; $L=2.5\mu m$.

(i) single crystal silicon, $W=50\mu\text{m}$;
 $L=2.5\mu\text{m}$.

Fig 5.3(a-c) Theoretical I-V characteristics using a combination of SUPREM-II and SPICE
 (a) $W=L=50\mu\text{m}$; (b) $W=50\mu\text{m}, L=7\mu\text{m}$;
 (c) $W=50\mu\text{m}, L=2.5\mu\text{m}$.

$$V_t = \phi_{ms} - \frac{Q_{ss}}{C_o} + U_s - U_B - \frac{Q_B}{C_o} \dots\dots\dots (5.1)$$

where ϕ_{ms} is the metal semiconductor work function difference, Q_{ss} is the semiconductor-insulator interfacial charge, U_s is the surface potential at the onset of inversion layer, U_B is the Fermi potential in the neutral region, Q_B is the charge in the depletion layer and C_o is the oxide capacitance per unit area.

The major effect of the semiconductor material will be reflected through Q_B in equation (5.1). The threshold voltage measured on the laser crystallized polysilicon MOS devices were 1.5 Volts and 1.4 Volts for devices with channel lengths 50 microns and 7 microns respectively and 0.85 Volts and 0.8 Volts for devices fabricated on single crystal silicon with approximately the same substrate doping of approx. $1E16/cm^3$. Since the devices were fabricated following the same process steps, the substantial difference in the threshold voltage is thought to be due to the imperfect crystallization of the polysilicon during laser irradiation. For insight into the problem, it is worthwhile to examine the effect of bulk defect levels on the threshold voltage.

Fig 5.4 show the energy band diagram of a P-type semiconductor with defect levels above (fig.5.4.a) and below (fig.5.4.b) the Fermi level in the bulk. In Fig.5.4.a, the

deep defect acceptor level lies above the Fermi level in the neutral bulk region, i.e., $N_a > N_t$. Thus the defect giving rise to this level is uncharged. The depletion layer may be considered to consist of two parts, viz. from X_1 to X_d where the defect level lies above the Fermi level and the defects are neutral and charge density in this region is just qN_a (assuming complete depletion), and from $X=0$ to X_1 where the defects are negatively charged the defect level lying below the Fermi level in this region. The net charge density in this region is $q(N_a + N_t)$. Solving Poisson's equation in the two regions and joining the solutions at $X=X_1$ gives X_1 and X_d . Then Q_B is given by:

$$Q_B = q(N_a + N_t) \cdot X_1 + qN_a (X_d - X_1) \\ = [2\epsilon q \{N_a (U_B - U_S) + N_t (U_t - U_S)\}]^{1/2} \dots\dots\dots (5.2)$$

where U_t is defect energy level. In this case the Fermi potential of the neutral region will be same as in the case of single crystal silicon, assumed to be defect free for the sake of comparison, for which Q_B is given by:

$$Q_B = [2\epsilon q N_a (U_B - U_S^*)]^{1/2} \dots\dots\dots (5.3)$$

A comparison of equations (5.2) and (5.3) shows that for a P-type substrate Q_B will be higher in the imperfectly crys-

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Fig 5.4(a) Energy band diagram showing a defect level above Fermi level.

Fig 5.4(b) Energy band diagram showing a defect level below Fermi level.

tallized polysilicon than than in the case of defect free single crystal silicon for an acceptor type defect level. This fact will be reflected in a higher value of threshold voltage found for MOS devices fabricated on laser crystallized polysilicon.

The case shown in Fig 5.4(b) is simpler than the that discussed above. Here the defect level is below the Fermi level both in the bulk and the depletion region and can be treated as an additional shallow acceptor level. Q_B is given by:

$$Q_B = q(N_a + N_t) \cdot X_d$$

$$= [2\epsilon q (N_a + N_t) (U_B - U_S)]^{1/2} \quad \dots (5.4)$$

The Fermi potential, now, is given by:

$$U_B = U_{B0} + \frac{KT}{q} \cdot \ln \left(1 + \frac{N_t}{N_a} \right) \quad \dots (5.5)$$

where U_{B0} is the Fermi potential in a defect free material. As depicted by equation (5.4), Q_B again increases with the presence of an acceptor type defect level. Hence V_t will be found to be greater than that found for the single crystal case. To get an idea about the magnitude of the defect level density, consider the case as shown in Fig 5.4(a).

Assuming that the defect level is very close to the intrinsic level, so that $U_t \approx 0$, gives from equation 5.2,

$$Q_B = [2\epsilon q \{N_a (U_B - U_S) + N_t (0 - U_S)\}]^{1/2} \\ = [2\epsilon q \{N_a (U_B - U_S) - N_t \cdot U_S\}]^{1/2} \quad \dots\dots (5.6)$$

From equation (5.1) the threshold voltage is given by,

$$V_t = \phi_{ms} - \frac{Q_{ss}}{C_o} + U_S - U_B - \frac{Q_B}{C_o} \quad \dots\dots\dots (5.7)$$

When deep acceptor type defect levels are present, the difference in the threshold voltage from that of a device fabricated on single crystal silicon is given by,

$$\Delta V_t = \frac{[2\epsilon q \{N_a (U_B - U_S) - N_t U_S\}]^{1/2} - [2\epsilon q \{N_a (U_B - U_S)\}]^{1/2}}{C_o} \\ = \frac{[2\epsilon q \{2|\phi_p| N_a + N_t |\phi_p|\}]^{1/2} - [4\epsilon q N_a |\phi_p|]^{1/2}}{C_o} \quad \dots\dots (5.8)$$

where ϕ_p is the Fermi potential in the semiconductor bulk defined by,

$$\phi_p = \frac{kT}{q} \ln \left(\frac{N_a}{n_i} \right) \quad \dots\dots (5.8.a)$$

For a channel length of 50 microns, the threshold voltage measured on the single crystal silicon substrate was 0.85 volts while that for a laser crystallized polysilicon substrate was 1.5 volts. Putting the values of $|\phi_p|$, N_a , q and C_o in equation (5.8) gives,

$$1.6E16 = 0.85E16 + N_t | \phi_p | \dots\dots (5.9)$$

From equation (5.9) the concentration of the deep defect levels based on the threshold voltage difference calculation is found to be $2E16/cm^3$. A similar calculation of defect density for the device with channel length of 7 microns gives a value of $1.77E16/cm^3$ which is 12% less than that found for $L=50\mu m$.

From the above consideration, it appears that the substantial difference in the measured threshold voltage of MOS devices on laser crystallized polysilicon and single crystal silicon results from the presence of deep defect levels in the polysilicon bulk. Assuming the presence of shallow defect levels, a calculation using equation (5.4) and (5.5) suggests a defect density of $1.04E16/cm^3$ for the same observed threshold voltage difference for $L=50\mu m$. It is also interesting to note that the concentration of the defect levels is almost equal to the concentration of the boron impurity. This suggests the possibility that the crystallization phenomenon could start with the boron atoms as nucleating (crystallizing) sites. A program to determine whether a direct correlation exists between the defect density and the concentration of impurities is a possible area of fruitful research. Should it be determined that the defect concen-

tration depends on the concentration of boron impurities, then a substantial increase in defect density would be expected as device dimensions are shrunk and doping concentration increased as demanded by scaling laws. This would be accompanied by a substantial increase in the threshold voltage compared to that of the devices made on single crystal silicon. At some point, the decrease in the threshold voltage due to scaling might be compensated by an increase in the threshold voltage due to the increased defect density. This would have wide implications in logic circuits fabricated on laser crystallized polysilicon.

5.5 Channel Conductance (g_{ds})

Once the inversion layer has been formed after an application of gate voltage greater than the threshold voltage of the MOST, the output conductance is defined as [30],

$$g_{ds} = \left. \frac{\partial I_d}{\partial V_{ds}} \right|_{V_{gs}, V_{bs}} \quad \dots\dots\dots (5.10)$$

Using the I-V relationship in the nonsaturation region, the channel conductance has been found [30] to be,

$$g_{ds} = \frac{C_o \cdot \mu \cdot W}{L} \times \left[V_{gs} - V_x - V_{ds} - \left(\frac{-2\epsilon q N_a (V_{ds} - V_{bs} + \phi_p)}{C_o} \right) \right] \quad (5.11)$$

For very small drain to source voltages, ie $V_{ds} \rightarrow 0$ and $V_{bs} = 0$, this reduces to

$$g_{ds} \Big|_{V_{ds} \rightarrow 0} = \frac{C_o \cdot \mu \cdot W}{L} (V_{gs} - V_t) \quad \dots\dots\dots (5.12)$$

Fig 5.5(a) Channel conductance vs. gate voltage for single crystal silicon substrate; L=50micron

Fig 5.5(b) Channel conductance vs gate voltage for polysilicon on single crystal silicon substrate; L=50micron

Fig 5.5(c) Channel conductance vs gate voltage for polysilicon on silicon dioxide substrate; L=50micron

Fig 5.6(a) Channel conductance vs gate voltage for single crystal silicon substrate; L=7micron

Fig 5.6(b) Channel conductance vs gate voltage for polysilicon on single crystal silicon substrate; L=7micron

Fig 5.6(c) Channel conductance vs gate voltage for polysilicon on silicon dioxide substrate; L=7micron

Equation (5.12) shows the channel conductance to be linearly dependent on the gate to source voltage for small V_{ds} . The experimental results of channel conductance, measured at a drain voltage $V_{ds} = 0.1$ volts, for different gate voltages are given in Figs 5.5(a-c) and 5.6(a-c).

As is shown in figure 5.5(a-c), the channel conductance depends on V_{gs} as predicted by the theory-taking a decrease in field effect mobility for higher gate voltages into account. In the linear region, g_{ds} for laser crystallized polysilicon devices is 10% less than the g_{ds} of the devices fabricated in single crystal silicon. This can be explained in terms of a lower field effect mobility due to scattering effects by the grain boundaries in the laser crystallized polysilicon. A close examination of the curves shows that at higher V_{gs} , the decrease in channel conductance in the laser crystallized polysilicon devices is less than that for single crystal silicon devices for the same gate voltage. For example, at a gate voltage of 14 volts, there is a 9% decrease in g_{ds} for single crystal devices whereas the corresponding figure for laser crystallized devices is only 4%. Before attempting to explain this intriguing behaviour of g_{ds} with the increasing gate voltage, the existing theories used to explain surface mobility reduction at higher gate voltages, will be briefly reviewed.

There are two theories used to explain the behaviour of surface mobility at higher gate voltages. One is based on surface scattering, while the other is based on quantum mechanical considerations. Surface scattering consists of specular scattering, in which there is an elastic collision of the carriers at the Si-SiO₂ interface, and diffuse scattering which describes a random scattering. Specular scattering has no effect on surface mobility, since momentum of the carriers in the direction of current flow is preserved[32]. On the contrary, diffuse scattering causes a reduction in the carriers' mean free path and hence a decrease in the surface mobility. The quantum mechanical scattering becomes important whenever an atomic particle is confined to dimensions smaller than its wavelength in free space. Due to a quantization of the inversion layer carrier wave function in the direction perpendicular to the silicon surface, the effective mass of the mobile carriers is affected which leads to a decrease in the surface mobility[32].

For diffuse scattering to explain the behaviour of channel conductance at high normal fields for devices fabricated on laser crystallized polysilicon and single crystal silicon, one would expect a greater reduction in channel conductance in the former case than in the latter due to increased scattering at the grain boundaries. This, however, is not observed. Quantum mechanical theories would also pred-

ict a greater decrease in gds for laser crystallized polysilicon devices. Hence it may be concluded that some other mechanism operates at high gate to source voltages to prevent expected decrease in effective mobility.

Obviously, an attempt to lump the effect of reduced channel conductance into mobility cannot explain the phenomenon observed. The model proposed here to explain the smaller reduction in gds at higher gate voltages for laser crystallized polysilicon devices in terms of a release of carriers from dormant donor levels in the laser crystallized polysilicon. In the previous section the presence of deep acceptor levels was postulated. It is postulated here that donor levels are also present. At low gate voltages, the donor type defects are 'dormant' and hence do not affect the threshold voltage which otherwise would have been found to be lower (because donor type defect levels tend to decrease the V_t for an acceptor type bulk). As the gate voltage is increased, these 'dormant' donor type defects become active and release mobile carriers. This would result in a smaller decrease in gds compared to single crystal devices. To verify such a model will require considerable further research to identify the presence of and determine the relative concentration of acceptor and donor type defects in laser crystallized polysilicon.

5.6 Gate Transconductance (g_m)

The gate transconductance is defined by,

$$g_m = \left. \frac{\partial I_d}{\partial V_{gs}} \right|_{V_{ds}, V_{bs}} \quad \dots\dots\dots (5.13)$$

In the two regions of MOS transistor operation, g_m is given by,

$$g_m = \frac{C_o \cdot \mu \cdot W \cdot V_{ds}}{L} \quad , \text{triode region} \quad \dots\dots\dots (5.14)$$

$$g_m = \frac{C_o \cdot \mu \cdot W \cdot (V_{gs} - V_t)}{L} \quad , \text{saturation region} \quad \dots\dots (5.15)$$

From equation (5.14) it is clear that the gate transconductance is independent of the gate to source voltage in the triode region, while it is linearly dependent on V_{gs} in the saturation region (equ. 5.15). The experimental results of transconductance vs gate voltage are given in Figs. 5.7(a-c) and 5.8(a-c) for channel lengths of 50 and 7 microns respectively. In general at a particular value of V_{gs} and V_{ds} , g_m is less in the case of laser crystallized devices than that for the single crystal devices. This is due to the lower mobility in the case of laser crystallized polysilicon. Comparing the transconductance of the devices fabricated on laser crystallized polysilicon and single crystal silicon, shows that at higher gate voltages, the reduction in g_m is less for laser crystallized devices than for single crystal devices. The transconductance falls off

Fig 5.7(a) Gate transconductance vs. gate voltage for a polysilicon layer on single crystal substrate; L=50micron

Fig 5.7(b) Gate transconductance vs gate voltage for a single crystal substrate; $L=50\mu\text{m}$;

Fig 5.7(c) Gate transconductance vs gate voltage for a polysilicon on silicon dioxide substrate; L=50micron

Fig 5.8(a) Gate transconductance vs gate voltage for a single crystal substrate; L=7micron

Fig 5.8(b) Gate transconductance vs gate voltage for a polysilicon layer on single crystal substrate; L=7micron

Fig 5.8(c) Gate transconductance vs gate voltage for a polysilicon layer on silicon dioxide substrate; L=7micron

at higher gate voltages due to a reduction in mobility. In the case of the laser crystallized devices, the fall off in g_m is less, suggesting the presence of a competing mechanism to counteract the surface field induced reduction in the field effect mobility. The proposed model of section 5.4 which hypothesizes the existence of 'dormant' donor type defect levels in the semiconductor bulk would provide such a mechanism.

5.7 Discussion Of Results

From the discussion of the previous sections, it is clear that the parameters of a MOS transistor fabricated on laser crystallized polysilicon are influenced by the presence of defect levels and grain boundaries in the laser crystallized polysilicon bulk. The effect of the acceptor type defect level is to increase the threshold voltage for an N-channel MOS transistor. For example, a V_t of 3 volts was measured for a 50 μ m channel length nMOST in laser crystallized polysilicon on SiO₂; while the same geometry device had a V_t of 1.5 volts for polysilicon on single crystal silicon and 0.85 volts fabricated in single crystal silicon. All of the substrates had a doping concentration of $1E16/cm^3$. Clearly the defect density is greatest for the laser crystallized polysilicon on insulator.

Once a conducting channel is formed between the source and the drain of the MOS transistors, the devices made on all the three types of substrates showed good triode region characteristic. As the gate to source voltage was increased, the channel conductance reduced due to scattering phenomenon at the Si-SiO₂ interface and quantum mechanical scattering. However, for a particular V_{gs} , the drop in g_{ds} for laser crystallized polysilicon devices was observed to be less than the corresponding drop in g_{ds} for single crystal silicon devices. This observation is significant, since it cannot be explained in terms of mobility reduction due to scattering mechanisms. A possible explanation has been presented, which involves postulation of the presence of 'dormant' donor type defects in the polysilicon which act to supply carriers at higher gate voltages, thus pulling up the channel conductance. A similar phenomenon was observed for the gate to source transconductance.

The presence of grain boundaries has a significant influence on the field effect mobility. Longer channel devices on laser crystallized polysilicon exhibit a lower value of field effect mobility than that for smaller channel devices. In general, it was found that devices fabricated on laser crystallized polysilicon with underlying single crystal silicon have lower field effect mobility than single crystal devices but higher than those on laser crystallized

polysilicon on SiO₂ for a particular channel length. These results are summarized for convenience in table 5.1.

For the devices fabricated on laser crystallized polysilicon on SiO₂, a gradual increase in the drain to source current was observed with increasing V_{ds}; these devices showed poor saturation characteristics. Similar effects have been observed for silicon-on-sapphire (SOS) devices (33,34). For short channel devices the tendency to saturate is still less compared to long channel devices. Besides the silicon thin film being on an insulating substrate, which affects the characteristics of short channel devices; punch-through could also contribute to the poor saturation tendencies. The breakdown mechanisms in laser crystallized polysilicon should be studied to establish the effect of grain boundaries on the breakdown mechanism.

The theoretical results of I-V characteristic show a higher value of current because of overestimation of current by the circuit simulation program, SPICE. This is also thought to be as a result of the device parameters being undetermined in absence of a parameter extraction software package. Hence the theoretical results do not lend themselves to a comparison with the experimental results in a meaningful way. Similarly, the effect of floating substrate in the case of MOS transistors on polysilicon layer on silicon dioxide, on some of the observed phenomena in this research work, remains to be studied.

TABLE-5.1

Summary Of MOS Parameters

Substrate	Chan-Length(um)	Mobility	Threshold V
single crystal	50.0	773.0	0.85
Poly On single Crystal Si	50.0	300.0	1.5
Poly On SiO2	50.0	150.0	3.0
Single crystal	7.0	780.0	0.8
Poly On single Crystal	7.0	362.0	1.4
Poly On SiO2	7.0	180.0	2.75
Single Crystal	2.5	775.0	0.75
Poly On Single Crystal Si	2.5	500.0	1.25
Poly On SiO2	2.5	200.0	2.0

CHAPTER-6

CONCLUSION AND FUTURE WORK

6.1 Conclusion:

The characteristics of MOS devices fabricated in laser crystallized polysilicon on single crystal silicon and silicon dioxide, and in single crystal silicon have been compared in this thesis. It has been shown that the laser can be used to crystallize polysilicon deposited on an insulating substrate. An increase in grain size from a starting range of 100-500Å to laser crystallized grain size of 2µmX40µm has been achieved.

Devices fabricated in laser crystallized polysilicon were found to show I-V characteristics similar to those of the devices fabricated on single crystal silicon substrate. Generally, however, for the same terminal voltage levels the devices in polysilicon showed lower values of channel conductance and gate transconductance. This is thought to be the result of a lower mobility in the laser crystallized polysilicon. At higher gate to source voltages a significant phenomenon was observed. In normal MOS devices, the channel conductance drops at higher V_{gs} due to a decrease in the field effect mobility caused by scattering at the Si-SiO₂ interface. For the triode region, a smaller drop was drop

was observed for the value of transconductance. For the devices on laser crystallized polysilicon, this drop was less than that found for single crystal devices. To explain this behaviour of g_{ds} and g_m at high V_{gs} , it was hypothesized that there are donor defect levels present in the polysilicon bulk which are 'dormant' at low gate voltages but release carriers in the channel at higher gate voltages.

A measured value of threshold voltage for laser crystallized polysilicon devices was found to be higher than that for single crystal devices. This is felt to be due to a presence of acceptor type defect levels in the polysilicon bulk. A modified expression for the threshold voltage was derived taking into account the defect levels. From this it was found that the defect concentration was approximately equal to the doping concentration in the polysilicon bulk.

6.2 Future Work:

Since it has been shown that a high powered laser can be used to crystallize polysilicon, and working MOS transistors can be fabricated on such a substrate, the main thrust of future work in this area should be directed towards the following research areas:

- (1) Optimize laser crystallization parameters;

(2) Model MOST, taking into account the grain boundaries and the defect levels;

(3) Fabricate both p-channel and n-channel MOST's and measure parameters in detail;

(4) Attempt to confirm the 'dormant defect level' model;

(5) Determine effects of grain boundaries on mobility and I-V characteristics of MOST's for short channel devices;

(6) Try to establish direct relationship between doping density and defects and doping density and nucleation sites.

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APPENDIX-A

A PROGRAM FOR MICROPROCESSOR 6502 TO CONTROL THE X-Y DRIVER STAGE

LABEL	OPCODE	BYTE1	BYTE2	BYTE3	COMMENT
INIT:	CLD	D8	1	--	
	LDA	A9	00	--	
	STA	85	AA	--	
	STA	85	BB	--	
	STA	85	CC	--	
	STA	85	DD	--	
	LDA	A9	KK	--	KK:SCAN PERIOD
	STA	T5	EE	--	
	LDA	A9	00	--	
	STA	8D	00	17	
	LDA	A9	FF	--	
	STA	8D	01	17	
START:	LDA	A9	00	--	
	STA	85	FF	--	
	STA	85	GG	--	
PULSE:	LDA	AD	00	17	COMPLEMENT THE CLOCK
	EOR	49	01	--	
	STA	8D	00	17	
	CLC	18	--	--	
	LDA	A5	FF	--	
	ADC	69	01	--	
	STA	85	FF	--	INCREMENT M1
	LDA	A5	GG	--	
	ADC	69	00	--	
	STA	85	GG	--	
	LDA	A9	NN	--	
	SEC	38	--	--	
	SBC	E5	FF	--	
	LDA	A9	MM	--	IS M1 > A?
	SBC	E5	GG	--	IF YES,BRANCH TO KD1
	BCC	90	1A	--	
	LDA	A9	NN	--	
	SEC	38	--	--	
	SBC	E5	FF	--	
	STA	85	HH	--	
	LDA	A9	MM	--	IS M1 = A?
	SBC	E5	GG	--	IF NOT,BRANCH TO DEL1
	ORA	05	HH	--	OTHERWISE JUMP TO DEL2
	BNE	D0	60	--	
	JMP	4C	E6	02	(02E6:ADDRESS OF DEL2)
KD1:	LDA	A9	NN+4	--	
	SEC	38	--	--	
	SBC	E5	FF	--	IS M1 = B?

	STA	85	11	--	IF NOT, BRANCH TO DEL1
	LDA	A9	MM	--	IF YES, JUMP TO KAM
	SBC	E5	JJ	--	
	ORA	05	11	--	
	BNE	D0	46	--	
	JMP	4C	d7	02	(02d7: ADDRESS OF KAM)
KAM1:	JSR	20	ba	02	JUMP TO SUBROUTINE DEL AT 02ba
	INC	E6	AA	--	
	LDA	A9	FF	--	INCREMENT M2
	SEC	38	--	--	IS M2 = 2?
	SBC	E5	AA	--	IF NOT, BRANCH TO START
	BNE	D0	9D	--	
	LDA	A9	10	--	
	EOR	4D	00	17	CHANGE DIRECTION
	STA	8D	00	17	
	CLC	18	--	--	
	LDA	A5	BB	--	
	ADC	69	01	--	
	STA	85	BB	--	INCREMENT M3
	LDA	A5	CC	--	
	ADC	69	00	--	
	STA	85	CC	--	
	LDA	A5	CC	--	
	SEC	38	--	--	
	SBC	E5	BB	--	
	STA	85	JJ	--	IS M3 = C?
	LDA	A5	LL	--	IF YES, BRANCH TO BREAK
	SBC	E5	CC	--	
	ORA	05	JJ	--	IF NOT, M2=0, AND GO TO START
	BEQ	F0	07	--	
	LDA	A9	00	--	
	STA	85	AA	--	
	JMP	4C	1A	--	
BREAK:		BRK	00	--	--
KAM2:	JSR	20	ba	02	
	JMP	4C	20	02	JUMP TO PULSE
DEL1:	LDA	A9	3d	3d	
	STA	85	PP	PP	DELAY D1
	DEC	C6	PP	PP	
	BNE	D0	FC	FC	
	JMP	4C	20	02	JUMP TO PULSE
DEL:	LDA	A9	FF	--	
	STA	85	QQ	--	
	LDA	A9	FF	--	
	STA	85	RR	--	
	DEC	C6	RR	--	DELAY FOR RELAY TO OPERATE
	BNE	D0	FC	--	
	DEC	C6	QQ	--	

	BNE	D0	F4	--	
	RTS	60	--	--	
KAM:	JSR	20	bA	02	JUMP TO DEL AT 02bA
	LDA	A9	04	--	
	EOR	4D	00	17	
	STA	85	00	17	CHANGE Y TO X
	JMP	4C	02	71	JUMP TO KAM1
DEL2:	JSR	20	bA	02	JUMP TO DEL AT 02bA
	LDA	AD	00	17	
	ORA	09	14	--	CHANGE X TO Y AND DIRECTION
	STA	8D	00	17	
	JMP	4C	A9	02	JUMP TO KAM2

NOTE: AA, BB, CC, DD, EE, FF, GG, HH, II, JJ, KK, PP, QQ, RR ARE ZERO PAGE MEMORY LOCATIONS.

*** STANFORD UNIVERSITY PROCESS ENGINEERING MODELS PROGRAM ***

*** VERSION 0-03 ***

```

1....  TITLE NMOS THRESHOLD CALCULATION
2....  GRID DYSI=.1,DPTH=1,YMAX=2.5
3....  SUBS ELEM=B,CONC=12E15,ORNT=100
4....  COMM SILOX DEPOSITION
5....  STEP TYPE=DEPO,TIME=32,GATE=31.25E-3
6....  PRINT HEAD=Y
7....  STEP TYPE=ETCH,TEMP=25
8....  COMM GATE OXIDATION
9....  STEP TYPE=OXID,TEMP=1200,TIME=22,MODL=DRY0
10.... STEP TYPE=OXID,TEMP=1200,TIME=10,MODL=NITO
11.... STEP TYPE=ETCH,TEMP=25
12.... STEP TYPE=OXID,TEMP=1200,TIME=22,MODL=DRY0
13.... STEP TYPE=OXID,TEMP=1300,TIME=10,MODL=NITO
14.... MODL NAME=SPH1,GATE=-.0550,4E10,CBLA=1
15.... STEP TYPE=OXID,TEMP=1000,TIME=30,MODL=NITO,MODL=SPH1
16.... END

```

*** THRESHOLD CALCULATION

*** DEPOSITION

```

***
*** TEMPERATURE = 25.0 DEGREES C
*** TIME = 1.0 MINUTE
*** TEMPERATURE = 1000.0 DEGREES C
*** TIME = 1.0000 MINUTE

```

```

*** SURFACE CONCENTRATION = 1.700000E+15 ATOMS/CM2

```

E-03 I

SURFACE CONCENTRATION = 9.787029E+15 ATOMS/CM2

```

GATE MATERIAL      = N+ POLY SILICON UNDER GATE = P - TYPE
OXIDE THICKNESS   = 1020.4 ANG. CAPACITANCE/AREA = 3.38E-04 PF/UM2
THRESHOLD VOLTAGE = 1.08 VOLTS AT SURFACE STATES = 4.00E+10

```

JUNCTION DEPTH	I	SHEET RESISTANCE
	I	5430.97 OHMS/SQUARE

NET ACTIVE CONCENTRATION

OXIDE CHARGE	=	5.725244E+10	IS	2.00	% OF TOTAL
SILICON CHARGE	=	2.801033E+12	IS	98.0	% OF TOTAL
TOTAL CHARGE	=	2.858285E+12	IS	100.	% OF INITIAL
INITIAL CHARGE	=	2.858308E+12			

!C SPCT

C CALCULATION OF SPOT-SIZE

REAL L

DATA Z,F,L,W0/0.5,5E-5,9E-2/

W2=(F*L)/(3.14*W0)

Z=-.05

DO 1 IZ=1,50

Z=Z+.05

W3=W2*SQRT(1+((L*Z)/(3.14*W2**2))**2)

W=W3*2E4

WRITE(1,2)Z,W

2 FORMAT(2F7.2)

1 CONTINUE

END

!C SFOJ1

.00	17.69	1.25	450.35
.05	25.24	1.30	468.33
.10	40.11	1.35	486.32
.15	56.82	1.40	504.31
.20	74.14	1.45	522.30
.25	91.72	1.50	540.29
.30	109.44	1.55	558.28
.35	127.24	1.60	576.27
.40	145.08	1.65	594.26
.45	162.96	1.70	612.25
.50	180.87	1.75	630.24
.55	198.79	1.80	648.24
.60	216.72	1.85	666.23
.65	234.67	1.90	684.22
.70	252.62	1.95	702.22
.75	270.58	2.00	720.21
.80	288.54	2.05	738.21
.85	306.51	2.10	756.20
.90	324.48	2.15	774.20
.95	342.46	2.20	792.19
1.00	360.43	2.25	810.19
1.05	378.41	2.30	828.18
1.10	396.39	2.35	846.18
1.15	414.38	2.40	864.17
1.20	432.36	2.45	882.17

END

0 610 6.8 3

FIN