A 5.8mW Fully Integrated Multi-Gigahertz Frequency Synthesizer in 0.13-μm CMOS

by

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Abstract

This thesis describes the design of a low power multi-gigahertz fully integrated phase locked loop based frequency synthesizer. The synthesizer includes a conventional tri-state phase frequency detector, a fully differential charge pump, a 2^{nd}-order on-chip loop filter, a voltage-controlled ring oscillator and an integer-*N* multi-modulus divider. The synthesizer is implemented in a 0.13μm CMOS process and consumes less than 5.8mW of power at a supply voltage of 1.2V. The entire synthesizer is designed using current mode logic and occupies an active area of $0.34mm^2$.

Acknowledgements

First and foremost I would like to thank Dr. John W. M. Rogers for giving me the opportunity to study under his direction for which I am forever grateful for the knowledge gained through this experience.

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Finally I would like to thank my parents Phillip and Fadia Karam for their support and encouragement which enabled me to attend Carleton University. I can whole heartedly say that this horse will always be thirsting for a drink of water.

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Abbreviations

CML	Current Mode Logic
PFD	Phase Frequency Detector
CP	Charge Pump
VCO	Voltage-Controlled Oscillator
MMD	Multi-Modulus Divider
PN	Phase Noise
PLL	Phase Locked Loop
CMOS	Complementary Metal Oxide Silicon
NMOS	N-Type Metal-Oxide-Semiconductor
PMOS	P-Type Metal-Oxide-Semiconductor
PDA	Personal Digital Assistant

1. Introduction

In this thesis a low powered frequency synthesizer will be designed and implemented to function in the multi-gigahertz range. The frequency synthesizer will be designed using a 0.13μm CMOS process.

1.1. Motivation

Motivated by a continuing demand for efficiency in battery-operated applications, an RF frequency synthesizer is investigated by pushing the limits of low power operation. Increasing demand for wireless devices and applications such as cellular phones, PDA's and other mobile devices have been a continuing driving force in the pursuit of low power consumption and battery efficiency. Frequency synthesizers can be found in most any wireless device that requires channel selection within a particular frequency band. In general, frequency synthesizers are required to provide a stable reference frequency with programmability, thereby allowing channel selection within a particular communication band.

1.2. Thesis Focus

When choosing a synthesizer design, several circuit architectures are possible; however, the integer-*N* or fractional-*N* type-II structure is most popular for its low phase noise, low power consumption and simplicity [1]. Advancements in CMOS technology are leading to low power, low noise, and cost effective, fully integrated solutions. Current mode logic (CML) is partially responsible for making these claims possible [2]. CML circuits can operate at a lower signal swing, and maintain a higher frequency of operation at lower supply voltages than static CMOS [3], thereby reducing power consumption. This thesis presents a fully integrated on-chip frequency synthesizer generally geared towards the 2GHz frequency band. The synthesizer is designed in a 0.13μm CMOS process with a supply voltage of 1.2V. The current consumption of all the blocks in the synthesizer total 4.83mA, yielding a total power consumption of 5.8mW. The synthesizer also makes use of an integrated 2^{nd}-order loop filter designed with a high loop bandwidth, thus facilitating faster lock times and smaller integrated capacitance requirements.

A comparison between frequency synthesizers proclaiming low power design are summarized in Table 1.1. The tabulated synthesizers were selected based on publicized claims of low power design and of similar output frequency. A field of merit (FOM) was derived as the output power divided by the output frequency such that their performance results are somewhat normalized for comparison purposes.

Table 1.1: Published low power frequency synthesizers

Reference	Power	Frequency	Technology	FOM
[4]	23mW	5.5GHz	0.25μm CMOS	4.2
[8]	22.6mW	1.76GHz	0.35μm BiCMOS	12.8
[9]	22mW	900MHz	0.5μm AMI C5N	24.4
[10]	22mW	2.4GHz	0.18μm CMOS	9.2
[6]	15mW	900MHz	0.8μm CMOS	16.7
[7]	12mW	900MHz	0.35μm CMOS	13.3

1.3. Contributions

This research has contributed a low power CML based frequency synthesizer that can operate up to 1.52GHz which also includes an on-chip loop filter to the development of synthesizer design.

1.4. Thesis Outline

This thesis is composed of 5 chapters and is organized as follows:

Chapter 1 contains the thesis introduction.

Chapter 2 provides background information regarding PLL architecture and design methodology of common PLL building blocks.

Chapter 3 discloses the circuit design used for this synthesizer and addresses techniques used to achieve low power operation.

Chapter 4 presents simulation and measurement results. The discrepancies between simulated and measured results are analysed.

Chapter 5 provides a summary of the work presented, concluding remarks and presents opportunity for future work.

2. Frequency Synthesizer Overview

2.1. Introduction

In general a PLL is a closed-loop frequency control system, which uses feedback to maintain the phase of its output signal with respect to the phase of a reference signal. PLL's have been used in a vast array of applications, such as internal clocks and clock multipliers, demodulation or modulation of radio signals, and frequency synthesis in digitally tuned radio receivers or transmitters. Although the latter will be studied, most PLL's are composed of a phase frequency detector (PFD), charge pump, loop filter, voltage-controlled oscillator (VCO) and divider. For adequate performance it is critical that these components be designed and interfaced correctly.

The following sections will give the reader a basic understanding of the components used to construct a frequency synthesizer. Section 2.2 will describe the nature of a frequency synthesizer. Section 2.3 will describe PFDs and charge pumps, while section 2.4 and 2.5 will describe VCOs and dividers, respectively. Section 2.6 will describe PLL loop filters and finally Section 2.7 will describe current mode logic.

2.2. Synthesizer Overview

Frequency synthesis occurs in PLL's when a programmable divider is placed in line with the feedback loop of the PLL, between the VCO and the PFD; this gives the PLL the ability to vary its output frequency by varying the divider's ratio. When the divider with division ratio N is added, the PFD attempts to reduce the phase difference between the reference frequency θ_{ref} and the feedback frequency θ_o. The PFD will signal to the loop that its frequency f_{out} needs increasing such that the phase of the divided signal in the feedback loop matches the phase of the reference signal. For this to be true, the VCO must then run at a frequency f_{out} equal to the reference frequency multiplied by the division ratio, f_{ref} x N. Now if the division ratio is altered by one, then the VCO will have to compensate for this change in its frequency by one multiple of the reference frequency. This tells us that the step size f_{step} is equal to the reference frequency. An illustration depicting a frequency synthesiser is shown in Figure 2.1.

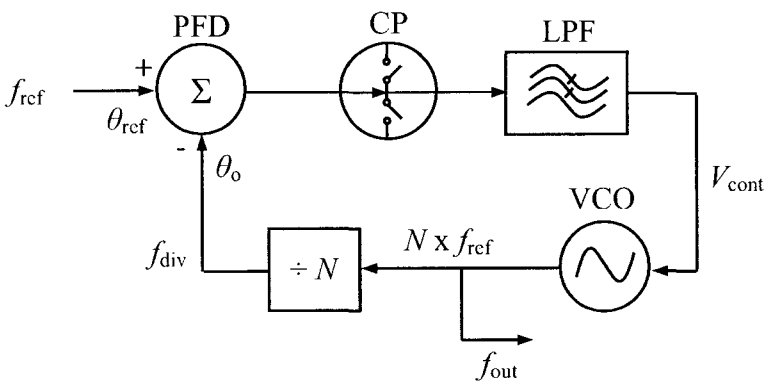


Figure 2.1: Frequency synthesizer architecture.

There are two main types of PLL based synthesizers, integer-*N* and fractional-*N*. In a conventional integer-*N* design a tri-state PFD is used to compare the phase of the divided VCO signal f_{div} to that of the reference signal f_{ref}. After making this comparison, the PFD passes any errors in phase to the charge pump CP, which in turn uses a train of current pulses I_{cp} to add or remove charge on the loop filter. The voltage residing on the loop filter is then used as a control voltage V_{cont} for the VCO. The multi-modulus divider (MMD) is used to scale down the VCO frequency, its signal is in turn passed into the PFD for continual comparison with the reference. In an integer-N design, the output frequency of the VCO f_{out} is controlled by changing the division ratio of the multi-modulus divider. The division ratio of the divider can be changed using control bits P_n. Depending on the divider architecture, a five stage divide-by-2/3 based MMD may lend itself to the following equations.

$$f_{out} = f_{ref} \cdot N \tag{1}$$

$$f_{out} = f_{ref} \cdot (P_1 + 2^1 P_2 + \ldots + 2^{n-2} P_{n-1} + 2^{n-1} P_n + 2^n) \tag{2}$$

$$f_{out} = f_{ref} \cdot (P_1 + 2P_2 + 4P_3 + 8P_4 + 16P_5 + 32) \tag{3}$$

There are several PLL performance characteristics, these specifications vary with application and can be categorized as power dissipation, noise, accuracy, lock time and layout area. There may be others as well depending on the application.

2.3. Phase Frequency Detector and Charge Pump

The PFD is used to output a signal proportional to the phase difference of its two input signals, namely the phase of the reference signal θ_{ref} and the phase of the divided feedback signal θ_{div}. The PFD is used in conjunction with the charge pump to decrease the phase difference between its two input signals. The PFD will signal to the charge pump to either source or sink current to or from the loop filter by using an *Up* and a *Down* pulse respectively. The most commonly used PFD is the tri-state PFD; its state diagram is shown in Figure 2.2.

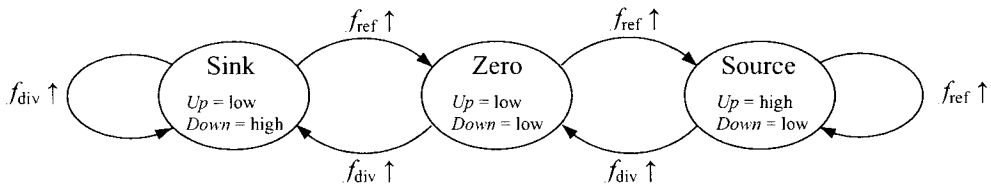


Figure 2.2: PFD state diagram.

The above figure will be used to help demonstrate how a tri-state PFD works. It is important to note that state changes only occur on the rising edge of signals f_{ref} and f_{div}. If for example $f_{ref} = f_{div}$ and there respective phases $\theta_{ref} = \theta_{div}$, all is fine and the PFD will remain in state "Zero". However, if $f_{ref} > f_{div}$, and the leading edge of the reference signal is ahead of the leading edge of the divider output signal, the *Up* signal is set to high and the PFD will enter state "Source". This state will signal the charge pump that it must source current to the loop filter such that the control voltage on the VCO increases, re-

sulting in an increase in f_{div}. The PFD will remain in state Source until the next positive edge of f_{div} arrives, thereby sending a *Down* pulse and bringing the PFD back to state "Zero". This means that both *Up* and *Down* pulses are high for a short period of time, namely the time it takes these signals to propagate through the AND gate in Figure 2.3, also known as the Delay cell. During this period the charge pump will be instructed to source and sink current from the loop filter simultaneously, if the charge pump is ideal the net charge applied to the loop filter will be zero, in reality there will always be a slight mismatch between the two. Conversely, if $f_{div} > f_{ref}$ the Down signal will be set to high and the PFD will enter the "Sink" state, thus instructing the charge pump to remove charge from the loop filter such that the control voltage on the VCO decreases, resulting in a decrease in f_{div}.

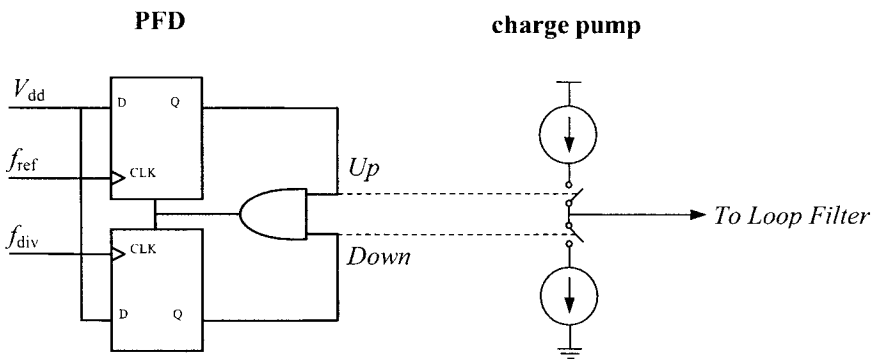


Figure 2.3: Tri-state PFD and charge pump.

A phenomena known as Dead Zone occurs when the phase difference between f_{ref} and f_{div} reach a minimum detectable level. This is caused by the switching delays of the *Up* and *Down* pulses in the PFD and the switching delay of the charge pump. This effect

can be minimized by increasing the propagation delay in the Delay cell mentioned earlier, thus permitting the charge pumps transistors to fully switch before resetting the PFD.

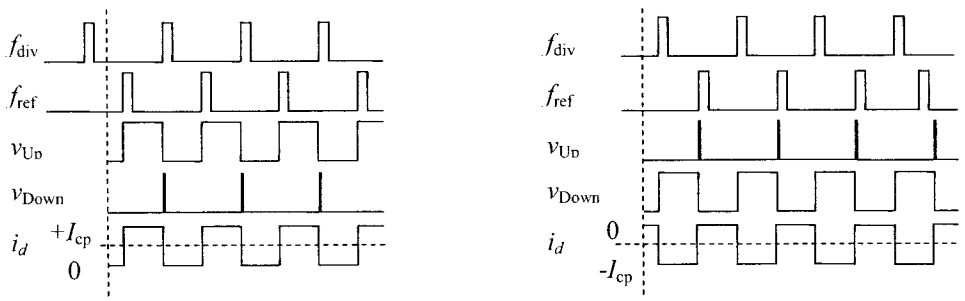


Figure 2.4: PFD operation when $\theta_{ref} \neq \theta_{div}$.

From previous discussion and by observing Figure 2.4, it is known that the PFD output signals (*Up*, *Down*) directly influence the charge pump's ability to source or sink current from the loop filter. If we assume that the phase difference between f_{ref} and f_{div} is large, it is clear that either v_{Up} or v_{Down} signals will remain high for a longer period of time than if their phase differences were very close together. Since the PFD has a phase response between -2π and 2π as shown in Figure 2.5, and taking into account that the phase difference between f_{ref} and f_{div} is directly proportional to the output current we can now deduce the average current i_d from the charge pump:

$$i_d = \left(\frac{I_{cp}}{2\pi}\right)\left(\theta_{div} - \theta_{ref}\right). \tag{4}$$

From this, a proportionality constant K_{phase} is conceived where,

$$K_{phase} = \frac{I_{cp}}{2\pi}. \tag{5}$$

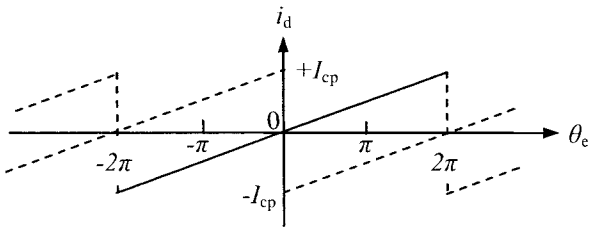


Figure 2.5: Average output current vs. phase of PFD operational range.

In charge pumps, it is desirable that the characteristic current used to apply charge $+I_{cp}$, and remove charge $-I_{cp}$, to or from the loop filter be equally matched and linear over the charge pump's output voltage. However this is not possible because of the short channel effect in MOS transistors, which causes the output resistance of the charge pump to vary with the voltage level on the loop filter. An illustration of this effect is shown in Figure 2.6. Mismatch in charge pumps leads to undesirable reference spurs, therefore care must be taken to minimize this behaviour by increasing the output impedance. This can be done by increasing the lengths of the charge pump's output transistors.

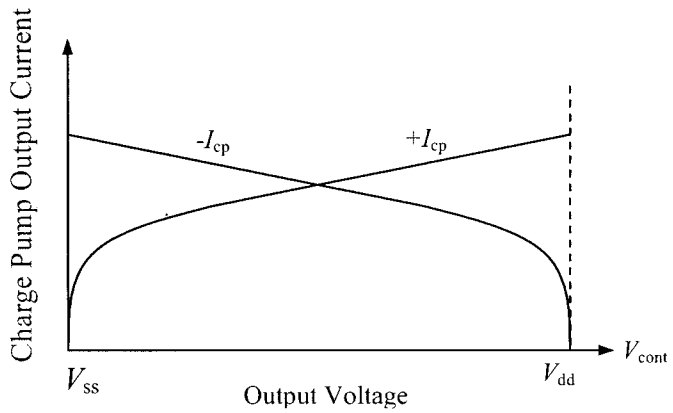


Figure 2.6: Charge pump output current vs. charge pump control voltage.

2.4. Voltage-Controlled Oscillator

The VCO is used to send a clean output signal to be used as a frequency generator for its intended purpose or function. The VCO must also be controllable, such that its output frequency depends on the voltage level held by the loop filter. Figure 2.7 shows a common frequency response of a VCO, where K_{VCO} is the rate of change of frequency per change in voltage. There are two common architectures for VCO design, an LC based oscillator or a ring oscillator. Ring oscillators are known to have higher tuning ranges but lower phase noise performance as compared to an LC based oscillator.

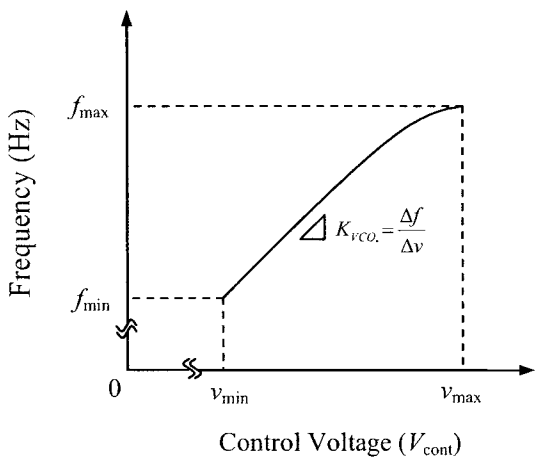


Figure 2.7: VCO frequency vs. tuning range.

All oscillators must satisfy what is known as the Barkhausen criteria in order for oscillation to occur. The criteria states that the gain of the oscillator must be greater than or equal to one and that the phase of the complete system must be an integer multiple of 360°.

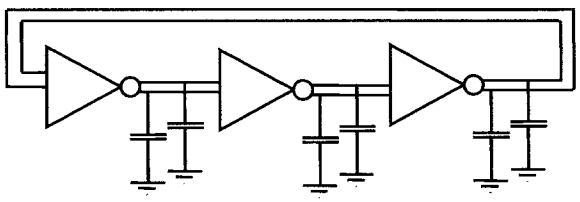


Figure 2.8: A 3-stage ring oscillator.

If one assumes a three stage ring oscillator as illustrated in Figure 2.8, is the chosen topology. Each inverter has a phase shift of 180° giving a total of 540° for the loop, in order for oscillation to occur an additional 180° phase shift must be added such that the total phase shift around the loop is $2n\pi$, or in this case 720°. Therefore the extra phase shift needed for oscillation can be shared by each oscillator. This means that an additional phase shift of 60° can be added to each inverter. This is usually accomplished by means of an RC shift created by capacitors which follow the inverter and intrinsic resistors in the inverters. In general the frequency of oscillation for an *N*-stage oscillator can be found using:

$$f_o = \frac{1}{2N\tau} \tag{6}$$

where:

τ is the delay created by the resistive and capacitive elements in between each stage,

N is the number of stages in the ring-oscillator.

2.5. Divider

The purpose of the divider is to scale down the VCO output frequency in the feedback system of the PLL. For frequency synthesis, it is necessary to control or modify the division ratio. The most popular divider topology that allows for controllable frequency selection is the multi-modulus divider. In its simplest form, a dual-modulus divider allows frequency division of either 2 or 3 by toggling an input bit P, between zero and one respectively. Figure 2.9 shows an input signal with frequency f_o as it would enter the divider from the VCO, following a division ratio of 2, we see that the output of the divider is high every two phases and low for every other two phases. When the divide-by-3 bit P is high, the output frequency is a third of the input frequency. The division ratio possibilities of a simple dual-modulus divider are any integer values beginning at 4 and ending at 7.

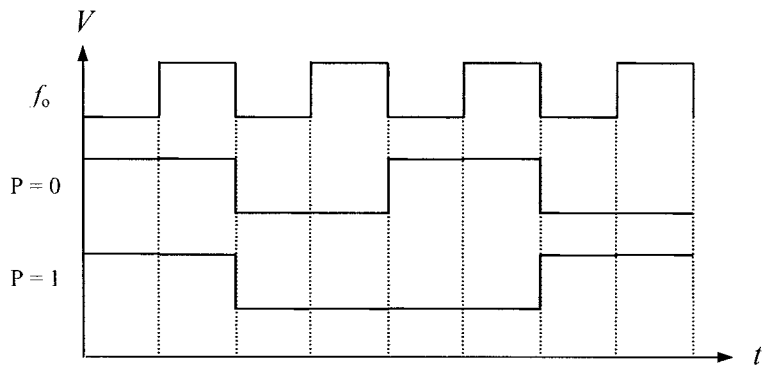


Figure 2.9: Divider input and output signals.

By cascading several dual-modulus dividers together, we essentially create a multi-modulus divider with numerous division ratio possibilities. The diagram in Figure 2.10 illustrates a cascade of five divider stages.

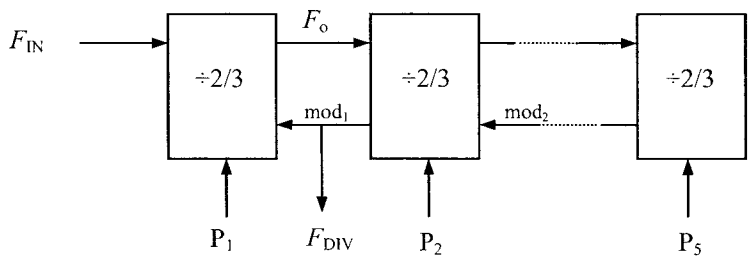


Figure 2.10: 5 cascading divide-by-2/3 stages.

If for example all stages were set to divide by two, each stage would have an output frequency that is half of its input frequency and the output frequency would be 2^5 or 32 times less than the input frequency. Depending on the orientation of each *P* bit, we can cascade five divide-by-2/3 dividers and use equation (3) to tell us that the division ratio possibilities are between 32 to 63 inclusive.

2.6. Loop Filter

The loop filter's primary objective is to integrate the current pulses from the charge pump such that a bias voltage can be established for frequency tuning of the VCO.

Loop filters are most often designed as passive low pass filters because of their simplicity, low noise performance, low cost and power efficiency. However, active filters are also common. The loop filter configuration for a type II 2nd-order filter is illustrated in Figure 2.11.

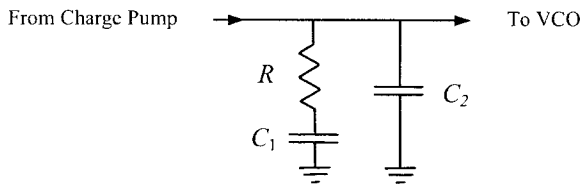


Figure 2.11: 2nd-order passive loop filter.

Elements C_1 and R_1 are chosen to define characteristics of the PLL's behaviour, such as settling time, stability and loop bandwidth. The shunt capacitor C_2 is added to minimize discrete voltage changes on the control line of the VCO. The frequency response of the loop filter can be described by the following equation:

$$F(s) = \frac{1 + sC_1R}{s^2(C_1 \cdot C_2 \cdot R) + sC_1 + sC_2} \tag{7}$$

2.7. Current Mode Logic

Current Mode Logic (CML) is fast becoming the topology of choice over its conventional static CMOS counterpart because of its superior power and noise performance

in low voltage high-speed applications. [3] The current consumption is constant and independent of the synthesizer's output frequency. Once optimized for low power operation, the logic gates can operate at a range of frequencies while maintaining excellent low power performance. The constant current source leads to lower switching noise, while the fully differential property of CML removes common mode noise sources generated from the power supply and the substrate at the time of switching. Figure 2.12 illustrates the architecture of a CML differential pair.

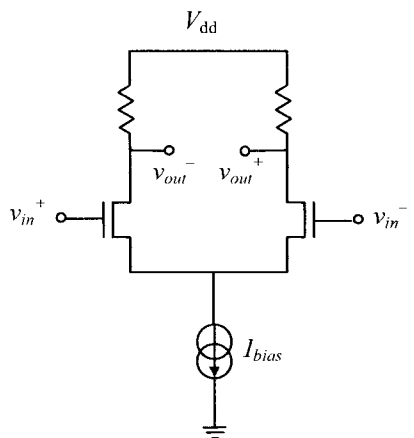


Figure 2.12: CML differential pair.

3. Frequency Synthesiser Design

The synthesizer was designed based on high speed, low power and acceptable noise criteria. The following chapter will discuss in detail all of the elements and ideas which made the synthesizer realizable.

3.1. Current Mode Logic

A circuit diagram illustrating a typical latch configuration (shown in Figure 3.1) is used throughout the design of the divider circuit. The first consideration that must be made when designing a CML circuit is the output swing voltage level. If the output swing level is too small, transistors M_3 and M_4 will not be able to fully switch, thus yielding large leakage currents and poor signal propagation. However, if the output swing level is too large, low headroom will cause the current sourcing transistor to fall out of the saturation region. The differential amplitude of the switching voltage was kept at approximately 400mV. In order to ensure good switching behaviour at minimal switching voltage, transistors M_1 and M_2 were sized using minimum length dimensions with a width of 2.8μm. Transistors M_3 and M_4 were sized using minimum length dimensions with a width of 1.6μm. It was found that for adequate switching for frequencies up to 2GHz, a 100μA

current was required. Therefore, in order to achieve a signal swing of 400mV, the load resistors were set to 4kΩ.

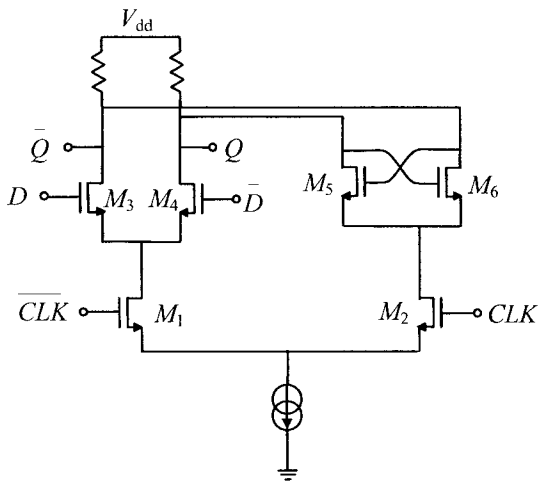


Figure 3.1: Typical CML latch configuration. [5]

3.2. Phase Frequency Detector

A standard tri-state PFD as mentioned in section 2.3 was implemented using two resetable flip-flops and an AND gate. The flip-flops were designed using NOR gates and were realized using differential CML logic; the configuration used is illustrated in Figure 3.2. An AND gate was used to reset the PFD when both *Up* and *Down* signals were high.

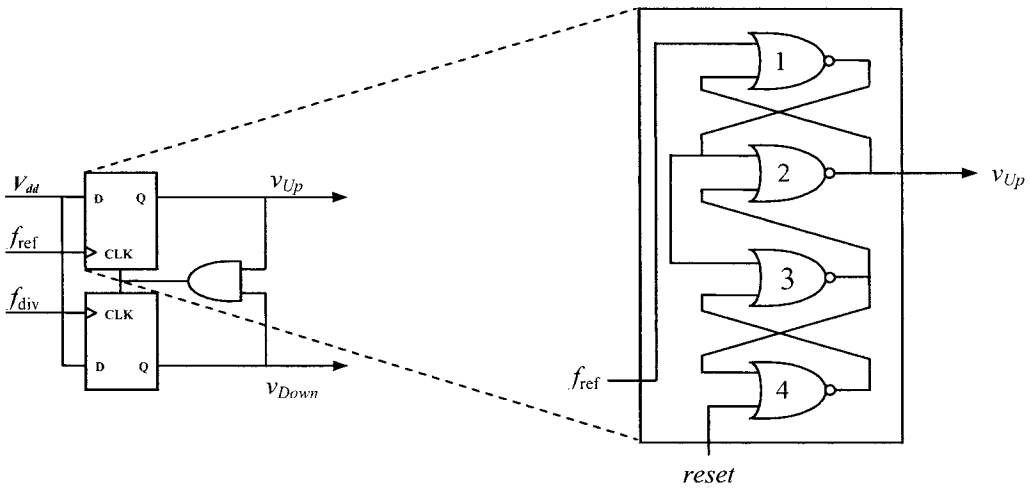


Figure 3.2: Tri-state PFD and latch implementation.

The PFD was designed to accept a 40MHz signal from the reference XTAL and from the divider. Each NOR gate in the PFD was designed to handle the requirements necessary for fail-safe operation while optimizing other performance features such as power dissipation at the same time. It was found that by reducing the current drawn by non-critical gates and by increasing current drawn by critical gates such as those used to drive the charge pump, the overall power dissipation of the PFD was optimized. For example, most NOR gates were designed using a current of 25μA, however because gate #2 (shown in Figure 3.2) is required to drive the gate capacitances of the charge pump as well as the parasitic capacitances in the interconnect between them, these gates were designed using currents of 100μA.

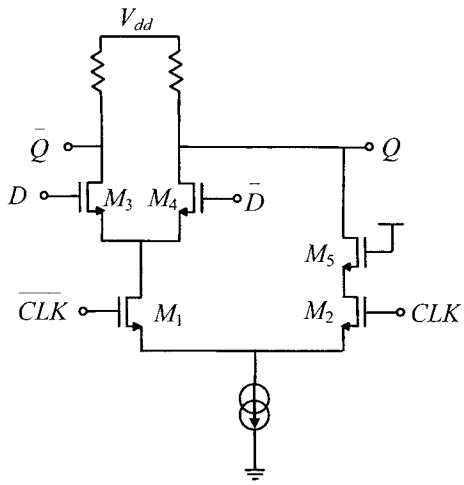


Figure 3.3: Typical CML AND gate configuration. [5]

To eliminate dead-zone, delay elements were added to the AND gate in the reset path. Figure 3.3 illustrates one of four AND gates which were added as delay elements to ensure that both *Up* and *Down* signals were fully on before the reset was applied. The delay was accomplished by limiting the current drawn by these gates to 6.25μA, thus translating to slower rise times, fall times and ultimately slower switching speeds.

3.3. Charge Pump

The charge pump as shown in Figure 3.4 is responsible for adding or removing charge from the loop filter, which in turn will increase or decrease the control voltage on the VCO. Careful design of a charge pump is necessary such that flicker and thermal noise contributors to in-band phase noise are mitigated [4]. A differential CMOS charge

pump with a single ended output was used in conjunction with the CML based PFD. Since the gain of the PMOS transistor is similar to that of the NMOS transistor (unlike in bipolar transistors), a CMOS design can be more advantageous in decreasing current mismatching issues normally associated with charge pump design. The purpose of using a differential design is improved phase noise performance as all common mode noise will be removed. This will lead to improved supply and ground noise rejection.

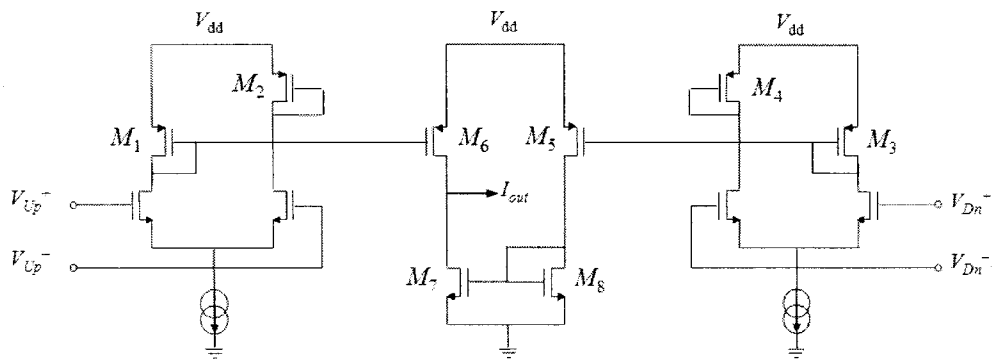


Figure 3.4: Differential input single-ended output charge pump.

The power consumption was reduced by designing the charge pump to operate with a modest current of 100μA. The total simulated power dissipated by the charge pump is 240μW. However, the implications of a low current design are directly reflected in noise performance [5]. In general, as the charge pump current I_{CP} decreases, the charge pump's total average output noise also decreases, as shown in,

$$i^2_{noTotalAvg} = 2\left[\frac{2K\mu}{L^2 f} I_{CP} + 4kT\left(\frac{2}{3}\right)\sqrt{2\mu C_{ox}\left(\frac{W}{L}\right) I_{CP}}\right]\frac{\delta}{T}. \qquad (8)$$

where, K is a proportionality constant, μ is the electron mobility, L is the MOS gate length, f is the frequency of operation, I_{CP} is the drain-to-source current, k is Boltzmann's constant, T is the period, C_{ox} is the gate oxide capacitance, W is the MOS gate width and δ is the amount of time that up and down currents are simultaneously on.

However, since the gain of the PFD/Charge Pump (K_{PHASE}) decreases with I_{CP} as given by (5)

$$K_{PHASE} = \frac{I_{CP}}{2\pi}. \tag{9}$$

The input referred phase noise of the charge pump φ, given below in (10), will increase providing K_{PHASE} is increasing faster than the dominant noise sources of the charge pump.

$$\vartheta = 2\pi\left[\sqrt{\frac{2K\mu}{I_{CP}L^2 f}} + \sqrt{\frac{2\mu C_{ox}}{I_{CP}^{\ 2}}}\right]\frac{\delta}{T}. \tag{10}$$

With decreasing I_{CP}, the output resistances of transistors M_6 and M_7 increases and the current mismatch between the up and down currents decrease when the output voltage is varied. The NMOS and PMOS current mirrors of the charge pump were all 1:1 for easier current mirroring. The diode connected PMOS transistors M_1, M_3, and corresponding diode connected NMOS transistor M_8, were sized for a low drain source saturation voltage $V_{DS,SAT}$, to maximize the control line voltage (the charge pump's output) range. However, care must be taken not to make these transistors too large, as their delay increases due to device parasitics.

The charge pump's output transistors M_6 and M_7 should have high output impedance. This will minimize current mismatch between up and down currents as the output voltage is varied. Furthermore, M_6 and M_7 must also be g_m matched to better equalize charge and discharge times, respectively.

3.4. Voltage-Controlled Oscillator

A 3-stage ring oscillator type VCO was implemented for its simplicity and wide tuning range. For power conservation and area reduction, the number of stages was reduced to three. When designing a ring oscillator with a low voltage supply, it is essential that the tuning range is maximized. This is achieved by adding a constant bias transistor in parallel with the control voltage source transistor such that the control voltage can range from 1.2V all the way down to 0V and still maintain frequency oscillation. A diagram showing a circuit level implementation of the VCO can be seen in Figure 3.5. Here V_{bias} is connected to a reference current such that current is always flowing through the inverters, thereby maintaining oscillation. V_{cont} is the voltage left on the control line by the loop filter, as this voltage increases, more current will flow through the inverters thereby charging their output loading capacitors (of the next stage) more quickly which in turn will increase the frequency of operation.

It was found that for the desired frequency of oscillation, the capacitance required between stages was minimal. It was also found that the gate capacitances corresponding

to the transistors in the next stage were of sufficient value such that it was not necessary to implement capacitive components. The widths of the switching gates in the VCO were varied until the desired output frequency was reached. The VCO is designed to oscillate with control voltages between 0.2v and 1.2v, corresponding to an output frequency range of 1.58GHz to 2.16Hz.

The oscillator's inverters were designed to provide sufficient output swing while maintaining operation over large current variations for optimal tuning range. The maximum power drawn by the VCO is approximately 500μW.

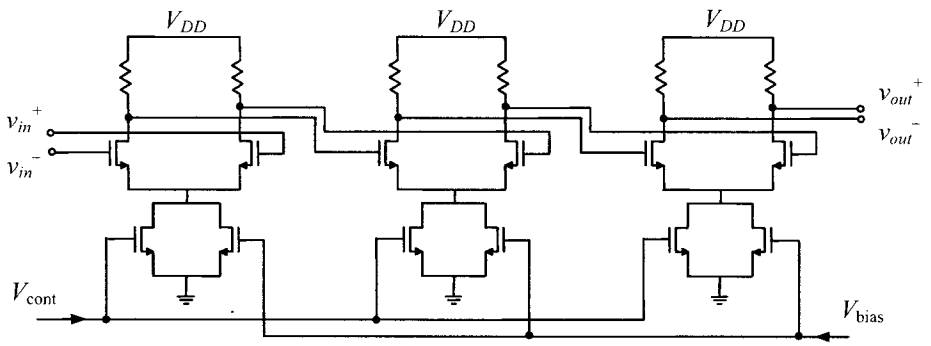


Figure 3.5: A 3-stage voltage controlled oscillator.

3.5. Divider

The divider was formed by cascading 5 divide-by-2/3 stages to produce a minimum divide ratio of 32 and a maximum divide ratio of 63. Using a reference frequency of 40MHz, the possible input frequency range that the divider could function is between 1.28GHz to 2.52GHz, with channel spacing of 40MHz. However, because the synthe-

sizer was designed to operate between 1.6GHz and 2GHz, the division ratio required was only between 40 and 50. The divider architecture for a single stage is as shown in Figure 3.6. This particular circuit is cascaded 5 times to produce the overall divider.

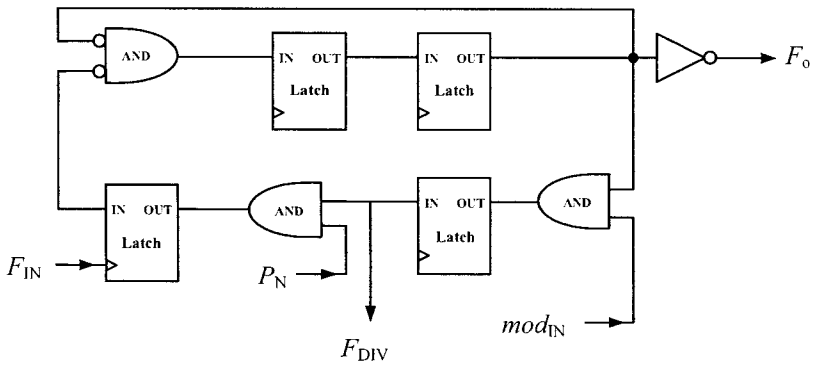


Figure 3.6: Divide-by-2/3 circuit diagram.

The N^{th} individual multi-modulus divide-by-2/3 cell has three differential input signals, a signal input (F_{IN}), a control signal (P_N) for divide-by-2 or divide-by-3 operation and a division return signal (mod_{IN}). Each divide-by-2/3 cell also has 2 differential output signals, a single stage divided output signal (F_o) and a total frequency divider output return signal (F_{DIV}). The output signal F_o is a divided down signal of the input signal F_{IN}. The signal F_o is 1/3 of the frequency of F_{IN} when mod_{IN} and P_N are both enabled, and 1/2 of the frequency of F_{IN} otherwise. The equation defining the division ratio is given by:

$$N = P_1 + 2P_2 + 4P_3 + 8P_4 + 16P_5 + 32 \qquad (11)$$

Therefore, if all P bits are low then the division ratio will be 32 and if all P bits are high then the division ratio will be 63. The control pins were individually routed to

individual bond pads such that each pin could be toggled manually to test for division functionality.

The current of the divider was dominated by the first divide-by-2/3 stage. This stage consumes 1.47mW, which was 50% of the total power dissipated in the divider. Because each stage is operating at half the frequency of the previous stage [7] [8], the current is halved for each successive stage leading to a total power dissipation of 2.94mW for the complete divider.

3.6. Loop Filter

A simple 2^{nd}-order passive filter was implemented for its simplicity, low noise performance and power efficiency. A 2^{nd}-order filter is also better suited towards tweaks and modifications after implementation [9]. The loop filter was implemented such that the synthesizer would have a loop bandwidth natural frequency (ω_n) of 1MHz with the option of being modified to have a loop bandwidth natural frequency up to 2MHz through laser trimming. The elements R, C_1 and C_2 used to obtain a 1MHz loop bandwidth are 2.5KΩ, 200pF and 20pF respectively. The values of elements R, C_1 and C_2 for a 2MHz loop bandwidth are 5KΩ, 50pF and 5pF respectively. By observing Figure 3.7, one can see how it is possible to trim interconnect such that a loop bandwidth of 2MHz is achieved.

The loop damping constant (ζ) was chosen to be 0.707. The settling time of the PLL is approximately 2.5μs. The main driving factor which led towards choosing a high-bandwidth filter was that the loop filter was to be implemented on-chip, therefore die real-estate was minimized as it was important that the loop filter take up as little room as possible.

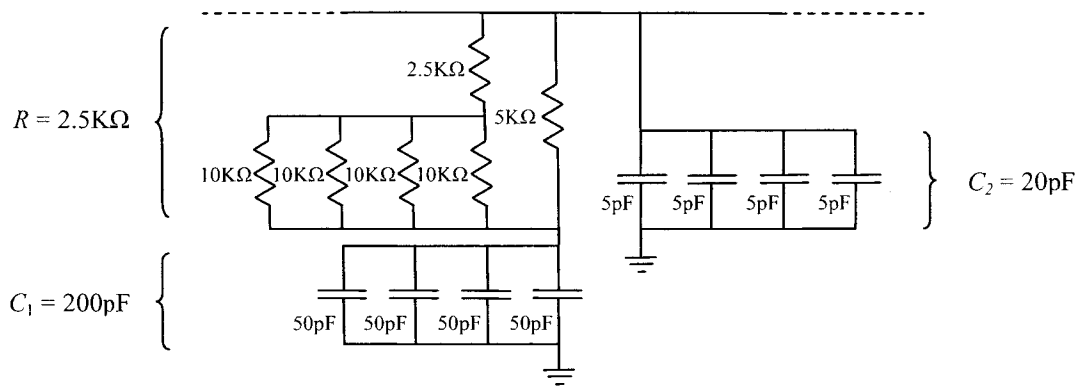


Figure 3.7: 2nd-order passive loop filter.

3.7. Output Buffers

Two output buffers were added to the synthesizer such that the output signal from the VCO as well as the output signal from the divider could be observed using a spectrum analyzer or an oscilloscope. Figure 3.8 shows the output buffer placement relative to the synthesizer. It was essential that the output buffers were capable of driving a 50Ω load as this is the load seen by the buffer when driving either a spectrum analyser or an oscillo-

scope. This was accomplished by constructing a single-ended source follower. However, since the buffer had a high input capacitance, it was necessary to begin by using a series of buffers in which their sizes were gradually scaled upwards so as not to affect the VCO's performance.

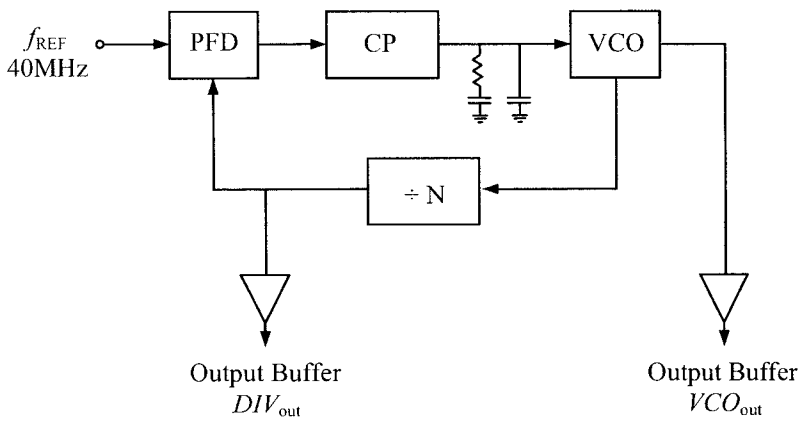


Figure 3.8: Output buffer placement.

A series of 4 CML buffers were implemented with a scaling factor of 2x to drive the source follower. Figure 3.9 illustrates the CML and cascade buffer stages as well as transistor sizing, and Table 3.1 shows the transistor sizing for each stage in the buffer. The total current consumption for the buffer was 11.04mW. Output buffers were implemented for testing purposes only and were therefore discounted in total power dissipation calculations.

Table 3.1: Output buffer transistor sizing.

Stage	1	2	3	4	5[1]
Diff Pair W/L	12.5μ/120n	25μ/120n	50μ/120n	100μ/120n	200μ/120n
Current Source W/L	18μ/600n	36μ/600n	72μ/600n	144/600n	144μ/600n
Power Consumption	480μW	960μW	1.92mW	3.84mW	3.84mW

[1]Source Follower

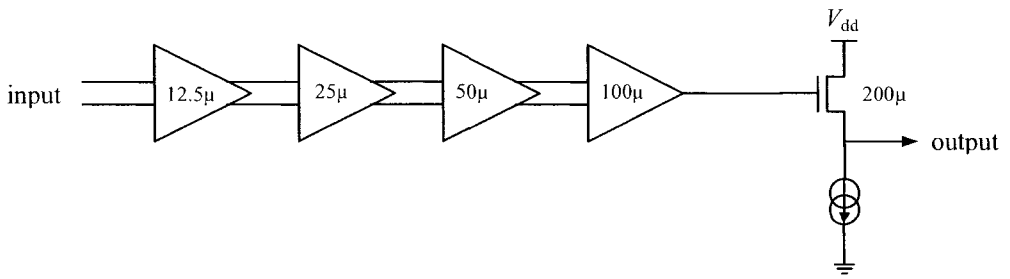


Figure 3.9: Output buffer topology and transistor sizing.

3.8. Interface and Test Circuitry

For testing purposes transmission gates were added in the feedback path of the synthesizer. This allowed for partial testing of the loop if for some reason there was a failure with one of the components in the PLL. Figure 3.10 below shows the placement of the transmission gates in the loop. There are two sections in which the transmission gates are added, one in between the VCO and the divider and another in between the divider and the PFD. If for example the PFD, CP or the VCO weren't working properly, a signal around 1.8GHz could then be sent into the loop and observed through the output buffer which follows the divider (DIV_{out}) to test the divider for functionality. In the same

manner, if the divider was not functioning properly, a signal around 40MHz could be sent into the PFD and then observed through the buffer that follows the VCO (VCO_{out}).

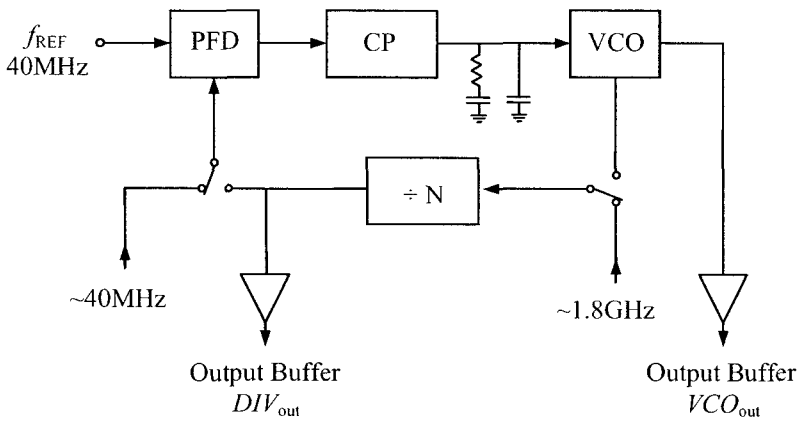


Figure 3.10: Transmission gates for testing.

The transmission gates operate by creating a high impedance open circuit in the feedback circuitry while simultaneously creating a path for test signals to propagate into the system. Figure 3.11 shows the circuitry used to input a high frequency signal into the divider. When the transmission gate toggle signal DIV_{TG} is low, transmission gate *A*, between the VCO and the divider is on, thereby allowing signals to propagate through the control line as expected. At the same time the transmission gate *B* is off, thereby creating a high impedance so as to not load the high frequency output travelling from the VCO to the divider. When the transmission gate toggle signal DIV_{TG} is high, transmission gate *B* is on, thereby allowing an external high frequency test signal to enter the divider (via

bond pad). At the same time, transmission gate *A* is off, thereby creating a high impendence so as to not load the incoming test signal and to protect the circuitry in the VCO.

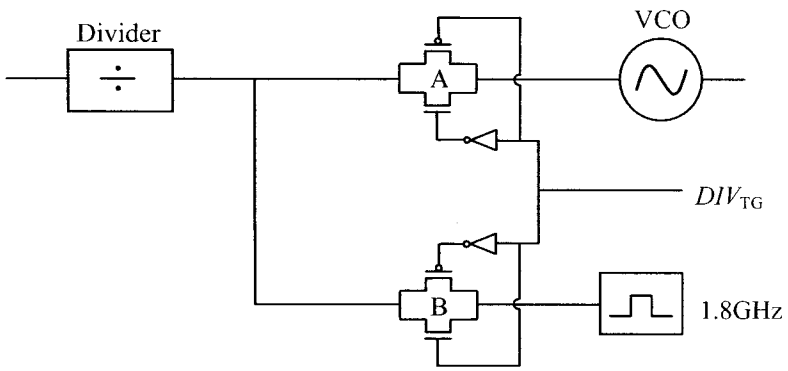


Figure 3.11: Transmission gate architecture between VCO and divider.

The circuitry used to input an external test signal into the PFD is shown in Figure 3.12 and operates in the same fashion as previously discussed. In this case a separate control signal PFD_{TG} is used to toggle the transmission gates.

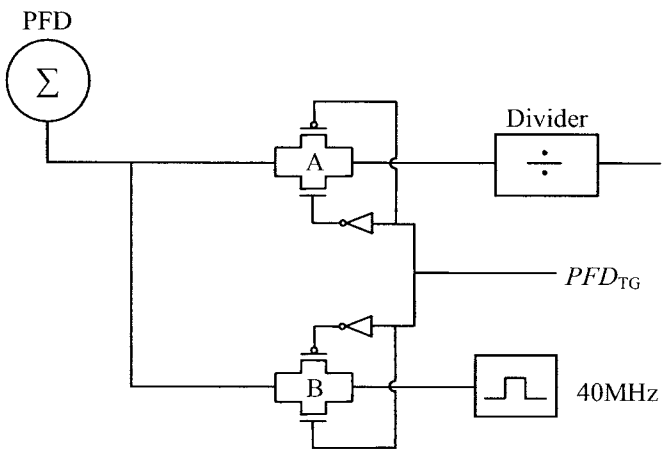


Figure 3.12: Transmission gate architecture between divider and PFD.

To optimize the utilization bond pads any differential signal required by the synthesizer was received as a single-ended signal and then converted to a differential signal on-chip, thereby cutting the number of required bond pads for these signals in half. Examples of signals which use the single-ended to differential circuit as shown in Figure 3.13 are the reference frequency f_{ref}, all five divider control pins P_N and transmission gate control signals DIV_{TG} and PFD_{TG}.

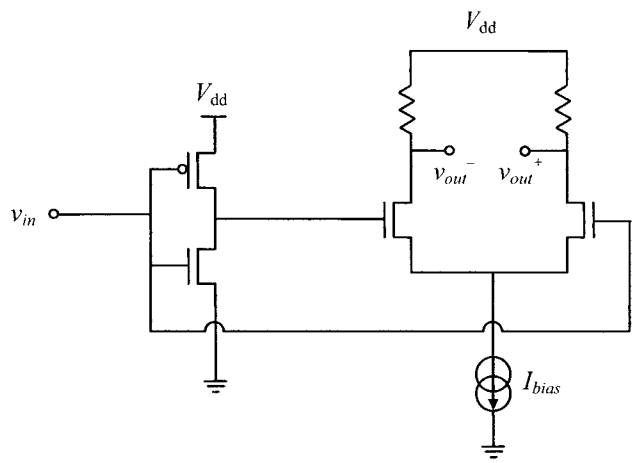


Figure 3.13: Single-ended to differential circuit.

3.9. Safety Buffers

Due to the extra load capacitances added by the output buffers, transmission gates and interconnect in the feedback path of the synthesizer, two safety buffers we added to overcome signal derogation. One directly following the VCO to help drive gate capacitances of the buffer and transmission gates which directly follow it. The other serves the same function but directly follows the divider. The buffers were designed using the CML

architecture consistent with other CML gates or inverters discussed in this thesis. Figure 3.14 shows the placement of the safety buffers relative to the synthesizer architecture.

The VCO safety buffer adds an extra 1.08mW of power consumption to the synthesizer while the divider safety buffer adds an extra 480μW.

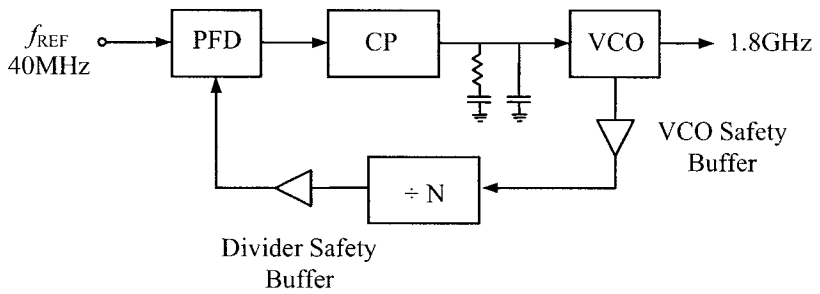


Figure 3.14: Safety buffers.

3.10. Power Routing

To reduce the effect that noise generated by the digital blocks (divider and PFD) has on the analog blocks (charge pump and VCO), separate power supplies were introduced. Another method of isolating the analog blocks from noisy circuitry propagating through the substrate was to add guard rings around both digital and analog blocks. Guard rings and separate power supplies also applied to the output buffer block. The four

main blocks are illustrated in Figure 3.15 below, the remaining silicon was filled using de-coupling capacitors.

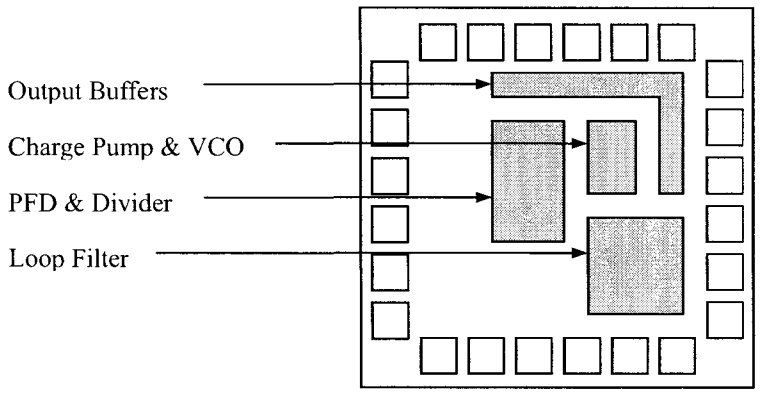


Figure 3.15: Chip placement of main synthesizer blocks.

To gain flexibility when powering the synthesizer during testing, an independent reference current was allocated to each functional block and was tuneable off-chip. Table 3.2 shows the different power supplies and reference current control lines for each functional block.

Table 3.2: Power supply and reference current allocation.

Functional Block	Power (V_{DD} & GND)	Value	Reference Current	Value
Divider	DIV/PFD	1.2V	I_{ref} *DIV*	100µA
PFD	DIV/PFD	1.2V	I_{ref} *PFD*	100µA
Charge Pump	VCO/CP	1.2V	I_{ref} *CP*	100µA
VCO	VCO/CP	1.2V	I_{ref} *VCO*	120µA
Output Buffers	BFR	1.2V	I_{ref} *BFR*	400µA

4. Simulation and Measurement

The synthesizer was fabricated in an 8 metal layer, 1.2V, 0.13μm CMOS process. The total die size of the frequency synthesizer measures 1.4mm^2. The synthesizer measures 0.34mm^2, which includes dual output buffers and the on-chip filter. A photomicrograph of the chip is shown in Figure 4.1. Simulations were done using the Cadence Analog Environment Spectre Tool. The layout portion of the chip design was accomplished using the Virtuoso Layout Editing tool.

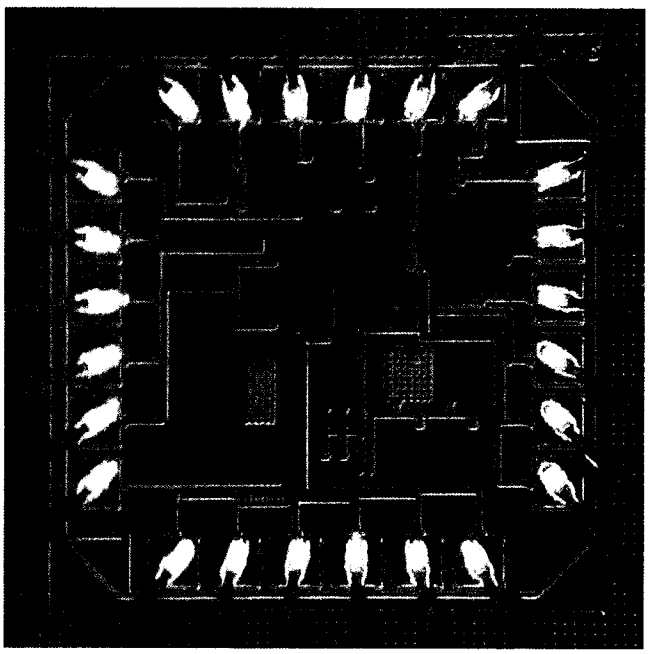


Figure 4.1: Chip micrograph.

4.1. Test Set-up

The chip was set in a 24pin CQF package provided by CMC Microsystems. The package was then mounted onto a printed circuit board also provided by CMC Microsystems. A Hewlet Packard Spectrum Analyzer (HP8564E 30Hz - 40GHz) was used to monitor the output of the VCO, while a Tektronix Oscilloscope (TDS684B 1GHz, 5Gsamples/s) was used to monitor the output following the divider. The synthesizer was powered using an Agilent Power Supply (E3646A) while power consumption and current measurements were performed using a Keithley Source Meter (2400 LV). A 40MHz reference signal was applied using a Rhode and Schwarz Signal Generator (SME06). The test set-up is illustrated in Figure 4.2.

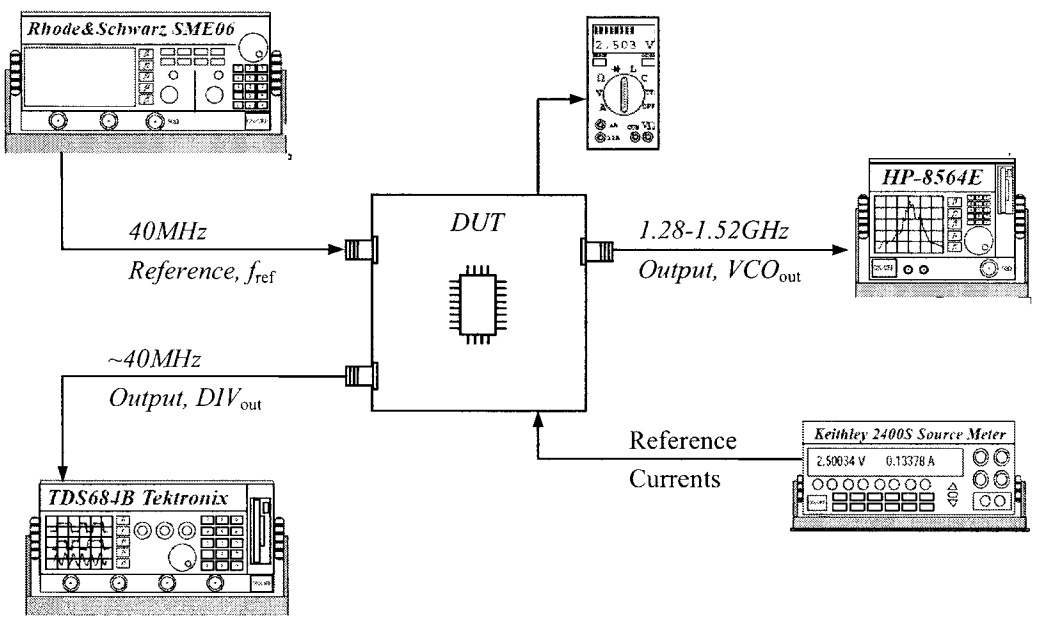


Figure 4.2: Synthesizer test set-up.

4.2. Phase Frequency Detector

The PFD was simulated to operate as illustrated in Figure 4.3. The power consumption of the PFD was simulated to be 504μW. The power consumption of the PFD was measured at DC by turning off all supply voltages and reference currents to other blocks while leaving the supply voltage and reference current required for PFD operation on. Measured power consumption amounted to a slightly higher value of 530μW.

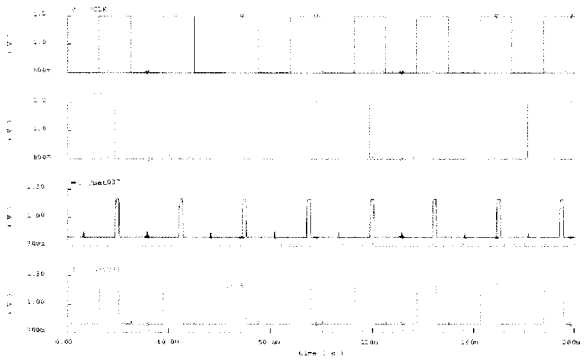


Figure 4.3: PFD simulation plot.

4.3. Charge Pump

As mentioned in previous discussion, when the control voltage on the loop filter varies, the sourcing and sinking abilities by the charge pump's output transistors do not necessarily match. This is illustrated by simulation in Figure 4.4. The charge pumps cur-

rent consumption was simulated to be 240μW, while measured power consumption amounted to 334μW. The power consumption of the charge pump was also measured at DC by turning off all supply voltages and reference currents to other blocks while leaving the supply voltage and reference current required for charge pump operation on.

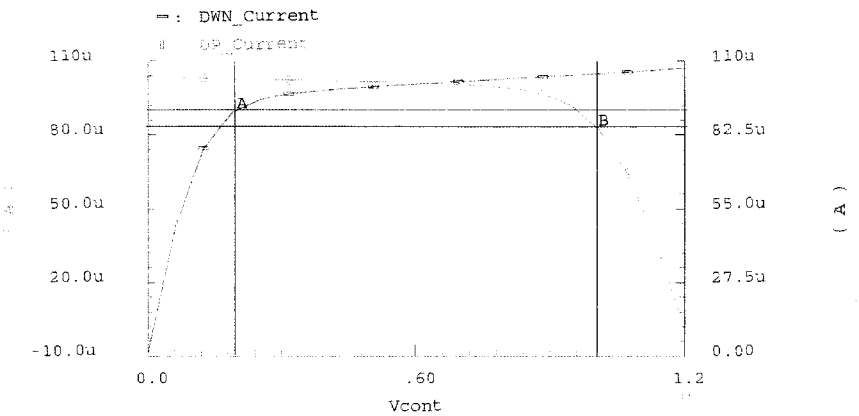


Figure 4.4: Charge pump mismatch simulation.

4.4. Voltage-Controlled Oscillator

The VCO was simulated to have an output frequency range from 1.52GHz to 2.02GHz and a K_{VCO} of 680MHz/V. The actual VCO was characterized by monitoring the control voltage on the loop filter while recording the output frequency. The measured VCO takes on the same basic shape as the simulated VCO and can be seen in Figure 4.5; however, the output frequency of the measured VCO is approximately 300MHz less than

simulated. The frequency range attainable by the actual VCO is now from 1.24GHz to 1.72GHz with a K_{VCO} of approximately 760MHz/V. The causes of the discrepancy between simulated and measured results of the VCO can be attributed to parasitic capacitances which were unaccounted for in the Calibre extraction simulation tool. The output frequency range of the VCO directly affects the possible output frequency range attainable by the synthesizer. Given the possible divide ratios provided by the divider, the synthesizer now has the potential of attaining a frequency range from 1.28GHz to 1.72GHz using divide ratios of 32 to 43 respectively.

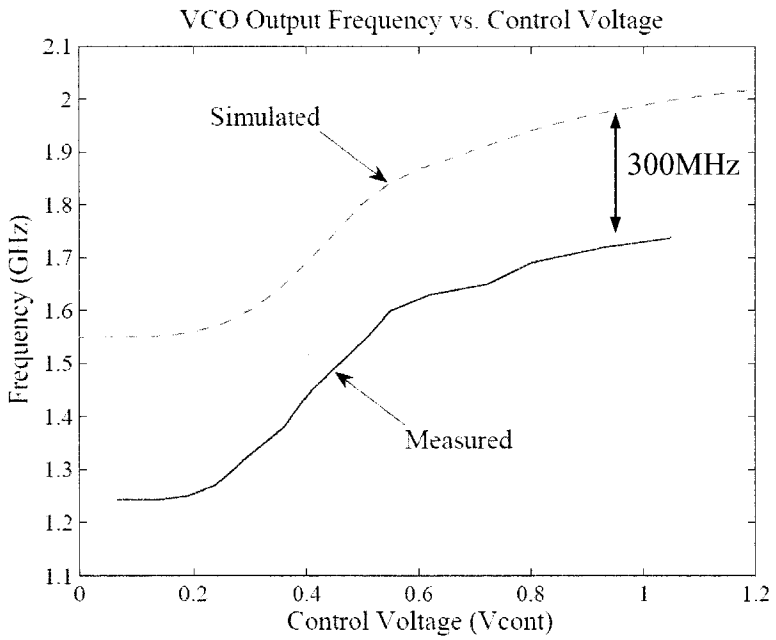


Figure 4.5: VCO simulated and measured.

Post measurement simulations were done to gain a better understanding of the causes behind the frequency shift. Figure 4.6 shows a parametric simulation wherein the capacitance in between VCO inverter stages is swept from 1fF to 20fF. From the figure

it was found that a 12fF increase in capacitance corresponds to a 300MHz decrease in output frequency. Because 12fF is a fairly small value, it can be stated that parasitic capacitances which were unaccounted for in post extraction simulations were most likely the root cause of the VCO output frequency shift.

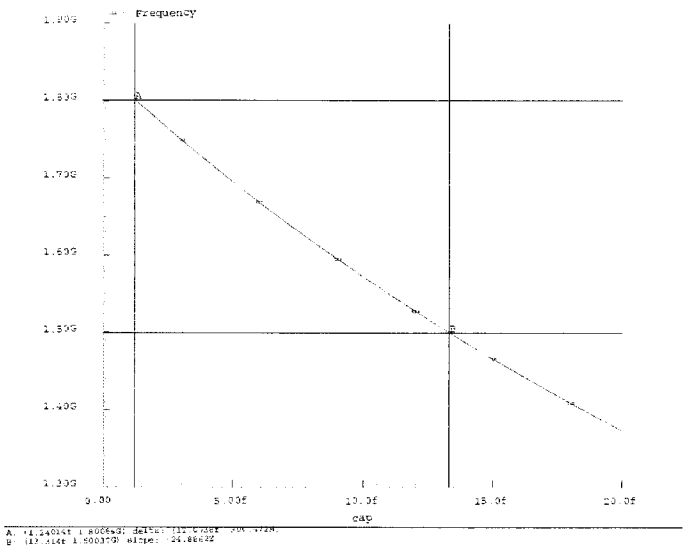


Figure 4.6: VCO frequency analysis.

The simulated power dissipation of the VCO was 600mW while the measured power dissipation was 608mW. The method used to measure power dissipation was at DC and was equivalent to the methods used to measure PFD and charge pump current.

4.5. Divider

A simulation illustrating the divider output signals in between each of the five divider stages is shown in Figure 4.7. The first output signal in the illustration is the di-

vider output signal f_{div} (~40MHz) and the last output signal in the illustration is the VCO input signal (~1.8GHz). It can be seen that the divider output signal has a very small duty cycle of only 5%.

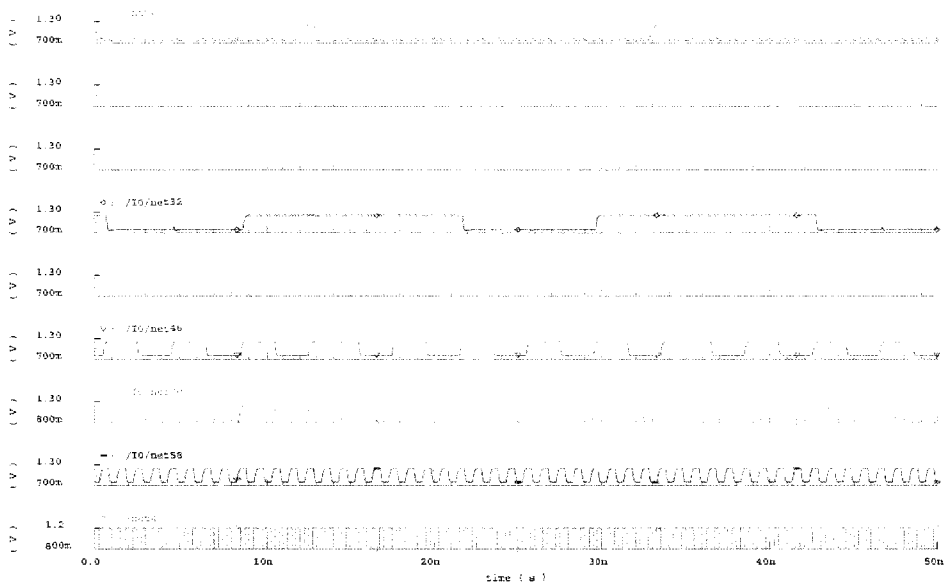


Figure 4.7: Divider output signals.

During measurement of the synthesizer it was found that the divider output signal began to diminish in amplitude due to capacitive loading between divider stages at a frequency of 1.44GHz. Figure 4.8 (a) shows the divider output when the synthesizer is programmed to output 1.44GHz, the signal begins to decrease in amplitude. Figure 4.8 (b) shows the divider output signal at 1.52GHz, at this point the signal is severely degraded, thereby hindering signal propagation between divider stages and eventually leading to overall system failure. Therefore, the synthesizer will effectively operate between the

lower limit of the VCO output frequency and the point at which the divider fails, or between 1.28GHz and 1.52GHz.

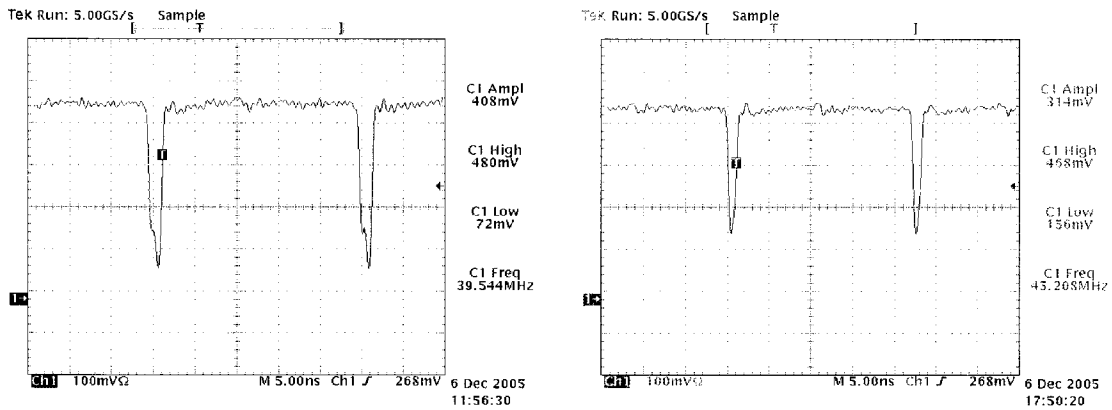


Figure 4.8: Divider output (a) 1.44GHz (b) 1.52GHz

The power consumption of the simulated divider was 2.64mW while the measured power dissipation of the divider was 2.94mW.

4.6. PLL Phase Noise

The phase noise of the synthesizer was simulated using MATLAB (see Appendix B), an illustration depicting the noise contributions from each functional block is shown in Figure 4.9. The synthesizer is expected to have a close in phase noise of -97dbc/Hz at an offset of 1MHz. At higher offset frequencies, the closed loop phase noise is dominated

by the VCO. Given that the VCO uses a ring oscillator architecture, the VCO achieves a respectable -110dBc/Hz at an offset of 10MHz.

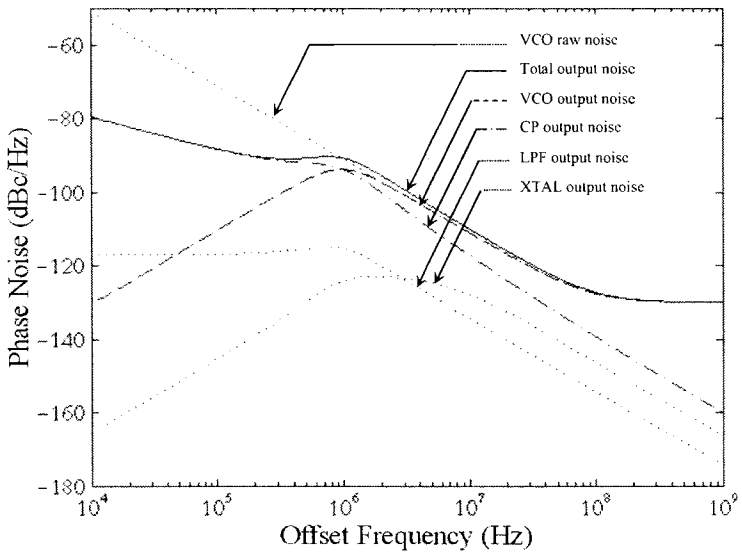


Figure 4.9: Simulated PLL phase noise.

The reference spurs caused by charge pump mismatch were simulated to appear at -50dBc from the carrier signal, Figure 4.10 shows the simulated results.

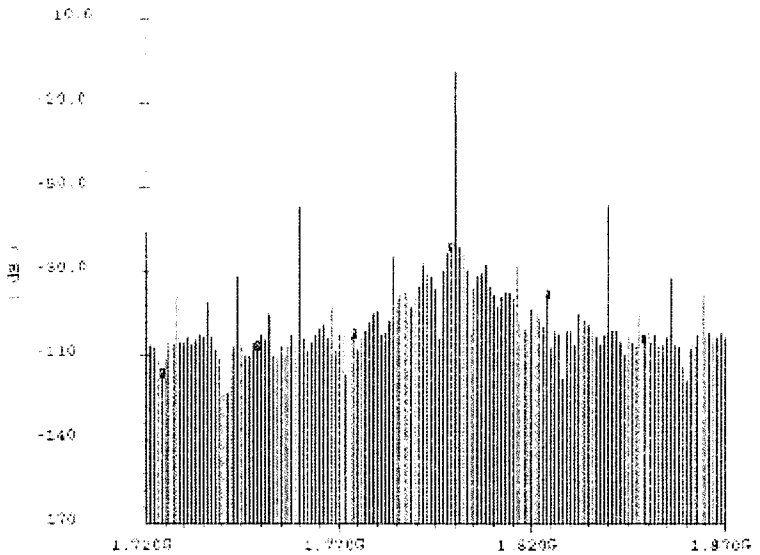


Figure 4.10: Simulated reference spurs.

Measured results for reference spurs were taken at -47dBc from the carrier signal as illustrated by the spectrum analyser screen capture shown in Figure 4.11.

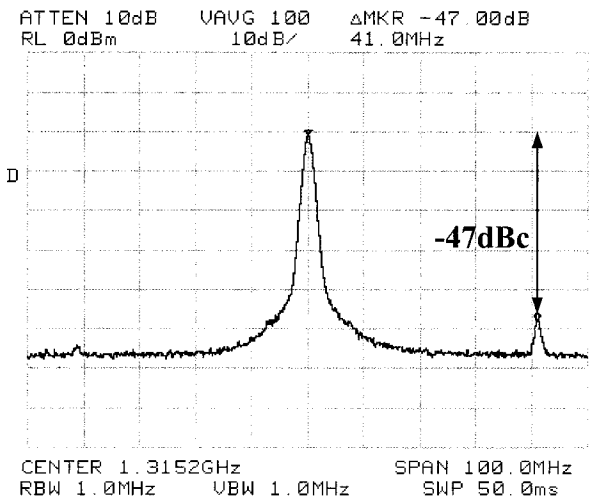


Figure 4.11: Measured reference spurs.

A screen capture depicting the synthesizer noise performance using a special module built into the spectrum analyser is shown in Figure 4.12 The synthesizer achieves a close-in phase noise (PN) of –88dBc/Hz at an offset of 1MHz. At higher offset frequencies the closed loop phase noise is dominated by the VCO, which achieves a PN –104dBc/Hz at an offset of 10MHz and is shown in Figure 4.13.

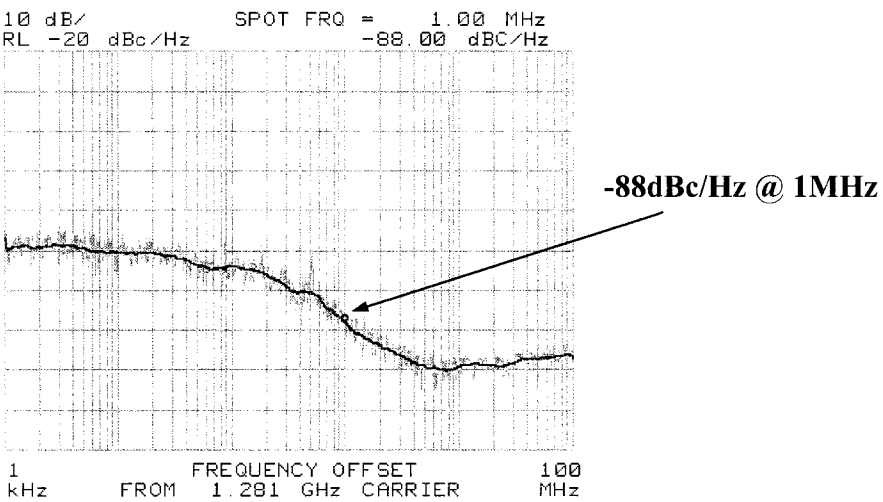


Figure 4.12: Measured phase noise @1MHz offest.

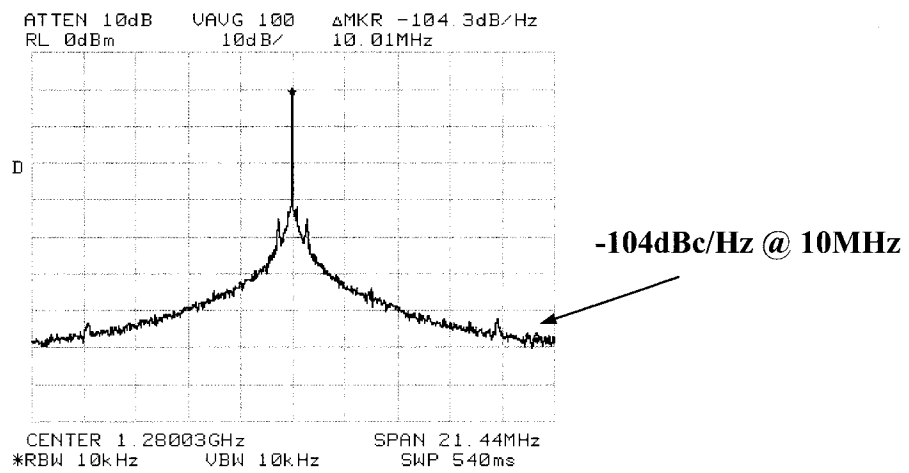
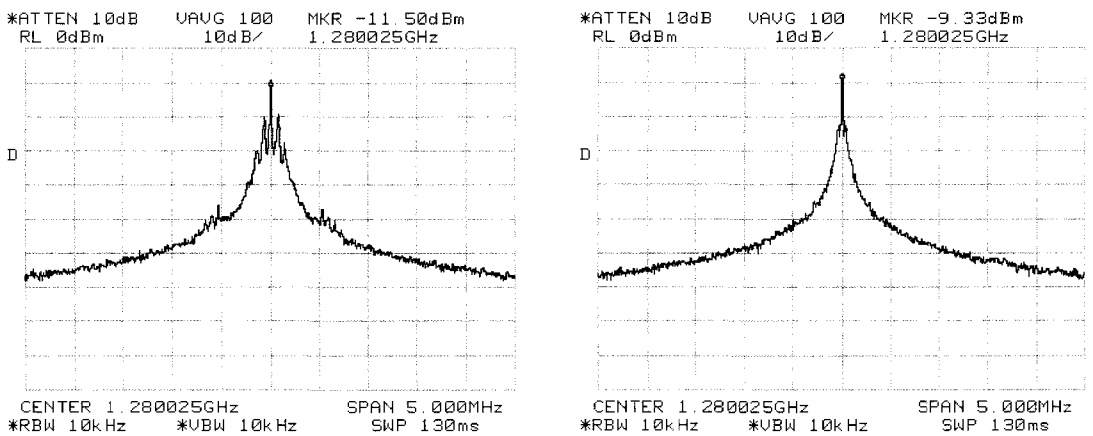


Figure 4.13: Measured phase noise @10MHz offset.

A brief investigation was performed to decipher whether there are any performance advantages to be had if the power supplies of the digital blocks (PFD and divider) and the analog blocks (charge pump and VCO) are kept separate. A conventional power supply was used to power the digital blocks while a battery set to 1.2V was used to supply power to the analog blocks. Figure 4.14 shows the output spectrums of the two cases. In Figure 4.14 (a) we see that the output signal spectrum of the frequency synthesizer with shared power supply is noisier than when using independent power supplies for digital and analog blocks, Figure 4.14 (b). The improvement performance measures are tabulated in Table 4.1. Both output power and phase noise measures see great improvements.



(a) (b)

Figure 4.14: (a) Shared power supply (b) independent power supply.

Table 4.1: Shared power supply vs. independent power supply

Specifications	Shared Power Routing	Independent Power Routing
Output Power	-11.5dBm	-9.3dBm
PN @ 1MHz	-80.2dBc/Hz	-86.3dBc/Hz
PN @ 10MHz	-91.8dBc/Hz	-104.3dBc/Hz

4.7. Overall Performance

The transient response of an 80MHz frequency step was observed by switching the divider ratio from 32 to 34 (1.28GHz to 1.36GHz) and can be seen in Figure 4.15 below. The settling time was measured to be 6.5μs for an 80MHz step in frequency. The simulated settling time required for an 80MHz step in frequency was 2.5μs. An investigation as to the cause of the discrepancy between simulated and measured settling times was done by analysing the divider switching signal against the control line voltage level. It was found that the signal used to switch the divider had a slow rise time, which may have attributed to the extra delay in the frequency synthesizers settling time. A 1pF, 1MΩ probe was used to measure the voltage on the control line such that the added capacitance of the probe did not affect the loop filter value and loop dynamics.

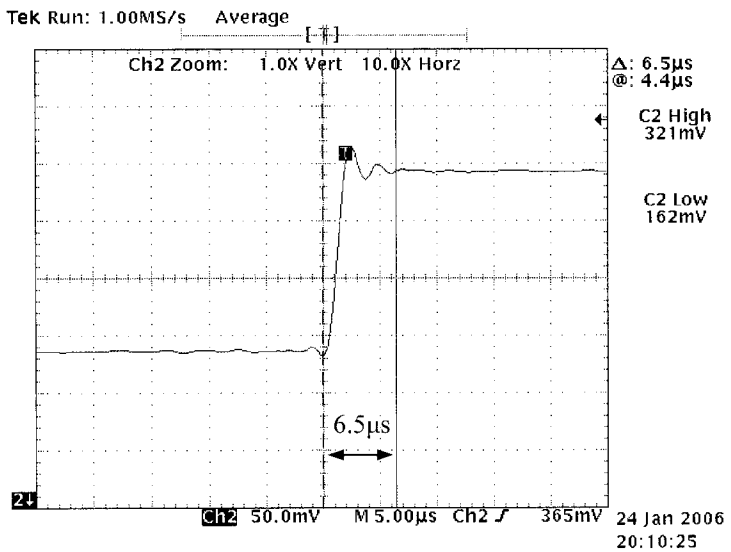


Figure 4.15: Channel step transient response.

The loop bandwidth was also verified using the measured transient response of the frequency step. By analyzing the period of the ringing waveform in the transient response (Figure 4.16) it is possible to deduce the loop natural frequency ω_n, whereby

$$\omega_n = [(2.4\mu s)^{-1}] \cdot 2\pi = 2.62 Mrad/s . \quad (12)$$

The loop bandwidth ω_{3dB} can then be determined using,

$$\omega_{3dB} = \omega_n \cdot (1 + \varsigma\sqrt{2}) = 5.24 Mrad/s . \quad (13)$$

Finally the loop bandwidth in Hertz is given by,

$$f_{3dB} = 833.27 KHz . \quad (14)$$

Therefore, the simulated loop bandwidth was 1MHz whereas the measured loop bandwidth was 833kHz. It was concluded that additional capacitance either on chip or in the measurement equipment added to the capacitance on the loop filter, which in turn lead to a smaller loop bandwidth.

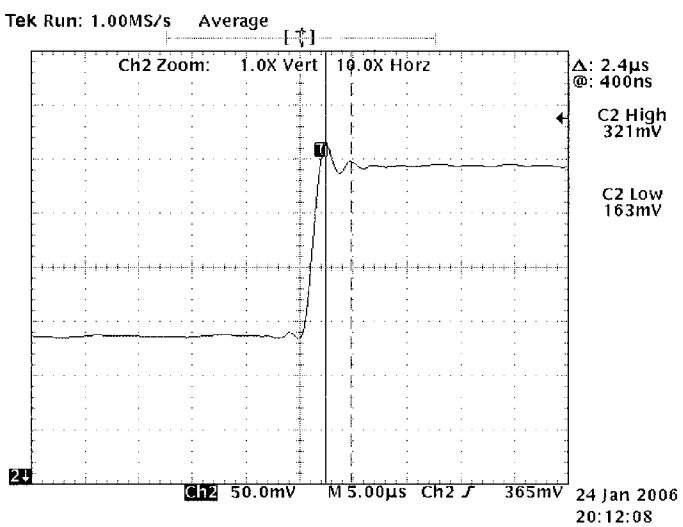


Figure 4.16: Measuring ω_n using the transient response.

The simulated and measured results of the synthesizer are summarised below in Table 4.2. The total power consumption of the synthesizer is 5.8mW as compared to the simulated power consumption of 5.06mW.

Table 4.2: Overall synthesiser performance.

Specification	Simulated	Measured
Supply voltage	1.2V	1.2V
Output Frequency range	1.56 - 2GHz	1.28 - 1.52GHz
Charge pump bias current	100μA	---
VCO Tuning Range	1.52 - 2.02GHz	1.24 - 1.72GHz
K_{VCO}	680MHz/V	760MHz/V
Main Loop filter capacitator	200pF	---
Loop Filter Resistor	2.6KΩ	---
Secondary Loop filter capacitor	20pF	---
Loop corner frequency	1MHz	833kHz
Settling Time	2.5μs	6.5μs
Frequency step	40MHz	40MHz
In-band PN @ 1MHz offset	-97dBc/Hz	-88dBc/Hz
PN @ 10MHz offset	-110dBc/Hz	-104dBc/Hz
Ref. spur @40MHz offset	-50dBc	-47dBc
Divider power	2.64mW	2.94mW
VCO power	0.6mW	0.608mW
CP power	0.24mW	0.334mW
PFD power	0.504mW	0.530mW
In-line Buffers	1.08mA	1.41mW
Total power	5.06mW	5.80mW

5. Summary and Conclusions

5.1. Summary

In this thesis a functional multi-gigahertz synthesizer was designed and implemented in 0.13μm CMOS technology. The synthesizer was designed to operate with high efficiency in a 1.2V environment using CML circuit topology. The synthesizer exhibits a tri-state phase frequency detector, a fully differential charge pump, a 2^{nd}-order on-chip loop filter, a voltage-controlled ring oscillator and an integer-*N* multi-modulus divider. Achieving a total power dissipation of 5.8mW, the synthesizer operates in a frequency band from 1.28GHz to 1.52GHz. The synthesizer achieves a close-in phase noise of –82dBc/Hz at an offset of 1MHz and a phase noise of –99dBc/Hz at an offset of 10MHz. Reference spurs at 40MHz offsets were -47dBc.

5.2. Conclusions

The designed synthesizer was operational and performed 300MHz less than expected. The difference in frequency was attributed to parasitic capacitances. The synthe-

sizer was proven to be operational within 16% of the simulated power dissipation. The noise performance of the synthesizer was within 10% of the simulated estimates. Channel selection was verified and proven to be operational between the frequency of 1.28GHz and 1.52GHz. Table 5.1 refers to the same table as described in section 1.2, it shows that a field of merit of 3.8 exceeds that of all other synthesizer designs.

Table 5.1: Publicized low power synthesizer comparison.

Reference	Power	Frequency	Technology	FOM
[4]	23mW	5.5GHz	0.25μm CMOS	4.2
[8]	22.6mW	1.76GHz	0.35μm BiCMOS	12.8
[9]	22mW	900MHz	0.5μm AMI C5N	24.4
[10]	22mW	2.4GHz	0.18μm CMOS	9.2
[6]	15mW	900MHz	0.8μm CMOS	16.7
[7]	12mW	900MHz	0.35μm CMOS	13.3
This Work	**5.8mW**	**1.52MHz**	**0.13μm CMOS**	**3.8**

5.3. Future Work

There are further methods to quantify the performance of this synthesizer that have not been implemented. There are also methods that could be undertaken in a re-design such that the synthesizer's performance is improved.

Some possibilities for improved output and noise measurements such as using a crystal oscillator in lieu of a noisier signal generator would have most likely lead to a

cleaner VCO output signal. Another method to reduce noise would have been to apply power using batteries rather than a noisier power supply.

Future design work may include the implementation of a sigma-delta ($\Sigma\Delta$) modulator to create a fractional-N frequency synthesizer. It would also be imperative to alter the design such that all high speed blocks take into account parasitic capacitances which were unaccounted for in simulations.

6. References

[1] B. Zhang, P. E. Allen, J. M. Huard, "A fast switching PLL frequency synthesizer with an on-chip passive descrete-time loop filter in 0.25-μm CMOS," IEEE J. Solid-State Circuits, vol. 38, pp. 855-865, June 2003.

[2] M. Yamashina, H. Yamada, "An MOS current mode logic (MCML) circuit for low-power sub-GHz processors," IEICE Trans. Electron., vol. E57-C, pp. 1181-1187, Oct. 1992.

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[7] E. Hegazi, A. Abidi, "A 17-mW transmitter and frequency synthesizer for 900-MHz GSM fully integrated in 0.35-μm CMOS," IEEE J. Solid-State Circuits, vol. 38, pp. 782-792, May, 2003.

[8] R. Ahola, K. Halonen, "A 1.76-GHz 22.6-mW $\Delta\Sigma$ fractional-N frequency synthesizer", IEEE J. Solid-State Circuits, vol. 38, pp. 138-140, Jan. 2003

[9] K. Waheed, K. Desai, P. Seddighrad, F. M. Salam, "A completely integrated, low noise, low power CMOS frequency synthesizer for GSM communications", MWSCAS, vol 3, pp. 540-543, Aug. 2002.

[10] S. K. Singh, T. K. Bhattacharyya, A. Dutta, "Fully integrated CMOS frequency synthesizer for ZigBee aplications", VLSID, pp. 780-783, Jan. 2005.

Appendix A

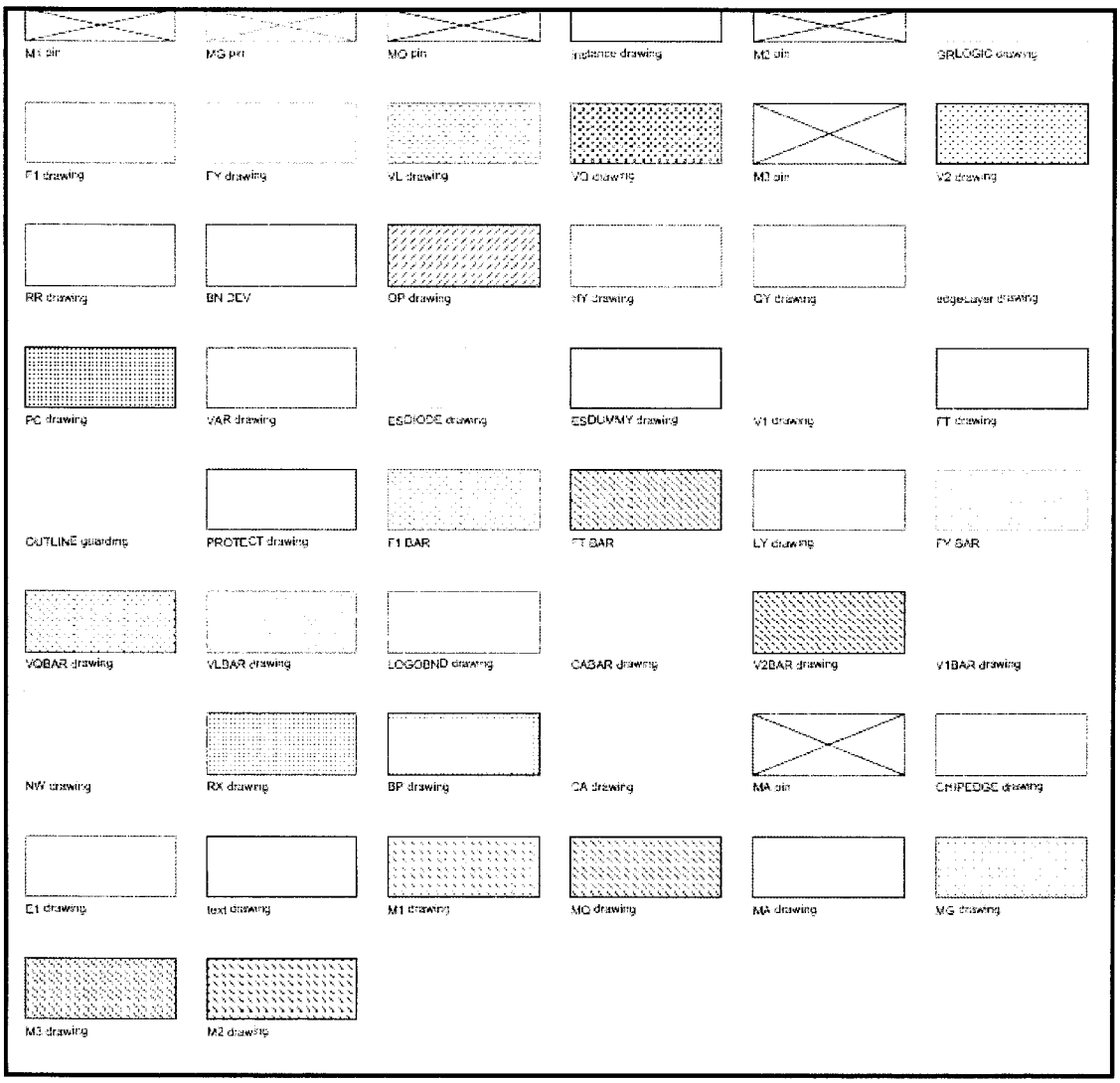
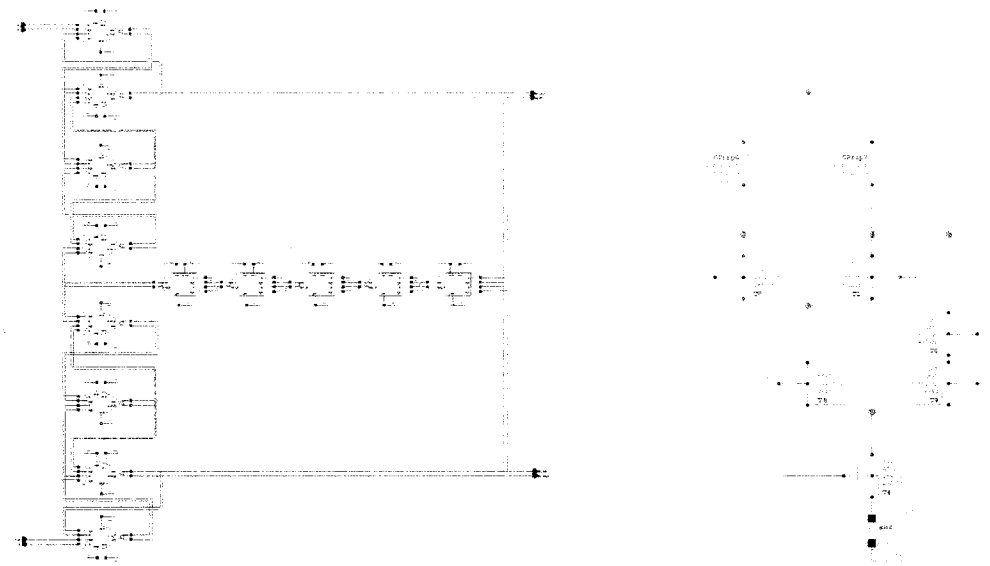


Figure A.1: Legend depicting layout colour scheme and physical layer.

A.1. Phase Frequency Detector



(a) (b)

Figure A.2: (a) PFD schematic (b) PFD NOR gate schematic.

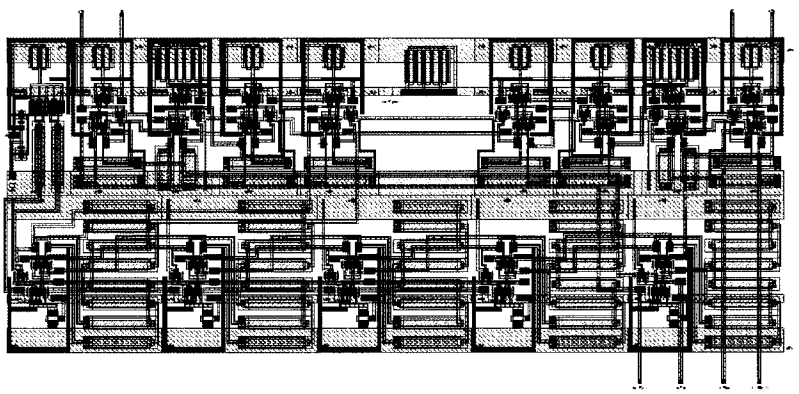


Figure A.3: PFD layout.

A.2 Charge Pump

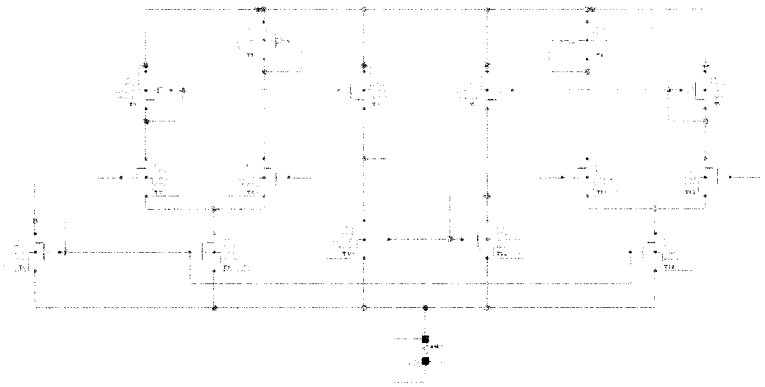


Figure A.4: Charge pump schematic.

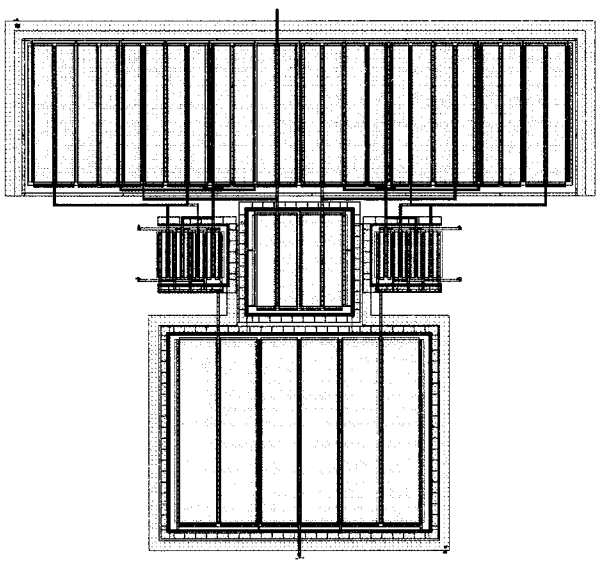


Figure A.5: Charge pump layout.

A.3 Voltage-Controlled Oscillator

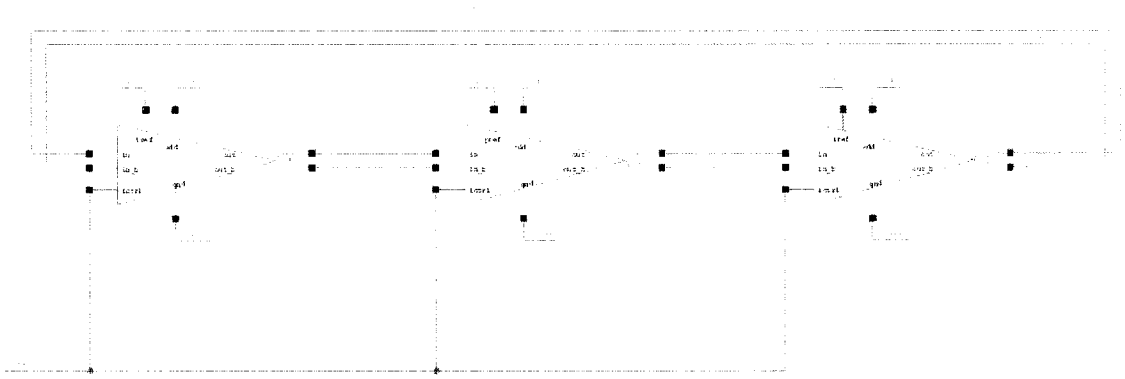


Figure A.6: VCO schematic.

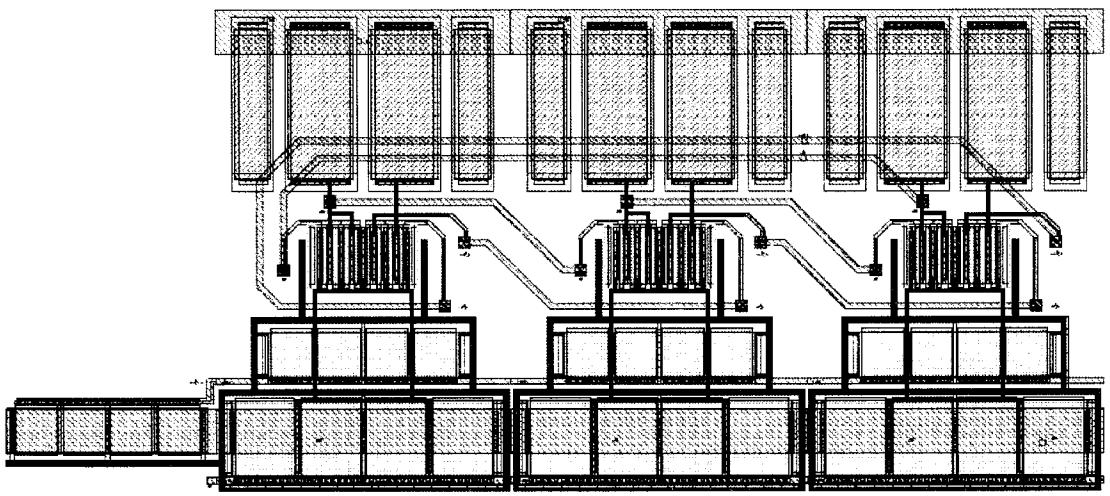


Figure A.7: VCO layout.

A.4 Divider

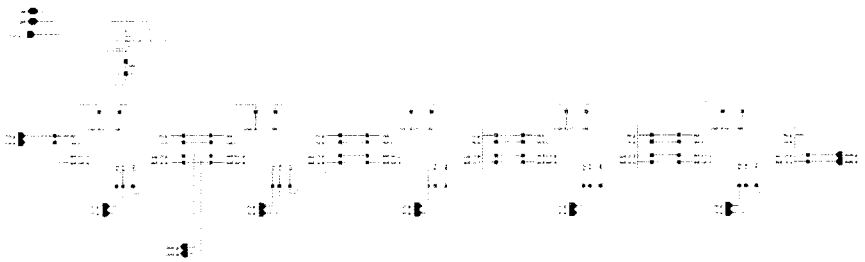


Figure A.8: 5-stage divider.

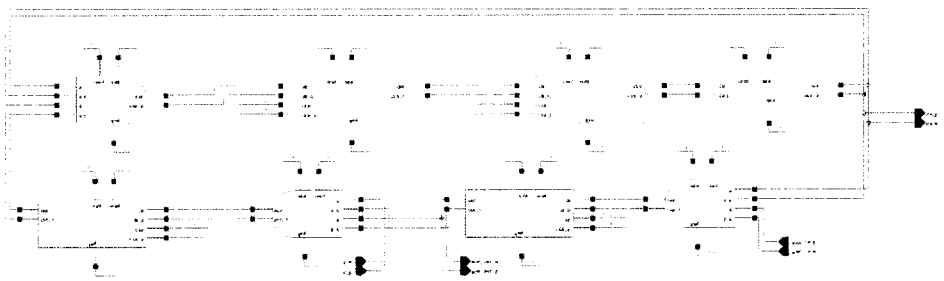


Figure A.9: Divide-by-2/3 stage.

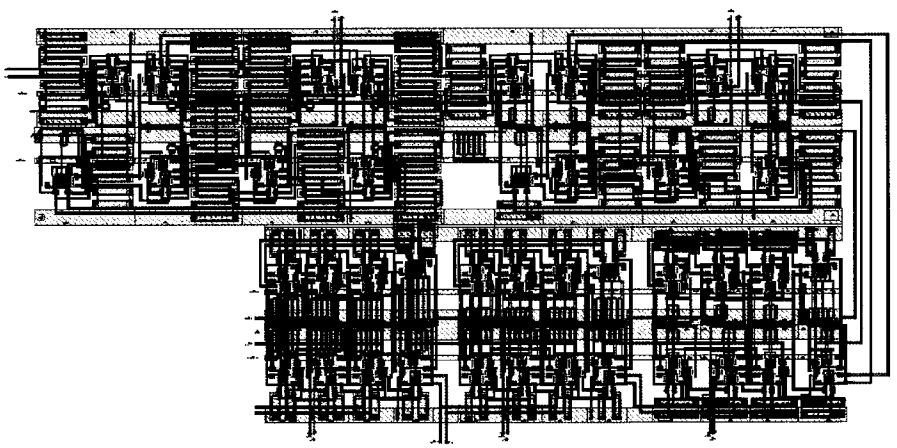


Figure A.10: Divider layout.

A.5 Loop Filter

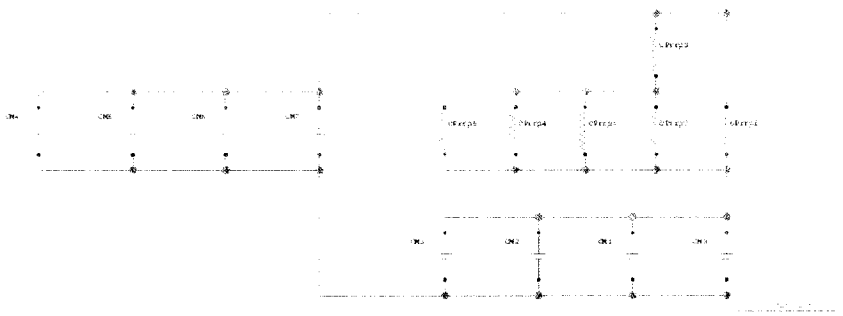


Figure A.11: Loop filter schematic.

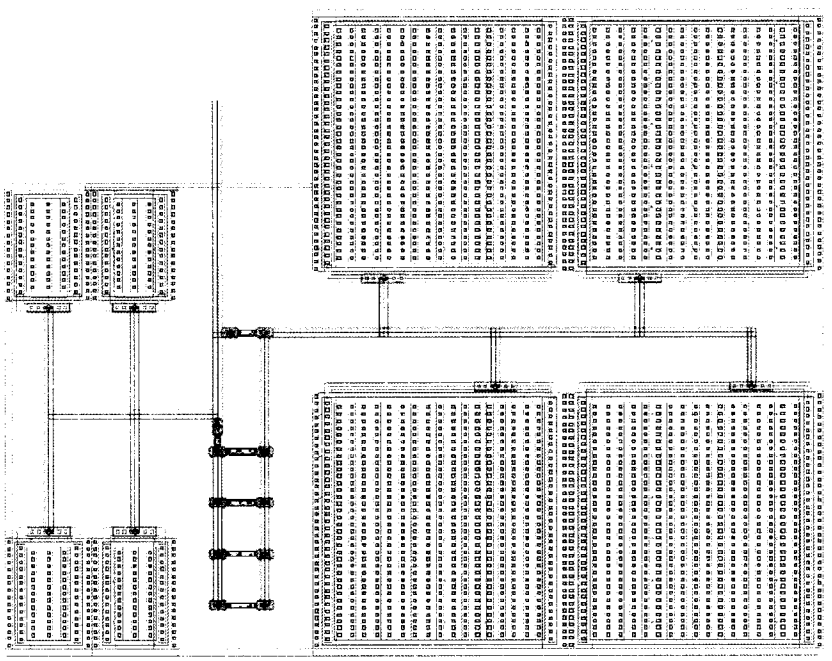


Figure A.12: Loop filter layout.

A.6 Output Buffers

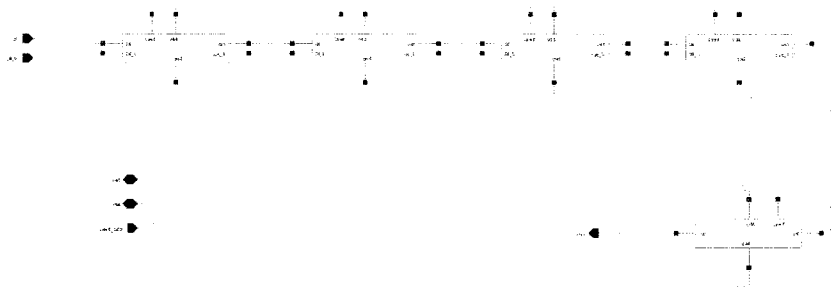


Figure A.13: Output buffer schematic.

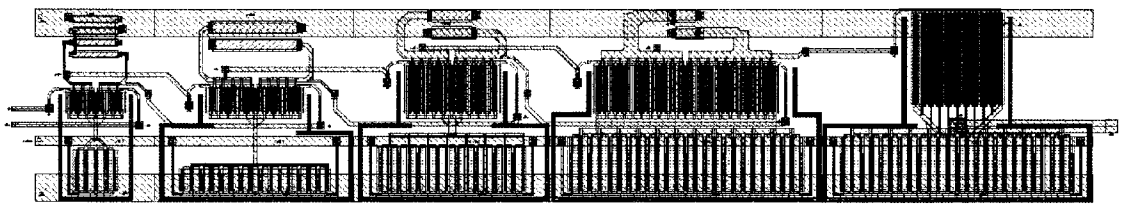


Figure A.14: Output buffer layout.

A.7 Interface and Test Circuitry

ESD

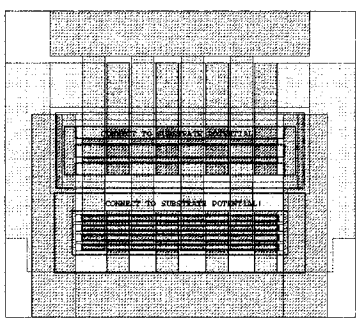
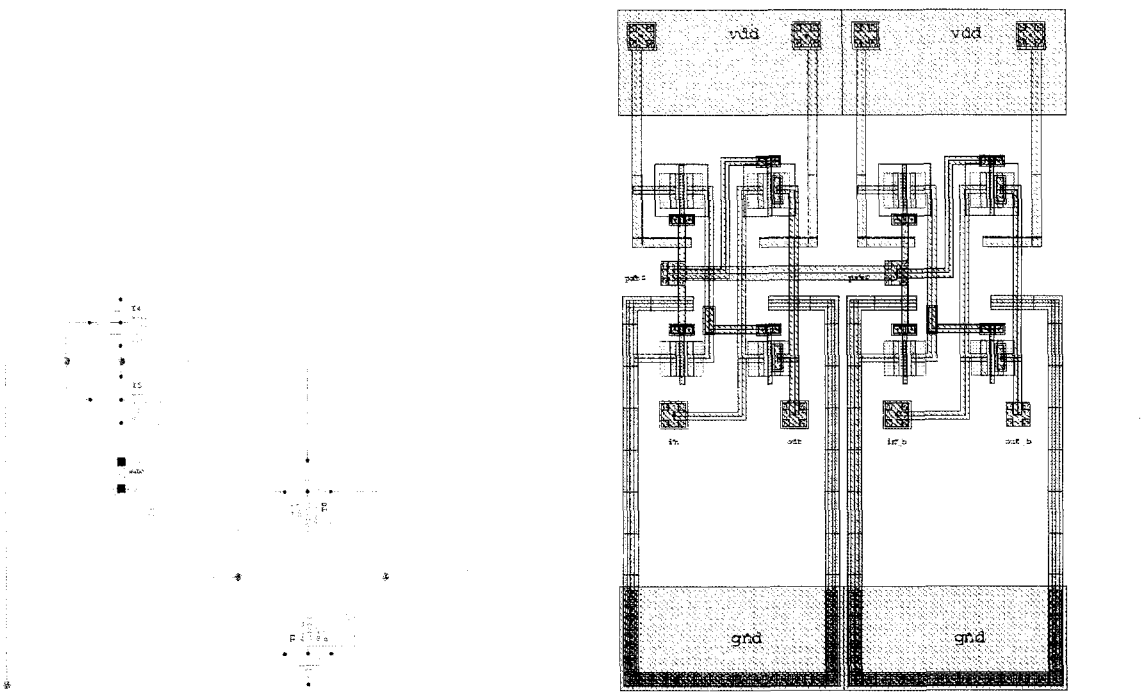


Figure A.15: ESD layout.

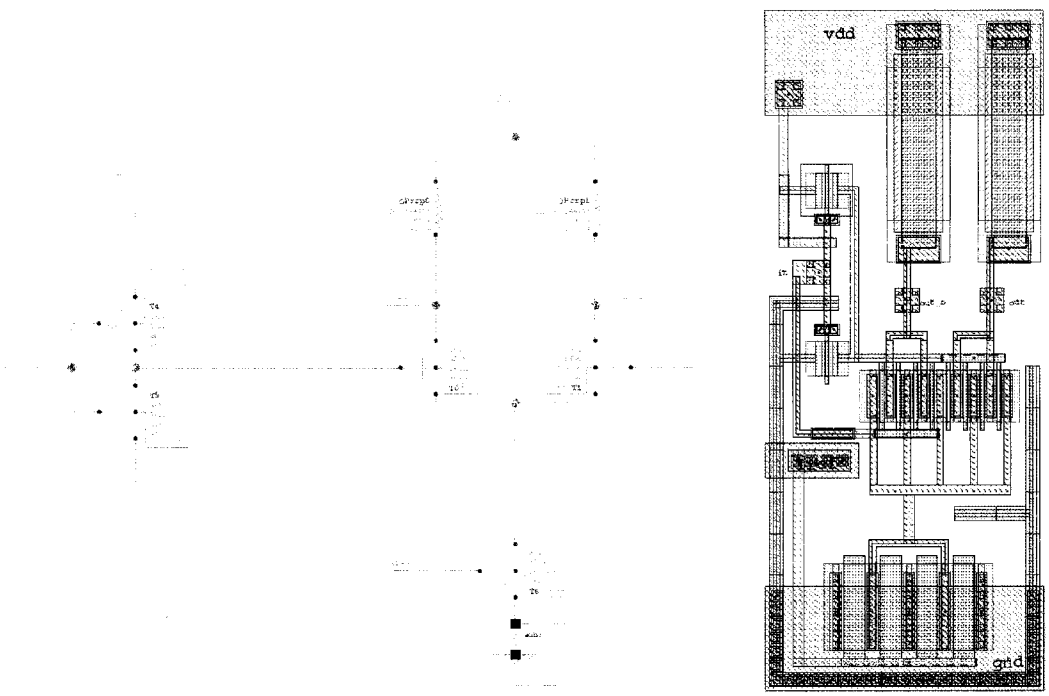
Transmission Gates



(a) (b)

Figure A.16: Transmission gate (a) schematic (b) layout.

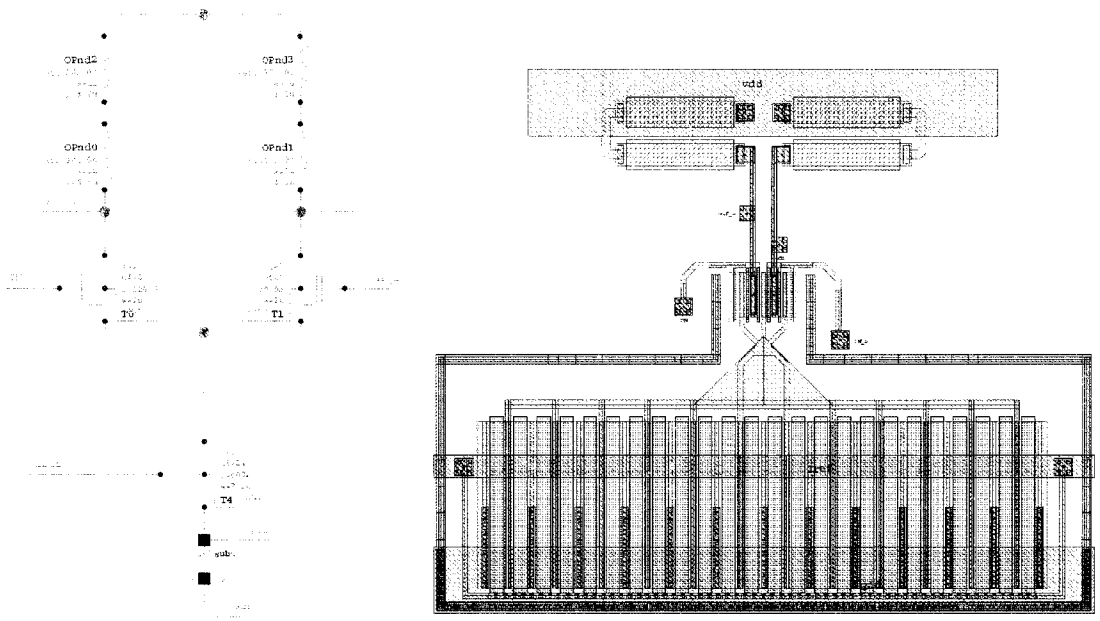
Single-ended to Differential



(a) (b)

Figure A.17: Single-ended to differential (a) schematic (b) layout.

Safety Buffers



(a) (b)

Figure A.18: Feedback safety buffer (a) schematic (b) layout.

A.8 Complete Chip Layout

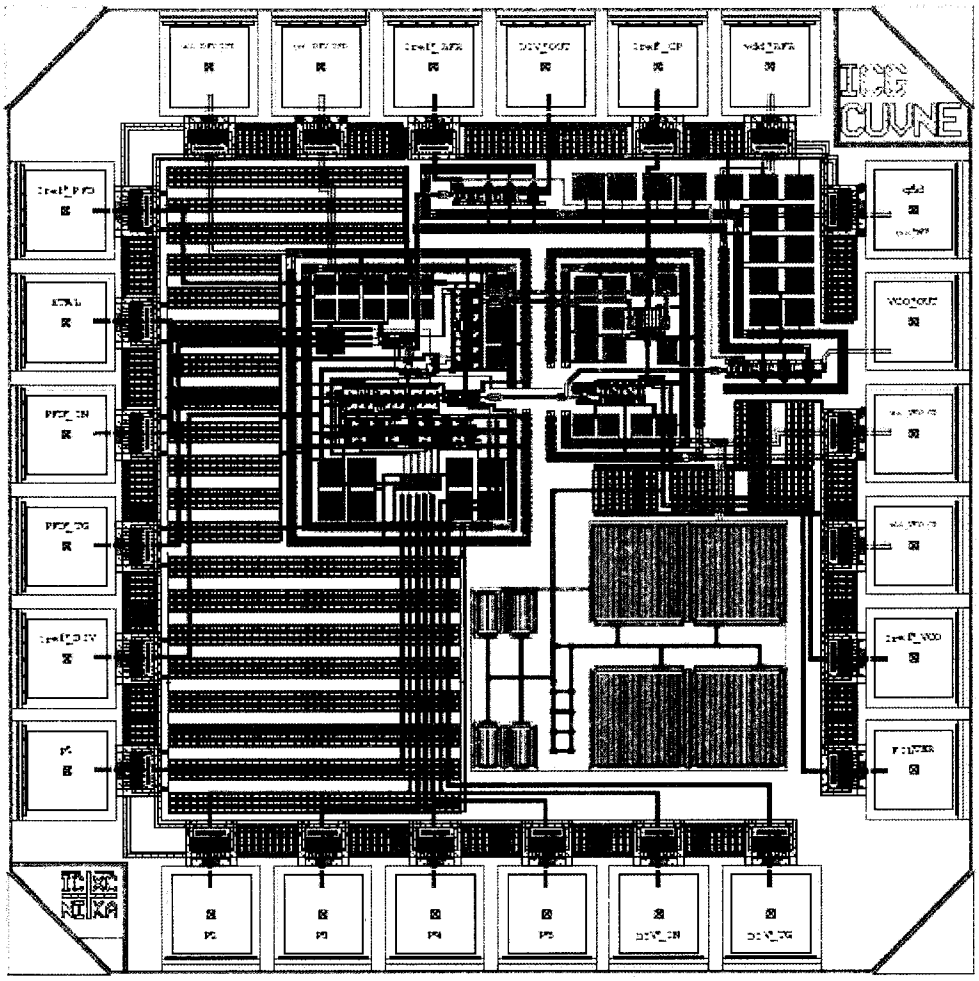


Figure A.19: Complete synthesizer layout.

Appendix B

Phase Noise MATLAB code

```
%
% Noise Analysis of PLL
% Vincent Karam
%
%
function phase_noise(zeta,w3db)

N = 45;
Kvco = 2*pi*400e6;                          % rad/V
fref = 40e6;                                % Hz
wn = loop_bw(w3db, zeta, 'a');              % rad
Icp = 100e-6;
c =  find_c1(Icp, Kvco, N, wn);              %c1
c2 = c/10;                                  %c2
r  = find_r(zeta, N, wn, Icp, Kvco);
Kphase = Icp/(2*pi);

CP_noise = 11.98e-12;  %@150kHz              %Output noise A/sqrt(Hz),
not input-refered phase noise

QL = 8e4;                                  % Q of xtal

% frequency range sweep
start = 1e4;    %Hz
stop = 1e9;     %Hz
step = 500;     %Hz


freq=start:step:stop;    %Hz
w = freq*2*pi;          %rad

      %grouped terms to save space
    partA = ((Icp*Kvco)/(2*pi*c*N));

    PNvco = sqrt(((31.5e3)./((w).^2)) + 100e-15);
    PNvco_out = ( [(j*w).^2]./[(j*w).^2 + (j*w).*partA*r*c + partA] ).*
PNvco ; %PNvco mult by transfer function
    PNvco_log = 20*(log10(abs(PNvco)));     %raw vco phase noise
    PNvco_out_log = 20*(log10(abs(PNvco_out)));  %in loop vco phase
noise
```

```
    PNcp2 = CP_noise/Kphase;
    PNcp = (2.5e-12 + (3.5e-9)./(sqrt(w/(2*pi))))/Kphase;
    PNcp_out =  ( [partA*N*(1 +(j*w)*r*c)]./[(j*w).^2 + (j*w)*partA*r*c
+ partA] ).* PNcp;
    PNcp_out_log = 20*(log10(abs(PNcp_out)));

    PNfilter = [1/(r*Kphase)]*abs( [sqrt(1.6e-20*r)*(j*w)]./[(j*w) +
(1/(c2*r))] );    %note 4kT = 1.6*10e-20
    PNfilter_out = ( [partA*N*(1 +(j*w)*r*c)]./[(j*w).^2 +
(j*w)*partA*r*c + partA] ).*PNfilter;
    PNfilter_out_log = 20*(log10(abs(PNfilter_out)));

    PNxtal = sqrt(1e-15*[1 + [(fref*2*pi)./(2*w*QL)].^2 ]);
%noise floor of xtal -150dBc/Hz
    PNxtal_out = ( [partA*N*(1 +(j*w)*r*c)]./[(j*w).^2 +
(j*w)*partA*r*c + partA] ).*PNxtal;
    PNxtal_out_log = 20*(log10(abs(PNxtal_out)));


    %take the magnitude? Because you don't want imaginary numbers!
    PNtotal_out = sqrt(abs(PNvco_out).^2 + abs(PNcp_out).^2 +
abs(PNfilter_out).^2 + abs(PNxtal_out).^2);
    PNtotal_out_log = 20*(log10(abs(PNtotal_out)));

    %function_handle (@)
    PNvco_out_w     = @(w) abs(([(j*w).^2]./[(j*w).^2 +
(j*w).*partA*r*c + partA] ).* sqrt((39.5./((w).^2)) + 100e-15)) .^2;
    PNcp_out_w      = @(w) abs(( [partA*N*(1 +(j*w)*r*c)]./[(j*w).^2 +
(j*w)*partA*r*c + partA] ).* PNcp2) .^2;
    PNfilter_out_w  = @(w) abs(( [partA*N*(1 +(j*w)*r*c)]./[(j*w).^2 +
(j*w)*partA*r*c + partA] ).* [1/(r*Kphase)].*abs( [sqrt(1.6e-
20*r)*(j*w)]./[(j*w) + (1/(c2*r))] ) ) .^2;
    PNxtal_out_w    = @(w) abs(( [partA*N*(1 +(j*w)*r*c)]./[(j*w).^2 +
(j*w)*partA*r*c + partA] ).*  sqrt(1e-15*[1 +
[(fref*2*pi)./(2*w*QL)].^2 ])) .^2  ;

    lower_limit_w = 100*2*pi;   %Rad
    upper_limit_w = 10e6*2*pi;  %Rad

    quad_vco = quad(PNvco_out_w,lower_limit_w,upper_limit_w,1e-10);
%1e-10 is the tolerance factor, had to be increased from default 1e-6
    quad_cp =quad(PNcp_out_w,lower_limit_w,upper_limit_w,1e-10);
    quad_filter = quad(PNfilter_out_w,lower_limit_w,upper_limit_w,1e-
10);
    quad_xtal = quad(PNxtal_out_w,lower_limit_w,upper_limit_w,1e-10);

    quad_total =   quad_vco + quad_cp +  quad_filter +  quad_xtal;
    Jitter =  [(180*sqrt(2))/pi]*[sqrt(quad_total/(2*pi))];
%div by 2*pi from Hz to rad

disp([' The RMS Jitter from ', num2str(lower_limit_w/(2*pi),'%0.3g'),
' Hz to ', num2str(upper_limit_w/(2*pi),'%0.3g'), ' Hz is ',
num2str(Jitter,'%0.3g'), ' degrees']);
```

```
semilogx(freq,PNvco_log,':k',freq,PNvco_out_log,'--
k',freq,PNcp_out_log,'-
.k',freq,PNfilter_out_log,':k',freq,PNxtal_out_log,':k',freq,PNtotal_ou
t_log,'-k');
legend('VCO Raw Noise','VCO Output Noise','CP Output Noise', 'LPF Out-
put Noise', 'XTAL Output Noise', 'Total Output Noise');

xlabel('Offset Frequency (Hz)');
ylabel('Phase Noise (dBc/Hz)');
```