A Low Cost and Low Phase Noise Oscillator for E-band Applications

by

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Abstract

This thesis shows the proposed, designed and fabricated 38 GHz oscillator system capable of achieving phase noise of -120 dBc/Hz at 100 kHz offset. This phase noise value can allow a high data transmission rates of up to 1.5 Gbps with a modulation scheme of 256 QAM at the E-band frequencies. The low phase noise oscillator system is assembled in a gold-plated brass jig package in which a high quality factor (Q approaching 5300) hemispherical cavity resonator is embedded. The active circuitry of the low phase noise oscillator comprises commercially available and low cost components surface mounted on a low loss millimeter-wave substrate. The 19 GHz commercial oscillator chip makes use of a frequency doubler to drive a sub-harmonically pumped mixer aimed for E-band frequencies of 80 GHz which is an ideal application of the hemispherical resonator with resonance at around 19 GHz.

Acknowledgements

I would like to take this opportunity to thank my supervisors, Prof. Langis Roy, Prof. Rony E. Amaya and Prof. Barry Syrett for supporting me through my master's thesis and research and helping me gain valuable knowledge and experiences. I want to especially thank Rony for guiding me step-by-step from the start of the thesis project to the end.

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Special thanks to Elizabeth Ruscito, my partner in crime through these years. E' stato divertente cercare di sopravvivere insieme in questo ospedale psichiatrico. Con entrata libera e uscita controllata.

The first word I say is what matters to me the most: 媽媽。Thank you for all your support throughout all these years and let me always cuddle by your side. 沒有您的關心、愛護與指導，我就不會是今天的我了。謝謝您，我最愛的媽媽。也謝謝爸爸跟姐姐，很驕傲我有那麼關心和支持我的家人。

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List of Abbreviations and Symbols

ADS	Advanced Design System
AM	Amplitude modulation
ASK	Amplitude shift keying
BER	Bit error rate
BPSK	Binary phase shift keying
CD	Common drain or source follower
CG	Common gate
COTS	Commercial off-the-shelf
CS	Common source
dB	Decibel
DSP	Digital signal processor
DUT	Device-under-test
E-band	71-76 GHz, 81-86 GHz and 92-95 GHz
E_b/N_o	Energy per bit to noise power spectral density ratio
ECC	Error-correcting coding
EIRP	Equivalent Isotropically Radiated Power
erfc	Complementary error function
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission
FET	Field effect transistor
FM	Frequency modulation
f_o	Fundamental oscillating frequency
GaAs	Gallium-arsenide
GaN	Gallium-nitride

Gbps	Gigabit per second
G-S-G	Ground-Signal-Ground
HB	Harmonic Balance
HBT	Heterojunction bipolar transistor
HEMT	High electron mobility transistor
HFET	Heterostructure field effect transistor
I_{ds}	Drain current
IF	Input frequency
LNA	Low noise amplifier
LO	Local oscillator
LTCC	Low temperature co-fired ceramic
Mfr.	Manufacturer
MMIC	Millimetre-wave integrated circuits
OFDM	Orthogonal frequency-division multiplexing
P_{1dB}	Power at 1-dB compression
PA	Power amplifiers
PCB	Printed circuit board
pHEMT	Pseudomorphic high electron mobility transistor
PM	Phase modulation
PN	Phase noise
P_{out}	Output power
PPSD	Phase power spectral density
Q	Quality factor
QAM	Quadrature amplitude modulation
Q_L	Loaded quality factor
Q_u	Unloaded quality factor
R_{in}	Input resistance
RF	Radio frequency
SiGe	Silicon-germanium
SMT	Surface mount technology
SNR	Signal-to-noise ratio

SRF	Self-resonant frequency
SSA	Signal source analyzer
SSB	Single-sideband
UMS	United Monolithic Semiconductor
V_{ds}	Drain voltage
V_{gs}	Gate voltage
X_{in}	Input reactance
Z_o	Characteristic impedance
Z_{in}	Input impedance

Chapter 1

Introduction

1.1 Motivation

The wireless communications market continues to demand better wireless systems with higher speeds, longer ranges and lower costs. As the market seeks the ultimate wireless system, it is inevitable to consider the licensed broadband spectrum available at E-band frequencies. Many research companies are becoming interested in developing communication systems at the ultra-high frequencies ever since the allocation of 13 GHz of unused spectrum at 71 GHz to 76 GHz, 81 GHz to 86 GHz and 92 GHz to 95 GHz was made available in USA, Europe, Russia and Australia [1]. The growing interest in E-band frequencies is due to its ability to provide multi-gigabit speed wireless communications over distances of a mile or more. This allows for speeds that are comparable to the wired fibre optic networks and can further enhance these networks by providing wireless communication links between the network gaps where fibre connections cannot be implemented due to high infrastructure cost and long deployment time. This multi-gigabit wireless communication network will allow 75% of commercial buildings that are located in the network gaps, but are within a mile to an already buried fibre, to finally be multi-gigabit wireless connected [2].

The E-band transceivers would be able to transmit at faster speeds because of the co-existence of band frequencies 71 GHz to 76 GHz and 81 GHz to 86 GHz. These full-duplex transceivers could have up to 5 GHz of bandwidth in each channel, giving a

total of 10 GHz of usable channel spacing allowing more than enough spectrum for 1 Gbps of data transmission using some of the simplest modulation schemes, such as amplitude shift keying (ASK) or binary phase shift keying (BPSK). Furthermore, it would be possible to implement a more complex modulation scheme such as 256 QAM or higher to allow for more than 10 Gbps of data transmission. The channel spacing at the 92 GHz to 95 GHz frequency band is smaller and hence implementation of complex modulation scheme becomes more difficult. Nevertheless, the E-band frequencies still hold a very strong advantage over the other frequency bands as they only suffer fairly low sea level attenuation (Figure 1.1).

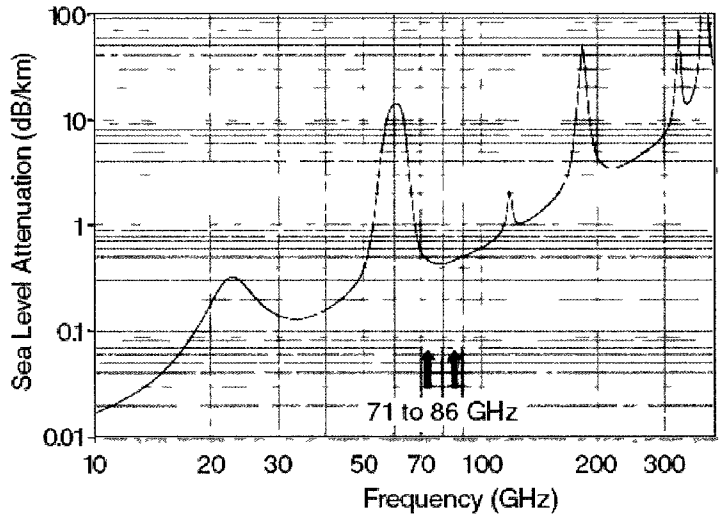


Figure 1.1 Sea level attenuation for microwave frequencies

With lower sea level attenuation, the atmospheric interference is also lowered and therefore a faster and longer range wireless transmission can be established, which is more desirable. For example, the sea level attenuation rises to a peak of approximately 15 dB/km for the 60 GHz band frequencies but is only attenuated by 0.5 dB/km for the E-band frequencies [2]. This is one of the reasons why it is very difficult for the 60 GHz frequency band to provide multi-gigabit speed transmission over long range. Furthermore, the E-band frequency spectrum is a licensed band whereas the 60 GHz band is unlicensed. This makes the E-band a premium class band and thus much less crowded as many companies prefer using the free bands at 60 GHz.

As discussed in the previous paragraph, at E-band frequencies, a high speed transmission of more than 10 Gbps is possible with a more complex modulation scheme. This is because with higher complexity, the frequency spectrum can be used more efficiently resulting in a higher channel capacity. This can be described by the Shannon Theorem for channel capacity (Equation (1.1)).

$$C = B \cdot \log_2(1 + S/N) \tag{1.1}$$

where C is the channel capacity in bps, B is the channel bandwidth and $M = (1 + S/N)$ is the modulation scheme. By reducing the required frequency spectrum, meaning less bandwidth needed per gigabit of data, a faster transmission can be achieved. However, spectrum efficient modulation would increase the complexity in the DSP (digital signal processor) and baseband sections of the radio transceiver (Figure 1.2). There are several parameters in the front-end radio components that will degrade the performance of the modulating signal and thus affect the data transmission rate. These parameters include the local oscillator (LO) phase noise, the low noise amplifier (LNA) noise, the limited output power (P_{out}) and linearity of power amplifiers (PA), the inter-channel interference, the cascaded receiver noise figure and more [1]. Hence, the radio front-end components have to be carefully designed to minimize the signal degradation. Another difficulty arises at the limitations of integrated circuit technologies at ultra-high frequencies. While there are several ways to design radio front-end components able to achieve the required high data rate, their cost is typically high, especially for mass production. The work presented here will attempt to achieve a high performance and cost effective oscillator design for E-band applications.

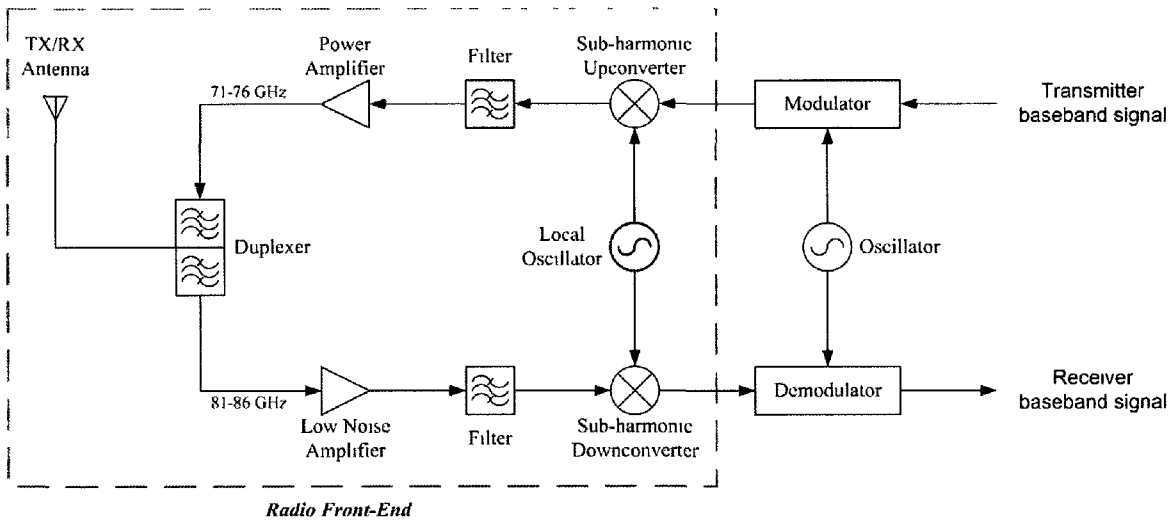


Figure 1.2 A simple full-duplex transceiver

1.2 Previous Work and Thesis Objectives and Contributions

Commercial wireless transceivers using simple modulation schemes such as ASK or BPSK and with data rates of up to 1.25 Gbps are currently available. However, this data rate is limited due to the fact that the spectral efficiency for ASK or BPSK is below 1 bit/Hz [1]. In order to achieve higher data rate, simple modulation schemes are insufficient. A more complex modulation scheme will allow more internet data and better quality voice-over-IP to be transmitted over the point-to-point communication links at a faster speed. Yet, more complex modulation schemes will trigger several factors that can affect the performance of the transmission speed, such as LO phase noise, as mentioned in the previous section. That is why achieving lower noise and/or higher power in the radio transceiver becomes so crucial. Such designs have also been developed where the achieved data rate is 6 Gbps with 2.4 bit/Hz spectral efficiency using an 8PSK (phase shift keying) modulation scheme [3]. Most of the solutions available in the literature are implemented using one or more custom millimetre-wave integrated circuits (MMIC). In this study, the key focus will be on an oscillator system design using commercial off-the-shelf (COTS) components for a cost effective and low noise oscillator.

Oscillators operating at E-band are very difficult to design and implement due to the greater parasitic effects. One of the ways to resolve this problem is to use sub-

harmonic up/down converters in the transceiver design. With the sub-harmonic design, a 40 GHz LO can be implemented such that the second harmonic at 80 GHz can be used as the E-band LO. As the frequency requirements are reduced, MMIC designs become less difficult to implement and hence the cost and the complexity are reduced [1].

Therefore, the objective of this thesis will be to determine the feasibility of producing a low cost and low phase noise oscillator at 40 GHz using standard COTS active chips with a high Q package-embedded resonator (which will be discussed in more detail in later chapters). The steps in achieving this goal are to first analyze a detailed MMIC oscillator design to determine optimum circuit configuration in order to meet the targeted specifications, and to identify a commercially available equivalent MMIC. The second step is to design and fabricate the system module incorporating the available oscillator chip and the package-embedded resonator along with the standard coaxial connector interface. The third and final step is to assess the oscillator performance.

The work of this thesis will contribute to the scientific community in two ways. First, it will enable the capability of immediate use of the designed oscillator module in commercial mass production, since standard COTS components were used. Secondly, this work will contribute to the availability of a ready-to-use template allowing designers to study the oscillator performance trade-offs when components are replaced. This would also include changes in material, location of component placement, the effects of bondwire, the effects of decoupling capacitors, the assembly parameters, and most importantly the parametric study of the phase noise (PN), the output power and the oscillation frequency.

The realization of the overall oscillator system was a collaborative effort with fellow Master of Applied Science student Elizabeth Ruscito [4]. This dissertation is focused on the design and challenges involved with the 40 GHz LO active circuitry and component integration. An overview of the entire system concept including resonator component is given in Chapter 2, but the design details and challenges specific to this work only are presented in this thesis.

1.3 Thesis Organization

This thesis is organized into five major sections to provide a detailed insight into oscillator system design that can be used for E-band transceivers.

Chapter 2 provides a literature review of transceiver system analysis which will show the relation between data rate and phase noise. The background on circuit technology and phase noise theory is also explained.

Chapter 3 shows a 40 GHz oscillator design using a United Monolithic Semiconductor (UMS) 0.15 μm GaAs pHEMT technology. Detailed optimizations on phase noise and output power are also analyzed.

Chapter 4 presents the oscillator system design, characterization and modeling of several system components and assembly parameters. The parametric simulation of the system design and the trade-offs are also discussed.

Chapter 5 discusses the fabrication and process concerns and restrictions and compares the experimentally measured result of the oscillator system design with the software simulated results.

Chapter 6 concludes the thesis by summarizing the research work and outlining the thesis contributions. Possible future research work is also discussed.

Chapter 2

System Analysis and Background Review

There are three main components to this chapter. The first one, Section 2.1, shows a system breakdown from transceiver target specification to the required phase noise for oscillator design. The second one, Sections 2.2 and 2.3, reviews the phase noise background theory and discusses the choices for realizing low phase noise oscillators. The third one, Section 2.4, proposes the oscillator system concept.

2.1 System Analysis for Phase Noise Specification

2.1.1 Effects of Phase Noise on System Performance

Phase noise is the most detrimental form of noise in any circuit system because of its continual existence. In comparison to the additive noise that may also exist within a system, phase noise is multiplicative, which means that it cannot be easily reduced just by increasing the signal-to-noise ratio (SNR). That is why it is very important to understand the effects of phase noise and the methods to reducing them (will be discussed in Section 2.2). Phase noise affects a system through the process of phase modulation (PM). Modulation is the process of providing "piggy-back" services for data signals to sit on a carrier signal and thus be able to transmit more efficiently at a high data rate. Amplitude modulation (AM) is another modulation technique that can be used to modulate signals and the noise can be easily reduced; however, phase modulation is usually required for a high capacity and thus more expensive channel bandwidth [5]. There are three main

undesired effects that will appear in the system when a signal is being modulated and as results of phase noise and they are: data decision error, phase jitter and receiver desensitization.

In order to effectively describe data symbol errors, a constellation map has been computed which will be discussed further (Figure 2.1). Under ideal condition when a data signal is being modulated with no noise being present, each data symbol will match exactly to one constellation point (Figure 2.2 (a)). However, with the noise being present, data symbols will start to shift away from the ideal location depending on the amount of noise present (Figure 2.2 (b)). The distribution of additive noise and phase noise where a larger circle or arc implies higher noise density, respectively, can be found on Figure 2.1. The two noises can also form combinational effects. When phase noise is present, the data symbol will deviate along the arc at an angle away from the ideal location of the designated constellation point. If this angle is small, the data symbol will subtend within the correct decision boundary. However, if this angle is too large, the data symbol will cross over the decision boundary (like the red grid dots shown in Figure 2.1) and thus causing two data symbols being mapped to the same constellation point. This is a data error.

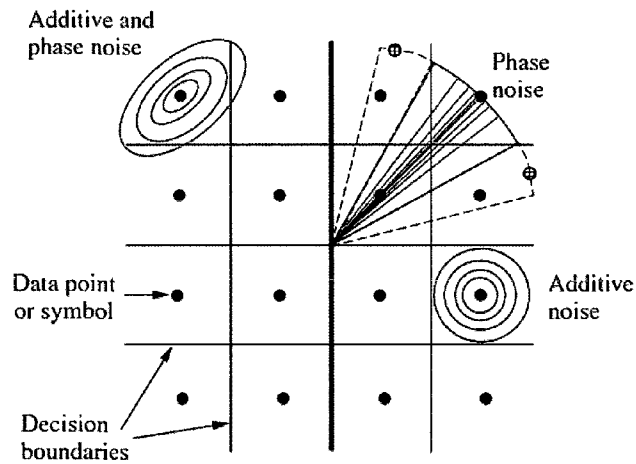
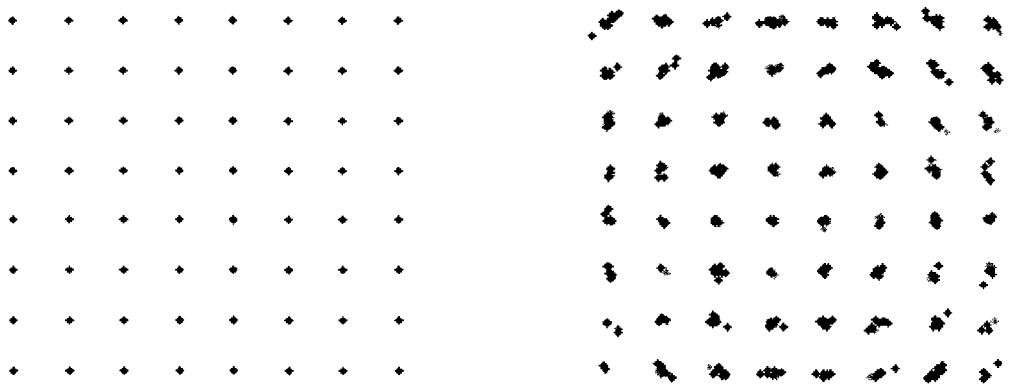


Figure 2.1 Constellation of data symbols with probability of noise distributions [6]



(a) (b)

Figure 2.2 Constellation (a) without noise and (b) with noise obtained using Matlab

In the time domain, a more obvious phase noise effect is evident. A modulated data signal with a modulation period of T_m can be found in Figure 2.3. If no phase noise is present, the modulation period will be constant and hence the clock is synchronized. However, with the presence of phase noise, the modulation period will be affected causing an increasingly more evident phase shift as time progresses. This phase jitter, as seen in Figure 2.3, will cause the clock to de-synchronize, which will result in a time delay between the time the data arrives and the sampling time. This will cause the system to acquire the same data point twice or not at all [6]. This is another type of data error that can be caused by phase noise.

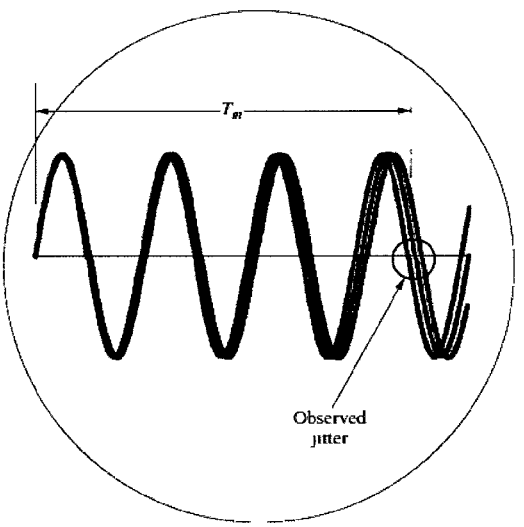


Figure 2.3 Phase jitter observed in time domain [6]

The third major effect of phase noise is the receiver desensitization. This is an error caused by an insensitive receiver with low adjacent channel rejection when incoming signals are being down-converted to baseband. In Figure 2.4, only one signal landing at the input frequency (IF) should be present. However, due to the spread of the phase noise over a large spectrum, a noisy LO signal actually exists and is buried in the phase noise spectrum. If there happens to be an unwanted signal away from the noisy LO that the frequency between them is equal to the IF, the unwanted signal will also be down-converted and will sit directly on the desired IF signal. This will cause an incorrect received signal and hence an incorrect data [7].

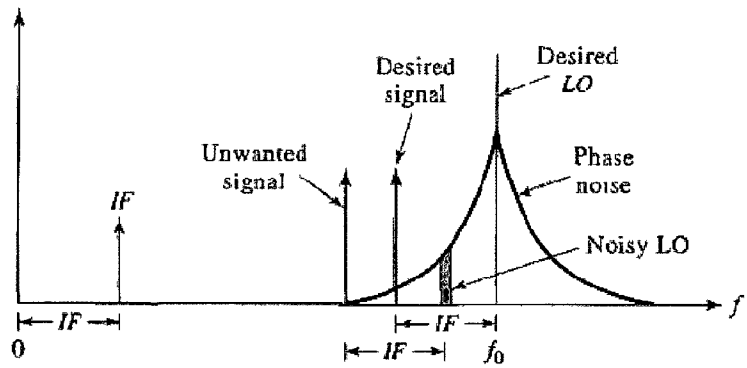


Figure 2.4 Phase noise in LO leading to unwanted IF signal [7]

2.1.2 Target Specification and System Phase Noise Analysis

Although phase noise can affect the system performance in many ways and it is unavoidable, there are many different ways in circuit design to help minimize these effects. Therefore, it is very important to specify a maximum phase noise tolerance the system can handle so proper circuits can be designed to meet the target specification.

As mentioned earlier, the focus of this project is to design a LO source capable of driving the transceiver for higher data rate using higher modulation scheme at the E-band frequencies. The detailed target specifications can be found in Table 2-1 and the United States Federal Communications Commission (FCC) and the European

Telecommunications Standards Institute (ETSI) standards on emission restrictions at E-band frequencies can be found in Table 2-2.

Table 2-1 E-band transceiver system target specification

	Target Value
System standard	Fixed point-to-point system using OFDM
Frequency of operation	71-76 and 81-86 GHz
Mode of operation	Full duplex
Data rate	$\geq$ 1.5 Gbps
Channel bandwidth	250 MHz
BER	10^{-9}
Code rate	3/4

Table 2-2 FCC and ETSI regulation standards [8, 9]

	FCC	ETSI
Frequency range	71-76 and 81-86 GHz	71-76 and 81-86 GHz
Maximum allowable EIRP*	+55 dBW	+45 dBW
Minimum channel bandwidth (aggregation permitted)	n/a	Multiples of 250 MHz
Guard band (upper and lower)	n/a	125 MHz

* *Equivalent Isotropically Radiated Power*

a. Frequency allocation and modulation scheme

According to the FCC and the ETSI standards listed in Table 2-2, the ETSI has a more stringent regulation than the FCC. The ETSI has a limitation on channel bandwidth, a requirement for guard bands as well as its maximum allowable EIRP is also 10 dB lower than the FCC standards. As for this reason, the ETSI standards will be adapted for the system analysis so the final design can meet both standards.

As mentioned in the introduction, there are two 5 GHz bands, 71-76 and 81-86 GHz, allocated in the E-band; one for transmitting and one for receiving. Each 5 GHz

bandwidth will have a 125 MHz guard band at the start of the band (lower side) and at the end of the band (upper side); Figure 2.5. The remaining bandwidth is equally divided into nineteen channels at 250 MHz each. In order to achieve a data rate of 1.5 Gbps or higher with 250 MHz channels, a higher modulation scheme is required and can be approximated using Equation (2.1) [10], where M is the required number of symbols in the constellation for quadrature amplitude modulation (QAM) (i.e. M-QAM). The bit rate is the minimum required data rate at 1.5 Gbps and the symbol rate is equal to the bandwidth at 250 MHz.

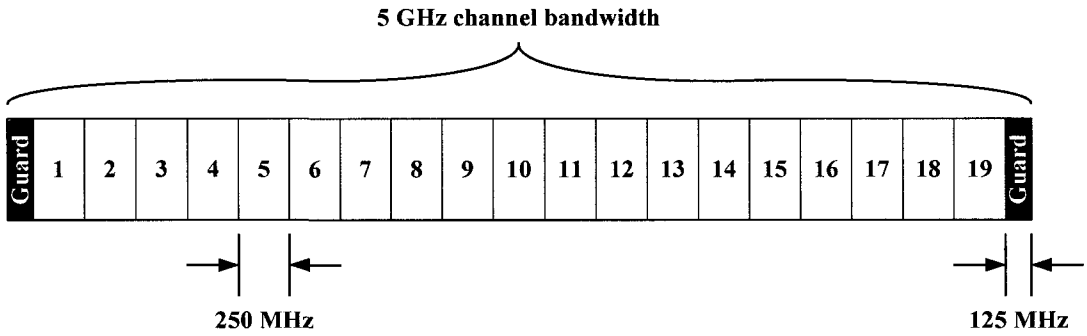


Figure 2.5 Frequency allocation

$$bit\ rate = symbol\ rate \times log_2 M \tag{2.1}$$

The minimum required modulation scheme is found to be 64 QAM (i.e. M = 64). Since this is only the bare minimum requirement for 1.5 Gbps, the safer choice would be a step higher using a 256 QAM modulation scheme. However, both modulation schemes will be analyzed to provide an alternative to the 256 QAM if only the bare minimum is preferred.

b. Ideal SNR

Since phase noise can directly influence the SNR level, it is essential to find the ideal SNR in order to set the value for the maximum allowable phase noise that the system can tolerate. Using Equation (2.2) [11], the maximum SNR without any error control coding

is obtained, where E_b/N_o is obtained from the bit error rate (BER) graph using Matlab at $BER = 10^{-9}$ (Figure 2.6). The BER graph is a plot of probability of bit error that can happen using the respective modulation scheme. The probability of bit error equations for 64 QAM and 256 QAM are shown in Equations (2.3) and (2.4), respectively [12]. The symbol frequency, f_s, in Equation (2.2) is again equal to the bandwidth and the BW is the channel bandwidth.

$$SNR = \frac{E_b}{N_o} \cdot \frac{f_s}{BW} \cdot log_2 M \tag{2.2}$$

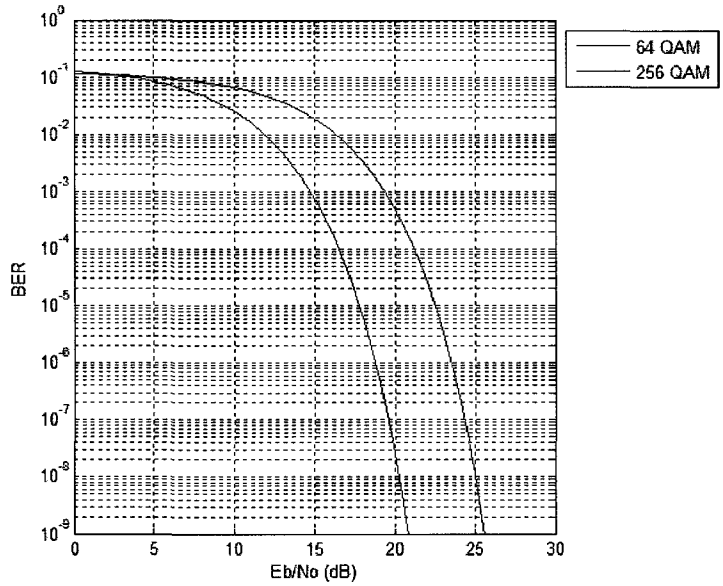


Figure 2.6 BER versus E_b/N_o without any coding

$$P_{64QAM}\left(\frac{E_b}{N_o}\right) = \frac{7}{24} \cdot erfc\left(\sqrt{\frac{1}{7} \cdot \frac{E_b}{N_o}}\right) - \frac{49}{384} \cdot erfc^2\left(\sqrt{\frac{1}{7} \cdot \frac{E_b}{N_o}}\right) \tag{2.3}$$

$$P_{256QAM}\left(\frac{E_b}{N_o}\right) = \frac{15}{64} \cdot erfc\left(\sqrt{\frac{4}{85} \cdot \frac{E_b}{N_o}}\right) - \frac{225}{2048} \cdot erfc^2\left(\sqrt{\frac{4}{85} \cdot \frac{E_b}{N_o}}\right) \tag{2.4}$$

The ideal SNR is found to be 28.64 dB using 64 QAM and 34.65 dB using 256 QAM when no error coding is used. The error-correcting coding (ECC) is used when a system has a limited SNR level but requires a BER that is lower than the normally

achievable BER without coding. The code rate required for this system is 3/4 as specified in Table 2-1. Taking into consideration of the code rate, the SNR equation can be rewritten as in Equation (2.5).

$$SNR = code\ rate \cdot \frac{E_b}{N_o} \cdot \frac{f_s}{BW} \cdot log_2 M \tag{2.5}$$

Therefore, the ideal SNR with coding is 27.39 dB using 64 QAM and 33.40 dB using 256 QAM. The values are summarized below in Table 2-3.

Table 2-3 Summary for maximum obtainable SNR

	64 QAM	256 QAM
Without coding	28.64 dB	34.65 dB
With coding	27.39 dB	33.40 dB

c. Maximum phase variance and minimum phase noise

In order to find the minimum phase noise required for the system, first the phase variance will need to be determined. The maximum tolerated phase variance depends on the SNR; the higher the SNR, the higher the tolerance. The relationship between phase variance, σ_φ, and SNR in an OFDM system can be related using Equation (2.6) [13], where $SNR_{without\sigma_\varphi}$ is the E_b/N_o for respective QAM.

$$SNR_{with\sigma_\varphi} = \frac{SNR_{without\sigma\varphi}}{1+4\cdot\sigma_\varphi{}^2\cdot SNR_{without\sigma\varphi}} \tag{2.6}$$

As more noise is introduced into the system, the probability of bit error will increase. This means that with the same level of SNR, the BER will be higher. In order to examine these changes, the BER plots with different degrees of phase variance are shown in Figure 2.7. This graph is obtained by combining Equation (2.6) with Equations (2.4) and (2.5) using Matlab. The details on the Matlab code can be found in Appendix A.

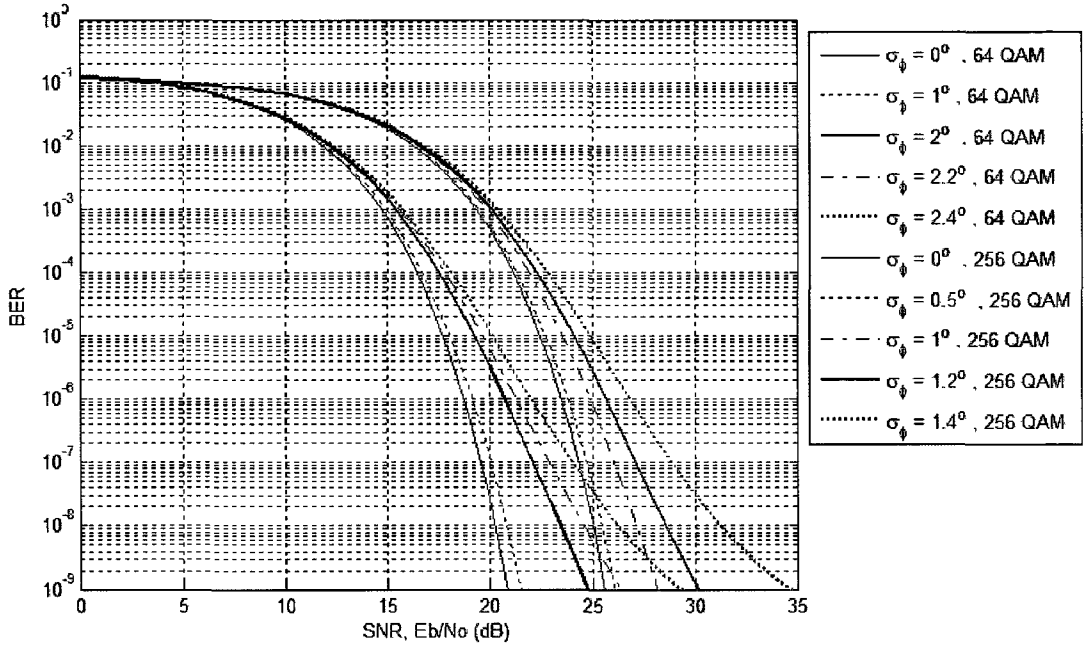


Figure 2.7 BER with phase noise

There are two sets of BER plots shown in Figure 2.7: the blue waterfall curves represent 64 QAM and the red waterfall curves represent 256 QAM. Both modulation schemes shows an increase in BER when the variance is increased. Looking more specifically at the 64 QAM plots where the phase variance is varied from 0° to 2.4°, the curve with the highest phase variance, σ_φ, = 2.4°, sets the boundary for $BER = 10^{-9}$ when a maximum obtainable signal power is used. This means that the phase variance should be set at a value less than 2.4° to provide some margin below the maximum SNR so the system can still operate if SNR is lower at some point in time during data transmission. Comparing the values for the maximum obtainable SNR from Table 2-3, 28.64 dB without coding and 27.39 dB with coding, to the SNR values in Figure 2.7 at the $BER = 10^{-9}$ crossing for 64 QAM, the SNR values that does not exceed the maximum obtainable SNR happens for curves with σ_φ, = 2.2° or smaller. A safer choice for the coded system would be σ_φ, = 2° or smaller. This concludes that the maximum phase variance tolerated in the system with 64 QAM is σ_φ, = 2°. Similar analysis done for the 256 QAM curves yields a maximum tolerated phase variance of σ_φ, = 1.2°.

Phase variance is the total integrated phase power spectral density (PPSD), S_φ, over a modulation frequency range as described by Equation (2.7) [6].

$$\sigma_\varphi{}^2|_{f_1}^{f_2} = \int_{f_1}^{f_2} S_\varphi(f_m)\, df_m \tag{2.7}$$

In order to obtain a specific phase noise number for the circuit design, some approximation on the PPSD is needed and can be described by Equation (2.8), where b is the slope parameter of S_φ on a log plot from the lowest, $f_{m1,}$ to the highest, $f_{m2,}$ modulation frequency that bounds the slope. The parameter b corresponds to a slope of $10b$ dB/decade [6]. The slope is chosen to be at b = *-2*, meaning -20 dB/decade, from 1 kHz to 10 MHz to best approximate the PPSD at the region of interest (more detail will be discussed in the next section).

$$\sigma_\varphi{}^2|_{f_{m1}}^{f_{m2}} = \frac{f_{m1}\cdot S_\varphi(f_{m1})}{b+1}\left[\left(\frac{f_{m2}}{f_{m1}}\right)^{b+1} - 1\right] \tag{2.8}$$

Substituting the maximum tolerated phase variance found above, σ_φ, = 2° for 64 QAM and σ_φ, = 1.2° for 256 QAM, in Equation (2.8), the PPSD at f_{m1} = 1 kHz are found. The PPSD at 100 kHz can be extrapolated using the -20 dB/decade ratio by adding -40 dB. The phase noise, L_φ, also called the single-sideband (SSB) density, at a specified offset is related to the PPSD through Equation (2.9), where the offset, Δf, equals the modulation frequency, f_m.

$$L_\varphi(\Delta f)|_{dBc/Hz} = S_\varphi(f_m)|_{dBr/Hz} - 3\ dB \tag{2.9}$$

The values computed above are summarized in Table 2-4. The minimum phase noise at 100 kHz offset is found to be -102 dBc/Hz for 64 QAM and -106 dBc/Hz for 256 QAM. Since 256 QAM is a safer choice for data rate of 1.5 Gbps or higher, the circuit design will base on achieving the goal of a minimum SSB phase noise of -106 dBc/Hz at 100 kHz offset.

Table 2-4 Summary of phase noise requirement at 80 GHz

	64 QAM	256 QAM
Phase variance, σ_φ	2^o	1.2^o
PPSD @ 100 kHz, $S_\varphi(100\ kHz)$	-99	-103
SSB phase noise @ 100 kHz offset, $L_\varphi(100\ kHz)$	-102	-106

2.2 Phase noise Theory and Analysis

Noise within an oscillator circuit comes from many parts of the circuit design and in many forms including thermal noise, transistor noise, noise from the resonator or buffer amplifier and more. Within all the noise sources, there are three major noises that will directly affect the phase noise of an oscillator and they are low frequency noises, noises from the resonator and the noise floor of the system.

Phase noise is best described by the Leeson model shown in Equation (2.10), where F is the noise figure, k is Boltzmann's constant, T is the absolute temperature, P_{out} is the output power, f_o is the carrier frequency, Q_L is the loaded quality factor from the resonator and Δf is the offset frequency [14]. This equation is broken down into three parts to provide a simple model that describes the three major noise sources. The first term of the equation models the noise floor, the second term models the noise from the resonator that is dependent on the quality factor of the resonator and the third term describes the low frequency noise. In order to fully understand the relationship between this equation and the phase noise plot shown in Figure 2.8, it is helpful to expand the equation out fully so three major sub-equations, Equations (2.10a), (2.10b) and (2.10c), can be seen. Each of the three sub-equations fits into the three noise regions in Figure 2.8. The first region where the slope is the steepest dropping at a rate of -3 exponentially (-30 dB/decade) is the region where low frequency noise sources dominate. This can be seen from the corresponding Equation (2.10a) as it has a Δf^3 term. The second region where the slope drops at a rate of -2 exponentially (-20 dB/decade) is where the resonator noise dominates. As a resonator is always described by its quality factor, Q factor, Equation (2.10b) shows the how phase noise is dependent on the resonator Q. The last part of the

graph, region 3, is flat since the noise floor does not depend on frequency as it has been normalized by the bandwidth frequency, Δf, and this can also be seen in Equation (2.10c) [15].

$$L_{\varphi}(\Delta f)|_{dBc/Hz} = 10\log\left[\frac{2FkT}{P_{out}}\left\{1+\left(\frac{f_o}{2Q_L\Delta f}\right)^2\right\}\left(1+\frac{f_c}{\Delta f}\right)\right] \tag{2.10}$$

$$L_{\varphi}(\Delta f)|_{dBc/Hz} = \begin{cases} 10\log\left[\frac{2FkT}{P_{out}}\left\{\frac{f_c}{\Delta f}+\frac{f_c{f_o}^2}{4{Q_L}^2\Delta f^3}\right\}\right], & \Delta f < f_c \quad (2.10a) \\ 10\log\left[\frac{2FkT}{P_{out}}\left(\frac{f_o}{2Q_L\Delta f}\right)^2\right], & f_c \le \Delta f \le \frac{f_o}{2Q_L} \quad (2.10b) \\ 10\log\left[\frac{2FkT}{P_{out}}\right], & \Delta f > \frac{f_o}{2Q_L} \quad (2.10c) \end{cases}$$

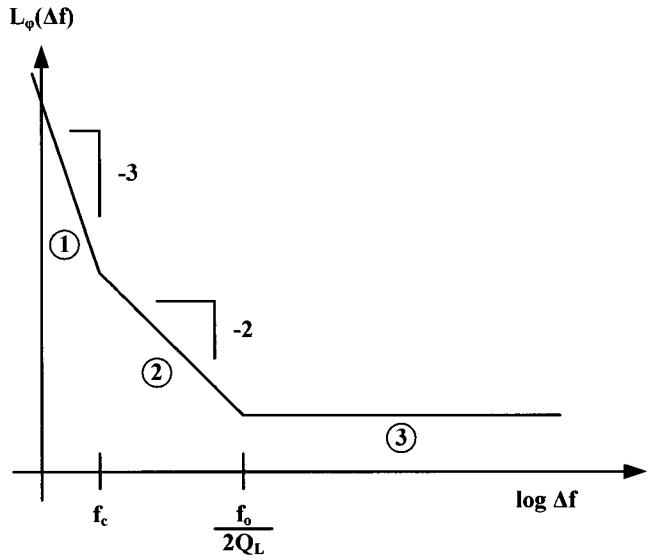


Figure 2.8 Leeson model of phase noise [14]

2.2.1 Flicker Noise

In the low frequency region, many noise sources exist such as thermal noise, shot noise and flicker noise, however the most significant and thus dominating noise is the flicker noise. Flicker noise, also called 1/f noise, is a noise caused by the random fluctuations of the electron carrier density in an active device [16]. Although it is a low frequency noise, it can be up-converted to the carrier frequency due to the mixing nature resulting from the

nonlinearities of the active device. Different transistor choice will also provide different levels of flicker noise. The advantage of lower flicker noise is not only that it lowers the noise level but by doing so it also shifts the flicker noise corner frequency (f_c in Figure 2.8) towards DC. This is desirable as flicker noise is a very strong noise at the low frequency region and thus the smaller region it dominates, the less it will affect the overall performance. In a transistor noise assessment summary done by QinetiQ (Figure 2.9; [17]), it can be seen that oscillator design adapting technologies such as SiGe HBT and GaAs pHEMT provide a lower flicker noise level than the two GaN HEMT variants. Other studies also shows that HBT technology is the best in providing the lowest flicker noise for oscillator designs while BJT also provides good performance at lower frequencies [18, 19]. Most of the advantages point towards the bipolar based transistor technologies in terms of low flicker noise, especially HBT at higher frequencies; however, a major drawback about the bipolar technologies is that it provides lower gain than the HEMT and the FET based technologies especially at higher frequencies. This makes it more difficult to obtain a high output power which is also important to reducing phase noise (more detail in Section 2.2.3) [20, 21]. Looking again at the noise assessment from QinetiQ, although the GaAs pHEMT technology is less ideal compared to the SiGe HBT technology in terms of flicker noise but it is still much superior to the GaN HEMT technology, as such, the GaAs pHEMT technology is used in this project.

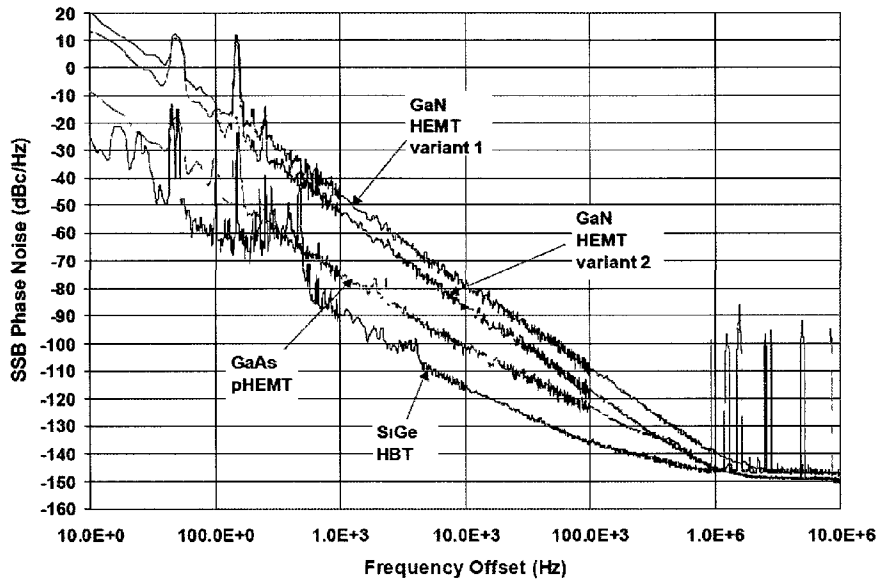


Figure 2.9 Oscillator phase noise using different transistors from QinetiQ's noise assessment summary [17]

2.2.2 Resonator Noise versus Quality Factor

The noise from the resonator is very much dependent on the loaded quality factor of the resonator, Q_L. This can be seen in Equation (2.10b) as the phase noise is inversely proportional to the square of Q_L. Since only the quality factor is inside the square bracket, it is intuitively understood that region 2 in Figure 2.8 is basically controlled by Q_L. Higher Q_L will lower the region 2 slope line providing a lower phase noise from an offset of f_c to $f_o/2Q$ and hence improving the overall oscillator phase noise performance.

The quality factor of a resonator depends on its physical structure and material used and thus it has a large range of values. It can be as simple as a microstrip resonator with a typical Q of around 100 to 300 or it can be resonator made of sapphire with a Q of over 250k [22, 23]. Although high Q is always better for oscillator phase noise performances, many high Q resonators are expensive and/or difficult to implement. In this study, the oscillator design will be simulated both with a simple microstrip resonator having a very low loss tangent that yields an unloaded quality factor, Q_u, of 350, and with a high Q package-embedded resonator realized by E. Ruscito [4] which

yields a Q_u of around 5300. Both resonators are intended for integration into the proposed oscillator system design, with low fabrication costs in mind.

2.2.3 Noise Floor

Noise floor exists throughout the entire spectrum and is independent of frequency within the normalized bandwidth. This can be seen in Equations (2.10a) to (2.10c) as the parameters describing the noise floor in Equation (2.10c) also appears in Equations (2.10a) and (2.10b). The parameters contributing to the noise floor are ones that are affected by the entire circuit system such as thermal noise, FkT, and output power, P_{out}.

The thermal noise, also called the white noise, is always present in any conducting medium as it is the noise caused by the movement of electrons. The thermal noise is usually approximated to be kT = -174 dBm/Hz at the room temperature (T = 290 K) multiplied by the noise figure, F, of the system. The noise figure is a model of thermal noises that are introduced within the circuit design without any external elements, such as resonator or load. It is measured as the input SNR over the output SNR, Equation (2.11), as it is very difficult to narrow down to the individual thermal noise sources within a circuit as they can come from any resistors and/or transistors used in the circuit. The noise figure can also be described by the additional noise power added by the circuit system, N_{add}, over the input noise power, N_{in} as seen in Equation (2.11). Hence, the noise figure can be minimized by an impedance match at the input port [15].

$$F = \frac{SNR_{in}}{SNR_{out}} = 1 + \frac{N_{add}}{N_{in}} \tag{2.11}$$

Another parameter affecting the noise floor is the output power. The output power is inversely proportional to the phase noise and thus should be maximized to lower the phase noise. The output power can be improved if the output of the circuit is properly matched to the load. It is important to note that the increase in output power is desired not only to lower the phase noise but also to provide enough power to drive the mixer.

2.3 Ultra Low Phase Noise Oscillators

Ultra low phase noise oscillators are commonly achieved by the use of high Q resonators, such as dielectric, sapphire or LTCC (low temperature co-fired ceramic) resonators and appropriate transistor technologies. Although LC tank or microstrip resonator can provide compact design and if carefully implemented can also achieve a low phase noise, it still cannot compete with the high Q resonators that can easily achieve lower phase noise. Some of the previous research done on low phase noise planar oscillators around 40 GHz frequencies are tabulated (Table 2-5). As it can be seen, microstrip and on-chip lumped LC tank resonators cannot provide a low enough phase noise for various active devices [24-26]. The two oscillators with the dielectric and LTCC resonators [27, 28] seem to be promising if the Q can be further increased.

Table 2-5 Research summary on low phase noise oscillators around 40 GHz

f_o (GHz)	Active Device Technology	Resonator	Q_u	P_{out} (dBm)	PN * (dBc/Hz)	Ref.
36.2	AlGaAs/InGaAs HEMT	microstrip	n/a	19.4	-57	[24]
43	SiGe	LC tank	n/a	-17	-87	[25]
39	AlGaN/GaN HEMT	LC tank	n/a	25	-94	[26]
37	InGaAs/GaAs PM-HFET	dielectric	3000	10	-97	[27]
29	GaAs pHEMT	LTCC	1000	11	-102	[28, 29]

* @ 100 kHz offset

2.4 Proposed Oscillator System Concept

In this work, a low cost and low phase noise oscillator is proposed based on GaAs pHEMT transistor technology and package-embedded hemispherical cavity resonator [4].

The concept is illustrated in Figure 2.10. The resonator is aperture-coupled to the planar active circuitry by means of a slot in the substrate's ground plane.

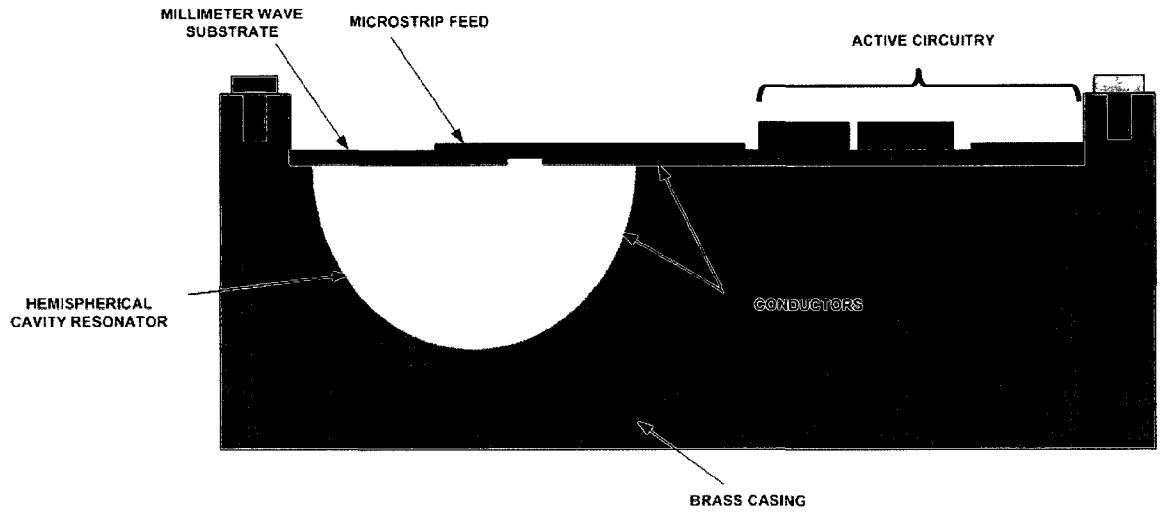


Figure 2.10 Proposed Oscillator System Concept [4]

Based on available GaAs chips, the oscillator core operates at 20 GHz with the output frequency being at 40 GHz due to an on-chip frequency doubler. The promised resonator unloaded Q is about 5300, which should be sufficient to achieve the target phase noise of -112 dBc/Hz at 40 GHz (more detail will be provide in Chapter 3 to determine the actual required Q). The value of -112 dBc/Hz specified here is based on the assumption that a frequency multiplier will degrade the phase noise by approximately *20 log n*, where *n* is the multiplication factor [16]. Therefore, with a frequency doubler (outside of the proposed oscillator system) the -112 dBc/Hz at 40 GHz will degrade by 6 dB when multiplied up to 80 GHz, providing the target phase noise of -106 dBc/Hz as specified earlier in Section 2.1. Thus a 20 GHz high Q hemispherical cavity resonator [4] is incorporated into this project. The target specification is tabulated (Table 2-6).

Table 2-6 Target Specification for the proposed 40 GHz oscillator system

f_o (GHz)	Active Device Technology	Resonator	Q_u	P_{out} (dBm)	PN * (dBc/Hz)
40	GaAs pHEMT	hemispherical cavity (f_o = 20 GHz) [4]	5300	15 (w/ buffer)	-112

* @ 100 kHz offset

The target output power of 15 dBm will require a buffer amplifier. The use of GaAs pHEMT technology as the oscillator's active device is able to provide a relatively high output power of around 10 dBm at a lower carrier frequency [28]. Higher frequency will result in a lower transistor gain and hence it will be more difficult to achieve higher output power. Based on this assumption, it is expected that a buffer amplifier will be required to achieve the target specification.

2.5 Summary

Three main components were covered in this chapter. This includes a breakdown of the transceiver target specification for the required phase noise for oscillator design and is followed by a background on the theory of phase noise. The last component of the chapter covered the proposed oscillator system concept.

Chapter 3

Oscillator Design for E-band Applications

This chapter presents the custom design of a 40 GHz low phase noise oscillator in a GaAs MMIC process. The goal is not to proceed with a physical implementation of the design, but to evaluate the performance and suitability of the components required for acceptable oscillator performance. These include a negative impedance active circuitry, a buffer amplifier and a frequency doubler. In addition to the hemispherical resonator based design concept being pursued, a microstrip resonator based oscillator design is given for comparison.

3.1 Introduction of Active Device Technology

3.1.1 Process Overview

The technology selected for the oscillator circuit design in this project is the 0.15 μm pseudomorphic high electron mobility transistor technology (pHEMT) process from UMS (PH15). This UMS foundry process, PH15, is a high performance GaAs process capable of delivering very low noise for MMIC designs and productions. The 0.15 μm process provides even lower noise performance than its predecessor, 0.25 μm process (PH25). The PH15 is one of lowest noise process developed within the UMS HBT, pHEMT and MESFET technologies and is also one of the few processes that is able to provide circuit production for frequencies up to 80 GHz. Some of the major features of this foundry process include:

- the low resistance and great reliability of the 0.15 μm T-shaped aluminum gate
- the low cost electroplating used for lines and interconnect
- the use of via holes [30]

3.1.2 Technology Limitations

The active device developed with the PH15 is modelled using three different electrical equivalent circuit models. The models are linear FET (denoted FET), nonlinear HOT FET (denoted NHF) and nonlinear COLD FET (denoted NCF), which are derived under different operating conditions. The linear FET includes noise models while the nonlinear FETs do not. On the other hand, the HOT FET is based on Curtice type model to account for HEMT behaviour while the COLD FET is developed for simulating switch circuits and mixers. Since the nonlinear HOT FET can more accurately model the output characteristic, in this project, the parametric studies will be mainly based on the HOT FET. The linear FET is only used in the small-signal domain to compare with the HOT FET result since it cannot be simulated in large signal Harmonic Balance simulation. These FETs can provide up to eight gate fingers with unit finger gate width of 20 to 75 μm. The linear FET is operational at drain voltages, V_{ds}, of 2.5 V or 3.5 V with a drain current, I_{ds}, of 50 – 300 mA/mm while the nonlinear HOT FET is operational from V_{ds} of 1.5 V to 3.5 V and gate voltages, V_{gs}, of -1.0 V to +0.6 V. Furthermore, the maximum DC line current is 7.5 mA/μm [30].

3.2 Negative Impedance Active Circuitry

The core of the oscillator, the negative impedance active circuitry block, utilizes a common gate oscillator topology. This configuration is chosen due to its simplicity and its capability of providing a strong negative resistance over a wide frequency range, which is most suitable for oscillators [15]. The resonant frequency is at 20 GHz as previously discussed and with the use of a frequency doubler, the output of the oscillator will be at 40 GHz in order to drive the sub-harmonic mixer up to 80 GHz.

The following sub-sections will be focused on the 20 GHz negative impedance circuit (Figure 3.1, Figure 3.2) design and optimization through proper bias, FET size and load selection as well as finding the required gate inductance for condition of oscillation. A FET size of 2x20 μm was arbitrary selected in order to start the simulation but was later found to be the ideal size. The simulations are accomplished using Agilent's RF and microwave circuit design software, the Advanced Design System (ADS), in both the S-parameter small-signal domain and the Harmonic Balance (HB) large-signal domain.

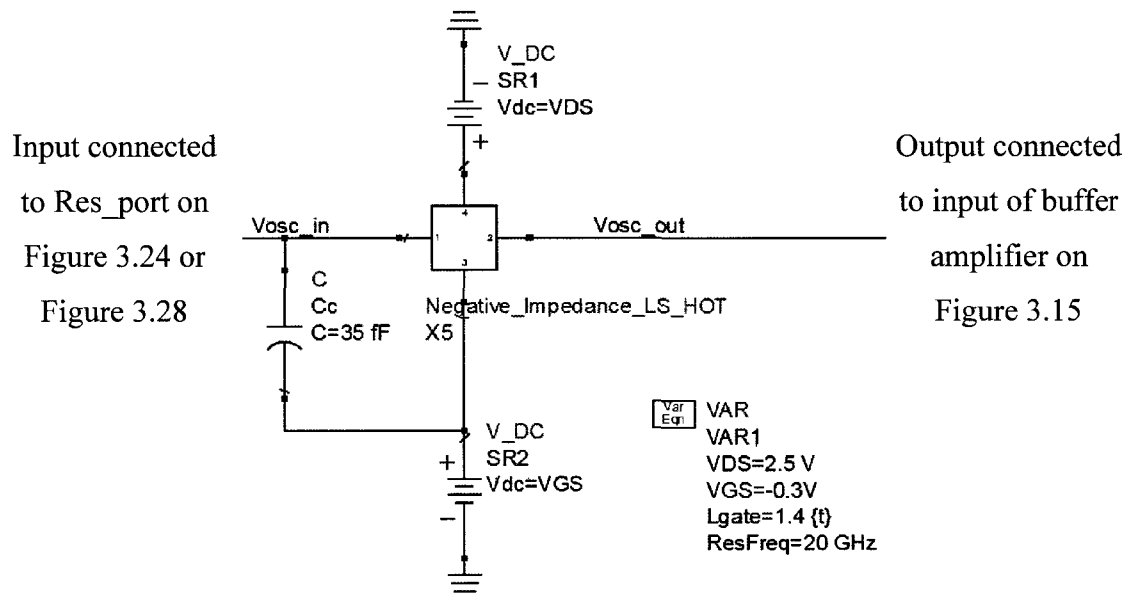


Figure 3.1 Negative impedance block with DC sources

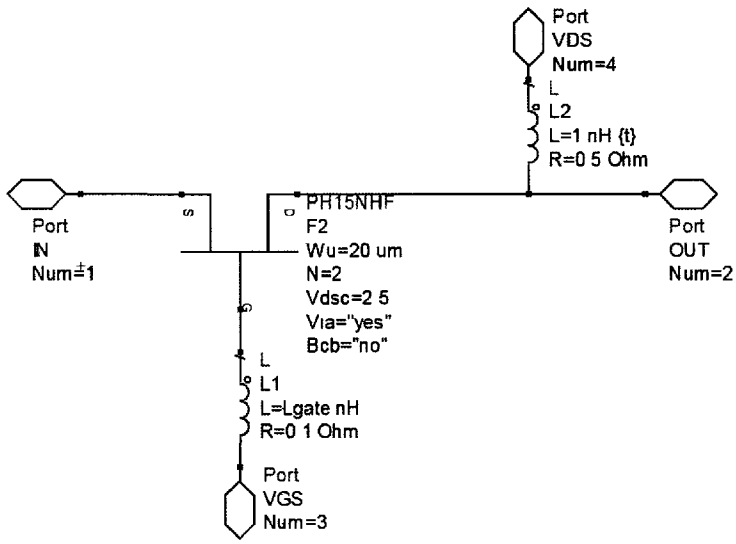


Figure 3.2 Internal circuitry of negative impedance block

3.2.1 Biasing

The bias voltages, V_{ds} and V_{gs}, are chosen based on literature review of typical current consumption within an oscillator core. The typical drain current, I_{ds}, consumption is around 5 mA to 30 mA [31-34]. Since smaller current consumption implies smaller power consumption which is desired for its lower heat dissipation, the bias voltages are chosen to dissipate a current of around 5 mA. This is later proved to be the optimal bias point for phase noise performance.

The drain voltage, V_{ds}, is chosen arbitrarily in the middle region of the NHF operating range (1.5 V to 3.5 V) at 2.5 V as shown in the I-V characteristic curve (Figure 3.3). The gate voltage, V_{gs}, is then selected to be -0.3 V to accommodate an I_{ds} of 5 mA.

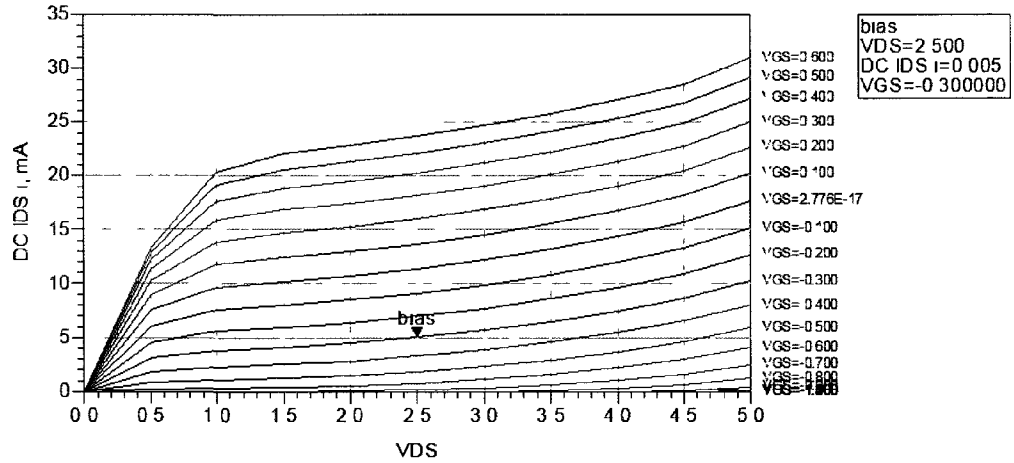


Figure 3.3 I-V characteristic curves for NHF

Further analyses are performed on the bias voltages to ensure optimal phase noise. The bias voltages were first swept together at a broader range of voltages to see the approximate optimal point, then it was pin-pointed down to V_{gs} = -0.3 V. Hence, the test is done by varying V_{ds} from 1.5 V to 3.5 V while V_{gs} is fixed at -0.3 V. The frequency is kept as close to 20 GHz as possible by adjusting feed inductance (L2 in Figure 3.2) and parallel capacitance (*Cc* in Figure 3.1). The resulting phase noise and output power as V_{ds} varies are plotted (Figure 3.4). The phase noise showed a minimum of -117 dBc/Hz at 100 kHz offset at V_{ds} = 2.5 V. The output power increases almost linearly with V_{ds} as expected since higher voltage adds more power to the circuit. However, the goal of this analysis is to optimize the phase noise whereas the output power is less of a concern and thus the drain voltage is selected to be 2.5 V.

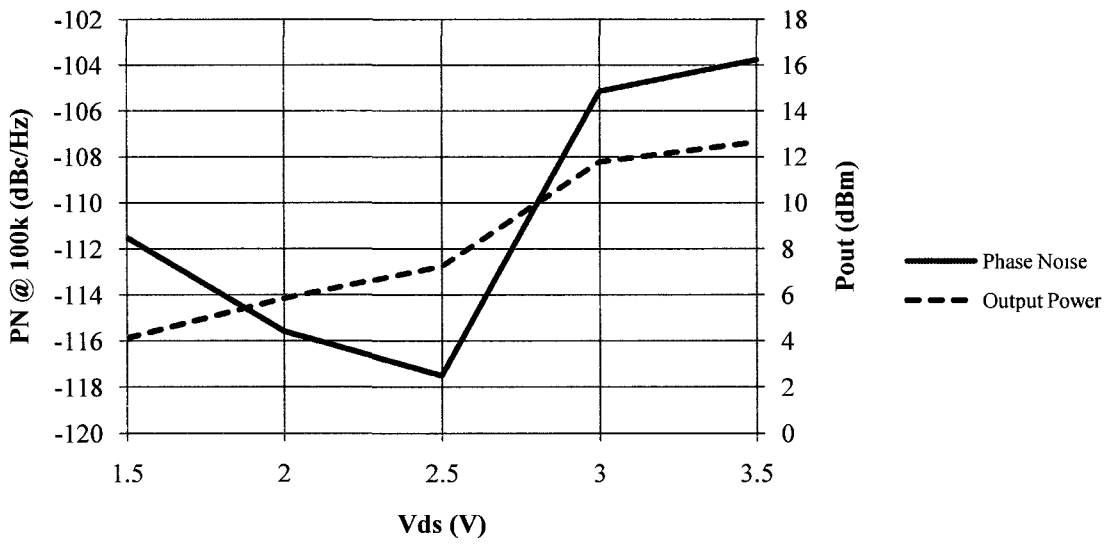


Figure 3.4 PN and P_{out} performances while varying V_{ds}

The second test is done similarly by varying V_{gs} while V_{ds} is fixed at 2.5 V (Figure 3.5). This is again to find the optimal phase noise but this time the V_{gs} voltage is being varied. The frequency is again kept close to 20 GHz. The phase noise increased linearly with V_{gs} starting at V_{gs} = -0.3 V, however, a much shallower slope is present below V_{gs} = -0.3 V. This may be caused by the inaccuracy of the simulator tool while modelling the FET performance at very small I_{ds} (below 5 mA, since I_{ds} decreases with V_{gs}). At very small I_{ds}, it is unsure if the FET is conducting and thus the data may be false and should be avoided. On the other hand, the output power decreases linearly with V_{gs} as expected since lower V_{gs} provides a higher peak swing voltage and thus power is higher. As a result of avoiding the inaccurate data below V_{gs} = -0.3 V, the optimal V_{gs} is then at -0.3 V. Therefore, the optimal bias point is determined to be at V_{ds} = 2.5 V, V_{gs} = -0.3 V and I_{ds} = 5.01 mA.

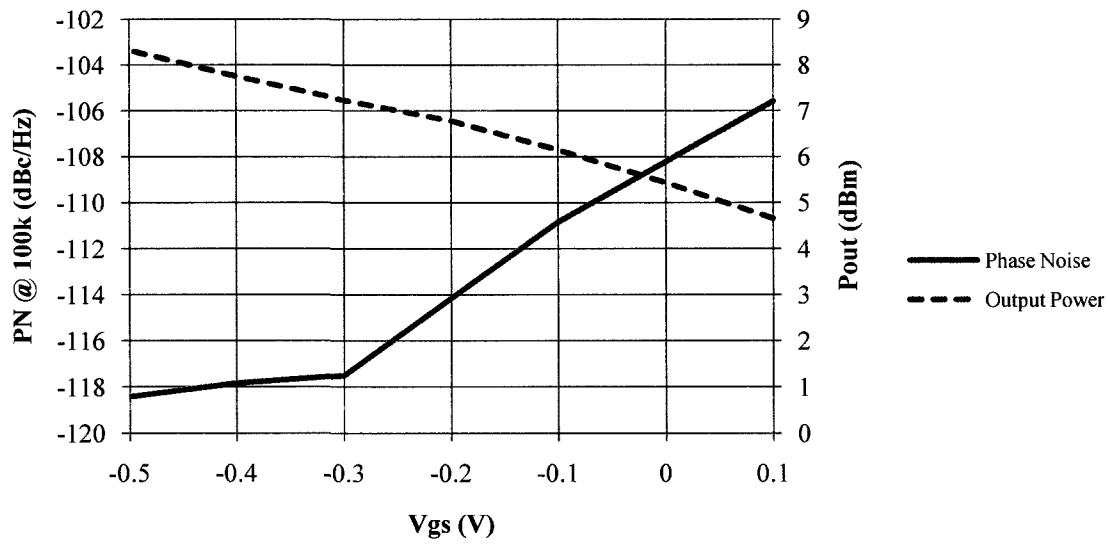


Figure 3.5 PN and P_{out} performances while varying V_{gs}

3.2.2 Oscillation Conditions

Since the oscillator topology chosen is the common gate configuration, the oscillation is mainly controlled by the gate inductance, L_{gate}. Hence, L_{gate} is varied to determine the region of oscillation. In theory, the oscillation condition is met when the reflected signal from the resonant port (input to the negative impedance block) is equal to or greater than the incident signal. This implies that the real part of S_{11}, $Re\{S_{11}\}$, equals to or greater than one and the imaginary part of S_{11}, $Im\{S_{11}\}$, equals to zero. This condition, however, is usually affected when the nonlinear effects of the FET are taken into consideration.

Small signal simulation is first performed on the oscillator circuit in order to determine the region of oscillation at 20 GHz when L_{gate} is varied (Figure 3.6). Seeing from $Re\{S_{11}\}$, the oscillation should occur between L_{gate} of 1.12 nH to 2 nH. However, $Im\{S_{11}\}$ shows that the condition is only true around 1.6 nH to 1.7 nH as $Im\{S_{11}\}$ is closer to zero.

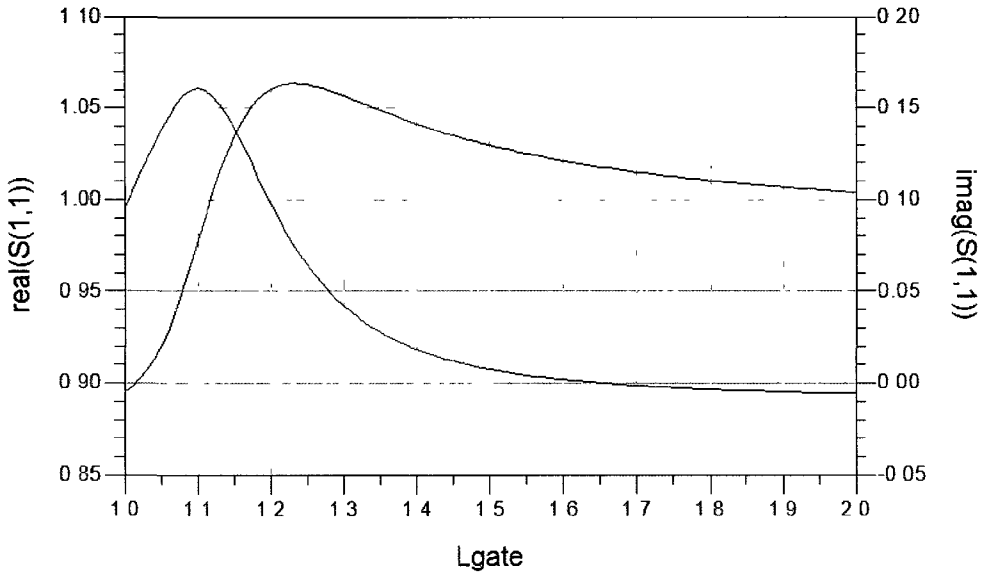


Figure 3.6 S_{11} at the resonant port as L_{gate} varies

Large signal harmonic balance simulation showed a different result. Oscillation did not occur for L_{gate} of 1.6 nH to 1.7 nH, but instead it oscillates at around 1.3 nH. This is likely because the $Re\{S_{11}\}$ at 1.6 nH is too close to one. Although, in theory, it should start to oscillate when the reflection $Re\{S_{11}\}$ is equal to one, the nonlinearities of the circuit tend to lower the negative impedance seen at the port causing a lower reflection and thus oscillation would not occur. This problem is usually overcome when the negative impedance is set higher, or in other words, the reflection is set at a margin higher than one. The $Re\{S_{11}\}$ at L_{gate} = 1.3 nH is much higher than one and hence it oscillates. However, the $Im\{S_{11}\}$ is much higher than zero at L_{gate} = 1.3 nH, which means that the oscillating port sees a very inductive circuit. This causes the oscillating frequency to drift away from 20 GHz. As an oscillating frequency of 20 GHz is required to accommodate the external resonator, there are several methods that can help to re-adjust the frequency back to 20 GHz.

One way to adjust the frequency is to increase the parallel inductance seen from the port, this would be L_{gate} or the feed inductance *L2* (Figure 3.2) to decrease the overall inductance. However, by doing so, the oscillating condition is again changed back to low $Re\{S_{11}\}$. Since the oscillation is heavily dependent on the parallel inductances, not

only L_{gate} but also *L2*, and therefore oscillation would not occur. This method is then discarded as it does not yield the desired outcome.

Another way to re-adjust the oscillating frequency is to increase the size of the transistor since this will decrease the series capacitance between the gate and the source of the FET and thus making the input port less inductive. This is achieved at 19 72 GHz using 4x20 μm FET with L_{gate} = 1.4 nH (Figure 3.7). However, at this FET size, the oscillation condition becomes very sensitive ($Re\{S_{11}\}$ is very close to point of failure at 1.001) since changing the FET size also changes the input resistance of the FET and thus affecting the $Re\{S_{11}\}$. This method is too risky and therefore is not suited.

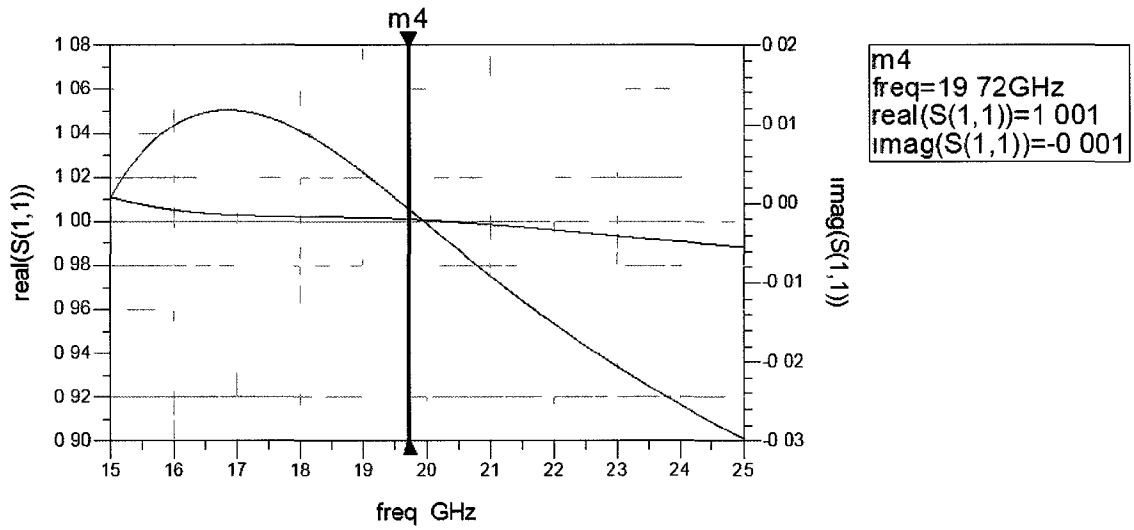


Figure 3.7 S_{11} at the resonant port for 4x20 μm FET

The third way to adjust the frequency is to simply add a compensating capacitor *Cc* (Figure 3.1) in parallel with the input of the negative impedance block so the overall capacitance is increased. The added capacitance will balance out the excess inductance at the port making the port less reactive. This method easily achieves an oscillation at 20.14 GHz with *Cc* = 35 fF and L_{gate} = 1.4 nH using the large signal HB simulation. The small signal simulation also showed a very healthy oscillation condition (Figure 3.8).

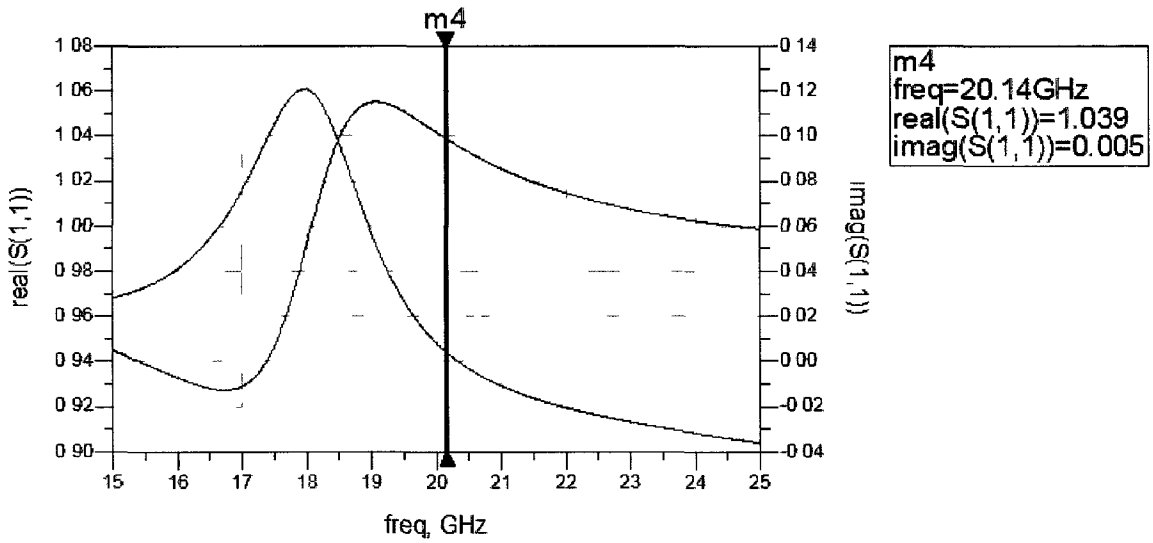


Figure 3.8 S_{11} at the resonant port versus frequency when *Cc* is added

3.2.3 Device Size

The analysis done in this sub-section is to determine the optimum device size for best phase noise performances. The bias point and frequency are fixed in this analysis.

Phase noise does not seem to follow any trend as the FET size varies (Figure 3.9). However, this data only shows the noise coming from the resonator and the noise floor (region 2 and 3, respectively, as described in Section 2.2) due to the technology limitation on noise analysis as discussed in Section 3.1.2. As reviewed in the background section of the phase noise theory (Section 2.2), the noise contribution coming from the FET device is heavily dependent on the flicker noise. Flicker noise is, however, dependent on the device size; smaller device size would exhibit lower flicker noise as shown in [35]. Hence, taking into account the effects of flicker noise, it is suggested to use a smaller FET size to improve the phase noise performance. The device size is then kept at 2x20 μm as it fits all the requirements.

Output Power, on the other hand, shows a slight increase as FET size is increased up and including a FET size of 4x20 μm. This is expected as the drain current I_{ds} increases as FET size increases, meaning more power is being added to the circuit. The output power only shows a slight increase since a loadpull was not done in this

analysis. However, if a loadpull was done in each case, the output power should show a better increasing slope as FET size increases.

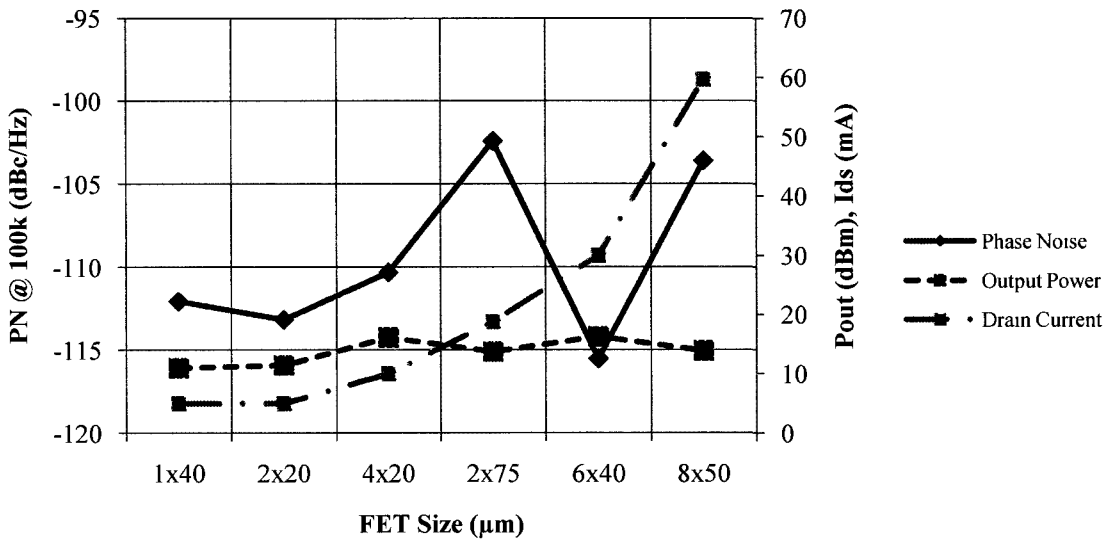


Figure 3.9 PN, P_{out} and I_{ds} performances versus device size

3.2.4 Load Impedance and Buffer Amplifier

The initial oscillator design was done by first designing the negative impedance block then a buffer (short for buffer amplifier) was added to improve the output power. However, this design poses a very difficult problem at the output stage and that is the difficulty to maintain oscillation condition with the presence of a buffer. Many iterations of re-designing the negative impedance block has to be done in order for oscillation to work again. Even by doing so, the output power is still not maximized as the priority was to make oscillation happen and to optimize phase noise. Since oscillation condition heavily depends on the output stage, the oscillator was re-designed by first designing the buffer for maximum gain (details are Section 3.3), then the negative impedance block is designed around the buffer to accommodate it while optimizing phase noise. This allows for less optimization iterations as well as better output power. The output power of the initial design method (Figure 3.10) is 5.5 dB lower than the second improved design

method (Figure 3.11) at an output load (R_{load}) of 200 Ω. Therefore the second design method is adapted.

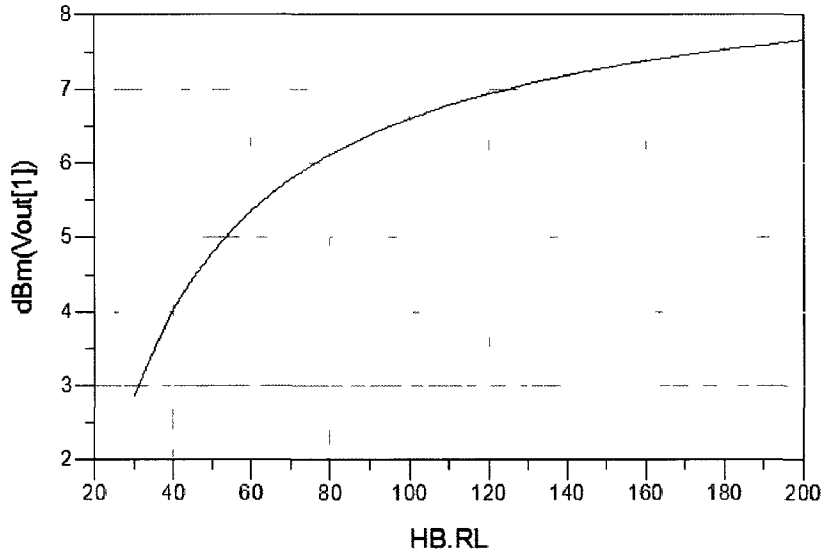


Figure 3.10 P_{out} versus load resistance using initial design method

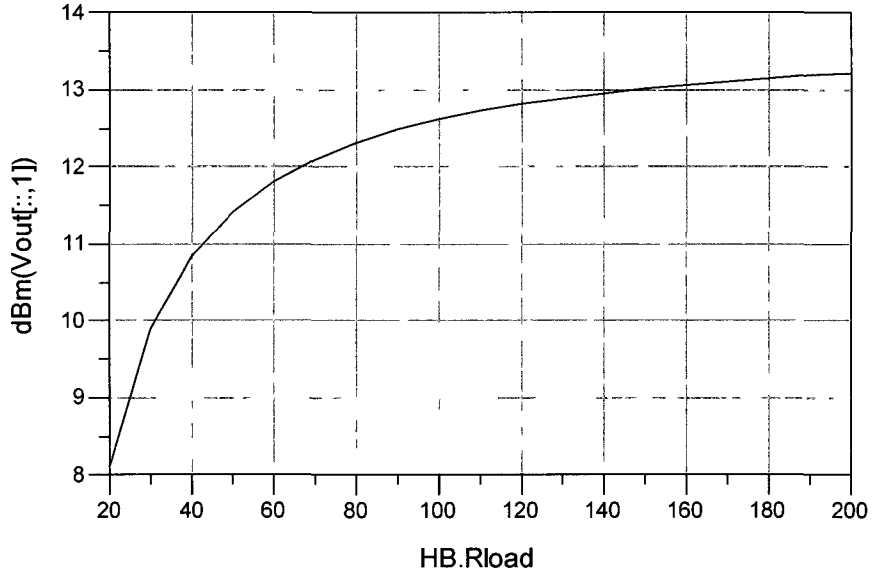


Figure 3.11 P_{out} versus load resistance using the improved design method

3.3 Buffer Amplifier

The buffer amplifier was designed for maximum small-signal gain (S_{21}) while taking into consideration of the required input and output impedances. As mentioned in the previous section, the buffer was designed prior to the negative impedance block to improve design performances. However, if the buffer is designed with arbitrary input impedance, for example 50 Ω, a matching issue would exist between the output of the negative impedance block and the input of the buffer. This mismatch would cause degradation to the oscillator performances.

Thus, in order to design the buffer properly, the output of the negative impedance block should be estimated which can be achieved through a simple FET impedance test setup (Figure 3.12). The input port (source port of the FET) is shorted to represent a reflection of one as negative impedance occurs when the reflective is equal or greater than one. The gate of the FET is grounded as it is a common gate oscillator configuration. Using this test setup, the estimated output impedance is found to be 100 Ω (Figure 3.13). The imaginary part is not considered as it is most likely very inaccurate as the feed inductance *L2* at the drain port can greatly affect the imaginary part.

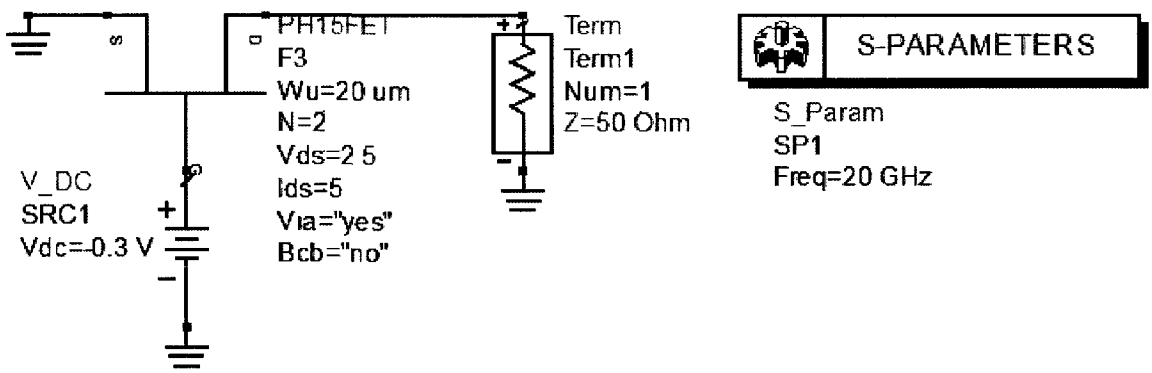


Figure 3.12 Simple FET impedance test setup

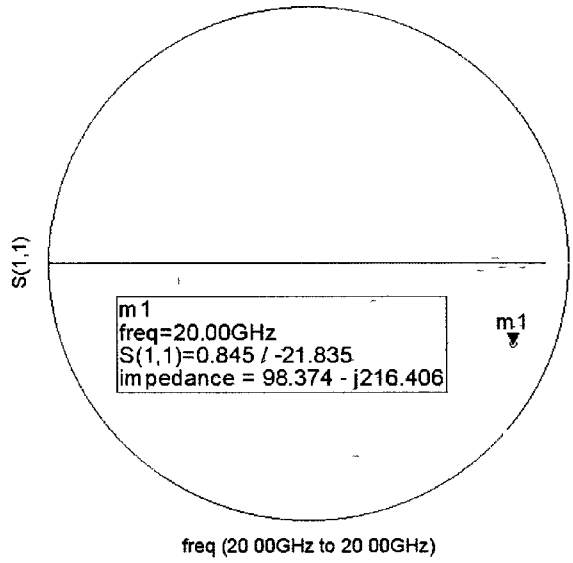


Figure 3.13 Output impedance of simple FET test

Once the estimated input impedance is known, the next step is to find the best buffer configuration to provide optimum gain (high S_{21}) with lowest loss and good matching (low S_{11} and S_{22}) using 100 Ω as input impedance and 50 Ω as output impedance (Figure 3.14). The details of the three types of amplifier designs (common drain, common gate and common source) are shown in Appendix B and are discussed below in Section 3.3.1 to 3.3.3. The final results are summarized below Section 3.3.3.

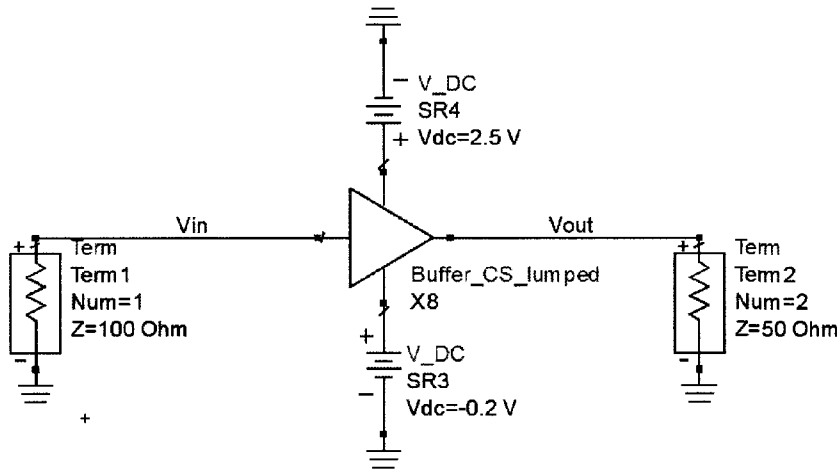


Figure 3.14 Buffer amplifier configuration test bench

3.3.1 Common Drain (Source Follower)

The source follower (CD) amplifier design is problematic in terms of stability and matching in the presence of small FET size and drain resistance (*R2* = 10 Ω). However, this is overcome by using a large FET size, 8x40 μm, and a higher resistance, *R2* = 50 Ω. The details of the design are shown in Appendix B (B-1, pp. 130). The results provide a moderate matching at the input port ($|S_{11}|$ = 0.729 or -2.7 dB) and an excellent matching at the output port (very close to 50 Ω; $|S_{22}|$ = 0.049 or -26 dB) but poor gain (S_{21} = -3 dB). However, poor gain is expected in a source follower configuration as the primary function of CD is to provide good matching and thus a typical 3 dB loss is expected.

3.3.2 Common Gate

The common gate (CG) amplifier design features an excellent input match and a better S_{21} gain than the source follower configuration but has a very poor output match. The selected FET size also has to be quite large to enhance the output match as well as the gain. The details are again shown in Appendix B (B-2, pp. 133). With a FET size of 6x40 μm and a gate resistance *R1* of 500 Ω, input match for the CG amplifier design ($|S_{11}|$ = 0.291 or -8 dB) is 5 dB more superior than the CD amplifier design. The S_{21} gain is also improved by 1.6 dB (S_{21} = -1.4 dB for CG) from CD to CG design. Output match, however, is significantly degraded compared to the CD design; the output reflection ($|S_{22}|$ = 0.468 or -6.5 dB) for CG configuration is almost 20 dB worse than the CD configuration as previously discussed.

3.3.3 Common Source

The common source (CS) amplifier design features an excellent S_{21} gain and output match but with a poor input match. The FET size in common source configuration is not as important as the above two method since only the output match is improved as FET size increases but not the input match or the gain. However, a sweet spot in terms of input match ($|S_{11}|$ = 0.805 or -1.9 dB) and gain (S_{21} = 11.4 dB) can be found when the FET size is being varied and the optimum size is found at 2x50 μm when the stabilizing resistor *R1*

= 5 Ω is used. The stabilizing resistor is used to ensure unconditional stability for the amplifier at all frequencies and can be used to improve the input match. However, by doing so, both the gain and the output match degrade and thus stabilizing resistor is kept low. The output match is also found to be excellent when 2x50 μm FET is used ($|S_{22}|$ = 0.377 or -8.5 dB). The details are again shown in Appendix B (B-3, pp. 136).

In order to select the best amplifier configuration for use as the buffer amplifier in the oscillator design, it is very useful to look at Table 3-1 where pros and cons of the three types of amplifiers are summarized. The pros and cons are scaled based on the simulated s-parameter values where:

- Excellent implies values above 8 dB/below -8 dB
- Good implies values between 6 to 8 dB/-8 to -6 dB
- Moderate implies values between 4 to 6 dB/-6 to -4 dB
- Fair implies values between 2 to 4 dB/-4 to -2 dB
- Poor implies values between 0 to 2 dB/-2 to 0 dB

Table 3-1 Pros and Cons summary of the three amplifier configurations

	CD Amplifier	CG Amplifier	CS Amplifier
Input match	Fair	Excellent	Poor
Output match	Excellent	Good	Excellent
Gain	Fair	Poor	Excellent

Based on comparing the three amplifier configurations, the CS configuration was selected as it holds two excellent features, the output match and the gain (Table 3-1). However, as the input match is very poor, the design of the negative impedance block may be difficult. The CG configuration, although less ideal, can also be considered. The problem with the CG configuration is that gain is very poor, and therefore a second amplifier would be required to obtain the target output power. Since more circuitry would add more complexity and noise to the design, the CG configuration was not selected. In comparison with CG and CS, the CD configuration only stood out in one category, the output match, and hence the choice was obvious.

3.4 Noise Reduction

Thanks to the advanced simulator tool in ADS, noise reduction is made easy by looking at the noise contributor chart (Table 3-2). Since the oscillator design will make use of an external high Q resonator, it is necessary to make sure the highest contributor on the noise contributor list is coming from the resonator. This is to ensure that all noise is lower than the noise coming from the resonator and thus if resonator Q is improved, the phase noise will improve as well.

Table 3-2 Noise contributor list before noise reduction

index	vnc	name	var("type")
noisefreq=100.0 kHz			
0	-111.2 dBc	_total	_total
1	-115.9 dBc	R1	R
2	-116.9 dBc	X4.R1	R
3	-118.9 dBc	X1.R3	R
4	-119.6 dBc	X5.L1	L
5	-125.4 dBc	X5.L2	L
6	-126.9 dBc	X4.L6	L
7	-143.8 dBc	X4.L5	L
8	-300.0 dBc	UMS_TechInclude	UMS_TechInclude
9	-300.0 dBc	X4.F3	PH15NHF
10	-300.0 dBc	X5.F2	PH15NHF

In the noise contributor list, the main concerns are noises index 1 and 2 since index 3 with the noise of -116.9 dBc/Hz from *X1.R3* is the noise coming from the parallel resonant circuit (Table 3-2). *R1* is the final output load impedance and *X4.R1* is the stabilizing resistor from the buffer amplifier. In order to reduce the losses through *X4.R1* (index 2), the resistance on the stabilizing resistor is further reduced. It was determined that 3 Ω is the lowest that the buffer can tolerate while maintaining unconditional stability. On the other hand, the loss through the output load impedance *R1* (index 1) can be reduced if the resistance value *R1* is increased as the oscillator would like to see a high impedance load, 200 Ω or higher (details in Section 3.2.4). However, in order to keep the output load at 50 Ω for lower loss at the connector interface, a quarter-wave transformer is required to transform the high impedance back down to 50 Ω (Figure 3.15). The noises

can be reduced with the added quarter-wave transformer and the resulting dominating noise is now from the resonant circuit, *X1.R3* (Table 3-3).

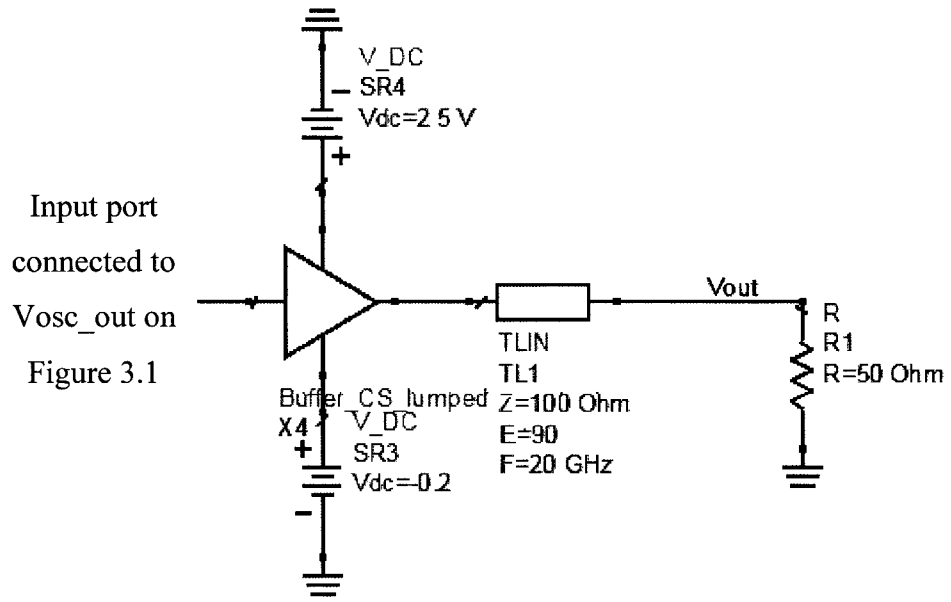


Figure 3.15 Output matching with quarter-wave transformer

Table 3-3 Noise contributor list after noise reduction

index	vnc	name	var("type")
noisefreq=100.0 kHz			
0	-113.9 dBc	_total	_total
1	-119.4 dBc	X1.R3	R
2	-119.6 dBc	X5.L1	L
3	-120.2 dBc	R1	R
4	-121.5 dBc	X4.R1	R
5	-128.1 dBc	X5.L2	L
6	-131.5 dBc	X4.L6	L
7	-142.3 dBc	X4.L5	L
8	-300.0 dBc	UMS_TechInclude	UMS_TechInclude
9	-300.0 dBc	X4.F3	PH15NHF
10	-300.0 dBc	X5.F2	PH15NHF

3.5 Frequency Doubler

A frequency doubler is briefly examined here as the oscillator examined in the previous sections need to have an output of 40 GHz in order to meet the specification. The frequency doubler is a very simple transmission line harmonic trap implemented inside

the buffer amplifier. It is at the gate port of the FET to ensure only the second harmonic is being amplified while the first and third harmonic is shorted to ground (Figure 3.16).

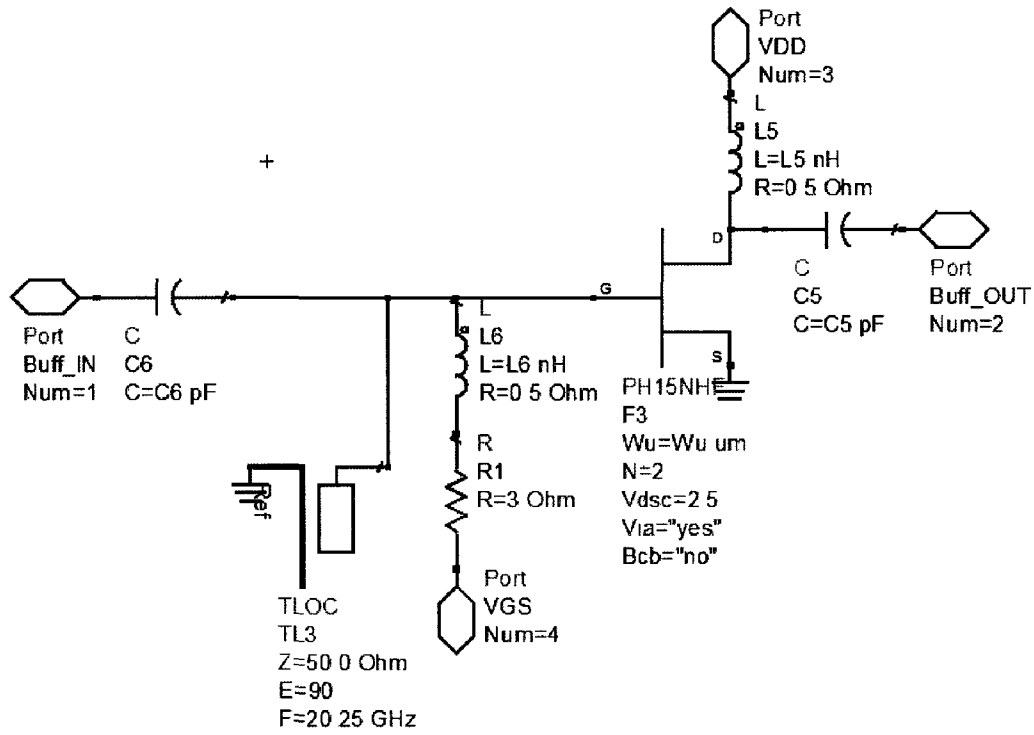


Figure 3.16 Buffer amplifier with embedded frequency doubler

Since a new component, the open transmission line stub (TL3 on Figure 3.16), is being introduced into the buffer amplifier, it is necessary to tune the buffer amplifier again in order to obtain optimal phase noise and output power. The first parameter to test is the size of the buffer which was tested by fixing the bias voltages to the same value as used for the negative impedance block in order to minimize DC sources but it was tuned later to find the optimal point. When the harmonic trap is added, the phase noise performance is excellent with values over -112 dBc/Hz for all gate finger width (*Wu*) above 30μm (-112 dBc/Hz at 100 kHz offset is the target goal at 40 GHz as specified in Section 2.3). Thus the size is being tuned for optimal output power for any *Wu* equal or greater than 30 μm. The output power reaches a maximum when *Wu* = 35 μm (this is for gate fingers of 2; Figure 3.17).

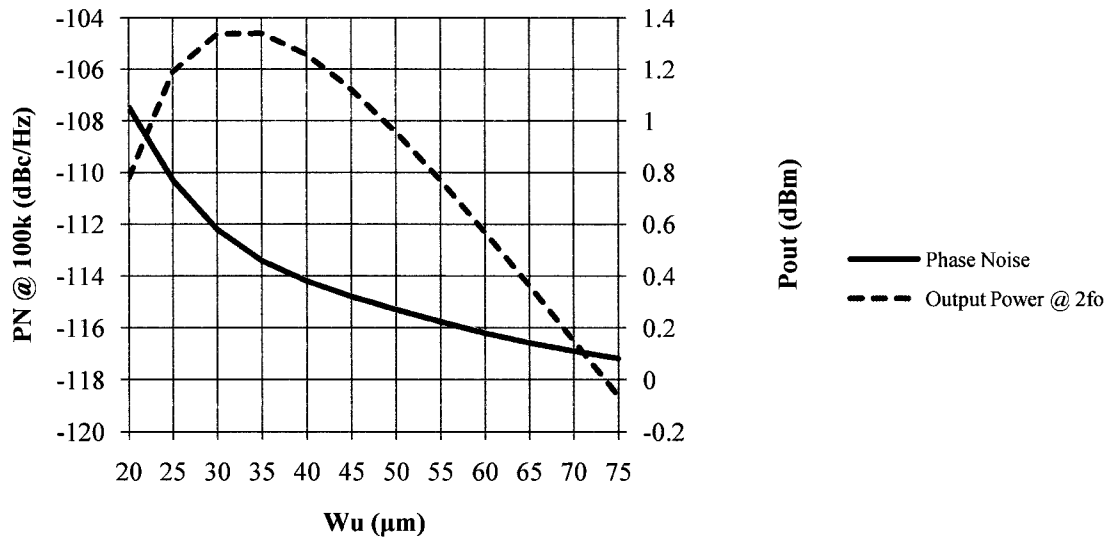


Figure 3.17 PN and P_{out} versus W_u with presence of doubler

The biasing voltages, VDD and VGG, for drain and gate biases of the buffer are also optimized for power. The bias voltages were first swept together at a broader range of voltages to see the approximate optimal point, then it was pin-pointed down to VGG = 0.1 V. Hence, the gate bias, VGG, is found to be optimal at 0.1 V (Figure 3.18) and the drain bias, VDD, is optimal at 2 V (Figure 3.19). The power at the second harmonic is still very low at around 2.4 dBm with the change in bias voltages hence further tuning in required in the buffer, such as the feed inductances or the blocking capacitors.

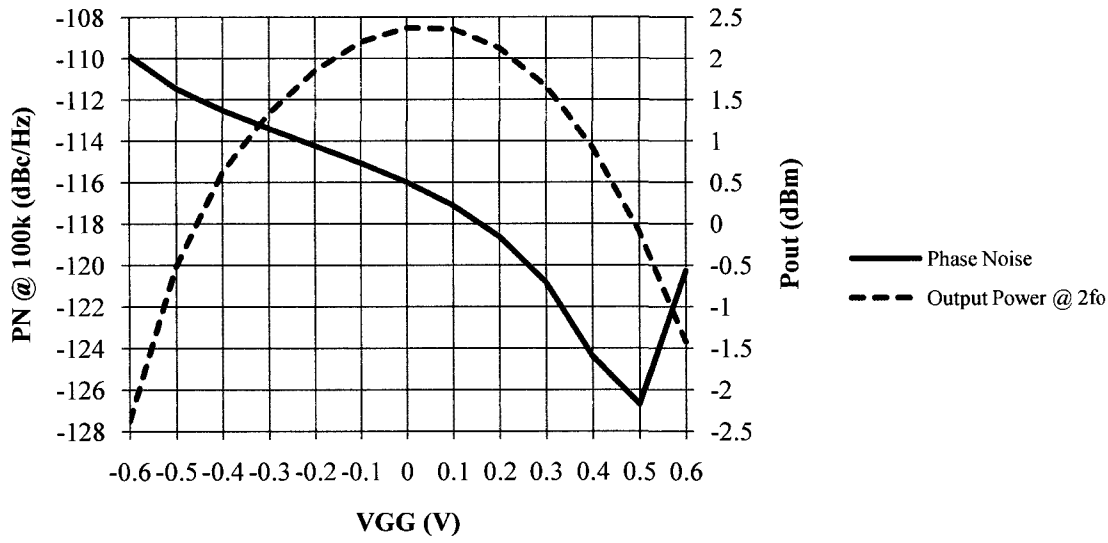


Figure 3.18 PN and P_{out} versus VGG with presence of doubler

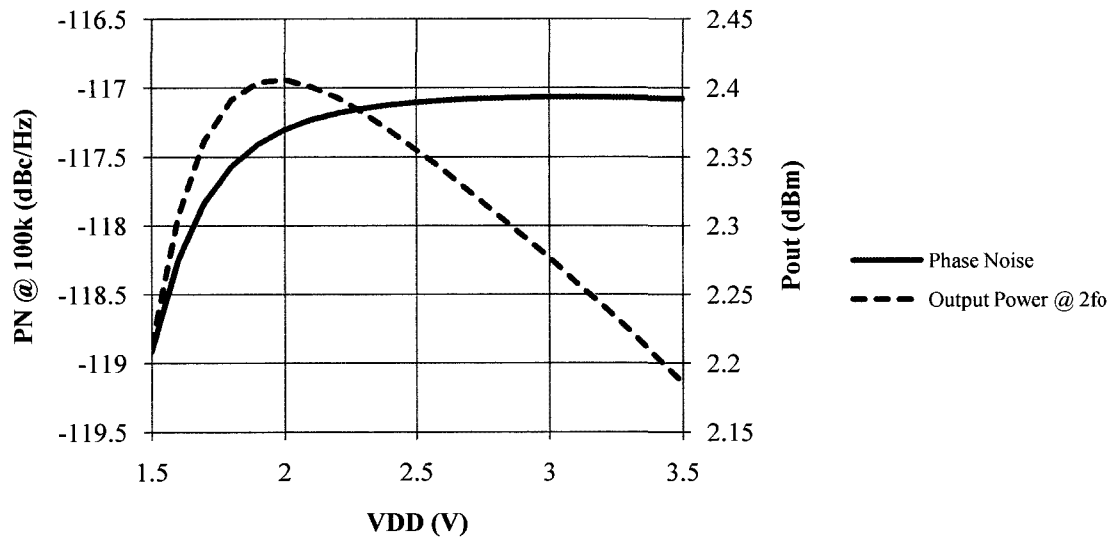


Figure 3.19 PN and P_{out} versus VDD with presence of doubler

The feed inductances *L5* and *L6* (Figure 3.16) are expected to lead to higher output power if their parasitic losses are reduced with lower inductance values. However, it is also very important to ensure the feed inductances still function properly by an RF block while maintaining a short circuit path for DC currents. The phase noise and output power start to degrade for inductances below 0.2 nH as *L6* is varied (Figure 3.20). At this

point (0.2 nH), it appears that the feeding mechanism starts to malfunction. The values of *L6* was chosen to be 0.3 nH to be on the safe side as well as maintaining good phase noise at around -114 dBc/Hz at 100 kHz offset. The output power is now improved to around 5 dBm.

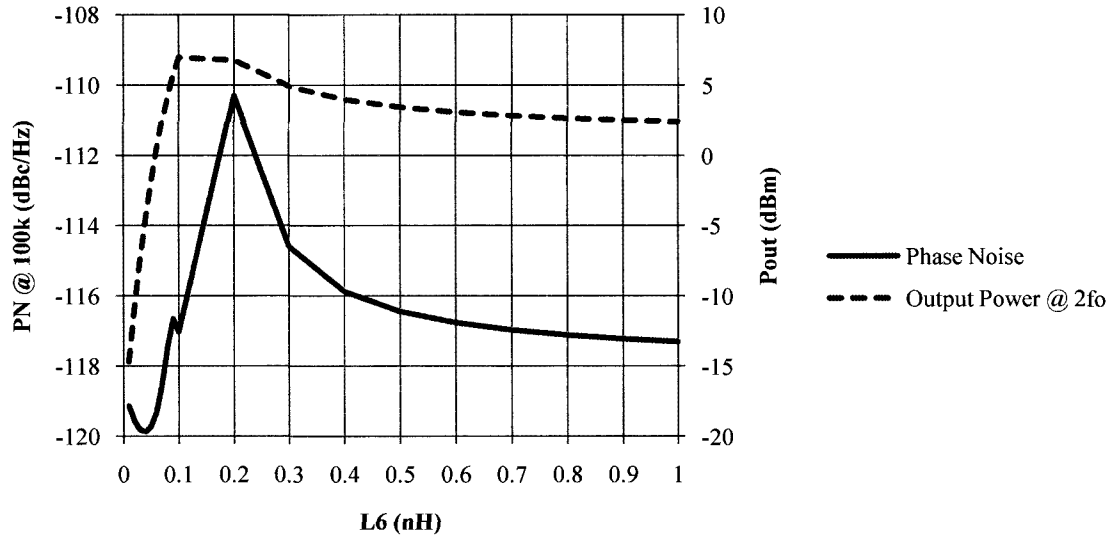


Figure 3.20 PN and P_{out} versus *L6* with presence of doubler

The drain feed inductance, *L5*, gave similar results except there is not much improvement in the output power. The feed inductance once again starts to malfunction for values below 0.2 nH (Figure 3.21). The values of *L5* is again chosen to be 0.3 nH to provide some safe margin and the phase noise and output power at this point is -115.5 dBc/Hz at 100 kHz offset and 5.1 dBm, respectively.

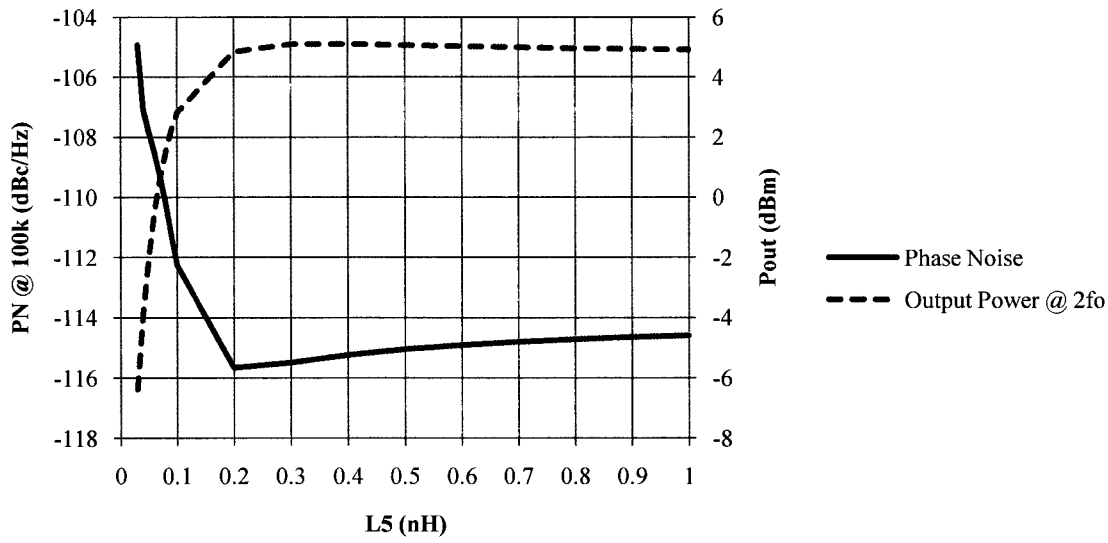


Figure 3.21 PN and P_{out} versus *L5* with presence of doubler

Contrary to the feed inductances, the input series blocking capacitances, *C6*, should be increased in order to minimize losses. The output power saturates at around *C6* = 2 pF (Figure 3.22).

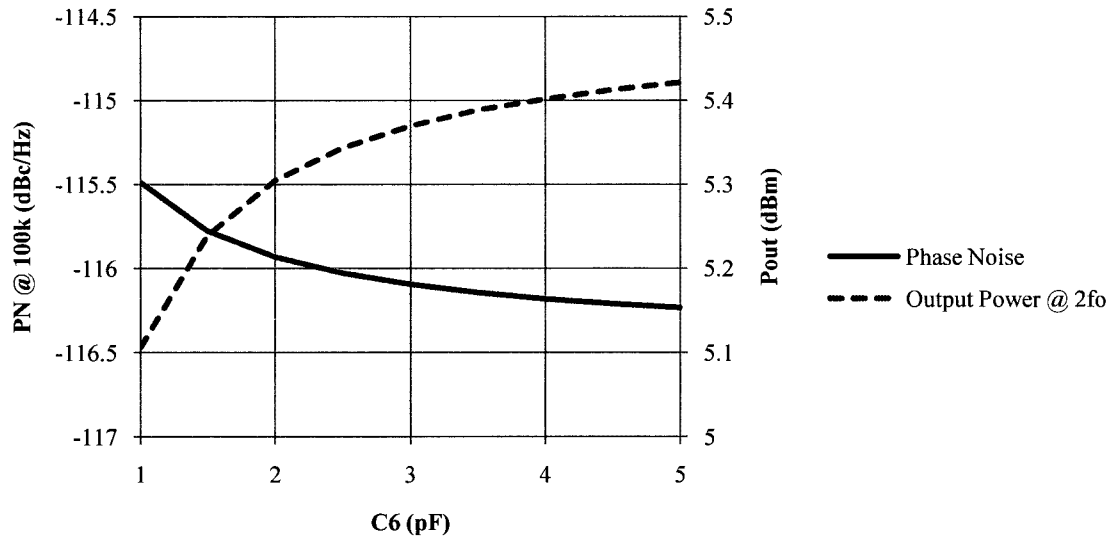


Figure 3.22 PN and P_{out} versus *C6* with presence of doubler

The output series blocking capacitance, *C5*, however, should be decreased since a high impedance load is preferred for high output power. Similar to the feed inductance, the blocking capacitor's function is to provide a virtual open circuit to the DC currents. The blocking capacitor is found to malfunction for capacitances below *C6* = 0.3 pF; hence, 0.3 pF is used (Figure 3.23). It should be noted that although tuning the capacitances can slightly improve the output power, no significant enhancement was observed. The final output power is 5.3 dBm (0.2 dB improvement) and the phase noise is at -116 dBc/Hz at 100 kHz offset.

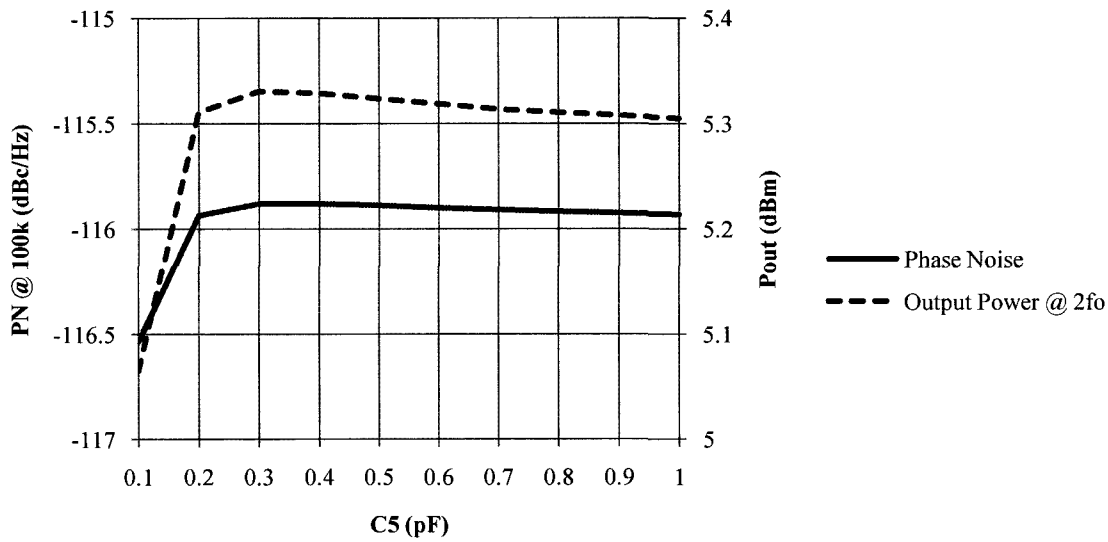


Figure 3.23 PN and P_{out} versus *C5* with presence of doubler

Throughout the above analyses, the oscillating frequency changed slightly from 40.3 GHz down to 39.9 GHz. Since in Section 3.2.2, the compensating capacitance is added to lower the frequency to 20 GHz, the Cc is now reduced to 30 fF to increase the frequency. The resulting second harmonic power is approximately the same at 5.4 dBm while the phase noise is improved to -121 dBc/Hz at 100 kHz offset.

The frequency doubler discussed in this section improves the performance of phase noise but the output power at the second harmonic still remains to be very low in comparison to the target specification. As a result, an external power amplifier would be required in order to bring the final output power to 15 dBm as specified.

3.6 Resonators and Limits of Quality Factor

As mentioned earlier, two kinds of external resonators will be simulated with the oscillator design. One is the λ/4 shorted microstrip on a RT/Duroid 5880 substrate from Rogers Corporation. The other one is the high Q hemispherical cavity resonator [4].

Although a higher quality factor, Q, helps to reduce the oscillator phase noise, this will reach a limit when other components inside the oscillator design begin to dominate. Thus, part of this thesis study involving the resonators is to study the limit of the resonator Q to the oscillator core design.

3.6.1 RT/Duroid 5880 Microstrip Resonator

In order to find the Q limits to the oscillator phase noise, calculations were done to transform the λ/4 RT/Duroid 5880 microstrip resonator to its parallel lumped components equivalent (i.e. parallel RLC). The complete analysis can be found in Appendix C. The resulting parallel lumped resonant circuit was designed (Figure 3.24).

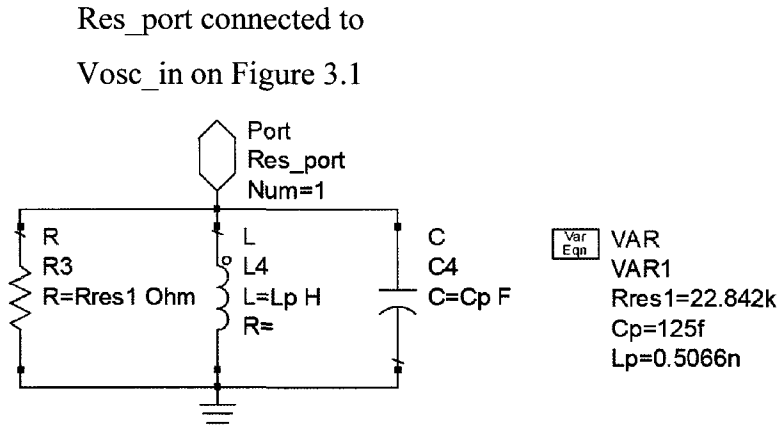


Figure 3.24 Parallel lumped equivalent resonant circuit for RT/Druoid 5880 λ/4 microstrip resonator

In order to find the point where phase noise no longer improves with better Q factor resonators (Q limit), the parallel resistance, *R*, is increased, while keeping the *LC*

tank the same. This is due to the relationship between Q and R defined by the equation (3.1) for parallel resonant circuits.

$$Q = \omega_0 RC = \frac{\omega_0 R}{L} \tag{3.1}$$

The resulting Q limit is around 2000 when the phase noise saturates close to -119 dBc/Hz at 100 kHz offset (Figure 3.25).

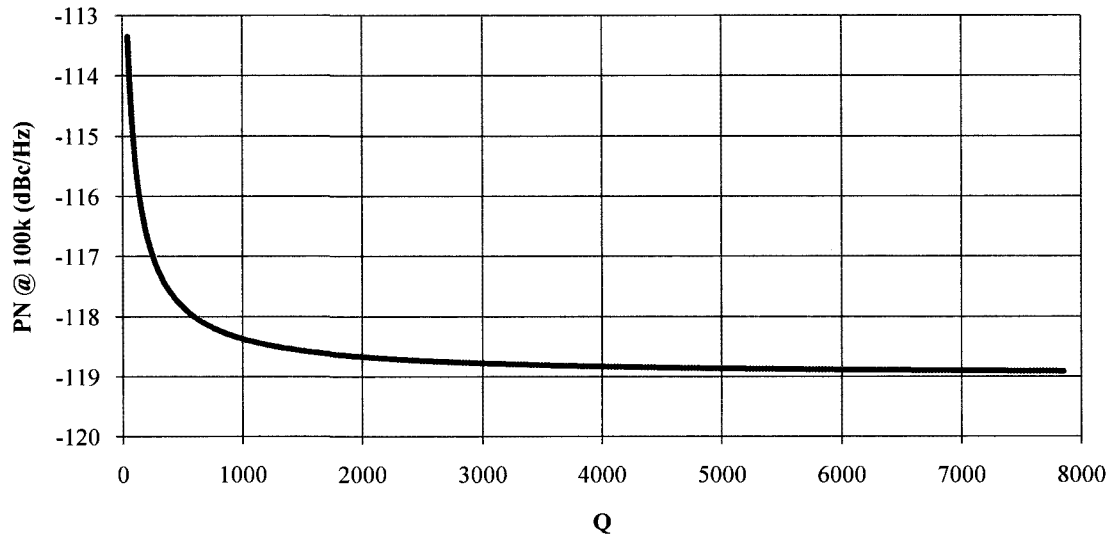


Figure 3.25 PN versus Q using parallel lumped equivalent of RT/Duroid 5880 λ/4 microstrip resonator

It was initially thought that the above method would be able to provide an insight to the Q needed if higher Q resonators using different materials are built, such as the hemispherical cavity resonator. However, in the next section, this is proven to be inaccurate for determining the actual needed quality factor.

3.6.2 High Q Package-Embedded Hemispherical Cavity Resonator

In the previous section, it was determined that the Q limit is at around 2000 with the phase noise of -119 dBc/Hz at 100 kHz offset. This was proven to be inaccurate when the

high Q hemispherical resonator was under test. The phase noise was simulated using the hemispherical cavity resonator .s1p file (one port s-parameter file) obtained from E. Ruscito (Figure 3.26). It can be seen that the phase noise is far better than just -119 dBc/Hz; the resulting phase noise at 100 kHz offset is -125 dBc/Hz.

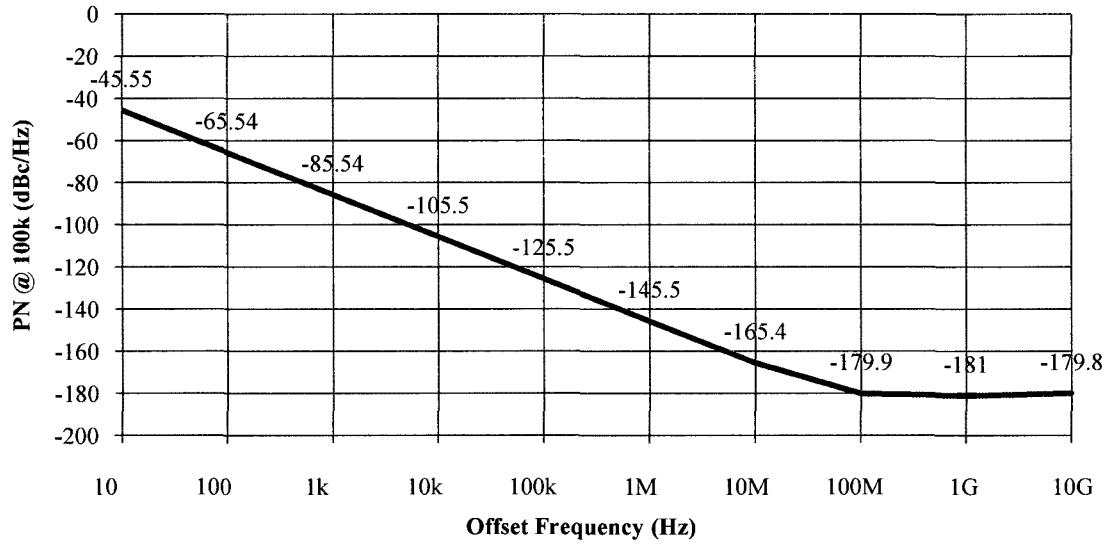


Figure 3.26 PN plot using high Q hemispherical cavity resonator .s1p file

Looking back at equation (3.1), it can be seen that besides the contribution from the parallel resistance, *R*, the Q factor is also defined by the parallel capacitance, *C*, and the parallel inductance, *L*. Since inductance and capacitance relates directly to the magnetic and electric field that is produced by the medium under test, it is understandable that the fields in the RT/Duroid 5880 microstrip would be different than the hemispherical cavity that is made of a gold plated brass metal. The Q factor depends heavily on the location of the maximum magnetic field [4]. It is then implicitly understood that the inductance that corresponds to the maximum magnetic field would provide the highest Q that is obtainable from the medium under test (in this case, the hemispherical cavity resonator).

In order to find the parallel lumped equivalent circuit for the hemispherical resonator, the parallel inductance, *L*, and the parallel capacitance, *C*, are tuned simultaneously to maintain the same resonant frequency (i.e. 20 GHz) while trying to

achieve a lower phase noise. The relationship is defined by the resonant frequency equation, (3.2).

$$\omega_o = \frac{1}{\sqrt{LC}} \tag{3.2}$$

The L and C are tuned until the saturating phase noise at Q of around 5300 matches the one found above using the Touchstone .s1p file (i.e. -125.5 dBc/Hz); Figure 3.27. This is because the Q of 5300 corresponds to the maximum Q that can be obtained using the hemispherical resonator [4].

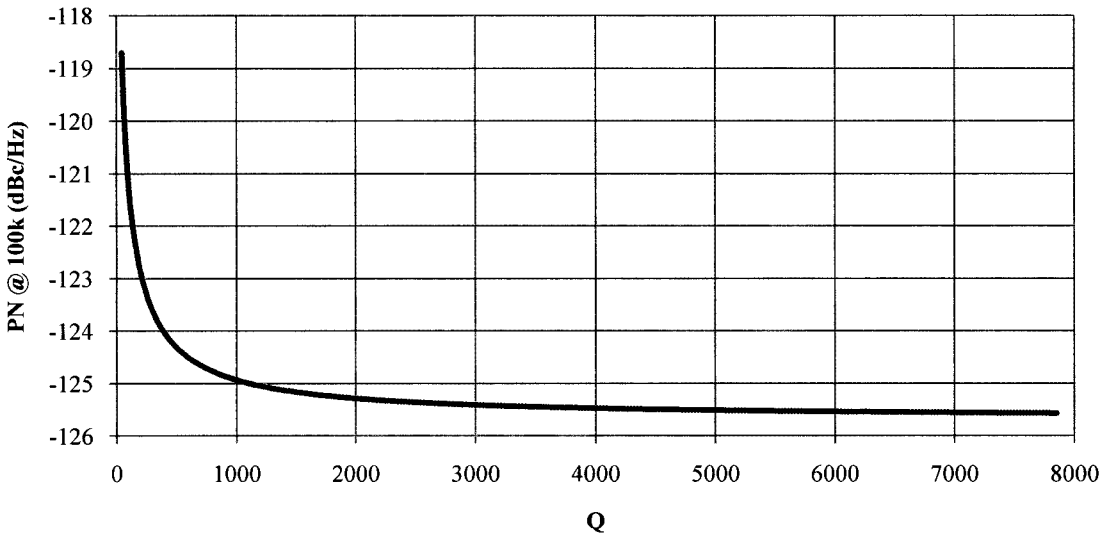


Figure 3.27 PN versus Q using parallel lumped equivalent of hemispherical cavity resonator

In the equivalent circuit shown in Figure 3.28, it can be seen that the inductance, 0.1456 nH, is 3.5 times smaller than the earlier value used in the RT/Duroid 5880 microstrip resonator (i.e. 0.5066 nH). This is as expected as smaller inductance increases the Q factor as defined by Equation (3.1).

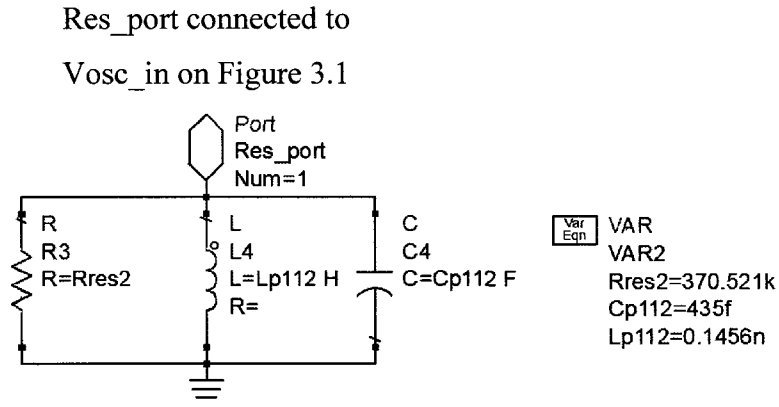


Figure 3.28 Parallel lumped equivalent resonant circuit for hemispherical cavity resonator

3.7 Parametric Simulations on 0.15-um GaAs pHEMT VCO

The parametric study of phase noise, output power and oscillating frequency are done in this section by utilizing the two kinds of the resonators describe in Section 3.6. The simulation results will be compared at the first harmonic, 20 GHz, before adding the frequency doubler as well as at 40 GHz (after adding the frequency doubler).

3.7.1 Modeling of Low Frequency Noise

In the beginning of this chapter, it was discussed that the design kit has some noise modeling technology limits and thus the phase noise simulation is affected. Since the FET noise is not included into the simulation results, the Harmonic Balance phase noise simulation plot (i.e. pnmx plot) only shows the noise from the resonator and the noise floor; it does not include the flicker noise. In order to model more closely to the actual phase noise that is produced at the output, the 1/f noise need to be included. This is done by extracting the low frequency phase noise data from the QinetiQ's noise assessment summary FET noise comparison plot seen earlier in Section 2.2.1 [17]. Since flicker noise is dominant at the low frequency, a slope line was drawn at the beginning of the GaAs pHEMT line and the resulting slope is around -30 dB/decade. This line is only an

estimated line as the flicker noise depends on the FET size and DC biases as well as the process technology. The closest data set found is the 0.25 μm GaAs pHEMT process from the QinetiQ's noise assessment summary. This is, however, a sufficient estimate as smaller FETs produces lower FET noise [35].

After extracting the noise data from the QinetiQ's noise assessment, the noise data is superimposed on the resonator and noise floor plot by means of adding them in the linear scale. An example using the RT/Duroid 5880 microstrip resonator at 20 GHz can be seen in Figure 3.29.

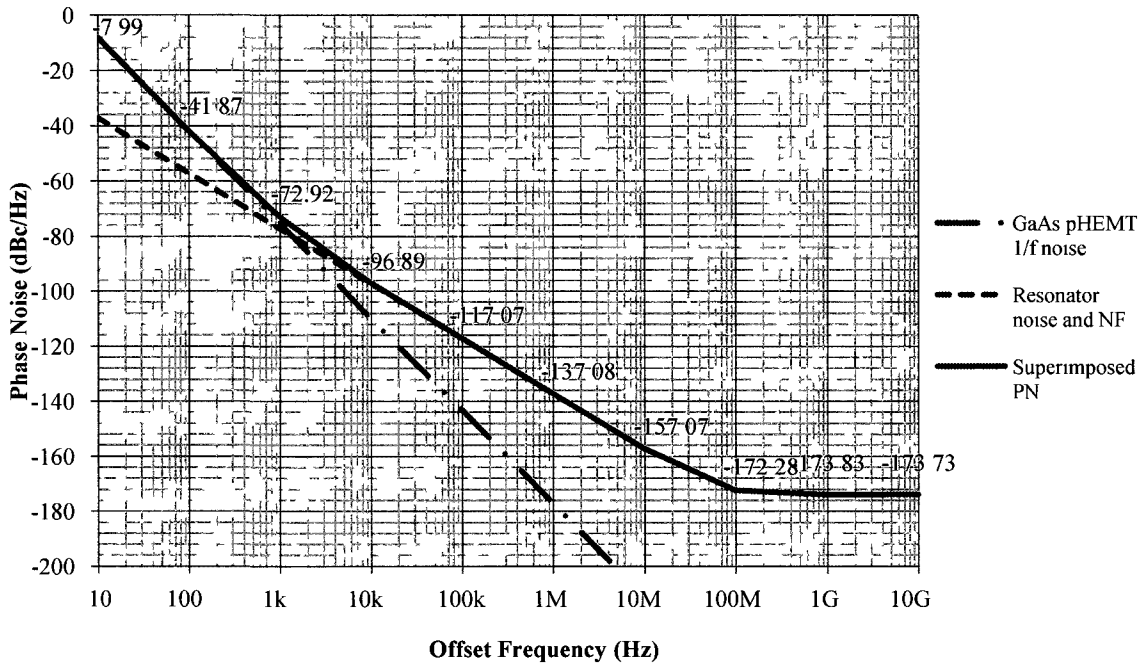


Figure 3.29 1/f noise, resonator noise and NF and superimposed PN using RT/Duroid 5880 microstrip resonator @ 20 GHz

3.7.2 Phase Noise

The oscillator designed in this chapter has been simulated with the two resonators, RT/Duroid 5880 microstrip resonator and embedded hemispherical cavity resonator, described in Section 3.6. Using the superimposition method discussed in the previous section, the single-sideband (SSB) phase noise using the two types of resonators at both

20 GHz (light-coloured lines) and 40 GHz (dark-coloured lines; Figure 3.30) can be estimated. The phase noise for the high Q hemispherical resonators (orange lines) have a lower region 2 than the microstrip resonators (green lines). At 100 kHz offset (approximately the centre of region 2, resonator noise dominant region; Figure 2.8), the phase noise difference between the RT/Duroid 5880 microstrip resonator and the hemispherical cavity is around 8 dB for 20 GHz and 9 dB for 40 GHz. This proves the theoretical assumption that the phase noise can be improved by higher quality factor resonators.

Comparing the PN difference between harmonics, the second harmonic (40 GHz) PN is worse than the first harmonic (20 GHz); the degradation is due to the frequency doubler. As mentioned earlier, the frequency doubler typically degrades the phase noise performance by around 6 dB. In the RT/Duroid microstrip resonator case, the degradation is around 4 dB (using 100 kHz offset). In the high Q hemispherical cavity resonator case, the degradation is less, at only 1 dB. The reason that the degradations are less than the typical 6 dB may be due to the optimization of the buffer amplifier after adding the frequency doubler. Since the phase noise depends on the output load, the improvement in the output stage can also help improve the phase noise.

At region 3 (noise floor dominant region; Figure 2.8), the phase noise differences between the harmonics are very obvious. The phase noises for 40 GHz degraded almost 40 dB from the 20 GHz PN for both types of resonators. This is because the output power at 40 GHz with the doubler is much lower than the power at 20 GHz without the doubler (more details are in the next section). In theory, one of the main controlling parameters for noise floor (region 3) is the output power. In the two cases shown in the graph below, the noise floor is heavily dependent on the output power (Figure 3.30).

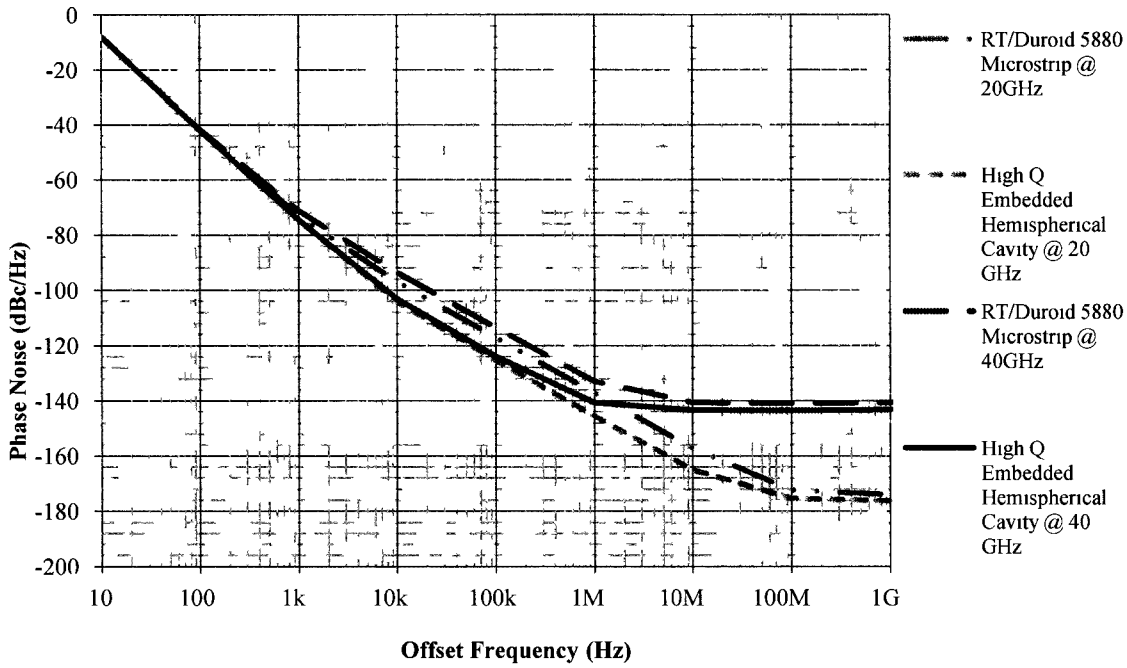


Figure 3.30 SSB phase noise using two types of resonators at 20 GHz and 40 GHz

A phase noise results summary compares the phase noise using the two resonators discussed above with the target phase noise at 100 kHz offset (Table 3-4). Overall, the phase noise performance for the low Q RT/Duroid 5880 microstrip resonator is most likely insufficient to achieve the target phase noise (the results of the idealized simulation only showed 1 dB better than the target). The summary results demonstrated that high Q resonator would be a safer choice to meet the target.

Table 3-4 Results and target summary of phase noise at 100 kHz offset (units: dBc/Hz)

Frequency (GHz)	RT/Duroid 5880 Microstrip	High Q Embedded Hemispherical Cavity	Target Phase Noise
20	-117	-125	-118
40	-113	-124	-112

3.7.3 Output Power

The output powers using the two types of resonators are compared at 20 GHz (Figure 3.31) and also at 40 GHz (Figure 3.32). At 20 GHz, the oscillator output power is around 7 dBm using the microstrip resonator and 9 dBm using the hemispherical resonator (Figure 3.31). This is as expected since output power is proportional to phase noise and the phase noise from the hemispherical cavity resonator is lower than the microstrip resonator as seen in the previous section.

Comparing the first harmonic power from the 20 GHz oscillator (Figure 3.31) with the second harmonic power from the 40 GHz oscillator (Figure 3.32), it can be seen that the 40 GHz oscillator power is twice as low as the 20 GHz oscillator power. The 40 GHz oscillator outputs 5 dBm of power using the microstrip resonator while only 6 dBm of power is achieved with hemispherical resonator (Figure 3.32). The main reason for the degradation is because of the added frequency doubler.

As seen in the 20 GHz output power graph, Figure 3.31, the second harmonic power using the hemispherical resonator is much lower compared to its first harmonic power; a difference of almost 15 dB is seen. This difference makes it difficult to increase the second harmonic power when the harmonic trap is used. The second harmonic power for the 40 GHz oscillator using the hemispherical resonator (Figure 3.32) turned out to be 3 dB lower than the first harmonic power of its corresponding 20 GHz oscillator (Figure 3.31).

A similar trend is seen with the use of the microstrip resonator although the difference is smaller. The power difference between the first harmonic power of 20 GHz oscillator (Figure 3.31) and the second harmonic power of 40 GHz oscillator (Figure 3.32) using the microstrip resonator turned out to be less, at around 2 dB.

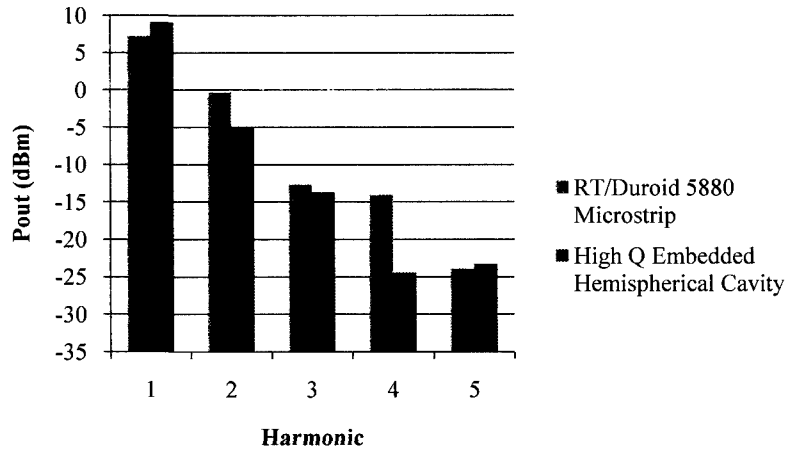


Figure 3.31 P_{out} using two types of resonators at 20 GHz

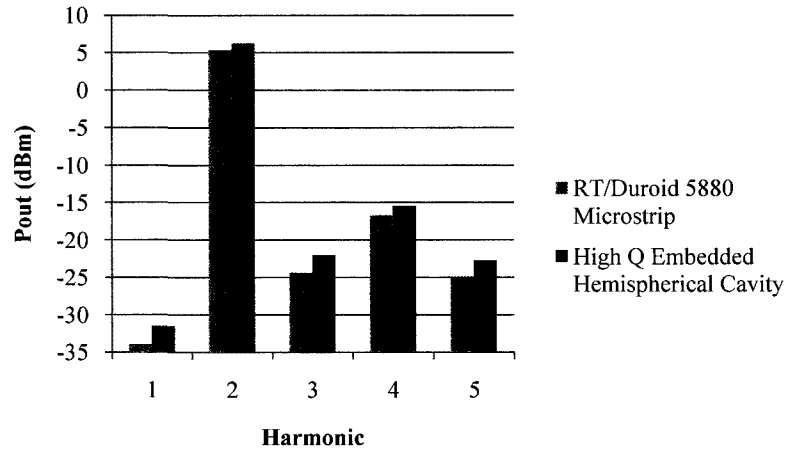


Figure 3.32 P_{out} using two types of resonators at 40 GHz

Overall, the target output power of 15 dBm at 40 GHz is certainly not achievable with the present configuration. Following the conclusion in Section 3.5, an external buffer amplifier would definitely be required.

3.7.4 Oscillation Frequency

The frequency of oscillation needs to be around 40 GHz to be useable for the transceiver design since sub-harmonic pump mixers will be used. However, the resonant frequency is kept at 20 GHz since the resonator is designed at 20 GHz (Table 3-5). This is why an

internal frequency doubler is required. The resonant frequency for the microstrip resonator is theoretically designed at 20 GHz while the resonant frequency for the embedded hemispherical cavity resonator is obtained from the thesis by E. Ruscito.

Table 3-5 Resonator and oscillator frequencies for both types of resonators

	Resonator Frequency (GHz)	Oscillator Frequency (GHz)
RT/Duroid 5880 Microstrip Resonator	20	40.19
High Q Embedded Hemipherical Cavity Resonator	20.26 [4]	40.09

3.8 Summary

This chapter has presented a simulated GaAs pHEMT MMIC design of the oscillator active circuitry. Great insight has been obtained, including the effects of different resonator Q's on achievable phase noise performance.

Chapter 4

40 GHz Ultra Low Phase Noise LO – Simulated Results

In this chapter, the physical layout of a 40 GHz oscillator will be discussed. As mentioned in Chapter 2 and 3, the local oscillator implemented in this chapter is comprised of available COTS components which will be characterized individually. The selected components will be discussed in order of appearance from the input port include: packaging materials, resonator, bondwires, oscillator, low noise buffer amplifier, decoupling and biasing techniques, output launcher and output v-connector (Figure 4.1). Components and final layout simulations will be done and compared with the oscillator design in Chapter 3.

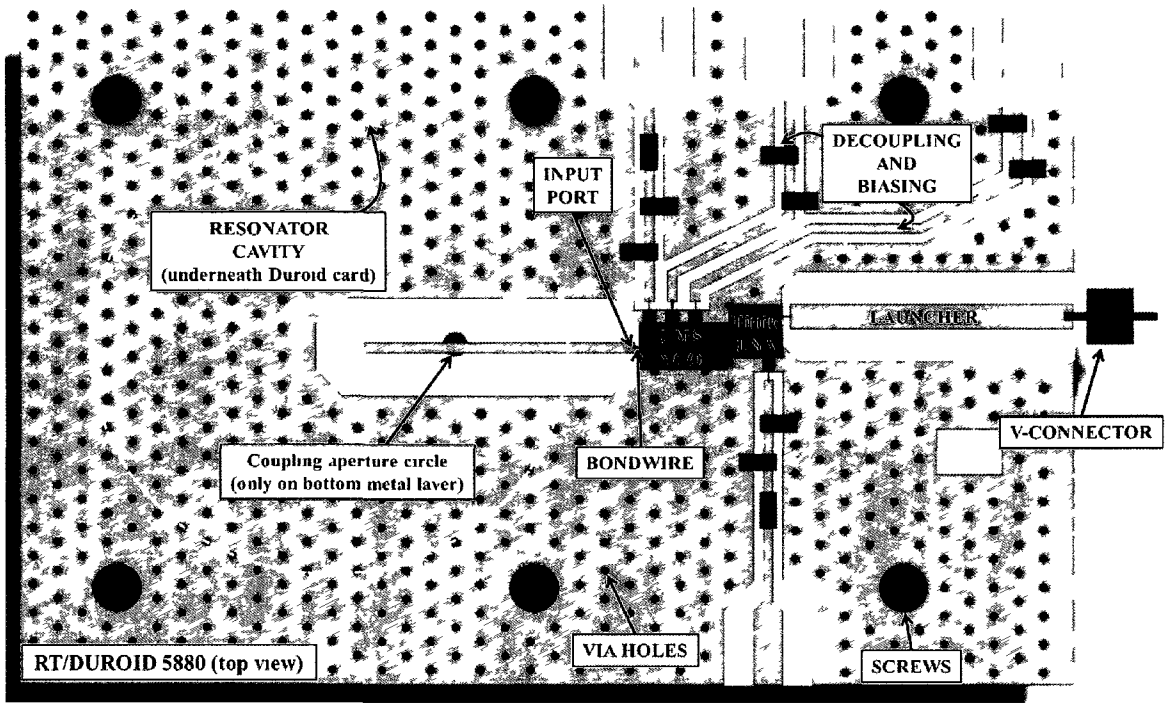


Figure 4.1 Top view of designed LO on RT/Duroid 5880 card

4.1 Packaging Materials

The choice of packaging materials is very important when considering a PCB (printed circuit board) design. This is because the properties of packaging materials can be very different from one another, due to their differences in chemical compositions, and thus can greatly affect the circuit performance. When considering a suitable substrate, the effects on microstrip lines, interfaces with other components, layout, placement and grounding issues need to be taken into account

In this project, RT/Duroid 5880 is selected to be the PCB substrate This is mainly because of its low loss tangent, low dielectric constant and low cost. A comparison between three types of materials, RT/Duroid 5880, alumina and DuPont LTCC (low temperature co-fired ceramic), has been summarized (Table 4-1).

Table 4-1 Material comparisons between RT/Duroid 5880, alumina and DuPont LTCC at 10 GHz [36-38]

	RT/Duroid 5880	Alumina 99.5	DuPont LTCC
Material	PTFE / Micro-fiber glass	Ceramic	Ceramic
Dielectric constant, ε_r	2.2	9.8	7.1
Loss tangent, tan δ	0.0009	0.0001	0.001
Coefficient of thermal expansion (ppm/°C)	x/y/z 31/48/237	7.0	5.8
Thermal conductivity (W/m°C)	0.26	25.5	4.6
Cost (per square foot) for a 2.5 cm x 5 cm piece	$160	$5,000	$18,000
Fabrication turnaround time	3 days	5 weeks	3 weeks

Advantages of RT/Duroid 5880:

- Low ε_r and low tan δ will provide faster wave propagation and lower losses in the substrate. Although tan δ is lowest in alumina, the resulting signal speed would be much slower due to the fact that the alumina has a much higher ε_r; hence, this material was not selected here [39].
- Low cost is one of the most attractive features of the RT/Duroid 5880. In comparison to DuPont LTCC, the cost of a 2.5 cm by 5 cm piece of RT/Duroid 5880 is only one hundredth of the cost of DuPont LTCC (prototyping cost).
- The fabrication turnaround time for RT/Duroid 5880 is also much shorter in comparison to the other materials. Thus, more revisions can be done.

Disadvantages of RT/Duroid 5880:

- Since RT/Duroid is a soft Teflon-based substrate whereas both alumina and DuPont LTCC are hard ceramic-based substrates, the thermal expansion of the RT/Duroid 5880 is much worse than the other two materials. This means that the

material geometry of the RT/Duroid 5880 is much more sensitive to temperature changes.

- Thermal conductivity is also an issue in the RT/Duroid 5880; it is much smaller than the other two types of materials. Higher thermal conductivity will provide better heat sinking for the circuit which is important to minimize thermal expansion problems. One way to help with heat sinking in the RT/Duroid 5880 is to have as many via holes as possible to make sure an effective ground is provided to the top of the substrate in order to have a low thermal resistance path for heat transfer (Figure 4.1).

Since the main purpose of this design is to build a low cost oscillator, RT/Duroid 5880 becomes the best choice. Although previous studies have shown that the high performance and robust features of multilayer LTCC is capable of providing excellent resonator Q and thus better oscillator performance, due to its extremely high cost, it was not chosen for this project [28]. Alumina was not selected either due to its long fabrication time and high dielectric constant.

4.2 High Q Package-Embedded Hemispherical Cavity Resonator

The resonator is one of the most important components in an oscillator design, thus this section will summarize the physical design of the high Q package-embedded hemispherical cavity resonator which is the subject of another thesis (E. Ruscito) [4].

The hemispherical resonator has been predicted to achieve an unloaded Q value of around 5300. This perfect hemisphere is etched from a brass metal and then gold plated afterwards for better conductivity. The packaging includes the etched hemisphere resonator as well as a support for the PCB circuitry mentioned above (Figure 4.2).

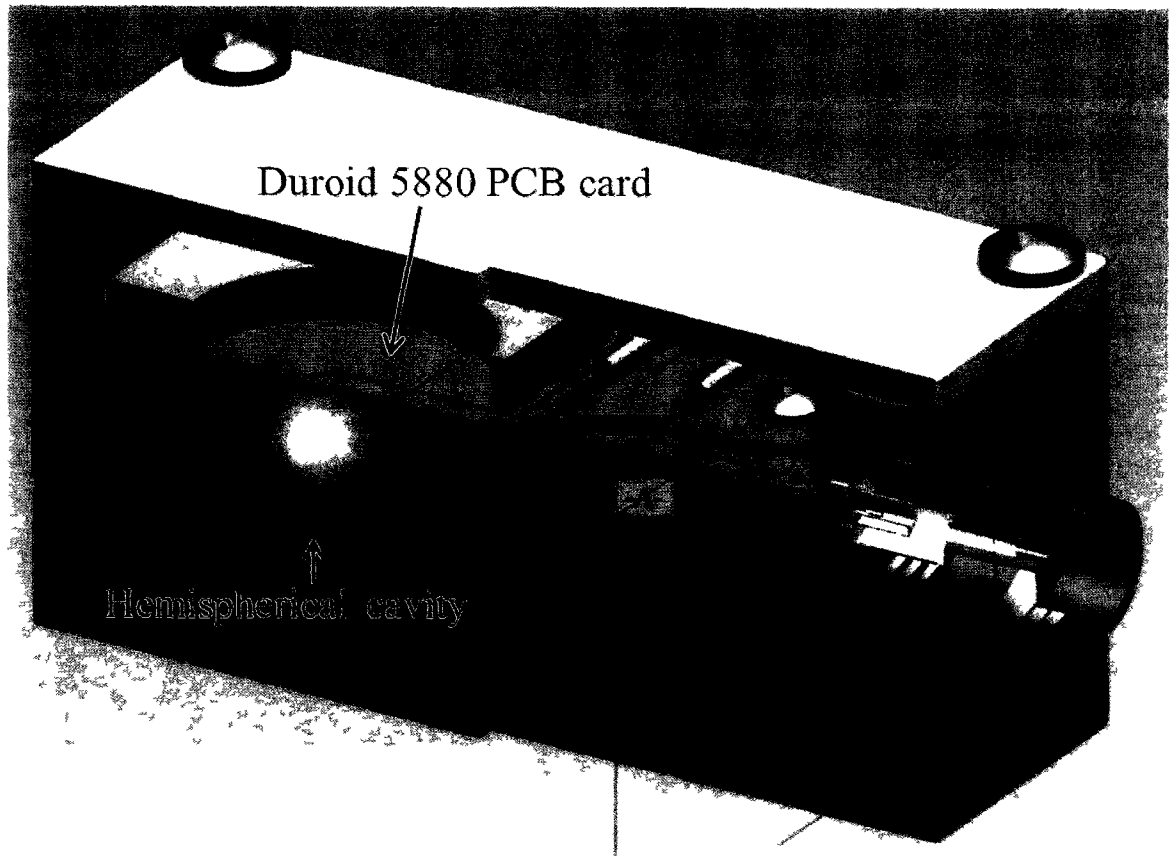


Figure 4.2 Gold-plated oscillator packaging with embedded hemispherical resonator

The hemispherical cavity is coupled to the oscillator circuitry through an circular aperture etched out of the bottom metal layer of the PCB as well as the microstrip feed on the top metal layer of the PCB. This means that both the aperture and the microstrip line have to be carefully designed in order to provide best coupling for highest quality factor. The detailed design again can be found in [4].

Once the energy is provided to the microstrip feed on the top metal layer, the connection between the resonator's feed and the oscillator's active circuitry is just a simple ribbon bondwire, which will be discussed in the next subsection (Figure 4.1). The spacing between the ground plane and the microstrip feed is also increased (around 1 mm) in order to ensure that no coupling can happen between the feed and the nearby ground plane. The sharp corners of the ground plane are tapered by 45 degrees to minimize corner losses (Figure 4.1).

4.3 Modeling of Bondwires

The losses in bondwires are also another important factor to consider in the oscillator design. This is especially important at the resonant port since the negative impedance might be affected and so the oscillation condition may change. In this sub-section, a single ribbon bondwire will be modelled using the simulator tool ADS. The ribbon bondwire has previously been characterized using the electromagnetic simulator tool from Ansoft, HFSS [4]. The ADS model done in this sub-section will be compared to the HFSS model. Both will be used to provide an accurate physical model (more details on the modeling can be found in [40]).

Using the Touchstone 2-port s-parameter file (.s2p) obtained from the HFSS model, the s-parameters can be translated into ABCD-parameters through the following function using ADS simulator.

$$ABCD = stoabcd(S, 50) \tag{4.1}$$

A two-port π-model using series and parallel admittances (Figure 4.3; [16]) can then be obtained using the ABCD-parameters, where

$$Y_1 = \frac{(D-1)}{B} \tag{4.2a}$$

$$Y_2 = \frac{(A-1)}{B} \tag{4.2b}$$

$$Y_3 = \frac{1}{B} \tag{4.2c}$$

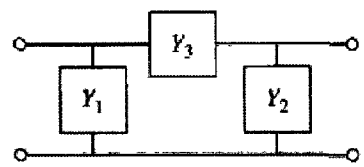


Figure 4.3 π-model circuit from ABCD-parameters [16]

The series inductance and the parallel capacitances are calculated from the admittances which form the ADS model for the ribbon bondwire using lumped components (Figure 4.4). A simpler but less accurate ADS predefined model is also shown for comparison purposes (Figure 4.5).

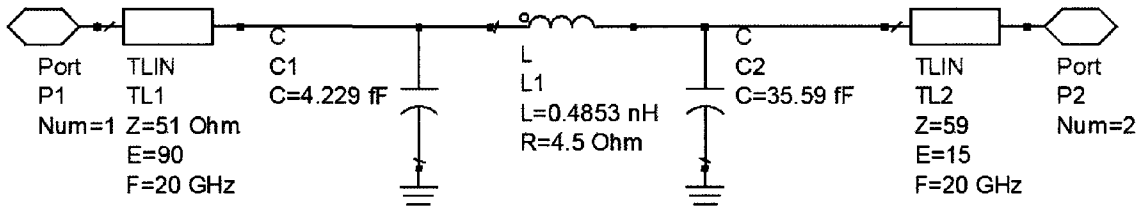


Figure 4.4 ADS lumped model of a ribbon bondwire

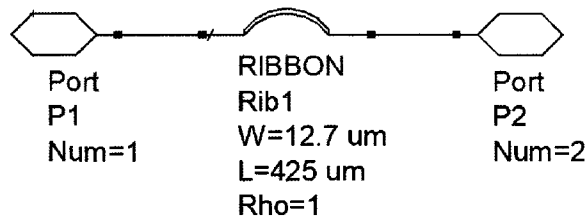


Figure 4.5 ADS predefined model of a ribbon bondwire

Although it is easy to understand the use of a series inductor to model a single bondwire, it is also important to discuss the necessity of the π-model as well as the added transmission lines (Figure 4.4). The reason that the parallel capacitors are needed in the model is because the bondwire interconnects two DC pads. These DC pads form small capacitances with the DC ground and hence it is necessary to model them. On the other hand, the transmission lines are added at the input and output port of the model for impedance matching. It is important to make sure the bondwire model presents the correct impedance at both the input and the output for accurate modeling.

The resulting return loss (S_{11}) and insertion loss (S_{21}) are found in Figure 4.6 and Figure 4.7 where blue lines represent the HFSS model, red lines represent the ADS lumped model and green line represents the ADS predefined model.

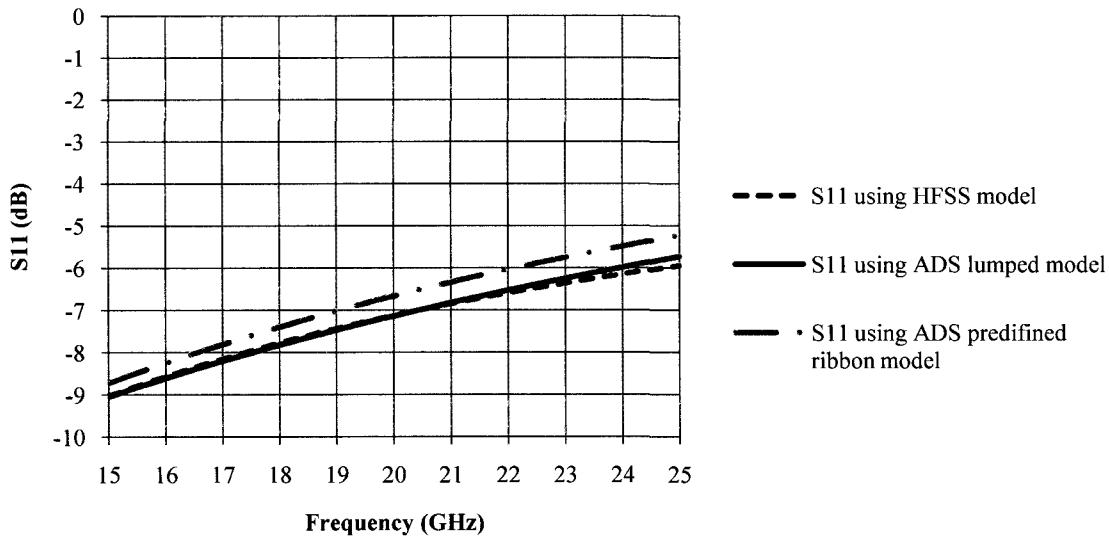


Figure 4.6 Return loss (S_{11}) using HFSS and ADS lumped and predefined models

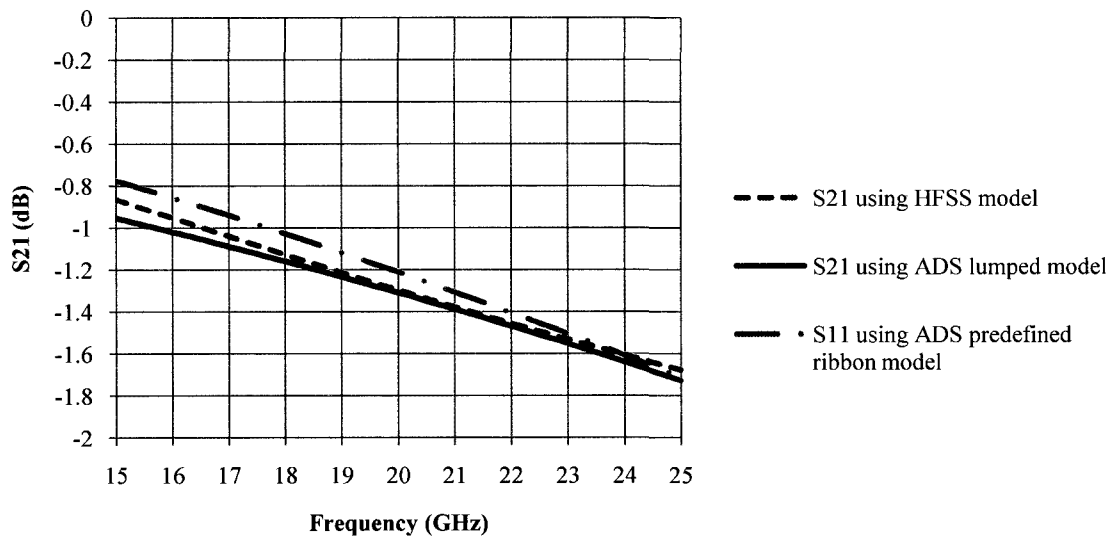


Figure 4.7 Insertion loss (S_{21}) using HFSS and ADS lumped and predefined models

Since this particular ribbon bondwire is for use at the resonant port (20 GHz), the values at 20 GHz are observed. The input return loss (S_{11}) is fairly good at around -7 dB for the HFSS (Figure 4.6) and ADS lumped models while the insertion loss is around -1.3 dB at 20 GHz (Figure 4.7). The ADS predefined model is less accurate compared to the lumped elements model and an optimistic difference in losses is seen in both the

return loss and the insertion loss (between 0.1 to 0.5 dB). Hence, the ADS predefined model will only be used at places where losses in bondwires are less critical. At the resonant port where bondwire loss is critical, the ADS lumped model will be used for more accurate large-signal modeling.

4.4 UMS GaAs K-band VCO and Q-band Doubler

As stated earlier, a commercial chip was used in the physical design. This commercial off-the-shelf (COTS) component from UMS is a GaAs MMIC manufactured with 0.25 μm gate length pHEMT process with the availability of via hole and air bridge technologies; more details can be found in Appendix D or the UMS CHV2240 datasheet [41]. This MMIC also contains a VCO with oscillation frequency around 19 GHz (tunable from 18 to 21 GHz) while the output frequency after the doubler is centered at 38 GHz. The relevant specifications are replicated below in Table 4-2. It should be noted that these specifications are tested using a high Q dielectric resonator with a Q of 10,000.

Table 4-2 UMS CHV2240 Specifications [41]

Parameter	Typical Value	Unit
Output Frequency	38.25	GHz
Tuning range	5	MHz
PN at 100 kHz (38 GHz)	-100	dBc/Hz
P_{out}	9	dBm

As only the s-parameter data (data provided up to 29 GHz with tuning voltages of VT = 0 V and 2 V) of the UMS VCO is available, the input return loss, S_{11}, was simulated to check the condition of oscillation without the presence of a resonator. The simulation was first done using the Touchstone 2-port s-parameter file (.s2p) for a tuning voltage of VT = 0 V. The oscillation occurs near 18 GHz when the magnitude of S_{11} is equal or greater than one and the imaginary part of S_{11} is close to zero (Figure 4.8).

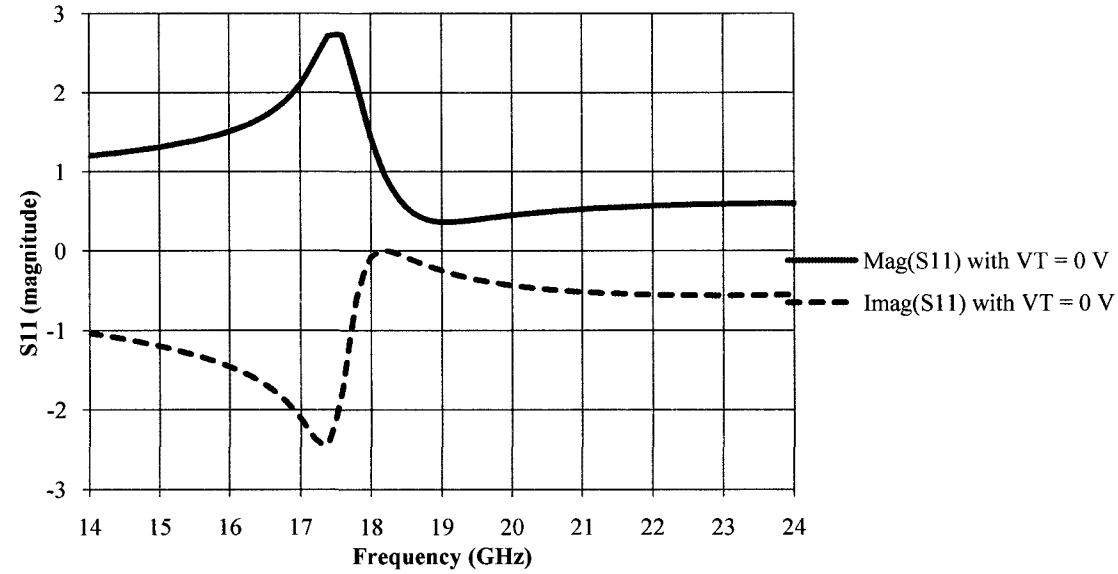


Figure 4.8 Return loss (S_{11}) of UMS CHV2240 with VT = 0 V

The second simulation was done using a tuning voltage of VT = 2 V. This time the oscillation occurs near 21 GHz (Figure 4.9).

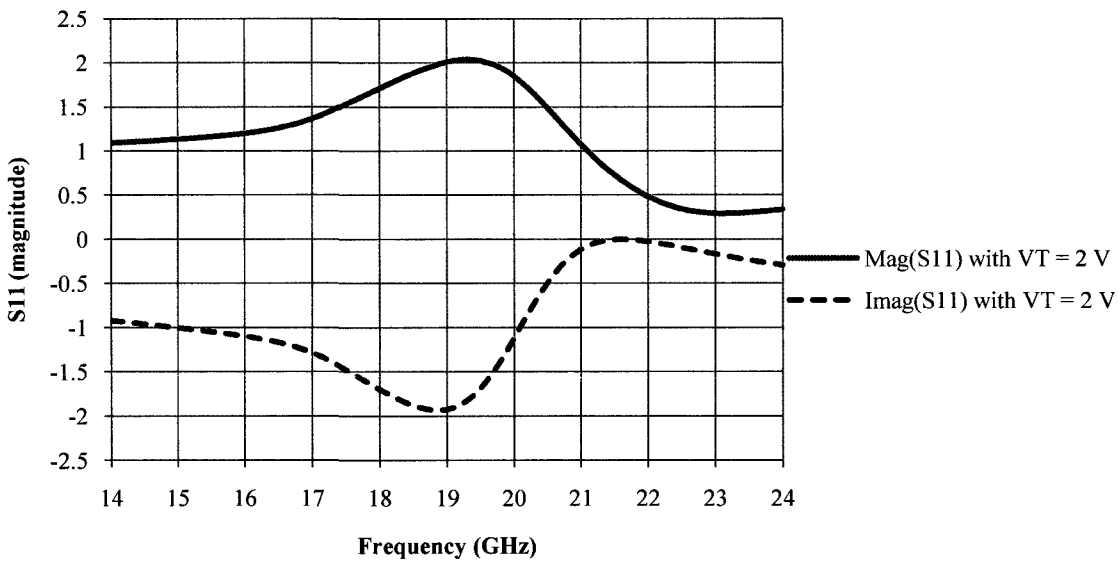


Figure 4.9 Return loss (S_{11}) of UMS CHV2240 with VT = 2 V

It should be noted that this UMS VCO was designed to have a tuning voltage from 0 V to 2 V as specified in the UMS CHV2240 datasheet. This means that the

maximum frequency tuning range can be estimated by combining the results from the minimum voltage, 0 V, S_{11} data (Figure 4.8) with the maximum voltage, 2 V, S_{11} data (Figure 4.9). The estimated tuning range was around 3 GHz (from 18 GHz to 21 GHz) where as the UMS CHV2240 datasheet showed a tuning range of only 5 MHz. This was because the s-parameter data cannot provide any noise or nonlinear information and hence the results were too idealistic. Nevertheless, the resonant frequency (close to 20 GHz) falls within this tuning range and also within the datasheet tuning range and therefore oscillation should occur.

4.5 Hittite GaAs Low Noise Buffer Amplifier

The Hittite low noise buffer amplifier (LNA) is selected based on the power level required by the sub-harmonic mixer which would follow. As mentioned earlier, the LO port of the sub-harmonic mixer requires a power level of 15 dBm. This can be achieved with the selected Hittite LNA (HMC-ALH445; Table 4-3); more details can be found in Appendix E or the Hittite HMC-ALH445 datasheet [42].

Table 4-3 Hittite HMC-ALH445 Specifications [43]

Parameter	Typical Value	Unit
Frequency Range	28 - 40	GHz
Gain	10	dB
Noise Figure (NF)	3.9	dB
P_{out} at 1 dB Compression	13	dBm

The reason that this particular amplifier was chosen was because of its power and gain level (Table 4-3). A 10 dB gain from the LNA is perfect to bring a 9 dBm of power from the VCO to an output level of 16 dBm (predicted saturated power) for the mixer. This would mean that the amplifier would be driven in saturation as a power of 19 dBm (9 dBm + 10 dB) is not obtainable with this Hittite chip.

Although it is important to drive the amplifier in saturation as temperature variations are minimal at saturated power since the output power is no longer affected by

the input power, it is also a great risk in doing so. Since the power amplitude can no longer be increased, much of the AM power would be converted into PM power which could potentially affect the phase noise performance. Nevertheless, on the mixer side, the saturated power will make sure the effects on the power level at the LO port of the mixer is minimized. The saturated power level for this particular amplifier should be around 16 dBm (just a few dBs above the 1 dB compression point, 13 dBm; Table 4-3). With a gain of 10 dB and an input power of 9 dBm, the amplifier will effectively be driven at its saturated power.

An added advantage to this amplifier is that it is also a low noise amplifier with a NF of only 3.9 dB. This means that the system noise will not increase by much with this additional component.

This LNA also provides an advantage in implementation as it is also a GaAs MMIC which is the same as the UMS VCO. This means that the height of the two MMIC (UMS VCO and Hittite LNA) is the same. This will prove to be of a great advantage since the MMICs can be placed much closer in proximity and the bondwire length can be made much shorter.

The input and output return loss as well as the small-signal gain are simulated with the provided .s2p file from Hittite. At the output frequency of 40 GHz, the input and output rejection are both excellent with S_{11} and S_{22} both at around -20 dB (Figure 4.10). On the other hand, the gain at 40 GHz is around 10.8 dB. This LNA also provides broadband gain of 10 dB from around 18 GHz to pass 40 GHz.

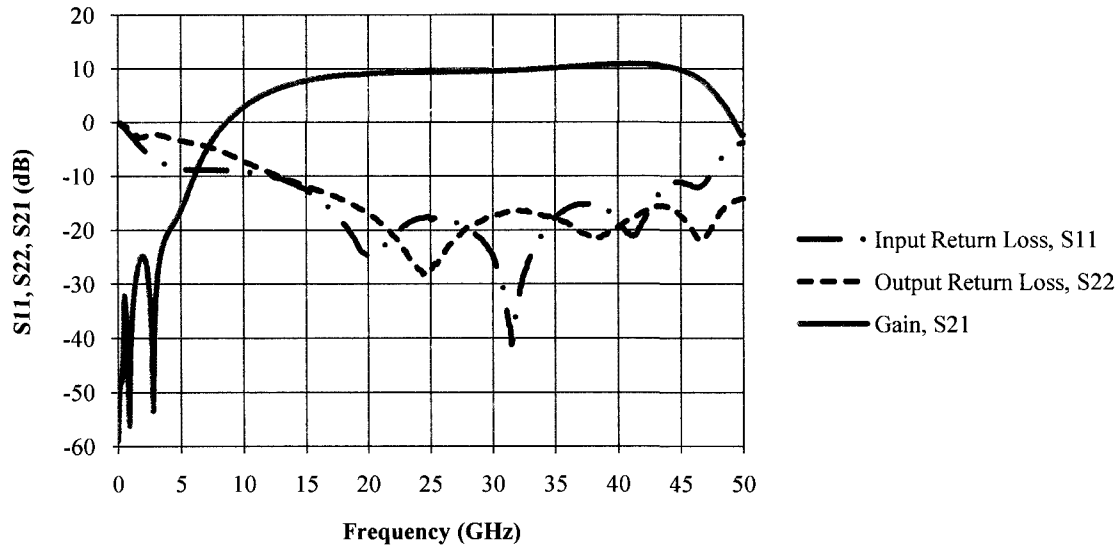


Figure 4.10 S_{11}, S_{22} and S_{21} of the Hittite HMC-ALH445 LNA

4.6 Decoupling and Biasing Techniques

In this section, the layout of the biasing circuit will be discussed. This includes explanations of decoupling and stabilizing component selections, component placement and spacing as well as DC supply lines and ground plane with vias (Figure 4.11).

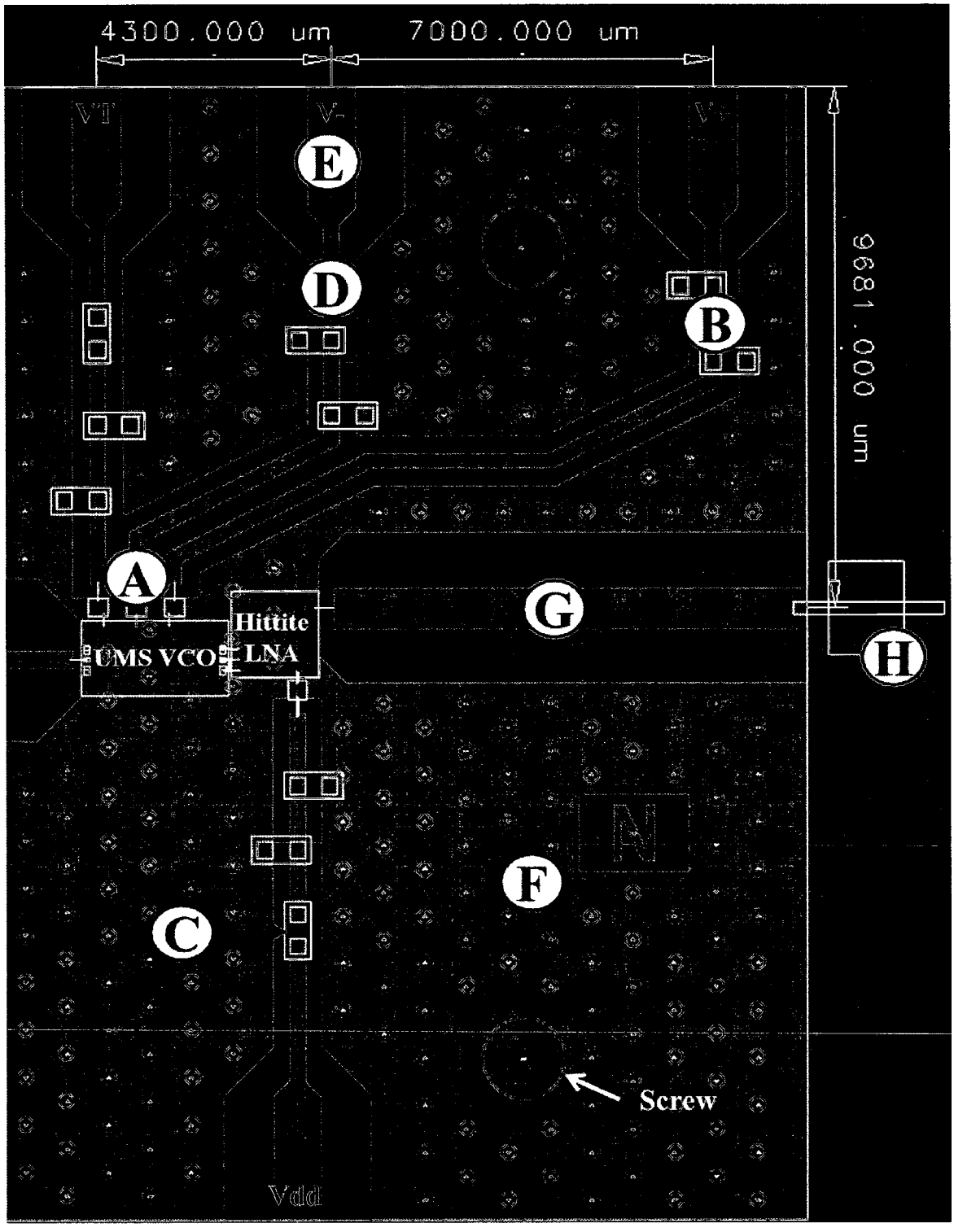


Figure 4.11 Biasing Circuit

4.6.1 Primary Decoupling Capacitor Selection

The primary decoupling capacitor is selected based on the specification sheet. From the specification sheet for the UMS VCO, it is suggested that the decoupling capacitance to be equal to or greater than 120 pF while the Hittite LNA suggests 100 pF. The function of these primary decoupling capacitors is to be able to provide storage for a sudden change in the current draw during transient start-up. This is to ensure a stable DC voltage can be provided to the circuits without affecting the RF (radio frequency) signal. It is required to place these primary capacitors in close proximity to each of the DC supply pads of the MMICs as the capacitance value can drastically be reduced with the added inductance of the bondwires (bondwires are required to connect the MMIC chips to the decoupling circuitry). Region A on Figure 4.11 shows where the primary decoupling capacitors are located and in addition a more detailed figure is shown in Figure 4.12. The short bondwires will help to minimize the added losses from the line inductance as well as to reduce the series resistance of the bondwires between the primary capacitor and the MMIC chip and therefore, helps the primary capacitors to behave normally even at higher frequencies (e.g. 100 MHz).

The primary decoupling capacitors used for both the UMS VCO and the Hittite LNA are single layer microwave bondable capacitors. This type of capacitor forms a shunt capacitor when it is bonded on the top layer and shorted to ground on the bottom layer. The single layer capacitors are usually more compact and hence lower values of capacitors are more readily available. It also does not need to be mounted on the DC tracks which can sometimes be much further away from the chip. The smaller physical dimension (less than 635 μm^2) allows the capacitors to be placed even closer to the MMIC chip to further reduce the bondwire losses. This is why it is more favourable than the surface mount capacitors. The capacitances of the single layer capacitors used in this design are 150 pF for the VCO and 110 pF for the LNA which should be enough to provide low impedance paths up to at least 100 MHz as the self-resonant frequency (SRF) is around 1 GHz (a rule of thumb for the safe stable region of a capacitor is around one third of the SRF).

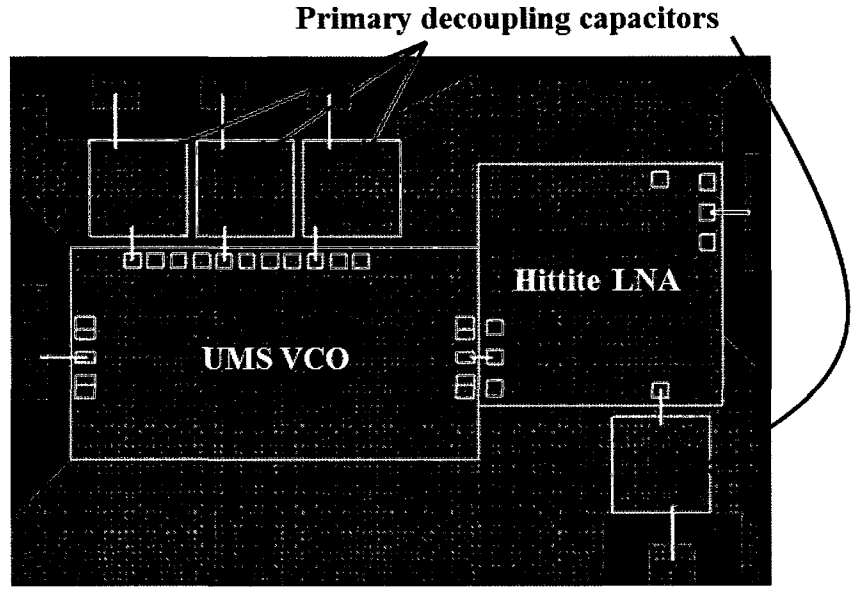


Figure 4.12 Primary decoupling capacitors

4.6.2 Additional Decoupling Capacitors and Stabilizing Resistors

In addition to the primary decoupling capacitors, two more capacitors (10 nF and 1 μF) are added in parallel onto each of the DC supply lines (region B of Figure 4.11). These capacitors have the same function as the primary capacitors but they are higher in capacitance. The reason for adding larger capacitors is to be able to provide low impedance paths for lower frequencies. Although the primary capacitors can provide low impedance paths for noisy signals up to a few hundred MHz, the energy storage is small due to a small capacitance value. Therefore, in order to ensure enough energy storage is provided in case of sudden high current draw, larger capacitance values are used to shunt the lower frequency noisy signals. These additional decoupling capacitors can be placed further from the MMIC chip as they are targeting only the lower frequencies so minimum separation is not critical.

It should be noted that the additional lower frequency capacitors are surface mount capacitors (Figure 4.11). Although these 0201 surface mount capacitors are bigger than the single layer capacitors, they are cheaper in price and also easier to add. Since they are surface mount capacitors, no pre-arranged ground spaces are required for them

as are needed for the single layer capacitors. Because of this advantage, it is also possible to add a third decoupling capacitor, aimed at lower frequencies, if necessary. However, this advantage builds on the fact that the spacing is available on the DC lines and the nearby ground plane.

The number 0201 is for denoting the standardized size of the surface mount technology (SMT) component where "02" means 20 mils in length and "01" means 10 mils in width. These components can be capacitors or resistors and can also have bigger sizes such as 0402 or 0603. In the biasing circuit (Figure 4.11), the extra rectangular box enclosing the two surface mount squares is for defining the footprint of the 0201 component. This footprint is important to ensure enough spacing is kept around the component in case of solder leakage (the details of the SMT footprint can be found in [44]).

In the same figure at region C, the 0201 stabilizing resistors are placed in series on two DC supply lines (Figure 4.11). This is to make sure the DC supply voltages are stable. The reason that a stabilizing resistor is added onto the power supply lines of the Hittite LNA (Vdd) but not to the UMS VCO (V- and V+) is because stability is much more critical to amplifiers than oscillators. The added resistance will make sure the amplifier is stabilized (also discussed in the previous chapter). On the other hand, a stabilizing resistor is also added onto the VT input of the UMS VCO. This is to ensure the voltage can be tuned more accurately; if the voltage is unstable, tuning would become difficult.

4.6.3 DC Biasing Techniques and Component Placements

For lower resistance and better power transfer, the DC supply lines should be made wider. Since the 0201 decoupling capacitors restricts the spacing between the DC lines and the ground wherever the components are placed, the width of the lines is selected to be the same as the width of the 0201 surface mount square (region D of Figure 4.11). Although line widths can be made wider for places without any nearby components, it is not done so (except where the DC connector pins are located) for two reasons. The first reason is because of simplicity. If the line width is changed in between components, the

surrounding ground would need to follow the same transition which may take up more area and pose more complexity. The second reason is because of the advantage of free placement. If the line widths are made wider in some areas and narrower in another, the components cannot be placed anywhere along the DC line but rather only in restricted areas where the component fits. This would make implementation much more difficult and time consuming, which is undesirable if a third or even a fourth decoupling capacitor is needed. As for the wider DC lines where the DC connector pins are located (region E of Figure 4.11), they are required to accommodate the wider pin widths. A tapered microtrip is also added in between the line width transition to minimize loss from discontinuity.

In terms of component positioning, there is no fixed restriction on the spacing between each component on the biasing circuit as long as they do not overlap. However, it is preferred to have the separation as large as possible to prevent the capacitors from resonating. Based on the knowledge from previous layout designs using 0201 components, a good separation is about the length of a 0201 footprint; hence, this separation is adapted into the biasing circuit design (Figure 4.11).

Similarly, the DC tracks are also separated as far as possible to prevent resonance as well as providing larger nearly ground planes. Since the ground of this circuit is made available to the top side of the Duroid card through vias (region F on Figure 4.11), it is important to make sure that enough vias are located in each ground plane block to ensure good grounding. This is why a bigger separation is preferred.

4.7 Output Launcher

In order to test the performance of the LO, an output launcher is required to provide isolation and shielding of the LO circuit from the output connector and external coaxial cable. A microstrip launcher should be sufficient in this case to provide good shielding from the output connector noise. The most convenient choice would be to absorb it into the RT/Duroid 5880 substrate.

Since the output of the buffer amplifier (Hittite LNA) is matched to 50 Ω, the microstrip launcher is designed to have characteristic impedance, Z_o, of 50 Ω for best

matching and thus minimizing loss through the transmission line. This is done by using the *LineCalc* function in ADS to provide the corresponding width and length of the microstrip for RT/Duroid 5880 substrate. The width of the microstrip is fixed by Z_o, but the length can be varied to make it longer to provide better isolation as well as to accommodate the output connector pin length. The width of the connector pin is not an issue here since the 50 Ω track is relatively wide.

In the biasing circuit shown in the previous section, Figure 4.11, region G locates the output microstrip launcher while region H shows the glass bead of the output connector. In order to make sure the 50 Ω track does not couple to the nearby grounds, the ground plane on each side of the microstrip is placed far away (1 mm) from the microstrip. The sharp corners of the ground plane are again mitered to minimize losses.

The ADS model and characterization of the microstrip launcher are shown in Figure 4.13 and Figure 4.14, respectively. The RT/Duroid 5880 microstrip launcher is well matched at around 40 GHz (S_{11} around -58 dB) and it poses a very low loss (S_{21} around -0.095 dB). Thus, it is predicted that the RF signal would not be degraded through this launcher.

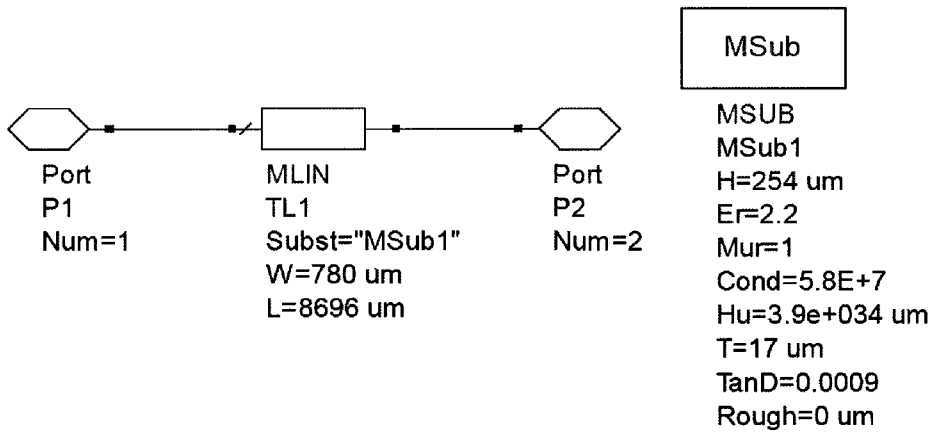


Figure 4.13 ADS model of output RT/Duroid 5880 microstrip launcher

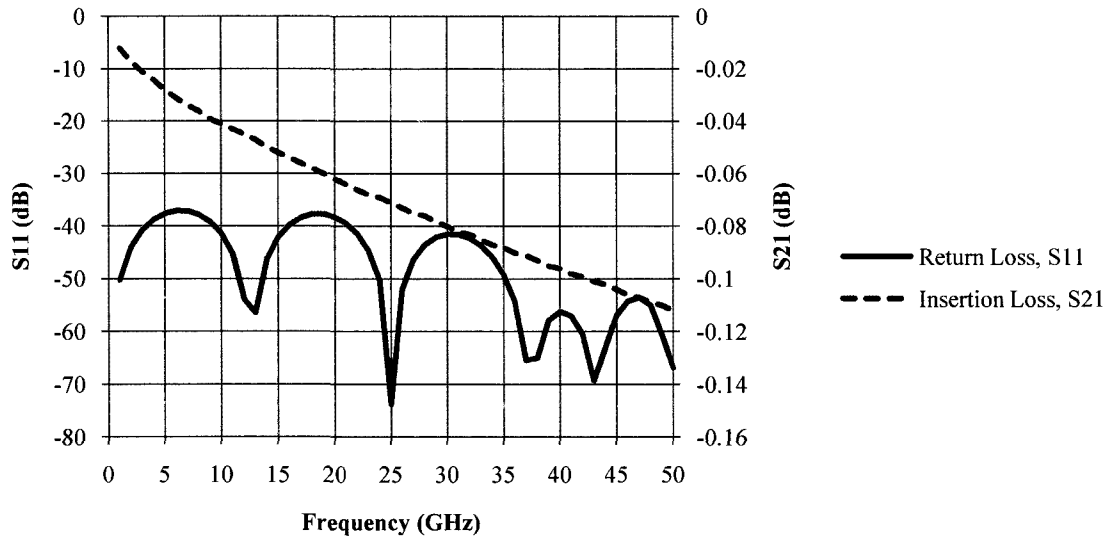


Figure 4.14 S_{11} and S_{21} of the characterized microstrip launcher

4.8 Output V-Connector

The last component to be characterized is the output connector. Although this component is not part of the Duroid PCB design, it is still very important to accurately characterize the loss through this connector as it will affect the overall system losses and the VCO's capability to drive the mixer stage.

The connector used in this work is selected based on its usable bandwidth. The Anritsu V102F V-connector (Figure 4.15) is capable of handling frequencies up to 110 GHz and it is also known for its low VSWR (low return loss) [45].

Figure 4.15 Anritsu V102F V-connector [45]

According to the outline drawing and specifications in [46] from Anritsu, the typical insertion loss (S_{21}) of the V102 V-connector is 0.7 dB and the typical VSWR is

1.38:1 (S_{11} = -15.9 dB). The insertion loss through the V-connector is much higher when compared to the loss through the launcher; the difference is around 0.6 dB. This loss of around 0.7 dB will be much more significant to the output power performance of the oscillator and should be kept in mind when estimating the output performance in the following section.

4.9 Proposed 40 GHz Oscillator System Performance Simulation

In this subsection, the system simulation of the proposed 40 GHz oscillator will be shown. This will provide an insight to the expected oscillating frequency, phase noise and output power as well as bondwire connection losses. The s-parameter simulation will be shown followed by the HB simulation (both simulated in ADS environment).

4.9.1 S-parameter Simulation for Matching

S-parameter simulation is done to determine the matching condition between the UMS VCO chip and the Hittite LNA. The setup utilizes the s-parameter data from both the hemispherical resonator (obtained from E. Ruscito) and the UMS VCO (Figure 4.16). From the S_{11} data of the Hittite LNA s-parameter file, the input impedance is found to be much closer to 40 Ω than 50 Ω; hence, the setup includes an output termination of 40 Ω.

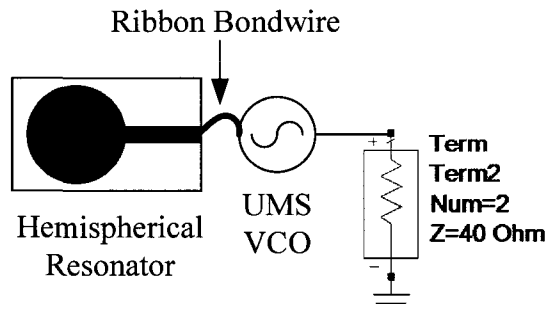


Figure 4.16 S-parameter simulation of UMS VCO using the hemispherical resonator

The output of the UMS VCO turned out to be poorly matched to 40 Ω as the output impedance is found to be fairly high at 205.6 – j14.7 Ω (Figure 4.17). This means that the output of the UMS VCO is poorly matched to the input of the Hittite LNA and thus the loss through the connecting bondwires may be significant. Hence, it is very important to estimate this bondwire loss.

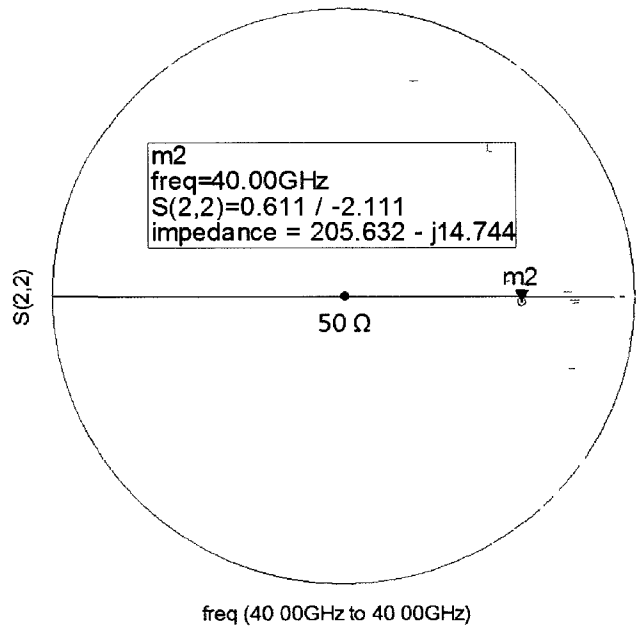


Figure 4.17 S_{22} of the simulated UMS VCO with hemispherical resonator

The setup shown below will help estimate the ribbon bondwire loss and microstrip loss at the output stage (Figure 4.18). There are two bondwire stages in the output stage: one locates between the VCO and the LNA and the other one between the LNA and the output launcher. Since the LNA is added to increase the output power level from the UMS VCO, the total gain including the bondwire and microstrip is estimated together to best predict the losses throughout the entire output stage. It should be noted that the input termination of this s-parameter simulation setup is set at the output impedance of the UMS VCO to best mimic the input condition.

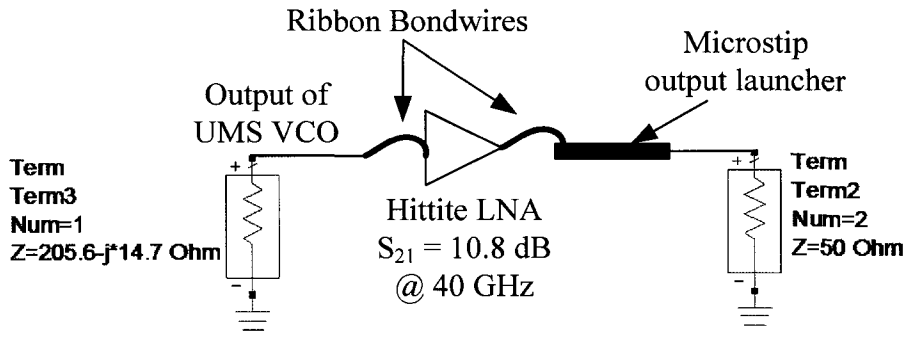


Figure 4.18 S-parameter simulation on the output stage including bondwires

The s-parameter simulation of the output stage shows an S_{21} gain of around 6 dB while the expected amplifier gain from the Hittite LNA is around 10.8 dB at 40 GHz (Figure 4.19). This means that the total losses at the output stage are 4.8 dB. This loss is most likely unavoidable as adding matching circuitry will introduce more losses into the system (e.g. adding a simple microstrip transformer with additional bondwires helps with matching but also yields more bondwire losses; the overall gain ended up to be around 6.7 dB which only improves the gain by 0.7 dB). Nevertheless, the oscillator will still be able to provide enough output power, 17 dBm, with only a gain of 6 dB at the output stage as the target specification only requires 15 dBm of output power.

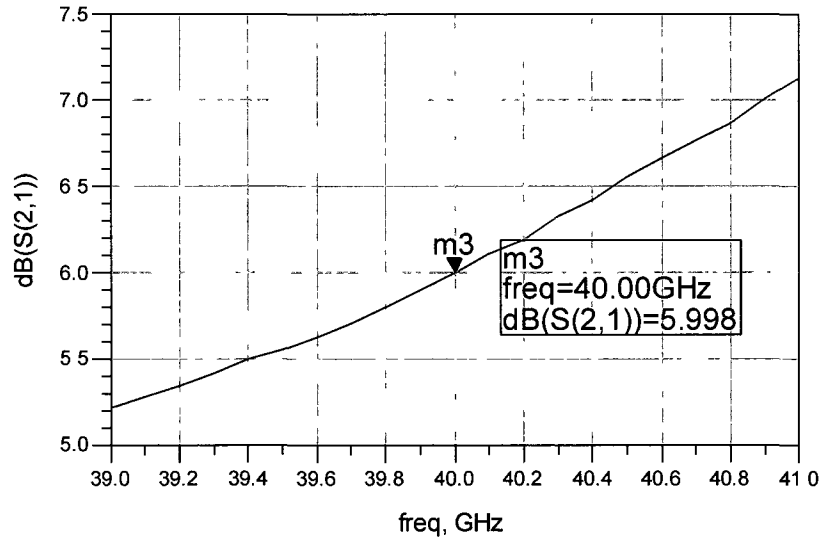


Figure 4.19 S_{21} gain of the output stage around 40 GHz

4.9.2 System Harmonic Balance Simulation for Parametric Study

Harmonic balance simulation is done to determine the phase noise, output power and oscillating frequency in large signal operation. In order to more accurately model the noise and nonlinear effects of the VCO, the simulation was done using large signal design files such as simulating the oscillator design from Chapter 3 in place of the s-parameter file of the UMS CHV2240 VCO. For a more realistic prediction, lossy components such as bondwires are included in the simulation to mimic the possible losses and the Hittite LNA specification is also manually entered into an ADS system amplifier component to include the noise figure and the power at 1 dB gain compression (Figure 4.20).

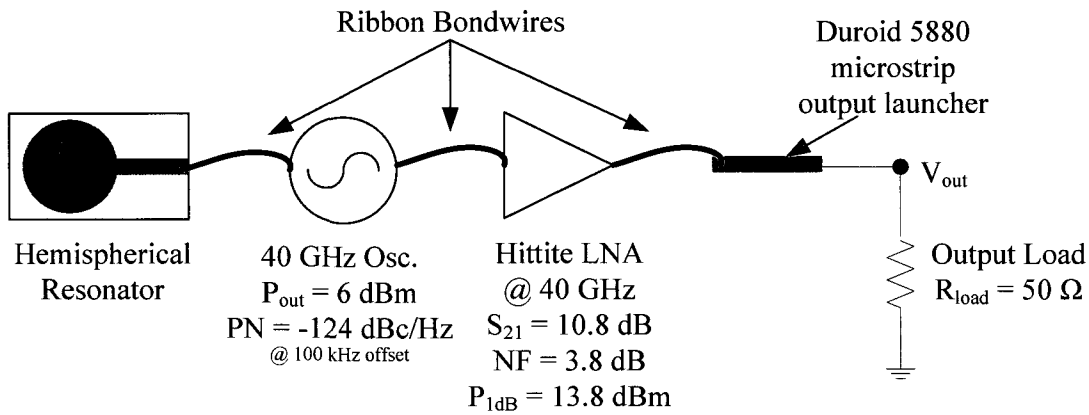


Figure 4.20 40 GHz high Q oscillator system setup including all lossy components

The HB simulation of the oscillator system was done first using the microstrip resonator and then the high Q hemispherical resonator. The simulation using the hemispherical resonator showed promising results meeting the target expectation while the microstrip resonator results did not. The resulting phase noise, output power and oscillating frequency will be discussed and summarized below.

a. Phase Noise

The phase noise of the entire 40 GHz oscillator system using the high Q package-embedded resonator turned out to be around -115 dBc/Hz at 100 kHz offset while using the microstrip resonator gives only around -103 dBc/Hz at 100 kHz offset (Figure 4.21). This mean that only the phase noise using the hemispherical resonator surpasses the required phase noise of -112 dBc/Hz for the target 40 GHz oscillator design for E-band applications. The phase noise is again obtained using the superposition technique discussed in Chapter 3.

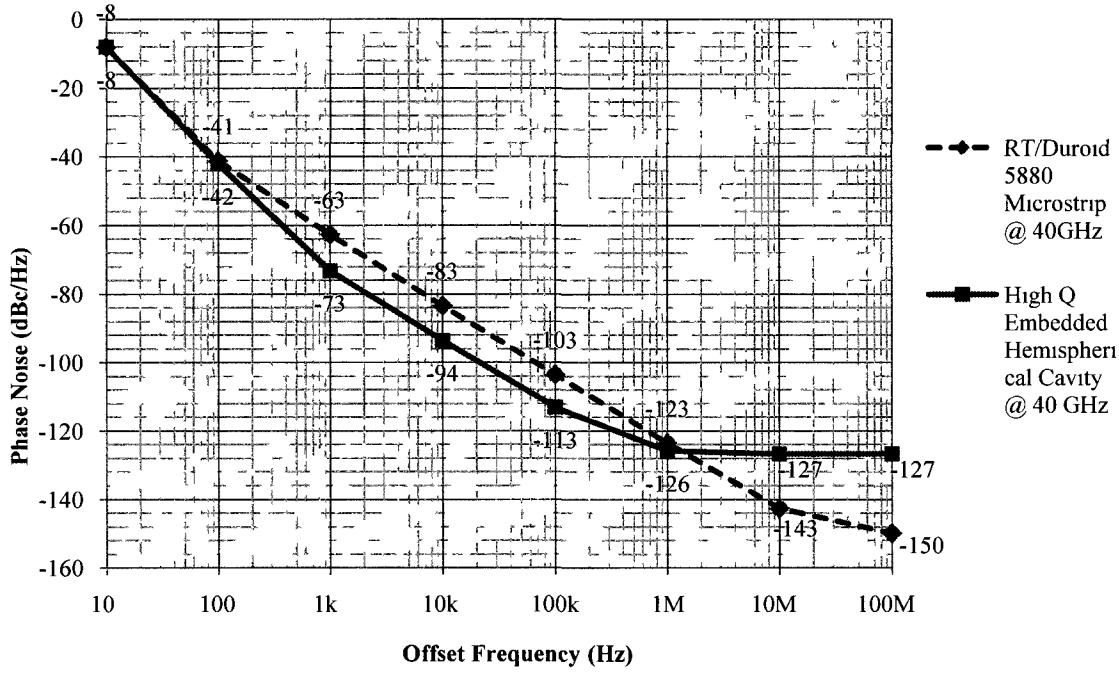


Figure 4.21 SSB phase noise of the designed 40 GHz oscillator system

b. Output Power

The simulated output power is less useful to estimate the system output power as the designed VCO from Chapter 3 provides an output power of 4 dBm when using the hemispherical resonator, which is 5 dB lower than the output power of the UMS VCO, 9 dBm (Figure 4.22). This makes it harder to predict the real system output power when the UMS VCO is used. However, if the output power of the VCO is assumed to be 9 dBm,

meaning adding 5 dB to each stage of the oscillator system but keeping in mind that the Hittite LNA has a saturated power of 16 dBm, an output power of 12 dBm can be predicted with the use of UMS VCO. This turned out to be less than the target specification of output power, 15 dBm.

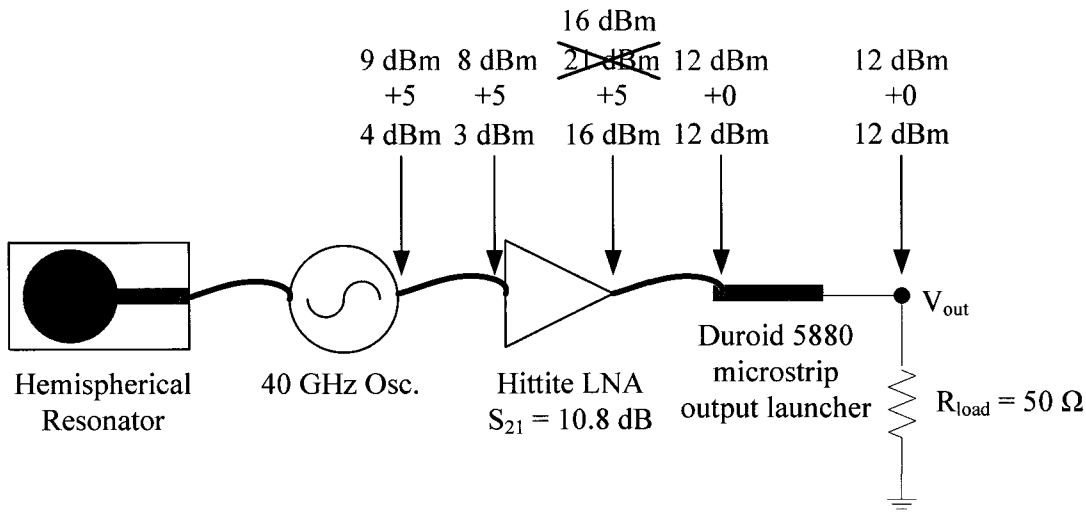


Figure 4.22 Output power at each stage in the oscillator system

The same analysis is applied to the oscillator using the microstrip resonator which yields an output power of 11 dBm.

c. Oscillating Frequency

On the other hand, the oscillating signal (using the hemispherical resonator) at 40.43 GHz (second harmonic) is quite clean as the odd numbered harmonics are quite low (Figure 4.23 orange bars). Even at the highest unwanted harmonic, the fourth harmonic, power is 18 dB below the wanted signal. Hence, harmonic noises are less of a concern when the hemispherical resonator is used. However, it is not the case when the microstrip resonator is used. The third harmonic power level is very high and can cause significant distortion to the RF signal.

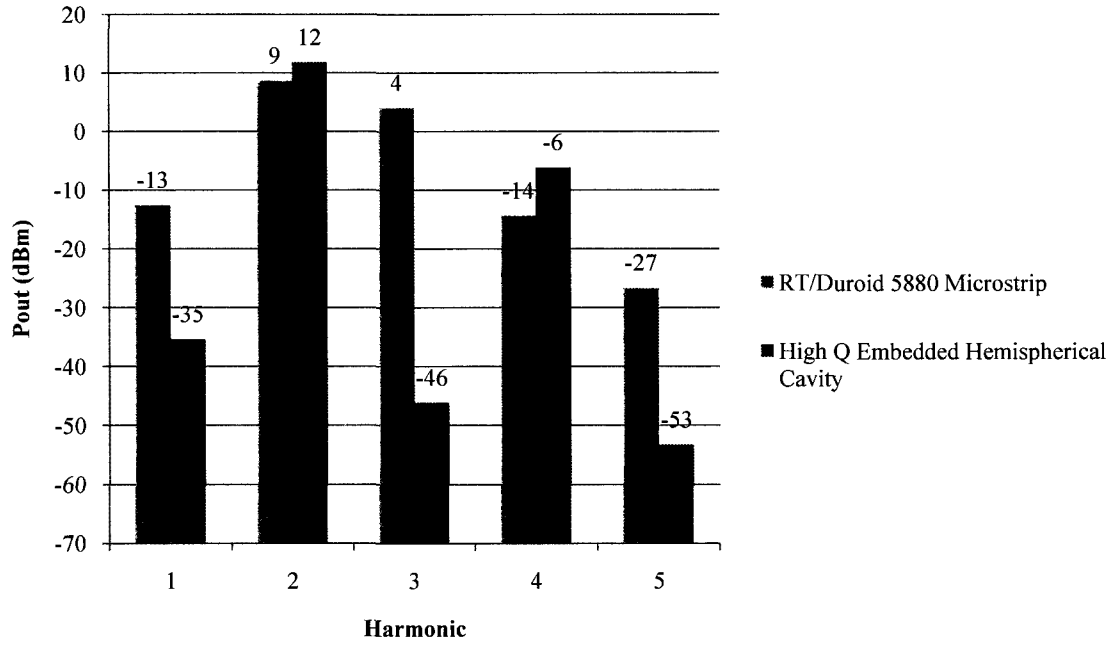


Figure 4.23 P_{out} of the designed 40 GHz oscillator system

Nevertheless, the oscillating frequency at the second harmonic is close to the desired 40 GHz for both the oscillator system using the hemispherical resonator and using the microstrip resonator.

Table 4-4 Oscillating frequency using two different types of resonator

	Oscillating Frequency (GHz)
RT/Duroid 5880 Microstrip Resonator	42.60
High Q Embedded Hemipherical Cavity Resonator	40.43

4.10 Summary

Summarizing the above system simulation results, it can be concluded that the target phase noise can be met with the proposed system (Table 4-5) while the output power is off by 3 dB. Although the predicted for phase noise meets the target specification, the margin room for fabrication error is not high, only around 1 dB. Hence, the fabrication

step becomes much more critical. However, uncertainties due to fabrication can usually be overcome or minimized when multiple copies of the same PCB circuit are available. This is exactly the advantage of choosing Duroid PCBs as its turnaround time is the quickest.

Table 4-5 Summary of the predicted and the target values of the oscillator system performance parameters for both resonator types

Parameters	Hemispherical Resonator	Microstrip Resonator	Target value
PN $_{@\ 100\ kHz\ offset}$ (dBc/Hz)	-113	-103	-112
P_{out} (dBm)	12	11	15
Oscillating Frequency (GHz)	40.43	42.60	40

Chapter 5

40 GHz Ultra Low Phase Noise LO – Fabrication & Measured Results

This chapter will include the measurement results of the designed 40 GHz oscillator using the package-embedded hemispherical resonator. The result using a microstrip resonator will also be compared. Some fabrication concerns and restrictions as well as the causes for performance degradation will be analyzed. The chapter will conclude with a detailed discussion of the performance of this 40 GHz oscillator system.

5.1 Fabrication Concerns and Restrictions

One of the main concerns of the RT Duroid PCB design was the grounding issue. The orientation of the designed layout was chosen to have the active chips (UMS VCO and Hittite LNA) sitting on top of the RT Duroid 5880 PCB card (Figure 5.1). This is to minimize bondwire length and also to simplify the assembly as compared to having the active chips sitting directly on top of the package wall with cut-out Duroid PCB card (Figure 5.2). Although the simpler method (with the active chips sitting on top of the PCB card) was adapted into the oscillator design, grounding became a concern. The proposed solution was to use as many via holes as possible to ensure the top and the bottom metal layers of the Duroid is connected together, and thus providing good ground for the active chips.

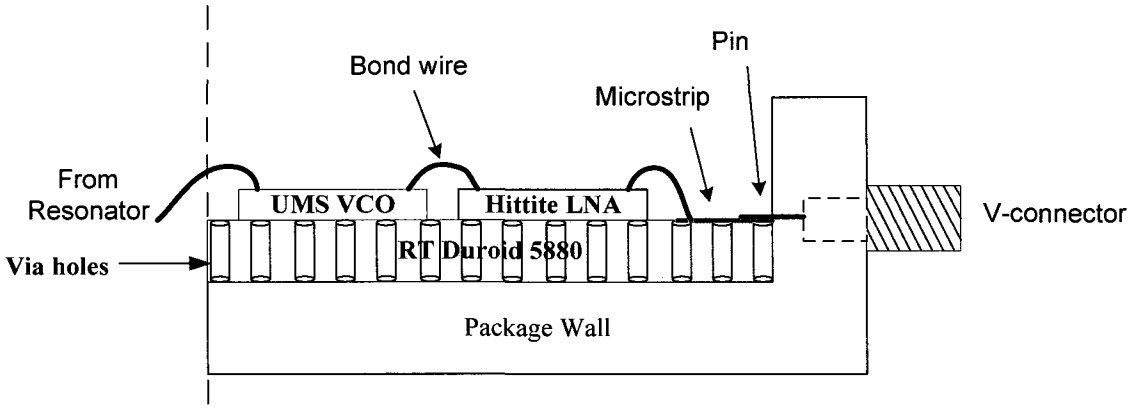


Figure 5.1 RT Duroid PCB design using via holes with active chips on top

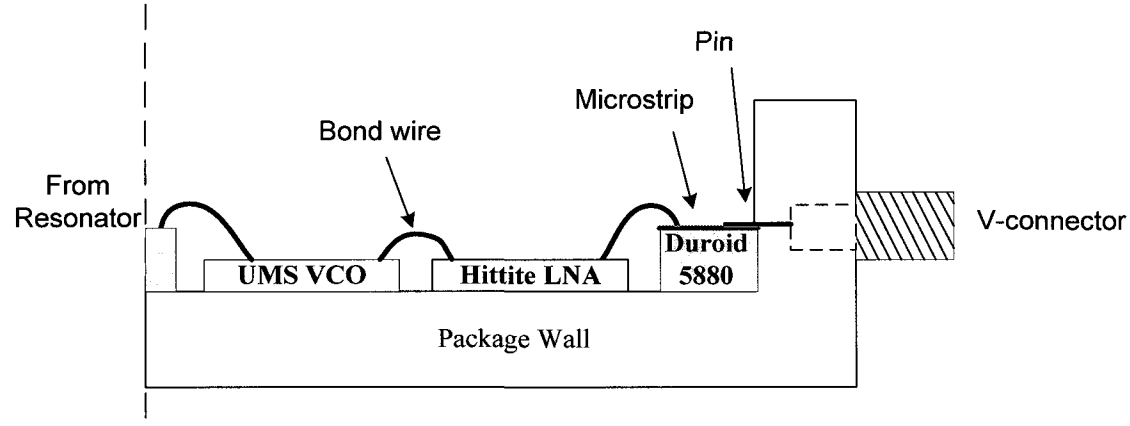


Figure 5.2 Alternate RT Duroid PCB card with cut-out areas for active chips (not pursued in this thesis)

In order to ensure the Duroid card makes good contact with the package wall to provide good grounding, the original proposed method was to use conductive epoxy to glue the PCB to the package wall. This was however soon rejected due to two reasons. The first one is because there are chances of this conductive epoxy leaking into the hemispherical part of the cavity which can greatly affect the quality factor of the resonator. Then the second reason comes in if the conductive epoxy is only applied to the active circuitry part and not the resonator part. If the latter is done, the epoxy on the active circuitry part will carry a certain thickness that will internally make a tiny air gap in between the resonator and the Duroid card on the resonator part of the circuit. This has to be avoided as the tiny air gap can affect the coupling of the hemispherical resonator to

the microstrip feed line. The unevenly distributed epoxy will also bend the Duroid card since Duroid is very flimsy.

Hence, a new solution was proposed without the use of any conductive epoxy. A gold-plated clamp (Figure 5.3) is placed on top of the Duroid card (Figure 5.4) which goes inside the jig packaging (Figure 5.3). This clamp only sits on top of the Duroid on the side of the hemispherical resonator to ensure the Duroid card tightly seals the hemispherical cavity (Figure 5.5). Four screws were used to make sure the clamp pressures the Duroid card onto the package wall. Another two screws are added onto the active circuitry side also to make sure the Duroid card sits flatly on top of the package wall and making good contact.

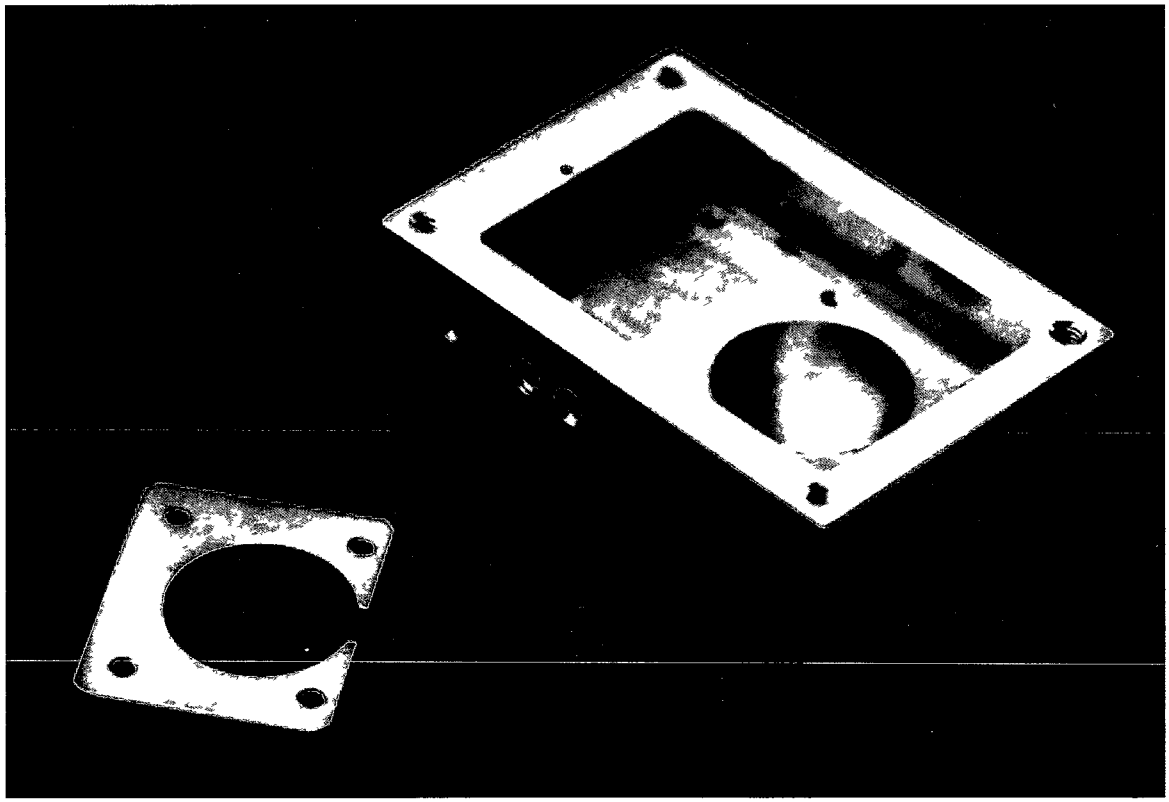


Figure 5.3 A picture of the gold-plated clamp and the jig packaging

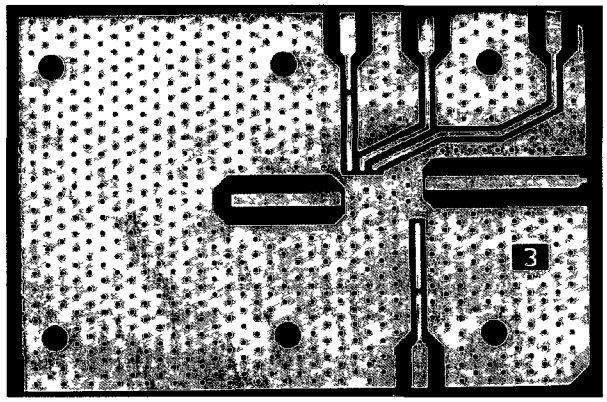


Figure 5.4 A picture of the gold-plated RT/Duroid 5880 card without component assembly

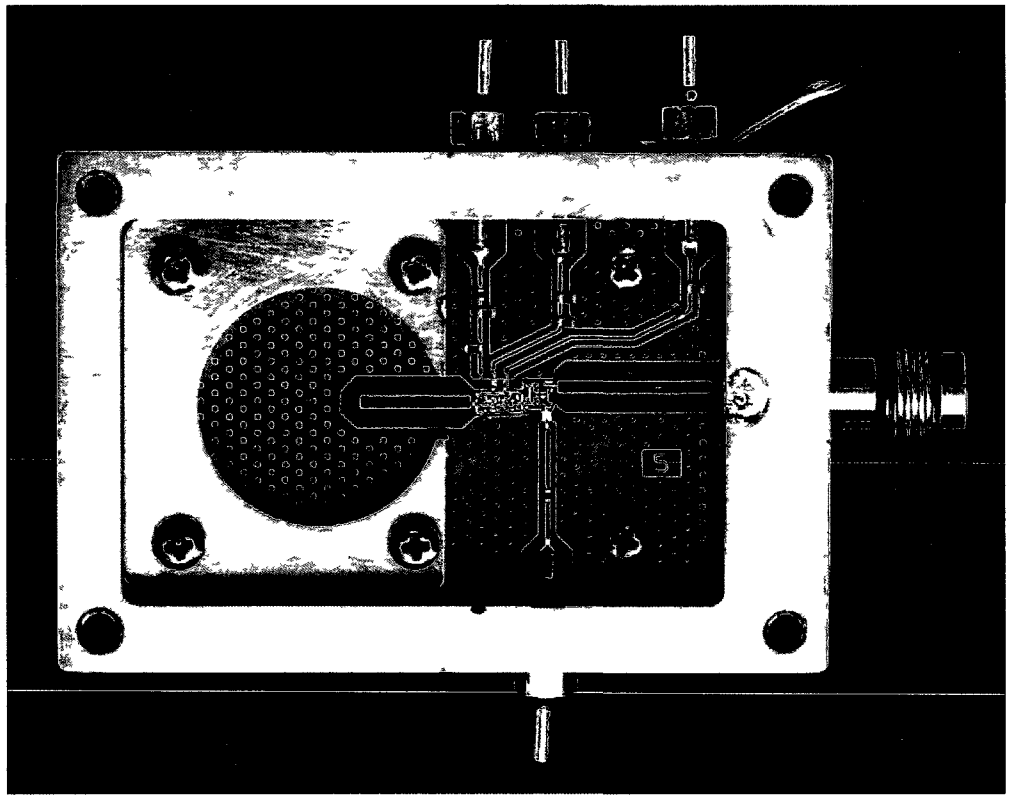


Figure 5.5 A picture of the complete 40 GHz oscillator system with all components assembled

Once the Duroid card is inserted into the packaging, there are some issues that need to be considered between the interface of the Duroid card and the packaging wall. The most critical concern is the alignment of the resonator aperture with the

package-embedded hemispherical resonator. The chosen alignment point is the output v-connector pin-hole (Figure 5.6). This is because the alignment at the resonator microstrip feed is very difficult as it is mid-way on the Duroid card. Using this alignment point, the procedure for alignment is as follows: first, the end of the output launcher is aligned with the v-connector pin-hole; then, the clamp and the screws are inserted to hold the card in place. Sometimes the card will need some trimming to be able to centre the card with the pin-hole precisely and this is due to the given manufacturing tolerance of 1 mil (25.4 μm).

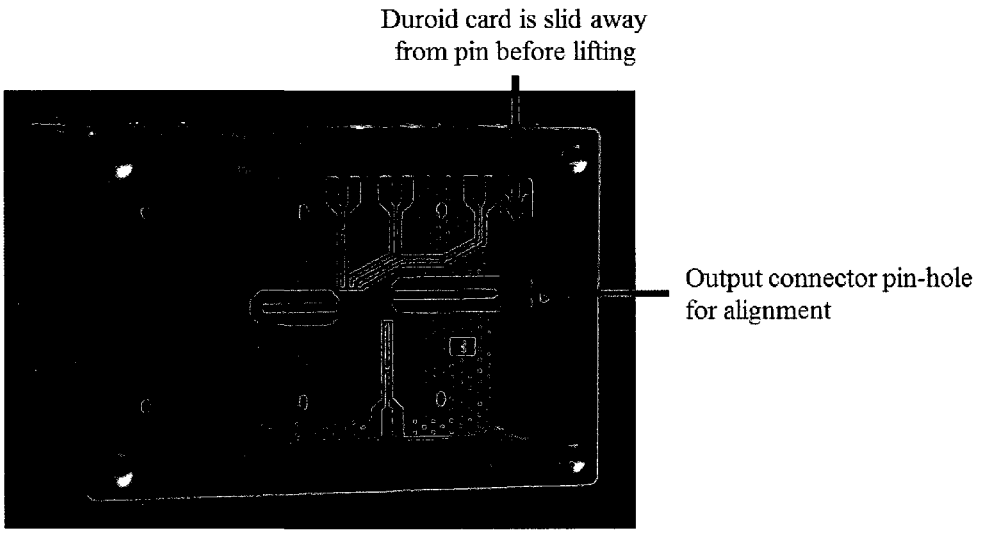


Figure 5.6 A picture showing the slid Duroid card and the output connector pin-hole

During the assembly process, it was found that the v-connector pin-hole's vertical alignment is off by 1.5 mil and thus the pin from the glass-bead of the v-connector ended up sitting directly on top of the Duroid card (in some cases, bending the Duroid card). This makes it very difficult to re-use the same package for different Duroid cards as removing the cards from the package will most likely damage the v-connector (has to be avoided as each v-connector cost around $60). In order to minimize damages to the v-connector, the Duroid cards are trimmed shorter in length on the resonator side so the card can slide away from the v-connector pin before being lifted (Figure 5.6). This method makes it very easy to exchange the different cards for each package and the measurement process becomes much more efficient.

5.2 Measuring Equipment

This section briefly describes the equipment used for measuring high frequency components. The specific manufacturer and model number are also listed.

- **Signal Source Analyzer (SSA)** is used to measure oscillating frequencies (the frequency spectrum), output powers and phase noise. The particular SSA used in this experiment is from Rohde & Schwarz (part number: FSUP) which has a frequency span from 20 Hz up to 50 GHz and has an internal power supply (Figure 5.7).

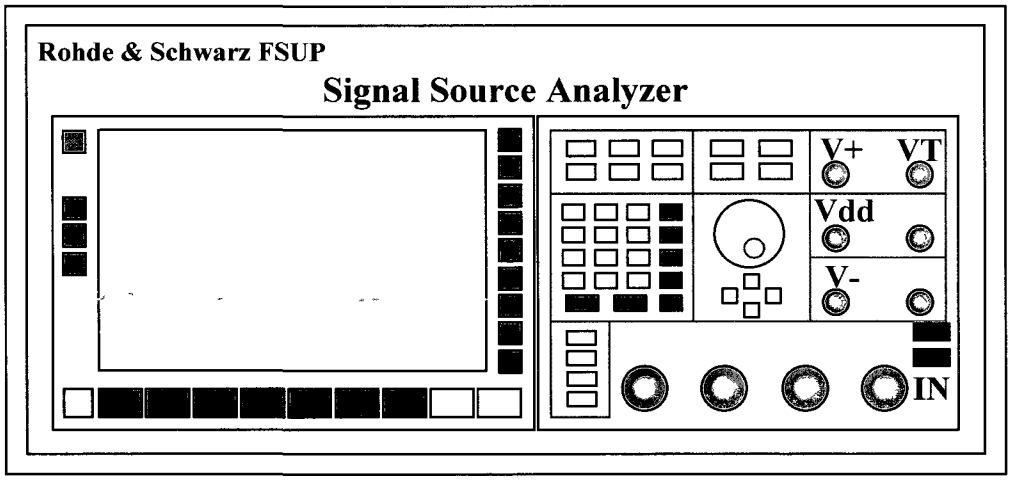


Figure 5.7 Rohde & Schwarz FSUP Signal Source Analyzer

- **Network Analyzer (PNA)** is used to measure s-parameters. The particular PNA used in this experiment is from Agilent (part number: E8361C) which has a frequency span from 10 MHz up to 67 GHz (Figure 5.8).

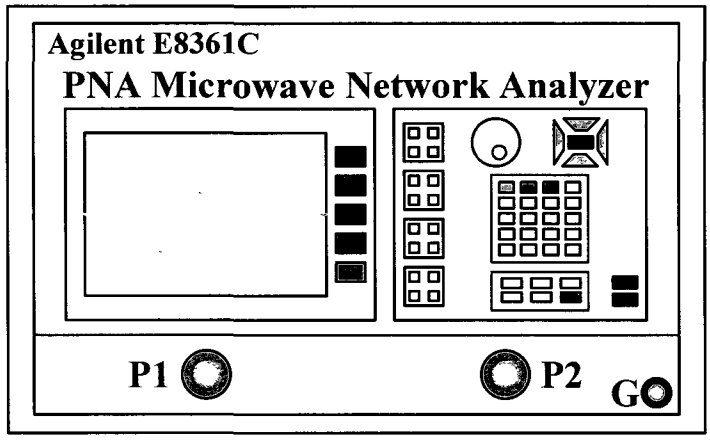


Figure 5.8 Agilent E8361C PNA Microwave Network Analyzer

- **Probing Machine** can include both 50 Ω RF probes (Ground-Signal-Ground; G-S-G) and DC probes (P-P-P-P-P-P-P-P-P) at the same time and is able to provide RF or DC power through the corresponding probes to the device-under-test (DUT). The particular probing machine used in this experiment is a Picoprobe from Karl Suss (Figure 5.9). The RF probes (150 μm to 250 μm) are calibrated using the CS5 SOLT (Short-Open-Load-Through) calibration kit from GGB Industries [47].

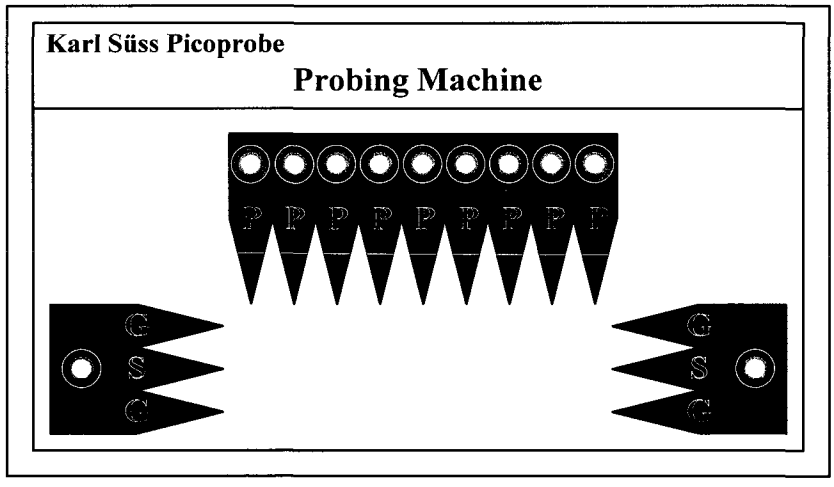


Figure 5.9 Karl Süss Picoprobe Probing Machine

- **DC Power Analyzer** is used to provide DC power to DUT (Figure 5.10).

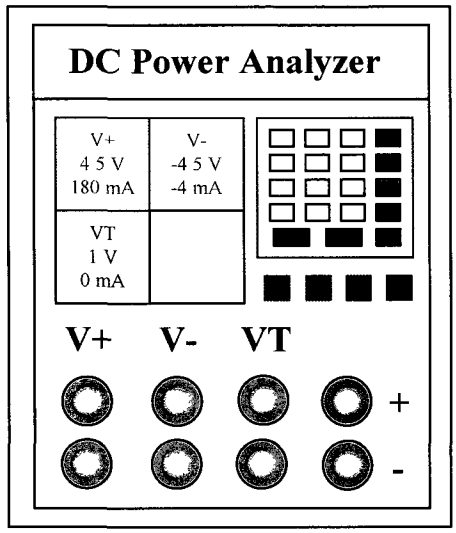


Figure 5.10 DC Power Analyzer for providing DC power

5.3 Final Measurement Results

This section will start with an overview of the different measurements that will be shown and discussed later in the section. The measured results will be compared to the simulated results from Chapter 4 where appropriate.

5.3.1 Overview of Measurements

There are several components in an oscillator system design that can affect the overall performance and thus it is important to verify that each component is behaving as predicted. The different measurements undertaken are for the hemispherical resonator, the UMS VCO, the hemispherical resonator with the UMS VCO, the Hittite LNA and for the whole system (Figure 5.11). The corresponding equipment used to obtain these specific measurements are tabulated with a short description of the purpose of each test (Table 5-1). The results of each test are either compared with the simulated results or with the manufacturer (mfr.) provided results.

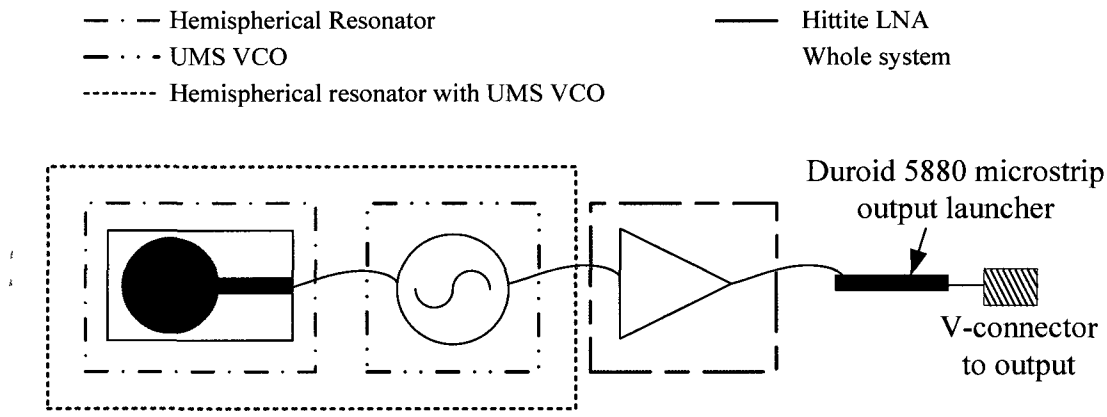


Figure 5.11 Component breakdown of the 40GHz Oscillator System

Table 5-1 Equipment used and measurement purpose for each testing component/module

Component/Module	Equipment Used	Purpose	In Section
Hemispherical Resonator	Obtained from E. Ruscito [4]		5.3.2
UMS VCO	PNA + Probing Machine	Compare s-parameter performance (measured vs. mfr. provided) and locate oscillating point	5.3.3
Hemispherical Resonator with UMS VCO	SSA with DUT in jig packaging	Evaluate oscillation performance and power level	5.3.4
Hittite LNA	PNA + Probing Machine	Compare s-parameter performance (measured vs. mfr. provided)	5.3.5
Whole system	SSA with DUT in jig packaging	Evaluate final Pout, PN and oscillation frequency performance (measured vs. simulated)	5.3.6

5.3.2 Hemispherical Resonator Measurement

As previously mentioned the design of the hemispherical resonator was done by another colleague; therefore, this sub-section will only show the final and most suitable result of the package-embedded hemispherical resonator that has a measured unloaded Q of 2200 (more details on the full analysis of the hemispherical resonator can be found in [4]).

The measured s-parameter result of the hemispherical resonator shows a strong resonance with an input return loss, S_{11}, of -4 dB at 19.96 GHz. Some smaller resonances also occurred at higher frequencies, 28.12 GHz, 32.69 GHz and 36.14 GHz, with magnitudes no greater than -2.4 dB (Figure 5.12).

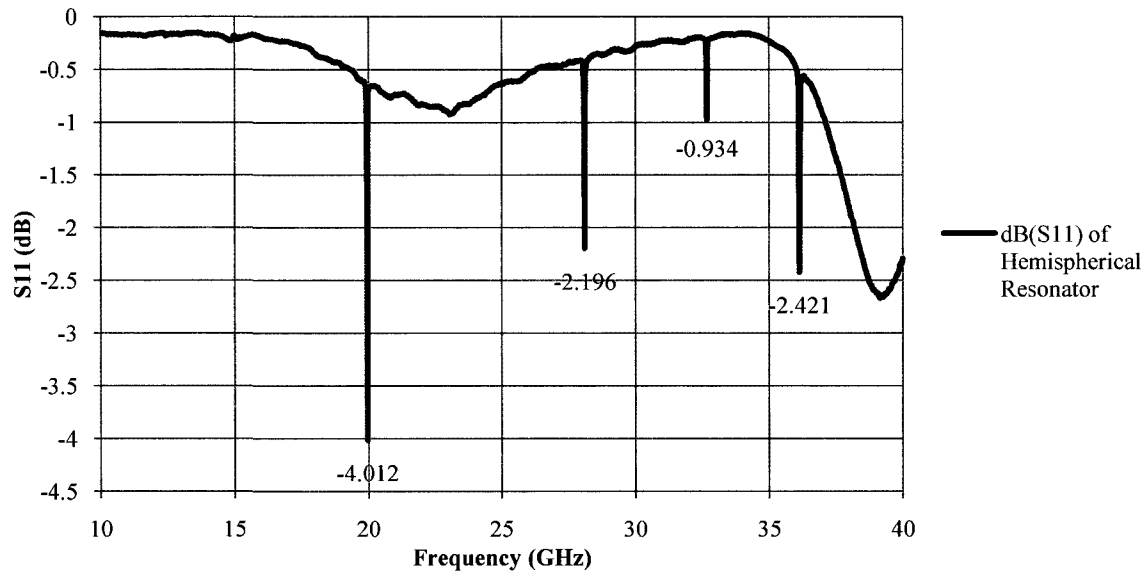


Figure 5.12 S_{11} of the package-embedded hemispherical resonator

The hemispherical resonator's real and imaginary input impedances (Z_{in}) are also shown as it is very important from the VCO's point of view (Figure 5.13). Apart from the high Z_{in} at around 17 GHz and 37 GHz, the input impedance of the resonator remains fairly constant at close to zero from 10 GHz to 40 GHz. The result shown here will be discussed in the next section after the input impedance of the UMS VCO is shown. The results of the two impedances will provide an estimate to the oscillation points.

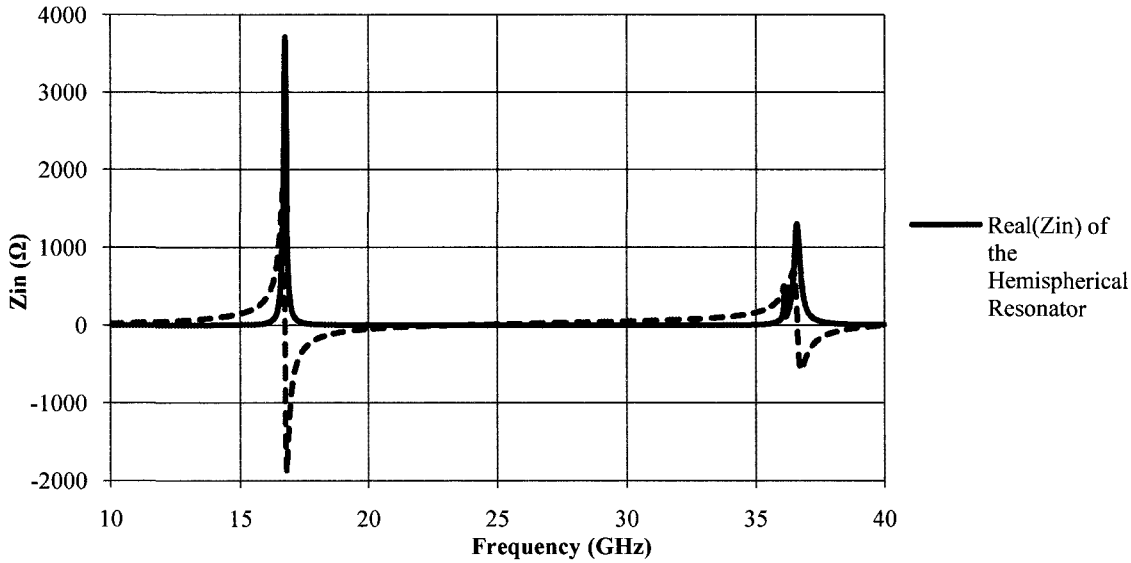


Figure 5.13 Z_{in} of the package-embedded hemispherical resonator

5.3.3 UMS VCO Measurement

As outlined in Section 5.3.1, the UMS VCO (part number: CHV2240) is measured alone before placing it into the system design. This is to compare the s-parameter data obtained from the UMS VCO chip with the manufacturer provided data and to verify the tuning frequency range. There are also two more reasons for doing this test. One is to obtain more data points using finer tuning voltages (as the mfr. provided data is only limited to VT = 0 V and VT = 2 V) in order to more easily locate the oscillating points when compared to the impedance of the hemispherical resonator. The other reason for the test is to confirm the isolation between the input and the output of the VCO chip to ensure the oscillation point is not affected by the output load.

The UMS VCO chip is tested using the PNA with connections to the probing machine and the DC power analyzer (Figure 5.14). The DC voltages and current consumption behaved normally and the resulting s-parameter data is read from the PNA.

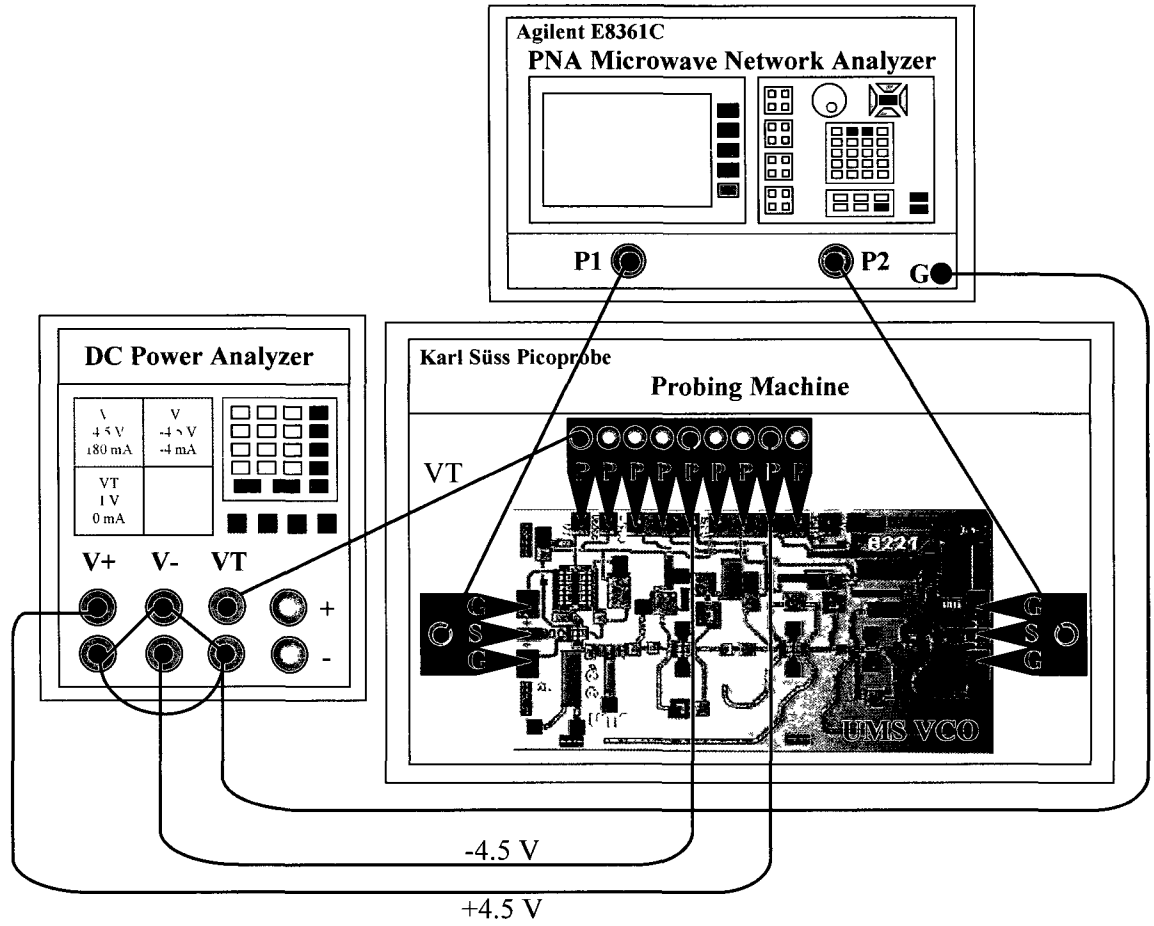


Figure 5.14 Test setup for measuring UMS VCO

The measured s-parameters are shifted in frequency (a few GHz higher) compared to the data provided by the manufacturer (Figure 5.15 and Figure 5.16). This is most likely due to the fact that the RF probe used for the measurement has a 50 Ω termination whereas the manufacturer provided data is obtained when the input is loaded with a COTS resonator. Nevertheless, the plots are comparable at the tuning level. As the tuning voltage increases, the oscillating frequency increases. The measured tuning frequency range is around 2.4 GHz (21.7 GHz to 24.1 GHz) which is 0.6 GHz less than the manufacturer data (3 GHz; shown in Chapter 4).

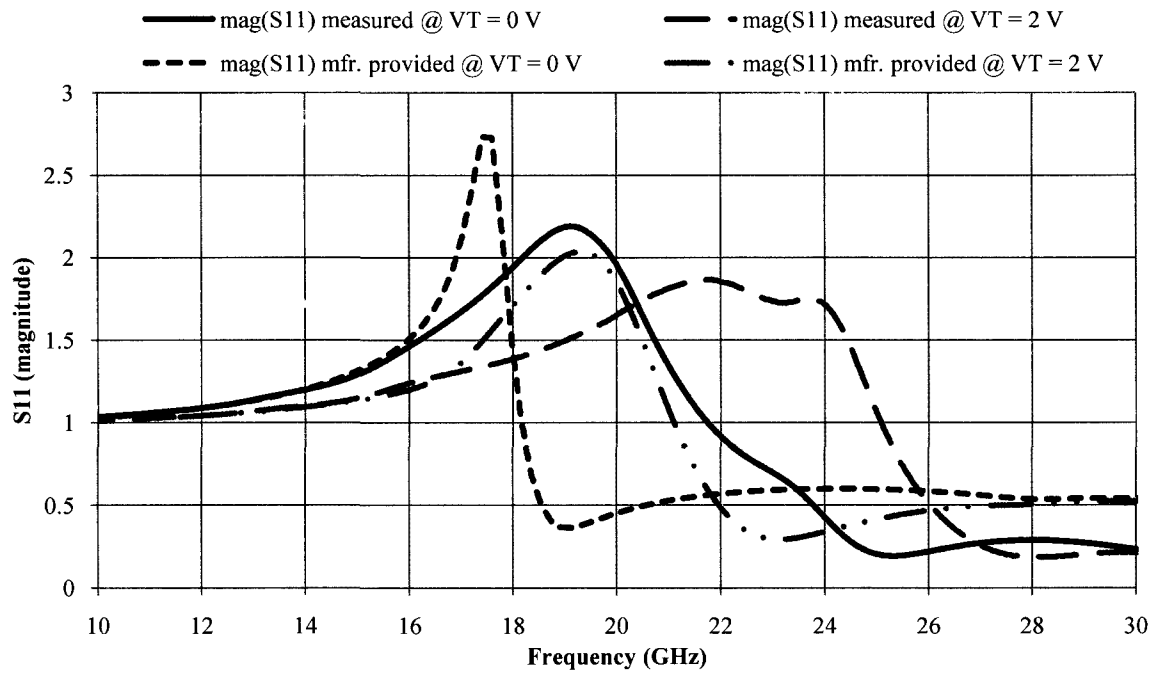


Figure 5.15 Comparison of the magnitude of S_{11} between measured and mfr. provided for the UMS VCO

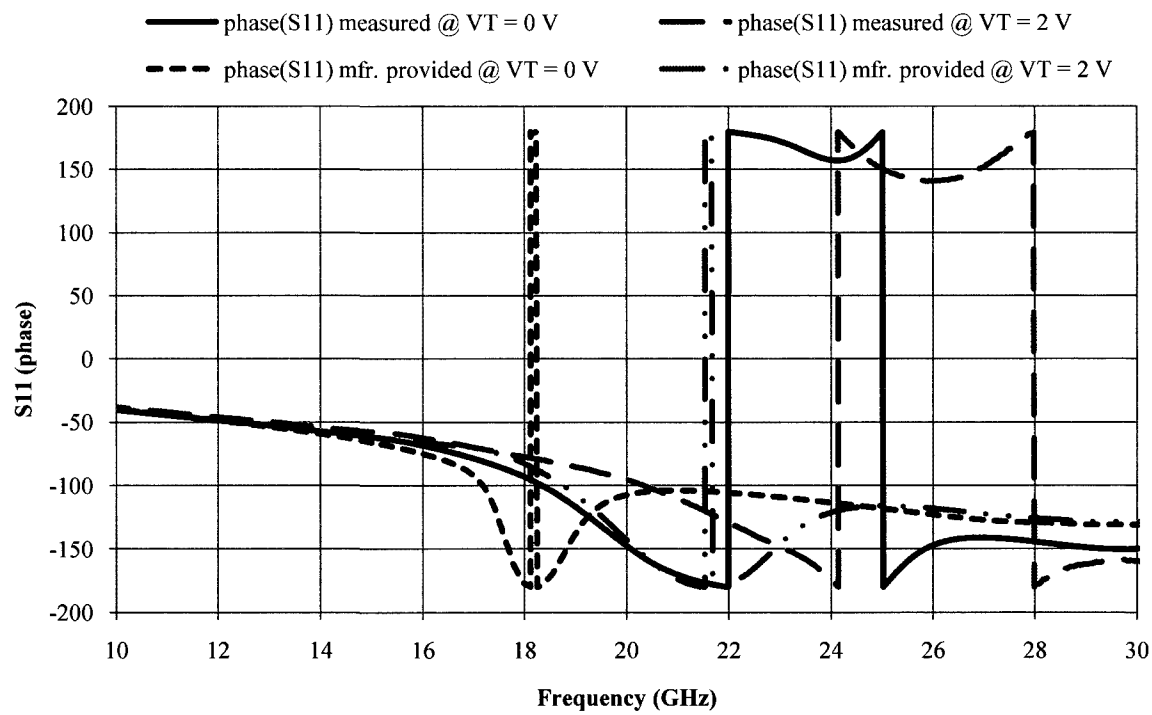


Figure 5.16 Comparison of the phase of S_{11} between measured and mfr. provided for the UMS VCO

In order to see the behaviour of the UMS VCO chip more clearly as the tuning voltage is adjusted, the measurements are taken at each 0.2 V increase. The resulting input impedances (Z_{in}) are compared with the Z_{in} of the hemispherical resonator. If the magnitude of the real part of Z_{in} for the VCO ($|R_{in,VCO}|$) is equal to or greater than (to some degrees; usually around three times) the hemispherical resonator's real part of Z_{in} ($R_{in,Resonator}$), and the imaginary part of Z_{in} (X_{in})of the two components cancel each other, then an oscillating point is located. Ideally, this point should only occur at the designed resonant frequency which is around 22.7 GHz when $|R_{in,VCO}|$ is around two times greater than that of the hemispherical resonator (i.e. at 22.74 GHz, $|R_{in,VCO}| = 5\ \Omega \approx 2 \times R_{in,Resonator}$ where $R_{in,Resonator} = 2.5\ \Omega$; Figure 5.17) and their imaginary part cancels each other (i.e. $X_{in,VCO} = -X_{in,Resonator} = 4\ \Omega$; Figure 5.18). However, seeing from R_{in} for the VCO, the unstable region starts as low as around 8 GHz up to around 25 GHz (Figure 5.17). Due to this extended unstable region, an oscillating point is found around 13.9 GHz when the impedance of the hemispherical resonator becomes very high and coincidentally meeting the oscillation condition (i.e. at 13.94 GHz, $|R_{in,VCO}| = 10.3\ \Omega \approx 5 \times R_{in,Resonator}$ where $R_{in,Resonator} = 2.1\ \Omega$ and $X_{in,VCO} = -X_{in,Resonator} = -90\ \Omega$; Figure 5.17 and Figure 5.18). This phenomenon becomes troublesome as two tones are being fed into the oscillator system. More details on this will be discussed in later sections.

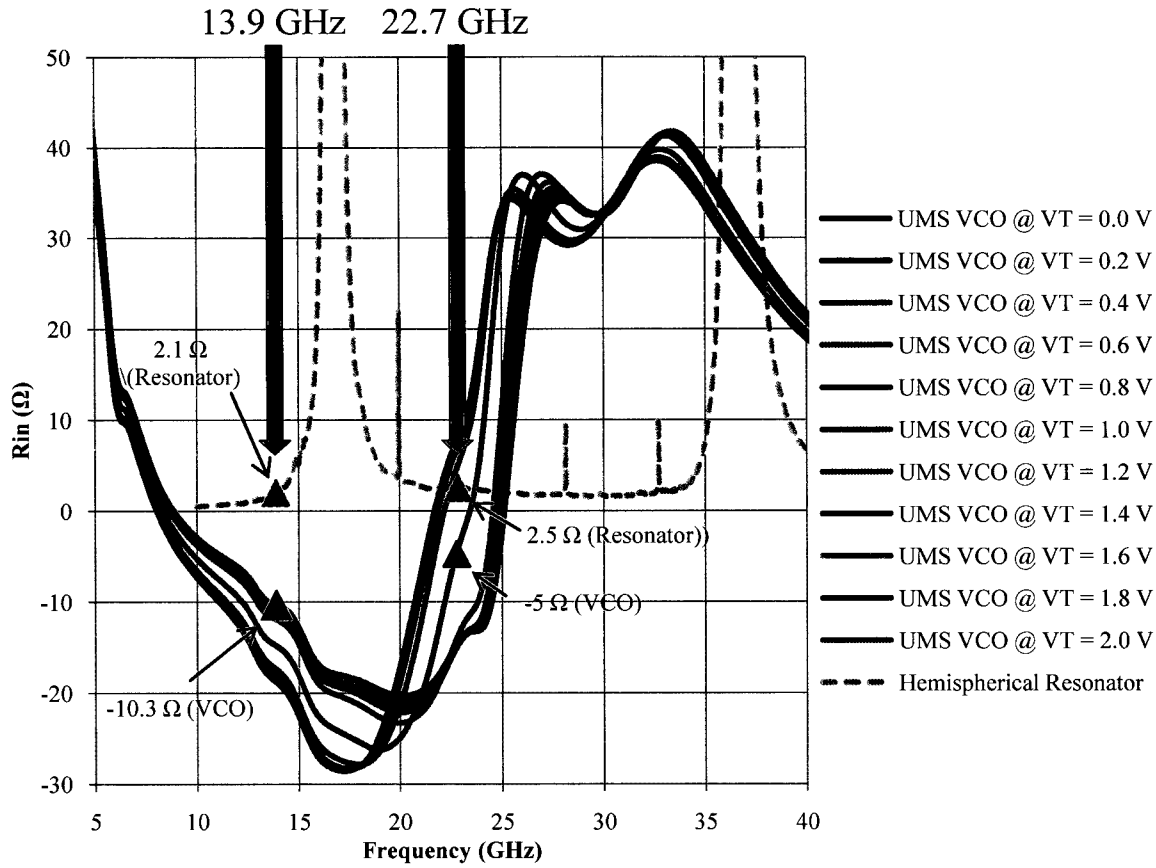


Figure 5.17 Comparison of R_{in} between the UMS VCO with VT varied from 0 V to 2V and the hemispherical resonator

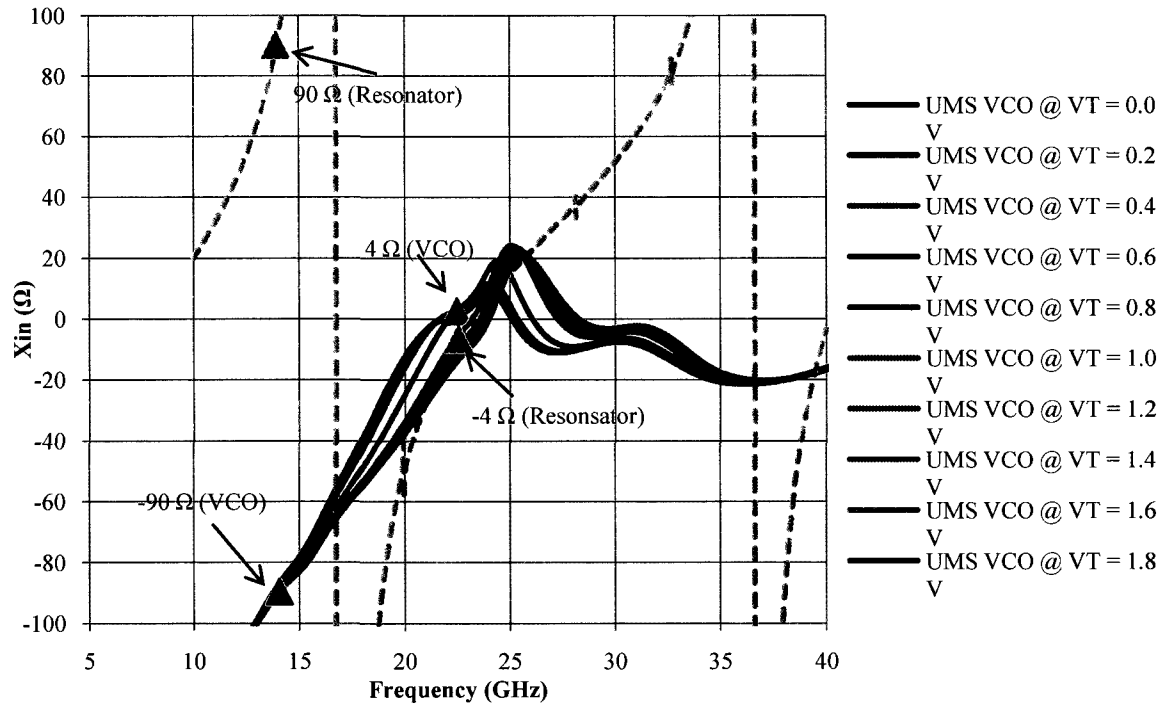


Figure 5.18 Comparison of X_{in} between the UMS VCO with VT varied from 0 V to 2V and the hemispherical resonator

The isolation of the two ports of the UMS VCO chip is tested by taking two measurements with different loads. The first one is taken with a 50 Ω load and the second one with an open circuit. The resulting input return loss (S_{11}) are compared and found to be almost identical (the largest difference is at the peak at 21.66 GHz with a difference of only 0.15 dB between the two curves; Figure 5.19). Since S_{11} remains almost the same with different output loads, this proved that the isolation between the input and the output of the VCO chip is fairly acceptable.

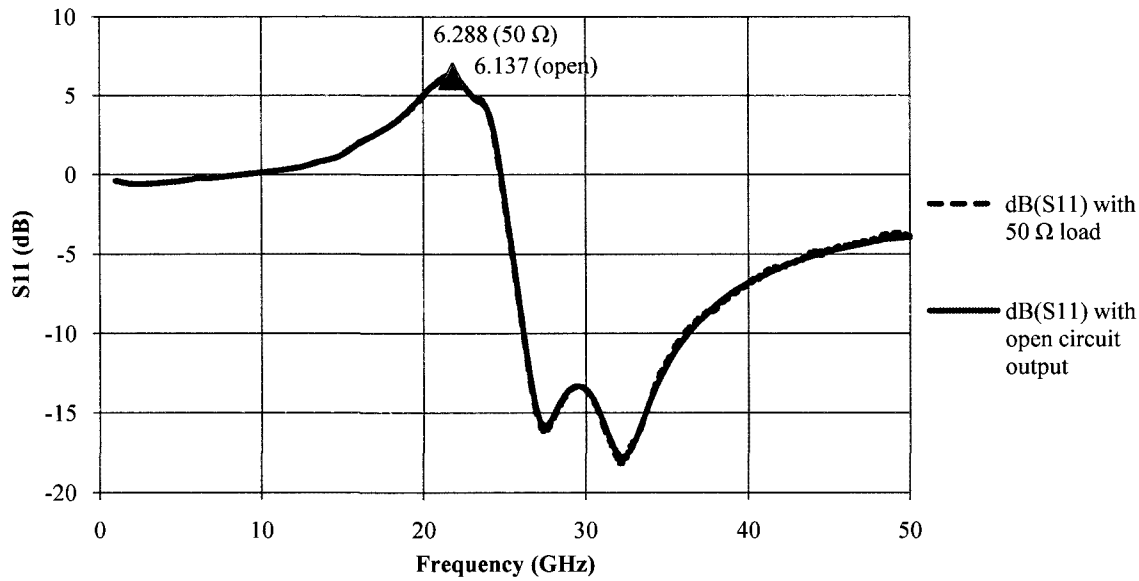


Figure 5.19 Comparison of S_{11} for two different loading conditions for the UMS VCO

5.3.4 Hemispherical Resonator with UMS VCO Measurement

The measurement for the hemispherical resonator with the UMS VCO is mainly used to confirm oscillation as well as to identify the power level without the presence of the buffer amplifier (Hittite LNA). The results are tested using a simple Duroid 5880 microstrip resonator as it is much easier to adjust the length of the microstrip in case the oscillating frequency is shifted.

The hemispherical resonator with the UMS VCO module is tested using the SSA with the Duroid card sitting in the designed jig packaging (the card does not have to sit in the jig packaging but it makes it easier to do the test as all the Duroid cards are designed the same way). The test setup for this module is much simpler than using the PNA with the probing machine as only one equipment is needed since the SSA has its internal power supply (Figure 5.20). The DC voltages and currents consumption behaved normally and the measured results are read from the SSA.

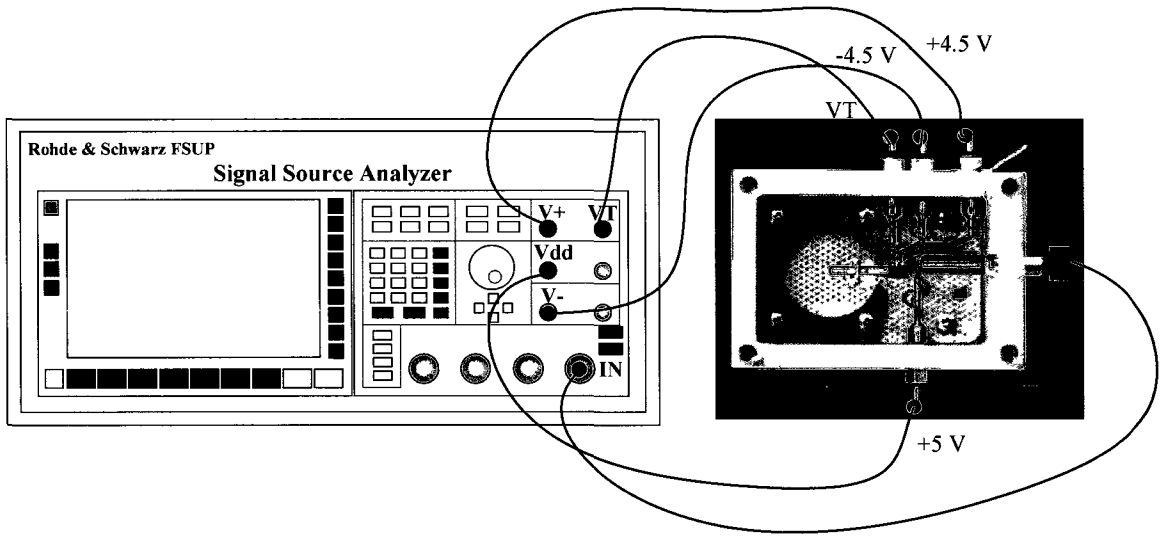


Figure 5.20 Test setup for measuring hemispherical resonator with UMS VCO

This test is used to check the oscillation frequency of the designed module to see if a resonance around 40 GHz can be detected. The oscillation was indeed found to be around 42.5 GHz with a power level of -5.87 dBm (Figure 5.21). The first harmonic is also present on the frequency spectrum at around 21.2 GHz with -32.11 dBm of power.

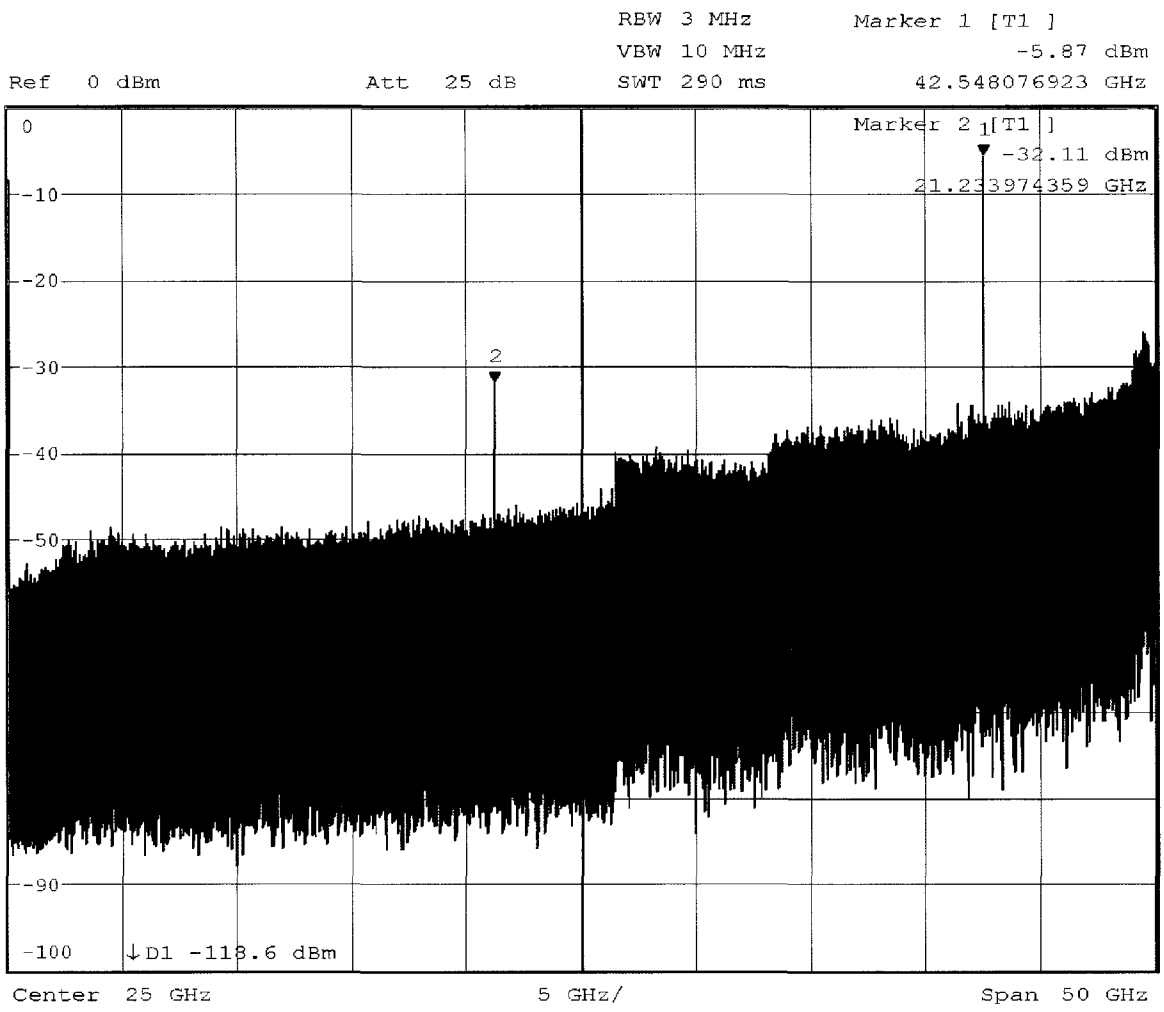


Figure 5.21 Frequency spectrum of the 42.5 GHz oscillator using the microstrip resonator without the presence of the Hittite buffer amplifier

5.3.5 Hittite LNA Buffer Amplifier Measurement

The measurement for the Hittite LNA (part number: HMC-ALH445) is to confirm the s-parameter data of the chip with the manufacturer provided data as well as to measure the saturated power of the amplifier as it was not provided.

The s-parameter data of the Hittite LNA is again measured using the PNA and the probing station (Figure 5.22). The DC voltages and currents consumption behaved normally and the s-parameter is again read off the PNA network analyzer.

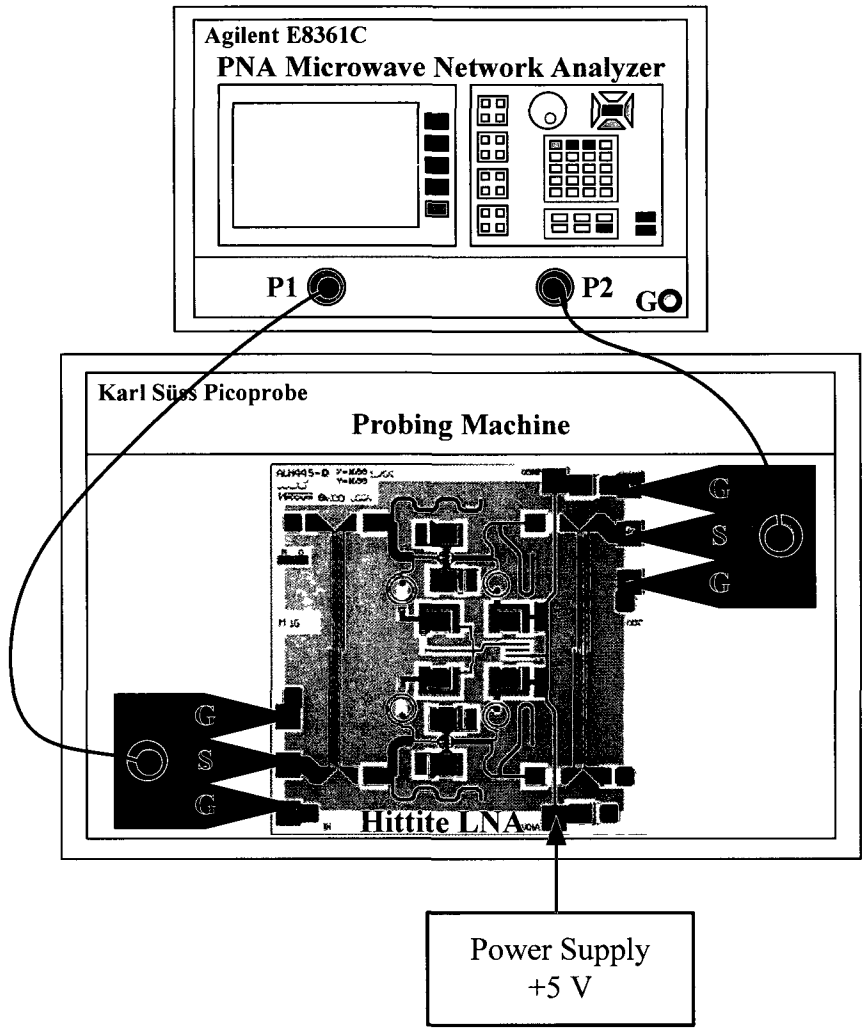


Figure 5.22 Test setup for measuring s-parameters of Hittite LNA

The measured s-parameter data did not show any significant difference compared to the manufacturer provided data (Figure 5.23). The S_{21} gain at 40 GHz is around 10.8 dB while the return losses, S_{11} and S_{22}, and the insertion loss, S_{12}, are kept fairly low at around -20 dB.

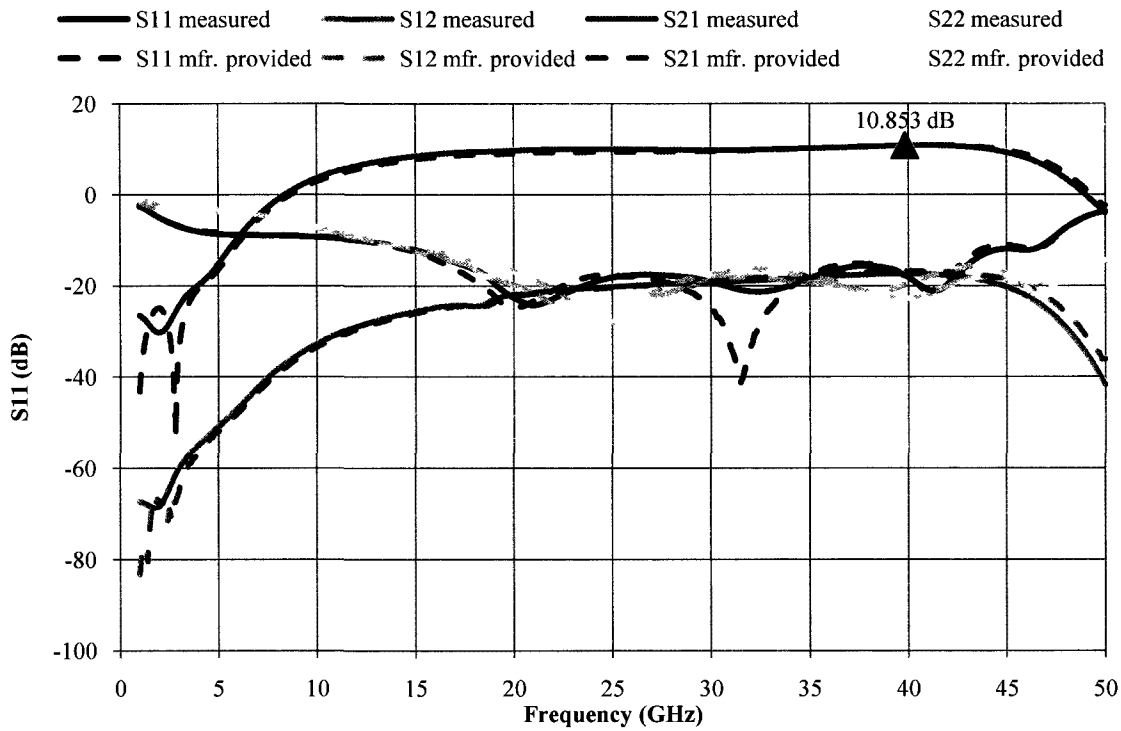


Figure 5.23 Comparison of s-parameters between measured and mfr. provided for the Hittite LNA

In order to measure the saturated power of the amplifier, an input power has to be supplied to the input of the Hittite LNA. This is done by connecting a function generator to the input RF probe while the output is connected to a power meter (Figure 5.24). The function generator is set to output a 40 GHz signal with variable power level. The output power level is then read from the power meter while varying the input power on the function generator.

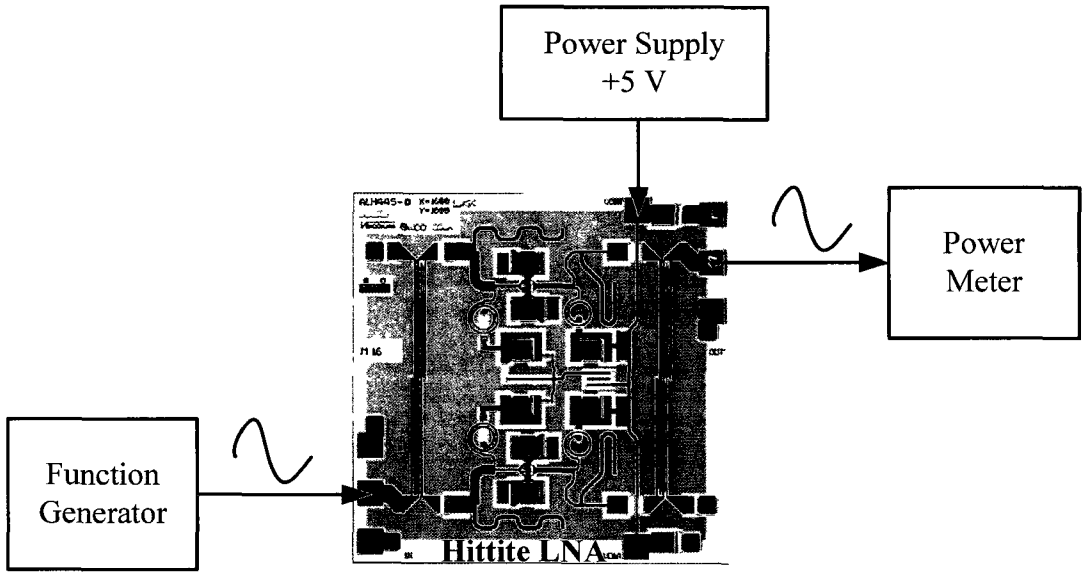


Figure 5.24 Test setup for measuring the output power of Hittite LNA as input signal power increases

The output power of the Hittite LNA reaches the 1-dB compression point (P_{1dB}) at around 13.57 dBm (Figure 5.25) which is fairly close to the manufacturer datasheet value (13.8 dBm). The saturated power is roughly estimated from the graph as the readings cannot be taken with higher input power since the maximum rating has been reached. The estimated saturated power is around 16 dBm.

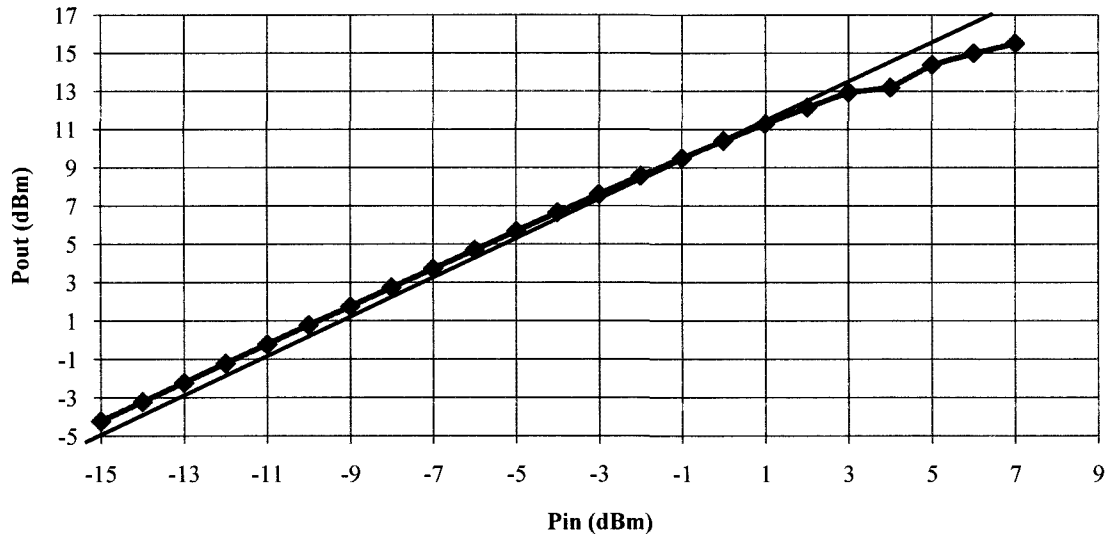


Figure 5.25 Measured output power level the of the Hittite LNA as input power increases

5.3.6 The Complete 40 GHz Oscillator System Measurement

This sub-section will show the most important measurement for the designed 40 GHz oscillator system including the measurements for the phase noise, the output power and the frequency spectrum. The 40 GHz oscillator module is tested using the SSA with the Duroid card sitting in the designed jig packaging (Figure 5.26). The DC voltages and currents consumption behaved normally and the results are read from the SSA.

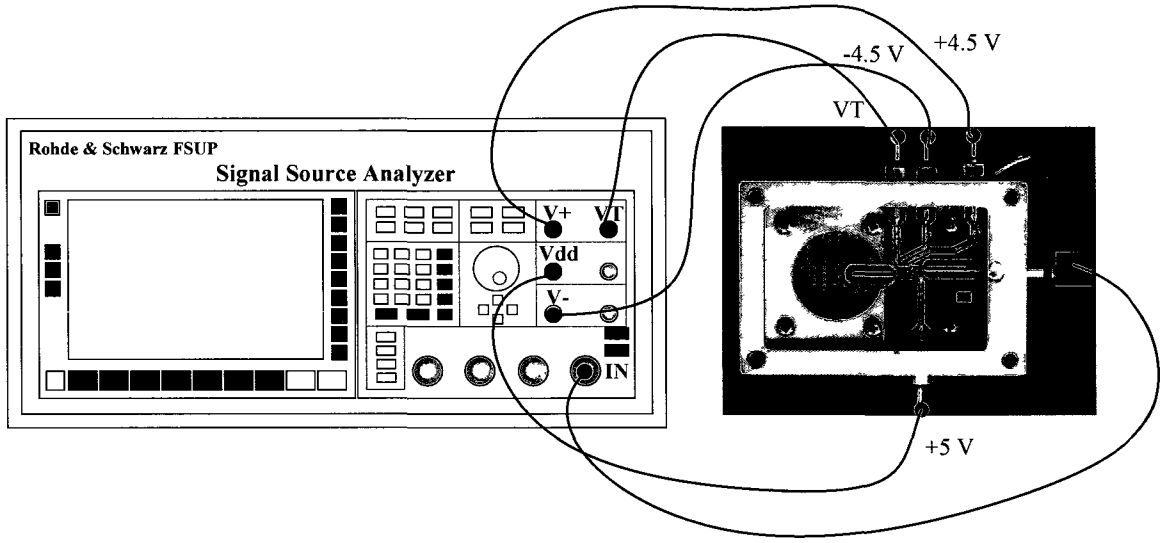


Figure 5.26 Test setup for measuring the complete designed 40 GHz oscillator system

The section will begin with the discussion of the frequency spectrum and the output power followed by the analysis of the phase noise. The results using the hemispherical resonator and the microstrip resonator will both be shown.

a. Oscillating Frequency and Output Power

The main oscillating frequency for the oscillator with the package-embedded resonator is at 44.47 GHz with the first harmonic at 22.2 GHz which is the expected frequency (Figure 5.27). In the impedance comparison discussed earlier in Section 5.3.3, the main oscillating point was found to be around 22.7. Although the oscillating frequency is expected, there is a problem with locking into this state at start-up. A manual "push" is required to cause the oscillator to lock into this state. More details will be discussed the results section, Section 5.4.

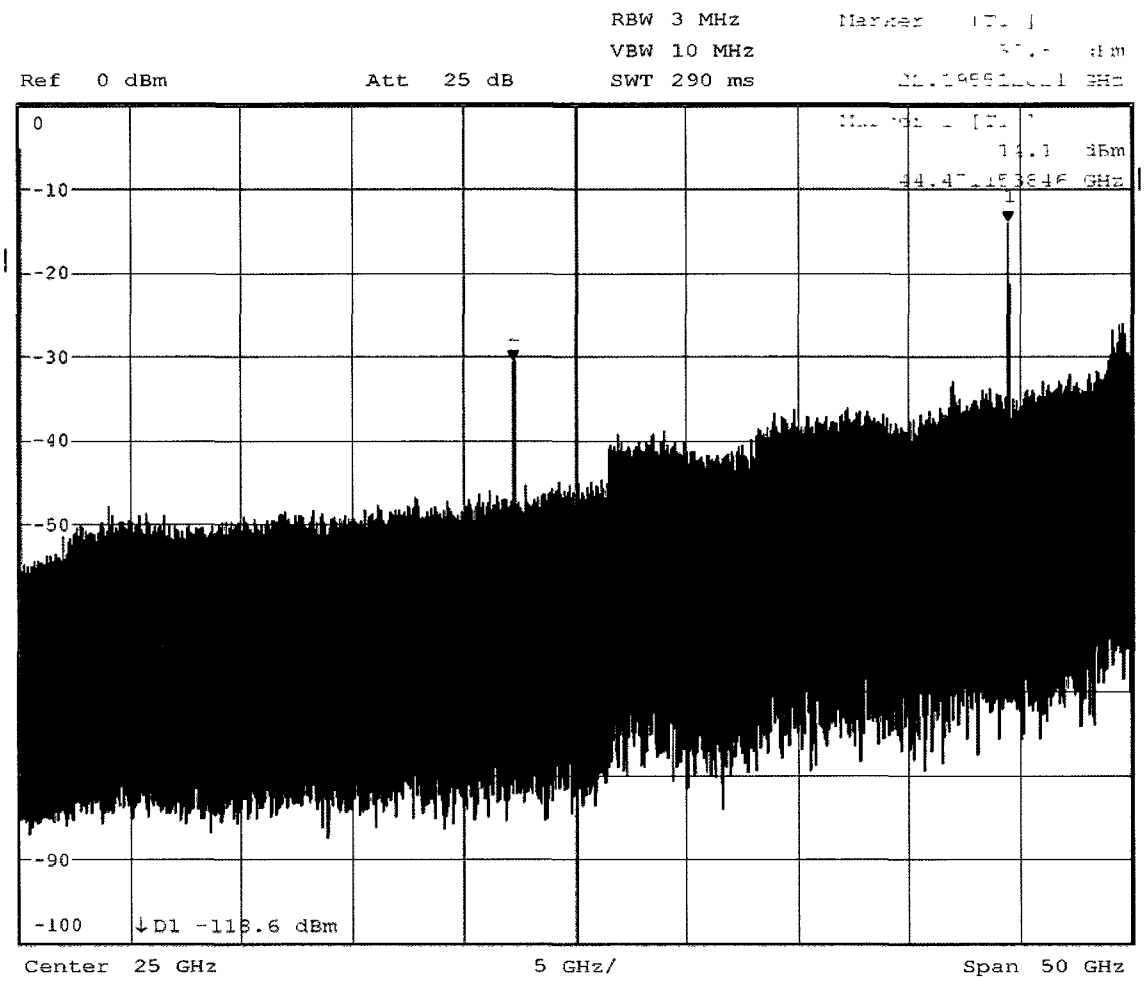


Figure 5.27 Frequency spectrum of the 44.47 GHz Oscillator System using the package-embedded hemispherical resonator (after finger pressure)

The measured frequency (fundamental oscillating frequency, f_o = 22.2 GHz) is shifted from the predicted frequency (f_o = 22.7 GHz) due to the added inductance from the ribbon bondwire. In E. Ruscito's measurement analysis [4], it was also found that the ribbon-bond connecting the resonator to the UMS VCO chip adds some impedance that would cause the resonant frequency to decrease. It is believed that the same thing has happened in the oscillator system and oscillating frequency has shifted down from 22.7 GHz to 22.2 GHz. Moreover, the tuning frequency range is also obtained. The tuning range is around 175 MHz when the tuning voltage is tuned from 0 V to 2 V.

The output power level for the desired tone (44.47 GHz) is fairly poor and this is most likely due to its unstable condition as well as a mismatch between the GaAs

chips (more details on the power losses will be discussed in the next section). The output power level for the 44.47 GHz signal is only at -14.18 dBm with the presence of a 10 dB attenuator that is used to protect the measuring equipment (Figure 5.27). Without the 10 dB attenuator, the output power level should be -4.18 dBm, which is still fairly poor compared to the simulated (12 dBm) or the target result (15 dBm). The measured results discussed above are compared with the simulated results at the end of this sub-section, ***a.*** (Table 5-2).

In the case of the microstrip resonator, the measured oscillator output is at 42.71 GHz with the first harmonic at 21.39 GHz (Figure 5.28). The frequency shift as compared to the simulated value of 42.6 GHz is again believed to be caused by the added inductance. The tuning frequency range for the oscillator using the microstrip resonator is around 960 MHz which is much higher compared to the oscillator using the hemispherical resonator (175 MHz). This is most likely due to the fact that the signal produced with the microstrip resonator is much more stable than the signal obtained using the hemispherical resonator (due to the required start-up condition).

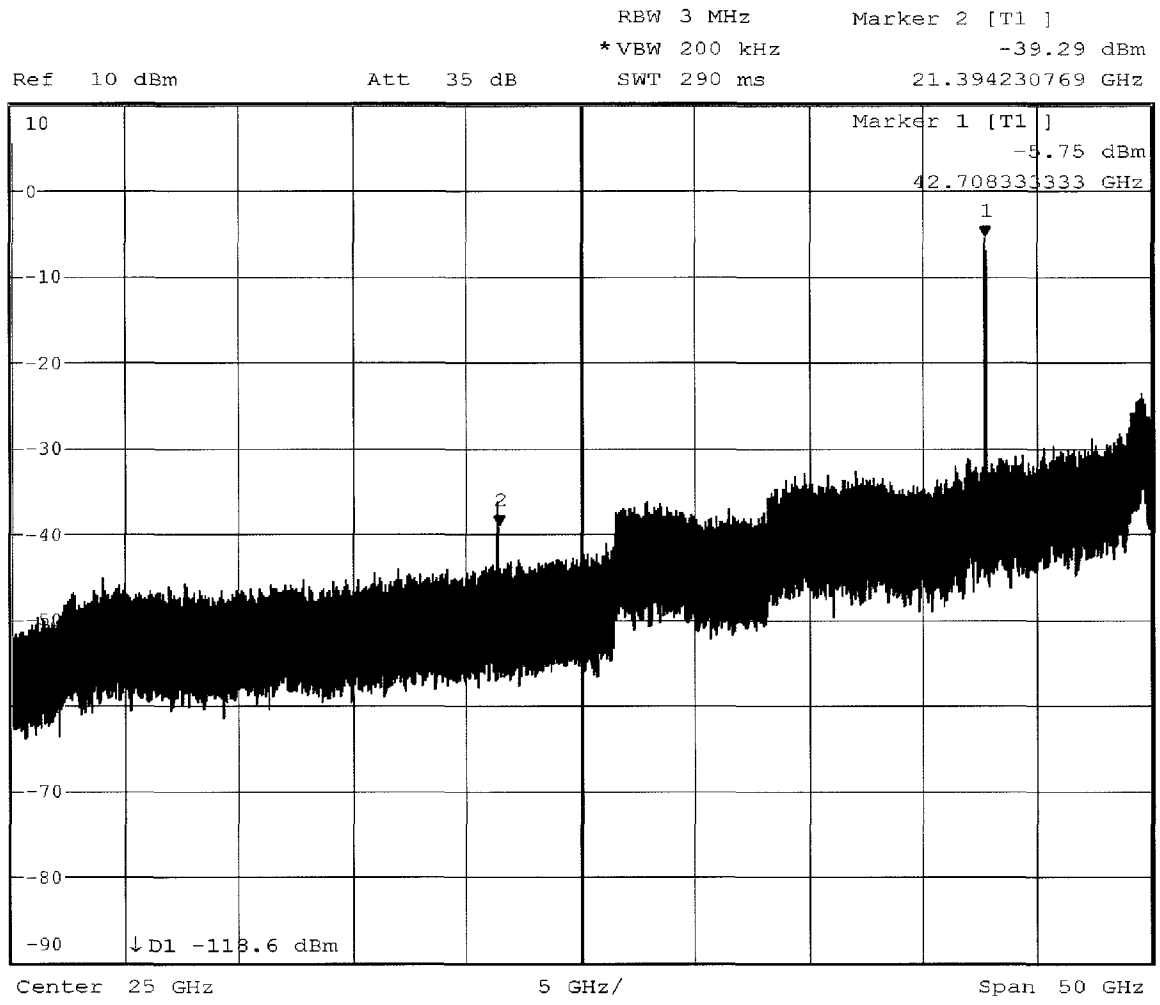


Figure 5.28 Frequency spectrum of the 42.71 GHz Oscillator System using the microstrip resonator

The output power of this module is also better than the power level of the oscillator system using the hemispherical resonator. The output power level using the microstrip resonator is at -5.75 dBm with a 10 dB attenuator in place; hence, the real output power is 4.25 dBm. This is better than the oscillator using the hemispherical resonator but it is still poor compared to the simulated value (11 dBm) as well as the target value (15 dBm). The power loss seen here are most likely coming from the bondwires and/or the impedance mismatches as there are no other significant tones in the frequency spectrum that would consume excessive power (more details on the power

losses are discussed in the next section). The measured results discussed above are compared with the simulated results (Table 5-2).

Table 5-2 Comparison between measured and simulated oscillating frequency, tuning range and output power for the oscillator system using the hemispherical resonator or the microstrip resonator

Parameters	Hemispherical Resonator (measured)	Hemispherical Resonator (simulated)	Microstrip Resonator (measured)	Microstrip Resonator (simulated)
Oscillating Frequency (GHz)	44.47	40.43	42.71	42.6
Tuning range (MHz)	175	3 GHz (simulated) *	960	3 GHz (simulated) *
Output Power (dBm)	-4.18	17	4.25	11

* 5 MHz (mfr. provided)

b. Phase Noise

The phase noise of the designed oscillator is very hard to measure as the carrier frequency is not as stable as desired (frequency drifts of up to 10 MHz observed in the process of taking a measurement). The phase noise of the oscillator using the hemispherical resonator is -112.4 dBc/Hz at 100 kHz offset (Figure 5.29). This value is very close to simulated value (-113 dBc/Hz at 100 kHz offset) and it able to meet the target value (-112 dBc/Hz at 100 kHz offset). Due to the drift in the carrier frequency, the first measurement (from 1 kHz to around 1 MHz) was unable to be completed, which a full measurement requires roughly four seconds to be completed, before the second measurement (from around 1 MHz to 30 MHz) begins (Figure 5.29). The bump that occurs from around 60 kHz to around 1 MHz is due to the equipment tracking issue and

this happens in every phase noise plot (it is more readable in the phase noise plot for the microstrip resonator which is shown later in this sub-section).

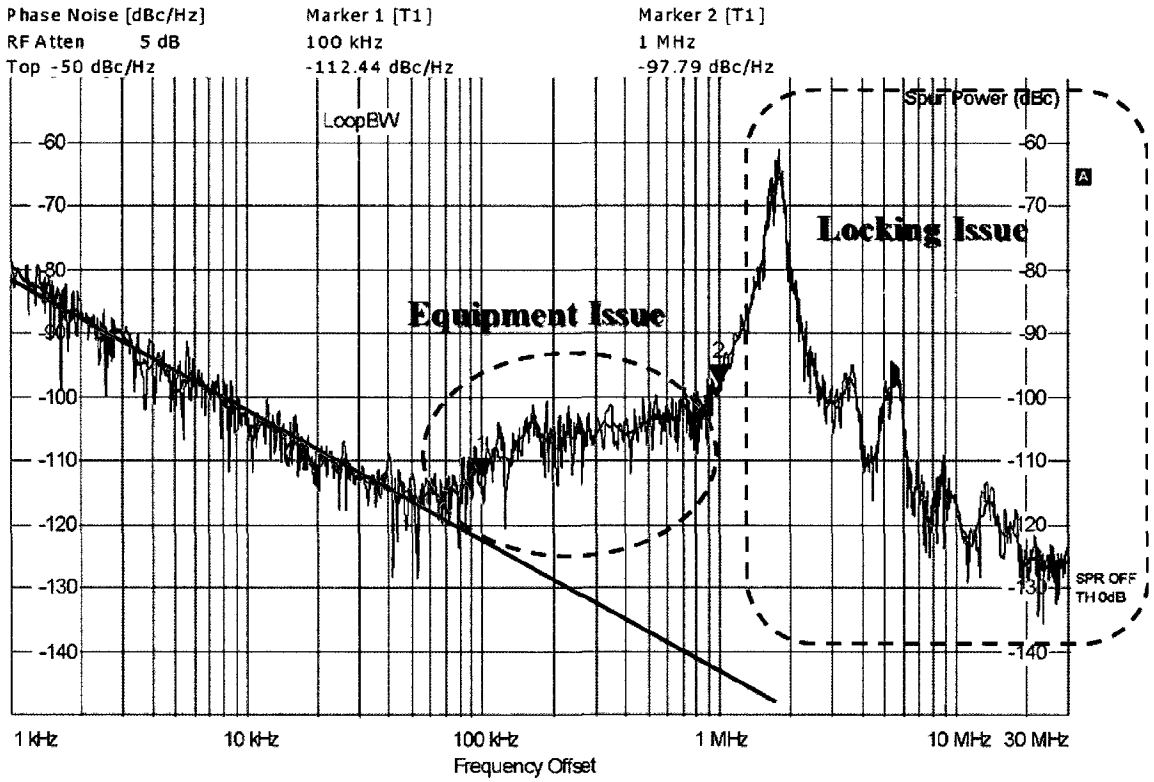


Figure 5.29 Phase noise of the 44.47 GHz oscillator system using hemispherical resonator

In order to properly predict the behaviour of the phase noise of the first measurement, a linear extrapolation is made (Figure 5.30). The extrapolated phase noise is -122 dBc/Hz at 100 kHz offset and -142 dBc/Hz at 1 MHz offset. This extrapolated value of -122 dBc/Hz is actually better than the simulated results by 9 dB and outperforms the target value by 10 dB. The measured results discussed above are compared with the simulated results at the end of this sub-section, ***b.*** (Table 5-3).

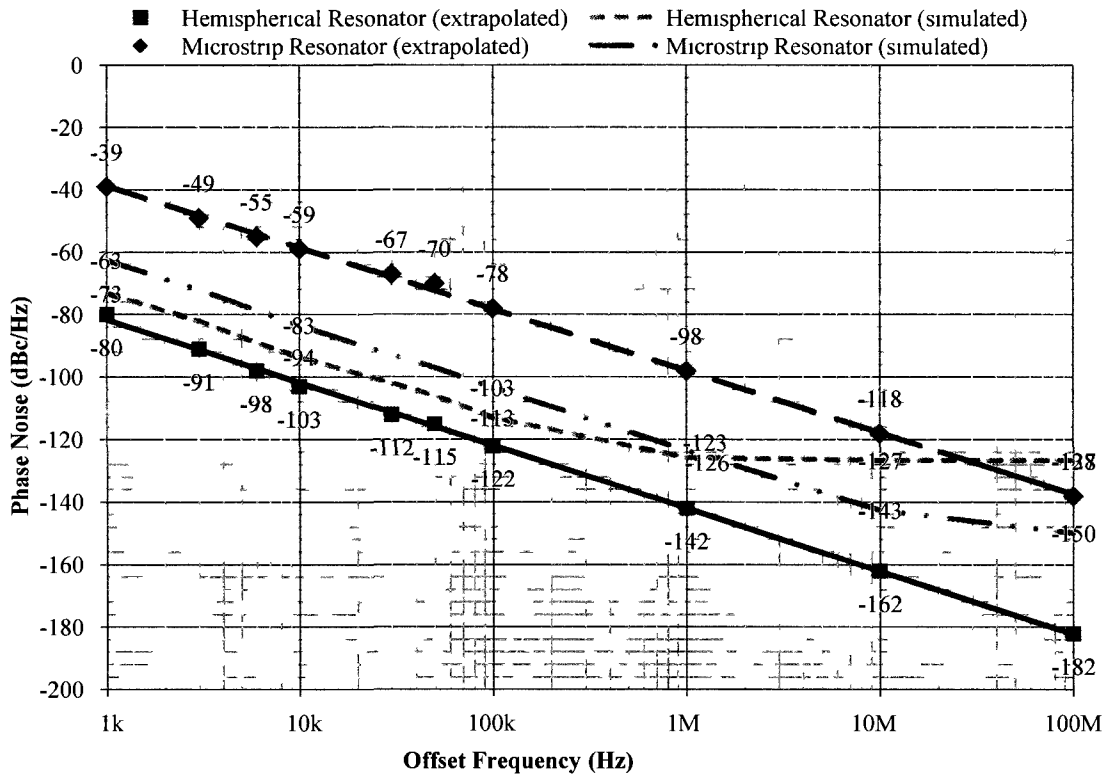


Figure 5.30 Extrapolated phase noise of the oscillator system using the high Q embedded hemispherical cavity resonator and the RT/Duroid microstrip resonator

On the other hand, the phase noise for the oscillator system using the microstrip resonator is far worse compared to using the hemispherical resonator. The phase noise is -62.75 dBc/Hz at 100 kHz offset with the tracking issue in place (Figure 5.31). The tracking issue is more readable in this plot (Figure 5.31) as the measurement was fully completed as opposed to the results using the hemispherical resonator, which was incomplete. The tracking issue (the bump) occurs from around 40 kHz to around 1 MHz and the result resumes its original path after 1 MHz; hence, an extrapolation was performed again to remove the bump. After the extrapolation, the phase noise becomes -78 dBc/Hz at 100 kHz offset and -98 dBc/Hz at 1 MHz offset (the plot is shown above on the same figure as for the hemispherical cavity resonator; Figure 5.30).

The reason that the measured phase noise using the microstrip resonator does not come relatively close to the simulated value may be because of the custom designed oscillator that had to be used in the simulation. The custom designed oscillator was

specifically designed using the lumped element representation of a microstrip resonator in order to meet the oscillation condition. Due to this fact, the input impedance of the custom designed oscillator that has been optimized for phase noise is different than the UMS VCO chip and hence the discrepancies are seen in the measurement. The results discussed above are again compared with the simulated value (Table 5-3).

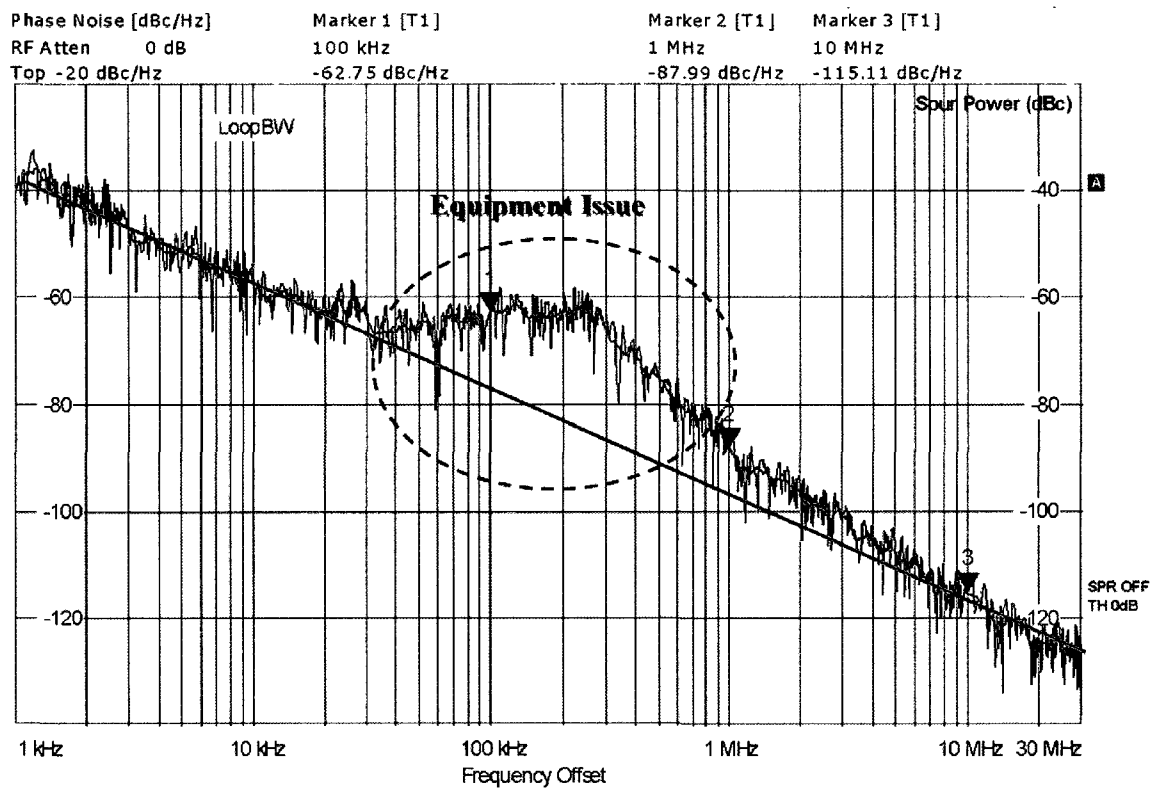


Figure 5.31 Phase noise of the 42.71 GHz oscillator system using microstrip resonator

Table 5-3 Comparison between measured and simulated phase noise for the oscillator system using the hemispherical resonator or the microstrip resonator

Parameters	Hemispherical Resonator (extrapolated*)	Hemispherical Resonator (simulated)	Microstrip Resonator (extrapolated*)	Microstrip Resonator (simulated)
PN @ 100 kHz offset **(dBc/Hz)**	-122	-113	-78	-103

* Extrapolated value of the measured data

5.4 Results Discussion

This section will discuss the measured results and provide explanation to the discrepancies observed when compared to the simulated results. There are three main factors that contributed to the discrepancies: one is the power loss issue, the other one is the equipment tracking and signal locking issues and the last one is the VCO start-up issue.

5.4.1 Power Loss Issue

The power level of the oscillator module is fairly poor for both the hemispherical resonator module and the microstrip resonator module. The power loss can come from several places in the circuit. The first issue is with the fabrication of the Duroid card. There are some discrepancies in the width of the microstrip lines as it is etched in and become thinner as compared to the designed width. For example, the 50 Ω impedance line for the output launcher was supposed to be close to 763 μm but the real width turned out to be closer to 690 μm (in some cases, the discrepancy is even larger). However, this is unavoidable as it is part of the manufacturing tolerances.

Another issue that may have caused the power loss is the decoupling capacitors. On the first assembly of the Duroid card, the 110 pF chip capacitors were used as they are more available. However, some of the power may have been lost in the DC lines as the decoupling capacitor value did not meet the specification. The UMS VCO specification indicates that the required decoupling capacitor value is equal to or greater than 120 pF. After replacing the 110 pF capacitors with 150 pF capacitors, the power level was improved by around 1 dB.

The last and the most important issue that may have caused the power loss is because of the mismatch between the UMS VCO and the Hittite LNA as well as the ribbon-bond losses. As mentioned in the last section (Section 5.3), the output power level of the oscillator system using the microstrip resonator with the Hittite LNA being connected is at -5.75 dBm (Section 5.3.6) while the power level using the same

configuration but without the Hittite amplifier is around -5.87 dBm (Section 5.3.4). This showed that a significant loss must be present after the UMS VCO chip that would almost cancel out all of the gain that the Hittite amplifier is able to provide (S_{21} = 10.8 dB). This is most likely due to the mismatch between the UMS VCO and the Hittite LNA which was identified in the simulation but not corrected as the predicted loss was not as significant. The ribbon-bonds may have added more loss to the circuit as the simulated length is around 300 μm but the actually length is around 500 μm to 800 μm. If the cause for the oscillator system using the microstrip resonator to lose roughly 10.68 dB of power (as less than 1 dB of improvement was seen by adding the Hittite LNA) is from the mismatched components and the longer ribbon-bonds, it is safe to say the oscillator system using the hemispherical resonator also experienced the same loss. This means that the power level for the 44.47 GHz oscillator system using the hemispherical resonator could have a power level of around 6.5 dBm (i.e. -4.18 dBm + 10.68 dB).

5.4.2 Equipment Tracking and Signal Locking Issue

As discussed in the previous section where the phase noise plots were shown (Section 5.3.6), there is always a "bump" on the phase noise plot around 100 kHz to 1 MHz that would offset the measured result. This is believed to be some equipment tracking issue that the Rohde & Schwarz SSA has as the bump only occurs in that region and for other kind of oscillators as well. The tracking issue is yet to be solved and further investigation is required.

Locking onto the output signal is also a major issue that occurred. As mentioned in Section 5.3.6, the free running oscillator shifts in frequency in less than four seconds before the SSA can capture a single complete data. This is very problematic when trying to obtain the correct phase noise measurements. There appears to be no immediate solution to this problem and the issue will need to be further invested.

5.4.3 Start-up Issue

As mentioned earlier, a manual "push" is required to make the oscillator lock into the correct state at 44.47 GHz after the power is turned on. In Section 5.3.3, the VCO was found to have two oscillating points: one at around 13.9 GHz and one at around 22.7 GHz. In measurement, at start-up, the oscillator tends to favour the unwanted 12.66 GHz (13.9 GHz in simulation) signal but was able to lock onto into the correct state at 22.2 GHz (22.7 GHz in simulation; comparing first harmonic) immediately after a pressure is applied to the top side of the Duroid card just above the resonator area (Figure 5.32). This was believed to be caused by a thin layer of air just below the coupling aperture and thus making the coupling very weak. Further investigation would be required to solve this issue. One of the methods would be to use a bigger aperture circle to acquire more coupling. Another method would be to cut a gap on the microstrip feed to add a small capacitance also to increase coupling.

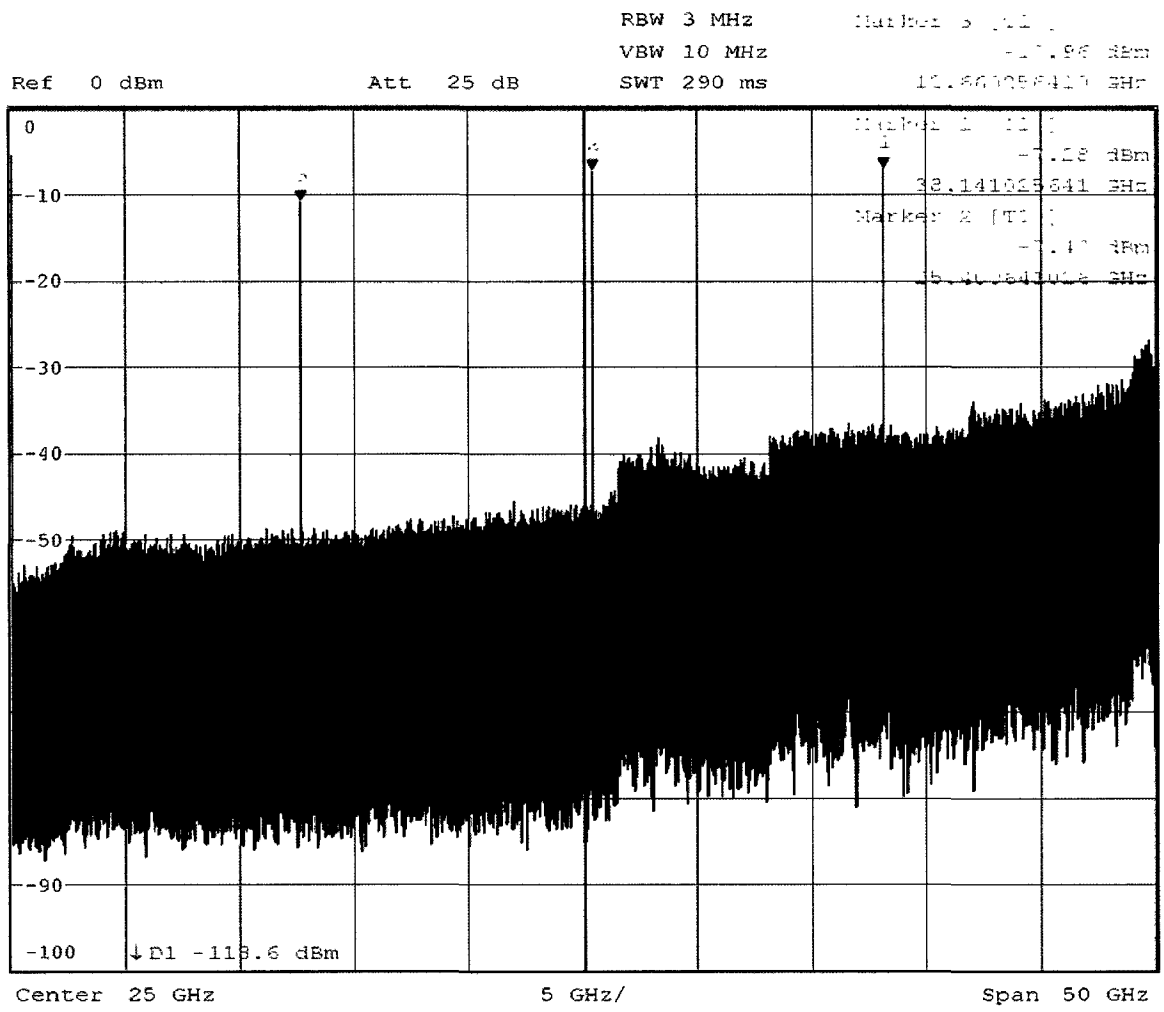


Figure 5.32 Frequency spectrum of the 38.1 GHz Oscillator System using the package-embedded hemispherical resonator

5.5 Summary

The chapter went through several measurements using different equipment and for different components/module and the whole oscillator system. Summarizing these measurements, it can be concluded that the phase noise and the oscillation frequency obtained using the hemispherical resonator meet the target value while the output power performs fairly poorly (Table 5-4). The extrapolated phase noise from the measured result for the oscillator system using the hemispherical resonator showed a phase noise of -120 dBc/Hz at 100 kHz offset which outperforms the target value of -112 dBc/Hz at 100

kHz offset by 8 dB. The oscillation frequency is at 38 GHz for the oscillator using the hemispherical resonator and at 42.5 GHz for the oscillator using the microstrip resonator. Both signals are close to the desired 40 GHz target. The output power level did not meet the target value due to several issues that may have caused the power loss. The main issue is due to the mismatch between components. The measurement obtained using the microstrip resonator did not meet the target specification (Table 5-5). On the other hand, some equipment tracking issue and signal locking issue requires further investigation.

Table 5-4 Summary of the measured, the simulated and the target values of the system parametric performances using the embedded hemispherical cavity resonator

Parameters	Measured	Simulated	Target value
PN @ 100 kHz offset (dBc/Hz)	-122*	-113	-112
***P*$_{out}$ (dBm)**	-4.18	12	15
Oscillating Frequency (GHz)	44.47	40.43	40
Tuning Range (MHz)	175	3 GHz**	as much as possible

* Extrapolated value from the measured data

** 5 MHz (mfr. provided)

Table 5-5 Summary of the measured, the simulated and the target values of the system parametric performances using the RT/Duroid 5880 microstrip resonator

Parameters	Measured	Simulated	Target value
PN @ 100 kHz offset (dBc/Hz)	-78*	-103	-112
***P*$_{out}$ (dBm)**	4.25	11	15
Oscillating Frequency (GHz)	42.71	42.60	40
Tuning Range (MHz)	960	3 GHz**	as much as possible

* Extrapolated value from the measured data

Chapter 6

Conclusion

This chapter summarizes the work done in this thesis including review of the design of the 40 GHz oscillator system and concluding on the performances it can provide for E-band applications. The highlights of the contributions will be reviewed and some of the possible future work will be mentioned.

6.1 Summary of Thesis Work

The design of a low cost and low phase noise oscillator is achieved with room for future work. The 40 GHz oscillator system was successfully designed and implemented with the 20 GHz package-embedded hemispherical resonator with close collaboration with another colleague, Elizabeth Ruscito, who designed the high Q and low cost hemispherical cavity resonator.

The oscillator system design was a success as many steps and precautions have been taken to achieve this. In Chapter 2, the fundamental background on phase noise and effects of phase noise on the system performance were reviewed. The phase noise requirement to achieve the target data rate of 1.5 Gbps was derived. At 80 GHz, the target phase noise is -106 dBc/Hz at 100 kHz offset.

In Chapter 3, a 40 GHz VCO was designed using the United Monolithic Semiconductor (UMS) 0.15 μm GaAs pHEMT technology design kit. The VCO was carefully studied to understand the internal performances and the design difficulties at 40

GHz using the GaAs pHEMT technology. A doubler was also designed in order to incorporate external resonators at 20 GHz to be comparable to the COTS component from UMS (part number: CHV2240).

In Chapter 4, a 40 GHz low cost oscillator system design using the COTS components, UMS CHV2240 VCO and Hittite HMC-ALH445 buffer amplifier, was designed on a RT/Duroid 5880 substrate. The designed Duroid card was then integrated onto the jig packaging to be incorporated with the 20 GHz high Q package-embedded hemispherical cavity resonator [4].

In Chapter 5, the fabrication concerns and tolerances of the implemented 40 GHz oscillator system were discussed. Several measurements were taken to study the performance at each stage in the system in order to identify any potential problems. The parametric measurements on phase noise, output power and oscillating frequency were compared between hemispherical resonator and microstrip resonator. The final result showed a phase noise of -120 dBc/Hz at 100 kHz offset is achievable at 38 GHz using the high Q hemispherical cavity resonator. The output power was however an issue and was discussed.

This chapter summarizes the thesis work, highlights the thesis contributions and points out potential future works.

6.2 Highlights of Thesis Contributions

The contributions of this thesis to the scientific community are summarized below.

- The designed 40 GHz oscillator system using package-embedded hemispherical cavity resonator confirms that suitably low phase noise levels are achievable.

- The low cost package of the oscillator module using COTS components confirms the capability of immediate commercial mass production.

- The oscillator designed using the UMS 0.15 μm GaAs pHEMT technology design kit allows designers to study the internal effects of a 40 GHz common gate oscillator when using the 0.15 μm GaAs pHEMT technology.

- The oscillator system designed using COTS components on the RT/Duroid 5880 substrate produces a ready-to-use template that could allow designers to study performance trade-offs when components are replaced (e.g. replace the substrate material with different dielectric constant, replace Hittite LNA with another COTS component, change the length of bondwires, etc.).

6.3 Future Work

The thesis provided excellent phase noise results for a low cost 40 GHz oscillator yet the power loss is significant. Re-designing the Duroid card with proper matching circuits would improve the power level. On the other hand, locking onto the output signal of the oscillator is very difficult and further experiment on signal locking methods will have to be investigated. The tracking issue with the Rohde & Schwarz SSA can also be investigated to help improve the precision of future measurements.

The design work done in Chapter 3 for the oscillator designed using the UMS 0.15 μm GaAs pHEMT technology design kit was limited to simulations. It would be a good idea to fabricate this design to compare and evaluate its performance. An efficient and performance maximized layout would need to be designed before fabrication.

Once the signal locking and the power issues for the designed 40 GHz oscillator are corrected, the logical next step would be to add a sub-harmonic mixer at the end of the oscillator to up-convert the LO signal to 80 GHz. This can then be tested in an E-band transceiver to see the data rate performance with the use of the designed low cost oscillator. If all goes well, the LO can be mass produced for use in many E-band applications.

Appendix A

Matlab Code

Core Function:

```
function [y1, y2] = BERvsX(Num, M, vdeg, k)
global DataRate, global BW,
global EbNo, global SNRwithoutPN, global SNRwithPN, global variance,
global x, global g,

DataRate = 1 5e9,
BW = 250e6,

if (Num == 1)
   %BERvsEbNo_noPN_noECC,
   %Equations from Sampei (Digital Wireless book)
   EbNo = 0 1 25,
   x = 10 ^(EbNo/10),
   g = x,

elseif (Num == 2)
   %BERvsSNR_noPN_noECC,
   SNRwithoutPN = (10 ^(EbNo/10)) * (DataRate/BW)
   g = SNRwithoutPN,
   x = EbNo,

elseif (Num == 3)
   %Equations from Ryu (Nonlinear Anlysis of the Phase Noise in the OFDM
   %Communication System)
   SNRwithoutPN = 0 1 35,
   variance = vdeg/180*pi,
   %SNRwithPN = (10 ^(SNRwithoutPN/10))/(1+(4*(variance ^2)*(10 ^(SNRwithoutPN/10)))),
   SNRwithPN = 1 /((1 /(10 ^(SNRwithoutPN/10)))+(4*(variance ^2))),
   g = SNRwithPN,
   x = SNRwithoutPN,
end
```

```
W = 0 5,
   if k == 1
      L = '-',
   elseif k == 2
      L = ' ',
   elseif k == 3
      L = '- ',
   elseif k == 4
      L = '--',
   elseif k == 5
      L = '-',
      W = 2,
   elseif k == 6
      L = ' ',
      W = 2,
   end
   vdeg
   variance

if (M == 64)
   %64 QAM
   y1 = (((7/24)*erfc(sqrt((1/7)*g)))-((49/384)*((erfc(sqrt((1/7)*g))) ^2))),
   semilogy(x,y1, 'blue',
            'LineStyle', L,
            'LineWidth', W),
elseif (M == 256)
   %256 QAM
   y2 = (((15/64)*erfc(sqrt((4/85)*g)))-((225/2048)*((erfc(sqrt((4/85)*g))) ^2))),
   semilogy(x,y2, 'red',
            'LineStyle', L,
            'LineWidth', W),
end

hold on,
```

Calling Function:

```
function myBER(Num)

if Num == 1
   BervsX(3,64,0,1)
   BervsX(3,256,0,1)
   ylim([0 000000001 1]), xlabel('Eb/No (dB)'), ylabel('BER'), grid on,
   legend('64 QAM', '256 QAM', 'Location', 'NorthEastOutside'),

elseif Num == 3

   BervsX(3,64,0,1)
   BervsX(3,64,1,2)
   BervsX(3,64,2,5)
   BervsX(3,64,2 2,3)
   %BervsX(3,64,2 4,4)
```

```
    BervsX(3,64,2 4,6)
    BervsX(3,256,0,1)
    BervsX(3,256,0 5,2)
    BervsX(3,256,1,3)
    %BervsX(3,256,0 8,4)
    BervsX(3,256,1 2,5)
    BervsX(3,256,1 4,6)
    ylim([0 000000001 1]), xlabel('SNR, Eb/No (dB)'), ylabel('BER'),
       grid on,
    legend('\sigma_\phi = 0^o  , 64 QAM', '\sigma_\phi = 1^o , 64 QAM',
       '\sigma_\phi = 2^o  , 64 QAM', '\sigma_\phi = 2 2^o , 64 QAM',
       '\sigma_\phi = 2 4^o , 64 QAM', '\sigma_\phi = 0^o  , 256 QAM',
       '\sigma_\phi = 0 5^o  , 256 QAM', '\sigma_\phi = 1^o , 256 QAM',
       '\sigma_\phi = 1 2^o , 256 QAM', '\sigma_\phi = 1 4^o , 256 QAM',
       'Location', 'NorthEastOutside'),

end
```

Appendix B

Buffer Amplifier Designs

B-1 Common Drain (Source Follower) Amplifier Design

The designed common drain (CD) amplifier circuit consists of a stabilizing resistor at the drain (*R2*) as well as a current sink resistor at the source (*R1*; Figure B.1).

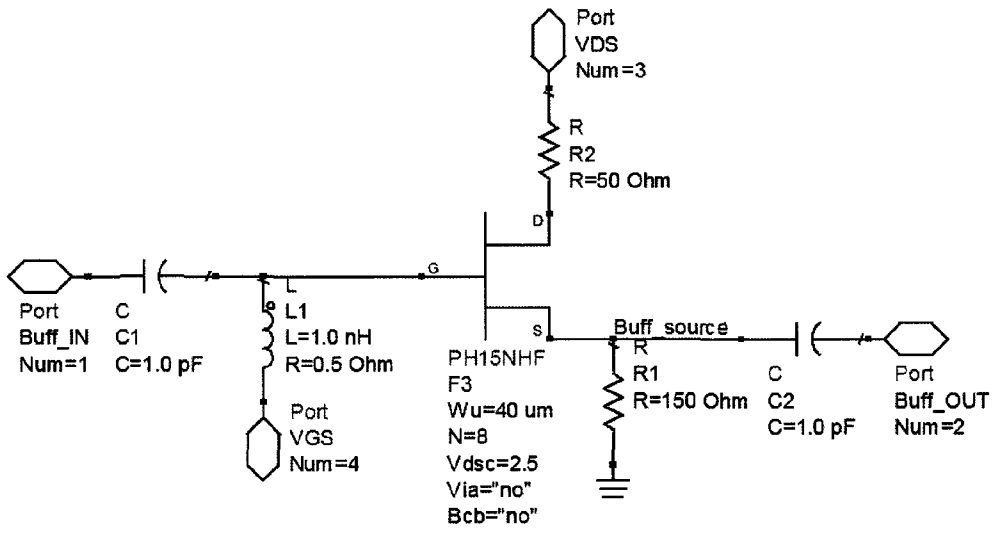


Figure B.1 Source Follower amplifier circuit

For small FET size and drain resistance, for example 2x20 μm and *R2* = 5 Ω, the FET is unstable (Figure B.2). The magnitude of S_{11}, $|S_{11}|$, needs to be below 1.0 in order to ensure stability. Unconditional stability ($|S_{11}|$ below 1.0 for all frequencies) is

very important in an amplifier design as unstable will make the amplifier oscillate and thus malfunction.

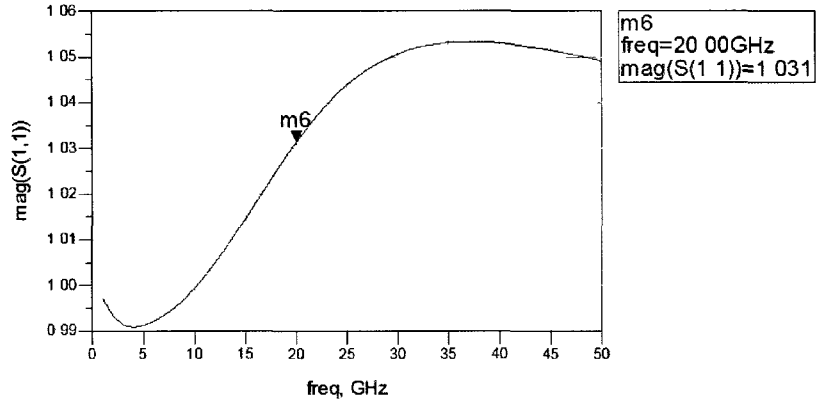


Figure B.2 CD amplifier S_{11} plot using 2x20 μm FET and *R2* = 5 Ω

Keeping the FET size the same and increasing the drain resistance *R2* to 50 Ω, stability is achieved but matching is very poor. For good matching, $|S_{11}|$ should be as close to zero as possible (no reflection) but in this case $|S_{11}|$ is very high, close to 1 (maximum reflection; Table B-1).

Unconditional stability and better matching is achieved when the FET size is large (the example shown below uses 8x40 μm; Figure B.3), which gives a S_{21} gain of around -3 dB (Figure B.4). This is expected as the function of a source follower is to provide good matching but sacrifice gain.

The output of the CD amplifier is also simultaneously matched by adjusting the source resistance *R1*. The output impedance is close to 50 Ω ($|S_{22}|$ is very close to zero at 0.049) at 20 GHz (Figure B.5). This is one of the biggest advantages of using a CD amplifier configuration as it provides isolation between input and output so matching can occur at both ports simultaneously.

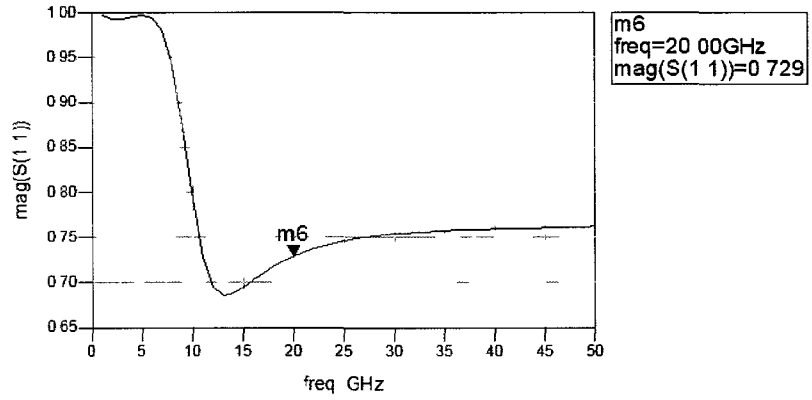


Figure B.3 CD amplifier S_{11} plot using 8x40 μm FET and $R2$ = 50 Ω

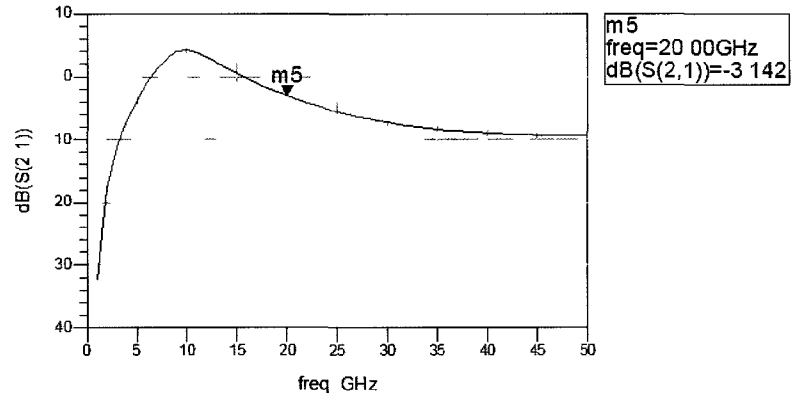


Figure B.4 CD amplifier S_{21} plot using 8x40 μm FET and $R2$ = 50 Ω

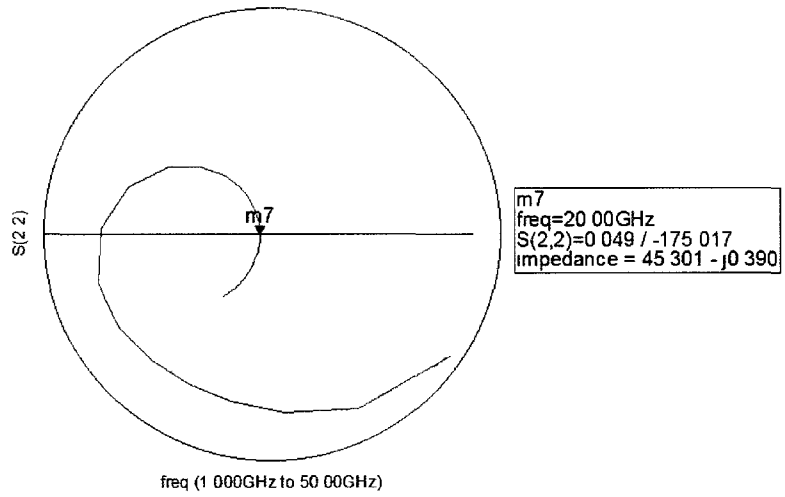


Figure B.5 CD amplifier S_{22} plot using 8x40 μm FET and $R2$ = 50 Ω

Table B-1 CD amplifier S-parameter results summary at 20 GHz

FET size (μm)	*R2* (Ω)	$\|S_{11}\|$	$\|S_{22}\|$	S_{21} (dB)
2x20	5	1.031	-	-
2x20	50	0.987	0.106	0.517
8x40	50	0.729	0.049	-3.142

B-2 Common Gate Amplifier Design

The designed common gate (CG) amplifier circuit consists of a resistor at the gate (*R1*; Figure B.6).

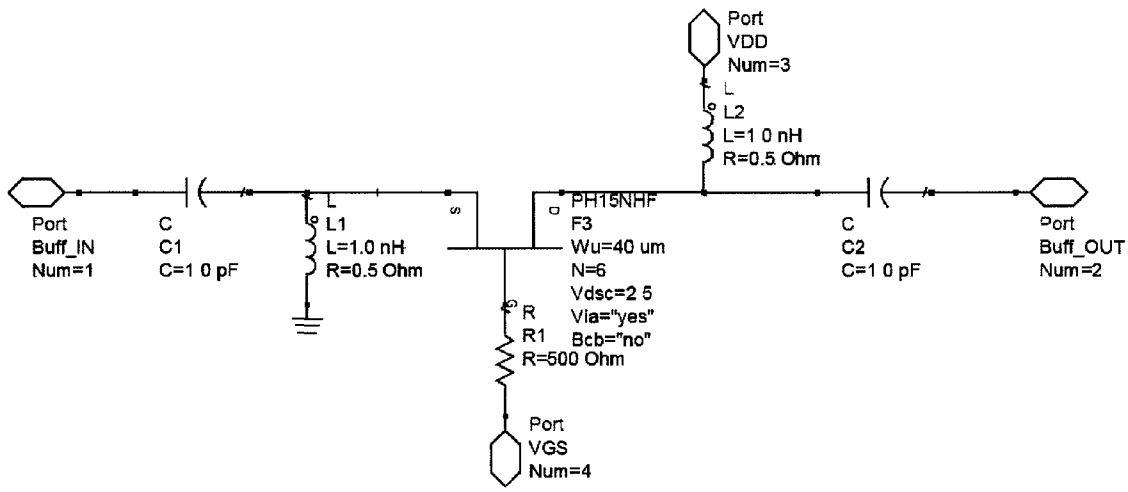


Figure B.6 Common gate amplifier circuit

For small FET size and gate resistance, for example 2x20 μm and *R1* = 5 Ω, the amplifier provides a very good input match at $|S_{11}|$ = 0.44 but very poor output match at $|S_{22}|$ = 0.948. The S_{21} gain is also not satisfying at -0.237 dB but it is better than the CD amplifier design. The results in CG amplifier design are summarized in Table B-2.

Keeping the FET size the same and increasing the gate resistance slightly helps with the output matching but degrades the S_{21} gain. The input match stays relatively the same. An example with 2x20 μm FET and *R1* = 200 Ω shows minor improvement in

output match ($|S_{22}|$ = 0.802) but has a significant degradation in S_{21} gain, from -0.2 dB to -2.5 dB.

On the other hand, keeping *R1* low at 5 Ω but increasing the FET size improved the gain but matching for both input and output got worse. The results of an example using 6x40 μm FET with *R1* = 5 Ω shows a degradation in matching as $|S_{11}|$ is increased from 0.44 to 0.824 and $|S_{22}|$ is much closer to 1.0 at 0.973. The S_{21} gain, however, is improved from -0.2 dB to 2 dB.

Since increasing FET size or gate resistance *R1* both demonstrated some improvements either in matching or gain, the combined analysis is also done by increasing both FET size and *R1*. The results with 6x40 μm and *R1* = 500 Ω improved both the input and the output match with slight degradation in gain. $|S_{11}|$ is reduced to -8 dB (Figure B.7), $|S_{22}|$ is finally improved ($|S_{22}|$ = 0.468; Figure B.8) and S_{21} is decreased to -1.4 dB (Figure B.9).

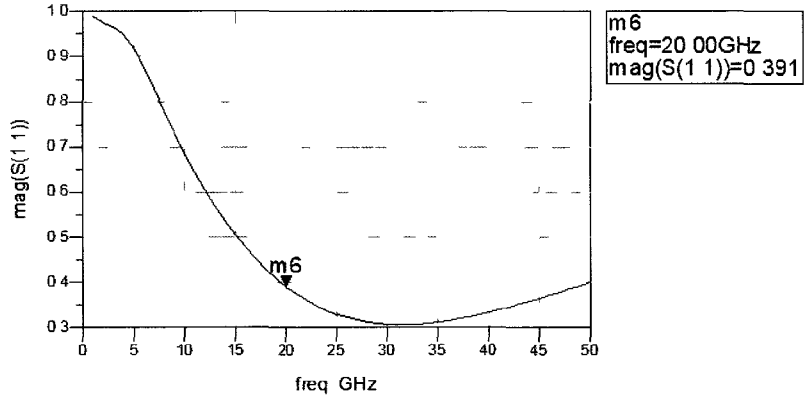


Figure B.7 CG amplifier S_{11} plot using 6x40 μm FET and *R1* = 500 Ω

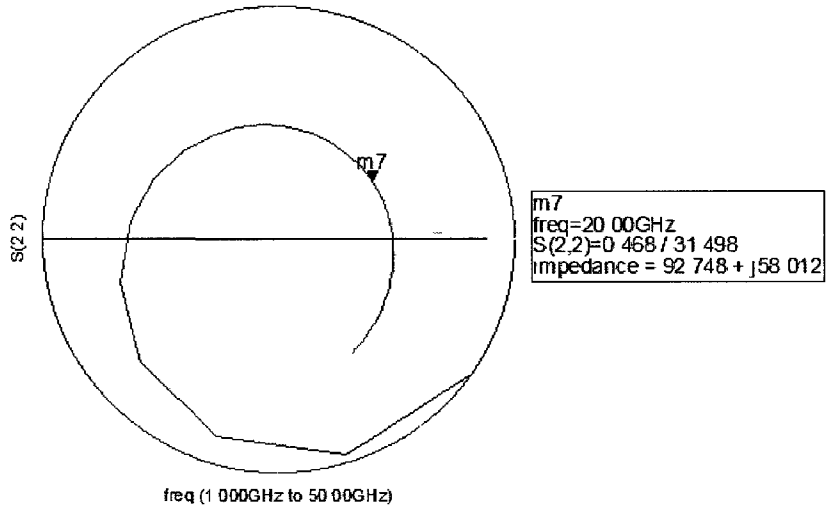


Figure B.8 CG amplifier S_{22} plot using 6x40 μm FET and $R1$ = 500 Ω

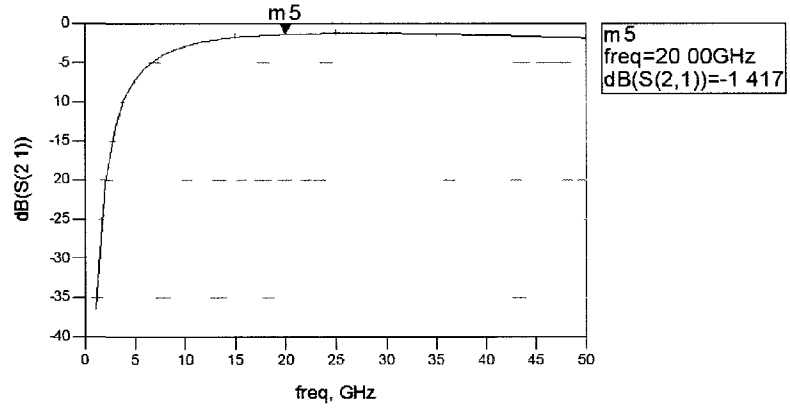


Figure B.9 CG amplifier S_{21} plot using 6x40 μm FET and $R1$ = 500 Ω

Table B-2 CG amplifier S-parameter results summary at 20 GHz

FET size (μm)	$R1$ (Ω)	$\|S_{11}\|$	$\|S_{22}\|$	S_{21} (dB)
2x20	5	0.440	0.948	-0.237
2x20	200	0.451	0.802	-2.538
6x40	5	0.824	0.973	2.181
6x40	500	0.391	0.468	-1.417

B-3 Common Source Amplifier Design

The designed common source (CS) amplifier circuit consists of a stabilizing resistor in series of the feed inductor at the gate (Figure B.10).

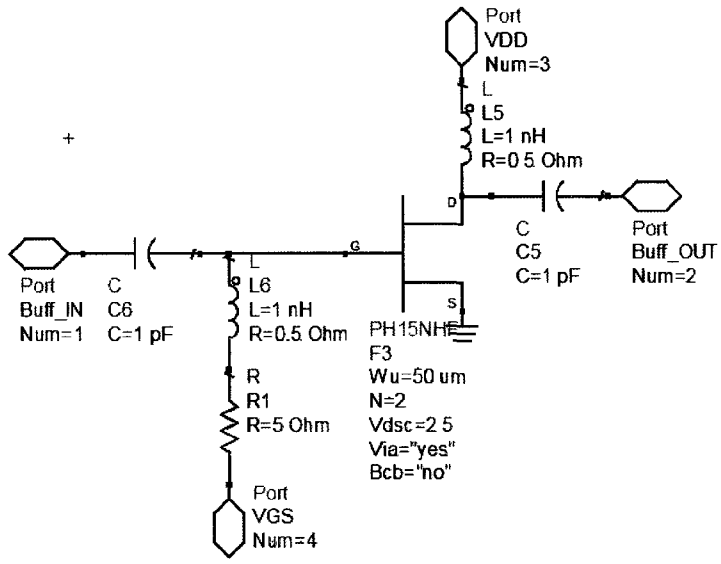


Figure B.10 Common source amplifier circuit

The common source configuration provides a very high S_{21} gain when compared to CD and CG configurations. This feature boosted the S_{21} gain to 8.8 dB when a 2x20 μm FET is under test. However, a great feature always comes with some sacrifices and that is the input and output matching. Both $|S_{11}|$ and $|S_{22}|$ are very close to 1.0 indicating the high losses in the input and output ports. Moreover, the S_{11} is not under 1.0 at all frequencies meaning it is not unconditionally stable. However, this can be easily overcome by adding a stabilizing resistor *R1*. The details of the CS amplifier design are again summarized in a table (Table B-3).

The stabilizing resistor *R1* helped the CS amplifier become unconditionally stable while slightly improving the input match (by around 0.05). However, the added *R1* also degraded the performance on S_{21} gain; S_{21} is degraded by 0.3 dB. Further analysis by increasing the *R1* shows that higher *R1* can improve the input match, S_{11}, but will also

decrease the S_{21} gain. This analysis also proved that the stabilizing resister has no effect on the output matching as S_{22} stays relatively constant as *R1* is being varied.

The size of the FET helped with the output matching but generally decreases the input matching and gain performances as it is increased (using higher gate fingers). However, using gate fingers = 2 and sweeping the unit gate width, W_u, shows that a sweet spot can be found at Wu = 50 with best input match and highest gain. The S_{11} and S_{21} performances as W_u is varied at 20 GHz (Figure B.11). It should be noted that this sweet spot only complied when the *R1* is at 5 Ω and would change if *R1* is changed. The resulting $|S_{11}|$ is decreased to 0.8 (Figure B.12), the output is well matched at 20 GHz ($|S_{22}|$ = 0.377; Figure B.13) and an excellent gain of 11 dB is achieved (Figure B.14).

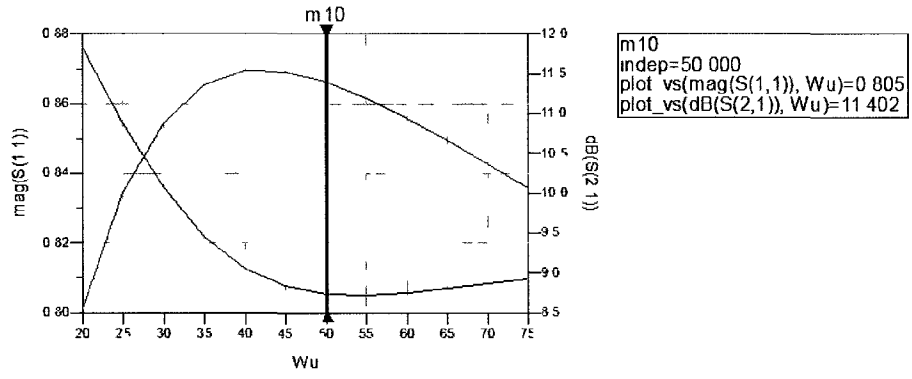


Figure B.11 CS amplifier S_{11} and S_{21} performances as W_u is varied at 20 GHz

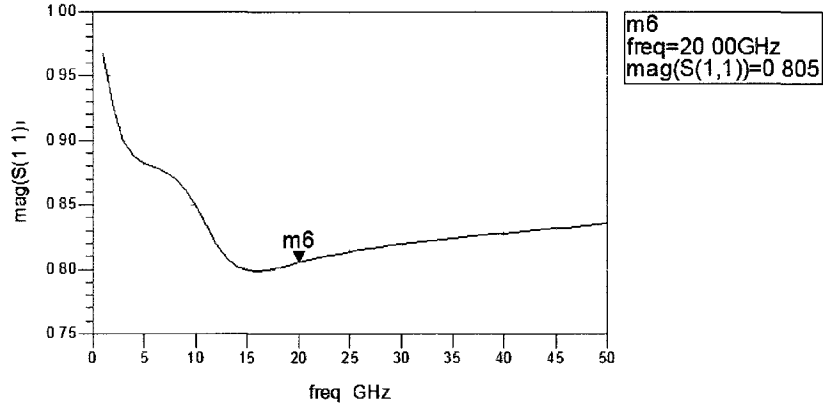


Figure B.12 CS amplifier S_{11} plot using 2x50 μm FET and *R1* = 5 Ω

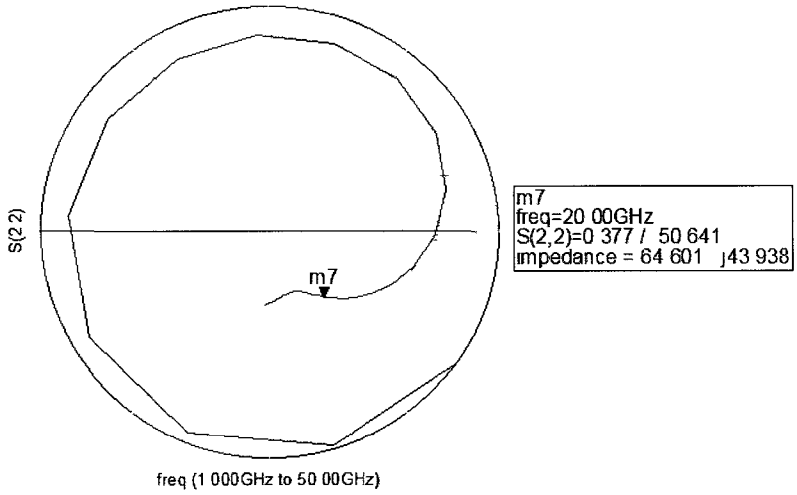


Figure B.13 CS amplifier S_{22} plot using 2x50 μm FET and $R1$ = 5 Ω

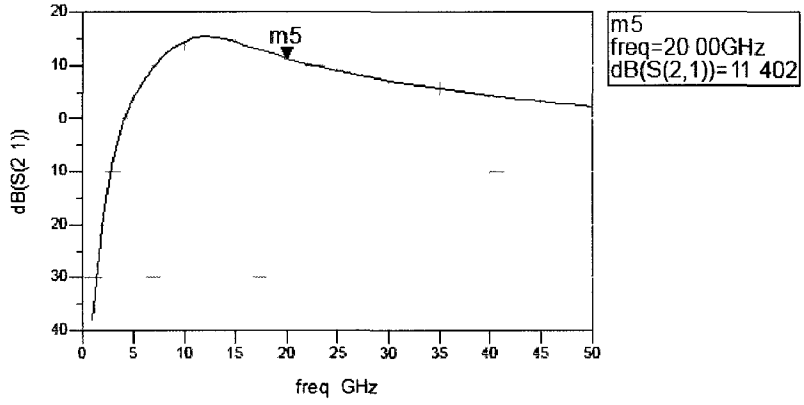


Figure B.14 CS amplifier S_{21} plot using 2x50 μm FET and $R1$ = 5 Ω

Table B-3 CS amplifier S-parameter results summary at 20 GHz

FET size (μm)	$R1$ (Ω)	$\|S_{11}\|$	$\|S_{22}\|$	S_{21} (dB)
2x20	-	0.933	0.816	8.816
2x20	5	0.876	0.817	8.555
2x20	30	0.654	0.816	7.400
6x40	5	0.859	0.374	7.002
2x50	5	0.805	0.377	11.402

Appendix C

Modeling of RT/Duroid 5880 Microstrip Resonator using Parallel Resonant Circuit

To model a λ/4 shorted RT/Duroid 5880 microstrip resonator at 20 GHz using the parallel resonant circuit, some parameters including the width of microstrip, W, the length of microstrip, l, and the attenuation, α_{dB} was required and can be obtained using ADS simulator tool. Using the LinCalc function in ADS, the mentioned parameters of a λ/4 microstrip resonator can be simulated if all the properties of the substrate material (in this case, RT/Duroid 5880; Figure C.1) as well as the resonant frequency, f_o (in this case, 20 GHz), the electrical length, E (in this case, 90°) and the characteristic impedances, Z_o (chosen to be 50 Ω) are specified.

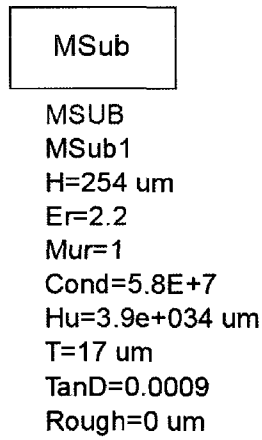


Figure C.1 RT/Duroid 5880 substrate properties

The parameter values obtained using ADS are as follows:

$$W = 763.624\ \mu m$$
$$l = 2733.46\ \mu m$$
$$\alpha_{dB} = 0.019\ dB$$

Since the designed microstrip resonator has a length of λ/4 and it is short on one side, this length also corresponds to the length obtained from ADS. Equating the two parameters would yields a wavelength, λ, of 0.01093 m.

The parallel RLC resonant circuit can then be calculated from the above values using the λ/4 shorted microstrip to parallel lumped RLC equations (Equations C.1 to C.3) described in Pozar's "Microwave Engineering" textbook [16].

$$R = \frac{Z_0}{\alpha_{Np/m} \cdot L} \tag{C.1}$$

$$C = \frac{\pi}{4 \cdot \omega_O \cdot Z_o} \tag{C.2}$$

$$L = \frac{1}{C \cdot {\omega_O}^2} \tag{C.3}$$

Substituting the above values and noting that there is unit conversion for the attenuation parameter, $\alpha_{Np} \approx \alpha_{dB} / 8.68$ and $\alpha_{Np/m} = \alpha_{Np} x L$, the RLC values are calculated. The values are as follows where $\omega_o = 2\pi f_o$:

$$R = 22.842\ k\Omega$$
$$C = 125\ fF$$
$$L = 0.5066\ nH$$

Finally, the unloaded quality factor, Q_u, can be extracted from the lumped RLC values using the Q factor equation for a λ/4 shorted microstrip resonator (Equation C.3; [16]):

$$Q = \omega_o RC \tag{C.3}$$

The yielded Q value is 358.8.

Appendix D

UMS CHV2240 VCO Specification Sheet

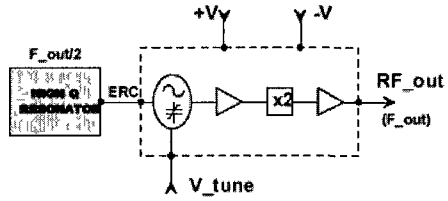
The following pages contain the replication of the first two pages of the Multifunction K-band VCO and Q-band Multiplier (part number: CHV2240) specification sheet from United Monolithic Semiconductor [41].

Multifunction K-band VCO and Q-band Multiplier

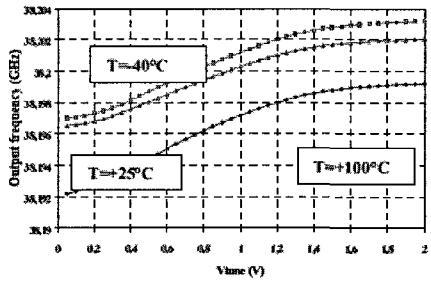
GaAs Monolithic Microwave IC

Description

The CHV2240 is a monolithic multifunction proposed for frequency generation at 38GHz. It integrates a K-band Voltage Controlled Oscillator, a Q-band frequency multiplier and buffer amplifiers. For performance optimisation, an external port (ERC) allows a passive resonator coupling to the oscillator (at half output frequency). This chip has been especially designed to be coupled to a high Q dielectric resonator. All the active devices are internally self biased.
The circuit is manufactured with the pHEMT process 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is available in chip form.



Multifunction block diagram



Typical tuning characteristic

Main Features

- K-band VCO + Q-band frequency multiplier
- External resonator for centre frequency control and phase noise optimisation
- High quality oscillator when coupled to a dielectric resonator
- On-chip varactor for electronic control
- Chip size 2.68 x 1.4 x 0.1 mm

Main Characteristics

Tamb = +25°C

Symbol	Parameter	Min	Typ	Max	Unit
F_out	Output frequency	37.5	38.25	39	GHz
F_t	Frequency tuning range (high Q resonator)		5		MHz
Pn	Oscillator phase noise @ 100kHz (38GHz)		-100		dBc/Hz
Pout	Output power		9		dBm

ESD Protections : Electrostatic discharge sensitive device observe handling precautions !

United Monolithic Semiconductors S.A.S.
Route Departementale 128 - B.P.46 - 91401 Orsay Cedex France
Tel. : +33 (0)1 69 33 03 08 - Fax : +33 (0)1 69 33 03 09

Electrical Characteristics

Full temperature range, used according to section "Typical assembly and bias configuration"

Symbol	Parameter	Min	Typ	Max	Unit
F_out	Output frequency	37.5	38.25	39	GHz
F_osc	Oscillator frequency (1)		F_out/2		
F_stab	Frequency stability (1), (2)		4		ppm/°C
Pn	Phase noise @ 100kHz @ 38GHz (2)		-100		dBc/Hz
P_out	Output power	6	9		dBm
F_t	Frequency tuning range (2)		5		MHz
Vt	Voltage tuning range			0-2	V
I_vt	Tuning current			0.5	mA
VSWR_out	VSWR at output port		2:1		
+V	Positive supply voltage	4.4	4.5	4.6	V
+I	Positive supply current		120	180	mA
-V	Negative supply voltage	-4.6	-4.5	-4.4	V
-I	Negative supply current		3	10	mA
Top	Operating temperature range	-40		+100	°C

(1) The centre frequency is given by the external passive resonator
(2) This characteristic is obtained by using an external dielectric resonator (see section "Proposed External High Q resonator")

Absolute Maximum Ratings (1)

Tamb = +25°C

Symbol	Parameter	Values	Unit
P_erc	RF input power on ERC port (2)	13	dBm
+V	Positive supply voltage	5	V
-V	Negative supply voltage	-5	V
+I	Positive supply current	200	mA
-I	Negative supply current	10	mA
Top	Operating temperature range	-40 to +100	°C
Tstg	Storage temperature range	-55 to +155	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) Duration < 1s

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Appendix E

Hittite HMC-ALH445 LNA Specification Sheet

The following page contain the replication of the first page of the GaAs HEMT MMIC Low Noise Amplifier (part number: HMC-ALH445) specification sheet from Hittite Microwave Corporation [43].

HMC-ALH445

GaAs HEMT MMIC LOW NOISE AMPLIFIER, 18 - 40 GHz

Typical Applications

This HMC-ALH445 is ideal for:

- Wideband Communication Systems
- Point-to-Point Radios
- Point-to-Multi-Point Radios
- Military & Space
- Test Instrumentation

Features

Noise Figure: 3.9 dB @ 28 GHz

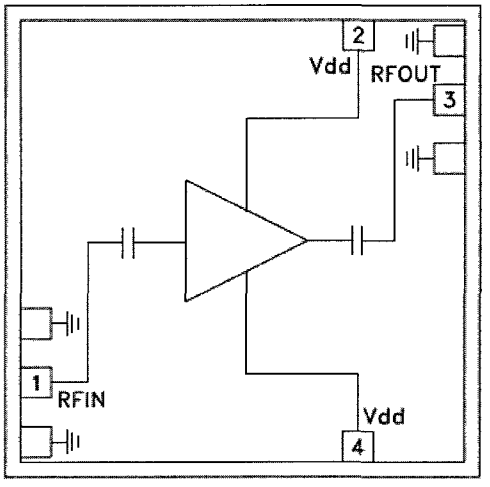
Gain: 9 dB

P1dB Output Power: +12 dBm @ 28 GHz

Supply Voltage: +5V @ 45 mA

Die Size: 1.6 x 1.6 x 0.1 mm

Functional Diagram



General Description

The HMC-ALH445 is a GaAs MMIC HEMT self-biased, wideband Low Noise Amplifier die which operates between 18 and 40 GHz. The amplifier provides 9 dB of gain, 3.9 dB noise figure at 28 GHz and +12 dBm of output power at 1 dB gain compression while requiring only 45 mA from a single +5V supply. The HMC-ALH445 amplifier is ideal for integration into Multi-Chip-Modules (MCMs) due to its small size.

Electrical Specifications*, T_A = +25° C, Vdd= +5V

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range		18 - 28			28 - 40		GHz
Gain	8	9		8	10		dB
Noise Figure		4	5		3.9	4.5	dB
Input Return Loss		10			10		dB
Output Return Loss		15			15		dB
Output Power for 1 dB Compression		12			13		dBm
Supply Current (Idd) (Vdd = 5V)		45			45		mA

*Unless otherwise indicated, all measurements are from probed die

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