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Tunable, Linear, G_m -C Filters

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B.Eng.(Electrical Engineering)

A thesis submitted to
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In partial fulfillment of
The requirements for the degree of

Master of Applied Science

In

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Acceptance of the thesis

Tunable, Linear, G_m -C Filters

Submitted by

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In partial fulfillment of

The requirements for the degree of
Master of Applied Science

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Abstract

The design of a tunable CMOS G_m -C second-order IF filter for applications in mobile radio is presented in this thesis. The work is part of a study aimed towards the implementation of an "integrated single-chip" radio. The objective of this work is to design an integrated bandpass filter capable of operation in the intermediate frequency (300MHz) range with high linearity, tunability and low power consumption. The filter is based on a tunable G_m -C integrator which is the main unit of the filter. Several control voltages are employed to tune the Quality factor (Q) and the centre frequency of the filter.

Three different types of G_m -C integrators are used to study and compare the linearity of the integrator circuits. The first one is a passive resistor-based source degeneration differential integrator which has good linearity. The second integrator circuit is designed in an attempt to improve the linearity by adding a feedback amplifier. Because neither circuit is tunable, the third tunable integrator which has reasonably good linearity is implemented.

A second-order bandpass filter based on the third tunable integrator was built. The filter demonstrated a frequency tuning range from 150MHz - 310MHz and Q tuning range of 3 to 10. Experimental measurements were in agreement with Cadence Hspice and SpectreRF simulation results, and illustrate the importance of properly modeling the test setup and measurement method of the circuit.

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List of Symbols

Amplifier

Antenna

Capacitor

Current Source

DC Power Terminal

Differential Transconductor

Differential Operational Amplifier

Filter

Ground Terminal

Mixer

N-Channel MOSFET

Operational Amplifier

P-Channel MOSFET

Resistor

Voltage Source

Abbreviations

ac		Alternating Current
BPF		Bandpass Filter
CCVS		Current Control Voltage Source
CMC		Canadian Microelectronics Corporation
CMOS		Complementary Metal Oxide Semiconductor
dB		decibel
FM		Frequency Modulation
GaAs		Gallium Arsenide
GHz		Giga-Hertz
G_m -C		Transconductor-Capacitor
IC		Integrated Circuit
IF		Intermediate Frequency
LNA		Low-Noise Amplifier
LO		Local Oscillator
MHz		Mega-Hertz
Q		Quality Factor, Ratio of Center Frequency to 3dB Bandwidth
RF		Radio Frequency
SAW		Surface Acoustic Wave
VCCS		Voltage-Controlled Current Source
VLSI		Very Large Scale Integration

CHAPTER 1

Introduction

Recent portable wireless communication systems require many complex transceiver components. Many design techniques have been proposed for monolithic filters as they are key components of transceiver systems. Since cost, reliability, performance, size and power consumption are main concerns of these components, they should ideally be realized as integrated circuits wherever possible. However, due to high frequency, RF filters are often discrete components. In the design of high-performance electronic circuits for the IF stage with low cost and low power consumption for high-speed applications, analog filters are preferred. At baseband, filters are mostly digital which will not be discussed in this thesis. On the whole, filters can appear in three places:

- (1) RF stage: RF filters are mostly discrete components.
- (2) IF stage: IF filters are analog integrated components.
- (3) Baseband: Digital filters are typically applied.

Among analog filters, continuous-time filters offer many advantages over analog discrete-time filters such as switched-capacitor and switched-current filters. The design of analog continuous-time filters is full of trade offs such as: component matching, high speed performance, high linearity, low-power dissipation, frequency tuning and Q tuning. If speed and low power consumption are considered to be the most important priorities, the transconductance-C filter is a good choice as it uses an integrator built from an open-loop transconductance amplifier with a capacitive load. Recent work on transconductance-C filters in CMOS technology has demonstrated feasibility in the range from 500 kHz to 450 MHz. [1][2][3]. Because of its simple structure the integrator can be fast, but it should not be expected to be very linear due to its open-loop nature. In the literature, few examples of research can be found on the linearity limitations of the transconductance-C integrator. Thus, linearity limits of the integrator should be analysed.

Due to process variations, temperature variations, power supply variations and parasitic effects, tuning is essential. One way to achieve tuning is to add an extra multiplier at the output of the transconductance filter. This allows for the design of a transconductor with high linearity and maximum tunability, however it has higher power consumption and requires more chip space than a tunable transconductor which is another way to achieve tuning without adding extra circuitry.

In this thesis, the design of analog transconductance filters aimed at the IF stage of a radio will be explored. Issues such as tunability and linearity will be examined.

1.1 Thesis Goals

This research sets out to design a completely integrated CMOS tunable band pass filter working around 150MHz - 310 MHz. Currently there are few reported examples of this type of fully integrated CMOS filter. The main goals in the research will be to consider the trade-offs between speed, linearity, tunability and low power consumption in an effort to achieve the requirements.

It is hoped that this research will help to achieve a high level integrated tunable bandpass filter as part of the RF front end, which would open up possibilities for new integrated wireless communication circuits.

1.2 Thesis Outline

This thesis is organized as followed. The background and theory of analog filters will be reviewed in Chapter 2. Fully differential circuits are introduced, and design considerations for transconductance-C integrators are discussed. In Chapter 3, the analysis of the linearity limits of the designed integrators are discussed, followed by a description of the designed bandpass filter circuit including simulation results. Chapter 4 presents the circuit layout, the experimental setup and the measurement results for the G_m -C based bandpass filter. Finally, Chapter 5 presents conclusions and provides suggestions for further study.

CHAPTER 2

Overview and Theory of Filters

In this chapter the general background of a classical radio receiver and its components are presented followed by an overview of how filters are employed in a receiver system. In the filter overview, different types of filters are described with a focus on CMOS transconductance-C filters and recent papers which describe them and other similar filters.

There are many characteristics of analog components that affect the behaviour of the overall receiver so their consideration is very important during the analog design procedure. The three main characteristics of interest are: linearity of the devices, speed-performance, and noise figure, all of which have major effects on the quality of the processed analog signal. These characteristics lead to conflicting design requirements. Thus the design of an optimum analog component will be a compromise between the individual characteristics.

2.1 Overview of a Radio Receiver

A generalized block diagram of a heterodyne down-conversion radio receiver is shown in Figure 2.1[4]. This type of receiver design is typically used to provide good signal to noise ratio and channel isolation for an RF input which varies widely in signal strength, and which might contain adjacent channel interference.

The RF signal enters the system at the antenna and is then amplified by the LNA (low noise amplifier) after the out-of-band signals have been removed by the RF filter. The main function of the LNA is to provide enough gain to overcome the noise of the following stages such as the image rejection filter and the mixer. Moreover, the LNA should add minimum noise as noise introduced by the LNA has a large effect of the overall noise

Figure 2.1 Block Diagram Of A Typical Radio Receiver.

performance of the receiver. It should also accommodate large signals without distortion or, equivalently, it should have good linearity. The design of the LNA is a trade-off between optimum gain, low noise figure, high linearity, low power consumption and optimum input and output matching. At the output of the LNA is an image reject filter whose function is to suppress any noise or signals present at the image frequency. The image reject filter's output should match to the input of the mixer for optimum power gain.

After amplification of the received signals by the LNA, both the desired signal and noise are translated down to a fixed intermediate frequency (IF) by a mixer utilizing a Local Oscillator (LO) as illustrated in Figure 2.2. The mixer has system requirements such as good conversion gain, low noise figure, low power consumption and high linearity. An integrated silicon implementation of the mixer may help to reduce the overall power consumption compared to a passive diode mixer. For example, if both the LO and mixer are on chip, the impedance levels may be higher which reduces the required LO power drive and improves the mixer's conversion gain. But, this may be at the expense of higher noise figure and lower linearity.

A high-Q filter is employed at the output of the mixer to remove out of band interfer-

Figure 2.2 Signal Spectrum Moving Through The Receiver.

ence (IF filters). Different types of filters, such as Surface Acoustic Wave (SAW), crystal, or active tuned filters, will be discussed in detail in the following sections. The output of the IF filter is further processed, either by a demodulation block where information is extracted from the IF signal, or by an A/D converter.

2.2 Filter Overview

Modern communication systems, such as radio, TV and telephone, contain various types of filters. In general, the filters can be divided into two types: passive filters and active filters. From 1920 to the late 1960s, most filters were made of passive components such as resistors, capacitors and inductors. Passive LC-ladder filters are a useful heritage of those days since it was discovered that they were highly insensitive to component variations [5]. In the 1950s it was recognized that both size and cost could be reduced by replacing the large and costly passive inductors with active circuitry. In the mid 1960s high-quality active components such as operational amplifiers became economically available. When active RC filters became very popular in the mid 1970s, system integration came into fashion and fully integrated filters in a compatible technology became desired [6].

Over the last two decades, active integrated filters have become increasingly important

for many signal processing applications. In such circuits the active components are integrated monolithically (i.e. on a single chip). These filters have several advantages over active filters built with discrete components including: reduction of the number of components in a system, simplification of design due to the good matching of components on chip, possibility of automatic tuning circuitry which could reduce the errors from process and temperature variations, reduction of parasitic capacitance on chip compared to discrete passive filters, low-cost when these filters are fabricated in large numbers.

Filters have to be interfaced with other components and in the case of the RF or IF filter, with the analog world. Analog filters can do this directly. In the baseband, digital filters can directly interface with signal processing circuitry, however in the IF stage, the filter input would be an analog signal and needs to be conditioned by an analog filter before being digitized. Part of the IF filtering could be moved to the baseband, but some analog filtering must remain at the IF stage. For this reason, digital filtering will not be considered in this thesis.

The different types of monolithic active filters can be distinguished as shown in Figure 2.3. The design trend of most of these circuits is to scale down the dimensions of the transistors so as to incorporate in a single chip as many building blocks as possible. These specifications can only be achieved with IC realizations.

Typically, the available technologies for integrated circuits are Complementary-Metal-Oxide-Semiconductor (CMOS), Bipolar, Bipolar-CMOS (BICMOS), Gallium-Arsenide (GaAs) and Surface Acoustic Wave (SAW). Each one of these has advantages and drawbacks. For example: commonly used SAW filters have the advantages of high selectivity (Q values from 2×10^3 to 2×10^4) [8], and high speed performance (centre frequency runs from 30MHz to a few GHz) [9]. Their main disadvantage is size: approximately 0.25cm^2 for GHz filters and 1.0cm^2 for filters near 50 MHz, package heights tend to be 3-

Figure 2.3 Classifications Of Active Filters.

10 mm² or more, almost independent of the chip thickness. CMOS technology is the most popular technology due to its higher circuit density, low cost and maturity.

2.3 CMOS Analog Filters

In CMOS technologies, analog filter design techniques can be divided into analog discrete-time and continuous-time techniques. Switched-Capacitor and Switched-Current filters both use discrete-time techniques. RC active filters, MOSFET-C filters and Gm-C filters can be classified together as continuous-time techniques.

2.3.1. Discrete-time Filters.

Analog discrete-time filters also process signals of discrete-time nature. The techniques for realizing this type of filters are: switched-current filters [10], charge-coupled device filters [11], [12] and switched-capacitor filters [13], [14]. Switched-capacitor filters are the most popular of these filters. Most applications of switched-capacitor filters can be found

ranging from the audio frequency band [15] to video frequencies [16], [17] and beyond [18]. The main characteristics of switched-capacitor filters are determined by a clock frequency and by capacitor ratios. Both parameters, clock frequency and capacitor ratios, are independent of process and temperature variations. Hence, a major advantage of this technique is the high accuracy of its integrator time constant which can be as good as 0.1% [18]. Therefore, the use of additional tuning circuits is avoided. Unfortunately, these advantages are not necessarily maintained for high-frequency applications. Because switched capacitor filters require sampling in the time domain, the clock rate must always be at least twice that of the highest frequency being processed to eliminate aliasing. In fact, typically the clock rate is much greater than twice the signal bandwidth, to reduce the requirements of an anti-aliasing filter and to allow complete settling of sampling transients. As a result, switched-capacitor filters are limited in their ability to process high-frequency signals. A typical switched capacitor circuit is shown in Figure 2.4.

Figure 2.4 A First-Order Switched Capacitor Filter: (a) Circuit, (b) Switch symbol.

The switched-current technique has been introduced recently [19], [20]. The operation of these filters are similar to these of switched-capacitor filters, but instead of charge packages switched-current filters, it drives current packages. Thus, the transfer function de-

depends on both clock frequency and current source ratios. These parameters are almost independent of process variations and temperature variations and can be accurate to within 1% [20]. This makes the use of additional tuning circuits unnecessary. Due to the absence of operational amplifiers (opamps) this type of filter can be faster than the switched-capacitor variety. However, there are several practical limitations. A major drawback of this technique is clock feed through. Clock feed through reduces the accuracy of the filter and increases both noise level and distortion [20]. Lastly, a linear voltage-to-current transducer is required at the input of the filters.

On the whole, it can be said that discrete-time filters need an antialiasing continuous-time filter to band-limit the frequencies of the input signal. Due to sampling, high-frequency noise can be aliased into the base band, further increasing the in-band noise level. This effect reduces the filter dynamic range drastically. Another filtering technique which avoids some of the above disadvantages is the continuous-time filtering technique.

2.3.2. Continuous-time Filters.

Analog continuous-time filters directly process analog signals without the need for AD and DA converters, sampling, holding, or anti-aliasing filters. Owing to their continuous-time nature, these filters are an alternative to sampled-data filters in high-frequency applications. Currently, integrated continuous-time filters can reach hundreds of MHz [22]-[26]. The precision of these filters is in the range of 30%-50% [21] which is the major disadvantage of continuous-time filters. Fortunately, with an on-chip self tuning system, filter coefficients can be set to an accuracy of about 1% [27] with the penalty of more complex circuitry.

For the design of high-performance CMOS active filters, there are three main types of continuous-time filters: RC active filters, MOSFET-C filters and Transconductance-C filters.

RC active filters consist of opamps, resistors and capacitors as basic elements. In integrated circuits, the resistors can be implemented either as diffused or poly-silicon resistors. The accuracy of these filters are limited, and can be as poor as 50%. This is because the filters are sensitive to variations of the RC product which is a strong function of both technology tolerances and temperature variations. But, they can be improved by adding certain kinds of tuning, either on chip or externally. The active RC filter is mostly used in low-frequency applications often for reasons related to the technology, for example, the resistors are implemented in long strips over field oxide or over active areas. As a result there is a distributed capacitance connected to the resistor. These distributed capacitors limit both the precision and the high-frequency performance of the filter. A technique which uses discrete capacitor banks to improve the precision of these filters has been proposed [28]-[30]. Its accuracy is limited by the resolution of the banks, e.g. an accuracy of 5%. However, this technique is not discussed in this thesis.

MOSFET-C filters are basically active RC filters but with the resistors implemented with an equivalent CMOS tunable transistor biased in the triode region [29]. The most important problem is distortion, which can be diminished by using a transistor array instead of a single transistor [31]. Because of the use of transistors as simulated resistors, small output impedance opamps should be employed, which means multi-stage opamps are needed. The limited frequency response of opamps with two or more stages and of MOS transistors biased in the linear region limits their use to low-frequency applications. Example applications of these filters have been in the design of antialiasing and smoothing filters at frequencies less than 100KHz [29], [32].

Transconductance-C (G_m -C) filters have been widely adopted for high frequency applications such as digital video, IF filters, etc. with frequency ranges from a few kHz to several hundred MHz, [22], [24], [25], [26], [33], [34]. The basic building block of G_m -C filters is a voltage-to-current transconductance (G_m) loaded with a capacitor (C). G_m -C fil-

ters offer many advantages over other continuous-time filters previously discussed. Compared to RC active and MOSFET-C filters, they have lower power and higher frequency capability. Because G_m -C filters use an integrator built from an open-loop transconductance amplifier driving a capacitive load they can be very fast compared to the other two continuous-time integrators. The three types of integrators are shown in Figure 2.5.

Figure 2.5 Continuous-Time Integrators: (a) RC Active (b) MOSFET-C (c) G_m -C.

Recently, G_m -C based filters with resonant frequencies in the range of several hundreds of MHz have been reported [1], [25]. A comparison of the useful frequency range for both OPAMP and G_m based circuits is shown in Figure 2.6 [35].

In [36] 30 dB of opamp gain was taken as the minimum requirement for well behaved opamp-based circuits. If the gain is less than 30 dB the GBW (Gain Bandwidth) effects of the opamp degrades the characteristics of the system. For a single pole opamp, this implies a useful frequency range of the order of $GBW/30$. This fact makes it extremely difficult to design high-frequency opamp based filters. Due to the open-loop nature of G_m -C filters, the useful frequency range of these circuits is limited only by the G_m -C gain-bandwidth product as seen in Figure 2.6. Thus, even though the GBW of the G_m -C integrator may be

Figure 2.6 Useful Frequency Range For A Single Pole Opamp And G_m -C.

lower than that of the opamp, the G_m -C filters can operate to higher frequency so it is a good option for filter design.

One major drawback of G_m -C filters is poor linearity due to their open-loop nature. The linearity level of these filters is determined mostly by the voltage-current transconductors. However, due to process variations, temperature variations and component mismatching, reported harmonic distortion components were of the order of -40dB for input signals up to 1 Volt [36]-[37]. To reduce the effects of process variations, an additional tuning system is necessary. The techniques used to improve linearity and to design the tuning system require careful consideration when designing G_m -C filters.

2.4 Transconductance-C Integrators

A G_m -C integrator is the main building block for G_m -C filters. It is made up of a transconductor and a load capacitor as shown in Figure 2.7. A transconductor is essentially a transconductance cell (an input voltage creates an output current) with the requirement that the output current is linearly related to the input voltage by

$$i_o = g_m \cdot v_i \quad (2.1)$$

where g_m is the transconductance of the cell. This output current i_O is applied to the integrating poly-silicon capacitor, C_L , resulting in the voltage across C_L being given by

$$v_o = \frac{i_o}{s \cdot C_L} = \frac{g_m \cdot v_i}{s \cdot C_L} \quad (2.2)$$

The integrator unity-gain frequency ω_t can be found to be

$$\omega_t = \frac{g_m}{C_L} \quad (2.3)$$

Thus, we can write

$$v_o = \frac{v_i \cdot \omega_t}{s} \quad (2.4)$$

From the expression for ω_t it can be seen that integrator's frequency can be tuned by var-

Figure 2.7 A Single-Ended G_m -C Integrator.

ying the value of transconductance. The G_m -C integrator has several advantages as discussed before, but, its major drawback is the lack of a very linear and efficient voltage-to-current transconductor. The aim of this thesis is to design a high frequency tunable G_m -C filter with low nonlinear distortion. The filter should have a frequency tuning range of 150 MHz to 300 MHz, this allows the filter to operate within the frequency range requirement as well as compensate for process and temperature variations. To achieve a highly linear

G_m -C IF filter, an understanding of distortion mechanisms is very important. This will be discussed in Section 2.4.2.

2.4.1 Sources of Noise

The performance of G_m -C filters is limited by noise which is an example of an unwanted signal. Such noise is generated from a variety of electrical devices and the various noise sources are uncorrelated. This implies that noise is unwanted, but special and careful design techniques can minimize the overall noise of the system. In general, there are two types of noise:

- (1) device noise generated by itself. Noise generated by the device itself is generally due to the discrete nature of the current flowing through the transistors and also due to the imperfections of the transistor interface. e.g. silicon-silicon oxide interface. In CMOS transistors, there are two dominant noise sources, namely, channel thermal noise and $1/f$ or flicker noise.
- (2) unwanted signals generated due to the coupling of the device to the surrounding circuit. The coupling is due to the finite impedance of the power-supply sources and to the coupling capacitors in the chip, namely: bulk capacitors, metal-metal capacitors, etc.

Thermal noise is due to the random motion of electrons in a resistive material, and is proportional to the resistance and temperature of the material. For a CMOS transistor, the channel acts like a resistor controlled by the gate-source voltage. Thus, the random flow of the carriers produces thermal noise. It can be demonstrated that the spectral density of thermal noise current in the drain of a CMOS transistor biased in the triode region, $v_{DS} < v_{GS} - V_{th}$, is approximated by [38]

$$i_{Dn}^2 = \frac{8}{3} kT \mu C_{ox} \frac{W}{L} \left(\frac{3(v_{GS} - V_{th})v_{DS} - \left(3(v_{GS} - V_{th})^2\right) - v_{DS}^2}{2(v_{GS} - V_{th}) - v_{DS}} \right)$$

(2.5)

where k , T , μ and C_{ox} are Boltzmann constant, temperature (in Kelvin), channel mobility and gate capacitance per unit of gate area, respectively. W and L are the width and length of the transistor gate. In the linear region the voltage V_{ds} is very small and can be neglected. so, the thermal noise is approximated by:

$$i_{Dn}^2 = 4kT \left(\mu C_{ox} \frac{W}{L} (v_{GS} - V_{th}) \right) = 4kT g_m \quad (2.6)$$

where g_m is the small-signal conductance of the transistor. Thermal noise is modeled as a current source for a MOSFET transistor as illustrated in Figure 2.8.

Figure 2.8 Thermal And 1/f Noise Model For a MOSFET In Saturation Region.

In the saturation region, $v_{DS} > v_{GS} - V_{th}$, the noise can be calculated from (2.7):

$$i_{Dn}^2 = \frac{8}{3} kT g_m \quad (2.7)$$

This type of noise is often called White noise or Gaussian noise [39].

1/f noise (flicker noise). 1/f noise is a low-frequency phenomenon which occurs in all active devices and some passive elements. 1/f noise in a MOSFET transistor is caused mainly by the surface states and traps in the silicon-silicon oxide interface randomly interfering with charge flowing through the channel. Thus, 1/f noise is strongly dependent on the technology. The technology dependence of flicker noise is commonly expressed as a

constant K_f which is a fitting parameter. The spectral density of the $1/f$ noise drain current is characterized in the form [38]

$$i_{Dn}^2 = \frac{K_f \cdot I_{DS}}{C_{ox} \cdot L^2 \cdot f} \quad (2.8)$$

where I_{DS} is the bias drain current, f is the frequency in Hertz. The flicker noise spectral density is usually expressed as an input referred spectral noise voltage and is shown in Figure 2.8. This is useful as it allows the comparison of the input signal with the noise of the system. The input referred spectral density of the noise of a MOSFET can be calculated from:

$$v_{Gn}^2 = \frac{i_{Dn}^2}{g_m^2} = \frac{i_{Dn}^2}{\left(\mu \cdot C_{ox} \cdot \frac{W}{L}\right)^2 \cdot (v_{Gs} - V_{th})^2} = \frac{K_f}{\mu \cdot C_{ox}^2 \cdot WLf} \quad (2.9)$$

with i_{Dn}^2 characterized by equation (2.8). Larger MOSFETs have a larger gate capacitance which serves to reduce charge fluctuations in the channel due to charge trapping. Thus $1/f$ noise is inversely proportional to the gate dimensions.

The second type of noise is due to the coupling of the device to the surrounding circuitry. The coupling is because of power-supply source impedance and coupling capacitors on the chip, namely, bulk capacitors and metal-metal capacitors. The noise generated in the power supply and V_{ss} will interfere with the wanted signals. Fortunately by using fully differential circuits such noise can be minimized.

2.4.2 Distortion

Distortion is a result of the intrinsic nonlinearities of electronic devices. Unwanted signals are generated due to the nonlinear nature of the relationship between the input and the output signal. If only one simple sinusoidal signal is applied at the input, the unwanted out-

put noise or signals are at multiples of the input signal frequency. Such noise is called harmonic distortion of the output signal and is typically measured as the Total Harmonic Distortion (THD). The THD is the RMS value of the contribution of all the harmonic distortion and will be discussed in detail later on. If two or more signals with different frequencies are applied at the input, sum frequencies and difference frequencies are generated at the output of the circuit. This is called Intermodulation Distortion (IM). For narrowband systems, intermodulation distortion is the main limitation of the system for large signals.

Harmonic distortion can be determined in the case of an applied simple sinusoidal input. The output current of the single-ended G_m integrator shown in Figure 2.9 can be expanded in Taylor series around the quiescent operating point (V_Q, I_Q):

Figure 2.9 G_m Integrator Nonlinear System.

$$i_o = k_1 v_i + k_2 v_i^2 + k_3 v_i^3 + \dots \quad (2.10)$$

where $K_{1,2,3,\dots}$ are constant terms. The coefficient k_1 is the linear term and the higher-order coefficients, $k_2, k_3, \dots$, represent nonlinear distortion terms. With a simple sinusoidal signal as the input for example, $v_i = v_p \cdot \cos \omega t$, the corresponding output current is:

$$i_o = k_1 \cdot v_p \cdot \cos \omega t + \frac{1}{2} k_2 \cdot v_p^2 \cdot (1 + \cos 2\omega t)$$

$$+ \frac{1}{4}k_3 \cdot v_p^3 \cdot (3 \cos \omega t + \cos 3\omega t) + \dots \quad (2.11)$$

Collecting corresponding cosine terms, we get:

$$\begin{aligned} i_o = & \left(\frac{1}{2}k_2 v_p^2 + \dots \right) + \left(k_1 + \frac{3}{4}k_3 v_p^2 + \dots \right) v_p \cos \omega t \\ & + \left(\frac{1}{2}k_2 + \dots \right) v_p^2 \cos 2\omega t + \left(\frac{1}{4}k_3 + \dots \right) v_p^3 \cos 3\omega t + \dots \end{aligned} \quad (2.12)$$

For quasilinear systems, the power series terms converge rapidly and coefficients above k_3 can be ignored. Then (2.12) becomes:

$$\begin{aligned} i_o = & \frac{1}{2}k_2 v_p^2 + \left(k_1 + \frac{3}{4}k_3 v_p^2 \right) v_p \cos \omega t \\ & + \frac{1}{2}k_2 v_p^2 \cos 2\omega t + \frac{1}{4}k_3 v_p^3 \cos 3\omega t \end{aligned} \quad (2.13)$$

For small input where $\frac{3}{4}k_3 v_p^2 \ll k_1$, the approximation can be obtained:

$$i_o = k_1 v_p \cos \omega t + \frac{1}{2}k_2 v_p^2 \cos 2\omega t + \frac{1}{4}k_3 v_p^3 \cos 3\omega t \quad (2.14)$$

The integrator's Harmonic Distortion is defined as the ratio of the output signal amplitudes at frequencies $2\omega, 3\omega, \dots$ to the linear output:

$$\begin{aligned} HD_2 &= \frac{\text{Signal} \cdot \text{Amplitude} \cdot \text{at} \cdot 2\omega}{\text{Signal} \cdot \text{Amplitude} \cdot \text{at} \cdot \text{Fundamental}} \approx \frac{1}{2} \frac{k_2}{k_1} v_p \\ HD_3 &= \frac{\text{Signal} \cdot \text{Amplitude} \cdot \text{at} \cdot 3\omega}{\text{Signal} \cdot \text{Amplitude} \cdot \text{at} \cdot \text{Fundamental}} \approx \frac{1}{4} \frac{k_3}{k_1} v_p^2 \end{aligned} \quad (2.15)$$

$$THD = \sqrt{HD_2^2} + \sqrt{HD_3^2} + \sqrt{HD_4^2} + \dots \quad (2.16)$$

Higher order terms are defined similarly. The total harmonic distortion (THD) is defined

as the root-mean-square (RMS) sum of all harmonic distortion components. It is an important parameter to determine the linearity of the circuit. From equation (2.16), the distortion products at the output for a prescribed sinusoidal input can be readily estimated with a given power series expansion.

Intermodulation distortion. The output spectrum of a nonlinear system exhibits more spectral components for multiple sinusoidal input signals. Let the system input consist of two cosines at different frequencies ω_1 and ω_2 : $v_i = v_{p1} \cos \omega_1 t + v_{p2} \cos \omega_2 t$. As an intermediate step we need to find v_i^2 :

$$\begin{aligned} v_i^2 = & \frac{1}{2} (v_{p1}^2 + v_{p2}^2) + \frac{1}{2} v_{p1}^2 \cos 2\omega_1 t + \frac{1}{2} v_{p2}^2 \cos 2\omega_2 t \\ & + v_{p1} v_{p2} \cos(\omega_1 + \omega_2)t + v_{p1} v_{p2} \cos(\omega_1 - \omega_2)t \end{aligned} \quad (2.17)$$

To find an expression for third order distortion, we need to find v_i^3 :

$$\begin{aligned} v_i^3 = & \frac{3}{4} (v_{p1}^3 + 2v_{p1} v_{p2}^2) \cos \omega_1 t + \frac{3}{4} (v_{p2}^3 + 2v_{p2} v_{p1}^2) \cos \omega_2 t \\ & + \frac{1}{4} v_{p1}^3 \cos 3\omega_1 t + \frac{1}{4} v_{p2}^3 \cos 3\omega_2 t \\ & + \frac{3}{4} v_{p1}^2 v_{p2} [\cos(2\omega_1 + \omega_2)t + \cos(2\omega_1 - \omega_2)t] \\ & + \frac{3}{4} v_{p2}^2 v_{p1} [\cos(2\omega_2 + \omega_1)t + \cos(2\omega_2 - \omega_1)t] \end{aligned} \quad (2.18)$$

To simplify the expressions for intermodulation distortion, a two-tone input with $v_{p1}=v_{p2}=v_p$ is usually considered. The third-order intermodulation distortion IM3 is defined by the ratio of the system output component at frequencies at $2\omega_2 \pm \omega_1$ and $2\omega_1 \pm \omega_2$ to the component at ω_1 or ω_2 . Substituting (2.17),(2.18) into (2.10) and simplifying produces normalized third-order intermodulation distortion:

$$IM_3 = \frac{3k_3}{4k_1} v_p^2 \quad (2.19)$$

By comparing of (2.19) with (2.15) we get:

$$IM_3 = 3HD_3 \quad (2.20)$$

From (2.19) it can be predicted that as input signal v_p rises, third-order intermodulation distortion rises, eventually swamping the linear output tone as shown in Figure 2.10. The

Figure 2.10 The Third-Order Distortion Intercept Point.

value of v_p where the intermodulation-distortion products extrapolate to equal the extrapolated linear output magnitude is called the 3rd order distortion intercept point (IP_3) and is a normalized measure of a circuit's non linearity. By setting the magnitude of IM_3 equal to unity in (2.19), we get:

$$IP_3 = \left| \frac{4k_1}{3k_3} \right|^{\frac{1}{2}} \quad (2.21)$$

From the distortion intercept point, the magnitude of a system's output distortion products for any small two-tone input amplitude v_p can be determined. (2.19) can be expressed in the form:

$$|IM_3| = \left(\frac{v_p}{IP_3} \right)^2 \quad (2.22)$$

$$|IM_3|_{dB} = 2(|v_p|_{dB} - |IP_3|_{dB}) \quad (2.23)$$

Thus, to keep the circuit's IM_3 below -40dB, the input tones must be kept at least 20dB below the IP_3 . Conversely, if IM_3 is measured to be -40dB for a given input v_p , then IP_3 is determined to be 20dB above this input level. Thus IP_3 defines the linearity of the circuit.

2.5 Fully Differential G_m -C Integrators

In most analog applications it is desirable to keep the signal fully differential, which implies that only the difference in voltage or current between two halves of the circuit, represents the signal. Therefore, any noise which is common to both sides of the circuit (common-mode) will not affect the differential signal. Fully differential circuits ideally consist of a well balanced circuit with differential signals operating symmetrically around a common-mode voltage. Most noise such as power supply noise and V_{ss} noise appears equally on both sides of a differential circuit such that it doesn't affect the differential output signal. Another major benefit of using differential circuits is that the differential output signal will have only odd-order distortion. The cancellation of second order products is demonstrated in Figure 2.11 under the assumption that the nonlinear elements are identical, and for simplicity, the common-mode voltage is zero. The output of the circuit in figure 2.11 is obtained as a Taylor series expansion given by:

$$v_o = k_1 v_i + k_2 v_i^2 + k_3 v_i^3 + k_4 v_i^4 + \dots \quad (2.24)$$

where k_i are constant terms. In this case, the differential output v_o , consists of only the odd-order distortion terms, which are often much smaller than the second-order term [27], and

Figure 2.11 The Distortion Improvement In Fully Differential Circuit.

the linear term. With these two important advantages over single-ended circuits, fully differential G_m -C integrators should be considered when designing G_m -C filters. In the following sections, both advantages and drawbacks of some reported fully differential G_m -C integrators will be discussed. The major design problems of these integrators are described in section 2.5.1.

2.5.1 Fully Differential Topologies

The most well known and widely used design for differential transconductors is the source-coupled transistor pair shown in Figure 2.12, with the MOSFETs operating in the saturation region, the transconductance of the differential pairs is:

$$g_m = \frac{2i}{v_{id}} = \frac{dI_Q}{d(V_{GS} - V_{tn})} = \sqrt{2KI_Q} \quad (2.25)$$

where g_m is transconductance of each transistor, $v_{id} = v_{IN}^+ - v_{IN}^-$ and i is the ac current, $K = \mu_{n,p} \cdot C_{ox} \cdot \frac{W}{L}$. It is evident that the transconductance of the circuit can be set and tuned via the bias current I_Q . Because the transconductance of the circuit is proportional to the square-root of I_Q , a drawback of this circuit is that a large bias current change results in a smaller transconductance change. Moreover, linearity of the circuit cannot be expected to be good.

The distortion of the circuit can be determined by:

$$\frac{v_{id}}{V_{eff}} = \sqrt{1 + \frac{i}{I_Q}} - \sqrt{1 - \frac{i}{I_Q}} \quad (2.26)$$

$$= \frac{i}{I_Q} + \frac{1}{8} \left(\frac{i}{I_Q} \right)^3 + \dots \quad (2.27)$$

where $V_{eff} = V_{GS} - V_{tn} = \sqrt{2I_Q/K}$. V_{eff} is the effective dc gate bias of each MOSFET. From equation (2.15), we get:

$$HD_3 = -\frac{1}{32} \left(\frac{i_p}{I_Q} \right)^2 \quad (2.28)$$

where i_p is the peak value of i .

Figure 2.12 Source-Coupled Differential Pairs.

The distortion performance of this elementary circuit can be improved by increasing the quiescent current I_Q , but the penalty is power consumption. Furthermore, since the circuit transconductance varies with I_Q , increasing bias current will result in an increase of g_m . As a result, in order to maintain a prescribed unity frequency, from equation (2.3), the

capacitors in the circuit would have to be made larger to accommodate this increased transconductance.

Resistor degeneration can be used to reduce distortion as shown in Figure 2.13, where increased linearity can be obtained with increased resistors value. The circuit's transcon-

Figure 2.13 A Resistor Degenerated Differential Pair

ductance can be derived as [46]:

$$g_m = \frac{2i}{v_{id}} = \frac{I_Q/V_{eff}}{1 + (I_Q R)/V_{eff}} = \frac{\sqrt{2KI_Q}}{1 + R\sqrt{2KI_Q}} \quad (2.29)$$

when R is big enough and $I_Q R \gg V_{eff}$, $g_m \approx \frac{1}{R}$. In such a case, the transconductance can't be tuned any more. For this reason, there are two different ways to resolve this tuning problems: one technique is first to design a very linear but non-tunable transconductor, and then to connect to a multiplier style controller as shown in Figure 2.14. The drawback of this technique is that additional circuitry is needed. This results in higher power dissipation, more noise sources and greater chip area usage.

The other way of resolving the tuning problem is to use a tunable integrator, many examples of which have been proposed recently [22]-[26]. One particular transconductor

Figure 2.14 Block diagram of multi style G_m -C integrator.

shown in Figure 2.15, with improved linearity performance over the simple resistive source-degenerated pair was reported [3]. As shown below, this integrator is based on

Figure 2.15 Schematic Of Improved Linearity Integrator.

source-degeneration with a linear resistor. The tuning process can be accomplished by three transistors M_1 , M_2 and M_3 operating in the triode region. By choosing $2W/L(M_2, M_3) = W/L(M_1)$, the transconductance of the circuit can be tuned by the control voltages V_{C1} and V_{C2} at the gates of the three transistors. The transconductance, g_m , of the integrator can be calculated as:[3]

$$g_m = \left[\frac{1}{2} + \frac{V_{cd}}{2(V_{cm} - V_t - V_A)} \right] \frac{1}{R} = \alpha \frac{1}{R} \quad (2.30)$$

where $V_{cd} = (V_{C1} - V_{C2})/2$, $V_{cm} = (V_{C1} + V_{C2})/2$, V_A is the dc bias voltage at the node A, and V_t is the threshold voltage of the transistor M_1 . The linearity performance of the integrator is determined by the three tuning transistors. The output current is $i_o = I_d - I_1 = ((V_i - V_t)/R) - I_1$ as $I_d = (V_i - V_t)/R$ and I_1 is the current through M_1 transistor. If M_1 behaves as a linear resistor the integrating output current i_o is linearly proportional to V_{in} . Since the tuning transistor M_1 works in the triode region, the current flowing through it can be calculated as:

$$I_1 = \mu C_{ox} \frac{W}{L} \left[(V_{C2} - V_A - V_t)(V_B - V_A) - \frac{(V_B - V_A)^2}{2} \right] \quad (2.31)$$

where $V_B - V_A$ is the voltage across the tuning transistor M_1 . From equation (2.31) it can be derived that the transistor M_1 behaves as a linear resistor as long as the voltage V_A and V_B are differential [40]. In practice, due to nonlinearity V_A and V_B are not very differential for large signal, but, by using tuning transistors with large W/L ratios to keep the voltage swing across M_1 very small, the behaviour of M_1 approximates the behaviour of a linear resistor. This type of integrator based bandpass filter has been used for telecommunication applications, ranging from a few kHz to several hundreds kHz with centre frequencies ranging from 165-505 kHz [3]. To meet the requirements of other communication systems like video frequency receivers in the range of MHz to several hundreds of MHz, a high-frequency circuit is required. As the tuning is achieved by a tunable transistor acting as a

tunable resistor, it is important to examine the resistor's impact on tuning and linearity. In the following section the study and overview of MOSFET resistors will be discussed.

2.5.2 MOSFET Resistors Working In The Triode Region.

The MOSFET transistor, operating in the triode region, employed as a tunable resistor in the triode region is shown in Figure 2.16 [41], [42], [43]. The drain current flow through

Figure 2.16 The MOSFET Resistor Operating In Triode Region.

the MOSFET is given by:

$$i_d = \mu C_{ox} \frac{W}{L} \left[(V_{GS} - V_t)(V_D - V_S) - \frac{(V_D - V_S)^2}{2} \right] \quad (2.32)$$

All three terminals: drain, source, and gate are used to control drain-source current. In this case, the drain and the source are used as the resistor terminals and the tuning of the resistor i_d is carried out by the gate voltage. The resistance of the MOS transistor biased in the linear region is given by:

$$R_{ds} = \frac{1}{K(V_G - V_t - V_D)} = \frac{1}{K\left(V_G - V_t - \left(V_{CM} - \frac{V_{DS}}{2}\right)\right)} \cong \frac{1}{K(V_G - V_t - V_{CM})} \quad (2.33)$$

where $V_{CM} = (V_D + V_S)/2$ is the common-mode drain-source voltage, and $K = \mu C_{ox} \frac{W}{L}$. Typically, the resistance is controlled through the gate voltage. For low supply voltages, such as 3.3V, common-mode voltage is limited to around 1.65V which results in $V_G - V_{CM} - V_t \approx 0.95V$. The resistance can be tuned in the range of $[\frac{1}{K(V_{DD} - V_t)}, \infty]$ when $V_{CM} = 0V$ and $V_G - V_t - V_{CM} = 0$. However, a useful range can be calculated by assuming that $V_G = V_{DD}$, $V_{CM} = V_{DD}/4$ resulting in $V_G - V_{CM} - V_t \approx V_{DD}/2$ in this case, a $\pm 50\%$ tuning range can be obtained. This tuning range is high enough for most low-Q applications.

For the MOSFET based resistor, most of the even order nonlinearities can be reduced by subtraction using symmetrical structures. If the MOSFET transistor is connected to the output of a fully-differential circuit, ideally the even order nonlinearities cancel out. From equation (2.32) it can be shown that for fully differential output signals, $V_D = -V_S$, the third-harmonic distortion of the MOSFET transistor biased in the triode region is given by:[37]

$$HD3 = \frac{1}{4} \frac{k_3}{k_1} V_P^2 \approx \frac{1}{4} \frac{1}{(V_G - V_t - V_{CM})} \cdot V_{DS}^2 \quad (2.34)$$

From equations 2.33 and 2.34, it is clear that the resistance and the distortion of the MOS resistors are sensitive to V_{CM} . Hence the accuracy of the value of resistor is limited. This effect is present in all circuits based on this type of NMOS transistor. In these circuits, the dc offset voltage, (quiescent operation point) due to the common-mode voltage, plays a very important role in the accuracy of the system such as transconductor based circuits. Thus the study of common-mode feedback, which is a loop that determines the operation point of the system, is critical.

2.5.3 Common-Mode Feedback.

As mentioned before, the major advantage of fully-differential structures is that the signal is differential instead of being referred to ground. The major disadvantage of this technique is also associated with this fact. The common-mode voltage of the topology (quiescent operation point) cannot be stabilized by the differential output feedback. Thus, in order to define the common-mode voltage of the structure, additional circuitry has to be included. The loop that determines the operation point of the structure is the Common-Mode Feedback (CMFB). Common-mode loop is often the most difficult part of the opamp to design because the output signal is mainly differential and the common-mode signal must be detected as fast as possible with simple, fast and stable circuitry. The additional CMFB circuitry results in more silicon area use, a more complex layout and more power consumption. Furthermore, harmonic distortion generated in this loop can introduce additional distortion in the whole circuit.

One way to stabilize the common-mode signal is by applying a feedback circuit at the output of the Transconductance-C integrator as shown in Figure 2.17. A typical implemen-

Figure 2.17 The Block Diagram of The CMFB System.

tation is shown in Figure 2.18 where the summation is performed by a summer and the common-mode feedback controls the integrator bias current. In this way the common-

Figure 2.18 The common-mode feed back circuit.

mode output voltage (V_{CMFB}) shown in Figure 2.18 is set by comparison with the common-mode reference voltage V_{REF} . The common-mode feed back voltage feeds back to control the common-mode voltage of the G_m -C integrator as long as V_{OCM} is not high enough to turn off one of the differential pair transistors M_1 or M_2 .

2.6 Summary

In this chapter a study of the main limitations of G_m -C integrators has been carried out. The analysis includes harmonic distortion, noise, tunability and common-mode feedback of the G_m -C structure. The techniques to deal with these limitations have been discussed. Uses of these techniques are discussed in the next chapters.

CHAPTER 3

Design of G_m -C Integrators and Continuous-Time Filters

The basic elements of early continuous-time filters were capacitors, inductors and resistors. With the evolution of integrated circuits (IC), the inductors have been replaced by equivalent elements composed of active devices and capacitors. The resulting topologies are called Active RC filters which are based on either opamps or transconductors, see Figure 2.5 (Chapter 2). For high-frequency applications the G_m -C based circuits have been preferred.

An integrator is the basic building block of continuous-time IC filters. To realize an integrator in G_m -C technology, a transconductor and a capacitor can be used as shown in Figure 2.7 (Chapter 2) with single-ended signals. In most integrated applications it is desirable to keep the signals fully differential. As discussed in Chapter 2, fully differential circuits have better noise immunity and distortion properties. For this reason, the G_m -C integrator used in this thesis is fully differential. A fully differential transconductor has two outputs: one positive output (current flowing out for a positive input voltage) and one negative output (current flowing in for a positive input voltage) as shown later in Figure 3.1. A transconductor is a transconductance cell in which the output current is ideally linearly related to the input voltage. Linearity is one of the most important issues in transconductor design. The most widely used design for differential transconductors is the source-coupled transistor pair shown in Figure 2.12 (Chapter 2) with the transconductance equal to:

$$g_m = \frac{2i}{v_{id}} = \frac{dI}{dV_{eff}} = \sqrt{2KI_Q}$$

where $K = \mu_{n,p} \cdot C_{ox} \cdot \frac{W}{L}$. It is obvious that output current is not linearly related to

input voltage.

This chapter presents the design for G_m -C integrators as well as continuous-time filters. A circuit description, DC analysis and small-signal analysis are given for each circuit. Simulation results are presented including parasitics capacitors, which have a major impact on the frequency response of a circuit. In this chapter, the linearity limit of the G_m -C based integrator is studied in Section 3.1. Two circuits for linearity analysis have been analysed and compared. Because these two circuits were not tunable another integrator with tunability is presented in Section 3.2. This integrator was implemented in CMOS 0.35 μ m technology and built as the basic element of a continuous-time filter. The circuit description and simulation results of the continuous-time filter are described in Section 3.3. Finally, the implementation as well as layout is presented in Section 3.4.

3.1 Resistor Based Linear Transconductor

G_m -C filters offer many advantages in terms of low-power consumption and high-frequency capability because of their simplicity and open-loop nature. An integrator built from an open-loop transconductance amplifier driving a capacitive load can be very fast. however it may perform poorly as far as linearity is concerned. How to improve the linearity of the circuit is one of the main concerns for G_m -C design.

3.1.1 Circuit Description

The approach taken in this thesis to linearize the G_m -C integrator is to use source degeneration with a passive resistor as shown in Figure 3.1. The use of a passive resistor gives good linearity. Let us analyse the operation of the circuit. Starting with the differential input voltage v_{id} and using equation (2.26) we get:

$$v_{id} = v_{IN^+} - v_{IN^-} = \Delta I \cdot R + \left(V_{eff} \cdot \sqrt{1 + \frac{\Delta I}{I}} \right) - \left(V_{eff} \cdot \sqrt{1 - \frac{\Delta I}{I}} \right) \quad (3.1)$$

where V_{eff} of transistors M_1 and M_2 is $V_{eff} = V_{GS} - V_{tn}$. V_{tn} is the threshold voltage

$$\begin{aligned} \frac{v_{id}}{V_{eff}} &= \frac{I \cdot R}{V_{eff}} \cdot \frac{\Delta I}{I} + \sqrt{1 + \frac{\Delta I}{I}} - \sqrt{1 - \frac{\Delta I}{I}} \\ &= \left(1 + \frac{I \cdot R}{V_{eff}}\right) \cdot \frac{\Delta I}{I} + \frac{1}{8} \cdot \left(\frac{\Delta I}{I}\right)^3 + \dots \end{aligned} \quad (3.2)$$
$$\begin{aligned} \frac{g_m}{2} &= \frac{\Delta I}{v_{id}} = \frac{I/V_{eff}}{1 + \frac{I \cdot R}{V_{eff}}} \\ &= \frac{\sqrt{2K \cdot I}}{1 + R \cdot \sqrt{2K \cdot I}} \end{aligned} \quad (3.3)$$

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harmonic distortion which determines linearity is obtained:

$$HD_{3a} = \frac{\text{Signal Amplitude at } 3\omega}{\text{Signal Amplitude at Fundamental}} = \frac{1}{32 \cdot \left(1 + \frac{I \cdot R}{V_{eff}}\right)} \cdot \left(\frac{\Delta I_p}{I}\right)^2 \quad (3.4)$$

where ΔI_p is the peak value of ΔI . From equation (3.3), we know that the transconductance value g_m depends on the gate to source voltages (V_{gs}) of transistors M_1 and M_2 , which cause the distortion of source-degeneration fixed transconductance. As an example, consider NMOS devices in a conservative IC technology, with $\mu_n \cdot C_{ox} = 45 (\mu A)/V^2$. Choosing $W/L = 100$ makes $K = 4.5(mA)/V^2$. Then for $2I = 1$ mA, we obtain $V_{eff} = 472$ mV. Letting $R = 6.6$ K Ω , then $IR = 3.3$ V and $IR/V_{eff} = 6.99$. Hence

$$HD_3 = \frac{1}{32 \cdot \left(1 + \frac{I \cdot R}{V_{eff}}\right)} \cdot \left(\frac{\Delta I_p}{I}\right)^2 = \frac{1}{32 \cdot (1 + 6.99)} \cdot \left(\frac{\Delta I_p}{I}\right)^2 = \frac{1}{255} \cdot \left(\frac{\Delta I_p}{I}\right)^2 \quad (3.5)$$

To keep HD_3 less than -60dBc, ΔI_p must be restricted to a little less than $I/2$. Furthermore, the IR/V_{eff} term is fairly small, so that temperature drift of V_{eff} will appreciably affect the overall circuit's transconductance. Section 3.1.2 will demonstrate a way to reduce the distortion.

3.1.2 Enhanced Circuit

To reduce the degenerated differential pair's distortion, the quantity $(I \cdot R)/V_{eff} = \frac{1}{2}g_m R$ must be increased (where g_m is the quiescent transconductance of MOSFET). There are two ways to reduce the distortion without modifying the circuit. One is to use a large bias current, which will also increase the power consumption of the circuit. The other is to use a small input signal, which would decrease the dynamic range of the circuit. The circuit can be modified to improve the distortion by adding an extra pair of amplifiers, as shown in Figure 3.2. [28]

gate-source voltages of M_1 and M_2 . Let us analyse the operation of the circuit:

$$v_C = V_T + v_A + \sqrt{\frac{2I}{K} \cdot \left(1 + \frac{\Delta I}{I}\right)} \quad (3.6)$$

$$v_D = V_T + v_B + \sqrt{\frac{2I}{K} \cdot \left(1 - \frac{\Delta I}{I}\right)} \quad (3.7)$$

and

$$v_{IN} + = v_A + \frac{v_C}{A_{op}} \quad (3.8)$$

$$v_{IN-} = v_B + \frac{v_D}{A_{op}} \quad (3.9)$$

where A_{op} = open-loop opamp gain.

Therefore,

$$v_{IN+} = \frac{V_T}{A_{op}} + \left(1 + \frac{1}{A_{op}}\right) \cdot v_A + \frac{1}{A_{op}} \cdot \sqrt{\frac{2I}{K}} \cdot \left(1 + \frac{\Delta I}{I}\right) \quad (3.10)$$

$$v_{IN-} = \frac{V_T}{A_{op}} + \left(1 + \frac{1}{A_{op}}\right) \cdot v_B + \frac{1}{A_{op}} \cdot \sqrt{\frac{2I}{K}} \cdot \left(1 - \frac{\Delta I}{I}\right) \quad (3.11)$$

So,

$$v_{id} = (v_{IN+}) - (v_{IN-}) = \left(1 + \frac{1}{A_{op}}\right) \cdot (v_A - v_B) + \frac{1}{A_{op}} \cdot \sqrt{\frac{2I}{K}} \cdot \left(\sqrt{1 + \frac{\Delta I}{I}} - \sqrt{1 - \frac{\Delta I}{I}}\right) \quad (3.12)$$

As $v_A - v_B = \Delta I \cdot R = IR \cdot (\Delta I)/I$, so that

$$v_{id} = \left(1 + \frac{1}{A_{op}}\right) \cdot IR \cdot (\Delta I)/I + \frac{1}{A_{op}} \cdot \sqrt{\frac{2I}{K}} \cdot \left(\sqrt{1 + \frac{\Delta I}{I}} - \sqrt{1 - \frac{\Delta I}{I}}\right) \quad (3.13)$$

Normalizing by V_{eff}/A_{op} and expanding the square-roots in a power series, we get:

$$\frac{A_{op} v_{id}}{V_{eff}} = \left(1 + \left(1 + \frac{1}{A_{op}}\right) \cdot \frac{A_{op} I \cdot R}{V_{eff}}\right) \cdot \frac{\Delta I}{I} + \frac{1}{8} \cdot \left(\frac{\Delta I}{I}\right)^3 + \dots \quad (3.14)$$

if ϵ is very small, the formula is simplified

$$= \left(1 + \frac{A_{op} I \cdot R}{V_{eff}}\right) \cdot \frac{\Delta I}{I} + \frac{1}{8} \cdot \left(\frac{\Delta I}{I}\right)^3 + \dots \quad (3.15)$$

The circuit transconductance is determined from the linear term above in equation (3.15):

$$g_m = \frac{\Delta I}{v_{id}} = \frac{I/V_{eff}}{1 + \frac{A_{op} I \cdot R}{V_{eff}}} = \frac{\sqrt{2K \cdot I}}{1 + \frac{1}{A_{op}} R \cdot \sqrt{2K \cdot I}} \quad (3.16)$$

The third harmonic distortion can be obtained according to equation (2.15) (Chapter 2):

$$HD_{3b} = \frac{\text{Signal Amplitude at } 3\omega}{\text{Signal Amplitude at Fundamental}} = \frac{1}{32 \cdot \left(1 + \frac{A_{op} I \cdot R}{V_{eff}}\right)} \cdot \left(\frac{\Delta I}{I}\right)^2 \quad (3.17)$$

Equation (3.17) has the same form as equation (3.4) except that V_{eff} has been replaced by V_{eff}/A_{op} . When e is small and $I \cdot R \gg V_{eff}/A_{op}$, we can see that $g_m \approx \frac{1}{R}$. Comparing equation (3.4) to equation (3.17) for equal ΔI_p , I , R and e , we obtain:

$$\frac{HD_{3b}}{HD_{3a}} = \frac{32 \cdot \left(1 + \frac{I \cdot R}{V_{eff}}\right)}{32 \cdot \left(1 + \frac{A_{op} I \cdot R}{V_{eff}}\right)} \approx \frac{1}{A_{op}} \quad (3.18)$$

For an opamp with a gain of ten, the HD_3 of circuit in Figure 3.2 is improved by 20dB over that of the circuit in Figure 3.1. It's obvious that the dc gain of the opamp determines the linearity of the circuit. Thus, the opamp's design becomes important. The opamp should be a simple circuit resulting in less distortion and it should have a reasonable open-loop gain. To realize it, a gain stage is presented in Figure 3.3. This circuit is a typical opamp with a

Figure 3.3 A Differential-input, Single-ended-output Opamp.

differential input and a current mirror as an active load resulting in a single-ended output. To analyse the circuit a simple small-signal model is shown in Figure 3.4. The gain is ob-

Figure 3.4 Small-signal Model for the Differential-input Opamp.

tained as:

$$A_v = \frac{v_{out}}{v_{in}} = g_m \cdot z_{out} \quad (3.19)$$

where $z_{out} = r_{out} \parallel 1/(s \cdot C_L)$, g_m is the transconductance of transistor M_1 . The output resistance $r_{out} = r_{ds2} \parallel r_{ds4}$ where r_{ds2} and r_{ds4} are the output resistances of transistor M_2 and M_4 respectively.

3.1.3 Bias Circuit

Normally for prototypes the bias current or voltage is provided from the outside world. This results in maximum flexibility for testing. In order to provide the correct bias current or voltage in spite of process, temperature and power-supply voltage variations, a bias circuit is necessary.

The wilson current mirror bias circuit is shown in Figure 3.5(a). First assume that $(W/L)_1 = (W/L)_2$, $(W/L)_3 = (W/L)_4$. This equality results in both sides of the circuit having the same current due to the current-mirror pair M_1 , M_2 . As a result, $I_{ref} = I_{D1} = I_{D2}$ and $I_{D3} =$

Figure 3.5 Bias Circuits (a) Wilson Current Mirror Circuit (b) Simple Circuit

I_{D4} . If all the transistors' sizes are equal, W/L of each transistor can be calculated by:

$$I_{REF} = \frac{1}{2} \cdot \mu_{n,p} \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_t)^2 \quad (3.20)$$

where I_{REF} is the reference current, and μ_n and C_{ox} are parameters according to the process technology. The Wilson current mirror should have employed in this circuit instead of a simple current mirror bias circuit in Figure 3.5(b) as it is adjustable. By changing the value of V_{ref} the reference current (I_{REF}) is approximately equal to input current independent of process and temperature.

3.1.4 Small-Signal Simulation Results

Small-signal simulations from HSPICE were performed to verify that the circuit's operation matched the equations for the small-signal model. Also, the previous two integrators were compared with each other. The AC analysis simulation results for the passive resistor based integrator in Figure 3.1 are plotted in Figure 3.6. Figure 3.7 shows the AC analysis simulation results for the enhanced integrator in Figure 3.2. From equation (3.3) and (3.16) if the gain of the extra amplifier is greater than 1, the enhanced circuit has a

Figure 3.6 AC Analysis of Circuit 1

Figure 3.7 AC Analysis of Circuit 2

greater transconductance than the original one. Thus, higher voltage gain can be achieved. By comparing the two AC frequency responses shown in Figure 3.6 and Figure 3.7, we can see that the output gain of enhanced integrator is nearly 2dB higher than the passive resistor based circuit. Due to the input stage opamp, the enhanced circuit has more parasitic capacitance and as a result, its frequency response rolls off at a lower frequency, but its unity gain bandwidth is nearly the same.

3.1.5 Large-Signal Simulation Results

Large signal simulations were also performed on the two circuits. These simulations ex-

exercised the circuits' nonlinearity, providing a means of predicting distortion in the two circuits.

3.1.5.1 DC Analysis

The DC large-signal analysis simulation was performed on the original circuit and the linearity enhanced circuit (Figure 3.2) with output shorted to verify that the transconductance of the circuit depends more on the input voltage and the passive resistor, thus a more linear circuit could be achieved compared to the circuit of Figure 3.1. The simulation results are shown in Figure 3.8 and Figure 3.9 respectively. It shows that with the opamp at each

Figure 3.8 DC Analysis of Circuit 1

Figure 3.9 DC Analysis of Circuit 2

input, the input voltage is forced to appear across the passive resistor. For this reason, com-

pared to the original circuit the input voltage vs output current plot in Figure 3.9 is linear until cutoff is reached. The DC analysis gives rough results that indicates the enhanced circuit has better linearity than the original circuit.

3.1.5.2 1dB Compression, IP3 Simulation Methodology

A series of large-signal analyses were also performed to determine the 1 dB compression point and third-order intercept point of the two G_m -C integrators which gives another estimate of the linearity of the circuits. SpectreRF was used to simulate the 1dB compression and IP_3 point of the integrators instead of Hspice. To run the simulation of 1dB compression and IP_3 point a P_{sin} source was applied to the input of the circuit instead of the V_{sin} input voltage source used in Hspice simulation. The setup used to simulate differential input and output G_m -C integrator using the P_{sin} (power source) model is shown in Figure 3.10. For SpectreRF design, there is a 50Ω impedance inside the P_{sin} which is defined as

Figure 3.10 SpectreRF Simulation Setup For G_m -C Integrator

a parameter (Note: the value of impedance is changeable). In SpectreRF design the output power was simulated while in Hspice design the output voltage was simulated. To compare the results, it is necessary to convert between voltage (dB) and power (dBm). The definition of dBm and dB is shown in equation (3.21) and (3.22) respectively.

$$dBm = 10 \cdot \log \frac{V_{rms}^2 / R}{1mw} \quad (3.21)$$

$$dB = 20 \cdot \log \frac{V}{1v} \quad (3.22)$$

dBm can be converted to dB by the equation:

$$\left(10 \cdot \log \frac{V_{rms}^2 / R}{1mw} \right) dBm = \left(20 \cdot \log \frac{V}{1v} - (10 \cdot \log (R \cdot 2 \cdot 1mw)) \right) dB \quad (3.23)$$

$$dBm = dB + 30 - (10 \cdot \log (R \cdot 2)) \quad (3.24)$$

where R is the output impedance. For RF design, the output impedance is typically 50Ω value. In order to simplify the comparison of integrators, 50Ω is defined as the output impedance value for all the integrators in this Chapter. In this case, we get the power conversion formula as:

$$dBm = dB + 10 \quad (3.25)$$

Hence, the data of dBV presented later in this section should be scaled up by a factor of 10 to convert to dBm. Tone1 and Tone2 shown in Figure 3.10(a) are the two-tone signals parameters inside the P_{sin} . By filling in the proper values, a two-tone signal simulation can be run to determine the 1dB compression and IP_3 points of the integrators.

3.1.5.3 1dB Compression, IP_3 Simulation Results

The two-tone signal simulation was performed by applying one tone at 300MHz, the second tone at 301MHz to the input of the integrator. The 1 dB compression point was performed first. The results of this simulation for passive resistor based integrator (Figure 3.1) are plotted in Figure 3.11. The horizontal axis shows the input power sweep range (dBm) and the vertical axis shows the output power in dBm. This was obtained from the original

Figure 3.11 Plot of 1dB Compression Point for Passive Resistor Based Integrator With 20dB Gain at 300MHz.

plot in dBV by adding 10 as discussed before in Section 3.1.5.1. Two curves are presented in this plot, the first curve, which is a straight line, is the ideal case where the output power keeps increasing linearly with input voltage. The second curve is the actual case which shows the output voltage compressing with increasing input voltage. The 1 dB compression point occurs when the measured output deviates from the ideal curve by 1 dB. Figure 3.11 indicates that the input 1 dB compression point is -24.45 dBm. Because the gain of the passive resistor based integrator at 300MHz is 20dB (unity gain frequency is at 1GHz), the output 1dB compression point occurs at -4.5dBm. Figure 3.12 shows the output 1 dB compression point when the gain at 300MHz of this passive resistor based integrator is 0dB (unity gain frequency is at 300MHz). Gain was adjusted by changing the load capacitor.

The results of the 1dB compression simulation for the enhanced integrator (Figure 3.2) are plotted in Figure 3.13, and show that the input 1 dB compression point is -20.08 dBm. The output 1 dB compression point, for this plot, occurs at - 1.0 dBm, since the gain of the

Figure 3.12 Plot of 1dB Compression Point for Passive Resistor Based Integrator With Unity Gain at 300MHz.

Figure 3.13 Plot of 1dB Compression Point for Enhanced Integrator With 20dB Gain at 300MHz.
enhanced integrator at 300MHz was set to 20dB. Figure 3.14 shows the output 1 dB com-

Figure 3.14 Plot of 1dB Compression Point for Enhanced Integrator With Unity Gain at 300MHz
pression point when unity gain of this enhanced integrator was set to 300MHz.

The third order intercept point is the power level where the power in the third order products equals the power in the fundamental. A two tone test was performed for the third order intercept. The two equal amplitude tones were closely spaced, within the 3 dB bandwidth of the integrator with one frequency at 300 MHz and the other at 301 MHz. The results of the third-order intercept point simulation for the passive resistor based integrator (Figure 3.1) is shown in Figure 3.15. As in the previous plot the horizontal axis shows the input power and the vertical axis shows the output power. There are four curves presented in the plot. the first two curves are the fundamental output ideal linear case and the fundamental compression curve. The third curve is the third-order ideal case where the output voltage keeps increasing linearly with input voltage. The fourth curve is third-order actual case which shows the output compressing with increased input voltage. The third-order intercept point is where the two ideal cases intersect. The input third-order intercept point is -10.32 dBm which is approximately 15 dBm above the 1 dB compression point at -24.45 dBm. Figure 3.16 shows the third-order intercept point when unity gain frequency is set to

Figure 3.15 Plot of The Third-Order Intercept Point for Passive Resistor Based Integrator With 20dB Gain at 300MHz.

300MHz.

The results of the third-order intercept point simulation for the enhanced integrator (Figure 3.2) is plotted in Figure 3.17. The input third order intercept point is -5.01dBm which is approximately 15 dBm above the 1 dB compression point at -20.08 dBm. Another third-order intercept point plot is shown in Figure 3.18 with unity gain frequency set at 300MHz.

The plots of 1db compression point and third-order intercept point indicate the follows:

- (1) The linearity of each integrator changed little as its unity gain frequency was adjusted by varying the output load capacitor.
- (2) The enhanced integrator (Figure 3.2) with opamp at input forces the voltage directly

Figure 3.16 Plot of The Third-Order Intercept Point for Passive Resistor Based Integrator With Unity Gain Frequency at 300MHz.

Figure 3.17 Plot of The Third-Order Intercept Point for Enhanced Integrator With 20dB Gain at 300MHz.

Figure 3.18 Plot of The Third-Order Intercept Point for Enhanced Integrator With Unity Gain Frequency at 300MHz.

across the resistor R and offers a 5dBm improvement in linearity.

- (3) Linearity mainly depends on the input. In other words, IIP3 is determined by the value of passive resistor R , with the same R value IIP3 changes little with different output loads.

The comparison of these two circuits with the same voltage gain is shown in Table 3.1.

Table 3.1 Comparison of Circuit 1 and 2

Parameters	Results (circuit1)	Results (circuit2)
Power Supply	3.3 V	3.3 V
Current Consumption	1.16 mA	1.76 mA
Unity Gain Frequency	300 MHz	291 MHz
Linearity Range	0.40 Vp-p	0.52 Vp-p
Max DC Gain	20 dB	23 dB
Two Tones 1 dB Compression	- 24.4 dBm	- 20.18 dBm
IP3	- 10.03 dBm	- 5.12 dBm

and Table 3.2 Though circuit 2 consumes more power than circuit 1, it has improved lin-

Table 3.2 Comparison of Circuit 1 and 2

Parameters	Results (circuit1)	Results (circuit2)
Power Supply	3.3 V	3.3 V
Current Consumption	1.16 mA	1.76 mA
Unity Gain Frequency	1G MHz	989 MHz
Max DC Gain	20 dB	22 dB
Two Tones 1 dB Com- pression	- 24.45 dBm	- 20.08 dBm
IP3	- 10.32 dBm	- 5.02 dBm

earity performance due to the input stage opamp. The unity gain frequency of circuit 2 is less than that of circuit 1. The linearity range is obtained by adding the maximum and minimum voltage values, which can be applied to the circuit's input before the output current goes to its saturation region shown in Figure 3.8 and Figure 3.9. Both the 1 dB compression point simulations and 3rd harmonic intercept point simulations show that circuit 2 (Figure 3.2) offers a 5dBm linearity improvement. The linearity is not affected so much by output load but, it mainly depends on the input. The passive resistor R and input stage opamp play important roles in the linearity performance. Two additional simulations have been done to verify that linearity mainly depends on input (value of passive resistor R) and hardly affected by the output load.

An additional two-tone (300MHz-301MHz) IP3 point simulation was performed for each of the integrator. The simulation parameters were kept the same as in the previous IP3 simulations except the voltage gain was dropped by 10dB for both integrators by increasing the value of the passive resistors R by a factor of about 3. The third-order intercept point results are shown in Figure 3.19 and Figure 3.20 . The simulation data is presented in Table

Figure 3.19 Plot of The Third-Order Intercept Point for Passive Resistor Based Integrator With -15dB Gain at 300MHz

Figure 3.20 Plot of The Third-Order Intercept Point for Enhanced Integrator With -15dB Gain at 300MHz.

3.3. With lower voltage gain of the integrator achieved by modifying the input circuit e.g

Table 3.3 Comparison of Circuit 1 and 2

Parameters	Results (circuit1)	Results (circuit2)
Power Supply	3.3 V	3.3 V
Unity Gain Frequency	120 MHz	110 MHz
Max DC Gain	10 dB	10 dB
Gain at 300 MHz	-15 dB	-15 dB
Two Tones 1 dB Compression	- 21.8 dBm	- 16.5 dBm
IP3	- 7.18 dBm	- 1.25 dBm

10dB, both circuits in Figure 3.1 and Figure 3.2 a lower distortion can be achieved as the input stage opamp forces the input signal directly across the passive resistor with less loss on the gate and source voltage of both M1 and M2 transistors in Figure 3.2 an additional 6dBm distortion improvement has been obtained. This verifies that the linearity of the integrator mainly depends on the input.

Another two-tone (300MHz-301MHz) IP3 point simulation was performed as well for each of the integrator with output shorted as shown in Figure 3.21. The third-order intercept point results are shown in Figure 3.22 and Figure 3.23. The simulation data is presented in Table 3.4. With the output shorted, only ac current can get through and the effect of the out-

Table 3.4 Comparison of Circuit 1 and 2

Parameters	Results (circuit1)	Results (circuit2)
Power Supply	3.3 V	3.3 V
Unity Gain Frequency	300 MHz	291 MHz
DC Voltage	1.647 V	1.645 V
Two Tones 1 dB Compression	-22 dBm	-21 dBm
IIP3	-9.24 dBm	-4.79 dBm

Figure 3.21 SpectreRF Simulation Setup For G_m -C Integrator With Output Shorted

Figure 3.22 Plot of The Third-Order Intercept Point for Passive Resistor Based Integrator With Output Shorted

put load is removed. An ideal CCVS (Current Controlled Voltage Source) with gain of 1 has been applied to convert current to voltage as SpectreRF can analyze dB but not dBI. With gain of the CCVS set to 1 the converted voltage has the same amplitude as the ac current. The simulation results show that the output load has less than 0.5 dBm effect on the linearity which proves that the output does not affect the linearity much.

Figure 3.23 Plot of The Third-Order Intercept Point for Enhanced Integrator With Output Shorted

Based on the simulation results some advice can be offered to the designer trying to increase the linearity of the circuit:

- (1) Increase the passive resistor value R . But, this causes the gain and bandwidth of the integrator to drop. To restore the bandwidth, a smaller output load capacitor is needed. A smaller output load capacitor may be more sensitive to process variations and parasitic capacitors.
- (2) It may be possible to decrease the size of transistor M_1 and M_2 shown in Figure 3.1 and Figure 3.2 to increase the effective values of degeneration resistance. However, for any changes to M_1 and M_2 , it is important to avoid changing the operating conditions. For example, smaller M_1 and M_2 will more easily operate in the triode region instead of in saturation, the intended region of operation.

3.2 Tunable Integrator

The simulation results presented in the previous section give us the idea of the linearity

performance limits of the resistor based integrator. The center frequency of the resistor based integrator is fixed and cannot be tuned. Since variations of temperature, process, and supply voltage could change the center frequency of the integrator, it is very important to make an integrator which is tunable and has reasonable linearity.

3.2.1 Tunable Transconductor Circuitry

The tunable integrator used to build a filter is shown in Figure 3.24. The transconductance

Figure 3.24 Tunable Integrator.

of the integrator is given by: (see equation (3.3))

$$g_m = \frac{\Delta I}{V_{id}} = \frac{\sqrt{2K \cdot I}}{1 + R_{ds} \cdot \sqrt{2K \cdot I}} \quad (3.26)$$

where R_{ds} is the resistance of M_7 . M_7 acts here like a tunable resistor: the drain and the source are used as the resistor terminals and the tuning of the resistor is carried out by gate

voltage. The resistance of M_7 biased in triode region is given by: (as derived in (2.33))

$$R_{ds} \equiv \frac{1}{K(V_G - V_t - V_{CM})} \quad (3.27)$$

where $V_{CM} = (V_D + V_S)/2$ is the common-mode portion of the drain-source voltage, and $K = \mu \cdot C_{ox} \cdot \frac{W}{L}$ which $\mu \cdot C_{ox}$ are process parameters and $\frac{W}{L}$ are design values. For low supply voltages, the resistance can be tuned by changing the control voltage at the gate of M_7 whose tuning range is enough for most of the low-Q applications. From equation (2.4) (Chapter 2) we know that center frequency of the integrator can be tuned by the transconductance value g_m which is related to R_{ds} as shown in equation (3.26). The tunable transistor M_7 also has important implications for linearity. The output current of the circuit can be calculated by:

$$\Delta I = \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot \left[(V_G - V_t) \cdot (V_D - V_S) - \frac{(V_{ds})^2}{2} \right] \quad (3.28)$$

where V_{ds} is the drain-source voltage of M_7 . With a large W/L ratio and a small V_{ds} swing, a reasonable linearity performance can be obtained.

3.2.2 Common-mode Feedback Circuitry

As discussed before, a fully differential circuit needs a common-mode feedback circuit. The reason is that although the differential signal remains stable due to the connections of the filter feedback network, the common-mode signal is free to drift if it is not also controlled using some feedback circuitry. So, additional circuitry is added to control the output common-mode voltage to be equal to some specified voltage, typically half of the supply voltage. As discussed before, the common-mode feedback circuit is more or less like a voltage amplifier which compares the common-mode voltage to a reference voltage and feeds back the error voltage to control the common-mode voltage of the integrator as shown in Figure 2.18 (Chapter 2). An example of a fully differential common-mode feedback circuit

Figure 3.25 Fully Differential Common-mode Feedback Circuitry

Since V_{out-} and V_{out-} are connected to the differential output of the transconductor. V_{out-} and V_{out-} are ideally equal in magnitude, but opposite in sign. Thus, the two differential pairs have the same applied differential voltages. The current in M_1 will be equal to the current in M_3 , while the current in M_2 will equal the current in M_4 . Now, letting the current in M_2 be $I_{d2} = I_B - i$, where $2I_B$ is the bias current of the differential pair and i is the signal change in I_{d2} , the current in M_3 is given by $I_{d3} = I_B + i$, and the current in M_5 is given by

$$I_{d5} = I_{d2} + I_{d3} = I_B + i + (I_B - i) = 2I_B \quad (3.29)$$

Thus, as long as the common-mode portion of V_{out+} is equal to the common-mode portion of V_{out-} , the current through diode-connected M_5 will not change and keep it equal to $2I_B$ even when large differential signal voltages are present. The voltage across diode-connected M_5 is used to control the bias voltage of the output stage of the transconductors. This means that when no common-mode voltage is present, the bias currents in the output

stage will be the same (equal to $2I_B$) regardless of whether a signal is present or not. It should be noted that the voltage on nodes X and Y shown in Figure 3.25 will follow the voltages V_{out+} and V_{out-} respectively, thus the bias current will not be completely constant. However, to a first order approximation the current through M5 and M6 should remain nearly constant.

Now, assume the common-mode voltage changes, for example, it increases a little. This increase in voltage will cause the currents in both M_2 and M_3 to decrease, which causes the current in diode-connected M_5 to decrease, which in turn causes its gate voltage to increase. This voltage is the bias voltage that sets the current levels in the p-channel current sources at the output of the transconductor. Thus, both current sources will have smaller currents flowing through them, which will pull down the common-mode voltage to compensate for the original positive common-mode voltage.

The size of the input signals to the common mode feed back circuit which can be processed without one of the differential-pair transistors turning off is maximized if the differential-pair transistors are designed to have large effective gate-source voltages. However, it is possible that the output differential voltage swing will be limited by the linearity of the common-mode feedback circuitry.

3.2.3 Small-Signal Simulation Results

The parametric AC analysis response which shows the frequency performance is shown in Figure 3.26. The parametric AC analysis whose control voltage is a parameter having different values shows how center frequency changes with respect to control voltage variations. This is because with different control voltages the integrator's transconductance is changed and causes the centre frequency of integrator changes.

Figure 3.26 Parametric AC Analysis of Tunable Integrator

3.2.4 Large-Signal Simulation Results

The DC parametric analysis of input voltage vs. output current is shown in Figure 3.27.

Figure 3.27 DC Analysis of Tunable Integrator

By sweeping the value of the control voltage at the gate of M_7 in Figure 3.24, different output current curves vs. the same input voltage were generated which give a rough estimation of linearity. The DC analysis response shows that with different control voltages the transconductance of the circuit is tuned. A series of large-signal analyses were also per-

formed to determine the 1 dB compression point and third-order intercept point of the tunable G_m -C integrator which gives a more accurate estimation of linearity. The two-tone signals are applied to the tunable integrator with one tone at 300MHz, and the second tone at 301MHz. The 1 dB compression point is plotted in Figure 3.28, which indicates that the

Figure 3.28 Plot of 1dB Compression Point for Tunable Integrator With 20dB Gain at 300MHz.

input 1 dB compression point is -25.78 dBm. When unity gain frequency is set to 300MHz, the 1dB compression Point is at -24.5 dBm as plotted at Figure 3.29. This value is very close to that of the resistor based integrator due to the high gain of the integrator. The output is not able to handle large amounts of power before being driven into non-linear operation and is clipped. The third-order intercept point is where the intersection of 3 dB/1 dB slope line and 1 dB/1 dB slope line occurs. The input third order intercept point is -12.3dBm. Results of the third-order intercept point simulation for the tunable integrator (Figure 3.24) are plotted in Figure 3.30. Another third-order intercept point simulation was also carried out with the integrator's unity gain frequency being placed at 300 MHz as shown in Figure 3.31. Both the 1dB compression point and the third-order intercept point, indicate that with 20dB gain, the tunable integrator has almost the same linearity performance as the previous two

Figure 3.29 Plot of 1dB Compression Point for Tunable Integrator With Unity Frequency at 300MHz.

Figure 3.30 Plot of The Third-Order Intercept Point for Tunable Integrator With 20dB Gain at 300MHz.

Figure 3.31 Plot of The Third-Order Intercept Point for Tunable Integrator With Unity Gain Frequency at 300MHz.

integrators which were based on a linear passive resistor. The simulation data of the tunable integrator is shown in Table 3.5. The comparison of these three integrators shows the ad-

Table 3.5 Tunable integrator simulation results

Parameters	Results(cir.3)	Results(cir.3)
Power Supply	3.3 V	3.3 V
Unity Gain Frequency	810 MHz ~ 990 MHz	220 MHz ~ 300 MHz
Linearity Range	0.4 V _{p-p}	0.4 V _{p-p}
Max DC Gain	21 dB	21 dB
Gain at 300MHz	21 dB	0 dB
Two Tones 1dB Compression	-25.78 dBm	-24.5 dBm
IP3	-12.28 dBm	-11.30 dBm
Control Voltage	1.40 V ~ 1.90V	1.40 V ~ 1.90V

vantages and disadvantages of each of them as shown in Table 3.6 and Table 3.7. As dis-

Table 3.6 Simulation Results of Three Integrators

Parameters	Circuit1 (Figure 3.1)	Circuit2 (Figure 3.2)	Circuit3 (Figure 3.24)
Power Supply	3.3V	3.3V	3.3V
Current Consumption	1.16 mA	1.76 mA	1.12 mA
Unity Gain Frequency	300 MHz	291 MHz	220 MHz ~ 300 MHz
Linearity Range	0.40 V _{p-p}	0.52 V _{p-p}	0.4 V _{p-p}
Max DC Gain	20 dB	22 dB	21 dB
1dB Compression(2 Tone)	- 24.4 dBm	- 20.18 dBm	-25.78 dBm
IIP3	- 10.03 dBm	- 5.12 dBm	-11.3 dBm

Table 3.7 Comparison of Three Integrators

Circuits	Advantages	Disadvantages
Passive resistor based integrator(Figure 3.1)	<ul style="list-style-type: none"> • Good linearity IIP₃ = -10.03 dBm 	<ul style="list-style-type: none"> • Needs multiplier -style tuning • Larger chip area
Enhanced passive resistor based integrator(Figure 3.2)	<ul style="list-style-type: none"> • Better linearity IIP₃ = -5.12 dBm 	<ul style="list-style-type: none"> • Needs multiplier -style tuning • Larger chip area
Tunable integrator (Figure 3.24)	<ul style="list-style-type: none"> • Tunability Frequency tunability Q value tunability 	<ul style="list-style-type: none"> • Less linearity IIP₃ = -11.3 dBm

cussed before in equation (3.18), in theory circuit 2 should have 10dB IP3 improvement over circuit 1 when the e of the extra opamp has 10dB gain but, only 5dB improvement has been obtained. The discrepancy may be due to distortion introduced by the extra opamp. however this has not been investigated further. .

3.3 Filter Design

For the design of the continuous time G_m -C filter a second-order biquad circuit topology was selected as it provided a simple structure that demonstrated the capabilities of the technology as well as higher speed performance compared to MOSFET-C and RC active-C. The transfer function for a general second-order filter is given by:

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{K_2 \cdot s^2 + K_1 \cdot s + K_0}{s^2 + \frac{\omega_0}{Q} \cdot s + \omega_0^2} \quad (3.30)$$

The fully differential version of this filter is shown in Figure 3.32. The transfer function

Figure 3.32 A Biquad Filter Using Fully Differential G_m -C Technology

of this general biquad filter is shown below:

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{s^2 \cdot \frac{C_x}{C_x + C_b} + s \cdot \frac{G_{m5}}{C_x + C_b} + \frac{G_{m2} \cdot G_{m4}}{C_a \cdot (C_x + C_b)}}{s^2 + s \cdot \frac{G_{m3}}{C_x + C_b} + \frac{G_{m1} \cdot G_{m2}}{C_a \cdot (C_x + C_b)}} \quad (3.31)$$

The block diagram representation of the biquad filter is shown in Figure 3.33. Equating

Figure 3.33 A Block Diagram of A General Biquad Continuous-Time Filter

the coefficients of both (3.30) and (3.31) results in:

$$\omega_o^2 = \frac{G_{m1} \cdot G_{m2}}{C_a \cdot (C_x + C_b)} \quad (3.32)$$

For Q , we note that $\frac{\omega_o}{Q} = \frac{G_{m3}}{C_x + C_b}$, and so, resulting in

$$Q = \sqrt{\frac{G_{m1} \cdot G_{m2}}{G_{m3}^2} \cdot \frac{C_x + C_b}{C_a}} \quad (3.33)$$

For a bandpass biquad filter the transfer function would be:

$$T(s) = \frac{a \cdot s}{s^2 + s \cdot \frac{\omega_o}{Q} + \omega_o^2} \quad (3.34)$$

This, results in: $G_{m4} = 0$, $C_x = 0$, $K_2 = 0$, $k_o = 0$. The transfer function of a bandpass biquad G_m -C filter is given by:

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{s \cdot \left(\frac{G_{m5}}{C_b} \right)}{s^2 + s \cdot \left(\frac{G_{m3}}{C_b} \right) + \frac{G_{m1} \cdot G_{m2}}{C_a \cdot C_b}} \quad (3.35)$$

From equation (3.32), we get that:

$$\omega_o = \sqrt{\frac{G_{m1} \cdot G_{m2}}{C_a \cdot C_b}} = \frac{G_{m1}}{C} \quad (3.36)$$

when $G_{m1} = G_{m2}$, $C_a = C_b = C$.

$$Q = \sqrt{\frac{G_{m1} \cdot G_{m2}}{G_{m3}^2} \cdot \frac{C_b}{C_a}} = \frac{G_{m1}}{G_{m3}} \quad (3.37)$$

$$a = \frac{G_{m5}}{C_b} \quad (3.38)$$

$$\text{Gain at } \omega_o = \frac{\frac{G_{m5}}{C_a} \cdot Q}{\omega_o} = \frac{G_{m5}}{G_{m3}} \quad (3.39)$$

The circuit of Figure 3.32 can be simplified and implemented as a bandpass G_m -C filter, using two pairs of balanced capacitors ($2C_a$, $2C_b$) (as shown in Figure 3.34).

3.3.1 Circuit Description

The overall schematic of the second-order transconductance-C filter is shown in Figure 3.35. The schematic shows all the control voltage inputs used for tuning. All tuning is done manually. The three control voltages provide: (1) Center frequency tuning, (2) Q value tuning and (3) Gain tuning. From equation (3.36), the unity gain frequency is tuned by changing the value of G_{m1} which is determined by control voltage V_{C2} . As Q is determined by G_{m1} , G_{m2} and G_{m3} value, by changing the gate voltages of V_{C3} , Q can be tuned. Finally

Figure 3.34 A bandpass biquad fully differential G_m -C filter

Figure 3.35 Complete Schematic of Second-order Bandpass G_m -C Filter

the gain at ω_o is determined by G_{m5} and G_{m3} which can be adjusted by varying voltages V_{C1} . The grounded capacitors were used instead of differential capacitors as they provide

stability of common-mode loop. The common-mode loop would otherwise be unstable since two integrators in a loop result in a complex conjugate pair of poles in the right half plane. Choosing to use grounded capacitors and minimizing common-mode gain bring these roots as close to the origin as possible for a given differential loop ω_0 . Grounded damping devices can then force both poles into the left half-plane to obtain common-mode stability.

3.3.2 Small-Signal Simulation Results

The small-signal simulation results of the bandpass filter for frequency tuning are shown in Figure 3.36. As discussed in Section 3.3.1, both frequency and Q tuning processes

Figure 3.36 Simulation Results for Frequency Tuning of Bandpass Filter

can be done manually: ω_0 (unity gain frequency) is tuned by G_{m1} by changing control volt-

age V_{C2} ; Gain is tuned by control voltage V_{C1} which varies G_{m5} ; Q is tuned by control voltage V_{C3} which sets G_{m3} . In parametric analysis, V_{C1} (gain control voltage) and V_{C3} (Q control voltage) were set to 2.8 volts and 1.4125 volts respectively. Three values of V_{C2} (frequency control voltage) from 1.368 volts to 3.0 volts were applied resulting in the low, medium and high frequency curves. Small signal simulation results show that the frequency tuning range is from low frequency (164 MHz) to high frequency (340 MHz).

The small-signal parametric analysis simulation results for Q tuning are shown in Figure 3.37. The frequency control voltage V_{C2} was set to 1.8 volts. The gain control voltage

Figure 3.37 Simulation Results for Q Tuning of Bandpass Filter

was adjusted to provide maximum gain of 24 dB which was achieved by setting V_{C1} to 2.8 volts. By sweeping three different values of Q control voltage V_{C3} which are 1.4125 volts, 1.30 volts and 1.0 volts results in high, medium and low Q value curves. The high Q curve has a gain of 24 dB with Q value of 10.3 and low Q curve has a gain of 12 dB with Q value

of 8.1. For this second-order filter, high speed performance can be achieved around 340 MHz, however, high Q value is hard to obtain. The simulation data is shown in Table 3.4.

Table 3.8 Bandpass Filter Simulation Results

Parameters	Results
Power supply	3.3 V
Power consumption	14 mW
Center frequency	164 - 340 MHZ
Bandwidth (-3dB)	15 - 30 MHZ
Equivalent Filter Q	8.1 - 10.3

3.3.3 Buffer Description

Normally, a buffer is required at the output nodes to drive the output load which is 50Ω . Because the current flow through the whole filter is very small, significantly less than 1mA a higher current is required to drive the load. As there is no voltage gain requirement, a typical buffers with a voltage gain close to unity is sufficient. Thus, a source follower is chosen as the buffer as shown in Figure 3.38. The current flow through the load impedance can be

Figure 3.38 Source-Follower Buffer (a) Schematic (b) An equivalent Small-Signal model

calculated by:

$$I_d = \frac{1}{2} \cdot \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{gs} - V_t)^2 \quad (3.40)$$

As long as transistor M_1 works in the saturation region and is fairly wide the output current can be kept large enough to drive the output load R_L which is 50Ω . The schematic of the band-pass filter with buffer is shown in Figure 3.39.

Band Pass G_m -C IF Filter Schematic

Figure 3.39 Complete Schematic of Second-order Bandpass G_m -C Filter With Buffer

3.3.4 Small-Signal Simulation Results with Buffer

The small-signal HSPICE simulations of the band pass G_m -C filter with buffer were compared with the previous simulation results on the filter without buffer shown in Figure 3.36 and Figure 3.37. Adjustments to component values were necessary to compensate for shifts in the desired center frequency due to transistor parasitic capacitances and the 50Ω output impedance. The small-signal analysis of the filter frequency tuning response with buffer is shown in Figure 3.40. The center frequency tuning is achieved through the proce-

Figure 3.40 Simulation Results for Frequency Tuning of IF Filter with Buffer

dure discussed in Section 3.3.2. V_{C1} (gain control voltage) and V_{C3} (Q control voltage) were set to 2.8 volts and 1.47 volts respectively. By sweeping three values of V_{C2} (frequency control voltage) from 1.48 volts to 3.0 volts results were obtained for low, medium and high frequency curves. Small signal simulation results show that the frequency tuning range is from a low frequency of 160 MHz to a high frequency of 311 MHz.

The Q tuning response of the band pass G_m -C filter with buffer is shown in Figure 3.41. The frequency control voltage V_{C2} was set to 3.0 volts. The gain control voltage was adjusted to provide maximum gain of 20 dB which was obtained when V_{C1} was set to 2.8 volts. By sweeping three different values of Q control voltage V_{C3} (1.47 V, 1.38 V and 1.2 V) high, medium and low Q value curves were obtained. The high Q curve has a gain of 20 dB which is around $Q = 10.5$ and low Q curve has a value of 8 dB with $Q = 8.1$. The simulation data is summarized in Table 3.9. From the simulation results we see that the

Figure 3.41 Simulation Results for Q Tuning of Bandpass Filter with Buffer

center frequency is decreased as the output loading is increased. The same conclusion can be derived from equation (2.4) (Chapter 2).

Table 3.9 Simulation Results with Buffer

Parameters	Results
Power supply	3.3 V
Power consumption	14 mW
Chip area	557*47 μm^2
Center frequency	160 - 311 MHZ
Bandwidth (-3dB)	15 - 30 MHZ
Equivalent Filter Q	8.1 - 10.5

3.3.5 Large-Signal Simulation Results

A series of large-signal analyses were also performed to determine the 1 dB compression point and third intercept point of the tunable G_m -C IF filter. Two-tone signals were applied to the tunable integrator with one tone at 300MHz, the second tone at 301MHz within the 3dB bandwidth of the bandpass filter. The 1 dB compression point simulation was performed yielding the results plotted in Figure 3.42. Figure 3.42 indicates that the input 1

Figure 3.42 Plot of 1dB Compression Point for Second Order Filter.

dB compression point is - 28.7 dB and the output 1 dB compression point is -8 dB. The values are a little bit lower than those of integrator, because the output driver was not able to handle large amounts of power before being driven into nonlinear operation. The gain of the passive resistor based integrator for this setting was 20dB.

A two tone test was also performed on the IF filter to determine the third order intercept

point. The two tones were closely spaced, within the 3dB bandwidth of this filter, with one frequency at 300 MHz and the other at 301 MHz. The simulated third order intercept point is plotted in Figure 3.43. The input third order intercept point is -15.0 dBm which is approx-

Figure 3.43 Plot of Third-Order Intercept Point for Second Order Filter.

imately 14 dB above the 1 dB compression point at -28.7 dBm.

3.4 Summary

In this chapter, we first analysed two passive resistor based integrators which gave us insight on linearity performance limits. Secondly, we analysed a tunable integrator implemented as the basic building block of G_m -C filter. It was found that the linearity of the integrator mainly depends on the input passive resistor R and input stage opamp of the integrator. Since a DC gain of 20 dB was desired for the integrator, the linearity performance of the tunable integrator was close to that of the passive resistor based integrators.

Thus, the tunable integrator became the best candidate for the G_m -C integrator used to implement a tunable filter.

Finally, a second-order bandpass filter was implemented. A circuit description and small-signal analysis was given for each circuit. HSpice simulation results for the filter including an output buffer were presented. The designed tunable G_m -C second-order filter is suitable for low-Q ($Q \sim 10$) applications. For high-Q applications some Q enhancement scheme for example with positive feedback might be required. However, linearity is expected to be affected and stability is a concern.

CHAPTER 4

G_m -C Filter Experimental Results

Experimental results are presented for the second-order G_m -C tunable filter. The test set-up and measurement procedures are discussed. Testing was performed to measure the following characteristics: frequency response, tuning range, Q-tuning, power dissipation and dynamic range. The measured results are also compared to the predicted results from HSPICE simulations.

4.1 G_m -C Integrator

This section presents the layout considerations of the integrator. The extracted layout is simulated and results compared to simulation results from the schematic. As the integrator is the main building block of the IF filter, its performance characteristics determine the performance of the filter directly. For these reasons, it is very important to test the characteristics of the integrator.

4.1.1 Integrator Layout Considerations

Layout is an important factor that must be given careful consideration for circuits working at high frequency. Parasitic capacitance and resistance of lines and pads introduce poles and zeros that play a role in shaping the frequency response of the circuit. Parasitic capacitance is one of the main factors which must be taken into account as it affects the integration coefficient. The integrator with load capacitance(C_L) and parasitic capacitance(C_p) is shown in Figure 4.1. The transfer function of the integrator is given by:

$$v_0 = \frac{g_m \cdot v_i}{s \cdot (C_L + C_p)} \quad (4.1)$$

Figure 4.1 G_m -C Integrator with Parasitic Capacitances.

To reduce parasitic series resistance, power and ground were constructed using the maximum allowable line width in the $0.35\mu\text{m}$ technology process. To ensure that power dissipation limits were not exceeded for elements and interconnecting lines, all transistors were operated well below their maximum power ratings and multiple vias were used for large current interconnects. To handle unexpected higher current density the width of interconnecting wires was designed slightly wider than the minimum requirement of design rules.

Latch-up can be avoided by using guard rings for transistors: In p-channel n well regions, an n^+ region has been placed and connected to the power supply. Similarly, in p regions, a p^+ region is placed and connected to global ground. In addition, the transistors that conduct large currents were surrounded by guard rings. These guard rings were connected to the substrate for n-channel transistors, or to the n well for p-channel transistors.

Coupling between adjacent elements causes unintended interaction between circuit elements. To reduce coupling between adjacent elements they were separated by several times the minimum allowable distance. Several ground and power pads were used to reduce the interaction of elements through the power lines. Pads also introduced pad parasitics

which lead to additional parasitic capacitances.

The G_m -C integrators were designed using the TSMC 0.35 μm technology. The layout area for each integrator was 70 μm X 63 μm , with testing pads the area expanded to 1131 μm X 260 μm as shown in Figure 4.2.

4.1.2 Simulation Results of Extracted Layout

The technology files from the IC layouts were submitted to the Canadian Microelectronics Corporation (CMC), and fabricated by the Taiwan Semiconductor Manufacturing Company (TSMC) in their 0.35 microns, 3.3 volt process. This process uses three layers of metalization, and floating poly-poly capacitors. The extracted layout contains all the parasitic capacitances added to the circuit in TSMC 0.35 μm technology. The extracted view of the design is closer to the real circuit after fabrication. Thus, the simulation results with parasitic capacitors can provide more important information of the performance of the real chip. Even with parasitic capacitance, the simulation results should be close to the original schematic simulation results. Both AC and DC analysis of the tunable integrator in Figure 3.14 are shown in Figure 4.3 and Figure 4.4 respectively. The main integrator extracted layout performance parameters are summarized in Table 4.1.

Table 4.1 Extracted Layout vs. Schematic Simulation Results

Parameters	Extracted Results	Schematic Results
Power Supply	3.3 V	3.3 V
Bias Current	1.2 mA	1.12 mA
DC Gain	22 dB	21 dB
Unity Gain Frequency	210 MHz~ 298 MHz	220 MHz ~ 300 MHz
Linearity Range	0.4 V _{p-p}	0.4 V _{p-p}
Control Voltage	1.50 V ~ 1.90 V	1.40 V ~ 1.90V

Figure 4.2 Layout of Tunable Integrator with Buffer.

Figure 4.3 Parametric AC Analysis of Extracted Layout of Tunable Integrator.

Figure 4.4 DC Response of Extracted Layout of Tunable Integrator.

4.2 Second-order IF Filter

This section presents the layout considerations, testing set-up, measurement procedures, experimental and simulation results for the tunable integrator-based second-order IF filter mounted in a Daico package. The performance of the circuit was measured in terms of the frequency tuning range, Q tuning range, third-order intermodulation (IM_3) and power dissipation. However, due to improper buffer bias setup, circuit operation was less than ideal. The large variations between the simulated and actual process parameters is also discussed.

4.2.1 Experimental Set-up and Measurement Procedure

The second-order G_m -C bandpass IF filter was fabricated using TSMC 0.35 μ m technology. The total layout area for the filter was 470 μ m x 1455 μ m, as shown in Figure 4.5. The test package for the G_m -C IF filter, mounted in a Daico package box is described in this section. The circuit was fabricated in TSMC 0.35 μ m technology in the form of a loose die and packaged in a CMC (Canadian Microelectronics Corporation) 20CFP surface-mount package as shown in Figure 4.6 and Figure 4.7. The substrate of the loose die was bonded to one layer which was connected to ground when mounted in the Daico package. The Daico package was a Daico Industries evaluation fixture package box with low package parasitics as shown in Figure 4.8. The surface-mount package with bonded G_m -C filter is mounted in Daico box to form a test package for the filter as shown in Figure 4.9.

An HP E3630A DC power supply was used to provide a 3.3 volt dc bias voltage, DC offset, dc control voltage, and reference voltage for the chip. A Rohde&Schwarz (100 KHz - 4320 MHz) signal generator with a 50 Ω output impedance was used to generate the input signal. A ZAPDJ-2 2-way power splitter with two ZFBT-4R2G bias-tees was connected to the signal generator to split the input signal and produce differential signals. The surface layer of the Daico package was shorted to ground resulting in the substrate of the loose die being connected to ground through bond wires. A diagram of the test set-up for the filter

Second order G_m -C Bandpass Filter

Figure 4.5 Layout of Second-Order G_m -C Bandpass Filter

Figure 4.6 Schematic of Surface-Mount Package with Filter Chip Loose Die Bonded.

Figure 4.7 Surface-Mount Package with the G_m -C Filter Chip Loose Die Bonded.

Figure 4.8 Daico Package Box.

Figure 4.9 Test Package For the G_m -C Filter. (The bonded surface-mount package mounted in Daico box)

is shown in Figure 4.10. A list of pin numbers and pin function is provided in Table 4.2. As

Table 4.2 Pin Number, Name and Description of Filter in Daico Package

Pin Number	Pin Name	Description
1	Vout ⁺	Positive Differential Filter Output PinC2

Figure 4.10 Schematic Diagram of Test Setup for the Filter

Table 4.2 Pin Number, Name and Description of Filter in Daico Package

Pin Number	Pin Name	Description
2	V_{DD}	Power Supply
3	V_{C2}	Frequency Tuning Control
4	V_{in}^-	Negative Differential Filter Input
5	V_{in}^+	Positive Differential Filter Input
6	V_{C1}	Gain Tuning Control

Table 4.2 Pin Number, Name and Description of Filter in Daico Package

Pin Number	Pin Name	Description
7	V_{ref}	Common-mode Feedback Reference
8	V_{C3}	Q Tuning Control

discussed in Section 3.3.1 (Chapter 3), the filter can be tuned by changing the control voltage. Both frequency and Q tuning can be achieved through the control voltage. Because the Diaco box did not have enough pins, only the positive differential filter output was connected to output port and connected to the analyzer.

There are several different possible ways to measure the output signal as shown in Figure 4.11. Figure 4.11 (a) shows resistor divider, the device output can be calculated by the

Figure 4.11 (a) Resistor Divider (b) Source Follower

equation $V_m = \frac{R_2}{R_1 + R_2} V_o$. For example if $R_1 = 450 \Omega$ and $R_2 = 50 \Omega$, then $V_m = V_o / 10$. In this way the circuit is loaded by a 500Ω resistor, yet the measurement setup is 50Ω . In this circuit, bandwidth is hardly affected by the measurement pad. Figure 4.11 (b) shows the source follower. The device output V_o can be calculated from the measured V_m from the following equation: $I_D = \frac{1}{2} \cdot \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{OM} - V_t)^2$ where $V_{OM} = V_o - V_M$ and $V_M / R_L = I_D$. A HP 8591E spectrum analyzer (9 KHz - 1.8 GHz) was connected to the output node of the filter buffer to measure the frequency response of the filter. The mod-

el of HP 8591E spectrum analyzer is shown in Figure 4.12 with a $50\ \Omega$ output resistance

Figure 4.12 Model of HP 8591E Spectrum Analyzer

in series with a coupling capacitor which was estimated to be $0.35\ \mu\text{F}$ by noting the lower cut off frequency was listed as 9kHz. Because of this AC coupling capacitor which was not accounted for in setting up the test equipment, no dc current could flow through the source follower transistor and as a result the output signal was attenuated. The test setup with the spectrum analyzer connected directly to the output of the filter buffer is shown in Figure 4.13. To avoid the attenuation introduced by the C_{gs} (estimated to be 160fF) of the source

Figure 4.13 (a) Measurement of filter with buffer. (b) Equivalent Circuit.

follower transistor and to supply the required DC bias current through the buffer, a modified

measurement setup should have been used and shown in Figure 4.14. The current through

Figure 4.14 Measurement Solution with Active DC basis Load

transistor M_2 and therefore the DC bias current could be changed by tuning V_{bias} .

In spite of the circuit being connected incorrectly, it still worked. Since C_{gs} was small it provided a high impedance which buffered the filter circuit. The output was attenuated, but otherwise showed the correct response.

4.2.2 Gain Correction

Because of the improper measurement setup, shown in Figure 4.13, no DC bias current could flow through the source follower which caused the gain of the output signal to be attenuated by 30dB. A comparison of simulated frequency and Q tuning response of V_m in Figure 4.11 (b) and Figure 4.13 is shown in Figure 4.15 and Figure 4.16. Both figures show that the shape of the frequency response was not affected by the C_{gs} of the source follower

(a) Simulated Frequency Tuning Response without Gain Loss

(b) Simulated Frequency Tuning Response with Gain Loss

Figure 4.15 Frequency Tuning Response Comparison

Figure 4.16 Q Tuning Response Comparison

transistor but the output gain dropped by approximately 30dB. Table 4.3 and Table 4.4

Table 4.3 Simulation Results of Two Measurement Setups, Frequency Tuning

Proper Setup (Figure 4.11(b))			Improper Setup (Figure 4.13)		
Freq (MHz)	Q	Gain (dB)	Freq dB	Q	Gain (dB)
159	7.9	18	158	7.93	-10
270	8.9	19	280	8.9	-12
320	10	20	320	10	-12

shows simulation results. In Figure 4.16, Q is quite different in (a) and (b) which tells us

Table 4.4 Simulation Results of Two Measurement Setups, Q Tuning

Proper Setup (Figure 4.11(b))			Improper Setup (Figure 4.13)		
Freq (MHz)	Q	Gain (dB)	Freq dB	Q	Gain (dB)
300	10.5	20	300	8.2	-10
300	8.3	12	300	4	-20
300	5.1	7	300	2.0	-16

that Q decrease when gain drops. A further discussion of the simulation results will be introduced in the next section. As we will see later, there was a total 40dB gain difference between the expected result and actual measured data. This 40dB attenuation came from 2 sources: (1) 30dB attenuation because of incorrect experimental setup, and (2) an extra attenuation of 6 dB is introduced by the loss in the cables, power splitters and bias Tees and 3 dB loss was estimated due to other sources. It has been observed that at 300 MHz significant loss can occur in the bond wires in the surface-mount package and the press contact between the surface-mount package and the Daico box. By adding a total of 39 dB gain correction to the experimental results of the bandpass filter, gain-corrected measurements were obtained.

4•3 Simulation and Measurement Results

Simulations, incorporating the extracted layout netlist and output impedance, were performed to provide an approximation to the expected measured results.

Figure 4.17 shows the simulation frequency response over three settings of the frequency control voltage with the actual (incorrect) setup as shown in Figure 4.12. The frequency control voltage was set to 1.40 V, 1.68 V and 3.3 V for the low (160 MHz), medium (280

Figure 4.17 Simulated Frequency Tuning Response with Improper Setup

MHz) and high (320 MHz) frequency response curves. The gain control voltage was set to 2.8 V. The Q control voltage is set to 1.46 V, 1.47 V and 1.47 V respectively for the three different frequency response curves as shown above. Figure 4.17 shows that because of improper buffer bias as discussed in Section 4.2.2 the simulated results were down by 30dB which is the main reason for the big gain loss for the filter.

Figure 4.18 shows the actual measured frequency response over three settings of the frequency control voltage. The frequency control voltage was set to 1.46 V, 1.68 V and 3.0 V for the low, medium and high frequency response curves. The gain and Q control voltage at each frequency was adjusted to provide an approximate gain of -20 dB. The gain control voltage was set to 2.8 V and the Q control voltage was set to 1.46 V, 1.47 V and 1.47 V respectively for the low, medium and high frequency response curves.

Figure 4.18 Measured Frequency Tuning Response

The measured results are in good agreement with the simulated results in terms of frequency tuning response. The tuning range for the simulated results in Figure 4.17 is 160 MHz from 280 MHz to 320 MHz. The tuning range for the measured results in Figure 4.18 is 160 MHz, from 230 MHz to 310 MHz. Simulation and measured results agree when a 10dB gain correction as discussed in Section 4.2.2 is included.

Figure 4.19 shows the simulated Q tuning response of the filter. The frequency control voltage was set to 3.3 volts, and the gain control voltage was set to 2.8 V. The Q control voltage was set to 1.47 V, 1.40 V and 1.0 V for the high, medium and lower Q curves. The

Figure 4.19 Simulated Q Tuning Response with Spectrum Analyzer Model

high Q curve has a value of -10.5 dB and the low Q curve has a value of -26 dB. Figure 4.19 shows that with the gain correction as discussed in Section 4.2.2, it agree with the simulation results shown in Figure 4.19.

Figure 4.20 shows the measured Q tuning response of the filter. The frequency control voltage was set to 3.3 volts, and the gain control voltage was set to 2.8 V. The Q control voltage was set to 1.47 V, 1.40 V and 1.0 V for the high, medium and lower Q curves. The high Q curve has a value of -20dB and low Q curve has a value of -40.5 dB. The Q value of the filter can be tuned by changing the control voltage which is in agreement with simulation. In terms of the gain the agreement is good once the gain corrections as specified earlier in Section 4.2.2 are applied.

Figure 4.20 Measured Q Tuning Response

A comparison of the simulated and measured frequency tuning data is presented in Table 4.5. A comparison of the simulated and measured Q tuning is shown in results of Table

Table 4.5 Frequency Tuning Results of Simulations and Measurements

Setup			Simulations		Measurements		
V_{C1} (volt)	V_{C2} (volt)	V_{C3} (volt)	FC (MHz)	Gain (dB)	FC (MHz)	Gain (dB)	Corrected Gain (dB)
2.8	1.46	1.46	159	-10	160	-22	-13
2.8	1.68	1.47	271	-8	230	-20	-11
2.8	3.0	1.47	320	-9	310	-21	-12

4.6. The measured gain of the filter agrees with the simulated gain again if gain correction

Table 4.6 Q Tuning Results of Simulations and Measurements

Setup			Simulations			Measurements			
V_{C1}	V_{C2}	V_{C3}	FC	Gain	Q	FC	Gain	Corrected Gain	Q
volt	volt	volt	MHz	dB		MHz	dB	dB	
2.8	3.3	1.47	320	-10	10	300	-20	-11	10
2.8	3.3	1.40	320	-20	8.9	305	-30	-21	9.3
2.8	3.3	1.0	320	-25	5.0	310	-40	-31	8.4

discussed in Section 4.2.2 is included. The difficulty in measuring differential outputs is the mismatch of simulation results and measurement results. Only one filter output could be measured leaving the other output floating because of the Daico package box output ports results the mismatch of output impedance.

The simulated results for both frequency tuning and Q tuning response are in good agreement with the measured results when the 39 dB gain correction is included. A 30 dB gain loss out of 39 dB can be corrected by using proper buffer bias as shown in Figure 4.14. By changing the bias voltage at the gate of transistor M_2 , the dc bias current flowing through the source follower transistor M_1 can be tuned to meet the requirement.

CHAPTER 5

Conclusions and Recommendations

5.1 Conclusions

The design of a fully-integrated tunable bandpass G_m -C IF filter was presented in this thesis. It was successfully implemented in a CMOS 0.35 μ m technology from TSMC and achieved operation in the megahertz range. Reasonable frequency and Q tuning was demonstrated.

Simulations of linearity performance of three different G_m -C integrator were performed. The first and second G_m -C integrators were passive, resistor-based circuits. Small-signal simulations were performed to study the frequency responses of the integrators. Large signal simulations were performed to compare the IP_3 values of the two circuits which indicated that 5 dB improvement of IP_3 was possible by using the enhanced circuitry. It was determined that low voltage gain at the output did not improve linearity because the linearity of the integrator was limited at the input as discussed in Chapter 3. A transistor-based integrator was explored because it had the advantage of tunability while the resistor-based integrator did not. It was found that there was not much linearity difference between the passive resistor-based and transistor-based integrator. The IF filter was implemented based on this tunable integrator. A source follower buffer was added to the filter as a buffer to drive a 50 Ω load. Small-signal simulations after layout and extraction were also performed. This experiment demonstrated the importance of a complete process and parasitic capacitance simulation before sending the circuit out for fabrication. Simulation results of the 1dB compression point of the filter indicated that the linearity performance of the overall IF filter was reasonable.

Measurements of the tunable IF filter involved the integrated filter packaged in a surface-mount package and an 8 pin Daico electronics package box. Several problems were encountered during the testing of the filter. These were:

- (1) The filter needed at least 10 pins connection while the Daico package box had only 8 pins and so only one of the differential outputs was connected resulting in signal loss and increase in noise. The other output was not connected.
- (2) The frequency response of the filter was measured by the HP 8591E spectrum analyzer (9 KHz - 1.8 GHz). Unfortunately, the output buffer was improperly biased resulting in a 30 dB gain loss at the output of the filter. The attenuation of the power splitter, bias Tees, all cables and all Daico box connections and bond wires was estimated to be approximately 9 dB. Overall, a total gain correction of 39 dB was introduced.

The center frequency of the filter could be tuned by changing the control voltage of the integrator. The frequency response was in good agreement with the simulation results with center frequency tunable from 160MHz to 310MHz. The Q tuning of the filter resulted in a gain change range of 20dB. This was in good agreement with simulation. This measurement indicates how important it is to simulate with all testing equipment parameters included. Also, set-up is one of the key things for the simulation to be in agreement with the real chip measurement. Design should include consideration of how testing will be done otherwise, test results could be quite different from expected.

5.2 Recommendations and Future Work

It is important for any designer to do initial research into radio system requirements and system architecture which will help to focus the design task as well as provide more specifications to work towards. The study of the SAW filter and its capabilities in terms of frequency response and linearity provide a starting point for a filter designer.

The research of the three different Gm-C integrators also suggests a method of linearity improvement as well as a way towards tunability. The fully-integrated CMOS Gm-C IF filter demonstrated a well behaved frequency and Q tuning response in simulations though this tuning was achieved manually. Further work in this area should include the design of a higher-order filter which can provide a sharper transition between passband and stopband. The linearity of this type of tunable filter is poor because of the nonlinearity of a transistor based resistor. Further

study of the MOSFET based resistor is recommended as it may be possible to increase the linearity of the circuit while maintaining the tunability. This circuit was differential which should have improved noise performance, including power supply variations. however, the circuit was not tested differentially. Future work could be done with 0 degree and 180 degree power combiners to allow differential measurement.

In the event of a redesign, special attention should be paid to increasing the linearity. The increase of linearity can be accomplished by the following approaches:

- (1) Add a external load resistor to the output, or replace the output source follower by an adjustable output buffer as shown in Chapter 4 Figure 4.14. This would allow adjustment of the current in the output source follower.
- (2) Automatic frequency tuning is required to provide channel selection and to account for process variation. An automatic Q-tuning circuit is also required to compensate for shifts in the process and the dependence of Q on center frequency.
- (3) Design a complete IF filter by using a multiple resonators. Measured results indicated that Q of 10 could be achieved. This will not be sufficient for a complete IF filter, so Q enhancement techniques should be considered.

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