FREQUENCY MULTIPLICATION TECHNIQUES FOR
SUB-HARMONIC INJECTION LOCKING OF LC OSCILLATORS AND
ITS APPLICATION TO PHASED-ARRAY ARCHITECTURES

By

Yasser Khairat Soliman, B.Sc., M.A.Sc.

A thesis submitted to the
Faculty of Graduate and Postdoctoral Affairs
in partial fulfillment of the requirements for the degree of
DOCTOR OF PHILOSOPHY
in
ELECTRICAL ENGINEERING

Ottawa-Carleton Institute for Electrical and Computer Engineering

Carleton University

Ottawa, Ontario, Canada

© Yasser KH. Soliman, 2013

Abstract

A frequency multiplication and phase steering technique that utilizes the injection locking phenomena of LC local oscillators (LO) is reported. The potential application of this technique to LO-path based phase-shifting in RF/millimeter-wave integrated phased-array architecture is proposed. Advantages and disadvantages of the proposed technique are discussed in reference to those of the recently reported architectures in the literature. A high-order harmonic synthesis approach is introduced at the core of the proposed frequency multiplication technique for which a mathematical formulation is provided to highlight the underlying principles and trade-offs. Architectural variations on the high-order harmonic synthesis approach are also introduced and contrasted. The proposed multiplication and phase steering techniques have been investigated and prototyped in a main stream 130-nm CMOS process. Simulation and measurement results of the prototype are provided to substantiate the proposed techniques. Measurement results include output phase noise performance of -115 and -107.17 dBc/Hz, maximum phase shift errors of 2.35° and 2.1° after calibration, extracted peak-to-null ratios of > 28 dB and current consumptions of 26.8 mA and 30.3 mA at 18.31 GHz and 21.51 GHz, respectively.

*He that spared not his own Son, but delivered him up for us all, how shall
he not with him also freely give us all things? (Romans 8:32)*

Acknowledgement

I would like to thank my friends and colleagues who contributed to the completion of this work. First and for most, I wish to thank Professor Ralph Mason not only for giving me the opportunity to pursue my academic studies in a field that I have always been interested in, but also for his patience, guidance and support throughout the entire research program. Ralph, thanks for quietly teaching me by example how someone can be very hard working, extremely efficient and organized while maintaining a good balance and enjoying.

I would like to thank the faculty members, staff, fellow graduate students and alumni in the Department of Electronics who have always been there to listen, help and give advice. I wish to thank Professor Calvin Plett for giving me the opportunity to become the graduate RFIC course TA. It certainly was a great learning experience which provided me with the necessary research foundation for a field that I always dreamed to be in. I acknowledge the hardware and computer networking support of Mr. Nagui Mikhail and Mr. Scott Bruce. I am grateful to the enormous help and support of our amazing departmental administrator, Ms. Blazenka Power, and our wonderful graduate assistant, Ms. Anna Lee. I also wish to thank my fellow graduate colleagues, Bachir Tamer, Kimia Ansari, Tony Forzley, Irfan Ahmed, Ramin Shariat, A. Ahmed and Reza Youssefi who made this research period enjoyable.

I wish to thank my early mentors in life, Adel Ishak, Mamdouh Helmy, Karam Eleya, Galal Saeed, Samir Yousef, Mounir Halim and Bahgat Samaan. I also wish to thank those who have continuously been helping and supporting me during this work, H.H.P. Kyrillos VI, St. Mina and St. Mary.

To my daughter, Joy, the time has come that I can enjoy listening to you play the piano, watching you dance or paint our life with your joyful colours. To my son, Jonathan, the time has also come that I can enjoy listening to your daily innovations and help you make them come true. To you both I say, now I realized why I am here!

My most sincere thanks are reserved to my wife, Tay, who sacrificed her family and career to

provide me with her unconditional support and love. Thank you so much for showing me, one more time, how someone's life could be fully devoted for unconditional giving.

At last, I thank my Lord and good savior, Jesus Christ, for bringing me through this experience; to Him be all the glory.

Table of Contents

Abstract	ii
Acknowledgement	iv
Table of Contents	vi
List of Tables	ix
List of Figures	x
1 Introduction	1
1.1 Research Motivation and Objectives	1
1.2 Thesis Organization	2
2 Radio Frequency Integrated Phased-Array Transceivers and Their Architectures: A Review	4
2.1 Advantages of Phased-Array Transceivers	5
2.2 Selected Applications of Array Transceivers	8
2.3 Coherent Combining Principles in Electronically Steerable Phased-Array Architectures	9
2.3.1 Array Factor	12
2.3.2 Spatial Filtering in Phased-Arrays	15
2.3.3 Space Diversity Signal Combining versus Array Processing and Beamforming	16
2.4 Phased-Array Architectures	17
2.5 Local Oscillator Based Phase Shifting Schemes for Coherent Combining in Phased-Array Architectures	20
2.6 Summary	28
3 Injection Locking of LC-Oscillators and Higher Harmonic Synthesis	31
3.1 Frequency and Phase Locking in LC-Oscillators by Injection	31
3.2 Phase-lock Stability and Beat Oscillation Modes	35
3.3 Frequency Multiplication Techniques	37
3.4 High-order Harmonic Synthesis for Injection Locking and Frequency Multiplication	38

3.4.1	Harmonic Synthesis by resembling a Square-wave	39
3.4.2	Time-delays of a Square-wave and Phase Angles of its Harmonics	40
3.4.3	Rise- and Fall-time of a Non-ideal Square-wave and its Harmonic Content	40
3.4.4	Duty-cycle and the Relative Magnitudes of the Harmonics	41
3.5	Summary	45
4	Proposed LO-Path Phase-Shifting Architecture	46
4.1	Proposed Architecture	46
4.2	Details of the LO-Path Phase Shifting Operation	48
4.3	Architecture Building Blocks	50
4.3.1	Quadrature phase synthesis and Cartesian Phase Shifters	51
4.3.2	High-order Harmonic Synthesis	57
	Circuit Analysis and Design	59
	Noise Considerations	63
	Architecture Variations and Trade-offs	64
4.3.3	Current injectors and the LC-VCO Design	69
4.3.4	Output Buffers	74
4.4	Simulations Results of the Complete Architecture	80
4.5	Calculation of the Injection Locking Bandwidth and Injection Strength	84
4.6	Summary	90
5	Isolation of LO-Elements on Silicon	92
5.1	Potential Coupling Scenarios in the LO-phase Shifting Architecture	92
5.2	Isolation Techniques Adopted and Simulations	94
5.2.1	At The Active Device Level	94
5.2.2	At The Technology And Process Level	94
5.2.3	At The Passive Device Level	96
5.3	Summary	101
6	Phase Calibration Techniques	102
6.1	Phase Shift Mismatches in the Proposed Architecture	102
6.2	Phase Shift Calibration	103
6.3	Calibration Sensitivity Analysis	105
6.3.1	Sensitivity to Oscillator Quality Factor	105
6.3.2	Sensitivity to the Oscillator Tail Current	106
6.3.3	Sensitivity to the Injection Strength	110
6.3.4	Sensitivity to Phase-Interpolator I & Q Weights	111
6.4	Summary	114
7	Prototype Implementation and Measurement Results	115
7.1	Measurement Setup and Results	117
7.1.1	Free Running Oscillator and Tuning Range	119
7.1.2	Measurements of the High-order Harmonic Synthesis Stage	122
7.1.3	Injection Locking Range Measurements	125

7.1.4	Testing a Variation on the Proposed Frequency Multiplication Technique . . .	128
7.1.5	Phase Noise and Integrated Jitter Measurements	129
7.1.6	Phase Shift Measurements of One LO-element and the Associated Beam Steering Results	132
7.1.7	The Effect of Phase Steering on the Phase Noise Performance	136
7.1.8	Sensitivity of Phase Shifts to Oscillator Core Tail Current	140
7.1.9	Sensitivity of Phase Shifts to Phase Interpolator Cartesian Weights	141
7.2	Measurements of the Edited Chip	142
7.2.1	Tuning Range and Injection Locking Bandwidth Measurements	144
7.2.2	Measurements of the Isolation between the two LO-elements at 21 GHz . . .	145
7.2.3	Phase Shift Measurements of the Two LO-elements and the Associated Beam steering Results at 21 GHz	149
7.2.4	Phase Noise Performance Measurements and Its Sensitivity to Phase Steering	150
7.3	Comparison to Integrated LO-Path Phased-Array Architectures from Literature . .	155
7.4	Summary	160
8	Conclusion	163
8.1	Thesis Contributions	165
8.2	Future Work	167
Appendix A Extraction Formulae for the Double-π Inductor Model Parameters		169
Appendices		169
Appendix B Layout Views of the Fabricated Building Blocks		172
Bibliography		177

List of Tables

2.1	A qualitative comparison summarizing the advantages and disadvantages of LO-path based phase shifting techniques in phased-array architectures	29
2.2	A qualitative comparison summarizing the advantages and disadvantages of LO-path based phase shifting techniques in phased-array architectures (Continued) . .	30
4.1	Interpolation regions for the second stage PI	56
4.2	Active and passive device sizes as implemented in the harmonic synthesis block in Fig.4.14	63
4.3	A comparison between the three harmonic synthesis approaches	65
4.4	Active and passive device sizes and current consumption as implemented in current injectors, LC-VCO and buffers in Fig. 4.14	72
4.5	Geometric parameters for the symmetrical spiral inductor in place of the T-coil transformer in Figure 4.28.	79
4.6	A list of the fitting parameters for the distributed circuit model shown in Figure 4.29.	79
4.7	Device sizes and current consumption as implemented in the output buffer stages in Fig. 4.26	80
4.8	A summary of the simulation results obtained	88
5.1	Extracted parameters for the double- π inductor model in Figure 5.7.	100
7.1	Frequencies of Potential Interferers	125
7.2	Comparison to similar works from literature	159

List of Figures

2.1	A system-level illustration of a combining stage in an array receiver.	6
2.2	An n -element linear array receiver with its elements located on the z -axis and spaced apart by a constant distance d . The wave-front of the propagating plane-wave signal progressively excites the array elements at different time instants. A conceptual delay-and-sum RF stage is adopted to combine the received RF signals.	9
2.3	Example of a true time-delay, τ_k , and its equivalent phase shift, ϕ_k , at a carrier frequency, $\omega_c = 2\pi f_c$	11
2.4	Illustration of the required phase shift for a pure time delay versus the constant phase shift approximation across a finite bandwidth.	12
2.5	An illustration of beam steering results for a 8-element uniform linear array and $\lambda/2$ separations between the elements. Three arbitrary beam patterns are shown in response to progressive phase shifts $\varphi = \Delta\phi$ of $[0^\circ, -90^\circ, -180^\circ, \dots]$, $[0^\circ, 0^\circ, 0^\circ, \dots]$ and $[0^\circ, 90^\circ, 180^\circ, \dots]$	13
2.6	Beam patterns for 4-, 8- and 12-element arrays with a $\lambda/2$ separation. It is seen that increasing the number of elements decreases the main lobe beamwidth which increases the directivity. The number of pattern nulls and the sidelobes increases with the associated sidelobe levels decaying faster.	14
2.7	Beam patterns for 8-element arrays with $\lambda/4$, $\lambda/2$ and λ separations. As the inter-element spacing increases, the main lobe beamwidth decreases with an increasing number of sidelobes. When $d = \lambda$, the level of the grating lobes at $\theta = \pm 90^\circ$ becomes as high as the main lobe.	15
2.8	An illustration of the null steering results for a 8-element uniform linear array and $\lambda/2$ separations between the elements. The synthesized complex weights are for an initial -25 dB Chebychev pattern with two adjacent nulls placed over the 27° to 32° sector.	16

2.9	Architectural variations in phased-array receivers where the required phase shifting for coherent combining can be realized in (a) the RF/millimeter-wave signal domain, (b) the IF domain, (c) the base-band or digital domain or (d) the LO domain.	19
2.10	A continuous LO-based phase shifting scheme in integrated phased-array architectures.	20
2.11	The LO-based phase shifting scheme adopted in [1] for an integrated phased-array architectures. A centralized multi-phase millimeter-wave PLLs is employed for the generation of 16 phases of a 19.2 GHz LO. In this architecture, the 16 (or, 8 differential) LO phases are distributed to each of n 16 : 1 phase selectors in a symmetric binary tree structure, where n is the number of array elements.	22
2.12	A refinement to the LO-based phase shifting scheme in [1] (Fig. 2.12) where millimeter-wave phase rotators are employed at each front-end location to generate the desired LO phase shift locally avoiding the need to distribute multiple LO phases to n array elements [2].	23
2.13	A unilateral injection locking based LO-path phase shifting architecture. A low phase-noise RF signal is optically distributed to injection-lock a cascade of two millimeter-wave oscillators in each array element. The phase shifting is obtained by controlling the center frequency of the resonator in each $f_0/2$ oscillator through DC biasing (V_{tune}).	24
2.14	An unconventional injection-locked PLL (ILPLL) built around a MESFET push-pull self-oscillating mixer. The high conversion gain of the mixing operation enabled the architecture to exclude frequency multipliers or dividers prior to the PLL phase comparison stage.	25
2.15	Bilateral injection-locking of oscillators and its application to LO-path phase shifting in phased-array architecture. Oscillators are bilaterally coupled to their nearest neighbours forming a “coupled-oscillator array” where a uniform division of the pre-determined phase shift, $(N + 1)\Delta\phi$, along the array is possible and hence the potential for beam steering applications.	26

2.16	A scalable phased-array transmitter architecture based on integrated coupled-oscillator arrays [3]. The top level architecture is shown in (a). The in- and quadrature-phases of the third sub-harmonic - relative to the carrier - are used as the bilateral inter-injection locking signals among the coupled array cells. The details of each array cell is shown in (b) where the inter-injection locking signals are re-synthesized at each array LO-element.	27
3.1	A model for an LC oscillator under current injection. The nonlinearity in the active device is captured through its voltage dependant conductance, $G_d(V)$. The oscillator loading is in the purely real admittance, Y_L . The reactive loading of the oscillator is assumed to be lumped into the oscillator LC tank.	33
3.2	Phase transient acquisition process	35
3.3	Tangential (left) and absolute (right) phase variations of an LC-oscillator output under injection in the quasi-lock and fast beat modes as expressed by (3.2.1). . . .	36
3.4	Output spectra of an LC-oscillator under injection in the quasi-lock mode with higher- (left) and lower-side (right) injection cases depicted.	37
3.5	Output spectra of an LC-oscillator under injection in the fast beat mode with higher- (left) and lower-side (right) injection cases depicted.	37
3.6	An illustration of a square-wave signal synthesis through a progressive accumulation of the constituting harmonics in its Fourier series representation. The incremental addition of the harmonics with the correct amplitude and phase spectra results in an enhancement of the rise and fall times and in amplitude saturation. . .	39
3.7	A trapezoidal wave resembling a square wave with non-zero rise- and fall-time. . .	40
3.8	The normalized attenuation of the magnitudes of odd harmonics contained in the trapezoidal signal in Fig. 3.7 as a function of its normalized rise- and fall-time. The normalization of the rise- and fall-time is calculated relative to the period of the fundamental, τ	42
3.9	A periodically repeated ideal rectangular pulse with a δ pulse width.	42

3.10	A comparison between the relative magnitudes of Fourier coefficients for the fundamental and the ninth harmonic components of an ideal rectangular pulse with $0 < \beta < 1$. The pulse-width compression case (i.e. $\varepsilon = \beta\tau/\nu_d$) may, at its best, yield identical odd harmonic magnitudes to that in the $\varepsilon = \beta\tau$ case. The magnitude of the fundamental can be reduced by about 82% at $\beta = 0.5$ without affecting that of the targeted harmonic if the duty cycle of the rectangular pulse is chosen such that $\varepsilon = \beta\tau/\nu_d$	44
4.1	Proposed Architecture.	47
4.2	Fundamental phase locking.	49
4.3	Sub-harmonic phase locking.	49
4.4	One phase interpolator basic cell architecture.	51
4.5	A schematic showing the two successive RC-CR polyphase filter stages.	52
4.6	Worst-case phase shift variations among the outputs of the two-stage RC-CR polyphase filter with temperature and process variations.	53
4.7	Worst-case amplitude mismatch percentage error between the in-phase and the quadrature phase outputs of the two-stage RC-CR polyphase filter with temperature and process variations.	53
4.8	A two-stage cartesian phase interpolator architecture to accompany the i^{th} LO-element.	54
4.9	An illustration of the vectorial current summation in the first (a) and second stage (b) phase interpolators (PI). In (b), The two summed components are those resulting from the first PI stages with angles $\Omega_{i,1}$ and $\Omega_{i,2}$	55
4.10	Schematics of the cartesian phase interpolation cells in the first (a) and the second (b) stages of the phase interpolator. The topology of the current-steering DAC in the second interpolation stage is also shown in (b).	55
4.11	Illustration of the three interpolation regions to keep the bias currents ratios and the corresponding g_m weights within the most linear range of the second stage enabling the architecture to avoid the non-linearities that would otherwise occur at the boundaries where bias current weights differ by large amounts.	56
4.12	Output phase errors obtained from the two stage phase shifter.	58
4.13	Schematics of the pre-amplifier stages in (a) and the high-speed latch in (b).	58

4.14	A zoomed in schematic showing the latch, its input transconductance and the cascode transconductance following it. The equivalent small-signal schematic is also shown where the input transconductance is included via the differential current source. Except for the inductive peaking load, all other single ended capacitive and resistive loads at nodes X and Y are lumped into G and C_D , respectively.	60
4.15	Schematics of the pre-amplifier stages in (a), the high-speed latch in (b) and the Q-enhanced tuned amplifier stage in (c).	64
4.16	A single-ended time domain signal and its frequency content at the output of the high-speed latch as obtained from a periodic steady-state (PSS) simulation.	66
4.17	Shown at the top are the single-ended time-domain signals at the latch output and the Q-enhanced filter following it. The frequency content of the Q-enhanced filter output is shown at the bottom. Results are obtained using a periodic steady-state (PSS) simulation.	66
4.18	Shown at the top is the single-ended time-domain signal at the output of the Q-enhanced filter directly following the preamplifiers in the third approach. The frequency content of the Q-enhanced filter output is shown at the bottom. Results are obtained using a periodic steady-state (PSS) simulation.	67
4.19	Phase noise profiles of the three high-order harmonic synthesis approaches without the phase shifter or the VCO connected.	68
4.20	Phase noise profiles of the three high-order harmonic synthesis approaches with the phase shifter and VCO connected.	68
4.21	Schematics of the injection transconductor, the negative- g_m oscillator and buffers.	69
4.22	Single-ended variable capacitance range and associated Q values of the combined thin and thick oxide nMOS varactors. The capacitance range has been obtained in simulations by continuously varying the control voltage of the thick oxide nMOS varactor (DGncap) while keeping that of the thin oxide nMOS varactor (ncap) constant at 1, 1.1 and 1.2, V.	73
4.23	Differential inductance and quality factor as extracted from a two port simulation of the symmetrical tank inductor.	74
4.24	The oscillator tuning range as obtained in simulations by continuously varying the control voltage of the thick oxide nMOS varactor (DGncap) while keeping that of the thin oxide nMOS varactor (ncap) constant at 1, 1.1 and 1.2, V.	75

4.25	Simulated phase noise performance of the oscillator while connected to the injection transconductance stage and buffers.	76
4.26	Detailed schematics of the two buffer stages and output T-coil network.	76
4.27	(a) Input capacitance of the f_T doubler stage, (b) Output T-coil network with parasitic loading elements.	77
4.28	T-coil structure realized as a symmetric spiral inductor with its center tap representing the input terminal X	78
4.29	A distributed model for the T-coil structure when realized as a symmetric spiral inductor.	78
4.30	Total differential inductance and quality factor of the symmetrical spiral inductor in place of the T-coil transformer as extracted from a two port ADS Momentum EM simulation.	80
4.31	Superimposed time-domain waveforms individually obtained through periodic steady-state simulations. Each waveform corresponds to a locked oscillator output to a separate phase-shifter state as outlined in Section 4.3.1.	81
4.32	Obtained versus desired phase shifts and the associated maximum phase errors before and after calibration for <i>approach 1</i> (top) and <i>approach 3</i> (bottom).	82
4.33	Peak-to-peak time and phase deterministic jitter as obtained from 15 separate phase shift simulations between 0 and 2π with 22.5° steps.	83
4.34	Variations of the phase noise floor performance at 100 KHz, 1 MHz and 10 MHz offsets across the whole span of 0 to 2π phase shifts attained.	83
4.35	Oscillator output spectrum under a fundamental tone injection with $\Delta\omega_{inj}/2\pi = 100\text{ MHz}$ (top) and the details of the locations of the sidebands (bottom).	86
4.36	Oscillator output spectrum in a quasi-lock mode under square-wave injection with $\delta\omega_{inj}/2\pi = 125\text{ MHz}$	87
4.37	A locked oscillator spectrum with $\omega_{inj}/2\pi = 18.046\text{ GHz} + 116\text{ MHz} = 18.162\text{ GHz}$	88
4.38	Oscillator output spectrum in a quasi-lock mode under square-wave injection with $\delta\omega_{inj}/2\pi = -112\text{ MHz}$ (top) and a locked oscillator spectrum with $\Delta\omega_{inj}/2\pi = -111\text{ MHz}$ (bottom).	89
5.1	Potential Coupling channels in the proposed LO-phase phase-shifting architecture.	93
5.2	A block diagram of two LO-elements separated by Moat areas.	94

5.3	Location of Moat areas on chip (top) and a resulting conceptual schematic and test bench (bottom).	95
5.4	Floating patterned metal shields under the VCO tank inductor.	97
5.5	A 3-D view of the differential two-port coupling model for the two oscillator tank inductors in ADS Momentum atop of a silicon substrate for the tank inductors. . .	98
5.6	Magnitudes of the forward transmission coefficient, $ S_{21} $, as obtained in simulations for i) two oscillators' differential tank inductors and ii) two LC tank resonators. Two mutually coupled double- π inductor models were used based on the s-parameters data obtained from Momentum EM simulations in Figure 5.5. The inductors center-to-center separation distance, S , was varied between 341, 682 and $1364\ \mu\text{m}$	99
5.7	A compact broadband inductor model.	100
5.8	Test bench used for evaluating the LC tank resonators coupling based on the two-port S-parameters data obtained from EM simulations in Figure 5.5. The inductor coupling model uses two mutually coupled double- π inductor models (Fig. 5.7) with coupling coefficient K values $0.9\text{E-}3$, $70\text{E-}6$ and $1.25\text{E-}6$ corresponding to $S = 341, 682$ and $1364\ \mu\text{m}$, respectively.	100
6.1	Resulting phase offset, θ_i , as a function of Q_i , the injection strength, $ I_{inj,i} / I_{osc,i} $ and the relative injection bandwidth $(\omega_{0,i} - \omega_i)/\omega_{0,i}$. The arrow indicates the direction of increasing Q	105
6.2	Effect of the input impedance of the compensated oscillator tank as seen by the injection transconductor at resonance.	106
6.3	A time-domain representation of the relationship between I_{osc} and I_{ss} in a tail-biased negative-gm oscillator.	107
6.4	A plot showing the sensitivity of the LO-element output phase to changes in the core oscillator current, $\partial\phi_{ss,i}/\partial I_{ss,i}$, as a function of the injection frequency offset, $\Delta\omega_i$, for tank quality factors, $Q = 5, 7$ and 10	108
6.5	Simulated output phase sensitivity to changes in the tail oscillator current, $\Delta I_{ss,i}$ and the associated phase noise variations.	109
6.6	A plot showing the sensitivity of the LO-element output phase to changes in the injection transconductor tail current, $\partial\phi_{ss,i}/\partial I_{ssinj,i}$, as a function of the injection frequency offset, $\Delta\omega_i$, for tank quality factors, $Q = 5, 7$ and 10	111

6.7	A plot showing the sensitivity of the phase offset to changes in the phase interpolator quadrature current weight, $d\theta_i/dI_{Bias,Q_i}$, as a function of the injection bandwidth, $\Delta\omega_i$ for tank quality factors, $Q = 5, 7$ and 10	112
6.8	Simulated output phase sensitivity to I_{Bias,Q_i} with lower-side injection and the associated phase noise performance variations.	113
7.1	A layout view of the $2\text{ mm} \times 2\text{ mm}$ chip along with a description of the probing pads located on its four sides.	116
7.2	Micrograph of the $2\text{ mm} \times 2\text{ mm}$ fabricated prototype chip.	117
7.3	The frequency and time-domain measurement setup for the two LO-elements which were implemented on the prototype chip. Except for the cartesian phase shifter bias current weights, $I_{Bias,I,Q}$, DC biasing details have been omitted for clarity. . .	118
7.4	Example of the measured free running oscillations spectra in 18 GHz	120
7.5	Example of the measured free running oscillations spectra in 18 GHz	120
7.6	Measured tuning range as a function of the the thick oxide varactor control voltage, $V_{ctrl,DGncap}$ for four thin oxide varactor settings.	121
7.7	Measured spectra of the multiplier output <i>without</i> the oscillator enhancement effect using one of the FT doublers buffer outputs.	123
7.8	Measured spectra of the LO-element output with the oscillator enhancement in effect as obtained separately using the individual outputs of the FT doubler buffer. . .	124
7.9	A quasi-lock case as obtained in measurements using $\Delta\omega_{inj}/2\pi = -160\text{ MHz}$ to lock one LO-element with its oscillator free running at $\omega_0/2\pi = 18.151\text{ GHz}$ using a ninth subharmonic reference. $\omega_b/2\pi \approx 27\text{ MHz}$ is obtained evidencing a single-sided locking range of approximately 157 MHz at an injection power level of $P_{inj} = -1.5\text{ dBm}$	126
7.10	A quasi-lock case as obtained in measurements using $\Delta\omega_{inj}/2\pi = -137\text{ MHz}$ to lock one LO-element at $\omega_0/2\pi = 18.227\text{ GHz}$ using an eleventh subharmonic reference. $\omega_b/2\pi \approx 30\text{ MHz}$ is obtained evidencing a single-sided locking range of approximately 133 MHz at an injection power level of $P_{inj} = -1.5\text{ dBm}$	127
7.11	Measured locking ranges for the ninth and the eleventh subharmonic references used versus the input power level.	127
7.12	Measured spectra of the multiplier output <i>without</i> the oscillator enhancement effect using one of the FT doublers buffer outputs.	129

7.13	(a) Measured phase noise performance of an LO-element at 18 GHz when it was injection locked to an up multiplied ninth subharmonic reference at 2 GHz. The recorded phase noise is -102 dBc/Hz and -105 dBc/Hz at 10 KHz and 100 KHz offsets from a 18 GHz carrier, respectively. (b) Measured phase noise profile of the reference signal generator at 2 GHz.	130
7.14	(a) A comparison between the output phase noise of an LO-element with its oscillator initially left freely running at 18.31 GHz and when it was injection locked using Agilent (E4432B) signal generator. (b) Phase noise measurement of the injection signal source at $18.31 \text{ GHz}/9 = 2.035 \text{ GHz}$	131
7.15	Measurement of the integrated RMS phase jitter as calculated by the spectrum analyzer with its maximum integration limits between 100 Hz and 100 MHz.	132
7.16	Superimposed time-domain waveforms individually obtained through time-domain measurements. Each waveform corresponds to a locked oscillator output to a separate phase-shifter state as outlined in Section 4.3.1.	134
7.17	Obtained versus desired phase shifts and the associated phase errors before and after calibration as measured for one LO-element at 18.27 GHz (top) and those from simulations (bottom). The maximum phase shift errors as obtained from measurements are 8.5° and 2.35° before and after calibration, respectively.	135
7.18	Phase steering results for 4-element arrays based on the phase shifts obtained from measurements with and without calibration and how they compare to the ideal case. Phase shift sequences used are (a) $[0^\circ, -22.5^\circ, -45^\circ, \dots]$, (b) $[0^\circ, 45^\circ, 90^\circ, \dots]$, (c) $[0^\circ, -90^\circ, -180^\circ, \dots]$ and (d) $[0^\circ, 90^\circ, 180^\circ, \dots]$	136
7.19	Phase steering results for 8-element arrays based on the phase shifts obtained from measurements with and without calibration and how they compare to the ideal case. Phase shift sequences used are (a) $[0^\circ, -45^\circ, -90^\circ, \dots]$, (b) $[0^\circ, 45^\circ, 90^\circ, \dots]$, (c) $[0^\circ, -135^\circ, -270^\circ, \dots]$ and (d) $[0^\circ, 135^\circ, 270^\circ, \dots]$	137
7.20	Measurement of the effect of phase steering one of the oscillator outputs on its phase noise performance while injection-locked to the 9^{th} harmonic of the distributed reference.	138
7.21	A comparison between two measured phase noise profiles for a locked LO-Element at 0° and 337.5°	139
7.22	Measured versus simulated Δ phase-steps as a function of percentage $\Delta I_{ss,i}$ changes and the accompanying variations in the phase noise measurements.	140

7.23	Measured versus simulated Δphase – steps as a function of percentage $\Delta I_{\text{Bias}_{Q,i}}$ changes and the accompanying variations in the phase noise measurements. A maximum error of 3° is seen at $\Delta I_{\text{Bias}_{Q,i}} \leq 20\%$	142
7.24	Two chip layout views showing the details of the metal interconnects which have been edited. A full-chip view showing the locations of the FIB edit marked with ellipses (top) and a zoomed-in view showing the interconnect between the two thin-oxide varactors and the oscillator tank of one of the two identical LO-elements (bottom).	143
7.25	Measured tuning range of the free-running oscillator on the edited chip.	145
7.26	Measured locking range for the ninth subharmonic reference used versus the input power level at 21 GHz.	146
7.27	Locked oscillator spectrum at 21.51 GHz while phase shifts are being captured simultaneously in time domain.	146
7.28	Measured spectra of the two VCOs running simultaneously. One VCO was left free running (left) while the other was injection-locked (right).	147
7.29	An illustration of the four probes while landed on the four sides of the chip.	148
7.30	Measured spectrum leakage between two LO-elements.	148
7.31	Superimposed time-domain waveforms obtained from a number of phase shift measurement steps. Each waveform corresponds to an output of a locked LO-element in response to a separate phase-shifter state as outlined in Section 4.3.1.	150
7.32	Measured phase shifts and associated errors between two oscillator outputs before and after calibration.	151
7.33	Phase steering results for 4-element arrays based on the phase shifts obtained from measurements with and without calibration and how they compare to the ideal case. Phase shift sequences used are (a) $[0^\circ, -22.5^\circ, -45^\circ, \dots]$, (b) $[0^\circ, 45^\circ, 90^\circ, \dots]$, (c) $[0^\circ, -90^\circ, -180^\circ, \dots]$ and (d) $[0^\circ, 90^\circ, 180^\circ, \dots]$	152
7.34	Phase steering results for 8-element arrays based on the phase shifts obtained from measurements with and without calibration and how they compare to the ideal case. Phase shift sequences used are (a) $[0^\circ, -45^\circ, -90^\circ, \dots]$, (b) $[0^\circ, 45^\circ, 90^\circ, \dots]$, (c) $[0^\circ, -135^\circ, -270^\circ, \dots]$ and (d) $[0^\circ, 135^\circ, 270^\circ, \dots]$	153
7.35	(a) Measurement of the phase noise performance for one of the LO-elements while injection locked to subharmonic injection signals at (a) 21.7 GHz/9 and (b) 21.51 GHz/9 from Agilent E8257C and E4432B signal generators, respectively.	154

7.36	Measurement of the effect of phase steering one of the oscillator outputs on its phase noise performance while both oscillators are injection-locked to the 9 th harmonic of the distributed reference.	155
A.1	A compact broadband inductor model.	169
A.2	A low-frequency (below 1 GHz) inductor model for extraction of oxide capacitances and substrate resistances.	170
B.1	A layout view of the two-stage RC-CR polyphase filter.	172
B.2	A layout view of a phase interpolator cell.	173
B.3	A layout view of the high-order synthesis block and the injection transconductor. .	174
B.4	A layout view of the negative-g _m LC-oscillator, the source-follower and FT-doubler buffer stages along with the T-coil and ESD structures.	175

List of Abbreviations and Symbols

ADC	analog to digital converter
ADS	<i>Advanced Design System</i> simulation tool by Agilent Technologies Inc.
CMDLL	Clock multiplier delay-locked loop
CML	Current-mode logic
CMOS	Complementary Metal Oxide Semiconductor
C_{gb}	Gate-to-bulk capacitance of a MOSFET
C_{gd}	Gate-to-drain capacitance of a MOSFET
C_{gs}	Gate-to-source capacitance of a MOSFET
C_{OX}	Oxide capacitance per unit area
C_{db}	Drain-to-bulk capacitance of a MOSFET
C_{sb}	Source-to-bulk capacitance of a MOSFET
C_{SUB}	Capacitance to substrate
C_P	Port-to-port capacitance of an inductor model
T.L.	Transmission-line
dB	Decibels
dBm	$10 \log_{10}(\text{Power in Watts}/1 \text{ mW})$
dBV	$20 \log_{10}(\text{Voltage in } V_p \text{ V})$
dBmV	$20 \log_{10}(\text{Voltage in } V_p \text{ mV})$
DAC	digital to analog converter
DGncap	N+ polysilicon gate over n-well with a thick oxide structure
ϵ_{ox}	dielectric permittivity of SiO ₂
ϵ_s	dielectric permittivity of Si
EIRP	Effective isotropic radiated power
ESD	Electro-static discharge
f_T	Unity current-gain frequency
f_{max}	Maximum frequency of oscillation
$\phi_{ss,i}$	Steady-state output phase of the i^{th} injection locked oscillator
GaAs	Gallium Arsenide
g_m	Transconductance

g_{m,I_i} & g_{m,Q_i}	In-phase and quadrature-phase transconductance weights of phase interpolators in the i^{th} LO-element
I_{Bias,I_i}	The in-phase bias current weight for the i^{th} phase interpolator
I_{Bias,Q_i}	The quadrature-phase bias current weight for the i^{th} phase interpolator
$I_{inj,i}$	AC injected current into the i^{th} oscillator
$I_{osc,i}$	The AC current of the i^{th} oscillator
ILPLL	Injection-locked phase-locked loop
J_{peak,f_T}	Peak- f_T current density
LNA	Low-noise amplifier
LO	Local Oscillator
L_{DC}	Low frequency inductance
MESFET	Metal-semiconductor field-effect transistor
ncap	N+ polysilicon gate over n-well with a thin oxide structure
ω_i & ω_{inj}	Angular frequency of the injected signal into an oscillator
$\Delta\omega_{m,i}$ & ω_L	One-sided injection locking bandwidth of the i^{th} oscillator
PI	Phase interpolator
PLL	Phase-locked loop
PN	Phase noise performance of an oscillator in dBc/Hz
PSS	Periodic steady state simulation engine
Q	Quality factor
SNR	Signal to noise ratio
SNIR	Signal to noise plus interference ratio
SRF	Self-resonance Frequency
VCO	Voltage-controlled oscillator

Chapter 1

Introduction

1.1 Research Motivation and Objectives

The growing demand for more functionality and ease of information access in a mobile form is among the main reasons behind how ubiquitous wireless communication has become. Thanks to the maturity of main stream silicon semiconductor processes, by today's wireless device user standards, embedding more functionality or, *electronics*, in a mobile form is not only subject to cost, battery life and form factor, but also to the reliability of information access in a congested frequency spectrum. This is especially important given the growing markets for high volume RF/millimeter-wave wireless applications demanding high-definition video links (e.g. 802.11ad) and multi-Gb/s data transfer rates among storage devices.

Transmitter beamforming and receiver spatial selectivity schemes have been thus adopted in the form of integrated phased-arrays to alleviate the impact of path-loss, attenuating obstacles and interference. The evolutionary process continued and multiple input multiple output (MIMO) or distinct spatial streaming schemes have been introduced with their accompanying stringent speed, power and silicon real-state demands of the front-end transceiver architectures. With more redundant, or distinct, parallel wireless data streams put to work, new power budgets are there to be dealt with at least as far as the added front-end redundancy in a wireless transceiver. Moreover, these schemes have traditionally been realized in discrete modules using expensive compound semiconductor processes such as GaAs which not only complicates the assembly at the system level, but also increases the overall system cost limiting the scalability of the solution and thus making it difficult to take advantage of the degrees of freedom offered by large-scale arrays [4].

In this specific research context, the focus is on the phase-shifting techniques that are needed for the coherent combining operation in phased-array architectures. Coherent combining in such

architectures may be achieved at the RF, IF or baseband levels. At the IF level, the coherent combining operation is achieved through progressive phase-shifting among the LO signals feeding the RF mixers and thus the "*LO-path phase shifting*" terminology.

One of the main challenges that face integrated LO-path phase shifting based phased-array architectures on silicon is the generation and distribution of multiple phases of RF/millimeter-wave signals to several distant on-chip mixers. These mixers are usually located close to LNAs, integrated antenna elements or feed structures. Integrated RF/millimeter-wave buffers and low-loss matched transmission-line structures are needed for the routing and the distribution of multiple LO phases. This is to combat the loss of, and coupling to the low-resistivity substrate [1,2,5]. The power consumption of power-matched RF/millimeter-wave buffers and the challenges in designing integrated low-loss and area-efficient transmission-lines also at millimeter-wave frequencies on silicon motivated researchers to seek alternative architectures to relax these challenges [2,3,6–8]. The objective of this research was to investigate a new architecture for LO-path phase-shifting which takes advantage of frequency multiplication and injection-locking of LC-Oscillators to alleviate the challenges associated with RF/millimeter-wave integrated phased-array architectures in a standard CMOS technology.

1.2 Thesis Organization

This thesis document is arranged as follows. Chapter 2 reviews the basic principles and the various approaches of coherent combining in electronically steerable phased-array transceiver architectures. It also highlights the progress of LO-based phase-shifting schemes. In Chapter 3, the phenomena of injection locking in LC-Oscillators is briefly reviewed from both a system and a network theory perspective. The possibility of multiple solutions for the transient form of Adler's equation is highlighted and the existence of only one steady solution is emphasized as the basis for the proposed architecture in Chapter 4. The oscillator pulling phenomena is also introduced in terms of the *quasi-lock* and *fast beat* modes. The mathematical background behind the harmonic synthesis technique adopted in this work is also discussed in details. With all the needed background material already presented, Chapter 4 introduces the proposed LO-path phase shifting scheme and its mathematical formulation. The design and implementation details of the individual building blocks constituting the proposed LO-based phase shifting architecture are then provided. Architectural variations on the high-order harmonic synthesis block are introduced and compared highlighting the advantages and disadvantages. The chapter concludes with a discussion on the obtained simulation results and performance. Chapter 5 discusses the isolation techniques

that were adopted at the active and passive device as well as the technology levels to isolate the implemented LO-elements. In Chapter 6, sources of phase shift mismatches among the outputs of the LO-elements are highlighted. Various means for phase offset fine-tuning and calibration have been introduced and mathematically analyzed. The prototype chip details, its test setup, measurement procedures and results are provided in Chapter 7 to validate the main concepts in the proposed architecture. In light of the reported test results, a comparison to similar works from the literature is also provided. Finally, Chapter 8 outlines the contributions of this thesis to the field of RF integrated circuits and proposes a number of future research ideas to be explored further based on the findings of research work reported herein.

Chapter 2

Radio Frequency Integrated Phased-Array Transceivers and Their Architectures: A Review

In wireless communication systems such as point-to-point terrestrial links, satellite communications and air-traffic radars, focused radiation patterns, beam-peak steerability, maximum side-lobe level control and the locations of the nulls are among the key enabling factors that shape the performance of these systems. An antenna array, a spatial arrangement of multiple radiating elements, is an approach through which these key factors can be controlled depending on the relative spatial location of the antenna elements in the array, their relative amplitude and phase excitations [9] [10]. Additionally, most of these key factors can be controlled electronically which eliminates the need for a *mechatronic* orientation overhead.

In the past, antenna-array transceivers have been realized by employing discrete modules (Front-end units, beam-forming networks, baseband and digital control units) using compound semiconductor processes such as gallium arsenide (GaAs) and advanced packaging techniques [11,12]. This led to cost, size and performance related challenges especially at operating frequencies well into the millimeter- and sub-millimeter-wave range [13]. Under the context of integrated phased array solutions, the size, cost and performance are critically inter-related due to the direct proportionality between the number of array elements and the achievable directive resolution. The recent maturity of main stream CMOS IC technology with the noticeable improvement in transistors' f_T and f_{max} [14] [15] enabled the integration of key RF and millimeter-wave circuit blocks along with the digital control circuits on silicon [2]. This not only largely alleviates the packaging overhead among multiple chips, but also allows for considerably cheaper implementations of dense arrays. Moreover, the current push towards millimeter-wave bands (e.g. E-band)

to take advantage of the available bandwidths makes the integration of major parts of these dense array transceivers more feasible from a silicon real-estate point of view [16].

In this chapter, key performance advantages of deploying antenna-array based wireless transceivers are discussed. Examples of recent applications of array transceivers are highlighted. The basic principles of coherent combining in phased array receivers are then reviewed. Phased-array transceiver architectures are categorized and qualitatively compared. Several examples from the literature are then reviewed and discussed.

2.1 Advantages of Phased-Array Transceivers

In an array receiver, the wave-front of a propagating plane-wave signal progressively excites the array elements at different time instants. The array selectively combines these spatial excitations coherently from a selected receive angle enhancing the receiver sensitivity and its ability to reject interferers in a desired direction. In an array transmitter, the information signal is split and delayed to excite the radiating array elements forming a beam-peak in a selected direction and enhancing the effective isotropic radiated power (EIRP*).

Prior to addressing the basic principles of the antenna array transceiver architectures, a quick look at the system-level illustration of a combining architecture in an array receiver in Fig. 2.1 may clarify a few important benefits of these transceivers. In this illustration, only two gain stages are considered before and after the combining operation of an array receiver. The combining is assumed through a passive $n : 1$ combiner. More details on the practical realization and architectural variations are provided later in this chapter.

Assuming no added noise due the passive combiner, the noise figure of the n -element array receiver in Fig. 2.1 can be shown to be expressed as,

$$NF|_{Array} = \frac{n^2 G_1^2 G_2^2 \overline{V_{n,in}^2} + G_1^2 G_2^2 \sum_{i=1}^n \overline{V_{n1,i}^2} / n + G_2^2 \overline{V_{n2}^2}}{n^2 G_1^2 G_2^2 \overline{V_{n,in}^2}} \quad (2.1.1)$$

$$= 1 + \frac{\overline{V_{n1}^2}}{n^2 \overline{V_{n,in}^2}} + \frac{\overline{V_{n2}^2}}{\overline{V_{n,in}^2}} \cdot \frac{1}{n^2 G_1^2}. \quad (2.1.2)$$

Similarly, for a single element receiver (i.e. $n = 1$), the noise figure can be expressed as,

$$NF|_{Single\ element} = 1 + \frac{\overline{V_{n1}^2}}{\overline{V_{n,in}^2}} + \frac{\overline{V_{n2}^2}}{\overline{V_{n,in}^2}} \cdot \frac{1}{G_1^2}. \quad (2.1.3)$$

---

*The ratio of the power radiated by an antenna to that radiated by an isotropic source [9].

Figure 2.1: A system-level illustration of a combining stage in an array receiver.

In (2.1.2) and (2.1.3), $\overline{V_{n,in}^2}$ represents the normalized noise power at the input of each array element and is measured in V^2/Hz . With a fraction of a wavelength separation (i.e. $\lambda/2$ or $\lambda/4$) between the antenna elements, it is assumed that all elements receive the same noise power from a common noise source. As such, these noise powers are assumed equal and fully correlated (i.e. identical) and therefore combine coherently through the passive $n : 1$ power combiner [17]. This implicitly assumes a worst case scenario in combining the noise power*. $G_{1,i}$ and G_2 are the lumped voltage gains of the existing blocks before and after the combining node, respectively. $\overline{V_{n1,i}^2}$ and $\overline{V_{n2}^2}$ are the input-referred normalized noise powers of the array-elements' gain blocks, $G_{1,i}$ and G_2 , respectively. Unlike, $\overline{V_{n,in}^2}$, the noise sources $\overline{V_{n1,i}^2}$ where $i = 1, \dots, n$ are assumed uncorrelated and combine incoherently leading to no noise temperature[†] change at the output of the $n : 1$ combiner [18]. Hence, the attenuation by a factor of n in the summation term in (2.1.1) [17]. Upon comparing (2.1.2) and (2.1.3), it is seen that the noise contribution of the stages before and after the combining node is attenuated by a factor of n^2 relative to that of a single element. This is contrasted to an attenuation factor of n if the noise power received through the antenna elements, $\overline{V_{n,in}^2}$, is assumed uncorrelated with one another.

In integrated array transceivers, if the coherent combining is performed in the current domain

*A more practical, but more involved, assumption is to assume partial correlation among all these noise sources. In this case, portions of the noise power from each noise source add up incoherently [17]. However, preference has been given to the adopted assumption herein due to the unavailability of correlation coefficients data.

[†]maximum available noise power transferred to the load normalized to KB where, K is Boltzmann's constant and B is the bandwidth across which this noise is delivered [18].

without matching (i.e. no matched power combining techniques are assumed [19] [18]), it is instructive to re-derive the expression for the noise figure of the n -element array receiver in Fig. 2.1. In this particular case, the uncorrelated noise power combines with no attenuation and the resulting expression for the noise figure is given by,

$$NF|_{Array} = \frac{nG_1^2 G_2^2 (\overline{nV_{n,in}^2} + \overline{V_{n_1}^2}) + G_2^2 \overline{V_{n_2}^2}}{n^2 G_1^2 G_2^2 \overline{V_{n,in}^2}} \quad (2.1.4)$$

$$= 1 + \frac{\overline{V_{n_1}^2}}{n\overline{V_{n,in}^2}} + \frac{\overline{V_{n_2}^2}}{\overline{V_{n,in}^2}} \cdot \frac{1}{n^2 G_1^2}. \quad (2.1.5)$$

Upon comparing (2.1.2) and (2.1.5), one observes that the noise contribution of the gain stages preceding the combining node is attenuated less by a factor of n relative to the case where a matched power combiner is used.

The gain of an antenna array is closely related to its directivity* and hence it improves with the increasing number of elements [17]. The antenna gain, however, takes into consideration the losses within the antenna and its feed structure. This explains how the antenna array gain eventually saturates as the losses in the passive signal distribution or combining network overshadow the increase in directivity [9]. From an array receiver perspective, where the information signals collected by the array elements are coherently combined in the current or voltage domains, gain improves by $20\log_{10}(n)$ in decibels where n is the number of array elements. From an array transmitter point of view, the EIRP, in Watts, is enhanced by a factor of n^2 in the direction where the beam-peak is steered [16]. For a given path loss, such an enhancement in the radiated power improves the SNR level at the input of the targeted receiver front-end.

The signal-to-noise ratio (SNR) at the output of the combiner in an array receiver can be shown to be expressed as,

$$SNR|_{Array} = \frac{G_1^2 \overline{V_{in}^2}}{G_1^2 \overline{V_{n,in}^2} + G_1^2 \sum_{i=1}^n \overline{V_{n_1,i}^2}/n^2 + G_2^2 \overline{V_{n_2}^2}/n}. \quad (2.1.6)$$

The SNR at the output of the combiner is seen to improve with n in (2.1.6) with an upper bound set by the losses due to the signal distribution and the combining network as previously discussed.

Spatial filtering is the ability to attenuate interfering signals arriving at certain angles other than the desired angle of arrival. Antenna array transceivers are capable of dynamically placing nulls in their radiation patterns by controlling the distribution of the complex weights among the array elements [20]. This has been among the key advantages of using antenna array systems in

---

*The radiation intensity in a given direction relative to that of an isotropic source [9].

military applications. In civilian applications, this advantage is adopted to enhance the dynamic range of transceivers where *in-band* blockers can be *spatially* attenuated. This topic is re-visited in Section 2.3 after the coherent combining principles have been introduced.

Antenna arrays can be realized as one-, two- or three-dimensional arrays. In this treatment, focus is put on one dimensional antenna array receivers to briefly introduce the fundamental concepts.

2.2 Selected Applications of Array Transceivers

Historically, antenna-array transceivers found applications in radar, radio astronomy, communications, direction-finding, seismology and medical diagnosis and treatment systems. Despite the similarity of the core idea in most of these systems, the propagation models of the information signals and the interferers in the associated communication mediums with each application area may greatly influence the design details of the array transceiver [20].

In biomedical engineering, array transceivers are adopted in early-stage breast cancer detection systems [21]. For instance, antenna array beam steering can be employed to compensate for frequency-dependent propagation effects to focus the backscattered energy. Areas of large backscatter energy levels indicate malignant tumors due to their significantly different dielectric properties compared to a normal tissue [21]. Phased-arrays are also used in hyperthermia systems that are used to treat tumors in human limbs [22]. In this application, the beam peak is focused to heat the tumor inside the limb leaving surrounding healthy tissues at relatively lower temperatures.

More recently, the benefits of antenna arrays in extending the communication range and enhancing the signal qualities have been investigated in indoor communication channels. In a recent investigation [23], the resulting delay spread and the k-factor* were compared between two scenarios; directional versus isotropic transmitters and receivers. An improvement of better than 56 % in the delay spread at 10 ns was observed in 90 % of the locations in the directional transmitter and receiver case. The k-factor was estimated at 7 dB in the directional receiver and transmitter case (in 90 % of the locations) versus less than 5 dB in the isotropic case (in 50 % of the locations). In [24], a 4-element 2 GHz phased-array with adaptive beam-forming was tested. Measurement results demonstrated 30 to 50 dB SINR improvements in rural, line-of-sight conditions.

---

*K-factor is defined as ratio between the dominant signal component to the sum of the power in the random multi-path component [23]

Figure 2.2: An n -element linear array receiver with its elements located on the z -axis and spaced apart by a constant distance d . The wave-front of the propagating plane-wave signal progressively excites the array elements at different time instants. A conceptual delay-and-sum RF stage is adopted to combine the received RF signals.

2.3 Coherent Combining Principles in Electronically Steerable Phased-Array Architectures

In the n -element linear array shown in Fig. 2.2, the array elements are located on the z -axis and spaced apart by a constant distance d . The wave-front of a propagating plane-wave signal arrives at an angle θ and progressively excites the array elements at different time instants. The time delay, τ , between these progressive excitation instants is related to the spatial separation distance between the array elements, d , and θ by,

$$\tau = \frac{d \sin \theta}{c}. \quad (2.3.1)$$

In (2.3.1), c is the speed of the wave propagation in the medium. For an n -element array, let the locations of array elements on the z -axis be described by p_{z_k} where, $k = 1, 2, \dots, n$ relative to the first element. The time delay between the excitation instants of the first element and that of the k^{th} element in the array is therefore given by,

$$\tau_k = p_{z_k} \frac{\sin \theta}{c} = d(k-1) \frac{\sin \theta}{c} = \tau(k-1). \quad (2.3.2)$$

It is seen that there is a need for a time delay compensation mechanism such that a coherent summation of the n captured signals is obtained. Fig. 2.2 shows an illustration of a conceptual

delay-and-sum beamformer for n signals that are captured with an accumulative delay of τ_k relative to the first element. This ideal coherent summation can be expressed as,

$$S(t) = \sum_{k=1}^n s \left(t - \tau_k - \frac{d \sin \theta}{c} (n - k) \right). \quad (2.3.3)$$

More details concerning the practical realization of the required time delay compensation can be discussed upon considering a bandpass representation of the received signals expressed by,

$$s(t, p_{z_k}) = \sqrt{2} \Re \{ \tilde{s}(t, p_{z_k}) e^{j\omega_c t} \}, \quad k = 1, \dots, n, \quad (2.3.4)$$

where, ω_c is the angular frequency of the modulated carrier, $\tilde{s}(t, p_{z_k})$ is a complex envelope signal associated with the array elements' locations, p_{z_k} , on the z-axis and $\Re\{\cdot\}$ denotes the real part. In this case, the bandpass system in (2.3.4) becomes,

$$\begin{aligned} s(t, p_{z_k}) &= s(t - \tau_k) \\ &= \sqrt{2} \Re \{ \tilde{s}(t - \tau_k) e^{j\omega_c(t - \tau_k)} \}, \quad k = 1, \dots, n. \end{aligned} \quad (2.3.5)$$

It is seen from (2.3.5) that the ideal time delay compensation expressed in (2.3.3) can be further categorized into two distinct time delays; one is in the complex envelope signal and the other is in the modulated carrier.

An integrated variable time delay element that offers a relatively flat low loss and constant non-zero group delay response at RF/millimeter-wave frequencies with a broadband operation is challenging to realize on silicon. This challenge is exacerbated by the need for a cost effective silicon real-state design. Although this has been an active area of research, alternative approaches have been successfully adopted [1] provided that a few approximations are allowed [20] - as will be discussed shortly. Practically, the complex envelope signal is often limited to be within a certain maximum bandwidth B_s . In a n -element linear array, let's assume that the maximum travel time of a plane wave between the farthest two elements in the array is $\Delta T_{max} = \tau(n - 1)$. If the bandwidth of the complex envelope modulating signal is small enough such that $B_s \cdot \Delta T_{max} \ll 1$, the following approximation can be made about the complex envelope signal [20],

$$\tilde{s}(t - \tau_k) \simeq \tilde{s}(t). \quad (2.3.6)$$

The approximation made in (2.3.6) implicitly states that no time delay compensation is to be provided across the bandwidth of the complex envelope modulating signal, B_s . It follows that (2.3.5) simplifies to,

$$s(t, p_{z_k}) = \sqrt{2} \Re \{ \tilde{s}(t) e^{-j\omega_c \tau_k} e^{j\omega_c t} \}, \quad k = 1, \dots, n. \quad (2.3.7)$$

Figure 2.3: Example of a true time-delay, τ_k , and its equivalent phase shift, ϕ_k , at a carrier frequency, $\omega_c = 2\pi f_c$.

It is seen from (2.3.7) that an approximate coherent combining of the n received signals can be realized if only the time delay in the modulated carrier (i.e. $\tau_k \equiv \tau(k-1)$) is compensated for. In Fig. 2.3, it is shown that a time delay τ_k is equivalent to a phase shift $\phi_k \equiv \omega_c \tau_k = 2\pi(d/\lambda)(k-1)\sin\theta$ where, T is the period of that signal. Only at this frequency, ω_c , that this phase shift, ϕ_k , represents this time delay, τ_k . For a phase shifter to provide the equivalent phase shift, ϕ_k , and compensate for the time delays across a wide bandwidth, the group delay, $\partial\phi/\partial\omega$ should remain a non-zero constant. The fact that an approximate coherent combining can be achieved by employing phase shifters is what gave rise to the familiar “Phased-Array” terminology.

In this case, the coherent summation in (2.3.3) can be re-expressed as,

$$S(t) = \sum_{k=1}^n w_k^* s(t, p_{z_k}) \quad (2.3.8)$$

where $w_k^* \equiv A_k \exp(j\phi_k)$ are complex weights describing the variable magnitude, A_k , and phase shift, ϕ_k , an RF signal experiences through the k^{th} array element. The variable magnitudes are usually realized through variable gain LNA’s while the different phases through a chosen phase-shifting technique implemented in each element.

Several architectural variations exist in the literature among which the main distinction is where the approximate time delay compensation (or, the equivalent phase shift) is realized. A detailed discussion on these variations can be found in Section 2.4. Another important approximation that is often encountered in phased-array architectures is the constant phase shift approximation. In this approximation, the provided phase shift across the bandwidth of the modulated carrier in each channel is constant. In order to quantify the error associated with this

Figure 2.4: Illustration of the required phase shift for a pure time delay versus the constant phase shift approximation across a finite bandwidth.

approximation, consider a time delay $\hat{\tau}_k$ that is to be approximated by a phase shift $\hat{\phi}$ across an absolute channel bandwidth of $\Delta\omega = 2\pi B_s$ around a center frequency ω_0 . As shown in Fig. 2.4, if a constant phase shift, $\phi_0 = \omega_0 \hat{\tau}_k$ is used to approximate the required phase shifts ϕ_1 and ϕ_2 at ω_1 and ω_2 , respectively, the error in either case is given by,

$$\begin{aligned} \text{Phase error}(\%) &= \frac{(\omega_0 \pm \frac{\Delta\omega}{2})\hat{\tau}_k - \omega_0 \hat{\tau}_k}{(\omega_0 \pm \frac{\Delta\omega}{2})\hat{\tau}_k} \\ &\simeq \pm \frac{\Delta\omega}{2\omega_0} \left| \frac{\Delta\omega}{\omega_0} \ll 2 \right|. \end{aligned} \quad (2.3.9)$$

It is seen from (2.3.9) that the phase shift error is directly proportional to the fractional bandwidth across which the constant phase shift approximation is applied. In [1], the error vector magnitude (EVM)* has been used as a measure for constellation spreading due to approximating time delays by constant phase shifts. A 3.1 % fractional bandwidth (i.e. $\Delta\omega/\omega_0 = 750 \text{ MHz}/24 \text{ GHz}$) has been shown to yield EVM less than 2° for an 8-element array receiver at 24 GHz.

2.3.1 Array Factor

The *array factor* of an antenna array represents the output response of the delay-and-sum process and it is a function only of the array geometry and the time-delay compensation (or, the equivalent phase shift) provided assuming isotropic point sources (or, sensors) with no mutual coupling[†].

*root mean squared difference between a perfectly demodulated signal and its distorted version

[†]The total array pattern of the antenna array is the product of two patterns: that of one of the individual elements and that of the array factor [9].

The array factor is often normalized to yield a peak value of unity or 0 dB. Using (2.3.7) and (2.3.8) and assuming identical magnitudes of all complex weights, that is, $A_1 = A_2 = \dots = A_n$, the magnitude of the normalized array factor, AF , can be shown to be expressed as,

$$|AF| = \left| \frac{\sin(N\Psi/2)}{N \sin(\Psi/2)} \right| \quad (2.3.10)$$

where

$$\Psi = 2\pi \frac{d}{\lambda} \sin \theta - \varphi. \quad (2.3.11)$$

In (2.3.11), $\varphi \equiv \Delta\phi = (\phi_{k+1} - \phi_k)$ is the required inter-element progressive phase shift compensation to achieve the coherent combining. The array factor is often evaluated versus the angle of incidence, or the *steering angle*, θ in (2.3.11). An example of three array factor patterns of a uniform linear array with 8 elements and $\lambda/2$ separations between the elements is shown in Figure 2.5. The three illustrated patterns are for progressive phase shifts $\varphi = \Delta\phi$ of $[0^\circ, -90^\circ, -180^\circ, \dots]$, $[0^\circ, 0^\circ, 0^\circ, \dots]$ and $[0^\circ, 90^\circ, 180^\circ, \dots]$. Two parametric plots are also shown in Figures 2.6 and 2.7

Figure 2.5: An illustration of beam steering results for a 8-element uniform linear array and $\lambda/2$ separations between the elements. Three arbitrary beam patterns are shown in response to progressive phase shifts $\varphi = \Delta\phi$ of $[0^\circ, -90^\circ, -180^\circ, \dots]$, $[0^\circ, 0^\circ, 0^\circ, \dots]$ and $[0^\circ, 90^\circ, 180^\circ, \dots]$.

to illustrate the effects of varying the number of and the separation between the array elements on the beam pattern, respectively. Figure 2.6 shows patterns for 4-, 8- and 12-element arrays with a $\lambda/2$ separation. It is seen that increasing the number of elements decreases the main lobe beamwidth thereby improving the directivity* and resolution. The number of pattern nulls

---

*For a broadside array with $d = \lambda/2$, the directivity reduces to $D = n$.

and the sidelobes increases with the associated sidelobe levels decaying faster. The number of elements, however, is usually bounded by the losses of the array feed network of the RF signals which have been shown to overshadow the array gain beyond about 100 elements for a *planar* array* [9]. The inter-element spacing, d , also affects the directional pattern of the array factor

Figure 2.6: Beam patterns for 4-, 8- and 12-element arrays with a $\lambda/2$ separation. It is seen that increasing the number of elements decreases the main lobe beamwidth which increases the directivity. The number of pattern nulls and the sidelobes increases with the associated sidelobe levels decaying faster.

as is shown in Figure 2.7. A larger spacing not only leads to less coupling between the array elements but also facilitates their physical realization and handling. As the inter-element spacing increases, the main lobe beamwidth decreases with an increasing number of sidelobes. When $d = \lambda$, that is, the spacing reaches one full wavelength, the level of the grating lobes at $\theta = \pm 90^\circ$ becomes as high as the main lobe. As d exceeds λ , grating lobes with similar levels to that of the main lobe advance closer towards the main lobe implying some energy received (or, radiated) in an undesired direction reducing the directivity. As such, a trade-off exists between the mutual coupling effects among the antenna elements if $d < \lambda/2$ is used and the obtained levels of grating lobes for $d > \lambda/2$. Therefore, $d = \lambda/2$ is often a good choice for inter-element spacing for linear arrays.

---

*This figure has been calculated based on an estimated loss of $0.15 \text{ dB}/\lambda$ per each signal feed path [9].

Figure 2.7: Beam patterns for 8-element arrays with $\lambda/4$, $\lambda/2$ and λ separations. As the inter-element spacing increases, the main lobe beamwidth decreases with an increasing number of sidelobes. When $d = \lambda$, the level of the grating lobes at $\theta = \pm 90^\circ$ becomes as high as the main lobe.

2.3.2 Spatial Filtering in Phased-Arrays

The advantages of antenna arrays and its ability to perform spatial filtering have been previously highlighted. Spatial filtering can be achieved by controlling the main lobe width, the sidelobe level of the array factor or, by placing nulls (or, minimas) in a given direction to eliminate the effect of the interfering signals. In an n -element array, upon independently varying the complex weights (i.e. gain and phase) among the array elements, $(n - 2)$ nulls can be dynamically placed in specific directions to nullify interferers while simultaneously optimizing for a desired signal reception. The output SINR* can therefore be greatly enhanced by the array [25]. In order to perform this task, several synthesis and optimization algorithms can be adopted to generate the complex weights vector, $\mathbf{w}$, in (2.3.8) for a desired beam pattern. The trade-offs among these algorithms are the main-lobe width and the sidelobe level. The details of these algorithms are discussed in the literature [20] [25, 26] under the context of array processing and are beyond the scope of this work. However, in order to demonstrate the potential of beam pattern shaping using synthesis algorithms and phased arrays, an example of a beam null placement and a sidelobe level control is shown Figure 2.8. In this example, the complex weights vector, $\mathbf{w}$, have been synthesized using a Chebychev distribution along with a *least square error* approach to place two adjacent nulls

---

*Signal to interference-plus-noise ratio (SINR).

over the 27° to 32° sector with an initial -25 dB sidelobe level in the beam pattern of a 8-element array and a $\lambda/2$ separation*. Better than -60 dB of beam peak to null is seen over the chosen null placement sector emphasizing the potential of spatial filtering in mitigating strong in-band interferers.

Figure 2.8: An illustration of the null steering results for a 8-element uniform linear array and $\lambda/2$ separations between the elements. The synthesized complex weights are for an initial -25 dB Chebychev pattern with two adjacent nulls placed over the 27° to 32° sector.

2.3.3 Space Diversity Signal Combining versus Array Processing and Beam-forming

Space diversity techniques are often employed in transceivers to mitigate multipath channel fading issues and improve spectral efficiency [27] [28]. Making several replicas of the information-bearing signal available over independently fading channels increases the likelihood that at least one of the received signals will not have undergone severe fading by the time it reaches the receiving end. To achieve this, multiple transmit and receive antennas are adopted with adequate inter-element spacing to ensure the independence of the possible fading events occurring in the channel. On the receive side, for example, the inter-element spacing should be designed such that the outputs of the multiple receiving antennas are independent from one another. This requirement is usually

---

*The Matlab® code for this example was initially adopted from [20] but has been modified for a 8-element array and the specified null steering sector.

satisfied with spacings on the order of *several* wavelengths, that is, $d/\lambda \gg 1$. Maximal-ratio combining (MRC) is one of several diversity-combining techniques* that can be used to combine the outputs from these statistically independent fading channels. The illustrated delay-and-sum stage in Figure 2.2 would be identical to that needed for an MRC combiner. It is noted however that although the MRC combiner and the RX conceptual beamformer described earlier share the same underlying coherent combining architecture, they bear a number of differences that are important to highlight. First, unlike the independent fading channels assumption with the receive diversity combining, a key assumption with RX beamforming is the minimal to no variations among the levels of the received signals for all antenna elements. Second, while RX beamformers are capable of simultaneous beam and null steering which is instrumental in adaptive co-channel interference mitigation, the required inter-element spacing ($d/\lambda \gg 1$) in the MRC combiner does not allow it due to the elevated gain in the grating lobes as per the discussion pertaining to Figure 2.7. Third, increasing the number of antenna elements in MRC combiners reduces the likelihood of complete signal outage [27] while for RX beamformers it means a finer beamwidth, increased directivity and increased degrees of freedom[†] for beam/null steering, beam peak optimization and interference cancelation [28]. As such, the number of elements in MRC based systems is usually less than that needed for RX beamformers and thus its potential for a fully digital baseband processing (see Figure 2.9(c)) with less power consumption penalties. Examples of commercially developed and tested prototypes include 4-, 8-, 16- and 32-element transceiver arrays [29–31]. Phased-array architecture variations and the associated trade-offs are discussed next.

2.4 Phased-Array Architectures

In a phased-array transceiver, phase shifts can be realized in the RF/millimeter-wave, LO, IF or base-band/digital domains. Architectural naming conventions arose to reflect the corresponding *RF/millimeter-wave signal path*, *LO-path*, *IF*, or *digital* phase-shifting architectures. Fig. 2.9 depicts the four architectures showing the various locations where the delay (or, the equivalent phase shifting) stages can be introduced. From a mathematical view point, all of the architectures shown in Fig. 2.9 should ideally yield equivalent results to the conceptual “delay and sum” coherent combining process that is previously illustrated in Fig. 2.2. The location of where the phase shifts are realized in a transceiver is decided upon based on what benefits the architecture

---

*Other combining techniques are selection combining (SC), equal-gain combining (EGC) and square-law combining [27].

[†]There exists $(n - 1)$ degrees of freedom for a n -element array.

performance matrix the most - for a given application context.

The architecture in Fig. 2.9(a) calls for a variable low-loss phase shifter in the RF/millimeter-wave signal path. Phase shifting and signal combining in the RF/millimeter-wave path allows for the down-conversion stage and the subsequent IF and base-band/digital processing to be realized the same way it is usually done in a single antenna receiver. This is a significant advantage considering the associated area and power savings with this architecture. Moreover, if the spectral content in the RF path is conditioned against strong interferers immediately after the signal combining stage, the dynamic range specifications can be relatively relaxed for the subsequent blocks [1] [32]. It is noted, however, that variable phase shifters that offer low loss at RF/millimeter-wave frequencies with flat gain/loss and linear performance are challenging blocks to design and implement in a main stream CMOS technology and continue to be an active area of research - especially at carrier frequencies in the millimeter-wave range [33–39]. Variable Gain RF/millimeter-wave amplifiers are needed to compensate for the variable phase shifter losses between minimum and maximum phase shifts. If phase shifters involve active means for providing the phase shifts, their non-linearity performance is expected to influence the dynamic range of the transceiver and its robust performance subject to co-existing blockers.

Similarly, phase shifting may be performed in an intermediate IF domain or digitally in the base-band domain as is shown in Fig. 2.9(b) and 2.9(c), respectively. In the IF domain, phase shifters are implemented at relatively lower frequencies allowing less signal attenuation than that associated with their RF/millimeter-wave counterparts. IF domain designs also allow more tolerance for a phase shifter attenuation after possible IF gain stages. However, the sensitivity of the delay compensation and the power combining operation to RF, LO, and IF path mismatches complicates the implementation considerably.

Implementing the conceptual “delay and sum” processor in the digital base-band domain promises a more flexible and versatile solution [40–42]. It has the potential for a reconfigurable architecture that supports both MIMO and signal combining architectures. It must be noted, however, that the n parallel signal paths must extend from RF to base-band. This dictates challenging linearity and dynamic range requirements from the IF stage(s) and ADC blocks in each parallel path to allow robust co-existence with non-nullified interferers. Additionally, for an n -element array, the number of parallel IF stages and ADC blocks is also multiplied by n which translates to area and power consumption penalties linearly growing with n . In this case, two options are available for the digital processing of $n \times M$ -bit ADC outputs. One option is to employ an on-chip DSP core for which silicon area and power consumption concerns add to the already

Figure 2.9: Architectural variations in phased-array receivers where the required phase shifting for coherent combining can be realized in (a) the RF/millimeter-wave signal domain, (b) the IF domain, (c) the base-band or digital domain or (d) the LO domain.

Figure 2.10: A continuous LO-based phase shifting scheme in integrated phased-array architectures.

established baseband challenges. The other option is to use an existing processor on a backplane for which the data transfer to and from this backplane becomes increasingly challenging as the data rates and the number of array elements increase.

Phase shifting can alternatively be employed in the LO path for the combining to occur in the IF domain as is shown in Fig. 2.9(d). In a lower-side LO injection architecture (i.e. $f_{RF} > f_{LO}$), this allows the phase shifting to be performed at lower frequencies compared to the RF path phase shifting approach. Given the large LO amplitude levels required to switch RF mixers, possible attenuation due to phase shifting in the LO path is offset by the amplification prior to driving those mixers. This makes the sensitivity to non-flat gain/loss phase shifting techniques less pronounced compared to the RF signal path phase shifting architecture in Fig. 2.9(a) [1]. It is noted, however, that the number of RF mixers in this case is equal to the number of parallel RF paths or array elements.

2.5 Local Oscillator Based Phase Shifting Schemes for Coherent Combining in Phased-Array Architectures

Several architectural variations exist in the literature for which LO-based phase shifting is the central theme. These variations can be differentiated in the techniques they use for the generation, distribution or control of multiple LO phases.

A continuous Local Oscillator (LO) based phase shifting scheme is conceptually illustrated in Fig. 2.10 for an n -element array [43]. In this scheme, an auxiliary control frequency, ω_c , is employed to contribute an additive variable phase shift to a single phase LO tone, ω_0 . The control frequency, ω_c , is initially mixed with the LO tone by a single sideband (SSB) mixer to produce a lower sideband at $\omega_0 - \omega_c$. Multiple copies of this resulting sideband are then re-mixed

with multiple time-delayed versions of the original ω_c to obtain LO tones at $\omega_0 t + (\omega_c \pm \Delta\omega_c)\tau_i$ where $i = 1, 2, \dots, n$ at the output of the second set of the upper-sideband mixers and τ_i is the accumulated time delay up to the i^{th} tap output. In case of ideal SSB mixers and for a delay-line tap spacing s , the relative phase at the output of each mixer at ω_0 for the n^{th} element compared to the first element can be expressed as,

$$\begin{aligned}\Delta\phi &= \angle\phi_n - \angle\phi_1 \\ &= (n-1)s \left(\frac{\omega_{c0}}{v_c} \right) \pm (n-1)s \left(\frac{\Delta\omega_c}{v_c} \right)\end{aligned}\tag{2.5.1}$$

$$= (n-1)s \left(\frac{2\pi}{\lambda} \right) \pm (n-1)s \left(\frac{2\pi}{\lambda} \right) \left(\frac{\Delta f_c}{f_{c0}} \right)\tag{2.5.2}$$

where,

$$v_c = \frac{s}{\tau} = \frac{c}{\sqrt{\epsilon_r}}.\tag{2.5.3}$$

In (2.5.1) - (2.5.3), ϵ_r , v_c and λ are the relative permittivity, the velocity of propagation and the wavelength in the delay line, respectively. Equal phases are obtained at $\Delta\omega_c = 0$, when the first term in (2.5.1) is an integer multiple of 2π . One way to achieve this is by designing the delay-line tap spacing such that $s = \lambda = \lambda_0/\sqrt{\epsilon_r}$. In this case, it follows from (2.5.1) that,

$$\Delta\phi = 2\pi(n-1) \left(1 \pm \frac{\Delta f_c}{f_{c0}} \right).\tag{2.5.4}$$

This style of LO-based phase shifting has the advantage of providing continuous phase shifting through possible fine steps of $\pm\Delta\omega_c$. It seen however that several practical challenges may be encountered in the realization of this architecture. First, is the need for $(n+1)$ RF/millimeter-wave SSB mixer blocks with adequate carrier and sideband suppression [44]. This is necessary so that neither the control frequency, ω_c , nor the intermodulation tones (other than $\omega_o - \omega_c$) has significant side-band magnitude levels in the output spectrum. Second, the requirement that $s = \lambda$ suggests that the nominal control frequency, ω_{c0} , should be chosen to allow an area efficient implementation. Depending on the number of array elements, the accumulation of the losses in the delay-line sections may result in substantially different amplitude levels presented at the input of the second set of SSB mixers. Unless the gradually attenuated amplitude levels are compensated for, the progressive element-to-element phase shifts produced may suffer from significant mismatches. Third, the delay-line elements should maintain a non-zero group delay across the desired $\Delta\omega_c$ bandwidth through which a continuous phase shifting is to be synthesized. It is also noted that, despite the advantage of distributing the low control frequency ω_c , the

Figure 2.11: The LO-based phase shifting scheme adopted in [1] for an integrated phased-array architectures. A centralized multi-phase millimeter-wave PLLs is employed for the generation of 16 phases of a 19.2 GHz LO. In this architecture, the 16 (or, 8 differential) LO phases are distributed to each of n 16 : 1 phase selectors in a symmetric binary tree structure, where n is the number of array elements.

Figure 2.12: A refinement to the LO-based phase shifting scheme in [1] (Fig. 2.12) where millimeter-wave phase rotators are employed at each front-end location to generate the desired LO phase shift locally avoiding the need to distribute multiple LO phases to n array elements [2].

distribution of the carrier frequency ω_0 to all of the front-end locations on the chip entails power-matched buffers and low-loss transmission-line structures at RF/millimeter-wave frequencies.

In [1,5] and [45], integrated 24 GHz receivers and transmitters phased-array architectures with LO-based phase shifting were reported on silicon where centralized multi-phase millimeter-wave PLL's were employed for the generation of 16 phases of a 19.2 GHz LO. In this architecture (Fig.2.11), the 16 (or, 8 differential) LO phases are distributed to n phase selectors in a symmetric binary tree structure, where n is the number of array elements. The challenges in coherently distributing these multiple phases to each phase selector at each of the n front-end locations were thoroughly analyzed and emphasized. In an LO distribution bus of 16 metal lines, EM crosstalk between these lines and the possibility of multi-mode excitation led to potential phase and magnitude errors [1]. Although this has been a remarkable milestone towards integrated phased arrays on silicon, re-thinking the architecture in regards to the generation and distribution of multiple LO-phases was necessary due to i) the power consumption of the $n \times (16 : 1)$ RF/millimeter-wave phase selectors and the differential power-matched buffers per each array-element front-end, ii) the silicon area associated with the parallel distribution tree structures at 19.2 GHz [2].

In [2], the distribution of multiple millimeter-wave LO phases has been replaced by distributing a single-phase of a 52 GHz LO signal after employing millimeter-wave phase rotators at each array

Figure 2.13: A unilateral injection locking based LO-path phase shifting architecture. A low phase-noise RF signal is optically distributed to injection-lock a cascade of two millimeter-wave oscillators in each array element. The phase shifting is obtained by controlling the center frequency of the resonator in each $f_0/2$ oscillator through DC biasing (V_{tune}).

element prior to the mixing stage in each front-end as shown in Fig. 2.12. Employing millimeter-wave phase rotators at each front-end location allowed to generate the desired LO phase shift locally avoiding the need to distribute multiple LO phases to n array elements. This lead to significant power and silicon area savings compared to the architecture in [1]. It is noted, however, that the challenges associated with designing millimeter-wave phase rotators and distributing multiple copies of a millimeter-wave LO signal to multiple distant front-ends on silicon remained as potential bottlenecks. This is due the power consumption and the silicon area associated with intermediate power-matched buffering and transmission line structures, respectively, as required in millimeter-wave distribution networks.

Other techniques for beam steering or power combining have been realized employing the non-linear oscillator injection locking phenomena discussed in Chapter 3. Both unilateral and bilateral schemes have been demonstrated in [6, 8, 46–49]. Eliminating the need for a phase-shifting stage at each array element is among the key advantages of adopting these schemes.

In situ, unilateral injection locking of RF/millimeter-wave oscillators has been proposed in [6] for large aperture optically controlled phased arrays. The injection signal has been optically distributed to each array element and then converted back to an RF signal with the aid of photo-detectors. The RF signal is then used to injection-lock the first of two cascaded millimeter-wave oscillators at each element as shown in Fig. 2.13. Each two cascaded oscillators were built with GaAs MESFET devices to oscillate at $f_0/2$ and f_0 , respectively. In this architecture, the phase shifting approach is solely dependent on controlling the center frequency of the resonator of the first oscillator in each cascaded pair. By controlling the varactor diode in the resonator, the center frequency of the $f_0/2$ oscillator can be tuned to achieve $\pm 90^\circ$ phase shift as discussed in Chapter 3. Upon injecting the output of the $f_0/2$ oscillator into the f_0 oscillator, a $\pm 90^\circ$ phase

Figure 2.14: An unconventional injection-locked PLL (ILPLL) built around a MESFET push-pull self-oscillating mixer. The high conversion gain of the mixing operation enabled the architecture to exclude frequency multipliers or dividers prior to the PLL phase comparison stage.

variation of former results in a $\pm 180^\circ$ in the latter and thus a 360° phase shift is obtained. Since each oscillator needs to operate near the edge of its locking range to provide a relative $\pm 90^\circ$ phase shift, this approach leads to undesired coarse phase shifts and phase noise performance degradation when the maximum phase shift is desired.

More recently, successful integrated architectures employing unilateral harmonic and super-harmonic injection locking of LC-oscillators have been reported to overcome a similar challenge in microprocessors' clock distribution and de-skewing [7]. Fig.2.13 still captures the main idea with the optical transmission media being replaced by on-chip transmission-line (T.L.) structures. Distributing multiple copies of a fundamental LO frequency, or a higher multiple of it, to multiple distant front-ends on silicon involves more design and implementation challenges - especially at operating frequencies approaching the millimeter-wave range.

In [8], a $0^\circ - 180^\circ$ (or, $\pm \pi/2$) LO phase shifting technique has been demonstrated through an unconventional injection-locked PLL (ILPLL) built around a MESFET push-pull self-oscillating mixer. The high conversion gain of the mixing operation enabled the architecture to exclude frequency multipliers or dividers prior to the PLL phase comparison stage as shown in Fig. 2.14. Employing a combination of injection locking and PLL techniques allowed for phase tracking across a larger sub-harmonic IL frequency range. Compared to a pure IL case, an improvement in the phase noise (PN) level was reported up to a de-tuning phase of 70° . In this architecture, however, since the phase shifting was realized by adjusting the dc bias (V_{tune}) of a varactor diode

Figure 2.15: Bilateral injection-locking of oscillators and its application to LO-path phase shifting in phased-array architecture. Oscillators are bilaterally coupled to their nearest neighbours forming a “coupled-oscillator array” where a uniform division of the pre-determined phase shift, $(N + 1)\Delta\phi$, along the array is possible and hence the potential for beam steering applications.

in the oscillator feedback network through an active loop filter, the relative dependence of the phase noise performance on the amount of phase de-tuning could still be observed.

Bilateral injection-locking in coupled-oscillator arrays and its application to coherent power combining in phased-arrays was first proposed in [46] as an alternative approach to unilateral coupling. In this architecture, instead of relying on individual injection locking reference signals being routed to oscillators in each array element’s front-end, oscillators have been bilaterally coupled to their nearest neighbours forming a “coupled-oscillator array”. As illustrated in Fig.2.15, upon injecting two versions of a locking signal with a pre-determined phase shift $\omega_{inj}\tau$ between them onto the array end elements, the dynamics of the this system have been shown to be captured by a modified version of Adler’s equation for mutually coupled-oscillator array [49],

$$\frac{d\phi_i}{dt} = (\omega_{0,i} - \omega_i) - \frac{\epsilon_i \omega_i}{2Q} [\sin(\phi_i - \phi_{i-1}) + \sin(\phi_i - \phi_{i+1})] + \frac{\omega_i \rho_i}{2Q} \sin(\psi_i - \phi_i). \quad (2.5.5)$$

In (2.5.5), $\omega_{0,i}$ and ϕ_i are the free-running frequency and phase of the i^{th} oscillator where $i = 1, \dots, n$. ψ_i and ρ_i are the injection signal phase and strength into the i^{th} oscillator. ϵ_i is the coupling strength relative to the i^{th} oscillator amplitude. It has been shown that a constant progressive phase shift given by $\varphi = \phi_i - \phi_{i-1}$ can be a solution to (2.5.5) provided that; i) $\omega_i = \omega_{inj} = \omega_0$ and ii) $\phi_1 - \psi_1 = -(\phi_n - \psi_n) = \varphi$ [49]. If the phase of the first injection signal is taken as a reference (i.e. $\psi_1 = 0$), it follows that $\phi_i = i\varphi$ and hence $\psi_n = (n+1)\varphi$. This implicitly means that a pre-determined phase shift of $\omega_0\tau = (n+1)\varphi$ between the injection signals of the two end elements yields a uniform division of this phase shift along the oscillator array and thus the potential for beam steering and power combining applications.

Figure 2.16: A scalable phased-array transmitter architecture based on integrated coupled-oscillator arrays [3]. The top level architecture is shown in (a). The in- and quadrature-phases of the third sub-harmonic - relative to the carrier - are used as the bilateral inter-injection locking signals among the coupled array cells. The details of each array cell is shown in (b) where the inter-injection locking signals are re-synthesized at each array LO-element.

Later, the scheme proposed in [46] has been investigated further in [47, 48, 50]. More specifically, an investigation of the tuning conditions of each element in the bilaterally coupled-oscillator array resulted in a simplification of the architecture proposed in [46]. It has been demonstrated in [50] that a steady-state progressive phase shift in the range of $-47^\circ \leq \varphi \leq +90^\circ$ can be synthesized by detuning only the end elements of the coupled-oscillator array in opposite directions. This resulted in -15° to $+30^\circ$ beam-scanning off broadside. Common to the two main approaches in [46–48, 50], however, is; i) the sensitivity of the synthesized progressive phase shift to oscillator amplitude non-uniformities, ii) the frequency response of the coupling networks, iii) non-nearest neighbour interactions and iv) the non-uniform tuning profiles of the VCO's subject to PVT variations [49]. The susceptibility to phase noise degradation and loss of lock if the array oscillators are detuned near the edge of their locking ranges [51] limited the achievable phase shifts to $\pm\pi/2$. Additionally, mode stability analysis in coupled-oscillator arrays highlighted the possibility of undesired mode-jumps [52] [53] in denser arrays. These factors have limited the practicality of these schemes and their successful deployment in beam steering applications.

A scalable phased-array transmitter architecture based on integrated coupled-oscillator arrays was reported in [3] (Fig. 2.16). The adopted carrier frequency synthesis scheme allowed the choice

of the third sub-harmonic (i.e. 20 GHz) - relative to the carrier (60 GHz) - as the inter-injection locking signal frequency among the coupled oscillators. This choice aimed at minimizing the attenuation of the inter-injection signals among the coupled-oscillator array elements and hence the improvement in the locking range. In this scheme, however, the inter-injection locking signals were inherently re-generated at each array LO-element and routed to the next in a bi-lateral arrangement. As a result, overcoming the potential rapid degradation in the PN performance with the increasing array size [51] remains a challenge especially if the oscillator array elements undergo frequency de-tuning due to PVT variations. In addition, the realization of phase-shifting at millimeter-wave frequencies and the distribution of a low carrier-to-injection-frequency-ratio ($N = 3$) has led to a challenging power budget of 375 mW per element.

2.6 Summary

In this chapter, the reasons behind the recent interest in a main stream CMOS integrated phased-array transceivers and their advantages have been discussed. An investigation of a simplified system-level model of a linear antenna-array receiver front-end architecture demonstrated a possibility for noise figure and SNR improvement when compared to a single antenna element architecture. Some of the potential applications of phase arrays were briefly highlighted. The coherent combining principles in a linear array receiver were reviewed in details while paying attention to approximations that are often encountered in practical “delay and sum” signal combining schemes. Using the array factor, the effects of the number of elements and the inter-element spacing on the beam pattern were explored parametrically. The ability of antenna arrays to perform beam steering and null placement was then discussed as a potential means for spatial filtering. Spatial diversity combining was also contrasted to beamforming highlighting the main differences between the two approaches. A number of array transceiver architecture variations were explored and qualitatively compared. Finally, various examples of the LO-path based phase shifting architecture were selected from the literature and reviewed in details. The advantages and disadvantages of these architectures are summarized in Tables 2.1 and 2.2.

Table 2.1: A qualitative comparison summarizing the advantages and disadvantages of LO-path based phase shifting techniques in phased-array architectures

Architecture Type	Advantages	Disadvantages
Continuous frequency-controlled phase shifting	• Availability of continuous high resolution phase-shift • Potential for distributing a low frequency control signal	• Need for $(n + 1)$ RF/millimeter-wave SSB mixers with adequate sideband suppression • Delay-line losses lead to amplitude and phase mismatches • RF/millimeter-wave LO distribution to n front ends
Centralized RF/Millimeter-wave synthesizer with multi-phase fundamental LO distribution	• A single RF/Millimeter-wave oscillator is needed	• Coherent distribution of 2^M different RF/millimeter-wave phases to each array element • The need for $n \times (2^M - 1)$ RF/millimeter-wave MUXs for phase selection in a n-element array
Centralized RF/Millimeter-wave synthesizer with a single-phase fundamental LO distribution	• A single RF/Millimeter-wave oscillator is needed • Distribution of a single RF/Millimeter-wave LO phase to all array elements	• The need for a low-loss RF/Millimeter-wave phase shifter for each array element at the fundamental LO frequency • RF/Millimeter-wave distribution buffers and area-efficient low-loss T.L. structures are still needed

Table 2.2: A qualitative comparison summarizing the advantages and disadvantages of LO-path based phase shifting techniques in phased-array architectures (Continued)

Architecture Type	Advantages	Disadvantages
Optical and RF/Millimeter-wave signal distribution of super-harmonic or fundamental LO synchronizing signals	• Low loss distribution of synchronizing signals to each array element (if optically distributed) • No need for phase shifters	• The unavailability of optical distribution in a main stream technology to-date. • Operation near ± 90 degrees degrades the phase noise performance considerably • RF/Millimeter-wave distribution buffers and T.L. structures are still needed for harmonic or super-harmonic synchronizing signals • The need for $2 \times n$ oscillators to achieve 360° phase shifting in a n-element array
Subharmonic Injection-locked PLL (ILPLL)	• Improved phase noise performance stability up to a de-tuning phase of 70° • More robust tracking than direct sub-harmonic injection-locking schemes	• The need for oscillator de-tuning and hence the associated phase-noise degradation • The achieved phase shift was limited to $[0^\circ 180^\circ]$
Bilateral injection locking of coupled-array oscillators	• RF/Millimeter-wave synchronizing signals may only be distributed to the two end elements of the array	• Sensitivity of progressive phase-shift to oscillators amplitudes and tuning profile mismatches • Susceptibility to loss of lock, mode jumps and degradation of phase noise near the edge of the lock range in dense arrays • The achieved phase shift was limited to $[-47^\circ 90^\circ]$

Chapter 3

Injection Locking of LC-Oscillators and Higher Harmonic Synthesis

Among the various LO-path phase shifting schemes considered thus far for phased-array architectures, injection locking of RF/millimeter-wave oscillators has been a recurring principle. In this chapter, the phenomena of frequency and phase locking in LC-Oscillators by injection is reviewed from both a system and a network theory perspective. The possibility of multiple solutions for the transient form of Adler's equation is highlighted and the existence of only one stable solution is emphasized as the basis for the proposed architecture in Chapter 4. The mathematical background behind the harmonic synthesis technique adopted in this work is also discussed.

3.1 Frequency and Phase Locking in LC-Oscillators by Injection

Since the observation made by Huygens about the mutual mechanical synchronization between pendulums [54], the phenomenon of frequency “entrainment” in an autonomous system while being acted upon by an external force has been studied in great details by mathematicians and scientists [55–58]. A general form of a differential equation that describes an oscillatory system acted upon by a periodic force is given by [57],

$$\frac{d^2v}{d\tau^2} + \omega_0^2 v = \mu f(\omega\tau, v, \frac{dv}{d\tau}). \quad (3.1.1)$$

In (3.1.1), ω_0 is the natural frequency of the system, μ is a parameter that describes the magnitude of the non-linearity of the system and $f(\omega\tau, v, dv/d\tau)$ is a periodic function with a period of $2\pi/\omega$. An example of an oscillatory system of the self-excited type ($\mu > 0$) under the influence of a periodic signal is that described by Van der Pol's equation with a forcing term,

$$\frac{d^2v}{d\tau^2} - \mu(1 - v^2)\frac{dv}{d\tau} + \omega_0^2 v = B \cos \omega\tau \quad (3.1.2)$$

where, B is the amplitude of the acting periodic signal. A synchronization range for an oscillator is commonly described by a frequency range within which the oscillator can be fully synchronized to the acting signal. This range is a function of the oscillator circuit parameters as well as the relative power or amplitude of the synchronization signal. If the frequency of the synchronization signal, $\omega/2\pi$, and its amplitude, B , place it inside the oscillator synchronization range, the oscillator is said to be “entrained” by, synchronized or *locked* to the synchronizing signal. In this case, the oscillation frequency and phase become *locked* to that of the synchronization signal. Outside of this synchronization range, one of two scenarios may occur. Either beat oscillation frequencies appear or, an entrainment of the natural frequency of the system to a multiple (i.e. synchronization to a sub-harmonic) or a sub-multiple (i.e. synchronization to a super-harmonic) of the driving frequency takes place [58] [57]. The synchronization range for the latter scenario is a function of the system non-linearity and the ratio of the natural frequency of the system to the driving frequency. In this case, an approximate solution is given by [58],

$$v(\tau) \approx \begin{cases} b_1 \sin \omega\tau + b_2 \cos \omega\tau & \text{for harmonic synchronization,} \\ \frac{B}{1-\omega^2} \cos \omega\tau + b_1 \sin(\frac{p}{q})\omega\tau + b_2 \cos(\frac{p}{q})\omega\tau & \text{for sub- or super-harmonic synchronization,} \end{cases} \quad (3.1.3)$$

where,

$$\left(\frac{p}{q}\right) = 2, 3, \dots \quad \text{for sub-harmonic synchronization,} \quad (3.1.4)$$

$$\left(\frac{p}{q}\right) = \frac{1}{2}, \frac{1}{3}, \dots \quad \text{for super-harmonic synchronization.} \quad (3.1.5)$$

In (3.1.3), for sub- or super-harmonic synchronization, the first term shows that the solution contains an attenuated component of the acting periodic signal frequency while the rest of the solution shows that the resulting oscillation frequency is in the neighborhood of the the natural frequency of the system at $(p/q)\omega$.

Kurokawa investigated the frequency and phase locking phenomena of microwave oscillators through injection from a microwave network theory perspective relying on frequency-domain impedance quantities [59] [60]. Fig. 3.1 shows a model for an oscillator circuit under current injection. This model is adopted from [61] and is employed herein to briefly review the dynamics of oscillator locking by injection. The oscillator circuit is modeled by a core oscillator admittance, $Y_{osc}(\omega)$, that is loaded by an external admittance, $Y_L(\omega)$. $Y_{osc}(\omega)$ includes a non-linear, frequency independent, active element $G_d(V)$ which is needed to provide energy restoration for the parallel LC resonator circuit the loading of which is lumped into $Y_L(\omega)$. The total admittance is given

Figure 3.1: A model for an LC oscillator under current injection. The nonlinearity in the active device is captured through its voltage dependant conductance, $G_d(V)$. The oscillator loading is in the purely real admittance, Y_L . The reactive loading of the oscillator is assumed to be lumped into the oscillator LC tank.

by,

$$Y_t(\omega, V) = Y_{osc}(\omega, V) + Y_L(\omega). \quad (3.1.6)$$

The output voltage is expressed as,

$$v(t) = A(t)e^{j[\omega_0 t + \phi(t)]} \quad (3.1.7)$$

$$= \tilde{v}(t)e^{j\omega_0 t}. \quad (3.1.8)$$

In (3.1.7), A and ϕ describe the dynamic phase and amplitude of the output voltage. $\tilde{v}(t) = A(t)e^{j\phi(t)}$. The relationship between the injection current and the output voltage is obtained by applying KCL to the circuit in Fig. 3.1 as,

$$I_{inj}(\omega) = Y_t(\omega, V)V(\omega). \quad (3.1.9)$$

Assuming $\omega^2 - \omega_0^2 \simeq 2\omega(\omega - \omega_0)$ near resonance, $Y_t(\omega, |V|)$ can be approximated as,

$$Y_t(\omega, A) \simeq G_d(A) + G_L + 2jC(\omega - \omega_0). \quad (3.1.10)$$

In (3.1.10), $\omega_0 = 1/\sqrt{LC}$ and it is assumed that Y_L is purely real and that any appreciable reactive components are lumped into the resonator. It is also noted that the voltage dependance of the active device conductance, G_d , and that of the total admittance is now expressed in the complex envelope amplitude $A(t)$. Using Kurokawa's substitution* everywhere in the admittance transfer function, $Y_t(\omega, |A|)$, adopting a slowly varying envelope approximation (i.e. $d\phi/dt \ll \omega_0$,

---

*i.e. replacing ω by $\omega_0 + d\phi/dt - j(1/A)(dA/dt)$ [59]

$(1/A)(dA/dt) \ll \omega_0$) in expanding $Y_t(\omega, |A|)$ around ω_0 [59], and performing an inverse Fourier transform, (3.1.9) can be shown [61] to yield,

$$I_{inj}(t) = v(t) \left[Y_t(\omega_0, A) + \frac{dY_t(\omega_0, A)}{d\omega} \left(\frac{d\phi}{dt} - j \frac{1}{A} \frac{dA}{dt} \right) \right]. \quad (3.1.11)$$

Two coupled differential equations can be obtained by separating the real and imaginary parts in (3.1.11) such that

$$\frac{dA}{dt} = A \Re\{F(A, \phi)\} \quad (3.1.12)$$

$$\frac{d\phi}{dt} = \Im\{F(A, \phi)\} \quad (3.1.13)$$

where,

$$F(A, \phi) = \frac{I_{inj}/v(t) - Y_t(\omega_0, A)}{dY_t(\omega_0, A)/d(j\omega)}.$$

The obtained equations in (3.1.12) and (3.1.13) describe the instantaneous phase and amplitude dynamics under injection. Assuming weak injection, the differential equation describing the instantaneous phase dynamics ($d\phi/dt$) - also known as Adler's equation - can be decoupled from that describing the amplitude dynamics (dA/dt) and expressed in its transient form as,

$$\frac{d\phi(t)}{dt} = -(\omega_{inj} - \omega_0) - \Delta\omega_m \sin[\phi(t) - \psi] \quad (3.1.14)$$

where,

$$\Delta\omega_m|_{|I_{inj}| \ll |I_{osc}|} = \frac{\omega_0}{2Q} \frac{|I_{inj}|}{|I_{osc}|}. \quad (3.1.15)$$

In (3.1.14) and (3.1.15), ω_0 and ω are the frequencies of the free running oscillator and the injected signal, respectively. $\phi(t)$ is the instantaneous output phase of the oscillator while ψ is its injected phase. $I_{inj} \equiv |I_{inj}| \exp[j(\omega_{inj}t + \psi)]$ and $I_{osc} \equiv |I_{osc}| \exp[j(\omega_0t + \phi(t))]$ are the injected and the oscillator currents, respectively. $\Delta\omega_m$ is the one-side locking range of the oscillator. The external quality factor $Q \equiv \omega_0 C / G_L$ [62]. If the combination of the frequency and power characteristics of the injected signal places it within the locking range of the oscillator, a steady state frequency and phase lock is reached after a transient phase acquisition process [54] [63] the dynamics of which are captured by (3.1.14). In the steady state, the output phase of the oscillator, ϕ_{ss} , will be locked to its injected signal phase, ψ , with a phase offset, θ . Under low injection levels, this steady-state phase offset, θ , is given by [64],

$$\theta_{ss}|_{|I_{inj}| \ll |I_{osc}|} = \phi_{ss} - \psi \approx \sin^{-1} \left(\frac{\omega_0 - \omega_{inj}}{\Delta\omega_m} \right). \quad (3.1.16)$$

Figure 3.2: Phase transient acquisition process

3.2 Phase-lock Stability and Beat Oscillation Modes

In order to highlight some important aspects of the dynamics of the phase acquisition process in (3.1.14), the instantaneous output phase of an oscillator under injection, $\dot{\phi} = d\phi(t)/dt$, is normalized to the one-side locking range, $\Delta\omega_m$, and is plotted against $\phi(t)$ in Fig. 3.2. In this figure, there exists two nodes in each cycle, depicted as black and white circles, where the normalized instantaneous change of the oscillator output phase is zero (i.e. a steady state case) [54] [65]. Upon applying perturbation on both nodes, only one in each cycle retains its phase (i.e. remains stable) while the other node loses its apparent zero instantaneous change towards the other stable node. For example, if ϕ_{ss} is perturbed slightly to the right of a "black" node, the sign of $\dot{\phi}$ is negative leading to $\phi(t)$ decreasing back to the same node, ϕ_{ss} . A slight perturbation to the left at the same node (by slightly decreasing ϕ_{ss}) would still force $\phi(t)$ to increase towards the same node due to the positive sign of $\dot{\phi}$ in this case, hence the stability of this "black" node. Performing the same exercise on the "white" node shows its instability. The direction of the arrows in Fig. 3.2 shows the trajectories of $\phi(t)$ upon perturbation at each node. While [54] reached this conclusion when applying injection locking concepts to oscillating lasers, both [65] and [66] arrived at similar conclusions upon undertaking perturbation analysis for first order loop PLLs. Therefore, based on this analysis, LO-based phase steering can be theoretically achieved by oscillator phase lock through injection. This conclusion will be exploited further in the proposed architecture in chapter 4.

Figure 3.3: Tangential (left) and absolute (right) phase variations of an LC-oscillator output under injection in the quasi-lock and fast beat modes as expressed by (3.2.1).

Two beat oscillation modes have been considered: *quasi-lock* and *fast beat* [64] [67,68]. One of the two modes occur when the frequency and amplitude of the injected signal place it outside the oscillator locking range while the injection and oscillation frequencies are not integer multiple or sub-multiple of each other. Performing a separation of variables on (3.1.14) assuming a zero reference phase (i.e. $\psi = 0$), it can be shown [64] that

$$\tan\left(\frac{\phi(t)}{2}\right) = \frac{\Delta\omega_m}{\omega_0 - \omega_{inj}} + \frac{\omega_b}{\omega_0 - \omega_{inj}} \tan\left(\frac{\omega_b t}{2}\right) \quad (3.2.1)$$

where

$$\omega_b = \sqrt{(\omega_0 - \omega_{inj})^2 - \Delta\omega_m^2}. \quad (3.2.2)$$

In the quasi-lock mode, the injection signal frequency is just above or below the locking range, e.g., $\omega_{inj} < \omega_0 - \Delta\omega_m$ provided that $|\omega_{inj} - \omega_0|/\Delta\omega_m \approx 1$. Under this condition, the first term on the right-hand side of (3.2.1) is dominant (≈ 1) for ω_b is relatively small and so $\tan \omega_b t/2$ is less than one reaching a large magnitude only for a very short duration every $2\pi/\omega_b$ [64]. Fig. 3.3 shows a qualitative plot of the cycle-to-cycle behaviour of $\tan(\phi(t)/2)$ and that of the derived $\phi(t)$. It is seen that $\phi(t)$ is pinned near $\pi/2$ for most of the $2\pi/\omega_b$ period with a rapid 2π change near the edges. As such, the oscillator stays locked to the injection signal for most of the period and thus the dominant component of its spectrum at ω_{inj} as shown in Fig. 3.4. The spectrum also exhibits sidebands spacing of ω_b due to the periodic variation of $\phi(t)$ at the same rate.

The fast beat mode occurs for ω_{inj} which is farther away from the edge of the locking range leading to an increased beat frequency and larger ω_b separation between the spectrum sidebands. Given the shorter time the oscillator spends being locked at ω_{inj} , the dominant frequency component is no longer at ω_{inj} but at $\omega_{inj} + \omega_b$ instead, which is the closest beat frequency that lies

Figure 3.4: Output spectra of an LC-oscillator under injection in the quasi-lock mode with higher- (left) and lower-side (right) injection cases depicted.

Figure 3.5: Output spectra of an LC-oscillator under injection in the fast beat mode with higher- (left) and lower-side (right) injection cases depicted.

near the edge of the locking range in this case as shown in Fig. 3.5 [64].

3.3 Frequency Multiplication Techniques

Frequency multiplication is a technique to realize low phase noise LO signals in the RF/millimeter-wave range from good quality low-frequency sources. Successful multiplier architectures [69–76] showed how this technique may relax the challenges associated with designing conventional PLL building blocks for RF/millimeter-wave oscillators. Lies at the core of common frequency multipliers, a higher frequency synthesis technique. The main idea behind most of these synthesis techniques fall under one of the following three approaches. The first approach employs an intrinsic non-linear transfer function that is associated with an active device under certain biasing conditions to generate harmonics from a low-frequency signal. The output is then filtered to suppress the undesired harmonics. Controlling the conduction angle of field-effect transistors

(FETs) or exploiting the non-linear capacitance in varactor and step-recovery diodes are among the common techniques for the generation of harmonics. In this approach, the power in the desired harmonic is dependent on the non-linear transfer function offered by the active device or its biasing arrangement. Successful implementations found in the literature focused on large-signal levels (e.g. > 0 dBm [69–71, 77]) to drive the active device non-linearity and obtain sufficient power in the carrier. For the purpose of generating high-order harmonics, the lossy nature of diode multipliers and their scarce availability in a main stream digital process limited their use to applications that are more suited for compound semiconductor processes. FET based multipliers on the other hand, although more efficient, are limited to quadruplers. This is due to the maximum gate-to-drain junction voltage a FET can tolerate which puts a lower limit on the achievable conduction angles [78].

The second approach employs a non-linear transfer function to mix two good-quality low-frequency reference signals (e.g. ω_1 and ω_2 where, ω_2 may be derived from ω_1) and condition the mixed output, either through single side-band mixing or filtering, such that a higher frequency tone is obtained [3] [72]. The use of multiple mixing stages (possibly single side-band), doublers and dividers (if ω_2 is derived from ω_1) may lead to challenging power requirements, specially at frequencies well into the RF/millimeter-wave range. The third approach, employs a low frequency reference signal to sub-harmonically injection lock a free-running oscillator at the desired frequency. This approach depends on the inherent non-linear transfer function in the oscillator core [76] or the injection circuitry [79] [80] to generate the desired harmonic and lock the oscillator. Owing to the “weak” synchronizing harmonic and hence the limited lock range, fine pre-tuning of the oscillator free-running center frequency is crucial for the successful deployment of this architecture [76].

3.4 High-order Harmonic Synthesis for Injection Locking and Frequency Multiplication

In this work, an approach that combines high-order harmonic synthesis and injection locking of oscillators is adopted as part of the proposed architecture in chapter 4. In this approach, upon synthesizing harmonics from a N^{th} sub-harmonic frequency reference, the desired harmonic is enhanced and employed to injection-lock a free running LC-oscillator at the desired frequency [81]. Unlike the first approach that was mentioned earlier, the power in the carrier in this case is that of the locked oscillator and therefore, to a first order, is independent of the magnitude of the synthesized harmonic. Moreover, unlike the third approach, this injection-locking based frequency

Figure 3.6: An illustration of a square-wave signal synthesis through a progressive accumulation of the constituting harmonics in its Fourier series representation. The incremental addition of the harmonics with the correct amplitude and phase spectra results in an enhancement of the rise and fall times and in amplitude saturation.

multiplication architecture has the advantage of an improved locking range due to the enhanced magnitude of the synchronizing harmonic. These advantages encouraged further investigations of this frequency multiplication approach and its adoption as the core of the proposed architecture in chapter 4. The details of injection locking of oscillators have been reviewed in Section 3.1. What remains is a detailed investigation of a high-order harmonic synthesis technique which can be employed to realize the synchronizing harmonic for injection locking. The remaining part of this chapter reviews the mathematical background behind the harmonic synthesis technique adopted in this work.

3.4.1 Harmonic Synthesis by resembling a Square-wave

An ideal square wave signal such as that shown in Fig. 3.6 is represented by its trigonometric Fourier series components given by,

$$x(t) = \frac{1}{2} + \frac{2}{\pi} \left(\cos t - \frac{1}{3} \cos 3t + \frac{1}{5} \cos 5t - \frac{1}{7} \cos 7t + \dots \right). \quad (3.4.1)$$

The results of the incremental addition of this series components are also plotted in Fig. 3.6. It is observed that the incremental addition of odd harmonics with the correct amplitude and phase spectra results in an enhancement of the rise and fall times. It is also seen that this

Figure 3.7: A trapezoidal wave resembling a square wave with non-zero rise- and fall-time.

results in a slowly varying amplitude levels or, amplitude saturation. This directly suggests that high-order harmonics can be synthesized by saturating the amplitude of a sinusoidal signal to a square-wave like signal while enhancing the rise and fall times. This harmonic synthesis technique is proposed for implementation at the circuit level in chapter 4.

3.4.2 Time-delays of a Square-wave and Phase Angles of its Harmonics

When an arbitrary time delay, t_0 , is introduced into the general form of (3.4.1), it follows that,

$$\begin{aligned} x(t - t_0) &= \alpha_0 + \sum_{\nu=1}^{\infty} \alpha_{\nu} \cos \nu \omega_0 (t - t_0) \\ &= \alpha_0 + \sum_{\nu=1}^{\infty} \alpha_{\nu} \cos [\nu \omega_0 t - \nu \omega_0 t_0]. \end{aligned} \quad (3.4.2)$$

In (3.4.2), ω_0 is the angular frequency of $x(t)$ and ν denotes the constituting harmonic number in a trigonometric Fourier series representation of $x(t)$. It is seen from the RHS of (3.4.2) that delaying $x(t)$ by t_0 results in an equivalent linearly incrementing phase-lag of $\nu \omega_0 t_0$ in each constituting harmonic [82]. Similarly, introducing an equivalent phase shift ψ at the fundamental frequency of the periodic $x(t)$ yields an equivalent phase shift of $\nu \psi$ radians in the corresponding ν^{th} harmonic.

3.4.3 Rise- and Fall-time of a Non-ideal Square-wave and its Harmonic Content

In order to capture the impact of the rise- and fall-time on the magnitude of the constituting harmonics of a non-ideal square wave with finite rise and fall times, a trapezoidal wave such as that shown in Fig. 3.7 is to be analyzed further. Relying on a modified procedure for evaluating

Fourier series coefficients, as outlined in [82], a general expression for the series coefficients has been re-derived for this trapezoidal wave using its second derivative. The general expression is given by,

$$\alpha_\nu = \begin{cases} \frac{1}{j\pi\nu} \left[\frac{\sin \nu\omega_0\delta}{\nu\omega_0\delta} \right] & \text{if } 0 < \delta \leq \tau/4, \\ \frac{1}{j\pi\nu} & \text{if } \delta = 0. \end{cases} \quad (3.4.3)$$

In (3.4.3), 2δ denotes the equal 0-100% rise- and fall-time, ω_0 is the radian frequency of the waveform, τ is its period and ν is the constituting odd harmonic number. The magnitudes of the coefficients, as obtained from (3.4.3), have been normalized to their corresponding maximum values (i.e. $2\delta = 0$ and $|\alpha_\nu| = 1/\pi\nu$) and then plotted for several rise/fall times for each harmonic. Fig. 3.8 shows the normalized attenuation of these magnitudes of the Fourier coefficients as a function of the normalized rise- and fall-time. The normalization of the rise- and fall-time has been calculated relative to the period of the fundamental, τ . Upon inspecting Fig. 3.8, it is seen that the higher the constituting harmonic number, the faster the degradation in its magnitude as the rise/fall time increases. For instance, the magnitude of the coefficient for the ninth harmonic component is seen to be attenuated by about 20 dB for a rise/fall time of 8% relative to period of the fundamental. It is also seen that for each harmonic number, there exists a first null in the magnitude of its corresponding coefficient at a specific rise/fall time. Once the location of the null is crossed, it can be observed that the magnitude of the coefficient re-rises up to another maxima at a larger rise/fall time. Taking the magnitude of the eleventh harmonic coefficient as an example, a normalized rise/fall time of 10% may lead to the same coefficient magnitude as that obtained at a normalized rise/fall time of 6%. This re-rising of the magnitudes of the coefficients is explained as follows. As the rise/fall time of a trapezoidal signal increases, the harmonic components that existed for a shorter rise/fall time version of the same trapezoidal signal re-appear with the same magnitudes and a notable 180° phase shift. This interesting property can be exploited in applications where i) the respective coefficient magnitudes can still be useful and ii) the notable 180° phase shift is of no concern under that application context.

3.4.4 Duty-cycle and the Relative Magnitudes of the Harmonics

It is also instructive to compare the effect of the duty-cycle on the harmonic content of a periodically repeated ideal rectangular pulse such as that shown in Fig. 3.9. This rectangular pulse is equivalent to an ideal square wave with an arbitrary duty-cycle, ε/τ . The general expression for

Figure 3.8: The normalized attenuation of the magnitudes of odd harmonics contained in the trapezoidal signal in Fig. 3.7 as a function of its normalized rise- and fall-time. The normalization of the rise- and fall-time is calculated relative to the period of the fundamental, τ .

Figure 3.9: A periodically repeated ideal rectangular pulse with a δ pulse width.

the Fourier coefficients is given by [82],

$$\alpha_\nu = \frac{\varepsilon E}{\tau} \left[\frac{\sin \nu \omega_0 \varepsilon / 2}{\nu \omega_0 \varepsilon / 2} \right]. \quad (3.4.4)$$

In (3.4.4), ε represents the width of the ideal rectangular pulse and E is its amplitude. Substituting $\omega_0 = 2\pi/\tau$ yields,

$$\alpha_\nu = \frac{\varepsilon E}{\tau} \left[\frac{\sin \pi \nu (\varepsilon / \tau)}{\pi \nu (\varepsilon / \tau)} \right]. \quad (3.4.5)$$

If the duty cycle is 50 % relative to the period of the fundamental (i.e. $\varepsilon = 0.5 \tau$), the resulting Fourier coefficients are,

$$\alpha_\nu|_{\varepsilon=0.5\tau} = \begin{cases} 0 & \text{if } \nu \text{ is even,} \\ \mp \frac{E}{\nu\pi} & \text{if } \nu = \pm 3, \pm 7, \pm 11 \dots, \\ \pm \frac{E}{\nu\pi} & \text{if } \nu = \pm 1, \pm 5, \pm 9 \dots \end{cases} \quad (3.4.6)$$

This is contrasted to the case where the rectangular pulse-width is compressed such that it is 50 % of the period of the desired harmonic, ν_d , that is, $\varepsilon = 0.5 \tau / \nu_d$. In this case, the resulting coefficients are given by,

$$\alpha_\nu|_{\varepsilon=0.5\tau/\nu_d} = \frac{E}{2\nu_d} \left[\frac{\sin(\frac{\pi}{2} \frac{\nu}{\nu_d})}{\frac{\pi}{2} \frac{\nu}{\nu_d}} \right]. \quad (3.4.7)$$

Upon substituting $\nu = \nu_d$ in (3.4.7), one obtains the coefficients as $\alpha_{\nu_d}|_{\varepsilon=0.5\tau/\nu_d} = E/\pi\nu_d$ for all possible values of ν_d . Upon comparing this result to that of (3.4.6), it is seen that aside from a notable 180° phase shift between the $(2k+1)^{th}$ harmonics (depending on whether k is an even or an odd integer), the magnitudes of the odd harmonics are identical in the two cases; the 50 % duty cycle case and the compressed pulse case (i.e. $\varepsilon = 0.5 \tau / \nu_d$). The result of this substitution, however, does not convey much information about the magnitude of the fundamental in this case* (i.e. $\varepsilon = 0.5 \tau / \nu_d$) as compared to the case where $\varepsilon = 0.5 \tau$. For this reason, more general forms of (3.4.6) and (3.4.7) are obtained by substituting $\varepsilon = \beta\tau$ and $\varepsilon = \beta\tau/\nu_d$ in (3.4.5), respectively, where, $0 < \beta < 1$. These substitutions yield,

$$\alpha_\nu|_{\varepsilon=\beta\tau} = \beta E \left[\frac{\sin(\pi\nu\beta)}{\pi\nu\beta} \right] \quad (3.4.8)$$

and

$$\alpha_\nu|_{\varepsilon=\beta\tau/\nu_d} = \frac{\beta E}{\nu_d} \left[\frac{\sin(\pi\nu\beta/\nu_d)}{\pi\nu\beta/\nu_d} \right] \quad (3.4.9)$$

---

*This is due to the fact that substituting $\nu_d = \nu$ in (3.4.7) eliminates the harmonic number from the expression and thus only yields information about the magnitude of that harmonic number substituted for outside the brackets.

Figure 3.10: A comparison between the relative magnitudes of Fourier coefficients for the fundamental and the ninth harmonic components of an ideal rectangular pulse with $0 < \beta < 1$. The pulse-width compression case (i.e. $\varepsilon = \beta\tau/\nu_d$) may, at its best, yield identical odd harmonic magnitudes to that in the $\varepsilon = \beta\tau$ case. The magnitude of the fundamental can be reduced by about 82% at $\beta = 0.5$ without affecting that of the targeted harmonic if the duty cycle of the rectangular pulse is chosen such that $\varepsilon = \beta\tau/\nu_d$.

, respectively. The resulting magnitudes of the fundamental and the ninth harmonic coefficients, as obtained from (3.4.8) and (3.4.9), are compared in Fig. 3.10 where, $E=1$. It is observed that the duty-cycle compression (i.e. $\varepsilon=\beta\tau/\nu_d$) may, at its best, yield identical odd harmonic magnitudes to that in the $\varepsilon = \beta\tau$ case. More notably, however, is the possible 82% reduction in the magnitude of the fundamental in the former case at $\beta = 0.5$ without affecting the magnitude of the desired harmonic. From an application perspective, if a periodic square wave or a rectangular pulse is synthesized to be used in high-order harmonic synthesis, duty-cycle compression relative to the period of the targeted harmonic is only desired as a step towards suppressing the fundamental. This, however, does not enhance the magnitude of the desired harmonic component. It is also noted that compression allows for non-zero even harmonics - in case they are desired.

3.5 Summary

In this chapter, the phenomena of injection locking in LC-Oscillators has been briefly reviewed. It was illustrated that only one solution is stable among the two solutions that exist for the transient form of Adler's equation. This stable solution can be exploited as the basis for phase locking through injection as is discussed in Chapter 4.

Several techniques for frequency multiplication were discussed. Emphasis has been put on injection locking of oscillators using harmonics of a low-frequency source. A technique for generating high-order harmonics by synthesizing a square-wave like signal has been discussed. The harmonic content of a trapezoidal wave, as an example of a non-ideal square wave, has been analyzed in details. The impact of the rise- and fall-time of a trapezoidal wave on the magnitudes of the coefficients of its Fourier series representation has been discussed. It has also been shown how may be achieved through compression. The effect of the duty cycle of an ideal rectangular pulse on the magnitudes of its harmonic components relative to one another has also been highlighted and explored in details. A significant reduction of the magnitude of the fundamental relative to that of the desired harmonic has been demonstrated mathematically through duty cycle compression.

Chapter 4

Proposed LO-Path Phase-Shifting Architecture

4.1 Proposed Architecture

In this work, an injection locking scheme is proposed for integrated LO-path phase shifting based phased-array architectures. The architecture takes advantage of the frequency multiplication through the generation of high-order harmonics in high-speed limiting amplifiers and latches to synthesize multiple phases of ninth-harmonic tones. These multiple phases are synthesized at the destination and in close proximity to RF/millimeter-wave injection-locked oscillators. This enables the architecture to relax the challenges associated with i) multi-phase signal generation and distribution, ii) designing phase shifters and conventional PLL building blocks at fundamental RF/millimeter-wave frequencies. Synthesizing a high-order harmonic prior to injection such that the injected tone is a fundamental to the oscillator admits a higher injection strength than that of a sub-harmonic injection and thus a wider locking bandwidth. The architecture also allows for a digital phase calibration means which is necessary to overcome inevitable phase mismatches in integrated phased-arrays.

The proposed LO phase shifting scheme is shown as part of the high-level receiver architecture in Fig. 4.1 targeting the industrial, scientific and medical (ISM) radio band at 24 GHz. Antenna-array elements receive multiple phases of the incoming modulated carrier which are then fed into variable gain LNAs setting the NF and gain of the front-end. In a dual-IF heterodyne receiver, the conditioned 24 GHz signal phases are down-converted to the first IF by phase-shifted 18 GHz LO signals through RF mixers. The phase-shifted LO signals are generated by injection-locked 18 GHz LC-VCOs. The down-converted RF signals are coherently combined at the first IF stage at 6 GHz.

Figure 4.1: Proposed Architecture.

4.2 Details of the LO-Path Phase Shifting Operation

The phase shifting of the LO signals is achieved as described below. A central low-frequency PLL synthesizes a single differential 2 GHz reference signal (i.e. the ninth subharmonic of 18 GHz). In an n -element phased-array, this subharmonic reference signal is distributed to n distant LC-oscillators where the RF/millimeter-wave front-ends are located. At each of these locations, the 2 GHz reference signal is fed to a phase-shifter to obtain the desired relative phase shift. Each phase shifter consists of a quadrature differential synthesis block, and a two-stage cartesian phase interpolator. The phase interpolators are digitally controlled via 4-bit current steering DACs. High-speed limiting stages and a latch are adopted at each location to synthesize higher harmonics from the phase shifted 2 GHz reference signal as per the analysis presented in Section 3.4. A Q-enhanced tuned amplifier is optionally* employed at each location to boost the ninth-harmonic tone while attenuating the undesired harmonics. Enhancing the harmonic corresponding to the fundamental frequency of the injection-locked oscillator allows for a wide locking range as discussed in Section 3.4. The ninth-harmonic phase shifted signals are used to injection lock their respective LC-VCOs locally. Based on the analysis presented in Section 3.1, phase steering of the individual oscillators' outputs, relative to one another, can be achieved by oscillator phase lock through injection. If the frequency and power of each injected signal is within the locking range of its respective oscillator, a steady state frequency and phase lock is reached after a transient phase acquisition process [54] [63] the dynamics of which are captured by,

$$\frac{d\phi_i(t)}{dt} = -(\omega_{0,i} - \omega_i) - \Delta\omega_{m,i} \sin(\phi_i(t) - \psi_i). \quad (4.2.1)$$

where,

$$\Delta\omega_{m,i}|_{|I_{inj,i}| \ll |I_{osc,i}|} = \frac{\omega_{0,i}}{2Q_i} \frac{|I_{inj,i}|}{|I_{osc,i}|}. \quad (4.2.2)$$

In (4.2.1) and (4.2.2), $\omega_{0,i}$ and ω_i are the frequencies of the free running i^{th} oscillator and its locally injected signal, respectively. $\phi_i(t)$ is the instantaneous output phase of the i^{th} oscillator while ψ_i is its injected phase. $|I_{inj,i}|$ and $|I_{osc,i}|$ are the magnitudes of the injected and the oscillator currents, respectively. $\Delta\omega_{m,i}$ is the one-side locking range of the i^{th} oscillator. In the steady state, the average output phase of the i^{th} oscillator, $\phi_{ss,i}$, will be locked to its locally injected 18 GHz signal phase, ψ_i , with a phase offset, θ_i . Under low injection levels, this steady-state average phase offset (due to the periodic phase perturbation), θ_i , is given by [64],

$$\theta_i|_{|I_{inj,i}| \ll |I_{osc,i}|} = \phi_{ss,i} - \psi_i \approx \sin^{-1} \left(\frac{\omega_{0,i} - \omega_i}{\Delta\omega_{m,i}} \right). \quad (4.2.3)$$

---

*Possible architectural variations will be discussed in details in Section 4.3.2.

Figure 4.2: Fundamental phase locking.

Figure 4.3: Sub-harmonic phase locking.

In the n -element LO-based phase shifting array, shown in Fig. 4.3, to obtain a successive phase shift, φ , between the outputs of the n oscillators, the phase shifters are adjusted through their DAC's to phase shift the received reference signals to a phase sequence of $\psi_i/N, \psi_{i+1}/N, \dots, \psi_n/N$ such that $(\psi_i/N - \psi_{i+1}/N) = (\psi_{i+1}/N - \psi_{i+2}/N) = \dots = \varphi/N$, where $N = 9$ in this case. Upon synthesizing the ninth harmonic locally, the injection signals at the output of the tuned amplifiers following the comparators will have a phase sequence of $(\psi_i + \epsilon_i), (\psi_{i+1} + \epsilon_{i+1}), \dots, (\psi_n + \epsilon_n)$ at 18 GHz where, ϵ_i is a systematic phase shift introduced by the i^{th} synthesis stage. The phase multiplication by the harmonic number, N , is discussed in Section 3.4.2. Phase mismatches caused by routing the subharmonic reference signals to distant front-end locations may all be lumped into the ϵ_i error stated earlier instead of adding it to $\Omega_{0,i}$. It is assumed that mismatches between these systematic phase shifts can be calibrated out, as will be discussed in Chapter 6. Therefore, the successive phase shifts between the outputs of the n injection locked oscillators

can now be expressed with the aid of (4.2.3) as,

$$\begin{pmatrix} \phi_i - \phi_{i+1} \\ \phi_{i+1} - \phi_{i+2} \\ \vdots \\ \phi_{n-1} - \phi_n \end{pmatrix} = \begin{pmatrix} (\psi_i - \psi_{i+1}) + (\theta_i - \theta_{i+1}) \\ (\psi_{i+1} - \psi_{i+2}) + (\theta_{i+1} - \theta_{i+2}) \\ \vdots \\ (\psi_{n-1} - \psi_n) + (\theta_{n-1} - \theta_n) \end{pmatrix}$$

It is seen from (4.2.3) that for the case of matched oscillators and equal injection strength, $\theta_i = \theta_{i+1} = \dots = \theta_n$. Therefore, a progressive phase shift, φ , can be obtained between the outputs of the n oscillators, that is $(\phi_i - \phi_{i+1}) = \dots = (\phi_{n-1} - \phi_n) = \varphi$.

In contrast to the proposed phase-shifting architecture, distributing much lower frequency references on the order of 10 to 100 MHz and realizing local PLLs or clock multiplier DLLs (CMDLL) at each front-end with localized phase shifting capability bears a few trade-offs that are worth noting. First, the higher the implicit frequency up-multiplication operation performed by a local PLL or a CMDLL, the higher the required resolution of the phase shifting operation if it is to be performed at the reference frequency. For a N th sub-harmonic reference signal, the minimum phase step required from an M -bit phase shifter at the N th sub-harmonic is $2\pi/(N \cdot 2^M)$. For example, a 4-bit phase shifter operating on a $f_{ref} = 100$ MHz while targeting $f_0 = 18$ GHz needs a minimum phase step of 0.0022° without incorporating phase shifter errors or non-idealities. A phase shifter with such a resolution is impractical to design and calibrate over PVT variations.

Alternatively, if the phase shifting operation is to be performed on the carrier frequency at the output of the oscillator, millimeter-wave, highly linear phase shifters and buffers would be required given the desired large LO swing needed for the RF mixers. Phase shifter non-linearity can result in zero-crossing distortions of the phase shifted LO signal since the generated harmonics will not experience the inherent high-Q filtering of the oscillator [83]. Second, the realization of millimeter-wave PLLs or CMDLL building blocks at each *LO-element** entails further power consumption and area trade-offs [1] [2] as is discussed in Section 4.3.

The implementation details of all the circuit blocks in the proposed phase-shifting scheme are covered next. in Section 4.3.

4.3 Architecture Building Blocks

In this section, the analysis, design and implementation of each building block constituting the proposed architecture are treated in details. Possible architectural variations are explored when

---

*The term "*LO-element*" shall designate the phase shifters, harmonic synthesis blocks and the oscillator associated with each front-end in the phased-array architecture considered in this document.

Figure 4.4: One phase interpolator basic cell architecture.

feasible and trade-offs are discussed. Simulation results are provided at both the circuit and architectural levels. Comparison to similar works from literature is also provided to highlight the potential power savings that can be achieved by employing the proposed phase-shifting architecture.

4.3.1 Quadrature phase synthesis and Cartesian Phase Shifters

The proposed architecture calls for a high resolution phase shifter that can provide angles between 0 and $(2\pi/N)$ degrees with a minimum phase step of $(2\pi/(N \cdot 2^M))$ for the N^{th} subharmonic and a M -bit phase shifter. A 4-bit phase shifter operating on a ninth subharmonic reference makes $N = 9$ and $M = 4$. This results in a minimum phase step of 2.5° and a total required phase shift of 40° . In order to realize such a high resolution phase shifter, a two-stage cartesian phase interpolator architecture is employed for each LO-element [81, 84].

A cartesian phase shifter, in its most basic form, consists of a quadrature phase generation stage followed by a phase interpolation (PI) stage [39] as shown in Fig. 4.4. By controlling the g_{mI_i} and g_{mQ_i} through bias currents, the originally applied differential signal (i.e. v_+ and v_-) undergoes phase shifting through interpolation. The quadrature phase generator stage is needed to provide the in-phase and quadrature phase signal components for the phase interpolation operation. The differential quadrature phase generator in this implementation is realized by a two-stage RC-CR polyphase filter as shown in Fig. 4.5. The two successive RC-CR stages have been adopted to ensure robustness against potential phase and amplitude mismatches as a result of process variations. Staggered tuning between $f_1 = 1.77$ GHz and $f_2 = 2.22$ GHz of

Figure 4.5: A schematic showing the two successive RC-CR polyphase filter stages.

the two RC-CR stages has been used to ensure a sub 1 dB amplitude error across $\pm 20\%$ of this bandwidth [85, 86]. The resistor values R_1 and R_2 are related to the capacitor values C_1 and C_2 in the first and second filter stages, respectively, such that,

$$R_{1,2} = \frac{1}{2\pi f_{1,2} C_{1,2}}. \quad (4.3.1)$$

For a $C_1 = C_2 = 0.2$ pF, $R_1 \approx 450 \Omega$ and $R_2 \approx 358 \Omega$. For testing purposes, the input impedance of the filter is matched to 100Ω differential through a 150Ω resistor connected between the two differential inputs. Figures 4.6 and 4.7 show the worst-case phase shift variations and differential amplitude mismatches among the outputs of the two-stage polyphase filter as obtained in Monte Carlo simulations across temperature ($-40^\circ - +65^\circ$) and process variations with ten iterations.

In this proposed architecture, the quadrature phase synthesis stage (i.e. RC-CR filter in this case) is followed by a two-stage PI for which the high-level architecture is shown in Fig. 4.8. The first phase interpolation stage employs two identical cartesian PI stages in parallel. Together, the two parallel stages can selectively provide a suitable phase interpolation region for the second PI stage. Each interpolation region lies between two adjacent phase angles, $\Omega_{i,1}$ and $\Omega_{i,2}$ which are set by the first stage PI.

For a matched in-phase and quadrature phase amplitudes input from the RC-CR filter, a

Figure 4.6: Worst-case phase shift variations among the outputs of the two-stage RC-CR polyphase filter with temperature and process variations.

Figure 4.7: Worst-case amplitude mismatch percentage error between the in-phase and the quadrature phase outputs of the two-stage RC-CR polyphase filter with temperature and process variations.

Figure 4.8: A two-stage cartesian phase interpolator architecture to accompany the i^{th} LO-element.

cartesian interpolation operation is illustrated graphically in Fig. 4.9(a) for which the resulting current-domain interpolation can be expressed as,

$$i_{total}\angle\Omega_{i1,2} = v_{I,Q}\sqrt{g_{m,I_{i1,2}}^2 + g_{m,Q_{i1,2}}^2}\angle\tan^{-1}\left(\frac{g_{m,Q_{i1,2}}}{g_{m,I_{i1,2}}}\right). \quad (4.3.2)$$

Schematics of unit cells in the first and second PI stages are shown in Fig. 4.10(a) and Fig. 4.10(b), respectively [87]. Keeping bias current densities below $0.15\text{mA}/\mu\text{m}$ allows for a safe square-law assumption [88] for the interpolation devices ($M_{I,1-4}$, $M_{Q,1-4}$). Assuming a square-law operation region where $g_m \propto \sqrt{I_{Bias}}$, the g_m weights in the first stages are set externally such that

$$\Omega_{i1,2} = \tan^{-1}\left(\frac{g_{m,Q_{i1,2}}}{g_{m,I_{i1,2}}}\right) = \tan^{-1}\left(\sqrt{\frac{I_{Bias,Q_{i1,2}}}{I_{Bias,I_{i1,2}}}}\right). \quad (4.3.3)$$

In (4.3.3) and (4.3.2), $g_{m,I_{i,j}}$, $g_{m,Q_{i,j}}$, $I_{Bias,I_{i,j}}$ and $I_{Bias,Q_{i,j}}$ are the transconductances and bias currents for the in-phase and the quadrature phase branches in the first stages of the i^{th} phase phase shifter, respectively. In order to improve the accuracy of the current copying between the biasing branches and interpolator devices, wide swing current mirrors were used for biasing the in-phase and quadrature-phase branches in the first stage. This significantly improved the accuracy of the obtained $g_{m,I}$ and $g_{m,Q}$ weights.

Figure 4.9: An illustration of the vectorial current summation in the first (a) and second stage (b) phase interpolators (PI). In (b), The two summed components are those resulting from the first PI stages with angles $\Omega_{i,1}$ and $\Omega_{i,2}$.

Figure 4.10: Schematics of the cartesian phase interpolation cells in the first (a) and the second (b) stages of the phase interpolator. The topology of the current-steering DAC in the second interpolation stage is also shown in (b).

Table 4.1: Interpolation regions for the second stage PI

Interpolation Region	$\Omega_{i,1} - \Omega_{i,2}$
Region 1	$(-\pi/8) - (\pi/8)$
Region 2	$0 - (\pi/4)$
Region 3	$(\pi/8) - (3\pi/8)$

Figure 4.11: Illustration of the three interpolation regions to keep the bias currents ratios and the corresponding g_m weights within the most linear range of the second stage enabling the architecture to avoid the non-linearities that would otherwise occur at the boundaries where bias current weights differ by large amounts.

The second interpolation stage (Fig. 4.10(b)) operates in one of three regions to generate the desired ψ_i/N angle. The three interpolation regions are shown in Table 4.1.

Since the two angles defining the edges of the three interpolation regions are no longer in a quadrature relationship (see Table 4.1), the interpolation operation can no longer be described by (4.3.2) and (4.3.3). Instead, a graphical representation of this non quadrature interpolation operation is illustrated in Fig. 4.9(b). Straight forward analysis yields the following expression for a desired phase shift of ψ_i/N at the output of the second stage PI:

$$\angle\left(\frac{\psi_i}{N}\right) = \tan^{-1} \left[\frac{(\sqrt{2I_{Bias_1}/I_{Bias_2}} + 1) \tan \Omega_{i,1} + 1}{(\sqrt{2I_{Bias_1}/I_{Bias_2}} + 1) - \tan \Omega_{i,1}} \right]. \quad (4.3.4)$$

In (4.3.4), $\Omega_{i,1}$ is the angle defining the lower edge of the selected interpolation region. I_{Bias_1} and I_{Bias_2} are the required current-domain weights to yield the desired output phase shift angle at ψ_i/N where N is subharmonic number. It is noted that the expression in (4.3.4) is only valid when the components being interpolated are at $\Omega_{i,1}$ and $\Omega_{i,1} + \pi/4$ as is seen in Table 4.1. Otherwise, a more general expression should be used and it is given by,

$$\angle\left(\frac{\psi_i}{N}\right) = \tan^{-1} \left[\frac{\sqrt{I_{Bias_1}/I_{Bias_2}} \sin \Omega_{i,1} + \sin \Omega_{i,2}}{\sqrt{I_{Bias_1}/I_{Bias_2}} \cos \Omega_{i,1} + \cos \Omega_{i,2}} \right]. \quad (4.3.5)$$

A current steering DAC with 9 cells [87] has been adopted to set the appropriate g_m weights by setting the corresponding I_{Bias_1} and I_{Bias_2} for the second interpolation stage. The schematic of the second interpolation stage along with the current-steering DAC cells are shown in Fig. 4.10(b). For a constant current budget, $I_{total} = I_{Bias_1} + I_{Bias_2}$, and a desired output phase ψ_i/N , (4.3.4) is used to solve for the required current weights I_{Bias_1} and I_{Bias_2} and the resulting expressions have been obtained as,

$$I_{Bias_1} = \frac{I_{total}[1 - \sin(2\Psi_{i,1})]}{2 - \cos(2\Psi_{i,1}) - \sin(2\Psi_{i,1})} \quad (4.3.6)$$

and

$$I_{Bias_2} = \frac{2I_{total} \sin(\Psi_{i,1})^2}{2 - \cos(2\Psi_{i,1}) - \sin(2\Psi_{i,1})}, \quad (4.3.7)$$

where,

$$\Psi_{i,1} = \psi_i/N - \Omega_{i,1}. \quad (4.3.8)$$

The resulting bias currents, I_{Bias_1} and I_{Bias_2} , from expressions (4.3.6) and (4.3.7) have been used to design the 9 current steering DAC cells. These bias currents and the corresponding g_m weights have been re-used among the three interpolation regions in Table 4.1 to cover the entire range of $[0^\circ \ 40^\circ]$ with 2.5° steps as previously discussed.

Employing a two-stage PI while selectively switching to the appropriate interpolation region keeps the bias currents ratios and the corresponding g_m weights within the most linear range of the second stage. This enables the architecture to avoid the non-linearities that would otherwise occur at the boundaries where bias current weights differ by significant amounts. The output phase error of the two-stage phase shifter is plotted in Fig.4.12.

The maximum phase error does not exceed 0.25° at 2 GHz. This translates to 2.25° error at the ninth harmonic. This error can be calibrated out as part of the calibration step. The loss of the phase shifter ranges between ± 1.5 dB and it is compensated for by the following limiter stage.

4.3.2 High-order Harmonic Synthesis

Once the distributed ninth-subharmonic reference signals are phase shifted to the desired phase sequence, high-order harmonics are synthesized at each front-end location. The harmonic synthesis technique that has been discussed in Section 3.4 is adopted in this case. That is, by saturating

Figure 4.12: Output phase errors obtained from the two stage phase shifter.

Figure 4.13: Schematics of the pre-amplifier stages in (a) and the high-speed latch in (b).

the amplitude of the distributed reference signal and reducing its rise and fall times to a sufficient level (Fig. 3.8), the corresponding harmonic content (i.e. the ninth harmonic in this case) is enhanced. Optional tuned amplification can be performed prior to current injection into the oscillator depending on the harmonic synthesis approach sought, as will be discussed shortly.

In order to realize this harmonic synthesis block, a circuit technique has been adopted from high-speed regenerative comparators. According to (3.4.6), the harmonic content of a non-ideal square-wave (as expressed by the coefficients of the different harmonics in its Fourier series representation) is improved by enhancing both the amplitude, E , and the rise-time, δ . As such, in this technique, a number of preamplifier stages (i.e. negative exponential response) are employed to boost the input amplitude of the reference to sufficiently large levels. Once the desired level is reached, the reference signal is applied to a positive exponential response block, a high-speed latch in this case, to obtain the desired rise and fall times as per the analysis in Section 3.4.

The reason behind cascading negative and positive exponential blocks to allow faster rise and fall times has been analyzed under the context of high-speed regenerative comparators [89] and is explained as follows. As the distributed reference signal swing reaches the desired level, the pre-amplifiers' outputs are limited by their slew rate and hence the need for a circuit with a regenerative response to enhance the rise- and fall-time.

The harmonic synthesis stage is shown in Fig.4.13 as a cascade of three differential gain cells with resistive loads followed by a differential transconductance and a high-speed latch with inductive peaking. A dedicated current sink for the cross-coupled positive feedback transistors has been employed to allow for a faster response [90].

Circuit Analysis and Design

A small-signal s-domain analysis for the latch circuit and its equivalent model in Fig. 4.14 has been conducted and the results are used herein to aid the qualitative and quantitative understanding of the operation of this circuit block. An expression for the differential latch output voltage, ΔV_{out} , when responding to a differential input current, ΔI_{in} , is given by,

$$\frac{\Delta V_{out}(s)}{\Delta I_{in}(s)} = \frac{s + R_D/L}{s^2 + s \left(\frac{G-g_m}{C_D} + \frac{R_D}{L} \right) + \frac{(G-g_m)R_D+1}{LC_D}} \quad (4.3.9)$$

where the damping factor, ζ , and natural frequency, ω_n , are given by

$$\zeta = \frac{(G - g_m)L + R_D C_D}{2\sqrt{[(G - g_m)R_D + 1]LC_D}} \quad (4.3.10)$$

Figure 4.14: A zoomed in schematic showing the latch, its input transconductance and the cascode transconductance following it. The equivalent small-signal schematic is also shown where the input transconductance is included via the differential current source. Except for the inductive peaking load, all other single ended capacitive and resistive loads at nodes X and Y are lumped into G and C_D , respectively.

and

$$\omega_n = \sqrt{\frac{(G - g_m)R_D + 1}{LC_D}} \quad (4.3.11)$$

, respectively. In (4.3.10) and (4.3.11), g_m and G are the trans- and output conductances of the latch transistors, respectively. R_D and L are the series load resistance and inductance, respectively. C_D is the total single-ended load capacitance seen at X and Y to ground including $C_{gd,1,2} + C_{db,1,2} + C_{gs,3,4} + C_{db,3,4} + 4C_{gd,3,4} + C_{gs,5,6} + 2C_{gd,5,6}$.

It is noted from the transfer function in (4.3.9) that the addition of the inductor in series with the load resistor resulted in an increasing impedance with frequency, a zero at $-R_D/L$, enhancing the latch bandwidth. The closer the zero location is to the complex* poles at $-\zeta\omega_n \pm j\omega_n\sqrt{1-\zeta^2}$, the faster the rise-time of the latch at the expense of an increased overshoot provided that both the available bandwidth and the slew-rate are sufficient as will be discussed shortly.

Fully switching the tail current between transistors M_1 and M_2 forces the $|\Delta I_{in}|/2$ to initially discharge (charge) the parasitic load capacitance C_D on node X and charge (discharge) that on Y. This is due to the inductors impeding the instantaneous change of the differential current through them. This in turn sets up the latched state for switching prior to letting the differential current flow through load resistors. Once the differential current is through the load resistors, the change in voltage on X and Y by $\pm\Delta I_{in}R_D/2$ turns M_4 off (on) and M_3 on (off) while re-enforcing one another (due to the positive feedback) completing the latch switching operation.

---

*Upon expanding the term $(2\zeta\omega_n)^2 - 4\omega_n^2$ symbolically using (4.3.10) and (4.3.11), the resulting terms included $-(2/LC)^2$ which is many orders of magnitudes higher than any other positive term and hence the complex roots of (4.3.9).

Upon performing parametric analysis on the time-domain expression obtained from the inverse La-place transform of the transfer function in (4.3.9), it has been observed that the magnitude of this ΔI_{in} and the switching speed of M_1 and M_2 significantly impact the speed of the latch operation and consequently the rise/fall time. The steady-state output swing $(\Delta I_{in} + I_{latch})R_D$ is also a strong function of the this differential current and so is the magnitude of the harmonic.

In order to quantify the slew-rate and bandwidth requirements of the latch and synthesize a circuit design strategy, the analysis in Section 3.4 has been re-adopted. According to (3.4.3), for a trapezoidal signal with a differential output swing of ΔV_{out} , the required slew-rate at the output can be expressed as

$$\begin{aligned} \left. \frac{dv(t)}{dt} \right|_{max} &= \frac{d}{dt} \left\{ \frac{2\Delta v_{out}}{\pi} \sum_{n=1}^N \left[\frac{\sin[(2n-1)\delta\omega]}{(2n-1)\delta\omega} \cdot \frac{\sin[(2n-1)\omega t]}{(2n-1)} \right] \right\} \\ &= \frac{2\Delta v_{out}}{\delta\pi} \sum_{n=1}^N \left[\frac{\sin[(2n-1)\delta\omega]}{(2n-1)} \right] \end{aligned} \quad (4.3.12)$$

where, $\delta = 0.625t_{rise}^*$. If the trapezoidal output signal is represented by up to the ninth-harmonic of its Fourier components (i.e. $2n-1 = 9$), (4.3.12) yields a required slew-rate better than 12 mV/ps for a $\Delta v_{out}=450$ mV and $t_{rise} > 35$ ps.

As for the latch bandwidth requirement, for a desired $t_{rise} < 35$ ps, the -3 dB bandwidth should exceed $0.35/t_{rise} > 10$ GHz. As was mentioned previously, inductive peaking extends the bandwidth and therefore having a bandwidth requirement can aid the choice of the load inductor if a direct relationship is established. Moreover, the choice of the inductor may deliberately be made to yield a maximally flat group delay behaviour to preserve the phase relationships among the different harmonics [85].

In order to establish a relationship between the latch bandwidth and the load inductor, an estimate of the bandwidth enhancement due to inductive peaking has been sought. Following the procedure in [85] where the ratio $m = (R_D C_D)/(L/R_D)$ is used as a design parameter. By equating the square of the magnitude of the transfer function $|\Delta V_{out}(\omega)/\Delta I_{in}(\omega)|^2$ in (4.3.9) to $(1/2)[R_D/(1+(G-g_m)R_D)]^2$ (i.e. half of the squared magnitude of the its DC value), ω_{-3dB} can be solved for. Normalizing the result to the uncompensated bandwidth, $\omega_{-3dB} = (G'-g_m)/C_D$, where $G' = G + 1/R_D$, a rather involved expression is obtained for the enhancement ratio $\omega_{-3dB}/\omega'_{-3dB}$. However, assuming $G \ll g_m$, this expression has been used to confirm that the maximally flat group delay choice of $m = 3$ yields an enhancement ratio of 1.6, in agreement with that in [85]

---

*It is noted that 2δ is equivalent to 0-100% rise- and fall-time by inspection from Fig. 3.7. For a 10-90% equivalent, t_{rise} is set to 80% of 2δ .

despite the inclusion of the negative g_m stage herein. It has also been found that this enhancement ratio is fairly constant (changes are below 4%) for a $g_m R_D < 1$.

As a result, $(C_D R_D)/(L/R_D) = 3$ has been used. For a targeted $\omega_{\text{3dB}} = 10 \text{ GHz}$, the uncompensated bandwidth is $\omega'_{\text{3dB}} \simeq 6.25 \text{ GHz}$. Letting $\omega'_{\text{3dB}} \approx 1/(C_D R_D)$, it follows that $(L/R_D) \approx 54 \text{ ps}$ - a very useful design relationship between the load inductor and resistor. For a desired output differential swing, ΔV_{out} , and a current budget $(\Delta I_{\text{in}} + I_{\text{latch}})$, R_D is initially determined and so is L_D . Also, it has been initially assumed that $\Delta I_{\text{in}} = I_{\text{latch}}$ subject to changes during the design such that the total current is kept constant. It must be noted however that the previously discussed slew-rate requirement dictates a lower bound on ΔI_{in} for a given C_D which is only known after the transistor sizes have been determined. This means a number of iterations through these design calculations are to be expected until all performance numbers are satisfied.

A high-speed current centric design approach [88] [91] has been adopted in designing this circuit. In this approach, each transistor in a fully-switching differential pair is sized and biased to carry a current density of $0.15 \text{ mA}/\mu\text{m}$ in its balanced state. This way, when the CML pair is fully switched, the ON transistor is operated at its $J_{\text{peak},f_T} = 0.3 \text{ mA}/\mu\text{m}$.

In order to ensure full switching at the latch input transconductance pair, $\Delta V_{\text{in},\text{min}} \leq 600 \text{ mV}$ is assumed *. The required transconductance of $M_{1,2}$ is therefore $g_{m_{1,2}} = \Delta I_{\text{in}}/\Delta V_{\text{in},\text{min}}$. Knowing that g_m saturates at about $0.75 \text{ mS}/\mu\text{m}$ for a transistor current density above $0.3 \text{ mA}/\mu\text{m}$ [88], M_1 and M_2 widths have been selected such that $W_{1,2} = g_{m_{1,2}}/0.75$. Except for the current sink devices, gate lengths were kept at minimum size for higher f_T . The same sizing approach has been applied to the cross-coupled positive feedback transistors.

Once all transistor sizes are determined, C_D can be readily calculated based on transistors' widths, W_x , as

$$C_D = W_{1,2}(C'_{gd} + C'_{db}) + W_{3,4}(C'_{gs} + 4C'_{gd} + C'_{db}) + W_{5,6}(C'_{gs} + 2C'_{gd}), \quad (4.3.13)$$

where the per-unit-width parasitic capacitances C'_{gs} , C'_{gd} and C'_{db} are estimated as $1 \text{ fF}/\mu\text{m}$, $0.45 \text{ fF}/\mu\text{m}$ and $1.541 \text{ fF}/\mu\text{m}$, respectively [92]. The slew rate requirement can be checked at this point and iterations may proceed by altering ΔI_{in} or the total current if need be.

The pre-amplifier stages have been designed with a total gain of 12 dB to boost the voltage amplitude level from that available at the output of the phase shifter to that required at the latch input to fully switch the transconductance current. This effectively de-sensitizes the latch switching speed to the slight gain variations of the phase shifter as pointed out in Section 4.3.1.

---

*Employing an input voltage swing of about 1.5 times the minimum switching voltage of 400 mV has been recommended for this technology to ensure full switching [88].

Table 4.2: Active and passive device sizes as implemented in the harmonic synthesis block in Fig.4.14

M_{preamp}	R_{preamp}	$M_{1,2}$	$M_{3,4}$	$M_{5,6}$	L	R_{latch}
$16\ \mu m/120\ \text{nm}$	$700 - 800\ \Omega$	$18\ \mu m/120\ \text{nm}$	$16\ \mu m/120\ \text{nm}$	$18\ \mu m/120\ \text{nm}$	$470\ \text{pH}$	$50\ \Omega$

After a number of design iterations using the methodology outlined above, a 470 pH inductor with a peak Q at 21 GHz has been selected in this design to achieve a bandwidth enhancement of about 1.5 times [85]. The rest of the component values are listed in table 4.2. The harmonic synthesis stage draws a total of 10.5 mA.

Noise Considerations

Given that the signal amplitude available for the latch circuit to switch is much larger than the latch transition region, the mechanisms by which different types of noise corrupt the output can be understood in a much similar manner to that in a single balanced mixer [93] [94].

Flicker noise in the tail current source is commutated and translated up by the switching cross coupled pair as AM sidebands near the fundamental and its odd harmonics producing no PM in this case. Noise near the fundamental and its odd harmonics (i.e. $\omega_{0,n}$, $3\omega_{0,n}$, $5\omega_{0,n}$, $7\omega_{0,n}$ ... etc.) produce sidebands at very low frequencies and near the corresponding even harmonics (i.e. $2\omega_0$, $6\omega_0$, $10\omega_0$, $14\omega_0$ ... etc.) many of which are beyond the latch bandwidth and hence largely attenuated. Noise components originating near the even harmonics $2\kappa\omega_{0,n}$ where κ is a positive integer - or those transferred due to mixing - land on sidebands near $9\omega_0$ through another mixing process with the square-wave fundamental frequency and its odd harmonics. It is noted that for the mixing frequency pairs to yield PM sidebands, one sideband needs to be a result of a frequency downconversion (e.g. $(10\omega_{0,n} - \omega_0)$) while the other be of a frequency upconversion (e.g. $4\omega_{0,n} + 5\omega_0$)*. Since the magnitudes of the mixing odd harmonics are unequal, these mixing processes yield non symmetric outputs partially contributing single sidebands near the carrier. Therefore, in the absence of a AM-PM conversion mechanism, only the even harmonic noise components originating in the tail current source or those generated through a mixing process produce phase noise [94].

White noise in the cross coupled switching transistor pair contributes noise at the output only during the window of time when they are both ON at the zero-crossings. The power spectral density of the output noise current has been shown in [93] to be inversely proportional to the slope at the zero crossing. Designing for fast rise- and fall-time is in line with maximizing this slope

---

*If this condition is *not* satisfied, the mixing process yields AM sidebands (e.g. $(10\omega_{0,n} - \omega_0)$ and $(12\omega_{0,n} - 3\omega_0)$).

or minimizing the window of time during which both transistors are ON and therefore leading to less white noise contribution from the switching pair to phase noise at the output.

Flicker noise in the switching transistors at $\omega_{m,n}$ contribute noise to the output at $\omega_{m,n}$ and at $2\kappa\omega_0 \pm \omega_{m,n}$ where κ is a positive integer [93] [94]. Once again, a mixing process with the square-wave fundamental frequency or its odd harmonics yields non symmetric sidebands near the carrier. The output flicker noise current is also inversely proportional to the slope at the zero crossing and is minimized by ensuring fast rise- and fall-time.

Architecture Variations and Trade-offs

Once a harmonic-rich signal has been synthesized, it is either injected directly into the oscillator relying solely on its filtering or, an additional filtering stage is added to suppress the fundamental and undesired harmonics. We denote the former as *approach 1* and the latter as *approach 2* (Fig. 4.15). Subject to its insertion loss, passive filtering attenuates the injected fundamental and its undesired harmonics at the expense of the desired harmonic amplitude and the oscillator locking range. A Q-enhanced tuned filter can be employed to simultaneously attenuate the injected fundamental while boosting the desired harmonic [81].

Figure 4.15: Schematics of the pre-amplifier stages in (a), the high-speed latch in (b) and the Q-enhanced tuned amplifier stage in (c).

Another variation on this latter technique is to rely on the tuned amplification of the Q-enhanced filter to boost the desired harmonic at the output of the pre-amplifiers while eliminating the high-speed latch. We denote this as *approach 3*. The resulting phase noise, the amplitude of the desired harmonic, the power dissipation and the silicon area are among the important trade-offs involved. The three harmonic synthesis circuit approaches have been investigated to explore and compare these trade-offs. In designing the corresponding circuits for each approach, the amplitude of the ninth harmonic output has been kept approximately constant. With all other building blocks unchanged, this yields a relatively constant oscillator locking range and allows

a fair comparison among the phase noise profiles of the three approaches*. Table 4.3 highlights and compares a number of performance metrics among the three approaches. The time-domain output signals and their frequency content are shown in Figures 4.16, 4.17 and 4.18. The phase noise floor profiles for the three circuit approaches have been compared twice in simulations; first, as a stand-alone block and second, with the whole architecture (i.e. poly-phase filter, phase-interpolator, the circuit approach being investigated and the VCO). The two comparisons are shown in Fig. 4.19 and Fig. 4.20.

Table 4.3: A comparison between the three harmonic synthesis approaches

	Limiting amplifiers +Latch	Limiting amplifiers + Latch + QEN [†]	Limiting amplifiers + QEN
Magnitude of 9th Harmonic	63.5 mV _{pp}	63 mV _{pp}	62.9 mV _{pp}
Magnitude of fundamental	540.7 mV _{pp}	1.6 mV _{pp}	1.63 mV _{pp}
Current consumption	10.5 mA [†]	10.6 mA [†]	5.6 mA [†]
Phase Noise (stand-alone)	Fig. 4.19		
Phase Noise (Complete chain)	Fig. 4.20		

[†] The injection transconductance consumes 3.6 mA to 3.8 mA - not included here since it is not part of the harmonic synthesis operation.

It is noted that the phase noise profiles in Figures 4.19 and 4.20 have been obtained through driven periodic steady state (PSS) and periodic noise (PNoise) simulations. In these simulations, an ideal signal source has been used and therefore, the numbers obtained represent the best phase noise possible, or the phase noise floor, for a given design for each of the three circuit approaches.

It is seen that *approach 1* (i.e. limiting amplifiers and latch) has a better phase noise floor compared to the other two at the expense of a higher power consumption and magnitude of the injected fundamental as shown in Figures 4.16 to 4.19. It is believed that the better phase noise floor in this approach is due to the inherently rich 9th harmonic content of the synthesized trapezoidal signal. This is unlike the other two approaches (2 & 3) where a Q-enhanced filter has been employed to boost the 9th harmonic at the output of the limiting amplifiers. The noise shaping in the Q-enhanced tank circuit raises the phase noise floor near the desired harmonic. Moreover, the inclusion of varactors in the Q-enhanced tank provides a means of AM-PM conversion. Flicker noise originating in the tail current source which gets up-converted near the carrier as AM sidebands can now be converted to PM degrading the close-in phase noise - as discussed

---

*The normalization to carrier power per unit bandwidth is the same among the three circuit approaches in this case.

Figure 4.16: A single-ended time domain signal and its frequency content at the output of the high-speed latch as obtained from a periodic steady-state (PSS) simulation.

Figure 4.17: Shown at the top are the single-ended time-domain signals at the latch output and the Q-enhanced filter following it. The frequency content of the Q-enhanced filter output is shown at the bottom. Results are obtained using a periodic steady-state (PSS) simulation.

Figure 4.18: Shown at the top is the single-ended time-domain signal at the output of the Q-enhanced filter directly following the preamplifiers in the third approach. The frequency content of the Q-enhanced filter output is shown at the bottom. Results are obtained using a periodic steady-state (PSS) simulation.

Figure 4.19: Phase noise profiles of the three high-order harmonic synthesis approaches without the phase shifter or the VCO connected.

Figure 4.20: Phase noise profiles of the three high-order harmonic synthesis approaches with the phase shifter and VCO connected.

in Section 4.3.2. It is also noted that due to the large Q values that can be reached by using Q -enhanced filters and the sensitivity of the magnitude of the desired harmonic to the peak- Q frequency, a tuning scheme is needed where a Q -enhanced filter is used. This further complicates the adoption of either *approach 2* or, *approach 3*, especially if this tuning scheme is needed next to each array element front-end. The magnitude of the transferred reference fundamental tone to the output influences the amount of deterministic phase jitter of a locked VCO as will be discussed in Section 4.4. Lastly, the extra silicon real-state penalty in *approach 2* due to the added circuitry and passive components proves unnecessary as its performance nears the other two approaches. As a result, the second approach is dismissed from any further comparative discussions.

4.3.3 Current injectors and the LC-VCO Design

A differential transconductor stage has been employed to convert the output voltage signal of the harmonic synthesis stage to a current signal and inject it into the tank of an NMOS negative-gm oscillator as is shown in Fig. 4.21. Due to the isolation provided by the transconductor, this coupling technique approximates a unilateral coupling between the harmonic synthesis stage and the oscillator. Biasing of both the transconductor and the oscillator current sink devices has been arranged such that it can be modified by off-chip DACs to facilitate phase offset calibration as previously discussed.

Figure 4.21: Schematics of the injection transconductor, the negative- g_m oscillator and buffers.

Owing to the Q limitation of the thin oxide accumulation-mode nMOS varactors available in the 130 nm kit at 18 GHz, thick oxide MOS varactors were used for tuning instead. Upon inspecting their correlation curves and characterizing their C-V behaviour, it was observed that 99% of the maximum varactor capacitance could be reached at $V_{gd} = 1.2$ V. It is noted however that C_{max}/C_{min} is lower than that of the thin oxide nMOS varactors and so a direct trade-off between the tuning range and the overall tank Q is a result in this case.

It is also noted that the metal-insulator-metal (MiM) capacitors in the desired range exhibited Q values close to 10 at 20 GHz and therefore, thin oxide varactors were used in place of fixed capacitors - despite the inherent AM-PM conversion obtained. Maintaining a fixed source/drain bias allowed for a constant Q value which is better than that of the MiM capacitors.

A comparison between the measured Q values of the available inductors and varactors in the design kit at 18 GHz revealed that the total tank Q is a strong function of both components. Unlike the case in the early gigahertz range, the equivalent parallel tank resistance, R_p , is now shared almost equally between the tank inductor and varactors*. Based on an observation of the correlation curves, an initial estimate of $Q_L > 20$ and $Q_V \leq 20$ was used as a starting point for the design leading to an initial total tank $Q_{tank} \approx 10$. However, this total Q is expected to degrade further due to input impedance of the buffer stage and the finite output impedance of the cross-coupled transistor pair and the injection transconductors.

A relationship between the negative-gm oscillator peak-to-peak differential voltage swing, $v_{pp,d}$, and its differential tank resistor, $R_{p,d}$, is given by

$$v_{pp,d} = \frac{4}{\pi} I_{SS} R_{p,d} \quad (4.3.14)$$

where,

$$R_{p,d} = \frac{R_{P,L} R_{P,v}}{R_{P,L} + R_{P,v}} \quad (4.3.15)$$

$$= Q_{tank} \omega_0 L_d \quad (4.3.16)$$

$$= \frac{Q_{tank}}{\omega_0 C_{v,d}} \quad (4.3.17)$$

and

$$\frac{1}{Q_{tank}} = \frac{1}{Q_{L,d}} + \frac{1}{Q_{V,d}}. \quad (4.3.18)$$

In (4.3.14), (4.3.15) and (4.3.18), $C_{v,d}$, L_d , $R_{P,L}$ and $R_{P,v}$ are the differential tank inductance, varactor capacitance and their associated parallel equivalent resistances, respectively. Let us choose one of the smallest symmetrical parallel spiral inductors available in the kit with $L_d \approx 178 \text{ pH}$ and a peak $Q_L > 20$ at 18.1 GHz[†]. With an average range of the total varactor $Q_V \leq 20$, an equivalent differential parallel tank resistance $R_{p,d} = Q_{tank} \omega_0 L_d = 208 \Omega$ is obtained. A differential peak-to-peak output swing of $v_{pp,d} \approx 1.2 \text{ V}$ initially requires an oscillator core tail current of $I_{SS} \approx 4.5 \text{ mA}$.

---

*Passive components model characterizations showed that varactors Q are more dominant in this frequency range as will be discussed shortly.

[†]An overall $Q_{tank} \approx 10$ is what has been used in the calculations since $Q_V \leq 20$.

The dimensions of the cross-coupled transistors have been chosen such that they experience complete switching with the specified output voltage swing [95] while delivering the required g_m to ensure oscillations startup. For a differential pair to experience complete switching, the differential input swing is related to the tail current and device dimensions by

$$\Delta v = \sqrt{\frac{2I_{SS}}{\mu C_{OX} \frac{W}{L}}}. \quad (4.3.19)$$

Substituting the numbers above in (4.3.19) yielded a $W/L = 28 \mu m / 0.12 \mu m$ assuming $\mu_n C_{OX} \approx 224 \mu A / V^2$ obtained through curve fitting of similar device dimensions and $0.35 V \leq V_{od} \leq 0.7 V$. A minimum channel length has been selected for these devices to minimize their capacitance contributions [95]. The condition for the startup of oscillation is given by

$$\frac{2}{g_m} \leq R_{p,d}. \quad (4.3.20)$$

It is noted however that the $R_{p,d}$ in (4.3.20) should represent all loss mechanisms in the oscillator but has been initially assumed to represent only that of the tank at this point in the design. It must also be noted that the g_m in (4.3.20) is the resulting average transconductance of the switching cross-coupled pair during a complete cycle. Owing to the nearly complete transistor switching and hence the multiple regions of operation during each cycle, this resulting g_m falls below $2/R_{p,d}$ for part of the period which may lead to cease of oscillation [95] [96]. Therefore, the estimated small-signal g_m has been verified against a greater value than $2/R_{p,d}$. For a $R_{p,d} = 208 \Omega$, (4.3.20) yields an overall $g_m \geq 10 \text{ mA/V}$ for oscillations to start. Given that the small-signal g_m reaches about $0.65 \text{ mA/V}/\mu m$ at a $J = 0.14 \text{ mA}/\mu m$ (i.e. $4 \text{ mA}/28 \mu m$) [88], a $28 \mu m$ device satisfied this oscillation startup condition.

For a defined single-ended load of $100 \mu m \times 100 \mu m$ RF chip pads, ESD structures and off-chip 50Ω termination, two buffer stages have been designed for the chosen output swing of the oscillator as will be discussed shortly. The first stage is a source follower for which the input transistor size is $28 \mu m / 0.12 \mu m$. With the dimensions of the cross-coupled, injection transconductance and buffer devices determined, an estimate of the minimum and maximum single-ended capacitance, $C_{var,min}$ and $C_{var,max}$ to allow a tuning range of 10% can be obtained by

$$\frac{1}{\sqrt{0.5L_d (C_{gs} + 4C_{gd} + C_{db} + C_L + C_{var,max} + C_{db,inj} + C_{gd,inj})}} = 0.95 \omega_0 \quad (4.3.21)$$

and

$$\frac{1}{\sqrt{0.5L_d (C_{gs} + 4C_{gd} + C_{db} + C_L + C_{var,min} + C_{db,inj} + C_{gd,inj})}} = 1.05 \omega_0. \quad (4.3.22)$$

Table 4.4: Active and passive device sizes and current consumption as implemented in current injectors, LC-VCO and buffers in Fig. 4.14

$M_{5,6}$	$M_{7,8}$	M_9	$M_{10,11}$	M_{12-15}	$M_{16,17}$
16 $\mu\text{m}/120\text{ nm}$	30 $\mu\text{m}/120\text{ nm}$	180 $\mu\text{m}/600\text{ nm}$	48 $\mu\text{m}/120\text{ nm}$	80 $\mu\text{m}/120\text{ nm}$	200 $\mu\text{m}/360\text{ nm}$

Varactors (ncap)	Varactors (DGncap)	L_d	$I_{SS, \text{inj}}$	$I_{SS, \text{VCO}}$
0.24 $\mu\text{m} \times 1\text{ }\mu\text{m} \times 18 \times 10$	0.24 $\mu\text{m} \times 1\text{ }\mu\text{m} \times 22 \times 10$	169 pH	3.6 mA	5 mA

In (4.3.21) and (4.3.22), $C_{gs} + 4C_{gd} + C_{db}$ is the load capacitance attributed to the cross-coupled pair while $C_{db, \text{inj}} + C_{gd, \text{inj}}$ to that of the injection transconductance pair. C_L models the input capacitance of the source-follower buffer stage following the oscillator. An additional C_p term could have been added under the square root to model the parasitic capacitance of the inductor but has been omitted here to simplify the calculations. The determined transistor sizes have been used to calculate the various parasitic capacitances in (4.3.21) and (4.3.22) where the per-unit-width parasitic capacitances C'_{gs} , C'_{gd} and C'_{db} were estimated as 1 fF/ μm , 0.45 fF/ μm and 1.541 fF/ μm , respectively [92]. The calculated $C_{\text{var}, \text{min}}$ and $C_{\text{var}, \text{max}}$ were 780 fF and 595 fF, respectively. Now that all active and passive device sizes have been determined, $R_{p,d}$ can be refined to a more accurate $R_{p,d, \text{total}}$ which can be estimated as

$$R_{p,d, \text{total}} = \left[\frac{1}{R_{P,L}} + \frac{1}{R_{P,v}} + \frac{1}{2R_{DS, \text{inj}}} + \frac{1}{2R_{DS, \text{ngm}}} \right]^{-1}. \quad (4.3.23)$$

The new estimate for the parallel equivalent differential tank resistor in (4.3.23) have been used to re-calculate the output swing and to verify the oscillation startup condition refining the obtained design until all specifications were met. A series of periodic steady-state (PSS), phase noise simulations and optimizations were performed and later followed by the layout design for which the final design details are provided in Table 4.4.

The characterization results of the final varactors and inductor are shown in Fig. 4.22 and Fig. 4.23, respectively. It is noted that by switching the fixed thin oxide nMOS varactor biasing between 1.2 V to 1.5 V, a wider range of $C_{\text{var}, \text{min}}$ and $C_{\text{var}, \text{max}}$ could be achieved. The oscillator tuning range is shown in Fig. 4.24 for three distinct biasing conditions of the thin oxide nMOS varactors. Since the oscillator is always going to be under injection of a ninth subharmonic source, its phase noise performance is dictated by the injection source with estimated phase noise degradation of $20 \log_{10}(N)$ where, $N = \omega_{0,i}/\omega_i$ at best [97]. This demanded that part of the design optimization effort be devoted to minimizing the $1/f$ and thermal noise propagating from the

Figure 4.22: Single-ended variable capacitance range and associated Q values of the combined thin and thick oxide nMOS varactors. The capacitance range has been obtained in simulations by continuously varying the control voltage of the thick oxide nMOS varactor (DGncap) while keeping that of the thin oxide nMOS varactor (ncap) constant at 1, 1.1 and 1.2, V.

Figure 4.23: Differential inductance and quality factor as extracted from a two port simulation of the symmetrical tank inductor.

phase steering and harmonic synthesis blocks (i.e. quadrature synthesis, phase interpolators, limiting amplifiers, the high-speed latch and the injection transconductance) and in turn degrading the oscillator phase noise [65].

The oscillator phase noise performance has been simulated with the injection transconductor stage and is shown in Fig. 4.25.

4.3.4 Output Buffers

The oscillator's tank has been isolated from external loads through a resistively loaded source follower stage acting as a low impedance node. In order to facilitate testing, a differential FT-doubler with a transformer-based T-coil peaked load [98] has been employed as a second buffer stage. A detailed schematic of the source follower and the FT-doubler buffers with the adopted wideband T-coil structure is shown in Fig.4.26. Not only that this topology approximately halves the load capacitance on the preceding buffer stage as is illustrated in Figure 4.27(a) [99], but also has been exploited to steer 3.4mA of 18GHz single-ended peak current to the combined T-coil/ESD structure, chip pads, on- and off-chip terminations.

Figure 4.24: The oscillator tuning range as obtained in simulations by continuously varying the control voltage of the thick oxide nMOS varactor (DGncap) while keeping that of the thin oxide nMOS varactor (ncap) constant at 1, 1.1 and 1.2, V.

The T-coil structure at the output of the FT-doubler buffer offers two key advantages. First is its ability to absorb large capacitive loads at node X while displaying a purely resistive output impedance, $Z_{out} = R_T$, at node A across a broadband frequency range [98] [100] where, R_T is an on-chip termination resistor for the output matching. It can be shown that for $R_o \gg R_T$ in Figure 4.27(b), Z_{out} remains resistive for all frequencies if the following conditions hold [98],

$$L_{1,2} = \frac{C_L R_T^2}{4} \left(1 + \frac{1}{4\zeta^2} \right) \quad (4.3.24)$$

$$C_B = \frac{C_L}{16\zeta^2} \quad (4.3.25)$$

$$K = \frac{4\zeta^2 - 1}{4\zeta^2 + 1}. \quad (4.3.26)$$

In (4.3.24)-(4.3.26), ζ is the damping factor of the T-coil network transfer function v_A/i_X and K is the coupling coefficient between L_1 and L_2 . For a uniform group-delay response, we have $\zeta = \sqrt{3}/2$ leading to $K = 0.5$, $L_{1,2} = C_L R_T^2/3$ and $C_B = C_L/12$.

The second advantage of adopting the T-coil structure is its bandwidth enhancement effect by

Figure 4.25: Simulated phase noise performance of the oscillator while connected to the injection transconductance stage and buffers.

Figure 4.26: Detailed schematics of the two buffer stages and output T-coil network.

Figure 4.27: (a) Input capacitance of the f_T doubler stage, (b) Output T-coil network with parasitic loading elements.

a factor of 2.72, a 70% increase over that attained through inductive peaking for the same type of response [85] [98]. This bandwidth enhancement technique is particularly useful to adopt in the FT-doubler output buffer as it provides a broadband measurement visibility into the harmonic content at the output of each LO-element.

The convenient fact that $L_1 = L_2$ in the governing equations enabled the realization of the T-coil network as a symmetric spiral inductor with its center tap representing the input terminal X as is shown in Figure 4.28 [98]. It is noted from (4.3.24) that the total inductance between terminals A and B , $L_{AB} = 2L_{1,2}(1 + K)$, is proportional to the square of the required termination impedance (i.e. R_T^2). As such, a trade-off has been encountered between the quality of the output match and the availability of a symmetric spiral inductor with an inductance value of L_{AB} , a suitable self-resonance and peak Q frequency for operation in the K-band. For example, with a capacitive load of $C_L = C_{ESD} + 2(C_{db} + C_{gd})^* = 458$ fF to be placed at node X and a termination admittance magnitude $|R_L^{-1} + R_{pad}^{-1} + sC_{pad}| \approx 47 \Omega$ at node A , the required total inductance for a uniform group-delay response (i.e. $K = 0.5$) is $L_{AB} = 2L_{1,2}(1 + K) = 3L_{1,2} \approx 1$ nH. Upon performing preliminary modeling in ASITIC[†], the choice of R_T had been lowered in calculations,

* C_{db} and C_{gd} have been estimated as 1.451 fF/ μm and 0.45 fF/ μm for the 80 μm width devices M_{13} and M_{15} , respectively [92].

[†]A symmetrical spiral inductor with the prescribed attributes (i.e. L_{AB} , SRF and Q) for operation in the K-band was unavailable in the IBM 130 nm kit at the time of design and had to be modeled from scratch.

Figure 4.28: T-coil structure realized as a symmetric spiral inductor with its center tap representing the input terminal X .

Figure 4.29: A distributed model for the T-coil structure when realized as a symmetric spiral inductor.

and in concurrent simulations with ideal lumped components, to about $38\,\Omega$ to yield a realizable $L_{AB} \approx 630\,pH$ with an initial SRF around 62 GHz in ASITIC. The number of turns, the outer diameter and the line width were synthesized to obtain the desired L_{AB} using the expressions in [101] while the turn spacing has been fine tuned to reach a coupling coefficient $K = 0.5$. The attributes of the implemented symmetrical spiral in place of the T-coil transformer are provided in Table 4.5 and its ADS Momentum EM simulation results are shown in Figure 4.30.

Table 4.5: Geometric parameters for the symmetrical spiral inductor in place of the T-coil transformer in Figure 4.28.

Outer Diameter	Width	Turn spacing	No. of turns
$78.5\,\mu m$	$4.24\,\mu m$	$5\,\mu m$	4

The distributed model shown in Figure 4.29 has been employed to represent the T-coil spiral structure in circuit simulations. As depicted, the spiral layout structure has been divided into eight identical sections ($A - 1, 1 - 2, \dots, 6 - B$) [98] which correspond to the unit sections in the distributed circuit model. The capacitive coupling between the adjacent turns is represented by the interwinding capacitances, C_{iW} , the fitting value of which allowed $C_B = C_L/12$ to be safely absorbed into the structure without the need for an extra lumped component [85]. The capacitance to the substrate, C_{sub} , the total inductance L_{AB} and the series resistance R_s have been distributed equally among the unit sections through C_{subU} , L_U and R_{sU} , respectively. A list of the fitting components' parameters are provided in Table 4.6.

Table 4.6: A list of the fitting parameters for the distributed circuit model shown in Figure 4.29.

L_U	R_{sU}	R_{pU}	C_{subU}	C_{iW}
$74.7\,pH$	$322.5\,m\Omega$	$2.69\,K\Omega$	$1.25\,fF$	$4.5\,fF$

Figure 4.30: Total differential inductance and quality factor of the symmetrical spiral inductor in place of the T-coil transformer as extracted from a two port ADS Momentum EM simulation.

Table 4.7: Device sizes and current consumption as implemented in the output buffer stages in Fig. 4.26

$M_{10,11}$	M_{12-15}	$M_{16,17}$	$I_{\text{buff,SF}}$	$I_{\text{buff,FT}}$
$48 \mu\text{m}/120 \text{ nm}$	$80 \mu\text{m}/120 \text{ nm}$	$200 \mu\text{m}/360 \text{ nm}$	2 mA,	12 mA

4.4 Simulations Results of the Complete Architecture

Two identical LO-elements were simulated in Cadence® Analog Design Environment® using the periodic steady-state (PSS) engine . The two LO-elements were isolated as described in Chapter 5. One LO-element was injection locked at a constant angle acting as a reference while the other being locked to 15 phase shifts between 0 and $2\pi/9$ with steps of 22.5° . Each phase shift has been generated by selecting the appropriate interpolation region $\Omega_{i_1} - \Omega_{i_2}$ through $I_{\text{Bias}, I_{i_j}}$ and $I_{\text{Bias}, Q_{i_j}}$ as described in Section 4.3.1. In each simulation, the resulting phase difference was calculated based on the delay between the oscillators time-domain waveforms over one period of the ninth subharmonic reference (i.e. nine periods of the oscillators outputs). A snap-shot of the locked oscillator waveforms are shown in Fig. 4.31 where a number of simulations results have been superimposed onto each other.

In Fig. 4.32, the obtained phase shifts are compared against the desired ones for *approach 1*

Figure 4.31: Superimposed time-domain waveforms individually obtained through periodic steady-state simulations. Each waveform corresponds to a locked oscillator output to a separate phase-shifter state as outlined in Section 4.3.1.

and 3, respectively. The maximum associated phase errors appear to be -3.1° and 0.5° before and after calibration for *approach 1*, respectively. As for *approach 3*, a maximum phase shift error of 4.29° is obtained. After calibration, this error has been brought down to 0.42° .

Due to the periodic phase perturbation of the subharmonic reference, both peak-to-peak time and phase deterministic jitter have also been recorded for 15 phase shifts between 0 and 2π when employing an ideal ninth subharmonic reference source. Fig. 4.33 shows a peak-to-peak time and phase deterministic jitter of 54.6 fs and 0.355° , respectively for *approach 1*. For *approach 3*, simulation results indicate a worst case 11 fs pk-to-pk deterministic jitter.

In order to emphasize effectiveness of the proposed phase shifting technique and differentiate it from other LO phase steering techniques, the resulting phase noise floor performance has also been recorded for each phase shift. This is to monitor any possible variations and to evaluate the impact of LO phase steering on the phase noise floor. As depicted in Fig. 4.34, the phase noise floor profile varies by a maximum of ± 0.6 , ± 0.4 and ± 0.3 dB at 100 KHz, 1 MHz and 10 MHz offsets, respectively, across the whole span of 0 to 2π phase shifts attained. These minor variations are believed to be due to the associated change of the phase shifter gain and biasing condition among different phase shifts. The fact that, with this proposed technique, the oscillator needs

Figure 4.32: Obtained versus desired phase shifts and the associated maximum phase errors before and after calibration for *approach 1* (top) and *approach 3* (bottom).

Figure 4.33: Peak-to-peak time and phase deterministic jitter as obtained from 15 separate phase shift simulations between 0 and 2π with 22.5° steps.

Figure 4.34: Variations of the phase noise floor performance at 100 KHz, 1 MHz and 10 MHz offsets across the whole span of 0 to 2π phase shifts attained.

not to operate at the edge of its locking bandwidth explains the observed independence of the obtained phase shifts from the phase noise performance. This is considered one of the main expected contributions of this work as compared to discussed techniques in Section 2.5.

4.5 Calculation of the Injection Locking Bandwidth and Injection Strength

Employing a square-wave to injection lock an oscillator has the advantage of enriching the injection strength, or ratio I_{inj}/I_{osc} , over that associated with *fundamental* tone injection (i.e. $f_{inj} = f_0$). In order to investigate the enhanced injection strength and the resulting locking bandwidth, an accurate estimate of the Q_{ext} has been sought to aid the calculation. A modified testbench where *only*, but *equal*, fundamental injection has been used to accurately determine the external tank Q_{ext} .

The one-sided injection locking bandwidth of the oscillator has been given in (3.1.15) as,

$$\Delta\omega_m|_{|I_{inj}| \ll |I_{osc}|} = \frac{\omega_0}{2Q_{ext}} \frac{|I_{inj}|}{|I_{osc}|}. \quad (4.5.1)$$

For an initial estimate of the tank $Q \approx 6.35$ based on (4.3.23) and a fundamental injection ratio $|I_{inj}|/|I_{osc}| \approx 7\%$ obtained from simulations, (4.5.1) predicted a single-sided locking bandwidth $\Delta\omega_m = 2\pi 100 \text{ MHz}$. Since this is only an estimate of the locking range, it is preferred to aim for a *quasi-lock* or a *fast beat* case in simulations. This allows us to exploit the resulting beat frequency, ω_b , to reach a more accurate estimate of $\Delta\omega_m$. It is noted that ω_b is the geometric mean of $(\omega_0 + \Delta\omega_m) - \omega_{inj}$ and $(\omega_0 - \Delta\omega_m) - \omega_{inj}$ [64] and therefore,

$$\Delta\omega_m = \sqrt{\Delta\omega_{inj}^2 - \omega_b^2} \quad (4.5.2)$$

where, $\Delta\omega_{inj} = \omega_0 - \omega_{inj}$. In extracting ω_b from simulations, a DFT operation of the oscillator output with a 1 MHz bin resolution requires simulation time in excess of $1 \mu\text{s}$. To shorten the simulation time without loss of accuracy, $\omega_b/2\pi$ has been deliberately selected larger than 10 MHz. Substituting in (4.5.2) yields $\omega_{inj}/2\pi \approx 100 \text{ MHz}$. Fig. 4.35 shows the DFT of the steady-state oscillator output as a result of injecting a signal at $\omega_{inj}/2\pi = (\omega_0 + \Delta\omega_{inj})/2\pi = 18.1465 \text{ GHz} + 100 \text{ MHz}^*$. It is seen that the resulting output spectrum is that of a *fast beat* case with an extracted $\omega_b/2\pi \approx 45 \text{ MHz}$. For higher side injection, the dominant sideband is at $(\omega_{inj} -$

---

*Upon modifying the testbench to that of only a fundamental injection, $\omega_0/2\pi = 18.1465 \text{ GHz}$. The oscillator center frequency could have been restored to its 18 GHz by modifying the varactors biasing but this has been avoided not to alter the tank between fundamental and square-wave injection cases.

$\omega_b)/2\pi = 18.2015$ GHz. The estimated single-sided locking range is thus obtained from (4.5.2) being approximately 89 MHz. Further simulations have revealed that the actual locking range for the oscillator fundamental injection is 90 MHz. Substituting in (4.5.1), the actual Q_{ext} has been solved for and is equal to 7.1 - 12 % higher than initially estimated.

A DFT of the oscillator output under higher side square-wave injection for a $\omega_{inj}/2\pi = 18.046$ GHz + 125 MHz = 18.171 GHz is shown in Fig. 4.36. The resulting output spectrum is that of a *quasi-lock* case with dominant spectrum component at ω_{inj} with $\omega_b/2\pi \approx 39$ MHz. Substituting in (4.5.1) using the Q_{ext} determined above yielded an estimated single-sided locking range $\Delta\omega_m/2\pi \approx 119$ MHz. Further simulations with $\omega_{inj}/2\pi$ at 18.163 GHz and 18.162 GHz (i.e. $\Delta\omega_{inj}/2\pi$ is 117 MHz and 116 MHz, respectively) revealed the actual single-sided locking range for a square-wave injection is $\Delta\omega_m/2\pi \approx 116$ MHz for which a locked oscillator spectrum is shown in Fig. 4.37.

Similarly, approaching the edge of the locking range from the lower end, a square wave injection at $\Delta\omega_{inj}/2\pi = -116$ and -112 MHz resulted in *fast beat* and *quasi-lock* cases, respectively, revealing an asymmetric locking bandwidth. Fig. 4.38 shows the resulting spectrum in the latter case with an $\omega_b/2\pi \approx 16.3$ MHz leading to a lower side locking range of 111 MHz. The spectrum of the locked oscillator at 17.935 GHz (i.e. $\Delta\omega_{inj}/2\pi = -111$ MHz) is shown in Fig. 4.38.

Now that the upper and lower locking ranges have been determined for the square-wave injection case, (4.5.1) was used to solve for the total injection strength and it is 9%, a 29% increase from the fundamental injection case. The resulting increase in the effective injection strength is due to the injected square-wave harmonic components which land on the oscillator fundamental after mixing in the injection transistor pair and the oscillator core. This also explains the corresponding enhancement in the locking bandwidth when it is compared to either the fundamental injection case mentioned above or to the filtered harmonic case in *approach 3*. Table 4.8 summarizes the simulation results obtained.

Figure 4.35: Oscillator output spectrum under a fundamental tone injection with $\Delta\omega_{inj}/2\pi = 100 \text{ MHz}$ (top) and the details of the locations of the sidebands (bottom).

Figure 4.36: Oscillator output spectrum in a quasi-lock mode under square-wave injection with $\delta\omega_{inj}/2\pi = 125 \text{ MHz}$.

Table 4.8: A summary of the simulation results obtained

Phase noise (free running)	-101 dBc/Hz to -102.5 dBc/Hz at 1 MHz offset
Phase noise floor (locked w/ the whole chain)	See Fig. 4.20
Oscillator tuning range (GHz)	16.98 - 19.3
Phase shift errors (max.)	-3.1° (without calibration) +0.5° (with calibration)
Deterministic phase jitter (p-p)	0.355°
Δ Phase noise variation (Max.)	± 0.6 dB at 100 KHz offset ± 0.4 dB at 1 MHz offset ± 0.3 dB at 10 MHz offset
Injection locking range ($\Delta\omega_m$)	116 MHz (upper) 111 MHz (lower)
Determined oscillator Q	7.1

Figure 4.37: A locked oscillator spectrum with $\omega_{inj}/2\pi = 18.046$ GHz + 116 MHz = 18.162 GHz

Figure 4.38: Oscillator output spectrum in a quasi-lock mode under square-wave injection with $\delta\omega_{inj}/2\pi = -112\text{ MHz}$ (top) and a locked oscillator spectrum with $\Delta\omega_{inj}/2\pi = -111\text{ MHz}$ (bottom).

4.6 Summary

An injection locking scheme has been introduced for LO-path phase shifting based phased-array architectures. The architecture takes advantage of frequency multiplication to synthesize multiple phases of ninth-harmonic tones in close proximity to RF/millimeter-wave injection-locked oscillators. This enables the architecture to relax the challenges associated with multi-phase signal distribution and designing phase shifters and conventional PLL building blocks at fundamental RF/millimeter-wave frequencies. A high-level description of the proposed architecture has been introduced highlighting its advantages. The details of the phase-shifting operation have been provided.

Later in this chapter, the analysis, design and implementation of the architecture building blocks have been discussed in details. Possible architectural variations have been explored for the harmonic synthesis block where a Q-enhanced bandpass filter was employed in two ways. Initially, the Q-enhanced filter was inserted after the limiting stages and high-speed latch to suppress the ninth-subharmonic fundamental prior to injection into the oscillator. Later, the filter enhancement of the desired harmonic has been exploited to completely replace the high-speed latch.

Simulation results have been provided for each variation at both the circuit block and architectural levels. The resulting phase noise performance, the amplitude of the desired harmonic, the power dissipation and the silicon area were among the important trade-offs discussed. Most notably, phase noise simulations revealed that the adoption of the Q-enhanced filter in *approach 2* and *approach 3* raises the noise floor considerably.

The maximum phase shift errors for *approach 1* were -3.1° and 0.5° before and after calibration, respectively. As for *approach 3*, a maximum phase shift error of 4.29° was obtained. With calibration, this error has been brought down to 0.42° . A peak-to-peak time and phase deterministic jitter of 54.6 fs and 0.355° , respectively have been obtained for *approach 1*. For *approach 3*, simulation results indicate a worst case 11 fs pk-to-pk deterministic jitter.

The impact of LO phase steering on the phase noise floor has also been observed for each phase shift. The phase noise floor profile had a maximum variation of ± 0.6 , ± 0.4 and ± 0.3 dB at 100 KHz, 1 MHz and 10 MHz offsets, respectively, across the whole span of 0 to 2π phase shifts attained. The use of external phase rotators eliminated the need for oscillators de-tuning to realize the phase shifts and thus the observed independence of the obtained phase shifts from the phase noise performance.

Finally, a comparison has been made to similar works from the literature to highlight the

potential power savings that can be achieved by adopting the proposed phase-shifting architecture.

Chapter 5

Isolation of LO-Elements on Silicon

In implementing the proposed architecture, unintentional coupling between distant but concurrently running oscillators on silicon may lead to undesired on-chip interactions. These interactions may yield oscillators driven into undesired modes of operations deviating from the originally intended functionality [52] [53]. While researchers focused on techniques to minimize coupling of passive components to and from low resistivity silicon substrates [102] [103], active devices still play an important role in coupling noise to and from the substrate and hence the need for circuit-, layout- and technology-based isolation techniques to weaken the effect of these undesired coupling channels.

As such, techniques at the active and passive device as well as the technology levels were employed to isolate the multiple K-band oscillators and the high-order harmonic synthesis blocks in each LO-element. The implementation details of the adopted isolation techniques are described in this chapter.

5.1 Potential Coupling Scenarios in the LO-phase Shifting Architecture

Potential coupling channels between LO-elements consisting of phase shifters, harmonic synthesis blocks and VCOs are highlighted in Fig. 5.1. These coupling channels can be categorized as; i) Active device level coupling through the substrate, ii) Passive device level coupling and iii) Coupling through supply rails and the pad ring.

Coupling at the active device level between LO-elements may occur through the source- and drain-bulk junction capacitances and through the body contact of each device while sharing the substrate. With a $1\ \Omega\cdot\text{cm}$ substrate resistivity, the LO-element to element isolation is challenging in this architecture due to the harmonic synthesis stages and the multiple on-chip LO's. The large

Figure 5.1: Potential Coupling channels in the proposed LO-phase phase-shifting architecture.

signal levels associated with the limiting action through the cascaded pre-amplifiers (Fig. 4.21), the rise/fall time enhancement through the high-speed latch and the large LO drive (needed for the down-conversion mixers) are treated as noise being injected into the substrate and picked up by a neighbour LO-element. This effect is considered critical in this architecture since the progressive phase-shift between the array LO-elements is provided through injection locking through an up-multiplied subharmonic. As such, instead of having independently phase-locked oscillators through injection on the same die, noise traveling through the substrate may render the multiple on-chip oscillators as a coupled oscillator array, an undesired arrangement in this case due to its limited scanning range and gradual phase-noise degradation [49]. Alternatively, if coupling through these identified channels is too weak to result in a coupled oscillator array, the magnitude of any coupled tones should be minimum to avoid significant spurs in the LO spectrum or DC offsets if a mixing process (between two phases of the same tone) is to occur between LO-elements.

Potential coupling between LC-VCOs through the near-field regions of their respective tank inductors [103] or through inductors' noise pickup from the substrate can lead to oscillator frequency pulling (e.g. quasi-lock or fast beat phenomenon described in Section 3.2) [102]. In addition to this coupling possibility through oscillator tank inductors, the inductive peaking required in the high-order harmonic synthesis block (Fig. 5.1) may also yield the undesired inter-injection locked oscillator-array arrangement discussed earlier if the isolation between the passive components of

Figure 5.2: A block diagram of two LO-elements separated by Moat areas.

the various LO-elements is insufficient.

5.2 Isolation Techniques Adopted and Simulations

A number of different techniques and simulations were adopted in order to detect, minimize and test any potential coupling between the LO-elements on the same substrate. The following subsections describe the techniques and simulations involved.

5.2.1 At The Active Device Level

All NMOS transistors were implemented using the triple-well (TW) technology. The TW RF devices are formed inside a local P-Well over an isolating deep N-Well layer on a P^+ substrate. In each local P-Well island, the P-Well contacts (i.e. device body) were connected to the device source terminal shorting C_{sb} . Reverse biasing the P-/N-Well and the P^+ /N-Well parasitic diodes at the respective Well interfaces was implemented through low-impedance bias paths to dedicated power rails. To avoid potential N-Well coupling, power rails were decoupled for each LO-element through high density dual-MiM capacitors to save area as shown in Fig. 5.3. Moreover, the impedance level of the Well-bias paths bears an important trade-off. While lower impedance levels are more effective in shorting noise, higher impedance levels imply higher intrinsic voltage gain for the TW devices [104]. The Well-bias path impedance-level was optimized for shorting the noise frequency at 18 GHz while allowing a reasonable TW device intrinsic gain. More effective TW isolation was realized by employing separate - as opposed to merged - TW's for the critical devices and circuit blocks (e.g. VCO and harmonic synthesis) in each LO-element.

5.2.2 At The Technology And Process Level

The two LO-elements were further isolated by the high impedance of the lightly doped substrate regions (i.e. MOATs) after a substrate contact ring surrounding each element. As depicted in

Figure 5.3: Location of Moat areas on chip (top) and a resulting conceptual schematic and test bench (bottom).

Fig. 5.3, potential noise injection from each LO-element into the substrate is surrounded by an AC-grounded N-Well, a shunt low-impedance path to chip ground through the substrate contact ring and a series high impedance path (i.e. MOATs) to the substrate ring of the neighbour LO-element. A shallow trench isolation (STI) covers the blocked implant area above the P⁺ substrate. Each LO-element is also assigned a separate set of shielded pads to avoid coupling through the pad ring. By utilizing this combination of TW devices and the implicit filtering technique at the edge of each LO-element (i.e. Moat, substrate contact regions and N-Well), LO-element to element crosstalk through the substrate has been adequately suppressed as evidenced by the simulations results in Section 4.4. That is, noise injected into the substrate network by one LO-element was not sufficient to injection-lock or pull the other element and hence the independent phase steering achieved and the reported phase noise performance as reported in Chapter 7.

The schematic in Fig. 5.3 was simulated to estimate the achievable isolation levels. Two TW transistors were used in a source follower configuration separated by $100\mu\text{m}$ wide MOAT ring and surrounded by a substrate contact ring of $5\mu\text{m}$ width. The two substrate contact rings were connected through an estimated MOAT resistance calculated from the process parameters. The shorted source/body terminals of each device were used to access the foundry-modeled substrate network allowing signal injection into and pick-up from the substrate. Power rails were decoupled by 40 pF dual-MiM caps on each side of the MOAT ring. The isolation levels, $|S_{21}|$, were compared for several MOAT areas with and without decoupling. The worst-case isolation levels obtained were -77 and -53 dB with and without decoupling, respectively. This emphasized the effectiveness of power rails decoupling especially when employed to reverse bias the parasitic Well diodes despite the case of triple-well devices and MOAT areas.

5.2.3 At The Passive Device Level

Of all the passive components in the proposed architecture, the employed inductors are the most susceptible to contribute to LO-element to element coupling. Their contribution to coupling can be through substrate noise pickup or through the near-field EM coupling with other elements [103].

One of the techniques to shield inductors from coupling to and from the substrate is to place patterned ground shields directly underneath them. Shield patterns, or slots, prevent the flow of the induced currents on the shield itself to avoid short circuiting the magnetic flux [85]. Formed by metal, silicided poly-silicon or buried layers, ground shields are often connected to the available on-chip ground. However, obtaining a true 0 V reference potential on this “grounded” shield is challenging due to the inevitable interconnect parasitic inductance [105]. Due to the resulting non-zero charge on the shield, this impairment not only leads to loss mechanisms in the passive structure, but also makes the fluctuating ground shared among various blocks on the same die. Since ground level fluctuations can be strong functions of their respective circuit activity, a direct coupling between various passives among multiple circuit blocks occurs [105]. Floating metal shields is an effective technique through which a relative 0 V shield can be obtained [105]. The fact that each differential inductor has its relative 0 V shield, no direct interconnect exists between various circuit blocks on the die. This isolation is critical given the employed passives in the LC-oscillators. All differential inductors are implemented on the top metal layer and placed above floating patterned M1 shields to minimize coupling to and from the other oscillator and high-order harmonic synthesis blocks through the substrate. Fig. 5.4 shows the floating metal shielding employed in each oscillator tank inductor.

Figure 5.4: Floating patterned metal shields under the VCO tank inductor.

At a targeted oscillation frequency of 18 GHz, the operating wavelength λ_0 is 16.7 mm in free-space and about half as long in SiO_2 ($\sqrt{\epsilon_r} \approx 2$). Given a designed single octagonal loop oscillator tank inductor with a diameter of $100 \mu\text{m}$ and a turn width of $8.5 \mu\text{m}$, the circumference is approximated by $l \approx 314 \mu\text{m}$ allowing a safe electrically small loop antenna assumption for $l < \lambda_0/10$ [106]. Approximating this inductor by a circular loop antenna [107] placed in space such that its surface area vector is along the z -axis of a spherical coordinate system, the general expressions for the radiated fields can be shown [9] to take the form,

$$\begin{aligned} H_r &= \frac{jka^2 I_0 \cos \theta}{2} \left(1 + \frac{1}{jkr} \right) \frac{e^{-jkr}}{r^2}, \\ H_\theta &= \frac{-(ka)^2 I_0 \sin \theta}{4} \left(1 + \frac{1}{jkr} - \frac{1}{(kr)^2} \right) \frac{e^{-jkr}}{r}, \\ H_\phi &= E_r = E_\theta = 0, \\ E_\phi &= \frac{\eta(ka)^2 I_0 \sin \theta}{4} \left(1 + \frac{1}{jkr} \right) \frac{e^{-jkr}}{r}. \end{aligned} \quad (5.2.1)$$

In (5.2.1), a is the loop radius, I_0 is the current flowing around the loop, η is the intrinsic impedance of the medium and $k = 2\pi/\lambda$ where λ is the guided wavelength. The spherical region around the loop where $r < 0.1\lambda$ (or equivalently, $r \ll \lambda$), but still $r > l$, is known as the near-field region. In this region, $(kr)^{-3} \gg (kr)^{-2} \gg (kr)^{-1}$ and so only the terms with the largest inverse powers of r in the field expressions are dominant. This makes the imaginary terms of the magnetic, H_r , or electric, E_ϕ , field intensities more dominant than the real terms indicating reactive power associated with these fields [9], much like the case with electromagnetic and LC resonators [106]. That is, in the near-field region, the reactive power density is more dominant than the radiated power density and the energy oscillates between the electric and magnetic fields. In the far-field region, however, the situation is reversed and the radiated power density is more dominant as

$(kr)^{-1} \gg (kr)^{-2} \gg (kr)^{-3}$. The boundary between the near and far field regions is located at a radial distance r such that the magnitudes of the real and imaginary terms of H_r or E_ϕ in (5.2.1) are equal. This occurs when $kr = 1$, or equivalently, at $r = \lambda/2\pi$. In SiO_2 , the near/far field boundary for the loop under consideration corresponds to $r \approx 1.32 \text{ mm}$ at 18 GHz . For a $2 \text{ mm} \times 2 \text{ mm}$ silicon area allocated for the test chip, inductors are likely to be placed either well within this near field region or tens of micrometers away from its boundary. The existence of the floating metal shields underneath the oscillator tank inductors further complicates calculations and as such electromagnetic field solvers have been used to obtain an estimate of the potential field coupling between inductors. As per the floor planning of the final test chip, the oscillators' tank inductors were placed 1.364 mm apart (center to center). Figure 5.5 shows a 3-D view of the differential two-port model of the tank inductors in ADS Momentum atop of a silicon substrate. The resulting magnitudes of the forward transmission coefficient, $|S_{21}|$, are shown in Figure 5.6

Figure 5.5: A 3-D view of the differential two-port coupling model for the two oscillator tank inductors in ADS Momentum atop of a silicon substrate for the tank inductors.

where the inductors' center-to-center separation distance, S , was varied between 341 , 682 and $1364 \mu\text{m}$ in simulations. As expected, it is seen that the coupling increases as the inductors are brought close together. An estimate of the coupling between the two LC tank resonators was obtained as follows. Each oscillator tank inductor was fitted to the double- π broadband model [108, 109] shown in Figure 5.7 for which the component values extraction formulae are provided in Appendix A. The resulting two-port inductor coupling s-parameters data that was

Figure 5.6: Magnitudes of the forward transmission coefficient, $|S_{21}|$, as obtained in simulations for i) two oscillators' differential tank inductors and ii) two LC tank resonators. Two mutually coupled double- π inductor models were used based on the s-parameters data obtained from Momentum EM simulations in Figure 5.5. The inductors center-to-center separation distance, S , was varied between 341, 682 and 1364 μm .

obtained from Momentum® simulations in Figure 5.5 was fitted to that resulting from mutually coupling the corresponding two double- π models. The resulting mutual coupling coefficient K values between the two inductor models were 0.9E-3, 70E-6 and 1.25E-6, corresponding to $S = 341$, 682 and 1364 μm , respectively. The obtained two-port inductor coupling model was then connected to the oscillators' tank varactors on each side along with an estimate of the fixed I/O capacitive loading as illustrated in Figure 5.8. Simulation results of the LC tank resonator coupling are also shown in Figure 5.6 revealing increased coupling levels when compared to those obtained due to inductors only with the same separation distances.

It is noted that integrated phase arrays typically occupy large areas on silicon. For example, the 8-element array receiver in [1] occupied $3.5\text{ mm} \times 3.3\text{ mm}$ where the separation distance among the front-end modules was estimated at about 475 μm . Another example is the 4×4 integrated array transceiver in [2] which occupied $6.8\text{ mm} \times 3.8\text{ mm}$ with an estimated 1.75 mm separation distance among the front-end modules. As such, the chosen separation distances between inductors in simulations herein are representative of actual peer implementations from the literature.

In the proposed LO-path based phase shifting architecture, all the LO-elements are to be

Figure 5.7: A compact broadband inductor model.

Table 5.1: Extracted parameters for the double- π inductor model in Figure 5.7.

L	R_m	L_f	R_f	$C_{OX_{11}}$	$C_{SUB_{11}}$	$R_{SUB_{11}}$
76 pH	$458.6 \text{ m}\Omega$	10 pH	$236.3 \text{ m}\Omega$	9.67 fF	8.2 fF	219Ω
$C_{OX_{12}}$	$C_{SUB_{12}}$	$R_{SUB_{12}}$	$C_{OX_{22}}$	$C_{SUB_{22}}$	$R_{SUB_{22}}$	C_P
48.45 fF	16.37 fF	226.5Ω	14 fF	8.174 fF	243.2Ω	14 fF

Figure 5.8: Test bench used for evaluating the LC tank resonators coupling based on the two-port S-parameters data obtained from EM simulations in Figure 5.5. The inductor coupling model uses two mutually coupled double- π inductor models (Fig. 5.7) with coupling coefficient K values $0.9\text{E-}3$, $70\text{E-}6$ and $1.25\text{E-}6$ corresponding to $S = 341$, 682 and $1364 \mu\text{m}$, respectively.

operated at the same frequency with independent phase steering rendering the potential for frequency pulling among elements out of context. The discussed potential for *inter-injection* phase locking among the LO-elements, however, has been investigated in simulations by checking for oscillator coupling for which independent 360° phase steering is not possible [95]. Two LO-elements were simulated using the coupled tank inductors model in Figure 5.8 with independent output phase steering between 0° to 360° in steps of 22.5° as discussed in Section 4.4. In all element to element phase shifting scenarios, no phase coupling impairments were observed in simulations* that would restrict the independent phase shifting revealing no potential for inter-injection phase locking among the designed LO-elements. Resistors, capacitors and varactors were each implemented on isolated N-Wells.

A number of measurement test cases were carried out on the actual die to obtain the total spectral leakage levels and to further investigate any potential for inter-injection locking among the LO-elements. A discussion of the measured spectral leakage, its effects on oscillators' coupling and the results of leakage de-embedding is deferred until Chapter 7.

5.3 Summary

In this chapter, potential coupling scenarios in the proposed phase shifting architecture have been highlighted and discussed. In order to minimize coupling between two integrated LO-elements, a number of isolation techniques have been adopted at the active- and passive- device as well as the technology-levels. The implementation details of the adopted isolation techniques have been described. Due to their critical coupling role in oscillators' coupling on chip, passive tank inductors were treated as loop antennas and EM simulations were carried out to investigate their interaction at separation distances encompassing the boundary of their near-field regions. The associated coupling among the tank resonators have also been investigated revealing increased coupling levels compared to that solely due to tank inductors. Phase steering simulations of two LO-elements incorporating a developed inductors coupling model showed no phase coupling or inter-injection locking impairments.

---

*No coupling impairments have been observed in measurements as is discussed in Chapter 7

Chapter 6

Phase Calibration Techniques

Phase shift mismatches between multiple distant LO-elements in the proposed architecture are inevitable due to process variations in a naturally large chip. These mismatches are considered detrimental to the accuracy of the beam steering operation. The accuracy of the beam steering in the proposed architecture can be enhanced by seeking means of fine tuning the obtained phase-shifts. In this chapter, sources of phase-shift mismatches among LO-elements are highlighted. Multiple means of phase-shift fine-tuning and calibration are introduced. The sensitivity of these means are further analyzed mathematically.

6.1 Phase Shift Mismatches in the Proposed Architecture

Recall that in a n -element array, to obtain a successive phase shift, φ , between the outputs of the n oscillators, the phase shifters at each location are adjusted through their DAC's to phase shift the received reference signals to a phase sequence of $\psi_i/N, \psi_{i+1}/N, \dots, \psi_n/N$ such that $(\psi_i/N - \psi_{i+1}/N) = (\psi_{i+1}/N - \psi_{i+2}/N) = \dots = \varphi/N$, where $N = 9$ in this case. Upon synthesizing the ninth harmonic locally, the injection signals at the output of the comparators will have a phase sequence of $(\psi_i + \epsilon_i), (\psi_{i+1} + \epsilon_{i+1}), \dots, (\psi_n + \epsilon_n)$ at ω_i where, ϵ_i is a systematic phase shift introduced by the i^{th} harmonic synthesis stage. It is noted that any initial phase mismatches caused by routing the reference signals to distant front-end locations may all be lumped into the ϵ_i error. Therefore, the successive phase shifts between the outputs of the n injection locked oscillators can now be expressed with the aid of (6.2.1) as,

$$\begin{pmatrix} \phi_i - \phi_{i+1} \\ \phi_{i+1} - \phi_{i+2} \\ \vdots \\ \phi_{n-1} - \phi_n \end{pmatrix} = \begin{pmatrix} (\psi_i - \psi_{i+1}) + [\Delta\epsilon_i + \Delta\theta_i] \\ (\psi_{i+1} - \psi_{i+2}) + [\Delta\epsilon_{i+1} + \Delta\theta_{i+1}] \\ \vdots \\ (\psi_{n-1} - \psi_n) + [\Delta\epsilon_{n-1} + \Delta\theta_{n-1}] \end{pmatrix}. \quad (6.1.1)$$

In (6.1.1), the terms in brackets on the RHS represent the total LO-element to element phase error where $\Delta\epsilon_i = \epsilon_i - \epsilon_{i+1}$ and $\Delta\theta_i = \theta_i - \theta_{i+1}$. Only when these errors are eliminated can a desired progressive phase shift, φ , be obtained between the outputs of the n oscillators, that is $(\phi_i - \phi_{i+1}) = \dots = (\phi_{n-1} - \phi_n) = \varphi$.

It is seen from (6.2.2) and (6.2.1) that for the case of matched oscillators and equal injection strength, $\theta_i = \theta_{i+1} = \dots = \theta_n$. Sound layout skills and careful chip floor-planning may also help in improving the mismatches between the systematic phase-shifts among the individual blocks of each LO-element. However, Given the process, threshold voltage and temperature (PVT) variations, a robust calibration means is called for.

6.2 Phase Shift Calibration

Phase shift mismatches may arise between the outputs of the n LO-elements due to a number of sources: i) Phase shifters may introduce mismatches because of process variations. This effect is exacerbated by the naturally large chip areas of integrated phased arrays with each phase shifter located close to a distant front-end. ii) Phase shift mismatches may also occur as a result of unequal systematic phase shifts, ϵ_i , from the harmonic synthesis stages and reference signal routing to each LO-element. iii) Passive and active device mismatches between oscillators can further lead to $\theta_i \neq \theta_{i+1} \neq \dots \neq \theta_n$ as it is observed from (6.2.1) and (6.2.2). Careful chip floor-planning and sound layout skills can help in improving these mismatches among the individual blocks of each LO-element. However, given the inevitable process, threshold voltage and temperature (PVT) variations, a phase-shift calibration scheme and means are critical to make the architecture robust against such sources of phase shift mismatches.

Sources of fine tuning and calibration means are best introduced by recalling that in the steady state, the average output phase of the i^{th} oscillator, $\phi_{ss,i}$, will be locked to its locally injected signal phase, ψ_i , with a phase offset, θ_i , given by [64],

$$\theta_i|_{I_{inj,i} \ll I_{osc,i}} = \phi_{ss,i} - \psi_i \approx \sin^{-1} \left(\frac{\omega_{0,i} - \omega_i}{\Delta\omega_{m,i}} \right), \quad (6.2.1)$$

where,

$$\Delta\omega_{m,i}|_{|I_{inj,i}|\ll|I_{osc,i}|} = \frac{\omega_{0,i}}{2Q_i} \frac{|I_{inj,i}|}{|I_{osc,i}|}. \quad (6.2.2)$$

Upon re-examining (6.2.1) and (6.2.2), it is noted that for a given injected phase, ψ_i , at each location, the resulting phase offset, θ_i , is a function of the oscillator $Q_{i,osc}$, its center frequency, $\omega_{0,i}$, and the injection strength, $|I_{inj,i}|/|I_{osc,i}|$. These parameters can be exploited to perform the fine tuning of phase shift mismatches provided that the corresponding phase offset sensitivity to each parameter is adequate. Additionally, the cartesian phase-shifter current weights can also be used as a calibration means.

In order to illustrate this further, (6.2.2) is substituted in (6.2.1) and re-arranged to give,

$$\theta_i|_{|I_{inj,i}|\ll|I_{osc,i}|} \approx \sin^{-1} \left[\left(\frac{\omega_{0,i} - \omega_i}{\omega_{0,i}} \right) \left(\frac{2Q_i}{|I_{inj,i}|/|I_{osc,i}|} \right) \right]. \quad (6.2.3)$$

In Fig. 6.1, θ_i has been plotted versus the one-side relative injection bandwidth, $(\omega_{0,i} - \omega_i)/\omega_{0,i}$, for two different injection strength levels, $|I_{inj,i}|/|I_{osc,i}|$, and several Q_i values. It is shown how the step sizes of the phase offset can be controlled depending on the injection strength ($\propto |I_{inj,i}|/|I_{ss,i}|$) and its relative bandwidth. While $I_{ss,i}$ and $\omega_{0,i}$ of each oscillator may appear as two degrees of freedom for fine tuning, it is noted that the two are practically coupled from a circuit perspective. We defer this discussion to Section 6.3.1.

In order to gain more insight, the sensitivity of the LO-element output phase-offset, θ_i , is investigated analytically for each of the calibration means mentioned.

Figure 6.1: Resulting phase offset, θ_i , as a function of Q_i , the injection strength, $|I_{inj,i}|/|I_{osc,i}|$ and the relative injection bandwidth $(\omega_{0,i} - \omega_i)/\omega_{0,i}$. The arrow indicates the direction of increasing Q_i .

6.3 Calibration Sensitivity Analysis

6.3.1 Sensitivity to Oscillator Quality Factor

The oscillator tank $Q_{i,osc}$ has been shown to change as a function of the varactor biasing as discussed in Section 4.3.3. As such, it is instructive to examine the sensitivity of the phase offset, θ_i , as a function of the oscillator $Q_{i,osc}$. Expression (6.2.3) relates θ_i to $Q_{i,osc}$ in the vicinity of the oscillator center frequency at $\Delta\omega_i = \omega_{0,i} - \omega_i$. Differentiating (6.2.3) with respect to $Q_{i,osc}$, we have

$$\frac{d\theta_i}{dQ_{i,osc}} = \frac{(\Delta\omega_i/\omega_0)}{\sqrt{(I_{inj,i}/I_{osc,i})^2 - 4Q_{i,osc}^2(\Delta\omega_i/\omega_0)^2}} \quad (6.3.1)$$

Three main observations can be made here. First, $d\theta_i/Q_{i,osc}$ can be positive or negative depending on whether the frequency of the injected signal is below ($\Delta\omega_i > 0$) or above ($\Delta\omega_i < 0$) the center frequency of the oscillator, respectively. Second, the farther away the injection from the oscillator center frequency, the higher the sensitivity of the phase offset to changes in $Q_{i,osc}$. Third, $d\theta_i/Q_{i,osc}$ is inversely proportional to the injection strength, $|I_{inj,i}|/|I_{osc,i}|$. That is, for a given oscillation current, a larger magnitude of injection current makes the phase offset, θ_i , less sensitive to variations in $Q_{i,osc}$. This observation supports the idea of performing the frequency

multiplication prior to injection as has been proposed in Chapter 4. Synthesizing a high-order harmonic prior to injection such that the injected tone is a fundamental to the oscillator admits a higher injection strength than that of a sub-harmonic injection and thus the reduced sensitivity to variations in $Q_{i,osc}$.

6.3.2 Sensitivity to the Oscillator Tail Current

Varying the oscillator core current density by controlling the gate bias of the tail current sink, V_Q , has a direct effect on the phase offset, θ_i . In practical implementations, however, employing a DAC to control the oscillator core current will also have an effect on the oscillator center frequency. The accompanying change in the oscillator output swing, the bias-dependant parasitics and the asymmetric varactor voltage dependance are among the main reasons behind this effect [95]. Equation (6.2.3) points to another separate dependency of θ_i on $\omega_{0,i}$ and therefore, a change in the oscillator core current leads to a combined effect on the phase offset.

One way to investigate the combined sensitivity of the phase offset to variations in $I_{ss,i}$ is by expressing it using the total derivative and the chain rule as,

$$\frac{d\theta_i}{dI_{ss,i}} = \frac{\partial\theta_i}{\partial I_{osc,i}} \cdot \frac{\partial I_{osc,i}}{\partial I_{ss,i}} + \frac{\partial\theta_i}{\partial \omega_{0,i}} \cdot \frac{\partial \omega_{0,i}}{\partial I_{ss,i}} + \frac{\partial\theta_i}{\partial I_{inj,i}} \cdot \frac{\partial I_{inj,i}}{\partial Z_{in,i}} \cdot \frac{\partial Z_{in,i}}{\partial I_{ss,i}}, \quad (6.3.2)$$

where $I_{ss,i}$ is the bias tail current of the i^{th} oscillator core and $Z_{in,i}$ is the input impedance of the compensated oscillator tank as seen by the injection transconductor at resonance. This is illustrated in Fig. 6.2. The individual terms on the R.H.S. of (6.3.2) express the sensitivity of θ_i to changes in $I_{ss,i}$ through its direct dependence on $I_{osc,i}$, $\omega_{0,i}$ and $I_{inj,i}$. We now seek to develop expressions for these individual terms on the R.H.S of (6.3.2).

Figure 6.2: Effect of the input impedance of the compensated oscillator tank as seen by the injection transconductor at resonance.

A direct relationship between θ_i and $I_{osc,i}$ is found in (6.2.3). Differentiating (6.2.3) with

respect to $I_{osc,i}$ yields,

$$\begin{aligned}\frac{\partial \theta_i}{\partial I_{osc,i}} &= \frac{2Q_{i,osc}(\Delta\omega_i/\omega_0)}{\sqrt{I_{inj,i}^2 - 4I_{osc,i}^2 Q_{i,osc}^2 (\Delta\omega_i/\omega_0)^2}} \\ &= \frac{\tan \theta_i}{I_{osc,i}}.\end{aligned}\quad (6.3.3)$$

Recognizing that $I_{osc,i}$ and $I_{ss,i}$ are related as shown in Fig. 6.3, mathematically, the relationship can be expressed as,

$$\begin{aligned}I_{ss,i} &= \frac{I_{osc,i}}{2\pi} \int_0^{2\pi} |\sin \omega t| d(\omega t) \\ &= \frac{2}{\pi} I_{osc,i}.\end{aligned}\quad (6.3.4)$$

Figure 6.3: A time-domain representation of the relationship between I_{osc} and I_{ss} in a tail-biased negative-gm oscillator.

Therefore,

$$\frac{\partial I_{osc,i}}{\partial I_{ss,i}} = \frac{\pi}{2}.\quad (6.3.5)$$

The second term on the R.H.S. of (6.3.2) can be obtained as,

$$\begin{aligned}\frac{\partial \theta_i}{\partial \omega_{0,i}} \cdot \frac{\partial \omega_{0,i}}{\partial I_{ss,i}} &= \frac{\partial}{\partial \omega_{0,i}} \left[\sin^{-1} \left(\frac{2Q_i \Delta\omega/\omega_{0,i}}{|I_{inj,i}|/|I_{osc,i}|} \right) \right] \cdot \frac{\partial \omega_{0,i}}{\partial I_{ss,i}} \\ &= \tan \theta_i \left[\frac{1 - (\Delta\omega_i/\omega_{0,i})}{\Delta\omega_i} \right] \cdot \frac{\partial \omega_{0,i}}{\partial I_{ss,i}}.\end{aligned}\quad (6.3.6)$$

The third term on the R.H.S. of (6.3.2) can be expanded further as,

$$\begin{aligned}\frac{\partial \theta_i}{\partial I_{inj,i}} \cdot \frac{\partial I_{inj,i}}{\partial Z_{in,i}} \cdot \frac{\partial Z_{in,i}}{\partial I_{ss,i}} &= \frac{-\tan \theta_i}{I_{inj,i}} \cdot \frac{-I_s Z_{s,i}}{(Z_{s,i} + Z_{in,i})^2} \cdot \frac{\partial Z_{in,i}}{\partial I_{ss,i}} \\ &= \frac{\tan \theta_i}{(Z_{s,i} + Z_{in,i})} \cdot \frac{\partial Z_{in,i}}{\partial I_{ss,i}}.\end{aligned}\quad (6.3.7)$$

Substituting (6.3.3), (6.3.5)-(6.3.7) in (6.3.2), we have,

$$\frac{d\theta_i}{dI_{ss,i}} = \tan \theta_i \left[\frac{1}{I_{ss,i}} + \frac{1 - (\Delta\omega_i/\omega_{0,i})}{\Delta\omega_i} \cdot \frac{\partial\omega_{0,i}}{\partial I_{ss,i}} + \frac{1}{Z_{s,i} + Z_{in,i}} \cdot \frac{\partial Z_{in,i}}{\partial I_{ss,i}} \right]. \quad (6.3.8)$$

The derivative terms $\partial\omega_{0,i}/\partial I_{ss,i}$ and $\partial Z_{in,i}/\partial I_{ss,i}$ were evaluated in simulations as $2\pi \times 48.6 \text{ MHz/mA}$ and $37 \Omega/\text{mA}^*$, respectively. In order to facilitate comparisons between simulations and measurements and since $\phi_{ss,i}$ is the angle that is directly monitored at output of the LO-element, an expression relating $\partial\phi_{ss,i}/\partial I_{ss,i}$ and $\partial\theta_i/\partial I_{ss,i}$ is sought. Differentiating (6.2.1) w.r.t. $I_{ss,i}$ and substituting (6.3.8) in the result, we have,

$$\begin{aligned} \frac{\partial\phi_{ss,i}}{\partial I_{ss,i}} &= \frac{\partial\theta_i}{\partial I_{ss,i}} + \frac{\partial\psi_i}{\partial I_{ss,i}} \\ &= \tan \theta_i \left[\frac{1}{I_{ss,i}} + \frac{1 - (\Delta\omega_i/\omega_{0,i})}{\Delta\omega_i} \cdot \frac{\partial\omega_{0,i}}{\partial I_{ss,i}} + \frac{1}{Z_{s,i} + Z_{in,i}} \cdot \frac{\partial Z_{in,i}}{\partial I_{ss,i}} \right]. \end{aligned} \quad (6.3.9)$$

Figure 6.4 shows the sensitivity of $\phi_{ss,i}$ to changes in the core oscillator current as expressed by (6.3.9) versus the injection frequency offset, $\Delta\omega_i^\dagger$, for tank quality factors, $Q = 5, 7$ and 10 .

Figure 6.4: A plot showing the sensitivity of the LO-element output phase to changes in the core oscillator current, $\partial\phi_{ss,i}/\partial I_{ss,i}$, as a function of the injection frequency offset, $\Delta\omega_i$, for tank quality factors, $Q = 5, 7$ and 10 .

Two main observations can be made here. First, the slope of $\partial\phi_{ss,i}/\partial I_{ss,i}$ can be positive or negative depending on whether the frequency of the injected signal is below ($\Delta\omega_i > 0$) or

*This slope increases to $47.5 \Omega/\text{mA}$ towards $\Delta I_{ss,i} = -10\%$.

[†]Recall from (6.2.3) that θ_i is also a function of $\Delta\omega_i \equiv \omega_{0,i} - \omega_i$ and hence the choice to treat the latter as the independent variable despite the $\tan \theta_i$ term in (6.3.9).

Figure 6.5: Simulated output phase sensitivity to changes in the tail oscillator current, $\Delta I_{ss,i}$ and the associated phase noise variations.

above ($\Delta\omega_i < 0$) the center frequency of the free running oscillator, respectively. Second, the $\partial\omega_{0,i}/\partial I_{ss,i}$ term* in (6.3.9) makes this sign change of slope asymmetrical about $\Delta\omega_i = 0$. Figure 6.5 depicts the simulated $\Delta\phi_{ss,i}$ to changes in the tail oscillator current, $\Delta I_{ss,i}$, and the associated phase noise performance. A slope of $-1.7^\circ/\text{mA}$ is obtained at $\Delta\omega_i/2\pi = -43\text{ MHz}$ which is in good agreement with that observed in Figure 6.4 at the same injection frequency offset. The change of slope towards $\Delta I_{ss,i} = -10\%$ is attributed to a 27% increase in the $\partial Z_{in,i}/\partial I_{ss,i}$ term of (6.3.9) which was observed in simulations.

The appreciable amount of $\Delta I_{ss,i}$ which may be needed to calibrate phase errors in excess of 4° [†] can lead to altering the oscillator intrinsic operating region and performance. For example, while a considerable increase in $I_{ss,i}$ leads to a transition from a current limited to a voltage limited operating regime negatively impacting the phase noise performance, a gradual reduction in $I_{ss,i}$ steers the operating region below the current limited regime impacting the output signal swing and phase noise and may ultimately lead to cease of oscillations in extreme cases. In addition, since it is desirable to injection lock the oscillator near ω_0 to operate the closest possible to the $20\log_{10} N$ impact of frequency multiplication on phase noise, the asymmetric sign change of

*The $1/I_{ss,i}$ term in (6.3.8) is insignificant when it is compared to $\partial\omega_{0,i}/\partial I_{ss,i}$.

[†]As has been seen in simulations in Figure 4.32 and is further discussed in the prototype measurements chapter in Section 7.1.6.

$\partial\phi_{ss,i}/\partial I_{ss,i}$ about $\Delta\omega_i = 0$ makes it challenging to predict the trend of the calibration behaviour and automate it without an accurate measurement of $\partial\omega_{0,i}/\partial I_{ss,i}$.

6.3.3 Sensitivity to the Injection Strength

In studying the sensitivity of the phase-offset to the injection strength, $|I_{inj,i}|/|I_{osc,i}|$, it is noted that, in this architecture, the injection strength is controlled by varying the tail current of the injection transconductor pair, $I_{ss,inj}$. An expression describing the change in the phase offset due to a change in $I_{ss,inj}$ can be obtained as,

$$\frac{\partial\theta_i}{\partial I_{ss,inj,i}} = \frac{\partial\theta_i}{\partial(I_{inj,i}/I_{osc,i})} \cdot \frac{\partial(I_{inj,i}/I_{osc,i})}{\partial g_{m_{inj,i}}} \cdot \frac{\partial g_{m_{inj,i}}}{\partial I_{ss,inj,i}} \quad (6.3.10)$$

where $g_{m_{inj,i}}$ is the transconductance of the injection pair. The first term on the R.H.S of (6.3.10) can be obtained by differentiating (6.2.1) w.r.t. $(I_{inj,i}/I_{osc,i})$ to yield,

$$\begin{aligned} \frac{\partial\theta_i}{\partial(I_{inj,i}/I_{osc,i})} &= -\frac{2Q_{i,osc}(\Delta\omega_i/\omega_0)}{(I_{inj,i}/I_{osc,i})^2 \sqrt{1 - \frac{4Q_{i,osc}^2(\Delta\omega_i/\omega_0)^2}{(I_{inj,i}/I_{osc,i})^2}}} \\ &= -\frac{\tan\theta_i}{(I_{inj,i}/I_{osc,i})}. \end{aligned} \quad (6.3.11)$$

Recognizing that $\partial(I_{inj,i}/I_{osc,i})/\partial g_{m_{inj,i}} = v_N/I_{osc,i}$ where v_N is the N^{th} harmonic component input to the differential g_m injector stage and the fact that $\partial g_{m_{inj,i}}/\partial I_{ss,inj,i} = \beta/(2\sqrt{2I_{ss,inj,i}})$ where $\beta = \sqrt{\mu_n C_{OX} W/L}$, (6.3.10) can be re-written as,

$$\begin{aligned} \frac{d\theta_i}{dI_{ss,inj,i}} &= -\frac{\tan\theta_i}{(I_{inj,i}/I_{osc,i})} \cdot \frac{v_N}{I_{osc,i}} \cdot \frac{\beta}{2\sqrt{2I_{ss,inj,i}}} \\ &= -\frac{\tan\theta_i}{4I_{ss,inj,i}}. \end{aligned} \quad (6.3.12)$$

Expressing (6.3.12) in terms of $\phi_{ss,i}$ for it is the angle that is directly monitored at output of the LO-element, we have,

$$\begin{aligned} \frac{\partial\phi_{ss,i}}{\partial I_{ss,inj,i}} &= \frac{\partial\theta_i}{\partial I_{ss,inj,i}} + \frac{\partial\psi_i}{\partial I_{ss,inj,i}} \\ &= -\frac{\tan\theta_i}{4I_{ss,inj,i}}. \end{aligned} \quad (6.3.13)$$

It is seen from (6.3.13) that for a given $I_{ss,inj,i}$, the sensitivity of $\phi_{ss,i}$ to variations in the injection transconductor sink current has a strong dependency on the initial phase offset. Moreover, this sensitivity grows rapidly with the injection frequency offset, $\Delta\omega_{inj,i}$. Investing more current in $I_{ss,inj,i}$ to attain a desired locking bandwidth allows a finer tuning resolution. It must be noted

however that the obtained tuning slope is unsymmetrical about $\Delta I_{ssinj,i} = 0$. This is seen by inspection of (6.2.1) and (6.2.2) where a negative $\Delta I_{ssinj,i}$ (i.e. less injection current is used) leads to a narrower locking range $\Delta\omega_{m,i}$ or a larger phase offset, θ_i . This implies the risk of operating closer to the edge of the locking range and hence a phase noise performance impact. Therefore, this technique may only be considered when a sufficient locking bandwidth has been secured.

Figure 6.6: A plot showing the sensitivity of the LO-element output phase to changes in the injection transconductor tail current, $\partial\phi_{ss,i}/\partial I_{ssinj,i}$, as a function of the injection frequency offset, $\Delta\omega_i$, for tank quality factors, $Q = 5, 7$ and 10 .

6.3.4 Sensitivity to Phase-Interpolator I & Q Weights

Calibration can also be achieved in the phase interpolator following the quadrature synthesis block as shown in Fig. 4.1. Assuming a square-law device where $g_m \propto \sqrt{I_{Bias}}$, a desired angle ψ_i/N is realized by setting the g_m weights of the phase interpolators such that,

$$\psi_i/N = \tan^{-1} \left(\frac{g_{m,Q_i}}{g_{m,I_i}} \right) = \tan^{-1} \left(\sqrt{\frac{I_{Bias,Q_i}}{I_{Bias,I_i}}} \right). \quad (6.3.14)$$

In (6.3.14), I_{Bias,I_i} , I_{Bias,Q_i} , g_{m,I_i} and g_{m,Q_i} are bias currents and transconductances for the in-phase and the quadrature phase branches for the i^{th} phase interpolator, respectively.

For comparison purposes and since $\phi_{ss,i}$ is the angle that is physically monitored at output of the LO-element, expressions are recast in $\phi_{ss,i}$. Substituting (6.3.14) in (6.2.1), we have

$$\phi_{ss,i} = \theta_i + N \cdot \tan^{-1} \left(\sqrt{I_{Bias,Q_i}/I_{Bias,I_i}} \right). \quad (6.3.15)$$

It follows that the sensitivity of the output phase $\phi_{ss,i}$ to variations in I_{Bias,Q_i} is given by,

$$\frac{d\phi_{ss,i}}{dI_{Bias,Q,i}} = \frac{d\theta_i}{dI_{Bias,Q,i}} + \frac{N}{2} \cdot \frac{\sqrt{I_{Bias,I_i}/I_{Bias,Q_i}}}{(I_{Bias,I_i} + I_{Bias,Q_i})}. \quad (6.3.16)$$

The first term on the *R.H.S.* of (6.3.16) can be further expanded using the total derivative * to yield,

$$\frac{d\theta_i}{dI_{Bias,Q,i}} = \tan \theta_i \left[\frac{1 - (\Delta\omega_i/\omega_{0,i})}{\Delta\omega_i} \cdot \frac{d\omega_{0,i}}{dI_{Bias,Q,i}} - \frac{1}{I_{inj,i}} \cdot \frac{dI_{inj,i}}{dI_{Bias,Q,i}} \right]. \quad (6.3.17)$$

The derivative terms inside the brackets on the *R.H.S.* of (6.3.17) have been evaluated in sim-

Figure 6.7: A plot showing the sensitivity of the phase offset to changes in the phase interpolator quadrature current weight, $d\theta_i/dI_{Bias,Q_i}$, as a function of the injection bandwidth, $\Delta\omega_i$ for tank quality factors, $Q = 5, 7$ and 10 .

ulations as $d\omega_{0,i}/dI_{Bias,Q,i} \approx -1.14 \text{ MHz/mA}$ and $dI_{inj,i}/dI_{Bias,Q,i} \approx -0.77 \mu\text{A/mA}$ yielding a $d\theta_i/dI_{Bias,Q,i} < 5 \text{ m}^\circ/\text{mA}$ for more than 50% of the locking bandwidth as is plotted for three Q values in Figure 6.7. Comparing this resulting sensitivity to $1.3^\circ/\text{mA}$ which was obtained from the second term in (6.3.16), we have

*

$$\begin{aligned} \frac{d\theta_i}{dI_{Bias,Q,i}} &= \frac{d\theta_i}{d\omega_{0,i}} \cdot \frac{d\omega_{0,i}}{dI_{Bias,Q,i}} + \frac{d\theta_i}{dI_{inj,i}} \cdot \frac{dI_{inj,i}}{dI_{Bias,Q,i}} \\ &= \frac{d}{d\omega_{0,i}} \left[\sin^{-1} \left(\frac{2Q_i \Delta\omega/\omega_{0,i}}{|I_{inj,i}|/|I_{osc,i}|} \right) \right] \cdot \frac{d\omega_{0,i}}{dI_{Bias,Q,i}} + \frac{d}{dI_{inj,i}} \left[\sin^{-1} \left(\frac{2Q_i \Delta\omega/\omega_{0,i}}{|I_{inj,i}|/|I_{osc,i}|} \right) \right] \cdot \frac{dI_{inj,i}}{dI_{Bias,Q,i}}. \end{aligned}$$

$$\frac{d\phi_{ss,i}}{dI_{Bias,Q,i}} \approx \frac{N}{2} \cdot \frac{\sqrt{I_{Bias,I,i}/I_{Bias,Q,i}}}{(I_{Bias,I,i} + I_{Bias,Q,i})}. \quad (6.3.18)$$

The expression in (6.3.18) shows that the sensitivity of the output phase to variations in $I_{Bias,Q,i}$ is directly proportional to the frequency multiplication factor, N . This sets a practical limit on the $I_{Bias,Q,i}$ resolution steps needed for this calibration. It is also noted that a finer resolution (i.e. lower slope) can be obtained at the expense of a higher phase interpolator bias current (i.e. $I_{Bias,I,i} + I_{Bias,Q,i}$). Simulation results in Figure 6.8 show the sensitivity of the output phase to percentage variations in $I_{Bias,Q,i}$. Also shown in the same plot is the associated phase noise variations, ΔPN , which did not exceed ± 0.4 dB up to $\pm 30\%$ change of $I_{Bias,Q,i}$. The observed weak sensitivity of $d\omega_{0,i}/dI_{Bias,Q,i}$ and $dI_{inj,i}/dI_{Bias,Q,i}$ along with the relatively linear phase step and the minor phase noise degradation admitted phase interpolator $I_{Bias,I,Q}$ weights as good candidates for phase calibrations or fine tuning. Increasing the number of bits for the phase interpolator current steering DAC (to achieve finer phase steps) will naturally increase the available resolution of this fine tuning technique. As such, this fine tuning technique has been adopted during LO-element phase shift measurements as is discussed in Section 7.1.6. Simulation results are also contrasted to those observed in measurements in Section 7.1.9.

Figure 6.8: Simulated output phase sensitivity to $I_{Bias,Q,i}$ with lower-side injection and the associated phase noise performance variations.

6.4 Summary

Sources of phase shift mismatches among the outputs of the LO-elements in the proposed architecture have been discussed. Various means for phase offset fine-tuning and calibration have been introduced. The corresponding sensitivities of the fine-tuning means have been analyzed mathematically and the associated dependencies have been highlighted.

It has been shown how performing the phase fine tuning by varying the oscillator core current density can have a composite effect on the phase offset, θ_i due to the accompanying change in the oscillator output swing, the bias-dependant parasitics and the asymmetric varactor voltage dependance. It was also discussed how an appreciable amount of $\Delta I_{ss,i}$ may alter the oscillator intrinsic operating region and performance. Also worthy of note is the asymmetric sign change of $\partial\phi_{ss,i}/\partial I_{ss,i}$ about $\Delta\omega_i = 0$ which may complicate the prediction of the calibration behaviour and its automation.

The sensitivity of the phase shift to changes in the injection strength has been investigated revealing a strong dependency on the initial phase offset and an unsymmetrical tuning slope about $\Delta I_{ssinj,i} = 0$ due to the resulting narrower locking range in one direction. This implied the risk of operating closer to the edge of the locking range and phase noise performance impact.

Finally, the sensitivity to variations in the cartesian phase interpolator weights was investigated. Despite its direct proportionality to the frequency multiplication factor, it has the potential for an increased phase step resolution. Increasing the number of bits for the phase interpolator current steering DAC (to achieve finer phase steps) will naturally increase the available resolution of the fine tuning. Assuming minor phase shifter gain variations among the various phase shifts, the phase noise performance impact is the least in this case due to the minimal impact on the oscillator intrinsic operating point and its injection strength.

Chapter 7

Prototype Implementation and Measurement Results

A prototype chip has been fabricated in a standard 130-nm CMOS process to validate the main concepts in the proposed architecture. A single poly-silicon, eight metal layers with two top-level thick metals were available in the selected metallization option in this main stream process. Inductors and low-loss signal routing made extensive use of the top two thick metal layers at $4\text{-}\mu\text{m}$ thickness. Two LO-elements have been integrated in the prototype chip. Each LO-element consisted of a phase shifter followed by a high-order harmonic synthesis stage, a differential current injector, an oscillator and two buffer stages. In order to facilitate testing, the phase shifter in this prototype implementation included a two-stage RC-CR polyphase filter (Figure 4.5) followed by a single-stage phase interpolator (Figure 4.10(a)). This is to allow full and continuous control over the LO phase steering by setting off-chip DACs for the cartesian bias current weights (i.e. $I_{\text{BiasI},i}$ and $I_{\text{BiasQ},i}$). The high-order harmonic synthesis stage was ac-coupled to the phase shifter stage with its first-stage limiting amplifier and all current sink devices biasing generated on-chip. The rest of the limiting stages, the high-speed latch and the injection transconductor were self-biased through direct inter-stage DC-coupling. The injection transconductor was directly coupled onto the oscillator tank while receiving its DC bias current through the center tap of the differential oscillator tank inductor. The oscillator made use of thick oxide MOS varactors for tuning while thin oxide varactors were used in place of fixed capacitors as discussed in Section 4.3.3. The oscillator's tank is isolated from external loading through a resistively loaded source follower stage acting as a low impedance node followed by a differential FT-doubler with a transformer-based T-coil peaked load as a second buffer stage (Figure 4.26). RF signal long interconnects to I/O chip pads made use of 50Ω differential transmission line structures with side and ground shielding above the substrate and whose models and artwork were already provided in the kit.

Staggered pad arrangements were used at the north and south sides of the chip to facilitate debugging internal DC nodes in each LO-element as discussed shortly. The total area associated with one LO-element is 0.305 mm^2 . This includes the oscillator, the high-order harmonic synthesis blocks, phase shifters, signal routing and decoupling. Figure 7.1 shows a screen capture of the full layout view of the implemented chip along with a description of the probing pads located on its four sides. More detailed layout views of the individual blocks are provided in Appendix B. A picture of the $2 \text{ mm} \times 2 \text{ mm}$ fabricated prototype is also shown in Figure 7.2.

Figure 7.1: A layout view of the $2 \text{ mm} \times 2 \text{ mm}$ chip along with a description of the probing pads located on its four sides.

Figure 7.2: Micrograph of the $2\text{ mm} \times 2\text{ mm}$ fabricated prototype chip.

7.1 Measurement Setup and Results

The chip I/O and power pads were arranged such that the functionality of each LO-element can be fully tested by probing the chip from two sides at a 90° angle. That is, one LO-element would be tested using the West and South sides of the chip with its debugging pads located on the North side while the other would be tested using the North and East sides with its debugging pads on the South side. Measurement test cases were planned to be performed on the die using Multi-Contact Wedge (MCW) 8-pin Picoprobe^{®*} on the four sides of the chip, simultaneously. Figure 7.3 depicts the details of the frequency and time-domain measurement setup for the two LO-elements. The Agilent E8257C signal generator was used as a reference for the injection signals for the LO-elements. Ceramic based off-chip transformers[†] with 1.6-2.6 GHz bandwidth were used to realize differential injection signals from the signal generators. Despite the available differential outputs on the chip, only single-ended measurements were performed in both frequency and time domains due to the unavailability of discrete K -band transformers at the time of measurements. The two differential outputs of each of the two LO-elements were used to simultaneously allow frequency and

*By GGB Industries Inc.

[†]Mini Circuits TCN2-26 and its TB-287 evaluation board with a total insertion loss of $\leq 1\text{ dB}$, amplitude and phase imbalances of 0.6 - 0.7 dB and 1.1 - 6° between 2-2.41 GHz, respectively.

Figure 7.3: The frequency and time-domain measurement setup for the two LO-elements which were implemented on the prototype chip. Except for the cartesian phase shifter bias current weights, $I_{Bias,I,Q}$, DC biasing details have been omitted for clarity.

time-domain measurements. The spectra of the two LO-elements were monitored by HP8564E and HP8593E spectrum analyzers while the time domain signals and phase relationships were monitored by a dual-channel 50-GHz HP83480A sampling scope.

7.1.1 Free Running Oscillator and Tuning Range

In this test case, the oscillator was DC biased as per the simulations in Section 4.4 but free-running oscillations could only be obtained by applying a voltage to overwrite the fixed thin oxide nMOS varactor biasing through a dedicated pad. Recall from Section 4.3.3 that thin oxide varactors were used in place of fixed capacitors by maintaining a constant source/drain bias on chip. Upon debugging the DC bias level at the thin oxide source-drain node through on chip probing to measure the varactor tuning port potential, it was found setting at 1.12 Volts, 88 mV below the chip V_{DD} . This yielded a $V_{gd,ncap} > 0$ leading to $Q_{var,ncap}$ levels below 5*. Also recall that, according to Figure 4.24, oscillations were still possible at 18 GHz with the thin oxide varactor models biased at $V_{gd,ncap} \leq +0.2$ V in simulations. However, not until $V_{ctrl,ncap}$ had been changed through a chip pad that was available for debugging on the north side such that $V_{gd,ncap}$ became well below -0.5 V[†] that free running oscillations were observed at the targeted 18 GHz band as is shown in Figures 7.4 and 7.5. This observed biasing discrepancy between simulations and measurements highlighted model inaccuracies in capturing the thin oxide varactor losses leading to larger predicted Q than actually obtained in measurements and hence the need to modify the on chip generated $V_{ctrl,ncap}$ to reach oscillations.

Simulations indicate single ended power level of -15.9 dBm into a 50 Ω . Due to the unavailability of on-chip de-embedding structures or calibration substrates for the 8-pin MCW differential RF probes at the time of measurements, only cable and DC-blocking capacitor losses could be de-embedded. With a combined attenuation of about 2 dB at 18 GHz, a de-embedded output power level of about -18 dBm has been predicted. This is in good agreement with the measured output power of -17.67 dBm in Figure 7.4 at one of the RF ports. A -2 dB difference has been observed when swapping the RF ports as recorded in Figure 7.5. This is believed to be due to what had been initially observed in simulations as a slight asymmetry in the VDD biasing path of the FT doubler buffer and for which the initial resulting output power level mismatch did not exceed -0.2 dB. This effect seems to have been exacerbated in the prototype chip leading to this difference seen in measurements. It is also noted that this latter measurement has been taken

---

*This Q level has been extracted by interpolating between two foundry provided model correlation curves for two ncap varactors sizes at 18 GHz.

[†]Foundry provided model correlation curves are not available below -0.5 V.

Figure 7.4: Example of the measured free running oscillations spectra in 18 GHz.

Figure 7.5: Example of the measured free running oscillations spectra in 18 GHz.

while the second RF port was being directly terminated at the RF connector port of the MCW probe with a $50\ \Omega$ “dummy” load (i.e. no matched T.L. was connected to the second RF port).

The tuning range of the oscillator is shown in Figure 7.6 as a function of the the thick oxide varactor control voltage, $V_{\text{ctrl,DGncap}}$, for four thin oxide varactor settings. It is noted that the measured tuning range could not be directly compared to that obtained in simulations due to the discussed discrepancy between the thin-oxide varactor model in simulations in Figure 4.24 and its measured performance. This is especially seen in having to maintain $V_{\text{ctrl,ncap}} \geq 1.99\ \text{V}$ and $V_{\text{ctrl,DGncap}} \geq 2.1\ \text{V}$ in order to reach a sufficient overall tank Q and satisfy the oscillation startup conditions. Recall from Figure 4.24 that oscillation startup conditions were satisfied for $V_{\text{ctrl,ncap}} \geq 1\ \text{V}$ and for the full range of $0\ \text{V} \leq V_{\text{ctrl,DGncap}} \leq 1.5\ \text{V}$. It is also noted from Figure 7.6 that the varactors’ biasing regions for which oscillations were obtained lie in the negative region of the corresponding V_{gd} where the variations in capacitance are limited and hence the slope of the tuning range curves. The author acknowledges the impracticality of the measured tuning range ($\approx 2.2\%$) and that it is reported here for completeness and to demonstrate that each of the two LO-elements could still be fully tested individually at the targeted frequency (i.e. 18 GHz) with a sufficient tunability to allow enough range for the injection locking test cases.

Figure 7.6: Measured tuning range as a function of the the thick oxide varactor control voltage, $V_{\text{ctrl,DGncap}}$ for four thin oxide varactor settings.

Lately, because of the way the prototype chip floor planning has been arranged and due to

the need to overwrite $V_{\text{ctrl,ncap}}$ for each LO-element through a debugging pad whose north side location would prevent the other LO-element from being tested concurrently (at this frequency), the plan for testing the functionality of the prototype has been as follows:

- (a) The functionality of a complete LO-element has been initially tested individually at the targeted 18 GHz band.
- (b) In order to test the functionality of the two LO-elements simultaneously, each element must be made fully testable using only two sides of the chip. To make this possible, oscillations must be enabled for each element without having to overwrite its $V_{\text{ctrl,ncap}}$ through a debugging pad which occupies a third side of the chip. By disconnecting the thin-oxide varactors from the tank, their degrading effect on the overall tank Q is removed and oscillations are enabled without the need to overwrite $V_{\text{ctrl,ncap}}$ for each LO-element. This way, each LO-element can be tested by probing two sides of the chip for a total of four sides for the two elements. More details on these test cases are provided in Section 7.2.

7.1.2 Measurements of the High-order Harmonic Synthesis Stage

In this test case, the phase shifter of one LO-element has been biased with equal $g_{mI,Q}$ weights (i.e. $I_{\text{Bias},I_{i_j}} = I_{\text{Bias},Q_{i_j}}$) while a -15 dBm, 2.03 GHz differential reference signal is fed at the input of the RC-CR polyphase filter as is shown in the test bench in Figure 7.3. The gate bias of the oscillator core current sink transistor has been selectively switched *ON* and *OFF* in order to examine the effect of the injection-locked oscillator core on the amplitude or power levels of the synthesized harmonics. Figure 7.7 shows the output spectra of the high-order harmonic synthesis stage with the oscillator negative g_m core switched *OFF*. Evident from the magnitudes of the odd harmonics, especially that of the ninth harmonic at 18.27 GHz, is the effective high-order harmonic generation even in the absence of the tuned active enhancement by the oscillator. This clearly demonstrates the effective role of the limiting stages along with the high-speed latch in enriching the harmonic content of the injected single tone at the ninth subharmonic (i.e. 2.03 GHz). With a Q of 7, an equivalent single-ended parallel tank resistance is calculated as $Q\omega L/2 \approx 70 \Omega$. Assuming the same injection current of 257 μA and the losses in the buffers as in simulations, a single-ended power level of -37.8 dBm is estimated versus -36.3 dBm de-embedded from measurements (27.3 dBmV versus 25 dBmV at the tank output, respectively). It is also noted that the relative magnitudes of the synthesized harmonics as they appear in Figure 7.7 are due to the filtering effect of the uncompensated oscillator tank bandpass transfer characteristics and that of the two buffer stages succeeding it. Upon switching the oscillator core current sink

Figure 7.7: Measured spectra of the multiplier output *without* the oscillator enhancement effect using one of the FT doublers buffer outputs.

device *ON*, the 9th harmonic power level at 18.27 GHz was observed to have been enhanced by 21.8 dB reaching -16.5 dBm as is illustrated in Figure 7.8. With a -2 dB losses in cables and DC-blocking capacitors at 18 GHz, this output power level aligns well with a predicted -14.51 dBm in simulations.

The level of the even harmonics could have been significantly reduced if differential measurements were possible. As has been mentioned earlier, despite the available differential outputs of each LO-element, only single-ended measurements were possible due to the unavailability of discrete *K*-band transformers at the time of testing.

It is noted that one of the plots in Figure 7.8 was taken at one of the differential RF ports while the other is terminated at the time-domain sampling scope port through a matched pair of transmission lines. This is contrasted to the other plot where; i) the connections to the RF ports were swapped and ii) the second RF port was being directly terminated at the RF connector port of the MCW probe with a $50\ \Omega$ “dummy” load after a DC blocking capacitor (i.e. no matched T.L. was connected to the second RF port). The FT doubler load mismatch between the two measurement cases explains the difference in the level of the harmonics.

Although largely depend on the RF and IF frequency planning within the band of interest, the image frequency and mixing spurs issues are important to discuss in light of the resulting LO spectra. Considering the fact that switching RF mixers multiply the RF input signal of an

Figure 7.8: Measured spectra of the LO-element output with the oscillator enhancement in effect as obtained separately using the individual outputs of the FT doubler buffer.

array element at $\omega_{RF_{in}}$ by a hard-limited or a square-wave LO, it is viewed as a multiplication by the odd harmonics of the LO signal [95]. With the proposed multiplication based sub-harmonic phase locking, besides the high-order LO harmonics, the sub-harmonics of the resulting LO signal must also be considered as potential sources of mixing spurs. Assuming a dual-IF heterodyne receiver for the sake of this discussion, the first RF mixer produces frequency components at $\omega_{in} \pm m\omega_{LO1}/N$ and the second mixer produces components at $\omega_{in} \pm (m\omega_{LO1} \pm n\omega_{LO2})/N$ where m , n and N are integers. While m and n refer to various LO harmonic numbers, the value of N will depend on whether one considers the mixing spurs due to high-order LO harmonics or those due to its sub-harmonics (i.e. the harmonics of the up multiplied reference). In the former case, $N = 1$ while $N = 9^*$ in the latter. The desired information signal is down-converted to $\omega_{RF_{in}} - \omega_{LO1} - \omega_{LO2}$. Potential interferers, at ω_j , as well as their images, may also be down-converted to the second IF corrupting the desired signal when

$$\omega_j \pm (m\omega_{LO1} \pm n\omega_{LO2})/N = \omega_{RF_{in}} - \omega_{LO1} - \omega_{LO2}. \quad (7.1.1)$$

With the normal case of $N = 1$ being covered in RF texts [95] [110], the focus here is on the $N = 9$ case where the mixing spurs are due to the harmonics of the multiplied reference (i.e. the LO sub-harmonics). Assuming the even sub-harmonics of the LO are completely eliminated differentially, m and n may only assume odd integers. Consider the frequency planning such that $\omega_{RF_{in}}/2\pi = 24$ GHz, $\omega_{LO1}/2\pi = 18$ GHz and $\omega_{LO2}/2\pi = 6$ GHz as an example for the sake of

---

*Recall that the proposed architecture makes use of an up-multiplied ninth sub-harmonic for phase locking through injection.

this discussion. Since the higher the order of the mixing operation that produces the spurious tones, the lower the spur level, only $m = n = 1, 3, 5, 7$ values are considered. Upon solving (7.1.1) for the frequencies of the potential interferers, and their images, which may corrupt the desired signal at IF, the closest $\omega_j/2\pi$ were at 12, 16, 20 and 28 GHz that is -12, -8, -4 and +4 GHz away from the RF input frequency, respectively. The resulting frequencies are shown in Table 7.1. With less than or equal an octave away from the RF signal at $\omega_{RF_{in}}$ and noting that the

Table 7.1: Frequencies of Potential Interferers

LO Reference	ω_{IF_1}	Harmonic Number				
18 GHz/9	6 GHz	3 rd	5 th	7 th	9 th	11 th
Interferer Frequency (GHz)		12	4,16	8,20	12	16,28

mixing tones due to the LO sub-harmonics are initially at -30 dB from the desired LO in Figure 7.8, the interfering tones at these frequencies can be dealt with at the pre-select and image filters. More importantly, in addition to the attenuation of the pre-select and image reject filtering which the interfering tones experience, phased-array architectures provide extra degrees of freedom in mitigating in-band interferers. Taking advantage of the complex weights (i.e. magnitude and phase) available for each array element, a null can be spatially placed in the direction of the interferer's angle of arrival while the beam peak is in the direction of the desired signal [20]. Moreover, if both the desired signal and the interfering tone have the same direction of arrival, employing spectro-spatial diversity techniques further allows the desired signal frequency to be spatially steered off the broadside significantly attenuating the interfering tone [111–113]*.

In the absence of interfering tones, the amount of the image thermal noise which is down-converted to the first IF due to the LO sub-harmonics and the associated image tones at $\omega_j/2\pi = 12, 16, 20$ and 28 GHz will be a strong function of the order of the image reject filters employed and their attenuation at these image bands prior to mixing [95].

7.1.3 Injection Locking Range Measurements

The injection locking range of one LO-element has been measured twice at 18 GHz; first with a ninth subharmonic reference and second with an eleventh subharmonic reference. In the case of a -1.5 dBm ninth subharmonic reference, Figure 7.9 shows a quasi-lock case where an injection signal at $\Delta\omega_{inj}/2\pi = -160$ MHz has been used. It is also seen from Figure 7.9 that the resulting beat frequency is $\omega_b/2\pi \approx 27$ MHz predicting a single-sided locking range of 157 MHz. Although

---

*The suppression of the interferer in this case is a strong function of the resolution of the spectral filtering prior to the spatial filtering.

Figure 7.9: A quasi-lock case as obtained in measurements using $\Delta\omega_{inj}/2\pi = -160$ MHz to lock one LO-element with its oscillator free running at $\omega_0/2\pi = 18.151$ GHz using a ninth subharmonic reference. $\omega_b/2\pi \approx 27$ MHz is obtained evidencing a single-sided locking range of approximately 157 MHz at an injection power level of $P_{inj} = -1.5$ dBm.

the staggered tuning of the polyphase filter along with the high-order harmonic synthesis stage have been designed to allow about -30 dBv of the ninth harmonic at the latch output, an appreciable eleventh harmonic content is still available at its output as has been shown in Figure 4.16. Recalling from Section 4.3.1 that the lower edge of the polyphase filter bandwidth is at 1.77 GHz, an eleventh subharmonic input at $\omega_{inj}/2\pi \geq 1.657$ GHz could still be used to lock the oscillator over an appreciable bandwidth. Figure 7.10 shows a quasi-lock case where an injection signal at $\Delta\omega_{inj}/2\pi = -137$ MHz has been used to lock one LO-element at $\omega_0/2\pi = 18.227$ GHz and a resulting beat frequency of $\omega_b/2\pi \approx 30$ MHz correctly predicting a single-sided locking range of approximately 133 MHz.

The effect of the injection power, P_{inj} , on the locking range has also been investigated in each of the two test cases above (i.e. the ninth and the eleventh subharmonic references). In each test case, the input power of the reference signal was progressively reduced while monitoring the lock range until a case of no lock was reached. The locking ranges for the ninth and the eleventh subharmonic reference cases have been plotted versus the input power level and are shown in Figure 7.11. It is noted that the input RF power levels have been de-embedded after about -5.5 dB of loss in the RF balun, two Bias-T's and the input network cables.

Figure 7.10: A quasi-lock case as obtained in measurements using $\Delta\omega_{inj}/2\pi = -137$ MHz to lock one LO-element at $\omega_0/2\pi = 18.227$ GHz using an eleventh subharmonic reference. $\omega_b/2\pi \approx 30$ MHz is obtained evidencing a single-sided locking range of approximately 133 MHz at an injection power level of $P_{inj} = -1.5$ dBm.

Figure 7.11: Measured locking ranges for the ninth and the eleventh subharmonic references used versus the input power level.

Note the relative independence of the locking bandwidth to the input power level above -10.5 dBm into the phase shifter (i.e. RC-CR polyphase filter followed by the phase interpolator). In the absence of the losses associated with the phase shifter block*, this would translate into an estimated equivalent input power level of -13.5 dBm into the multiplier (i.e. high-order harmonic synthesis block followed by the oscillator).

7.1.4 Testing a Variation on the Proposed Frequency Multiplication Technique

A number of frequency multiplication schemes have been qualitatively compared in Sections 3.3 and 3.4. Having verified the proposed technique at hand, namely, a high-order harmonic synthesis stage followed by an injection locked oscillator, a variation on this technique has also been investigated in this measurement test case. If the DC biasing of the oscillator core tail current device is modified such that it sets at the verge of oscillations, the oscillator acts as a Q-enhanced filter. That is, the multiplication technique being investigated in this case relies on a high-order harmonic synthesis stage followed by a Q-enhanced filter instead of an oscillator. Figure 7.12 shows the resulting output spectra when carrying out this experiment at the same injection frequency (i.e. 18.27 GHz/9). It is seen that the magnitude of the enhanced ninth harmonic at 18.27 GHz has degraded by about 4 dB relative to the case of an injection locked oscillator. Comparing the magnitudes of the carrier with and without the filter enhancement in Figures 7.7 and 7.12, respectively, the Q-enhanced filter has resulted in a 15.5 dB improvement. The frequency of the injection signal has been varied to measure the -3 dB bandwidth. This test resulted in 324 MHz, a 45 % larger bandwidth than the two-sided injection locking bandwidth. Given that the measured power in the carrier is in good agreement with simulations (after de-embedding cables and component losses) and that the injection locking bandwidth corresponds well to that obtained in simulations, a conversion gain/loss can thus be estimated. With a -22.83 dBm carrier power into 50 Ω in Figure 7.12, a 54 mV ninth sub-harmonic signal at the input of the harmonic synthesis stage and -5 dB of second stage buffer loss, a conversion loss of 0.48 dB has been estimated in voltage terms. Additionally, with a -30 dBV of ninth harmonic prior to the injection stage, a harmonic multiplication/conversion loss is also estimated as 4.6 dB in voltage terms. With a similar phase noise performance to that of the injection locked oscillator, the resulting magnitude of the carrier in this multiplication technique varies with the magnitude of the synthesized harmonic for which the Q-enhanced filter acts as a tuned amplifier with a high

---

*According to simulations, a loss of -4.5 dB in the RC-CR polyphase filter combined with a gain of 1.5 dB in the PI, a combined loss of -3 dB is obtained in Voltage units.

Q load. As discussed in Section 3.4, this is contrasted to the proposed technique where the magnitude of the carrier is, to a first order, independent of the magnitude of the synthesized harmonic prior to injection provided that the latter is sufficient to injection lock the oscillator.

Figure 7.12: Measured spectra of the multiplier output *without* the oscillator enhancement effect using one of the FT doublers buffer outputs.

7.1.5 Phase Noise and Integrated Jitter Measurements

Phase noise measurements have been performed using the HP8564E spectrum analyzer. As previously noted earlier, only single-ended measurements were possible due to the unavailability of discrete K -band transformers at the time of this test case. As such, all measurements have been carried out at a lower output signal power level than available*.

Figure 7.13(a) shows the phase noise performance of an LO-element when it was injection locked to an up multiplied ninth subharmonic reference at 2 GHz (Agilent E8257C). The recorded phase noise is -102 dBc/Hz and -105 dBc/Hz at 10 KHz and 100 KHz offsets from a 18 GHz carrier, respectively. Also shown in Figure 7.13(b) is the phase noise profile of the reference signal generator at 2 GHz when it is directly connected to the spectrum analyzer. With a phase noise performance of the injected ninth subharmonic signal measuring -120.33 dBc/Hz at 100 KHz offset, this is 3.75 dB better than the predicted $20 \log 9 \approx 19.1$ dB phase noise degradation as per the

---

*A transformer combining the two differential RF signals available at the output of each LO-element would allow an additional 3 dB less its insertion loss in power terms.

established theory in the case of a frequency multiplication process [97]. The actual phase noise profile specification of the signal generator is -124 dBc/Hz at a 100 KHz offset [114] but is believed to have been recorded higher due to the close-in sensitivity of the phase noise measurement system used.

Figure 7.13: (a) Measured phase noise performance of an LO-element at 18 GHz when it was injection locked to an up multiplied ninth subharmonic reference at 2 GHz . The recorded phase noise is -102 dBc/Hz and -105 dBc/Hz at 10 KHz and 100 KHz offsets from a 18 GHz carrier, respectively. (b) Measured phase noise profile of the reference signal generator at 2 GHz .

Figure 7.14(a) also shows a comparison between the output phase noise of an LO-element when its oscillator was initially left freely running at 18.31 GHz and when it was injection locked to the up multiplied ninth subharmonic reference using another signal generator (Agilent E4432B). It is noted that the oscillator circuit was *not* isolated from the rest of the circuit blocks preceding it when measuring its free running phase noise performance. Except for the phase interpolation devices (i.e. M_{I-4} and M_{Q-4} in Figure 4.10(a)), which could selectively be turned off through DC external biasing, all phase noise measurements have been carried out with the rest of the LO-element circuit blocks being connected and biased. That is, the phase noise performance shown in Figures 7.14(a) and 7.13(a) includes the effects of $1/f$ and thermal noise generation and propagation through the LO-element circuit blocks and its contribution to the overall phase noise of the free running oscillator as discussed in Section 4.3.2.

A locked phase noise performance of -115 dBc/Hz and -105 dBc/Hz at 1 MHz and 100 KHz

is seen in Figure 7.14(a) evidencing an improvement of 30 dB and 37 dB, respectively. With a phase noise performance of the injected ninth subharmonic (i.e. $18.31 \text{ GHz}/9$) signal measured at -134.8 dBc/Hz , this is 0.7 dB away from the predicted $20 \log 9 \approx 19.1 \text{ dB}$ phase noise degradation [97]. The measured phase noise profile of the signal generator used in this test case has also been recorded in Figure 7.14(b) for the reader's reference.

In a LO-path phase-shifting architecture, the phase noise of the LO signal translates to jitter affecting the element to element progressive phase shift and thus the beam steering direction. In order to estimate this degradation, the integrated RMS jitter has been calculated by the spectrum analyzer with its maximum possible integration limits between 100 Hz and 100 MHz and it is 0.2147° as is shown in Figure 7.15. This is compared to 0.296° which has been obtained in simulations using identical integration limits. In order to capture the effect of the fundamental side band on the overall beam jitter, the upper integration limit has been extended in simulation to 17 GHz leading to a calculated RMS jitter of 2.256° . With each element phase shift jittering by this RMS amount, the resulting effect on beam steering is comparable to that illustrated in Figures 7.18 and 7.19 where the errors in the progressive phase shift were on the same order after calibration.

Figure 7.14: (a) A comparison between the output phase noise of an LO-element with its oscillator initially left freely running at 18.31 GHz and when it was injection locked using Agilent (E4432B) signal generator. (b) Phase noise measurement of the injection signal source at $18.31 \text{ GHz}/9 = 2.035 \text{ GHz}$.

```
EXECUTE will integrate the phase noise
of trace A to give RMS Phase Noise
in radians and in degrees.
```

```
This may take a few minutes,
depending on the number of points.
```

```
Lower integration limit:    100 Hz
Upper integration limit:    10.0 MHz
All points are integrated.
```

```
RMS PHASE NOISE =    .0037 RADIANS
                  .2147 DEGREES
```

Figure 7.15: Measurement of the integrated RMS phase jitter as calculated by the spectrum analyzer with its maximum integration limits between 100 Hz and 100 MHz.

Evident from these test cases is close to minimal phase noise degradation despite the $1/f$ and thermal noise generation and propagation through the LO-element circuit blocks (i.e. RC-CR polyphase filter, phase interpolators, limiters, high-speed latch and current injector blocks). This result signifies the feasibility of the proposed multiplication and injection locking technique as a practical approach towards achieving superior phase noise performance at K-band with an independent phase steering capability.

7.1.6 Phase Shift Measurements of One LO-element and the Associated Beam Steering Results

Phase shift measurements have been performed for one LO-element relative to an external 18 GHz synchronized reference. The external reference was used due to the need to overwrite $V_{ctrl,ncap}$ for each LO-element through a debugging pad whose north side location prevented the other LO-element from being tested simultaneously (at this frequency) as previously discussed. As such, the 110 MHz reference of the Agilent signal generator which acted as the source for the injection signal in Figure 7.3 has been used to synchronize an external 18 GHz source (Agilent 8257C). The spectra of the two signals (the output of one LO-element and that of the 18 GHz source) were monitored by HP8564E and HP8593E spectrum analyzers while the two time-domain signals and their relative phase relationships were monitored by a dual-channel 50-GHz HP54752A sampling scope.

In each phase-shift measurement, the errors of the phase shifting operation of one LO-element were determined as follows. The cartesian $g_{m,I,Q}$ weights were set to their balanced case by

setting $I_{Bias,I_1} = I_{Bias,Q_1}$. The initial phase difference between the external source and the LO-element output was recorded. The cartesian $g_{m,I,Q}$ weights are then set to phase shift the LO-element output phase to a desired angle, ψ , by setting I_{Bias,I_1} and I_{Bias,Q_1} such that $\tan(\psi/N) = g_{m,Q}/g_{m,I} = \sqrt{I_{Bias,Q_1}/I_{Bias,I_1}}$, where $N = 9^*$. The resulting delta phase shift between the external source and the LO-element output was then recorded. This process has been repeated for $0 \leq \psi \leq 2\pi$ with steps of 22.5° . All the required g_m weights and their corresponding $I_{Bias,I}$ and $I_{Bias,Q}$ calculations for $0^\circ \leq \psi/N \leq 40^\circ$ were fully automated and set by a MATLAB program which was developed to control the programmable Keithley® power supplies as illustrated in Figure 7.3.

A snap shot of a number of waveforms are shown in Figure 7.16 as individually obtained from the time-domain measurements. Each waveform corresponds to a locked oscillator output using a separate phase-shifter setting. The amplitude variations in Figure 7.16 are believed to be due to the sensitivity of the measurements to the planarization of the simultaneously landed probes on the four sides of the die. Figure 7.17 shows the obtained versus desired phase shifts and the associated maximum phase errors before and after calibration for one LO-element at 18.27 GHz. The maximum phase shift errors were 8.5° and 2.35° before and after calibration, respectively. Calibrations have been performed using $I_{Bias,I}$ and $I_{Bias,Q}$ for this technique has demonstrated the least impact on the phase noise performance as is discussed shortly.

It is noted that the recorded phase shifts in the procedure described above is $\varphi = \Delta\phi_i \equiv \Delta\psi_i + \Delta\theta_i$. In words, the measured phase shift at the output of an LO-element is the multiplied up phase shift $\Delta\psi_i$ injected into the oscillator and added to the phase offset $\Delta\theta$. Comparing the obtained phase shifts from measurements in Figure 7.17 to those from simulations in Figure 4.32, the trend of negative phase errors is evident between 67.5° and 225° . The difference in phase errors within this region can be explained in light of the locked oscillator phase offset expression as previously introduced in Section 6.2 and is given by,

$$\theta_i|_{|I_{inj,i}| \ll |I_{osc,i}|} \approx \sin^{-1} \left[\left(\frac{\omega_{0,i} - \omega_i}{\omega_{0,i}} \right) \left(\frac{2Q_i}{|I_{inj,i}|/|I_{osc,i}|} \right) \right]. \quad (7.1.2)$$

Differentiating w.r.t. the tank Q, one obtains

$$\frac{d\theta_i}{dQ_{i,tank}} = \frac{(\Delta\omega_i/\omega_{0,i})}{\sqrt{(I_{inj,i}/I_{osc,i})^2 - 4Q_{i,osc}^2(\Delta\omega_i/\omega_{0,i})^2}}. \quad (7.1.3)$$

It is seen in (7.1.2) and (7.1.3) that the phase offset is directly proportional to $\Delta\omega_{inj,i} \equiv \omega_{0,i} - \omega_i$ with its sign determined by whether the frequency of the injected signal is above ($\omega_{0,i} < \omega_i$) or

---

*This approximation is based on the assumption of a biasing level at a current density of $J \leq 0.15 \text{ mA}/\mu\text{m}$ [88], as discussed in Section 4.3.1

Figure 7.16: Superimposed time-domain waveforms individually obtained through time-domain measurements. Each waveform corresponds to a locked oscillator output to a separate phase-shifter state as outlined in Section 4.3.1.

below ($\omega_{0,i} > \omega_i$) the center frequency of the free running oscillator. With $\Delta\omega_{inj} = -14.2 \text{ MHz}^*$ (i.e. higher side injection) used in measurements, a Q of 7 and an injection strength of 9%, $\theta_1 \approx -3.4^\circ$. This is in good agreement with the difference in the phase shift errors between measurements and simulations in the 67.5° - 225° region where a similar negative error trend was observed[†]. Additionally, the fact that a single stage phase interpolator has been implemented in the prototype chip while keeping $I_{Bias,I_i} + I_{Bias,Q_i} = \text{constant}$ made I_{Bias,I_i} and I_{Bias,Q_i} differ by increasingly larger amounts above this region. This not only led to reduced linearity in the $g_{mI,Q}$ weights but also impacted the phase shifter gain. While the reduced linearity of the $g_{mI,Q}$ weights leads to larger phase errors, pronounced phase shifter gain variations alters the injection ratio, $I_{inj,i}/I_{osc,i}$, which according to (7.1.2) yields a nonzero $\Delta\theta_i$ and in turn adds to the measured phase shift errors.

It is important to note that despite the negative trend in phase shift errors observed *without* calibration, LO-element to element delta phase shifts yielded minor phase steering errors compared to the ideal case with a peak-to-null ratio of better than 30 dB. This is illustrated

*Versus $\Delta\omega_{inj} = -6 \text{ KHz}$ used in simulations.

[†]The Q_{tank} used here has been extracted from the lock range simulations (and calculations) as was discussed in details in Section 4.5. Carrying out the same calculation with $Q_{tank} = 6.5$ yields $\theta_i \approx -3^\circ$ which is in a better agreement with the difference between measurements and simulations in the same region.

Figure 7.17: Obtained versus desired phase shifts and the associated phase errors before and after calibration as measured for one LO-element at 18.27 GHz (top) and those from simulations (bottom). The maximum phase shift errors as obtained from measurements are 8.5° and 2.35° before and after calibration, respectively.

in Figures 7.18 and 7.19 where normalized array patterns have been plotted for several sequences of progressive phase shifts for four- and eight-element arrays, respectively. That is, $(\phi_i - \phi_{i+1}) = \dots = (\phi_{n-1} - \phi_n) = \varphi$. Only those sequences yielding the worst case progressive phase shifts and hence array patterns are shown.

Figure 7.18: Phase steering results for 4-element arrays based on the phase shifts obtained from measurements with and without calibration and how they compare to the ideal case. Phase shift sequences used are (a) $[0^\circ, -22.5^\circ, -45^\circ, \dots]$, (b) $[0^\circ, 45^\circ, 90^\circ, \dots]$, (c) $[0^\circ, -90^\circ, -180^\circ, \dots]$ and (d) $[0^\circ, 90^\circ, 180^\circ, \dots]$.

7.1.7 The Effect of Phase Steering on the Phase Noise Performance

The challenges associated with LO phase steering by solely tuning the center frequency of the oscillator and its negative impact on the obtained phase noise performance [6–8, 115] were previously highlighted. In order to emphasize the effectiveness of the proposed phase shifting technique

Figure 7.19: Phase steering results for 8-element arrays based on the phase shifts obtained from measurements with and without calibration and how they compare to the ideal case. Phase shift sequences used are (a) $[0^\circ, -45^\circ, -90^\circ, \dots]$, (b) $[0^\circ, 45^\circ, 90^\circ, \dots]$, (c) $[0^\circ, -135^\circ, -270^\circ, \dots]$ and (d) $[0^\circ, 135^\circ, 270^\circ, \dots]$.

and differentiate it from other LO phase steering techniques, the impact of LO phase steering on the obtained phase noise was recorded.

Figure 7.20: Measurement of the effect of phase steering one of the oscillator outputs on its phase noise performance while injection-locked to the 9th harmonic of the distributed reference.

Figure 7.20 demonstrates the measured phase noise performance at 1 MHz offset from a 18.27 GHz carrier for all phase shifts where a maximum phase noise variation of ± 1 dB is observed at an input power level of -14 dBm. A sample of two superimposed phase noise measurements at 0° and 337.5° (i.e. extreme cases) is also shown in Figure 7.21. Compared to ± 0.4 dB in simulations, this increased variation is believed to be due to the associated change of the phase shifter gain and biasing condition (i.e. I_{Bias,Q_i} and I_{Bias,I_i} and the associated $g_{mI,Q}$ weights) among different phase shifts. The fact that, with this proposed technique, the oscillator needs not to operate near the edge of its locking bandwidth explains the observed relative independence of the obtained phase shift from the phase noise performance. Additionally, it has been observed in measurements that these phase noise variations could be reduced to ± 0.5 dB when higher injection power was used at the expense of increased phase shift errors. This emphasized an important trade-off between the accuracy of the phase shifter and the degree of independence of the phase noise performance of this architecture. The linearity of the phase shifter with respect to the injection power level made available at its input plays an important role in this trade-off. That is, improving the phase shifter linearity allows sufficient subharmonic injection signal power to be

introduced at its input without compromising its phase shift accuracy. According to Figure 7.11, an input power level of -10.5 dBm at the RC-CR input yielded a one-sided locking bandwidth of 122.4 MHz. This relatively large locking bandwidth reduces the sensitivity of the phase noise performance of the locked oscillator to gain and biasing variations of the phase shifter*.

Figure 7.21: A comparison between two measured phase noise profiles for a locked LO-Element at 0° and 337.5° .

A distinction must be made clear between the reduced sensitivity of the locking bandwidth to the distributed reference signal level and that of the accuracy of the phase shifter to it. The former type of de-sensitization has been achieved successfully through the limiting approach that was adopted in the high-order harmonic synthesis block[†], as has been illustrated in Figure 7.11 beyond -10.5 dBm. The latter type of de-sensitization, however, is what needs to be improved upon further by linearizing the phase shifter interpolation stage such that a power level of -10 dBm or higher may be introduced at its input without compromising its phase shift accuracy. This way, the observed trade-off between the independence of the phase noise performance and the accuracy of the phase shift can be broken to a greater extent.

*The wider the injection locking bandwidth for a given oscillator circuit, the slower the degradation of its locked-state phase noise performance as the injection locking frequency ω_{inj} departs from its free running center frequency ω_0 i.e., $\omega_{inj} \neq \omega_0/N$, where $N = 1, 2, \dots$ etc.

[†]by providing sufficient injection signal level to the oscillator at its fundamental and securing a wide locking range (see Figure 7.11).

7.1.8 Sensitivity of Phase Shifts to Oscillator Core Tail Current

In Section 6.3.1, the sensitivity of the output phase shift to changes in the tail current of the oscillator core has been analyzed in details. It has been discussed how a considerable increase or decrease in $I_{ss,i}$ may lead to altering the oscillator intrinsic operating regime (i.e. current versus voltage limited) and eventually deviating from the originally intended performance. Additionally, we have also observed the asymmetric sign change of $\partial\phi_{ss,i}/\partial I_{ss,i}$ about $\Delta\omega_i = 0$ which made it practically challenging to predict the trend of the calibration behaviour and automate it without an apriori accurate measurement of $\partial\omega_{0,i}/\partial I_{ss,i}$. As such, this fine tuning technique has been evaluated in this measurement test case only for completeness. Figure 7.22 shows measured versus simulated Δ phase-steps as a function of percentage $\Delta I_{ss,i}$ changes and the accompanying variations in the phase noise measurements. It is seen that the slope of $\Delta\phi_{ss,i}/\Delta I_{ss,i}$ is $-4.3^\circ/\text{mA}$ versus $-1.7^\circ/\text{mA}$ which was obtained in simulations. Recall $\partial\phi_{ss,i}/\partial I_{ss,i}$ was derived in Section 6.3.2 as,

$$\frac{\partial\phi_{ss,i}}{\partial I_{ss,i}} \approx \tan\theta_i \left[\frac{1 - (\Delta\omega_i/\omega_{0,i})}{\Delta\omega_i} \cdot \frac{\partial\omega_{0,i}}{\partial I_{ss,i}} + \frac{1}{Z_{s,i} + Z_{in,i}} \cdot \frac{\partial Z_{in,i}}{\partial I_{ss,i}} \right]. \quad (7.1.4)$$

Upon performing a parametric analysis on (7.1.4), it was found that the increase in the slope can

Figure 7.22: Measured versus simulated Δ phase-steps as a function of percentage $\Delta I_{ss,i}$ changes and the accompanying variations in the phase noise measurements.

be largely attributed to the last term inside the brackets. That is, the $(\partial Z_{in,i}/\partial I_{ss,i})(Z_{s,i} + Z_{in,i})^{-1}$

term is believed to have increased to about $70\Omega/\text{mA}$ when $V_{\text{ctrl,ncap}}$ was modified to reach a sufficient overall tank Q and satisfy the oscillation startup conditions as discussed in Section 7.1.1.

7.1.9 Sensitivity of Phase Shifts to Phase Interpolator Cartesian Weights

In this test case, the sensitivity of the phase shift to changes in phase interpolator cartesian weights, (i.e. $I_{\text{BiasI},i}$ and $I_{\text{BiasQ},i}$) has been evaluated through measurements. Assuming the symmetry of the effect of $I_{\text{BiasI},i}$ and $I_{\text{BiasQ},i}$ on the LO-element output phase shift, Δphase – steps and the associated phase noise performance changes were only recorded for $I_{\text{BiasQ},i}$. Figure 7.23 illustrates the Δ phase-steps as a function of percentage $\Delta I_{\text{BiasQ},i}$ changes along with the accompanying variations in the phase noise measurements. It is noted that the measured Δphases steps are in a relatively good agreement with simulations for $-30\% \leq \Delta I_{\text{BiasQ},i} \leq 20\%$ (maximum error of 3° at $\Delta I_{\text{BiasQ},i} \leq 20\%$). Although beyond the desired calibration range (i.e. $\pm 10\%$), the calibration phase step error between measurements and simulations reaches -6° at $\Delta I_{\text{BiasQ},i} = 30\%$. The saturation in the g_{m,Q_i} at this $\Delta I_{\text{BiasQ},i}$ level is believed to be the reason behind this error. This saturation of g_{m,Q_i} can also be confirmed by observing the negative trend in the measured and simulated phase shift errors in Figure 7.17 at angles $90^\circ \leq \varphi \leq 225^\circ$ where $I_{\text{BiasQ},i}$ reached similar levels (i.e. $I_{\text{BiasQ},i} \geq 2.275\text{mA}$). It is emphasized however that the required phase calibration did not need to exceed 10° for which the range is seen to be relatively linear. The associated phase noise variations with this calibration technique are also shown in Figure 7.23 and are seen to be within 0.8dB evidencing the minor impact this technique has on the phase noise performance. The difference between measurements and simulations is also within 0.8dB and is again attributed to the difference in the tank Q which has been brought about due to the need to modify $V_{\text{ctrl,DGncap}}$ and the on chip generated $V_{\text{ctrl,ncap}}$ to reach oscillations as previously discussed. With its minor impact on phase noise, its relatively linear behaviour with $I_{\text{BiasI},i}$ and $I_{\text{BiasQ},i}$ and its potential for finer resolution*, this technique proves feasible for integrated calibration architectures and hence its use in fine tuning the phase shift measurement test cases in Sections 7.1.6 and 7.2.3.

---

*As discussed in Section 6.3.4, increasing the number of bits for the phase interpolator current steering DAC (to achieve finer phase steps) will naturally increase the available resolution of this fine tuning technique.

Figure 7.23: Measured versus simulated Δ phase – steps as a function of percentage $\Delta I_{\text{Bias}_{Q,i}}$ changes and the accompanying variations in the phase noise measurements. A maximum error of 3° is seen at $\Delta I_{\text{Bias}_{Q,i}} \leq 20\%$.

7.2 Measurements of the Edited Chip

In order to test the functionality of the two LO-elements while both simultaneously running, the thin-oxide varactors have been disconnected from the oscillator tank. Focused ion beam (FIB) technology was employed to chop the top-level metal interconnect between the two thin-oxide varactors and the oscillator tank thereby removing their degrading effect on the overall tank Q. Figure 7.24 shows a full-chip layout view with the locations of the FIB edit marked by ellipses. A zoomed-in view is also shown to illustrate the exact location of the interconnects between the two thin-oxide varactors and the oscillator tank of one of the two identical LO-elements. The main idea behind this chip edit was to enable oscillator startup without having to modify $V_{\text{ctrl,ncap}}$ for each of the LO-elements through a debugging pad which occupied a third side of the chip and prevented probing the other LO-element to test it simultaneously.

Simulations of the extracted view after performing similar cuts in the chip layout indicated a shift in the oscillation frequency to a minimum of 22.16 GHz. With an upper corner frequency of the RC-CR polyphase filter being at 2.22 GHz, a ninth or eleventh subharmonic injection near $22.16 \text{ GHz}/9 \approx 2.462 \text{ GHz}$ or $22.16 \text{ GHz}/11 = 2.0145 \text{ GHz}$, respectively, was still possible with an

Figure 7.24: Two chip layout views showing the details of the metal interconnects which have been edited. A full-chip view showing the locations of the FIB edit marked with ellipses (top) and a zoomed-in view showing the interconnect between the two thin-oxide varactors and the oscillator tank of one of the two identical LO-elements (bottom).

appreciable locking bandwidth. The chip edit thus seemed a feasible solution to proceed with in order to enable simultaneous LO-elements testing.

7.2.1 Tuning Range and Injection Locking Bandwidth Measurements

Upon biasing each LO-element on the edited chip, free-running oscillations have been observed between 21.4 GHz and 22.6 GHz. The measured tuning range in the edited chip is shown in Figure 7.25. Unlike the case with the un-edited chip, oscillations were obtained by touching down on only two (as opposed to three) sides of the chip for each LO-element and thus allowed testing the two elements simultaneously by probing the four sides. It is noted that the measured tuning range was only possible for $V_{\text{gd,DGncap}} < 0$. Foundry measurement curves revealed the highest $Q \approx 20$ for devices of comparable sizes only at $V_{\text{gd,DGncap}} = -0.5$ and hence the $V_{\text{ctrl,DGncap}}$ being well above the supply voltage for sustained oscillations. The available 5 % tuning range of the oscillators in the edited chip allowed some flexibility in choosing the free running oscillation frequency and hence the injection frequency offset, $\Delta\omega_i$, such that it is an integer multiple of the 110 MHz signal generator reference signal. It also facilitated a number of LO-element to element isolation test cases to be carried out which are discussed in details shortly. As illustrated in the measurement testbench in Figure 7.3, the 110 MHz reference signal has been employed as the synchronizing reference between the two signal generators which acted as external subharmonic injection sources.

Due to the shift in the center frequency of the oscillators on the edited chip, the frequency of the injection signals had to be shifted accordingly. With a minimum frequency of oscillation of 21.43 GHz as shown in Figure 7.25, a ninth subharmonic injection signal frequency must be above 2.33 GHz. This is above the upper corner frequency of the RC-CR polyphase filter at 2.22 GHz and therefore a ninth subharmonic injection signal experiences a slightly more than 3 dB of attenuation at a rate of 6 dB/octave. To offset this loss, the phase interpolator current had to be increased by about 1.5 mA. Moreover, since the high-order harmonic synthesis block has been designed for operation near 18 GHz, the synthesized harmonic content in the 21 GHz range is lower than that at 18 GHz. Although relatively inconsequential to the phase shift measurements in this case*, the reduced harmonic content has resulted in more than 70 % reduction in the locking bandwidth for the same input power as is shown in Figure 7.26. This clearly emphasized

---

*Recall that the main goal for the chip edit was to enable phase shift measurements of two simultaneously running LO-elements. A narrower injection locking bandwidth should have a negligible effect on LO-element to element phase shift measurements so long as the injection frequency is chosen near the element free running frequency.

Figure 7.25: Measured tuning range of the free-running oscillator on the edited chip.

the critical role of the high-order harmonic synthesis stage prior to injection and its effectiveness in enhancing the locking bandwidth when operated in the frequency range it was designed for (i.e. as with the case of the unedited chip)*. The output spectrum of one LO-element is also shown in Figure 7.27 while being injection locked.

7.2.2 Measurements of the Isolation between the two LO-elements at 21 GHz

Prior to performing any phase shift measurements of the two LO-elements while simultaneously running, it was important to measure the spectral leakage and to further check if any existing leakage could potentially lead to element to element coupling preventing independent phase steering as previously discussed in Chapter 5.

A number of isolation test cases were executed through on-chip probing. The spectra of the two VCOs were monitored by HP8564E and HP8593E spectrum analyzers. Initially, the center frequencies of the two oscillators were tuned to nearby frequencies and left freely running simultaneously. The center frequency of one oscillator was then swept across the entire tuning range while continuously monitoring to check for any possible inter-injection locking phenomena (i.e. a coupled oscillators array). The same experiment was repeated when one VCO was left freely running while the other was injection-locked to a ninth sub-harmonic external signal. This

---

*See Figure 7.11.

Figure 7.26: Measured locking range for the ninth subharmonic reference used versus the input power level at 21 GHz.

Figure 7.27: Locked oscillator spectrum at 21.51 GHz while phase shifts are being captured simultaneously in time domain.

was performed to investigate if the leaked power from the locked VCO or the associated high-order harmonic synthesis block in one LO-element was sufficient to injection-lock the VCO of the neighbor LO-element. Finally, the two VCOs were injection locked to two separate, but equal, ninth sub-harmonic external signals, simultaneously. The spectrum of one VCO output was measured relative to that leaked from the other.

In all of the test cases outlined above, no inter-injection locking or pulling was observed between the two VCOs while either or both were freely running or injection locked. Figure 7.28 shows the spectra of the two VCOs where one was freely running while the other was injection locked. No leaked tones from the other LO-element can be observed above the obtained noise floor across the full span of the spectrum analyzer.

Figure 7.28: Measured spectra of the two VCOs running simultaneously. One VCO was left free running (left) while the other was injection-locked (right).

In trying to de-embed the lateral leakage between probes while landed on the chip as shown in Figure 7.29, the leaked spectrum from one LO-element to the other was recorded twice; one time when the two probes were landed (one probe per each LO-element) and another when one probe has been lifted off while the other was landed. Figure 7.30 shows the measured spectrum leakage after narrowing the span and the resolution bandwidth. It is seen that at the higher end of the tuning range, the leakage is weaker when the receiving probe was lifted off the chip. At the lower-end of the tuning range, however, the leakage was mostly stronger when the receiving probe was lifted off. This implied that the recorded leakage was dominated by the lateral coupling between the probes. It also lead to the conclusion that the coupling through the near-field, the substrate and the pad-ring was too weak to be extracted through this test setting since the measured lateral

Figure 7.29: An illustration of the four probes while landed on the four sides of the chip.

Figure 7.30: Measured spectrum leakage between two LO-elements.

coupling between the probes overshadowed any weaker coupling through other channels.

With a phase noise performance ranked among the best published in the K-Band for CMOS (Figures 7.35(a) and 7.35(b)), and an independent phase shifting capability across the entire 360° with steps of 22.5° as is reported shortly, these results attest not only to the practicality of the isolation techniques employed but also to the possibility of realizing multiple independent phase-locked K-band oscillators in a main stream CMOS technology with superior phase noise performance and independent phase steerability through sub-harmonic injection on the same die.

7.2.3 Phase Shift Measurements of the Two LO-elements and the Associated Beam steering Results at 21 GHz

With the two LO-elements simultaneously running on the same die, element to element delta phase shift measurements were made possible. The measurement setup for this test case is as described in Section 7.1.6 and illustrated in Figure 7.3. The two signal generators which have been used as the sub-harmonic injection signal sources were synchronized through their readily available 110 MHz I/O reference. Again, the spectra of the two LO-element output signals were monitored by HP8564E and HP8593E spectrum analyzers while the two time-domain signals and their relative phase relationships were monitored by a dual-channel 50-GHz HP54752A sampling scope.

In each phase shift measurement, the element to element phase errors were determined in a similar procedure to that followed with the unedited chip at 18 GHz with minor modifications as follows. The cartesian $g_{m,I,Q}$ weights were set to their balanced state by setting $I_{Bias,I_1} = I_{Bias,Q_1}$ for each element and the initial phase difference was recorded. The cartesian $g_{m,I,Q}$ weights of one element was then set to phase shift its output phase to a desired angle, ψ , by setting I_{Bias,I_1} and I_{Bias,Q_1} such that $\tan(\psi/N) = g_{m,Q}/g_{m,I} = \sqrt{I_{Bias,Q_1}/I_{Bias,I_1}}$, where $N = 9$. The resulting delta phase shift between the two outputs was then re-recorded and compared to that expected from theory. This process was repeated for $0 \leq \psi \leq 2\pi$ with steps of 22.5° . As previously mentioned, all the required g_m weights and their corresponding $I_{Bias,I}$ and $I_{Bias,Q}$ calculations for $0^\circ \leq \psi/N \leq 40^\circ$ were fully automated and set by a MATLAB program which was developed to control the programmable Keithley® power supplies through a PC interface as illustrated in Figure 7.3.

A sample of a number of captured time-domain waveforms with various phase relationships are shown in Figure 7.31. Shown in Figure 7.32 are measurements of all the element to element phase shifts and the associated phase shift errors between the outputs of the two simultaneously

injection locked oscillators over the entire 360° range with steps of 22.5° . A maximum phase shift error of 9.86° is obtained. After calibration, the maximum error is 2.1° . Due to its potential for high phase resolution and its minor phase noise impact, phase calibrations have been achieved by fine tuning the phase-interpolator I & Q g_m weights as discussed in Section 6.3.4.

Figure 7.31: Superimposed time-domain waveforms obtained from a number of phase shift measurement steps. Each waveform corresponds to an output of a locked LO-element in response to a separate phase-shifter state as outlined in Section 4.3.1.

In order to investigate the impact of the measured phase shift errors on beam steering, the normalized array factor has been plotted for several sequences of progressive phase shifts for four- and eight-element arrays in 7.33 and 7.34, respectively. Once again, it is seen that the LO-element to element delta phase shifts errors yield minor phase steering errors compared to the ideal case with a peak-to-null ratio of better than 30 dB*.

7.2.4 Phase Noise Performance Measurements and Its Sensitivity to Phase Steering

The phase noise performance has been recorded for one of the LO-elements while injection locked to subharmonic injection signals at 21.7 GHz/9 and 21.51 GHz/9 from Agilent E8257C and E4432B signal generators, respectively. In each test case, the two LO-elements were injection locked simultaneously using two synchronized signal generators. Shown in Figures 7.35(a) and 7.35(b) is the phase noise performance at 21.7 GHz and 21.51 GHz, respectively. It is seen that

---

*Similar to the beam steering results plotted for the unedited chip at 18 GHz, only those sequences yielding the worst case progressive phase shifts and hence array patterns are shown.

Figure 7.32: Measured phase shifts and associated errors between two oscillator outputs before and after calibration.

better than -107 dBc/Hz was obtained at 1 MHz offset in both cases. It is also seen that the close in phase noise profile is better in the 21.7 GHz case (where E8257C was used). In case of the 21.7 GHz carrier, -98 dBc/Hz and -103.17 dBc/Hz were obtained at 10 KHz and 100 KHz offsets, respectively, versus -81 dBc/Hz and -99 dBc/Hz at the same respective offsets for the 21.51 GHz carrier. In both cases, however, it was observed that the phase noise profiles followed the $20 \log N$ estimate [97], where $N = 9$ for each signal generator. For example, the phase noise of the injected signal at $21.51 \text{ GHz}/9 = 2.39 \text{ GHz}$ has been measured -126 dBc/Hz at 1 MHz . That is, the phase noise propagation through the quadrature phase generation, the phase interpolation, the high-order harmonic synthesis and the injection transistor stages has resulted in a phase noise degradation of -18.83 dB . Once again, this is within fractions of a dB to the expected $20 \log 9 \simeq 19.1 \text{ dB}$ phase noise degradation due to the up multiplication process [97]. This result signifies the feasibility of the adopted injection locking technique as a viable approach towards achieving superior close in phase noise performance at K-band.

In Section 7.1.7, the impact of LO phase steering on the obtained phase noise performance was examined in the unedited chip successfully demonstrating their relative independence at 18 GHz . Although the LO-element to element leakage (i.e. isolation) test cases (Section 7.2.2) have shown no sign of inter-injection locking or coupling phenomena, it was still important to

Figure 7.33: Phase steering results for 4-element arrays based on the phase shifts obtained from measurements with and without calibration and how they compare to the ideal case. Phase shift sequences used are (a) $[0^\circ, -22.5^\circ, -45^\circ, \dots]$, (b) $[0^\circ, 45^\circ, 90^\circ, \dots]$, (c) $[0^\circ, -90^\circ, -180^\circ, \dots]$ and (d) $[0^\circ, 90^\circ, 180^\circ, \dots]$.

Figure 7.34: Phase steering results for 8-element arrays based on the phase shifts obtained from measurements with and without calibration and how they compare to the ideal case. Phase shift sequences used are (a) $[0^\circ, -45^\circ, -90^\circ, \dots]$, (b) $[0^\circ, 45^\circ, 90^\circ, \dots]$, (c) $[0^\circ, -135^\circ, -270^\circ, \dots]$ and (d) $[0^\circ, 135^\circ, 270^\circ, \dots]$.

Figure 7.35: (a) Measurement of the phase noise performance for one of the LO-elements while injection locked to subharmonic injection signals at (a) 21.7 GHz/9 and (b) 21.51 GHz/9 from Agilent E8257C and E4432B signal generators, respectively.

re-examine the phase steering to phase noise relationship especially with the two LO-elements simultaneously running on the same die. Figure 7.36 shows the measured phase noise performance at 1 MHz offset from a 21.69 GHz carrier for various phase shifts across the entire 360° range. A maximum phase noise variation of less than 1.5 dB can be observed demonstrating once again a similar independence of phase steering. This 0.5 dB difference from that obtained at 18 GHz is believed to be due to the associated change of the phase shifter gain among different phase shifts especially that the input reference at 2.41 GHz experiences more attenuation beyond the -3 dB corner frequency of the polyphase filter at 2.22 GHz as already discussed in Section 7.2.1. With this relatively constant and superior phase noise performance at K-Band for a main stream CMOS implementation* as well as the independent phase steering capability of each of the two LO-elements while simultaneously running on the same die, the feasibility of the proposed architecture and its successful functionality is thus shown at 18 and 21 GHz.

---

*The phase noise performance reported is a function of the phase noise profile of the signal generators, however, the $20 \log N$ expected degradation due to the frequency up-multiplication has not been exceeded in all of the test cases despite the $1/f$ and thermal noise generation and propagation through the LO-element circuit blocks.

Figure 7.36: Measurement of the effect of phase steering one of the oscillator outputs on its phase noise performance while both oscillators are injection-locked to the 9th harmonic of the distributed reference.

7.3 Comparison to Integrated LO-Path Phased-Array Architectures from Literature

Making a fair comparison between the phase steering architecture described in this work and the available alternatives previously published in the literature is a challenging task. Although the power saving advantages that this architecture offers may seem straightforward to compare quantitatively to other implementations, comparisons become non-trivial when the alternative implementations choose to only report an architectural level, as opposed to a detailed block level, power consumption for the individual circuits comprising these architectures (e.g. RF/millimeter-wave global and local LO distribution buffers and phase shifters) that the new architecture is trying to improve on by lowering their frequencies. Additionally, the design challenges that are associated with i) multi-phase signal generation and distribution and ii) designing phase shifters, transmission line structures and conventional PLL building blocks at fundamental RF/millimeter-wave frequencies, which the presented architecture offers to relax are unquantifiable yet advantageous. As such, comparisons are discussed in the following paragraphs and summarized in Table 7.2 to the best the author could compile and isolate performance data as reported in the corresponding publications of the compared alternatives. However, to the best of the author's knowledge at the

time of publishing this work, no previously published work suggested a similar LO-path based phase-steering technique for a phased array architecture on bulk CMOS at 18 GHz which allows distributing a ninth sub-harmonic LO reference with a 2π phase shifting capability in steps of 22.5° . The author is also unaware of a previously published high-order harmonic synthesis stage that is capable of harmonic enhancement up to the the ninth harmonic at 18 GHz which lead to the reported injection locking bandwidth at that frequency.

The phase shifting schemes in [1] and [5] were parts of an integrated phased-array receiver and a transmitter at 24 GHz with LO-based phase shifting on silicon where centralized multi-phase millimeter-wave PLLs were employed for the generation of 16 phases of a 19.2 GHz first LO. As has been shown in Fig.2.11, the 16 (or, 8 differential) LO phases are distributed to eight phase selectors in a symmetric binary tree structure. Coherently distributing these multiple phases to each phase selector at each one of the eight front-end locations were subject to EM crosstalk between with adjacent lines. Multi-mode excitation because of these arrangements led to potential phase and magnitude errors [1]. In both the receiver and the transmitter, the reported current consumption for each phase selector was 24 mA and 34 mA, respectively, from a 2.5 V at 19.2 GHz. This is due to the need for 3 sets of 8 differential pairs (i.e. 2 sets for I and Q weights and third dummy set for load balancing). The frequency synthesizer was $180 \text{ mA} \times 2.5 \text{ V}$ normalized to 8 elements. The estimate for the VCO buffers slightly varied between the transmitter and the receiver and averaged about 9.8 mW per element. A per-element power consumption of $59 \text{ mA} \times 2.5 = 147.5 \text{ mW}$ and $61 \text{ mA} \times 2.5 = 152.5 \text{ mW}$ has been reported for the receiver and the transmitter, respectively. As discussed in Section 2.5, this has been a remarkable milestone towards integrated phased-arrays on silicon but the generation and distribution scheme of multiple LO-phases needed to be improved on due to i) the power consumption of the $n \times (16 : 1)$ RF/millimeter-wave phase selectors and the differential power-matched buffers per each array-element front-end, ii) the silicon area associated with the parallel distribution tree structures at 19.2 GHz [2].

In [2], an integrated 77 GHz four-element phased-array transceiver was introduced in a $0.12 \mu\text{m}$ SiGe BiCMOS technology with a first LO at 52 GHz. The realization of multiple LO phases has been achieved by employing 52 GHz millimeter-wave phase rotators at each array element location prior to the mixing stage in each front-end. This enabled the architecture to replace the distribution of multiple millimeter-wave LO phases by a single-phase LO signal at 52 GHz. Employing millimeter-wave phase rotators at each front-end location allowed to generate the desired LO phase shift locally which lead to significant silicon area savings compared to the

architecture in [1] especially with increased number of elements and phase resolution. The challenges associated with designing millimeter-wave phase rotators and distributing multiple copies of a millimeter-wave LO signal to multiple distant front-ends on silicon at 52 GHz remained as potential bottlenecks. This is due the power consumption and the silicon area associated with intermediate power-matched buffering and transmission line structures, respectively, as required in millimeter-wave distribution networks. The LO-path power consumption included $10\text{ mA} \times 2.5\text{ V}$ for VCO and buffers, $14\text{ mA} \times 2.5\text{ V}$ in each millimeter phase rotator and $12\text{ mA} \times 2.5\text{ V}$ for each distribution buffer but the number of distribution buffers were not specified. The reported phase noise was -95 dBc/Hz at 1 MHz offset.

In [3], an integrated coupled-oscillator arrays was reported for a 60 GHz phased-array transmitter architecture in a $0.13\text{ }\mu\text{m}$ SiGe BiCMOS technology. A 20 GHz input was adopted as the inter-injection locking signal among the coupled oscillators. As such, the 20 GHz inter-injection signal is passed through a frequency doubler prior to injection into each 40 GHz VCO. For a 60 GHz carrier to be synthesized, the output of each 40 GHz coupled VCO is mixed up with its divided-by-2 output (i.e. 20 GHz) in a SSB operation. This re-synthesized inter-injection locking signal at each array element gets routed to the next in a bi-lateral arrangement. The choice of the third subharmonic and frequency doubling aimed at minimizing the attenuation of the inter-injection signals among the coupled-oscillator array elements and hence the improvement in the locking range. As a result, overcoming the potential rapid degradation in the PN performance with the increasing array size [51] remained a challenge especially as the oscillator array elements undergo frequency de-tuning due to PVT variations. In addition, the realization of phase-shifting at millimeter-wave frequencies, the distribution buffers along with the frequency doubler at 20 GHz, a divider at 40 GHz and two SSB mixing operation to yield I and Q outputs at 60 GHz at each array element has led to a challenging power budget of 375 mW per element. While no power consumption was mentioned for the phase shifters at 52 GHz which is likely to be large, the architecture consumed $25\text{ mA} \times 2.5\text{ V}$ in each static frequency divider and $125\text{ mA} \times 2.5\text{ V}$ in the oscillator, the frequency doubler and the coupling LO buffers. The reported phase noise is -112 dBc/Hz at 1 MHz offset from a 40 GHz carrier.

In [116], a 6-18 GHz $0.13\text{ }\mu\text{m}$ CMOS tunable concurrent dual-band multi-beam phased-array receiver has been reported. The 12 GHz LO signals that are generated from the frequency synthesizers are distributed to two RF mixers (Vertical and horizontal polarizations) and to four IF mixers and phase rotators (two bands per polarization) where the phase steering is performed at the first IF at 6 GHz. The worst case LO distribution length became as long as 3.7 mm for

the lower band at 6 GHz where phase steering is performed at 3 GHz. As such, LO buffers were needed to compensate for the insertion loss and bandwidth limitation which were caused by the excessively long signal distribution. Each LO distribution path included a two-stage buffer (a self-biased cascode followed by a common-source amplifier with shunt peaking). The fact that the LO phase shifting is not performed until the first IF allowed the phase rotators and the first IF LO signal and distribution buffers to be at half the first LO frequency (12 GHz). This lead to power consumptions of $4.8\text{ mA} \times 2.5\text{ V}$ in the phase rotator, $64\text{ mA} \times 2.5\text{ V}$ and $19\text{ mA} \times 1.2\text{ V}$ in the LO distribution buffers. The reported phase noise performance is -99 dBc/Hz at 1 MHz. Although this architecture might seem at first to have reduced the power consumption in the LO path, this should not be taken as the complete story. Phase shifting at the first IF forces the individual RF signal paths to extend from each antenna element to the first IF where the coherent combining step is completed implying that the number of first IF mixers, the IF LO signals and distribution buffers is multiplied by the number of antenna elements. This makes the apparent reduction in the first LO-path power simply show up as an increase in the RF signal path circuitry. This is likely to worsen as the architecture scales up in size, number of bands, concurrent beams and the frequency of operation.

Although implemented at a lower frequency than the proposed architecture in this work, the architecture in [116] is a clear example of how future integrated phase-array architectures may evolve to denser implementations with multi-beam multi-band capabilities and hence the critical role of the proposed high-order subharmonic LO signal distribution and phase shifting architecture.

Table 7.2: Comparison to similar works from literature

Ref.	Technology	LO Frequency (GHz)	PN at 1 MHz (dBc/Hz)	Peak-to-Null Ratio (dB)	Power consumption (per element)
[1]	0.18 μ m SiGe BiCMOS	19.2	-103	20	83 mA $\times$ 2.5 V
[2]	0.12 μ m SiGe BiCMOS	52	-95	>12	(24+12 $\times$ k [†]) mA $\times$ 2.5 V
[3]	0.13 μ m SiGe BiCMOS	40	-112	-	150 mA $\times$ 2.5 V [†]
[5]	0.18 μ m CMOS	19.2	-103	>23	95 mA $\times$ 2.5 V
[116]	0.13 μ m CMOS	12	-99	>21.5	(12 [§] +4.8) mA $\times$ 2.5 V + buffers ^{§§}
[117] ^{‡‡}	90 nm CMOS	23.5-25	-93.7	-	51.4 mA [¶] $\times$ 1.2 V
this work	0.13 μ m CMOS	18.31	-115	> 28	26.8 [¶] mA $\times$ 1.2 V
this work	0.13 μ m CMOS	21.51	-107.17	> 28	30.3 [¶] mA $\times$ 1.2 V

[†]k denotes the number of 52 GHz LO distribution buffers per array element but was not explicitly specified.

[‡]Reported power consumption is for synthesizing quadrature 60 GHz LO signals locally. Phase shifter power consumption per element was not reported.

[§]VCO (12 mA/2.5 V) is shared between all array elements.

^{§§}LO distribution buffers consumed (64 mA/2.5 V) and (19 mA/1.2 V) but could not be isolated for each array element.

^{‡‡}A 4 $\times$ 4 multi-beam passive Butler matrix with no phase steering.

[¶]Power consumption of the quadrature LC-VCO normalized to one element.

^{¶¶}This is excluding current consumption of the FT-doubler buffer that has been used to drive the ESD structures, chip pads and off-chip loads for the prototype chip.

7.4 Summary

Free running oscillations were observed at the targeted 18 GHz for the two LO-elements with a de-embedded output power of -15.67 dBm and -17.67 dBm, respectively. This was obtained after modifying the thin-oxide varactor control voltage through a chip pad that was available for debugging. As such, the functionality of each of the two LO-elements could still be fully tested separately at 18 GHz. Also a limited tuning range of 2.2 % was obtained due to the thin-oxide varactor model inaccuracies in capturing the loss mechanisms which degraded the overall tank Q only permitting oscillations within the negative $V_{ncap_{gd}}$ range. Nonetheless, this tuning range was enough to test the full functionality of the LO-elements.

The high-order harmonic synthesis stage was initially tested using an injection signal at 2.03 GHz with the oscillator negative g_m switched OFF. Harmonics were observed up to 20.3 GHz (i.e. the tenth harmonic) successfully demonstrating its functionality. Once switched ON, the oscillator negative g_m core resulted in a 21.8 dB enhancement of the 9th harmonic power level at 18.27 GHz reaching -14.51 dBm which aligned well with simulations. With an achieved one-sided locking range above 110 MHz and approaching that obtained in simulations at an injection power level below -10.5 dBm, the effective role of the harmonic synthesis block is thus proven. The idea of using a Q-enhanced filter instead of an oscillator to realize the ninth harmonic carrier has also been tested. The resulting power in the carrier for this technique measured -22.83 dBm, about 6 dB less than that of the injection locked oscillator approach. A -3 dB bandwidth of 324 MHz has also been observed which is about 45 % larger than the injection locking bandwidth in the oscillator based technique.

The measured phase noise performance for an injection locked LO-element attained -102, and -105 dBc/Hz at 10 KHz, 100 KHz offsets, respectively, from a 18 GHz carrier using Agilent's E8257C signal generator. At 1 MHz offset from a 18.31 GHz carrier, the recorded phase noise was -115 dBc/Hz using Agilent's E4432B signal generator. In all cases, close to minimal phase noise degradation has been achieved despite the 1/f and thermal noise generation and propagation through the LO-element circuit blocks. The integrated RMS jitter has been calculated by the spectrum analyzer with integration limits between 100 Hz and 100 MHz and it is 0.2147°.

Phase-shift measurements have been initially performed for one LO-element relative to a synchronized external reference at 18.27 GHz. The maximum phase shift errors were 8.5° and 2.35° before and after calibration, respectively, yielding minor phase steering errors compared to the ideal case.

The effect of phase steering on the phase noise performance was recorded. The measured

phase noise performance at 1 MHz offset from a 18.27 GHz carrier for all phase shifts resulted in a maximum phase noise variation of ± 1 dB demonstrating their relative independence in this architecture.

Measurements of the sensitivity of the output phase shift to changes in the tail current of the oscillator core revealed that the slope of $\Delta\phi_{ss,i}/\Delta I_{ss,i}$ is $-4.3^\circ/\text{mA}$ versus $-1.7^\circ/\text{mA}$ which was obtained in simulations. The sensitivity of Phase Shifts to changes in phase interpolator cartesian weights has also been evaluated through measurements where a slope of 10° per 10 % change in $I_{BiasQ,i}$ was obtained for a range of $-30\% \leq \Delta I_{BiasQ,i} \leq 20\%$.

Testing the functionality of the two LO-elements simultaneously could only be possible after disconnecting the thin-oxide varactors from the oscillator tank. This resulted in a shift in the center frequency of oscillation and a resulting tuning range of 21.4 GHz to 22.6 GHz.

The spectral leakage was monitored between the two LO-elements while simultaneously running. A number of isolation test cases were also executed through on-chip probing to check if any existing leakage could potentially result in element to element coupling. No inter-injection locking or pulling was observed between the two VCOs while either or both were freely running or injection locked. Moreover, it was found that coupling through the near-field, the substrate and the pad-ring was too weak to be extracted since the measured lateral coupling between the probes overshadowed any weaker coupling through these channels.

LO-element to element phase shifts and phase steering errors were measured at 21.51 GHz. A maximum phase shift error of 9.86° is obtained. After calibration, the maximum error is 2.1° .

The phase noise performance has been measured at 21.7 GHz and 21.51 GHz when injection locked to a ninth subharmonic input from Agilent E8257C and E4432B signal generators, respectively. Slightly better than -107 dBc/Hz was obtained at 1 MHz offset in both cases. The close in phase noise profile seemed to be better in the 21.7 GHz case (where E8257C was used). For example, -98 dBc/Hz and -103.17 dBc/Hz were obtained at 10 KHz and 100 KHz offsets, respectively, versus -81 dBc/Hz and -99 dBc/Hz at the same respective offsets for the 21.51 GHz carrier. This is believed to be due to the difference in the phase noise profile between the two signal generators used. The sensitivity of the phase noise performance to phase steering were also investigated at 1 MHz offset from a 21.69 GHz carrier for different phase shifts where a maximum phase noise change of less than 1.5 dB was observed.

With all of the measurement test cases summarized herein, the functionality of the LO-elements have been fully tested separately at 18 GHz and while simultaneously running at 21 GHz successfully demonstrating the feasibility of the proposed architecture.

Comparing the phase steering architecture described in this work with published alternatives has been a challenging task. Distributing a high-order sub-harmonic LO reference to reduce the power consumption that is associated with multi-phase signal generation and distribution at RF/millimeter-wave frequencies may seem straightforward to compare to alternative approaches. However, comparisons become non-trivial if the alternative implementations do not report the associated power consumption of the individual circuit blocks (e.g. RF/millimeter-wave distribution buffers) that the proposed architecture is trying to improve on by scaling down their frequencies (e.g. LO distribution buffers and phase shifters). Additionally, the design challenges in i) multi-phase signal generation and distribution and in ii) designing phase shifters and conventional PLL building blocks at fundamental RF/millimeter-wave frequencies, which the presented architecture offers to relax are unquantifiable yet advantageous. Comparisons to phased-array architectures from the literature showed not only that the proposed LO distribution scheme is in good standing in terms of its power consumption, but also showed that its phase noise performance has not been compromised. In fact, it seemed that the phase noise performance of the proposed injection locking approach outperforms those reported. It must be emphasized, however, that at the time of the publication of the proposed architecture, the author is unaware of a previously published results suggesting a similar LO-path based phase-steering technique for a phased array architecture on bulk CMOS which allows distributing a ninth sub-harmonic LO reference with a $2\pi/9$ phase shifting capability. The author is also unaware of a previously published high-order harmonic synthesis stage that is capable of harmonic enhancement up to the the ninth harmonic at 18 GHz which lead to the reported injection locking bandwidth at the same frequency.

Chapter 8

Conclusion

This thesis has focused on integrated LO-path based phase-shifting techniques for phased-array architectures with the goal of i) reducing the power consumption that is associated with multi-phase LO signal generation and distribution, and ii) relaxing the need to design phase shifters, transmission line structures and conventional PLL building blocks at fundamental RF/millimeter-wave frequencies.

To this end, a novel sub-harmonic LO-path phase shifting architecture has been developed for integrated phased-arrays on silicon at K-band. The proposed architecture consisted of a high resolution cartesian phase shifter which has been developed to provide angles between 0 and $(2\pi/N)$ degrees with a minimum phase step of 22.5° at the 9th subharmonic. The architecture exploited the implicit frequency multiplication operation through the generation of high-order harmonics in high-speed limiting amplifiers and latches to synthesize multiple phases of ninth-harmonic tones. A high-order harmonic synthesis stage consisting of cascaded limiting amplifiers followed by a high-speed latch has been developed to enhance the harmonic content of the phase shifted reference prior to injection in to a free running K-band oscillator at the ninth harmonic of the injected reference. These multiple phases are synthesized at the destination and in close proximity to RF/millimeter-wave injection-locked oscillators. The architecture then takes advantage of the existence of only one stable solution for Adler's transient equation for oscillators *phase* locking through injection to control the output phases of each LO-element oscillator and thus the phase steering capability in each element.

A prototype chip with two integrated LO-elements have been fabricated in a standard 130-nm CMOS process. The functionality of each of the two LO-elements has been fully tested separately at 18 GHz. Phase-shift measurements for one LO-element relative to a synchronized external reference resulted in maximum phase shift errors of 8.5° and 2.35° before and after calibration,

respectively, yielding minor phase steering errors compared to the ideal case. The measured phase noise performance for an injection locked LO-element reached -102, and -105 dBc/Hz at 10 KHz, 100 KHz offsets, respectively, from a 18 GHz carrier. At 1 MHz offset from a 18.31 GHz carrier, the recorded phase noise was -115 dBc/Hz. In all cases, close to minimal phase noise degradation has been achieved despite the $1/f$ and thermal noise generation and propagation through the LO-element circuit blocks. The integrated RMS jitter has been calculated by the spectrum analyzer with integration limits between 100 Hz and 100 MHz and it is 0.2147° .

The two LO-elements have also been tested simultaneously at 21 GHz resulting in a maximum element to element phase shift errors of 9.86° and 2.1° before and after calibration, respectively. Better than -98 dBc/Hz and -103 dBc/Hz and -107 dBc/Hz of phase noise performance were obtained at 10 KHz and 100 KHz and 1 MHz offsets from a 21.51 GHz carrier.

Techniques and experimental results for isolating multiple K-band CMOS oscillators, harmonic synthesis blocks and phase-shifters were demonstrated. The adopted techniques yielded a worst-case spectrum leakage level of -77 dBm between two integrated LO-elements. While the reported leakage levels are believed to be overshadowed by a lateral probe-to-probe coupling, the reported phase noise performance, the absence of inter-injection locking between the oscillators and the ability to steer the phase of each oscillator independently demonstrates the practicality of the utilized isolation techniques.

With the prototype measurement results obtained, the proposed architecture has demonstrated three unique key distinguishing features to it; First, distributing a high-order sub-harmonic LO reference not only helps significantly reduce the power consumption that is associated with multi-phase signal generation and distribution at RF/millimeter-wave frequencies (see Table 7.2), but also relaxes the challenges associated with designing integrated power-matched buffers and low-loss transmission-line structures that are needed for the LO distribution in the same frequency range. Second is the large injection locking bandwidth obtained. With an achieved one-sided locking range above 110 MHz approaching that obtained in simulations at an injection power level below -10.5 dBm, the effective role of the harmonic synthesis block in enhancing the locking bandwidth is thus demonstrated. Synthesizing a high-order harmonic prior to injection such that the injected tone is a fundamental to the oscillator admits a higher injection strength than that of a sub-harmonic injection and thus a wider locking bandwidth. Third is the relative independence of the phase noise performance from phase steering which has been successfully demonstrated in this architecture upon measuring a maximum phase noise variation of ± 1 dB and < 1.5 dB at 1 MHz offset from 18.27 GHz and 21.69 GHz carriers, respectively, across the entire 360° phase

shift range. This is seen as another true key differentiator of the proposed technique. Since, in this scheme, subharmonic phase shifters control the output phase of each LO-element, none of the oscillators needs to operate near the edge of its locking bandwidth nor does it need to change its intrinsic operating point in order to realize any phase shift, this thus explains the observed independence of the obtained phase shift from the phase noise performance of the LO-elements.

A number of examples in the literature [2] [111,116,117] have recently demonstrated how future integrated phased-array architectures are expected to evolve to much denser implementations with concurrent multi-beam and multi-band capabilities. With the increased number of front-end(s) accompanying each array element and the current push towards higher RF/millimeter-wave frequency bands (e.g. Q-, U-, V-, E- and W-bands) along with the naturally large chip areas of integrated phased-arrays, the critical role of the proposed high-order subharmonic LO signal distribution architecture and its outlined key advantages are clearly emphasized.

8.1 Thesis Contributions

A number of contributions to the field of RF integrated circuit design have resulted from this thesis. These include:

1. The development of an integrated two-element LO-path based phase steering architecture which employs phase-shifters at the ninth sub-harmonic followed by frequency multiplication up to the 9^{th} harmonic and injection locking. The architecture is extendable to a n -element array, where $n > 2$. This main contribution can be divided into the following sub-contributions:
  - (a) The idea of distributing ninth sub-harmonic reference copies to the distant on-chip front-ends that are co-located with the array elements. This approach relaxes the design challenges and reduces the power consumption that are associated with RF/millimeter-wave routing and buffering of a fundamental LO signal as compared to that with a 9^{th} subharmonic reference. [81] [84].
  - (b) The idea of phase steering utilizing phase shifters at the ninth sub-harmonic instead of performing the same operation at the fundamental. This relaxes the design challenges and the power consumption requirements that are associated with phase-shifters at RF/millimeter-wave frequencies [81] [84].
  - (c) Design and implementation of a novel 9^{th} harmonic synthesis block with an output

harmonic content at 18 GHz in a main stream CMOS technology enhancing the measured oscillator injection strength and the locking bandwidth. Two main architectural variations were compared as follows:

- The first approach utilizes cascaded pre-amplifiers for amplitude limiting followed by a high speed latch to enhance the rise/fall time and thus the harmonic content of the output signal [118].
  - The second approach replaces the high-speed latch with a Q-enhanced filter stage to selectively improve the 9th harmonic output. [84].
- (d) The demonstration of the relative independence of the phase noise performance from the achievable phase shift across the entire 360° range for each LO-element separately at 18.27 GHz for two simultaneously running elements at 21.69 GHz. This is a result of performing the phase shifting operation without the need for oscillator de-tuning [118].

The above contribution items have initially been reported at the 2009 IEEE Asia Pacific Microwave Conference (APMC) [84]. A variation on the architecture has been reported at the 2010 IEEE Radio and Wireless Symposium [81]. Based on the paper presented at the APMC conference [84], the authors were invited to submit an article on the proposed architecture to the December, 2010, special issue of the Transactions on Microwave Theory and Techniques [118].

2. Demonstration of the feasibility of integrating multiple K-band injection locked oscillators, high-order harmonic synthesis blocks and phase-shifters on a main stream CMOS process with a worst-case spectrum leakage level of -77 dBm at 21 GHz and the ability to steer the phase of each oscillator independently. This has been reported at the 2011 IEEE Asia Pacific Microwave Conference (APMC) [119].
3. The sensitivity analysis of the inter-element phase-mismatch fine-tuning and calibration means. The conducted mathematical analysis in Chapter 6 along with measurements in Sections 7.1.8 and 7.1.9 quantitatively explores the parameters governing the attainable phase offset resolution for each of the fine-tuning techniques discussed. This has been reported at the 2012 IEEE Radio and Wireless Symposium (RWS) [120].
4. The mathematical analysis showing the relationship between the duty cycle of a rectangular waveform and its fundamental-to -desired-harmonic ratio. This clarified the advantages of

duty-cycle compression when the fundamental-to-desired-harmonic ratio is of a performance implication to the application. This has been reported in Section 3.4.4.

5. The development of a circuit design methodology for the high-speed latch to enhance the harmonic content of an amplitude limited input signal. The methodology aims at synthesizing active and passive component values for a desired rise-time and harmonic content. This has been reported in Section 4.3.2 and [118].

8.2 Future Work

Having successfully demonstrated the feasibility of the proposed architecture and its potential advantages to the observed evolution trend of future integrated phased-array architectures, a number of research ideas are yet to be explored further with the goal of learning more about the trade-offs in expanded versions of this architecture.

A newer prototype version can be fabricated with integrated 24 GHz front ends. Each front end consists of a variable gain low noise amplifier (LNA) and a down-conversion mixer while each LO-element oscillator drives the LO ports of the corresponding RF mixer. The number of elements may also be expanded to four elements. Current domain coherent combining can be accomplished through a common load for all the RF mixers or alternatively through off chip power combiners at the IF. The variable gain LNA along with the LO-path phase shifting capability will enable conceptual beam and null steering with the aid of the resulting complex weights*. Integrated on-chip matching networks for the LNAs will also facilitate the use of off-chip 24 GHz phase shifters to emulate a plane wave striking the receive elements with various delays[†] to test the receiver performance against several angles of arrival.

Another modification is to introduce antenna elements at the input of the LNAs. In this case, the conceptual beam steering and coherent combining capability of the receiver can be tested with true plane waves having certain angles of arrival in an anechoic chamber setting. This is a closer step towards exploring, and perhaps isolating, the antenna elements coupling effects and their impact on beam steering and coherent combining.

Replacing the ideal ninth sub-harmonic reference at 2 GHz with a fully integrated PLL and a commercial crystal clock reference is an important research step towards realizing the impact of a completely integrated solution on the phase noise performance of the LO-elements in general

---

*In theory, complex weights are obtained by the magnitude of the LNA gains and the LO phase shift. However, non-idealities are to be expected in which case, LO phase calibration may compensate in extreme cases.

[†]A narrow band, true-time delay approximation is assumed in this case.

and on the receiver SNR/SINR performance in particular.

Another possible modification to the architecture is to introduce a differential duty cycle compression circuit in the high-order harmonic synthesis stage prior to injection of the up-multiplied tone into the oscillator. The benefits of this modification has been already discussed in details in Chapter 3. The detailed mathematical analysis in Section 3.4.4 revealed about 82% reduction in the magnitude of the LO reference relative to that in the case of 50 % duty cycle without affecting the magnitude of the desired harmonic (See Figure 3.10). This modification should result in a proportional reduction in the magnitudes of the undesired harmonics as seen in Figure 7.8 and hence considerably improve on the issues of mixing spurs, image frequency and interference in the proposed architecture.

Once the phase steering practical circuit impediments have been identified through the modifications above, automated tuning and calibration techniques based on sub-sampling architectures, such as those reported in [76], [121] and [122], can be developed. The practically proven architecture in [123] can be ported to initially tune the center frequency of the LO-elements' oscillators. Once the LO-elements are tuned and injection locked, the same sub-sampling architecture can be reused to automate the element to element phase shift calibration through the fine tuning means discussed in Chapter 6 (e.g. I_{Bias_I} and I_{Bias_Q}). This is one step forward towards the realization of the proposed architecture in a much denser array and in presence of process, supply voltage and temperature (PVT) variations.

Appendix A

Extraction Formulae for the Double- π Inductor Model Parameters

The double- π inductor model in Fig. A.1 has been shown to accurately capture various frequency dependent loss mechanisms over a broadband range [108, 109]. The effect of the substrate is modeled by an elaborate distributed RC network. The increased series loss at RF/millimeter-wave frequencies due to the skin effect is modeled by a ladder network consisting of L_f and R_f in parallel with R_m [109].

Figure A.1: A compact broadband inductor model.

The double- π model parameters can be extracted from the y -parameters simulations on two steps. Initially, the low frequency series inductance and resistance for the single- π low-frequency model in Figure A.2 are extracted from y_{12} as,

$$L_{DC} = \frac{\Im\{-y_{12}^{-1}\}}{\omega} \quad (\text{A.0.1})$$

and

$$R_{DC} = \Re\{-y_{12}^{-1}\}. \quad (\text{A.0.2})$$

Figure A.2: A low-frequency (below 1 GHz) inductor model for extraction of oxide capacitances and substrate resistances.

The oxide capacitances and substrate resistances that are associated with the single- π low-frequency model in Figure A.2 can also be extracted from simulations as,

$$C_{OX1} = \frac{\left[\Im \left\{ \frac{1}{y_{11} + y_{12}} \right\} \right]^{-1}}{\omega}, \quad (\text{A.0.3})$$

$$C_{OX2} = \frac{\left[\Im \left\{ \frac{1}{y_{22} + y_{21}} \right\} \right]^{-1}}{\omega}, \quad (\text{A.0.4})$$

$$R_{SUB1} = \Re \left\{ \frac{1}{y_{11} + y_{12}} \right\}, \quad (\text{A.0.5})$$

and

$$R_{SUB2} = \Re \left\{ \frac{1}{y_{22} + y_{21}} \right\}. \quad (\text{A.0.6})$$

The substrate network parameters for the double- π model can then be systematically determined as,

$$C_{OX11} = \frac{C_{OX1}}{2}, \quad (\text{A.0.7})$$

$$C_{OX22} = \frac{C_{OX2}}{2}, \quad (\text{A.0.8})$$

$$C_{OX12} = C_{OX11} + C_{OX22}, \quad (\text{A.0.9})$$

$$R_{SUB11} = 2 \cdot R_{SUB1}, \quad (\text{A.0.10})$$

$$R_{SUB22} = 2 \cdot R_{SUB2}, \quad (\text{A.0.11})$$

and

$$R_{SUB12} = 2R_{SUB1} \parallel 2R_{SUB2}. \quad (\text{A.0.12})$$

The substrate network capacitances C_{SUB11} , C_{SUB12} and C_{SUB22} may then be determined based on the dielectric relaxation time of the substrate and the corresponding substrate resistances as

$$R_{SUB_{ij}}C_{SUB_{ij}} = \epsilon_0\epsilon_r\rho_{si}. \quad (\text{A.0.13})$$

In (A.0.13), ϵ_0 is the permittivity of free space, ϵ_r is that of the substrate (i.e. 11.7 for silicon) and ρ_{si} is the substrate resistivity in $\Omega \cdot \text{m}$.

The port-to-port capacitance of the double- π model, C_P , is extracted from y_{12} beyond the self-resonance frequency (SRF) of the inductor where its effect is dominant as,

$$C_P = \frac{\Im\{-y_{12}\}}{\omega} \bigg|_{\omega \gg \omega_{SRF}}. \quad (\text{A.0.14})$$

Finally, the series inductance and resistance L and R_m can initially assume the extracted $L_{DC}/2$ and $R_{DC}/2$ values in (A.0.1) and (A.0.2), respectively, but need to be optimized along with the rest of the frequency dependent loss network parameters L_f , R_f to reach a broadband agreement between the double- π model and the inductor behaviour in simulations [108].

The parameter extraction procedure described above has been adopted to fit each oscillator tank inductor to a double- π model. The experimental work in [105] has shown that although the floating shield does not reduce the extracted substrate network resistors, it significantly increases its capacitance shunting current away from the substrate network resistors. As the frequency increases, this lowers the substrate losses. As such, the complete double- π model has been retained in this exercise. The fitted models were mutually coupled through the L inductance elements to investigate the potential EM coupling and its possible impact on the independent phase steering among the integrated LO-elements as discussed in Section 5.2.3.

Appendix B

Layout Views of the Fabricated Building Blocks

Figure B.1: A layout view of the two-stage RC-CR polyphase filter.

Figure B.2: A layout view of a phase interpolator cell.

Figure B.3: A layout view of the high-order synthesis block and the injection transconductor.

Figure B.4: A layout view of the negative- g_m LC-oscillator, the source-follower and FT-doubler buffer stages along with the T-coil and ESD structures.

Publications

The following is a list of articles containing various aspects of the work presented in this thesis:

Publications in Refereed Conference Proceedings

Y. Soliman and R. Mason, “Phase calibration techniques for injection-locking LO-path based phase-shifting phased-array architectures,” in *Radio and Wireless Symposium (RWS), 2012 IEEE*, pp. 415 – 418, 15-18 Jan. 2012.

Y. Soliman and R. Mason, “Results of active and passive isolation techniques for multiple K-band oscillators on silicon ICs,” in *Microwave Conference, 2011. APMC 2011. Asia Pacific*, pp. 339 – 342, 5-8 Dec. 2011.

Y. Soliman and R. Mason, “A frequency multiplication based LO phase shifting technique for phased-array architectures,” in *Radio and Wireless Symposium (RWS), 2010 IEEE*, pp. 88 – 91, 10-14 2010.

Y. Soliman and R. Mason, “A subharmonic injection-locking scheme for LO phase shifting phased-array architectures,” in *Microwave Conference, 2009. APMC 2009. Asia Pacific*, pp. 1731 –1734, 7-10 2009.

Publications in Refereed Journals

Y. Soliman and R. Mason, “Application of subharmonic injection-locking of LC-oscillators to LO-based phase shifting phased-array architectures,” *Microwave Theory and Techniques, IEEE Transactions on*, vol. 58, no. 12, pp. 3475 – 3484, Dec. 2010

Bibliography

- [1] H. Hashemi, X. Guan, A. Komijani, and A. Hajimiri, "A 24-GHz SiGe phased-array receiver-LO phase-shifting approach," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 53, pp. 614 –626, Feb. 2005.
- [2] A. Natarajan, A. Komijani, X. Guan, A. Babakhani, and A. Hajimiri, "A 77-GHz phased-array transceiver with on-chip antennas in silicon: Transmitter and local LO-path phase shifting," *Solid-State Circuits, IEEE Journal of*, vol. 41, pp. 2807 – 2819, Dec. 2006.
- [3] J. Buckwalter, A. Babakhani, A. Komijani, and A. Hajimiri, "An integrated subharmonic coupled-oscillator scheme for a 60-GHz phased-array transmitter," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 54, pp. 4271 –4280, Dec. 2006.
- [4] F. Bohn, H. Wang, A. Natarajan, S. Jeon, and A. Hajimiri, "Fully integrated frequency and phase generation for a 6-18 GHz tunable multi-band phased-array receiver in CMOS," in *Radio Frequency Integrated Circuits Symposium, 2008. RFIC 2008. IEEE*, pp. 439 –442, June 2008.
- [5] A. Natarajan, A. Komijani, and A. Hajimiri, "A fully integrated 24-GHz phased-array transmitter in CMOS," *Solid-State Circuits, IEEE Journal of*, vol. 40, pp. 2502 – 2514, Dec. 2005.
- [6] X. Zhang and A. Daryoush, "Full 360° phase shifting of injection-locked oscillators," *Microwave and Guided Wave Letters, IEEE*, vol. 3, pp. 14 –16, Jan 1993.
- [7] L. Zhang, B. Ciftcioglu, and H. Wu, "A 1 V, 1 mW, 4 GHz injection-locked oscillator for high-performance clocking," in *Custom Integrated Circuits Conference, 2007. CICC '07. IEEE*, pp. 309 –312, 16-19 2007.
- [8] X.-S. Zhou, X. Zhang, and A. Daryoush, "A new approach for a phase controlled self-oscillating mixer," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 45, pp. 196 –204, Feb 1997.
- [9] A. Petosa, "Antennas and Arrays." Course Notes, Carleton University, Ottawa, Canada, 2009.
- [10] C. A. Balanis, *Antenna Theory: Analysis and Design*. New York: John Wiley & Sons, Inc., second ed., 1997.

- [11] D. Parker and D. Zimmermann, "Phased arrays - part 1: theory and architectures," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 50, pp. 678–687, Mar. 2002.
- [12] D. Parker and D. Zimmermann, "Phased arrays-part II: implementations, applications, and future trends," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 50, pp. 688–698, Mar. 2002.
- [13] E. Laskin, M. Khanpour, S. Nicolson, A. Tomkins, P. Garcia, A. Cathelin, D. Belot, and S. Voinigescu, "Nanoscale cmos transceiver design in the 90-170 GHz range," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 57, pp. 3477–3490, Dec. 2009.
- [14] B. Jagannathan, M. Khater, F. Pagette, J.-S. Rieh, D. Angell, H. Chen, J. Florkey, F. Golan, D. Greenberg, R. Groves, S. Jeng, J. Johnson, E. Mengistu, K. Schonenberg, C. Schnabel, P. Smith, A. Stricker, D. Ahlgren, G. Freeman, K. Stein, and S. Subbanna, "Self-aligned SiGe NPN transistors with 285 GHz f_{MAX} and 207 GHz f_T in a manufacturable technology," *Electron Device Letters, IEEE*, vol. 23, pp. 258–260, May 2002.
- [15] P. Chevalier, B. Barbalat, M. Laurens, B. Vandelle, L. Rubaldo, B. Geynet, S. Voinigescu, T. Dickson, N. Zerounian, S. Chouteau, D. Dutartre, A. Monroy, F. Aniel, G. Dambrine, and A. Chantre, "High-speed SiGe BiCMOS technologies: 120-nm status and end-of-roadmap challenges," in *Silicon Monolithic Integrated Circuits in RF Systems, 2007 Topical Meeting on*, pp. 18–23, 10-12 2007.
- [16] S. Jeon, A. Babakhani, and A. Hajimiri, "Integrated phased arrays," in *Advanced millimeter-wave technologies : antennas, packaging and circuits* (D. Liu, B. Gaucher, U. Pfeiffer, and J. Grzyb, eds.), John Wiley & Sons Ltd, first ed., 2009.
- [17] A. K. Bhattacharyya, *Phased Array Antennas: Floquet Analysis, Synthesis, BFNs and Active Array Systems*. Hoboken, New Jersey: Wiley-Interscience, first ed., 2006.
- [18] D. Pozar, *Microwave Engineering*. New York: Wiley, second ed., 1998.
- [19] P. Rizzi, *Microwave Engineering: Passive Circuits*. Englewood Cliffs, New Jersey: Prentice Hall, first ed., 1987.
- [20] H. L. V. Trees, *Optimum Array Processing Part IV of Detection, Estimation, and Modulation Theory*. New York: Wiley-Interscience, first ed., 2002.
- [21] E. Bond, X. Li, S. Hagness, and B. Van Veen, "Microwave imaging via space-time beam-forming for early detection of breast cancer," vol. 3, pp. 2909 – 2912, 2002.
- [22] P. Turner, "Mini-annular phased array for limb hyperthermia," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 34, pp. 508 – 513, May. 1986.
- [23] M. Williamson, G. Athanasiadou, and A. Nix, "Investigating the effects of antenna directivity on wireless indoor communication at 60 GHz," vol. 2, pp. 635 – 639, Sep. 1997.
- [24] W. Stutzman, J. Reed, C. Dietrich, B.-K. Kim, and D. Sweeney, "Recent results from smart antenna experiments-base station and handheld terminals," pp. 139–142, 2000.

- [25] J. Winters, "Optimum combining in digital mobile radio with cochannel interference," *Selected Areas in Communications, IEEE Journal on*, vol. 2, no. 4, pp. 528–539, 1984.
- [26] L. Godara, "Application of antenna arrays to mobile communications. II. beam-forming and direction-of-arrival considerations," *Proceedings of the IEEE*, vol. 85, no. 8, pp. 1195–1245, 1997.
- [27] S. Haykin and M. Moher, *Modern Wireless Communications*. Upper Saddle River, New Jersey: Pearson Prentice Hall, 2005.
- [28] L. Godara, "Applications of antenna arrays to mobile communications. I. performance improvement, feasibility, and system considerations," *Proceedings of the IEEE*, vol. 85, no. 7, pp. 1031–1060, 1997.
- [29] S. Shahramian, Y. Baeyens, N. Kaneda, and Y.-K. Chen, "A 70-100 GHz direct-conversion transmitter and receiver phased array chipset demonstrating 10 Gb/s wireless link," *Solid-State Circuits, IEEE Journal of*, vol. 48, no. 5, pp. 1113–1125, 2013.
- [30] A. Valdes-Garcia, S. Nicolson, J.-W. Lai, A. Natarajan, P.-Y. Chen, S. Reynolds, J.-H. Zhan, D. Kam, D. Liu, and B. Floyd, "A fully integrated 16-element phased-array transmitter in sige bicmos for 60-GHz communications," *Solid-State Circuits, IEEE Journal of*, vol. 45, no. 12, pp. 2757–2773, 2010.
- [31] S. Emami, R. Wiser, E. Ali, M. Forbes, M. Gordon, X. Guan, S. Lo, P. McElwee, J. Parker, J. Tani, J. Gilbert, and C. Doan, "A 60 GHz CMOS phased-array transceiver pair for multi-Gb/s wireless communications," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2011 IEEE International*, pp. 164–166, 2011.
- [32] B. Razavi, *RF Microelectronics*. Upper Saddle River, NJ: Prentice Hall, Inc., first ed., 1997.
- [33] K. Hayashi and M. Muraguchi, "An MMIC active phase shifter using a variable resonant circuit," vol. 3, pp. 1573 –1576 vol.3, Jun. 1998.
- [34] Y. Ayasli, S. Miller, R. Mozzi, and L. Hanes, "Wide-band monolithic phase shifter," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 32, pp. 1710 – 1714, Dec. 1984.
- [35] F. Ellinger, R. Vogt, and W. Bachtold, "Ultracompact reflective-type phase shifter MMIC at C-band with 360° phase-control range for smart antenna combining," *Solid-State Circuits, IEEE Journal of*, vol. 37, pp. 481 –486, Apr. 2002.
- [36] P.-S. Wu, H.-Y. Chang, M.-D. Tsai, T.-W. Huang, and H. Wang, "New miniature 15-20-GHz continuous-phase/amplitude control MMICs using 0.18- μ m cmos technology," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 54, pp. 10 – 19, Jan. 2006.
- [37] D.-W. Kang, H. D. Lee, C.-H. Kim, and S. Hong, "Ku-band MMIC phase shifter using a parallel resonator with 0.18- μ m CMOS technology," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 54, pp. 294 –301, Jan. 2006.

- [38] D.-W. Kang and S. Hong, "A 4-bit CMOS phase shifter using distributed active switches," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 55, pp. 1476 –1483, Jul. 2007.
- [39] K.-J. Koh and G. Rebeiz, "0.13- μ m CMOS phase shifters for X-, Ku-, and K-band phased arrays," *Solid-State Circuits, IEEE Journal of*, vol. 42, pp. 2535 –2546, Nov. 2007.
- [40] A. Bhohe and P. Perini, "An overview of smart antenna technology for wireless communication," vol. 2, pp. 875 – 883, 2001.
- [41] T. Ohira, "Adaptive array antenna beamforming architectures as viewed by a microwave circuit designer," pp. 828 –833, 2000.
- [42] C. Sun, A. Hirata, T. Ohira, and N. Karmakar, "Fast beamforming of electronically steerable parasitic array radiator antennas: theory and experiment," *Antennas and Propagation, IEEE Transactions on*, vol. 52, pp. 1819 – 1832, Jul. 2004.
- [43] H. Shnitkin, "Injection locking of microwave solid-state oscillators," *Proceedings of the IEEE*, vol. 4, pp. 57 – 64, Jan. 1961.
- [44] B. C. Henderson and J. A. Cook, "Image-reject and single-sideband mixers," *Watkins-Johnson Tech-note*, vol. 12, May 1985.
- [45] X. Guan, H. Hashemi, and A. Hajimiri, "A fully integrated 24-GHz eight-element phased-array receiver in silicon," *Solid-State Circuits, IEEE Journal of*, vol. 39, pp. 2311 – 2320, Dec. 2004.
- [46] K. Stephan, "Inter-injection-locked oscillators for power combining and phased arrays," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 34, pp. 1017 – 1025, Oct 1986.
- [47] R. York and R. Compton, "Measurement and modelling of radiative coupling in oscillator arrays," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 41, pp. 438 –444, Mar 1993.
- [48] R. York, P. Liao, and J. Lynch, "Oscillator array dynamics with broadband N-port coupling networks," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 42, pp. 2040 – 2045, Nov 1994.
- [49] R. York and T. Itoh, "Injection- and phase-locking techniques for beam control," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 46, pp. 1920 –1929, Nov 1998.
- [50] P. Liao and R. York, "A varactor-tuned patch oscillator for active arrays," *Microwave and Guided Wave Letters, IEEE*, vol. 4, pp. 335 –337, Oct 1994.
- [51] H.-C. Chang, X. Cao, M. Vaughan, U. Mishra, and R. York, "Phase noise in externally injection-locked oscillator arrays," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 45, pp. 2035 –2042, Nov 1997.

- [52] K. Stephan and S.-L. Young, "Mode stability of radiation-coupled interinjection-locked oscillators for integrated phased arrays," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 36, pp. 921–924, May 1988.
- [53] J. Lynch and R. York, "Stability of mode locked states of coupled oscillator arrays," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on*, vol. 42, pp. 413–418, Aug 1995.
- [54] A. E. Siegman, *LASERS*. Sausalito, CA: University Science Books, first ed., 1986.
- [55] B. van der Pol, "The nonlinear theory of electric oscillations," *Proceedings of the Institute of Radio Engineers*, vol. 22, pp. 1051–1086, Sep. 1934.
- [56] R. Adler, "A study of locking phenomena in oscillators," *Proceedings of the IRE*, vol. 34, pp. 351–357, Jun. 1946.
- [57] N. Bogoliubov and Y. Mitropolsky, *Asymptotic methods in the theory of non-linear oscillations*. New York: Gordon and Breach Science Publishers, second ed., 1961.
- [58] C. Hayashi, *Nonlinear oscillations in physical systems*. New York: McGraw-Hill, second ed., 1964.
- [59] K. Kurokawa, "Some basic characteristics of broadband negative resistance oscillator circuits," *Bell System Technical Journal*, Aug. 1969.
- [60] K. Kurokawa, "Injection locking of microwave solid-state oscillators," *Proceedings of the IEEE*, vol. 61, pp. 1386–1410, oct. 1973.
- [61] J. Lynch, H. Chang, and R. York, "Coupled-oscillator arrays and scanning techniques," in *Active and Quasi-Optical Arrays for Solid-State Power Combining* (R. York and Z. Popović, eds.), John Wiley & Sons, Inc., first ed., 1997.
- [62] K. Kurokawa, "Developments of microwave oscillator theory," in *RF and microwave oscillator design* (M. Odyniec, ed.), Norwood, MA: Artech House, Inc., first ed., 2002.
- [63] R. Adler, "A study of locking phenomena in oscillators," *Proceedings of the IRE*, vol. 34, pp. 351–357, June 1946.
- [64] B. Razavi, "A study of injection locking and pulling in oscillators," *Solid-State Circuits, IEEE Journal of*, vol. 39, pp. 1415–1424, Sept. 2004.
- [65] F. M. Gardner, *Phaselock Techniques*. New Jersey: Wiley Interscience, third ed., 2005.
- [66] A. Blanchard, *Phase-locked loops: Application to coherent Receiver Design*. New York: John Wiley & Sons Inc., first ed., 1976.
- [67] H. Stover, "Theoretical explanation for the output spectra of unlocked driven oscillators," *Proceedings of the IEEE*, vol. 54, pp. 310–311, feb. 1966.
- [68] M. Armand, "On the output spectrum of unlocked driven oscillators," *Proceedings of the IEEE*, vol. 57, pp. 798–799, May 1969.

- [69] B. Thibaud, D. Barataud, M. Campovecchio, J. Nebus, S. Tranchant, P. Quentin, and D. Floriot, "CAD oriented design methods of frequency multipliers. application to a millimeterwave MMIC PHEMT tripler and a microwave HBT doubler," in *Microwave Symposium Digest, 1999 IEEE MTT-S International*, vol. 4, pp. 1747 – 1750, 1999.
- [70] H. Fudem and E. Niehenke, "Novel millimeter wave active MMIC triplers," in *Microwave Symposium Digest, 1998 IEEE MTT-S International*, vol. 2, pp. 387 – 390, Jun. 1998.
- [71] A. Boudiaf, D. Bachelet, and C. Rumelhard, "A high-efficiency and low-phase-noise 38-GHz pHEMT MMIC tripler," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 48, pp. 2546 – 2553, Dec. 2000.
- [72] S. Hackl, J. Bock, G. Ritzberger, M. Wurzer, H. Knapp, L. Treitinger, and A. Scholtz, "A 45 GHz SiGe active frequency multiplier," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2002 IEEE International*, vol. 1, pp. 82 – 447, Feb. 2002.
- [73] Y. Zheng and C. Saavedra, "A broadband CMOS frequency tripler using a third-harmonic enhanced technique," *Solid-State Circuits, IEEE Journal of*, vol. 42, pp. 2197 – 2203, Oct. 2007.
- [74] W. Chan and J. Long, "A 56 - 65 GHz injection-locked frequency tripler with quadrature outputs in 90-nm CMOS," *Solid-State Circuits, IEEE Journal of*, vol. 43, pp. 2739 – 2746, Dec. 2008.
- [75] M.-C. Chen and C.-Y. Wu, "Design and analysis of CMOS subharmonic injection-locked frequency triplers," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 56, no. 8, pp. 1869–1878, 2008.
- [76] H. Ahmed, C. DeVries, and R. Mason, "A digitally tuned 1.1 GHz subharmonic injection-locked VCO in 0.18 μm CMOS," in *Solid-State Circuits Conference, 2003. ESSCIRC '03. Proceedings of the 29th European*, pp. 81 – 84, 2003.
- [77] E. Camarago, *Design of FET Frequency Multipliers and Harmonic Oscillators*. Norwood, MA: Artech House Inc., first ed., 1998.
- [78] S. A. MAAS, *Nonlinear Microwave and RF Circuits*. Norwood, MA: Artech House Publishers, second ed., 2003.
- [79] S.-W. Tam, E. Socher, A. Wong, Y. Wang, L. D. Vu, and M.-C. Chang, "Simultaneous subharmonic injection-locked mm-wave frequency generators for multi-band communications in CMOS," in *Radio Frequency Integrated Circuits Symposium, 2008. RFIC 2008. IEEE*, pp. 131 – 134, April 2008.
- [80] J. Lee and H. Wang, "Study of subharmonically injection-locked PLLs," *Solid-State Circuits, IEEE Journal of*, vol. 44, pp. 1539 – 1553, May 2009.
- [81] Y. Soliman and R. Mason, "A frequency multiplication based LO phase shifting technique for phased-array architectures," in *Radio and Wireless Symposium (RWS), 2010 IEEE*, pp. 88 – 91, Jan. 2010.

- [82] E. A. Guillemin, *Theory of Linear Physical Systems*. New York: John Wiley & Sons, Inc., first ed., 1963.
- [83] H. Wang, S. Jeon, Y. jiu Wang, F. Bohn, A. Natarajan, A. Babakhani, and A. Hajimiri, "A tunable concurrent 6-to-18ghz phased-array system in CMOS," in *Microwave Symposium Digest, 2008 IEEE MTT-S International*, pp. 687 –690, Jun. 2008.
- [84] Y. Soliman and R. Mason, "A subharmonic injection-locking scheme for LO phase shifting phased-array architectures," in *Microwave Conference, 2009. APMC 2009. Asia Pacific*, pp. 1731 –1734, 7-10 Dec. 2009.
- [85] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. New York: Cambridge Univ. Press, second ed., 2004.
- [86] S. Galal, H. Ragaie, and M. Tawfik, "RC sequence asymmetric polyphase networks for RF integrated transceivers," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, vol. 47, pp. 18 –27, jan 2000.
- [87] J. Bulzacchelli, M. Meghelli, S. Rylov, W. Rhee, A. Rylyakov, H. Ainspan, B. Parker, M. Beakes, A. Chung, T. Beukema, P. Pepeljugoski, L. Shan, Y. Kwark, S. Gowda, and D. Friedman, "A 10-Gb/s 5-Tap DFE/4-Tap FFE transceiver in 90-nm CMOS technology," *Solid-State Circuits, IEEE Journal of*, vol. 41, pp. 2885 –2900, Dec. 2006.
- [88] T. Dickson, K. Yau, T. Chalvatzis, A. Mangan, E. Laskin, R. Beerkens, P. Westergaard, M. Tazlauanu, M.-T. Yang, and S. Voinigescu, "The invariance of characteristic current densities in nanoscale mosfets and its impact on algorithmic design methodologies and design porting of Si(Ge) (Bi)CMOS high-speed building blocks," *Solid-State Circuits, IEEE Journal of*, vol. 41, pp. 1830 –1845, Aug. 2006.
- [89] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*. New York: Oxford University Press, second ed., 2002.
- [90] P. Heydari and R. Mohanavelu, "Design of ultrahigh-speed low-voltage CMOS CML buffers and latches," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 12, pp. 1081 – 1093, Oct. 2004.
- [91] T. Chalvatzis, K. Yau, R. Aroca, P. Schvan, M.-T. Yang, and S. Voinigescu, "Low-voltage topologies for 40-Gb/s circuits in nanoscale CMOS," *Solid-State Circuits, IEEE Journal of*, vol. 42, pp. 1564 –1573, Jul. 2007.
- [92] S. Voinigescu, D. McPherson, F. Pera, S. Szilagyi, M. Tazlauanu, and H. Tran, "RF and millimeter-wave IC design in the nano-(Bi)CMOS era," in *Si-Based Semiconductor Components for RF Integrated Circuits* (W. Z. Cai, ed.), Transworld Research Network, first ed., 2006.
- [93] H. Darabi and A. Abidi, "Noise in RF-CMOS mixers: a simple physical model," *Solid-State Circuits, IEEE Journal of*, vol. 35, pp. 15 –25, Jan. 2000.
- [94] J. J. Rael, *Phase Noise in Oscillators*. PhD thesis, University of California, Los Angeles, 2007.

- [95] B. Razavi, *RF Microelectronics*. Upper Saddle River, NJ: Prentice Hall, Inc., second ed., 2011.
- [96] F. Ellinger, *Radio Frequency Integrated Circuits and Technologies*. New York: Springer, first ed., 2007.
- [97] W. P. Robins, *Phase Noise In Signal Sources (Theory and Applications)*. London, UK: Institution of Engineering and Technology, first ed., 1982.
- [98] S. Galal and B. Razavi, "Broadband ESD protection circuits in CMOS technology," *Solid-State Circuits, IEEE Journal of*, vol. 38, pp. 2334 – 2340, Dec. 2003.
- [99] B. Razavi, *Design of Integrated Circuits for Optical Communications*. New York: McGraw-Hill, first ed., 2003.
- [100] T. T. True, "Bridged-T termination network." US Patent 3155927, Nov. 1964.
- [101] S. Mohan, M. del Mar Hershenson, S. Boyd, and T. Lee, "Simple accurate expressions for planar spiral inductances," *Solid-State Circuits, IEEE Journal of*, vol. 34, no. 10, pp. 1419–1424, 1999.
- [102] H. Veenstra and M. Notten, "60GHz VCOs with transmission line resonator in a 0.25 μm SiGe BiCMOS technology," in *Radio Frequency Integrated Circuits Symposium, 2008. RFIC 2008. IEEE*, pp. 119 –122, Apr. 2008.
- [103] R. Amaya, P. Popplewell, M. Cloutier, and C. Plett, "EM and substrate coupling in silicon RFICs," *Solid-State Circuits, IEEE Journal of*, vol. 40, pp. 1968 – 1971, sept. 2005.
- [104] P. Park and C. Yue, "Modeling of triple-well isolation and the loading effects on circuits up to 50 GHz," in *Custom Integrated Circuits Conference, 2008. CICC 2008. IEEE*, pp. 217 –220, Sept. 2008.
- [105] T. Cheung and J. Long, "Shielded passive devices for silicon-based monolithic microwave and millimeter-wave integrated circuits," *Solid-State Circuits, IEEE Journal of*, vol. 41, pp. 1183 – 1200, May 2006.
- [106] B. M. Notaroš, *Electromagnetics*. Upper Saddle River, NJ: Pearson Education, Inc., first ed., 2011.
- [107] P. H. R. Popplewell, "Using Oscillator Gain and Injection-Locking to Measure On-Chip Inductor Coupling," Master's thesis, Carleton University, Ottawa, Ontario, Canada, 2004.
- [108] T. Dickson, M.-A. LaCroix, S. Boret, D. Gloria, R. Beerkens, and S. Voinigescu, "30-100-GHz inductors and transformers for millimeter-wave (Bi)CMOS integrated circuits," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 53, no. 1, pp. 123–133, 2005.
- [109] Y. Cao, R. Groves, X. Huang, N. Zamdmer, J.-O. Plouchart, R. Wachnik, T.-J. King, and C. Hu, "Frequency-independent equivalent-circuit model for on-chip spiral inductors," *Solid-State Circuits, IEEE Journal of*, vol. 38, no. 3, pp. 419–426, 2003.

- [110] Q. Gu, *RF System Design Of Transceivers For Wireless Communications*. New York, NY: Springer Science, Business Media Inc., first ed., 2005.
- [111] S. Patnaik, S. Kalia, B. Sadhu, M. Sturm, M. Elbadry, and R. Harjani, "An 8 GHz multi-beam spatio-spectral beamforming receiver using an all-passive discrete time analog base-band in 65 nm CMOS," in *Custom Integrated Circuits Conference (CICC), 2012 IEEE*, pp. 1–4, Sept.
- [112] W. Su, Z. Safar, and K. Liu, "Towards maximum achievable diversity in space, time, and frequency: performance analysis and code design," *Wireless Communications, IEEE Transactions on*, vol. 4, no. 4, pp. 1847–1857, 2005.
- [113] E. Akay and E. Ayanoglu, "Achieving full frequency and space diversity in wireless systems via BICM, OFDM, STBC, and viterbi decoding," *Communications, IEEE Transactions on*, vol. 54, no. 12, pp. 2164–2172, 2006.
- [114] Agilent Technologies, Inc., "Agilent E8247C/57C PSG CW and Analog Signal Generators Data Sheet," Feb. 2007.
- [115] M. Hossain and A. Carusone, "CMOS oscillators for clock distribution and injection-locked deskew," *Solid-State Circuits, IEEE Journal of*, vol. 44, Aug. 2009.
- [116] S. Jeon, Y.-J. Wang, H. Wang, F. Bohn, A. Natarajan, A. Babakhani, and A. Hajimiri, "A scalable 6-to-18 GHz concurrent dual-band quad-beam phased-array receiver in CMOS," *Solid-State Circuits, IEEE Journal of*, vol. 43, pp. 2660–2673, Dec. 2008.
- [117] H. Krishnaswamy and H. Hashemi, "A 4-channel 4-beam 24-to-26 GHz spatio-temporal RAKE radar transceiver in 90 nm CMOS for vehicular radar applications," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International*, pp. 214–215, Feb.
- [118] Y. Soliman and R. Mason, "Application of subharmonic injection-locking of LC-oscillators to LO-based phase shifting phased-array architectures," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 58, no. 12, pp. 3475–3484, 2010.
- [119] Y. Soliman and R. Mason, "Experimental results of active and passive isolation techniques for multiple K-Band LC-oscillators on silicon ICs," in *Microwave Conference, 2011. APMC 2011. Asia Pacific*, pp. 339–342, 5–8 Dec. 2011.
- [120] Y. Soliman and R. Mason, "Phase calibration techniques for injection-locking LO-path based phase-shifting phased-array architectures," in *Radio and Wireless Symposium (RWS), 2012 IEEE*, pp. 415–18, 15–18 Jan. 2012.
- [121] C. DeVries and R. Mason, "A 0.18 μm CMOS, high Q-enhanced bandpass filter with direct digital tuning," in *Custom Integrated Circuits Conference, 2002. Proceedings of the IEEE 2002*, pp. 279–282, 2002.
- [122] B. Grave, A. Frappe, and A. Kaiser, "A reconfigurable 60 GHz subsampling receiver architecture with embedded channel filtering," in *Circuits and Systems (ISCAS), 2012 IEEE International Symposium on*, pp. 1295–1298, 2012.

- [123] R. Mason, J. Fortier, and C. DeVries, “Complete SOC transceiver in $0.18\text{ }\mu\text{m}$ CMOS using Q-Enhanced filtering, sub-sampling and injection locking,” *Solid-State Circuits, IEEE Journal of*, vol. 47, pp. 1800–1809, Aug. 2012.