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EMITTER RESISTANCE AND CURRENT GAIN IN
POLYSILICON EMITTER TRANSISTORS

by

(C) Edward Patrick Keyes, B.Sc.

This thesis is submitted to the Faculty of Graduate
Studies and Research in partial fulfilment
of the requirements for the degree of

Master of Engineering

Department of Electronics
Faculty of Engineering
Carleton University
Ottawa, Canada
March, 1987

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Polysilicon Emitter Transistors"

submitted by Edward Patrick Keyes in partial fulfilment of the
requirements for the degree of Master of Engineering.

Prof. N. G. Tarr
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March, 1987

ABSTRACT

This research concerns a novel polysilicon emitter structure characterized by high emitter efficiencies and capable of producing bipolar transistors with gains in excess of 30,000. The emitter is fabricated from in-situ phosphorus doped polysilicon deposited by LPCVD. Emitter metallization problems are examined and an acceptable metallization scheme outlined. The effect on emitter efficiency of surface treatments, polysilicon thickness, deposition temperature, and a post deposition furnace anneal are examined.

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TABLE OF SYMBOLS

SYMBOL	DESCRIPTION	UNITS
α_R	reverse common base current gain	---
G_E	emitter Gummel number	s/cm^4
G_B	base Gummel number	s/cm^4
h_{FE}	forward current d.c. gain	---
J_C	collector current density	$amps/cm^2$
J_B	base current density	$amps/cm^2$
J_{BK}	emitter back injection current density	$amps/cm^2$
J_{oc}	collector saturation current density	$amps/cm^2$
J_{rev}	diode reverse leakage current density	$amps/cm^2$
k	Boltzmann's constant	$1.38 \times 10^{-23} J/K$
n_i	intrinsic carrier concentration	$1.1 \times 10^{10}/cm^3$
ρ	bulk resistivity	$ohm-cm$
ρ_c	contact resistivity	$ohm-cm^2$
ρ_e	specific emitter resistivity	$ohm-cm^2$
q	elementary charge	$1.6 \times 10^{-19} C$
R_{bi}	intrinsic base resistance	$ohms$
R_{bx}	extrinsic base resistance	$ohms$
R_e	static emitter resistance	$ohms$
T	absolute temperature	K
V_{BE}	base-emitter voltage	$volts$
V_{CB}	collector-base voltage	$volts$
V_T	thermal voltage	$25.9mV \text{ at } 300K$

CHAPTER 1: INTRODUCTION

1.1

BACKGROUND

The term "Polysilicon Emitter" is generally applied to several different bipolar transistor structures. Their common feature is the use of polysilicon to form at least part of the emitter.

In some structures [Nils80] an emitter is formed by ion implantation into the single crystal substrate. Polycrystalline silicon is deposited and furnace annealed to act as a contact to this monocrystalline emitter.

In another type of device [AsSo83] the polysilicon acts as a diffusion source for emitter formation. It is deposited over the emitter window and then furnace annealed at a temperature high enough to cause dopant diffusion into the substrate. A thin interfacial oxide layer is chemically grown over the emitter window prior to the polysilicon deposition. The presence of the oxide is not essential but has been demonstrated to increase the current gain.

In both the structures described above the polysilicon is deposited undoped and then doped by ion implantation. To prevent implant damage the implant energy is chosen so the impurity atoms come to rest within the polysilicon. A high temperature furnace anneal must be performed to uniformly dope the polysilicon. The drive-in has several unintentional side-effects including increased grain size, dopant segregation to the grain boundaries, possible

disruption of any thin interfacial oxide, epitaxial regrowth of the polysilicon and dopant diffusion into the single crystal substrate.

In a third type of structure developed at Carleton [RoTa85], in-situ doped polysilicon is deposited by Low Pressure Chemical Vapor Deposition (LPCVD) at a low enough temperature to prevent dopant diffusion into the single crystal base. The use of in-situ doped polysilicon makes the high temperature anneal unnecessary. In this type of "true" polysilicon emitter device the emitter is composed exclusively of polysilicon. This structure offers several fabrication advantages over diffused or implanted emitter structures. These include reduced thermal budget, precise control of the base width and doping profile and the elimination of anomalous diffusion effects such as emitter-collector pipes [Sze83].

A common feature of all polysilicon emitter structures is reduced minority carrier back-injection into the emitter compared to conventionally fabricated devices. This enhances the forward current gains (h_{FE}) and improves the bandwidth. Bandwidth can be further improved by trading the gain improvement for a heavier base doping and consequent lower base resistance. The back injection current (J_{BK}) can be described by a quantity known as the emitter Gummel number (G_E)

$$J_{BK} = (qn_i^2/G_E) \exp(qV_{BE}/kT) \quad (1.1)$$

Where V_{BE} is the base-emitter bias voltage. In a conventional emitter, G_E is related to the integrated emitter doping. G_E is analogous to the more familiar base Gummel number (G_B) which

determines the collector current density (J_C) through the relation:

$$J_C = (qn_i^2/G_B) \exp(qV_{BE}/kT) \quad (1.2)$$

In modern bipolar transistors the base current is dominated by J_{BK} . The static common emitter current gain (h_{FE}) can be expressed as:

$$h_{FE} = G_E/G_B \quad (1.3)$$

G_E is the appropriate figure of merit to measure emitter back injection performance rather than h_{FE} since a high gain device can be made by simply decreasing G_B without improving G_E .

Conventional bipolar transistors have G_E values of no greater than $5 \times 10^{13} \text{ s/cm}^4$ [GeGo83]. The use of polysilicon in the emitter has been shown to significantly increase G_E . Several authors have attempted to explain this improvement.

Neugroschel et. al. [NAK185] have suggested an explanation based on transport within the polysilicon. They postulate the existence of a very thin (less than 10 nm), highly disordered layer at the poly-single crystal interface characterized by a very low hole mobility which suppresses back injection.

Ning and Issac [Nils80] put forward a two region model of their device in which the gain improvement is based on a lower hole mobility in the bulk of the polysilicon. The polysilicon extends the length of the emitter while the low mobility retards the transport of injected carriers.

DeGraaf and DeGroot [DeDe79] explain the improved gains by the existence of an ultra thin oxide (less than 1 nm) at the interface. The hole current is limited by tunneling through the oxide while the electron current is limited by transport processes in the semiconductor [Gree74].

Patton et. al. [PaBP86] have suggested that dopant segregation to the interface during the polysilicon anneal creates a potential barrier to minority carrier transport which acts in conjunction with the oxide barrier.

None of the above theories can claim to completely explain the observed hole current suppression. In part this may be due to the several different types of emitter structures under investigation.

1.2

GOALS

This research investigated both the "true" and diffused polysilicon emitter structures. Of particular interest was the source of the high emitter resistance observed for the true structure by earlier workers [Rowl87]. The goal was to determine whether this resistance could be reduced or whether it was intrinsic to the true structure. An understanding of the high emitter efficiency was also sought, in particular the role of the interfacial oxide, the effects of annealing and whether the hole current suppression was an interface or bulk property.

Chapter 2 details the fabrication and geometry of the poly emitter transistors used. Chapter 3 investigates low resistance metal contacts to poly-single crystal junctions. Chapter 4 examines the problem of emitter resistance in the poly emitter structure. Chapter 5 looks at the effect of surface treatments, polysilicon thickness and furnace annealing on the emitter efficiency in an attempt to understand the phenomenon of high gains. Chapter 6 describes experiments with polysilicon films deposited amorphous and then recrystallized. Chapter 7 contains a summary of the research and recommendations for further research.

CHAPTER 2: DEVICE FABRICATION

2.1

TRANSISTOR STRUCTURE

A simplified diagram of the transistor structure used throughout the research is shown in figure 2.1.1. The n-type substrate acts as the collector. An extrinsic base region helps minimize the base resistance. The lightly doped intrinsic base is formed by ion implantation of $^{11}\text{B}^+$. The polysilicon emitter is deposited by LPCVD and wet etched. The low deposition temperature prevents dopant diffusion into the single crystal base. The base-emitter junction of a true poly emitter coincides with the poly-single crystal interface. Diffused poly emitters were also studied. In these devices a 900°C post deposition anneal causes dopant diffusion and creates a shallow single crystal emitter.

2.2

PROCESSING DETAILS

Considerable wafer to wafer variation in device characteristics was observed by earlier workers at Carleton [Rowl87], making comparisons between devices on different wafers untrustworthy. To circumvent this problem a special nine level mask set was created which allowed for two separate polysilicon depositions on the same wafer. Using this mask set devices with different surface treatments, polysilicon thicknesses and thermal treatments could be compared side by side. This eliminated spurious effects from wafer to wafer variation in the base, collector or metallization characteristics.

FIGURE 2.1.1: STRUCTURE OF A POLYSILICON EMITTER TRANSISTOR

FIGURE 2.1.2: TOP VIEW OF TRANSISTOR

The mask set contains transistors with emitter areas ranging from $5 \times 5 \mu\text{m}^2$ to $10 \times 175 \mu\text{m}^2$. A stripe geometry (figure 2.1.2) consisting of a single emitter stripe with two base stripes on either side was chosen. The clearance between the emitter and extrinsic base windows was varied from 0 to $5 \mu\text{m}$ to examine the importance of the resistance of the intrinsic base. Test structures to measure the intrinsic and extrinsic base sheet resistance, the polysilicon sheet resistance and the polysilicon to metal contact resistivity were also included.

The transistors were fabricated on 50 mm , 100 orientation, n-type silicon with a bulk resistivity of about 3.5 ohm-cm . The extrinsic base was formed by a heavy boron diffusion and drive in producing a junction depth of $2.3 \mu\text{m}$. The intrinsic base was formed by ion implantation of $^{11}\text{B}^+$. Implant doses and energies ranged from 10^{12} to $5 \times 10^{12} \text{ atoms/cm}^2$ and 30 keV to 100 keV respectively. Implant damage was removed by a 1 hr low temperature anneal at 650°C followed by a 30 min high temperature anneal at 1000°C . The polysilicon was deposited at a temperature of 627°C and a pressure of 0.4 torr by Low Pressure Chemical Vapour Deposition (LPCVD) from a 170:1 ratio of silane to phosphine and then wet etched to form the emitters. The chemical phosphorus concentration from SIMS (Secondary Ion Mass Spectroscopy) measurements is roughly $4 \times 10^{20} \text{ atoms/cm}^3$ although a large percentage of the dopant is not electrically active as deposited. Immediately prior to the deposition the wafers were flash dipped in 10% hydrofluoric acid (HF) to minimize the native oxide thickness in the emitter windows. Some devices were then chemically treated to deliberately regrow an

ultra thin oxide of about 1.5nm. A detailed outline of the process is contained in Appendix 1. Appendix 2 contains the processing details of individual wafers.

Devices were also fabricated with annealed polysilicon for comparison. The furnace anneal was carried out at 900°C for 30 min in N₂ ambient. Dopant diffusion from the polysilicon into the neutral base can completely destroy lightly doped devices. In our experiments devices with implant doses of less than 2×10^{12} atoms/cm² at 50 keV did not survive the anneal. This result highlights one of the advantages of the true structure. The base and emitter doping concentrations can be set independently allowing the creation of very lightly doped bases.

Devices implanted with 10^{12} atoms/cm² at 100 keV did survive the anneal; however, their base-collector junctions were ohmic rather than rectifying. This is attributed to implant damage caused by the high energy of the implant.

The double polysilicon deposition poses a processing problem in that the first poly deposition must be protected when the second deposition is patterned. Consequently, transistors formed during the first deposition have a polysilicon overlayer from the second deposition. This has important implications for the emitter resistance which will be discussed in chapter 4.

Base contacts were formed by vacuum evaporation of aluminum followed by sintering at 450°C in H₂ for 20min.

CHAPTER 3: METALLIZATIONS FOR A POLYSILICON JUNCTION

3.1

INTRODUCTION

A good quality emitter contact should be ohmic, of low contact resistivity (p_c) and not compromise the electrical properties of the underlying junction. In a commercial process the "target" resistivity of a metal contact is typically about 10^{-7} $\mu\text{Ohm-cm}^2$ [Sze83].

Forming good metal contacts to an unannealed polysilicon emitter is not a trivial exercise. The junction is shallow (the typical polysilicon thicknesses is 100 nm) and the polysilicon grain boundaries provide an easy path for diffusion of metal atoms to the interface. In addition, since a large percentage of the phosphorus in unannealed polysilicon is not electrically active, the surface carrier concentration is low, which generally leads to a high value of p_c [LeAn69].

A significant problem with early devices fabricated at Carleton was the large series resistance of the base-emitter junction. Aluminum, widely used in the semiconductor industry, diffuses rapidly along the polysilicon grain boundaries above about 375°C [FOSS79]. The standard post deposition, 450°C "sinter" will easily short a polysilicon junction. Accordingly, early devices fabricated at Carleton used thermally evaporated unsintered aluminum contacts [RoTa85]. It was suspected that this metallization could be quite resistive and therefore account for the observed poor current handling of the transistors [Rowl86]. Before examining the emitter resistance of the junction this type of contact and several alter-

natives were investigated.

Titanium is a promising contact material for polysilicon junctions. It is thermally stable in contact with silicon up to a temperature of 550°C [KaNa76]. It has the lowest barrier height among the noble and refractory metals (about 0.5eV for n^{+} silicon) [OtTu80]. It is an oxygen getter and will reduce native oxide on silicon. In addition titanium is the only refractory metal which can be evaporated by resistive heating, avoiding e-beam evaporation and the attendant radiation damage [TiCr82]. Ting and Crowder [TiCr82] report p_c values of between 0.36 and $2.2 \mu\text{Ohm-cm}^2$ for contacts to n^{+} single crystal silicon for doping levels between 1.9×10^{20} and 1.0×10^{20} atoms/cm³.

Titanium silicide (TiSi_2) was also investigated as a possible contacting technology. TiSi_2 has the lowest resistivity of all the refractory silicides [MRDF82] and is widely used in device fabrication. Ting and Crowder [TiCr82] report p_c values in the low 10^{-6} ohm-cm^2 for Al/TiN/ TiSi_2 /Si contacts.

Contacts to annealed polysilicon were also investigated. The anneal is known to electrically activate phosphorus and decrease the bulk resistivity by about an order of magnitude. It was suspected that there might be a similar effect on the contact resistance.

3.2

TEST STRUCTURES

A mask set containing a Van der Pauw cross to measure polysilicon sheet resistance and a four terminal Kelvin resistor to measure p_c was designed. Polysilicon thicknesses of between 200 nm and 300nm

were deposited onto thermally oxidized wafers at 627°C and 0.4 torr by LPCVD from a 170:1 mixture of silane and phosphine. The bulk resistivity of annealed and unannealed polysilicon was 10^{-3} ohm-cm and 10^{-2} ohm-cm respectively. The furnace anneal was done at 900°C for 30 min in N_2 . The polysilicon was patterned by wet etching and an insulating layer of SiO_2 deposited. Contact windows were opened in the oxide and followed by metal deposition and patterning. The metals were deposited by vacuum evaporation either thermally or by e-beam. The aluminum was wet etched in phosphoric acid and the titanium in a combination of nitric and hydrofluoric acid.

A detailed run sheet is contained in Appendix 3. It has been shown that the resolution of a Kelvin resistor depends on the size of the metal-diffusion contact opening and the sheet resistance of the substrate [LoSD85]. Using 10umx10um contact windows the minimum measurable values for our resistors were 2 $\mu\text{Ohm-cm}^2$ and 20 $\mu\text{Ohm-cm}^2$ for annealed and unannealed polysilicon respectively. #

Polysilicon diodes with areas ranging from 4×10^{-6} to 8×10^{-3} cm^2 were also fabricated to measure junction quality. Thermal oxide was grown on 2 ohm-cm p-type silicon wafers and windows etched. The wafers were RCA cleaned and flash dipped in 10% HF to remove the native oxide. A 100 nm thickness of polysilicon was deposited immediately using the deposition parameters described above. The backs of the wafers were metallized with aluminum to serve as the substrate contact. Front contacts were made using the metallizations outlined below. A detailed run sheet is contained in Appendix 4.

All measurements were taken with an HP4145 Semiconductor Parameter Analyzer. During the p_c measurements the metal contact was kept negative with respect to the polysilicon - corresponding to the bias polarity of an npn transistor in forward active operation.

3.3

RESULTS

Tables 3-1 and 3-2 summarize the results of the experiments.

(i) Aluminum/unannealed Polysilicon

As anticipated, unsintered aluminum contacts to unannealed polysilicon were of poor quality with non-ohmic behavior and p_c values of about 2000 uOhm-cm^2 . This behavior is attributed to the presence of a thin native oxide on the silicon surface. After sintering the contact became ohmic and p_c decreased to a value of 100 uOhm-cm^2 .

Figure 3.3.1 is a plot of the logarithm of current density (J) versus bias voltage (V) for an unannealed polysilicon diode of area $4 \times 10^{-6} \text{ cm}^2$ contacted with unsintered aluminum under forward bias. Series resistance causes the current density to depart from an exponential dependence on V at about 100 A/cm^2 . It is difficult to extract an emitter resistance from this structure because of the large resistance of the 300 um thick lightly doped substrate. Reverse leakage current (J_{rev}) was measured on the largest diodes (8×10^{-3}) to reduce surface leakage effects from the perimeter. An average value of around 20 nA/cm^2 was obtained.

Figure 3.3.1: I-V characteristic of an unannealed polysilicon-silicon diode of area 20umx20um.

The diode characteristics degraded sharply when the diodes were sintered. J_{rev} began to increase for sintering temperatures above 350°C. The junction was completely destroyed after a 20 min 400°C sinter, having a J_{rev} of 0.1 A/cm².

(ii) Aluminium/annealed Polysilicon

Unsintered aluminum contacts to annealed polysilicon exhibited similar non-ohmic behavior and large values of p_c . The sinter produced ohmic contacts and a considerable reduction in p_c , an order of magnitude below the value obtained above for sintered aluminum to unannealed polysilicon. The most likely explanation of the difference is increased surface carrier concentration due to the increased dopant activation in annealed polysilicon.

The reverse leakage for annealed polysilicon diodes was about 1 nA/cm², about a ~~factor~~ of ten less than for unannealed devices. This is attributed to the movement of the space charge region away from the interface during annealing. The trap density at the interface is almost certainly higher than in the bulk, resulting in higher recombination currents for unannealed devices.

Annealed polysilicon junctions contacted with aluminum were not damaged after sintering in contrast to the results for aluminum contacted unannealed polysilicon junctions. Finnetti et.al. [FOSS80] reported similar results for Al/n⁺ polysilicon contacts to shallow single crystal junctions.

Polysilicon grain size and structure is known to change during annealing from 30nm diameter columnar grains to equiaxial grains of

diameter from 100nm to 200nm [HKS83]. Learn and Nowicki [LeNo79] have shown that increased grain size retards material diffusion. They theorize that the lower relative volume of grain boundaries in annealed polysilicon would be expected to inhibit material transport and regrowth. Their experiments depended on TEM observations of the polysilicon surface and looked for regrowth and pitting. They did not fabricate junctions however and it seems doubtful that increased grain size could completely eliminate material transport.

The effect can also be explained by dopant diffusion across the interface during the polysilicon anneal, creating a shallow single crystal emitter. Bevel and stain measurements indicated that the junction was 0.25um below the interface. Severe degradation of shallow single crystal junctions by the inter-diffusion of Al-Si during sintering is well known [McCa70]. The interdiffusion is localized however, occurring at favorable weak spots. It seems likely that in the case of an annealed polysilicon junction the disordered polysilicon structure provides more favorable transport pathways for the metal atoms than the single crystal.

The effect of the sinter on hole current is unobservable using a diode since the bulk of the current is carried by electrons. The presence of aluminum at the interface will increase the hole recombination however. Transistors were fabricated from annealed polysilicon and contacted with unsintered aluminum. Figure 3.3.2 illustrates typical transistor characteristics before and after sintering. Collector current breaks at a higher value after the sinter indicating decreased resistance. The base current has

increased significantly however. H_{FE} decreased from 3000 to 1000.

iii) Titanium/unannealed Polysilicon

Unsintered titanium contacts to unannealed poly were ohmic, with lower resistivities than either sintered or unsintered aluminum to unannealed poly. Sintering of the titanium produced no improvement in p_c nor did it increase the reverse leakage current. Leakage current actually decreased due to hydrogen passivation of radiation damage from the e-beam metal evaporation. Diodes with polysilicon thicknesses as low as 20 nm were fabricated and sintered without observing any junction degradation. These results demonstrate conclusively that Ti is not mobile in polysilicon at 450°C.

(iv) Titanium/annealed Polysilicon

Titanium contacts to annealed polysilicon were also ohmic with an order of magnitude decrease in p_c over Ti/unannealed polysilicon. Again sintering did not change p_c or increase the leakage current. The improvement in p_c for annealed polysilicon is again attributed to increased surface carrier concentration. The value obtained compares reasonably well to those obtained by Ting and Crowder [TiCr82].

Figure 3.3.2: Gummel plot of Al contacted annealed polysilicon emitter before and after contact sinter. Note increase in base current at low bias showing junction penetration.

(v) Titanium Silicide

The results of the experiments with TiSi_2 are shown in table 3-2. Results for titanium are included for comparison. The quality of our silicide contacts proved to be worse than that of the unreacted metal. The contact resistance of the silicide to polysilicon (annealed and unannealed) was higher in both cases. The cause is almost certainly oxygen contamination. Oxide formation during silicide formation is a common problem [MFSL80], [WaAn86], [WHPS82].

In the first experiment, 100 nm of Ti was evaporated over a 300nm thickness of polysilicon and reacted at 650°C for 30 min in N_2 at atmospheric pressure. This procedure should result in the formation of about 50nm of silicide [WMT86]. A surface oxide layer was inadvertently grown over the titanium during this procedure. The oxide was removed by sputtering. The ρ_c values from this experiment were quite high, particularly the value for unannealed polysilicon ($3 \times 10^4 \text{ uOhm-cm}^2$). Subsequent silicidation was carried out in an LPCVD tube at reduced pressure using Ultra Pure nitrogen gas. This reduced the oxide thickness but did not eliminate it. The results from this experiment are in table 3.2. Wang and Anthony [WaAn86] report that oxygen concentrations as low as 10ppm in the furnace lead to high resistivity, non-homogeneous films. Our results indicate that it adversely affects contact resistance also.

TiSi_2 contacted diodes were tested before and after formation of the silicide. Only diodes made with unannealed polysilicon were fabricated. Initially a polysilicon thickness of 100 nm and a

titanium thickness of 200 nm was used. The diodes were sintered at 650°C for 30 min. After the sinter the diodes were no longer rectifying. This result cannot be explained by consumption of the polysilicon during silicidation. Formation of the silicide should only consume about 30nm of polysilicon.

Subsequent experiments were done at shorter sintering times (5 min) and reduced titanium thicknesses (20 nm). None of these experiments produced successful diodes. One possible explanation for the failure seems to be diffusion of titanium down the grain boundaries during sintering, resulting in spike-through of the junction. Although Ti is not mobile at 450°C it appears to be mobile at 650°C. Previous studies have reported rapid diffusion of titanium along the grain boundaries during silicide formation [NBFP86] at 850-900°C. TEM studies by Wong et. al. [WWM86] indicate that silicides formed at 800°C and 30min will penetrate a 300nm thickness of annealed polysilicon. It seems reasonable that unannealed polysilicon junctions should be even more susceptible to silicide penetration.

TABLE 3.1

CONTACT	POLYSILICON	p_c ($\mu\text{Ohms}/\text{cm}^2$)	J_{rev} nA/cm^2
unsintered Ti	unannealed poly	65	200
sintered Ti	unannealed poly	65	20
unsintered Ti	annealed poly	5	--
sintered Ti	annealed poly	5	--
unsintered Al	unannealed poly	2000-500 at $10\text{A}/\text{cm}^2$	10
sintered Al	unannealed poly	100	$0.1\text{A}/\text{cm}^2$
unsintered Al	annealed poly	2000-1000 at $10\text{A}/\text{cm}^2$	1
sintered Al	annealed poly	10	1

TABLE 3.2

CONTACT	POLYSILICON	p_c ($\mu\text{Ohms}/\text{cm}^2$)	J_{rev} nA/cm^2
Ti	unannealed poly	65	20
TiSi ₂	unannealed poly	120-80 at $10^3\text{A}/\text{cm}^2$	$10\text{mA}/\text{cm}^2$
Ti	annealed poly	5	--
TiSi ₂	annealed poly	50-10 at $10^3\text{A}/\text{cm}^2$	--

While titanium was the best contact material of those investigated, its high bulk resistivity (40 $\mu\text{Ohm-cm}$) implies a large emitter spreading resistance. For this reason a double metal aluminum/titanium emitter metallization scheme was used.

Several processing problems were encountered during the patterning of the emitter contacts. Initially the titanium and aluminum were deposited sequentially and patterned together. The titanium etch used readily attacks Al, however, and frequently caused open circuits in the aluminum base contacts between the contact and the probe pad. This occurred despite protection of the base contacts with photo-resist. Subsequently, patterning of the titanium layer before the aluminum deposition was tried. The aluminum deposition overlays both base and emitter contacts and will therefore repair any damage to them. This procedure resulted in an enormous increase in the apparent contact resistance however. The increase was caused by formation of a thin oxide on the titanium surface during patterning. Kelvin resistors fabricated with an Al/Ti/unannealed polysilicon structure, initially showed p_c values of 700 $\mu\text{Ohm-cm}^2$, in contrast to the previously stated value of 65 $\mu\text{Ohm-cm}^2$ for simple Ti/unannealed polysilicon. Low temperature (400°C, 20min) sintering of the resistors reduced p_c to 50 $\mu\text{Ohm-cm}^2$. The oxide barrier broke down electrically under an applied voltage of about 8V.

It has been reported by Ting and Crowder [TiCr82] that a 100nm thickness of Ti will act as a barrier to Al migration and protect shallow junctions from Al penetration for sinters at 400°C for 5hr or

450°C for 30 min, making a sinter of the Al/Ti contacts possible. Our experiments indicate that this is not the case and that diffusion of Al through a Ti barrier does occur. Figure 3.4.1 is a plot of collector and base current density versus base-emitter voltage for a 25 μm^2 unannealed poly emitter device with an Al/Ti emitter contact before and after sintering at 420°C for 20 min. The Ti thickness was 140nm. The increase in base current is clearly visible, demonstrating that Ti is an imperfect barrier to Al. The current gain decreased from 15,400 to 7,000. Figure 3.4.2 is the characteristic of a 100 μm^2 device showing complete degradation of the base emitter junction. Devices of this size and larger were completely degraded by the sinter, while the majority of 25 μm^2 devices survived reasonably intact. This indicates that Al migration through the barrier is localized, probably occurring at weak spots in the Ti film.

Sintering experiments were also done with annealed polysilicon transistors. Figure 3.4.3 shows the characteristic of a 1.75 $\times 10^3 \mu\text{m}^2$ annealed device with 140 nm of Ti before and after a 20min, 420°C sinter. The increase in base current in the low bias region is less pronounced than with unannealed polysilicon but does occur. In many instances there was no measurable increase in the base current for smaller area devices. The different result for annealed and unannealed devices agrees qualitatively with the previous sintering experiments involving aluminum contacts. It confirms that unannealed polysilicon junctions are much more easily damaged by sintering. Also of interest in Figure 3.4.3 is the large increase in current

Figure 3.4.1: Gummel plot of an Al/Ti contacted unannealed poly emitter before and after sintering. Gain decreased from 15,000 to 7000.

Figure 3.4.2: Gummel plot of an $10\mu\text{m} \times 10\mu\text{m}$ Al/Ti contacted unannealed polysilicon emitter showing complete degradation after sintering.

Figure 3.4.3 Gummel plot of Al/Ti contacted annealed poly emitter transistor before and after sintering showing slight increase in base current and large decrease in emitter resistance. Gummel number before sintering was 3×10^{14}

handling that occurs after the sinter, indicating breakdown of the thin metal oxide mentioned above.

The above results indicate that Ti is not a barrier to material transport of Al and Si. The unannealed poly emitter structure is an extremely sensitive detector of metal diffusion. This sensitivity probably accounts for the discrepancy with earlier results [TiCr82] which used an implanted emitter. The situation is similar to that reported for the Al/TiSi₂/Si system [TiWi83]. Although the Al/TiSi₂/Si system is thermally stable up to 550°C, material diffusion of Al and Si through the silicide takes place at temperatures as low as 400°C.

The above considerations led to the choice of titanium for both the base and emitter contacts. Both metals were thermally evaporated sequentially without breaking vacuum and patterned together. Titanium is known to make good ohmic contact to heavily doped p-type single crystal silicon [TiCr82]. The use of titanium for the base contact avoids the problem of over-etching and eliminates one processing step. It does however prevent a sinter of the base contacts. The contact windows are therefore cleared of oxide immediately prior to deposition using dilute hydrofluoric acid. Figure 3.4.4 is an example of the improvement in current handling of the final process over unsintered aluminum contacts. A 10x10um² poly emitter transistor originally contacted with unsintered aluminum was recontacted using the new process, resulting in an increase in collector current of almost two orders of magnitude.

Figure 3.4.4: Gummel plot of unannealed poly emitter contacted initially with unsintered Al and recontacted with Al/Ti. Note improved current handling. Gummel number of this device is 1×10^{14} .

Aluminum was an unsuitable contact to polysilicon junctions because of its high p_c when unsintered and junction penetration when furnace sintered. Rapid sintering remains to be investigated.

The problems of junction penetration and oxide formation also make $TiSi_2$ an unsuitable contact without recourse to more sophisticated preparation techniques such as cosputtering or rapid thermal annealing [NBFT86]. In addition $TiSi_2$ will not act as a diffusion barrier for aluminum [TiWi82], ruling out the use of aluminum as a low resistance overlayer.

Unannealed polysilicon junctions are much more susceptible to metal diffusion and junction penetration than annealed polysilicon junctions. This is attributed to the reduced grain boundary volume in annealed poly and the movement of the junction into the single crystal during annealing.

Of the materials investigated titanium was the best contact to an unannealed poly emitter. It requires an aluminum overlayer to reduce the spreading resistance however. The value of p_c is still quite large in comparison to typical commercial values however and will certainly compromise the use of unannealed polysilicon emitters in VLSI. A dopant activating anneal of the polysilicon appears to be essential for low resistance contacts. Contrary to reports elsewhere Ti is not a barrier to Al-Si interdiffusion at 400°C. This rules out a furnace sinter and requires sequential evaporation of Ti and Al without breaking vacuum to prevent oxide formation.

CHAPTER 4: EMITTER RESISTANCE

4.1

INTRODUCTION

To evaluate transistor performance, collector and base current densities were measured as a function of base-emitter voltage (V_{BE}). Fig 4-1.1 is a plot of the logarithm of J_C and J_B versus V_{BE} for an unannealed poly emitter device of emitter area $10 \times 10 \mu m^2$, frequently referred to as a "Gummel Plot". The important features of the plot are the vertical displacement between J_C and J_B , corresponding to the d.c. forward current gain (h_{FE}), and the point at which J_C starts to depart from a straight line indicating series resistance in the base-emitter junction or high level injection effects. J_C departs from an exponential dependence on V_{BE} at a current density of about $100 A/cm^2$ due to series resistance effects in the base-emitter junction. At about $1000 A/cm^2$ high current effects in the collector become noticeable. J_B continues to increase with an almost exponential dependence while J_C decreases sharply. For comparison a typical commercial device of similar geometry such as a National Semiconductor 2N3904 does not show series resistance effects until about $1000 A/cm^2$. Using the low resistance Al/Ti metallization the source of this resistance was investigated.

4.2

METHOD

The base geometry used in our devices is well known and was not expected to contribute significantly to the series resistance. Extrinsic base resistance R_{Bx} and intrinsic base resistance R_{Bi} were

Figure 4.1.1: Gummel plot of a true polysilicon emitter transistor. Upper line is collector current, lower is base current. Gummel number is $3 \times 10^{-4} \text{ s}/\text{cm}^4$, gain is 5000.

therefore not measured in a rigorous fashion.

The contribution to the series resistance from the lightly doped intrinsic base was assessed by comparing devices with no clearance between the emitter and the extrinsic base and devices with a 5 μm clearance. If the resistance of the intrinsic base is important, devices with zero clearance should have better current handling.

The effect of the extrinsic base contact was estimated using a device with two base contacts on either side of the emitter stripe. By comparing the characteristic with one and two base contacts the relative importance of R_{Bx} can be assessed.

Neither of the ~~two~~ above methods indicated that R_{Bi} and R_{Bx} were significant. Since the source of the high resistance was almost certainly the novel emitter structure, efforts were concentrated on accurate measurement of R_E .

Static emitter resistance (R_E) was measured using the open collector method [Giac72], [Getr78]. In this method the emitter-base junction is forward biased while the collector is kept open circuited. Emitter current density is plotted against collector-emitter voltage (V_{CE}). V_{CE} is related to J_E by the equation.

$$V_{CE} = V_T \ln(1/a_R) + R_E I_E \quad (4.2.1)$$

Where a_R is the reverse common base current gain and V_T is the thermal voltage (kT/q). R_E is equal to the inverse of the slope of the J_E - V_{CE} curve. Figure 4.2.1 illustrates the method used for a

commercial transistor, a National Semiconductor 2N3904. The low current "flyback" portion of the curve is caused by the decrease of the reverse beta at low currents. The value of R_E obtained was 0.99 ohms. To test the reliability of this method a 2.2 ohm resistor was placed in series with the emitter and R_E remeasured. The value obtained was 3.19 ohms, in excellent agreement with the first measurement. The device area was measured to be $5 \times 10^{-5} \text{ cm}^2$, giving an emitter resistivity of 50 uOhm-cm^2 .

An advantage of the open collector method is an immunity to high current effects in the collector in contrast to other R_E measurement methods. Ning and Tang [NiTa84] have proposed a method based on the measured deviation of base current from its ideal value. This method has several disadvantages however. It assumes an ideal $\exp(qV_{BE}/kT)$ dependence of base current on bias voltage which was not true for some of our devices. In addition, the method depends on high current effects to cause variation in h_{FE} while assuming that any deviation in J_B is due to series resistance only. It ignores variations in J_B caused by high current effects such as the Kirk effect and collector-base debiasing, both of which can significantly increase J_B .

Several different polysilicon emitter transistor structures were fabricated to determine the source of emitter resistance. A consequence of the double polysilicon mask set is that the first polysilicon deposition is overlaid by the second. Figure 4.2.2 shows the three types of device structures analysed. All had HF

Figure 4.2.1: Emitter resistance characteristic of a commercial transistor with and without a 2.2 ohm external resistor. Resistances are 0.99 and 3.19 ohms respectively.

TYPE A EMITTER

TYPE B EMITTER

TYPE C EMITTER

FIGURE 4.2.2: THREE TYPES OF EMITTER STRUCTURES

cleaned interfaces. Type A were made with unannealed polysilicon without an overlayer. Type B devices had furnace annealed polysilicon overlaid with unannealed and type C had furnace annealed polysilicon only. The anneal was done at 900°C in N_2 for 30min. These structures allowed contact resistance to the polysilicon and intrinsic emitter resistance to be separated.

4.3

RESULTS

In contrast to the results for the commercial device the J_E vs V_{CE} characteristics of the type A devices were not straight lines. Figure 4.3.1 is the J_E - V_{CE} characteristic for the $100\text{ }\mu\text{m}^2$ device shown in figure 4.1.1. V_{CE} is proportional to the square root of current. This implies that R_E is proportional to the inverse of the square root of the emitter current. The slope of the curve at the V_{CE} intercept is very nearly zero indicating that R_E is initially quite high. This is reflected in figure 4.3.2, a plot of extracted resistivity versus J_E . Emitter resistivity was extracted using the formula

$$p_e = (V_{CE} - V_T \ln(1/a_R)) / J_E^E \quad (4.3.1)$$

The numerator of equation 4.2.1 is equal to the voltage drop across the emitter. The value of $V_T \ln(1/a_R)$ is taken to be the intercept of the curve with the V_{CE} axis. Variation in the reverse beta causes this quantity to change however the variation was measured to be less than 10 mV and is therefore not significant. Figure 4.3.3 compares the measured I_C - V_{CE} characteristic and one calculated by plotting the expected deviation from the ideal charact-

Figure 4.3.1: non-ohmic emitter characteristic of a $10\mu\text{m} \times 10\mu\text{m}$ type A transistor.

Figure 4.3.2: Emitter resistivity versus current for a 10umx10um type A poly emitter.

Figure 4.3.3: Measured and calculated (+) J_C - V_{CE} characteristic.

eristic based on the measured emitter voltage drop. Devices of all sizes showed similar characteristics. Figure 4.3.4 shows the characteristics for two devices from the same die, one of area $100\mu\text{m}^2$ and one of $1,750\mu\text{m}^2$. They have nearly identical J_C dependences illustrating that resistance scales with emitter area and is not a spreading resistance. Sintering of the Al/Ti contacts produced no change in emitter resistance (see figure 3.4.1) which further illustrates that R_E is not dominated by the metal contact.

Emitter resistivity was dependent on the particular polysilicon deposition with devices from the same deposition having similar resistivities. The resistivity at 500 A/cm^2 varied from 100 to $600\text{ }\mu\text{Ohm-cm}^2$ corresponding to voltage drops of between 50 and 300mV. The J_E - V_{CE} characteristics of the lowest resistivity devices were almost linear.

Type B devices showed improved current handling and a fairly ohmic emitter resistance. Figure 4.3.5 is a typical characteristic for a $25\mu\text{m}^2$ device. The slope of the line gives a value of about $35\text{ }\mu\text{Ohm-cm}^2$, quite close to contact resistance of Ti/unannealed polysilicon. This suggests that the contact resistance to the unannealed polysilicon overlayer dominates R_E and that the intrinsic emitter resistance of an annealed device is less than $35\text{ }\mu\text{Ohm-cm}^2$. In larger devices emitter resistivity was not constant but increased, further suggesting that parasitic effects dominate.

Type C devices exhibited the lowest emitter resistance.

Figure 4.3.4: Gummel plot comparison of 10µm x 10µm and 10µm x 175µm true poly emitter transistors.

Figure 4.3.5: Emitter characteristic of a $10\mu\text{m} \times 10\mu\text{m}$ type B transistor. Resistance is $33 \mu\text{ohm cm}^2$.

Figure 4.3.6 is a typical J_E versus V_{CE} characteristic. It is qualitatively similar to the characteristic for a type A device however the current values are much greater. This is reflected in the extracted values of ρ_e shown in figure 4.3.7. The initial value of ρ_e is roughly $16 \mu\text{Ohm-cm}^2$ and decreases to a minimum value of about $8 \mu\text{Ohm-cm}^2$. This is quite close to the limiting value of contact resistivity for Ti/annealed poly, suggesting that contact resistance will prevent much more of a decrease. Figure 4.3.8 is a Gummel plot of a $25\mu\text{m}^2$ type C device showing J_C and J_B as a function of the forward bias voltage. The sharp kink in J_C at 1000A/cm^2 and the exponential dependence of J_C below this value indicate that high current effects in the collector rather than emitter resistance is limiting current handling. This device is capable of sourcing 10^5A/cm^2 at 1.3 V forward bias.

4.4

ANALYSIS

The emitter resistance of the unannealed polysilicon devices is clearly limited by a non-ohmic resistance intrinsic to the poly emitter structure. The observed inverse square root dependence of R_E on J_E is characteristic of a tunnelling barrier [Wein82]. The presence of a thin tunneling barrier at the interface has been proposed by several authors [RiSA84], [DeDe79], [PaBP86]. Ricco et.al. [RiSA84] have suggested that the barrier is a thin "native" oxide which forms in the time between etching of the interface and deposition of the polysilicon. Patton et.al. [PaBP86] report the existence of a thin (less than 1nm) oxide at the interface of their,

Figure 4.3.6: Emitter resistance characteristic of a 5umx5um type C emitter.

Figure 4.3.7: Emitter resistivity versus current for $5\mu\text{m} \times 5\mu\text{m}$ type C emitter.

Figure 4.3.8: Gummel plot of type C emitter, Gain is 1000, J_{ec} is 133pA, Gummel number is 3×10^{-4} .

devices containing significant amounts of carbon. Our results support the existence of a tunneling oxide. The observed variation in emitter resistance from deposition to deposition suggests that the oxide growth is dependent on parameters beyond the control of the process such as oxygen contamination in the deposition furnace. The drastically lower emitter resistance after annealing suggests considerable disruption of the barrier and that carrier transport may be a mixture of tunneling and ohmic conduction. Patton et.al. [PaBP86] report that a high temperature anneal can cause disruption of the oxide and epitaxial regrowth of the polysilicon. The onset of disruption is a function of dopant concentration. Using arsenic doped polysilicon they report that a 900°C, 1hr anneal of polysilicon with a dopant concentration of 5×10^{20} will disrupt the oxide. The same anneal did not cause disruption for a dopant concentration of 2×10^{20} . Our use of phosphorus makes a direct comparison difficult, however, in view of the sharp reduction in resistance it seems likely that the oxide has been disrupted.

Ricco et.al. [RiSA84] suggest that the layer consists of oxidized silicon and propose the following approximate relationship between the majority carrier tunneling current J and the voltage across the barrier V :

$$J = \frac{q v_P C^2}{2 k T \epsilon_{Si}} V^2 \quad (4.4.1)$$

where v_P is the thermal electron velocity, P the tunneling probability, C the capacitance of the oxide layer, T the absolute temperature and ϵ_{Si} the dielectric constant of silicon. Using a

barrier height of 3eV for SiO₂ and thermal electron velocity of

$$v = (kT/m)^{1/2} \quad (4.4.2)$$

where m is the electron mass leads to a calculated oxide thickness of 0.9nm for the device shown in figure 4.1.1. This agrees with the Transmission Electron Microscope (TEM) results of Patton et.al. [PaBP86] who report a thickness less than or equal to 1.0 nm.

4.5

CONCLUSIONS

True polysilicon emitters suffer from a large non-ohmic emitter resistance probably caused by the presence of a thin (about 1 nm) unintentional oxide at the poly-monocrystal interface. This resistance severely limits the applicability of this emitter structure for VLSI. Emitter resistance is greatly reduced by a 900°C anneal, suggesting disruption of the oxide. The emitter resistance of the annealed devices is close to current bipolar VLSI values of 1 $\mu\text{Ohm}/\text{cm}^2$ [PBCE86] and is probably limited by metal contact resistance. An improved contact technology such as PtSi might therefore further improve performance.

CHAPTER 5: EMITTER EFFICIENCY

5.1

INTRODUCTION

As mentioned in chapter 1 the appropriate figure of merit for the back injection performance of a polysilicon emitter device is the emitter Gummel number (G_E) which is related to the back injection hole current J_{BK} by the relation.

$$J_{BK} = qn_i^2 \exp(qV_{BE}/kT)/G_E \quad (5-1)$$

The base current J_B is the sum of the back injection current and the recombination currents. A lower limit on G_E can be obtained by neglecting recombination and assuming the base current is due entirely to back injection. Therefore

$$J_B = qn_i^2 \exp(qV_{BE}/kT)/G_E \quad (5-2)$$

G_E can be obtained from the current gain h_{FE} and the collector saturation current density J_{oc} .

$$\text{Since } h_{FE} = J_C/J_B \quad (5-2)$$

$$\text{and } J_C = J_{oc} \exp(qV_{BE}/kT) \quad (5-3)$$

$$\text{then } G_E = qn_i^2 h_{FE}/J_{oc} \quad (5-4)$$

Measurement of J_{oc} is complicated for devices with lightly doped bases by base width modulation from the forward bias of the base-emitter junction. Under forward bias the base-emitter depletion region decreases in size, increasing the neutral base width. This

causes G_B to increase with applied forward bias and gives the $\log(J_C)$ versus V_{BE} line a slope of less than q/kT . This base "push-up" effect is most noticeable on devices with lightly doped bases. Figure 5.1.1 is a Gummel plot of a lightly doped base device showing the discrepancy between the ideal and actual dependence of J_C with 0 and 1 volts reverse bias on the collector base junction. The discrepancy is more pronounced with the larger value of V_{CB} since the base is narrower. To correctly calculate G_E from eqn 5-4 the correct value of J_{oc} must be used. J_{oc} must be measured by linearly extrapolating back to $V_{BE} = 0V$ from the point on the J_C curve at which h_{FE} is measured, using a slope of q/kT .

The measurement temperature for values quoted is $22^\circ C \pm 1.0^\circ C$. The value of temperature is quite important since a variation of 1.0K can cause a 20% change in J_{oc} . Another source of error in J_{oc} is the voltage drop across the emitter resistance. This reduces J_C and results in an underestimate of J_{oc} . A 10mV voltage drop will cause a 32% error in J_{oc} . Unannealed polysilicon emitter devices with large values of resistance are particularly susceptible to this problem.

5.2

TRUE POLYSILICON EMITTERS

A large variation in the G_E of devices formed with unannealed polysilicon deposited on HF cleaned interfaces was observed. Device characteristics were heavily dependent on the particular polysilicon deposition. Adjacent devices from different depositions exhibited drastically different characteristics while devices on different wafers but the same deposition were similar. Considerable

Figure 5.1.1: Base "push-up" in a transistor with a lightly doped base for a collector-base reverse bias of 1.0 V and 0.0 V. Straight line represents the ideal collector current slope.

across-the-wafer variation in G_E was noticeable in some cases also. G_E values ranged from below 10^{13} s/cm⁴ on poor depositions up to values in excess of 10^{15} s/cm⁴ for good depositions. The J_{oc} of these devices was measured by linear extrapolation to zero forward bias from a J_C value of 1 A/cm² on the $\log(J_C)$ curve to avoid the effect of the emitter resistance drop. The $\log(J_B)$ curves of some devices had slopes of value much less than q/kT indicating almost total suppression of the back injection current (figure 5.2.1). The low value of slope indicates that recombination in the depletion region is the most significant component of base current. In these devices J_C increases faster than J_B and gain is not constant but increases with forward bias. The G_E values quoted are calculated using the maximum h_{FE} . This still results in an underestimate of G_E since it partly neglects base push-up.

No correlation was observed between emitter resistance and G_E . Figure 5.2.2 illustrates the characteristics of two devices taken from the same wafer. Their collector currents are nearly identical indicating identical emitter resistance while the magnitudes of their base currents differ by almost two orders. In addition devices with low values of R_E and straight J_E - V_{CE} characteristics, had G_E values of greater than 10^{15} .

This large variation in G_E values for the unannealed poly emitter device cannot be explained at this time. As-deposited polysilicon is known to have an irregular structure consisting of small columnar grains. Neugroschel et.al. [NAKI85] have suggested the

Figure 5.2.1: Super beta true polysilicon emitter, transistor with gain of a maximum gain of 38,000. Note non-ideal base current. Gummel number is $3 \times 10^{-4} s/cm^4$.

Figure 5.2.2: Schematic plot of two HF cleaned true poly emitter transistors showing absence of correlation between emitter resistance and efficiency.

existence of a thin disordered layer at the interface characterized by a low hole mobility. They suggest that this layer could act as a hole barrier and would explain the low minority carrier injection. The poor reproducibility of good G_E values is consistent with this type of mechanism. Poor reproducibility is also consistent with an explanation based on the irregular growth of an ultra thin interfacial oxide as suggested by DeGraff et.al. [DeDe79]. In this model the oxide act as a tunnelling barrier and performance is analogous to an MIS (Metal-Insulator-Semiconductor) tunnel junction. The emitter resistance measurements of chapter 4 support the existence of a tunneling barrier and high resolution Transmission Electron Microscope (TEM) results [PaBP86] confirm its existence. The absence of any correlation between emitter resistance and G_E however, tends to suggest that the interfacial oxide cannot be the only factor in suppressing minority carrier injection, if it is important at all.

It should be noted that G_E values in excess of 10^{15} s/cm^4 are exceptionally high and have never before been reported for a silicon emitter. The only similar values are those reported for MIS or SIPOS emitter structures [MoGG86], [YaGm85]. When combined with a lightly doped base, gains in excess of 30,000 have been achieved. The device in figure 5.2.1 has a peak gain of 38,000. Figure 5.2.3 illustrates the I-V characteristics of this device. The lightly doped base punches through at about 8V. The Early voltage is 18V.

Figure 5.2.3: I-V characteristic of a super beta device. Early voltage is 18V, base current increment is 10nA.

Transistors were also fabricated from polysilicon which was furnace annealed at 900°C for 30 min in N_2 after deposition onto an HF cleaned interface. These devices showed far less variation in G_E and no marked dependence on the particular deposition. Annealed devices fabricated from the same polysilicon deposition as "poor" unannealed devices were no different than those fabricated from "good" depositions. The G_E values were quite uniform across the wafer and from run to run, averaging $3.0 \times 10^{14} \text{ s/cm}^4$. Annealed polysilicon devices could only be fabricated on wafers with heavy base implants ($5 \times 10^{12} \text{ atoms/cm}^2$) because of dopant diffusion during the anneal. Comparisons between annealed and unannealed devices on the same wafers showed consistently higher minority carrier back injection in the annealed devices.

The uniformity of annealed devices regardless of deposition suggests a reordering of the interface during annealing. Poor depositions seem to be enhanced by the anneal while good depositions are degraded. The emitter resistance results of chapter 4 indicate that the interfacial oxide is disrupted by the anneal. TEM studies of the interface [PaBP86] support the idea of a reordering. They show that epitaxial realignment of the polysilicon with the substrate occurs when the oxide is disrupted. Patton et. al. [PaBP86] also suggest that dopant segregation to the interface occurs during annealing and is necessary to passivate dangling bonds at the interface and reduce the trap density. If the low G_E values seen in some depositions are the result of a low dopant concentration at the

interface this would explain the improvement from annealing.

5.4

THIN POLYSILICON EMITTERS

Decreasing the emitter thickness in a conventional device results in increased hole current. The presence of the ohmic contact increases the minority carrier gradient and hence increases the diffusion current. This effect only becomes noticeable when emitter thickness is comparable to carrier diffusion length.

A weak dependence of hole current on polysilicon thickness has been reported in the literature [Nils80], [PaBP86]. Ning and Issac reported an increase in hole current for thicknesses of less than 100nm. More recently Patton et. al. reported similar results for some annealing conditions but not for others.

Unannealed HF cleaned emitters of thickness 25nm were fabricated and compared to 100nm thick emitters. There was no significant difference between thin unannealed devices and thick unannealed devices in terms of their Gummel numbers or resistances. G_E values of $7 \times 10^{14} \text{ s/cm}^4$ were recorded for the thin devices. The large variation in G_E values across the wafer seen with thick devices was also observed for thin ones.

Thin annealed devices were also fabricated. These devices were qualitatively similar to thick annealed devices however their G_E values were lower than the thick values by about a third, being about $1.2 \times 10^{14} \text{ s/cm}^4$. The emitter resistance was also about three times larger, being about $20 \mu\text{Ohm-cm}^2$. In addition there was less dopant diffusion into the base than with thick annealed devices. The

value of J_{oc} for the thin annealed devices was 50pA/cm^2 versus 100pA/cm^2 for thick annealed devices with identical base implants of 5×10^{17} atoms/cm².

The absence of any change in G_E for thin unannealed devices indicates the minority carrier concentration 25nm from the interface is at or close to equilibrium. It implies that the high emitter efficiency is an interface rather than a bulk effect.

The smaller G_E values of thin annealed devices indicate that hole current is no longer limited by the interface but rather by recombination at the metal contact. Dopant depletion of the emitter during annealing cannot explain the reduced G_E values. Simulations using SUPREM II indicate that the dopant concentration in the emitter after annealing is still above 5×10^{19} cm³. This suggests that the interfacial hole barrier is somewhat degraded by the anneal. This is consistent with the absence of very high G_E (above 10^{15} s/cm⁴) for thick annealed devices noted in section 5.3.

5.5

DELIBERATELY OXIDIZED INTERFACES

The role of the interfacial oxide in polysilicon emitter devices was investigated by deliberately oxidizing the interface and comparing to HF cleaned devices on the same wafer.

Ashburn and Soerowirdjo have shown that deliberately oxidizing the poly-single crystal interface prior to deposition of the polysilicon enhances gain [AsSo83], [AsSo84], lending support to the tunneling barrier theory. In their process the emitter windows are

first cleared of oxide using buffered hydrofluoric acid (HF) and then chemically oxidized using an RCA clean. Their process involves polysilicon doped by ion implantation and therefore requires an anneal.

It was our intention to see how a deliberately grown oxide would affect the performance of our devices. Previous workers have been unable to measure device characteristics before the polysilicon anneal since the polysilicon was deposited undoped. Using in-situ doped polysilicon it was possible for the first time to measure the characteristics of a deliberately oxidized device which had not been annealed and to precisely see the effect of the anneal.

Two oxidation techniques were investigated. The first involved a thermal oxidation at 500°C in dry O_2 for 30 min. The second oxidation was done chemically following the recipe given by Duffill and involved treatment with a 1:1:6 solution of $\text{HCl}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ at 80°C for 10 min which results in the formation of 1.0 to 1.5 nm of oxide. [Duff82]

Preliminary experiments were done using polysilicon diodes to avoid the lengthy processing involved in transistor fabrication. The diodes cannot show the effect of the oxide on the hole current but they can indicate the presence of oxide series resistance and recombination generation currents. The diodes were fabricated in a similar fashion to those used in the metallization experiments.

Figure 5.5.1 is a $\log(J)$ versus voltage plot of the forward

Figure 5.5.1: I-V characteristics of three polysilicon diodes given different surface treatments. A=HF cleaned, B=chemical oxidation, C=thermal oxidation.

characteristics of three diodes given different surface treatments prior to polysilicon deposition. The HF cleaned diode has an almost ideal characteristic over seven decades of current. The presence of series resistance in the junction is indicated by the departure from a linear relationship at 20A/cm^2 . It is difficult to extract an accurate emitter resistance from this structure because of the large contribution from the 300 μm thick lightly doped substrate. The chemically oxidized diode has increased current at low forward bias indicating increased depletion layer recombination. In addition the characteristic breaks from a straight line at a current density of about 2A/cm^2 indicating increased series resistance. The thermally oxidized diode shows an enormously increased series resistance breaking at about $2 \times 10^{-2} \text{ A/cm}^2$ and even more recombination current. For this reason only chemical oxidation was used in the transistor experiments.

Transistors were fabricated and comparisons made between deliberately oxidized and HF cleaned devices on the same wafer. Annealed and unannealed devices were fabricated. Figure 5.5.2 is a Gummel plot for an unannealed deliberately oxidized device and the HF cleaned counterpart. The severe degradation in performance is obvious. The oxide increases emitter resistance to greater than 10^4 uOhm-cm^2 and increases the hole current. The G_E of this device is $0.5 \times 10^{12} \text{ s/cm}^4$ and H_{FE} is less than 20. The HF cleaned counterpart on same die had a gain of 34,000 and a G_E of $8 \times 10^{14} \text{ s/cm}^4$. This result contradicts the tunneling barrier theory since a thicker oxide would be expected to increase emitter efficiency.

Figure 5.5.2: Gummel plot comparison between HF cleaned and chemically oxidized true poly emitters. Gummel number of HF device is 8×10^{14} , gain is 34,000. Gummel number of oxidized device is $.5 \times 10^{12}$

✓
The performance of the annealed oxidized devices was quite different. Figure 5.5.3 is a typical result comparing two side-by-side annealed devices, one with an oxidized surface and one without. The hole current of the oxidized device is clearly lower. The J_C curves break at about the same value indicating no substantial difference in emitter resistance. The G_E values of the oxidized devices were between 7.5 and 8.0×10^{14} s/cm⁴ while the unoxidized devices had values of 2.5 to 3.0×10^{14} s/cm⁴. This result agrees with Ashburn et. al. [AsSo83], [AsSo84] who reported an increase in emitter efficiency for deliberately oxidized diffused emitters. Figure 5.5.4 is the emitter resistance characteristic of the two devices. The oxidized device has a slightly higher initial value of p_e , however it quickly decreases to the same value as its HF cleaned counterpart.

The emitter resistance results suggest that the deliberate oxide is disrupted by the 900°C anneal in much the same fashion as the thin oxide formed unintentionally on HF cleaned devices. This implies that there is no tunneling barrier and requires another explanation of the hole current suppression. A thick deliberate oxide would be expected to retard the reordering of the interface. Bravman et.al. [BrPP85] have conducted XTEM studies of the morphology of the interface after a 1000°C anneal. They report that HF cleaned interfaces showed regions of epitaxial realignment an order of magnitude greater than for deliberately oxidized samples. If the decrease in G_E after annealing is due to reordering then this would explain the larger G_E values of deliberately oxidized samples.

Figure 5.5.3: Gummel plot comparison of chemically oxidized (A) and HF cleaned (B) annealed poly emitter transistors. Note decreased base current of oxidized device.

Figure 5.5.4: Comparison of emitter characteristics of HF cleaned and deliberately oxidized transistors.

The oxide tunneling theory of minority carrier suppressions disagrees with our results. There was no correlation between R_E and G_E for HF cleaned unannealed devices. Devices with high G_E values would be expected to have thicker oxides and therefore larger values of R_E . Thick oxides produced by chemical oxidation increased rather than decreased base current in unannealed emitters. Furthermore, annealed polysilicon devices had high G_E values despite emitter resistance results which suggest that the interfacial oxide is disrupted by annealing. An improvement in G_E was measured for deliberately oxidized annealed devices however no increase in emitter resistance was observed. This suggests that deliberate oxides are disrupted by annealing in the same manner as the native oxide. It implies that the back injection improvement of the deliberately oxidized devices cannot be due to an increased tunneling barrier but must be due to other factors.

Neugroschel's [NAK185] theory of a thin disordered region of low hole mobility near the interface could explain our results however high resolution TEM studies [BrPP85], [VASB82] show no evidence of the existence of this region.

It seems clear that a reordering of the interface takes place during annealing. The decrease in G_E from annealing seems connected with this reordering. The back injection improvement of chemically oxidized devices could be due to reduced realignment of the polysilicon with the interface. Quantum reflection of hole waves at the interface is one possible explanation of the back injection

improvement. The orientation of polysilicon grains is predominantly 111. The abrupt transition from the 100 orientation substrate lattice to the polysilicon could cause reflection of the hole waves and reduced back injection.

CHAPTER 6: AMORPHOUS RECRYSTALLIZED FILMS

The transistors described so far have have been fabricated with polysilicon deposited by LPCVD at a temperature of 627°C . Lower deposition temperatures result in an amorphous structure. Recently Waechter et.al. [WaTa87] have studied phosphorus doped silicon films deposited amorphous by LPCVD at 560°C and then annealed at 650°C to become polycrystalline. The resistivity of these film is significantly lower than those deposited at 627°C . This effect has been attributed to larger grain size and the absence of grain boundary dopant segregation during deposition. The resistivity reduction has obvious advantages for high density MOS circuits. This deposition method was investigated for application in poly emitter devices.

Diodes were fabricated to quickly determine junction quality following the procedures and using the same mask set as outlined in Chapter 3. A film thickness of 80 nm was deposited from a 300:1 mixture of SiH_4/PH_3 resulting in a dopant concentration of $5 \times 10^{20} \text{ cm}^{-3}$. Figure 6.1.1 is a typical forward bias characteristic of one of the diodes produced together with a conventionally deposited polysilicon diode. The resistance of the amorphous recrystallized diode is larger and there is significantly increased depletion region recombination as evidenced by the higher current at low bias. The rectifying properties of these junctions were poor. Reverse bias currents in excess of 1 mA/cm^2 were measured. Typical values for the control devices were about 10 nA/cm^2 . The resistivity of the amorphous recrystallized film and as deposited polysilicon were 5.6

Figure 6.1.1: I-V characteristics of (A) -amorphous recrystallized diode and (B) as-deposited polysilicon diode.

and 20 mOhm-cm respectively, confirming the resistance reduction. Subsequent experiments were done at annealing temperatures of 800°C and 900°C. Figure 6.1.2 illustrates typical forward bias characteristics obtained. The decrease in resistance and recombination current with increased annealing temperature is obvious. These effects can be attributed to crystal regrowth and the movement of the depletion region away from the interface under dopant diffusion.

These results are difficult to explain particularly the increased resistance of the diodes recrystallized at 650°C. More research is clearly necessary. Differences in the bulk properties of the recrystallized film cannot account for the increased resistance and recombination. This suggests that the critical difference must be at the interface. The absence of grain boundary dopant segregation in amorphous recrystallized films during deposition implies a lower dopant concentration at the poly-single crystal interface. The increase in recombination could, therefore be a result of unpassivated bonds.

Figure 6.1.2: I-V characteristics of three diodes fabricated from amorphous recrystallized polysilicon annealed at (A)-650 °C, (B)-800 °C, (C)-900 °C.

CHAPTER 7: SUMMARY AND RECOMMENDATIONS

7.1

SUMMARY

This thesis had several goals, one of which was to investigate the high series resistance of the true poly emitter structure. The results showed that this resistance was caused by a poor emitter metallization and a non-ohmic emitter resistance intrinsic to the true structure. Good quality metal contacts to unannealed polysilicon junctions are difficult to fabricate because of rapid metal migration along grain boundaries during contact sintering leading to junction penetration. An acceptable metallization scheme using thermally evaporated titanium with an aluminum overlayer was developed. The contact resistance to unannealed polysilicon is still substantial however, (about 60 uOhm-cm^2) and is attributed to the low dopant activation of as-deposited in-situ doped polysilicon.

The intrinsic non-ohmic resistance of the true structure has the characteristics of a tunneling barrier and is thought to result from the presence of a thin (about 1nm) native oxide inadvertently grown at the poly-monosilicon interface. The magnitude of resistance is dependent on the particular deposition and varied from 100 to 600 uOhm-cm^2 at 500A/cm^2 , corresponding to voltage drops of between 50 and 300mV. This resistance severely limits the application of the true poly emitter structure. Emitters formed from polysilicon annealed at 900°C had substantially lower resistances (8 uOhm-cm^2) which suggests that the oxide is disrupted during annealing.

The high emitter efficiency of an unannealed poly emitter

structure has been demonstrated. Values in excess of 3×10^{15} s/cm⁴ have been recorded. These values are the highest ever reported for a silicon emitter. The only comparable values are those reported for MIS or SIPOS emitters. When combined with the narrow base width made possible by the absence of an emitter anneal this structure offers the potential for bipolar transistors with current gains in excess of 30,000. A serious drawback is the large variation and poor reproducibility of the high emitter efficiency. A second goal of this thesis was a better understanding of these effects.

The results of the investigation into emitter efficiency were not conclusive however they cast doubt on the oxide tunneling barrier theory. There was no correlation between R_E and G_E for true polysilicon emitters as one might expect. In addition, deliberately grown oxides disastrously affected the gain of the true poly emitter structure. Experiments with different emitter thicknesses indicated that the hole current suppression is a property of the interface and not of the bulk. Emitters as thin as 25nm were fabricated without any noticeable degradation in efficiency. Minority carrier reflection from a thin disordered region of low hole mobility at the interface as suggested by Neugroschel et.al. [NAK185] is a plausible explanation however TEM studies to date show no evidence for the existence of such a region. Quantum reflection of hole waves at the interface is another possible explanation of the back injection improvement. The orientation of polysilicon grains is predominantly 111. The abrupt transition from a 100 lattice to the polysilicon would be expected to cause reflection of the hole waves and reduced back injection.

Emitters formed from polysilicon furnace annealed at 900°C had more uniform although somewhat reduced emitter efficiencies (3×10^{14} s/cm⁴). This reduction could be related to the epitaxial realignment of the polysilicon with the substrate that occurs during annealing. The efficiency of these devices is improved by deliberate oxidation however emitter resistance is unaffected. The deliberate oxide may reduce the amount of realignment rather than act as a hole barrier. A drawback of furnace annealing is that it precludes the use of narrow base widths. It also increases thermal budget and introduces anomalous diffusion effects. Annealed devices still have an order of magnitude improvement in G_E over conventional devices, however, and emitter resistivities of about $8 \mu\text{Ohm-cm}^2$, close to modern bipolar VLSI values. An improved contacting technology such as PtSi could further improve their emitter resistance.

7.2

RECOMMENDATIONS

Commercial application of the true poly emitter structure would only be feasible with a number of process improvements. A method to reliably reproduce the high emitter efficiencies is essential. This requires a better understanding of the mechanism behind the high G_E values. An examination of HF cleaned and deliberately oxidized interfaces using XTEM for the presence of a 'disordered layer, oxide disruption and epitaxial regrowth is required. To date there have been no TEM studies of the unannealed in-situ doped interface. A SIMS analysis of the interface to determine dopant concentration is also necessary.

Some method to reduce the emitter resistance is also essential. If the emitter efficiency of the true structure is not related to the presence of the interfacial oxide, a process which avoids oxide growth could produce acceptable devices. Dopant activation in the polysilicon must also be increased for an acceptable metal contact resistance. Rapid thermal annealing (RTA) is a possible solution to the latter difficulty. It should be possible to anneal without causing significant dopant diffusion into the substrate. The effect of RTA on G_E , R_E , grain size and the integrity of the interfacial oxide should be investigated.

The deliberately oxidized annealed poly emitter structure appears to have adequate current handling and high and reproducible emitter efficiencies. A logical next step is the fabrication of transistors with a buried collector layer to measure dynamic characteristics such as bandwidth and switching time and the creation of simple digital circuits. Integration of annealed poly emitter transistors within an existing CMOS process could also be a very rewarding research direction. Bipolar CMOS hybrid processes offer the low power and high device density of CMOS with the high speed and current drive of bipolar logic [YHSP83], [ZAWB85]

The anomalous results with amorphous recrystallized silicon also deserve further investigation, particularly the phosphorus concentration at the interface of these devices.

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APPENDIX 1: RUN SHEET FOR POLYSILICON EMITTER TRANSISTORS

- 1) Field Oxide Growth
 - a) RCA Clean
 - b) Oxidation at 1100°C
 - 5 min pre heat
 - 10 min dry O₂
 - 15 min wet O₂
 - 10 min dry O₂
 - 30 min anneal in N₂
 - 10 min cool
- 2) Open Extrinsic Base Windows
mask CU-078-01 negative PR, etch until bare Si
- 3) Extrinsic Base Boron Diffusion
 - a) RCA Clean
 - b) Pre-dep, 1000°C
 - 5 min pre heat
 - 5 min warm-up O₂+N₂
 - 10 min dope O₂+N₂+dopant
 - 10 min hold O₂+N₂
 - 10 min cool
 - c) Boron de-glaze
30 sec dip in HF
 - d) Drive-In 1100°C
 - 5 min preheat
 - 10 min dry O₂
 - 15 min wet O₂
 - 5 min dry O₂
 - 10 min cool
- 4) Phosphorus Backside Getter
 - a) strip oxide from wafer backs, RCA clean
 - b) Pre-dep 100°C
 - 5 min preheat
 - 5 min warm up O₂+N₂
 - 10 min dope O₂+N₂+dopant
 - 5 min hold O₂+N₂
 - 10 min cool
 - c) Phosphorus Deglaze: 10 sec dip in HF
 - d) Drive In 950°C,
 - 5 min preheat
 - 20 min wet O₂
 - 5 min dry O₂
 - 10 min cool
- 5) Open Intrinsic Base windows
negative PR, mask CU-078-D2, wet etch

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- 6) Implant Oxide Growth
 - a) RCA Clean
 - b) Oxidation 1000°C
 - 5 min preheat
 - 30 min dry $O_2 + HCl$
 - 5 min dry O_2
 - 10 min anneal N_2
 - 10 min cool
- 7) Intrinsic Base Implant
- 8) Base Implant Anneal
 - a) RCA Clean
 - b) Low Temperature Anneal 650°C
 - 60 min anneal N_2
 - c) High Temperature Anneal 950°C
 - 5 min pre heat
 - 30 min anneal
 - 10 min cool
- 8) Open first Emitter Window

negative PR, mask CU-078-03, wet etch
- 9) First Polysilicon Deposition
 - a) RCA Clean
 - b) Interface Treatment
 - 10 sec HF dip, 10 min rinse in D.I. water and blow dry
 - OR
 - HF dip as above followed by 10 min dip in solution of $HCl:H_2O_2:H_2O$ (1:1:6) at 80°C, 10 min rinse in D.I. and blow dry
- Proceed Immediately to Next Step
- c) Polysilicon deposition at 627°C, $SiH_4:PH_3$ 160:1, pressure 0.4 torr
- 10) Pattern Polysilicon

positive PR, wet etch, mask CU-078-04
- 11) Optional Polysilicon Anneal 900°C
 - a) RCA Clean
 - 5 min preheat N_2
 - 30 min anneal N_2
 - 10 min cool

- 12) Open Second Emitter Windows
positive PR, wet etch mask CU-078-05
- 13) Second Emitter Deposition
 - a) HF dip or chemical oxidation
 - b) Deposit as per first deposition
- 14) Pattern Second Polysilicon Layer
positive PR, mask CU-078-06, wet etch
- 15) Optional Anneal
- 16) Open Base Contact Windows
negative PR, wet etch, mask CU-078-07
- 17) Base and Emitter metallization
Flash dip in HF to clear residual oxide
 - a) Ti deposition by thermal evaporation to thickness of between 70 to 100nm Do not break vacuum after deposition
 - b) Al deposition by thermal evaporation to thickness of at least 0.5um.

APPENDIX 2: PROCESSING DETAILS OF WAFERS

Wafer	Base implant	First polysilicon	Second Polysilicon	Metallization
EK-1	50keV, 10^{12}	etched off	100nm, unannealed	Al, unsintered
EK-2	50keV, 10^{12}	no base after anneal	100nm, HF $G_E = 6 \times 10^{12}$, $p_e = 200$	Al, unsintered redone with 100nm Ti, 580nm Al
EK-3	50keV, 10^{12}	etched off	100nm, HF	Al, unsintered
EK-4	50keV, 10^{12}	100nm, HF, $p_e = 1000$ $G_E = 10^{12}$	25nm, HF, $p_e = 380$ $G_E = 10^{12} - 4 \times 10^{14}$	750nm Al 320nm Ti
EK-5	50keV, 10^{12}	100nm, RCA, $p_e = 2 \times 10^4$, G_E less than 10^{13}	100nm, HF, $p_e = 650$ $G_E = 6 \times 10^{14}$	89nm Ti 720nm Al
EK-8	50keV, 2×10^{12}	100nm, HF annealed	100nm, HF unannealed	Al, unsintered
EK-9	50keV, 2×10^{12}	100nm, HF $p_e = 1000$, G_E less than 10^{13}	25nm, HF, $p_e = 500$ $G_E = 1 - 7 \times 10^{14}$	89nm Ti 720nm Al
EK-11	50keV, 5×10^{12}	100nm, RCA, annealed, $p_e = 8$ $G_E = 7.5 - 8.0 \times 10^{14}$	100nm, HF, annealed $p_e = 8$, $G_E = 2.5 - 3.0 \times 10^{14}$	140nm Ti 700nm Al
EK-12	50keV, 5×10^{12}	100nm, HF, annealed, $G_E = 3 \times 10^{14}$	100nm, HF $G_E = 1.4 \times 10^{15}$	100nm Ti 580nm Al
EK-13	50keV, 5×10^{12}	100nm, HF, annealed $p_e = 5$, $G_E = 3.1 - 3.6 \times 10^{14}$	25nm, HF, annealed $G_E = 1.0 - 1.2 \times 10^{14}$ $p_e = 20$	140nm Ti 700nm Al

RCA-deliberately oxidized interface

HF- HF cleaned interface

p_e in uohm-cm², G_E in s/cm⁴

APPENDIX 2: CONTINUED

Wafer	Base implant	First polysilicon	Second Polysilicon	Metalization
EK-14	30keV, 10^{12}	no base after anneal	100nm, HF	Al, unsintered
EK-15	30keV, 10^{12}	100nm, RCA p_e more than 10^4 G_E less than 10^{13}	100nm, HF, $p_e=550$ $G_E=4 \times 10^{14}$	140nm Ti 700nm Al
EK-16	30keV, 5×10^{12}		100nm, HF, $p_e=125$	100nm Ti 580nm Al
EK-19	100keV, 10^{12}	100nm, HF, annealed, $p_e=50$ $G_E=2.8-3.2 \times 10^{14}$	100nm, HF unannealed, $p_e=360$ no base-collector junction	320nm Ti 750 nm Al

APPENDIX:3

Fabrication Details of Kelvin Resistors

Wafers already have 100nm of thermal oxide

- 1) Polysilicon Deposition SiH_4 -19.4%, SiH_4 -15%, Temp=627°C
pressure=0.28 torr, time = 3hr, target thickness=300nm
- 2) Pattern Polysilicon
positive PR, wet etch, mask CU-083-01
- 3) Optional Polysilicon Anneal, 900°C, N_2 ambient, 30 min
- 4) Deposit Oxide 100nm, undoped LOTOX
Recipe 1, Pressure= 0.32 torr, SiH_4 -25%, O_2 - 27.5%,
Temp=410°C, 10min deposition
- 5) Open Oxide Windows, mask CU-083-02
negative PR,
- 6) Deposit Metal
Vacuum evaporation, e-beam or thermal

APPENDIX:4

FABRICATION DETAILS OF POLYSILICON-SILICON DIODES

Starting Materials- p-type, 100 orientation, 50mm wafers, resistivity of 1.8-2.6 ohm-cm (wafers already have 100nm of thermal oxide)

- 1) Open Emitter Windows
mask CU-060-01, negative PR, etch in buffered HF until Si surface exposed, strip PR in Caro's
- 2) Polysilicon Deposition
RCA Clean and flash dip in 10% HF immediately prior to deposition, rinse in D.I. water and spin dry

Deposit at 627°C, SiH₄-37%, SiH₄/PH₃-15%, target thickness 100nm
- 3) Pattern Polysilicon
mask CU-060-02, positive PR
- 4) Optional Anneal, 900°C, N₂, Phosphorus Drive-In tube
- 5) Back Contact
flash HF dip, deposit at least 0.5um of Al by e-beam
- 6) Back Contact Anneal
450°C, H₂ ambient, 20 min
- 7) Emitter Metallization

END

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FIN