A HIGHLY RECONFIGURABLE SINGLE-ENDED LOW NOISE AMPLIFIER FOR SOFTWARE DEFINED RADIO APPLICATIONS

By

Richard Stuart Beare

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Ottawa-Carleton Institute for Electrical Engineering
Department of Electronics
Faculty of Engineering
Carleton University
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ABSTRACT

With multiple standards and different requirements, there is a growing interest in reconfigurability potentially leading to the software defined radio. Although ideally a software defined radio would consist only of an antenna and an analog to digital converter, with current technology limitations, at the very least, some filtering and amplification is required. This thesis is about the design of a highly reconfigurable low noise amplifier aimed at software defined radio.

In this thesis, core radio-frequency concepts are covered followed by a discussion of the design process of the 0.13μm CMOS low-cost highly-reconfigurable low-noise amplifier with reconfigurable gain, bandwidth and center frequency. The design process included the balancing of the merits and drawbacks of various LNA topologies and of the various techniques that were applied to grant the high degree of reconfigurability. At the schematic-level, the design achieved with a 1.2V supply a minimum-to-maximum 3dB bandwidth ratio of approximately 3.1, a maximum gain of about 16dB, a noise figure as low as 2.5dB, less than -10dB return loss over all bands, and an IIP3 as high as -0.9dBm at low gain. Though the fabricated LNA did provide most of the desired functionality (variable gain and center frequency), an unfortunate design oversight caused a great reduction in the gain, matching and noise performance of the amplifier. This is reported in the results section of this thesis.

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LIST OF ACRONYMS

ADC	–	Analog to Digital Converter
BW	–	Bandwidth
CMOS	–	Complementary Metal-Oxide Semiconductor
DC	–	Direct Current
DSP	–	Digital Signal Processor
DUT	–	Device Under Test
ESD	–	Electrostatic Discharge
FCW	–	Frequency Control Word
FET	–	Field-Effect Transistor
F	–	Noise Factor
GPS	–	Global Positioning System
IIP3	–	Input Referred Third Order Intercept Point
IM3	–	Third Order Intermodulation Product
LNA	–	Low Noise Amplifier
LVS	–	Layout vs. Schematic
MIMCAP	–	Metal-Insulator-Metal Capacitor
MOSFET	–	Metal-Oxide Semiconductor Field-Effect Transistor
NFA	–	Noise Figure Analyzer
NF	–	Noise Figure
OIP3	–	Output Referred Third Order Intercept Point
P1dB	–	Input Referred 1dB Compression Point
PVT	–	Process Variance and Temperature
Q	–	Quality Factor
RFID	–	Radio Frequency Identification
RF	–	Radio Frequency
RMS	–	Root Mean Square
SDR	–	Software Defined Radio
SINAD	–	Signal to Noise and Distortion Ratio
SNR	–	Signal to Noise Ratio
SRF	–	Self Resonant Frequency
TRL	–	Through-Reflect-Load
VDD	–	Drain Supply Voltage
VNA	–	Vector Network Analyzer
VSS	–	Source Supply Voltage (ground)

CHAPTER 1

INTRODUCTION

1.1 MOTIVATION AND OVERVIEW

The demand for low-cost, integratable and highly reconfigurable radio systems for future radio-frequency applications has generated a demand for highly reconfigurable integratable RF systems. An effective approach for adaptive and reconfigurable radio is to integrate multiple analog communications receivers and transmitters in a device to cover each wireless standard individually. This approach allows the designers to optimize the design of each receiver/transmitter for each individual standard, but with the drawback of high chip space requirements and thus high cost. Unfortunately, this is not sustainable for an increasing need for adaptability, as required chip area and cost will increase indefinitely. The most feasible future solution is to use software defined radio techniques [1]. The ideal software defined radio receiver consists of an antenna, an analog-to-digital converter (ADC) and a digital signal processing (DSP) chip. Modern ADCs are pushing multiple GHz sample rates [2], which indicates that pseudo-SDR is practical in base-station applications. Currently, such radios are unsuitable for portable applications due to the high power consumption of high-speed ADCs.

True SDR converts the modulated RF analog signal directly from the antenna into digital format that is processed totally digitally. Unfortunately, the inputs of modern ADCs are sensitive to large interfering signals, which may not get rejected by the antenna [3]. As well, in most cases ADCs require the RF signals to be amplified and unwanted RF

energy (noise and interfering tones) filtered before the analog-to-digital conversion such that the signal power is adequately larger than the noise and interfering signals so that it can be processed with minimal error. In order to achieve this, the system must include a filter and a low noise amplifier (LNA) in addition to the antenna, ADC and DSP. The combination of the filter and the LNA could provide the necessary signal amplification and noise and interferer rejection required for the ADC and DSP. The job of the LNA is to amplify the wanted RF signal while rejecting noise and unwanted signal energy, adding as little noise as possible and maintaining the shape of the signal as accurately as possible (i.e. possess highly linear performance). In the case where the RF signal could exist at any frequency, then the frequency where amplification occurs would have to be adjustable in order to cover the required range of frequencies. As well, the strength of the signal is highly dependent on position of the receiver relative to the RF signal source, so variable gain is required to adapt to varying signal strength. Different RF standards require different bandwidths, so the bandwidth of the LNA also needs to be variable. In this thesis, a 0.13μm CMOS LNA with adjustable centre frequency, bandwidth and gain with good low-noise performance and linearity is presented to suit these requirements. The benefit of designing in digital CMOS technology is that the LNA can be integrated on-chip with the SDR, greatly reducing cost and required area for the system.

1.2 THESIS OBJECTIVES

The objective of this thesis is to present a highly reconfigurable low noise amplifier (LNA) for software defined radio applications. The goal of the proposed design is to provide a software defined radio system with selective amplification of wanted RF signals, while rejecting unwanted RF signals and noise. This LNA was developed on the IBM 0.13μm digital CMOS process, and was fabricated through MOSIS. This well-characterized design kit provides highly reliable device models at RF frequencies, and provides FETs that perform quite well at RF frequencies below 10GHz.

1.3 CONTRIBUTIONS

This research contributes to the advancement of techniques for providing software defined radio inputs with low-noise and distortion signals over a broad range of frequencies. This implementation of an RF low-noise amplifier provides the uncommon feature of variable bandwidth. In addition to variable bandwidth, variable gain and center frequency functions are included. This technology can improve SDR system performance when operating over a wide range of RF standards.

1.4 THESIS OUTLINE

Chapter 2 covers the necessary background material: basic RF and analog electronics concepts such as noise figure, linearity, stability, impedance matching and scattering parameters, passives and more. The second part of chapter 2 goes through basic LNA design techniques and topologies, a brief review of literature, as well as a general review of SDR radio architecture and the proposed pseudo-SDR architecture. Chapter 3 presents and discusses the design process and the simulated and measured results of the proposed LNA. In chapter 4, conclusions are made and future work is discussed.

CHAPTER 2

RF CONCEPTS AND THEORY

This chapter covers the essential RF concepts and theory required to understand the function and implications of the design choices in the presented LNA design.

2.1 FUNDAMENTAL RF CONCEPTS

In this section, fundamental RF design concepts such as impedance matching and scattering parameters, stability, noise, quality factor of passive components, nonlinearity, dynamic range and analog to digital converters are covered.

2.1.1 IMPEDANCE MATCHING AND SCATTERING PARAMETERS

Impedance matching is an essential part of the design of RF systems. Conjugate matching ($Z_L=Z_S^*$) is the standard technique which creates the condition for maximum power transfer from the source to the load. Conjugate impedance matching prevents reflections back to the signal source, which can negatively affect the response of the preselect filter, and cause retransmission and/or standing waves on the line. Reactive lossless matching is the most desirable approach for low noise performance and narrow bandwidth applications, though suffer from the need for large, fixed-value inductors. Feedback

matching techniques are suitable for broadband matching; though these techniques generally suffer from higher minimum noise figure. Fifty ohms is the standard source impedance used in RF systems, and is the signal impedance used in this thesis. This characteristic impedance is approximately in between the optimal impedance for maximum power handling and minimum loss for coaxial cables. This is often not optimal for every system design, but is often used for compatibility.

The quality of a match can be described by scattering parameters (S-parameters). S-parameters describe the behavior of a linear system in terms of the reflected and transmitted voltage with reference to an input voltage waveform. These are used to describe small signal behavior of microwave systems. Generally in RF and microwave design, this is applied to 2-port networks, where S_{11} refers to input voltage reflection coefficient, S_{21} refers to forward voltage gain, S_{22} refers to the reverse voltage reflection coefficient, and S_{12} to the reverse voltage gain.

2.1.2 STABILITY

Stability is an important factor to consider when dealing with circuits or systems with gain. Instability is caused when the loop gain is greater than unity at that particular frequency. In other words, the output of the system is fed back to the input, reinforcing that input, causing the system to oscillate. This can involve dominant rail-to-rail oscillations or smaller spectral tones that can decrease the signal to noise and distortion ratio. Stability can be measured using S-parameters by the K-factor, where S_{11} is the input voltage reflection coefficient, S_{22} is the output voltage reflection coefficient, S_{21} is the forward voltage gain, and S_{12} is the reverse voltage gain. The K factor is given by (2.1) [30].

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|}{2|S_{21}S_{12}|} \tag{2.1}$$

where Δ is given by

$$\Delta = S_{11}S_{12} - S_{12}S_{21} \tag{2.2}$$

The system is potentially unstable if K<1. Cadence Virtuoso also offers a secondary stability factor B1f that can be used to help judge the stability of a circuit.

2.1.3 NOISE FACTOR AND NOISE FIGURE

The noise factor of a device can be described by (2.3) [15].

$$F = \frac{N_{o,total}}{N_{o,source}} = \frac{N_{o,total}}{G \cdot N_{i,source}}$$
$$= 1 + \frac{N_{i1,added}}{N_{i,source}G_1} + \frac{N_{i2,added}}{N_{i,source}G_1G_2} + \cdots + \frac{N_{iN,added}}{N_{i,source}G_1G_2 \cdot \ldots \cdot G_n} \tag{2.3}$$

This equation applies for any number n stages, and N_i refers to input noise, and N_o refers to output noise. The equivalent noise model of a system with N series stages is shown in figure 2-1 below:

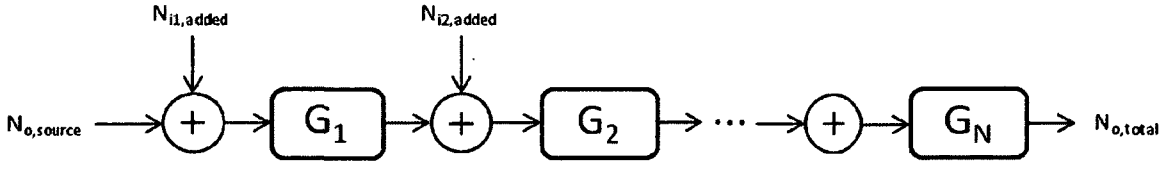

Figure 2-1: Noise model of a system

For each noise source (i.e. $Ni_{1,added}$), the appropriate input-referred noise quantity must be computed. The noise figure, as most commonly used in telecommunications, is defined as

$$NF = 10log_{10}F \tag{2.5}$$

For devices with XdB of loss, the noise figure is the same as the loss since the signal gets XdB lower for the same quantity of noise power.

2.1.4 NOISE MATCHING FOR MINIMUM NOISE IN MOSFETS

Noise factor (F) is the standard term used to describe the degradation of signal to noise ratio in a system, and is usually reported as noise figure (NF), which is simply $10\log_{10}(F)$. Noise factor is defined in (2.3). In LNAs, it is desirable to achieve absolute minimum possible noise. The CMOS transistor contributes noise from a number of internal sources. These sources consist of 1) white thermal noise due to parasitic gate poly resistance, 2) the thermal channel noise, and 3) flicker noise in the channel. Generally, flicker noise can be ignored in analysis of LNA noise, as the 1/f noise corner is well below RF frequencies. The noise factor in the MOSFET can be modeled by

$$F = 1 + \frac{R_g}{R_S} + \frac{\gamma}{g_m R_S} + \frac{1}{g_m{}^2 R_S R_L} \tag{2.6}$$

[15] where γ is the thermal noise coefficient, and describes the fraction of the channel that is not pinched off. This coefficient is 2/3 for a long-channel device but is much higher in short channel devices, and approaches 1 as V_{DS} approaches 0V [4]. R_g is the parasitic gate poly resistance, which is

$$R_g = \frac{1}{12}\rho_s \frac{W}{L} \tag{2.7}$$

where ρ_s is the sheet resistance of the poly and W and L are the MOSFET gate width and length dimensions respectively. The factor of 1/12 describes the distributed nature of resistance throughout the gate for a gate accessed from two sides. R_S and R_L are simply the source and load impedance respectively, and g_m is the transconductance of the MOSFET. The noise due to the gate can be reduced by using multiple gates in parallel to reduce the net gate resistance.

Based on (2.6), it would be expected that the noise factor should reduce indefinitely with increasing transconductance (and current). This is actually not the case, as the relationship between g_m and I_D begins to weaken past a certain current density, and g_m ultimately stops increasing with I_D. The γ factor increases linearly with gate-source overdrive voltage and causes the noise figure to reduce as g_m stops increasing with I_D.

This relationship means that an optimal current density exists for a given device, and must be considered in LNA design.

In order to achieve noise matching, a designer can match for power and lowest minimum noise figure (NF_{min}) simultaneously. The minimum NF_{min} exists at a specific source impedance for given transistor dimensions and bias conditions. For a fixed current density, the width of the transistor can be adjusted to set the source impedance for lowest NF_{min} to 50 Ohms.

2.1.5 QUALITY FACTOR AND DESIGN CONSIDERATIONS OF PASSIVE COMPONENTS

In real passive components, loss is unavoidable. The quality factor or Q of a component can be described by the ratio of its complex impedance to its equivalent parallel parasitic resistance, by

$$Q = \left|\frac{Im(Z)}{Re(Z)}\right| \tag{2.9}$$

where Z is the impedance of the component. Generally, the losses in on-chip capacitors are very low due to the high purity of on-chip dielectrics. The losses in varactors are much higher than that of a normal dielectric capacitor, as the p-n junction contains a great deal more impurities than would exist in dielectric. Inductors also suffer from losses due to losses in the metal (affected by the skin effect), substrate coupling losses and magnetic coupling. Inductors are generally the lowest Q passive components on-chip. As such, they must be carefully designed to meet the needs of the design specifications.

In inductors, Q is enhanced and peak Q frequency is lowered by increasing the metal width, but inductance and the self-resonant-frequency (SRF) are lowered due to increased substrate-coupling capacitance. Decreased line spacing can enhance the inductance and result in higher Q, but keeping the lines tight increases inter-winding capacitance which can reduce the self-resonance-frequency. Larger inductor area increases the inductance

due to an increase in the spiral area, but this causes a reduction in the Q and the peak Q frequency at high frequencies due to increased substrate currents. Adding more turns to an inductor increases its inductance, but increases its inter-winding capacitance. Also, the more that turns are added, the less the additional turns affect the inductance and the more that these additional turns increase the losses.

2.1.6 NONLINEARITY IN DEVICES AND SYSTEMS

The nonlinearity of a component can be represented in a number of ways. Nonlinearity is inherent in active devices; ideally, the output of a system is linearly related to the input, but in reality this is not the case. In the frequency domain, nonlinearity can be described by stating that certain quantities of the total energy of the output signal are distributed to frequencies that are not equivalent to the frequencies of the input signal. This is often undesired in analog circuits, particularly in amplifiers (but not always, i.e. it is necessary in mixers and switches). For a memoryless system, the output voltage nonlinearity can be represented as power series expansion by

$$v_{out} = k_0 + k_1 v_{in} + k_2 v_{in}^2 + k_3 v_{in}^3 + \cdots \tag{2.10}$$

where the k terms are the power-series coefficients, and v_{in} is simply the input voltage signal. The first three terms can define the nonlinear behavior of a circuit to a reasonable degree of accuracy, which is useful for paper analysis. The third order intermodulation products, and sometimes the second order mixing products are of great concern in design. When two tones X_1 and X_2 are applied to the input of a nonlinear device, the following result can be seen (to the third order):

$$V_{out} = k_0 + k_1(X_1 + X_2) + k_2(X_1 + X_2)^2 + k_3(X_1 + X_2)^3$$

$$= k_0 + k_1(X_1 + X_2) + k_2(X_1^2 + 2X_1X_2 + X2^2) + k_3\left(X_1^3 + \mathbf{3X_1^2X_2} + \mathbf{3X_1X_2^2} + X_2^3\right) \tag{2.11}$$

The two products in bold are the third order intermodulation products, which mix to $2f_1 - f_2$ and $2f_2 - f_1$. These are of concern, as the product of these two tones can land within the

receive band and detract from the signal to noise and distortion ratio (SINAD) of the receiver. The other products land far enough out of band that they can usually be filtered out easily. Second order nonlinear products from the mixer is of concern in direct down-conversion and ultra wideband architectures, but the second order nonlinear products of the LNA can generally be easily filtered after the LNA.

Third order intercept point (IP3) is the standard way that the linear performance of a device is measured and presented. The voltage at which this occurs can be expressed by (2.12) [15].

$$v_{IP3} = 2\sqrt{\frac{k_1}{3|k_2|}} \tag{2.12}$$

The IP3 can either be input (IIP3) or output (OIP3) referred. Generally, it is input referred, and is expressed in terms of power, by

$$IIP3 = P_i + \frac{1}{2}[P_1 - P_3] \tag{2.13}$$

where P_1 is the power of the fundamental tone and P_3 is the power of the third order intermodulation tone at the output for a given input tone P_i.

Another important factor in assessing the linearity of a device is the 1dB compression point, usually expressed in terms of power (P1dB). The P1dB occurs when the output power versus input power relationship (linear below the P1dB point) reduces by 1dB from its linear trend. This is caused by compression, where the gain cannot be sustained beyond a given input power. The knowledge of this parameter is particularly useful when dealing with the dynamic range of a system, and when a device must be designed to sustain a certain maximum input power without gain compression. The 1dB compression point can be expressed in terms of input voltage and the first and third order power series coefficients by

$$v_{1dB} = 0.38\sqrt{\frac{k_1}{k_3}} \tag{2.14}$$

The 1dB compression point can be related to the third order intercept point by

$$\frac{v_{IP3}}{v_{1dB}} = \frac{2\sqrt{\frac{k_1}{3|k_2|}}}{0.38\sqrt{\frac{k_1}{k_3}}} = 3.04 = 9.66dB \tag{2.15}$$

When two tones are applied in the case of a two tone test, the net input power increases, causing a decrease in the 1dB compression point for a given tone-power (assuming both tones are of equal power). The relationship between v_{IP3} and v_{1dB} in this case can be expressed by

$$\frac{v_{IP3}}{v_{1dB}} = \frac{2\sqrt{\frac{k_1}{3|k_2|}}}{0.22\sqrt{\frac{k_1}{k_3}}} = 5.25 = 14.4dB \tag{2.16}$$

Tests of linearity of a device can be performed by applying two tones of equal magnitude to the input of the device under test. By applying two tones of equal magnitude and spaced in frequency so that the third order intermodulation products land in-band, the input power can be swept and the first and third order products can be measured at each increment of input power. With these results, the P1dB and IIP3 can be found. An example of the results of a two-tone test in a transistor amplifier is shown in Figure 2-2. In this figure, a 14dB difference in input power exists between the P1dB and the IIP3, very close to the theoretical 14.4dB expected for a two-tone-test. These results were taken from simulation of a generic simultaneously noise and power matched common-source amplifier, as shown in Figure 2-3.

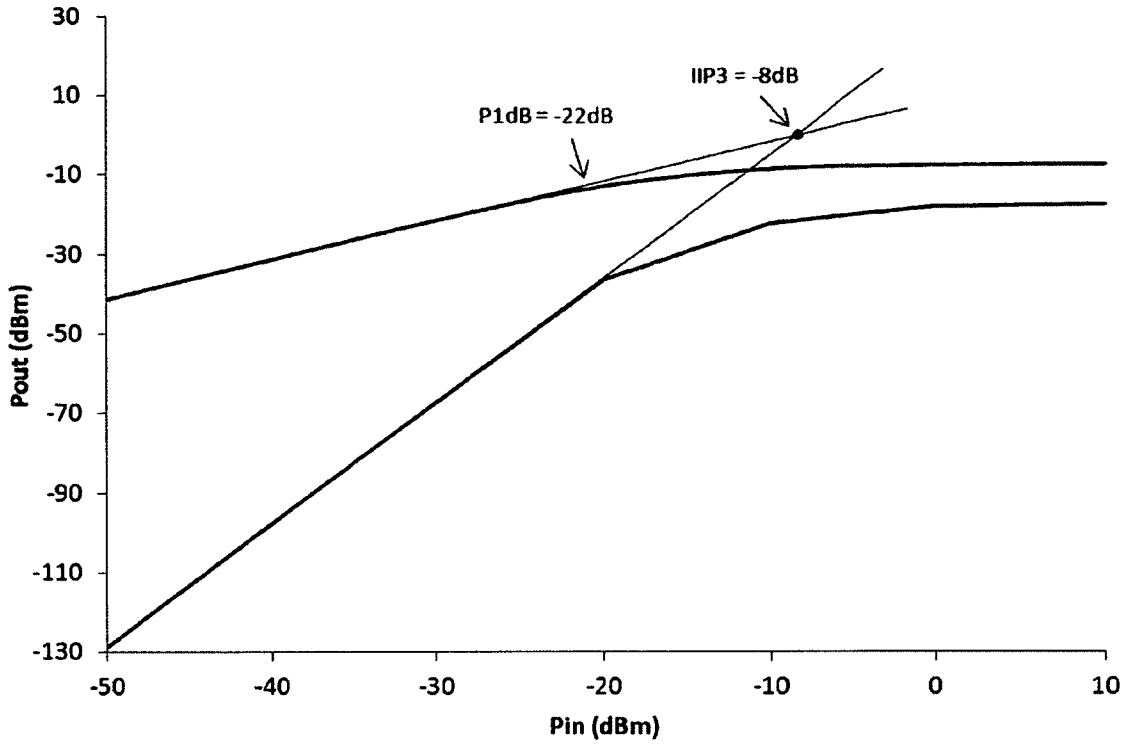

Figure 2-2. Output power and IM3 product versus input power for a transistor amplifier

When components are in series, the net nonlinearity of the entire system can be computed with the knowledge of the nonlinearity of the series components. The IIP3 of a system with cascaded gain stages can be computed by

$$\frac{1}{IIP3} = \frac{1}{IIP3_1} + \frac{G_1}{IIP3_2} + \frac{G_1 G_2}{IIP3_3} + \cdots + \frac{G_1 G_2 \cdot \ldots \cdot G_N}{IIP3_{N+1}} \qquad (2.17)$$

where G is the gain of the N_{th} stage, and IIP3 is the input referred third order intercept point of the $N+1^{th}$ stage. This equation works, assuming all stages are matched to a given characteristic impedance. The system P1dB has the exact same form as (2.17), except the IIP3s are replaced with P1dB. It can be seen that the further down the chain a component is in a system, the greater effect they have on the overall linearity (this is assuming that the net gain is greater than unity).

2.1.7 NONLINEARITY IN MOSFETS

MOSFETs inherently posses nonlinear behavior. The current-voltage transfer characteristic can be roughly modeled by the well known square law model

$$I_D = \frac{u_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \qquad (2.18)$$

With very small input voltage swing, one can expect an approximately linear output current swing. As the input voltage swing becomes more significant, second order products become more apparent. Based on the square-law model, one would not expect there to be any third order intermodulation products, though this is not the case in reality, as the drain-source voltage is dependent on the gate-source voltage when there is a load applied to the source or drain. For large input signal amplitudes, the swing can approach the $V_{GS}>V_T$ and $V_{DS}>V_{GS}-V_T$ limits, which yields odd order terms. The dependence of the drain current on the drain-source voltage (λV_{DS} term) is also nonlinear in reality.

2.1.8 ANALOG TO DIGITAL CONVERTERS

ADCs are used to digitize analog signals. ADCs are used in all digital telecommunications systems [5], which include cell phones, digital cable TV, network interface cards, Wi-Fi, military radio, electronic warfare systems and a great deal more. The vast majority of modern telecommunications systems use digital architectures and modulation schemes. The reason for this is the much higher degree of achievable spectral efficiency (i.e. the achievable data rate for a given bandwidth) with digital radio compared to analog radio [6]. Comparing a digitally modulated RF signal to an analog-modulated RF signal with the same signal-to-noise ratio (SNR) and bandwidth, the maximum achievable data rate for the digital signal is a great deal higher. The major limitation to the maximum RF frequency that SDR can operate at is limited to the maximum sampling rate in combination with the effective number of bits of the ADC of the receiver. Currently, the fastest single ADC units on the market can sample at a rate of

3.6GSPS with 12 bits and an achievable SFDR of 75dB [2], although higher sampling rates have been reported in literature [7], [8]. Satisfying the required nyquist frequency of half of the sampling frequency, the theoretical maximum RF input frequency that can be sampled is 1.8GHz. Software defined radio architectures require ADCs with very fast sampling rates that surpass the nyquist rate for the sampling of RF signals. In standard digital radio, the RF signal is down converted to baseband, and the ADC is required to have a sampling rate of at least the bandwidth of the signal; therefore, the demands for high sampling rates are more relaxed in standard digital radio. ADCs in SDR also need a high number of effective bits in order to accommodate the high dynamic range of input signals, and to achieve the best possible spurious-free dynamic range (SFDR). The need for high dynamic range is generally less stringent in standard digital radio, as the receivers generally incorporate automatic gain control. The spurious-free dynamic range is proportional to both the number of effective bits and the oversampling rate (the ratio of the sampling rate and the nyquist rate). Therefore, it is necessary to maximize both of these parameters while staying within the power, cost and size requirements of the system.

Multiple ADCs can be placed in parallel (pipelined) and sampling can be time-interleaved to multiply the effective sampling rate by the number of ADCs [9]. Thus, the nyquist rate (and thus the maximum RF input signal frequency) can theoretically be increased by the number of ADCs. The issue with such a technique is increased complexity, size, cost, sampling time and other mismatch errors [10] (which cause reduction in SFDR) and increased power consumption. Due to these issues, such a technique is not always feasible or desired. At the present moment, based on the maximum nyquist rate of 1.8GHz for a 3.6GSPS ADC, SDRs with one ADC can cover the 800MHz mobile phone standard, GPS, RFID, some aeronautical radio-navigation and mobile standards, mobile satellite and amateur radio to name a few [11]. As ADC technology improves, so does the range of applications for SDR.

2.1.9 DYNAMIC RANGE

With the understanding of linearity and noise figure, one can consider the dynamic range of a system. Dynamic range describes the absolute minimum and absolute maximum input signal power that can be handled by the system. If the input signal is too small, the resultant signal after digitization is too small to be effectively differentiated from the noise and the bit-error-rate or symbol-error-rate (both are correlated) become too high for practical use. The minimum detectable system is referred to as the *sensitivity* of the system, reported as an input RF signal power quantity. If the input signal is too large, then the input of the ADC can be saturated or dominated by nonlinear products, and will be unable to detect the signal of interest. It is thus important that a radio receiver can provide high linearity, low-noise properties and necessary filtering in order to achieve the required sensitivity, and gain control so as to prevent desensitization of the ADC.

2.2 LNA DESIGN AND ARCHITECTURE

In this section, basic LNA design techniques and topologies will be covered. Following this, a brief review of literature will be presented, and then broadband architectures and the proposed pseudo-SDR will be discussed.

2.2.1 BASIC LNA THEORY AND DESIGN

The LNA is considered to be in many cases the most important component in a receiver chain. This is the case, as the LNA is generally the device that dominates the overall receiver noise figure. The purpose behind this device is to amplify the desired RF energy and reject noise and other unwanted RF energy. It is thus very important that LNAs are designed with low noise in mind. This can be achieved with noise matching techniques, proper transistor sizing and biasing and selecting a suitable topology.

The LNA must be impedance matched to the output impedance of the preceding filter (usually 50Ω) and must be capable of effectively driving the input of the mixer. Impedance matching is required in order to ensure maximum power transfer into the LNA to avoid reflections back into the filter. Reflected RF energy can denature the filter performance and can cause re-transmission, and is thus undesirable. In the case of SDR, the LNA would be required to have output driving power sufficient to drive the input of the ADC. In other words, it is desirable to have optimum voltage transfer to the mixer or ADC such that the gain is maximized. For integrated receivers, matching is generally not required between the output of the LNA and the input of the mixer or ADC as they are generally integrated on the same chip, and the distance between the devices relative to the wavelength of the RF signal on the chip is insignificant; thus transmission line effects do not occur and subsequently reflections do not occur.

Linearity is another important factor that contributes to the performance of the LNA and the overall receiver chain. In LNA's, gain is traded off with linearity performance. As gain is increased, linearity is decreased and vice-versa. This is the case, as the output voltage swing of the amplifying transistor increases with increasing gain for the same input signal amplitude. As the output voltage swing increases, the transistor approaches compression which causes signal distortion. High gain is desirable in the case where the input signal power is low, and vice versa. The benefit of this relationship is that the smaller the input signal is, the more linear the output is. Thus, the gain can be maximized for minimum size input RF signals without sacrificing the linear performance of the system. When the input signal is large, low gain is required, and thus linearity can be preserved by adjusting the gain.

Generally, in selective narrowband systems, the bandwidth of the LNA is not given strong consideration, but by putting emphasis on optimizing the LNA bandwidth for the desired signal, the out-of-band noise power and interferer power can be reduced. Addressing this consideration in an LNA can improve the signal-to-noise and distortion ratio of the system.

2.2.2 BASIC LNA TOPOLOGIES

There are a number of possible techniques that can be applied to match the impedance of a source and a load. These techniques can be split into both narrowband and broadband varieties. The most common topology for narrowband amplification is the common source LNA with simultaneous noise and power matching. Such a match can create an ideally noiseless and purely real 50Ω input match, leaving the transistor and load as the only noise contributors in the circuit. This technique includes an inductor in the gate and source, and its topology is shown in figure 2-3 below.

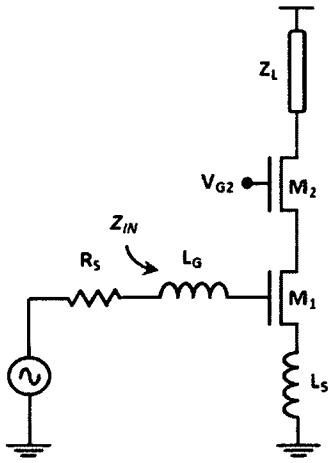

Figure 2-3. Simultaneous noise and power matched amplifier

Inductor L_S effects both the real and imaginary components of the input impedance, but its purpose is to match the real component by providing positive feedback to the source. Inductor L_G is used to match the imaginary component, setting it to zero ohms by resonating out the input capacitance of the FET (for standard purely real 50Ω source). The first step in the process of simultaneous noise and power matching is to find the optimal noise resistance for the load (the common source FET). This can be done by adjusting the gate resistance of the FET by means of adjusting the length, width and/or number of fingers in the gate. Generally, a drain-source current is selected for optimal noise performance, and then the width is increased while maintaining constant current density, until Γ_{opt} is found, as described in section 2.1.4. Following this, the source

inductance can be calculated based upon the transconductance, the gate-source capacitance and the required source impedance, by

$$L_S = \frac{C_{gs}R_s}{g_{m1}} \tag{2.19}$$

The gate inductance in is designed to resonate out the remaining complex impedance looking into the gate, and can be found with

$$L_G = \frac{1}{C_{GS1}\omega^2} - L_S \tag{2.20}$$

The gate-drain capacitance is generally ignored in the case where a cascode stage is included, as this makes for an adequately accurate and simple first-order approximation for the values of the matching inductors. This particular technique provides a very good narrow-band input noise and power match for very good power transfer and low noise within the band. The noise performance is limited to the transistors noise performance and the quality factor (Q) of the input matching inductors. The quality of the power match and the bandwidth of the match are also dependent on the Q of these inductors. As well, process variance can affect the resonant frequency of the input matching circuit, and thus the frequency point at which the input match is optimal. Unfortunately, given the narrowband nature of this match, this technique cannot be used for the design described in this thesis. The possibility of switching in and out various matching inductors does exist, though such a technique would require far too much chip area.

Another commonly used topology is that of shunt-feedback common source. Shunt-feedback involves connecting a passive element from the output of a common source amplifier to the input of said amplifier, as shown in figure 2-4 below.

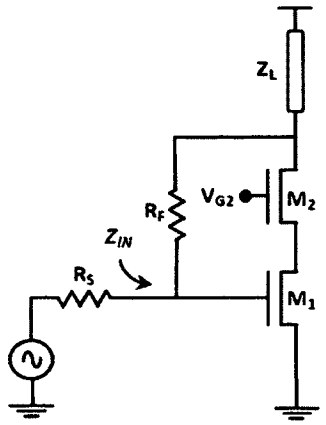

Figure 2-4. Shunt-feedback amplifier

Generally, a resistor is used to provide the feedback, though reactive components or combinations of reactive and resistive components can be used for ultra-wideband LNAs, transimpedance amplifiers, and for amplifier stabilization [12], [13], [14]. This technique is popular for achieving a broadband input match with low NF and reasonable linearity while eliminating the need for large inductors for matching [16]. This shunt-feedback technique offers the advantages of reduced area (no matching inductors), reasonably low NF, enhanced stability caused by the negative feedback, and enhanced robustness to process, voltage and temperature variation (PVT) due to reduced reliance of performance on transistor parameters [16], [17]. The principle of this technique is as follows. Assume an ideal transistor with infinite input impedance and a fixed transconductance. The voltage incident on the gate of the transistor inhibits a current through the load, which consists of a load resistor and the feedback resistor in parallel. The voltage generated on the output due is 180 degrees out of phase with the input voltage, and causes current to be drawn through the parallel feedback and load resistors, given by $(V_{in}-V_{out})/R_{fb}$. The smaller the feedback resistance is relative to the load resistor, the higher is the ratio of drain current drawn from the source through R_{FB} than through the load R_L (for a given input voltage), and thus the lower the input impedance is. 50 Ohm impedance can be achieved when V_{in}/I_{in} is 50Ω, thus the feedback resistor can be adjusted in order to set this input impedance. The equation used to describe this relationship is

$$Z_{in} = \frac{R_{FB} + Z_L}{1 + g_{m1}R_L} \tag{2.21}$$

And the gain can be described by

$$A_v = \frac{Z_{in}}{Z_{in} + Rs} \cdot \frac{-g_{m1}R_L}{1 + R_L/R_{FB}} \tag{2.22}$$

As the feedback resistance decreases, the gain decreases as the negative feedback effect forces the gain down.

Another useful topology is the common-gate topology. Looking into the source of the common gate, an impedance of approximately $1/g_{m1}$ is seen, thus by setting the transconductance to $1/R_S$, a theoretically perfect input match can be achieved by resonating out the parasitic input capacitance with an inductor [17]. Such topology is shown in figure 2-5 below.

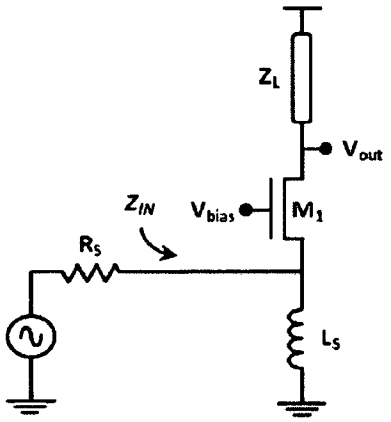

Figure 2-5. Common gate amplifier

Assuming that the parasitic input capacitance is resonated out by inductor L_s, then the gain can be described by

$$A_v = \frac{Z_{in}}{Z_{in} + Rs} \cdot g_{m1}R_L \tag{2.23}$$

It should be noted that for broadband frequency response, a low Q source inductor is required. Such architecture with a broadband input match offers a broad frequency

response, superior stability and robustness to PVT variation compared to the common-source structure [17]. Unfortunately, without the use of special techniques [18], the dependence of gain and NF on g_m is fairly restrictive, as the g_m must be fixed at $1/R_S$ for optimal input match [17]. Due to restrictions on g_{m1} for satisfying the input match, this topology is not suitable for variable-gain applications.

2.2.3 LITERATURE REVIEW

Variations on the shunt-feedback method have been quite popular for multi-band LNAs, due to their naturally broad frequency response. Some recent implementations are discussed below. Common-gate structures have also been employed for multiband and multi-gain LNAs, as they can be biased to provide a 50Ω match over a broad range of frequencies.

a) A 2.4 to 5.4 GHz Low Power CMOS Reconfigurable LNA for Multistandard Wireless Receiver [19]

This paper describes an LNA which employs variable gain with three parallel common source FETs, and variable centre frequency with a multi-tapped inductor. Broadband input matching is achieved with dual-reactive feedback technique for broadband matching as described in [11]. This design achieves a maximum 25dB of gain, a minimum -1dBm IIP3, a minimum 2dB NF with under 5mW power consumption with a 1V supply. The detriment of the dual-reactive feedback matching circuit is that it requires the use of an on-chip transformer, which is quite space consuming.

b) A 0.045mm^2 0.1-6GHz reconfigurable multi-band, multi-gain LNA for SDR [20]

This paper describes a circuit that employs a dual-LNA topology to cover a wide range of bands. Both LNAs employ active-resistive feedback networks, as is used in this work. Such a method does negatively impact linearity, but provides a high-quality input match

over a broad bandwidth while maintaining a low NF [13]. This also provides a degree of design freedom, where the designer could adjust the bias current to provide the most optimal input match and enhance linearity (with increasing bias current). The low-band LNA employs a simple resistive load for broad-band response from DC to 2GHz. The high-band LNA employs a multi-tapped inductor with a 3-bit switched capacitor bank for fine frequency tuning around bands cantered at 3GHz, 4.5GHz and 6GHz. Gain can be adjusted between 0dB (bypass mode) to 22dB, with a minimum noise figure of 2.7dB and a maximum IIP3 of -4dBm. A multiplexer at the output selects either the high or low band LNA outputs and provides some additional gain. This implementation is a very good example of the use of active-feedback, simple gain control and band switching for multiband/multi-gain implementations.

c) Reconfigurable Multiband Multimode LNA for LTE/GSM, WiMAX , and IEEE 802.11.a/b/g/n [21]

This paper describes a LNA with an inductively-degenerated common source gain stage (which consists of four parallel CS FETs for adjustable gain) and multiple selectable loads for various resonant frequencies. Input matching is achieved with three switchable series gate-inductors, which are in addition to the RF input bondwire, which was included in the design. Such a design selects the amount of inductance by bypassing or not bypassing the three on-chip series gate inductors. Such a technique provides excellent input matching and good noise performance, but with the drawback of large space requirements and high complexity. Two inductors were employed in the loads to cover the four bands, which range from 1.9GHz to 5.2Ghz.

Table 1 below summarily compares the performance of these three designs to the design presented in this thesis.

TABLE 1. PERFORMANCE COMPARISON

	[19]	[20]	[21]	This Work
Gain (dB)	11.0 to 25.4	12 to 22	5 to 17	5 to 16
Freq (GHz)	2.4 to 5.4	0.5 to 6	1.9 to 5.2	2.1 to 5.95
Number of Bands	5	6	4	16
NF (dB)	2.2 to 4.9	2.7 to 4.0	1.5 to 3.1	2.5 to 7.1
IIP3 (dBm)	-3.2 to 0.0	-10 to -4.4dBm	-19.6 to -16.2	-21.5 to -0.9
Power (mW)	3.6 to 4.7	12 to 31.2	3 to 5.3	6.7 to 12.6
Technology	TSMC 0.13μm	UMC 90nm	0.18μm	IBM 0.13μm
Size (mm^2)	0.49 (no pads)	0.045	N/A	0.58
Bandwidth Range (GHz)	Fixed	Fixed	Fixed	0.31 to 1.05

Note that [20] uses a resistively-loaded LNA to achieve coverage from 0.5GHz to 2.5GHz. Also note that in this work, the upper end of the noise figure exists in low gain (i.e. lowest transconductance) mode with negative resistance employed to achieve minimum bandwidth with 16dB of gain. Also, the worst case IIP3 exists at the highest achievable gain (16dB) at low bandwidth, which requires the most amount of negative resistance which is inherently nonlinear.

2.2.4 RECEIVER ARCHITECTURES FOR BROADBAND COVERAGE

It is well understood that LNAs must be designed to provide sufficient gain, low noise and low distortion while operating with sufficiently low power. Low noise is particularly important, as the LNA is generally the first active component providing gain in the system, and thus dominates the system noise figure. High linearity is required in order to withstand large in-band interferers such that the system can maintain high signal to noise and distortion ratio. In order to ensure low-noise performance, maximum power transfer, ensure stability, and to prevent desensitizing the pre-select filter, the LNA must provide a good input match.

A number of LNA design methods have been employed to cover a large range of frequency bands. Multiple radio receivers, each with a dedicated LNA can be designed to cover all required frequencies. With this topology, each receiver can be optimized to its own unique band, and overlapping of bands from receiver-to-receiver can yield broadband coverage with good performance. This issue with this method is that it is not

sustainable, as the size of the chip (and thus cost) will increase indefinitely as demand for spectrum coverage increases. Broadband implementations are one alternative to this. Broadband LNAs can provide flat gain over a broad range of frequencies, and can thus provide a classic receiver or SDR with signals in the desired range. The issue with broadband LNAs is that they amplify all signals over a wide range, which can cause a great deal of distortion products that can land near or on top of the signal of interest. As well, these amplifiers generally have lower gain, due to a bandwidth-gain-power trade-off. As well, this is not suitable for SDR as the ADC is sensitive to blockers and can saturate. The signal must be appropriately conditioned before reaching the ADC, such that the desired signal uses as much of the ADCs input voltage range as possible, while ensuring that noise, interferers and distortion products are minimal.

2.2.5 RECONFIGURABLE LNA FOR PSEUDO-SDR

Having looked at SDR in the literature it is apparent that it is not currently practical in the strictest sense. However, pseudo-SDR can be made practical with some front-end analog signal processing. Such an architecture is shown in Figure 2-6.

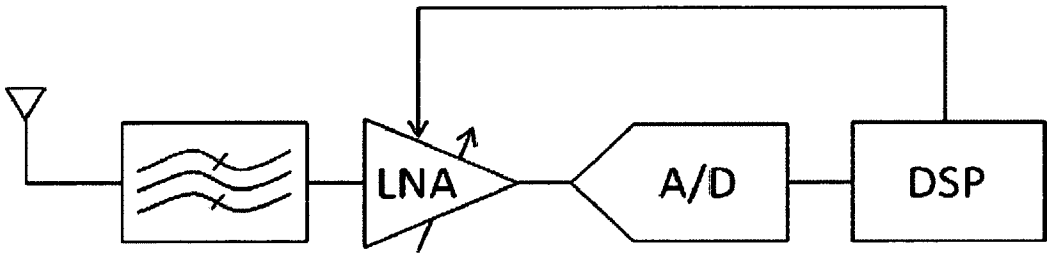

Figure 2-6. Pseudo-SDR architecture

True SDR would only consist of the antenna, A/D and the DSP. The reconfigurable LNA selectively amplifies signals from the antenna at a centre frequency, gain and bandwidth programmed by the DSP. The amplification and natural filtering provided by the reconfigurable-narrowband nature of the LNA is designed to minimize the total noise and

blocker power and maximize the fundamental signal is amplified. This ensures that the signal is conditioned for the ADC so as to achieve the best possible signal to noise and distortion ratio (SINAD). The broadband-preselect filter filters out frequencies above and below the highest and lowest achievable centre frequency of the reconfigurable LNA in order to minimize the effects of blockers and noise on the ADC. The ADC then digitizes the RF signal, and the resulting digitized signal can be further amplified, down-converted and filtered digitally by the digital radio programmed into the DSP. Once the digitized RF signal is processed by the digital radio, the DSP can process the baseband data. The function of the radio can be entirely configured through programming of the DSP and virtually any receiver architecture can be implemented in this way.

The LNA design approach described in the next section is geared to produce a final design that can help suit the front-end analog processing needs of the pseudo-SDR architecture.

CHAPTER 3

HIGHLY RECONFIGURABLE LNA DESIGN

In this chapter, the design process performed for the presented LNA will be discussed.

3.1 OVERVIEW OF THE LNA DESIGN

In order to overcome the issues mentioned for parallel radio architectures and broadband architectures, an adjustable bandwidth, gain, and centre frequency LNA has been designed and is reported in this thesis. Such an LNA can provide band-selective amplification and promote the rejection of out-of-band noise and blockers. This LNA was designed with the 1.8GHz band as a low end and the 5.5GHz band at the high end in mind. The design was not made with a specific radio standard in mind, but was designed to achieve reasonably-balanced performance (gain, noise figure, linearity, power consumption) throughout its full range of operation in the hopes to ensure a high degree of adaptability over a broad range of RF standards.

A resistive/active shunt-feedback input matching technique was employed in this design, to minimize the required chip space needed to provide an adjustable and broadband input match. Such a structure was chosen due to its small size, high gain, reasonable linearity and low noise, and its potential for a high-degree of reconfigurability. An inductively matched common source structure was deemed unsuitable due to its large size, and a

common-gate structure was also deemed unsuitable due to the difficulty of providing gain-control with this topology.

The proposed technique provides -10dB or better input match regardless of load and frequency. A negative g_m cell provides the user with control over the quality factor of the resonant load. A negative g_m cell grants the freedom to adjust the quality factor of the resonant load [22], [23], thus granting freedom to adjust gain and bandwidth. Variable gain was achieved with three common-source (CS) FETs (M_1) in parallel at the input. These FETs can be switched on and off to provide three discreet gain settings. Frequency selectivity was achieved with the use of a switchable quad-capacitor bank. A noise cancelling output stage was included for enhanced gain and noise performance [28], [29]. A simplified schematic of the reconfigurable LNA is shown in figure 3-1, below.

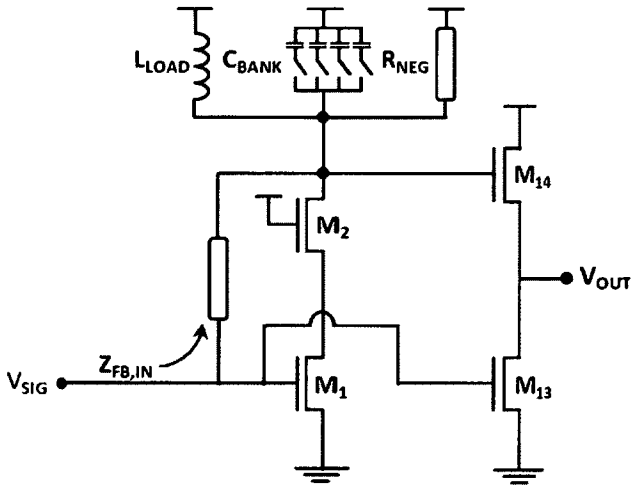

Figure 3-1. Simplified schematic of the reconfigurable LNA.

3.2 LNA DESIGN

In this section, the design process of the subject LNA will be presented.

3.2.1 VARIABLE GAIN STAGE

Variable gain functionality improves the dynamic range of the LNA. In this design, a switchable parallel gain-FET method was used. While it would be possible to combine this with continuous gain control, a discretely stepped gain control has advantages of simplicity, small-area and the ability to maintain constant current density for keeping noise figure at a minimum [20]. A simplified circuit diagram of this stage is shown in figure 3-2 below.

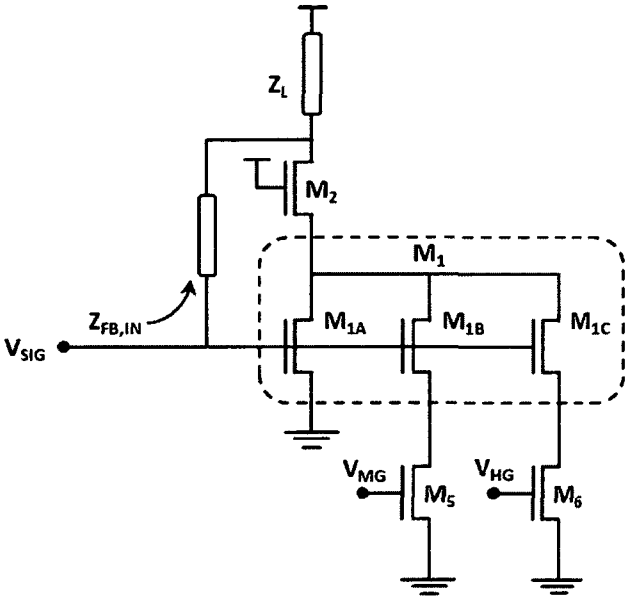

Figure 3-2. Variable gain stage.

Constant current density is desired as there exists an optimum density for lowest minimum noise figure (NF_{min}). In order to achieve absolute minimum NF_{min} in an amplifier, the transistor area must be set such that the optimal source impedance for minimum NF_{min} is equal to the desired source impedance.

The current density for lowest NF_{min} was first found through simulation by sweeping the bias current through a 20μm transistor with 5μm fingers, then plotting the NF_{min} vs. bias current. The experimental simulation setup was set up with a 20μm common source amplifier with 5μm fingers, a 200μm cascode FET with 10μm fingers (tied to VDD) and a 20mS output buffer. All FETs were minimum length, as is always maintained in the design process and a 1.2V supply was used. A current-mirror configuration was used to bias both the buffer and the common-source FETs. A resonant load consisting of a 1nH inductor in parallel with a 1.58pF capacitor and a 250Ω resistor was used to model a resonant load with an equivalent Q of 10. A 1nH inductor was selected as a reasonable design starting point, and a Q of 10 was chosen from a rough approximation of the expected losses in the switched capacitor bank in parallel with the inductor (it is known that inductors in this kit can achieve Qs of around 20). The optimal current density was found to be about 100μA per micron of gate width. By sweeping the drain current, and plotting NF_{min} versus drain current, the optimal current density for lowest NF_{min} was found, and is shown in figure 3-3 below.

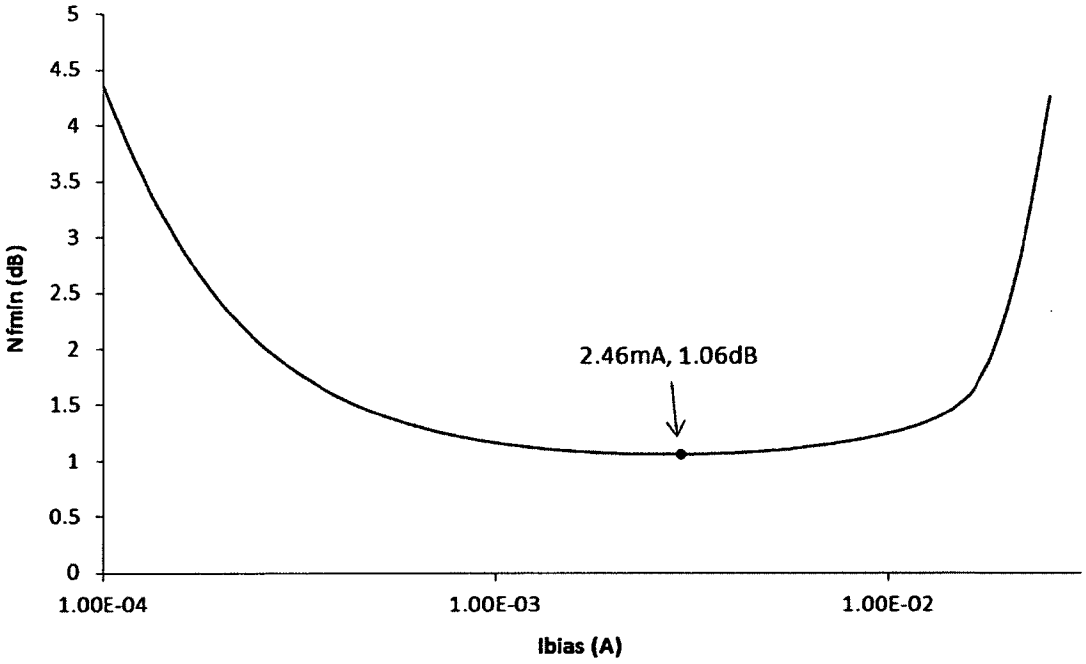

Figure 3-3. Minimum NF min for a 20μm CS FET

With a current of 3.15mA, the lowest NF_{min} is achieved, yielding an optimal current density of about 120uA/μm.

In order to find the optimal width for noise matching (to achieve absolute minimum NF_{min}), the width was swept while maintaining a constant current density of 120μA/μm until the source impedance for minimum NF_{min} reached 50 Ohms. On the Z-smith chart, this occurs when Γ_{opt} intersects the R=1 circle on the smith chart. It was found that the width for an optimal source impedance of 50 Ohms was 200um with 5um fingers, as shown in Figure 3-4. Given that a resistive feedback technique was used to provide a 50Ω input match, the gate sees the 50Ω impedance provided by the feedback mechanism in parallel with the 50Ω source. Thus, in actuality, the width should have been set to provide an optimal noise match at 25Ω, or when Γ_{opt} intersects the R=0.5 circle. This was an error made in the design process that can be considered for future work.

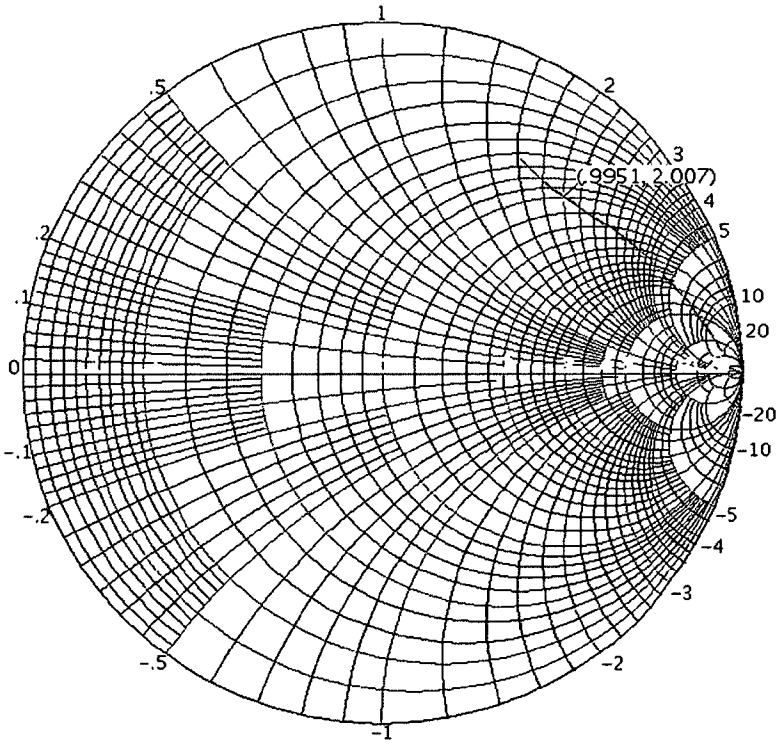

Figure 3-4. Γ_{opt} versus common source amplifier FET width

It was decided that the amplifier gain would be controlled in three discreet gain steps. The width of the primary gain FET was set to 100um, the secondary at 100um and the

tertiary at 150um. This base width of 100um was selected as the resistance for minimum noise swings evenly above and below 50Ω for low and high gain settings, and very nearly 50 Ohms for medium gain setting.

Based on these results, it was decided that the current density of about 15μA/μm was acceptable, as the 0.8dB increase in noise figure was quite minimal for a large saving in current.

As shown in Figure 3-2, three parallel FETs were sized at relative ratios of 1:1:1.5 for M_{1A}, M_{1B}, and M_{1C} respectively. These sizes were selected through simulation to ensure consistent gain steps from low to high gain, at about 2.2 dB per step. M_{1A} has its source tied directly to ground. The sources of M_{1B} and M_{1C} are tied to bypass FETs, which are switched on and off externally to adjust the total width and bias current which both determine the transconductance of the gain stage. Upon activation, these bypass FETs operate strongly in the triode region, which provides a linear low-impedance path to ground. These bypass FETs were sized at minimum length and 100um width with 5um fingers, which gives a reasonably low resistance of 5 ohms. Such low resistance also ensures a minimized impact on noise performance.

The cascode transistor was sized at 200um with 10um fingers at minimum length. This transistor is used to provide a low impedance seen from the drain of the common source amplifying FETs. A low impedance cascode source-drain ensures that minimal voltage is generated on the drain of the common source amplifying FET, such that the miller effect is minimized. The miller effect increases the effect of the drain-gate feedback capacitance of the CS FET thus reducing the broadness of the frequency response (lowers f_T and the gain cutoff frequency). There is a tradeoff with increasing the size of the cascode FET: the drain parasitic capacitances increase, thus reducing the maximum resonant frequency. The size was selected to provide a reasonable balance between the source-drain impedance and the maximum resonant frequency. This cascode FET was also tied to VDD throughout the design process, but in the implemented layout it was connected to an external pin for external bias control. This design choice was made because the gate bias can be adjusted to maximize the amplifier's linear output swing, thus maximizing the linearity of the LNA. This is to be considered for future work.

3.2.2 CONTINUOUSLY ADJUSTABLE ACTIVE SHUNT-FEEDBACK CIRCUIT

The shunt feedback matching technique has been proven to be effective for tunable narrowband circuits that may cover a relatively wide range. In this design, a shunt active/resistive feedback configuration was employed. This consists of an externally biased source follower in series with a 140 Ohm resistor (R_{FB}) in the feedback path, as seen in Figure 3-5, below.

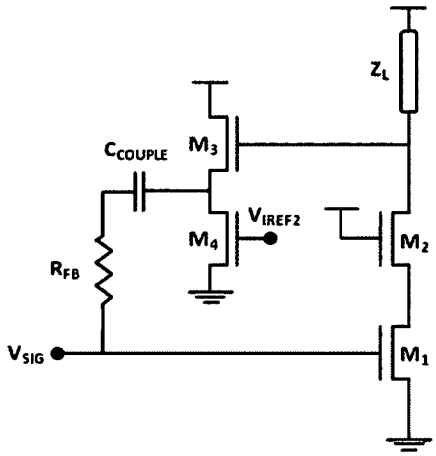

Figure 3-5. Active/resistive shunt-feedback circuit.

The function of this feedback circuit is essentially the same as with normal resistive feedback circuits, except that the output current is blocked from the feedback path by the gate of the feedback transistor. This design improves the amplifier gain and provides input matching reconfigurability, but with the drawback of reduced linearity performance due to the introduction of an active component in the feedback path.

The input impedance and gain for this circuit can be approximated by

$$Z_{in} = \frac{\left(R_{FB} + \frac{1}{g_{m3}}\right)}{1 + g_{m1}R_L} \tag{3.1}$$

and

$$A_v = g_{m1}R_L\left[\frac{R_{FB} + 1/g_{m3}}{R_{FB} + 1/g_{m3} + Rs(1 + g_{m1}R_L)}\right] \quad (3.2)$$

respectively. g_{m3} and g_{m1} is the transconductance of the feedback FET and common-source amplifying FETs respectively. R_L is the equivalent parallel resistance of the tuned resonant load, and R_{FB} is the resistance of the fixed feedback resistor. It can be seen that the dependence of gain on the feedback resistance is weakened when the source follower is used in the feedback path. This can be described by the fact that the output is not loaded by the series combination of the source resistance and feedback resistor, due to the isolation by the gate of M_3. The gain is reduced by the feedback action for a nonzero source resistance.

The source follower M_3 (with controllable current bias) provides the extra degree of freedom which is required to maintain a good input match regardless of load and transconductance of M_1. The drawback to using active feedback is that it introduces extra nonlinearity to the amplifier. In order to minimize the issues with nonlinearity, transistor M_3 is biased at V_{DD}. In addition, by placing a resistor in the feedback path (located between the source of the feedback source follower and the input of the LNA), the voltage gain of M_3 gets closer to unity due to an increase in load resistance and a required increase in g_{m3} as per (3.1), thus causing the maximum gate-source deviation on this FET to be reduced thereby enhancing its linearity. Noise is also impacted by the feedback resistance and decreases with increasing feedback resistance. As the feedback resistance is increased (as desired for high linearity and low noise), the minimum input impedance for a given load impedance (the effective load resistance changes over frequency due to frequency dependent load-Q) and g_{m1} is also increased. Therefore, the feedback resistor should be set in such that the feedback matching circuit can accommodate a 50Ω input impedance for all gains and frequency bands. Through simulation, a 140Ω feedback resistor (R_{FB}) was found to be optimal to minimize noise and maximize linearity while maintaining less than -10dB S11 over all of the operating points. The width of M_3 was set to 100μm, as this was large enough to provide low enough current for the required range of transconductance, while not being so large that it reduces the resonant frequency of the load too drastically.

An inductive/capacitive tuned load is used, which has a Q factor dependent on frequency. The effective load impedance at the operating frequency can be expressed by

$$R_L = wLQ||R_{p,cap}||R_{neg} \quad (3.3)$$

where $R_{p,cap}$ is the effective parallel resistance of the tuned capacitor bank at resonance, and R_{neg} is the effective negative resistance of the negative resistance cell (is negative in value). As shown in (3.1), g_{mFB} can be adjusted appropriately to achieve 50Ω at the input. The selected inductor's peak Q is just beyond 5.5GHz, thus as frequency increases, the R_L increases accordingly. For example, as frequency and gain is decreased, g_{mFB} must increase to maintain R_{in} of 50 Ohms. An increase in the feedback FETs' current results in an increase in linearity, which is advantageous when dealing with larger signals and a lower required gain. Unfortunately, g_{mFB} must be reduced with increasing frequency in order to stay matched, which indicates that linearity could be worse at higher frequencies.

Linearity simulations were performed for the two gain extremes: at the highest frequency band and highest gain setting, and the lowest frequency band at the lowest gain setting. The test bench was set up with emulation of the effect of the input signal on the source of the feedback FET M_3. This was modeled as an RF port in series with R_{FB} with a signal power lower than the signal power at the gate of M_3 by the gain from the signal source to the output of the cascode stage. The signal power at the gate of M_3 is simply the input signal voltage times the voltage gain from the signal source to the cascode output (to be called A_v^1), which is 6dB greater than the LNA gain due to the roughly 6dB voltage loss of the output buffer. Power was not applied directly to the gate of M_3, but a voltage of $-V_{sig} \cdot A_v^1$ is applied and swept. The output power is measured from the source of M_3 to ground, with a port that is isolated from the circuit by a unity-gain voltage controlled voltage source. The results of the two linearity measurements are shown in Figure 3-6 below. The input power in this plot is referred to the power of the signal source.

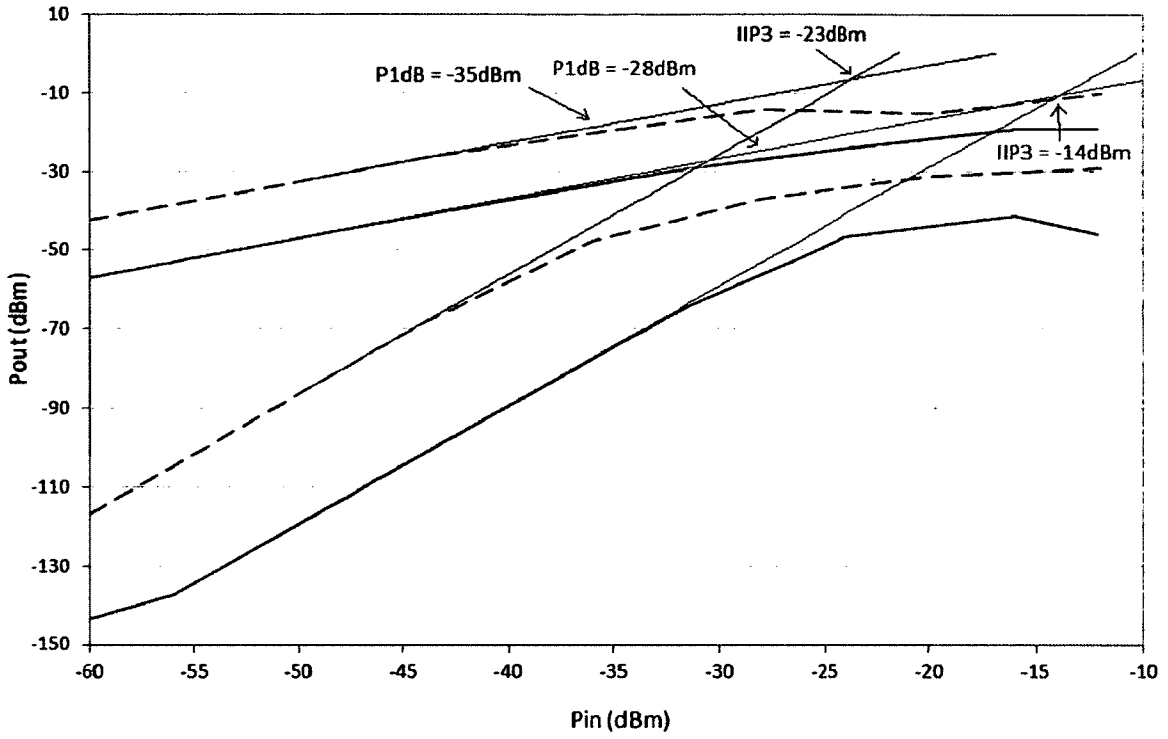

Figure 3-6. Linearity of the feedback source-follower for high gain at the highest frequency band (dotted line), and low gain at the lowest frequency band (regular line), with power referred to the signal source

It can be seen in figure 3-6 that the higher gain case results in lower linearity, as expected. The loss in linearity (13dB between P1dBs) is virtually equivalent to the increase in gain, as the LNA gain for the low gain case is 3dB and 16dB for the high band case. Thus, the linearity of the LNA is limited to these two extremes.

3.2.3 TUNABLE NEGATIVE RESISTANCE LOAD

Variable bandwidth RF components provide SDR systems with the ability to adapt to a variety of RF standards. Including this functionality in LNAs can help reduce total noise and blocker power, hence improving SNR and thus reducing the requirements for filtering further down the chain. This leads to reduction in chip space, cost and power consumption. The bandwidth and gain of an inductive load is directly proportional to its

effective parallel resistance (R_P) at resonance. The bandwidth is determined by f_c/Q, where $Q = |R_P/Z_L|$, and the gain is determined by $-g_{m1}R_L$, where f_c is the centre frequency. If the transconductance of the amplifier along with the effective parallel resistance of the load can be adjusted independently, then the bandwidth can be adjusted. By employing a negative resistance cell in parallel with the tuned load, the effective parallel resistance can be increased to a degree dictated by the transconductance of the negative g_m cells' gain FETs (M_7 and M_8). This particular topology was chosen due to its simplicity, low power requirements and low chip-space requirements.

The impedance of this device is described by

$$R_{neg} = -\frac{1}{g_m^2 R_x} \tag{3.4}$$

and the effective parallel resistance is

$$R_{P,eff} = \frac{Q_L Z_L}{1 - Q_L Z_L * g_m^2 R_x} \tag{3.5}$$

where $g_{m7} = g_{m8} = g_m$. The schematic of this cell is shown in Figure 3-7 below.

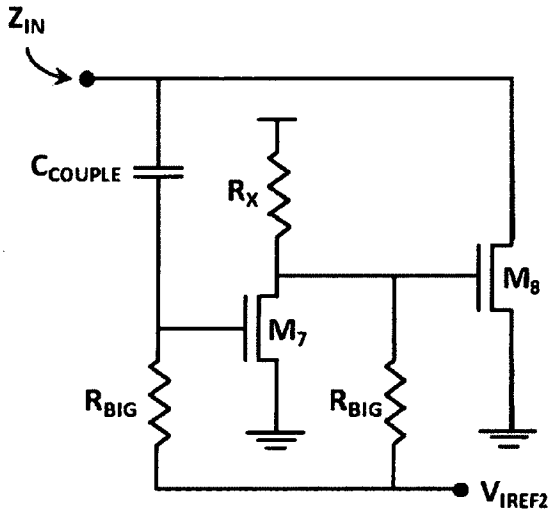

Figure 3-7. Tunable negative resistance circuit

This topology functions on a simple positive-feedback transconductance premise, and it functions as follows. Transistor M_7 with resistor R_x provides inversion and amplification of the applied voltage by $-g_mR_x$. M_8's output current tracks the input voltage swing by transconductance g_m. This mechanism generates an increasing output current for decreasing applied voltage, and a decreasing output current for an increasing applied voltage. It is necessary to ensure that the transconductance is not set too high, or the effective parallel resistance will go negative, and could cause oscillation. The transistor widths were chosen to be 10μm with minimum length of 0.12μm. The sizes were kept small in order to minimize capacitive loading at the resonant load so as to minimize the impact on the resonant frequency and maintain highest possible tuning range. Also, maintaining a small gate capacitance reduces deviation from the ideal 0^o output current to input voltage relationship of M_7 and M_8. As the current-to-voltage relationship deviates from this ideal, so does the value of the negative resistance and the impedance adopts an increasingly capacitive component. The load resistance was chosen to be 800Ω as this sets a reasonable balance between the linearity and the required maximum current (and thus maximum required power consumption) for the maximum desired value of negative resistance. In other words, as the drain current increases, the required Rx for a given value of negative resistance decreases proportionally, as R_{neg} is proportional to $I_dR_x^{-1}$ and transistor M_7 and M_8 are pushed more heavily into the saturation region, enhancing linearity since the same drain-source voltage drop across M_7 is maintained. The negative resistances have an achievable range approaching negative infinity (at bias current approaching zero) up into the negative tens of Ohms with bias current approaching 1mA. This grants more than enough range of operation to cover the desired range of load resistances. Unfortunately, due to high frequency effects, the full range of negative resistance is not achievable, as the phase shift from input voltage to output current deviates from the ideal 180 degrees. By reducing the size of the FETs further, the parasitic capacitances of M_7 and M_8 would be reduced and thus the performance at high frequencies could be enhanced. This would be considered for future work.

The linearity of the negative resistance load can be analyzed. For the test bench, the output current of M_8 was isolated from the input test voltage by a unity gain voltage controlled voltage source. The voltage source was implemented as an RF port with a

0.1Ω source resistance, to ensure that virtually all of the voltage reaches the gate of M_7 (and drain of M_8).

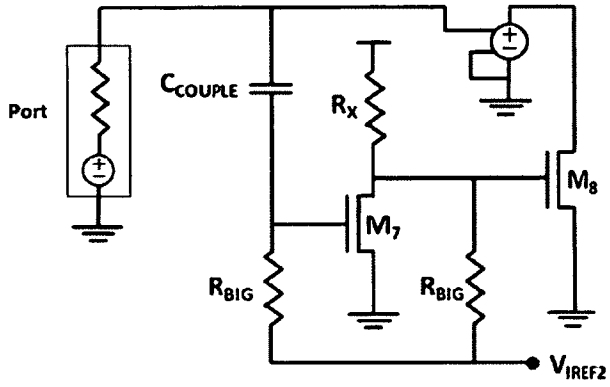

Figure 3-8. Linearity test-bench for negative resistance circuit

Figure 3-9 below shows the simulated linearity results of this circuit at 3GHz over various bias currents, plotted in terms of RMS output current in dB-mA and RMS input voltage in dB-mV.

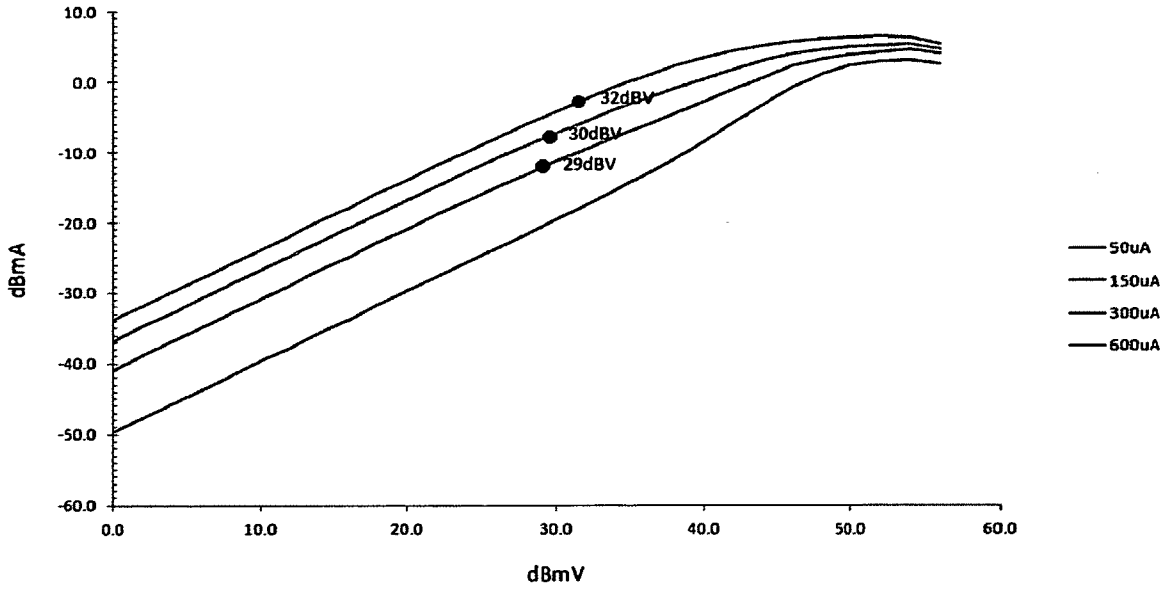

Figure 3-9. Linearity results for selected negative resistance bias currents

The third order intercept points were found to be very close to 14dB beyond the 1dB compression points for two tone tests. The enhancement of linearity with increasing negative resistance is apparent here. The 1dB compression point for the 50uA case is not shown, as the curve trends upwards prior to dropping, making the P1dB artificially high. These compression points (and curves) can be referred back to the input power with the knowledge of the gain of the LNA and the equivalent parallel load resistance of the resonant load. The input power for a given load voltage swing would be $10\log\left(\frac{10^{\frac{dBmVload-60dB-Av}{10}}}{Rin}\right)+30$ in dBm, where R_{in} is 100Ω for a matched amplifier. The worst-case scenario is at the highest operating frequency where Q is highest and the gain is maximum and thus voltage swing at the load is maximum, as reported in section 3.3; at this operating point, the gain of the LNA is 16dB. Approximating a 6dB RF voltage loss across the output buffer stage, the gain from the source to the resonant load would be expected to be 22dB. This would indicate that for the three compression points listed in Figure 3-9, the resulting source–referred P1dBs would be -40dBm for 600uA, -42 for 300uA and -43dB for 150uA. These linearity values are rather low, so some improvements could be made in enhancing the linearity by exploring different techniques for generating negative resistance, or by optimizing this design.

Negative resistance/conductance cells have previously been used in LNAs to provide Q-enhancement [22], [23]. Other negative resistance topologies as shown in [23] were considered, but the chosen topology was selected due to its ideally non-frequency dependent negative resistance. For future work, the two single-ended topologies illustrated in [23] should be further analyzed and compared to the implemented topology to determine if their performance could surpass that of the implemented negative resistance. The frequency-dependent nature of the topologies discussed in [23] could in fact be made useful for maintaining gain flatness across all frequency bands.

3.2.4 INDUCTIVE LOAD

An inductive load is necessary for achieving frequency selective gain, which can be achieved by using the resonant nature of parallel capacitor-inductor pairs. A number of inductor dimensions are available for adjustment in order to adjust the trade offs. Larger inductor metal widths realizes lower loss and thus higher Q, but at reduced inductance and lower self resonant frequency (SRF), due to increased self-capacitance and coupling to the substrate. Larger outer dimension (i.e. bigger loop diameter) yields higher inductance, but lower self-resonant frequency due to increased inductance and self-capacitance. Larger number of turns increases the inductance, but also increases self capacitance, and thus has a lower SRF than an equivalent inductor with less turns and larger area.

The inductive load was initially designed to be 1nH with the peak Q as low in frequency as possible with the intent to land it in the middle of the frequency tuning range. This value of inductance was chosen, as this inductance would resonate with the approximated 750fF net load parasitic capacitance to produce the desired 5.5GHz maximum peak S21 frequency. This net load parasitic capacitance includes the capacitive parasitics of the cascode transistor, the feedback source follower, the output buffer, and the four disabled capacitor bank switching FETs. Setting the peak Q of the inductor to the centre of the tuning range is desirable, as this would create the best condition for maximum gain flatness across the S21 peaks of all 16 bands. The turns were set to 1.5 in order to avoid the need for a long underpass. The outer dimension was maximized at the 300um limit in order to bring the peak Q frequency down, then the metal width was set to the maximum 25um to bring the peak Q down and bring down the inductance, which (in combination with switchable capacitor bank) should grant a reasonable frequency tuning from 2.5GHz to 5.5GHz. This procedure was followed in order to achieve low peak-Q frequency, and high peak Q value. A 1.5 turn inductor with a 300um outer dimension, 25um metal width, default (minimum) underpass width of 15um, and a (un-modifiable) 5um line spacing was designed. The response for this inductor is shown in figure 3-10 below.

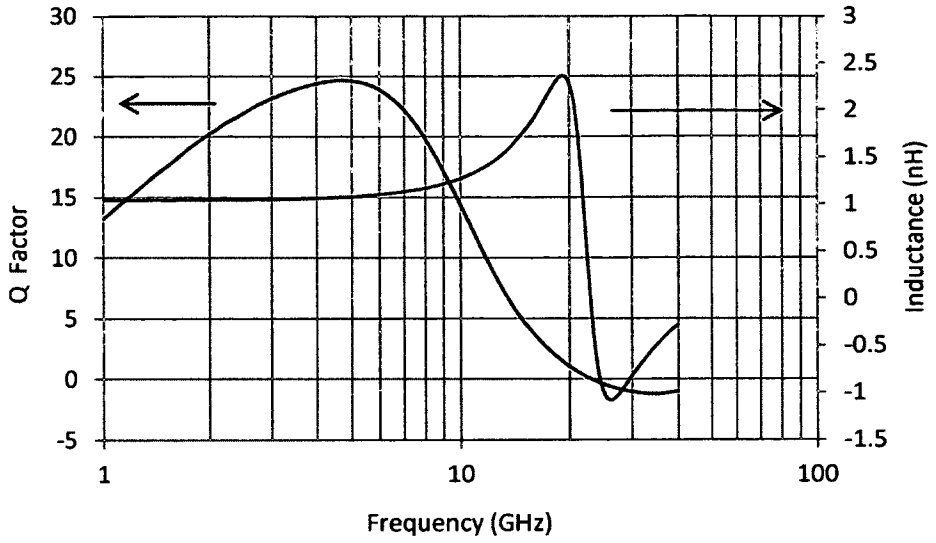

Figure 3-10. Q and Inductance of desired inductor

The peak Q frequency for this inductor exists at about 4GHz, near the center of the desired frequency tuning range. It can be seen that the inductance increases with increasing frequency, which can potentially cause a reduction in the maximum achievable frequency tuning range. In this case, the inductance shifts by a reasonably low 0.03μH between 1.8GHz and 5.5GHz which a 3% change, and is thus of little concern. This can be attributed to the fact that the SRF (about 24.5GHz) is quite a bit higher than the high-end of the tuning range.

Unfortunately, due to space constraints in the layout, this large of an inductor could not be used. These space-constraints were encountered, as the majority of the LNA was laid-out prior to including the inductor, and the dimensions of the laid-out LNA did not permit such a large inductor with guard ring; with some re-design, it could be possible to fit such an inductor; this would be considered for future work. As a result, the outer dimension was reduced to 170μm, and the metal width to 5um. With these dimensions, the ground ring size was manageable, and the inductance was reduced to 760μH to account for additional layout parasitics. Unfortunately, due to these changes, the peak Q frequency lies beyond the high-end of the tuning range, and thus amplifier gain reduces with decreasing frequency. The response of this inductor can be seen in Figure 3-11 below.

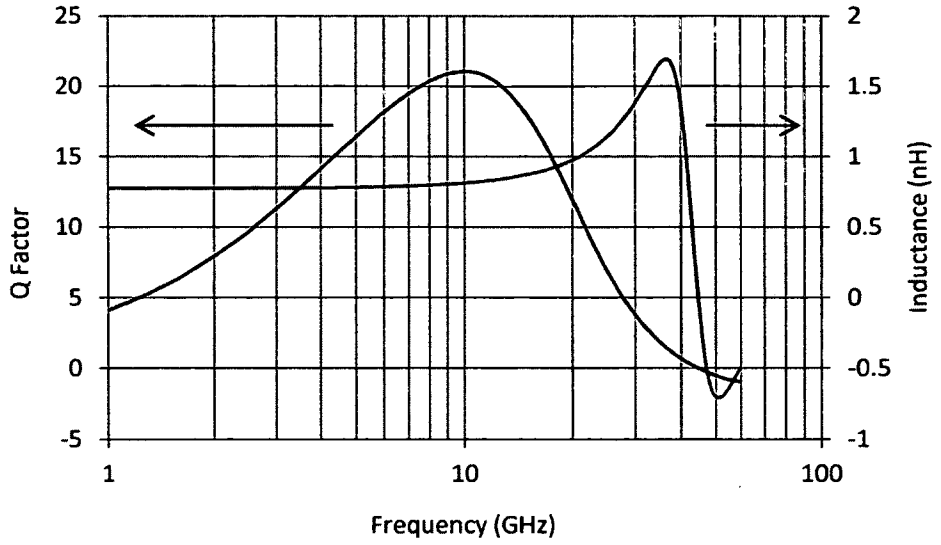

Figure 3-11. Q and Inductance of used inductor

The Q factor shifts from 10.0 to 17.3 over the tuning range of 2.5GHz to 5.5GHz, with a peak Q of 21 at 10GHz. The inductance shifts from 750pH to 830pH over the whole tuning range. It was desirable to increase the metal width further beyond 5um in order to achieve lower peak Q frequency and higher peak Q value, but this would have required an increase in inductor area to maintain the inductance value.

3.2.5 SWITCHABLE CAPACITIVE LOAD

A switchable capacitor bank realizes the tunable frequency component of this amplifier. This switchable bank incorporates FETs as switches to enable or disable individual capacitors, as illustrated in Figure 3-12.

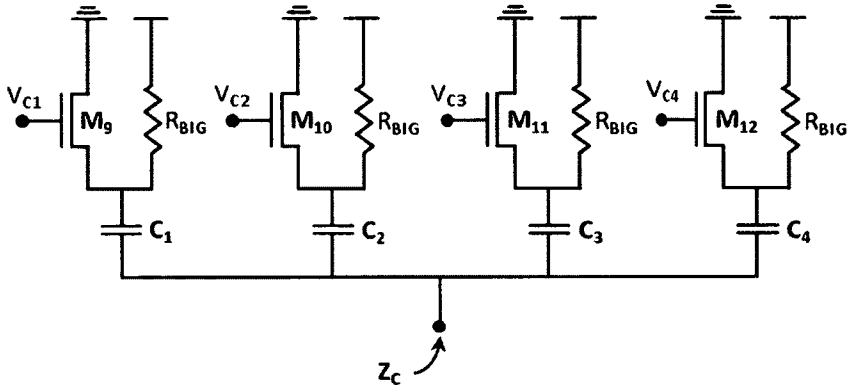

Figure 3-12. Switchable capacitive load for frequency tuning

Such a topology was chosen due to its small size and ease of integration, and provides 16 discreet bands. The other most applicable candidate for frequency tuning would be to use multi-tapped inductors as used in [20] and [19], but such a design would require custom-designed inductors that are not modeled in the process. Such custom-designed inductors would require the use of a 3-D electromagnetic simulator to generate a working model, and this is beyond the scope of the intended thesis work. Varactors were not considered as the main frequency control device, as the tuning range of varactors in this process is not wide enough to cover the desired frequency range. It should be noted that the use of a single varactor was considered to help provide a more continuous frequency tuning between the 16 distinct frequency bands, but was rejected as there were not enough available pads on-chip, and the addition of this capacitance would reduce the frequency tuning range. Capacitor banks for frequency tuning in LNAs have been successfully used in other designs [24], [21], [25]. The values of the four capacitors in the capacitor bank were chosen to provide binary weighted frequency transitions across all bands, and are shown in table 2, below.

TABLE 2. SWITCHABLE CAPACITOR BANK VALUES

C1	C2	C3	C4
3.70pF	1.41pF	748pF	360pF

M_9 through M_{12} are the switches (RF NFETs), which provide low-resistance paths to ground or open circuits for the RF signal that is applied to C_1 through C_4. The R_{BIG} resistors are each 10KΩ, and were intended to provide a low-current DC bias to the switching FETs, and provide a good RF choke when switched off. It was realized after the design submission that these resistors weren't required, as the channel simply needs to be inverted in order to provide a low-resistance channel without the need for any DC current flow. Regardless, their impact on performance (gain and noise figure) is minimal. V_{C1} through to V_{C4} are the switch control voltages, which pull the gates to ground to switch the transistors off, and apply a 1.2V for a strong overdrive for lowest drain to source resistance. Enabled capacitors add in parallel and resonate with the inductor at a frequency equal to $2\pi\sqrt{LC_{total}}^{-1}$. C_{total} includes the bank capacitors as well as the parasitic capacitances due to all FETs connected to the drain of M_2, including the parasitics of disabled capacitor bank switch FETs. The quality factor of these capacitors is determined by the ratio of the impedance of the capacitor to the series impedance of the switching FET channel. The effective parallel resistance is expressed in (2.3). The switching FETs were sized at 130μm with 6.5μm fingers at minimum length to achieve a reasonable balance between load-Q and tuning range. This gives a channel resistance of 3.7Ω.The quality factor of the capacitor bank was measured for all 16 discreet capacitances, at the appropriate resonant frequencies:

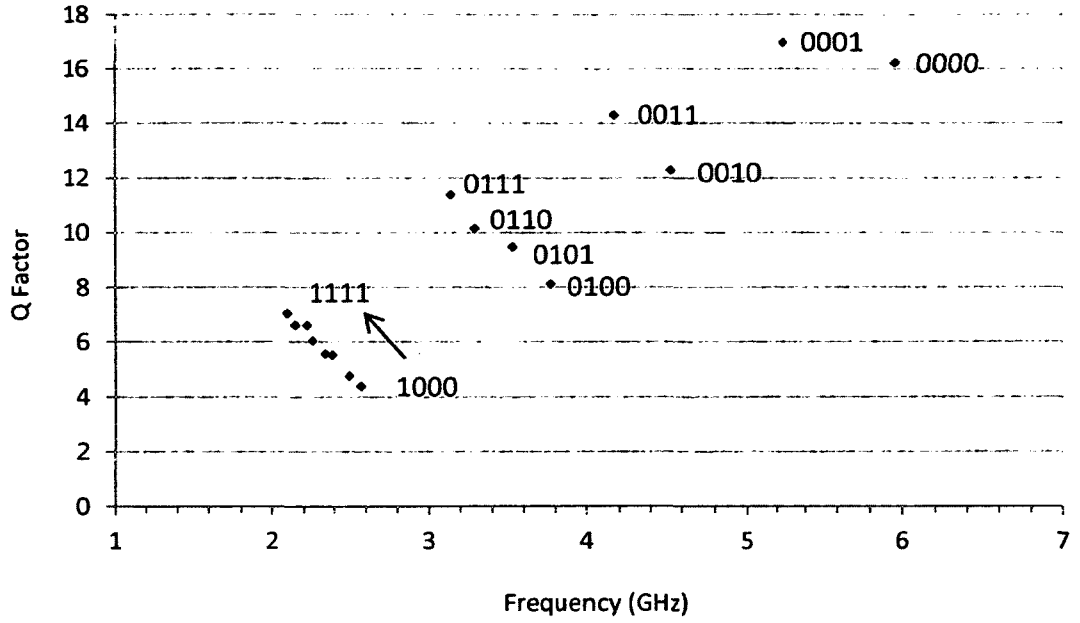

Figure 3-13. Simulated Q vs. resonant frequency of the tunable resonant load. The numbers shown beside the points indicate the 4-bit digital frequency control word of pins V_{c1} through V_{c4}.

The four distinct trend lines that are apparent in Figure 3-13 exist due to increasing capacitor impedance with decreasing resonant frequency, as resonant frequency reduces by $1/\sqrt{C}$, and impedance reduces faster, by 1/C. The discreet jumps in Q that occur between these four distinct trends occur due to the introduction of a lower Q capacitor-switch pair.

Instead of using the same switch sizes for each capacitor in the bank, one could choose to size these switches to help mitigate this Q reduction with reducing frequency. With the Q flat across frequency, the equivalent parallel impedance of the capacitor bank will increase with decreasing frequency, as this resistance is directly proportional to $1/\sqrt{C}$ for a resonant tank. The inverse is true for the inductor, where its parallel resistance is proportional to $\sqrt{L}$ for a resonant tank. The inductive loads' quality factor curve also increases with frequency; therefore this could potentially be mitigated by a negatively sloped capacitor Q vs. frequency curve, though this would require unreasonably large switching FETs, which reduces the frequency tuning range and can become space-

prohibitive. Given an inductor with a peak Q frequency in the centre of the tuning range, having a flat Q response would be quite desirable. This would make for a reasonably flat peak S21 over all 16 bands. Such a flat response can be achieved with some adjustment of the capacitor switching FETs. Through optimization in Cadence Virtuoso, the widths required to achieve relatively flat Q across all bands was solved for. These (nearly) optimal widths are as follows:

TABLE 3. OPTIMIZED SWITCHABLE CAPACITOR SWITCHING FET WIDTHS

M_9	M_{10}	M_{11}	M_{12}
603μm	307μm	188μm	140μm

With these widths and the inductor used in the final design, the curve for capacitor bank Q as shown in Figure 3-14 is achieved.

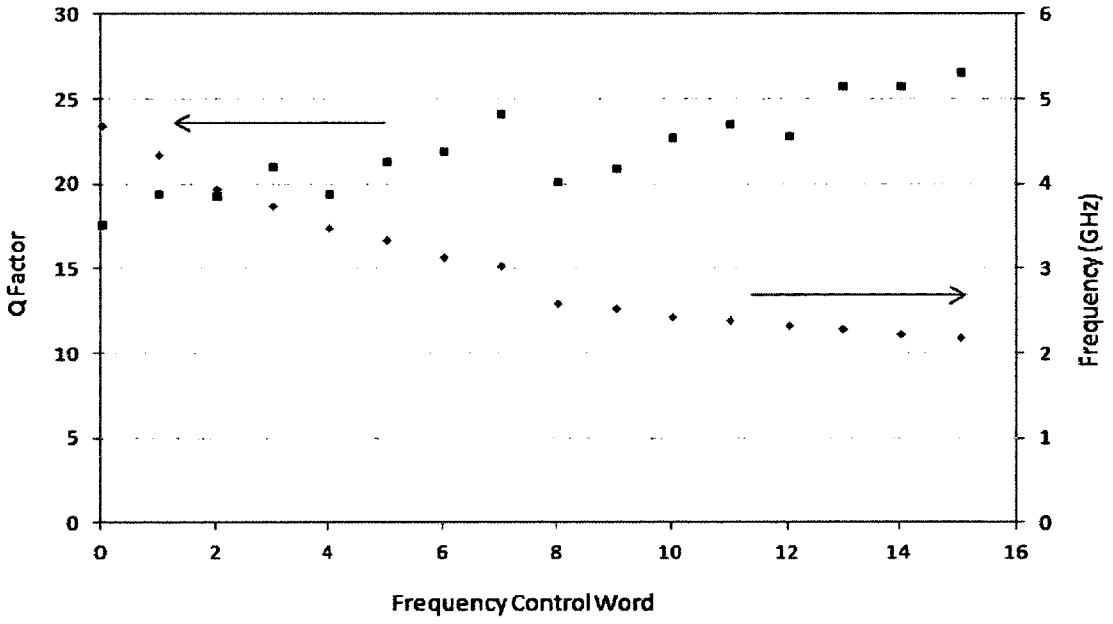

Figure 3-14. Q factor and frequency versus frequency control word of the resonant load with a capacitor bank optimized for gain flatness

This optimization was achieved with a 30% reduction in frequency range, with the highest achievable peak S21 frequency reduced from 5.8GHz to 4.8GHz (in schematic

level simulation). The slope of Q vs. frequency has been reversed in this optimization, which helps to compensate for reducing inductor Q with decreasing frequency. With the optimized capacitor bank and the inductor used in the final design, the resulting S21 vs. frequency was calculated.

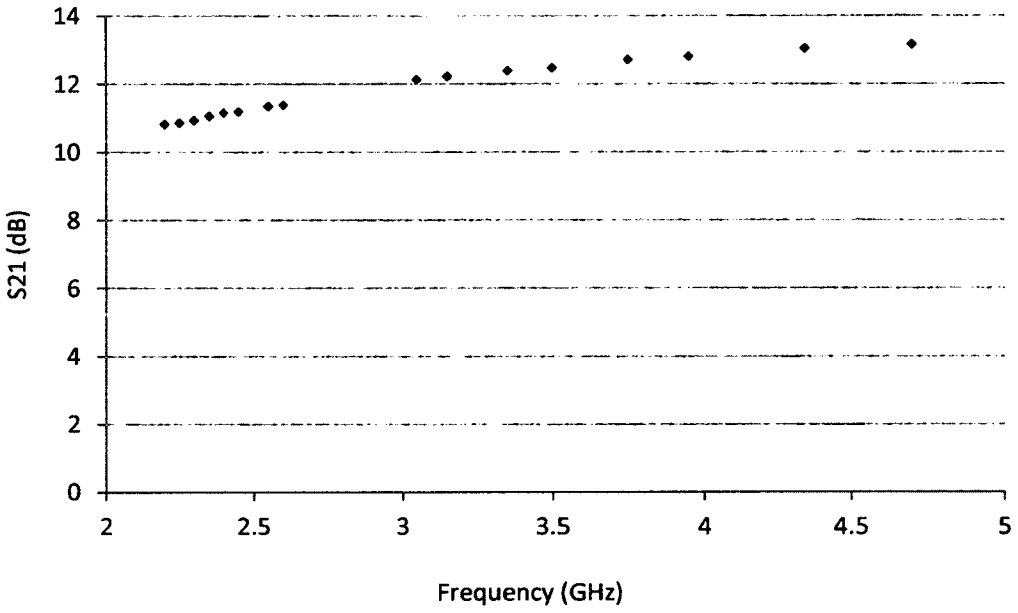

Figure 3-15. Simulated S21 versus resonant frequency with capacitor bank optimized for gain flatness

Observing Figure 3-15, it can be seen that the gain deviation across the band is now a reasonably low 2.34dB, due to the optimization of the capacitor bank transistors.

It should be noted that with layout parasitics included, this frequency range will be reduced even further, so it would be wise to design for a higher frequency than the desired target frequency by reducing the load inductance. As well, the deviation in gain over frequency can be further reduced by using a lower peak-Q inductor.

3.2.6 NOISE CANCELLING OUTPUT STAGE

The output stage benefits performance by improving gain and cancelling out noise generated by the primary gain FET, M_1 [28]. Common source transistor M_{13} is placed in parallel with M_1, and provides gain of $-g_{m13}/g_{m14}$. Source follower M_{14} buffers the output and provides a 50Ω output impedance for measurement. The gain between gate and source terminals is approximately unity for M_{14}. The noise cancelling phenomena can be explained as follows. Noise current generated in M_1's channel generates a noise voltage at the output of M_2, and a lesser noise voltage at the input due to the feedback action of Z_{FB}. Transistor M_{13} amplifies and inverts the input signal along with this input noise voltage. The source of M_{14} follows the signal at the output of M_2 along with the output noise voltage. Signal amplified by M_{13} and M_{14} is in phase at their outputs, whereas the noise is out-of-phase. These inverse noise voltages sum at the V_{OUT} node and subtract one another, while the signal sums in phase. The noise cancelling stage can be seen in Figure 3-16. The low frequency gain of the entire LNA is summarized in (5), where Z_L is purely real at resonance.

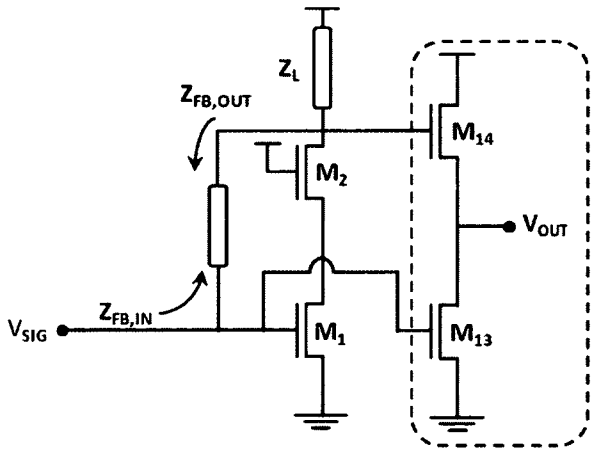

Figure 3-16. Noise cancelling output stage

3.2.7 COMPLETE LNA CIRCUIT DIAGRAM

The top-level LNA circuit diagram can be shown with all of the previously discussed circuit blocks, and can be seen in Figure 3-17. In this circuit diagram, current mirrors and some DC blocking capacitors and biasing resistors are not shown.

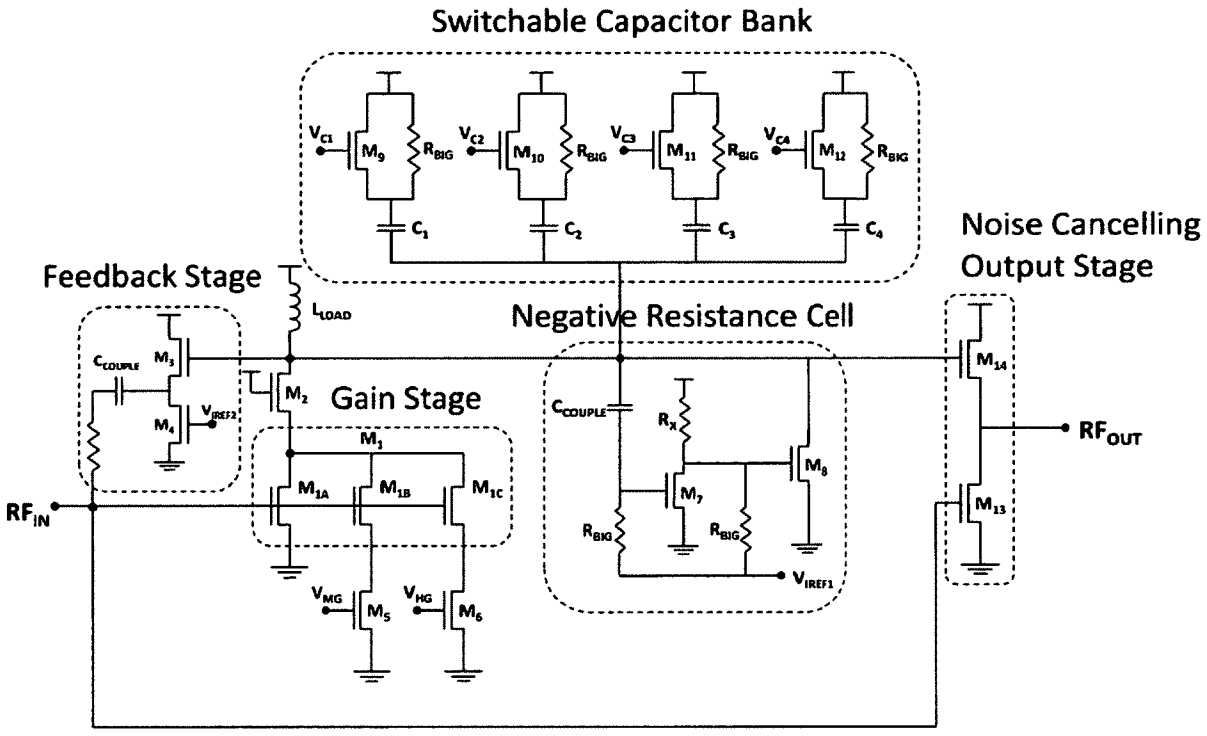

Figure 3-17. Complete LNA circuit diagram

3.2.8 LNA IC LAYOUT

The layout of the LNA was designed with the goal of minimizing parasitic elements on signal lines by keeping them a short as possible, and reasonably balancing the width to length ratios of the lines, in order to optimize the balance between parasitic capacitance and series resistance. In RF, it is generally not optimal to use minimum-width lines, as is generally done in digital design. This is the case, as components are generally much larger and as a result are less tightly spaced. For larger signal routing distances, upper-

layer metals should be used because the sheet-resistances of the upper layers are generally lower. Power and ground lines are made very wide to reduce voltage drop along the power traces, to ensure that all components have solid ground and supply connections. Also, this increases coupling to the substrate and other nearby DC lines, helping to minimize noise on these lines. Power and ground are also decoupled with large MIMCAPs which are placed as close as possible to the LNA, in order to provide a path for noise currents thus preventing the generation of noise voltages in the LNA. RF grounds are connected to the DC ground, and are effectively grounded through these large MIMCAPs. For DC lines used to provide gate-bias voltages, the thickness of the lines is not too much of an issue because there is virtually no DC current flow; these lines should be decoupled at the gates of the FETs that they are biasing in order to minimize noise and decouple line-inductances. This is particularly important if the voltage is supplied off-chip, as bond wires are high in inductance (on the order of 1nH/mm of bondwire length) and can thus effect the circuit behavior at RF frequencies (e.g. can generate negative resistances, which can cause oscillations). ESD protection is applied to all dc and signal pads in order to protect the circuit from ESD spikes which can be applied by equipment and human contact.

A screenshot of the layout of the LNA, a microphotograph of the fabricated LNA, and a photograph of the chip on the custom-designed breakout board can be seen in figures 3-18 through 3-20 below.

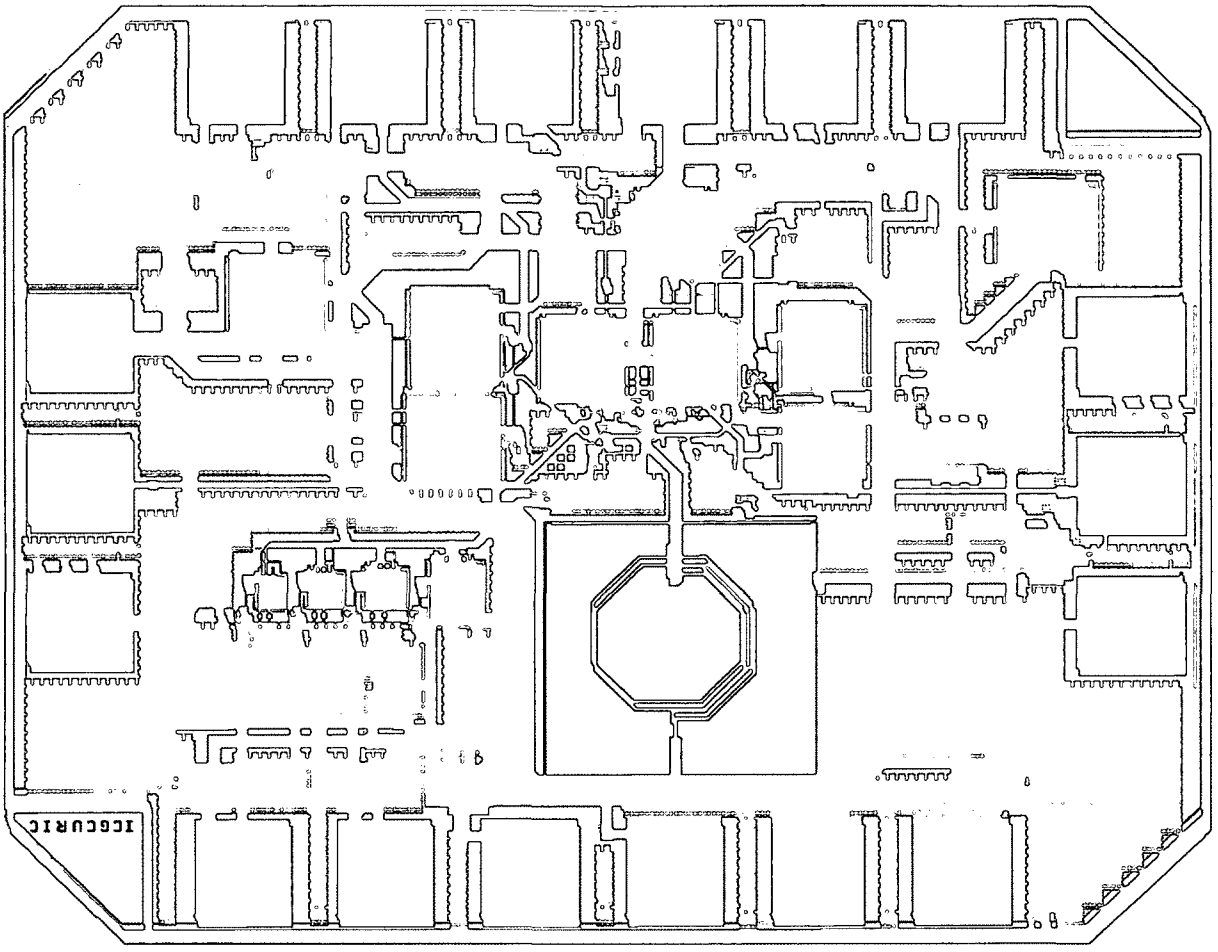

Figure 3-18. Screenshot of the LNA layout

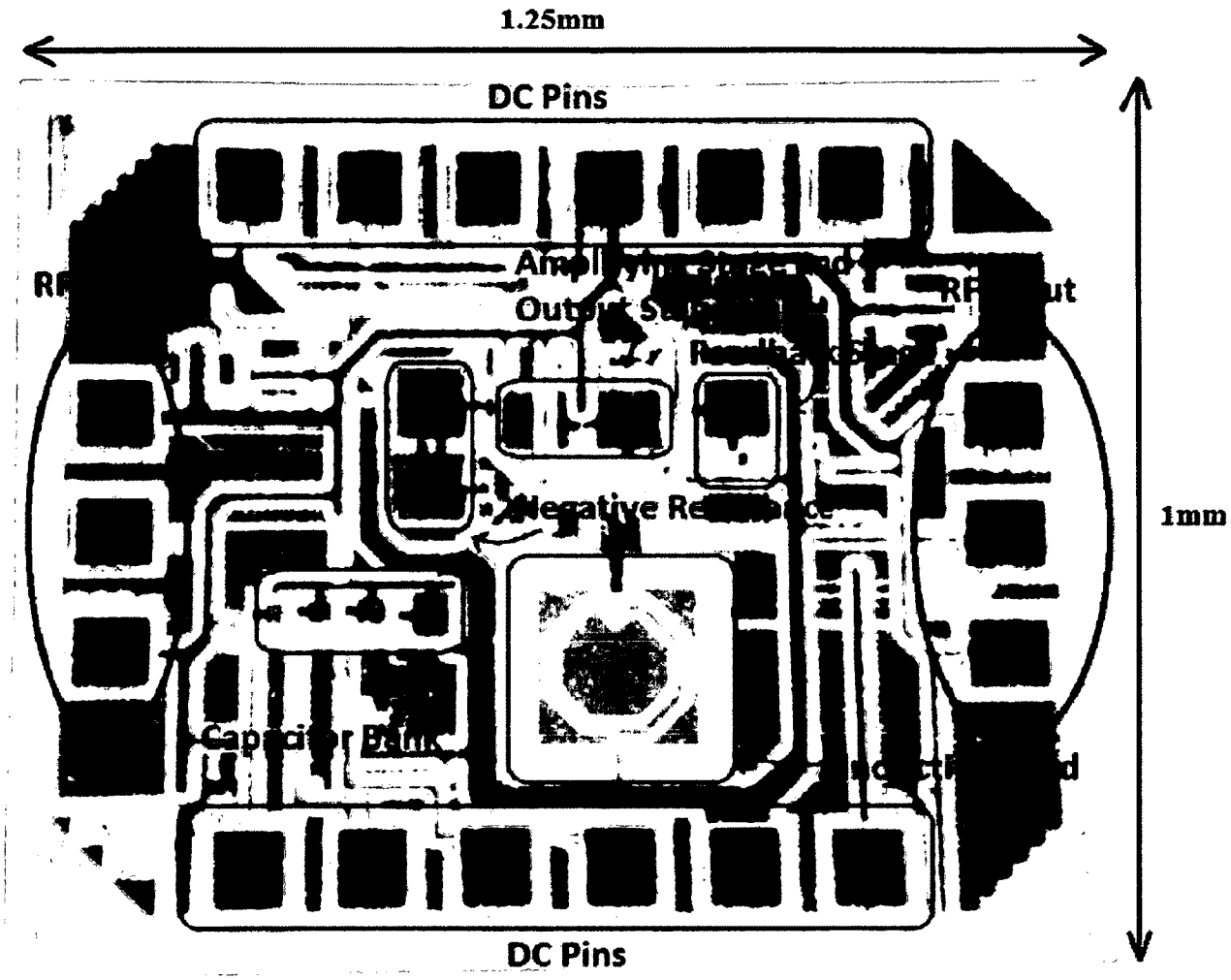

Figure 3-19. Micro-photograph of the LNA

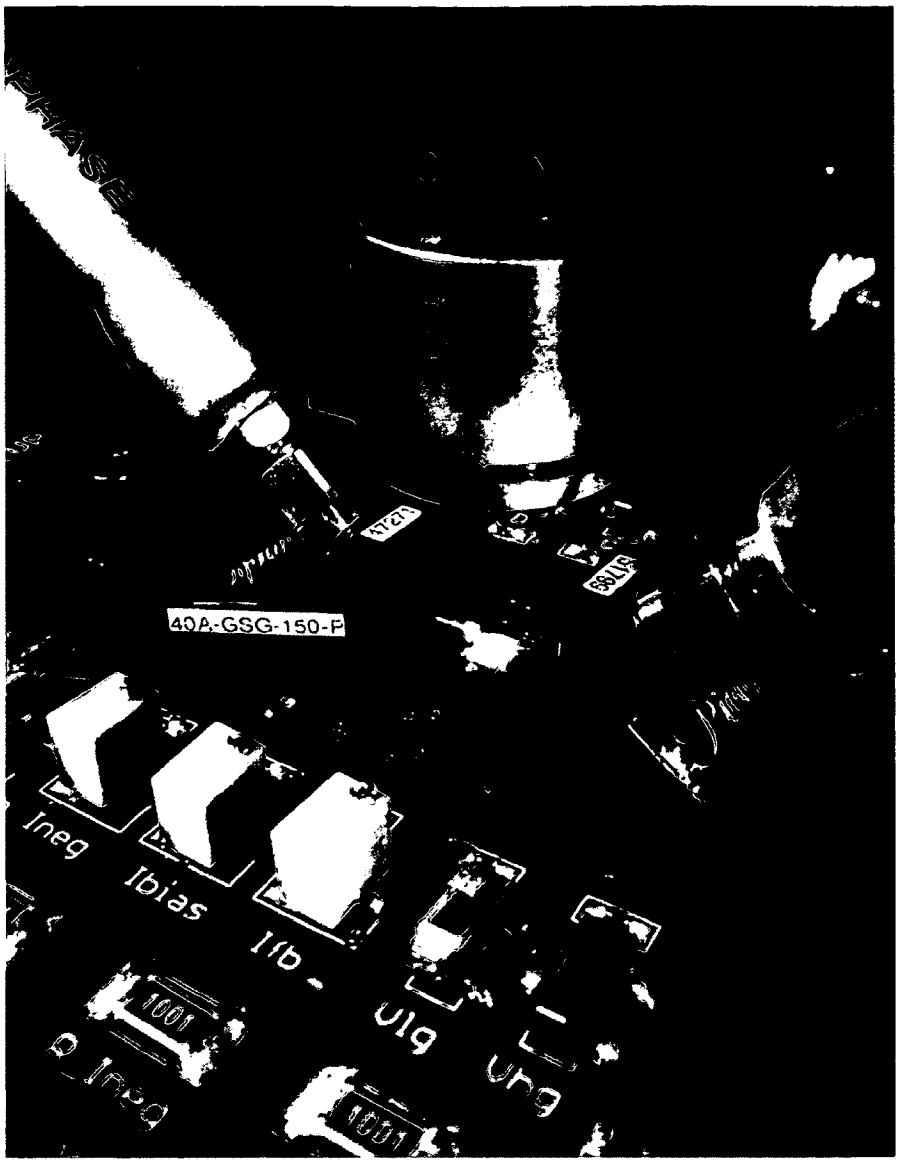

Figure 3-20. A photo of the chip on the breakout board in its test bench

Figure 3-17 shows the board that was used to provide the DC biasing and control voltages and reference currents to the chip. The control voltages were implemented with switches and potentiometers. The reference currents were set with potentiometers to use as a reference for the simple current mirrors. High-precision resistors were used in series with the potentiometers to provide reliable current readings.

Unfortunately, a few oversights were made in the design of the schematic and layout of this amplifier that had a major impact on the performance of the fabricated LNA. The

first oversight was that three substrate connections were made at the sources of three non-isolated transistors of which were at a non-zero voltage. The bulks of these transistors were tied to their sources with the aim of avoiding the bulk-effect, but this was done without much thought and the obvious issue with this was overlooked. The simple solution to this problem would be to use a triple-well FET to isolate the FETs bulk from the rest of the substrate, such that its bulk can be biased at its non-zero source voltage without negatively impacting the operating point, RF performance and quality of the grounding throughout the substrate while mitigating its own bulk-effect. The impact of this bad bulk connection on performance and operating point is not modeled by the simulator. The bulk of each FET in the simulator (whether it is a regular RF NFET or a triple well NFET) is treated as its own net, and is isolated from all other bulk connections. In schematic level simulation, the simulator has no way of modeling the substrate impedances between various contacts. Generally, such modeling would never need to occur, as the bulk is intended to be set to a common potential in virtually all cases. Layout extraction also does not take into account the implicit connection between substrate contacts, and treats each contact as existing within its own net, which matches the model in schematic level (this is necessary for LVS). Therefore, in order to model this issue, the mutual coupling between these bad substrate contacts must be modeled manually. A basic schematic level model of these substrate impedances between these contacts was created, and is shown in Figure 3-21 below:

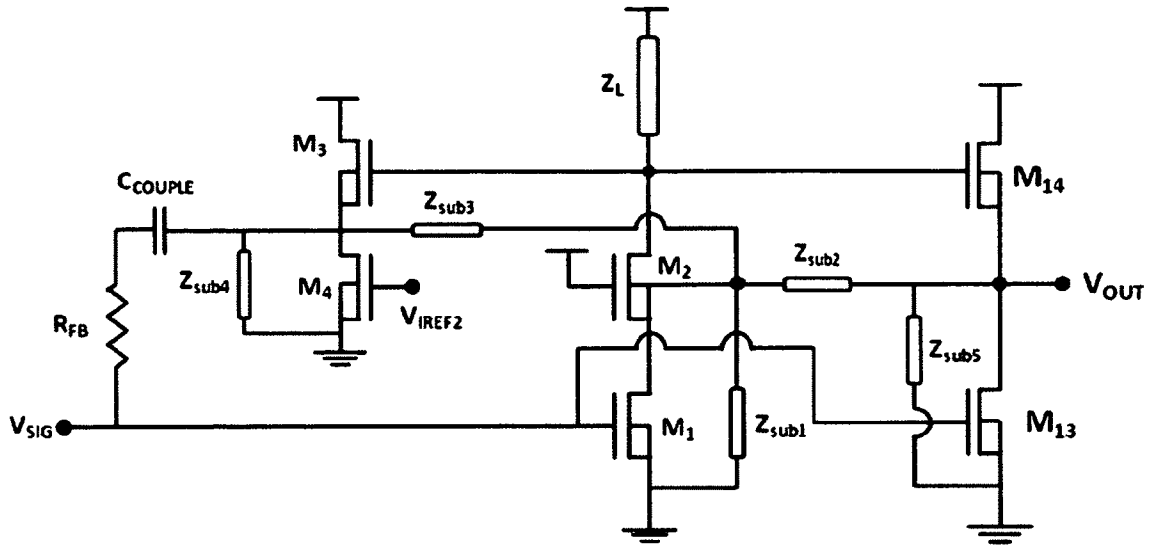

Figure 3-21. Simplified schematic of the LNA including the coupling of the bad substrate contacts to ground and one another

These three bad contacts couple to one another through Z_{sub2} and Z_{sub3} and (more importantly) couple more strongly to more nearby, more numerous and larger ground contacts as modeled by Z_{sub1}, Z_{sub4} and Z_{sub5}. The resistances between contacts can be roughly modeled with the knowledge of the substrate resistivity (available in the IBM documentation) and an approximation of the effective depth. The effective depth describes the effective depth that current traverses between one substrate contact to the next but this can be only very roughly estimated without the assistance of an 3-D finite element solver. With these two parameters the effective sheet resistance can be computed and then the path resistance between substrate contacts can be roughly computed. Through DC measurement, the DC currents through a number of different paths in the circuit were measured and compared with simulation. By doing this, the DC path resistances to ground for these bad substrate contacts could be tuned to match the DC measurements. In order to more accurately model the DC resistivity of the substrate contacts, a number of DC measurements were taken to record the supply current draw for various conditions. Loose die were probed with DC probes.

(1) Current was measured when VDD and VSS pins were connected at 1.2V and ground with all other pins grounded. This test enables current flow through feedback FET M_3 and source follower M_{14}.

(2) The cascode FET M_2 was biased at VDD and current was measured again. By doing this, the sum of the current through M_3, M_{14} and M_2 could be known.

With these two measurements, an approximation of the DC substrate resistivity could be approximated. The resistivity of output buffer M_{14}s substrate path to ground (Z_{sub5}) could be approximated by comparing to the measured S22. Introducing resistance Z_{sub5} increases the current flow through M_{14}, thereby decreasing its output impedance. It also reduces the LNAs output impedance by existing in parallel with the output of M_{14}. By sweeping Z_{sub5}, it was found that 500Ω provided a suitably accurate match between the simulated and measured S22. With the knowledge of the substrate current draw through M_{14}, the DC resistivity of the feedback source follower M_3 could then be easily found by setting up simulation to match case 1, then sweeping the value of M_3s substrate resistance to ground (Z_{sub4}) until the total simulated supply current draw matched the measured supply current draw from case 1. Resistance Z_{sub4} was found through this simulation to be 150Ω. With the knowledge of the Z_{sub3} and Z_{sub4}, the DC substrate resistance to ground at the source of cascode transistor M_2 (Z_{sub1}) could be found. By setting up the simulator to match case 2, this resistance was easily found by sweeping its value and choosing the value that creates a match between the simulated and the measured supply current draw from case 2. Resistance Z_{sub1} was thus found through simulation to be 170Ω.

After implementing these contact resistances, it was found that the simulated gains were still much higher than the gains measured by the VNA for the same bias conditions. As such, it was concluded that the substrate impedance at RF frequencies differs from the DC resistance significantly. Transistors M_2 and M_{14} are the two potential candidates for loss in gain, as current lost to ground through the substrate means less RF current driven through the load. RF current lost to ground through M3's substrate contact would actually result in a slight increase in gain as the feedback current (negative feedback) is reduced, but results in reduced control over the input match. It was also apparent that the cascode transistor was by far the main contributor to the reduction in gain, given its very close

proximity to grounded contacts, and the fact that current lost to ground is current that doesn't reach the load and thus results in a reduced output voltage swing. Transistor M_{14} would have less of an impact on the gain, as its substrate path resistivity is quite a bit higher than M_2s. Thus, a high-frequency substrate impedance model was implemented between the bulk connection of the cascode transistor and ground. From the measured results it was noticed that the substrate impedance increased with increasing frequency. A simple model was generated to emulate this effect, and is shown in figure 3-22.

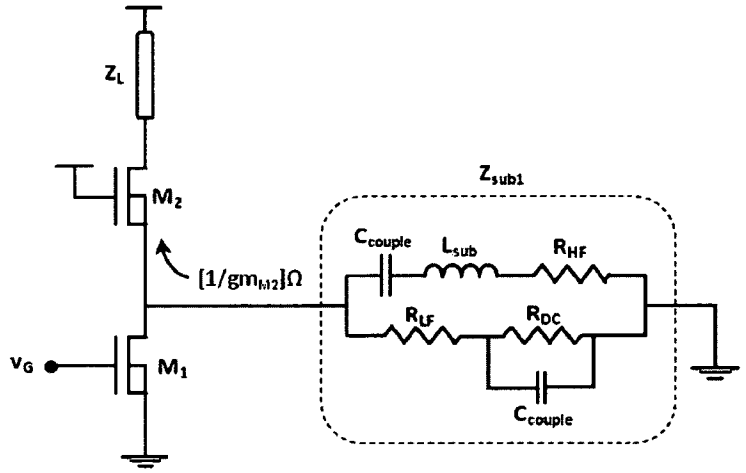

Figure 3-22. Substrate impedance model for Z_{sub1}

The physical implication of the inductance through the substrate (L_{sub}) is difficult to realize, given the distributed nature of current flow through a thick sheet, but with this inductor the impedance response was modeled fairly accurately. It was found that with R_{HF} of 0Ω, R_{LF} of 25Ω, R_{DC} of 170Ω and an L_{sub} of 350pH models both RF and DC substrate coupling quite well. The series combination of R_{LF} and R_{HF} models the DC substrate resistivity. C_{couple} is a large capacitor that simply couples RF to ground, preventing DC current flow through L_{sub}.

It should be noted that this model is likely only valid over the frequency range that it is applied to. Additionally, this model likely does not represent the physical behavior of the substrate in any way, and is only being used to model the behavior. Another approach to modeling could have been done with the use of Cadence's substrate coupling analysis tool, which would have provided a truer model. This was not used, as it was believed that

the required kit for this analysis was not available. Instead of going through the process of modeling the substrate impedance, this problem could potentially be fixed through microsurgery, but micro-cuts would have to be performed at the lowest metal layer and the cost for such a service would be far too high.

The second thing that was overlooked in the design of this amplifier was the decoupling of the gate of the cascode transistor. Given that the gate connection to the bias voltage is through a relatively long on-chip trace to the pad, through a bondwire and then through a printed circuit board trace, it is no surprise that a lack of coupling could drastically affect performance. This performance hit exists as the gate of the FET is no longer RF grounded and a complex (inductive) impedance is seen from the gate of this FET. This causes a positive feedback that can produce negative resistance looking into the source of the cascode FET M_2. Modeling of the impedance seen by the gate of M_2 was attempted, but did not result in matching with measurements.

3.3 LNA POST-EXTRACT SIMULATION

In this section, the simulation results of the LNA will be presented and discussed.

The following results reflect the final extracted schematic-level design. First, we can observe the S-parameter and noise figure results over all bands in low and high gain modes, in order to show the two performance extremes. In both low and high gain cases, S22<10dB and S12<20dB, and are not plotted. Note that unconditional stability was confirmed over all operating conditions.

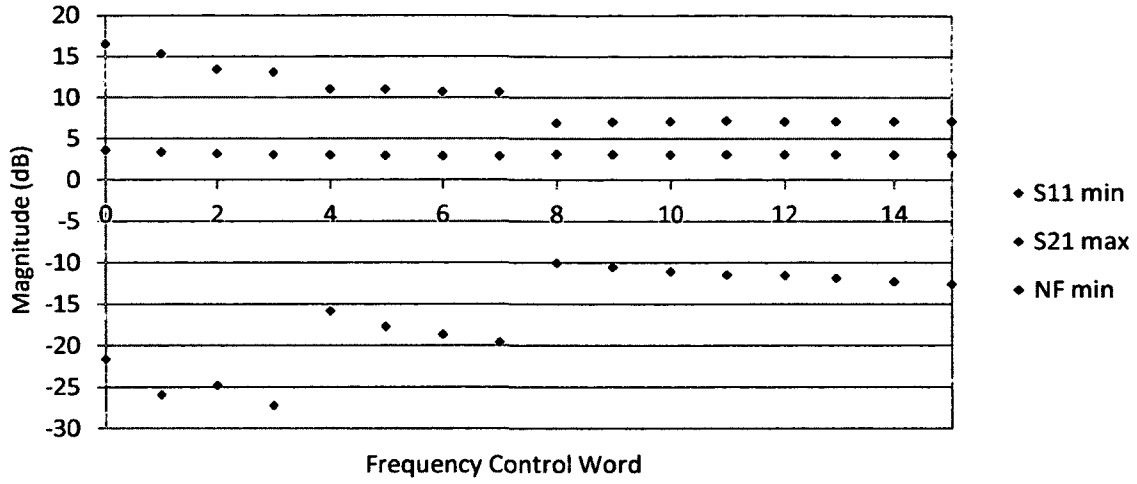

Figure 3-23. S21, S11 and NF results for highest gain setting, 150μA feedback reference current and no negative resistance. Note that frequency reduces with increasing frequency control word.

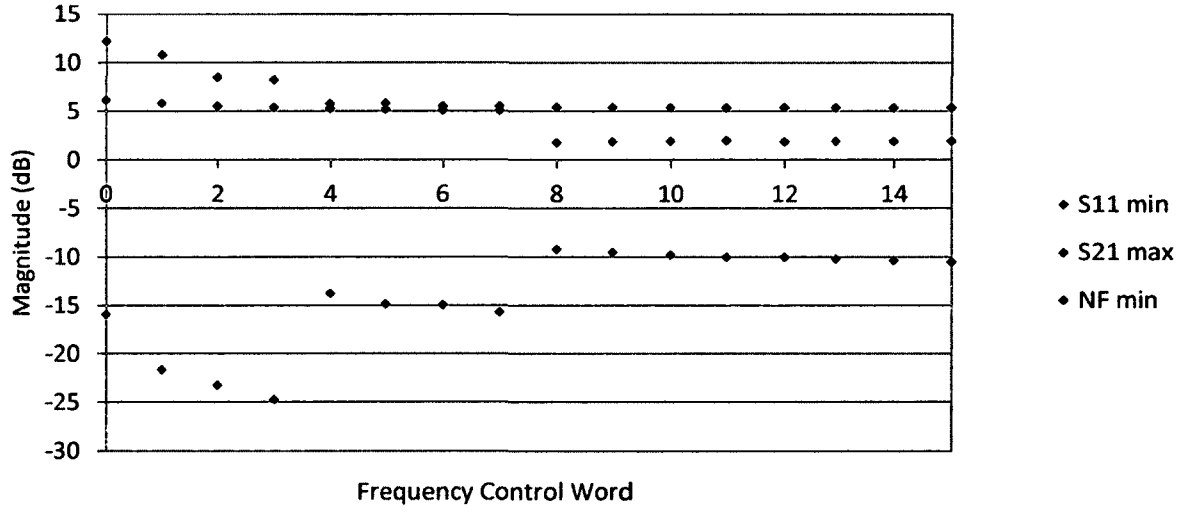

Figure 3-24. S21, S11 and NF results for lowest gain setting, 500μA feedback reference current and no negative resistance. Note that frequency reduces with increasing frequency control word.

It is apparent in figures 3-23 and 3-24 that the gain reduces with decreasing frequency (increasing frequency control word), and is caused by decrease in the effective parallel resistance of the inductive load and capacitor bank with decreasing frequency. Also,

there are two significant jumps in S11, when the frequency control word transitions from 3 to 4 and 7 to 8. The jump in S11 from a frequency control word of 3 to 4 occurs as the quality factor of the load and hence the load's effective parallel resistance changes fairly drastically in this transition. The jump in S11 from frequency control word of 7 to 8 occurs for the same reason, coupled with a more significant jump in frequency which affects the complex component of the input impedance. This more significant jump in frequency was caused by a slight deviation from the desired binary-weighted frequency transition of the resonant load in this particular frequency step, and can be observed in Figure 3-13.

Figure 3-25 below shows the bandwidth variance of the amplifier over frequency (as frequency control word is swept) for both high and low gain cases. These bandwidth results were acquired with the negative resistance disabled.

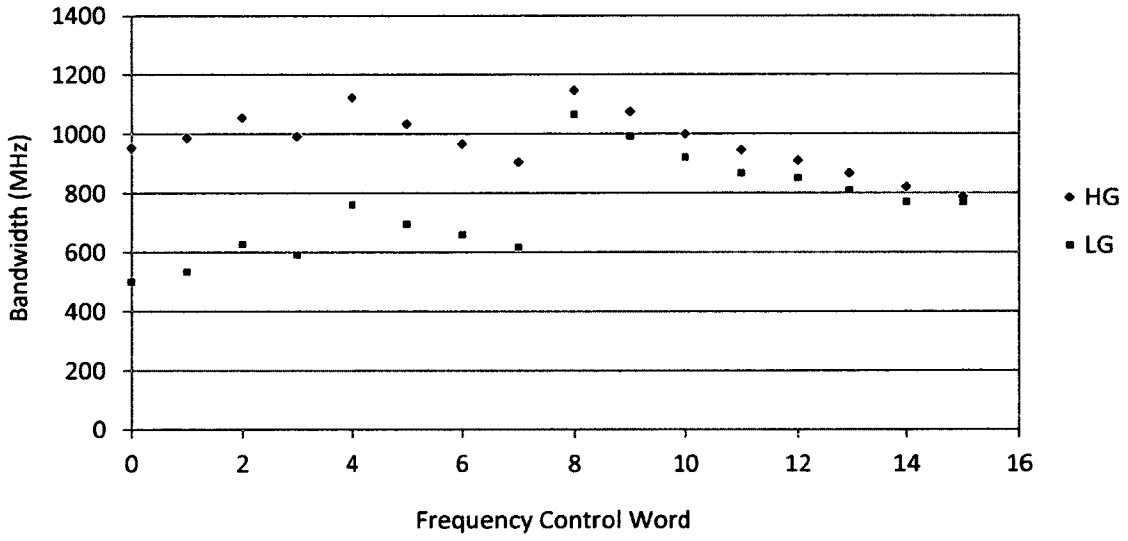

Figure 3-25. Bandwidth results for highest and lowest gain setting, 150μA feedback reference current for high gain, 500uA feedback reference current for low gain, and no negative resistance. Note that frequency reduces with increasing frequency control word.

In the high gain case, the bandwidth remains reasonably flat over frequency, given that bandwidth is determined by f_c/Q, and the Q drops with frequency. In the low gain case, the bandwidth drops by a significant amount from the 8^{th} frequency control word to the

7^{th}. This is caused by a significant increase in the quality factor of the resonant load when the 3^{rd} capacitor is switched off when transitioning from the 8^{th} to the 7^{th} frequency control word.

The variable bandwidth function can be simulated. The variable-bandwidth performance will be shown for two frequency control words for conciseness. The following three figures present the variable-bandwidth performance at a frequency control word of 7.

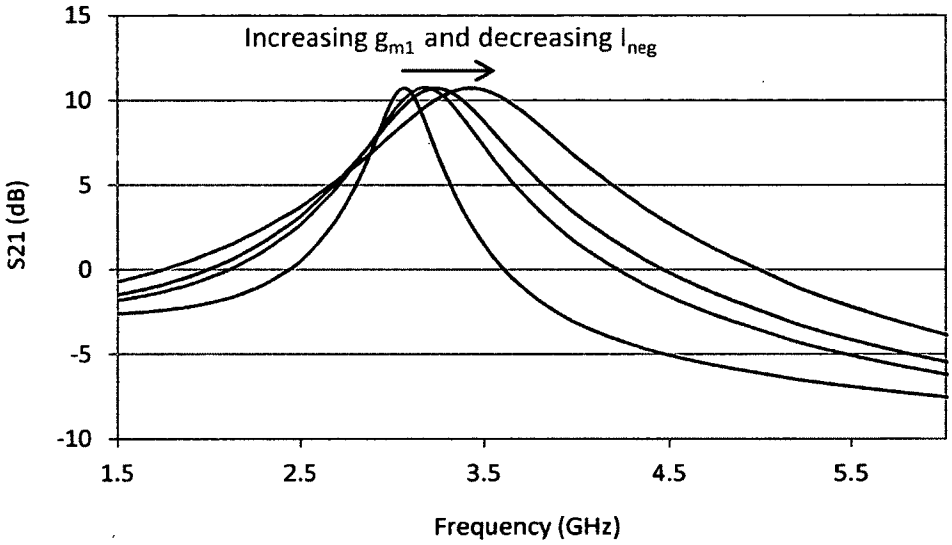

Figure 3-26. Demonstrating variable bandwidth with frequency control word 7 and a feedback reference current of 150μA.

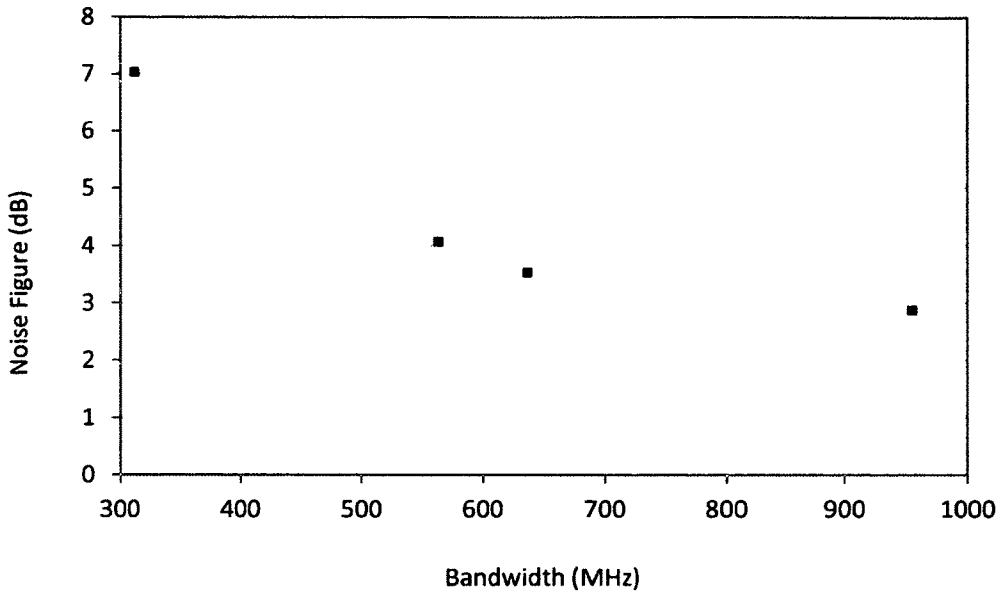

Figure3-27. Bandwidth and in-band noise figure vs. gain level for a frequency control word of 7 and a feedback reference current of 150μA.

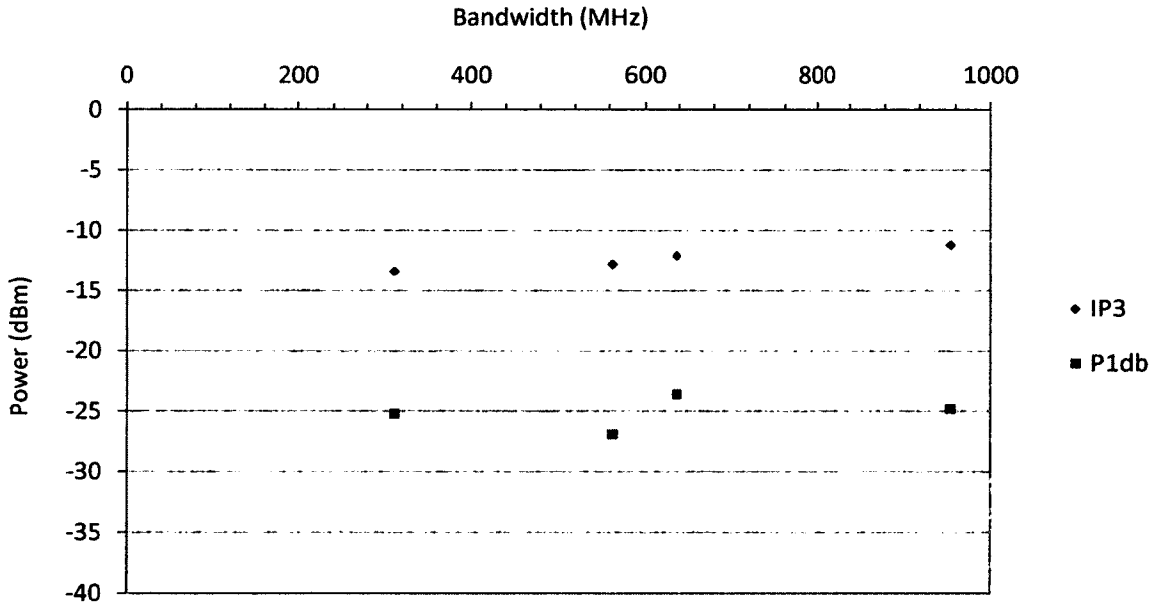

Figure 3-28. P1dB and IIP3 vs. bandwidth for a frequency control word of 7 and a feedback reference current of 150μA.

It can be seen in Figure 3-26 that there is an undesired frequency shift that accompanies the change in negative resistance. This occurs, as the parasitic capacitance of the transistors in the negative resistance circuit become more capacitive with increasing bias current. This behavior could be corrected with a varactor connected in parallel with the load. The achievable quality factors over the entire tuning range of a varactor in the IBM 0.13μm process are sufficiently high such that they would not bring down the effective load resistance at resonance. This was not included in the design, due to a limitation on the number of available control pins that could be fit on chip.

Figure 3-27 shows the exact bandwidths achievable for a 10.2dB S21 at a FCW of 7. This plot shows the in-band noise figure increasing with decreasing bandwidth. This occurs, as the S21 remains fixed, while the noise contribution of the negative-resistance cell increases. This increase can be attributed to the increase in drain-source channel noise with increasing bias current, while the peak gain is not increasing. Fortunately, the total in-band noise power reduces with decreasing bandwidth, and in this design, the overall noise power does not increase with decreasing bandwidth. Total noise power at the output can be found by multiplying the resulting output noise by the bandwidth; therefore, the noise power in dBm is proportional to $10\log_{10}(BW)$. Given that we have a minimum-to-maximum bandwidth ratio of $10\log_{10}(335MHz/935MHz)$ = -4.3dB, and a 3.5dB increase in noise figure, the net change in noise power would be -0.8dB when adjusting the bandwidth from the maximum to the minimum with a FCW of 0. For most cases, the net change in noise power is negative when moving from a higher bandwidth to a lower bandwidth.

Figure 3-28 illustrates the linearity of the device at a FCW of 7 over all four fixed-gain bandwidths. The linearity improves only slightly with increasing with increasing bandwidth; this slight improvement in linearity can be attributed to a reducing negative resistance with increasing bandwidth. . The IIP3 and P1dB points for each bandwidth setting differ from 11.5dB to 14.1db, fairly close to the theoretical 14dB IIP3-P1dB difference.

The following three figures present the simulated variable bandwidth performance for a frequency control word of 0.

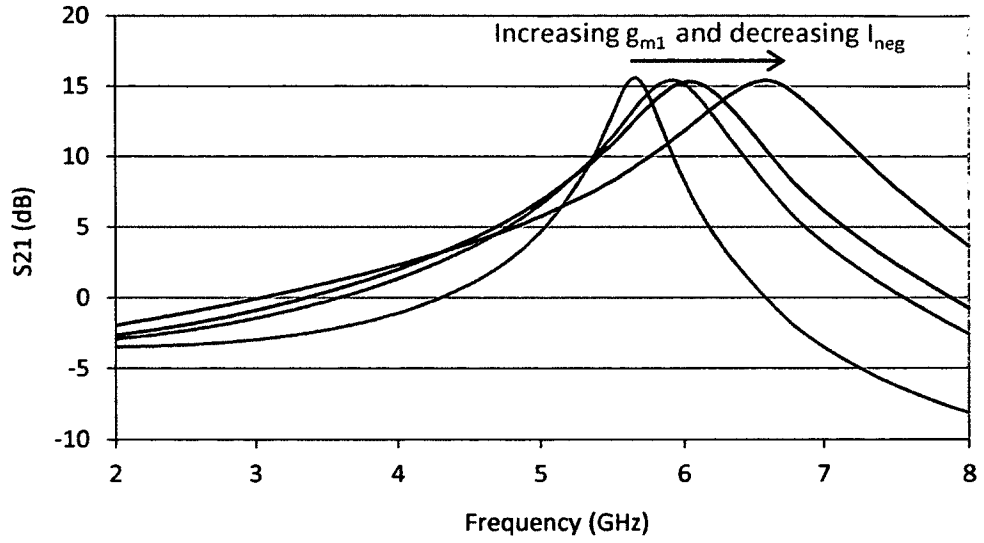

Figure 3-29. Demonstrating variable bandwidth with frequency control word 0 and a feedback reference current of 500μA.

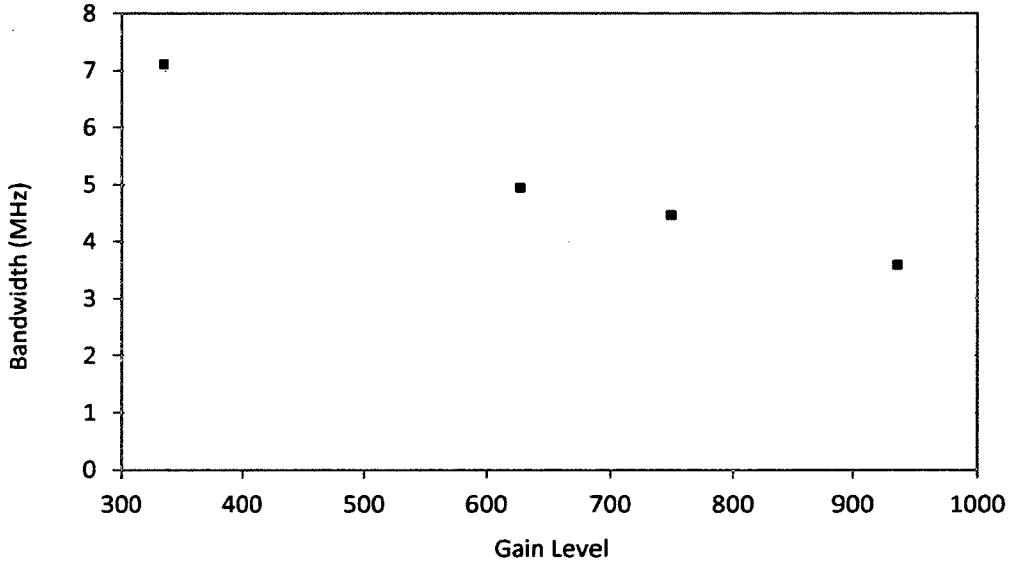

Figure 3-30. Bandwidth and in-band noise figure vs. bandwidth select for a frequency control word of 0 and a feedback reference current of 500μA.

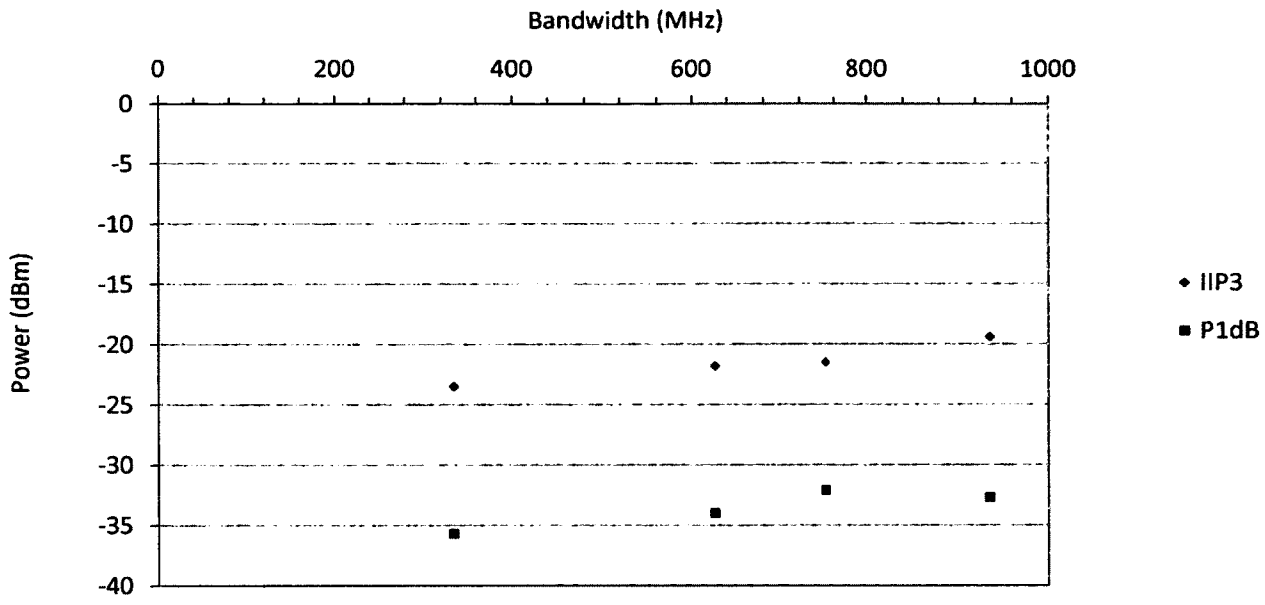

Figure 3-31. P1dB and IIP3 vs. bandwidth for a frequency control word of 0 and a feedback reference current of 500μA.

Observing Figure 3-29, it can be seen that the frequency shift with bandwidth is more pronounced than the frequency control word of 7 case, as the sensitivity of frequency to change in load capacitance is higher.

The noise figure vs. bandwidth trend shown in Figure 3-30 shows that there is a slight increase in the total in-band noise power from minimum to maximum bandwidth of $(NF_{minBW} - NF_{maxBW}) - (10\log_{10}(BW_{max}) - 10\log_{10}(BW_{min})) = (7.4dB - 2.6dB) - (10\log_{10}(890) - 10\log_{10}(450)) = 1.84dB$.This is an unfortunate result, as it is desired to have decreasing in-band noise power with decreasing bandwidth. Future work could be done to find a solution to this issue.

The linearity versus bandwidth trend shown in Figure 3-31 shows minor improvements in linearity with increasing bandwidth, as peak gain remains constant and the negative resistance cell contributes less with increasing bandwidth. The IIP3 and P1dB points for each bandwidth setting differ from 12.2dB to 13.3db, fairly close to the theoretical 14dB IIP3-P1dB difference.

The functionality of this design also includes basic variable gain control, as seen in Figure 3-32 below.

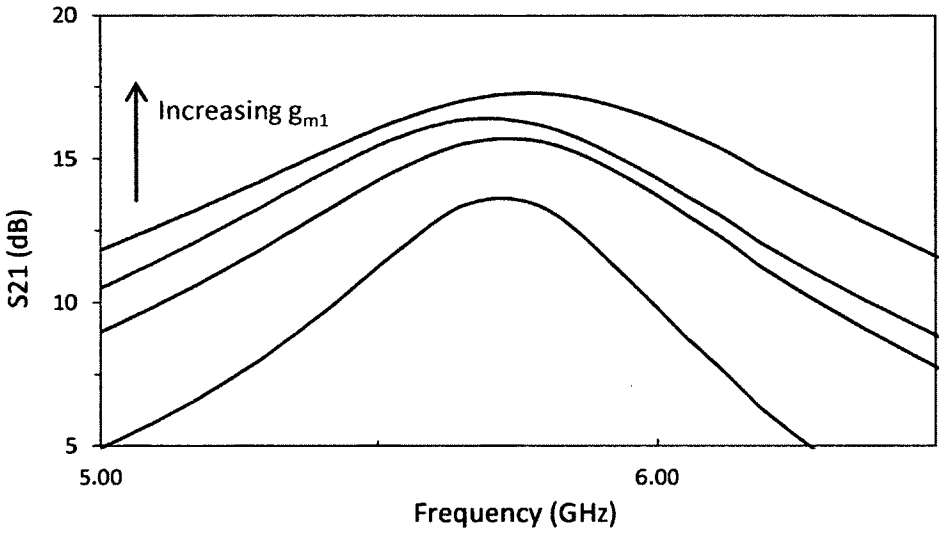

Figure 3-32. Variable gain functionality for frequency control word of 0. This is performed by switching on and off M_{1A} and M_{1B}.

This variable gain was achieved by switching the variable gain FETs on and off. Further control of the gain can be achieved by enabling the negative-resistance cell, but with the drawback of decreased linearity and peak in-band noise figure, though at reduced bandwidths.

3.4 LNA MEASUREMENTS

In this section, measurements of the fabricated LNA will be presented and discussed. The simulation results that are used for comparison to the measured results are derived from simulation that includes the modeling of the bad bulk-source substrate contacts. This is a schematic-level simulation, not post-extract. This is so because it would not be practical to perform such modeling in post-extract simulation, due to the need for a perfectly matched layout and schematic. Therefore, the parasitic capacitance that caused a reduction in center frequency had to be modeled with a simple capacitor to ground at the

drain of cascode transistor M_2. The other parasitics were not modeled. The RF pad-to-gate input on-chip line inductance and the M_{14}s output-to-pad on-chip line inductance could have easily been modeled, but this was overlooked. These inductances were on the order of 300pH, and fortunately had very minor effect on the performance; virtually only affecting the S11 and S22 by a maximum of 1dB. Hence, the results are still considered quite valid.

3.4.1 SCATTERING PARAMETER AND NOISE FIGURE RESULTS

An HP 8720ES vector network analyzer was used to take S-parameter measurements. The input and output ports were connected to a 50Ω standard cable with 150μm pitch Picoprobe ground-signal-ground probes for connecting to the input and output of the LNA. The VNA, cable and probes were calibrated out prior to each measurement in order to ensure that the VNA reported only the performance of the LNA alone. TRL calibration was performed on a Picoprobe CS-5 calibration substrate across the frequencies of interest and at a source power well below the lowest 1dB compression point of the amplifier. Calibration structures were not included on-chip, so the effects of the pads could not be calibrated out, though the post-extract simulation did take into account the modeled pad parasitics.

Noise figure was measured with the HP8975A noise figure analyzer. This device was calibrated with a 50Ω noise source, whose noise profile is characterized in a table loaded on the NF analyzer. For calibration, the noise source is connected from the output of the NF analyzer, then to an RF probe landed on a through on a calibration substrate, then through a second RF probe to the input of the NF analyzer. The through on the calibration substrate provides a short from one probe tip to the other, so that the cables, connectors, and probes can be calibrated out of the noise measurements, ideally making the LNA the only additional noise contributor in the calibrated measurement. The NFA's measurement bandwidth was set to 4MHz and the ambient temperature setting was set to automatic so that the NFA detects the ambient temperature with its built-in temperature sensor. Measurements were taken over three bands at high and low gain settings. Over

100 points were taken over each of these bands and each point was averaged 10 times for accuracy. The expected noise performance on other bands can be interpolated from these results.

The VNA and NFA setups were as follows:

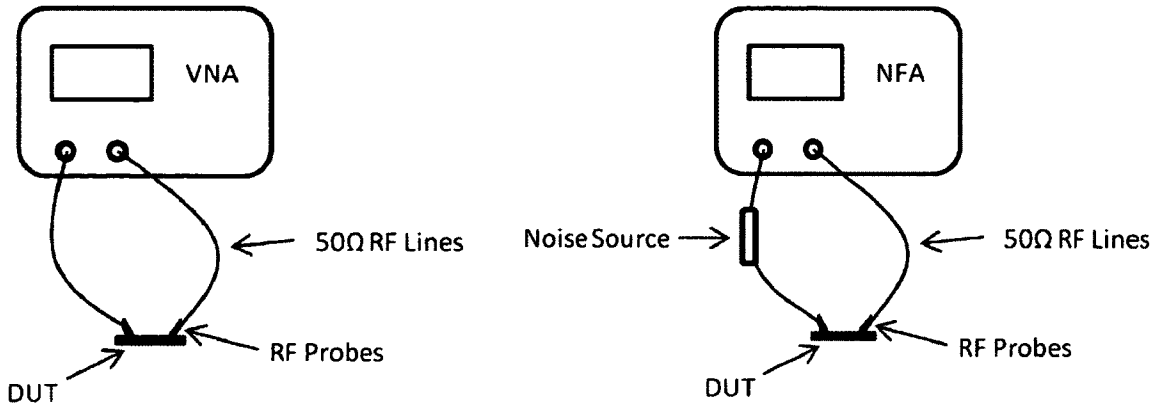

Figure 3-33. Vector network analyzer and noise figure analyzer test bench setups for S-parameter measurement

The S parameter and noise figure measured and simulated results are shown in figures 3-34 through 3-36.

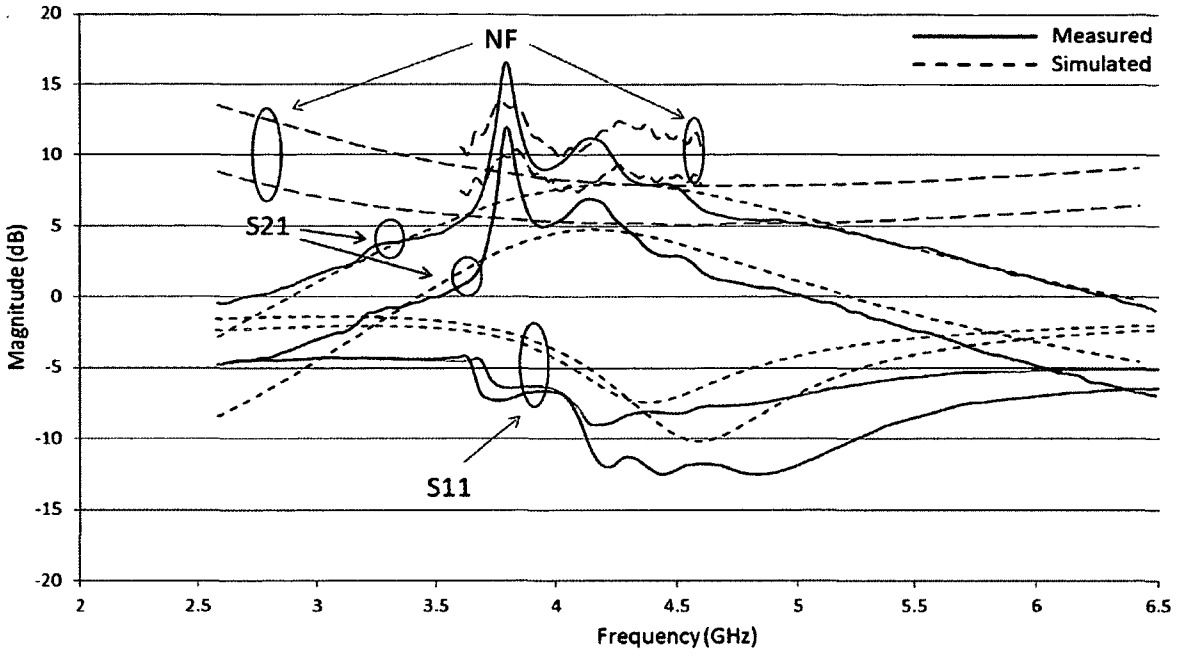

Figure 3-34. Measured and simulated S21 and S11 for high and low gain settings at the highest frequency band. Simulated results include the model of substrate conductivity.

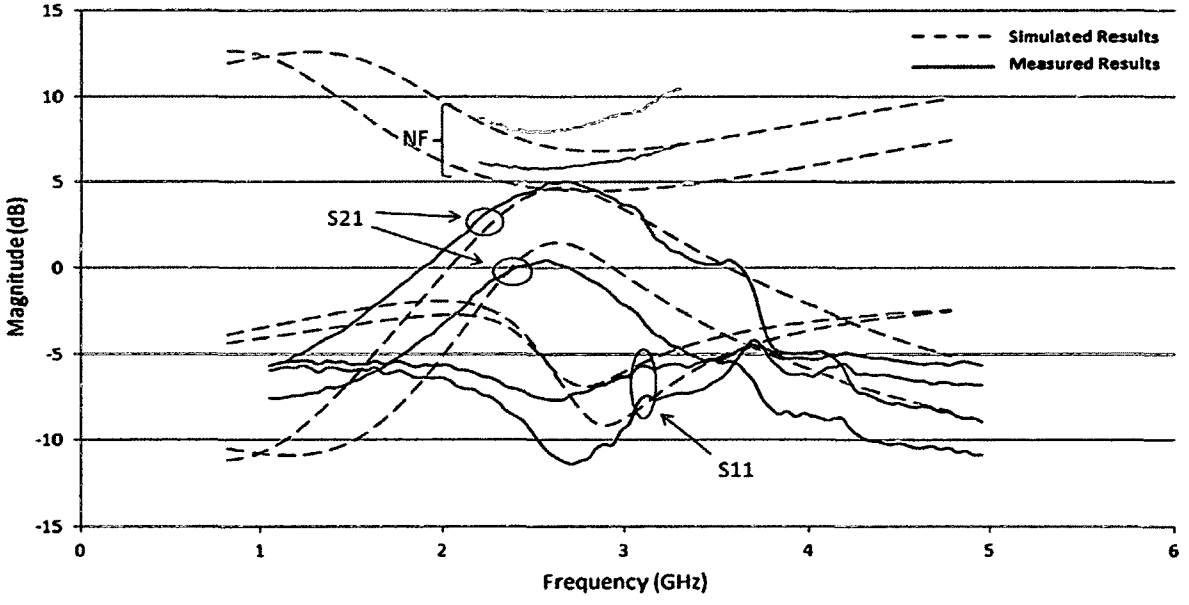

Figure 3-35. Measured and simulated S21 and S11 for high and low gain settings at the middle frequency band. Simulated results include the model of substrate conductivity.

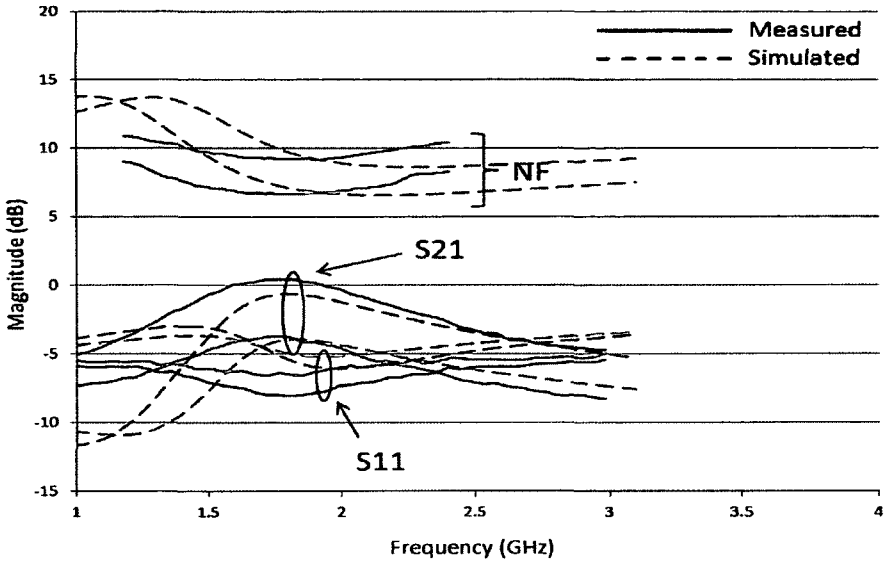

Figure 3-36. Measured and simulated S21 and S11 results for high and low gain settings at the lowest frequency band. Simulated results include the model of substrate conductivity.

Note that S22 was not shown in the above plots, but is approximately -8dB to -9dB in both simulation and measurements at all frequency bands and at all gains. The S22 is quite flat across the band with only about 8% deviation due to the isolation of the output stage from the resonant load. The lack of achieving less than 10dB output match can be attributed to the bad source-to-bulk contact made on the output FET M_{14}. The impedance seen is the source-drain resistance of M_{14} ($1/g_{m14}$) in parallel with the substrate resistance to ground, which, based on some simple analysis of the proximity of the contact to surrounding ground contacts along with comparisons with measurements, was approximated to be 500Ω as discussed in section 3.2.8. This 500Ω reduces the output impedance of the LNA by causing M_{14} to draw more current and bringing the$1/ g_m$ below the desired 50Ω.

Figures 3-34 through 3-36 compare the measured S-parameter and NF results to the coinciding simulation results which include the modeling of the bad substrate contacts. It is apparent with these results that the bad substrate contacts have drastically reduced the gain performance that was expected from the simulated results. In Figure 3-34 the effect

of the two series bondwire inductances that exist between the cascode gate and the VDD pad of the chip is quite apparent. It can be seen that the simulated and measured gain trend in Figure 3-34 is quite similar and only deviates in-band, where resonance occurs with the two bondwires and the parasitic capacitances seen by these inductors. These differences are quite obviously caused by the effect of the bondwire inductances, which could not be accurately modeled. It could be approximated that the in-band gain response of the amplifier would accurately match the simulated results if the cascode gate was adequately decoupled. The gain control here shows results close to the expected 4dB range from high to low gain. The S11 results are quite similar in their magnitudes and trend. The undesired but expected frequency offset is apparent in both measured and simulated cases. Therefore it can be said that the effect of the cascode bondwire inductances have minimal effect on the feedback matching performance, as would be expected due to the typically high gate-drain isolation of the cascode FET M_3 and common source amplifying FET M_1. Noise figure results show two peaks; the dip between these two humps shows an NF that drops down to about 10dB at low gain, and about 8dB at high gain. This is somewhat comparable to the simulated NF of about 8dB and 5.25dB at the center of the high frequency band for low and high gain modes respectively. The poor noise performance here can be attributed to RF signal loss to the substrate due to the bad substrate contacts.

The results in Figure 3-35 show a closely matched gain response. It is apparent here that the bondwire inductances are not affecting the performance here, as they are resonating beyond the cutoff. The measured and simulated S11s do differ, as the simulated one is offset in frequency. This is likely due to issues in the modeling of the bad bulk-source substrate contact of M_3 in the feedback network combined with a lack of modeling of the layout-parasitics. The simulated and measured noise performance are reasonably comparable, though the minimum simulated noise figures are offset in frequency due to the simulated S11 frequency offset.

In Figure 3-36, the peak gains and peak gain frequencies are nearly identical, though S11 is slightly off center and slightly higher in magnitude than what was measured. It is apparent here that the bondwire inductances do not influence the results at the lowest

frequency band, as the response is relatively smooth and comparable to the simulated results. The simulated and measured peak S21 frequencies match up quite closely, and peak gains are within about 1dB of each other. The simulated and measured minimum S11 points do differ by about 160MHz and magnitudes differ from 2-3dB in the low and high gain cases respectively. This difference is likely caused by a combination of measurement inaccuracy and inaccuracy in the substrate modeling. The noise figure results are fairly similar in magnitude, but minimum NF frequencies are somewhat offset.

Note that variable-bandwidth results are not shown, as it was found that the negative resistance had a nearly immeasurable effect on the RF performance. This can likely be attributed to high frequency effects, as discussed in section 3.2.3.

3.4.2 LINEARITY RESULTS

Linearity was measured with the use of two signal generators, a power combiner, high quality RF coaxial lines and a spectrum analyzer (SA). Before taking measurements, a manual calibration of the test bench was performed. The path loss from the output of each signal generator to the input of the device under test (DUT) and the path loss from the output of the DUT to the input of the SA were measured. The two input path losses were measured by supplying RF power from each signal generator separately and measuring the power at the end of the input path with the SA. When measuring the input path loss from one of the signal generators, the unused input of the power combiner was terminated at 50Ω to prevent unwanted reflections back from the unused terminal of the combiner thus ensuring an accurate measurement. Following these two measurements, the path loss from the output of the DUT to the SA was measured. With the knowledge of all of these path losses, the RF power incident at the input pads of the LNA as well as the RF power at the output pads of the LNA can be known. Also, with knowledge of the difference between the two input path losses, an offset in the input power can be made on one of the signal generators in order to match the powers of the two tones incident on the DUT, thus ensuring proper IIP3 measurements. In addition to measuring the path losses,

the signal generator output vs. input power response was measured. It was found that this response was linear for all of the input powers that were to be tested.

The measurement setup is shown in Figure 3-37 below.

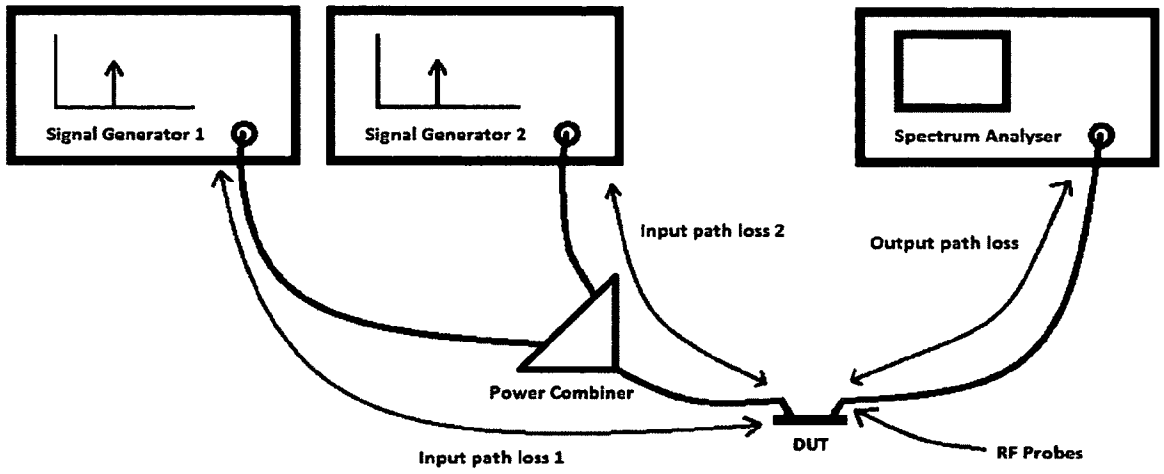

Figure 3-37. Linearity measurement setup

Given the virtually limitless reconfigurations available for this LNA, it was decided that the linearity would be measured for only a handful of cases. The best and worst case linearity exists at high gain at the highest frequency band, and the best case linearity exists at low gain at the lowest frequency band, as these operating points have the two gain extremes. For completeness, linearity was measured at low and high gain for both the highest and lowest frequency bands. The results of this test are tabulated in table 4 below. The two spikes seen in Figure 3-33 were avoided in measurement by ensuring that the two input tones and IM3 products landed well in-between these two humps.

TABLE 4. LINEARITY RESULTS

Test	FCW	Gain Setting	Gain(dB)	I_{FB}(uA)	P1dB(dBm)	IIP3(dBm)	$P1dB_{sim}$(dBm)	$IIP3_{sim}$(dBm)
1	0	Highest	7.5	150	-15.5	-2	-15.6	0.1
2	0	Lowest	4.8	150	-7	8	-8.7	7.7
3	15	Highest	0.9	150	-2.5	11.5	-3.5	9.6
4	15	Lowest	-3.1	150	0	13.5	0.3	12.9

These results show quite a good match between simulated and measured P1dB and IIP3 for all cases. This further supports that the bad bulk-source-substrate path impedances are adequately modeled. The high-frequency band (FCW = 0) results matching simulation suggests that these two spikes are anomalies (resulting from the effects of the bondwire) and do not affect the operation elsewhere. This further validates the conclusion that the effect of the bondwires can be neglected, except of course at these two peaks. The well-known relationship between gain and linearity is apparent in these results, as the linearity improves with decreasing gain.

Note that the curves are plotted in the appendix for all four cases listed in table 4. Observing these curves, it is apparent that there is more than one major contributor to the third order intermodulation products. This can be seen, as the IM3 curve is not consistently 3dB/dB below the 1dB compression point. This is apparent in Figure A-4, where the IM3 curve obviously deviates from its 3dB/dB past an input power of around -15dBm. This nonlinear behavior can likely be attributed to the nonlinear contributions of the feedback source follower. The 3dB/dB curve prior to this deviation is the sum of the IM3 contribution of the cascode gain stage/output stage and the contribution of the feedback source follower. This non 3dB/dB IM3 output trend discussed above makes the standard figure for third-order intercept point less representative of the actual behavior of the device. Regardless, it was decided that the IP3 point would be reported by extrapolating from the 3dB/dB region closest to compression (in some of these plots there exist more than one 3dB/dB region). Therefore, when analyzing the reported number, it should be understood that the actual performance may not be quite representative of the expected performance for certain input powers.

CHAPTER 4

CONCLUSION

In this chapter, conclusions about the presented design will be made and future work will be discussed.

5.1 CONCLUSION

For this thesis, a highly-reconfigurable radio-frequency low noise amplifier with variable gain, bandwidth and center frequency was developed in 0.13μm CMOS. As technology improves, such designs could provide applications like software-defined radio with the ability to operate over a wide frequency range in a diverse RF environment without the need for complex, dedicated and expensive circuitry. The subject LNA presents a potential design that could be improved to provide such a low-power and low cost solution.

This design was successful in producing variable-gain with 4dB of range, 16 independent frequency bands from 1.8GHz to 4.1GHz, and variable bandwidth with up to 68% bandwidth tuning range in simulation. Unfortunately due to a few oversights, the chips performance was much degraded from the simulated performance. The absolute maximum and minimum measured gains ranged from 7.5dB at the highest frequency band, down to -3.5dB at the lowest frequency. In post-extract simulation, the gain ranged

from an absolute minimum of 2dB to a maximum of 16.5dB. Some analysis was done post-design submission that helped to mitigate the vast range in gain from the highest to lowest frequency bands, and this is discussed in section 3.2.5. The measured IIP3 ranged from 0.1dBm to 12.9dBm. The resulting measured noise figure ranged from an absolute minimum of 7.5dB to a maximum of 9dB. The quality of the input match was measured to be quite poor due to a mistake made which resulted in current being shunted to ground through the substrate in the feedback-matching circuit. The variable bandwidth functionality was not realized in measurements due to high frequency effects deteriorating the performance of the negative resistance circuit.

5.2 FUTURE WORK

Some potential future work has been noted for this design. The design of this LNA was not performed with any particular specifications in mind. Such a design could be improved to better suit the needs of software defined radio by working towards a given list of specifications. It should be made known that power consumption of the LNA could easily be neglected in the design process as the power consumption of the LNA is insignificant when compared to that of the ADC and DSP combined, though this was not recognized during the design process discussed in this thesis. With power as a non-issue, the noise performance and gain could be improved by increasing the bias current through M1 to decrease noise figure and increase gain, at the expense of linearity. Alternatively, the M1 bias current could be increased, and equivalent load resistance at resonance decreased to maintain the same gain for a decrease in noise figure and an increase in linearity. Current could also be increased in the output stage with a reduced buffer width (to maintain 50Ω match for measurement) for enhanced noise cancellation and gain.

One of the main issues in the presented design that requires improvement is the performance of the negative resistance cell. This particular circuit seemed to have difficulties operating effectively at high frequencies due to parasitics. Also, this design did suffer from relatively poor linearity. A more expansive study could be done on other

more viable candidates for a tunable negative resistance circuit. This could include capacitive source-degenerated FET, common gate with inductor tied to the gate, or a cross coupled pair [23]. The feedback stage also posed some linearity limitations to the LNA, and further optimization of this circuit could be made to improve and appropriately trade-off linearity, power consumption and noise. Some more analysis into the influence of this feedback stage on the noise figure should be carried out. Another area for future work would include improving the resonant load design in order to provide a more even gain distribution across all bands. Optimization of the tunable capacitor bank was discussed in section 3.2.5, and could be implemented in future designs. Linearity could be enhanced in the future by adjusting the gate bias of the cascode transistor. This functionality was intended, but was not explored. In order to reduce the noise, proper noise matching should be carried out in the future (as discussed in section 3.2.1), and the output noise cancelling stage could be tweaked. It was found through this design process that by using negative resistance in the drain of the amplifying stage in combination with transconductance control of the amplifying FETs to adjust bandwidth resulted in high noise figures at low bandwidths. It is desired that in-band noise power should decrease by $10\log_{10}(BW)$, so other solutions to providing bandwidth control without increasing in noise figure with decreasing bandwidth could be researched. Following improvements on the things discussed in the previous paragraph, this LNA could be integrated into a software-defined radio receiver system.

APPENDIX

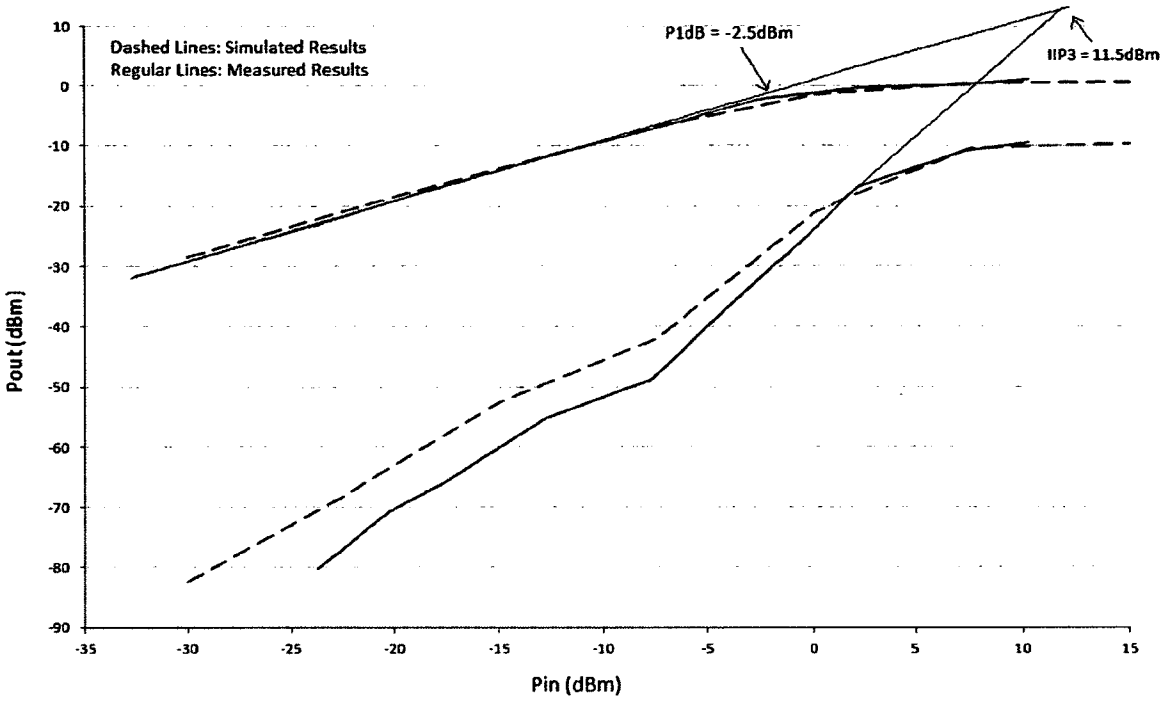

Figure A-1. Simulated and measured linearity results for highest gain at lowest frequency band

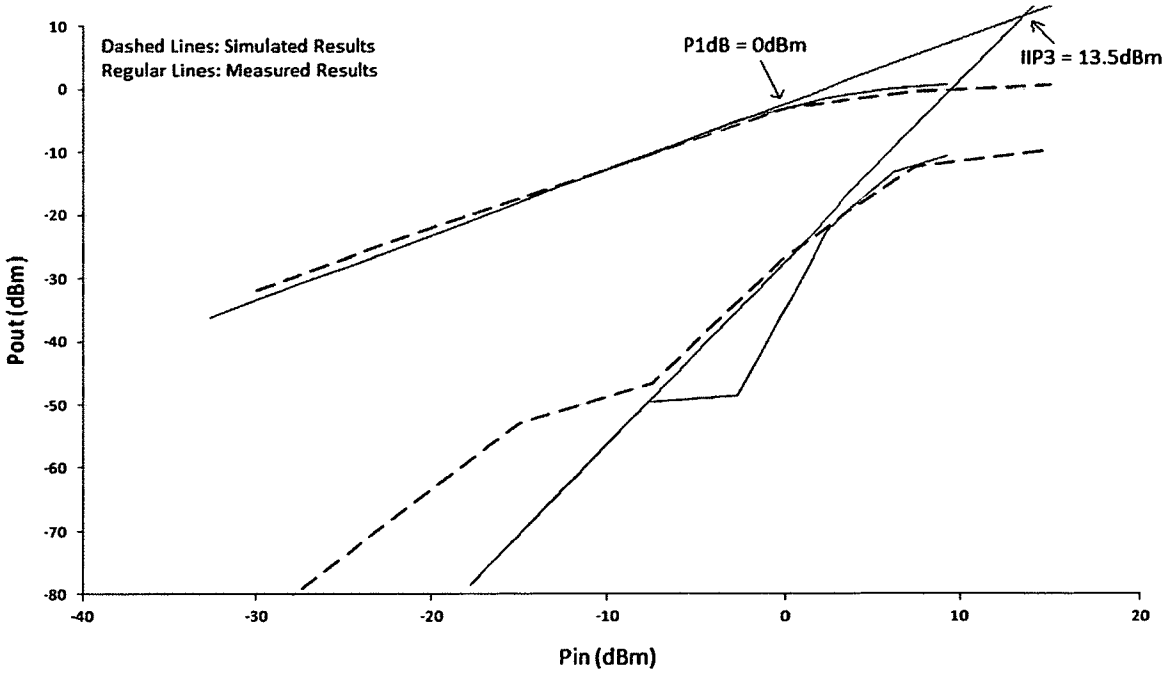

Figure A-2. Simulated and measured linearity results for lowest gain at lowest frequency band

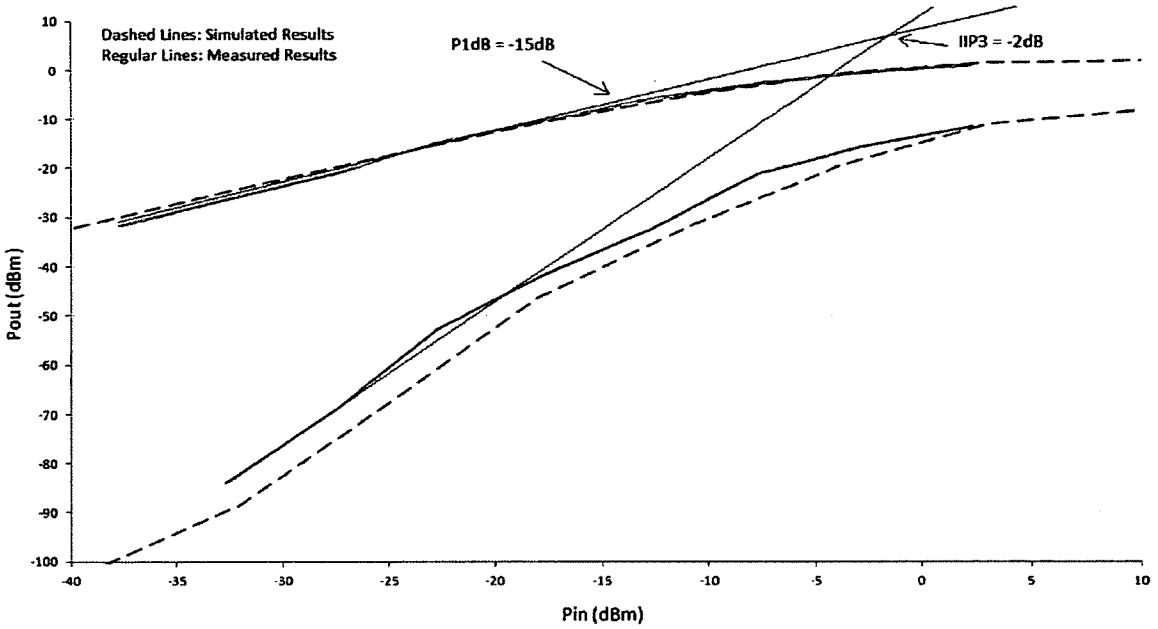

Figure A-3. Simulated and measured linearity results for highest gain setting at highest frequency band

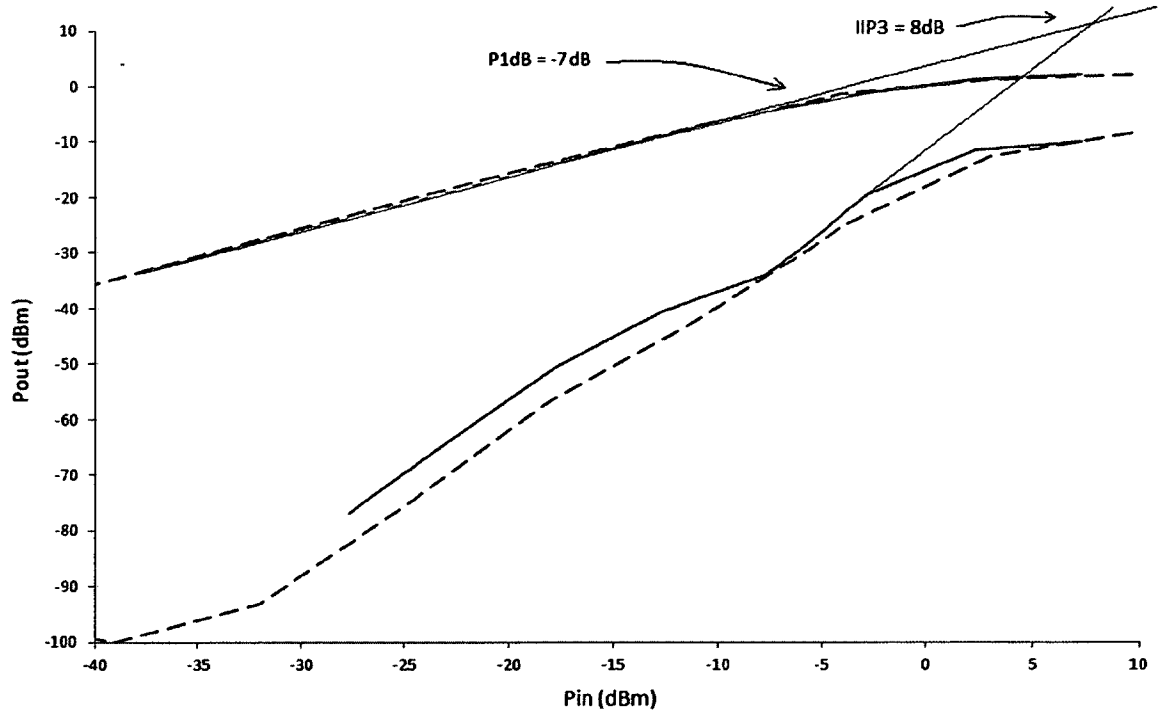

Figure A-4. Simulated and measured linearity results for lowest gain setting at highest frequency band

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