A Low-Voltage CMOS Imager with Wide Dynamic Range

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requirements for the degree

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The undersigned recommend to the Faculty of Graduate Studies and Research the acceptance of this thesis:

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submitted by Justin Fortier in partial fulfillment of the requirements for the degree of Master of Engineering.

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Abstract

CMOS image sensors offer lower cost and the potential for higher levels of system integration than do charge coupled device (CCD) imager sensors. To take full advantage of this potential for system integration, it will be necessary to migrate imager designs to more advanced CMOS processes, as technology scales. This in turn will require the design of imagers capable of operating with greatly reduced power supply voltages compared to those now commonly in use. Reduction in power supply voltage is known to degrade the dynamic range of conventional imagers.

A CMOS imager designed and fabricated in a 0.18 μm digital CMOS technology operating from a 1.2V power supply is presented in this thesis. The imager uses column parallel, second-order delta-sigma analog-to-digital converters, along with a digital signal processing technique to achieve high dynamic range for this low supply voltage. In experimental tests the imager was shown capable of measuring input light levels ranging over 5 orders of magnitude.

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CHAPTER 1.0 Introduction to CMOS Imaging

Solid-state imagers use a large array (e.g., 1024x1024) of photo detecting elements, or pixels, to capture an image. Each pixel provides an electrical output that is proportional to the light intensity at the appropriate point in the image. The pixel's output is converted into a digital value with an analog-to-digital converter, it is stored in a random access memory, and it is later read by a computer for processing and printing.

Presently, there are two competing device structures used in solid-state imaging. These are CMOS and charge-coupled devices (CCD). Imaging systems benefit from CMOS implementation over that of CCDs for several reasons. The main ones are listed below:

- The cost of the system is reduced because of the possibility of implementing a complete system on chip;
- The process is cheap and generic making it easily accessible to fabless design houses;
- The power supply is at digital logic levels increasing its suitability for portable consumer products by reduced power consumption;
- The array can be accessed in ways that make for easy processing, (for example, windowing, subsampling, random access, etc.)

CCDs are made with a very specialized, and consequently expensive, process technology that promotes low leakage, low thermal noise, and high photo-absorption. They achieve higher image quality than CMOS imagers and are presently dominant in consumer applications.

The first two of the points above are the driving force behind the recent burst of research activity in the field of CMOS imaging. As state-of-the-art CMOS processes drop to 0.1 μ m the ultimate goal of a fully monolithic digital camera becomes more of a possibility. However, the reduction in feature size forces a reduced supply voltage. The reduction of supply voltage will pose a challenge to obtaining the required resolution and dynamic range from the pixel array.

1.1 Process Scaling and its Effect on Imager Dynamic Range

For imagers, dynamic range is the ratio of the largest “nonsaturating” pixel output signal and the standard deviation of the pixel’s output noise under dark conditions.

Reducing the supply voltage, as required when migrating from a 0.5 μm to 0.15 μm CMOS process, may reduce the largest nonsaturating pixel input by 12 dB. This corresponds to a factor of 4 reduction in pixel swing, incurred when going from a 5 V to a 1.25 V system. This seems likely to reduce the dynamic range achievable by the imager.

If the three-sigma (3σ) noise component of the pixel output is less than the ADC least-significant-bit (LSB) voltage, then dynamic range is not lost, (this assumes that the required number of bits is attainable in the new technology). Quantitatively,

$$V_{LSB} = \frac{V_{REF}}{2^N}, \quad (\text{EQ 1})$$

where V_{REF} is the max. input voltage (dependent on V_{dd}), N is number of bits, and thus V_{LSB} is the minimum voltage level that can be quantized by an ADC.

If the pixel output noise is greater than the required V_{LSB} , then it will limit the dynamic range of the imager.

1.2 Summary of This Work

This thesis presents a 1.2V CMOS image sensor implemented in 0.18 μm digital process. It employs column-level oversampling and digital decimation filtering to reduce the sensitivity of the low-voltage imager to background circuit noise. The combination of oversampling and customized digital filtering yield an imager with a dynamic range of over five orders of magnitude.

This thesis is organized into 7 chapters:

Chapter 2 begins with a brief description of the electrical processes at work within a typical CMOS imager. It then goes on to highlight the problem of the imager's limited dynamic range and gives a literature review of recent research aimed at tackling the problem. The benefit of oversampling is expressed, particularly when implementing imagers in state of the art CMOS processes. This leads into a review of previously reported oversampled imagers and then into the background theory of delta-sigma analog-to-digital conversion.

Chapter 3 specifically describes the method by which wide dynamic range is achieved here at the low supply voltage of 1.2 V. Oversampling at the column along with digital decimation filtering is used to reduce the pixel's circuit noise contribution, increasing the signal-to-noise ratio for low illumination levels. This, in combination with the use of a high resolution analog-to-digital converter expands the capability of the imager to capture illumination information within a short photo integration period. Pixel saturation time is also recorded should it occur during the integration time. This expands the dynamic range for high illumination levels. The number of samples, clock frequency, and the resulting frame rate are specified in this chapter.

Chapter 4 goes through the design methodology used for the 4x4 test array, implemented in TSMC 0.18 μ m, 1P6M, digital CMOS process. The test chip is designed for a 1.2V supply voltage. Test structures include a pixel array, timing and readout circuitry, and four column-parallel second order-delta sigma modulators. Special attention is paid to the design of a high resolution delta-sigma modulator such that it fits into the tight aspect ratio prescribed by the pitch of the pixel array. Both simulation data and plots of the physical IC layout are presented to support and illustrate key points of the design.

Chapter 5 goes through the sinc decimation filtering algorithm with particular attention to its hardware implementation. Simulation data of the noise attenuation capabilities of a first-order and second-order sinc filter are presented in relation to the specific application of decimation filtering for the column level second order modulator. An estimate of the number of flip flops required to implement the necessary second order filter is given. An algorithm for the overall pixel slew rate

calculation based on a least mean squares regression technique is also given. Simulation data for the over-all system is presented.

Chapter 6 presents data obtained through the characterization of the test chip with the digital signal processing algorithms. The pixels are tested in isolation to characterize their dark leakage current. The second-order, delta-sigma modulator is also tested alone to characterize its output response to an input tone of varying amplitude. In doing this an estimate of the modulator's effective number of bits is found. Next the modulator and digital signal processing technique are tested for input ramps of varying slew rates. In this way the dynamic range of the analog-to-digital conversion process, as it will be used within the imaging system, can be observed. Next the array is tested under illumination. The digitized column outputs are compared to observe fixed pattern noise introduced by the column level, delta sigma modulators.

Chapter 7 draws the thesis conclusions and proposes future work.

CHAPTER 2.0 Background

The CMOS imager's focal array is laid out in a manner similar to that of a random access memory, as shown below in Figure 1.

FIGURE 1. Block level diagram of the arrangement of pixels in the focal array

The rows and columns are used to access the pixel voltage when taking an image. The pixel structure and its mode of operation are described next:

2.1 The CMOS 3-T Active Pixel Sensor

The three transistor (3-T) active pixel sensor (APS) has become the standard pixel structure used in CMOS imagers. A schematic is given below in Figure 2.

FIGURE 2. Circuit schematic of the three transistor active pixel sensor (3-T APS)

Photo-integration and pixel read-out are described below:

1. The photodiode (PD) is initially precharged to a high level through transistor M1 and is then isolated by turning M1 off.

The precharge reverse biases the diode, charging the depletion capacitance. The stored “pre-charge” begins to slowly leak away due to thermally generation of electron-hole (e-h) pairs in the depletion region. This thermally generated current is known as “dark current”.

2. When the imager is exposed to light (i.e., the scene to be imaged) incoming photons are absorbed by the silicon, generating e-h pairs at a rate that is proportional to the impinging light intensity.

Photons in the visible light range have a greater energy than the band gap of silicon. The photon’s energy will excite an electron from the valence band into the conduction band. These photo-

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induced carriers drift to, and are swept across, the depletion region, making the pre-charge voltage leak away at a rate effectively proportional to the light intensity.

The photodiode's response to different wavelengths of light does vary. Red light, being of a long wave-length (and low photon energy), has a probability of travelling further into the silicon than blue light, before exciting an e-h pair. Where the photon is absorbed in the photodiode has an effect on conversion efficiency. For simplicity unit quantum efficiency, (i.e., one photon to one e-h pair), is usually assumed.

3. After some amount of time (T_{int}) the voltage level of the pixel is read out (via a Row addressed access transistor -- M3 in Figure 2, pg. 14) onto the pixel's column line.

The pixel voltage is driven onto the column line via a source follower (M2 in Figure 2) which serves to buffer the photodiode from the column.

An example of the voltage waveform at the pixel output is given below in Figure 3.

FIGURE 3.

Pixel voltage waveform with respect to various points of time within the integration period

4. Correlated double sampling (CDS) is used to cancel any mismatch in the threshold voltages of the read out and precharge transistors.

Correlated double sampling involves sampling the pixel's output voltage level immediately after precharge (Sample 1) and then later subtracting the output level after the integration period (Sample 2). For ease of implementation, often Sample 2 is taken first, then the pixel is reset and Sample 1 is obtained. This allows for the processing to be done in the analog domain prior to digital conversion.

5. A rolling shutter is often used for imagers using the 3-T pixel format.

The rolling shutter technique involves reading out one row while the next row -- (and a number of subsequent rows) -- are in their integration period. This makes for a fast read-out and thus high frame rate. Integration periods of from 3 - 10 ms are common in a 5V system [1] [4] [8].

2.2 *Enhancing the Imager's Dynamic Range*

Light intensities may vary over 7 orders of magnitude in a typical scene illuminated by natural light. Our eyes can easily register light intensity variations of about 4 orders of magnitude in any one scene. Interestingly, a "good" black and white film will only capture an image with intensities varying by a factor of 128 (or, 7 f-stops) [2]. This is a motivation for maximizing the dynamic range of CMOS imagers and using post processing to enhance the appearance of the resulting image. Figure 4 illustrates this point.

If we were to view a scene, like that in Figure 4, our eyes would naturally adjust to the average illumination levels (or, white balance). We would be able to resolve much of the detail within the shadows as well as those areas illuminated by sunlight. The photograph on the left in Figure 4 is the original image. The histogram below it shows the number of pixels that fall within each of the digitized quantization levels (between 0 and 256). Here most of the information about the scene is

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made up of tightly spaced quantization levels around black (0), and thus, the contrast is too low to resolve much, if any, of the detail.

FIGURE 4. Dynamic range enhancement through white balancing.

By remapping the digital levels so that they encompass a broader range, (i.e., by spreading them out), the contrast is increased and details become more resolvable. The difference is seen in the image on the right.

The captured image data can be manipulated to produced a higher quality photo, (i.e., a picture that looks better), but this data must be first captured. The problem associated with capturing an image with a large “intrascene” dynamic range is the subject of much research. A summary of the recent literature presents a few of the reported techniques used to increase the dynamic range of CMOS imagers.

2.3 Literature Survey and Summary

This section has been included to give the reader a background on the depth of research dedicated to solving the problem of limited capture range. The articles presented do not specifically address the limitations imposed by a low-voltage design.

[3] introduces a pixel with logarithmic response to light intensity. The pixel resembles that of the integration mode 3-T APS but the gate of the reset transistor is kept at the positive supply. This device (M1 in Figure 1, on page 3) operates in sub-threshold for a range of photocurrents, and acts as a load to the photodiode. The pixel has a logarithmic response for 5 decades of light intensity. The major problem with this type of pixel structure is that it is difficult to use CDS to cancel threshold mismatch and $1/f$ noise. This paper reports a pixel fill factor of 25%, and a frame rate of 8 s^{-1} .

[4] reports a technique that uses digital post processing to achieve a wide dynamic range image. At least two images of the scene are taken, one with a short integration time and then another with a long integration time. The short integration time captures information about the high level illumination aspects, while neglecting the low level illumination aspects of the scene. A subsequent long integration time captures the low level illumination aspects. These two images are then digitally averaged using post processing techniques to synthesize an image with wide dynamic range. A disadvantage of this method is that each image must be captured twice. This paper reports a pixel fill-factor of 15% and a synthesized dynamic range of 105 dB.

[5] introduces a pixel which has a digitally controlled illumination to output voltage transfer function. The pixel is the standard 3T APS in structure but its mode of operation is different. The pixel is precharged by driving the gate of M1 high, but then instead of bringing the gate low directly, during the integration time, it is successively stepped down in voltage. The voltage across the photodiode is not allowed to drop below ($V_{gs} - V_t$, of M1) over the integration period. The pixel's response to high illumination is compressed. CDS techniques are used to correct for threshold mismatch. However, a disadvantage is that clock feed through to the pixel can't be com-

pensated for easily. This paper reports a pixel fill-factor of 49%, a maximum dynamic range of 96 dB at the pixel while using column-parallel 9 bit on chip ADCs to quantize the pixel's output. An impressive maximum frame rate of 390 s^{-1} for the $256 \text{ k} \times 256 \text{ k}$ array is reported.

[6] reports the use of an ADC technique which compresses the digitized output of a pixel's high light level outputs and expands the pixel's low level outputs. This technique doesn't increase the light range that the pixel is able to handle, but instead it merely performs white balancing within the ADC after the image has been captured. The paper reports 10 bit (60dB) resolution with a 3.3V supply.

[7] introduces a current mode pixel structure in which each pixel has one photodiode and one MOSFET. Each group of four pixels share buffer circuitry that feeds the pixel's output photocurrent onto the column line. The buffered photo-current is used to slew down a relatively large column level capacitance, and voltage is read from the capacitor after an integration time. Here range is increased at the cost of sensitivity.

[8] uses an ADC within the CMOS imager's pixel structure so that pixel values are available to the ADCs at all times throughout integration. Here, four pixels time multiplex a single-slope ADC, made up of a simple opamp and capacitor. The ADC is bit serial and reads out at 2^N time intervals during an integration period. This is similar to the technique of [4] in that multiple images of the scene are effectively captured for short and long integration times, and an image with wide dynamic range is synthesized by averaging these images. A trade off between frame-rate and dynamic range is highlighted in this paper. The technique achieves a dynamic range of 4 orders of magnitude with a composite 16 bit output word. The pixel fill-factor is 29%.

[9] reports an asynchronous pixel-parallel ADC structure. The pixel is used as an integrator in a sigma-delta modulator. Wide dynamic range is obtained by allowing the pixel to slew down until a threshold is crossed, outputting a digital one and then precharging the pixel again. Accuracy is achieved by repeating the process many times and digitally processing the output data over some

integration period. Each pixel contains 19 transistors and a photodiode. Fill factor and frame rate are not given.

After reviewing the literature, one thing becomes clear: dynamic range enhancement always adds complexity to the imaging system, over that described in Section 2.1 on page 14. The techniques usually involve manipulating the sensitivity of the pixel, such that it is less sensitive to high illumination levels, or adaptively setting the integration time based on illumination levels. These also involve tailoring the analog-to-digital conversion technique and using digital post processing to make an image with wide dynamic range.

Most of the techniques described above do not make provisions for low voltage implementation, and thus, are not inherently suitable for implementation in a state of the art digital CMOS processes. The technique proposed in this thesis is driven by a low-voltage implementation. It achieves wide dynamic range by reducing the system's sensitivity to pixel noise. It does this by increasing the system's digital complexity and post processing.

2.4 *Dynamic Range Expansion Through Noise Filtering*

Correlated double sampling uses the minimum number of samples required to calculate the pixel's slew-rate, (i.e. 2 samples). Calculating slope inherently cancels any DC offset and attenuates the low frequency noise in the pixel's output. Higher frequency noise, however, must be a small percentage of the pixel's output or else noise will 'fold-over' during sampling [10] and it will corrupt the slew calculation.

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Noise becomes especially problematic with reduced supply voltage. The effect of fold-over can be seen in Figure 5.

FIGURE 5. Noisy voltage ramp representing pixel output voltage over the integration period

If integration time is increased to achieve an adequate signal-to-noise ratio for a darker pixel, then a brighter pixel will saturate and nothing is gained. Pixel noise could be filtered before the correlated double sampling operation, but high order low-pass filters are typically not used in imager systems because of their high power and area requirement. Reducing pixel noise is the focus of much research [11] [12] [13].

Besides using strict analog circuit design techniques to reduce noise, pixel output noise can be reduced by oversampling the pixel and digitally filtering the digitized pixel output [14]. That is, the more data points that are taken, the more accurate the calculation of pixel slew-rate becomes. Oversampling will bring more of the high frequency noise into the digital domain such that it can be filtered there.

Generally speaking, the signal-to-noise ratio increases by a factor of $\sqrt{2}$ (or 3 dB) for every doubling of the minimum number of samples. That is, every time the number of samples needed for conversion is doubled, the signal component doubles and the noise component increases by a fac-

tor of $\sqrt{2}$. This gives a net gain in the signal-to-noise ratio of a factor of $\sqrt{2}$, assuming a gaussian noise distribution [15].

This increase in the pixel's signal-to-noise ratio will allow for shorter integration times and thus wider dynamic range. Computing the pixel's slew rate in the digital domain is simple enough: digital low-pass filters are easily implementable and require far less silicon area than analog switch-capacitor filters, especially in modern CMOS processes.

2.5 *Oversampling the Pixel Output at Low-Voltage*

Pixel-level oversampling has been reported [9] [16]. Both of these references make use of first order $\Delta\Sigma$ type ADCs. They report the wide dynamic ranges of 103 dB and 85 dB, respectively. Pixel-level ADCs are attractive because of their process scalability and digital read-out over the column bus. One bit, single loop, $\Delta\Sigma$ modulators are fairly insensitive to component mismatch and can achieve high resolution conversion by way of quantization noise shaping [15]. Matching from pixel-to-pixel is as good as to 1% when a switched-C implementation is employed [16]. However, the pixel level ADC causes a significant loss in fill factor. A fill-factor of 3% was reported in [16]. Also, the limited space at the pixel makes building a high performance $\Delta\Sigma$ modulator impossible and thus SNR is low for darker pixels. This rules out pixel-level oversampling.

Column-level data conversion requires a mid-speed ADC for a given frame rate. Successive approximation ADCs have been used at the column [17] [18] [19]. Column-to-column mismatch becomes a concern for ADC's that depend on analog component matching for linearity. Successive approximation ADCs rely on binary scaled capacitors for digital encoding of the analog input. The tight pitch constraints of the column make common centroid layout of capacitors difficult. Device matching and circuit noise limit the resolution of the ADC especially when small capacitors are used to fit column pitch constraints. At low supply voltages, a high resolution successive approximation ADC might be unrealizable -- this can be seen by the image captured in [19] with a low power supply voltage of 1.2V.

One-bit, column-level, $\Delta\Sigma$ modulators have been reported previously [20] [21]. [20] reports the use of a second order “current mode” $\Delta\Sigma$ modulator to convert the pixel’s DC photocurrent into an output bitstream. The pixel’s output here is a DC quantity making pixel offset cancellation a more cumbersome task (not merely the calculation of slope). Pixel offset (known to cause fixed pattern noise) is reduced by subtracting a pixel reference current from the pixel photo-current prior to converting it to digital. The $\Delta\Sigma$ modulator’s digital bitstream is filtered with a first order digital averaging filter. This thesis shows, in Section 5.1 on page 62, that a first order averaging filter will not sufficiently attenuate the out-of-band noise produced by a second order modulator for wide dynamic range analog-to-digital conversion. The paper predicts a rather low frame rate of 1 s^{-1} for a 1M array. [21] uses a column-level first order $\Delta\Sigma$ modulator implemented with a standard switched-capacitor topology. The pixel output voltage is sampled 1024 times, thus converting its output voltage into 1024 one-bit digital values. These one-bit outputs are then digitally summed, which is the equivalent of averaging, and the pixel output is represented by a 10 bit binary number. Once again, dynamic range is limited by the $\Delta\Sigma$ modulator’s quantization noise, and the pixel’s fixed pattern noise.

This thesis will show that with proper digital signal processing, a CMOS imager employing column level $\Delta\Sigma$ modulators can achieve very wide dynamic range, with a reasonable frame rate, even at low supply voltages. [22] reports a 77 dB, $\Delta\Sigma$ modulator with a sampling frequency of 1.538 MHz realized in a $0.5 \text{ }\mu\text{m}$ standard CMOS process. This modulator dissipates $40 \text{ }\mu\text{W}$ of power with a supply voltage of 900 mV. This is adequate for the purposes of column-level over-sampling and this leads to a brief background on $\Delta\Sigma$ ADCs.

2.6 $\Delta\Sigma$ ADC Background

$\Delta\Sigma$ analog-to-digital converters have gained popularity in low bandwidth applications because of their suitability for digital sub-micron CMOS implementation.

The $\Delta\Sigma$ ADC system architecture does away with the need for highly matched analog components. The modulator combines oversampling with quantization noise-shaping to achieve high digital resolution in a narrow band. A digital decimation filter attenuates out-of-band noise and reduces the sampling rate. A single loop, one bit, low pass $\Delta\Sigma$ ADC is shown below:

FIGURE 6. A block level diagram of a low pass, $\Delta\Sigma$ analog-to-digital converter.

The decimation filter, in Figure 6, can be implemented with purely digital circuit blocks, and thus high-order rolloff is readily achieved. Its operation is discussed further in Chapter 5.

The $\Delta\Sigma$ modulator is often implemented with discrete time, “mixed-signal”, circuit components. The order of the low pass filter ($LPF(z)$) defines the order of the modulator. $LPF(z)$ shapes quantization noise away from the input frequency band. This can be seen by writing a transfer function for a linear approximation of the modulator.

A linear approximation of the $\Delta\Sigma$ modulator assumes that the quantization error ($E(z)$) is not correlated to the input ($IN(z)$).

FIGURE 7.

Linearized model of the $\Delta\Sigma$ modulator

EQ. 2, below, describes $Y(z)$ in terms of $IN(z)$ and $E(z)$, as derived from the block diagram above. The multiplying factors of $IN(z)$ and $E(z)$ are called the signal transfer function (STF) and the noise transfer function (NTF) respectively. Here it can be seen that $E(z)$ is attenuated and $IN(z)$ is passed to the output when the magnitude of $LPF(z)$ is sufficiently large. This is the general idea behind noise shaping converters.

$$Y(z) = \frac{LPF(z)}{1 + LPF(z)} IN(z) + \frac{1}{1 + LPF(z)} E(z) \quad (\text{EQ 2})$$

2.6.1 First Order $\Delta\Sigma$ Modulator

The transfer function equations defining the First-order, Low-Pass, $\Delta\Sigma$ Modulator are given below. Key to its design is the use of a discrete-time delaying integrator for the $LPF(z)$.

$$LPF(z) = \frac{z^{-1}}{1 - z^{-1}} \quad (\text{EQ 3})$$

Substituting EQ. 3 into EQ. 2 gives:

$$Y(z) = z^{-1} \cdot IN(z) + (1 - z^{-1}) \cdot E(z) \quad (\text{EQ 4})$$

Background

From EQ. 4 the STF has a magnitude of 1 for all frequencies ($0 < f < f_s/2$):

$$STF = z^{-1} = e^{-j2\pi\frac{f}{f_s}} \quad (\text{EQ 5})$$

The NTF, on the other hand, has a magnitude of 0 at DC ($f = 0$) and a magnitude of 2 at high frequencies ($f = f_s/2$). Hence, quantization noise is “shaped” away from DC.

$$NTF = 1 - z^{-1} = 1 - e^{-j2\pi\frac{f}{f_s}} \quad (\text{EQ 6})$$

The magnitude and phase response of this noise transfer function is given below:

FIGURE 8. Magnitude and phase response of the NTF of the first order modulator, plotted for angular frequencies normalized to π .

So, if the input is band limited such that spectrally it “fits” into the quantization noise notch created by the NTF, then the output of the modulator can be lowpass filtered digitally to render a high resolution analog-to-digital conversion. To do this, however, the input must be “oversampled”, that is, the input signal bandwidth (up to f_{in}) must be much less than half of the sampling

frequency ($f_s/2$) as shown in the block diagram of Figure 6. The ratio of $f_s/2$ to f_{in} is known as the oversampling ratio (OSR). The quantization noise power “in band” is usually calculated with respect to the OSR [15].

$$P_{noise} = \frac{\Delta^2 \pi^2}{36} \left(\frac{1}{OSR} \right)^3 \quad \text{where: } \Delta \text{ is the LSB step size} \quad (\text{EQ 7})$$

Every doubling of the OSR leads to a 9 dB increase in signal to quantization-noise ratio, within the input frequency band. Compare this with the 3 dB increase in SNR obtained from just oversampling alone, without noise shaping, as obtained for the input signal.

Intuitively speaking, squaring the noise transfer function of EQ. 6 will create even less quantization noise in band, (the square of a small number is a smaller number). This is the basis for the design of the second order, low-pass, $\Delta\Sigma$ modulator.

2.6.2 Second Order Modulator

The block diagram for the second order modulator is exactly the same as that in Figure 6. The loop filter, $LPF(z)$, has characteristics such that the modulator’s noise transfer function is given by EQ. 8.

$$NTF_{order2} = (1 - z^{-1})^2 = 1 - 2e^{-j2\pi\frac{f}{f_s}} + e^{-j4\pi\frac{f}{f_s}} \quad (\text{EQ 8})$$

Here, quantization noise is lower in-band but the level rises more steeply as frequency increases. The in-band quantization noise power for a second order modulator is given by [15]:

$$P_{noise, 2} = \frac{\Delta^2 \pi^4}{60} \left(\frac{1}{OSR} \right)^5 \quad (\text{EQ 9})$$

Substituting EQ. 8 into the NTF of EQ. 2 and solving for $LPF(z)$ gives:

$$LPF(z) = \frac{z^{-1}(2 - z^{-1})}{(1 - z^{-1})^2} \quad (\text{EQ 10})$$

Direct substitution of this $LPF(z)$ to solve for the STF of the second-order modulator yields a transfer function with a non-flat spectral response:

$$STF_{order2} = 2z^{-1} - z^{-2} \quad (\text{EQ 11})$$

EQ. 11 gives a STF with magnitude of 1 at $f = 0$ and a magnitude of 3 at $f = f_s/2$. The Bode plot of this STF is given below:

FIGURE 9.

Phase and magnitude response of the STF of EQ 4, plotted for angular frequencies normalized to π .

The most common implementation of the $\text{LPF}(z)$ of EQ. 10 corrects for this non-flat STF. The $\text{LPF}(z)$ can be implemented with the cascade of two, discrete-time, integrators as show in Figure 10. These integrators are readily implementable switch-capacitor circuit components.

FIGURE 10.

A block level implementation of the linearized second order $\Delta\Sigma$ modulator with the typical implementation of the $\text{LPF}(z)$.

The NTF for the modulator in Figure 10 is that of EQ. 8, but the STF is simply z^{-2} . This STF has a magnitude of 1 for all input frequencies.

The quantizer is a two level comparator and the loop gain of the modulator forces the $\text{LPF}(z)$ DC output to be equal to the comparator trip-point. So the integrator gain can be set to keep signal levels within the circuit boundaries, while maintaining the proper STF and NTF.

2.7 Chapter Summary

Many methods have been proposed for enhancing the dynamic range of CMOS image sensors. Most methods adjust the integration time or pixel sensitivity so that the pixel will not saturate. Correlated double sampling and Nyquist rate analog-to-digital converters are typically used to suppress $1/f$ noise and pixel offset and to digitize the pixel slope function. The pixel's high fre-

quency noise will limit the dynamic range of low voltage CMOS imagers to unacceptably low levels. Oversampling the pixel output is a way to reduce the noise fold-over content during the analog-to-digital conversion process. Once digitized out of band noise can be filtered digitally, effectively increasing the signal-to-noise ratio of the pixel's output. $\Sigma\Delta$ modulators are well adapted to low voltage, high resolution, analog-to-digital conversion. They have been used in reported CMOS imagers.

CHAPTER 3.0 Low-Voltage Imager: Design Choices

CMOS imagers with a supply voltage on the order of two threshold voltages must implement circuit techniques to increase head room at the pixel. V_T of transistor M1, in Figure 11, could be reduced through process modification but this will cause unacceptable leakage during photo integration. Besides, process modification is expensive and therefore undesirable.

A solution to the pixel head room problem, as discussed in [23] and used in [19], is to overdrive the gate of M1. This increases the operating voltage range of the pixel by one MOSFET threshold voltage -- in this case almost doubling the signal swing. This can be accomplished the same way that it is for DRAM, either by bootstrapping, or by way of an on chip charge pump and level shifted driver.

FIGURE 11.

3-T APS and voltage waveform with respect to various points of time within the integration period with M1 being overdriven.

This alone is not enough to expand the dynamic range of the imager significantly. The imager's dynamic range is further increased by oversampling the pixel's output and digitally processing the output data in a way that is described in detail in the next section.

3.1 *Dynamic Range Expansion Through Saturation Detection*

Oversampling will increase dynamic range by making lower illumination signals resolvable for shorter integration periods, as was described in Section 2.4 on page 20. The $\Delta\Sigma$ modulator is also used to detect pixel saturation, should it occur during the photocurrent integration period. That is, $\Delta\Sigma$ modulators are known to overload when their input is driven out of the bounds of the feedback. When overload occurs the modulator outputs a string of 1,1,1,1,1 or 0,0,0,0,0 depending on the input level.

Pixel saturation will cause the $\Delta\Sigma$ modulator's input to go "out of bounds". By monitoring for such an occurrence (during decimation) a dual function ADC is created. This requires a little added digital circuitry, (i.e., two additional accumulators are needed to digitize the reference crossing: one that counts sequential 0's to a predetermined number, and another that counts clock-cycles during the decimation interval).

Low-Voltage Imager: Design Choices

A United States Patent Application entitled, “Imager Output Signal Processing”, Serial number 60/256,336, is based on the ideas illustrated below in Figure 12 and Figure 13.

FIGURE 12.

A plot of pixel voltage during the integration period with the corresponding mode of operation for the proposed ADC.

Matlab simulations showing the two modes of operation are given below to add detail:

FIGURE 13.

Matlab simulation plots for ADC processing for non-saturating pixels (on the left) and saturating pixels (on the right).

3.2 The Over-Sampling Imager

A conceptual floorplan of the new imager is shown in Figure 14. The standard 3T pixel is to be

FIGURE 14. Conceptual floor plan of the column level oversampled imager.

used in the focal array. Oversampling ADCs and decimation filters are column-parallel. Outputs from the decimation filter are to be time multiplexed and bused off-chip to a subsequent digital image processor. Here, the row access pulse is driven high for the entire integration time while the oversampling ADC and decimation filter quantizes the pixel output, as described in the previous section.

A second-order, single-bit, single-loop, $\Delta\Sigma$ modulator was the ADC architecture of choice because of its well understood behavior and wide dynamic range [15]. A pixel slew calculation was to be based on 1024 samples, (i.e., doubling the minimum number of samples nine times). This level of oversampling will increase the signal-to-noise ratio of the pixel's slew-rate by 27 dB. This increase in SNR enables the reduction of the required integration time. The sampling rate was chosen to be 10 MHz and thus the 100 μs photo integration period would yield a frame rate of 10 s^{-1} for a 1M array. 10 frames per second is typical for consumer-grade digital cameras running in "rapid-fire" mode [2].

The decimation rate change factor was chosen to be 64 so that, after decimation, the pixel's output would be represented by 16 high resolution samples, assuming saturation did not occur. An ideal second-order $\Delta\Sigma$ ADC will yield 13.5 bits for an oversampling ratio of 64, assuming "brick wall" decimation filtering and zero circuit noise at the input.

Sinc (or comb) decimation filters are typically used as the first down-sampler in multi-rate decimation schemes because of their simple architecture. Higher order filters are used to reduce the intermediate sampling rate to the Nyquist rate.

Here the sinc filter is to be followed by a slope calculation in the digital domain. This slope calculation is the last stage of filtering and could be performed by the image processing DSP performing linear regression.

3.3 Chapter Summary

In the imager system reported here, many samples are taken at a very high sampling rate with a $\Delta\Sigma$ modulator. The output from the modulator is then low-pass filtered and down sampled digitally, increasing the resolution of conversion and decreasing the sampling rate to manageable levels. Decimation filtering also attenuates the out of band noise, increasing the signal-to-noise ratio of the pixel output. Oversampling the pixel output with a $\Delta\Sigma$ modulator also allows for pixel saturation detection in the digital domain. In this way the $\Delta\Sigma$ modulator is being used as a high resolution analog-to-digital converter for pixels with low levels of illumination, and as a single slope converter for those with high levels. In a product version of this imager, the resulting "first stage" (decimation / saturation detection) digital signal processor would have to be implemented on the same die as the focal array and $\Delta\Sigma$ modulators so that data could be bused off chip. The final conversion step of slew rate calculation could be done in a separate digital image processor. The modulator sampling rate was selected so that a full scale (1000 x 1000) array would have a frame rate of 10 s^{-1} .

CHAPTER 4.0 Design and Implementation

A 4x4 test array has been designed for 1.2 V supply operation using TSMC's 0.18 μm (6M1P) digital CMOS process. The 1.5 mm x 1.5 mm test chip is bond pad limited, Figure 35, pg. 60. Although this is a very small pixel array (just 16 pixels), it serves to prove the general operation of the oversampling imager. Matlab routines have been written to process the output bitstreams from the column-level $\Delta\Sigma$ modulators. This software implementation of the decimation and slope calculation could later be replaced with dense digital logic designed using a standard RTL, synthesis, and place and route design flow.

This chapter presents design details of the fabricated imager test array. Layout and simulation data are presented to illustrate key points of consideration.

4.1 3T Active Pixel and Array Design

The cell structure used here is the typical 3T APS, refer to Figure 2, pg. 14. The photo receptor, a n+ p substrate photodiode, occupies 62% of the cell's total area. The cell dimensions are 15 μm x 15 μm . These design choices were made based on success in similar structures previously reported in [24]. The 4 x 4 pixel array occupies a total area of 5580 μm^2 . The resulting photodiode fill-factor is just over 40%. The layout could be tightened quite easily to increase this to an estimated 50%.

The silicide exclusion layer was used over the photodiode to ensure photo absorption in the cell. This exclusion mask layer is common in modern salicided CMOS processes to create poly silicon and diffusion resistors with a high sheet resistance. This is a necessary step for the CMOS pixel, since salicide is known to absorb light [25]. Metal 3 was used as a light shield, as in [25], for the

circuitry in the pixel. Here, metal 3 was chosen because of its close proximity to the silicon active layer, thus reducing the amount of light able to get in via sidewall reflection.

The pixel reset transistor's gate, (M1 in Figure 2), is driven with a clock voltage that is at least one threshold higher than the nominal V_{DD} . This transistor is of minimum width and slightly larger than minimum gate length ($0.5\ \mu\text{m} / 0.35\ \mu\text{m}$) to help reduce the off current caused by short channel effects (such as drain induced barrier lowering).

The pixel's source follower output buffer was designed to be a fairly large device ($20\ \mu\text{m} / 0.75\ \mu\text{m}$) with a longer channel length. This helps to reduce transistor g_m mismatch caused by gate length variation from pixel-to-pixel. Its 3 dB bandwidth is high enough to accommodate the brightest pixel. Simulation data of the source follower's gain with respect to input frequency is shown below. The pixel source follower bias current I_B is $9.5\ \mu\text{A}$, and its bandwidth ($F_{3\text{dB}}$) is 60 MHz.

FIGURE 15.

3 dB bandwidth of the 3-T APS source follower buffer

The output impedance of the source follower is also important, since it is driving the input of the $\Delta\Sigma$ modulator. The impedance must be low enough to ensure that the column line will settle quickly during switching transients caused by the modulator. Spectre simulation showed that the

worst case output impedance over the range of output voltages was 5.1 k Ω . This low resistance ensures that a column line with the capacitance of 1 pF will settle to 0.1% of its final value in 35 ns. This is suitable for application in a full sized array where column line capacitance is on the order of 1 pF.

4.2 Array Addressing and Pixel Reset

A clock divider is used to count the integration time for each row, allowing 1024 samples to be taken. Rows are selected using a two bit counter and standard decoding circuitry. The circuit diagram for the row addressing is shown in Figure 16.

FIGURE 16.

Integration period counter and row decoder logic

The pixel reset transistor is driven above the rail with a level shifting inverter. The raised supply voltage is supplied off-chip but an on-chip solution would be necessary for a single supply implementation. Techniques to generate this raised voltage on chip are well known and widely used in

DRAM circuits. The level shifting inverter circuit, shown in Figure 17, generates an inverted version of the row access signal ($\sim \text{row } n$) to take the pixel in and out of precharge.

FIGURE 17. Level shifting inverter used to drive V_{pre}

Timing between the pixel precharge (off) and row access (on) is critical in this design to maximize dynamic range. A coupling mechanism, described next, exists between the pixel and the column routing line. The 3T active pixel is shown in Figure 18 with parasitic capacitances clearly illustrated.

FIGURE 18. 3T-APS showing critical parasitic capacitances and steady-state voltages during precharge.

Initially, while the pixel is in reset, the capacitance associated with the photodiode is charged up to V_{DD} . The voltage across C_{gs2} settles to V_t and the capacitance C_S settles to $V_{DD} - V_t$. M2 is on the edge of being off/on.

Now, if the gate of M1 is driven low, M1 turns off and the pixel comes out of precharge. The clock (V_{pre}) couples to the photodiode and its initial voltage is reduced by an amount set by the ratio of the capacitors involved, approximately:

$$V_{DD} - \frac{C_{gs1}}{C_{gs1} + C_{PD}}(V_{DD} + V_t) . \quad (\text{EQ 12})$$

With a minimum sized M1, the charge sharing between C_{gs1} and C_{PD} is minimized.

The row select switch (M3) is next to be selected, (via the 'row' signal), for pixel read-out. The column line capacitance (C_{col}) is shorted to C_{gs2} . The source follower, M2, at this point in time has a high impedance output (since it is on the edge of being off/on). Charge sharing occurs from the column line to the photodiode through C_{gs2} . This brings the initial voltage of the photodiode down further. The bias current I_B eventually pulls the source of M2 down in relation to its gate ($V_{on} = V_{gs} - V_t$) and the source follower turns on. The overall dynamic range of the pixel has been significantly reduced even though it was precharged to full rail.

To avoid this problem the row select signal is activated, (i.e., switch M3 is closed), before the photodiode comes out of precharge. M1 now serves as a low impedance path for the charge from the column line capacitance and the photodiode remains at V_{DD} . Some short time after M3 is closed, M1 is turned off.

The timing circuitry in Figure 19 outputs a signal that delays the inversion of the rising edge of row, but not the falling edge, and this is used to delay pixel's coming out of precharge.

FIGURE 19.

Falling edge delayed inverter logic

4.3 Tight Pitch, Low-Voltage $\Delta\Sigma$ Modulator

The ability to design a relatively complex mixed-signal circuit, such as a $\Delta\Sigma$ modulator, without process modification is of key interest to this research. Determining if a $\Delta\Sigma$ modulator can achieve the required resolution when designed to meet limited area requirements is also of interest here.

A switch-C implementation is chosen for the loop filter design. It is implemented as a cascade of two full-delay integrators, as discussed in Section 2.6 on page 23. The transfer function of the full

delay integrator was given in EQ. 3. The circuit diagram illustrating its implementation is given in Figure 20.

FIGURE 20. Switch-C delaying integrator topology.

The transfer function based on circuit analysis is given in EQ. 13 and is equivalent to that given in EQ. 3.

$$\frac{V_{out}}{V_{in}} = \frac{C_1 z^{-1}}{C_2 \left(1 - \frac{1}{A_o}\right) - \frac{C_1}{A_o} + C_2 \left(\frac{1}{A_o} - 1\right) z^{-1}} \approx \frac{C_1 z^{-1}}{C_2 (1 - z^{-1})} \quad \text{for: } (A_o \gg 1) \quad (\text{EQ 13})$$

A block diagram of the modulator, explicitly showing the structure of the LPF(z) is found below in Figure 21. The comparator is clocked at the end of $\Phi 1$ (the sampling phase) to ensure complete

settling of the integrators. The two level DAC feedback is subtracted on $\Phi 2$, (the feedback levels are $V_{\text{ref High}}$ and $V_{\text{ref Low}}$).

FIGURE 21.

Second-Order, lowpass, one bit, $\Delta\Sigma$ modulator: block level diagram showing filter components explicitly.

The modulator topology is single-ended to help with the constrained area of the column. Differential capacitors, and common-mode feedback circuits are not needed here. The pixel output is also single-ended, and so, a single-ended to differential conversion circuit is also not needed.

The single-ended design causes some concern with power supply noise rejection and charge injection caused by the switches. The architecture might need to be migrated to a fully differential design to help reject a higher level of supply noise that is inevitable in a full imager array. The single-ended design will, however, prove the concept.

4.4 Capacitors Designed in a Digital Process

The pitch of the column will limit the size of capacitors to be used in the modulator. Achieving a high capacitance per unit area is definitely important for this design. One bit, single-loop modula-

tors are tolerant of gain errors caused by capacitor mismatch. This relaxes the need for precise capacitor matching.

TSMC's 0.18 μm CMOS process has six routing metal layers. Routing-isolation-Routing capacitors are inherently linear. The minimum pitch for metal lines, (e.g., M2-M2), is 0.28 μm . The distance between metal layers, (e.g., M2-M3) is 0.8 μm . Metal thickness is 0.53 μm . To get high capacitance per unit area every capacitance available is used, (i.e., lateral, fringe, and vertical). Interdigitated capacitors using layers of interconnect have been reported in [26] [27]. Tolerances on etching, metal thickness, interconnect isolation thickness, and the dielectric constant will affect the absolute value of capacitance. Matching is quite good [26] since it is mainly dependent on the process lithography. The layout of a unit device is shown below:

FIGURE 22.

Plan view and cross section of an interdigitated and stacked routing-isolation-routing unit capacitor.

Circuit extraction shows that the 5 μm x 5 μm unit capacitor in Figure 22 yields a 25 fF device. Top and bottom plate parasitic capacitors are 1.6 fF and 2 fF respectively. The plates are coplanar and this reduces the amount of noise injected into the substrate. Charge travelling through the substrate is localized, (i.e., the top plate parasitic is charging up while the bottom plate parasitic is

charging down). Isolation from substrate noise is further improved by using an n-well (tied to a quiet Vdd) below each capacitor structure.

4.4.1 Capacitor Sizing

Sampling a signal with a switch and a capacitor introduces noise to the system. kT/C is the associated noise power. Decimation filtering reduces the bandwidth of the sampling noise, thus, reducing its power. Input noise power is reduced by 3 dB ($10 \log 0.5$) for every octave of oversampling and decimation filtering used.

Capacitor ratio $C1 / C2$ must be set to $1 / 2$ to satisfy EQ. 10, while ensuring that the signal at the integrator output remains in bounds. $C1$ and $C2$ load the OTA and their absolute values will determine the slew rate needed from the amplifier for proper settling within a given sampling period. The trade off here is low noise for high power.

Since the clock period has been divided into two non-overlapping phases, the total time for opamp settling is just one phase of the clock. With a 10 MHz sampling clock one phase is 50 ns. Assuming half of the total time allotted is for slew rate limited settling, 10 μ A will slew a 250 fF capacitor by 1 V in 25 ns. Setting $C1$ to 200 fF and $C2$ to 400 fF will load the OTA with a 133 fF capacitance during $\Phi2$, refer to Figure 21, pg. 43. This gives some margin for added capacitance due to the input capacitance of the amplifier and compensation capacitors at the output.

The total sampling noise with an input capacitor of 200 fF is 144 μ Vrms. This will be reduced to 18 μ Vrms through oversampling by 64 times and decimation filtering to reduce the “excess” bandwidth. Three times this gives the 3σ peak noise voltage of 54 μ V. A 14 bit ADC at a 1.2 V supply voltage has a $V_{LSB} = 73 \mu$ V. The sampling noise will not be the limiting factor to the ADC resolution. Thus, the 200 fF sizing of $C1$ is considered adequate.

The sampling capacitor, C_3 , of the second stage integrator can be made smaller since noise at this input is differentiated (first order noise shaped) by the $\Delta\Sigma$ loop. This gives a reduction in noise power of 9 dB for every octave of oversampling. Capacitor ratio C_3 / C_4 can be less than 1 / 2 since the next stage is a one bit quantizer, as was discussed in 3.3.2. C_3 and C_4 were set to 50 fF and 200 fF respectively giving a ratio of 1 / 4.

4.4.2 Switches

Switch design is critical in a low voltage switch-C circuit. Both switch impedance and channel charge injection are non-linear functions of the input signal and thus can cause harmonic distortion in the modulator output.

To reduce the impedance of the switch its size should be increased but large switches cause serious problems for a single-ended design: their parasitic capacitances increase leading to charge injection problems and power supply noise coupling. Figure 23 shows the coupling mechanism where C_{in} and C_{out} are source/drain parasitic capacitors plus the capacitance of the circuitry attached to the switch.

FIGURE 23.

An nMOS switch with sources of error waiting to be injected into the system.

Here supply noise from the clock couples directly to the signal path and thus small switches must be used to reduce the coupling mechanism. Small devices also reduce the amount of channel charge (Q_{ch}) that will be injected into the circuit. These unwanted contributors to V_{OUT} are grouped together as $V_{FeedThrough}$ in EQ. 14.

$$V_{FeedThrough} = \frac{C_{overlap}}{C_{overlap} + C_{out}} V_{clk} + \frac{0.5 Q_{ch}}{C_{overlap} + C_{out}} \quad (EQ\ 14)$$

The first term in EQ. 14 is a voltage divided V_{clk} , so $C_{overlap}$ should be small in relation to C_{out} , to minimize clock feed through, and power supply noise. When the switch turns off channel charge travels via the path of lowest impedance. The second term of EQ. 14 implies that $C_{in} = C_{out}$ and $V_{in} = V_{out}$.

The input switch of Figure 20, pg. 42, of the delaying integrator is floating and must be able to accommodate full, rail-to-rail swing. To accomplish this it is implemented with a transmission gate. The effect of charge injected by this switch is reduced here by using bottom plate sampling [15]. Opening switches $\Phi1'$ and $\Phi2'$ before $\Phi1$ and $\Phi2$, (see Figure 21, pg. 43), makes the sampling capacitor high impedance to the signal dependent charge of the floating switch. Most of the charge flows toward the input of the switch.

All other switches have one terminal at a fixed potential or analog ground, and so, CMOS transmission gates are not needed. The charge injected from these switches is constant, (that is, not signal dependent), from one sample to the next and thus will only worsen the $\Delta\Sigma$ modulators DC performance.

At low supply voltages it is difficult to build a transmission gate with adequate conductance over the desired signal amplitude range. Much research has been presented to solve this problem [22]

[28] [29]. Here, the floating switch limits our supply voltage to 1.2 V. Simulation data below shows the transmission gate's conductance when using minimum sized devices.

FIGURE 24.

Transmission gate impedance over an input voltage ranging from 0 V to 1.2 V for $V_{dd} = 1$ V (on the left) and $V_{dd} = 1.2$ V (on the right).

Having 50 ns to settle to 7τ accuracy (0.1% ~ 10 bits) with 200 fF input capacitance requires that the worst case switch resistance be ~ 35 k Ω . Hence, greater than two times the minimum size devices are used at the input to ensure proper settling.

4.4.3 Operational Transconductance Amplifier (OTA)

The amplifier used is a low voltage OTA based on wide swing folded cascode with a slight change in the feedback, (Figure 25). The current mirror load is around the common gate cascode transistor. The circuit works in a similar manner to that of the typical folded cascode but with lower input impedance for the input differential pair which results in a wider unity gain bandwidth.

Low voltage, wide swing, folded cascode OTA with feedback around the input pair's input node.

R_L is the output impedance of the cascoded current source load of M_3 and M_4 :

$$R_L = ro_4 + (gm_3 \cdot ro_4 + 1) \cdot ro_3 \approx gm \cdot ro^2 \quad (\text{EQ 15})$$

G_{in} is the input conductance seen by i_{ac} :

$$G_{in} = gm_2 \cdot A + gm_1 + \frac{1}{ro_2} + \frac{1}{ro_1}(1-A) \quad (\text{EQ 16})$$

$$A = \left(gm_1 + \frac{1}{ro_1} \right) \left(\frac{R_L \cdot ro_1}{R_L + ro_1} \right) \approx gm \cdot ro \quad (\text{EQ 17})$$

substituting the approximation for A into EQ. 16:

$$G_{in} = gm \cdot (gm \cdot ro + 1) \quad (\text{EQ 18})$$

The bias currents I and I_B , in Figure 25, pg. 49, were set to $10\ \mu\text{A}$ and $16\ \mu\text{A}$ respectively so that slew limited settling would occupy 25 ns, or one half of the total settling time as outlined previously, (See “Capacitor Sizing” on page 45.). The rest of the settling time is dedicated to exponential settling.

The OTA must settle to within 0.1% (or ~ 10 bit accuracy) of its final value within 25 ns (the rest of the settling time). This sets the time constant:

$$7\tau = 25\text{ ns} \text{ or } \tau = 3.5\text{ ns} \quad (\text{EQ 19})$$

This time constant is related to the g_m of the OTA by:

$$\tau = \frac{C_{load}}{g_{m,ota}} \cdot \frac{C2 + C1}{C2} \quad (\text{EQ 20})$$

$$\frac{g_{m,ota}}{2} = g_{m,m10} = g_{m,m11} \quad (\text{EQ 21})$$

The g_m of the input transistors (M10 & M11) is set to over $30\ \mu\text{S}$ for proper linear settling. The input pair is over designed to have a $g_m = 180\ \mu\text{S}$ for the bias conditions stated above. A transient simulation of OTA's step response in closed loop configuration is given below. It settles to 0.1% accuracy within 30 ns for nominal temperature and process. It is assumed that this is enough mar-

gin to ensure adequate settling over process and temperature variation. However, the modeling accuracy of devices in subthreshold is somewhat questionable.

FIGURE 26. Step response of the OTA in closed loop configuration showing settling to 0.1% accuracy in 30 ns.

All transistors are sized for operation in subthreshold. A table of W/L values is given below.

TABLE 1. Transistor sizes and number of fingers used for the low voltage OTA.

Transistor Number	W/L ($\mu\text{m}/\mu\text{m}$)	Transistor Number	W/L ($\mu\text{m}/\mu\text{m}$)
M1	5 x (2 / 0.35)	M7	5 x (6 / 0.35)
M2	4 x (6 / 0.75)	M8	5 x (6 / 0.35)
M3	5 x (6 / 0.35)	M9	12 x (3 / 0.25)
M4	5 x (6 / 0.35)	M10	5 x (6 / 0.25)
M5	5 x (2 / 0.35)	M11	5 x (6 / 0.25)
M6	4 x (6 / 0.75)		

The input swing is not critical for switch-C design since voltages at the amplifier input are small and centered around analog ground. Operating the transistors in subthreshold helps with maximiz-

ing the output swing. The V_{ds} required to keep a transistor in saturation is only ~ 50 mV compared to approximately 150 mV for a device in strong inversion. This means that the wide-swing folded cascode can obtain a higher output swing before clipping. Figure 27 shows a simulation of V_{out} for an input ramp.

FIGURE 27. Transient response showing the OTA's output voltage range

MOSFETs biased in subthreshold also exhibit a higher output impedance. This helps to increase the DC gain of the OTA. Simulation shows over 50 dB DC gain with a unity gain bandwidth of 90

MHz. Figure 28 shows phase margin is 60° with the addition of a 100 fF compensation capacitor at the output of the amplifier.

FIGURE 28. Bode plot of OTA in open-loop configuration

Rules of thumb for OTAs to be used in $\Delta\Sigma$ modulators are that the combined DC gain of the stages (in this case two stages), must be on the order of the OSR for adequate noise shaping and the unity gain bandwidth should be 5 times the sampling rate for proper settling [28]. These are both met here.

4.4.4 Bias circuitry

Each OTA has its own bias circuitry. OTA 1 can run at higher power for better settling and noise performance than the less critical OTA 2. See Figure 34, pg. 59 for the overall layout of the modulator.

The circuitry is shown in Figure 29, pg. 54. Bias transistors have a size ratio of 1:1 with the OTA's transistors that they bias. The current through transistor P1 is tunable through an off chip potentiometer. It sets the bias current for the OTA1 of the modulator. Another identical circuit is used for OTA2.

Each column level $\Delta\Sigma$ modulator has its own set of bias circuits with a common biasing node that is set off chip. This helps with matching and reduces noise coupled from one modulator to the next, in the array.

FIGURE 29.

OTA bias circuitry

4.4.5 Low-Voltage Comparator

The comparator is not a critical circuit in single bit $\Delta\Sigma$ modulators. Mismatch between input transistors is seen as a DC offset that is corrected by the gain of the loop. The modulator performance is also relatively insensitive to hysteresis in the comparator [28]. The low supply voltage reduces the number of transistors that can be stacked. The comparator design is shown in Figure 30. It is made up of a differential pfet input stage that loads a regenerative cross coupled nfet amplifier.

Nfet pull downs are used to reset the cross-coupled nfet latch. The differential output drives a set-

FIGURE 30. Low voltage comparator with Set-Reset latch.

reset latch. The output of this set-reset latch (data) is held during reset ($\sim \Phi1_end = 1$).

The main design requirement is that nodes x and $\sim x$ are pulled low during reset, and that power dissipated is not high. With the reference input (in_m) at a potential of 0.6 V and $V_{DD} = 1.2$ V, the load transistor P2 is a high impedance that limits current flow from its source to be approximately 20 μA . The comparator burns the most power when data is 0. In this state, in_p has dropped below 0.6 V. P1 has a maximum source current of 200 μA upon reset. The reset transistors (with drain connected to node x and $\sim x$), must be the same size to balance parasitics and be able provide a proper reset. The ratio of the reset transistor to the pfet input (P1) must large enough that the voltage at output x is low even when P1 is turned on fully, otherwise the latch would exhibit hysteresis.

4.4.6 Switch Select

The loop feedback DAC, (refer to Figure 6, pg. 24, and Figure 21, pg. 43) is achieved by selecting a reference voltage to “switch in” during $\Phi2$. This will subtract the appropriate feedback voltage

from the input sampled on $\Phi 1$. Switch selection is a digital operation based on the output from the comparator. The digital circuitry is shown below:

FIGURE 31.

Switch select DAC

4.4.7 Two Phase Non-Overlapping Clock

It is important that both sets of switches not be on during the cross-over between phases -- otherwise charge will be lost. The circuit below, in Figure 32, ensures a non-overlapping clock. It generates the advanced versions of the clocks $\Phi 1'$ and $\Phi 2'$. The delayed version of $\Phi 1$ is obtained with the same gate delays as the switch select circuit of the previous sub-section.

FIGURE 32. Two phase Non-Overlapping clock generator and time delay logic

4.4.8 $\Delta\Sigma$ Modulator Simulation

Matlab was used to simulate the overall expected performance of the modulator. Input noise and finite DC gain have been included in the functional level model of the circuit to observe their effect on the overall performance of the circuit.

A power spectral density (PSD) based on a Hann windowed FFT with mean squared power is used to calculate signal-to-noise ratio. Noise is summed to 312.5 kHz, 156.25 kHz and 78.125 kHz corresponding to oversampling ratios of 16, 32, and 64 respectively. 2^{17} output bits are used for the FFT and thus each bin of the FFT corresponds to a bandwidth of 76.29 Hz. The first two points of the PSD are ignored in the noise calculation because of their high DC power content.

Through spectral analysis, non-shaped quantization noise and circuit input noise can be seen to limit the modeled modulator's performance. That is, quantization noise at low frequencies is not shaped to zero. This is caused by the finite DC gain of the OTAs (causing integrator leakage) and

the input referred noise of the first integrator in the loop. These will limit the achievable SNR of the $\Delta\Sigma$ modulator and thus will limit the accuracy of the ADC.

The PSD of the simulated modulator is plotted below.

FIGURE 33.

Power spectral density of 2^{17} output bits for the $\Delta\Sigma$ modulator modeled and simulated in MATLAB.

4.4.9 $\Delta\Sigma$ Modulator Layout

Layout must be carefully considered in switch-C design, especially when single-ended implementations are used. Switches and digital circuitry are known to inject noise into the substrate and into the supply line. The careful placement of circuit blocks can reduce the adverse affects of this.

To isolate power supply noise all of the digital circuitry is powered from dedicated V_{SS} and V_{DD} rails which are brought out to their own pins. This is done so that noise will not couple via the

power supplies to the sensitive analog circuitry. The switches will couple any power-supply noise into the critical nodes of the circuit. The circuitry driving the switches is connected to dedicated “quiet” V_{SS} and V_{DD} lines.

Many analog and digital supply rails and pins are used to reduce bond wire inductance in an effort to reduce the impedance to high frequency noise.

All of the digital circuitry is localized to a point far away from the more sensitive analog circuitry. This is illustrated in the block diagram of Figure 34. Most of the charge injected into the substrate by the digital circuitry will be picked up by substrate contacts surrounding the digital blocks. Substrate contacts fully surround all critical circuitry as well. By increasing the distance of the digital blocks from the analog blocks we are reducing the likelihood of stray charge being picked up by critical nodes. Once again, noise injected into the second stage integrator has little effect on the modulator’s performance.

FIGURE 34.

Block diagram illustrating the floor plan and relative sizes of the circuit components used in the $\Delta\Sigma$ modulator.

The output and input buffers are located far away from the rest of the circuitry and also have their own V_{DD} and V_{SS} rails.

4.5 Test Chip Microphotograph

The relative sizes of the circuit blocks can be seen in the micrograph of the test chip shown in Figure 35 below:

FIGURE 35.

Test chip
implemented in TSMC 0.18 μm CMOS.

4.6 **Column Power Consumption**

A table listing the quiescent current drawn per column is given below:

TABLE 2.

Quiescent current drawn and power dissipation for nominal process, $V_{dd} = 1.2\text{ V}$, and $T = 27\text{ }^{\circ}\text{C}$.

Circuit	Current	Power
Pixel Source follower	$10\text{ }\mu\text{A}$	$12\text{ }\mu\text{W}$
OTA 1	$36\text{ }\mu\text{A}$	$43\text{ }\mu\text{W}$
OTA 2	$36\text{ }\mu\text{A}$	$43\text{ }\mu\text{W}$
Bias 1	$50\text{ }\mu\text{A}$	$60\text{ }\mu\text{W}$
Bias 2	$50\text{ }\mu\text{A}$	$60\text{ }\mu\text{W}$
Comparator	$\sim 110\text{ }\mu\text{A}$	$\sim 132\text{ }\mu\text{W}$
Total	$\sim 300\text{ }\mu\text{A}$	$\sim 360\text{ }\mu\text{W}$

Using the values given in Table 2, a full sized array with 1000 modulators would dissipate 360 mW quiescent of power.

4.7 **Chapter Summary**

A 4×4 imager test array has been designed for 1.2 V supply operation using TSMC's $0.18\text{ }\mu\text{m}$ digital CMOS process. The pixel array was laid out such that it had a fill-factor of 40% and a column pitch of $15\text{ }\mu\text{m}$. Row timing was set to limit the amount of charge sharing incurred with the column line during read out, and dynamic range was maximized. Bootstrapping of the reset transistor was also necessary. The $\Delta\Sigma$ modulator was designed to fit within the column pitch. Transistors were biased in the subthreshold regime to keep power consumption low and make low voltage operation possible. Capacitors were made by interdigitated routing metal. 25 fF capacitance was achieved for a $5\text{ }\mu\text{m} \times 5\text{ }\mu\text{m}$ unit cell. Simulations showed that the modulator would be capable of 11.5 bit performance.

CHAPTER 5.0 Digital Signal Processing: Pixel Slew Rate Calculation

The decimation scheme used here is based on a multirate filtering architecture. The first stage is a comb filter selected because of its easy implementation and relatively low device count. This stage will reduce the 1024 one bit samples from the modulator at the 10 MHz sampling rate to 16 high resolution samples at a 156.25 kHz sampling rate. Conversely, if pixel saturation should occur, the time to saturation will be output. The final stage in the decimation calculates the pixel's slew rate over the integration period.

Attention here is focused on the implementation of the first stage of the decimation filter. This stage would eventually have to be implemented on the same chip as the pixel-array and column-level modulators to reduce the bandwidth requirements of data going off chip. The slope calculation could be done on a separate image processor chip.

Here again, design choices are made to reduce circuit size, such that it could be implemented monolithically with the focal array and the modulators. The Matlab design is presented next.

5.1 Comb Filter Decimation

To implement an oversampling imager, output pins would have to be shared to bus data off chip. This would require column level multiplexing. The sample rate of the data must be reduced to keep clock rates low. This is done in the first stage of the multi-rate decimation filtering. Comb (sinc) filters are used in multirate decimation filtering because they are easy to implement at high sampling rates -- no multipliers are needed [15] [30]. The filter structure is shown in Figure 36.

This averaging filter has a magnitude response that resembles $\sin x/x$. Its transfer function has 64 zeros distributed around the unit circle with one at DC ($1 < 0^\circ$) which is cancelled by a pole. The lowpass frequency response shown in Figure 38.

FIGURE 36. A block diagram of a first order sinc decimation filter with sampling rate change factor 64.

Doubling the number of stages gives what is known as a second order sinc filter. It has 64 second-order zeros around the unit circle, and one at DC which is cancelled by a second-order pole.

FIGURE 37. A block diagram of a second order sinc decimation filter with sampling rate change factor 64

The frequency and phase response of both the sinc and second order sinc filter are given below.

FIGURE 38. Phase and magnitude response of the Sinc (left) and Sinc² (right) decimation filters.

The power spectral density plots in Figure 39, pg. 65, show the result of passing 2^{17} output bits from a second order modulator, with frequency spectrum corresponding to that of Figure 33, pg. 58, through the two filters.

Here it can be seen that the high frequency noise is not sufficiently attenuated by the first order sinc filter. Only 29 dB SNR is achieved, which is 33 dB lower than that achievable through brick-

wall decimation. The second order sinc filter achieves 58.5 dB SNR in the 78.125 kHz band, which is much closer to optimal.

FIGURE 39. PSD of $\Delta\Sigma$ data passed through the first order sinc (left) and the second order sinc (right).

A 5 dB increase in SNR is achieved by going from a second order sinc filter to a third order filter, for this modulator. This, however, requires two additional registers, (that is, the z^{-1} blocks in Figure 36 and Figure 37, pg. 63), as well as two additional summation blocks. As will be seen in the next subsection going to a third order sinc also increases the number of bits required per register. The cost in gate count is significant.

5.2 Sinc Filter Implementation:

The registers needed for the filter can be of reasonable size if two's complement arithmetic is used. Here, register size must be such that overflow can only occur once during the decimation interval. A simple equation from [30] is used to calculate the number of bits required:

$$n_{bits} = 1 + N_{order} \times \log_2\left(\frac{1}{r_{change}}\right) \quad (\text{EQ 22})$$

This equation makes intuitive sense as well:

log₂(64) is the number of bits required to count up to the worst case (all ones) input within the decimation period. This number is multiplied by the latency of the filter and one bit is added for the two's complement sign bit.

The number of bits needed per register is 13 for the second order filter. EQ. 22 shows that going to a third order sinc filter would require 62 more flip-flops (per filter) than the required 52 flip-flops for the second order sinc filter. Since minimizing chip area is of great importance, the second order sinc filter is selected for implementation.

5.3 Saturation Detection

Saturation detection circuits are often used in higher order $\Delta\Sigma$ modulators to reset the loop filter should saturation occur [15]. These circuits look for long strings of 1,1,1,1,1 or 0,0,0,0,0 which indicate that the loop has become unstable.

Here, pixel saturation will drive the modulator out of bounds and cause the loop to become unstable. When this happens the modulator will output all zeros. A slope estimate can be made based on saturation time of the pixel.

Ten zeros in a row indicates that the pixel is sufficiently close to saturation. A 4-bit counter is used to count successive zeros, it is reset if the input is 1. The saturation time can be calculated based on non-saturated decimation intervals and the time within which a decimation interval saturation occurs. A 6-bit incrementer is needed to keep track of the time within on integration period. It is clocked at the same rate as the $\Delta\Sigma$ modulator. Upon saturation, it is stopped, held, and multi-

plexed out on the next decimated sample time. Refer to Figure 13, pg. 33 for the system level view.

5.4 Digital Decimation Power Estimation

$$P = \frac{C_{gate} \cdot V_{DD}^2 \cdot F}{2} \quad (EQ 23)$$

where P is the power needed to charge one digital gate with input capacitance C_{gate} once per clock period $1/F$. For a minimum sized device $C_{gate} \sim 10$ fF. Assuming in the worst case, all gates flip once per clock period and $F = 10$ MHz. A full scale array of 1000 columns might use a total of 500 000 gates (500 gates per column). This would dissipate 36 mW of power in total, according to EQ 23.

The benefit of using digital filtering in a submicron process is evident when comparing this to the quiescent power consumption estimated for the modulator, on pg. 61. The decimation filters burn 10 % of the power of the analog modulators.

5.5 Slope Calculation

The slope for the “line of best fit” of a non-saturating pixel is found with the following equations:

$$Slope = \frac{SS_{XY}}{SS_{XX}} \quad (EQ 24)$$

$$SS_{XY} = \sum_{i=1}^n x_i y_i - \frac{\left[\sum_{i=1}^n x_i \right] \left[\sum_{i=1}^n y_i \right]}{n} \quad (EQ 25)$$

$$SS_{XX} = \sum_{i=1}^n x_i^2 - \frac{\left[\sum_{i=1}^n x_i \right]^2}{n} \quad (\text{EQ 26})$$

EQ. 24, EQ. 25 and EQ. 26 are regression operations based on a least mean squares estimate of a line calculated with a number (n) of data samples. These equations are taken from [31] and Matlab is used to make the calculation. A plot of a line of best fit from a system level simulation is shown below.

FIGURE 40.

Plot showing the least means squares estimate of the line of best fit matched to the 15 valid output samples from the Sinc^2 filter.

The least mean squares method of calculating slope further filters noise from the 15 valid samples obtained from the second order sinc filter. Thus, it further increases the resolution of the conversion process.

The slope calculation for saturating pixels is found simply by means of rise/run. For this the initial precharge value of the average pixel must be known. Offset from pixel to pixel will affect the

accuracy of the calculation, however, since this method is measuring pixel slew-rates above 6000 V/s the offset causes a relatively small error.

5.6 Chapter Summary

This chapter shows, by way of simulation, that the noise attenuation capabilities of a second-order sinc filter far exceed that of a first-order sinc filter for specific application of decimation filtering of a second order modulator's output. Although a third-order sinc filter may provide more out-of-band noise attenuation, it also requires 114 flip-flops per filter. The second order filter, which requires only 52 flip-flops, is chosen for this application. An algorithm for the overall pixel slew rate calculation based on a least mean squares regression technique is also given. Simulation data for the over-all system is presented.

CHAPTER 6.0 Experimental Test Results

Components of the test chip were tested individually for the purpose of characterization. Since the imager array was only 4 x 4 pixels taking an image is not possible. Limited imager type testing, (such as, test for fixed pattern noise, and column-to-column mismatch), could be performed.

6.1 Measured Pixel Dark Leakage

The dark leakage was measured to be in the 100 mV/sec range -- this corresponds to that reported in [24]. The output captured from the Tektronix TDS 684B digitizing oscilloscope is shown in Figure 41 below.

FIGURE 41.

Measured dark pixel output voltage for a 1 second integration time

Here two cycles of a complete read out are given. The sampling clock has been slowed down from 10 MHz to 1 kHz and with 1024 samples per row, the time recorded for each row is 1.024 sec. Here it can be seen that reset brings the pixel output to ~ 550 mV. Also Row2 for this test column has a stuck at 1 fault. Row 4 is a leaky pixel having twice the slew rate of Row1 and Row3.

No stuck at faults were observed for pixels in the 4x4 array.

6.2 Modulator Results

The modulator was tested with a 1.2 V supply at the intended sampling rate of 10 MHz. A Rhode & Schwarz Dual Arbitrary Waveform Generator was used to generate an input tone with frequency of $20 \cdot (10 / 2^{14}) \text{ MHz}$ and offset 616 mV. This input frequency was chosen so that harmonic distortion up to 6th order could be observed in the 78125 Hz bandwidth, corresponding to $\text{OSR} = 64$. Analog ground was set to 480 mV and the current measured in each of the OTA bias resistors was 10 μA . The DAC feedback levels were 1.2 V and 0 V.

A Hewlett Packard 16500C Logic Analysis System was used to capture 2^{14} output bits for a Fast Fourier Transform. A power spectral density based on a Hann windowed FFT with mean squared power is used to calculate Signal to Noise plus Distortion Ratio (SNDR). Noise and distortion is integrated over a bandwidth from 0 to 312.5 kHz, 156.25 kHz and 78.125 kHz corresponding to an OSR of 16, 32, and 64 respectively. The first two points of the PSD are ignored in the noise calculation because of their high DC power content.

The noise shaping characteristic of the loop filter is clearly evident in the PSD. On the right is the corresponding bitstream passed through a 5th order Butterworth lowpass filter, with passband edge at 78125 Hz. The filtered time domain output shows approximately 1 mV peak to peak,

Experimental Test Results

which corresponds to the signal's mean squared power of -69 dB measured in the power spectral density. SNDR is calculated to be 9.1 dB.

FIGURE 42.

PSD of 2^{14} output bits (left) for a near maximum amplitude sinusoidal input. The time domain signal resulting from filtering the output bits with a 5th Order Butterworth LPF with pass band edge at 78.125 kHz is on the right.

In-band modulator noise is clearly present when looking at the filtered time domain output. The input signal amplitude is almost at the modulator's lower limit of performance.

Experimental Test Results

The 3rd and 5th order harmonics begin to gain power as the input signal increases in amplitude. Here SNDR is 50.1 dB over a 78.125 kHz bandwidth.

FIGURE 43.

PSD of 2^{14} output bits (left) for a near maximum amplitude sinusoidal input. The time domain signal resulting from filtering the output bits with a 5th Order Butterworth LPF with pass band edge at 78.125 kHz is on the right.

50.1 dB is the modulator's peak signal to noise+distortion ratio, see Figure 46. This corresponds to approximately 8-bits, meaning that the modulator's linearity is roughly that of an 8-bit ADC.

Harmonic distortion dominates the modulator output for input signals greater than 300 mV peak to peak.

Experimental Test Results

Next the modulator is close to being overdriven. The 2nd, 3rd and 4th harmonics are visible in the output spectrum. Noise shaping is starting to degrade and SNDR = 30.3 dB in the 78.125 kHz band.

FIGURE 44.

PSD of 2¹⁴ output bits (left) for a near maximum amplitude sinusoidal input. The time domain signal resulting from filtering the output bits with a 5th Order Butterworth LPF with pass band edge at 78.125 kHz is on the right.

Experimental Test Results

A plot of SNDR for increasing input tone amplitude shows the linearity characteristic of this modulator. Harmonic distortion causes the peak SNDR to be limited to 50 dB. Dynamic range of the modulator is over 70 dB for a 78.125 kHz bandwidth.

FIGURE 46.

Signal to noise plus distortion ratio plotted over increasing signal amplitude

Dynamic range found in dB for an input sinusoid can be converted to dynamic range in bits by using [15]:

$$DR(bits) = \frac{DR(dB) - 1.75}{6.02} \quad (EQ\ 27)$$

So the modulator is capable of achieving 11.5 bits in a 78.125 kHz bandwidth with brickwall decimation filtering.

6.3 Modulator, Decimation, and Slope Calculation Results

Input ramps were next fed into the modulator. The output bitstream was processed with the second order sinc filter and saturation time detection algorithm. The digital value of slope was then calculated based on a least mean squares or rise/run algorithm. This was done to characterize the overall analog-to-digital conversion technique. A plot of the digitized slope calculation against the input slew rate is given below.

FIGURE 47. Linearity and dynamic range plot of the conversion technique.

The conversion processing is seen to be linear for approximately five orders of magnitude. The converter is unable to resolve slew-rates below 2 V/s or slew rates above 100 000 V/s accurately. A gain error is observed for the two methods of calculating slope (i.e., least mean squares and rise over run). This causes a discontinuity in the transfer function of the analog-to-digital conversion. A gain error of approximately 3 is observed for the non-saturating pixel and a gain error of 4 for a saturating pixel.

This gain error will not adversely affect the image quality, in that it only affects the white balance of the image.

6.3.1 The Lower Limit of Dynamic Range and Pixel Sensitivity

Dark current leakage sets the minimum value of slew rate (proportional to light intensity) that can be observed in an imager. Section 6.1 on page 70, has shown that the dark leakage for these pixels is in the 100 mV/s range (with significant variance). Measurements below one order of magnitude above this limit would also be in error due to this variance. Thus, the analog-to-digital conversion process here is limited by the sensitivity of the pixel, and not by the shortened integration period.

6.3.2 The Sources of Gain error

Matlab simulations have shown that the gain error seen in Figure 47 is dependent on the finite DC gain of the integrators used to construct the LPF of the $\Delta\Sigma$ modulator, (refer to Figure 10, pg. 29 and Figure 21, pg. 43).

Finite DC gain in the integrators is known to cause non-shaped quantization noise in the spectrum of the output bitstream of the $\Delta\Sigma$ modulators [15]. Also, most of the analysis in the literature, and that presented in Section 2.6 on page 23, assume that the quantization noise is not correlated to the input. For this to be an accurate assumption the input signal must be spectrally rich, or busy [15]. This is not the case for a slowly varying input ramp.

It is believed that the quantization noise is correlated to the input of the modulator. That is, integrator leakage is contributing to the slew rate of the input and causing an overall gain error. A redesign of the OTA's for higher gain and the introduction of a dither signal to the modulator could be used to randomize the quantization noise and reduce the gain error observed in conversion.

6.4 Exposure to Light and Column-to-Column Mismatch

The test array was exposed to light. The light source was a tungsten-halogen flood lamp. The distance from the bulb to the test array was varied to vary the incident light power density while maintaining a constant output spectrum. An off chip PIN (p-doped, intrinsic, n-doped) silicon photodiode was used to measure relative light levels incident on the array. By measuring the short circuit photocurrent produced by the photodiode with a digital ammeter, the dynamic range of the imager could be estimated.

With incident light levels just below those detectable above the dark leakage floor of the pixel array, corresponding to 1 - 6 V/s pixel output slew, the PIN photodiode recorded a current of 0.5 ~ 1 μ m. At the onset of pixel saturation, the PIN photodiode gave a current of 1 ~ 2 mA. The incident light intensity could be increased by only one more order of magnitude past this point, which was not sufficient to produce system saturation. From the ADC system level characterization plot of Figure 47, it is projected that two orders beyond saturation could be imaged.

To get a true feeling for how well the imager is imaging, the column-to-column mismatch is observed for various light intensities. Bar graphs are plotted which show all four column outputs grouped together for each of the four row outputs. These are given below:

FIGURE 48.

Column output below the dark current and ADC threshold

FIGURE 49.

Column outputs for Non-Saturating input light intensities.

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FIGURE 50.

Column outputs for saturating input light intensities.

6.4.1 Discussion

The lower limit in dynamic range is clearly evident in Figure 48. Here pixel dark current and modulator quantization noise dominate the imager read out. Mismatch is at least 50% between converted pixel light intensities.

Throughout testing Column 4 was observed to be brighter than the rest. DC gain mismatch in the integrators $\Delta\Sigma$ modulators, from one column to the next, could result in a brighter column due to correlated quantization noise. This will contribute to column level fixed pattern noise. The average row level mismatch does not look as systematic.

To fully evaluate the ADC process a full array ($> 100\,000$ pixels) would have to be fabricated and calibrated measurements would have to be taken. The test measurements presented here give some insight into the problems that would occur in a full array.

CHAPTER 7.0 Conclusions and Recommendations

7.1 Conclusions

A CMOS active pixel sensor imaging array has been designed for 1.2 V operation in TSMC 0.18 μm , 1P6M, digital CMOS technology. The imager employs second-order, delta-sigma, modulators along with a digital signal processing technique to achieve wide dynamic range for this low value of supply voltage. Oversampling of the pixel output reduces white noise fold-over, and allows the time of saturation to be detected and recorded for pixels exposed to high light levels. The reduction of noise fold-over increases the signal-to-noise ratio of the digitally converted pixel output such that even low levels of illumination can be captured for short integration periods. Monitoring for saturation time expands the capability of this imager to capture illumination information at very high levels.

A working prototype 4x4 array was fabricated and successfully tested for operation with a 10 MHz clock, corresponding to a frame rate of 10 s^{-1} in a full scale 1000 x 1000 array. The prototype was found to be capable of measuring light levels varying by a factor of 1,000 between the noise floor and pixel saturation. Using the saturation detection scheme, the measurable light level can be increased by an additional factor of 100, providing a total dynamic range in input light level of 100,000.

A gain error of 3, caused by systematic quantization noise, was observed when characterizing the analog-to-digital conversion technique's response to input ramps of varying slew rate. Column output levels were observed to vary by approximately 5% of the mean value, over the usable input light range. This column level mismatch was also systematic resulting in a "bright" column. A possible cure for this fixed pattern noise is to introduce a dither signal to the delta sigma modulator input such that quantization noise is randomized.

7.2 Recommendations

A full 1M array would have to be fabricated to and tested to see how well the presented analog-to-digital conversion method will perform within a state of the art, low voltage, wide dynamic range, CMOS imager. Fixed pattern noise and integration uniformity could then be measured.

The entire DSP algorithm would have to be implemented in hardware with at least the first stage of decimation on the same chip as the focal array. Total power consumption with the increased digital complexity could be measured. System issues, such as data through-put and memory, requirements could only then be addressed.

It is anticipated that supply and substrate noise from the large digital portion would require that the $\Delta\Sigma$ would have to be implemented in a fully differential architecture.

Temperature compensated bias circuitry would have to be designed on chip to ensure that the devices biased in subthreshold remain in the correct region of operation over the range of all operating temperatures (e.g. -40 °C to 110 °C).

It is probable that a dithering signal would have to be introduced to the input of the modulator, such that systematic quantization noise be reduced.

References:

- [1] A Survey of CMOS Imager Systems, DALSA Internal Report, 1997.
- [2] John C. Russ, "**The Image Processing Handbook**", 2nd edition, IEEE Press, 1995.
- [3] D. Scheffer, B. Dierickx, G. Meynants, "**Random addressable 2048 × 2048 active pixel image sensor**", IEEE Transactions on Electron Devices, v 44 n, 10 Oct, 1997, IEEE, p 1716-1720.
- [4] O.Yadid-Pecht, E.R. Fossum, "**Wide intrascene dynamic range CMOS APS using dual sampling**", IEEE Transactions on Electron Devices, v 44, n 10, Oct 1997 IEEE, p 1721-1723.
- [5] S. Decker, R. McGrath, K. Brehmer, C. Sodini, "**256×256 CMOS imaging array with wide dynamic range pixels and column-parallel digital output**", Digest of Technical Papers - IEEE International Solid-State Circuits Conference, Feb 5-7, 1998.
- [6] Oh-Bong Kwon; Ki-Nam Park; Do-Young Lee, et. al., "**A novel double slope analog-to-digital converter for a high-quality 640 x 480 CMOS imaging system**", ICVC '99. 6th International Conference on VLSI and CAD, p 335 - 338, 26-27 Oct. 1999.
- [7] Yu-Chuan Shih, Chung-Yu Wu, "**The design of high-performance 128 x 128 CMOS image sensors using new current-readout techniques**", ISCAS '99. Proceedings of the 1999, IEEE International Symposium on Circuits and Systems, p 168 - 171 vol.5, 30 May-2 June 1999.
- [8] D.X.D. Yang, A.E. Gamal, B. Fowler, H. Tian, "**A 640 x 512 CMOS image sensor with ultrawide dynamic range floating-point pixel-level ADC**", IEEE Journal of Solid-State Circuits, p 1821 - 1834, Dec. 1999.
- [9] L.G. Mellrath, "**A low power, low noise, ultra-wide dynamic range CMOS imager with pixel-parallel A/D conversion**", Digest of Technical Papers -- IEEE Symposium on VLSI Circuits, p 24 - 27, June 2000.

-
- [10] C.C. Enz, G.C. Temes, “**Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization**”, Proceedings of the IEEE, p 1584 - 1614, November 1996.
- [11] Hui Tian, Boyd Fowler, Abbas El Gamal, “**Analysis of temporal noise in CMOS APS**”, Proceedings of SPIE - The International Society for Optical Engineering, v 3649, p 177-185, Jan 25-26, 1999.
- [12] Kalwant Singh, “**Noise analysis of a fully integrated CMOS image sensor**”, Proceedings of SPIE - The International Society for Optical Engineering, v 3650, p 44-51, Jan 27- 28, 1999.
- [13] Yavuz Degerli, Francis Lavernhe, Pierre Magnan, Jean A. Farre, “**Analysis and Reduction of Signal Readout Circuitry Temporal Noise in CMOS Image Sensors for Low-Light Levels**”, IEEE Transactions on Electron Devices, v 47, n 5, May 2000 IEEE, p 949 - 962.
- [14] Justin Fortier, N.Garry Tarr, Ashok Swaminathan, Calvin Plett, “**1.2 V 0.18 μ m CMOS Imager with Column-Level Oversampling**”, Proceedings of the 27th European Solid-State Circuits Conference, p 132-135, 18 - 20 September, 2001.
- [15] David Johns, Ken Martin, “**Analog Integrated Circuit Design**”, John Wiley & Sons, Inc., Toronto, 1997.
- [16] Boyd Fowler, “**CMOS Area Image Sensors with Pixel Level A / D Conversion**”, Ph.D. Dissertation, Stanford University, October 1995.
- [17] Z. Zhou, B. Pain, E.R. Fossum, “**CMOS Active Pixel Sensor with On-Chip Successive Approximation Analog-To-Digital Converter**”, IEEE Transactions on Electron Devices, v 44, n 10, Oct 1997 IEEE, p 1759-1763.
- [18] B. Pain, G. Yang, M. Ortiz, et. al., “**Single-chip programmable digital CMOS imager with enhanced low-light detection capability**”, Proceedings of the IEEE International Conference on VLSI Design The 13th International Conference on VLSI Design, Jan 3-7, 2000.

-
- [19] Kwang-Bo Cho, Alexander Krymski, Eric R. Fossum, "**A 1.2 V Micropower CMOS Active Pixel Image Sensor for Portable Applications**", Digest of Technical Papers - IEEE International Solid-State Circuits Conference, Feb 7-9, 2000.
- [20] J. Nakamura, B. Pain, T. Nomoto, T. Nakamura, E.R. Fossum, "**On-Focal-Plane signal Processing for Current-Mode Active Pixel Sensors**", IEEE Transactions on Electron Devices, v 44, n 10, Oct 1997, p 1747-1758
- [21] S.K. Mendis, B. Pain, R.H. Nixon, E.R. Fossum, "Design of a Low-Light Image Sensor with On-Chip Sigma-Delta Analog-to-Digital Conversion", Proceedings of SPIE - The International Society for Optical Engineering, v 1900, p 31-39, 1993.
- [22] V. Peluso, P. Vancorenland, A.M. Marques, M.S.J Steyaert, "**A 900-mV low-Power Delta Sigma A / D Converter with 77-dB Dynamic Range**", IEEE Journal of Solid-State Circuits, p 1887 - 1897, Dec. 1998.
- [23] H.S. Wong, R.T. Chang, E. Crabbe, P. Agnello, "**CMOS Active Pixel Image Sensors Fabricated Using a 1.8V, 0.25 μ m CMOS Technology**", IEEE IEDM, p 35.5.1 - 35.5.4, 1996.
- [24] Chunyan Wang, "**Photosensor Implementation Using the 0.25 Micron Technology**", Internal Report, Department of Electrical and Computer Engineering, Concordia University, 1999.
- [25] D.X.D. Yang, H. Min, B. Fowler, A.E. Gamal, M. Beiley, K. Cham, "**Test Structures for Characterization and Comparative Analysis of CMOS Image Sensors**", Proceedings of SPIE - The International Society for Optical Engineering, v 2950, p 8-17, 1996
- [26] H. Samavati, A. Hajimiri, A.R. Shahani, G.N. Nasserbakht, T.H. Lee, "**Fractal Capacitors**", IEEE Journal of Solid-State Circuits, v 33, n 12, December 1998.
- [27] R. Aparico, A. Hajimiri, "**Capacity Limits and Matching Properties of Lateral Flux Integrated Capacitors**", Digest of Technical Papers - IEEE Custom Integrated Circuits Conference, p 365 - 368, May 2001.

-
- [28] Seyfi Bazarjani, “**Mixed Analog-Digital Design Considerations in Deep Submicron CMOS Technologies**”, Ph.D. Dissertation, Carleton University, July 1996.
- [29] M. Keskin, U.K. Moon, G. Temes, “**A 1-V, 10-MHz Clock-Rate, 13-bit CMOS, Delta-Sigma Modulator Using Unity-Gain-Reset Opamps**”, Proceedings of the 27th European Solid-State Circuits Conference, p 532-535, September 2001.
- [30] E.B. Hogenauer, “**An Economical Class of Digital Filters for Decimation and Interpolation**”, IEEE Transactions on Acoustics, Speech, and Signal Processing, v assp-29, n 2, April 1981.
- [31] R.L. Scheaffer, J.T. McClave, “**Probability and Statistics for Engineers**”, Duxbury Press, Belmont, California, 1995.