High-Output Voltage Swing in Silicon Broadband Distributed Amplifiers

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Abstract

The various foundries are now producing CMOS, SiGe and BiCMOS technologies with device speeds that are comparable to some of the III-V technologies. Electro-optical modulators typically are driven with voltages in the range of a few volts to tens of volts, and recent research is producing silicon modulators that require voltages as low as one to two volts. Therefore, a silicon distributed amplifier could be used as a pre-driver, or driver, for the electro-optical modulator if it is able to achieve a minimum one to two volt peak-to-peak swings to drive a silicon electro-optical modulator.

The research is an exploration of techniques aimed at improving the large signal output performance of silicon distributed amplifiers for use in fibre optic communication systems. The experimental verification of these techniques involves the design and implementation of several distributed amplifiers in a standard readily available silicon process; ST Microelectronics BiCMOS9 process with eight metal layers and a minimum drawn length of 0.13 microns. A novel distributed amplifier topology has been designed that has artificial transmission lines composed of m-derived filter sections to increase the 3dB passband and a gain stage that increases the bandwidth over that which is available from a single device. The gain stage topology allows the designer to trade the extended bandwidth for the gain necessary to achieve a large output voltage swing. Three distributed amplifiers with bandwidths suitable for 40 gigabit per second data rates have been designed and fabricated and are as follows:

- A CMOS single-ended five-stage cascoded f_T doubler distributed amplifier producing better than 1V peak-to-peak output voltage swing.
- A HBT single-ended three-stage cascoded f_T doubler distributed amplifier producing better than 2V peak-to-peak output voltage swing.
- A HBT three-stage cascode differential to single-ended distributed amplifier producing better than 2V peak-to-peak output voltage swing.

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Table of Contents

Doctor of Philosophy	1
Abstract	ii
Acknowledgments	iii
Table of Contents	iv
List of Tables	vii
List of Figures	x
List of Symbols	xxi
Chapter 1: Introduction	1
1.1 Thesis Goals	2
1.2 Thesis Outline	5
Chapter 2: Distributed Amplifier Theory	6
2.1 Filter Sections	6
2.1.1 The Constant-k T Networks	7
2.1.2 The m-Derived T Section	10
2.1.3 The Bisected- π m-Derived Filter Section	16
2.1.4 Summary	17
2.2 Bandwidth	18
2.2.1 Gain-Bandwidth Product	18
2.2.2 Bandwidth and the Distributed Structure	20
2.2.3 Summary	23
2.3 Distributed Amplifier Theory	23
2.3.1 ABCD parameters	23
2.3.2 Image Parameters	25
2.3.3 Distributed Amplifier Analysis	27
2.4 Transistor Model	27

2.4.5	Artificial Transmission Lines	29
2.4.6	Gain.	30
2.4.7	Number of Stages	34
2.4.8	Maximum Gain Bandwidth Product.	34
2.4.9	Summary.	35
2.4	Literature Study and Figures of Merit	36
2.4.1	Recent Work in Distributed Amplification.	36
2.4.2	Figures of Merit	39
2.4.3	Distributed Amplifier Literature Summary	44
2.5	Summary.	47
Chapter 3: Device Breakdown and Linearity		49
3.1	Operation in the Breakdown Region of a Heterojunction Bipolar Transistor	49
3.1.1	The Common Emitter Breakdown Voltage	50
3.1.2	The Collector Base Breakdown Voltage	56
3.1.3	Summary.	58
3.2	Breakdown in MOSFET Transistors	59
3.2.1	Oxide Breakdown.	59
3.2.2	Punch Through	61
3.2.3	Avalanche Breakdown	61
3.2.4	Summary.	61
3.3	Device Speed and Linearity	63
3.3.1	Transit Frequency and the Maximum Frequency of Oscillation in a HBT	63
3.3.2	Linearity of the Bipolar Device	70
3.3.3	Transit Frequency and the Maximum Frequency of Oscillation in a MOSFET.	71
3.3.4	Linearity of the MOSFET Device	73
3.4	Summary.	74

Chapter 4: Distributed Amplifier Design.	76
4.1 Design Specifications	76
4.2 The Distributed Amplifier Topologies	77
4.2.1 CMOS MOSFET f_T Doubler	91
4.2.2 Topology of the CMOS Gain Stage	99
4.2.3 The HBT f_T Doubler Gain Stage.	104
4.2.4 The HBT Gain Stage.	107
4.2.5 The Artificial Transmission Line	112
4.3 The Distributed Amplifiers.	120
4.4 Summary.	142
Chapter 5: Experimental Results	144
5.1 Distributed Amplifier testing	144
5.2 The Measured Distributed Amplifier data	150
5.2.1 The CMOS single-ended five-stage cascoded f_T doubler distributed amplifier	151
5.2.2 The HBT single-ended three-stage cascoded f_T doubler distributed amplifier.	165
5.2.3 The HBT three-stage cascode differential to single-ended distributed amplifier.	180
5.3 Summary.	187
Chapter 6: Conclusions and Summary.	189
6.1 Thesis Summary and Conclusions	190
6.2 Thesis Contributions.	196
6.3 Future Work	198
References.	200

List of Tables

Table 2.1	Specifications of recent distributed amplifier publications.	37
Table 2.2	The gain bandwidth product and the modified gain bandwidth product for the publications presented in Table 2.1	44
Table 4.1	Summary for the simulated small signal S-parameters, group delay and power consumption of Figure 4.2 and Figure 4.3.	81
Table 4.2	Summary for the 11 Gbps simulated output eye of Figure 4.4.	81
Table 4.3	Summary for the 22 Gbps simulated output eye of Figure 4.5.	81
Table 4.4	Summary for the 40 Gbps simulated output eye of Figure 4.6.	82
Table 4.5	Summary for the simulated small signal S-parameters, group delay and power consumption of Figure 4.42 and Figure 4.43.	127
Table 4.6	Summary for the 11 Gbps simulated output eye of Figure 4.45.	127
Table 4.7	Summary for the 22 Gbps simulated output eye of Figure 4.46.	127
Table 4.8	Summary for the 40 Gbps simulated output eye of Figure 4.47.	127
Table 4.9	Summary for the simulated small signal S-parameters, group delay and power consumption of Figure 4.48 and Figure 4.49.	131
Table 4.10	Summary for the 11 Gbps simulated output eye of Figure 4.51.	131
Table 4.11	Summary for the 22 Gbps simulated output eye of Figure 4.52.	131
Table 4.12	Summary for the 40 Gbps simulated output eye of Figure 4.53.	131
Table 4.13	Summary for the simulated small signal S-parameters, group delay and power consumption of Figure 4.54 and Figure 4.55.	136
Table 4.14	Summary for the 11 Gbps simulated output eye of Figure 4.59.	136
Table 4.15	Summary for the 22 Gbps simulated output eye of Figure 4.60.	136
Table 4.16	Summary for the 40 Gbps simulated output eye of Figure 4.61.	136
Table 4.17	Summary for the 22 Gbps simulated output eye of Figure 4.62.	140
Table 4.18	Summary for the 40 Gbps simulated output eye of Figure 4.63.	140
Table 4.19	Summary for the 22 Gbps simulated output eye of Figure 4.64.	141
Table 4.20	Summary for the 40 Gbps simulated output eye of Figure 4.65.	141
Table 4.21	Summary of proposed distributed amplifiers.	142

Table 5.1	Summary for the de-embedded S-parameters, calculated group delay and power consumption of the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier.	154
Table 5.2	Summary for the measured 10 Gbps through eye of Figure 5.15 used to de-embed the test bench jitter contribution for Table 5.3	157
Table 5.3	Summary for the measured 10 Gbps output eye of Figure 5.13.	157
Table 5.4	Summary for the simulated 10 Gbps output eye of Figure 5.14.	157
Table 5.5	Summary for the measured 20 Gbps through eye of Figure 5.18	160
Table 5.6	Summary for the measured 20 Gbps output eye of Figure 5.16.	160
Table 5.7	Summary for the simulated 20 Gbps output eye of Figure 5.17.	160
Table 5.8	Summary for the simulated 20 Gbps output eye of Figure 5.19.	162
Table 5.9	Summary for the 22 Gbps simulated output eye of Figure 4.46 from Chapter 4	162
Table 5.10	Summary for the simulated 40 Gbps output eye of Figure 5.20.	162
Table 5.11	Summary for the measured 10 Gbps output eye of Figure 5.21.	165
Table 5.12	Summary for the simulated 10 Gbps output eye of Figure 5.22.	165
Table 5.13	Summary for the de-embedded S-parameters, calculated group delay and power consumption of the HBT single-ended three-stage cascoded f_T doubler distributed amplifier.	169
Table 5.14	Summary for the measured 10 Gbps through eye of Figure 5.30 used to de-embed the test bench jitter contribution for Table 5.15 . . .	172
Table 5.15	Summary for the measured 10 Gbps output eye of Figure 5.28.	172
Table 5.16	Summary for the simulated 10 Gbps output eye of Figure 5.29.	172
Table 5.17	Summary for the measured 10 Gbps through eye of Figure 5.33 used to de-embed the test bench jitter contribution for Table 5.18 . . .	174
Table 5.18	Summary for the measured 10 Gbps output eye of Figure 5.31.	174
Table 5.19	Summary for the simulated 10 Gbps output eye of Figure 5.32.	174
Table 5.20	Summary for the measured 20 Gbps through eye of Figure 5.34.	176
Table 5.21	Summary for the simulated 20 Gbps output eye of Figure 5.35.	177

Table 5.22	Summary for the simulated 20 Gbps output eye of Figure 5.35.	178
Table 5.23	Summary for the 22 Gbps simulated output eye of Figure 4.62.	179
Table 5.24	Summary for the 40 Gbps simulated output eye of Figure 5.37.	179
Table 5.25	Summary for the de-embedded S-parameters, calculated group delay and power consumption of the HBT three-stage cascode differential to single-ended distributed amplifier.	183
Table 5.26	Summary for the measured 20 Gbps output eye of Figure 5.43. De-embedding data is from Table 5.20.	185
Table 5.27	Summary for the simulated 20 Gbps output eye of Figure 5.44.	185
Table 5.28	Summary for the simulated 40 Gbps output eye of Figure 5.44.	187
Table 6.1.	Summary for the de-embedded S-parameters, calculated group delay and power consumption of the distributed amplifiers.	191
Table 6.2.	Summary for the 10 Gbps measured and de-embedded large-signal data for the distributed amplifiers.	192
Table 6.3.	Summary for the 20 Gbps measured and de-embedded large-signal data for the distributed amplifiers.	192
Table 6.4.	Summary for the 40 Gbps simulated large-signal data for the distributed amplifiers from Chapter 4 without the losses of the test bench, degraded transmission line termination and the long sequences of ones and zeros in the input prbs pattern.	193
Table 6.5	The gain bandwidth product and the modified gain bandwidth product for the distributed amplifier designs presented in this work. .	194

List of Figures

Figure 1.1.	A block diagram of a fibre optic transmit (Tx) and receive (Rx) channel showing a simple transmit and receive analog front end.	2
Figure 2.1.	(a) The constant-k T filter section and (b) The m-derived T filter section.	7
Figure 2.2.	The attenuation and phase constants versus frequency for the constant-k T filter section.	8
Figure 2.3.	The normalized image impedance of the constant-k T filter section.	10
Figure 2.4.	The (a) attenuation and (b) phase constants of the m-derived T filter section propagation constant for various values of m.	13
Figure 2.5.	(a) $ S_{21} $ and (b) $ S_{11} $ for the m-derived T section with resistive terminations for various values of m.	14
Figure 2.6.	Bisected- π m-derived termination.	16
Figure 2.7.	The normalized real portion of the output image impedance of the bisected- π m-derived filter section.	17
Figure 2.8.	An amplifier utilizing a two-terminal coupling network with impedance Z.	18
Figure 2.9.	A constant-k π filter section.	19
Figure 2.10.	Series-connected constant-k π filter sections.	20
Figure 2.11.	Resistively-terminated, constant-k T filter ladder network.	21
Figure 2.12.	(a) One and two-stage constant-k ladder networks and (b) the corresponding $ S_{11} $ and $ S_{21} $. Where $\omega_c = 2/\sqrt{LC}$, $C = 127$ fF and $L = 318$ pH.	22
Figure 2.13.	A generic two-port admittance π network.	24
Figure 2.14.	A simplified distributed amplifier (biasing is not shown).	27
Figure 2.15.	The π model for the heterojunction bipolar transistor.	28
Figure 2.16.	A simplified π model for the heterojunction bipolar transistor.	28

Figure 2.17.	A further simplified π model for the heterojunction bipolar transistor.	29
Figure 2.18.	The input artificial transmission line of a distributed amplifier.	29
Figure 2.19.	The output artificial transmission line of the distributed amplifier.	30
Figure 2.20.	A generic L section created by removing Y_I from the π network of Figure 2.13.	30
Figure 2.21.	Input line L section.	31
Figure 2.22.	Schematic of the cascaded multi-stage distributed amplifier from reference [26]	45
Figure 2.23.	Schematic of the distributed amplifiers for reference [34].	46
Figure 2.24.	Schematic of the stage-scaled distributed power amplifier for reference [38]	47
Figure 3.1.	Common emitter forced I_B configuration	50
Figure 3.2.	The I-V curves for the common emitter forced I_B configuration showing the operational limits for the device.	51
Figure 3.3.	Common emitter forced V_{BE} configuration.	52
Figure 3.4.	The I-V curves for the common emitter forced V_{BE} configuration showing the operational limits for the device.	53
Figure 3.5.	Common-base forced I_E configuration.	56
Figure 3.6.	The I-V curves for the common-base forced I_E configuration showing the operational limits for the device.	57
Figure 3.7.	MOSFET cross-section.	59
Figure 3.8.	Defects formed in the gate oxide of a MOSFET during a breakdown event.	60
Figure 3.9.	A defect conduction path formed in the gate oxide of a MOSFET.	60
Figure 3.10.	Simplified hybrid π bipolar transistor model.	63

Figure 3.11.	Percentage change in BVCEOR by operating below peak f_T .	69
Figure 3.12.	Simplified hybrid π MOSFET model.	71
Figure 4.1.	A CMOS single-ended five-stage distributed amplifier using a single device gain stage.	78
Figure 4.2.	Simulated S-parameters for the CMOS single-ended five-stage distributed amplifier of Figure 4.1.	79
Figure 4.3.	Simulated group delay for the CMOS single-ended five-stage distributed amplifier of Figure 4.1.	79
Figure 4.4.	Simulated 11 Gbps output eye for the CMOS single-ended five-stage distributed amplifier with a 700 mV 2^7 -1 prbs input to the test bench resulting in a 350 mV input prbs to the distributed amplifier of Figure 4.1.	80
Figure 4.5.	Simulated 22 Gbps output eye for the CMOS single-ended five-stage distributed amplifier with a 700 mV 2^7 -1 prbs input to the test bench resulting in a 350 mV input prbs to the distributed amplifier of Figure 4.1.	80
Figure 4.6.	Simulated 40 Gbps output eye for the CMOS single-ended five-stage distributed amplifier with a 700 mV 2^7 -1 prbs input to the test bench resulting in a 350 mV input prbs to the distributed amplifier of Figure 4.1.	81
Figure 4.7.	Common source amplifier with cascode transistors.	83
Figure 4.8.	(a) Schematic of a common-emitter amplifier, (b) schematic of a common-emitter common-base cascode amplifier.	84
Figure 4.9.	Common-emitter amplifier 1 dB compression point at 1 GHz.	85
Figure 4.10.	Common-emitter common-base (cascode) 1 dB compression point at 1 GHz.	85
Figure 4.11.	HBT cascode f_T doubler.	87
Figure 4.12.	HBT cascode f_T doubler 1 dB compression point at 1 GHz.	87
Figure 4.13.	CMOS single-ended five-stage cascoded f_T doubler distributed amplifier.	89

Figure 4.14.	HBT single-ended three-stage cascoded f_T doubler distributed amplifier.....	89
Figure 4.15.	HBT three-stage cascode differential to single-ended distributed amplifier.....	90
Figure 4.16.	Schematic for the single-ended CMOS f_T doubler.....	91
Figure 4.17.	High-frequency equivalent model for the f_T doubler.....	92
Figure 4.18.	Simplified schematic for the single-ended CMOS f_T doubler with resistive load.	95
Figure 4.19.	Low-frequency or DC equivalent model for the f_T doubler of Figure 4.18.....	96
Figure 4.20.	Cascode gain stage used in the CMOS distributed amplifier.	99
Figure 4.21.	Simplified high-frequency equivalent model for the f_T doubler.	100
Figure 4.22.	High frequency equivalent model for the cascode gain stage used in the CMOS distributed amplifier.	101
Figure 4.23.	The output artificial transmission line.....	102
Figure 4.24.	The input artificial transmission line.....	102
Figure 4.25.	HBT f_T doubler.	104
Figure 4.26.	High-frequency equivalent model for the HBT f_T doubler.	105
Figure 4.27.	HBT cascode differential pair gain stage.....	107
Figure 4.28.	Half circuit of the cascode differential gain stage.....	109
Figure 4.29.	Small-signal equivalent model for the single-ended emitter degenerated cascode amplifier.....	109
Figure 4.30.	Small-signal equivalent model of the differential cascode gain stage with the cascode base impedance Z_{BB}	111
Figure 4.31.	Constant-k T filter section (left) and m-derived π T filter section (right) with resistive terminations.	114

Figure 4.32.	A comparison between the constant-k T section and the m-derived T section ($m = 0.1$)..	114
Figure 4.33.	m-derived π T filter section (top) and constant-k T filter section with m derived bisected- π filter section (bottom) and resistive terminations.	115
Figure 4.34.	A comparison between the m-derived T section ($m = 0.1$) and a constant-k T section with bisected- π sections before the terminations ($m = 0.6$).	115
Figure 4.35.	m-derived π T filter section (top) and m-derived π T filter section with m derived bisected- π filter section (bottom) and resistive terminations.	116
Figure 4.36.	A comparison between the m-derived T section ($m = 0.1$) and a m-derived T section ($m = 0.1$) with bisected- π sections ($m = 0.6$) before the terminations.	116
Figure 4.37.	Inductor π model.	118
Figure 4.38.	Differential inductor T model.	119
Figure 4.39.	Layout of the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier.. . . .	120
Figure 4.40.	Layout of the HBT single-ended three-stage cascoded f_T doubler distributed amplifier.. . . .	121
Figure 4.41.	Layout of the HBT three-stage cascode differential to single-ended distributed amplifier.. . . .	122
Figure 4.42.	Simulated S-parameters for the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier.	124
Figure 4.43.	Simulated group delay for the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier.	124
Figure 4.44.	Input/Output referred 1dB compression point for the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier.. . . .	125

Figure 4.45.	Simulated 11 Gbps output eye for the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier with a 1.2 V 2^7 -1 prbs input to the test bench resulting in a 600 mV input prbs to the distributed amplifier.....	125
Figure 4.46.	Simulated 22 Gbps output eye for the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier with a 1.2 V 2^7 -1 prbs input to the test bench resulting in a 600 mV input prbs to the distributed amplifier.....	126
Figure 4.47.	Simulated 40 Gbps output eye for the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier with a 1.2 V 2^7 -1 prbs input to the test bench resulting in a 600 mV input prbs to the distributed amplifier.....	126
Figure 4.48.	Simulated S-parameters for the HBT single-ended three-stage cascoded f_T doubler distributed amplifier.	128
Figure 4.49.	Simulated group delay for the HBT single-ended three-stage cascoded f_T doubler distributed amplifier.	128
Figure 4.50.	Input/Output referred 1dB compression point for the HBT single-ended three-stage cascoded f_T doubler distributed amplifier.....	129
Figure 4.51.	Simulated 11 Gbps output eye for the HBT single-ended three-stage cascoded f_T doubler distributed amplifier with a 400 mV 2^7 -1 prbs input to the test bench resulting in a 200 mV input prbs to the distributed amplifier.....	129
Figure 4.52.	Simulated 22 Gbps output eye for the HBT single-ended three-stage cascoded f_T doubler distributed amplifier with a 400 mV 2^7 -1 prbs input to the test bench resulting in a 200 mV input prbs to the distributed amplifier.....	130
Figure 4.53.	Simulated 40 Gbps output eye for the HBT single-ended three-stage cascoded f_T doubler distributed amplifier with a 400 mV 2^7 -1 prbs input to the test bench resulting in a 200 mV input prbs to the distributed amplifier.....	130
Figure 4.54.	Simulated S-parameters for the HBT three-stage cascode differential to single-ended distributed amplifier.....	132
Figure 4.55.	Simulated group delay for the HBT three-stage cascode differential to single-ended distributed amplifier.....	132

Figure 4.56.	Common mode rejection ratio for the HBT three-stage cascode differential to single-ended distributed amplifier.	133
Figure 4.57.	Output referred power supply rejection ratio for the HBT three-stage cascode differential to single-ended distributed amplifier.	133
Figure 4.58.	Input/Output referred 1dB compression point for the HBT three-stage cascode differential to single-ended distributed amplifier.	134
Figure 4.59.	Simulated 11 Gbps output eye for the HBT three-stage cascode differential to single-ended distributed amplifier with a 400 mV 2^7 -1 prbs input to the test bench resulting in a 200 mV input prbs to the distributed amplifier.	134
Figure 4.60.	Simulated 22 Gbps output eye for the HBT three-stage cascode differential to single-ended distributed amplifier with a 400 mV 2^7 -1 prbs input to the test bench resulting in a 200 mV input prbs to the distributed amplifier.	135
Figure 4.61.	Simulated 40 Gbps output eye for the HBT three-stage cascode differential to single-ended distributed amplifier with a 400 mV 2^7 -1 prbs input to the test bench resulting in a 200 mV input prbs to the distributed amplifier.	135
Figure 4.62.	Simulated 22 Gbps output eye for the HBT single-ended three-stage cascoded f_T doubler distributed amplifier with a 600 mV 2^7 -1 prbs input to the test bench resulting in a 300 mV input prbs to the distributed amplifier.	139
Figure 4.63.	Simulated 40 Gbps output eye for the HBT single-ended three-stage cascoded f_T doubler distributed amplifier with a 600 mV 2^7 -1 prbs input to the test bench resulting in a 300 mV input prbs to the distributed amplifier.	139
Figure 4.64.	Simulated 22 Gbps output eye for the HBT three-stage cascode differential to single-ended distributed amplifier with a 800 mV 2^7 -1 prbs input to the test bench resulting in a 400 mV input prbs to the distributed amplifier.	140
Figure 4.65.	Simulated 40 Gbps output eye for the HBT three-stage cascode differential to single-ended distributed amplifier with a 800 mV 2^7 -1 prbs input to the test bench resulting in a 400 mV input prbs to the distributed amplifier.	141

Figure 5.1.	Photomicrograph of the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier.	144
Figure 5.2.	Photomicrograph of the HBT single-ended three-stage cascoded f_T doubler distributed amplifier.	145
Figure 5.3.	Photomicrograph of the HBT three-stage cascode differential to single-ended distributed amplifier.	146
Figure 5.4.	Simplified test bench diagram for S-parameter measurements	147
Figure 5.5.	Simplified test bench diagram for eye pattern measurements	148
Figure 5.6.	Distributed amplifier off-chip termination	149
Figure 5.7.	Corrected distributed amplifier off-chip termination	150
Figure 5.8.	Measured and simulated S_{11} (dB) for the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier	151
Figure 5.9.	Measured and simulated S_{22} (dB) for the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier	152
Figure 5.10.	Measured and simulated S_{21} (dB) for the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier	152
Figure 5.11.	Measured and simulated S_{12} (dB) for the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier	153
Figure 5.12.	Calculated group delay (ps) from measured and simulated data for the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier.	153
Figure 5.13.	Measured 10 Gbps output eye for the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier with a 1.5 V 2^7 -1 prbs input to the test bench resulting in a 750 mV input prbs to the distributed amplifier.	155
Figure 5.14.	Simulated 10 Gbps output eye for the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier with a 1.5 V 2^7 -1 prbs input to the test bench resulting in a 750 mV input prbs to the distributed amplifier.	155

Figure 5.15.	Measured 10 Gbps through eye (using a pad from the pad frame) with a 1.2 V 2^7 -1 prbs input to the test bench.	156
Figure 5.16.	Measured 20 Gbps output eye for the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier with a 1.12 V 2^9 -4 prbs input to the test bench resulting in a 560 mV input prbs to the distributed amplifier.	158
Figure 5.17.	Simulated 20 Gbps output eye for the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier with a 1.12 V 2^9 -4 prbs input to the test bench resulting in a 560 mV input prbs to the distributed amplifier.	159
Figure 5.18.	Measured 20 Gbps through eye (calibration standard) with a 1.12 V 2^9 -4 prbs input to the test bench.	159
Figure 5.19.	Simulated 20 Gbps output eye for the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier with the picoprobe and interconnect models removed from the simulation. A 1.12 V 2^9 -4 prbs input signal to the test bench resulting in a 560 mV input prbs to the distributed amplifier was used.	161
Figure 5.20.	Simulated 40 Gbps output eye for the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier with a 1.12 V 2^7 -1 prbs input signal to the test bench resulting in a 560 mV input prbs to the distributed amplifier was used.	162
Figure 5.21.	Measured 10 Gbps output eye for the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier with a 5 V rail voltage and a 1.2 V 2^7 -1 prbs input to the test bench resulting in a 600 mV input prbs to the distributed amplifier.	163
Figure 5.22.	Simulated 10 Gbps output eye for the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier with a 5 V supply and with the picoprobe and interconnect models removed from the simulation. A 1.2 V 2^7 -1 prbs input signal to the test bench resulting in a 600 mV input prbs to the distributed amplifier was used.	164
Figure 5.23.	Measured and simulated S11 (dB) for the HBT single-ended three-stage cascoded f_T doubler distributed amplifier.	166
Figure 5.24.	Measured and simulated S22 (dB) for the HBT single-ended three-stage cascoded f_T doubler distributed amplifier.	167

Figure 5.25.	Measured and simulated S21 (dB) for the HBT single-ended three-stage cascoded f_T doubler distributed amplifier.....	167
Figure 5.26.	Measured and simulated S12 (dB) for the HBT single-ended three-stage cascoded f_T doubler distributed amplifier.....	168
Figure 5.27.	Calculated group delay (ps) from measured and simulated data for the HBT single-ended three-stage cascoded f_T doubler distributed amplifier.....	168
Figure 5.28.	Measured 10 Gbps output eye for the HBT single-ended three-stage cascoded f_T doubler distributed amplifier with a 0.4 V 2^7 -1 prbs input to the test bench resulting in a 0.2 V input prbs to the distributed amplifier.....	170
Figure 5.29.	Simulated 10 Gbps output eye for the HBT single-ended three-stage cascoded f_T doubler distributed amplifier with a 0.4 V 2^7 -1 prbs input to the test bench resulting in a 0.2 V input prbs to the distributed amplifier.....	171
Figure 5.30.	Measured 10 Gbps through eye (calibration standard) with a 0.4 V 2^7 -1 prbs input to the test bench.	171
Figure 5.31.	Measured 10 Gbps output eye for the HBT single-ended three-stage cascoded f_T doubler distributed amplifier with a 0.8 V 2^7 -1 prbs input to the test bench resulting in a 0.4 V input prbs to the distributed amplifier.....	173
Figure 5.32.	Simulated 10 Gbps output eye for the HBT single-ended three-stage cascoded f_T doubler distributed amplifier with a 0.8 V 2^7 -1 prbs input to the test bench resulting in a 0.4 V input prbs to the distributed amplifier.....	173
Figure 5.33.	Measured 10 Gbps through eye (calibration standard) with a 0.8 V 2^7 -1 prbs input to the test bench.	174
Figure 5.34.	Measured 20 Gbps through eye (calibration standard) with a 700 mV 2^9 - 4 prbs input to the test bench.	176
Figure 5.35.	Simulated 20 Gbps output eye for the HBT single-ended three-stage cascoded f_T doubler distributed amplifier with a 0.7 V 2^9 - 4 prbs input to the test bench resulting in a 0.35 V input prbs to the distributed amplifier.....	177

Figure 5.36.	Simulated 20 Gbps output eye for the HBT single-ended three-stage cascoded f_T doubler distributed amplifier with the picoprobe and interconnect models removed from the simulation. A 700 mV 2^9 -4 prbs input signal to the test bench resulting in a 350 mV input prbs to the distributed amplifier was used.	178
Figure 5.37.	Simulated 40 Gbps output eye for the HBT single-ended three-stage cascoded f_T doubler distributed amplifier with a 0.7 V 2^7 -1prbs input to the test bench resulting in a 0.35 V input prbs to the distributed amplifier.....	179
Figure 5.38.	Measured and simulated S_{11} (dB) for the HBT three-stage cascode differential to single-ended distributed amplifier.	181
Figure 5.39.	Measured and simulated S_{22} (dB) for the HBT three-stage cascode differential to single-ended distributed amplifier.	181
Figure 5.40.	Measured and simulated S_{21} (dB) for the HBT three-stage cascode differential to single-ended distributed amplifier.	182
Figure 5.41.	Measured and simulated S_{12} (dB) for the HBT three-stage cascode differential to single-ended distributed amplifier.	182
Figure 5.42.	Calculated group delay (ps) from measured and simulated data for the HBT three-stage cascode differential to single-ended distributed amplifier.....	183
Figure 5.43.	Measured 20 Gbps output eye for the HBT three-stage cascode differential to single-ended distributed amplifier with a 600 mV 2^9 -4 prbs input to the test bench resulting in a 300 mV input prbs to the distributed amplifier.....	184
Figure 5.44.	Simulated 20 Gbps output eye for the HBT three-stage cascode differential to single-ended distributed amplifier with a 600 mV 2^9 -4 prbs input to the test bench resulting in a 300 mV input prbs to the distributed amplifier.....	185
Figure 5.45.	Simulated 40 Gbps output eye for the HBT three-stage cascode differential to single-ended distributed amplifier with a 600 mV 2^7 -1 prbs input to the test bench resulting in a 300 mV input prbs to the distributed amplifier.....	186

List of Symbols

A_0, A_1, A_2, A_3	Power series coefficients
A_B	Input (base) line attenuation per section
A, B, C, D	Transmission or ABCD matrix elements for a two-port network
A_C	Output (collector) line attenuation per section
ADC	Analog-to-digital converter
AGC	Automatic gain control amplifier
A_V	Voltage gain
α	constant calculated using the bit error rate and the complementary error function and used to relate RMS jitter to peak-to-peak jitter
β	Transistor current gain
B	Bandwidth
BER	Bit error rate
BV	Diode breakdown voltage
BV_{CBO}	Transistor collector-base breakdown voltage with the device in the common-base, open circuited emitter configuration
BV_{CEO}	Transistor common-emitter forced I_B collector-emitter breakdown voltage
BV_{CEOR}	Transistor base impedance dependent common-emitter forced V_{BE} collector-emitter breakdown voltage
BV_{GDSS}	Transistor gate-to-substrate or gate-to-drain/source breakdown voltage
C	Capacitor
C_{BE}	Base-emitter depletion capacitance
C_{jBC}	Base-collector junction capacitance
C_{jBCo}	Base-collector the junction capacitance at zero bias voltage

C_{jBE}	Base-emitter junction capacitance
C_{jBE0}	Base-emitter junction capacitance at zero bias voltage
C_c	Coupling capacitance
C_{DB}	Drain-to-bulk capacitance
C_{GB}	Gate-to-bulk capacitance
C_{GD}	Gate-to-drain capacitance
C_{GS}	Gate-to-source capacitance
C_{ox}	Oxide capacitance
C_o	Oxide/ dielectric capacitance
C_{sub}	Substrate capacitance
C_{SB}	Source-to-bulk capacitance
C_T	Emitter-base capacitance summed with the Miller capacitance
C_{Tx}	Emitter-base capacitance summed with the Miller capacitance per gain stage (where x = 1, 2,..., etc)
C_μ	Collector-base capacitance
$C_{\mu j}$	Miller capacitance (where j = 1, 2)
C_π	Emitter-base capacitance
DAC	Digital-to-analog converter
DCD	Duty-cycle-distortion
ϵ_{ox}	Oxide permittivity
f_{max}	Maximum frequency of oscillation
f_T	Unity current gain frequency
f	Frequency
G	Power gain

GBW	Gain bandwidth product
G_m	Transconductance of the CMOS f_T doubler gain stage
g_m	Transconductance
g_{mx}	Transconductance per gain stage (where $x = 1, 2, 3, \dots$, etc)
I	Current
I_C	Bipolar transistor collector current
I_{C0}	Bipolar transistor pre-avalanche breakdown collector current
I_B	Bipolar transistor base current
I_{B0}	Bipolar transistor pre-avalanche breakdown base current
I_j	Port currents (where $j = 1, 2, \dots$, etc)
I_R	Reverse bias current of junction diode
I_{RA}	Current near the breakdown voltage of a junction diode
I_x	Current at each node (where $x = 1, 2, 3, \dots$, etc)
I_{Z_C}	Total current at the terminations of the output (collector) line
i	Small-signal current added to calculate the current gain of the CMOS f_T doubler
i_B	Small-signal base current
i_C	Small-signal collector current
i_D	Small-signal drain current
i_G	Small-signal gate current
i_o	Small-signal output current\
$Jitter_{dut}$	Jitter for the device under test
$Jitter_{meas}$	Measured jitter

$Jitter_{p-p}$	Peak-to-peak jitter
$Jitter_{RMS}$	RMS jitter
$Jitter_{tb}$	Jitter contribution of the test bench
k	Characteristic impedance of the constant-k filter sections
L	Inductor
L_{ch}	MOSFET channel length
L_B	Input (base) line series arm inductance
L_{Bx}	Input (base) line series arm inductance per gain stage (where x = 1, 2,..., etc)
L_C	Output (collector) line series inductance
L_D	Output (drain) line series inductance
L_G	Input (gate) line series arm inductance
M	Multiplication factor
M	Mutual inductance
m	Variable used to control the resonant frequency of the m-derived T filter section
MGBW	Modified gain bandwidth product
μ_o	Carrier mobility
N	Total number of gain stages
N_{opt}	Optimum number of distributed amplifier stages
P_{1dB}	Power of the input-referred 1 dB compression point
P_{DC}	DC power consumed by the amplifier
P_{IIP3}	Power of the input-referred 3rd order intercept point
P_{in}	Signal power sent to the amplifier

P_{out}	Signal power sent to the load
prbs	Pseudo-random binary sequence
ψ	Propagation constant
ψ_B	Input (base) line phase shift per section
ψ_{BC}	Built-in base-collector junction potential
ψ_{BE}	Built-in base-emitter junction potential
ψ_C	Output (collector) line phase shift per section
ψ_D	Output (drain) line phase shift per section
ψ_G	Input (gate) line phase shift per section ψ_i Phase constant
ψ_k	Phase shift per section (where k = 1, 2,..., etc)
ψ_r	Attenuation constant
Q ₁ , Q ₂ , etc	Transistor name
R	Resister
R_B	Base resistance
r_e	Emitter resistor
R_E	Emitter degeneration resistor
R_G	Gate resistance
R_L	Load resistance
R_μ	Base-collector shunt resistance
R_O	Collector output resistance
R_π	Base input resistance
$R_{\pi x}$	Base input resistance per gain stage (where x = 1, 2,..., etc)
R_S	Source resistance

R_{sub}	Substrate resistance
R_X	Receiver
S_{11}	Input voltage reflection coefficient of a two-port network scattering parameter matrix
S_{12}	Reverse voltage gain of a two-port network scattering parameter matrix
S_{21}	Forward voltage gain of a two-port network scattering parameter matrix
S_{22}	Output voltage reflection coefficient of a two-port network scattering parameter matrix
s	Imaginary frequency in radians $j\omega$
τ_B	Base transit time
TIA	Trans-impedance amplifier
T_{ox}	Oxide thickness
T_X	Transmitter
θ	Mobility degradation coefficient
V	Voltage
V_{on}	Minimum voltage to place MOSFET into saturation
V_{added}	Voltage source added to calculate the output impedance of the simplified hybrid π bipolar transistor model
V_{BE}	Transistor base-emitter voltage
V_{CB}	Transistor collector-base voltage
V_{CE}	Transistor collector-emitter voltage
V_{DS}	Transistor drain-source voltage
V_i, V_{in}	Input voltage
V_j	Port voltages (where $j = 1, 2, \dots$, etc)
V_{out}	Output voltage

V_R	Diode reverse bias voltage
V_π	Small-signal voltage across the base-emitter resistor R_π
$V_{\pi X}$	Small-signal base-emitter voltage for the X^{th} transistor
V_T	Thermal voltage of a p-n junction $V_T = 26$ mV at 300 degrees Kelvin
V_{Th}	Transistor threshold voltage
V_x	Small-signal voltage across the gate source capacitance
V_y	Small-signal collector-emitter voltage
v_B	Small-signal base voltage
v_{sat}	Saturation velocity
W_{ch}	MOSFET channel width
ω	Frequency, in radians
ω_C	Cut-off frequency
ω_R	Resonant frequency
Y	Admittance
Z	Impedance of a two-terminal matching network
Z_B	Input (base) artificial transmission line termination
Z_{BB}	Cascode base impedance
Z_i, Z_{in}	Input impedance
$Z_{i_B^j}$	Input (base) line image impedance per section (where $j = 1, 2$)
$Z_{i_G^j}$	Input (gate) line image impedance per section (where $j = 1, 2$)
Z_C	Output (collector) artificial transmission line termination
Z_D	Output (drain) artificial transmission line termination
Z_G	Input (gate) artificial transmission line termination
Z_{ij}	Image impedance (where j is the port number = 1, 2,...,etc)

$Z_{i_n^j}$	Port image impedance per two port network (where j is the port number = 1, 2,..., etc and n is the two port network = 1,2,..., etc)
Z_I	Image impedance
Z_π	Constant-k π filter section image impedance
Z_O	Characteristic impedance
Z_o	Output impedance

Chapter 1: Introduction

Internet traffic, such as on-line video streaming, high-definition video telepresence and other multimedia services is putting a strain on the existing telecommunications infrastructure. The telecommunications industry needs to provide high data rates yet keep the cost of implementing this larger bandwidth as low as possible. Technologies like InP, GaAs, and GaN (a selection of the technologies that are often referred to as III-Vs) are expensive and do not offer the high integration density and lower cost that silicon technologies can provide. Furthermore, a BiCMOS process offers the end user a complementary metal oxide semiconductor (CMOS) solution for lower power consumption and high density digital processing coupled with Silicon Germanium (SiGe) Heterojunction Bipolar Transistors (HBTs) which provide the higher speed and gain than is available in the CMOS devices.

In fibre optic communications, distributed amplification has traditionally been implemented in the III-V technologies. These technologies are advantageous because they can provide distributed amplifiers with the large voltage swings needed to drive the electro-optical modulators (EOMs) used in fibre optic transmitters (as in Figure 1.1). The high substrate resistance of the III-V technologies provides better isolation and devices with less loss, and the high electron mobility and velocity allows for large bandwidths. However, advances in SiGe and CMOS have created technologies with f_T and f_{max} well in excess of 100 GHz [1,2]. The silicon foundries have implemented various techniques to reduce the parasitics and improve device isolation. The addition of more metal layers, with the top layers being thick copper, has resulted in better performing passive devices [1,2]. The performance of CMOS and SiGe is moving closer to that of the III-V technologies with respect to bandwidth and device speed. However, the output voltage swing and device breakdown are still limiting factors for distributed amplification in silicon substrates.

Figure 1.1. A block diagram of a fibre optic transmit (Tx) and receive (Rx) channel showing a simple transmit and receive analog front end.

To achieve higher density, and faster speeds, the foundries are producing silicon devices with smaller gate lengths and thinner gate oxides. As a result, the breakdown voltages are also getting smaller. The advantage of BiCMOS is the combination of the high density CMOS with the higher gain and breakdown voltage SiGe HBTs in a single technology. Although SiGe has a higher breakdown voltage than CMOS, it still has a breakdown voltage lower than what is available in the III-Vs. Therefore, if silicon is to be a viable alternative for distributed amplification, novel circuit techniques and an understanding of the breakdown mechanisms are required to achieve output voltage swings beyond the breakdown voltage limit of a single SiGe or CMOS device.

1.1 Thesis Goals

A distributed amplifier consists of a series of gain stages connected together by input and output transmission lines. The input signal propagates down the transmission

line and through the individual gain stages to be summed at the output transmission line. The operation of the distributed amplifier is dependant on the delays of the individual gain stages being matched in such a way that the outputs of the gain stages are summed in phase.

In the fibre optic system of Figure 1.1 the analog to digital converter (ADC) in the transmitter produces CML (current mode logic or source coupled logic) output voltage levels (typically around 300mV or less) that have to be amplified to a few volts or even tens of volts to drive the EOM [3,4,5,6,7,8]. This is typically done with III-V distributed amplifiers. A silicon distributed amplifier can be integrated or co-packaged with the ADC (and potentially with the pre-distortion block as well) to produce voltage levels on the order of 1 to 2 volts. Introducing the silicon distributed amplifier into the fibre optic system of Figure 1.1 has several advantages:

- 1) The need for multiple packaged amplifiers to drive the EOM can be reduced by integrating the silicon distributed amplifier with the rest of the CMOS or SiGe circuitry to function as a pre-driver for the III-V distributed amplifier. The silicon distributed amplifier could also be integrated or co-packaged with the III-V distributed amplifier and an EOM.
- 2) Research being conducted in silicon EOMs has yielded Mach Zehnder modulators requiring input signal voltage swings between 1 and 2 volts peak-to-peak with less than 50 mW signal power, as well as silicon EOMs with integrated SiGe drivers also producing less than 2 volt peak-to-peak output swings [5, 7]. Although the introduction of a silicon EOM into a commercially available optical system is still some years away, a silicon distributed amplifier could, in time, replace the III-V distributed amplifier as well as be integrated with the silicon EOM

- 3) Finally, the integration or co-packaging of the distributed amplifier with the rest of the CMOS circuitry or with the EOM will reduce the number of packaged parts, which can result in a significant cost savings. Also, reducing the number of packaged elements could improve the link budget by removing the associated losses of the aforementioned packaged elements.

Most of the available published results for distributed amplifiers in silicon substrates concentrates on the small signal results and provides little or no large signal information (as per the literature study in chapter 2). The research presented in this thesis is an exploration of techniques aimed at improving the large signal output performance of silicon distributed amplifiers for use in fibre optic communication systems. The experimental verification of these techniques involves the design and implementation of several distributed amplifiers in a standard, readily available, silicon process: ST Microelectronics BiCMOS9 process with eight metal layers and a minimum drawn length of 0.13 microns [1]. In pursuit of this objective, three distributed amplifiers with bandwidths suitable for 40 gigabit per second data rates (Gbps) have been designed and fabricated:

- A CMOS single-ended five-stage cascoded f_T doubler distributed amplifier producing better than 1V peak-to-peak output voltage swing.
- A HBT single-ended three-stage cascoded f_T doubler distributed amplifier producing better than 2V peak-to-peak output voltage swing.
- A HBT three-stage cascode differential to single-ended distributed amplifier producing better than 2V peak-to-peak output voltage swing.

The novel use of the f_T doubler gain stage, m-derived and constant-k filter sections in the first two distributed amplifier topologies increases the bandwidth and gain over that which is available from a single device gain stage distributed amplifier. The f_T doubler

gain stage allows the designer to trade the extended bandwidth for the gain necessary to achieve a large output voltage swing.

It is often necessary to transition from a differential signal to a single-ended signal. A novel approach is to use a distributed amplifier as a differential to single-ended converter that would either act as a pre-driver for a III-V distributed amplifier or drive the EOM itself (in the case of a silicon EOM). Therefore, the third distributed amplifier design is a novel differential input and single-ended output distributed amplifier intended to function as a high-speed broadband differential to single-ended converter.

1.2 Thesis Outline

Chapter 2 presents information on two-port networks and discusses issues concerning bandwidth, the gain-bandwidth product, and distributed amplifier design theory. Questions concerning breakdown of CMOS and heterojunction transistors, as well as linearity, are considered in Chapter 3. Chapter 4 contains the distributed amplifier designs and simulation data. The experimental results are discussed in Chapter 5. Finally, in Chapter 6 the thesis conclusions and a summary of the work are presented.

Chapter 2: Distributed Amplifier Theory

In this chapter some of the background theory necessary to the understanding of distributed amplification and how to improve the large-signal performance of a distributed amplifier is presented. The chapter is divided into three sections: 1) artificial transmission lines, 2) bandwidth and the advantages of distributing parasitic capacitances, and 3) the design of a distributed amplifier.

2.1 Filter Sections

A key component of distributed amplification is the artificial transmission line. If the definition of transmission lines is restricted to those lines that are used to transmit data, then transmission lines are a means of transporting data over large distances with minimal loss. The most frequently used transmission lines are twisted pair, coaxial line, parallel plate, microstrip, waveguide and optical fiber [9,10]. Transmission lines are frequently modeled as distributed circuits with resistive, capacitive and inductive elements. An artificial transmission line uses these same lumped elements to mimic the performance of an actual transmission line. These lines can be simplified by assuming that both the conductor and the dielectric are lossless. Therefore, a lossless artificial transmission line consists of capacitive and inductive elements.

2.1.1 The Constant-k T Networks

Figure 2.1. (a) The constant-k T filter section and (b) The m-derived T filter section.

The two-port networks of Figure 2.1 are frequently used to model the lossless artificial transmission lines of distributed amplifiers [11,12,13]. These two-port networks pass low-frequency signals while attenuating the high-frequency signals and can therefore be defined as low-pass filter sections. The frequency response of these networks is divided into two regions, the passband where, $\omega < \omega_c$, and the stopband, where $\omega > \omega_c$.

The cutoff frequency, ω_c , is defined as:

$$\omega_c = \frac{2}{\sqrt{LC}} \quad (2.1)$$

The propagation constant ψ for the constant-k T filter section (Figure 2.1 a) is used to describe the behavior of an incident wave passing through the filter section and is defined as:

$$\psi = \ln \left(1 - \frac{2\omega^2}{\omega_c^2} + \frac{2\omega^2}{\omega_c^2} \sqrt{\frac{\omega^2}{\omega_c^2} - 1} \right) \quad (2.2)$$

From (2.2) it can be shown that in the passband region of operation, or when $\omega < \omega_c$, the propagation constant is imaginary and is referred to as the phase constant ψ_l .

The phase constant represents the change in phase per filter section and is measured in radians (rad). Conversely, when $\omega > \omega_c$ as is the case for the stopband, ψ is real and referred to as the attenuation constant ψ_r . The attenuation constant is measured in nepers (Np) and represents the attenuation per filter section on an incident wave. For the ideal constant-k filter section, it can be clearly seen from Figure 2.2 that in the passband an incident wave experiences a phase change with no apparent attenuation until $\omega = \omega_c$, at which point the attenuation constant begins to grow.

Figure 2.2. The attenuation and phase constants versus frequency for the constant-k T filter section.

The two-port networks of Figure 2.1 can be analyzed by using the image parameter method. For the image parameter equations to be valid, the analysis requires the opposing port to be terminated with its image impedance (i.e., calculating the input impedance requires the output to be terminated with its output image impedance).

The image impedance of a network is the impedance seen looking into the ports of that network. Since the constant-k filter section is a symmetrical network, the input impedance is equal to the output impedance, which is equal to the image impedance and is given by [13]:

$$Z_I = \sqrt{\frac{L}{C}} \sqrt{1 - \frac{\omega^2 LC}{4}} = Z_O \sqrt{1 - \frac{\omega^2}{\omega_c^2}} \quad (2.3)$$

where the nominal characteristic impedance, Z_O , is:

$$Z_O = \sqrt{\frac{L}{C}} = k \quad (2.4)$$

The image impedance shown in (2.3) is not constant and is dependent on frequency. As can be seen in Figure 2.3, for $\omega < \omega_c$, the image impedance is real (the passband), while for $\omega > \omega_c$ (the stopband), the image impedance is imaginary. This dependency on frequency is a limitation of the constant-k T section, since the image impedance will not match any given source or load over all frequencies [13]. Furthermore, it can be clearly seen from Figure 2.2 that the attenuation near the cut-off frequency is small and, depending on the application, may not meet the passband and stopband requirements of the desired filter.

Figure 2.3. The normalized image impedance of the constant-k T filter section.

2.1.2 The m-Derived T Section

The m-derived T section of Figure 2.1 (b) is a modification of the constant-k T section. It can be shown that both filter sections still maintain the same image impedance as defined by (2.3) even though the m-derived T filter section has an LC series resonance in the shunt arm of the filter. This series resonance can be used to address the aforementioned attenuation and, by bisecting the m-derived T section, also address the termination impedance issues present in the constant-k T filter section.

The resonant frequency of the LC shunt arm is defined as [13]:

$$\omega_R = \frac{\omega_c}{\sqrt{1-m^2}} \quad (2.5)$$

Although the image impedance has not changed for the m-derived filter section, the shunt arm series resonance does affect the propagation constant. The m-derived T filter section propagation constant is defined as:

$$\psi = \ln \left(1 + \frac{1}{2} \frac{-\left(\frac{2\omega m}{\omega_c}\right)^2}{1 - (1-m^2)\left(\frac{\omega}{\omega_c}\right)^2} + \sqrt{\frac{-\left(\frac{2\omega m}{\omega_c}\right)^2}{1 - (1-m^2)\left(\frac{\omega}{\omega_c}\right)^2} \left(1 + \frac{1}{4} \frac{-\left(\frac{2\omega m}{\omega_c}\right)^2}{1 - (1-m^2)\left(\frac{\omega}{\omega_c}\right)^2} \right)} \right) \quad (2.6)$$

Note that $0 < m < 1$, and if m is set to 1, the passband and stopband characteristics are identical to those of the constant-k T section. Figure 2.4 shows the real and imaginary parts of the propagation constants versus frequency (recalling that the propagation constant transitions from a real to an imaginary number when the frequency equals the cut-off frequency) for the m-derived T filter section. The magnitude of the attenuation constant can be increased by choosing a value for m closer to 0 as can be seen from Figure 2.4 a). Similarly, it is clear from Figure 2.4 b) that the passband phase change due to the m-derived filter section is also impacted by the value of m . The phase change in the passband of the m-derived T filter section with $m = 1$ is linear for approximately 80% of the pass-

band and becomes more non-linear as the frequency approaches cutoff ω_c . However, the passband phase also becomes more non-linear as the value of m approaches 0.

A linear phase change implies an equal delay at all frequencies and therefore minimal phase distortion of the output. On the other hand, an increase in the attenuation near ω_c corresponds to a reduced magnitude for unwanted frequency tones and therefore reducing the distortion of the output data. Therefore, a trade-off exists between increased attenuation at the cutoff frequency ω_c and the linearity of the passband phase.

Recall that the required termination for the m -derived section is the image impedance of (2.3). This impedance is frequency dependant and not easily realizable and therefore is often replaced with a resistor. The filter sections image impedance provides a perfect match to the input/output of the filter section. As such, the scattering parameter or S-parameter input reflection coefficient (S_{11}) of the filter section can be used to see how far the output match has deteriorated by adding a resistive load. The forward voltage gain (S_{21}) can also be used to see the impact on the passband and stopband of the filter section. Figure 2.5 is a plot of the magnitudes of S_{21} and S_{11} for an m -derived T filter section with resistive terminations.

(a)

(b)

Figure 2.4. The (a) attenuation and (b) phase constants of the m -derived T filter section propagation constant for various values of m .

(a)

(b)

Figure 2.5. (a) $|S_{21}|$ and (b) $|S_{11}|$ for the m -derived T section with resistive terminations for various values of m .

From Figure 2.5 (a), we can see that for $m = 1$ and 0.6 the resistively terminated m -derived T filter section has an input reflection coefficient better than 0.3 , or approximately -10dB , for about 60% of the passband thereafter getting rapidly worse (quickly approaching unity) as the frequency approaches cut-off. This occurs because the real portion of the image impedance goes to zero at the cutoff frequency while the resistive termination remains constant over the entire frequency band. The best broadband match to the load in Figure 2.5 (a) is obtained when $m = 0.1$. With $m = 0.1$ the input reflection coefficient remains below 0.3 for approximately 80% of the passband. Therefore from Figure 2.5 (a), it can be concluded that $m \ll 1$ will result in a better input/output match to a resistive load. Unfortunately, the smaller m values also have a faster rate of change and a larger input reflection coefficient near cutoff.

Observing the forward voltage gain (S_{21}) from Figure 2.5 (b) when $m = 0.1$ the passband is flatter and exhibits a much sharper roll-off near the cut-off frequency (higher attenuation near the cut-off). This sharp roll-off can be useful for filtering out unwanted close in frequency tones with the caveat that $m = 0.1$ also results in a reduced phase linearity that rises rapidly near the cut-off frequency ω_c (see Figure 2.4). The rapid rise in phase requires that the desired input data be further away from the cut-off to avoid distortion. The trade-off between phase linearity and attenuation (roll-off) must be taken into account when deciding what value of m to use.

2.1.3 The Bisected- π m-Derived Filter Section

The m-derived and constant-k T filter sections have an image impedance that is a function of frequency. A resistor often replaces the required termination for these sections. As seen in Figure 2.5, a resistive termination reduces the performance of these two-port networks. One way to correct for this reduced performance is to convert the m-derived T section into a π section. This conversion changes the image impedance to [13]:

$$Z_I = Z_o \frac{1 - (1 - m^2)(\omega/\omega_c)^2}{\sqrt{1 - (\omega/\omega_c)^2}} \quad (2.7)$$

This new image impedance allows us to use m to minimize the effects of frequency. The π section can be bisected and used before a resistive termination as part of a network of filter sections. The new bisected- π m-derived filter section of Figure 2.6 has an input image impedance equal to that of (2.3) and an output image impedance as seen in (2.7). Figure 2.7 clearly shows that $m = 0.6$ provides the best broadband match to a resistive termination.

Figure 2.6. Bisected- π m-derived termination.

Figure 2.7. The normalized real portion of the output image impedance of the bisected- π m -derived filter section.

2.1.4 Summary

The filter section information presented thus far will be used in the following sections to design the artificial transmission lines that are integral to the design of distributed amplifiers. These filter sections can be used not only to design distributed amplifiers but to design filters and any other applications that require distributed networks. The choice of which combination, or simply which two-port network, to use is often determined not only by the required specifications of the design, but the space needed to implement that design.

2.2 Bandwidth

There are several performance metrics that are used to quantify the performance of an amplifier. In the next section one such metric, the gain-bandwidth product, is presented as well as a brief discussion on the frequency performance of constant-k two-port ladder networks.

2.2.1 Gain-Bandwidth Product

The gain of an amplifier can be maximized by inserting a passive matching network between the amplifier and its load. This passive network will provide the maximum power transfer and minimize any reflections from the load.

Figure 2.8. An amplifier utilizing a two-terminal coupling network with impedance Z .

The amplifier of Figure 2.8 has a two-terminal matching network with impedance Z . It can be shown that the matching network is composed of inductive L and capacitive C components. Therefore, the matching network has an impedance Z described by:

:

$$Z = \left[\frac{1}{2} (\sqrt{\omega_c^2 - \omega^2} + j\omega) C \right]^{-1} \quad (2.8)$$

where ω_c is the cut-off frequency and ω is the frequency of interest.

An amplifier's maximum gain bandwidth product, assuming an optimally matched load, via a two-port matching network can be shown to be[12]:

$$A_V B = \frac{g_m}{\pi C} \quad (2.9)$$

where A_V is the voltage gain, B is the 3 dB bandwidth in units of Hertz and C is the capacitance of the matching network.

Figure 2.9. A constant-k π filter section.

The T filter sections in Figure 2.1 also have a π form such as the constant-k π filter section of Figure 2.9. The image impedance of the of the π filter section is

$$Z_\pi = \left[\frac{1}{2} (\sqrt{\omega_c^2 - \omega^2}) C \right]^{-1} \quad (2.10)$$

It is immediately apparent that the impedance given in (2.8) is very similar to the image impedance of the constant-k π filter section of (2.10). To use a constant-k π filter section as a two-terminal matching network and obtain the maximum gain bandwidth product the filter section must be driven by a parallel capacitance of $C/2$. Incorporating the driving capacitance $C/2$ into (2.10) results in the desired impedance of (2.8).

2.2.2 Bandwidth and the Distributed Structure

The constant- k π filter section provides a means of connecting two devices without sacrificing the gain bandwidth product. The difficulty is achieving the desired gain with the required bandwidth.

The bandwidth issue can be addressed by connecting multiple constant- k π filter sections together to form a ladder network, as in Figure 2.10. This ladder network can be simplified by combining capacitances to form constant- k T sections as in Figure 2.11. The ideal termination for the ladder network is the filter sections image impedance but as has been previously discussed it is more common to terminate the network by a more easily realizable approximation. Therefore, it can be shown that converting from π to T sections and terminating with a resistive element (see Figure 2.11) provides a reasonable approximation to the ideal π ladder network with image impedance terminations [12].

Figure 2.10. Series-connected constant- k π filter sections.

Figure 2.11. Resistively-terminated, constant-k T filter ladder network.

The ladder network of Figure 2.11 is composed of several filter sections which are in turn composed of inductors and capacitors. The bandwidth of the ladder network can be increased by increasing the number of filter sections while maintaining the same total capacitance and inductance. In other words each filter section is composed of a fraction of the total inductance and capacitance of the ladder network. Figure 2.12 shows the impact of taking a single filter section and distributing the capacitance and inductance in a ladder network formed from two filter sections. Recall that the cut-off frequency for a constant-k T filter section is $\omega_c = \frac{2}{\sqrt{LC}}$ and therefore the cut-off frequency of each filter section in the ladder network (and consequently the ladder network itself) is increased as the L and C are reduced. Distributing the capacitance and inductance in this way can also be applied to the constant-k π filter section.

(a)

(b)

Figure 2.12. (a) One and two-stage constant-k ladder networks and (b) the corresponding $|S_{11}|$ and $|S_{21}|$. Where $\omega_c = 2/\sqrt{LC}$, $C = 127$ fF and $L = 318$ pH.

2.2.3 Summary

We now have a means of obtaining the desired bandwidth and gain from an amplifier. The distributed technique discussed in this chapter is the fundamental precept behind distributed amplification. The constant-k filter sections can be used to connect together multiple gain stages. The bandwidth of the amplifier increases as the input and output capacitances of the gain stages decrease. Therefore, it is desirable to reduce the size and gain of each gain stage in order to reduce the input and output capacitance. More gain stages can be added to achieve or maintain the desired gain of the amplifier. It is important to note that there is a practical limit to the number of gain stages. This limit is presented in the following section.

2.3 Distributed Amplifier Theory

A design methodology for a distributed amplifier employing artificial transmission lines is presented in this section. The analysis of the distributed amplifier is done using the image parameter method. The resulting equations can be used in computer-aided simulation for a more rigorous design analysis.

2.3.1 ABCD parameters

The analysis begins with the ABCD matrix, which will be used later in the analysis of the distributed amplifier. The ABCD matrix is a representation of the transmission characteristics of a two-port network. The ABCD matrix is defined as follows:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \quad (2.11)$$

The voltage and current of port one and port two are represented by V_1 , I_1 and V_2 , $-I_2$ respectively. The negative sign for I_2 indicates that current flows out of the terminal while positive current is defined to flow into the terminal [14, 15].

One of the benefits of using the ABCD matrix is that a cascade of two-port networks has an ABCD matrix that can be determined by the multiplication of the constituent two-port ABCD transmission matrices.

A cascade of two networks is as follows:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} \begin{bmatrix} V_3 \\ -I_3 \end{bmatrix} \quad (2.12)$$

An example of ABCD parameters expressed in terms of admittance Y for the two-port network of Figure 2.13 is as follows [13]:

$$A = 1 + \frac{Y_2}{Y_3}, \quad (2.13)$$

$$B = \frac{1}{Y_3}, \quad (2.14)$$

$$C = Y_1 + Y_2 + \frac{Y_1 Y_2}{Y_3}, \quad (2.15)$$

and

$$D = 1 + \frac{Y_1}{Y_3} \quad (2.16)$$

The ABCD parameters (2.13) - (2.16) will be used in the analysis of the distributed amplifier

Figure 2.13. A generic two-port admittance π network.

2.3.2 Image Parameters

The image parameter method is a simple way of analyzing the performance of a two-port filter network. The analysis uses the passband and stopband characteristics as well as the ABCD transmission matrix to design the network. The image impedances for a two-port network are defined as [13]:

image impedance of port one:

$$Z_{i1} = \sqrt{\frac{AB}{CD}} \quad (2.17)$$

image impedance of port two:

$$Z_{i2} = \sqrt{\frac{BD}{AC}} \quad (2.18)$$

The image impedances given by (2.17) and (2.18) are valid only when the other port is terminated with its corresponding image impedance.

The two-port voltage and current ratios can be expressed as follows [13]:

$$\frac{V_2}{V_1} = \sqrt{\frac{D}{A}}(\sqrt{AD} - \sqrt{BC}) \quad (2.19)$$

and

$$\frac{-I_2}{I_1} = \sqrt{\frac{A}{D}}(\sqrt{AD} - \sqrt{BC}) \quad (2.20)$$

where the propagation constant for the two-port network is:

$$e^{-\Psi} = \sqrt{AD} - \sqrt{BC} \quad (2.21)$$

In a reciprocal network $AD - BC = 1$, therefore:

$$e^{\Psi} = \frac{1}{\sqrt{AD} - \sqrt{BC}} = (\sqrt{AD} + \sqrt{BC}) \quad (2.22)$$

and

$$\cosh \Psi = \frac{(e^{\Psi} + e^{-\Psi})}{2} \quad (2.23)$$

We can show that

$$\cosh \psi = \sqrt{AD} \quad (2.24)$$

and

$$\sinh \psi = \sqrt{BC} \quad (2.25)$$

Using (2.17) through (2.25), we can define an ABCD matrix in terms of the two-port network image parameters:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} \sqrt{\frac{Z_{i1}}{Z_{i2}}} \cosh \psi & \sqrt{Z_{i1} Z_{i2}} \sinh \psi \\ \sqrt{(Z_{i1} Z_{i2})^{-1}} \sinh \psi & \sqrt{\frac{Z_{i2}}{Z_{i1}}} \cosh \psi \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \quad (2.26)$$

The matrix for a network composed of n two-port networks is as follows:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} \sqrt{\frac{Z_{i1}}{Z_{i2}}} \cosh \psi & \sqrt{Z_{i1} Z_{i2}} \sinh \psi \\ (\sqrt{Z_{i1} Z_{i2}})^{-1} \sinh \psi & \sqrt{\frac{Z_{i2}}{Z_{i1}}} \cosh \psi \end{bmatrix} \begin{bmatrix} V_{n+1} \\ -I_{n+1} \end{bmatrix} \quad (2.27)$$

where:

$$\psi = \sum_{k=1}^n \psi_k \quad (2.28)$$

and ψ_k is the phase shift per filter section.

The voltage and current ratios are now expressed as:

$$\frac{V_{n+1}}{V_1} = \sqrt{\frac{Z_{i2}}{Z_{i1}}} \sum_{k=1}^n e^{-\psi_k} \quad (2.29)$$

and

$$\frac{I_{n+1}}{I_1} = -\sqrt{\frac{Z_{i1}}{Z_{i2}}} \sum_{k=1}^n e^{-\psi_k} \quad (2.30)$$

With the equations thus far outlined we can now proceed to the analysis of the distributed amplifier of Figure 2.14.

Figure 2.14. A simplified distributed amplifier (biasing is not shown).

2.3.3 Distributed Amplifier Analysis

The image parameter method is commonly used to analyze the performance of the artificial transmission lines created in the design of distributed amplifiers. This method assumes that the networks are terminated with their characteristic impedances and, as such, serves only as an estimate to the actual performance of the distributed amplifier with resistively terminated artificial transmission lines. The image impedance is referred to as the characteristic impedance when a network is symmetrical or $Z_{i1} = Z_{i2}$.

2.4.4 Transistor Model

For this analysis the HBT device model of Figure 2.15 is used as a starting point.

Figure 2.15. The π model for the heterojunction bipolar transistor.

The model can be further simplified by assuming that R_O and R_μ are very large. Therefore, both R_O and R_μ have a negligible effect on the circuit and can be removed, which results in the new model seen in Figure 2.16.

Figure 2.16. A simplified π model for the heterojunction bipolar transistor.

Two further simplifications are employed (see Figure 2.17). Using Miller's Theorem, C_μ is split into $C_{\mu 1}$ and $C_{\mu 2}$; and to keep the value of capacitance constant over frequency a constant gain is assumed for the Miller capacitance. This, in turn, also means that the dis-

tributed amplifier also has a constant, or flat, gain in the passband. In Figure 2.17 C_T is the combination of C_π and $C_{\mu 1}$. Finally, R_B is removed to simplify the analysis.

Figure 2.17. A further simplified π model for the heterojunction bipolar transistor.

2.4.5 Artificial Transmission Lines

The distributed amplifier can be split into two segments: the input line and the output line which contains the gain elements. The network of Figure 2.18 uses constant- k T filter sections to create an artificial transmission line terminated with its characteristic impedance. The artificial transmission line is the input line of a distributed amplifier and, as such, has a voltage source as part of the left hand termination.

Figure 2.18. The input artificial transmission line of a distributed amplifier.

The output artificial transmission line of Figure 2.19 is terminated at both ends by its characteristic impedance. There are N gain stages, and unlike the input line, there are N input points where the signal is transmitted to the output line.

Figure 2.19. The output artificial transmission line of the distributed amplifier.

Both the input and output artificial transmission lines have an interstage propagation constant ψ_B and ψ_C , respectively.

2.4.6 Gain

To determine the voltage gain of the distributed amplifier we must first find a two-port network that has a port 2 image impedance equal to the following two-port network's port 1 image impedance or $Z_{i,2} = Z_{i_{n+1},1}$ (where n is used to identify the two-port network = 1, 2,..., etc) and is a fundamental repeatable unit of the artificial transmission line. Figure 2.20 depicts such a section which is commonly known as an L section.

Figure 2.20. A generic L section created by removing Y_1 from the π network of Figure 2.13.

The ABCD parameters for the L section in terms of Y parameters can be determined from (2.13) to (2.16):

$$A = 1 + \frac{Y_2}{Y_3}, \quad (2.31)$$

$$B = \frac{1}{Y_3}, \quad (2.32)$$

$$C = Y_2, \quad (2.33)$$

and

$$D = 1 \quad (2.34)$$

The voltage at any arbitrary node in the input line can be obtained by using the L section of Figure 2.21 and its corresponding two-port image impedance parameters.

Figure 2.21. Input line L section.

From (2.29) we have

$$V_{\pi x} = V_{in} \sqrt{\frac{Z_{i_B 2}}{Z_{i_B 1}}} e^{-(x-1/2)\psi_B} \quad (2.35)$$

where x is a number from 1 to N , and N is the number of gain stages. From Figure 2.19 the current for each gain stage can be expressed as:

$$I_x = -g_{mx} V_{\pi x} \quad (2.36)$$

The total current as seen at the output of Figure 2.19 can be expressed as:

$$I_{Z_C} = \frac{1}{2} e^{\frac{-\psi_C}{2}} \sum_{x=1}^N I_x e^{-(N-x)\psi_C} \quad (2.37)$$

Therefore, the output voltage is:

$$V_{out} = -\frac{Ng_m V_{in}}{2} Z_C \sqrt{\frac{Z_{i_B2}}{Z_{i_B1}}} e^{\frac{\psi_B - \psi_C}{2}} e^{-N\psi_C} \sum_{x=1}^N e^{x(\psi_C - \psi_B)} \quad (2.38)$$

where $\sum_{x=1}^N g_{mx}$ is replaced by Ng_m assuming $g_{m1} = g_{m2} \dots = g_{mN}$

The voltage gain can now be expressed as:

$$\frac{V_{out}}{V_{in}} = -\frac{Ng_m}{2} Z_C \sqrt{\frac{Z_{i_B2}}{Z_{i_B1}}} e^{\frac{\psi_B - \psi_C}{2}} e^{-N\psi_C} \sum_{x=1}^N e^{x(\psi_C - \psi_B)} \quad (2.39)$$

If we assume the input and output lines to be ideal and phase synchronized, then

$\psi = \psi_B = \psi_C$ and the voltage gain is now:

$$A_V = \frac{V_{out}}{V_{in}} = -\frac{Ng_m}{2} \sqrt{\frac{L_C}{C_{\mu2}}} \sqrt{\frac{Z_{i_B2}}{Z_{i_B1}}} e^{-N\psi} \quad (2.40)$$

where the characteristic impedance of the output line is: $Z_C = \sqrt{\frac{L_C}{C_{\mu2}}}$

Recall that power gain is defined as:

$$G = \frac{P_{out}}{P_{in}} = \frac{|I_{Z_C}|^2 Z_C}{\left| \frac{V_{in}}{Z_B} \right|^2 Z_B} \quad (2.41)$$

Therefore the power gain for the distributed amplifier is:

$$G = \frac{N^2 g_m^2 Z_{i_B2}}{4 Z_{i_B1}} e^{-2N\psi} \sqrt{\frac{L_C L_B}{C_{\mu2} C_T}} \quad (2.42)$$

From (2.31) to (2.34) and Figure 2.21 we can show that:

$$\frac{Z_{i_B2}}{Z_{i_B1}} = \left[\left(1 - \frac{\omega^2}{\omega_c^2} \right) + j \frac{\omega L_B}{4R_\pi} \right]^{-1} \quad (2.43)$$

where $\omega_c = \frac{2}{\sqrt{L_B C_T}}$

Therefore,

$$A_V = \frac{V_{out}}{V_{in}} = \frac{Ng_m}{2 \sqrt{\left(1 - \frac{\omega^2}{\omega_c^2} \right) + j \frac{\omega L_B}{4R_\pi}}} \sqrt{\frac{L_C}{C_{\mu2}}} e^{-N\psi} \quad (2.44)$$

and

$$G = \frac{N^2 g_m^2}{4 \left[\left(1 - \frac{\omega^2}{\omega_c^2} \right) + j \frac{\omega L_B}{4R_\pi} \right]} \sqrt{\frac{L_C L_B}{C_{\mu2} C_T}} e^{-2N\psi} \quad (2.45)$$

The derivations for voltage and power gain are valid only after a large set of assumptions:

- The output artificial transmission line is lossless and therefore uses ideal capacitors and inductors in the constant-k T sections. The input artificial transmission line is also assumed to be lossless except for the addition of R_π from the transistor model.
- A simplified hybrid- π transistor model is used that does not include all the capacitive and resistive elements present in the fabricated device.
- The feed-through properties of the HBT model due to C_μ and R_μ result in a coupling of the input and output artificial transmission lines. This coupling is not fully captured by the simplified hybrid- π transistor model.
- A constant gain is assumed to allow the use of Miller's Theorem.
- The frequency dependence of the constant-k T sections prevents the practical implementation of the terminations and are instead terminated resistively.
- The current sources are assumed to have a uniform excitation and are not phase synchronized to a wave propagating to one of the terminations.

2.4.7 Number of Stages

The above derivations for gain do not account for a practical limit on the number of gain stages. This practical limit occurs when the benefits of adding another gain stage to a distributed amplifier are outweighed by the losses introduced by the new stage. The optimum number of stages can be obtained by taking the derivative of the power gain equation for a distributed amplifier, equating the result to zero, and solving for N . The accuracy of this value is dependent on the inclusion of all sources of loss incurred in the design of the distributed amplifier. The optimal number of stages has been shown to be [11,12,13]:

$$N_{opt} = \frac{\ln(A_C/A_B)}{A_C - A_B} \quad (2.46)$$

where A_B and A_C represent the per stage input and output line attenuation.

It can be clearly seen from (2.46) that the optimal number of stages is limited only by the losses in the input and output lines. It is also clear that those losses increase in an exponential manner. The optimum number of stages may exceed ten, but for the III-V substrates it is widely accepted that little improvement is seen beyond eight stages [16,17]. The optimum number of stages may be significantly lower for lossy silicon substrates such as silicon.

2.4.8 Maximum Gain Bandwidth Product

In the III-V technologies there is an accepted limit to the maximum achievable gain bandwidth product. This limit was proposed by Beyer et al. for GaAs FET distributed amplifiers. The maximum possible bandwidth for a distributed amplifier is limited by f_{max} , the frequency where the maximum available power gain becomes unity. Beyer et al. observed that the maximum obtainable gain bandwidth product is approximately $0.8f_{max}$ [54]. This limitation assumes that the lowpass bandwidth of the amplifier is measured 1dB

down from the DC gain. Furthermore, according to Beyer et al. the maximum achievable bandwidth at unity gain is approximately $0.7f_{max}$. These bounds are typically applied to distributed amplifiers fabricated in the lossless III-V technologies but are less relevant for distributed amplifiers fabricated in lossy silicon substrates.

The CMOS and SiGe technologies have a silicon substrate that is significantly lossier than GaAs. The lossy substrate in circuit terms appears as a resistance and frequency-dependent capacitance that facilitates a substrate current and coupling between structures. This significantly reduces the quality factor of any passives, as well as increasing device parasitics. The parasitics present in a lossy substrate will limit the maximum achievable gain bandwidth product (GBW). As a result, the maximum GBW should be lower than that achieved in GaAs. In 2004 Amaya et al. observed that the maximum GBW for distributed amplifiers (measured at the unity gain frequency) in a bulk silicon substrate is approximately $0.55f_{max}$ [18]. This limit on the GBW was obtained by Amaya et al. via simulation, fabrication and test of a selection of distributed amplifier topologies. Although the study was thorough, it by no means was exhaustive as not all possible distributed topologies were tested. Therefore, the $0.55f_{max}$ limit to the bulk silicon GBW may be considered as an approximate upper limit that is subject to refinement as more distributed amplifiers are studied.

2.4.9 Summary

This chapter presented an analysis of some of the key points in the design of a distributed amplifier. The information presented in this chapter is intended to be used as a starting point for CAD simulation. Many aspects of the derivations have been simplified for this reason.

2.4 Literature Study and Figures of Merit

A literature study on some the latest advances in distributed amplification is presented in this chapter. The figures of merit used in distributed amplification are also discussed and a new one is proposed.

2.4.1 Recent Work in Distributed Amplification

Distributed amplification has been a popular research topic in the last few years. This short summary concentrates on the work done from 2002 to the present. The research papers assembled for this study were selected based on the following criteria:

- Papers from standard CMOS and SiGe processes
- Papers whose application is for the wireline and/or fibre broadband communications
- Papers for traditional distributed amplifiers.

Most of the published research work has focused on increasing the small-signal bandwidth and gain of silicon distributed amplifiers. However, distributed amplifiers are typically used to amplify signals in the data path and as such are large signal amplifiers.

The small signal S-parameters can be used to judge the large signal performance of the distributed amplifier by keeping in mind that small signal S-parameters are typically optimistic when compared to large signal S-parameters. Also, comparing the published gain bandwidth product to the maximum GBW available in the technology indicates whether the distributed amplifier has made the best use of topology and technology to maximise the small signal performance and therefore by inference the large signal performance.

Table 2.1 Specifications of recent distributed amplifier publications.

.Ref	Process	Gain (dB)	Gain Ripple or peaking (dB)	Single-Ended Output Swing (V_{p-p})	Jitter (ps)	Group Delay (ps)	-3 dB BW (GHz)/ unity gain BW (GHz)	S_{11} (dB)	S_{22} (dB)	Supply (V)	Power (mW)	Size (mm^2)	f_{max} (GHz)	f_T (GHz)
[19]	0.18 μ m CMOS	4	1.0	0.35	$\sim$ 8(p-p)	$\pm$ 15	39/39.5	-10	-10		140	1.1 x 3.0	100*	51*
[20]	0.18 μ m CMOS	10.6	$\pm$ 0.9				13.5/17.5	-11	-12	1.3	52	1.0 x 1.6		
[21]	0.18 μ m CMOS	7.3	$\pm$ 0.8				21.4/24	-8	-9	1.2	52	0.9 x 1.5	58*	70*
[22]	0.18 μ m BiCMOS (CMOS)	7.8	$\pm$ 1.3				25/27.14	-10	-10	1.8	54	1.0 x 1.3		
[23]	0.18 μ m CMOS	15	0				2/10	-7	-7	1.8, 1	56	0.4 x 0.8		
[24]	0.18 μ m CMOS	6	$\pm$ 1.0				26.94/27	-10	-10	3.3	68.1	1.8 x 0.9		
[25]	0.18 μ m CMOS	9.5	$\sim$ $\pm$ 2.0				32/38.06	-9	-10	2.2	97	0.94x0.86		
[26]	90nm CMOS	7	$\sim$ 10				70/80	-7	-12		122	0.9 x 0.8	142	160
[27]	0.6 μ m CMOS	6.5	$\pm$ 1.2				3.5/5	-7	-10	3.8	83.4	0.79x0.6		
[28]	0.6 μ m CMOS	5.5	$\pm$ 1.5				?/8.5	-9.5	-6	3.0	216	1.3x2.2		
[29]	0.18 μ m BiCMOS	7	$\pm$ 0.7				20.5/21.5	-8		3	132	1.8x1.0		
[30]	90nm CMOS	7.4	$\sim$ $\pm$ 2.0				80/98	-10	-8	2.4	120	1.2 x 0.6		
[31]	0.35 μ m BiCMOS (HBT)	10.5	$\sim$ $\pm$ 2.0			$\pm$ 10.5	41/46.25	$\sim$ -5	$\sim$ -12	5.3, 7.5	700	1.3 x 0.83	>90	80
[32]	0.18 μ m BiCMOS (HBT)	7.5	$\pm$ 0.5	0.15	1.5(RMS)	$\pm$ 8	22/25	$\sim$ -10	$\sim$ -15	3.3	100	1.0x0.9	100	120
[33]	SiGe on SOI (HBT)	6	$\sim$ $\pm$ 0.5				67/71	$\sim$ -2	$\sim$ -5	3.3	75.9	1.0x1.0	100	100
[33]	SiGe on SOI (HBT)	8	$\sim$ $\pm$ 0.5				62/77	$\sim$ -2	$\sim$ -5	3.3	75.9	1.0x1.0	100	100
[34]	SiGe (HBT)	21	$\pm$ 0.3	$\sim$ 0.4	1.5(RMS)	$\pm$ 5	37/50	-17	-15	5.2	1090	1.3x1.7	100	120
[34]	SiGe (HBT)	7	$\sim$ $\pm$ 3.0				81/84.62	$\sim$ -5	-20	5.5	495	1.3x0.9	>200	200
[35]	0.25 μ m BiCMOS (HBT)	11	$\pm$ 1.0				13/16.5	-12	-12	5.0	400	2.1	65.5*	41.5*
[36]	0.18 μ m CMOS	9	?				$\sim$ 7/27	-12	-8			0.4x1.0		
[37]	0.13 μ m CMOS	8.5	?			$\sim$ $\pm$ 5	$\sim$ 42/ $\sim$ 60	$\sim$ -10	$\sim$ -10			0.8x2.2		
[38]	0.13 μ m BiCMOS (HBT)	10	$\sim$ $\pm$ 5.0				110/>110	$\sim$ -5	$\sim$ -5	3	357	2.08x1.05		
[39]	0.18 μ m CMOS	16.2	$\pm$ 1.0	$\sim$ 0.3	$\sim$ 7.74(p-p)		33.4/37.5	-11	-12	2.8	260	1.28x1.8		
[39]	0.18 μ m CMOS	20	?	$\sim$ 0.2	$\sim$ 4.51(p-p)		39.4/42.5	-10	-20	2.8	250	1.6x1.4		
[40]	0.13 μ m CMOS	9.6	$\pm$ 1.0				43.9/44.6	-14	-18		103	0.6x2.5		
[41]	0.18 μ m CMOS	$\sim$ 10.5	$\sim$ $\pm$ 0.5				18.93/26.4	-16	-18	1.3	20.8	1.4x-0.85		

<i>.Ref</i>	<i>Process</i>	<i>Gain (dB)</i>	<i>Gain Ripple or peaking (dB)</i>	<i>Single-Ended Output Swing (V_{p-p})</i>	<i>Jitter (ps)</i>	<i>Group Delay (ps)</i>	<i>-3 dB BW (GHz)/ unity gain BW (GHz)</i>	<i>S₁₁ (dB)</i>	<i>S₂₂ (dB)</i>	<i>Supply (V)</i>	<i>Power (mW)</i>	<i>Size (mm²)</i>	<i>f_{max} (GHz)</i>	<i>f_T (GHz)</i>
This Work [42]	0.13μm BiCMOS (CMOS)	8.8	±1.0	1.2	3.64(RMS)		29.5/32.5	-10	-10	5	480	0.85x1	82.4*	95.6*
[43]	0.18μm BiCMOS (HBT)	7	±2.0			±10	>50/~52	-10	-15	5	125	1x1.1	100	120
[43]	0.18μm BiCMOS (HBT)	7.25	±1.25			±10	>50/~55	-10	-15	5	125	1x1.1	100	120
[44]	0.18μm CMOS	20.5				±25	35/~39	-8.4	-8.4	2.8	250	1.25x0.62		50
[45]	65nm CMOS	22	±3				65/~75	-10	~-8	1.3	97	1.58	200	160
[46]	0.13μm BiCMOS (HBT)	24.75	±1.75				>95/	~-20	~-5	3.3	247.5	1.05x0.62		200
[47]	0.13μm CMOS	13.2	±0.8				29.4/~37	-9	-9.5	1.5	136	1.5x0.8	130	90
[48]	90nm CMOS	15.4	~±0.5				~24/27.5	-6.5	-6.5		12.5	0.41		
[49]	0.13μm CMOS	9.6	±0.4				35/~46	-10	-10	1.2	18	0.5x1.2		85
[50]	0.18μm BiCMOS (HBT-CMOS)	8.2	±3				31/~47.3	> -10	> -10	4.9	181	1.3x0.58	85/86	72/43
[51]	0.18μm CMOS	20.5	±8			±25	35/~39	-8.4	-8.4	2.8	250	1.25x0.62		50
[51]	0.18μm CMOS	24	±6			±30	33/~38	-8	-8	2.8	238	1.22x0.68		50
[52]	0.13μm BiCMOS (HBT)	10	~±5.0			±18	110/114.2	~-5	~-5	3	357	2.08x1.05	270	200
[53]	65nm CMOS	22	±3				65/~75	-10	~-8	1.3	97	1.58	200	160

Note: The field in the table is left empty if no data is reported in the publication.

*: The reported f_T and f_{max} are not necessarily the maximum obtainable in the process, they can also be solely for the devices used in the distributed amplifier.

~: The parameter is not explicitly stated in the publication and is instead extrapolated from the Sparameter plot.

Upon looking at Table 2.1 it is immediately apparent that making an assessment as to the merits of one distributed amplifier over another is quite challenging, due to the amount of information and lack of a common reference point. A figure of merit can be used to reduce the volume of information by combining some of the data. The figure of merit also has the added benefit of creating a common reference point that easily allows the reader to assess the performance of one amplifier versus another. The gain bandwidth product is one such possible metric.

2.4.2 Figures of Merit

The gain bandwidth product (GBW) as most commonly used in distributed amplifier publications is a small-signal amplifier metric and can be defined as the 3dB bandwidth of the amplifier multiplied by the small-signal magnitude of the passband gain. There is a common problem that should be addressed at this point: it is not unheard of for the bandwidth used in this metric to be taken at the 1dB gain point or at unity gain. One needs to take care that a uniform frame of reference is used to properly make a comparison between amplifiers.

The GBW metric can be used to determine the trade-off between the gain and bandwidth of any given amplifier. For example:

If the passband voltage gain of the amplifier is 10dB
and the low pass 3dB frequency is 10GHz,
then the GBW is 31.62 GHz (recalling that the voltage magnitude is measured in
units of volt/volt).

This amplifier can have a bandwidth of 31.62GHz at unity gain or a gain of 30dB but with a bandwidth of 1 GHz. The obvious conclusion is that a larger gain bandwidth product is more desirable because of the larger available gain or bandwidth options that can be

achieved by the amplifier (i.e., replace the previous example with a GBW of 100GHz or 500 GHz). It is also obvious that the practical limits of the amplifier are not included in the GBW . It is well known that amplifier gain is limited by the conservation of energy (2.47), assuming the power added efficiency is 100%.

$$P_{out} - P_{in} = P_{DC} \quad (2.47)$$

This limitation places a bound on how much gain can be achieved by the amplifier. In other words, a GBW of 500 GHz does not necessarily mean that the amplifier can have a gain of 53.98 dB and a bandwidth of 1 GHz. The gain of the amplifier is further limited by the potential linearity requirements of the amplifier (assuming the need for a linear amplifier response) which would place a bound on the maximum allowable input and output power.

The GBW is further limited by the achievable bandwidth of the devices used in the amplifier. The maximum achievable device bandwidth is limited by the f_{max} and f_T of the technology. The device size, current density and number of fingers as well as the parasitics in the interconnect and passive structures may further limit the achievable bandwidth.

Finally, the gain roll-off after the cut-off frequency is not accounted for at all. If the amplifier has a single pole then the gain roll-off can be assumed to be 20dB per decade, however a distributed amplifier is a multi-pole system which may have gain peaking that increases the rate of attenuation after the cut-off (the resonant arm of the m-derived T filter section can be used to achieve this). Therefore, the unity gain frequency is not at all predictable by using the GBW alone.

Given these limitations on the gain and bandwidth of the amplifier, it makes sense to have a new modified gain bandwidth product ($MGBW$) that in some way includes these practical bounds. A single commonly reported metric must be chosen to apply to the GBW since, it is not possible to ensure that publications include all the aforementioned limits. The metric chosen is f_{max} because it is a technology dependant metric that is often

reported or can be easily ascertained from the foundry. Furthermore, the gain bandwidth product for silicon substrates can be expressed as a percentage of the maximum achievable gain bandwidth product - recalling that CMOS and SiGe technologies have a lossy silicon substrate that results in a maximum achievable GBW of approximately $0.55f_{max}$ [18]. Therefore,

$$MGBW = \frac{GBW}{0.55f_{max}} \quad (2.48)$$

In effect the $MGBW$ gives us a measure of how well the distributed amplifier makes use of the available GBW for a specific process or technology node. $MGBW$ is a unity gain metric since, the maximum achievable GBW is measured at unity gain. Therefore, the GBW of the distributed amplifier used in the $MGBW$ metric is also the unity gain frequency of the distributed amplifier.

In broadband wireline and fibre optic communication systems distributed amplifiers are most often used to transmit data. The distributed amplifier is uniquely suited to this task because of its broad bandwidth and large output swing. Although the GBW and $MGBW$ are small signal metrics they can be used to approximate the large signal performance with the caveat that the large signal performance of the distributed amplifier is typically worse than the small signal metric indicate. Therefore a more accurate measure of the large signal performance is needed.

A useful measure of the large-signal performance of an amplifier is the output eye diagram. The eye is a measure of signal distortion. In other words, the output eye diagram of the distributed amplifier is a measure of linearity, gain distortion, duty cycle distortion, inter-symbol interference, jitter, etc. These undesired elements of the output data close the eye diagram making individual symbols harder to detect. Unfortunately, the large-signal performance of a distributed amplifier is rarely presented in publications from refereed journals and conference proceedings. Instead, they generally give the small-signal perfor-

mance in terms of S parameters. Even though the S parameters are not a large-signal representation of the amplifier, some information can be extrapolated that applies to the large-signal performance.

From the S parameter matrix (assuming a two-port matrix, since most distributed amplifier publications are for single-ended amplifiers) the S_{21} is a measure of the forward gain of the amplifier. The gain may exhibit a ripple in the passband and/or peaking. If we assume data is being transmitted as a square wave, then the fundamental tone as well as the 2nd and 3rd harmonics are of concern. Given that data (a collection of 1s and 0s in virtually any combination and word length) may have a fundamental tone that may appear anywhere from nearly DC onwards, the flatness of the gain then impacts the shape of the square wave. In other words, any gain ripple or peaking in the passband can distort the square wave. Distorting the square wave will make it more difficult to identify the data (1 or 0) and close the eye diagram. Any passband ripple or peaking in the S_{21} will also be present in the large-signal gain but not necessarily with the same magnitude or periodicity. Therefore, although a flat small-signal passband gain does not guarantee a flat large-signal gain, the small-signal ripple or peaking can be used as a possible indicator of distortion in the large-signal gain.

The forward gain of the amplifier has a phase component as well as a magnitude. The phase of the forward gain can be used to calculate the group delay of the amplifier. Group delay is a measure of the frequency-dependent delay. Any variation in the group delay will distort the data by moving the fundamental and harmonics away from each other in time. This creates a sort of smearing effect that results in inter-symbol interference and jitter, both of which result in eye closure. Therefore, the small-signal group delay can be used as another indicator of a large-signal performance.

The input and output impedance of the distributed amplifier is most often terminated with passive elements. Typically, since the amplifier is required to have a large pass-

band, the termination for the transmission lines are resistive in nature but may also have some inductance to deal with the parasitics of the termination. The characteristic impedance of the input/output transmission lines are dominated by the passives of the line (inductors, capacitors and their parasitics) if the number of gain stages in the distributed amplifier is sufficiently large or the gain stages themselves are small. Otherwise, the bias-dependent device parasitics have a larger impact on the characteristic impedance of the line. With regards to the input and output match, S_{11} and S_{22} respectively, the small-signal metric will provide an increasingly inaccurate measure of the large-signal match as the device parasitics become a larger portion of the artificial transmission line. However, the pole and zero locations as well as the magnitude of the input/output match, as shown by S_{11} and S_{22} , are an indicator of the large-signal performance in that they show the general trends and shape of the waveforms. As such, the S_{11} and S_{22} can provide a reasonable measure of the ability of the amplifier to deliver maximum power to the load and receive incoming power with minimum power reflected (with the caveat that large-signal absolute values for S_{11} and S_{22} cannot be obtained by using small-signal metrics).

Both the GBW and $MGBW$ metrics are used to sort Table 2.1 since, not all publications listed the foundry or the f_T and f_{max} of the technology used to fabricate the designs. Using the GBW and $MGBW$ to sort the publications in Table 2.1 allows us to generate a new table (see Table 2.2) which can be used to select a few high-performing distributed amplifiers to review. It is also of interest to note that only one publication exceeds the estimated $0.55f_{max}$ limit to the unity gain GBW and only by a small fraction. However, this result is not enough to warrant a change to the $0.55f_{max}$ limit (the updated limit would be $0.56f_{max}$) as a single data point is not sufficient to make a meaningful conclusion.

2.4.3 Distributed Amplifier Literature Summary

Table 2.2 The gain bandwidth product and the modified gain bandwidth product for the publications presented in Table 2.1

<i>.Ref</i>	<i>GBW (GHz) at unity gain</i>	<i>MGBW</i>
[19]	39.5	0.72
[20]	17.5	
[21]	24	0.75
[22]	27.14	
[23]	10	
[24]	27	
[25]	38.06	
[26]	80	1.02
[27]	5	
[28]	8.5	
[29]	21.5	
[30]	98	
[31]	46.25	0.93
[32]	25	0.46
[33]	71	0.89*
[33]	77	0.96*
[34]	50	0.91
[34]	84.62	0.77
[35]	16.5	0.46
[36]	27	
[37]	~60	
[38]	>110	
[39]	37.5	
[39]	42.5	
[40]	44.6	
[41]	26.4	
This work [42]	32.5	0.72
[43]	~52	0.95
[43]	~55	1.0
[44]	~39	
[45]	~75	0.68
[46]	>95	
[47]	~37	0.52
[48]	~27.5	
[49]	~46	
[50]	~47.3	1.01/1
[51]	~39	
[51]	~38	
[52]	~114.2	0.77
[53]	~75	0.68

Notes:

*: The MGBW for the SOI substrate is calculated using the metric developed by Beyer et al. [54]

~: The parameter is not explicitly stated in the publication and is instead extrapolated from the Sparameter plot.

From Table 2.2, the following three publications have been chosen for a more detailed analysis:

Reference [26]: This publication presents a cascaded multi-stage distributed amplifier in a 90 nm CMOS process. The bandwidth is extended by using two cascaded DAs where the output transmission line of the first two-stage DA is the input transmission line of the second two-stage DA. The transmission lines are implemented as coplanar waveguides to reduce substrate losses in the design. The first distributed amplifier uses a single device gain stage while the second DA uses a cascoded gain stage. The small-signal gain at low frequency is nearly 20 dB but then degrades by approximately 10 dB before a sharp roll-off down to a -3 dB bandwidth of 70 GHz. There is no reported large-signal broadband performance nor is the group delay mentioned.

Figure 2.22. Schematic of the cascaded multi-stage distributed amplifier from reference [26]

Reference [34]: There are three broadband amplifiers presented in this publication, two of which are distributed amplifiers. There are also two SiGe processes used, the first has an $f_T = 120$ GHz and an $f_{max} = 100$ GHz, while the second process has f_T and f_{max} greater than 200 GHz. The first distributed amplifier is a five-stage differential design using coplanar waveguides for the input and output transmission lines. Each gain stage is composed of two gain elements connected together via an emitter-follower. The amplifier shows very good small-signal performance up to a -3 dB frequency of 37 GHz. The reported group delay variation of ± 5 ps up to 34 GHz. The 40 Gbps large-signal data is equally good with a maximum output swing of 850 mV_{p-p} differential.

The second distributed amplifier is also a five-stage differential design where the gain stage is composed of an emitter-follower and cascode amplifier. Although it is not explicitly mentioned, it appears that the transmission lines are of a coplanar design (from the photo micrograph). This design has a much larger -3 dB bandwidth of 81 GHz but significantly more passband ripple. The input/output return loss is better than -16 dB and -20 dB respectively, but is only given up to 50 GHz. There is no large-signal performance given nor is the group delay mentioned.

Figure 2.23. Schematic of the distributed amplifiers for reference [34]

Reference [38]: An eight-stage scaled distributed amplifier in SiGe is presented in this publication. The gain stage is a cascode amplifier with emitter degeneration and capacitive peaking. To improve the efficiency of the distributed amplifier, the devices in the gain stage are scaled by a factor of k (from stage to stage) and the output transmission line is tapered to gradually increase the characteristic impedance of the line. The transmission lines are implemented as microstrip lines. The DA has a -3 dB bandwidth of 110 GHz and the passband input/output reflection coefficients are below -10 dB up to approximately 40 GHz. The large signal -3 dB bandwidth is given as 77 GHz, but appears to have been determined by measuring the 1 dB compression point at various frequencies. The power added efficiency (PAE) is shown to be 20% better than other published results for distributed amplifiers. No other large-signal information is given.

Figure 2.24. Schematic of the stage-scaled distributed power amplifier for reference [38]

2.5 Summary

In this chapter, the key points in the design of a simple distributed amplifier are presented and the theory shown can be used to design a distributed amplifier with any gain

stage and artificial transmission line. This theory is a necessary first step in understanding how to improve the large-signal performance of a distributed amplifier.

A new figure of merit is also presented, the modified gain bandwidth product (MGBW), which can be used as a means of determining the performance achieved by a distributed amplifier independent of the technology used. This allows the reader to compare the amplifier to other designs to better understand the merits of the chosen topology and design.

Chapter 3: Device Breakdown and Linearity

In this chapter, a brief introduction on device breakdown for the Heterojunction Bipolar Transistor and the CMOS MOSFET are presented and the possibility of operating beyond the breakdown voltage is explored. This chapter will also briefly present the impact on the speed and linearity of the transistors when operating beyond, and extending, the breakdown.

3.1 Operation in the Breakdown Region of a Heterojunction Bipolar Transistor

The characteristics and operation of a transistor depend on its bias conditions. The transistor or device has operational boundaries (limitations on bias conditions) that may cause a performance drop and electrical or thermal instability when ignored. Operation under these conditions often leads to failure of the device or a reduced life span. One such boundary condition is the operational voltage limit. This limit is often determined by the avalanche characteristics of the device and is known as the *avalanche breakdown*.

The following section will explore the breakdown of the more common single-transistor configurations and, more specifically, their associated breakdown voltages will be presented.

3.1.1 The Common Emitter Breakdown Voltage

Figure 3.1. Common emitter forced I_B configuration

First we will consider the common emitter forced I_B configuration of Figure 3.1, which grounds the emitter terminal and supplies a constant current to the base of the device. This configuration is considered the worst for breakdown voltages, and results in the lowest breakdown voltage BV_{CEO} .

The mechanism of avalanche breakdown for the common emitter configuration is due to hole-electron pair generation from electrons injected into the base-collector region. The holes move towards the base (while the electrons move towards the collector) where they either exit through the base contact (not the case with forced I_B) or combine with electrons from the emitter. The re-combination with electrons from the emitter leads to a larger injection of electrons into the emitter, which means a larger emitter current. This increase in electrons facilitates a continued increase in electron-hole generation and thus an even larger emitter current. This cycle continues until the device goes into breakdown.

Figure 3.2. The I-V curves for the common emitter forced I_B configuration showing the operational limits for the device.

We can see from Figure 3.2 that the breakdown voltage is quite low and not constant for all bias conditions (this topic is expanded upon later in this chapter). Therefore, low breakdown voltage and the inability of the avalanche current to exit the base (which is the cause of the low breakdown voltage) makes the common emitter forced I_B configuration an undesirable device bias condition for anything other than device characterization.

Figure 3.3. Common emitter forced V_{BE} configuration.

On the other hand, the common emitter forced V_{BE} configuration in Figure 3.3 allows the avalanche current to escape and thus extends the breakdown voltage beyond the common emitter forced I_B breakdown voltage and is referred to as BV_{CEOR} . This configuration is commonly used for amplifier design because of its superior device stability under different load conditions. The stability is primarily due to a large output impedance and a smaller input impedance.

The number of holes exiting the base of the device versus those that recombine with electrons from the emitter are dependent on the external base impedance of the device. The lower base impedance of the common emitter configuration allows more holes to exit which results in a larger breakdown voltage, as can be seen in Figure 3.4.

Figure 3.4. The I-V curves for the common emitter forced V_{BE} configuration showing the operational limits for the device.

BV_{CEOR} is the base impedance dependent common emitter forced V_{BE} collector-emitter breakdown voltage. BV_{CEO} or the common emitter forced I_B collector-emitter breakdown voltage is a special case of BV_{CEOR} . When the base impedance is very large, or effectively infinite as is the case for the Common emitter forced I_B configuration, then BV_{CEOR} becomes BV_{CEO} .

An expression for the collector-emitter breakdown voltage BV_{CEOR} can be defined as follows:

From [55] we know that for a junction diode the reverse current near the breakdown voltage I_{RA} is defined as

$$I_{RA} = MI_R \quad (3.1)$$

where I_R is the reverse bias current of the diode and the multiplication factor M is

$$M = \frac{1}{1 - \left(\frac{V_R}{BV}\right)^n} \quad (3.2)$$

where BV represents the breakdown voltage, V_R is the reverse bias on the diode and n is defined as a value between 3 and 6.

So, for a bipolar transistor biased in the active region (or with base-emitter junction forward biased and the base-collector junction reverse biased) (3.1) becomes

$$I_C = MI_{C0} \quad (3.3)$$

where I_{C0} is the pre-avalanche breakdown collector current and M is now

$$M = \frac{1}{1 - \left(\frac{V_{CB}}{BV_{CBO}}\right)^n} \quad (3.4)$$

where V_{CB} is the collector-base voltage and BV_{CBO} is the collector-base breakdown voltage with the device in the common-base, open circuited emitter configuration.

The holes that exit through the base contact act to reduce the total base current by a factor of $M - 1$ [56]. The base current can then be expressed as

$$\begin{aligned} I_B &= I_{B0} - (M - 1)I_{C0} \\ &= \frac{I_{C0}}{\beta} - (M - 1)I_{C0} \end{aligned} \quad (3.5)$$

The collector-emitter breakdown voltage limit BV_{CEO} is reached when the avalanche base current leaving the base contact equals the base current entering the contact. Therefore, setting (3.5) to 0 yields

$$M = \frac{\beta + 1}{\beta} \quad (3.6)$$

and with (3.4) we can re-write (3.6) as:

$$V_{CB} = \frac{BV_{CBO}}{n\sqrt{\beta + 1}} \quad (3.7)$$

We know that $V_{CE} = V_{CB} + V_{BE}$ so we can now re-write (3.7) to obtain an expression for the collector-emitter breakdown voltage as follows:

$$BV_{CEOR} = V_{BE} + \frac{BV_{CBO}}{n\sqrt{\beta + 1}} \quad (3.8)$$

From (3.8) we can see that the collector-emitter breakdown voltage is the BV_{CBO} multiplied by the feedback multiplication factor of the current gain. It can also be seen that $BV_{CEOR} < BV_{CBO}$. The inclusion of the base-emitter voltage in (3.8) indicates that BV_{CEOR} has some dependence on the device bias. This is confirmed in Figure 3.2 and Figure 3.4 where BV_{CEO} and BV_{CEOR} changes with increasing current density.

There are several steps that can be taken to extend the common-emitter breakdown voltage. According to [56] the base current of the device can be made positive by increasing the base emitter bias. This occurs because the hole diffusion current across the base-emitter junction increases as the base emitter bias is increased so that I_{BO} is larger than $(M - 1)I_{CO}$. Also, the avalanche multiplication rate decreases at higher V_{BE} because it reduces the electric field of the collector-base depletion region. There is also an advantage to be had by having a large V_{CB} . If the collector-base voltage is very large, I_B goes posi-

tive due to the voltage drop over the collector and base parasitic resistances, device self-heating and electric field lowering in the base-collector junction due to the presence of mobile carriers.

However, we can see from Figure 3.4 that the common-emitter forced V_{BE} device, although having a larger overall breakdown voltage than the common-emitter forced I_B configuration, exhibits a reduction in collector-emitter breakdown voltage as the current density increases. This reduction in BV_{CEOR} occurs because, unlike the forced I_B configuration, the base current can go negative which then de-biases the device and reduces the breakdown voltage.

3.1.2 The Collector Base Breakdown Voltage

Figure 3.5. Common-base forced I_E configuration.

The final device configuration that will be discussed is the common-base forced I_E configuration, as seen in Figure 3.5. Since this configuration has a fixed collector/emitter current, the holes generated by the avalanche mechanism exit the device rather than

recombine to increase the emitter current. This allows the collector-base voltage to increase beyond any of the other configurations breakdown voltages resulting in the device's largest breakdown voltage BV_{CBO} , as seen in Figure 3.6. The base no longer controls the collector current once the device goes into breakdown and, although the mechanism itself is not destructive, the rapidly increasing current density results in a large rise in temperature which can damage the device. In effect, The collector-base junction will begin to breakdown as V_{CB} approaches BV_{CBO} [55,56,57]. Therefore, the collector-base breakdown voltage is a hard device limit under all bias/ load configurations.

Figure 3.6. The I-V curves for the common-base forced I_E configuration showing the operational limits for the device.

Interestingly, if the V_{CE} in Figure 3.6 continues to increase beyond 4 volts a performance degradation known as emitter collapse will occur and is brought about by device

overheating. In effect, emitter collapse occurs when one finger of the device is hotter than the others and therefore conducts more current and continues to get hotter and conducts more current. The collapse is because one finger conducts most of the current and thus decreases the device gain (until avalanche breakdown dominates the collector current, at which point the current experiences an exponential rise). A collapse is reversible, but repeated occurrences will damage the device (bjt thermal runaway is similar but not reversible and current gain does not drop, but increases with temperature) [56].

3.1.3 Summary

The avalanche multiplication has a strong dependence on the collector current density. Therefore, the device breakdown voltage has a strong dependence on the bias of the device and large V_{BE} and V_{CB} can change the BV_{CEOR} beyond what (3.8) depicts. H. Veenstra et. al. [57] has shown that (3.8) is valid for small to moderate values of V_{CB} and V_{BE} , and that the extrinsic base and collector resistances, as well as the Kirk effect (essentially a barrier for current flow into the collector), will cause BV_{CEOR} to deviate slightly from the expected.

An increase in breakdown voltage, although desirable, can come with a thermal penalty due to higher bias voltages and current densities that may/will degrade device performance and lifetime if not properly accounted for. Another point to consider is that BV_{CEOR} is not a hard limit for device operation. In fact, operation beyond the collector-emitter breakdown voltage does not result in damage to the device (assuming no other factors are involved) and therefore BV_{CEOR} can be described as the point where a performance degradation is incurred. All that is required is a means of managing any base current exiting through the device (i.e. the avalanche base current is larger than the input base current) since this current will alter the bias conditions of the device and reduce the breakdown voltage.

3.2 Breakdown in MOSFET Transistors

Oxide breakdown is one of the limiting factors when using CMOS MOSFETS in large voltage swing amplifiers. The scaling down of device sizes for increased density and speed has also resulted in a thinning of the gate oxide which results in a lower breakdown voltage.

3.2.1 Oxide Breakdown.

Figure 3.7. MOSFET cross-section.

Figure 3.7 is a simplified cross-section of a MOSFET. Gate oxide breakdown occurs when the gate-to-substrate or gate-to-drain/source voltage exceeds some voltage limit. This limit, beyond which the MOSFET gate oxide begins to breakdown can be referred to as the gate-to-substrate or gate-to-drain/source breakdown voltage, BV_{GDSS} [58].

Figure 3.8. Defects formed in the gate oxide of a MOSFET during a breakdown event.

The breakdown event occurs as follows: first a bias is applied to the gate such that the gate-to-source/drain or gate-to-substrate voltage exceeds BV_{GDS} . Figure 3.8 shows the formation of gate oxide defects due to a breakdown event. Repeated breakdown events will form a conduction path as seen in Figure 3.9. This conduction path allows current to flow. This small defect area has a high electric field and a high temperature due to the current concentration. This combination causes the phosphorus, which is present to improve conductivity in the gate, to further diffuse into the silicon bulk resulting in a diffusion contact [58].

Figure 3.9. A defect conduction path formed in the gate oxide of a MOSFET.

A breakdown event results in permanent damage by creating a path for current leakage. In fact, multiple breakdown events will increase the leakage current until the device ceases to function [59]. There is evidence that transistor parameters and other performance metrics, such as threshold voltage, electron mobility, gain, noise figure, input-referred 3rd-order intercept point, etc. are all adversely affected by a single breakdown event, let alone several events [60],[61].

3.2.2 Punch Through

At high drain/source bias voltages, lower than BV_{GDSS} , a phenomena known as *punch through* can occur. Punch through occurs when depletion layers around the drain and source merge into a single depletion region. This causes a rapid rise in drain current dependent on the drain source voltage. The punch through event generates holes that flow to the oxide and increase the gate current until breakdown occurs [62].

3.2.3 Avalanche Breakdown

At higher gate bias voltages avalanche breakdown can occur in the channel. This is the same mechanism described earlier in Section 3.1 for a pn junction. Also, there is a parasitic bipolar transistor between the source and drain that allows avalanche-generated holes to travel from drain to source. Finally, this mechanism forward biases a source-to-bulk diode which then allows electrons to flow to the drain where they recombine with holes (avalanche multiplication) to again increase the drain current. This rapidly increasing drain current causes the oxide to breakdown at an earlier voltage bias than would normally occur [63].

3.2.4 Summary

It is clear from Section 3.2.1 that any breakdown event in a MOSFET transistor is undesirable. A soft breakdown generates a leakage path through the gate oxide but may

still leave the transistor in a functional state. Repeated soft breakdown events will eventually destroy the transistor. A hard breakdown, on the other hand, immediately destroys the transistor.

A hard breakdown event occurs when the BV_{GDSS} limit is greatly exceeded and can result in the silicon melting in the breakdown region. However, soft breakdown events occur when the BV_{GDSS} limit is reached or marginally surpassed. A soft breakdown increases the devices leakage current and degrades its performance but does not destroy the device. The amount of performance degradation is also dependant on the breakdown location [58, 61]. Operation in soft breakdown is possible with the understanding that the device lifetime will be reduced and the performance of the device will be degraded.

It is also important to note that, oxide breakdown is further affected by avalanche breakdown and punch through which reduce the breakdown voltage BV_{GDSS} below the expected for the oxide breakdown (Section 3.2.1) which in turn increases the back-off required to operate the device safely.

There are a few options available to extend the breakdown voltage: thicker oxides and longer gate lengths will increase the breakdown voltage but also reduce the speed of the device. Another option is to shorten the channel width. Shorter widths have been shown to increase the breakdown voltage-this is because the breakdown voltage is somewhat dependent on the substrate resistance. It's important to note that the increase in breakdown voltage is reduced at smaller gate lengths [64].

The various foundries are reducing device sizes (length) and gate oxide thicknesses to improve speed and device density. The corresponding problem for amplifier designers is that the increased speed also comes with trade-offs, such as reduced breakdown voltages. One option that foundries are exploring is to replace the silicon dioxide

with other high dielectric-constant materials. These materials can be thicker and thus have a larger breakdown voltage, yet have the desired capacitance.

3.3 Device Speed and Linearity

The parasitics of a transistor limit the device's ability to operate at high frequency. Those same parasitics also impact the linearity of a device. If Silicon is to compete with the III-V technologies as a viable alternative for distributed amplification then the device must be able to provide large output voltage swings but still retain a linear broadband gain.

3.3.1 Transit Frequency and the Maximum Frequency of Oscillation in a HBT

Both the transit frequency (f_T) and the maximum frequency of oscillation (f_{max}) are device bandwidth metrics. The transistor transit frequency is usually measured with the device in the common emitter configuration as in Figure 3.3 and occurs when the short circuit current gain equals unity. Whereas f_{max} occurs when the maximum available power gain equals unity.

Figure 3.10. Simplified hybrid π bipolar transistor model.

The small signal model of the bipolar transistor of Figure 3.10, and the schematic of the common emitter connected transistor of Figure 3.3 can be used to obtain expressions for both f_T and f_{max} as follows:

The current flowing through C_μ can be neglected assuming that at the frequencies of interest $gm \gg sC_\mu$, where $s = j\omega$. Therefore, the collector or output current is:

$$i_C = gmV_\pi \quad (3.9)$$

To simplify the derivation the parasitic emitter and collector series resistances are assumed to be small and can be omitted from the small signal model of Figure 3.10. Therefore, the collector and emitter can be considered to be shorted together, recalling that V_{CC} from Figure 3.3. is considered AC ground. This allows us to obtain a simplified expression for V_π :

$$V_\pi = \frac{R_\pi}{1 + R_\pi(C_\pi + C_\mu)s} i_B \quad (3.10)$$

Then substituting (3.10) in (3.9) we get an expression for the current gain as follows:

$$\frac{i_C}{i_B} = \frac{gm \cdot R_\pi}{1 + R_\pi(C_\pi + C_\mu)s} \quad (3.11)$$

At high frequency the imaginary portion of (3.11) dominates the denominator and the current gain can be simplified to:

$$\beta = \frac{gm}{(C_\pi + C_\mu)s} \quad (3.12)$$

f_T occurs at unity current gain or when $\beta = 1$ and s can be expressed as $j\omega$, where $\omega = 2\pi f$. Therefore, an expression for f_T is:

$$f_T = \frac{gm}{2\pi(C_\pi + C_\mu)} \quad (3.13)$$

Using Figure 3.10 an expression for f_{max} can be obtained as follows:

The input impedance is

$$R_B + \frac{R_\pi}{1 + R_\pi(C_\pi + C_\mu)s} \quad (3.14)$$

and at high frequency (3.14) can be simplified to

$$R_B + \frac{1}{(C_\pi + C_\mu)s} \quad (3.15)$$

The frequency f_{max} is obtained when the maximum power is transferred to the device and load. This occurs when the input and output of the device are perfectly matched. Therefore the imaginary portion of the input impedance can be removed. The input impedance, Z_i , can then be further simplified to

$$Z_i = R_B \quad (3.16)$$

Therefore, the input power is

$$P_{in} = \frac{V_i^2}{Z_i} = \frac{v_B^2}{R_B} \quad (3.17)$$

where v_B is the small signal base voltage

An expression for V_π in terms of v_B can be obtained by means of a voltage divider and some simplification can occur by using the fact that the denominator of $R_\pi \parallel C_\mu s \parallel C_\pi s$ is dominated by its imaginary portion. Therefore, a simplified expression for V_π is

$$V_\pi = \frac{v_B}{R_B(C_\mu + C_\pi)s} \quad (3.18)$$

The output current expression is obtained by substituting (3.18) into (3.9):

$$i_C = \frac{g_m v_B}{R_B(C_\mu + C_\pi)s} \quad (3.19)$$

The assumption previously made was that some current flows through the Miller capacitance and, as such, the impact of C_μ cannot be ignored when calculating the output impedance. Attaching a voltage source at the output (V_{added}) between the collector and emitter, leaving the input between the base and emitter as an open circuit and using a voltage divider to obtain V_π with respect to this new source gives

$$V_\pi = \frac{V_{added} C_\mu}{C_\pi + C_\mu} \quad (3.20)$$

Therefore, the output impedance can be determined using (3.18), (3.19), and (3.20) as

$$Z_o = \frac{V_{added}}{i_C} = \frac{C_\pi + C_\mu}{g_m C_\mu} \quad (3.21)$$

The frequency f_{max} is calculated with maximum power delivered to the load. So, the output power can be shown to be

$$P_{out} = \frac{1}{4} i_C^2 Z_o = \frac{1}{4} \frac{g_m^2 v_B^2}{R_B^2 C_\mu (C_\pi + C_\mu) s} \quad (3.22)$$

Therefore, the power gain is

$$\frac{P_{out}}{P_{in}} = \frac{1}{4} \frac{g_m}{R_B C_\mu (C_\mu + C_\pi) s^2} \quad (3.23)$$

The frequency f_{max} occurs at unity power gain and remembering that s can be expressed as $j\omega$ leads to the following expression for f_{max} :

$$f_{max} = \sqrt{\frac{g_m}{16\pi^2 R_B C_\mu (C_\pi + C_\mu)}} \quad (3.24)$$

It is clear from (3.13) and (3.24) that f_T and f_{max} are both dependant on C_μ and C_π . These model capacitances represent actual physical junction and depletion capacitances. C_μ is the base-collector junction capacitance (C_{jBC}), while C_π is composed of two capacitances, the base-emitter depletion capacitance (C_{BE}), and the base-emitter junction capacitance (C_{jBE}). Each of these capacitances is impacted by the bias conditions of the device as can be easily seen from (3.25), (3.26) and (3.27) [55].

$$C_{jBC} = \frac{C_{jBCo}}{\sqrt{1 - \frac{V_{BC}}{\Psi_{BC}}}} \quad (3.25)$$

$$C_{jBE} = \frac{C_{jBEo}}{\sqrt{1 - \frac{V_{BE}}{\Psi_{BE}}}} \quad (3.26)$$

$$C_{BE} = \tau_B \frac{I_E}{V_T} \quad (3.27)$$

where Ψ_{BC} and Ψ_{BE} are the built-in junction potentials, C_{jBCo} and C_{jBEo} are the junction capacitances at zero bias voltage, τ_B is the base transit time and the thermal voltage of a p-n junction $V_T = 26$ mV at 300 degrees Kelvin.

In section 3.1.1 the bipolar transistor breakdown voltages and some of the concerns involved in operation beyond the collector-emitter breakdown were presented, as well as some of the means by which the breakdown voltage can be extended. To increase BV_{CEO} it is desirable to have a high V_{BE} and/or high V_{CB} as well as a higher emitter current density. However, the increase in breakdown voltage is minimal for the forced I_B configuration and the increased current density is not desirable for the forced V_{BE} configuration, as can be seen from Figure 3.4, where the higher current density results in a lower BV_{CEOR} .

Operating an HBT device at peak f_T and f_{max} requires a high emitter current density, which, in turn, reduces the BV_{CEOR} of the amplifier. Further increasing the current density to enhance the gain of the device not only reduces the breakdown voltage but also

results in larger junction and depletion capacitances (dependent on forward or reverse bias of the pn junction), which, in turn, results in smaller values of f_T and f_{max} .

Figure 3.11. Percentage change in BV_{CEOR} by operating below peak f_T

In other words, to maximize a device's BV_{CEOR} so as to maximize the output voltage swing, the emitter current density must be backed-off from the peak f_T current. Figure 3.11 show the percentage change in a typical HBT BV_{CEOR} as a function of back-off from peak f_T . It can be seen that the potential increase in breakdown voltage by operating the HBT device below peak f_T is approximately 5% for a 10% back-off from peak f_T and reducing the peak f_T by 60% increases the breakdown voltage by 8%. It is clear that the increase in breakdown voltage is not linear and rapidly becomes less advantageous for larger than a 20% back-off from the peak f_T current and although the increase in break-

down voltage is less than 10%, it still represents a potential increase in the low hundreds of millivolts.

3.3.2 Linearity of the Bipolar Device

Another important metric for a transistor is the device linearity or the ability of the device to respond linearly to a given stimulus. A measure of device linearity is to see when the output power of the device compresses by 1dB from the ideal linear output power for a given frequency. The point where this occurs is referred to as the 1 dB compression point.

The 1 dB compression point occurs because the output of the device is not simply the gain of the device multiplied by the input signal- the transistor generates harmonic and intermodulated tones that cause the output to be non-linear. A power series expansion with two input tones can be used to illustrate the non-linear impact of the device [65, 66].

$$V_{out} = A_o + A_1 V_{in} + A_2 V_{in}^2 + A_3 V_{in}^3 + \dots \quad (3.28)$$

where A_0 , A_1 , A_2 , and A_3 are the power series coefficients.

Substituting $V_{in} = V_1 \cos 2\pi f_1 t + V_2 \cos 2\pi f_2 t$ into (3.28) will generate terms corresponding to the even and odd order harmonics of the two tones (2nd, 3rd, 4th, etc.), and combinations of the two frequencies such as $f_1 \pm f_2$, $f_2 \pm f_1$, $2f_1 - f_2$, and $2f_2 - f_1$. The last two terms in the list are referred to as the 3rd-order intermodulation terms. The intermodulation terms (3rd-order and above) are the most responsible for the non-linear behaviour because they are close in frequency to the input tones and least likely to be filtered out. These tones generate the gain compression and harmonic distortion that limits the linear range of the device.

The device gain compression is not completely represented by the simplified power gain equation of (3.23). The linearity of a transistor is most impacted by the base-emitter junction capacitance. The intermodulation decreases with rising base-emitter junction capacitance until a minimum is reached at which point the linearity decreases (or intermodulation increases) with increasing capacitance. It is also worthy to note that the base-collector junction capacitance and the transconductance also have an impact on the linearity (but to a lesser degree) [56, 67].

3.3.3 Transit Frequency and the Maximum Frequency of Oscillation in a MOSFET

Figure 3.12. Simplified hybrid π MOSFET model.

As in the bipolar transistor, the f_T and f_{max} of a MOSFET transistor are important speed-related metrics. The simplified small-signal model of Figure 3.12 can be used to derive equations for these metrics. The derivation is very similar to that of the bipolar transistor, noting that Figure 3.12 is very similar to Figure 3.10, so it can be shown that

$$f_T = \frac{g_m}{2\pi(C_{GS} + C_{GD} + C_{GB})} \quad (3.29)$$

and

$$f_{max} = \sqrt{\frac{g_m}{16\pi^2 R_G C_{GD} (C_{GS} + C_{GD} + C_{GB})}} \quad (3.30)$$

In the saturation region of operation both C_{GB} and C_{GD} become much smaller than C_{GS} . Therefore the equations for f_T and f_{max} can be simplified to [55]

$$f_T = \frac{g_m}{2\pi C_{GS}} \quad (3.31)$$

and

$$f_{max} = \sqrt{\frac{g_m}{16\pi^2 R_G C_{GD} C_{GS}}} \quad (3.32)$$

The gate to channel capacitance is represented by C_{GD} and C_{GS} . In the saturation region of operation the channel is tapered and pinched-off at the drain which significantly reduces C_{GD} 's contribution to the gate-to-channel capacitance. In saturation, C_{GD} is typically a few femto farads and due mostly to the drain to gate overlap. Therefore the bulk of the charge stored in the channel is represented by C_{GS} . The gate-to-source capacitance also has an overlap capacitance component that can be ignored since its contribution to C_{GS} is typically much smaller than the channels contribution. C_{GS} can then be approximated as follows [55]

$$C_{GS} = \frac{2}{3} W_{ch} L_{ch} C_{ox} \quad (3.33)$$

where W_{ch} and L_{ch} are the width and length of the channel, respectively, and C_{ox} is the oxide capacitance given by

$$C_{ox} = \frac{\epsilon_{ox}}{T_{ox}} \quad (3.34)$$

where T_{ox} is the thickness of the oxide and ϵ_{ox} is the permittivity of the oxide.

As in the bipolar case, the capacitance in the denominator of (3.31) and (3.32) have a large impact on the performance of the device. Thinner oxides will increase the capacitance, but device scaling has also implemented a reduction in the width of the oxide to result in a net increase in the unity gain frequency and the maximum frequency of oscillation. One drawback of the device scaling is a lowering of the breakdown voltage of the device due to the smaller oxide layer.

3.3.4 Linearity of the MOSFET Device

As in the bipolar device the linearity can be described by a power series expansion. The series expansion leads to expressions for the input-referred 1 dB compression point and the input-referred 3rd-order intercept point. These expressions can then be mapped to device parameters and bias values [68].

$$P_{1dB} = \frac{\left(1 + \frac{\mu_1 V_{on}}{2v_{sat}L_{ch}}\right)^4}{2R_s \left(\frac{\mu_1}{2v_{sat}L_{ch}}\right)^2 \left[V_{on} \left(1 + \frac{\mu_1 V_{on}}{4v_{sat}L_{ch}}\right) + \frac{6.88v_{sat}L_{ch}}{\mu_1 \left(1 + \frac{\mu_1 V_{on}}{2v_{sat}L_{ch}}\right)^2} \right]} \quad (3.35)$$

and

$$P_{IIP3} = \frac{8}{3} \frac{v_{sat}L_{ch}}{\mu_1 R_s} V_{on} \left(1 + \frac{\mu_1 V_{on}}{4v_{sat}L_{ch}}\right) \left(1 + \frac{\mu_1 V_{on}}{2v_{sat}L_{ch}}\right)^2 \quad (3.36)$$

where $V_{on} = V_{GS} - V_{Th}$, v_{sat} is the saturation velocity, $\mu_1 = \mu_o + 2\theta v_{sat} L_{ch}$, and, assuming maximum power transfer, $R_s = R_G$.

It can be seen in (3.35) and (3.36), that the linearity of a MOSFET is independent of C_{ox} and the width of the device. Furthermore, the linearity of the device can be improved with increasing the V_{GS} bias and the length of the device.

3.4 Summary

For the HBT device, increasing the base-emitter junction capacitance of the transistor will increase the linearity (up to a point and then it begins to decrease) but it will also reduce f_T and f_{max} . Increasing V_{BE} as per (3.26) will also increase the breakdown voltage (from Section 3.1). However, the increase in current density that accompanies an increasing V_{BE} (assuming a forced V_{BE} configuration) will act to reduce the breakdown voltage. Therefore, to maximize the breakdown voltage it is advantageous to operate well below peak f_T current which can result in an increase to BV_{CEOR} by as much as 8%. So, there exists a potential trade off between extending the breakdown voltage, maximizing f_T, f_{max} and increasing the linearity of the device.

Operation beyond the breakdown voltage BV_{CEO} is possible without damaging the device (see Section 3.1). An option is therefore available to the circuit designer - bias the device for the best linearity and accept the resulting breakdown voltage and speed with the caveat that operation beyond BV_{CEO} is possible and that there are existing methods to increase f_T if necessary.

With regards to the MOSFET transistor - operation beyond the breakdown voltage is only possible in the soft breakdown region of operation and not a viable option beyond that voltage (hard breakdown).

From Section 3.3.4, it can be seen that some optimization of the MOSFET linearity is possible by choosing the appropriate device length and bias voltage. On the other hand, this optimization may result in a reduction of f_T and f_{max} .

Chapter 4: Distributed Amplifier Design

In Chapter 2 the theory necessary to design a distributed amplifier is presented. The theory is a starting point for the designs presented in this chapter.

4.1 Design Specifications

The distributed amplifiers presented in this chapter are intended for a 40 Gbps data rate fibre optic communication system. The following specifications are of a general nature since specific fibre optic system requirements are kept confidential. The specifications are as follows:

- Input and output reflection coefficients (S_{11} and S_{22}) better than -10 dB for the entire passband to minimize the amplitude of the reflected waves
- Input voltage swing is at the high end of standard CML voltage levels, approximately 400 mV single-ended peak-to-peak. This level was chosen to provide as large a signal as reasonably possible to the distributed amplifier.
- The output voltage swing should be at least 1 volt single-ended peak-to-peak to function as a pre-driver for an EOM and 2 volts for a driver of a low voltage EOM. Which corresponds to a voltage gain of 7.96 dB to 13.98 dB for a 400 mV peak-to-peak input signal.
- The 3 dB passband must be from as close to DC as possible (limited by the termination capacitors to the MHz range) to a minimum upper frequency of 20 GHz for 40 Gbps data rates
- The group delay of the distributed amplifier should show as little variation as possible in the passband of the amplifier

4.2 The Distributed Amplifier Topologies

The ST BiCMOS9 [69] process is an ideal choice for this work as it provides access to both a SiGe (f_T of 166 GHz and an f_{max} of 175 GHz) and a 0.13 μm CMOS node. The ability to design into both a CMOS and HBT technology node gives a better overview of the potential for these technologie(s) to integrate the distributed amplifier with the data converter circuitry (DAC/ADC) as well as the DSP.

The distributed amplifier specifications are challenging and during the design phase it is important to have as many tunable variables as possible to make meeting those specifications easier. However, a balance should be maintained between design tunability and overly complicating the design. A good starting point is choosing the transmission line type that will be used in the distributed amplifier. Recall from Chapter 2 that an artificial transmission line is composed of filter sections that can be individually optimized. Also, an analysis of several types of filter sections are presented in Chapter 2 and the m-derived filter section is shown to have the most options for tunability. Therefore, artificial transmission lines as the input/output transmission line topology are a good choice for the distributed amplifier designs. The next step is choosing the gain stage device(s) and topology.

In the ST BiCMOS9 process the MOSFET and high-speed HBT breakdown voltages, BV_{GDSS} and BV_{CEO} are below 1.5 and 2 volts respectively [69]. In Chapter 3 the general conclusion for a MOSFET device is that it is better to operate below the breakdown voltage to avoid damaging the device and incurring a performance degradation. However, the HBT device does not suffer permanent damage from operating slightly beyond the breakdown region and only requires a means of dealing with the base current exiting the device. With a single device gain stage it is not possible to achieve the minimum 1 volt output swings and the more desirable 2 volt swings with a MOSFET device

and is at the border of operation for the HBT device (even with the possibility of operating beyond the breakdown voltage as there is an associated reduction in linearity).

The breakdown limitation of a single device gain stage on the output voltage swing of a distributed amplifier can be easily demonstrated. Using the methodology presented in Chapter 2, a five-stage distributed amplifier with a single MOSFET device gain stage can be developed (Figure 4.1). The simulated S-parameters and group delay are in Figure 4.2 and Figure 4.3 respectively. Figure 4.4, Figure 4.5 and Figure 4.6 are the output eye diagrams of the distributed amplifier for a 11, 22 and 40 Gbps pseudo-random binary sequence (prbs) input signal. This distributed amplifier can also be used as a baseline to determine the potential performance improvement of the proposed distributed amplifiers.

Figure 4.1. A CMOS single-ended five-stage distributed amplifier using a single device gain stage.

Figure 4.2. Simulated S-parameters for the CMOS single-ended five-stage distributed amplifier of Figure 4.1.

Figure 4.3. Simulated group delay for the CMOS single-ended five-stage distributed amplifier of Figure 4.1.

Figure 4.4. Simulated 11 Gbps output eye for the CMOS single-ended five-stage distributed amplifier with a 700 mV 2^7 -1 prbs input to the test bench resulting in a 350 mV input prbs to the distributed amplifier of Figure 4.1.

Figure 4.5. Simulated 22 Gbps output eye for the CMOS single-ended five-stage distributed amplifier with a 700 mV 2^7 -1 prbs input to the test bench resulting in a 350 mV input prbs to the distributed amplifier of Figure 4.1.

Figure 4.6. Simulated 40 Gbps output eye for the CMOS single-ended five-stage distributed amplifier with a 700 mV 2^7 -1 prbs input to the test bench resulting in a 350 mV input prbs to the distributed amplifier of Figure 4.1.

Table 4.1 Summary for the simulated small signal S-parameters, group delay and power consumption of Figure 4.2 and Figure 4.3.

Gain (dB)	$S_{11} \leq -10$ dB (GHz)	$S_{22} \leq -10$ dB (GHz)	Passband S_{12} (dB)	Group Delay (ps)	-3 dB BW (GHz)	P_{DC} (mW)
6.04 ± 0.63	25.66	27.45	≤ -8.79	31.45 ± 7.74	41.97	21.11

Table 4.2 Summary for the 11 Gbps simulated output eye of Figure 4.4.

Eye height (mV)	Eye width (ps)	Jitter _{p-p} (ps)	Voltage _{p-p} (mV)
788.4	88.6	2.31	914.7

Table 4.3 Summary for the 22 Gbps simulated output eye of Figure 4.5.

Eye Height (mV)	Eye width (ps)	Jitter _{p-p} (ps)	Voltage _{p-p} (mV)
786	44.3	1.1	828

Table 4.4 Summary for the 40 Gbps simulated output eye of Figure 4.6.

Eye Height (mV)	Eye width (ps)	Jitter _{p-p} (ps)	Voltage _{p-p} (mV)
750.3	23.2	1.79	994.6

The distributed amplifier of Figure 4.1 was designed to have as much output swing and bandwidth as possible without exceeding the catastrophic breakdown voltage limitations. From Table 4.2, Table 4.3 and Table 4.4 it is immediately apparent that the single device gain stage cannot provide the necessary 1 volt minimum peak-to-peak output swing at 11 Gbps or 22 Gbps let alone 40 Gbps. Also, the simulated output swing is larger than would be expected from the fabricated distributed amplifier as the simulation does not include all the parasitic elements of the design. However, the small signal parameters in Table 4.1 indicate that there is more than sufficient bandwidth (keeping in mind that the small signal S-parameters can only be used as an indication of the large signal performance) and therefore the potential exists for a more complex gain stage that may trade bandwidth for gain as well as extend the breakdown voltage. Substituting a SiGe HBT single device gain stage in the distributed amplifier of Figure 4.1. would result in output voltage swings over a volt but still limited by the single device breakdown (recall that operation beyond the breakdown voltage in an HBT is possible but comes with a reduction in linearity) that can be easily extended with a more complex topology to achieve a 2 volt or more peak-to-peak output swing.

Figure 4.7. Common source amplifier with cascode transistors.

A possible solution for operation beyond the single device breakdown is to series stack or cascode devices. Transistor stacking allows the supply voltage to be raised because the output voltage swing is now distributed across multiple devices. The breakdown voltage BV_{GDSS} (in the case of Figure 4.7) in effect becomes nBV_{GDSS} where n is the number of stacked transistors, likewise V_{DD} is now nV_{DD} . However, the maximum supply voltage is still limited to the device to bulk breakdown voltage of a single transistor and the increased parasitics incurred by having multiple stacked devices would reduce the available bandwidth [70].

Figure 4.8. (a) Schematic of a common-emitter amplifier, (b) schematic of a common-emitter common-base cascode amplifier.

The circuits of Figure 4.8 can be used to demonstrate the improvement in output swing and linearity that can be achieved by stacking transistors. The input power is swept from -30 dBm to 10 dBm for a 1 GHz input frequency. The 1 dB compression point is simulated assuming a 50 Ohm input/output load. All the transistors have the same biasing and are biased well below the breakdown voltage.

Figure 4.9. Common-emitter amplifier 1 dB compression point at 1 GHz

Figure 4.10. Common-emitter common-base (cascode) 1 dB compression point at 1 GHz

Comparing Figure 4.9 to Figure 4.10 we see an improvement of 2.71 dB to the 1 dB compression point which translates to the difference between an output of 1.08 V peak-to-peak for the cascode to 795 mV peak-to-peak for the common-emitter amplifier (as expected it is very similar to the maximum output swing of Figure 4.1). It's important to note at this point that operation up to the 1 dB compression point results in about 10% distortion due to intermodulation components [72]. The 1 dB compression point is further complicated for distributed amplifiers in the data path because the input signal contains frequency components from DC (limited by terminations to the MHz range) to the maximum frequency, 20 GHz for the case of a 40 Gbps signal and potentially higher if all harmonics are to be considered.

For the designs presented in this chapter a single cascode transistor should be sufficient to increase the output to the minimum voltage swing specified in section 4.1 and in the case of the HBT transistor operating at or beyond the breakdown voltage will provide the 2 volt swings that make it possible for the HBT distributed amplifier to operate as a driver for an EOM. However, the bandwidth and gain of the devices may not be sufficient to meet specifications due to the parasitic elements in the gain stage and passive elements. As such a more complex gain stage than the common source/emitter amplifier and cascode transistor may be advantageous.

Figure 4.11. HBT cascode f_T doubler.

Figure 4.12. HBT cascode f_T doubler 1 dB compression point at 1 GHz

A possibly topology that addresses the potential bandwidth and gain concerns of the distributed amplifier gain stage is the f_T doubler (see Figure 4.11) which can provide an improved bandwidth, yet still be combined with a cascode to increase the breakdown voltage [73, 74]. A further benefit is the increase in linearity that the f_T doubler gain stage can provide when compared to the common-emitter or common-emitter common-base configurations.

It can be seen from Figure 4.12 that the input referred 1 dB compression point has improved when compared to Figure 4.9 and Figure 4.10. The input peak-to-peak voltage has increased to over 600mV and the output voltage is now over 1.2V peak-to-peak. The cascode f_T doubler configuration of Figure 4.11 was biased well below breakdown so it is possible that with some optimization a much larger output voltage swing can be obtained.

There are three distributed amplifier designs are analyzed in this chapter. Two of the design use the f_T doubler gain stage: Figure 4.13, a CMOS single-ended five-stage cascoded f_T doubler distributed amplifier and; Figure 4.14, a HBT single-ended three-stage cascoded f_T doubler distributed amplifier. The third design is intended to function as a broadband high-speed differential to single-ended converter and is an HBT three-stage cascode differential to single-ended distributed amplifier (see Figure 4.15).

Figure 4.13. CMOS single-ended five-stage cascoded f_T doubler distributed amplifier.

Figure 4.14. HBT single-ended three-stage cascoded f_T doubler distributed amplifier.

Figure 4.15. HBT three-stage cascode differential to single-ended distributed amplifier.

Although each of the three distributed amplifiers use the same type of artificial transmission lines, the gain stages utilize either a different topology or a different device type. The devices, HBT or MOSFET, bring different characteristics and performance capabilities to the distributed amplifiers, as do the differential structures of Figure 4.15.

4.2.1 CMOS MOSFET f_T Doubler

Figure 4.16. Schematic for the single-ended CMOS f_T doubler.

The five-stage CMOS distributed amplifier (Figure 4.13) uses a cascoded f_T doubler gain stage. The f_T doubler of Figure 4.16 is a modification of the Darlington pair configuration. The Darlington pair has a higher current gain than just a single transistor and, with the addition of the diode-connected device, a higher f_T as well. The gain stage has an increased f_T because at low frequencies, the current of the f_T doubler is twice that of a single device and assuming that the effective capacitance remains the same, the result is a doubling of the f_T . However, the inclusion of the various device parasitics that impact the high frequency performance will degrade the improvement in f_T that the f_T doubler provides. The transit frequency for the f_T doubler from the high-frequency equivalent model of Figure 4.17 can be derived as follows:

Figure 4.17. High-frequency equivalent model for the f_T doubler.

The simplified equivalent model for the f_T doubler of Figure 4.17 assumes the following:

- The bulk is grounded and the parasitic capacitances (C_{GB} , C_{DB} , C_{SB}) to the bulk are small and can be ignored.
- The output resistance R_o is very large and can be ignored.
- The gate resistance R_G and the gate-to-drain capacitance C_{GD} are ignored to simplify the equations.

From Figure 4.17 the input impedance of the f_T doubler is

$$Z_{in} = \frac{2gm + 3C_{GS} \cdot s}{C_{GS} \cdot s(gm + 2C_{GS} \cdot s)} \quad (4.1)$$

where $s = j\omega$ and $\omega = 2\pi f$

Equation (4.1) and all the subsequent equations for the f_T derivation assume the transconductances $gm_1 = gm_2 = gm_3 = gm$ and capacitances $C_{GS1} = C_{GS2} = C_{GS3} = C_{GS}$.

It can be shown that the output current i_o of the f_T doubler is

$$i_o = gmZ_{in}i \quad (4.2)$$

where the current source i is applied to the input of the circuit in Figure 4.17 (and referenced to ground) solely for the purposes of determining the current gain. An expression for the current gain can be found by substituting (4.1) into (4.2) and rearranging (4.2). The current gain is therefore

$$\left| \frac{i_o}{i} \right| = \frac{gm}{C_{GS} \cdot s} \left(\frac{2gm + 3(C_{GS} \cdot s)}{gm + 2(C_{GS} \cdot s)} \right) \quad (4.3)$$

Recalling that f_T of a single MOSFET is $f_T \approx \frac{gm}{2\pi C_{GS}}$ allows for (4.3) to be re-written as follows:

$$\left| \frac{i_o}{i} \right| = \frac{2\pi f_T}{s} \left(\frac{2 + 3\frac{s}{2\pi f_T}}{1 + 2\frac{s}{2\pi f_T}} \right) \quad (4.4)$$

The transit frequency of the f_T doubler can be found by setting the current gain equal to 1 or $\left| \frac{i_o}{i} \right| = 1$. Therefore, setting (4.4) equal to 1 and rearranging results in the following polynomial:

$$\frac{s^4}{4\pi^2 f_T^2} - 2s^2 - 4\pi^2 f_T^2 = 0 \quad (4.5)$$

The quadratic equation $ax^2 + bx + c = 0$ can be rearranged to solve for x ,

$$x = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} \text{ therefore the root of (4.5) is found to be:}$$

$$|s^2| \approx 9.66\pi^2 f_T^2 \quad (4.6)$$

Recall that $s = j2\pi f$, where f in this case is the unity current gain frequency of the f_T doubler. Solving for f gives us

$$f \approx 1.55f_T \quad (4.7)$$

The f_T doubler circuit does not provide a doubling of the transit frequency, (4.7) clearly shows only a 55% increase in f_T from what a single CMOS device would achieve. The reduced f_T is due to the increased capacitance of the f_T doubler when compared to a single device which can be easily seen from an inspection of Figure 4.17 and (4.3). It is also important to note that the various resistive and capacitive parasitics that were ignored in the derivation of (4.7), if included, would further reduce the f_T of the doubler.

The increase in f_T also results in a increase in the maximum available power gain. As previously stated, f_{max} occurs when the maximum available power gain equals unity.

$$\text{Recall that } f_{max} \text{ for a MOSFET is } f_{max} = \sqrt{\frac{g_m}{16\pi^2 R_G C_{GD} C_{GS}}} \text{ which can be re-written as}$$

$$f_{max} = \sqrt{\frac{f_T}{8\pi R_G C_{GD}}} \quad (4.8)$$

As previously stated the f_T doubler has a larger current gain when compared to a single transistor. Unfortunately, the increase in current gain does not result in a corresponding increase in voltage gain; assuming all the MOSFETS are of equal size. If, on the other hand the transconductance of the three devices making up the f_T doubler are not equal, then there exists a potential trade-off between gain and bandwidth.

Figure 4.18. Simplified schematic for the single-ended CMOS f_T doubler with resistive load.

The circuit of Figure 4.16 can be further simplified by realizing that the device Q_2 is in effect a resistor whose value is $1/gm_2$. Therefore, Figure 4.18 can be substituted for

Figure 4.16 and will be used to derive the voltage gain of the f_T doubler. Figure 4.16 also gives us a new visual insight into the operation of this circuit. In effect the f_T doubler is a source follower or unity gain stage followed by a common-source amplification stage. Connecting the two drains of the amplifiers together allows both amplifiers to directly contribute current to the output of the circuit. Another advantage of the f_T doubler is for a given load and current the devices in the f_T doubler can be smaller than a single transistor amplifier to achieve this same gain and thus reduce the gain stage input capacitance.

Using the T equivalent model for the devices in the f_T doubler, and ignoring the high frequency components, allows us to create a new simplified model (see Figure 4.19) to derive the DC or low frequency voltage gain of the f_T doubler.

Figure 4.19. Low-frequency or DC equivalent model for the f_T doubler of Figure 4.18.

An expression for the voltage V_{GS3} is

$$V_{GS3} = \frac{gm_1}{gm_2} V_{GS1} \quad (4.9)$$

V_{GS1} can be obtained by applying a voltage V_{in} at the input G of the f_T doubler in Figure 4.19 and can be expressed as follows:

$$V_{GS1} = \frac{V_{in}}{1 + \frac{gm_1}{gm_2}} \quad (4.10)$$

The voltage gain or voltage across the load resistor R_L divided by the input voltage is therefore:

$$\frac{V_o}{V_{in}} = \frac{gm_1(gm_2 + gm_3)R_L}{gm_1 + gm_2} \quad (4.11)$$

It is advantageous to have $gm_1 = gm_2 = gm$ so that the source follower and its resistor track across process and temperature as closely as possible with minimum mismatch. It is also of benefit to keep the two devices (Q_1 and Q_2) as small as possible to minimize the input capacitance of the f_T doubler. With the aforementioned changes (4.11) becomes

$$\frac{V_o}{V_{in}} = \frac{1}{2}(gm + gm_3)R_L \quad (4.12)$$

It is clear from (4.12) that gm_3 must be at least equal to gm so as to maintain the same gain as an equivalent single transistor amplifier. It is equally clear that a larger transcon-

ductance will increase the gain of the f_T doubler. So, let $gm_3 = gm + gm'$, where gm' represents an increase in transconductance beyond gm . The gain of the f_T doubler is now

$$\frac{V_o}{V_{in}} = gmR_L + \frac{1}{2}gm'R_L \quad (4.13)$$

For a given current and load any increase in gm_3 will increase the voltage gain of the f_T doubler, but at a rate of 50% of said increase and as the device Q3 gets larger it will also increase the capacitive parasitics, which in turn will reduce the f_T of the overall circuit.

Given that $gm = gm_1 = gm_2 \neq gm_3$ then (4.7) is now

$$f = \left(\sqrt{\frac{9f_{T3}^2}{8f_T^2} - \frac{1}{8}} + \frac{1}{8} \sqrt{81\frac{f_{T3}^4}{f_T^4} + 46\frac{f_{T3}^2}{f_T^2} + 1} \right) f_T \quad (4.14)$$

When $f_{T3} = f_T$ then the ratio of f_{T3} to f_T is 1 and (4.14) is equal to (4.7), but when device Q3 of the f_T doubler is made larger to increase the gain the ratio of f_{T3} to f_T becomes less than 1 and consequently the transit frequency of the f_T doubler is reduced (assuming the bias conditions are kept constant). The f_T doubler has the potential to increase the voltage gain over and above what a single transistor amplifier can provide at the expense of the bandwidth of the circuit. Also, reducing the size of Q1 and Q2 and increasing the size of Q3 (to offset the reduced transconductance of Q1 and Q2) has the added benefit of reducing the input parasitics when compared to a single device with equivalent gm.

However, with regards to a large output voltage swing the Q3 transistor represents a weak point. Stacking Q1 and Q2 allows for a larger output voltage swing, since the output voltage is spread across both transistors. On the other hand the same output voltage is across Q3 which forces the output voltage to remain under the breakdown voltage of a sin-

gle MOSFET device. The obvious answer, as discussed earlier is to add a cascode device to the gain stage.

4.2.2 Topology of the CMOS Gain Stage

Figure 4.20. Cascode gain stage used in the CMOS distributed amplifier.

A cascode design was chosen (as seen in Figure 4.20) for the individual gain cells of the distributed amplifier. The cascode transistor isolates the f_T doubler output capacitance from the output of the gain stage. Consequently, it also improves the isolation between the input and output artificial transmission lines. This isolation is brought about by the fact that the cascode transistor acts as a load or current buffer. It supplies a small

load resistance that reduces the Miller effect of C_{GD1} and C_{GD2} . Also, the common base configuration of the cascode transistor has the added benefit of removing the Miller effect of C_{GD4} . This removal and reduction of the Miller effect for the CMOS gain stage also increases the upper frequency limit of the gain cell by reducing its output capacitance. The trade-off for the improvements is the added pole and the reduction in output voltage swing for a given supply voltage. However, the supply voltage can be significantly increased because the stacking (or cascoding) of the devices splits the drain to source voltage between the cascode and f_T doubler circuits. The caveat is, that the individual breakdown voltages must still be respected (including the drain and source to bulk breakdown voltage which puts an upper limit on the supply voltage).

Figure 4.21. Simplified high-frequency equivalent model for the f_T doubler.

Based on the analysis thus far, the f_T doubler equivalent model of Figure 4.17 can be further simplified as is depicted in Figure 4.21, where Z_{in} is defined by (4.1) and $Gm = gm + \frac{1}{2}gm'$ as per (4.13). For simplicity, it is assumed that the bulk of the gate to drain capacitance of device Q3 appears across its drain and source. An equivalent model for the cascode gain stage of Figure 4.20 can now be generated (see Figure 4.22).

Figure 4.22. High frequency equivalent model for the cascode gain stage used in the CMOS distributed amplifier.

From the simplified cascode model of Figure 4.22 (ignoring capacitance) it can be shown that

$$V_{GS4} = -GmV_{in} \frac{1}{gm_4} \quad (4.15)$$

and the output voltage is:

$$V_{out} = gm_4 V_{GS4} R \quad (4.16)$$

Therefore, the DC gain of the cascode configuration is GmR , where R is the arbitrary resistive load of the amplifier and Gm is the gain of the f_T doubler.

Figure 4.23. The output artificial transmission line.

Figure 4.24. The input artificial transmission line.

In Chapter 2, the power and voltage gain equations for a simple distributed amplifier utilizing a common-emitter transistor for the gain stage are presented. The equations presented in Chapter 2 can be reused since the derivations remain largely the same. The input/output impedance contributed by the gain stage is the only difference and is dependent on the chosen architecture for the gain stage. In the case of the cascoded f_T doubler of Figure 4.20 the output impedance is due only to C_{GD4} as seen in Figure 4.23. Likewise, the input impedance has also changed (see Figure 4.24) from what is presented in Chapter 2. The impedance seen by the input artificial transmission line is derived from Figure 4.22 and (4.1) and is

$$Z_{in}^I = \left(\frac{C_{GS} \cdot s(gm + 2C_{GS} \cdot s)}{2gm + 3C_{GS} \cdot s} + C_{GD1}^I \cdot s \right)^{-1} \quad (4.17)$$

where C_{GD1} is split into C_{GD1}^I and C_{GD1}^{II} via Miller's Theorem.

Therefore, the new distributed amplifier gain and power equations can be derived starting with (2.40). The voltage gain is

$$A_V = -\frac{NGm}{2} Z_D \sqrt{\frac{Z_{iG2}}{Z_{iG1}}} e^{-N\Psi} \quad (4.18)$$

where the characteristic impedance of the output artificial transmission line is

$Z_D = \sqrt{\frac{L_D}{C_{GD4}}}$. The ratio of the output image impedance over the input image impedance

of the input artificial transmission line is

$$\frac{Z_{iG2}}{Z_{iG1}} = \left(1 + \frac{1}{4} L_G C_{GS} \cdot s^2 \left(\frac{gm + 2C_{GS} \cdot s}{2gm + 3C_{GS} \cdot s} \right) + L_G C_{GD1}^I \cdot s^2 \right)^{-1} \quad (4.19)$$

if it is assumed that $\frac{gm + 2C_{GS} \cdot s}{2gm + 3C_{GS} \cdot s} \approx \frac{1}{2}$ then the square root of (4.19) can be shown to be

$$\sqrt{\frac{Z_{iG2}}{Z_{iG1}}} \approx \sqrt{\left(1 - \frac{\omega^2}{\omega_c^2} \right)^{-1}} \quad (4.20)$$

where $\omega_c = \frac{2}{\sqrt{L_G C_G}}$ and $C_G = \frac{C_{GS}}{2} + C_{GD1}^I$. Therefore, the voltage gain is now

$$A_V = -\frac{NGm}{2\sqrt{1 - \frac{\omega^2}{\omega_c^2}}} Z_D \cdot e^{-N\psi} \quad (4.21)$$

and the power gain is

$$G = \frac{N^2 Gm^2}{4\left(1 - \frac{\omega^2}{\omega_c^2}\right)} Z_G Z_D \cdot e^{-2N\psi} \quad (4.22)$$

where Z_G is the characteristic impedance of the input artificial transmission line.

4.2.3 The HBT f_T Doubler Gain Stage

Figure 4.25. HBT f_T doubler.

The equations derived for the CMOS cascode f_T doubler gain stage can also be similarly derived for an HBT implementation of the f_T doubler seen in Figure 4.25 as follows.

Figure 4.26. High-frequency equivalent model for the HBT f_T doubler.

If $gm_1 = gm_2$ then the f_T of the circuit in Figure 4.26 can be shown to be the same as (4.7) or $f \approx 1.55f_T$ of a single device with the same caveat as before. In other words, the actual f_T will be less than the calculated f_T due to the parasitics that have been ignored or simplified out of the derivation. Unlike the MOSFET device, the HBT transconductance is not dependent on the length and width of the transistor. In fact, the gm of the HBT is dependent on the collector current and so there is no gain benefit from having a larger gm_3 . So if $gm_1 = gm_2 = gm_3 = gm$ then the input impedance can be similarly derived as in (4.17) and after some simplification can be shown to be

$$Z_{in}^I \approx \left(\frac{1}{2rR_{\pi}} + C_{\mu 1}^I \cdot s \right)^{-1} \quad (4.23)$$

Therefore, the square root of the ratio of the output image impedance over the input image impedance of the input artificial transmission line is

$$\sqrt{\frac{Z_{i_B2}}{Z_{i_B1}}} = \sqrt{\left(1 - \frac{\omega^2}{\omega_c^2} + j\frac{L_B\omega}{8R_\pi}\right)^{-1}} \quad (4.24)$$

The cascode output impedance is the diffusion and depletion capacitance of the base-collector junction of the cascode transistor or $C_{\mu4}$ of the Q4 transistor. Therefore, using (4.24), the voltage and power gain equations are

$$A_V = \frac{Ng_m}{2\sqrt{\left(1 - \frac{\omega^2}{\omega_c^2} + j\frac{\omega L_B}{8R_\pi}\right)}} Z_C e^{-N\psi} \quad (4.25)$$

and

$$G = \frac{N^2 g_m^2}{4\left[\left(1 - \frac{\omega^2}{\omega_c^2} + j\frac{\omega L_B}{8R_\pi}\right)\right]} Z_C Z_B e^{-2N\psi} \quad (4.26)$$

Although the HBT device has a better f_T and gm than an equivalently sized MOSFET device, the trade off is the input impedance. It is clear from (4.25) and (4.26) that the resistive loss of the HBT will impact the input artificial transmission line limiting the optimal number N of gain stages (as per Chapter 2).

4.2.4 The HBT Gain Stage

Figure 4.27. HBT cascode differential pair gain stage.

The final gain stage is the HBT cascode differential pair seen in Figure 4.27 and used in the three-stage cascode differential to single-ended distributed amplifier. The gain stage is designed to take a differential input but produce a single-ended output. The configuration was chosen because the input signal to the distributed amplifier in the transmit stage is typically from a current mode logic (CML) cell and therefore differential, but EOMs that drive the optical fibre are typically single-ended (although it is interesting to note that there is work being done in differential EOMs). The distributed amplifier provides an opportunity to transition from a differential signal to a single-ended one (noting

that high-speed broadband differential to single-ended converters are most commonly implemented as a differential pair with one end terminated locally).

The single-ended output of the differential amplifier suffers from poor noise immunity when compared to a fully differential output due to the lack of the complementary signal. Furthermore, the differential gain stage's ability to suppress the second harmonic is also compromised. The analysis and operation of the differential cascode gain stage depends on the virtual grounds between the base contacts of the cascode transistors and the emitter contacts of the differential pair. The virtual grounds are adversely affected by the local resistive termination. This termination is designed to match the characteristic impedance of the output artificial transmission line as well as the loading effect presented by the other gain stages. The virtual ground remains a virtual ground at low frequencies but begins to degrade as the frequencies increase and the characteristic impedance of the artificial transmission line changes (recalling that the characteristic impedance is frequency dependent) with respect to the resistively-terminated branch.

Figure 4.28. Half circuit of the cascode differential gain stage.

For the beginning of this analysis, it is assumed that the virtual grounds are intact. Therefore, the differential pair can be split into the half circuit of Figure 4.28 for analysis. From the preceding analysis of the HBT cascode f_T doubler gain stage, we know that the output impedance is the base-collector capacitance of the cascode transistor.

Figure 4.29. Small-signal equivalent model for the single-ended emitter degenerated cascode amplifier.

Furthermore, using the small-signal model of Figure 4.29 it can be clearly seen that the input impedance is the same as that of a single HBT transistor gain stage. Therefore, the analysis is virtually the same as the distributed amplifier gain stage presented in Chapter 2.

From the chapter on distributed amplifier theory (see Chapter 2), the ratio of the output image impedance over the input image impedance of the input artificial transmission line is (modified for the variable names in Figure 4.29)

$$\frac{Z_{i_B2}}{Z_{i_B1}} = \left[\left(1 - \frac{\omega^2}{\omega_c^2} \right) + j \frac{\omega L_B}{4R_\pi} \right]^{-1} \quad (4.27)$$

and the voltage gain is

$$A_V = \frac{Ng_m}{2 \sqrt{\left(1 - \frac{\omega^2}{\omega_c^2} \right) + j \frac{\omega L_B}{4R_\pi}}} Z_C e^{-N\psi} \quad (4.28)$$

and the power gain is

$$G = \frac{N^2 g_m^2}{4 \left[\left(1 - \frac{\omega^2}{\omega_c^2} \right) + j \frac{\omega L_B}{4R_\pi} \right]} Z_C Z_B e^{-2N\psi} \quad (4.29)$$

Equations (4.27), (4.28), and (4.29) do not take into account the potential degradation of the virtual grounds due to the frequency dependence of the artificial transmission line characteristic impedance. The cascode virtual ground will degrade because the output artificial transmission line and the local termination resistor present a non-symmetrical frequency dependant load to the cascode transistors. This will result in an offset between the cascode transistors that allows the base impedance to become part of the output impedance due to the signal path created by the base-collector capacitance C_μ as can be seen from Figure 4.30. This increased output impedance will degrade the bandwidth, the output

characteristic impedance (and therefore the output match) and the input/output isolation of the distributed amplifier.

Figure 4.30. Small-signal equivalent model of the differential cascode gain stage with the cascode base impedance Z_{BB} .

Assuming a perfectly differential input signal and perfectly symmetrical transistors for the differential pair than any degradation of the virtual ground at the emitter nodes of the differential pair will also be due to the mismatch cascode loads. This degraded virtual ground will in turn reduce the performance of the differential pair by creating a common mode offset.

The breakdown voltages (as discussed in Chapter 3) are of concern and, although the MOSFET device cannot operate beyond the device breakdown, the bipolar devices can. Therefore, the cascode bias circuitry for the HBT gain stages (including the HBT f_T doubler gain stage) are designed in such a way as to ensure that any current exiting the base during a breakdown event (which may in fact be the normal operation of the gain stage) will not significantly de-bias the amplifier. The bias circuitry for the gain stage of Figure 4.25 uses a small resistor to ground so that the current exiting the base will not change the base voltage to any significant degree. In Figure 4.27, the diode-connected

transistors establish the bias voltage while the small resistor, R , provides a path for the base current to exit while not significantly affecting the bias voltage.

4.2.5 The Artificial Transmission Line

The three distributed amplifiers use input and output artificial transmission lines to connect the gain stages together. As previously discussed, the artificial transmission line is composed of cascaded filter sections with a passive resistor termination. However, a passive resistor termination results in sub-optimal performance since the image impedance of the filter sections is frequency dependent and not matched by a resistor for the entire band of interest.

The different filter sections discussed in Chapter 2 have both advantages and disadvantages when used in artificial transmission lines. Figure 4.31 through Figure 4.36 show a performance comparison of the different filter sections with resistive terminations. Note that in Chapter 2 the values for m were chosen to be: $m = 0.1$ for the m -derived T filter section and $m = 0.6$ for the bisected- π filter section.

Figure 4.32 shows that the m -derived T section has a 3dB passband that is flatter and has a much sharper roll off than the constant- k T filter section and consequently a smaller bandwidth. The input reflection coefficient of the m -derived filter section is better than the constant- k T section up to a normalized frequency of approximately 0.95.

Figure 4.34 shows that the passband of the constant- k T filter section is flatter and has a similar roll-off but higher 3dB bandwidth compared to the m -derived section (with $m=0.1$) when a bisected- π matching section is added before the resistive terminations. However, the input match for the constant- k T section while improved is still not as good as the m - derived section up to a normalized frequency of approximately 0.7.

Finally, Figure 4.36 shows that the largest and flattest bandwidth is obtained by using m -derived T sections ($m=0.1$) with bisected- π matching sections ($m=0.6$). Note that this configuration also has the sharpest roll-off. With regards to the input reflection coefficient, the m -derived filter section still shows a better performance up to a normalized frequency of 0.75.

From the aforementioned comparison of filter sections the best choice for the distributed amplifiers presented in this thesis is the m -derived T filter section. The m -derived section takes up more layout area than the constant- k filter section but provides more flexibility with the inclusion of the resonant arm. The bisected π m -derived filter section is not used in any of the distributed amplifier artificial transmission lines proposed in this document. The required / desired specifications can be met without the bisected- π matching filter section. The omission of this filter section in the design also helps to reduce the complexity and size of the distributed amplifiers.

Figure 4.31. Constant-k T filter section (left) and m-derived π T filter section (right) with resistive terminations.

Figure 4.32. A comparison between the constant-k T section and the m-derived T section ($m = 0.1$).

Figure 4.33. m -derived π T filter section (top) and constant- k T filter section with m -derived bisected- π filter section (bottom) and resistive terminations.

Figure 4.34. A comparison between the m -derived T section ($m = 0.1$) and a constant- k T section with bisected- π sections before the terminations ($m = 0.6$).

Figure 4.35. m-derived π T filter section (top) and m-derived π T filter section with m derived bisected- π filter section (bottom) and resistive terminations.

Figure 4.36. A comparison between the m-derived T section ($m = 0.1$) and a m-derived T section ($m = 0.1$) with bisected- π sections ($m = 0.6$) before the terminations.

4.2.5.1 Inductor Models

Each inductor of the single-ended artificial transmission line is implemented as a stand alone passive device with minimum inductive or capacitive coupling to its neighbours. The isolation of the inductor is achieved by using a deep trench mesh under the inductor and by maintaining as large a distance as possible to the other passive and active structures. The deep trench mesh reduces the inductor's substrate coupling capacitance from between 10% and 40% depending on the distance of the conductor metal from the substrate. The reduced capacitance to the substrate also has the added benefit of increasing the resonant frequency of the inductor and therefore shifting the resonance further away from the distributed amplifier passband [71, 75, 76]. The inductors range from 100pH to 500pH and are implemented in the top copper metal layer. The inductors are of the horse shoe type which increases the distance between filter stages and therefore aids in isolating the resonant shunt inductors of the m-derived filter sections.

The circuit of Figure 4.37 is a result of a modeling exercise to determine a circuit that accurately represents the inductors used in the single-ended distributed amplifier artificial transmission lines. This circuit is crucial because it facilitates the inclusion of the inductor parasitic capacitance and resistance to that of the gain stage parasitic elements. Each inductor has multiple model stages to achieve a broadband fit to the S-parameter file of the inductor.

To model an inductor the layout is first created in the Cadence virtuoso layout editor tool. The layout is then imported to Agilent's momentum EM simulator to create an S-parameter file. The S-parameter file is then fitted to a lumped element inductor model using Agilent's ADS simulation tool. A lumped element model is used in place of the S-parameter file because the Cadence Virtuoso Spectre circuit simulator is a time domain simulation tool. As such, a circuit component must be added that converts the frequency domain S-parameter file to a curve fitted time domain model. This circuit element is com-

plex and difficult to properly implement and therefore prone to error. An alternative is to fit a lumped element model (such as Figure 4.37) to the S-parameter file.

Figure 4.37. Inductor π model.

The differential inductor model of Figure 4.38 is used in the filter sections of the input artificial transmission line of the three stage differential to single-ended distributed amplifier of Figure 4.15. A similar modeling exercise as the one used for the inductor of Figure 4.37 was used to arrive at the differential inductor model. The inductor model of Figure 4.38 is composed of two T sections connected by a coupling capacitor. It is interesting to note that the T type inductor model closely resembles the filter sections presented in Chapter 2 and connecting two T sections together in series results in the π model of Figure 4.37).

Figure 4.38. Differential inductor T model.

The inductor models (see Figure 4.37 and Figure 4.38) are composed of parasitic substrate capacitance C_{SUB} and R_{SUB} . An oxide/dielectric capacitance C_O and the series resistance and inductance of the conductor. The differential inductor, as previously mentioned, adds a coupling capacitance C_C between the two single-ended inductor models and also has a mutual inductance M .

4.3 The Distributed Amplifiers

The proposed distributed amplifier Figure 4.39, Figure 4.40, Figure 4.41 have been layed out and simulated using the ST BiCMOS9 process and the Cadence tool suit. All three distributed amplifiers use separate DC supplies to bias the input/output artificial transmission lines and the cascode bias. The DC supply voltages for both the input and output artificial transmission lines are applied via broadband bias-Ts (45MHz to 50GHz). The gain stage devices are biased and sized to maximize the output swing of the distributed amplifiers, while keeping the bandwidth of the distributed amplifiers as large as possible without sacrificing output voltage swing.

Figure 4.39. Layout of the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier.

Figure 4.40. Layout of the HBT single-ended three-stage cascoded f_T doubler distributed amplifier.

Figure 4.41. Layout of the HBT three-stage cascode differential to single-ended distributed amplifier.

To maximize the speed of the distributed amplifier gain stages the devices were kept small minimum gate length for CMOS with widths on the order of $40\ \mu\text{m}$ and small HBT devices were chosen with multiple collectors, bases and emitter widths around $4\ \mu\text{m}$. High quality capacitors and precision poly resistors were used to bias the cascode devices and create the on-chip artificial transmission line terminations. Small ESD diodes were added as well as clamps to protect the devices from an ESD or antenna event.

As previously stated the distributed amplifier artificial transmission line inductors are simulated with models created with Agilent's Momentum EM and ADS simulator tools. The distributed amplifiers employ on-chip $50\ \Omega$ terminations with on-chip (for high-speed) and off-chip (for low-speed) decoupling capacitors for the artificial transmission line terminations.

Due to test equipment limitations only 10 Gbps and 20 Gbps data is available for measurement. However, an 11 Gbps and 22 Gbps prbs will be used for simulations to ensure that the distributed amplifiers have enough margin for operation at 10 Gbps and 20

Gbps. Although the distributed amplifiers cannot be measured with a 40 Gbps prbs they will be simulated with a 40Gbps prbs to ensure that they will operate as desired.

The pulse pattern generator used in the measurement test bench produces a square wave prbs and as such the 2nd and 3rd harmonic of the signal source are present and can be used to qualify the distributed amplifiers. Recall that the amplifiers are designed for 40 Gbps data or a maximum frequency of 20 GHz (assuming sinusoidal prbs data). A 10 Gbps and 20 Gbps square wave prbs signals have second and third harmonics of 10 GHz and 15 GHz and, 20 GHz and 30 GHz respectively. Therefore, although a 40 Gbps prbs signal is not available the second and third harmonics of the 10 Gbps and 20 Gbps prbs signals can help qualify the performance of the distributed amplifiers and serve as an indicator of how well the distributed amplifiers will pass a 40 Gbps signal. In other words the distributed amplifiers are more likely to pass a 40 Gbps prbs signal if the 10 Gbps and 20 Gbps square wave output of the distributed amplifier have wide open eye patterns.

The following simulations for each of the distributed amplifiers was done at the typical process corner (for all the passives and actives) with a typical extraction for the interconnect parasitics. The typical corner was chosen because most of the BiCMOS9 MPW (multi-project wafer) runs that the high-speed ASIC development group at Nortel M.E.N, and later Ciena took part in have been at the typical corner or slightly fast. However, although not included in this document, the extreme process corners were also simulated to insure that the distributed amplifiers would still provide a reasonable response for a slow and fast fabrication run.

Figure 4.42. Simulated S-parameters for the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier.

Figure 4.43. Simulated group delay for the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier.

Figure 4.44. Input/Output referred 1dB compression point for the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier.

Figure 4.45. Simulated 11 Gbps output eye for the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier with a 1.2 V 2^7 -1 prbs input to the test bench resulting in a 600 mV input prbs to the distributed amplifier.

Figure 4.46. Simulated 22 Gbps output eye for the CMOS single-ended five-stage cas-coded f_T doubler distributed amplifier with a $1.2 \text{ V } 2^7\text{-1}$ prbs input to the test bench resulting in a 600 mV input prbs to the distributed amplifier.

Figure 4.47. Simulated 40 Gbps output eye for the CMOS single-ended five-stage cas-coded f_T doubler distributed amplifier with a $1.2 \text{ V } 2^7\text{-1}$ prbs input to the test bench resulting in a 600 mV input prbs to the distributed amplifier.

Table 4.5 Summary for the simulated small signal S-parameters, group delay and power consumption of Figure 4.42 and Figure 4.43.

Gain (dB)	$S_{11} \leq -10$ dB (GHz)	$S_{22} \leq -10$ dB (GHz)	Passband S_{12} (dB)	Group Delay (ps)	-3 dB BW (GHz)	P_{DC} (mW)
8.53 ± 0.65	40	40	≤ -24.4	37.62 ± 7.45	34.14	255.15

Table 4.6 Summary for the 11 Gbps simulated output eye of Figure 4.45.

Eye height (mV)	Eye width (ps)	Jitter _{p-p} (ps)	Voltage _{p-p} (V)
1.27	89.2	1.71	1.51

Table 4.7 Summary for the 22 Gbps simulated output eye of Figure 4.46.

Eye Height (mV)	Eye width (ps)	Jitter _{p-p} (ps)	Voltage _{p-p} (V)
1.48	43.65	1.80	1.63

Table 4.8 Summary for the 40 Gbps simulated output eye of Figure 4.47.

Eye Height (mV)	Eye width (ps)	Jitter _{p-p} (ps)	Voltage _{p-p} (V)
1.26	23.11	1.89	1.86

The simulated results for the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier show that although the bulk of the S-parameter results (Figure 4.42 and Figure 4.43 are summarized in Table 4.5) are within the desired specifications, the gain of the distributed amplifier is not sufficient to produce a minimum of a 1V peak-to-peak output swing from a CML level input signal. However increasing the input signal to 600mV will produce the desired output swing (see Table 4.6, Table 4.7 and Table 4.8). The penalty for increasing the input swing is an increased signal distortion as the distributed amplifier output signal begins to compress (at low frequencies) at an input power greater than -2 dB (see Figure 4.44), which for a 50 Ohm system translates to a peak-to-peak input swing of 502 mV.

Figure 4.48. Simulated S-parameters for the HBT single-ended three-stage cascoded f_T doubler distributed amplifier.

Figure 4.49. Simulated group delay for the HBT single-ended three-stage cascoded f_T doubler distributed amplifier.

Figure 4.50. Input/Output referred 1dB compression point for the HBT single-ended three-stage cascoded f_T doubler distributed amplifier.

Figure 4.51. Simulated 11 Gbps output eye for the HBT single-ended three-stage cascoded f_T doubler distributed amplifier with a 400 mV 2^7 -1 prbs input to the test bench resulting in a 200 mV input prbs to the distributed amplifier.

Figure 4.52. Simulated 22 Gbps output eye for the HBT single-ended three-stage cas-coded f_T doubler distributed amplifier with a 400 mV 2^7-1 prbs input to the test bench resulting in a 200 mV input prbs to the distributed amplifier.

Figure 4.53. Simulated 40 Gbps output eye for the HBT single-ended three-stage cas-coded f_T doubler distributed amplifier with a 400 mV 2^7-1 prbs input to the test bench resulting in a 200 mV input prbs to the distributed amplifier.

Table 4.9 Summary for the simulated small signal S-parameters, group delay and power consumption of Figure 4.48 and Figure 4.49.

Gain (dB)	$S_{11} \leq -10$ dB (GHz)	$S_{22} \leq -10$ dB (GHz)	Passband S_{12} (dB)	Group Delay (ps)	-3 dB BW (GHz)	P_{DC} (mW)
21.37±2.63	32.54	>40	≤−35.57	36.31±13.61	35.93	320.43

Table 4.10 Summary for the 11 Gbps simulated output eye of Figure 4.51.

Eye height (V)	Eye width (ps)	Jitter _{p-p} (ps)	Voltage _{p-p} (V)
1.37	89.31	1.60	1.62

Table 4.11 Summary for the 22 Gbps simulated output eye of Figure 4.52.

Eye Height (V)	Eye width (ps)	Jitter _{p-p} (ps)	Voltage _{p-p} (V)
1.45	44.45	1.00	1.60

Table 4.12 Summary for the 40 Gbps simulated output eye of Figure 4.53.

Eye Height (V)	Eye width (ps)	Jitter _{p-p} (ps)	Voltage _{p-p} (V)
1.32	23.32	1.68	2.46

The simulated results for the HBT single-ended three-stage cascoded f_T doubler distributed amplifier show that the an input peak-to-peak swing of 200mV easily generates the desired minimum 1V peak-to-peak output swing. From Figure 4.50 it can be seen that at higher frequencies the 1dB compression point occurs at lower input powers approaching 282mV peak-to-peak at 20GHz, which therefore provides the potential to increase the input power to achieve the more desirable 2V peak-to-peak output swings without incurring significant distortion.

Figure 4.54. Simulated S-parameters for the HBT three-stage cascode differential to single-ended distributed amplifier.

Figure 4.55. Simulated group delay for the HBT three-stage cascode differential to single-ended distributed amplifier.

Figure 4.56. Common mode rejection ratio for the HBT three-stage cascode differential to single-ended distributed amplifier.

Figure 4.57. Output referred power supply rejection ratio for the HBT three-stage cascode differential to single-ended distributed amplifier.

Figure 4.58. Input/Output referred 1dB compression point for the HBT three-stage cascode differential to single-ended distributed amplifier.

Figure 4.59. Simulated 11 Gbps output eye for the HBT three-stage cascode differential to single-ended distributed amplifier with a 400 mV 2^7-1 prbs input to the test bench resulting in a 200 mV input prbs to the distributed amplifier.

Figure 4.60. Simulated 22 Gbps output eye for the HBT three-stage cascode differential to single-ended distributed amplifier with a 400 mV 2^7 -1 prbs input to the test bench resulting in a 200 mV input prbs to the distributed amplifier.

Figure 4.61. Simulated 40 Gbps output eye for the HBT three-stage cascode differential to single-ended distributed amplifier with a 400 mV 2^7 -1 prbs input to the test bench resulting in a 200 mV input prbs to the distributed amplifier.

Table 4.13 Summary for the simulated small signal S-parameters, group delay and power consumption of Figure 4.54 and Figure 4.55.

Gain (dB)	$S_{11} \leq -10$ dB (GHz)	$S_{22} \leq -10$ dB (GHz)	Passband S_{12} (dB)	Group Delay (ps)	-3 dB BW (GHz)	P_{DC} (W)
16.05 ± 1.64	18.58	19.1	≤ -19.56	29.22 ± 7.25	31.70	924.93

Table 4.14 Summary for the 11 Gbps simulated output eye of Figure 4.59.

Eye Height (V)	Eye width (ps)	Jitter _{p-p} (ps)	Voltage _{p-p} (V)
1.37	88.07	2.84	1.73

Table 4.15 Summary for the 22 Gbps simulated output eye of Figure 4.60.

Eye Height (V)	Eye width (ps)	Jitter _{p-p} (ps)	Voltage _{p-p} (V)
1.37	41.06	4.39	1.72

Table 4.16 Summary for the 40 Gbps simulated output eye of Figure 4.61.

Eye Height (V)	Eye width (ps)	Jitter _{p-p} (ps)	Voltage _{p-p} (V)
1.18	21.58	3.42	1.92

The HBT three-stage cascode differential to single-ended distributed amplifier also shows significant potential to achieve the desired 2V peak-to-peak output swings without significant distortion incurred by increasing the input power to 300mV peak-to-peak (see Figure 4.58). However, the 1dB compression point of the distributed amplifiers (Figure 4.44, Figure 4.50 and Figure 4.58) can be misleading because the distributed amplifier is a broadband circuit in the data path. Therefore, the input signal has frequency components across the entire bandwidth which must be accounted for and are not accurately represented by a 1 or 2 tone test. The 1dB compression point is useful in that it can be used as an initial guide but a more accurate representation is the eye diagram.

Also, as expected the common mode rejection ratio (CMRR) and power supply rejection ratio (PSRR) of the HBT three-stage cascode differential to single-ended distributed amplifier are lower than would be expected for a differential amplifier. As has been

previously mentioned, the degradation in the common mode is due to the non-symmetrical frequency dependant load to the gain stage cascode transistors. The non-symmetrical load results in an offset between the cascode transistors that impacts the virtual ground of the cascode transistors and the differential pair by creating a common mode offset.

The data presented in Table 4.5 through Table 4.16 includes the small signal S21 or voltage gain of the distributed amplifiers which is presented as an average passband gain $\pm$ the gain ripple and the group delay that is measured with a back-off of 20% from the peak value of group delay. The group delay is the time delay of the input signal versus frequency and as such is a measure of the phase linearity or phase distortion of the distributed amplifiers. A flat group delay represents a linear phase (minimum distortion). The group delay of the distributed amplifiers peaks as the passband gain rolls-off. Therefore, it is desirable to back-off from the peak to reduce the signal distortion and consequently also limit the usable passband. A typical back-off from the group delay peak is 20% to 25%. Finally, the simulated eye diagram data from each of the distributed amplifiers is summarized in Table 4.5 through Table 4.16.

The distributed amplifier simulated results (Figure 4.42 to Figure 4.59 inclusive) show fairly good performance with regards to 11, 22 and 40 Gbps operation with a few caveats. Comparing Table 4.5 to Table 4.9 and Table 4.13 it is immediately apparent that the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier has significantly less gain than the other two HBT distributed amplifiers. This necessitates a much larger input voltage swing for the CMOS distributed amplifier to achieve the desired 1V minimum pre-driver output voltage swings.

Each distributed amplifier has some signal gain ripple or peaking and a non-flat group delay that are indicators of potentially lost large signal performance that can be seen in the eye diagrams. The eye closure seen in Figure 4.45 through Figure 4.47, Figure 4.51 through Figure 4.53 and Figure 4.59 through Figure 4.61 is indicative of wasted power

(peak to peak voltage ripple) and inter symbol interference (increased jitter). The closure is not significant and may be possible to reduce with further optimization. Also, some of the eye distortion can be attributed to non ideal terminations for the artificial transmission lines (Recall, that the terminations are frequency dependant), which can result in reflected waves that will distort the output eye. Further, the input signal is a square wave in which the fundamental tone and the second and third harmonic play a major role in determining the wave shape. The third harmonic of the 22 Gbps input data will have a high frequency of 33 GHz which is at the edge of the usable bandwidth (due to gain and group delay peaking) of the distributed amplifiers and the 40Gbps second and third harmonics (40GHz and 60GHz respectively) are well outside the distributed amplifiers passband. Typically, the bandwidth of a 40Gbps amplifier in the data path is limited to 20 to 25GHz due to system level requirements, this results in some eye closure due to the high frequency data having a wave shape closer to a sign wave than a square wave.

The breakdown voltage of the CMOS device limits the rail voltage of the CMOS f_T doubler distributed amplifier, the lower rail voltage coupled with the lower gain (when compared to the HBT distributed amplifiers) results in an output swing well below 2 V for a $1.2 V_{p-p}$ input signal that due to the maximum power transfer theorem results in a $600 mV_{p-p}$ input signal to the distributed amplifier (recall that the desired input is $400 mV_{p-p}$). However, the HBT f_T doubler and differential to single-ended cascode distributed amplifiers both have an output swing above $1 V_{p-p}$ for an input of $400 mV_{p-p}$ ($200 mV_{p-p}$ to the distributed amplifiers). Therefore, using a pre-driver to increase the input voltage to the HBT distributed amplifiers should facilitate the desired 2 V swings to drive a low voltage EOM.

Figure 4.62. Simulated 22 Gbps output eye for the HBT single-ended three-stage cas-coded f_T doubler distributed amplifier with a 600 mV 2^7 -1 prbs input to the test bench resulting in a 300 mV input prbs to the distributed amplifier.

Figure 4.63. Simulated 40 Gbps output eye for the HBT single-ended three-stage cas-coded f_T doubler distributed amplifier with a 600 mV 2^7 -1 prbs input to the test bench resulting in a 300 mV input prbs to the distributed amplifier.

Table 4.17 Summary for the 22 Gbps simulated output eye of Figure 4.62.

Eye Height (V)	Eye width (ps)	Jitter _{p-p} (ps)	Voltage _{p-p} (V)
2.4	42.97	2.48	2.8

Table 4.18 Summary for the 40 Gbps simulated output eye of Figure 4.63.

Eye Height (V)	Eye width (ps)	Jitter _{p-p} (ps)	Voltage _{p-p} (V)
2.2	22.98	2.02	2.97

Figure 4.64. Simulated 22 Gbps output eye for the HBT three-stage cascode differential to single-ended distributed amplifier with a 800 mV 2^7 -1 prbs input to the test bench resulting in a 400 mV input prbs to the distributed amplifier.

Figure 4.65. Simulated 40 Gbps output eye for the HBT three-stage cascode differential to single-ended distributed amplifier with a 800 mV 2^7 -1 prbs input to the test bench resulting in a 400 mV input prbs to the distributed amplifier.

Table 4.19 Summary for the 22 Gbps simulated output eye of Figure 4.64.

Eye Height (V)	Eye width (ps)	Jitter _{p-p} (ps)	Voltage _{p-p} (V)
2.25	41.23	4.22	2.43

Table 4.20 Summary for the 40 Gbps simulated output eye of Figure 4.65.

Eye Height (V)	Eye width (ps)	Jitter _{p-p} (ps)	Voltage _{p-p} (V)
2.24	20.96	4.04	2.86

Increasing the input voltage to 600 mV_{p-p} (300mV_{p-p} after the maximum power transfer) to the HBT f_T doubler distributed amplifier and 800 mV_{p-p} to the differential to single-ended distributed amplifier test bench results in the eye diagrams of Figure 4.62 through Figure 4.65. It can be seen in Table 4.17 through Table 4.20 that the resultant output eye height for both distributed amplifiers is above 2 V_{p-p}.

4.4 Summary

In this chapter three distributed amplifiers and their gain stages have been discussed in detail. Two of the distributed amplifiers use an f_T doubler gain-stage and the third distributed amplifier has a differential to single-ended cascode gain stage. All the distributed amplifiers were designed in such a way as to maximize the peak-to-peak output voltage swing without a significant bandwidth reduction. The MOSFET and the HBT distributed amplifiers show an increased output voltage swing when compared to a single transistor distributed amplifier. The distributed amplifier designs are summarized in Table 4.21.

Table 4.21 Summary of proposed distributed amplifiers.

Distributed Amplifier	Gain stage
5 stage CMOS	cascoded f_T doubler
3 stage HBT	cascoded f_T doubler
3 stage HBT	cascoded differential to single-ended

Each of the distributed amplifiers is designed to meet the specifications necessary for operation in a 40 Gbps communication system. Further, a minimum of 1 V_{p-p} is needed for the distributed amplifier to operate as a pre-driver and 2 V_{p-p} is preferable if the amplifier is to drive a low voltage EOM. It's clear from the simulation data that none of the distributed amplifiers can provide a 2 V_{p-p} swing from a 400 mV_{p-p} source input signal but with a pre-driver (the CMOS f_T doubler distributed amplifier could be used for this purpose) the HBT distributed amplifiers can provide a 2 V_{p-p} or more output swing with a source input voltage of 600 mV_{p-p} to 800 mV_{p-p} resulting in a input signal to the distributed amplifier of 300 mV_{p-p} to 400 mV_{p-p} assuming maximum power transfer.

One of the advantages of having a CMOS or SiGe (in the case of BiCMOS) distributed amplifier is the ability to maximize the voltage transfer from the source to the distributed amplifier. This can be achieved by incorporating a converter block that transitions

the input signal from the impedance of the CML cells to the characteristic impedance of the distributed amplifier input artificial transmission line. The output of this converter block can be designed as part of the distributed amplifier input artificial transmission line replacing the termination. The converter/distributed amplifier can then be used as a pre-driver for an HBT distributed amplifier where the output of one distributed amplifier (the pre-driver) and the input of the next can be designed to have a common transmission line. This configuration results in a maximization of the voltage swing from amplifier to amplifier by avoiding the halving effect of the maximum power transfer theorem.

Chapter 5: Experimental Results

In this chapter the measurement results for the distributed amplifiers discussed in Chapter 4 are presented, the large and small signal simulation results are verified and the test bench used to measure the amplifiers is presented.

5.1 Distributed Amplifier testing

All three distributed amplifiers (Figure 5.1, Figure 5.2, and Figure 5.3) were fabricated using ST's BiCMOS9 process. The process has 6 copper metal layers and 1 Aluminum top metal layer. The BiCMOS process has 0.13 micron CMOS devices and a SiGe HBT device with an f_T and f_{max} of 160GHz.

Figure 5.1. Photomicrograph of the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier.

Figure 5.2. Photomicrograph of the HBT single-ended three-stage cascoded f_T doubler distributed amplifier.

Figure 5.3. Photomicrograph of the HBT three-stage cascode differential to single-ended distributed amplifier.

The dice sent from the ST fabrication facility were glued to 4 inch wafers using an electrically conductive adhesive. The 4 inch wafers were then placed on a Cascade Summit 9000 probe station with GGB picoprobes for measurement.

The S-parameters were measured with an HP 8510C vector network analyzer (VNA). The test bench for the S-parameter measurements was configured as per Figure 5.4 where the two ports of the VNA were connected to the input and output of the distributed amplifiers. The HBT three-stage cascode differential to single-ended distributed amplifier has a differential input and single-ended output. Therefore to fully characterize the distributed amplifier three-port S-parameters are required. The two-port VNA was used to measure three-port S-parameters by taking multiple two-port measurements between all three ports of the distributed amplifier and terminating the unused port with a 50-Ohm resistor. The three-port S-parameters were then converted to two-port S-parameters [77].

The time domain 10 Gbps measurement data was observed using a Tektronix TDS 8000 digital sampling oscilloscope and generated with an Anritsu MP1763B pulse pattern generator. The 20 Gbps transient data was generated with an Anritsu MP1758A 4 channel pulse pattern generator and a SHF 4005A 40 Gbps 4:1 multiplexer. An Agilent 86100A digital sampling scope with the 83484A dual channel 50 GHz electrical module was used to observe the 20 Gbps signal. The test bench for the time domain measurements was configured as in Figure 5.5. Both the Anritsu MP 1758A pulse pattern generator and the SHF 4005A multiplexer have differential outputs, therefore the unused output was terminated with 50-Ohms for the single-ended distributed amplifier measurements.

All three distributed amplifiers use separate DC supplies to bias the input/output artificial transmission lines and the cascode bias. The DC supply voltages for the input/output artificial transmission lines are applied via HP 11612B broadband bias-Ts (45 MHz to 50 GHz). All the measurements used 2.4 mm connectorized cables and adaptors.

Figure 5.4. Simplified test bench diagram for S-parameter measurements

Figure 5.5. Simplified test bench diagram for eye pattern measurements

As has been previously mentioned (Chapter 4), due to test equipment limitations only 10 Gbps and 20 Gbps square wave prbs data is available for measurement. The input data has frequency components (harmonics) up to and including 15 GHz and 30 GHz for the 10 Gps and 20 Gbps prbs signals respectively. These high frequency components can be used to qualify the performance of the distributed amplifiers and serve as an indicator of how well the distributed amplifiers will pass a 40 Gbps signal.

Figure 5.6. Distributed amplifier off-chip termination

The input and output of the f_T doubler distributed amplifier artificial transmission lines are connected off-chip to picoprobes via the signal pads of the pad frame (see Figure 5.4 and Figure 5.5). At the other end of the input/output artificial transmission lines there are on-chip 50 Ohm terminations with on-chip (for high-speed) and off-chip (for low-speed) de-coupling capacitors for the artificial transmission line terminations. The off-chip capacitors are connected via picoprobes to the distributed amplifiers, as per Figure 5.6. The design of the artificial transmission line termination does not take into account the 50 Ohm characteristic impedance of the picoprobe and as a result the distributed amplifier transmission line termination impedance is degraded from the desired 50 Ohms.

Although not implemented in the distributed amplifiers presented in this thesis, a possible termination scheme that takes the aforementioned picoprobe impedance into account would result in the transmission line termination of Figure 5.7, where the tuned inductor is inserted to deal with the pad capacitance of the pad frame to present a 50 characteristic impedance to the picoprobe. Off-chip the picoprobe is terminated with a 50 Ohm resistor and a large capacitance to provide the low speed termination.

Figure 5.7. Corrected distributed amplifier off-chip termination

The test benches used to measure the distributed amplifiers includes picoprobes, cables, adaptors, bias-Ts, etc. Models for these interconnect elements are included in the simulations to have an accurate comparison between the measured and simulated results of the distributed amplifiers. The test equipment also introduces un-desired noise/losses in the measurement data that should also be accounted for.

5.2 The Measured Distributed Amplifier data

To accurately capture the performance of the distributed amplifiers when making S-parameter measurements the 2-port vector network analyzer (VNA) must be calibrated using a calibration substrate. The short open and load of the calibration substrate can be used to remove any errors from the S-parameter measurements due to the cables, connectors and picoprobes attached to the 2-ports of the VNA [78].

The distributed amplifiers have multiple signal pads connected to picoprobes for the artificial transmission line terminations and for the input and output of the distributed amplifiers. The impact of the signal pads on the input and output of the distributed amplifiers can also be corrected for by measuring the open and short of the signal pads and de-embedding the measured pad characteristics from the measured distributed amplifier S-parameters [79]. However, the off-chip artificial transmission line terminations, associated

signal pads and picoprobes are not de-embedded from the S-parameter measurements. The distributed amplifiers were designed to have off-chip termination capacitors and therefore they cannot be de-embedded from the measured distributed amplifier S-parameters.

The effect of the pads, picoporbes, cables, connectors and bias-Ts was not de-embedded from the measured time domain data. Instead models of the aforementioned elements were created to add to the simulation test bench of the distributed amplifiers.

5.2.1 The CMOS single-ended five-stage cascoded f_T doubler distributed amplifier

As has been previously mentioned the measured S-parameters have the effects of the signal pads at the input and output of the distributed amplifiers removed from the measured S-parameters. The resultant de-embedded S-parameters of the CMOS single-ended five-stage cascoded f_T doubled distributed amplifier line up well with the simulated results (Figure 5.8 through to Figure 5.12).

Figure 5.8. Measured and simulated S_{11} (dB) for the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier

Figure 5.9. Measured and simulated S_{22} (dB) for the CMOS single-ended five-stage cas-coded f_T doubler distributed amplifier

Figure 5.10. Measured and simulated S_{21} (dB) for the CMOS single-ended five-stage cas-coded f_T doubler distributed amplifier

Figure 5.11. Measured and simulated S_{12} (dB) for the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier

Figure 5.12. Calculated group delay (ps) from measured and simulated data for the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier.

Table 5.1 Summary for the de-embedded S-parameters, calculated group delay and power consumption of the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier.

Gain (dB)	$S_{11} \leq -10$ dB (GHz)	$S_{22} \leq -10$ dB (GHz)	Passband S_{12} (dB)	Group Delay (ps)	-3 dB BW (GHz)	P_{DC} (mW)
6.68 ± 0.48	22.65	21.7	≤ -22.1	35.82 ± 14.11	29.55	234.62

The simulated S-parameters in Figure 5.8 through Figure 5.12 show a reasonable match to the measured results but differ from the S-parameters presented in Chapter 4 (comparing Table 5.1 to Table 4.5). This is due to the addition of the off-chip capacitance, picoprobes and interconnect models as well as a change in simulation corner to more accurately reflect the measured results. The addition of the off-chip capacitance results in a low frequency resonance that can be seen in the forward gain (S_{21}) and the calculated group delay.

The match between the simulated and measured small signal S-parameters indicate that the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier is operating as expected and also serves as an indicator that the large signal performance may also meet expectations.

Figure 5.13. Measured 10 Gbps output eye for the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier with a 1.5 V 2^7 -1 prbs input to the test bench resulting in a 750 mV input prbs to the distributed amplifier.

Figure 5.14. Simulated 10 Gbps output eye for the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier with a 1.5 V 2^7 -1 prbs input to the test bench resulting in a 750 mV input prbs to the distributed amplifier.

Figure 5.15. Measured 10 Gbps through eye (using a pad from the pad frame) with a 1.2 V 2^7 -1 prbs input to the test bench.

A sum of squares equation (5.1) can be used to remove the jitter contribution of the test bench (source, oscilloscope, interconnect and picoprobes, etc) from the measured transient data of Figure 5.13. For the results of the equation to be valid the jitter must be uncorrelated and, if the measured jitter is close to the measurement noise floor the resultant de-embedded jitter may have a large uncertainty [80].

$$Jitter_{dut} = \sqrt{Jitter_{meas}^2 - Jitter_{tb}^2} \quad (5.1)$$

where, $Jitter_{meas}$ is the measured jitter and $Jitter_{tb}$ is the jitter contribution of the test bench.

The peak-to-peak jitter does not have to be converted to RMS jitter to use the sum of squares equation (5.1). The two are related by a constant that is dependant on the bit error rate (5.2).

$$Jitter_{p-p} = \alpha Jitter_{RMS} \quad (5.2)$$

where $BER = \frac{1}{2}erfc(\alpha\sqrt{2})$.

Therefore, assuming the same bit error rate for the measured jitter and the jitter of the device under test allows the constant α to be eliminated from the equation leaving only the peak-to-peak jitter terms [81,82].

Table 5.2 Summary for the measured 10 Gbps through eye of Figure 5.15 used to de-embed the test bench jitter contribution for Table 5.3

Eye height (mV)	Eye width (ps)	Jitter _{p-p} (ps)	Voltage _{p-p} (mV)
756	86.88	13.12	1.06

Table 5.3 Summary for the measured 10 Gbps output eye of Figure 5.13.

Eye height (V)	Eye width (ps)	De-embedded Eye width (ps)	Jitter _{p-p} (ps)	De-embedded Jitter _{p-p}	Voltage _{p-p} (V)
1.12	84	90.84	16	9.16	2.39

Table 5.4 Summary for the simulated 10 Gbps output eye of Figure 5.14.

Eye height (V)	Eye width (ps)	Jitter _{p-p} (ps)	Voltage _{p-p} (V)
1.19	93.69	6.31	1.71

The measured and simulated 10 Gbps eye patterns of Figure 5.13 and Figure 5.14 look very similar. The summaries in Table 5.3 and Table 5.4 show that the measured 10 Gbps eye has more jitter than the simulation predicts and the measured peak-to-peak voltage is much larger. The discrepancies are due to the prbs source which introduces jitter and amplitude ripple that is not present in the simulated results. Further, the limitations of the picoprobe and interconnect models will account for some of the discrepancies between the measured and simulated results. The models are simple lumped element representations that may not fully capture the performance (electrical length and therefore the phase

performance, complex input/output impedance, etc) of the picoprobes and other interconnect elements.

The Tektronix TDS 8000 and the Agilent 86100A digital sampling oscilloscopes were used to obtain the distributed amplifier 10 Gbps output eye and the 10 Gbps through eye respectively. The 10 Gbps through eye is used to de-embed the source jitter from the measured jitter and it does not matter which oscilloscope is used since the jitter contribution of the oscilloscope is insignificant when compared to the contribution of the source and distributed amplifier. Note, the difference in source jitter between the 1.2 V peak-to-peak input signal and the 1.5 V signal is also insignificant.

Figure 5.16. Measured 20 Gbps output eye for the CMOS single-ended five-stage cascaded f_T doubler distributed amplifier with a 1.12 V 2^9 -4 prbs input to the test bench resulting in a 560 mV input prbs to the distributed amplifier.

Figure 5.17. Simulated 20 Gbps output eye for the CMOS single-ended five-stage cas-coded f_T doubler distributed amplifier with a 1.12 V 2^9 -4 prbs input to the test bench resulting in a 560 mV input prbs to the distributed amplifier.

Figure 5.18. Measured 20 Gbps through eye (calibration standard) with a 1.12 V 2^9 -4 prbs input to the test bench.

Table 5.5 Summary for the measured 20 Gbps through eye of Figure 5.18

Eye height (mV)	Eye width (ps)	Jitter _{p-p} (ps)	Voltage _{p-p} (V)
522.04	40.55	9.45	1.18

Table 5.6 Summary for the measured 20 Gbps output eye of Figure 5.16.

Eye height (mV)	Eye width (ps)	De-embedded Eye width (ps)	Jitter _{p-p} (ps)	De-embedded Jitter _{p-p}	Voltage _{p-p} (V)
584	32.55	35.33	17.45	14.67	1.97

Table 5.7 Summary for the simulated 20 Gbps output eye of Figure 5.17.

Eye height (mV)	Eye width (ps)	Jitter _{p-p} (ps)	Voltage _{p-p} (V)
879.1	40.59	9.41	1.62

The SHF 4005A 4:1 multiplexer (MUX) used to generate the 20 Gbps signal has a 2.5 V peak-to-peak (although the specifications indicate 2.5 V the output was a bit less), adding a 6 dB attenuator reduce the peak-to-peak voltage to approximately 1.12 V. The resultant square wave 20 Gbps prbs input signal to the distributed amplifier has frequency components below the lower cut-off frequency of the Bias-Ts and right at the upper edge of the bandwidth (~30 GHz) of the distributed amplifier. The signals outside the bandwidth of the amplifier result in some eye closure and increased jitter. Also, long sequences of zeros or ones in the data pattern will generate a DC drift or duty cycle distortion (DCD) at the output of the distributed amplifier which also reduces the eye opening and increases the jitter. Finally, the SHF 4005A 4:1 MUX introduces significant peak-to-peak voltage ripple and jitter that closes the input prbs eye by 55.76% in the vertical direction and 18.82% in the horizontal direction. As a result the measured 20 Gbps eye diagram (Figure 5.16.) shows significant eye closure when compared to the 10 Gbps eye (Figure 5.13.).

The 20 Gbps prbs pattern used in the measurement was recorded and used to generate the 20 Gbps prbs used to obtain the simulated eye of Figure 5.17 (the pattern of zeros and ones was recorded and not the actual time domain data). Comparing the simulated 20 Gbps eye diagram to the measured (Table 5.6 and Table 5.7) shows that the measured eye

has more closure than the simulated and is most likely due to the aforementioned limitations of the picoprobe and interconnect models as well as the noise contribution of the prbs source that is not present in the simulations.

The new 20 Gbps prbs signal was also used in a simulation without the picoprobe and interconnect models to compare with the simulation of the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier in Chapter 4. Table 5.8 was generated from the Figure 5.19 eye diagram and comparing to Table 5.9 (copied from Chapter 4) it can be seen that the aforementioned issues with the 20 Gbps have closed the eye but not to the degree seen in the measured results. This result is as expected since the impact of the picoprobe models, interconnect models and the off-chip capacitance have been removed (see Table 5.7 to Table 5.8.)

Figure 5.19. Simulated 20 Gbps output eye for the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier with the picoprobe and interconnect models removed from the simulation. A 1.12 V 2^9 -4 prbs input signal to the test bench resulting in a 560 mV input prbs to the distributed amplifier was used.

Table 5.8 Summary for the simulated 20 Gbps output eye of Figure 5.19

Eye height (mV)	Eye width (ps)	Jitter _{p-p} (ps)	Voltage _{p-p} (V)
1.26	43.12	6.88	1.901

Table 5.9 Summary for the 22 Gbps simulated output eye of Figure 4.46 from Chapter 4

Eye Height (mV)	Eye width (ps)	Jitter _{p-p} (ps)	Voltage _{p-p} (V)
1.48	43.65	1.80	1.63

Figure 5.20. Simulated 40 Gbps output eye for the CMOS single-ended five-stage cas-coded f_T doubler distributed amplifier with a $1.12 \text{ V } 2^7\text{-1}$ prbs input signal to the test bench resulting in a 560 mV input prbs to the distributed amplifier was used.

Table 5.10 Summary for the simulated 40 Gbps output eye of Figure 5.20.

Eye height (mV)	Eye width (ps)	Jitter _{p-p} (ps)	Voltage _{p-p} (V)
832.2	21.7	3.3	1.52

The simulated and measured 10 and 20 Gbps eyes are reasonably matched and therefore, it's reasonable to assume that the 40 Gbps eye from Figure 5.20 (summarized in Table 5.10) depicts the slightly optimistic performance of the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier at 40 Gbps. The simulation uses a 2^7-1 prbs input signal that will not introduce significant DCD or exceed the low frequency bandwidth of the distributed amplifier. The simulated 40 Gbps eye has a lower eye height than either the 10 or 20 Gbps eyes but that is to be expected given the higher frequency content.

Figure 5.21. Measured 10 Gbps output eye for the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier with a 5 V rail voltage and a 1.2 V 2^7-1 prbs input to the test bench resulting in a 600 mV input prbs to the distributed amplifier.

As previously stated operating above the breakdown voltage of the CMOS device results in a performance degradation and eventual destruction of the device. However, the fabrication facility does provide a maximum voltage where the devices can safely operate but with a lifetime reduction and a performance degradation (what is often referred to as

soft breakdown). If the design of the amplifier incorporates / tolerates the degradation in the CMOS device the rail voltage can be raised with the understanding that the higher rail voltage will result in a shorter lifetime for the CMOS device.

The eye diagram of Figure 5.21 shows the 10 Gbps output of the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier with a 5 V rail. Comparing Table 5.11 with Table 5.3 shows only a slight improvement in the eye height but a significantly larger peak-to-peak voltage. The larger observed peak-to-peak voltage indicates that eye height may be larger once the degrading effects of the off-chip capacitance are removed

Figure 5.22. Simulated 10 Gbps output eye for the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier with a 5 V supply and with the pico-probe and interconnect models removed from the simulation. A 1.2 V 2^7 -1 prbs input signal to the test bench resulting in a 600 mV input prbs to the distributed amplifier was used.

Table 5.11 Summary for the measured 10 Gbps output eye of Figure 5.21.

Eye height (V)	Eye width (ps)	De-embedded Eye width (ps)	Jitter _{p-p} (ps)	De-embedded Jitter _{p-p}	Voltage _{p-p} (V)
1.19	74.91	79.89	16	11.02	3.12

Table 5.12 Summary for the simulated 10 Gbps output eye of Figure 5.22.

Eye height (mV)	Eye width (ps)	Jitter _{p-p} (ps)	Voltage _{p-p} (V)
1.7	96.8	3.2	2.14

As expected the simulated 10 Gbps eye opening is larger by almost 500 mV (Comparing Table 5.11 to Table 5.12). This indicates that there is a significant advantage to operating with a 5 V rail with the understanding that the larger rail voltage reduces the lifespan of the CMOS devices. The larger output swing of the distributed amplifier also indicates that the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier may have some potential to be used to directly drive a low voltage EOM (the CMOS distributed amplifier would still require a pre-driver as the input voltage swing is larger than standard CML levels). Furthermore, adding another cascode device to the gain stage of the distributed amplifier would allow for the larger voltage operation without sacrificing the performance and lifetime of the CMOS devices.

5.2.2 The HBT single-ended three-stage cascoded f_T doubler distributed amplifier.

As previously mentioned the de-embedding process requires the measurement of an open and short to remove the impact of the input/output signal pads from the measured S-parameters. The capacitance and resistance values that are being measured for the open and short of the signal pads are very small and susceptible to error due to ambient noise and the contact resistance of the picoprobe. Also, because the distributed amplifier is a broadband circuit the frequency is swept from 45 MHz to 40 GHz and at high frequencies the quality of the VNA calibration declines which introduces further errors.

Therefore, the de-embedded S-parameters (Figure 5.23 to Figure 5.27) have noise from the measured open and short that is not present in the measured or simulated S-parameters. However, the addition of the noise into the de-embedded result does not invalidate the S-parameters of the HBT single-ended three-stage cascoded f_T doubler distributed amplifier as the overall trends and levels are still easily discernible and line up reasonably well with the simulated results.

Figure 5.23. Measured and simulated S_{11} (dB) for the HBT single-ended three-stage cascoded f_T doubler distributed amplifier.

Figure 5.24. Measured and simulated S_{22} (dB) for the HBT single-ended three-stage cas-coded f_T doubler distributed amplifier.

Figure 5.25. Measured and simulated S_{21} (dB) for the HBT single-ended three-stage cas-coded f_T doubler distributed amplifier.

Figure 5.26. Measured and simulated S_{12} (dB) for the HBT single-ended three-stage cascoded f_T doubler distributed amplifier.

Figure 5.27. Calculated group delay (ps) from measured and simulated data for the HBT single-ended three-stage cascoded f_T doubler distributed amplifier.

Table 5.13 Summary for the de-embedded S-parameters, calculated group delay and power consumption of the HBT single-ended three-stage cascoded f_T doubler distributed amplifier.

Gain (dB)	$S_{11} \leq -10$ dB (GHz)	$S_{22} \leq -10$ dB (GHz)	Passband S_{12} (dB)	Group Delay (ps)	-3 dB BW (GHz)	P_{DC} (mW)
12.27 ± 2.03	13.67	31.23	≤ -19.33	33.36 ± 25.6	> 37	386.09

The simulations presented in Chapter 4 for the HBT single-ended three-stage cascoded f_T doubler distributed amplifier differ from what has thus far been presented for the distributed amplifiers in this chapter, this is not only due to the aforementioned off-chip capacitance and model limitations. The process corner chosen for the simulations also has an impact.

The higher DC current of the measured HBT distributed amplifier (lower for the CMOS distributed amplifier) when compared to the simulations in Chapter 4 may indicate that the devices are operating at a different process corner than is used in the Chapter 4 simulations. Also, the measured and de-embedded calculated group delay and forward gain (S_{21}) from Figure 5.25 and Figure 5.27 show more variation in the passband than in the simulations presented in this chapter. Some of this variation is due to the injected noise of the open and short but it can also be an indicator of a difference in process corner between the simulation and measured results.

The process corners of a technology represent the nominal and extremes of the process parameter variation which in turn impact the device and passive performance (i.e. variation in transconductance, capacitance, resistance, etc) Typically the extremes are 3 sigma (3 standard deviations from the mean) but can be higher, some newer CMOS processes have corners as high as 4.5 sigma. Using the minimum and maximum process corners in the simulations ensure that the design will function irrespective of where on the process variation curve a particular fabrication run lies. The process corners as a simulation tool do not provide an exact correlation to any particular process run and the design

may perform very differently from one process lot to the next yet still remain within the extremes represented by the corners. However, the fabrication facilities have the ability to generate specific process corner lots that are used to verify the process and in some cases the designer can request a corner lot as part of the design process or to improve production yield (typically at significant expense).

Figure 5.28. Measured 10 Gbps output eye for the HBT single-ended three-stage cascaded f_T doubler distributed amplifier with a $0.4 \text{ V } 2^7\text{-1}$ prbs input to the test bench resulting in a 0.2 V input prbs to the distributed amplifier.

Figure 5.29. Simulated 10 Gbps output eye for the HBT single-ended three-stage cas-coded f_T doubler distributed amplifier with a $0.4 \text{ V } 2^7\text{-1}$ prbs input to the test bench resulting in a 0.2 V input prbs to the distributed amplifier.

Figure 5.30. Measured 10 Gbps through eye (calibration standard) with a $0.4 \text{ V } 2^7\text{-1}$ prbs input to the test bench.

Table 5.14 Summary for the measured 10 Gbps through eye of Figure 5.30 used to de-embed the test bench jitter contribution for Table 5.15

Eye height (mV)	Eye width (ps)	Jitter _{p-p} (ps)	Voltage _{p-p} (mV)
228.4	86.8	13.2	407.5

Table 5.15 Summary for the measured 10 Gbps output eye of Figure 5.28.

Eye height (V)	Eye width (ps)	De-embedded Eye width (ps)	Jitter _{p-p} (ps)	De-embedded Jitter _{p-p}	Voltage _{p-p} (V)
1.03	83	89.29	17	10.71	2.37

Table 5.16 Summary for the simulated 10 Gbps output eye of Figure 5.29.

Eye height (V)	Eye width (ps)	Jitter _{p-p} (ps)	Voltage _{p-p} (V)
1.12	94.01	5.99	1.56

Comparing the simulated 10 Gbps eye of Figure 5.29 to the measured eye of Figure 5.28 shows a reasonably good match given the aforementioned issues with the test bench and transmission line terminations. It's also clear that the 400 mV peak-to-peak input signal is not sufficient to produce a 2 V peak-to-peak output (see Table 5.15 and Table 5.16). Recall, that in Chapter 4 the simulation results also indicated that a larger voltage than standard CML levels (300 mV to 400 mV) would be required to produce a 2 V peak-to-peak output voltage.

Figure 5.31. Measured 10 Gbps output eye for the HBT single-ended three-stage cas-coded f_T doubler distributed amplifier with a 0.8 V 2^7 -1 prbs input to the test bench resulting in a 0.4 V input prbs to the distributed amplifier.

Figure 5.32. Simulated 10 Gbps output eye for the HBT single-ended three-stage cas-coded f_T doubler distributed amplifier with a 0.8 V 2^7 -1 prbs input to the test bench resulting in a 0.4 V input prbs to the distributed amplifier.

Figure 5.33. Measured 10 Gbps through eye (calibration standard) with a 0.8 V 2^7 -1 prbs input to the test bench.

Table 5.17 Summary for the measured 10 Gbps through eye of Figure 5.33 used to de-embed the test bench jitter contribution for Table 5.18

Eye height (mV)	Eye width (ps)	Jitter _{p-p} (ps)	Voltage _{p-p} (mV)
443	85	15	720

Table 5.18 Summary for the measured 10 Gbps output eye of Figure 5.31.

Eye height (V)	Eye width (ps)	De-embedded Eye width (ps)	Jitter _{p-p} (ps)	De-embedded Jitter _{p-p}	Voltage _{p-p} (V)
1.51	70	74.02	30	25.98	3.12

Table 5.19 Summary for the simulated 10 Gbps output eye of Figure 5.32.

Eye height (V)	Eye width (ps)	Jitter _{p-p} (ps)	Voltage _{p-p} (V)
2.04	90.46	9.54	2.79

Increasing the input voltage to the distributed amplifier to 800 mV results in an increase of almost 500 mV to the horizontal eye opening (see Figure 5.31 and Table 5.18).

The increase in output voltage swing is also accompanied by a large increase in jitter, more than double than what was observed for the 400 mV peak-to-peak input voltage swing (see Table 5.15). The large increase in jitter is not seen in the simulated results (see Figure 5.32 and Table 5.19), which also has a much larger horizontal 2.04 V eye opening.

Both the simulated and the measured eyes show the same trend of non-symmetrical rising and falling edge. However, the measured 10 Gbps eye shows more jitter than is present in the simulated eye. As has previously been stated the noise inserted by the source is not present in the simulations and the model limitations will also account for some of the discrepancy. Also Figure 5.27 shows that the measured group delay has more ripple than is present in the simulations. This variation in the measured group delay will account for some of the eye closure seen in Figure 5.31.

The discrepancy between the simulation and measured results is also impacted by the limitations of the device and passive models provided by ST for the BiCMOS9 kit. There are proprietary documented issues with DC convergence and modeling that will impact the accuracy of the simulated distributed amplifiers. The modeling issues can also be seen in the simulation of the HBT single-ended three-stage cascoded f_T doubler distributed amplifier when the simulation fails to achieve DC convergence if the biasing or the peak-to-peak input voltage is changed slightly from what was used in the 10 Gbps measurement.

Figure 5.34. Measured 20 Gbps through eye (calibration standard) with a 700 mV 2^9-4 prbs input to the test bench.

Table 5.20 Summary for the measured 20 Gbps through eye of Figure 5.34.

Eye height (mV)	Eye width (ps)	Jitter _{p-p} (ps)	Voltage _{p-p} (mV)
352	37	13	735

The measured 20 Gbps output eye of the HBT single-ended three-stage cascoded f_T doubler distributed amplifier is fully closed (not shown here). This is due to several factors:

- The 20 Gbps input signal from the HFS 4005A 4:1 MUX has significant eye closure, 52.11% in the vertical direction and 26% in the horizontal direction (see Figure 5.34 and Table 5.20).
- The transmission line terminations are degraded due to the external capacitance
- There is more ripple in the measured group delay than the simulations predict
- There is duty cycle distortion (DCD) due to long sequences of zeros and ones

- The input prbs pattern has frequency content below the lower cut-off frequency and at the upper edge of the distributed amplifier bandwidth.
- There are issues with the accuracy of the simulations due to the limitations of the models provided by ST which may account for some of the eye closure

Figure 5.35. Simulated 20 Gbps output eye for the HBT single-ended three-stage cascaded f_T doubler distributed amplifier with a 0.7 V 2^9 -4 prbs input to the test bench resulting in a 0.35 V input prbs to the distributed amplifier.

Table 5.21 Summary for the simulated 20 Gbps output eye of Figure 5.35.

Eye height (mV)	Eye width (ps)	Jitter _{p-p} (ps)	Voltage _{p-p} (V)
920.4	37.3	12.7	2.94

Figure 5.36. Simulated 20 Gbps output eye for the HBT single-ended three-stage cas-coded f_T doubler distributed amplifier with the picoprobe and interconnect models removed from the simulation. A 700 mV 2^9 - 4 prbs input signal to the test bench resulting in a 350 mV input prbs to the distributed amplifier was used.

Table 5.22 Summary for the simulated 20 Gbps output eye of Figure 5.35.

Eye height (V)	Eye width (ps)	Jitter _{p-p} (ps)	Voltage _{p-p} (V)
1.50	39.6	10.4	3.40

The simulated 20 Gbps output eye of Figure 5.35 is summarized in Table 5.21 and shows that the frequency content, the picoprobe and interconnect models as well as the corner used for simulation have significantly closed the output eye. The simulation corner was chosen by running S-parameter simulations and comparing the simulated results with the measured and attempting to line up the two sets of S-parameters. The resultant corner differs from the typical corner used in the initial simulations of Chapter 4. Simulating the distributed amplifier without the picoprobes and interconnect models (see Figure 5.36 and Table 5.22) shows that the largest contributors to the eye closure are the frequency content

of the prbs signal and the simulation corner. This can be clearly seen when comparing Figure 5.35 to the 22 Gbps output eye of Figure 4.62, summarized in Table 5.23 (Recall that 22 Gbps was chosen to create a safety margin for 20 Gbps operation). The input 2^7-1 prbs pattern used in the 22 Gbps simulation does not have long sequences of zeros or ones and therefore no DCD and also does not exceed the bandwidth of the distributed amplifier. The amplifier is simulated at the typical corner.

Table 5.23 Summary for the 22 Gbps simulated output eye of Figure 4.62.

Eye Height (V)	Eye width (ps)	Jitter _{p-p} (ps)	Voltage _{p-p} (V)
2.61	44.19	1.26	2.76

Figure 5.37. Simulated 40 Gbps output eye for the HBT single-ended three-stage cas-coded f_T doubler distributed amplifier with a 0.7 V 2^7-1 prbs input to the test bench resulting in a 0.35 V input prbs to the distributed amplifier.

Table 5.24 Summary for the 40 Gbps simulated output eye of Figure 5.37.

Eye Height (V)	Eye width (ps)	Jitter _{p-p} (ps)	Voltage _{p-p} (V)
1.94	21.29	3.71	2.76

Recall, that due to test equipment limitations only 10 and 20 Gbps data was used for the measurement of the distributed amplifiers. Further, as previously mentioned the 20 Gbps eye is closed primarily due to the noise from the source, DCD and the low frequency content of the signal exceeding the bandwidth of the distributed amplifier. Removing these limitations and simulating the distributed amplifier with a 40 Gbps 2^7-1 prbs pattern results in the output eye of Figure 5.37 (summarized in Table 5.24). The eye opening is optimistic, and will have more jitter due to the aforementioned issues with the models, but is a good estimate of the distributed amplifiers 40 Gbps operation given the reasonably good match of the measured data to the simulated results.

5.2.3 The HBT three-stage cascode differential to single-ended distributed amplifier.

The S-parameters from Figure 5.38 to Figure 5.42 show more noise in both the measured and de-embedded data that comes from the measurement test bench. The test bench noise may be due to how well the picoprobes contact the pad frame and/or any dust in the adaptors and other connectors as well as ambient factors such as vibrations or noise generated by other test equipment running near by. Also, the measured open and short will introduce noise into the de-embedded S-parameters. There may also be process corner differences between the HBT three-stage cascode differential to single-ended distributed amplifier and the two f_T doubler distributed amplifiers as they were fabricated in two separate fabrication runs. However, the simulated S-parameters line up relatively closely with the measured and de-embedded results when one removes the noise on the measured data from consideration.

Figure 5.38. Measured and simulated S_{11} (dB) for the HBT three-stage cascode differential to single-ended distributed amplifier.

Figure 5.39. Measured and simulated S_{22} (dB) for the HBT three-stage cascode differential to single-ended distributed amplifier.

Figure 5.40. Measured and simulated S_{21} (dB) for the HBT three-stage cascode differential to single-ended distributed amplifier.

Figure 5.41. Measured and simulated S_{12} (dB) for the HBT three-stage cascode differential to single-ended distributed amplifier.

Figure 5.42. Calculated group delay (ps) from measured and simulated data for the HBT three-stage cascode differential to single-ended distributed amplifier.

Table 5.25 Summary for the de-embedded S-parameters, calculated group delay and power consumption of the HBT three-stage cascode differential to single-ended distributed amplifier.

Gain (dB)	$S_{11} \leq -10$ dB (GHz)	$S_{22} \leq -10$ dB (GHz)	Passband S_{12} (dB)	Group Delay (ps)	-3 dB BW (GHz)	P_{DC} (W)
12.85 ± 3.35	2.19	16.40	≤ -37.62	26.61 ± 14.26	30.71	1.11

From Table 5.25, it's clear that the HBT three-stage cascode differential to single-ended distributed amplifier has the worst input/output reflection coefficients of the three distributed amplifiers. Recall from Chapter 4, that the non-symmetrical frequency dependant load of the distributed amplifier will degrade the input/output reflection coefficients. The process variation will also impact the measured S-parameters

It's interesting to note that the measured and de-embedded S-parameters show less variation in the passband (S_{21}) and calculated group delay than the simulated results. This,

as has previously been mentioned may be do to the process corner used in the simulations. Recall, that the process corners represent the extremes of the process variation and may not exactly replicate the performance of a particular fabrication run. Also, the limitations of the device and passive models provided by ST will impact the simulation accuracy.

Figure 5.43. Measured 20 Gbps output eye for the HBT three-stage cascode differential to single-ended distributed amplifier with a 600 mV 2^9 - 4 prbs input to the test bench resulting in a 300 mV input prbs to the distributed amplifier.

Figure 5.44. Simulated 20 Gbps output eye for the HBT three-stage cascode differential to single-ended distributed amplifier with a 600 mV 2^9 - 4 prbs input to the test bench resulting in a 300 mV input prbs to the distributed amplifier.

Table 5.26 Summary for the measured 20 Gbps output eye of Figure 5.43. De-embedding data is from Table 5.20.

Eye height (mV)	Eye width (ps)	De-embedded Eye width (ps)	Jitter _{p-p} (ps)	De-embedded Jitter _{p-p}	Voltage _{p-p} (V)
459.5	30.8	35.87	19.2	14.13	2.13

Table 5.27 Summary for the simulated 20 Gbps output eye of Figure 5.44.

Eye height (mV)	Eye width (ps)	Jitter _{p-p} (ps)	Voltage _{p-p} (V)
740.8	36.13	13.87	1.74

Comparing the measured 20 Gbps eye (Figure 5.43) to the simulated 20 Gbps eye (Figure 5.44) for the HBT three-stage cascode differential to single-ended distributed amplifier it can be seen that the simulated eye height is larger than the measured eye. This is due to the previously mentioned limitations of the picoprobe and interconnect models used in the simulation as well as the source noise that is not included in the simulation.

Comparing the simulated and de-embedded peak-to-peak jitter shows a much closer match (see Table 5.26 and Table 5.27).

The data used to de-embed the source jitter from the measured jitter was collected on a different day and with a different oscilloscope. Since, the jitter numbers from the source and distributed amplifier are much larger than the oscilloscope jitter, any discrepancy seen in the jitter measurement by using a different oscilloscope or taking the measurement on a different day would be more likely to come from changes in the test bench. However, since the test bench was not changed the differences in measured jitter from day to day should not be significant and would only account for a slight variation in the measurement.

Figure 5.45. Simulated 40 Gbps output eye for the HBT three-stage cascode differential to single-ended distributed amplifier with a 600 mV 2^7-1 prbs input to the test bench resulting in a 300 mV input prbs to the distributed amplifier.

Table 5.28 Summary for the simulated 40 Gbps output eye of Figure 5.44.

Eye height (mV)	Eye width (ps)	Jitter _{p-p} (ps)	Voltage _{p-p} (V)
865.6	21.51	3.49	1.71

Given that the 20 Gbps simulated eye shows the same trends seen in the measured eye but with a larger eye opening it is reasonable to assume that the simulated 40 Gbps performance of the HBT three-stage cascode differential to single-ended distributed amplifier (Figure 5.45 and Table 5.28) is also slightly optimistic.

5.3 Summary

In this Chapter the test results for the CMOS and HBT single-ended cascoded f_T doubler distributed amplifiers and the HBT three-stage cascode differential to single-ended distributed amplifier are presented. The test data is compared with the simulated results of the distributed amplifiers. The performance of the three amplifier designs is as expected once the measurement issues are taken into account.

The off-chip de-coupling capacitors for the f_T doubler distributed amplifier artificial transmission line terminations do not take into account the 50 Ohm characteristic impedance of the picoprobe used to connect them to the pad frame and as a result the termination impedance is degraded from the desired 50 Ohms. The degraded transmission line termination accounts for some of the eye closure seen in the measured results.

The DCD present in all the 20 Gbps measurements is due to long sequences of ones and zeros. These long sequences are a product of the method used to generate the 20 Gbps signal (4 identical 5 Gbps 2^7-1 prbs signals multiplexed together to create a 20 Gbps 2^9-4 prbs) but are a real concern. Typically a feed back mechanism to dynamically correct for DC drift or signal encoding to remove long chains of ones and zeros (Signal encoding

is often used for higher data rates) are used to prevent the DC drift that creates the duty cycle distortion. Encoding the input data can also be used ensure that the data remains within a specified bandwidth.

By taking the DCD, non-ideal terminations and source noise injected into the measured results into account, it is clear that the distributed amplifiers show significant promise as drivers and pre-drivers for EOMs. It is equally clear that a 400 mV peak-to-peak input voltage is not sufficient for the distributed amplifiers to produce the desired 2 V peak-to-peak output signal. However, the HBT device distributed amplifiers can produce over 1 V peak-to-peak from a 400 mV peak-to-peak input and with the addition of a pre-driver the CMOS device distributed amplifier can do the same.

The 2 V peak-to-peak voltage swings can be obtained by adding a pre-driver to the HBT distributed amplifiers and by also adding another cascode device and increasing the supply voltage for the CMOS distributed amplifier. Recall, that the addition of the cascode device to the CMOS amplifier will also maintain the lifespan of the device that would otherwise be compromised by the increased voltage.

Chapter 6: Conclusions and Summary

The distributed amplifier is a key component in most high-speed high-bandwidth fibre optic communication systems. These amplifiers are typically implemented in the III-V technologies. Co-packaging or directly integrating silicon distributed amplifiers with existing circuitry as pre-drivers, or as possible replacements for the III-V amplifiers if/when silicon EOMS are introduced, is highly desirable. The introduction of silicon distributed amplifiers will reduce the number of packaged components and, as a result, reduce cost and losses in the link budget of the system.

The research presented in this thesis is an exploration of techniques aimed at improving the large signal output performance of silicon distributed amplifiers for use in fibre optic communication systems. The experimental verification of these techniques involve the design and implementation of three distributed amplifiers in the ST Microelectronics BiCMOS9 process [1].

The distributed amplifiers presented in this thesis use the techniques discussed in Chapters 2 and 3 to increase the bandwidth and the output voltage swing of the distributed amplifiers. In Chapter 4 a gain stage is presented that significantly increases the bandwidth of the distributed amplifier beyond what is needed for 40 Gbps operation. The extra bandwidth is sacrificed to increase the gain of the distributed amplifier by manipulating the transistor sizes of the gain stage.

6.1 Thesis Summary and Conclusions

In this thesis three distributed amplifiers were presented:

- A CMOS single-ended five-stage cascoded f_T doubler distributed amplifier.
- A HBT single-ended three-stage cascoded f_T doubler distributed amplifier.
- A HBT three-stage cascode differential to single-ended distributed amplifier.

The distributed amplifiers are intended for a 40 Gbps data rate fibre optic communication system and were designed fabricated and tested with the following specifications in mind:

- Input and output reflection coefficients (S_{11} and S_{22}) better than -10 dB for the entire passband to minimize the amplitude of the reflected waves
- Input voltage swing is at the high end of standard CML voltage levels, approximately 400 mV single-ended peak-to-peak. This level was chosen to provide as large a signal as reasonably possible to the distributed amplifier.
- Output voltage swing of at least 1 volt single-ended peak-to-peak to function as a pre-driver for an EOM, and 2 volts for a driver of a low voltage EOM. This corresponds to a voltage gain of 8 dB to 14 dB for a 400 mV peak-to-peak input signal.
- 3 dB passband from as close to DC as possible (limited by the termination capacitors to the MHz range) to a minimum upper frequency of 20 GHz for 40 Gbps data rates
- Group delay of the distributed amplifier to show as little variation as possible in the passband of the amplifier.

A performance summary of the three distributed amplifiers is given in Table 6.1.

Table 6.1. Summary for the de-embedded S-parameters, calculated group delay and power consumption of the distributed amplifiers.

	CMOS f_T doubler	HBT f_T doubler	HBT diff. to single-ended
- 10 dB Bandwidth of Input Match (GHz)	22.65	13.67	2.19
S_{12} (dB)	≤ -22.1	≤ -19.33	≤ -37.62
S_{21} (dB)	6.68 ± 0.48	12.27 ± 2.03	12.85 ± 3.35
-10 dB Bandwidth of Output Match (GHz)	21.7	31.23	16.40
-3 dB Transmission Bandwidth (GHz)	29.55	> 37	30.71
Unit Gain Freq. (GHz)	32.5	~ 48	~ 37
Group Delay (ps)	35.82 ± 14.11	33.36 ± 25.6	26.61 ± 14.26
P_{DC} (W)	0.23	0.39	1.11
Die Size (mm ²)	0.85 x 1.0	0.63 x 0.95	1.0 x 0.78

A comparison of the performance of the three distributed amplifiers shows that the HBT distributed amplifiers have more gain variation than the CMOS distributed amplifier. This is because the HBT distributed amplifiers were designed to have more gain peaking than the CMOS distributed amplifier. The peaking was added to all three distributed amplifiers in an attempt to compensate for any model limitations, add pre-distortion to address some of the attenuation present in the measurement test bench and to anticipate the difference between the large and small signal performance of the amplifiers. The low frequency peaking is due to the artificial transmission line terminations, the lower cut-off frequency of the off-chip capacitors, and the 45 MHz to 50 GHz Bias-Ts used in the measurement test bench.

The group delay variation is in large part also due to the aforementioned high and low frequency peaking but is also adversely affected by the artificial transmission line ter-

mination problem. Recall that the off-chip capacitance of the artificial transmission line terminations does not take into account the characteristic impedance of the picoprobes resulting in increased input/output reflections and a degradation of the distributed amplifier performance.

Table 6.2 and Table 6.3 summarize the large signal performance of the amplifiers for 10 Gbps and 20 Gbps respectively.

Table 6.2. Summary for the 10 Gbps measured and de-embedded large-signal data for the distributed amplifiers.

10Gbps	CMOS f_T doubler	HBT f_T doubler
Eye height (V)	1.12	1.03
Eye width (ps)	90.84	89.29
Jitter _{p-p} (ps)	9.16	10.71
Output Voltage _{p-p} (V)	2.39	2.37

Table 6.3. Summary for the 20 Gbps measured and de-embedded large-signal data for the distributed amplifiers.

20Gbps	CMOS f_T doubler	HBT diff. to single-ended
Eye height (mV)	584	459.5
Eye width (ps)	35.33	35.87
Jitter _{p-p} (ps)	14.67	14.13
Output Voltage _{p-p} (V)	1.97	2.13

The output eye diagrams of the distributed amplifiers show more closure than is desired due to the degraded transmission line terminations and test bench losses. However, the main source of eye closure for the distributed amplifier 20 Gbps output eye patterns is

the long sequences of ones and zeros in the NRZ input prbs. These long chains generate DCD in the output of the amplifiers, which closes the eye. The simulated 10 and 20 Gbps output eye diagrams of the distributed amplifiers line up reasonably well with the measured results when the afore mentioned issues are included in the simulations.

Table 6.4 summarizes the obtainable (simulated) large signal performance of the amplifiers for 40 Gbps operation with signal impairments removed.

Table 6.4. Summary for the 40 Gbps simulated large-signal data for the distributed amplifiers from Chapter 4 without the losses of the test bench, degraded transmission line termination and the long sequences of ones and zeros in the input prbs pattern.

40Gbps	CMOS f_T doubler	HBT f_T doubler	HBT diff. to single-ended
Eye height (mV)	1.26	2.2	2.24
Eye width (ps)	23.11	22.98	20.96
Jitter _{p-p} (ps)	1.89	2.02	4.04
Output Voltage _{p-p} (V)	1.86	2.97	2.86

Since the measured and simulated 10 and 20 Gbps large-signal performance of the distributed amplifiers are in reasonable agreement, it can be assumed that the simulated 40 Gbps performance summarized in Table 6.4 is also a reasonably accurate representation of the distributed amplifier performance.

It was shown in Chapter 5 that removing the test bench losses, correcting the artificial transmission line terminations and removing any long sequences of ones and zeros significantly increases the eye opening of the distributed amplifier output eye patterns. The simulated large-signal results show that all three distributed amplifiers are capable of producing eye heights over 1 volt peak-to-peak. However, the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier has just over half the small-signal gain of

the HBT distributed amplifiers, and requires a much larger input voltage than standard CML would provide. This could be addressed by adding a pre-driver to the distributed amplifier to provide the required input voltage swing. Also, adding a pre-driver to the HBT distributed amplifiers would allow them to produce over 2 volt peak-to-peak output eye heights, as can be seen in Table 6.4 where the input voltage swing to the HBT distributed amplifier test-bench is increased from 400 mV_{p-p} to 800 mV_{p-p} resulting in a 400 mV_{p-p} input to the distributed amplifier.

Although, the CMOS single-ended five-stage cascoded f_T doubler distributed amplifier does not produce the desired 2V peak-to-peak output swings, with some modification it may be able to provide the desired output swing. Using a pre-driver to compensate for the lower gain of the CMOS devices and adding another cascode device to the distributed amplifier gain stage will allow the rail voltage to be raised and consequently allow for a larger output swing.

Figure of merit for the designs in this work are given in Table 6.5.

Table 6.5 The gain bandwidth product and the modified gain bandwidth product for the distributed amplifier designs presented in this work.

	<i>GBW (GHz) at unity gain</i>	<i>MGBW</i>
CMOS cascoded f_T doubler [42]	32.5	0.72
HBT cascoded f_T doubler	~48	0.50
HBT cascode differential to single-ended	~36.79	0.38

A comparison of the measured results for the three distributed amplifiers presented in this thesis to the published amplifiers in Table 2.1 shows that the small-signal measured results are comparable to the current state of the art. However, using the MGBW in Table 6.5 as a means of comparison shows that the theoretical limit of $0.55f_{max}$ has not been reached [18]. This is to be expected, recalling that operation below peak f_T for an HBT device is desirable because higher current densities reduce the breakdown voltage of the

transistor. Therefore, the devices in the distributed amplifier gain stages were biased below peak f_T , resulting in a lower f_{max} .

Very few distributed amplifier publications include the large-signal performance. The large-signal performance of the three distributed amplifiers presented in this thesis compares very favorably to the publications in Table 2.1. Also, it should be noted that removing the various aforementioned distributed amplifier performance impediments increases the output voltage swing even further.

Although the distributed amplifiers performed well it is clear that not all the desired specifications were met and some optimization could be done to improve the group delay, gain and in the case of the differential to single-ended distributed amplifier, the input/output reflection coefficients. These improvements would increase the large-signal performance of the distributed amplifiers and while not reaching the theoretical limit would certainly improve the MGBW.

Comparing the performance of the three distributed amplifiers presented in this thesis, the f_T doubler distributed amplifiers show the most promise. However, it is obvious that for distributed amplification the III - V technologies, such as InP and GaAs, can outperform SiGe and CMOS in terms of output power, voltage swing and in some cases bandwidth. The benefits of using SiGe or CMOS for 40 Gbps applications are the cost savings and the ability to integrate the distributed amplifier with the rest of the silicon circuitry. It is important to note that although the III - V technologies can outperform silicon, the measured performance of the distributed amplifiers presented in this thesis show that both SiGe and CMOS can be used as either a driver or pre-driver for an EOM in a fibre optic system.

6.2 Thesis Contributions

In most broadband communication systems the distributed amplifier is a large signal amplifier, yet most of the available literature concentrates on the amplifiers small signal performance. When large signal metrics are presented, they are most commonly the 1 dB compression point or 3rd order intercept point. However, since the distributed amplifier is a broadband component, the 1dB compression point and the 3rd order intercept are not sufficient. There are typically a large number of frequency components present in the signal ranging from DC to the 3 dB bandwidth of the amplifier that must be accounted for.

The work presented in this thesis focused on the large-signal performance of the distributed amplifier. The device breakdown voltage, its impact on large-signal performance, device speed and linearity were presented. With the aforementioned factors the gain stage and transmission line topology were explored. All of these elements were combined with an image impedance analysis of a distributed amplifier to obtain a large-signal design.

The techniques aimed at improving the large signal output performance of silicon distributed amplifiers presented in this thesis were used to develop three distributed amplifiers. The novel use of the f_T doubler gain stage, m-derived and constant-k filter sections in the topology of two of the distributed amplifiers allowed for linearity, gain and bandwidth trade-off that would otherwise not be possible with a simpler distributed amplifier topology. The third distributed amplifier's novelty is its use as a high-speed broadband differential to single-ended converter that would either act as a pre-driver for a III-V distributed amplifier or drive the EOM itself (in the case of a silicon EOM). The three distributed amplifiers are as follows:

- A CMOS single-ended five-stage cascoded f_T doubler distributed amplifier producing better than 1V peak-to-peak output voltage swings with a bandwidth suitable for 40Gbps data rates.
- A HBT single-ended three-stage cascoded f_T doubler distributed amplifier producing better than 2V peak-to-peak output voltage swings with a bandwidth suitable for 40 Gbps data rates.
- A HBT three-stage cascode differential to single-ended distributed amplifier producing better than 2V peak-to-peak output voltage swings with a bandwidth suitable for 40 Gbps data rates.

The work done for this thesis has resulted in two publications in peer reviewed conference proceedings and an invited presentation, as indicated below. At the time the design of the f_T doubler distributed amplifier was published, no other report existed on the large signal results of a distributed amplifier design in either SiGe or CMOS using an f_T doubler gain stage combined with large signal design techniques. This work also marks the first time the relationship / trade-off between HBT device breakdown voltage and the back-off from peak f_T has been explained.

- R. Amaya, J. Aguirre, C. Plett, "Gain Bandwidth Considerations In Fully Integrated Distributed Amplifiers Implemented In Silicon," *proc. ISCAS*, pp. 273-276, Vol. 4, 2004.
- J. Aguirre, C. Plett, "Distributed Amplifier Design for Electro-Optical Applications," *Optical Networking Research Forum (ONRF)*, Ottawa, Ont., June 21-23, 2004.
- J. Aguirre, C. Plett, P. Schvan, "A 2.4V_{p-p} output, 0.045-32.5 GHz CMOS Distributed Amplifier," *Proc. IEEE Radio Frequency Integrated Circuits Symposium*, pp.427-430, June 2007.

This thesis has also influenced transmission line drivers, clock trees and CML buffers used in an ADC and DAC peer reviewed conference proceedings

- Y. M. Greshishev, J. Aguirre, et al., “A 40GS/s 6b ADC in 65nm CMOS,” *Proc. IEEE International Solid-State Circuits Conference*, pp.390-392, February 2010.
- Y. M. Greshishev, J. Aguirre, et al., “A 56GS/s 6b DAC in 65nm CMOS with 256x6b Memory,” *Proc. IEEE International Solid-State Circuits Conference*, pp.194-196, February 2011.

6.3 Future Work

Building upon the work done in this thesis, a number of research investigations and improvements to the distributed amplifier designs can be explored:

The off-capacitor used in the artificial transmission line terminations was not properly implemented to take into account the characteristic impedance of the picoprobe. In chapter 5, a termination that presents the proper terminations to the picoprobe was proposed but a passive resistor does not account for the frequency dependence of the characteristic impedance of the artificial transmission lines. An opportunity exists to explore different transmission line terminations in an effort to better match the frequency dependent termination. There may also be a means of reducing the impact of the artificial transmission line imperfections with an exploration of the constructive voltage and current effects present in the artificial transmission lines themselves.

Another avenue of exploration would be to improve the pass band gain, linearity and group delay of the distributed amplifiers by compensating for the internal gain-stage parasitics. Also, it would be of interest to explore programmable gain as well as programmable impedance matching as a means of dealing with variation due to process, temperature and supply voltage changes.

The distributed amplifiers presented in this thesis experienced duty cycle distortion which resulted in significant closure of the output eye. The output DC value experienced drift caused by long chains of ones and zeros shifting the output DC level. Assuming non-return to zero line code it is common practice to encode the prbs data to remove long sequences of ones and zeros to in turn prevent significant DCD. Another solution could be to use return to zero line code which return to zero after each pulse thus eliminating the long uninterrupted sequences of ones or zeros. However, it would still be of interest to explore feed-forward or feed-back techniques to remove or reduce the DCD.

A differential distributed amplifier has performance advantages over a single-ended implementation but requires four artificial transmission lines. These input/output transmission lines are difficult to realize without occupying significant layout area. An investigation of different types of coupled lines, such as a cross coupled pairs or offset pairs, may provide a solution.

Finally, it It would also be of interest to apply the techniques presented in this thesis to other circuits, such as high frequency active filters and variable gain amplifiers.

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