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THEORETICAL AND EXPERIMENTAL
ANALYSIS OF DOUBLE-DIFFUSED
MOS TRANSISTORS

by

© Donald B. Treen

B.A. Sc., University of Toronto, 1969

M. Eng., Carleton University, 1971

A thesis submitted to the Faculty of Graduate Studies
and Research in partial fulfillment of the requirements
for the degree of

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ABSTRACT

Inadequacies of present DMOS transistor models are highlighted showing the need for a new physical model which is analytic and which applies to all modes of operation. It is shown that the most suitable conventional MOS theory to use as a basis for the model is that of El-Mansy and Boothroyd.

DMOS fabrication is described and theoretical predictions are made for the lateral diffused profile of the devices fabricated at Carleton University. A simple exponential model for the graded profile region is then introduced.

An analytical model for the graded region is developed based on the profile model. This leads to an overall DMOS transistor model which is regionally analytic (implicitly requires some iterations to obtain solution for several regions simultaneously, each of which is itself analytic). Computer simulations using this model show good agreement with measured device characteristics over a wide range of operating conditions, including those which cause saturation in more than one region simultaneously (short channel effects are not included in the model since these effects are much less pronounced in a DMOS device with its heavily doped channel region than in a uniform channel device of the same physical dimensions).

The undersigned recommend to the Faculty of Graduate Studies and
Research the acceptance of the thesis:

"THEORETICAL AND EXPERIMENTAL ANALYSIS OF DOUBLE-DIFFUSED MOS
TRANSISTORS"

submitted by Donald Bruce Treen in partial fulfillment of the requirements
for the degree of Doctor of Philosophy.

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LIST OF PRINCIPAL SYMBOLS

Note that normalized voltages, denoted by U , are in units of thermal volts (units of kT/q).

a	$\frac{C_i}{C_D} e^{-U_f/2}$
C_D	ϵ_s/L_D , intrinsic Debye capacitance per unit area
C_i	ϵ_i/x_i , insulator capacitance per unit area
C_{gs}	gate capacitance per unit area
D_p, D_B	diffusion coefficient for phosphorous and boron impurities, respectively
D_n	diffusion coefficient for mobile electrons
E_c	critical field for carrier velocity saturation
E_{xs}	electric field normal to the surface
E_{ys}	longitudinal electric field at the surface
g_d	drain conductance
g_m	gate transconductance
I_d	drain current
J_n	electron current density
J_p	hole current density
k	Boltzmann's constant
L	channel length
L_D	intrinsic Debye length
ΔL	length of drain space charge region in current saturation model
n_i	intrinsic carrier concentration
n	electron concentration

LIST OF PRINCIPAL SYMBOLS (cont'd)

N	net doping
N_p	peak doping in the DMOST diffused channel
N_B	bulk doping concentration
N_0	surface concentration of impurities at $x=0$, $y=0$
p	hole concentration
q	electronic charge
Q_b	ionized charge in the surface space charge region per unit area
Q_g	gate charge per unit area
Q_m	mobile inversion layer charge per unit area
Q_s	$(Q_m + Q_b)$, total charge in the semiconductor surface space charge region per unit area
Q_{ss}	effective surface state charge density (includes charge in insulator)
t	time
T	temperature ($^{\circ}K$)
U	normalized electrostatic potential
U_{bs}	normalized applied substrate potential
U_f	normalized Fermi potential
U_{fp}, U_{fb}	normalized Fermi potential at the point of peak doping and the bulk, respectively
U_g	normalized effective gate potential
U_{gg}	normalized applied gate potential
U_n, U_p	normalized electron and hole quasi-Fermi potentials, respectively
U_s	normalized surface potential
U_{ss}, U_{sd}	value of U_s at the source and drain, respectively

LIST OF PRINCIPAL SYMBOLS (cont'd)

U_{sp}, U_{sm}	pinch-off surface potential (normalized)
V_{bs}	applied substrate voltage
V_d	applied drain voltage
V_g	effective gate voltage
V_{gg}	applied gate voltage
v_{sd}	drift velocity of mobile carriers
v_{sm}	scatter limited velocity of mobile carriers
x	distance normal to the surface measured from the silicon-oxide interface
x_d	thickness of space charge region from the depletion approximation
x_i	insulator thickness
x_m	thickness of surface inversion layer
x_s	thickness of model space charge region
y	distance along the channel measured from the source junction
y_d	distance of drain junction from source junction
y_p	distance from source junction to the point of peak doping
y_1	distance from source junction to the end of Region 1
y_2	distance from the source junction to the end of Region 2 (graded region)
y_3	distance from source junction to end of Region 3
y_4	y_d
y_T	distance from source junction to transition point in Region 2
z	width of the gate

LIST OF PRINCIPAL SYMBOLS (cont'd)

η	$a(U_g - U_s), U_b = 0$
ϵ_i, ϵ_s	permittivities of the insulator and silicon, respectively
ρ	space charge density
μ, μ_n	mobility of electrons
δ	separation of quasi-Fermi potentials in conventional theory and normalized effective channel potential in the model

CHAPTER 1

INTRODUCTION

1.1 Background

In the past decade, technological advances in the silicon planar process have resulted in ultra-reliable MOS (Metal Oxide Semiconductor) transistors and a wide variety of high-density, low-cost integrated circuits. They have not only found application in existing products but have made possible a whole new range of products heretofore thought to be not ~~feasible~~, e.g. pocket calculators, digital watches, semiconductor ROMs and RAMs, microprocessors.

In order to achieve higher density integrated circuits, channel lengths have been reduced and junctions made shallower. However, short channel effects such as high saturation drain conductance and low punch-through voltage become increasingly important. These effects can be reduced somewhat by surface channel ion implantation but subsurface punch-through from source to ~~drain~~ drain remains a problem.

A new type of MOS transistor that achieves very short channel lengths using conventional processing techniques, while at the same time maintains high breakdown voltage capability, was first announced nearly a decade ago [1], [2]. Named Double-Diffused MOS Transistors (DMOST), they have found application as gigahertz discrete transistors, nanosecond high-density low-power logic elements [9], and high-voltage power transistors.

The short channel length of a DMOS transistor is obtained by making successive p-type and n-type diffusions through the same oxide window into a lightly doped p-type substrate. The resulting profile along the surface from source to drain consists of a short p-type graded region, followed by a relatively long region with constant doping, as shown in Fig. 1.1,

The grading of the profile gives the DMOS transistor its unique characteristics and has complicated the task of modelling its behaviour. It is the purpose of this thesis to investigate the DMOS modelling problem with an aim to developing a model that not only is accurate but is also an efficient design tool in computer-aided device design.

To date, DMOS models can be classified into three different categories, depending on the approach taken:

- 1) the Velocity Saturation Model [1]
- 2) the Enhancement-Depletion Model [3], [4]
- 3) the Graded-Doping Model [5], [6].

As will be discussed in Chapter 4, each of these models has its merits and aids in the overall understanding of device behaviour but tends to be either too simplistic, and thus is severely limited in its range of application, or is too numerically cumbersome to be useful.

Conventional first-order MOS theory, which assumes that the channel is strongly inverted and consists of a spike of charge at the surface, is inadequate when modelling either the weak channel or the high current level regions of operation. Even in its most complete form [8], where rather than a spike at the surface the channel charge distribution is assumed to be Boltzmann, the results are essentially the

Fig. 1.1. DMOST cross-section and doping profile.

same at high current levels. This discrepancy is due, not to the assumptions of constant carrier mobility or the Gradual Channel Approximation (GCA), but to an underestimation of the contribution that the mobile channel charge makes to the surface potential. This, in turn, can be attributed to the choice of models used for this mobile charge distribution. The choice is necessarily limited to those which are analytically solvable and thus have limited accuracy.

In his search for a model which was accurate over the complete range from weak inversion to high current operation, El-Mansy [7], [40] made a rectangular or constant carrier density approximation to the distribution in the channel region and, using appropriate boundary conditions, obtained the drain current and other related device parameters in closed form. His results showed better agreement with experiment than Pao and Sah's [8] over the full range of operation from very weak to very strong channel conditions even though Pao and Sah resorted to numerical techniques to achieve the rigor necessary in obtaining accurate results. It should be noted here that both theories include the effects of diffusion current which is neglected in the simple first-order theory.

Not only does the closed-form nature of El-Mansy's model make it easy to use in CAD applications but in it the physical device parameters remain 'visible' which greatly simplifies the task of analyzing the results in terms of how they are affected by device design.

In addition, El-Mansy's formulation allows solution in closed-form when field-dependent mobility is included and he has developed a relatively simple two-dimensional saturation model which, when used in

conjunction with the non-saturation model, gives a complete representation of device operation [40], [41]. This is extremely useful when modelling short channel devices, especially those with lightly-doped substrates where two-dimensional effects may dominate in saturation and where longitudinal fields along the channel may, at some point, exceed the level required to cause carrier velocity saturation.

Due to its short effective channel length and non-uniform substrate doping density, it is to be expected that DMOS transistors exhibit one or both of the above effects throughout a wide range of operating conditions and it is therefore imperative that a model be used which incorporates these effects while achieving as high a level of accuracy as possible without departing from a closed-form analytic formulation. Although the graded nature of the substrate impurity profile complicates the task significantly, El-Mansy's model best meets the stated requirements and will be the basis of the DMOS modelling effort reported here.

1.2 Thesis Objective

In the pursuit of an accurate physical model to predict DMOS characteristics, the following approach will be taken. First of all, a detailed analysis is done of the diffused channel impurity profile so that the subsequent modelling of this profile retains the most important features while at the same time reduces the mathematical complexity. Next, physical regions of the device which can be modelled as separate units are identified and closed-form models are proposed for them. Considerable attention is paid to the region which has variable doping since this

region previously had no closed-form model and the approach taken here to model this region differs markedly from those reported elsewhere. Once established, the models are combined in an efficient computer program in order to compute device characteristics.

1.3 Outline of the Thesis

In Chapter 2, the fundamental equations describing semiconductor device operation are used to develop the conventional first-order theory of MOS device operation. El-Mansy's theory is then examined and the most pertinent features are pointed out.

In Chapter 3, fabrication of DMOS transistors is outlined and process design considerations are described in relation to the fabrication process used at Carleton University to produce experimental DMOS transistors.

In Chapter 4, previous DMOS models are examined and their advantages and disadvantages are discussed.

In Chapter 5, the exponential model for impurity grading is shown to satisfy well the requirements that the parameters peak doping, impurity profile gradient, and diffused channel length are represented in a mathematically simple form. It is shown that El-Mansy's model loses its 'integrability' when applied to a graded channel. By considering the relationship between Fermi level, effective gate voltage, and surface potential in a heavily-inverted graded region, an exponential charge model is developed. This model is valid up to a pinch-off point which is dependent on the applied gate and drain voltages in addition to the para-

meters of the impurity grading model. It facilitates a good approximation for current to be made without resorting to numerical integration.

In the type of DMOS transistor assumed in this study, there is a portion of the lightly-doped drain (drift) region which is purposely not covered by gate metal in order that the effects of this region on device characteristics may be investigated. A suitable model which allows carrier velocity saturation to occur is developed for this region.

In Chapter 6, theoretical calculations of device characteristics are presented and are compared to those measured on the experimental devices.

In Chapter 7, conclusions are drawn concerning the accuracy of the model and the correlation between device design and its terminal electrical characteristics.

CHAPTER 2

MOS THEORIES

2.1 MOST Structure

In this Chapter, the conventional uniform channel MOS transistor is described and various theories for its operation are developed from the basic semiconductor equations. In Fig. 2.1, the cross-section of an n-channel MOS transistor is shown both along its channel and normal to it. The situation depicted is one of non-equilibrium where the applied gate voltage U_{gg} has inverted the underlying p-type surface and the drain voltage U_d causes current I_d to flow along the conducting channel. The potential distributions are also shown along the surface in the y-direction and into the substrate in the x-direction for some value of y between source and drain. All quantities are assumed to be fixed with respect to the third spatial variable z since the planar fabrication process ensures uniformity of device physical parameters in this direction and all field lines emanating from the electrodes are confined to the x-y plane.* Thus, the device width Z can be treated as a scale factor where required in all subsequent discussion.

The various physical parameters and potentials shown in Fig. 2.1 are defined as follows (all potentials are normalized by the thermal voltage kT/q):

$U = U(x,y)$, the electrostatic potential

$U_s = U(0,y)$, the electrostatic potential at the semiconductor-insulator interface

* Narrow channel effects encountered in VLSI devices are not included.

Fig. 2.1. Cross-section of an n-channel MOS transistor.
 (a) along the channel and
 (b) normal to the channel

U_p = the quasi-Fermi potential for holes

U_n = the quasi-Fermi potential for electrons

$\delta = U_n - U_p$, the separation between quasi-Fermi potentials of electrons and holes at the surface

U_f , U_{f_s} , U_{f_d} , the Fermi potentials of the substrate, source, and drain, respectively

U_{gg} , U_d , the applied gate and drain potentials, respectively

U_g = the effective gate voltage (applied minus the flat-band voltage)

I_d = the drain current (defined as positive as shown for an n-channel device)

x_i = the insulator (oxide) thickness

L = the channel length

2.2 The Fundamental Semiconductor Equations

In developing a theory of MOS transistor operation, we must determine the spatial distributions of mobile carriers and electrostatic potentials in the surface space charge region with device physical constants as parameters and then determine a unique solution by applying boundary conditions determined by the externally applied voltages. The space charge region in question is bounded in the y-direction by the source and drain junctions (assumed to be abrupt) and in the x-direction by the semiconductor surface and the edge of the depletion layer which extends into the substrate.

Another space charge region exists in the gate oxide and by solving for the electrostatic potential distribution in this region the effect of

gate voltage on the semiconductor surface potential can be found by matching the boundary conditions of the two space charge regions at the semiconductor-insulator interface.

The fundamental semiconductor equations which must be solved in these space charge regions are:

i) Poisson's equation

$$\nabla^2 U = - \frac{q}{kT\epsilon} \rho \quad (2.1)$$

where

$$\frac{\rho}{\epsilon} = \frac{q(p-n-N)}{\epsilon_s} \quad \text{in the semiconductor}$$

and

$$\frac{\rho}{\epsilon} = \frac{\rho_i}{\epsilon_i} \quad \text{in the insulator.}$$

ii) Current continuity equations

$$\nabla J_n = -R$$

$$\nabla J_p = R$$

where

$$J_n = - qD_n n \nabla U_n$$

$$J_p = - qD_p p \nabla U_p$$

(2.2)

The solutions for these equations are subject to the following boundary conditions:

i) At the semiconductor-insulator interface ($x=0$)

$$a) U_i = U_s$$

$$b) \epsilon_i \left. \frac{\partial U}{\partial x} \right|_i = \epsilon_s \left. \frac{\partial U}{\partial x} \right|_s + \frac{q}{kT} Q_{ss} \text{ (Gauss' law)}$$

$$c) \frac{\partial U_n}{\partial x} = \frac{\partial U_p}{\partial x} = 0 \text{ (zero normal current)}$$

where Q_{ss} is the surface state charge density.

ii) At the neutral substrate boundary ($x=x_d$)

$$a) U=0 \text{ (for the reference potential chosen here)}$$

$$b) \frac{dU}{dx} = 0$$

iii) At the source junction ($y=0$)

$$\delta = U_n - U_p = 0 \text{ (source grounded)}$$

iv) At the drain junction ($y=L$)

$$\delta = U_d$$

v) At the gate boundary ($x=-x_i$)

$$U = U_{gg} - U_{FB} = U_g$$

where δ is the channel potential or difference between electron and hole quasi-Fermi potentials, and U_{FB} is the normalized flat-band voltage.

2.3 Conventional One-Dimensional MOS Transistor Theory

2.3.1 Non-Saturation Drain Current

In order to solve the above system of partial differential equations, some relationship must be assumed between mobile carrier concentration and potential. The usual assumption is that Boltzmann statistics apply:

$$n = n_i \exp(U - U_n)$$

$$p = n_i \exp(U_p - U)$$

(2.3)

These relations are valid as long as the exponent in either expression does not approach half the bandgap, i.e. non-degenerate conditions are assumed.

Further to this, the following are also generally assumed:

- i) The majority carrier quasi-Fermi level is constant and equal to the Fermi level, i.e. for n-channel devices, $J_p = 0$.
- ii) Mobility is constant, independent of both field and impurity doping level.
- iii) The net-generation recombination rate (R) is zero.
- iv) The charge which is distributed in the insulator can be represented by an equivalent charge

$$Q_i = \int_{-x_i}^0 \frac{x}{x_i} \rho_i(x) dx$$

located at the semiconductor insulator interface. It is then com-

bined with the surface state charge Q_{ss} to obtain an equivalent value for Q_{ss} which is used to calculate the flat-band voltage [18].

The above boundary-value problem can now be solved using various numerical techniques [11-16] to obtain device electrical characteristics over a wide operating range. These solutions are, however, limited in their usefulness due to their complexity.

Of primary consideration in the search for an analytical solution of the above equations is to reduce Poisson's equation (2.1) to a first-order ordinary differential equation. As first proposed by Shockley [17], for the JFET, the "Gradual Channel Approximation" (GCA) neglects the contribution to channel charge of the field gradient along the channel, i.e. $\partial^2 U / \partial y^2 = 0$. Thus, Eqn. (2.1) becomes:

$$\frac{d^2 U}{dx^2} = - \frac{q^2 n_i}{kT\epsilon_s} \left[e^{U_p - U} - e^{U - U_n} + e^{-U_f} - e^{U_f} \right] \quad (2.4)$$

Integrating Eqn. (2.4) from the bulk toward the surface gives the relation between the normal electric field and potential:

$$E_x = - \frac{dU}{dx} = \frac{1}{L_D} \cdot F(U, \delta, U_f) \quad (2.5)$$

where

$$F(U, \delta, U_f) = \left[e^{U - \delta - U_f} + e^{U_f - U} + (U - 1)e^{U_f} - (U + e^{-\delta})e^{-U_f} \right]^{1/2} \quad (2.6)$$

and

$$L_D = \left[\frac{kT\epsilon_s}{2q^2 n_i} \right]^{1/2}$$

is the intrinsic Debye length.

If we now express the effective gate voltage (U_g) in terms of the applied gate voltage and the flat-band voltage,

$$U_g = U_{gg} - \frac{q}{kT} \phi_{ms} + \frac{q}{kT} \frac{Q_{ss}}{C_i} \quad (2.7)$$

where ϕ_{ms} is the metal-semiconductor work-function difference and

$$C_i = \epsilon_i / x_i$$

then we can employ Gauss' law to express Q_g in terms of the surface potential U_s :

$$Q_g = \epsilon_i E_i = \frac{kT}{q} \frac{\epsilon_i}{x_i} (U_g - U_s) \quad (2.8)$$

where Q_g is the charge on the gate electrode supported by the field in the insulator. Applying Gauss' law again in the semiconductor yields:

$$Q_s = \epsilon_s E_{xs} = \frac{kT}{q} \frac{\epsilon_s}{L_D} F(U_s, \delta, U_f) \quad (2.9)$$

where Q_s is the total semiconductor charge consisting of both mobile carrier inversion layer charge, Q_m , and fixed ionized bulk charge, Q_b . From charge neutrality, we have $Q_g = -Q_s$ and combining Eqns. (2.8) and (2.9), we get [8]:

$$U_g = U_s + \frac{C_D}{C_i} F(U_s, \delta, U_f) \quad (2.10)$$

where

$$C_D = \epsilon_s / L_D$$

The mobile inversion layer charge for an n-channel device is given by:

$$Q_m = -q \int_0^{x_d} n dx = -qn_i \int_0^{x_d} e^{U - \delta - U_f} dx$$

$$\begin{aligned}
 &= qn_i \int_0^s \frac{e^{U-\delta-U_f} dU}{dU/dx} \\
 &= - \left(\frac{kT}{q} \right) \cdot \left(\frac{\epsilon_s}{2L_D} \right) \int_0^s \frac{e^{U-\delta-U_f}}{F(U, \delta, U_f)} dU
 \end{aligned} \tag{2.11}$$

where x_d is the point in the bulk where $U=0$ and n becomes negligible.

Using the current density equation (2.2), the drain current can be obtained by integrating:

$$\begin{aligned}
 I_d &= \int_0^{x_d} J_n(x, y) Z dx \\
 &= - Z D_n Q_m \frac{d\delta}{dy}
 \end{aligned} \tag{2.12}$$

or

$$I_d = \left(\frac{kT}{q} \right)^2 \left(\frac{Z}{2L} \right) \cdot \mu_n C_D \int_0^{U_d} \int_0^{U_s} \frac{e^{U-\delta-U_f}}{F(U, \delta, U_f)} dU d\delta \tag{2.13}$$

where μ_n is the electron mobility which is related to the electron diffusion coefficient by the Einstein relation $D_n = (kT/q)\mu_n$.

The integral in Eqn. (2.13) cannot be obtained analytically and must be evaluated numerically [8] if no further approximations are to be made. In the remainder of this section, the standard assumptions and approximations are made to illustrate the development of conventional analytical theory.

Since the charge neutrality condition states that

$$Q_g = - Q_s = - (Q_m + Q_b)$$

then we can write:

$$\begin{aligned}
 Q_m &= - (Q_g + Q_b) \\
 &= - \frac{kT}{q} C_i (U_g - U_s) + qn_i e^{U_f} X_d
 \end{aligned}
 \tag{2.14}$$

where X_d is the depletion region width.

If we now assume that the inversion layer charge Q_m is highly localized at the surface (the "Shallow Channel Approximation") [19-21], then we can use the depletion approximation to relate the surface potential to the depletion region width. Therefore, neglecting mobile carriers and also assuming that the substrate is sufficiently extrinsic that $e^{U_f} \gg e^{-U_f}$, Eqn. (2.4) becomes:

$$\frac{d^2 U}{dx^2} = \frac{q^2 n_i}{kT \epsilon_s} e^{U_f}
 \tag{2.15}$$

Integrating once gives us the normal surface field in terms of the substrate doping and the depletion width:

$$E_{X_s} = \frac{qn_i}{\epsilon_s} e^{U_f} X_d$$

and

$$\frac{dU}{dx} = \frac{q^2 n_i e^{U_f}}{kT \epsilon_s} (X - X_d)
 \tag{2.16}$$

A second integration yields:

$$U = U_s + \frac{q^2 n_i e^{U_f}}{kT \epsilon_s} \left(\frac{x^2}{2} - xX_d \right)
 \tag{2.17}$$

By setting $X=X_d$ and $U=0$ in Eqn. (2.17), we obtain:

$$X_d = \left[\frac{2kT\epsilon_s}{q^2 n_i} e^{-U_f/U_s} \right]^{1/2} \quad (2.18)$$

Substituting Eqn. (2.18) into Eqn. (2.14) yields:

$$Q_m = -\frac{kT}{q} C_i (U_g - U_s) + (2kT\epsilon_s n_i e^{U_f/U_s})^{1/2} \quad (2.19)$$

This expression for Q_m may be used in the current equation (2.12) but it still cannot be integrated unless some relationship between U_s and δ is assumed. It is usual to assume that diffusion current may be neglected as compared to drift current so that $d\delta/dy = dU_s/dy$ in Eqn. (2.12) and δ and U_s are thus linearly related. This relationship must take on an explicit form so that the integral may be evaluated at the source and drain boundaries. It is usual to assume that no current flows until the surface is strongly inverted to the point where the inversion charge density is equal to the majority carrier concentration in the substrate. The relationship is then:

$$U_s = \delta + 2U_f, \quad (2.20)$$

although it is more accurate to assume that [21]:

$$U_s = \delta + U_{ss}$$

where U_{ss} is the surface potential at the source obtained by setting $\delta=0$ in Eqn. (2.10).

Using Eqns. (2.20) and (2.19), we now obtain the drain current by integrating Eqn. (2.12) from the source to the drain:

$$I_d = \left(\frac{kT}{q}\right)^2 \cdot \frac{Z}{L} \cdot \mu_n C_i \left[(U_g - 2U_f - U_d/2)U_d - \frac{2}{3} \left(\frac{2q^2 \epsilon_s N}{kT C_i^2} \right)^{1/2} \cdot \left\{ (U_d + 2U_f)^{3/2} - (2U_f)^{3/2} \right\} \right] \quad (2.21)$$

where $N = n_i e^{U_f}$.

Equation (2.21) predicts that for a given U_g the drain current will first increase linearly with drain voltage (the linear region) and will then gradually level off as it approaches a saturated value (the saturation region). In the linear region, U_d is small and Eqn. (2.21) can be approximated for $U_d < 2U_f$ by expanding the third term in a series to give:

$$I_d \approx \left(\frac{kT}{q}\right)^2 \cdot \frac{Z}{L} \mu C_i \left[U_g - 2U_f - U_d/2 - \left\{ \frac{2q^2 \epsilon_s N(2U_f)}{kT C_i^2} \right\}^{1/2} \right] U_d \quad (2.22)$$

From Eqn. (2.22), it can be seen that, for any value of U_d , the drain current is reduced to zero when:

$$U_g = 2U_f + \left\{ \frac{2q^2 \epsilon_s N(2U_f)}{kT C_i^2} \right\}^{1/2} \quad (2.23)$$

This forms the basis for defining the familiar term "threshold voltage" which, in terms of applied gate voltage, is:

$$V_T = V_{FB} + 2\phi_f + \left\{ \frac{2\epsilon_s qN(2\phi_f)}{C_i^2} \right\}^{1/2} \quad (2.24)$$

and Eqn. (2.22) becomes;

$$I_d = \frac{Z}{L} \mu C_i \left[(V_{gg} - V_T) V_d + \frac{V_d^2}{2} \right] \quad (2.25)$$

for $V_d < (V_{gg} - V_T)$.

An n-channel device with a positive threshold voltage is commonly referred to as an enhancement transistor. If it has a negative threshold voltage, it is a depletion transistor.

2.3.2 Saturation Drain Current

Equation (2.25) is valid only up to the saturation point which may be found either by setting $Q_m = 0$ at the drain or by finding the value of U_d at which I_d as given by Eqn. (2.25) reaches a maximum. If it is assumed that Eqn. (2.25) is valid up to the saturation point, then the saturation drain voltage is given by:

$$V_{d_{sat}} = V_{gg} - V_T \quad (2.26)$$

Since the assumption that $U_d < 2U_f$ no longer applies in saturation, Eqn. (2.26) is valid only when N is small (lightly doped substrates) and C_i is large (thin oxides) for which the threshold voltage becomes:

$$V_T = V_{FB} + 2\phi_f \quad (2.26a)$$

The drain current in saturation then can be written:

$$I_{d_{sat}} = \frac{Z}{L} \mu C_i \frac{(V_{gg} - V_T)^2}{2} \quad (2.27)$$

which is a constant, independent of drain voltage. Eqn. (2.27) predicts that the drain conductance is zero in saturation although experimentally this is not observed.

The theory presented above breaks down in the saturation region because it assumes that the Gradual Channel Approximation is valid along the entire length of the channel from source to drain. However, for any fixed values of gate and drain voltages (non-equilibrium), we can see that as we proceed along the channel towards the drain the mobile inversion layer charge Q_m decreases and the longitudinal surface field increases in order that current continuity prevails (assuming negligible diffusion current). As the drain voltage is increased, the longitudinal field gradient also increases until it influences the charge in the surface space charge region and the GCA becomes invalid over a significant portion of the channel length adjacent to the drain junction for drain voltages comparable to the gate voltage. It is usual to divide the saturated channel into two sections, the source section where the GCA is valid and the drain section where two-dimensional space charge effects cannot be neglected. The potential at the end of the source section is taken to be the drain voltage at the onset of saturation given by Eqn. (2.26):

$$V_{d_{sat}} = V_{gg} - V_T \quad (2.26)$$

where a more accurate relationship defining the threshold voltage may be obtained by setting $Q_m=0$, in Eqn. (2.19) with $U_s = q/kT (V_{d_{sat}} + 2\phi_f)$. Equation

(2.19) then becomes:

$$C_i(V_{FB} - V_{gg} + V_{d_{sat}} + 2\phi_f) + \sqrt{2\epsilon_s qN(V_{d_{sat}} + 2\phi_f)} = 0.$$

Solving for $V_{d_{sat}}$ yields:

$$V_{d_{sat}} = V_{gg} - V_{FB} - 2\phi_f + \frac{\epsilon_s qN}{C_i^2} \left[1 - \sqrt{1 + \frac{2C_i^2(V_{gg} - V_{FB})}{\epsilon_s qN}} \right] \quad (2.28)$$

Comparing Eqn. (2.28) with (2.26) leads to an expression for V_T which reduces to Eqn. (2.26a) when N/C_i^2 is small, i.e. when $X_d \gg X_i$.

Even though $V_{d_{sat}}$ is defined, the length of the source section is yet to be determined. Various models ("Channel Shortening Models") have been proposed ranging from two-dimensional numerical solutions for the drain section [13,24] to simple one-dimensional solutions [22,23] which may include the use of empirical parameters to obtain better agreement with measured results [25-27].

The value of surface potential at which the channel "pinches off", corresponding to $V_{d_{sat}}$ given by Eqn. (2.28), can be written as:

$$U_{sp} = (U_g + U_A) - \sqrt{(U_g + U_A)^2 - U_g^2} \quad (2.29)$$

where

$$U_A = \epsilon_s q^2 N / kTC_i^2.$$

When the drain voltage is increased so that the drain surface potential U_{sd} rises above U_{sp} then a depletion region of length ΔL is

developed between the drain and the end of the channel leading to an effective channel length $L' = L - \Delta L$ which is less than the non-saturated channel length. The length of the drain region ΔL is determined from the solution of Poisson's equation in that region. The simplest theory uses step $n^+ - p$ junction theory and states that the length ΔL is equal to the depletion width of a reverse-biased junction with the potential $(U_{sd} - U_{sp})$ across it. Therefore, ΔL is given by:

$$\Delta L = \sqrt{\frac{2\epsilon_s kT}{q N} (U_{sd} - U_{sp})} \quad (2.30)$$

Not only does Eqn. (2.30) neglect the field at the end of the source section but it also neglects the contribution of mobile carriers to the field in the drain section. Both approximations cause an over-estimation of ΔL for all applied voltages. In addition, by neglecting the influence of the gate electrode, the rate of change of ΔL due to a change in drain voltage is also overestimated. Thus, this analysis is only valid in the case of high substrate doping and low gate voltages or current levels.

Once the value of ΔL has been determined, the drain current in saturation is given by:

$$I_d = \frac{I_{d\text{sat}}}{(1 - \Delta L/L)} \quad (2.31)$$

where $I_{d\text{sat}}$ is the drain current at pinch-off, i.e. when $U_{sd} = U_{sp}$, calculated using one of the first-order model relationships such as Eqn. (2.27) or (2.28).

2.4 El-Mansy's Model [7]

Due to the inadequacies of the model presented in the last section, there have been continued efforts to develop a new analytical MOS transistor model which gives accurate results for all regions of operation including subthreshold, high level, and saturation. Even the most complete non-saturation model to date [8], which is not analytical, is not accurate at high level (strong inversion). Under these conditions, the usual procedure is to use an empirical relationship between mobility and gate voltage to account for the apparent mobility reduction under the influence of high (transverse) gate fields. While it is indisputable that the gate field has some high-level effect on surface mobility, the arbitrary use of this curve-fitting technique gives the required accuracy for one device parameter, drain conductance, but fails to provide a significant increase in accuracy for other device parameters such as gate transconductance, g_m , and gate capacitance, C_{gs} . El-Mansy has shown that a model for the surface inversion layer charge which includes the effect of this charge on the surface potential, provides better agreement than previous theories for all the device parameters mentioned above even though a constant value for surface mobility is used. This channel model is formulated in such a way that solutions for the device terminal characteristics remain analytical.

2.4.1 Non-Saturation Region of Operation

If the distribution of mobile carriers in the surface inversion layer is approximated by a rectangle of finite height and width X_m [7], as shown in Fig. 2.2, then by integrating the one-dimensional Poisson's equation normal to the surface from $X=0$ to $X=X_d$, we get the surface potential:

$$U_s = - \frac{q}{2kT\epsilon_s} (Q_m X_m + Q_b X_d) \quad (2.32)$$

If we now define an equivalent rectangular space charge region of width X_s (see Fig. 2.2) such that $Q_s = Q_m + Q_b$ and with the same surface potential as above (Eqn. (2.32)) given by:

$$U_s = - \frac{q}{2kT\epsilon_s} Q_s X_s \quad (2.33)$$

then the essential features of the original space charge region are retained viz. U_s and Q_s .

The constant space charge density normal to the surface gives rise to a parabolic variation in potential in that region. The form is chosen to be:

$$U = U_s \left(1 - \frac{X}{X_s} \right)^2 \quad (2.34)$$

in order that at $X=X_s$ we have $\frac{dU}{dx}=0$ and $U=0$ (boundary condition (ii)).

We may now use the requirement that the electric displacement vector be continuous across the semi-conductor-insulator interface to

Fig. 2.2. Representation of the 'actual' surface space charge distribution and its equivalent 'model space charge'.

obtain the model space charge region thickness X_s :

$$\epsilon_s \left. \frac{dU}{dx} \right|_{x=0} = \epsilon_i \left. \frac{dU}{dx} \right|_i \quad (2.35)$$

where

$$\epsilon_s \left. \frac{dU}{dx} \right|_{x=0} = -2 \frac{\epsilon_s U_s}{X_s}$$

and

$$\epsilon_i \left. \frac{dU}{dx} \right|_i = -C_i (U_g - U_s)$$

Therefore,

$$X_s = \frac{2U_s}{\frac{C_i}{\epsilon_s} (U_g - U_s)} \quad (2.36)$$

Since the gate charge is given by:

$$Q_g = \frac{kT}{q} C_i (U_g - U_s) \quad (2.37)$$

and charge neutrality requires that $Q_g = -Q_s$, we can see that Eqn. (2.36) is consistent with Eqn. (2.33). This charge neutrality condition also allows us to calculate $Q_m = -(Q_g + Q_b)$, where

$$Q_b = -qNX_s = -qn_i e^{U_f} \cdot \frac{2U_s}{\frac{C_i}{\epsilon_s} (U_g - U_s)} \quad (2.38)$$

Therefore,

$$Q_m = -\frac{kT}{q} C_i (U_g - U_s) + qn_i e^{U_f} \cdot \frac{2U_s}{\frac{C_i}{\epsilon_s} (U_g - U_s)} \quad (2.39)$$

So far, we have developed expressions for the potential, space charge region width, and mobile charge in Eqns. (2.34), (2.36) and (2.39), respectively. These correspond to Eqns. (2.17), (2.18) and (2.19) of the conventional theory.

Even though the values of X_m and X_d are not known for the original space charge distribution as defined by Eqn. (2.32), certain conclusions regarding their relationship may be made. When the surface is depleted but not inverted, we have $n \ll N$ and $Q_m \ll Q_b$. Therefore, the semiconductor charge is dominated by the bulk charge term and we have $X_s = X_d$. As U_s is increased by increasing U_g , X_d increases and we still have $X_s = X_d$ until at some point Q_m becomes comparable in magnitude to Q_b . From this point on, Q_m increases rapidly with surface potential and more of the potential drop in the space charge layer is attributed to Q_m . Therefore, in this model, x_d is not assumed constant in strong inversion but must necessarily decrease and X_m increase as the inversion layer spreads so that when $Q_m \gg Q_b$ we have $X_s = X_m = X_d$.

Therefore, it can be seen that the approximation made in obtaining Eqn. (2.38), namely that $X_s = X_d$, is accurate in both extremes when Q_b is dominant and when Q_m is dominant. The transition from one extreme to the other is rapid, taking place as a result of an increase in U_s of several kT/q units. In this range, the above approximation would cause a slight under-estimation of Q_b and consequently an equal over-estimation of Q_m although Q_s , U_s , and $\left. \frac{dU}{dx} \right|_s$ would still be accurate.

Before proceeding further, it is convenient to define the following quantities:

$$a = \frac{C_i}{C_D} e^{-U_f/2} \quad (2.40)$$

$$\eta = a(U_g - U_s)$$

where $C_D = \epsilon_s / L_D$ and $L_D = \left(\frac{kT\epsilon_s}{2q^2 n_i} \right)^{1/2}$ as in Eqns. (2.10) and (2.6). Using these definitions, Eqn. (2.39) becomes:

$$Q_m = - \frac{kT}{q} \cdot C_i \frac{(\eta^2 + \eta/a - U_g)}{\eta a} \quad (2.41)$$

and the model electron density is:

$$\begin{aligned} n &= - Q_m / q \chi_s \\ &= n_i e^{U_f} \cdot \frac{(\eta^2 + \eta/a - U_g)}{U_g - \eta/a} \end{aligned} \quad (2.42)$$

In its present form, Eqn. (2.41) may be substituted instead of Eqn. (2.19) into the current equation (2.12) but the requirement still remains that we need an independent relationship between U_s and δ in order that the analysis be continued without further assumption, i.e. we want to avoid assumptions such as Eqn. (2.20) which seriously limit the range of application for the theory.

Comparing Eqn. (2.32) with Eqn. (2.33), we see that both space charge distributions have the same charge moment. Another important property shared by the two distributions is the invariance of the quantity $\int n dU$, where the integration is carried out from the surface to the neutral substrate. As shown in Appendix A, this property may be used to match boundary conditions between the model space charge region

and the Boltzmann distribution defined by Eqn. (2.3) at the source and drain junctions. Since the separation of the electron and hole quasi-Fermi levels is defined at these boundaries by the applied terminal source and drain voltages, we obtain as a result the relationship between U_g and δ ,

$$n^2 + n/a - U_g = e^{U_g - n/a - \delta - 2U_f} \quad (2.43)$$

where $n = a(U_g - U_s)$ and δ is the model channel potential or the separation of the model quasi-Fermi potentials.

The independent variables in this expression are U_g and δ with n (or U_s) the dependent variable.

Differentiating Eqn. (2.43), we get:

$$\begin{aligned} d\eta &= \frac{\partial \eta}{\partial U_g} dU_g + \frac{\partial \eta}{\partial \delta} d\delta \\ &= \frac{a}{n^2 + (2a+1/a)n + 1 - U_g} \left[(n^2 + n/a + 1 - U_g) dU_g - (n^2 + n/a - U_g) d\delta \right] \end{aligned} \quad (2.44)$$

Equation (2.12) for drain current may be written in the form:

$$I_d = - \frac{Z D_n}{L} \int_0^{U_d} Q_m d\delta \quad (2.45)$$

for the case of grounded source and $\delta = U_d$ at the drain. We may now substitute for Q_m using Eqn. (2.41) and for $d\delta$ (with $dU_g = 0$) using Eqn. (2.44) to obtain

$$\begin{aligned}
 I_d &= - \frac{kT}{q} \frac{Z D_n C_i}{L a^2} \int_{\eta_s}^{\eta_d} \left[\eta + 2a + 1/a + (1 - U_g)/\eta \right] d\eta \\
 &= - \frac{kT}{q} \frac{Z D_n C_i}{L a^2} \left[\frac{\eta^2}{2} + (2a + 1/a)\eta + (1 - U_g) \log \eta \right]_{\eta_s}^{\eta_d}
 \end{aligned} \tag{2.46}$$

where η_s and η_d are obtained by solving Eqn. (2.43) at the source and drain, respectively. Equation (2.46) expresses drain current in closed form and is valid for all regions of operation from subthreshold (weak inversion) to strong inversion.

Whereas the current expressions (2.21) and (2.25) in first-order theory must be cut off when the drain voltage reaches $V_{d \text{ sat}}$, given by Eqn. (2.28), Eqn. (2.46) can still be used in saturation due to the nature of relationship (2.43). Considering that the source is kept at a fixed potential while the drain voltage is increased without limit, we see that the lower limit of the integral (2.46) η_s remains fixed while η_d varies with drain voltage in a manner described by Eqn. (2.43). When $I_d = 0$, η_d is at a maximum with respect to drain voltage and as this voltage is increased η_d decreases and approaches a lower limit as the right-hand side of Eqn. (2.43) approaches zero. This limit is:

$$\eta = - \frac{1}{2a} + \sqrt{\left(\frac{1}{2a}\right)^2 + U_g}$$

and the corresponding value of U_s is given by:

$$U_{SM} = U_g + \frac{1}{2a^2} - \sqrt{\left(U_g + \frac{1}{2a^2}\right)^2 - U_g^2} \tag{2.47}$$

which is a maximum. Therefore, Eqn. (2.46) is self-limiting and predicts a constant drain current in saturation.

It is interesting to note that Eqn. (2.47) is identical to the expression (2.29) for the pinch-off surface potential and by inspection of Eqn. (2.41) it is seen that when $U_s = U_{SM}$, we have $Q_m = 0$.

The concept of threshold voltage is not required in this analysis since there is no need to make assumptions such as Eqn. (2.20) in order to obtain a closed-form solution. Thus, there is a smooth transition from weak channel to strong channel behaviour [29], as the gate voltage is increased from very low to high levels.

Closed-form expressions are also obtained from Eqn. (2.46) for other important device terminal parameters such as drain conductance g_d , gate transconductance g_m , and gate capacitance C_g .

Even though El-Mansy has reported very good results [7] with the assumption of constant mobility, he has since incorporated into the model the effects of mobility variation as a function of longitudinal surface field by expressing mobility as [30]:

$$\mu_n = \frac{\mu_{no}}{1 + \frac{\mu_{no}}{v_{sm}} \frac{kT}{q} \frac{dU_s}{dy}} \quad (2.48)$$

where μ_{no} is the low field mobility and v_{sm} is the scatter-limited velocity. By recognizing that $dU_s/dy = -(1/a)d\eta/dy$, we may substitute Eqn. (2.48) into Eqn. (2.46) prior to performing the integration. The resulting expression is the same except that in the new expression, the channel

length L is replaced by an effective channel length L_{eff} given by:

$$L_{\text{eff}} = L + \frac{\mu_{\text{no}}}{v_{\text{sm}}} \frac{kT}{q} (U_{\text{sd}} - U_{\text{ss}})$$

or

$$L_{\text{eff}} = L(1 + E_{\text{av}}/E_{\text{c}}) \quad (2.49)$$

where $E_{\text{av}} = kT(U_{\text{sd}} - U_{\text{ss}})/qL$ is the average field along the channel and $E_{\text{c}} = v_{\text{sm}}/\mu_{\text{no}}$ is the critical field above which the carriers reach scatter-limited velocity. We can see that this will affect the calculated value of drain current in devices where carrier velocity saturation effects are important and will effectively lower the value of saturation current for such devices (important for short channel devices).

2.4.2 Saturation

In Section 2.3.2, the inadequacies of the depletion approximation to calculate channel shortening in saturation were pointed out. The variation of potential in the drain section is determined by the two-dimensional interaction of fields produced by the gate and drain electrodes. Only by considering the two-dimensional aspect of this region can the saturation characteristics of an MOS transistor be modelled properly.

El-Mansy [7,10] considered the drain section to be approximated by a rectangle, as shown in Fig. 2.3. Boundary (1) is defined in terms of U_{s1} , E_1 and X_1 , the surface potential, longitudinal electric field, and channel thickness, respectively, obtained from the solution of the source

Fig. 2.3. Schematic of the two-dimensional drain section model for saturation.

section at the point where the GCA no longer becomes valid, i.e. where

$$\frac{\partial^2 U_s}{\partial x^2} \bigg/ \frac{\partial^2 U_s}{\partial y^2} = K$$

where K is chosen to have a value somewhat larger than unity. By treating the drain section as a closed surface, Gauss' law may be applied in its most general form:

$$\oint_S \mathbf{D} \cdot d\mathbf{S} = Q$$

or

$$\frac{kT}{q} \left\{ \int_0^{x_1} (\epsilon_s E_y - \epsilon_s E_1) dx + \int_0^y \epsilon_s E_x dy \right\} = -q \int_0^y \int_0^{x_1} (N+n) dx dy$$

where E_1 , E_y and E_x are the normalized electric fields normal to the planes at (1), y and (2), respectively, and the field at (4) is neglected.

Integration normal to the surface is facilitated by assuming a parabolic variation of potential in that direction. Further manipulation and integration along the surface yields:

$$\begin{aligned} E_{sd}^2 = E_{s_1}^2 + \frac{3C_i}{\epsilon_s x_1} \left\{ (U_{sd} - U_g)^2 - (U_g - U_{s_1})^2 \right\} + \frac{6q^2 N}{kT \epsilon_s} (U_{sd} - U_{s_1}) \\ - \frac{6q}{kT \epsilon_s x_1} \int_{U_{s_1}}^{U_{sd}} Q_m dU_s \end{aligned} \quad (2.50)$$

where E_{sd} is the normalized electric field at the drain.

The last term in Eqn. (2.50) can be written in terms of the drain current as:

$$\int_{U_{s1}}^{U_{sd}} Q_m dU_s = \frac{q}{kT} \left[\frac{L}{\mu Z} (I_d - I_1) + \frac{kT}{q} \frac{I_d}{v_{sm} Z} (U_{sd} - U_{s1}) \right] \quad (2.51)$$

where I_1 is the drain current for U_{s1} at the drain (corresponds to $I_{d \text{ sat}}$ in the first-order model).

The drain current can be written in terms of the drain conductance by applying the definition of drain conductance to the present saturation model.

The drain conductance of an MOS device is defined as:

$$g_d = \frac{kT}{q} \frac{\partial I_d}{\partial U_d}$$

which from Eqn. (2.45) is:

$$g_d = - \frac{kT}{q} \frac{Z D_n}{L} Q_{md}$$

Now, Eqn. (2.12) can be evaluated at the drain to obtain Q_{md} :

$$Q_{md} = - \frac{I_d}{Z D_n \left. \frac{d\delta}{dy} \right|_d}$$

In the drain section, we can neglect diffusion current and say that $d\delta/dy = dU_s/dy$. At the drain $\left. \frac{dU_s}{dy} \right|_d = E_{sd}$. Therefore, we have:

$$g_d = \frac{kT}{q} \frac{\partial I_d}{\partial U_{sd}} = \frac{I_d}{\frac{kT}{q} L E_{sd}} \quad (2.52)$$

or

$$I_d = \frac{kT}{q} g_d E_{sd} L \quad (2.53)$$

which expresses drain current in terms of drain conductance. Due to the presence of the dependent variable I_d in the expression for E_{sd} , Eqn. (2.52) cannot be integrated to get a closed-form solution for drain current.

It has been shown [7,23] that the presence of mobile carriers in the drain section has a negligible effect on the drain characteristics of the device except for short channel devices with lightly-doped substrates where scatter-limited velocity effects may dominate:

If we neglect mobile carriers by setting Q_m to zero in Eqn. (2.50), then the charge neutrality condition at boundary (1) becomes

$$qN_{x1} = kT/q C_i (U_g - U_{s1}).$$

Eqn. (2.50) now becomes:

$$E_{sd}^2 = E_{s1}^2 + A^2 (U_{sd} - U_{s1})^2 \quad (2.54)$$

where

$$A^2 = \frac{3C_i}{\epsilon_s x_1}.$$

From Eqn. (2.53), we have:

$$\frac{dI_d}{dU_{sd}} = \frac{I_d}{L} \cdot \frac{1}{[A^2 (U_{sd} - U_{s1})^2 + E_{s1}^2]^{1/2}}$$

which can be integrated to give:

$$I_d = I_1 \left\{ \sqrt{\frac{A^2}{E_{s1}^2} (U_{sd} - U_{s1})^2 + 1} + \frac{A}{E_{s1}} (U_{sd} - U_{s1}) \right\}^{1/LA} \quad (2.55)$$

This may be interpreted in terms of channel shortening with a relationship similar to Eqn. (2.31):

$$I_d = \frac{I_1}{(1 - \Delta L/L)} = I_1 \cdot \frac{L}{L'} \quad (2.56)$$

where L' is the effective (shortened) channel length in saturation.

The presence of the exponent $1/LA$ in Eqn. (2.55) is significant since it is small for devices with long channels, heavily-doped substrates, or thin gate insulators giving a rather flat saturation current characteristic. Conversely, for devices with short channels, lightly-doped substrates, or thick gate insulators, it predicts a large increase in saturation drain current with increasing drain voltage.

Using Eqn. (2.55), El-Mansy has achieved excellent agreement with experimental measurement over a wide range of device physical parameters.

Thus, it may be concluded that this model provides the best tool to date for analyzing MOS device behaviour. Consequently, it will be employed in Chapter 5 as the basis for developing a model for DMOST operation.

CHAPTER 3

DMOS TRANSISTOR FABRICATION

3.1 Process Design Considerations

One important advantage of DMOS devices is the process flexibility allowed in their fabrication [31]. For applications where high, constant gain and low feedback capacitance are necessary, the best choice of starting material is n^-/p^- epitaxial, n^- bulk, or n^-/SOS . In applications where the DMOS transistors are to be fabricated on the same chip as standard NMOS devices which have p-type substrates the surface of the low-doped section of the DMOS channel (drift region) can be ion implanted with n-type dopant to produce essentially the same effect while at the same time retaining self-isolation. The gate of the DMOST can be either polysilicon, which is compatible with standard self-aligned NMOS processing, or metal gate, which adds the flexibility of allowing the drain to be separated from the end of the gate by an arbitrary distance to increase the drain breakdown voltage and reduce the feedback capacitance. This feature is usually combined with field plate techniques to cover the drain junction in order to increase its breakdown voltage.

The process used for DMOS fabrication at Carleton University is a non-self-aligned, double diffused (no ion implantation), metal gate process. The starting material is a lightly-doped ($>100\Omega\text{-cm}$) p-type substrate. Fig. 3.1 shows the cross-section of this device which features a semi-overlapping gate electrode. This device was layed out in various configurations (described later) to observe the effect of the length of the uncovered drain region on device characteristics. Details of the mask levels used and process steps are given in Appendix B.

Fig. 3.1. The cross-section of a DMOS transistor with semi-overlapping gate.

The resultant impurity profile normal to the surface of the source diffusion is described theoretically by a double Gaussian diffusion profile (instantaneous source diffusion).

$$N(x) = N_{OP} \exp(-x^2/4D_P t_P) - N_{OB} \exp(-x^2/4D_B t_B) - N_B \quad (3.1)$$

where

N_{OP} , D_{OB} = the final surface concentration of phosphorous and boron, respectively

$D_P t_P$, $D_B t_B$ = the sum of the products of diffusion coefficient and diffusion time for the temperature cycles affecting the diffusion of phosphorous and boron, respectively

N_B = the background impurity concentration (boron).

However, as shown by Kennedy and O'Brien [32], the theoretical diffusion profile along the surface under the mask cannot be approximated by the one-dimensional solution obtained for diffusion perpendicular to the surface.

Solution of the three-dimensional diffusion equation for an instantaneous source shows that the profile along the surface is described by:

$$N(y) = N_{OP} \operatorname{erfc} \left(\frac{y}{2\sqrt{D_P t_P}} \right) - N_{OB} \operatorname{erfc} \left(\frac{y}{2\sqrt{D_B t_B}} \right) - N_B \quad (3.2)$$

The values of N_{OP} and N_{OB} are given by:

$$N_O = \frac{N_{O1}}{\pi} \left(\frac{D_1 t_1}{D_2 t_2} \right)^{1/2} \quad (3.3)$$

where N_{O1} is the surface concentration of the impurity at the predeposition temperature, $D_1 t_1$ is for predeposition and $D_2 t_2$ for all subsequent temperature cycles ($D_p t_p$ for phosphorus and $D_B t_B$ for boron).

Equation (3.3) assumes that the predeposition phase is extremely short compared to the drive-in phase, i.e.

$$\sqrt{D_1 t_1} \ll \sqrt{D_2 t_2}$$

and that the predeposition impurity diffusion can be approximated by a constant source or complementary error function (erfc) diffusion.

The profile given by Eqn. (3.2) is shown graphically in Fig. 3.2 where the origin ($y=0$) is taken at the edge of the source diffusion mask. As can be seen in Fig. 3.1, the entire p-type diffused region lies beneath the gate oxide. The most important parameter characterizing this region from the viewpoint of device design is the value of the peak doping N_p . This may be obtained by differentiating Eqn. (3.2) and setting the derivative to zero.

$$\frac{dN}{dy} = -\frac{2N_{OP}}{4D_p t_p \sqrt{\pi}} e^{-\frac{y^2}{4D_p t_p}} + \frac{2N_{OB}}{4D_B t_B \sqrt{\pi}} e^{-\frac{y^2}{4D_B t_B}} \quad (3.4)$$

Setting $dN/dy=0$ yields the position of the peak doping:

$$y_p = 2 \left[\frac{(D_p t_p)(D_B t_B)}{D_B t_B - D_p t_p} \log \left(\frac{N_{OP} D_B t_B}{N_{OB} D_p t_p} \right) \right]^{1/2} \quad (3.5)$$

Evaluating Eqn. (3.2) for $y=y_p$ gives N_p .

Fig. 3/2. Diffusion profile along the surface of a DMOS transistor.

Since N_p is the highest value of the doping in the channel, it will determine the threshold voltage of the whole device. Control over the value of N_p is therefore crucial if the threshold voltage variation from one device to another is to be within close tolerance limits. In order to determine a satisfactory diffusion and oxidation schedule that would produce a desirable value of N_p which is relatively insensitive to small variations in the diffusion and oxidation times, theoretical impurity profiles, characterized by Eqns. (3.2)-(3.5), were simulated on a digital computer for various values of drive-in and oxidation temperatures and times.

The results of the analysis showed that normal bipolar or MOS diffusion temperatures and times could not be used in DMOS transistor fabrication. The primary reason for this is that the dry oxidation cycle, which is necessary to grow the thin gate oxide, must take place after the phosphorous predeposition and drive-in phase have been completed. At the normal oxidation temperature of 1150°C, the phosphorous diffusion could easily overtake the boron diffusion since its diffusion coefficient is approximately a factor of 10 higher than that for boron at that temperature. By recognizing that the oxidation rate is not as sensitive a function of temperature as are the diffusion coefficients, the problem can be resolved by lowering the gate oxidation temperature to 1000°C and increasing the oxidation time accordingly. Similar considerations resulted in the phosphorous drive-in temperature being lowered from 1100°C to 1000°C.

Theoretical threshold voltage calculations by Richman [33] have shown that for p-type substrates, an oxide thickness of $1000\text{\AA}$, and $Q_{ss}/q = 1 \times 10^{11} \text{ cm}^{-2}$, the substrate impurity density must be greater than 10^{16} cm^{-3} in order that an enhancement-type device be produced. To account for uncertainty in the value of Q_{ss} and the extent of redistribution during the gate oxidation phase, a theoretical target value of $N_p = 2 \times 10^{16} \text{ cm}^{-3}$ was chosen.

Another problem inherent in the conventional processing techniques used is that the final boron surface concentration is high ($\sim 3 \times 10^{18} \text{ cm}^{-3}$) leading to a large impurity gradient in the diffused p-region. Ideally, this gradient should be low in order to obtain better control over threshold voltage. This may be achieved by using ion implantation as a low concentration diffusion source [34] for predeposition.

3.2 Device Geometry

Since the starting material used in this process is a lightly-doped non-epitaxial p-type substrate, the silicon surface outside the active area of the transistor will be inverted and be electrically shorted to the drains of all test transistors unless some isolation technique is employed. The simplest way to achieve this isolation is to design devices with circular geometry so that the p-type channel diffusion forms a ring around the n^+ drain diffusion. Otherwise, for rectangular geometry, a p-type channel stop diffusion is required.

The layout design rules are summarized by the following minimum dimensions:

Contact hole opening	= $7\mu\text{m}$
Spacing between source and drain diffusion windows	= $10\mu\text{m}$
Metal line width	= $10\mu\text{m}$
Spacing between metal lines	= $10\mu\text{m}$

A photomicrograph of a sample test chip is shown in Fig. 3.3. Included on this chip are 10μ , 20μ , 30μ and 40μ circular DMOS transistors, a 20μ rectangular DMOST, and a 10μ rectangular NMOS device. All DMOS devices have a 7μ long gate and the NMOS device has a 10μ gate. A photomicrograph of a sample 10μ DMOST is shown at higher magnification in Fig. 3.4.

Fig. 3.3. Photomicrograph of DMOS test chip.

Fig. 3.4. Photomicrograph of a DMOS transistor with circular geometry.

CHAPTER 4

EXISTING DMOS TRANSISTOR MODELS

4.1 The Velocity Saturation Model

In their analysis of DMOS transistor behaviour, Sigg et al [1] considered only the saturation region of operation where it was assumed that the device could be approximated by a short channel MOS transistor of length L' (see Fig. 3.1) in series with a depleted drift region of length $L-L'$ in which mobile carriers reached their scatter-limited velocity everywhere. The experimental device used for their analysis had a short channel length L' of $1\mu\text{m}$ and a drift region length $L-L'$ of $9\mu\text{m}$.

The requirement that the drift region is completely depleted and in addition that the longitudinal field in this region is everywhere greater than the critical field for carrier velocity saturation implies that the average field in the drain region must also be greater than this critical field, i.e.

$$\frac{V_D - V_{D_{\text{sat}}}}{L - L'} \geq E_c \quad (4.1)$$

where the critical field $E_c = 2.4 \times 10^4 \text{ V/cm}$, $L-L' = 9\mu\text{m}$, and $V_{D_{\text{sat}}}$ is the saturation voltage of the short channel device ($\sim 2.4\text{V}$). Substitution of these values into Eqn. (4.1) yields $V_D > 24\text{V}$. Thus, the following analysis is limited to situations where V_D is very high and for gate voltages low enough to allow complete depletion of the drift region.

Simple first-order theory was used in the analysis of the short channel device where it was concluded that if

$$\frac{V_{Dsat}}{L'} = \frac{V_G - V_T}{L'} \geq E_c \quad (4.2)$$

then the average carrier velocity is close to its limiting value given by:

$$v_{sm} = \mu_n E_c \quad (4.3)$$

Therefore, the saturation gate transconductance per unit channel width, given by:

$$\frac{g_m}{Z} = \mu_n C_i \frac{(V_G - V_T)}{L'} \quad (4.4)$$

will reach a maximum when the inequality (4.2) is valid. This maximum is:

$$\frac{g_{m \max}}{Z} = C_i v_{sm} \quad (4.5)$$

The current gain cut-off frequency is defined as:

$$\begin{aligned} f_t &= \frac{g_m}{2\pi C_i Z L'} \\ &= \frac{\mu_n (V_G - V_T)}{2\pi L'^2} \quad \text{in saturation.} \end{aligned} \quad (4.6)$$

When the carrier velocity reaches v_{sm} , the maximum value of f_t obtained by setting $g_m = g_{m \max}$ is given by:

$$f_t = \frac{v_{sm}}{2\pi L'} \quad (4.7)$$

Equation (4.2) is then used as a design criterion in order that g_m and f_t reach their maximum values in saturation.

Due to the highly simplified assumptions used, this analysis is restricted in its application to very high voltage operation and serves only as a guide in device design for microwave applications. It is therefore not appropriate for lower voltage (logic) applications.

4.2 The Enhancement-Depletion Model [3,4,34]

The DMOS device structure assumed in the enhancement-depletion (E/D) model is one with the gate electrode covering the full length of the drift region and overlapping the drain diffusion. The device is then assumed to be equivalent to an enhancement-type transistor with channel length L' in series with a depletion-type transistor with channel length $L-L'$. It is further assumed that the enhancement device has a uniform substrate doping of concentration N_p . In other words, the diffused profile in Fig. 3.2 is approximated by a rectangle of height N_p and length L' . The two-transistor equivalent circuit model is shown in Fig. 4.1.

In their analysis, Rodgers et al [4] assumed that the simple first-order theory characterized by Eqns. (2.25) and (2.27) is valid and that there is no back-gate bias effect (body effect) on the depletion device. This latter assumption is serious in that it ensures that a channel is always formed in the depletion transistor even when $V_X > V_G - V_{TD}$, where V_{TD} is the 'equilibrium' threshold voltage of the depletion transistor. This situation could, in fact, be violated for values of V_D such that both devices are operating in saturation, i.e. $V_D > V_g - V_{TD}$ and $V_X > V_g - V_{TE}$ where V_{TE} is the 'equilibrium' threshold voltage of the enhancement transistor. This problem is somewhat circumvented by assuming that the

Fig. 4.1. The two-transistor equivalent circuit model of a DMOS transistor.

current is given by:

$$I_D = \frac{Z}{L} \mu C_i \frac{(V_G - V_{TE})^2}{2} \quad (4.8)$$

whenever the enhancement device is saturated. In this manner, simultaneous solution of the appropriate first-order equations yields solutions for the drain current in three regions of operation, viz. linear-linear, linear-saturation and saturation-saturation. Although nothing is said about the saturation-linear region, it must be assumed that Eqn. (4.8) was taken to be valid also for that region.

In order to get a reasonable fit between theory and experiment, Rodgers et al assumed that the surface carrier mobility has a strong gate-voltage dependency given by

$$\frac{\mu}{\mu_0} = \frac{1}{1 + (V_G - V_{TD})/V_K} \quad (4.9)$$

where V_K is the effective gate voltage at which the measured mobility of electrons is one-half its value for $V_G - V_{TE} = 0$. The 'low field' value is μ_0 . Since both measurements are inferred from g_d versus $(V_G - V_{TE})$ data with the use of simple first-order theory, an automatic fit of theory to experiment is achieved for any particular value of V_D . Typical of this use of fitting parameters is the unrealistic value of mobility used in the theoretical model. Here, values of μ_0 of roughly $850 \text{ cm}^2/\text{Vsec}$ were used. This is much higher than the actual values measured for n-type inversion layers. It is also approximately double the value of bulk mobility

measured for an impurity concentration comparable to that which exists in the graded region of the DMOS channel [37].

All the curve-fitting 'physical' parameters were obtained to achieve a fit at $V_D=15V$. Nothing is stated about the fit at lower drain voltages where the graded nature of the profile determines the shape of the drain characteristics and the transconductance. Also, simple E/D theory is only useful for long channel devices that do not exhibit carrier velocity saturation. The use of full E/D theory with carrier velocity saturation is required to obtain good agreement for short channel devices. This requires an iterative procedure on the computer and is no longer fully analytic.

4.3 The Graded Doping Model

The approach used in the graded-doping model [5,6] is to make some approximation for the graded profile, either exponential [6] or triangular [5] and then to divide this profile up into many lumps (say 200) each of which is represented as a uniformly doped short-channel MOS transistor. All lumps are connected in series, the lump closest to the drain being identified as the depletion mode long channel transistor which represents the drift region. The graded doping is therefore discretized and the lumps are characterized by their individual substrate doping levels. First-order theory is then used in a computer simulation of the overall device I-V drain characteristics. The computation scheme first assigns gate voltage and drain current as input parameters and then solves Eqn. (2.21) for the 'internal' drain voltage of each lump in the non-saturation region. When a saturated lump is encountered, the drain current is lowered

so that a unique solution may be obtained for drain voltage. The lump drain voltages are computed starting from the source so that the drain voltage of one lump may be used as the source voltage of the next lump in series. Such solutions are therefore cut off at the value of overall drain voltage for which any one of the lumps is in saturation. Above this 'saturation' voltage, the drain current is assumed to be constant.

This model not only suffers from the use of first-order theory but it uses essentially a numerical integration to obtain device characteristics. It also is only valid in the non-saturation (or linear) region of operation and it neglects the important effect of carrier velocity saturation.

4.4 Summary

To summarize, DMOS transistor models to date have all used first-order theory in some form and have used one or more of the following approximations:

- a) the graded nature of the impurity profile is neglected;
- b) the operating point of the device is assumed to be well into saturation and carrier velocity saturation is assumed to exist either throughout the drift region or throughout the whole device;
- c) curve-fitting is used in conjunction with assumption a) to obtain analytical solutions which show reasonable agreement with measurement;

d) numerical integration is used to obtain solutions for the linear region of operation.

Clearly, an accurate model which simulates device behaviour over all regions of operation without making simplifying or physically unrealistic assumptions is required. Such a model must also be formulated in such a manner that it is an efficient design tool, i.e. numerical integration is ruled out.

CHAPTER 5

A NEW DMOST MODEL

In Chapter 2, a strong case was made for using El-Mansy's model for MOS device operation. This model was chosen as the one most suitable as the starting point in the development of a DMOS model and will be used exclusively in this Chapter. In Chapter 3, the structure of the DMOS transistor was examined and, in particular, the shape of the impurity profile along the surface of the diffused portion of the channel was illustrated. The task now becomes one of finding a suitable way to accurately represent this profile so that it is both mathematically simple and compatible with the formulation of the El-Mansy model. Then, the problem of modelling this region as a whole without resorting to numerical integration is dealt with. As will be shown later, similar considerations lead to a model for the section of the channel adjacent to the drain which has no overlying gate electrode.

5.1 The Impurity Profile

It is usual in MOS theory for uniform channel devices to assume that both the source and drain junctions can be well approximated by one-sided step junctions. This is especially valid at the n^+ -p source junction since longitudinal fields in the vicinity of the junction are negligible and the surface of the n^+ source diffusion is accumulated for normal

operating conditions. At the drain junction, the approximation introduces negligible error when an inversion layer is present and a small error in saturation if the substrate doping level is high enough that the depletion width on the drain side of the metallurgical junction is a significant portion of the total depletion width. In the case of a DMOS transistor, the p^- substrate doping is very low making the abrupt drain junction approximation appropriate.

Referring to Fig. 5.1, it can be seen that the region of the DMOS channel between the source junction and the point of peak doping has an extremely high, continuously variable grade constant which is highest at the junction and decreases to zero at the point of peak doping. In the interests of retaining the most important diffused region characteristics without mathematical complexity which is too severe to allow analytical formulations for device behaviour to be derived, we will here assume that the model profile is abrupt at the source and that it is uniform up to the point of peak doping and has a value equal to N_p .

As we proceed along the diffused profile beyond the point of peak doping, we recognize that a substantial portion of the remaining profile can be closely approximated by a single exponential function. Simulations of a wide range of likely impurity profiles have shown that this occurs in the region where the n^+ source diffusion no longer influences the profile and also that this exponential is well approximated by a straight line (on a semi-log scale) drawn from a point $y_1 = 2y_p$, and $N = N_p$, to a point y_2 , and $N = N_B$, where the diffused doping concentration is equal to the

Fig. 5.1. Calculated diffusion profile of a typical DMOS transistor.

background concentration. This line is shown in Fig. 5.1. Thus, if we increase the channel length of the uniformly doped source section to equal y_1 , we have a relatively simple, two-section profile model that meets the stated objectives. The overestimation of doping level immediately adjacent to the source junction and at y_1 will tend to cause an underestimation of current in subthreshold operation and will affect the accuracy of the model predictions whenever this source section is in saturation. These aspects will be discussed in further detail in Chapter 6.

The above approximations allow us to write expressions for the Fermi level as a function of distance along the channel:

$$\begin{aligned}\phi_f &= \phi_p, & 0 \leq y \leq y_1 \\ \phi_f &= \phi_p - K_1(y - y_1), & y_1 \leq y \leq y_2 \\ \phi_f &= \phi_B, & y_2 \leq y \leq y_d\end{aligned}\tag{5.2}$$

where

$$y_2 = L'$$

$$y_d = L$$

and

$$K_1 = \frac{\phi_p - \phi_B}{y_2 - y_1}$$

We now have a simple linear relationship for the Fermi potential in the graded region. The Fermi potential is simply related to the doping concentration by

$$N(y) = n_i e^{U_f(y)}\tag{5.3}$$

where

$$U_f(y) = \frac{q}{kT} \phi_f(y)$$

is the normalized Fermi potential.

5.2 Modelling the Graded Region

The most important relationships used by El-Mansy are:

$$Q_m = - \frac{kT}{q} C_i \frac{(\eta^2 + \eta/a - U_g)}{\eta a} \quad (5.4a)$$

$$\eta^2 + \eta/a - U_g = e^{U_g + \eta/a - \phi - 2U_f} \quad (5.4b)$$

$$I_d = - \frac{kT}{q} \frac{Z D_n C_i}{L} \int_{\eta_s}^{\eta_d} \frac{1}{a^2} \left[\eta + 2a + 1/a + (1 - U_g)/\eta \right] d\eta \quad (5.4c)$$

where

$$a = \frac{C_i}{C_D} e^{-U_f/2} \quad (5.4d)$$

and

$$\eta = a(U_g - U_s) \quad (5.4e)$$

Eqn. (5.4c) can be integrated for a uniform channel MOS device since the parameter a is a constant. However, in a graded channel device, a becomes a function of position in the channel and the integration cannot be carried out except by resorting to numerical methods.

5.2.1 Behaviour of Q_m and U_s

In order to develop a closed-form relationship for the current in the graded region ($y_1 < y < y_2$), we first examine the differential equation governing current flow:

$$I_d = - Z D_n Q_m \frac{d\delta}{dy} \quad (5.5)$$

and recognize that for current-continuity to prevail at any point along the channel we must have

$$\frac{d\delta}{dy} \propto \frac{1}{Q_m} \quad (5.6)$$

when current is flowing.

Since there is no apparent independent relationship which shows the variation of the inversion layer charge with gate voltage, surface potential and substrate doping, other than Eqns. (5.4a) and (5.4b), further information may be obtained by graphical observation of this variation. Computations were performed to generate this data for a range of values of substrate doping and plotted as a function of this doping for gate voltages ranging from 0 to 5 volts. The results for the equilibrium case ($\mathcal{E}=0$) are shown in Fig. 5.2. The values $Q_{ss}/q=1 \times 10^{11} \text{ cm}^{-2}$ and $x_i=1 \times 10^{-5} \text{ cm}$ were used. Due to the linear approximation for ϕ_f given by Eqn. (5.2), the horizontal scale is also linear in distance along the graded portion of the model channel ($y_1 < y < y_2$).

We can see that for all values of gate voltage the drain end of the graded channel is heavily inverted and as we move toward the source end, we reach a point where, for small gate voltages, Q_m and U_s drop off rapidly.

If we define the condition for heavy inversion as

$$U_s \geq 2U_f \quad (5.7)$$

where δ in Eqn. (2.20) is set to zero for equilibrium, we can see that a

Fig. 5.2. Variation of inversion layer charge (Q_m) and surface potential (U_s) as a function of substrate doping at equilibrium.

point exists in the graded channel where the U_s curve intersects the $2U_f$ curve. Thus, the channel is divided into two sections by this point, a source section which is depleted and a drain section which is heavily inverted. It is interesting to note here that had first-order theory been used the U_s curve would follow the $2U_f$ line exactly until the threshold voltage reaches the value of the applied gate voltage after which Q_m is assumed to be zero.

It is also evident that under heavy inversion conditions the slope of the U_s curve with respect to a change in doping is, in equilibrium,

$$\left. \frac{dU_s}{dy} \right|_{U_{gg}} = \frac{dU_f}{dy} \quad (5.8)$$

and as we move from a region of strong inversion to one of very strong inversion ($U_s - 2U_f$) increases linearly. By rewriting Eqns. (5.4a) and (5.4b) in terms of U_s , we can see how this variation in U_s is reflected in the behaviour of Q_m .

$$\begin{aligned} Q_m &= -\frac{kT}{q} C_i \frac{(\eta^2 - U_s)}{a^2 (U_g - U_s)} \\ &= -\frac{kT}{q} \frac{C_D^2}{C_i} e^{\frac{U_f}{U_g - U_s}} \frac{(\eta^2 - U_s)}{U_g - U_s} \end{aligned} \quad (5.9)$$

$$\eta^2 - U_s = e^{\frac{U_s - \delta - 2U_f}{U_g - U_s}} \quad (5.10)$$

Substitution of Eqn. (5.10) into Eqn. (5.9) yields:

$$Q_m = - \frac{kT}{q} \frac{C_D^2}{C_i} \cdot \frac{e^{U_s - \delta - U_f}}{U_g - U_s} \quad (5.11)$$

We also can use the fact that the metal-semiconductor work function difference ϕ_{ms} varies in direct proportion with the Fermi level ϕ_f to conclude that

$$\left. \frac{dU_g}{dy} \right|_{U_{gg}} = \frac{dU_f}{dy} \quad (5.12)$$

Therefore, for a given value of U_{gg} , $(U_g - U_s)$ and $(U_s - U_f)$ are both constants in Eqn. (5.11) so that Q_m becomes a constant for heavy inversion conditions in equilibrium, independent of substrate doping. This follows also by considering that under these conditions the inversion layer charge Q_m is dominant over the bulk charge Q_b so that to a good approximation $Q_m = -Q_g = -\frac{kT}{q} C_i (U_g - U_s)$. It is evident that for charge neutrality to prevail the surface potential must follow the variations in effective gate voltage due to changes in substrate doping level. These results are also valid for the more general equilibrium case when δ has some constant value greater than zero. The condition for strong inversion is then $U_s \geq \delta + 2U_f$.

In order to treat the non-equilibrium case for strong inversion where δ increases along the channel from source to drain, computations were performed using standard NMOS devices to evaluate Q_m and U_s as a function of δ with U_f held constant. The results for a doping level of $1 \times 10^{14} \text{ cm}^{-3}$ are shown in Fig. 5.3.

Fig. 5.3. Variation of inversion layer charge (Q_m) and surface potential (U_s) as a function of channel potential (δ) for a device with $N_B = 1 \times 10^{14} \text{ cm}^{-3}$, $Q_{ss}/q = 1 \times 10^{11} \text{ cm}^{-2}$, $x_i = 1 \times 10^{-5} \text{ cm}$. The validity of the GCA is assumed.

By comparing the slopes of the U_s curves in strong inversion to that of the $U_s = \delta + 2U_f$ line, we see that they are very nearly equal. Therefore, in strong inversion, we have another relationship:

$$\left. \frac{dU_s}{dy} \right|_{U_f} = \left. \frac{d\delta}{dy} \right|_{U_f} \quad (5.13)$$

We can now combine Eqns. (5.8) and (5.13) to obtain:

$$\left. \frac{dU_s}{dy} \right|_{U_{gg}} = \left. \frac{d\delta}{dy} \right|_{U_{gg}} + \frac{dU_f}{dy} \quad (5.14)$$

whenever $U_s > \delta + 2U_f$.

As can be seen in both Figs. 5.2 and 5.3, the slope of U_s departs from that given by Eqn. (5.14) whenever $U_s < \delta + 2U_f$ (weak inversion). Due to the GCA assumption, the quantity $(U_g - U_s)$ becomes constant and Q_m falls off exponentially with an increase in δ . The value of this constant can easily be computed by solving Eqn. (5.10) for $U_s \ll \delta + 2U_f$. Therefore, we have:

$$\eta^2 - U_s = 0$$

or

$$a^2 (U_g - U_s)^2 - U_s = 0.$$

This is a quadratic equation which gives U_s as a function of a and U_g only. The solution is:

$$U_{sm} = U_{ga} - \sqrt{U_{ga}^2 - U_g^2} \quad (5.15)$$

where

$$U_{ga} = U_g + \frac{1}{2a}$$

and

U_{sm} is the maximum value that U_s can have if the GCA is valid. As we can see in Fig. 5.2, the variation of U_s with U_f in weak inversion is well approximated by Eqn. (5.15) except in the vicinity of the $U_s = \delta + 2U_f$ point.

Returning now to the case of strong inversion and non-equilibrium, we see from Fig. 5.3 that when $U_s \ll U_g$ the Q_m versus δ curves are exponential in nature and not constant as would be expected if Eqn. (5.14) were strictly true. Thus, Eqn. (5.14) is the result of neglecting diffusion current in the analysis. However, it will be shown later that, by restricting the use of Eqn. (5.14) so that it is only used to predict the position of the point in the graded channel where there is a transition from strong inversion to weak inversion conditions, the resulting expressions for current flow include, to a good approximation, the diffusion current.

We now have expressions (5.14) and (5.15) which predict quite accurately the variation of the surface potential U_s in regions of strong inversion and weak inversion, respectively. Let us first look at Eqn. (5.15) and observe its characteristics. This may be done by using the

impurity profile model described by Eqn. (5.2) to define the dependence of U_g and a on the distance y along the graded channel. In Fig. 5.4, U_{sm} and $U_s > \delta + 2U_f$ are shown as computed from Eqns. (5.15) and (5.14) respectively. In this case, equilibrium conditions are assumed. It can be seen that the curves for U_{sm} and U_s intersect at a point along the channel where there is a transition from strong inversion to weak inversion if such a point exists. Otherwise, they do not intersect and the whole graded region is then either strongly inverted or weakly inverted. The transition point for each value of applied gate voltage, identified by a vertical arrow in Fig. 5.4, corresponds closely to the knee of the associated Q_m curve in Fig. 5.2. This transition point therefore divides the graded region into two sections which can be modelled separately.

5.2.2 Drain Current

If we consider the graded region ($y_1 \leq y \leq y_2$) as a modelling unit with known boundary conditions, an expression for its drain current can be obtained. Referring to the schematic in Fig. 5.5, the boundary conditions are δ_1 , δ_2 and U_{gg} . Therefore, at the end points y_1 and y_2 , the surface conditions are assumed to be known. The first task we now face is to find the position of the transition point y_T . In the simplest case, when $\delta_1 = \delta_2$, (equilibrium) then we must have $\delta_1 = \delta_T = \delta_2$ and y_T can be found from the intersection of the line

$$U_s = U_{s2} + K_1(y_2 - y) \quad (5.16)$$

Fig. 5.4. U_{sm} and U_s as a function of substrate doping and gate voltage for a device with $x_i = 1 \times 10^{-5}$ cm, $Q_{ss}/q = 1 \times 10^{11}$ cm $^{-2}$ and $\delta = 0$ (equilibrium). Arrows indicate points where $U_s = U_{sm}$.

Fig. 5.5. Schematic showing notation used for the graded region model.

with the line $U_s = U_{sm}$. In order that the formulation be as simple as possible, we approximate the line given by U_{sm} with a straight line given by

$$U_{sm} = U_{sm_2} - K_s(y_2 - y) \quad (5.17)$$

where

$$U_{sm_2} = U_{sm}(y_2)$$

and

$$K_s = \frac{U_{sm_2} - U_{sm_1}}{y_2 - y_1}$$

Combining Eqns. (5.16) and (5.17) yields:

$$y_T = y_2 - \frac{(U_{sm_2} - U_{s_2})}{K_1 + K_s} \quad (5.18)$$

As mentioned previously, Eqns. (5.16) and (5.17) are used only to predict the position of the transition point y_T . The surface potential which would result if y_T were substituted into Eqn. (5.16) or Eqn. (5.17) is not accurate since there is not a sharp transition from very weak to very strong inversion (see Fig. 5.2). However, once y_T and δ_T are known, we can find U_{fT} using Eqn. (5.2), U_{gT} from Eqn. (5.12) and U_{ST} and Q_{MT} from Eqns. (5.4a-e).

As shown above, y_T can be solved easily for the equilibrium case when $\delta_1 = \delta_T = \delta_2$. However, when $\delta_1 \neq \delta_2$, we do not know δ_T . Therefore, some

iterative method must be used. The obvious criterion for convergence of the iterative method is current continuity.

Although it was earlier shown that Q_m in equilibrium is a constant, independent of substrate doping, under very strong inversion conditions, it is apparent that, as U_s approaches $\delta + 2U_f$ from above, Q_m decreases in an approximately exponential manner. This is due to the sensitivity of Q_m to small changes in the quantity $U_s - \delta - U_f$ in Eqn. (5.11). Thus, if we know the conditions at both boundaries of a heavily inverted region, then we know Q_m at those boundaries and we express Q_m at any point within the region as

$$Q_m = Q_{m2} e^{-K_{T2}(y_2 - y)}$$

where

$$K_{T2} = \frac{\log(Q_{m2}/Q_{mT})}{y_2 - y_T} \quad (5.19)$$

The region in question here was taken to be $y_T < y < y_2$ where knowledge of y_T and δ_T are presumed. This form is general in that any two points in such a region may be taken. It also reduces to Q_m constant or Q_m linear if K_{T2} is zero or small, respectively.

Keeping in mind the fact that Q_m at each boundary is also a function of the channel potential δ at that boundary, we may now write the general current equation and separate the variables. From Eqn. (5.5), we have:

$$I_d = - Z D_n Q_m \frac{d\delta}{dy}$$

which can be rearranged to give

$$\frac{I_d}{Q_m} dy = - Z D_n d\delta.$$

Substituting Eqn. (5.19) for Q_m and integrating along the channel from y_T to y_2 ,

$$I_d \int_{y_T}^{y_2} \frac{e^{K_{T2}(y_2-y)}}{Q_{m2}} dy = - Z D_n \int_{\delta_T}^{\delta_2} d\delta$$

or

$$I_d = \frac{- Z D_n Q_{m2} K_{T2} (\delta_2 - \delta_T)}{(Q_{m2}/Q_{mT} - 1)} \quad (5.20a)$$

for $Q_{m2} \neq Q_{mT}$.

In the case where $Q_{m2} = Q_{mT}$, Eqn. (5.20a) reduces to:

$$I_d = \frac{- Z D_n Q_{m2} (\delta_2 - \delta_T)}{(y_2 - y_T)} \quad (5.20b)$$

On the other side of the transition point y_T , the channel is weakly inverted. If we write the inversion charge in terms of the independent variables affecting it at any point,

$$dQ_m = \frac{\partial Q_m}{\partial \delta} d\delta + \frac{\partial Q_m}{\partial U_g} dU_g$$

we have from Eqn. (5.11) $\left. \frac{\partial Q_m}{\partial \delta} \right|_{U_g} = - Q_m$ since here U_g is also a constant

(U_{sm}) and from Eqn. (5.12), $\frac{\partial Q_m}{\partial U_g} = \frac{\partial Q_m}{\partial U_f}$. As can be seen in Fig. 5.2, Q_m in weak inversion is a very strong function of substrate doping and is exponential in nature, increasing as U_f decreases. Let us represent $\frac{\partial Q_m}{\partial U_f}$ as $-K_A Q_m$ where K_A is some positive constant. Then we have:

$$\begin{aligned}\frac{dQ_m}{dy} &= -Q_m \frac{d\delta}{dy} - K_A Q_m \frac{dU_f}{dy} \\ &= -Q_m \frac{d\delta}{dy} + K_1 K_A Q_m\end{aligned}$$

Now, from Eqn. (5.5) and (5.6), we have:

$$\frac{d\delta}{dy} = -\frac{I_d}{Z D_n Q_m} \quad (5.21)$$

Therefore,

$$\frac{dQ_m}{dy} = \frac{I_d}{Z D_n} + K_1 K_A Q_m \quad (5.22)$$

Solving this differential equation, we have:

$$Q_m = \frac{I_d}{Z D_n} (y - y_1) + Q_{m1} e^{K_1 K_A (y - y_1)} \quad (5.23)$$

At $y = y_T$, we have:

$$Q_{mT} = \frac{I_d}{Z D_n} (y_T - y_1) + Q_{m1} e^{K_1 K_A (y_T - y_1)} \quad (5.24)$$

Since Q_m is a negative quantity, the two terms on the right-hand side of Eqn. (5.22) oppose each other. Considering that Q_{m1} corresponds to

weak inversion and Q_{mT} to strong inversion, we must have $Q_{mT}/Q_{m1} > 1$ so that the exponential term in Eqns. (5.23) and (5.24) is dominant over the linear term. We may therefore treat the surface charge variation in the same manner as for a strongly inverted region, namely

$$Q_m = Q_{m1} e^{K_{T1}(y-y_1)}$$

where

$$K_{T1} = \frac{\log(Q_{mT}/Q_{m1})}{y_T - y_1} \quad (5.25)$$

and the current in that region becomes:

$$I_d = \frac{-Z D_n Q_{mT} K_{T1} (\delta_T - \delta_1)}{(Q_{mT}/Q_{m1} - 1)} \quad , \quad Q_{mT} \neq Q_{m1} \quad (5.26a)$$

$$= \frac{-Z D_n Q_{m1} (\delta_T - \delta_1)}{(y_T - y_1)} \quad , \quad Q_{mT} = Q_{m1} \quad (5.26b)$$

In the foregoing analysis, it was assumed that y_T and δ_T were known. We will now develop an iterative scheme to solve for δ_T and y_T and thereby determine the current flow in the graded region.

Consider first the situation where $U_{s2} > \delta_2 + 2U_{f2}$ and $U_{s1} < \delta_1 + 2U_{f1}$. An equation similar to Eqn. (5.14) for the heavily inverted region is obtained for the non-equilibrium case by using Eqn. (5.14), i.e.

$$U_s = U_{s2} + K_1(y_2 - y) - (\delta_2 - \delta) \quad (5.27)$$

Combining Eqns. (5.27) and (5.17) yields:

$$y_T = y_2 - \frac{(U_{sm_2} - U_{s_2} + \delta_2 - \delta_T)}{K_1 + K_s} \quad (5.28)$$

where $\delta_T = \delta_2$ is the first estimate of δ_T .

Equations (5.26) and (5.20) are now used to calculate currents I_{dT1} and I_{dT2} in the weakly inverted and strongly inverted regions, respectively. The requirement of current continuity allows us to adjust δ_T , and from Eqn. (5.28) also y_T , until $I_{dT1} = I_{dT2}$. This method was found to converge very rapidly since the initial estimate for δ_T is close to the converged value.

When the applied gate voltage is high enough to heavily invert the whole of the graded region, then $y_T < y_1$, as calculated from Eqn. (5.28). We then take $y_T = y_1$ and use Eqn. (5.20) to calculate the drain current with $Q_{mT} = Q_{m1}$, $\delta_T = \delta_1$.

When the applied gate voltage is low and the drain voltage is high enough that the graded region is not heavily inverted at any point, then $y_T > y_2$. We take $y_T = y_2$, $Q_{mT} = Q_{m2}$, $\delta_T = \delta_2$ and use Eqn. (5.26) to calculate the drain current.

In both cases, when $y_T = y_1$ and $y_T = y_2$, no iterations are required to calculate the drain current for the graded region.

If it is assumed that, over the range of values of substrate doping used in the graded region, mobility varies linearly with substrate doping, then it varies exponentially with distance along the graded channel. Representing this relationship as

$$\mu_n = \mu_{n2} e^{-K_m(y_2 - y)}$$

where

$$K_m = \frac{\log(\mu_{n2}/\mu_{n1})}{(y_2 - y_1)}$$

enables us to include variable mobility into the expression for drain current in the graded region. Thus Eqn. (5.20a) becomes

$$I_d = -Z(K_m + K_{T2})(\delta_2 - \delta_T) \cdot \frac{\gamma_2}{\gamma_2/\gamma_T - 1}$$

where

$$\gamma = D_n Q_m.$$

Similar expressions are obtained for Eqn. (5.20b) and (5.26a,b).

5.3 The Drain Region

For modelling purposes, the whole device can be divided into the following four regions:

Region 1: $0 \leq y \leq y_1$, the uniformly doped source region where $U_f = U_{fp}$.

Region 2: $y_1 \leq y \leq y_2$, the graded region where $U_f = U_{fp} - K_1(y - y_1)$.

Region 3: $y_2 \leq y \leq y_3$, the uniformly doped drain region under the gate

where $U_f = U_{fB}$.

Region 4: $y_3 \leq y \leq y_d$, the uniformly doped region with no gate electrode

adjacent to the drain junction where $U_f = U_{fB}$.

These regions are shown schematically in Fig. 5.6. Regions 1 and 3 can be treated as normal uniform channel devices but region 4 cannot since it has no gate electrode.

Although the surface of region 4 is covered by a thick field oxide, the effective surface state charge in the oxide Q_{ss} is essentially the same as that for the thin gate oxide [36]. Therefore, in a strictly one-

Fig. 5.6. Schematic showing division of surface of DMOS transistor into four 'model' regions.

dimensional analysis of this region, the surface potential U_s will adjust itself in such a way that the total charge in the semiconductor is equal to Q_{ss} which is independent of applied gate and drain voltages. Therefore, if the thick oxide were replaced by the same thin oxide covering the rest of the device and a floating metal gate were added, the effective gate potential would follow the surface potential such that

$$U_g - U_s = \frac{q}{kT} \frac{Q_{ss}}{C_{i1}}$$

In an actual device, this one-dimensional behaviour is not a good representation although it predicts that the inversion layer charge Q_m is a maximum at y_3 and falls off as the channel potential ϕ , and therefore U_s .

increases towards $\delta=U_d$ at the drain.

5.3.1 The Fringing Gate Field

In the region $0 < y < y_3$, all field lines emanating from the gate electrode were assumed to be vertical and to terminate on charges at the semiconductor surface. This is true for all points covered by the gate electrode. However, when this electrode ends abruptly, there exists a fringing gate field which affects the surface conditions in regions adjacent to the gate. In these regions, the field lines are no longer vertical. This situation is illustrated in Fig. 5.7 where, for convenience, the region under consideration is taken to be $0 \leq y \leq L$.

In order to predict how this field affects the surface potential, we calculate the position-dependent vertical component of the field and interpret it in terms of an effective gate voltage for a uniformly thin gate oxide of thickness, X_i . It is assumed that the field lines shown in Fig. 5.7 are condensed to emanate from the corner of the gate metal at $y=0$. This approximation allows a straightforward calculation of the field components to be made.

Since the substrate doping and the surface state charge are uniform across this region, the flat-band voltage is constant and the effective gate voltage becomes:

$$\begin{aligned} U_g(y) &= U_{FB} + U_{gg} \sin \left(\tan^{-1} \frac{X_i}{y} \right) \\ &= U_{FB} + \frac{U_{gg}}{\sqrt{1+y^2/X_i^2}} \end{aligned} \quad (5.29)$$

where U_{gg} is the applied gate voltage on the gate electrode.

Fig. 5.7. Representation of the fringing gate field.

The fringing factor given by:

$$\frac{1}{\sqrt{1+y^2/X_i^2}} = \frac{U_g(y) - U_{FB}}{U_{gg}} \quad (5.30)$$

predicts the effective gate voltage at any point $0 \leq y \leq L$ relative to that at $y=0$, as shown in Fig. 5.8. The slope of this function is also plotted in Fig. 5.8 and we see that the effective gate voltage within 3 times the oxide thickness of the end of the gate electrode is a substantial fraction of the effective gate voltage at $y=0$. In fact, it can be significant even at the drain ($y=L$) for large values of applied gate voltage (U_{gg}).

As shown in Fig. 5.8 by the dashed lines, the essential features of this fringing effect can be taken into account by assuming a linear fall-off for U_g until it reaches a constant value given by

$$U_g = U_{FB} + U_{gg} \frac{X_i}{L} \quad (5.31)$$

By doing this, the problem of discontinuities at the boundary between regions 3 and 4 of the overall model are avoided and, at the same time, accuracy is improved.

The above approximation to the effective gate voltage in region 4 implies the definition of a new point y_4 which creates two sub-regions.

This point is given by:

$$y_4 = y_3 + 3X_i \left(1 - \frac{X_i}{L_4}\right) \quad (5.32)$$

Therefore, in the sub-region $y_3 \leq y \leq y_4$, U_g is given by:

Fig. 5.8. Normalized effective gate potential due to fringing gate field.

$$U_g = U_{FB} + U_{gg} \left(1 - \frac{y-y_3}{3x_i} \right) \quad (5.33)$$

where the coordinates of Fig. 5.6 have been used.

The slope of the model gate potential is now a constant:

$$\frac{1}{U_{gg}} \cdot \frac{dU_g}{d\left(\frac{y}{x_i}\right)} = -\frac{1}{3}$$

as shown in Fig. 5.8 and it approximates the horizontal component of the fringing field.

Under equilibrium conditions, the requirement that zero current flows in the presence of a constant horizontal field indicates that the electron density distribution must be exponential in nature. This ensures that drift and diffusion current components are equal and opposite. Since the above field is positive, the electron density in the surface inversion layer must decrease exponentially from y_3 to y_4 in equilibrium. This also approximates the variation of the surface inversion layer charge density Q_m if it is assumed that the space charge layer thickness is constant.

This situation closely parallels that in region 2 in that the model contains an effective gate potential which varies linearly and the mobile carrier surface charge density varies exponentially with distance along the channel. Thus, the solution for current flow in this sub-region is essentially the same as that for region 2 and will not be repeated here.

We now have regional solutions of the DMOS transistor assuming the GCA is valid at every point. It now remains to consider the case where saturation of one or more regions occurs and the GCA may no longer be valid over a substantial portion of the channel.

5.4 Saturation

Drain current saturation in an MOS transistor is caused by either channel 'pinch-off' or by carrier velocity saturation depending on which mechanism occurs first. Velocity saturation usually occurs first in those devices which have short channel lengths and are being operated at relatively high gate voltages. This situation is easily modelled by the incorporation of field-dependent mobility in the drain current expression (Eqn. 2.45) and results in the actual channel length L being replaced by an 'effective' channel length L_{eff} , which is larger than L , given by Eqn. (2.49).

Saturation by 'pinch-off' was treated in Section 2.4.2 where a theoretical two-dimensional channel-shortening model was developed.

Thus, regions 1 and 3 and 4B ($y_s \leq y \leq y_d$) of the DMOS transistor are well modelled in saturation as long as the GCA remains valid at the source end of each of these regions. This is true of region 1 where the source junction is at a fixed potential but may not be true for any of the other regions depending on the applied gate and drain voltages. This problem will be dealt with later.

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In Section 2.4.1, it was concluded that the effect of carrier velocity saturation in a region where the GCA is valid is to increase the effective length of that region in the current expression. The effective length, given by Eqn. (2.49), is:

$$L_{\text{eff}} = L(1 + E_{\text{av}}/E_c)$$

where L is the physical length of the region, E_{av} is the average longitudinal surface field and E_c is the critical field for scatter-limited velocity. Even though a similar relation cannot be obtained in closed form for regions 2 and 4A ($y_3 \leq y \leq y_4$), it will be assumed here that the effect is substantially the same if we define the average field as:

$$E_{\text{av}} = kT(\delta_d - \delta_s)/qL$$

where δ_d and δ_s are the drain and source channel potentials, respectively, and L is the physical length of the region (or sub-region) being considered.

We will now consider the various saturation conditions which may arise when the applied gate voltage U_{gg} is fixed and the drain voltage U_d is varied from very low to very high levels.

5.4.1 Region 1 Saturated

If the gate voltage is low enough that the surface of region 1 is not strongly inverted at equilibrium, then the transition point y_T in region 2 will have some value $y_1 < y_T < y_2$ at equilibrium and as U_d is increased y_T will move towards the drain in accordance with Eqn. (5.28). The channel

potential δ_1 at the drain end of region 1 increases and at some point will cause this region to go into saturation. The GCA is thus no longer valid at $y=y_1$ and Eqn. (2.41) of the one-dimensional theory cannot be used to calculate Q_m and U_s at $y=y_1$. These values must, however, be known for the solution of region 2 to be obtained. We therefore turn to the saturation model of Section 2.4.2 and in particular, Eqn. (2.54), which gives us the longitudinal surface field at $y=y_1$. This value can be inserted into the field-dependent mobility expression (Eqn. (2.48)) to obtain the effective mobility. If it is assumed that current flow in the drain space charge region of the saturated device (region 1) is purely by drift, then the mobile charge at the drain end of this region is given by:

$$Q_{m_d} = - \frac{q I_d}{kT Z v_{sd}} \quad (5.34)$$

where I_d is the drain current in saturation given by Eqn. (2.55) and v_{sd} is the carrier drift velocity defined by

$$v_{sd} = \mu_n E_{sd} \quad (5.35)$$

The surface potential at the same point is given by:

$$U_{sd} = \delta_d - \delta_s - (U_{s_1} - U_{ss}) \quad (5.36)$$

where the general subscripts denoting source and drain ends of the region have been used.

The normal one-dimensional model for current in region 2 can thus

be retained in this instance as long as the drain end of region 2 remains strongly inverted.

One of the unusual features of a DMOS transistor is that more than one saturation region may exist simultaneously separated by a region of strong inversion where the GCA applies. This is the subject of the next saturation condition.

5.4.2 Region 4 Saturated

When region 4 becomes saturated to the point that the source of sub-region 4B ($y=y_4$) is depleted (body effect), then all of sub-region 4B is depleted as well as a portion of 4A. We must then find a point y_{T4} in 4A at which the transition between strong inversion and weak inversion or depletion takes place. This, of course, assumes that region 3 is not saturated.

To find this transition point, we can use the same procedure as was used in region 2. The variation of U_{sm} given by Eqn. (5.15) in $y_3 \leq y \leq y_4$ can be approximated by a straight line similar to Eqn. (5.17):

$$U_{sm} = U_{sm3} - K_s(y-y_3) \quad (5.37)$$

where

$$U_{sm3} = U_{sm}(y_3) = U_{sm2}$$

and

$$K_s = \frac{U_{sm3} - U_{sm4}}{y_4 - y_3}$$

Since $dU_s \approx d\delta$ in the heavily inverted region under consideration, we have:

$$U_s = U_{s_3} + \delta - \delta_3 \quad (5.38)$$

We make a first estimate $\delta(y_{T_4}) = \delta_4$ and equate Eqns. (5.37) and (5.38) solving for $y = y_{T_4}$. Once y_{T_4} is estimated, we can find the effective gate voltage at that point and then the inversion charge Q_m .

The normal exponential charge current expression can now be used to estimate the drain current for that sub-region ($y_3 \leq y \leq y_{T_4}$).

If $L_4 \gg X_i$ the effective gate voltage over the major portion of region 4 is low compared to that over the rest of the device. Therefore, the two-dimensional analysis of Section 2.4.2 can be approximated by a one-dimensional analysis of the drain depletion region. Equation (2.50) then becomes:

$$E_{sd}^2 = E_{s_1}^2 + \frac{6q^2 N}{kT\epsilon_s} (U_{sd} - U_{s_1}) - \frac{6q}{kT\epsilon_s X_1} \int_{U_{s_1}}^{U_{sd}} Q_m dU_s \quad (5.39)$$

where the analysis assumes $E_x = 0$ at the surface. We also have

$$\int_{U_{s_1}}^{U_{sd}} Q_m dU_s = - \frac{I_d}{Z} \left[\frac{(U_{sd} - U_{s_1})}{v_{sm}} + \frac{qL}{kT\mu_o} \right] \quad (5.40)$$

Applying Eqns. (5.39) and (5.40) to the drain space charge region of region 4, we have:

$$L = y_d - y_{T_4}$$

$$U_{sd} - U_{s_1} = \delta_d - \delta_{T_4}$$

$$E_{s_1} = E_{s_{T_4}}$$

and $I_d = I_{d_4}$

as calculated for the sub-region $y_3 \leq y \leq y_{T_4}$.

At low levels of current, the bulk charge term in Eqn. (5.39) is dominant and the longitudinal surface field E_s varies linearly from y_{T_4} to y_d . In the other extreme, when the current is large and the carriers reach their scatter-limited velocity, Q_m is constant and the field again varies linearly. Although it is true that the field is not linear except in the above two limiting cases, it is maintained here that the linear approximation as formulated here is much better than the usual depletion approximation of first-order theory since the effects of both the mobile carriers and velocity saturation are included in the calculation of drain surface field. The average field in the drain space charge region is then

$$E_{av} = \frac{E_{s_{T_4}} + E_{sd}}{2}$$

and the difference in channel potential between the ends of this region is

$$\delta_d - \delta_{T_4} = E_{av}(y_d - y_{T_4}). \quad (5.41)$$

This gives us an independent estimate of δ_{T4} which in turn is used in Eqn. (5.38) to obtain a new estimate of y_{T4} and as a result also I_{d4} . This process is continued until the new value of δ_{T4} given by Eqn. (5.41) is the same as the previous value.

5.4.3 Region 3 Saturated

Saturation of region 3 implies that all of region 4 ($y_3 \leq y \leq y_d$) is depleted. In this case, δ_3 is estimated and drain current for region 3 is calculated using Eqn. (2.55). A one-dimensional analysis similar to that presented in the foregoing section for region 4 is then used to obtain a new estimate of δ_3 . This process is then repeated until δ_3 converges.

If region 1 is not heavily inverted, a substantial portion of the applied drain potential will be dropped across this region and a point will be reached where the source of region 3 will pinch off. When this point is reached, all of regions 3 and 4 will be depleted and it no longer is possible to express the current in this depleted region as a unique function of its boundary conditions. When this occurs, it will be assumed that all subsequent increases in drain voltage will be developed entirely across this depleted region, i.e. the current remains constant. This corresponds to the situation where the applied gate voltage is low ($-V_T$). Verification of this low level effect will be shown in Chapter 6.

5.5 Conclusion

A new DMOS transistor model has been presented. It features analytical solutions for specific regions of the device which are identified and characterized by the shape of the diffused profile and the device geometry. These model solutions also have continuous and well-matched boundary conditions.

In Chapter 6, we will compare the results of model calculations to experimental measurement and explore the model limitations.

CHAPTER 6

THEORETICAL AND EXPERIMENTAL RESULTS

Since the value of peak doping in the channel of a DMOS transistor is very sensitive to process variations [38], it is not advisable to rely entirely on the nominal profile parameters as calculated from the process data in Chapter 5 and listed in Fig. 5.1. This fact was evident during evaluation of the processed wafers, since there was a large spread of threshold voltages measured (-2.0 to +1.0 volts). In this chapter, the problem of evaluating device model parameters will be dealt with, then the predicted terminal electrical characteristics will be compared with experiment.

6.1 Model Parameter Determination

Due to the above considerations and the large number of parameters needed in a DMOS model, these parameters must be systematically obtained. The procedure is explained below.

6.1.1 Gate Oxide Thickness

Although the gate oxide thickness was designed to be 1000Å, this was not confirmed by capacitance measurements on a number of devices. By comparing the value of $C_{\max}$ measured on rectangular NMOS and adjacent rectangular DMOS devices with different gate areas (see Fig. 6.1), where

$$C_{\max} = C_i + C_{GS} + C_{GD} + C_s,$$

Fig. 6.1. Typical high frequency (1MHz) gate capacitance vs gate voltage characteristics.

the values of oxide thickness was determined to be 770Å. The value calculated for C_i (4.48×10^{-8} pF/cm²), when applied to circular geometry 10μ and 20μ DMOS devices, gave very consistent agreement with measurements. It is not known why the gate oxide was so much thinner than expected.

6.1.2 Substrate Doping (π Region)

Two independent methods were used to determine the surface concentration of impurities. Both are measurements on a rectangular NMOS device:

- i) If $C_{\max}$ is the maximum capacitance per unit area and $C_{\min}$ is the minimum capacitance per unit area, then

$$C_{\max} - C_{\min} = \frac{C_i^2}{C_i + C_d}$$

where C_d is the depletion capacitance per unit area. Solving this equation for C_d allows us to determine the substrate Fermi level U_f by using [39]:

$$C_d = \frac{\epsilon_s}{L_D} (1.6U_f - 1)^{-1/2}$$

where

$$L_D = \frac{1}{2} \left[\frac{kT\epsilon_s}{q^2 n_i} \cdot e^{-U_f} \right]^{1/2}$$

and

$$e^{U_f} = \frac{N}{n_i}$$

ii) To confirm the value determined above ($1 \times 10^{14} \text{ cm}^{-3}$) the 'threshold voltage', V_T , of the RN MOS (rectangular NMOS) device was measured as a function of substrate bias, V_{BS} , and the following equation was used to determine N_A :

$$|V_T| = |V_{T0}| + \frac{(2\epsilon_s q N_A)^{1/2}}{C_i} \left[|V_{bs} + 2\phi_f|^{1/2} - (2\phi_f)^{1/2} \right]$$

which simplifies to:

$$|V_T| = |V_{T0}| + \frac{(2\epsilon_s q N_A)^{1/2}}{C_i} \cdot V_{bs}^{1/2}, \text{ for } V_{bs} \gg 2\phi_f$$

6.1.3 Surface State Charge Density

Measurements of threshold voltage, V_{T0} , on the RN MOS device showed that the equivalent surface state charge density, Q_{ss}/q , was approximately $1.2 \times 10^{12} \text{ cm}^{-2}$. This value is very high for (100) oriented silicon and indicates that the processing environment was not clean enough to provide high quality surfaces.

6.1.4 Peak Doping and Other Diffused Channel Parameters

The parameter which is most directly related to peak doping is the DMOS threshold voltage. Using the same standard equation as was used to determine Q_{ss}/q , i.e.

$$V_T = \phi_{ms} + 2\phi_F - \frac{Q_{ss}}{C_i} + \frac{\sqrt{2\epsilon_s q N_A (2\phi_f)}}{C_i} \quad (6.1)$$

the value N_A at the peak of the diffused profile can be approximated. For the device under consideration here, which was selected for its positive

threshold and good drain characteristics, the value for peak doping was determined to be $N_p = 1.8 \times 10^{17} \text{ cm}^{-3}$. Questions of boron impurity redistribution during gate oxidation aside, this value is almost an order of magnitude higher than that calculated originally for the 'nominal' profile. To illustrate that this difference is possible, it is shown here that the impurity distribution, hence peak doping, are very sensitive to process changes. There are many ways to adjust the profile by changing the process parameters. One adjustment which is very reasonable is to reduce the gate oxide growth time to reflect the measured value. Reducing this time by 25% results in an increase in peak doping from 2.3×10^{16} to $5.4 \times 10^{16} \text{ cm}^{-3}$. The diffused channel length also increases from $2.3 \mu\text{m}$ to $2.5 \mu\text{m}$. Pocha et al [38] found it necessary to adjust the boron profile by multiplying the surface concentration by 1.2 to get better agreement between theory and experimental threshold voltage. In fact, there is enough scatter in their data to justify using a multiplying factor of 2.0 to obtain agreement with one data point. This implies that there may be another factor causing anomalous boron diffusion in addition to normal (expected) process tolerances.

Shown in Fig. 6.2 are the results of simulating the lateral profiles using Eqn. (3.1) with the above adjustments. It can be seen that the effects are predominantly felt at the source junction which gets shallower as the peak doping is increased. Multiplying the boron profile by a factor of 2.0 results in a peak doping of 1.74×10^{17} (a ~3x increase). This corresponds to the value of peak doping derived from measurements made on the device simulated here. This profile is felt to be representative

Fig. 6.2. Diffused channel profiles.

- a) Nominal
- b) Gate oxidation time reduced by 25%
- c) Same as b) with Predeposition $\sqrt{Dt} + 50\%$ for Boron, -50% for Phosphorous
- d) Same as b) with final $C_{O_2} \times 2.0$

of this device and represents one extreme among those measured (most had negative threshold voltages).

6.1.5 Mobility

Surface mobility has been one of the most widely studied topics in MOS theory. The standard approach taken is to derive mobility by measuring the slope of g_d vs V_G curves near zero conductance value. To account for the departure of drain conductance from straight line behaviour at high gate voltages, it is usual to allow mobility to fall off monotonically until it reaches one-half its low-gate-field value [4], [39]. The equation normally takes the form [4]:

$$\mu = \frac{\mu_0}{1 + (V_G - V_T)/V_K} \quad (6.2)$$

where μ_0 is the measured low-field value and V_K is the gate voltage at which $\mu = \mu_0/2$.

This mobility reduction model is easy to implement in the triode region of operation since it can be used as a simple current-reduction factor. However, the situation becomes complex in saturation, especially in situations where carrier velocity saturation takes place.

More complete models of MOS operation [8], [7] which do not use the "shallow channel" approximation ~~do not~~ require the use of gate-field-dependent mobility to fit theoretical with experimental results except at very high gate voltage levels. Field dependent mobility is therefore not required in the present model since this model is based on [7]. However, since the impurity doping level in the channel of a DMOS transistor can

vary by several orders of magnitude the effect of this profile on surface mobility must, in some way, be included. It is well known that, with well prepared surfaces, the surface mobility can approach one-half its value in the bulk [35]. For the device under investigation here, the bulk mobility values corresponding to the doping levels at the drain and at the point of peak doping are 1300 and $450\text{cm}^2/\text{V-sec}$, respectively. This factor of 3 variation in the bulk values is due primarily to the increased effect of ionic scattering in the more heavily doped region. To find the relative values of mobility at the surface, the most logical approach to take is to model the effect of the surface as a second type of lattice scattering effect which is not present in the bulk. Thus,

$$\frac{1}{\mu_n} = \frac{1}{\mu_o} + \frac{1}{\mu_{ls}} \quad (6.3)$$

where μ_o is the bulk value of mobility which can be readily obtained from standard curves [37], μ_n is the measured value of surface electron mobility, and μ_{ls} is the 'surface lattice' mobility.

Therefore, by measuring the surface mobility of an adjacent uniform substrate NMOS device, a value for μ_{ls} may be determined using Eqn. (6.3) which 'characterizes' the surface. This value may then be used in conjunction with different values of μ_o corresponding to different bulk values of doping to predict the surface mobility at the point of peak doping in the channel. Eqn. (6.3) was used to calculate μ_{ls} as a function of μ_n with μ_o fixed ($\mu_o = 1300\text{cm}^2/\text{V-sec}$). This function is plotted in Fig. 6.3 as well as curves of the predicted values of mobility at the point of peak doping (μ_{ns} for source). These curves predict that, for a measured

Fig. 6.3. Electron mobility at the source end of the device (μ_{ns}) as a function of the measured value of mobility in the low-doped drain end (μ_{nd}) with bulk value of μ_{os} (μ_{os}) as a parameter. Also, resulting surface lattice mobility μ_{ls} in Eqn. (6.3) vs μ_{nd} for $\mu_{od}=1300\text{cm}^2/\text{V-sec}$.

$\mu_{nd}=300$ (μ_{nd} for drain), $\mu_{ns}=200$ when $\mu_{os}=450$. In this case, it is apparent that surface scattering is more dominant than ionic scattering.

In the present DMOS model, separate values of mobility are allowed for the source and drain ends of the device. The model automatically varies the mobility in the graded region (region 2) in an exponential fashion between the two extremes. Further comments on the use of variable mobility will be made in the next section where experimental and theoretical results are compared.

6.2 Comparison of Theory with Measurement

In Table 6.1 are listed the input parameters used to model the 10 μ m circular DMOS devices shown in Fig. 3.4.

Table 6.1. Device data for an experimental DMOS transistor.

<u>Parameter</u>	<u>Value</u>	<u>Units</u>
N_p	1.8×10^{17}	cm^{-3}
N_B	1.0×10^{14}	cm^{-3}
X_i	770	$\text{\AA}$
Z	420	microns
L	5.5	microns
y_2	2.5	microns
y_1	0.46	microns
μ_{ns}	140	$\text{cm}^2/\text{V-sec}$
μ_{nd}	190	$\text{cm}^2/\text{V-sec}$
Q_{ss}/q	1.2×10^{12}	cm^{-2}

These parameters were derived in the manner described in Section 6.1. Theoretical curves of I_D vs V_D , g_d vs V_g , and g_m vs V_g are compared to measurements in Figs. 6.4-6.6.

Fig. 6.4. I_D - V_D characteristics for 10 μ m DMOST.

Fig. 6.5. Comparison of theoretical and experimental drain conductance curves for 10 μ m DMOST.

Fig. 6.6. Theoretical and experimental gate transconductance curves for 10 μ m DMOST.

The simulations of device characteristics were carried out with region 4 of the model set equal to zero. It was found that the inclusion of this region caused a large increase in the computational effort required. The device under study, in fact, has a very short region 4 ($\sim 1\mu\text{m}$ for perfectly aligned devices). Even though the I_D - V_D characteristics of Fig. 6.4 show good agreement, the effect of this uncovered region can be seen. At high gate voltages, the theoretical curves are steeper in non-saturation and flatter in saturation than the measured curves. The effect of region 4 would be to effectively lower the drain conductance at low drain voltages and increase it at higher drain voltages since it will cause the device to behave as if it had a shorter channel length. The situation is also complicated by the presence of carrier velocity saturation which tends to reduce the discrepancy.

The low drain voltage situation is well depicted by the drain conductance curves of Fig. 6.5. The 20% discrepancy between theory and experiment at $V_g = 5.0$ volts can be shown to be due entirely to the influence of region 4.

As can be seen in Fig. 6.4 at the knee of the theoretical curves, there is an anomalous behaviour over a small range of drain voltage which causes an unexpected change in slope of the curves. This effect is exemplified by the gate transconductance curves of Fig. 6.6 where the theoretical curves show reasonable agreement with the experimental except for the dips or oscillations which occur at these same operating points. In order to shed more light on the situation, the modes of operation of the DMOS transistor were determined from printouts of internal regional device

behaviour and plotted in Fig. 6.7. It can be seen that all four possible modes of operation occur over the range of gate and drain voltages simulated, viz.

- A: Region 1 Saturated/Region 3 Saturated
- B: Region 1 Linear/Region 3 Saturated
- C: Region 1 Linear/Region 3 Linear
- D: Region 1 Saturated/Region 3 Linear

Comparison of these curves to Figs. 6.4 and 6.6 indicates that the anomalous behaviour occurs where Region 1 is just entering saturation. When this occurs, the model relies on the Region 1 drain field prediction to determine a value of Q_m consistent with current continuity requirements to begin the Region 2 calculations. If this drain field is high enough to cause saturation (channel shortening) but not carrier velocity saturation, the neglect of mobile carriers in the saturated region will cause an over-estimation of the field (E_{sd1}) and an equal underestimation of Q_m at this point. This would, in turn, reduce the value of current calculated for Region 2. Subsequent iterations may, in some cases, cause Region 1 to oscillate into and out of saturation. A relatively small increase in V_D beyond this point causes a very large increase in the value of E_{sd1} and results in scatter-limited velocity effects of increasing importance. This allows Q_m at this point to rise so that the I_D - V_D characteristic 'recovers'. This problem can only be satisfactorily resolved if the saturation model is improved to take into account the effect of mobile carriers in the depleted region [41].

Fig. 6.7. Regions of operation calculated for the $10\mu\text{m}$ DMOST.
 A: Region 1 Saturated/Region 3 Saturated
 B: Region 1 Linear/Region 3 Saturated
 C: Region 1 Linear/Region 3 Linear
 D: Region 1 Saturated/Region 3 Linear

Referring again to Fig. 6.4, the overestimation of current in saturation (Regions D,A of Fig. 6.7) can also be explained by the neglect of mobile carriers in the saturation model. Since Region 1 of the DMOS device model is very short ($\sim 0.5\mu\text{m}$), the resulting overestimation of E_{sd1} and therefore of the amount of channel shortening will cause unusually large increases in the value of I_D calculated.

6.3 Internal Device Behaviour

In order to further illustrate the modes of operation of a DMOS transistor, Figs. 6.8-6.12 were drawn. They show variations along the channel of mobile inversion layer charge, Q_m , surface potential, U_s , normalized longitudinal field E_s , and channel potential, δ , for different values of applied gate voltage, V_G , with drain voltage, V_D , as a parameter. The curves drawn through the points shown are intended to provide a picture of the shape expected for these variables based on knowledge of model behaviour in the various regions.

At very low values of gate voltage ($V_G < 2.0\text{V}$), the source end of the channel is not strongly inverted. It, as a result, goes into saturation at very low values of drain voltage (see Fig. 6.8c) and exhibits carrier velocity saturation effects in a narrow region which begins at $y=y_1$ and spreads into Region 1 and Region 2 simultaneously. This spreading effect can be seen in Figs. 6.13 and 6.14.

In Fig. 6.13, the amount of channel shortening for Region 1 is plotted versus gate voltage with drain voltage as a parameter. It can be seen that for $V_D=1$ volt Region 1 is saturated for $V_G < 2$ volts and the

(a) Q_m vs y

(b) U_s vs y

(c) E_s vs y

(d) δ vs y

Fig. 6.8. Model calculations of Q_m , U_s , E_s , δ vs y for $V_G=1.0V$.

Fig. 6.9. Model calculations of Q_m , U_s , E_s , δ vs y for $V_G = 2.0V$.

(a) Q_m vs y (b) U_s vs y (c) E_s vs y (d) δ vs y Fig. 6.10. Model calculations of Q_m , U_s , E_s , δ vs y for $V_G = 3.0V$.

Fig. 6.11. Model calculations of Q_m , U_s , E_s , δ vs y for $V_G=4.0V$.

Fig. 6.12. Inversion layer charge, surface potential, longitudinal

Fig. 6.13. Model calculations of Region 1 channel shortening as a function of gate and drain voltage.

Fig. 6.14. Model calculations for position of transition point y_T in Region 2 as a function of gate and drain voltage.

channel shortening model predicts an effective channel length, $L_1' = .45L_T$ for $V_G = 1.0$ volt. Similarly, in Fig. 6.14 is shown the distance from the beginning of Region 2 to the transition point (where the channel becomes strongly inverted), normalized to the total length of Region 2 versus gate voltage. Here it is observed that at low gate voltages a small drain voltage is required to cause y_T to move towards the drain. As expected, at higher gate voltages, this movement is less rapid and does not begin until V_D rises above a threshold value. Similarly, in Region 1 at higher gate voltages, L_1' becomes shorter as the drain voltage is increased above saturation. The rate of change of L_1' is much less than that described above for Region 2 since Region 1 is modelled as a region of uniform background doping. This is not physically correct, as discussed previously, and requires a model parameter, y_1 , which is less than $2y_p$. Thus, a section of this region from the metallurgical junction to approximately half the distance of the point of peak doping is ignored. This distance is approximately equal to the zero bias source junction depletion half-width ($\sim 0.2\mu\text{m}$).

By comparing Figs. 6.8-6.12, it can be seen that for low values of V_G , Q_m in Region 1 is very low and most of the drain voltage is therefore dropped across this region. Therefore, as drain voltage is increased from zero Region 1 will saturate first and the field E_{sd1} will quickly increase to the point where body effects lower the value of Q_m in Region 3 so that this region also goes into saturation at higher drain voltages (i.e. we have moved from C to D to A in Fig. 6.7). At higher gate voltages, Region 1 can support a higher drain voltage before going into saturation. Consequently,

Region 3 may saturate first, primarily due to body effect. This effect is easily observed as a reduction in the value of Q_m at y_2 as V_D is increased. As shown in Fig. 6.7, the two curves, which separate domains of linear operation from saturation for Regions 1 and 3, intersect at a transition point where both saturate simultaneously.

6.4 Concluding Remarks

The new DMOS transistor model has been shown to be capable of predicting DMOST characteristics over a wide range of operating conditions. The accuracy is quite good, with some exceptions which were pointed out. The input data used for the calculations were not easy to determine because of deviations of the actual profile from that predicted by the Kennedy and O'Brien [32] diffusion model due to a combination of anomalous diffusion and process tolerances. It is expected that if the profile were known in detail with better certainty the accuracy would have been better.

The DMOST model algorithm, in the form of a Fortran computer program, is listed in Appendix C. Although it has not been optimized for speed of convergence, it requires typically less than 5 iterations to calculate a value of I_D for each set of V_G and V_D values. The time required is typically 0.6sec. per point on Carleton University's Xerox Sigma 9 computer. A complete set of curves such as is shown in Fig. 6.4 has approximately 175 different (V_G, V_D) points and uses less than 2 minutes of CPU time which in this case costs \$6 per minute.

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

A new approach to modelling Double-Diffused MOS (DMOS) Transistors has been presented. It represents a significant improvement over previous DMOST models in several essential features:

1) It includes the effect of the graded portion of the channel, which for the device studied here represented about one-half the total channel length. This feature is incorporated by recognizing that the boron profile can be accurately represented by a single exponential function from a point just beyond the position of peak doping. This graded region in the model is preceded by a short source region with a uniform doping equal to that at the peak and is followed by a longer drain region with a doping level equal to that of the substrate. This profile model retains the most pertinent profile characteristics which are important to the device/process designer, yet allows a large reduction in mathematical complexity.

2) It uses the most suitable 'complete' MOST model available in such a way that the solution for the graded region is analytical^{*} when the exponential profile model is used. Perhaps more significant is the fact that this solution retains its analyticity over the full range of operating conditions from weak to very strong inversion. It results in essentially a three-region model for the whole DMOST

^{*} Requires some iterations for solution when the graded region contains a sub-region of weak inversion and one of strong inversion.

(assuming that the gate extends from source to drain) with an analytical solution applying to each region and features region boundaries that are both physically and mathematically continuous. This not only results in smooth transitions from one mode of operation to another but also allows for rapid convergence of the solutions for the three regions. This latter point is crucial to the acceptance of the model as a CAD tool. Previous models which attempted to take into account the effect of the diffused profile relied on numerical integration and suffered from poorly matched boundary conditions and an inability to handle saturation.

3) All the usual features required for complete device modelling are available including current saturation (of one or more regions simultaneously), carrier velocity saturation, and weak inversion. In addition, the model easily facilitates the use of exponentially variable mobility to account for the effect of variable doping in the channel. A technique for determining the value of mobility at the source end of the channel as a function of that measured for the drain end is also presented.

When applied to an experimental short channel DMOS device fabricated at Carleton University, the model gave, with some exceptions, good accuracy over a wide range of operating conditions.

7.2 Future Work

7.2.1 Limitations of the Model

For low values of V_G and high values of V_d such that the depletion region, which starts at the drain end of Region 1, has caused a significant channel shortening of Region 1 and has spread right across Region 2 so

that $y_T = y_2$, the algorithm does not converge. This is because the Region 3 solution cannot accommodate both ends of that region being depleted at the same time. This perhaps is not a serious limitation since once this point is reached the $I_d - V_d$ characteristic is extremely flat and the current can be taken to be constant for further increases in drain voltage. Such increases merely cause the depletion region to spread rapidly towards the drain with little effect on Region 1.

The use of variable mobility in the graded region creates a problem when carrier velocity effects are important. In order to include these effects, the average mobility of this region is used to calculate the critical field in the expression (2.49) for effective channel length. This is not compatible with the use of exponentially variable mobility used in the drain current expression and does create some convergence problems. Of course, this problem gets worse as the difference in mobility specified between source and drain increases.

7.2.2 Future Work

In addition to the above-mentioned limitations of the model which require further investigation, the following suggestions are a result of problems encountered during the course of this work.

The prediction of lateral impurity profiles at the surface under a gate oxide (based on process information) requires the use of an empirical adjustment factor to achieve agreement on threshold voltage. No satisfactory explanation has yet been given to account for this anomalous diffusion.

Clearly, a detailed investigation of lateral diffusion under a masking oxide is required in order to accurately predict such lateral profiles.

The model predicts subthreshold current which varies exponentially with gate voltage. However, the current level for any particular value of V_G in subthreshold is extremely sensitive to the details of the 'model' profile in the vicinity of the point of peak doping. Since the length of Region 1 is small (about 0.5 microns) in the device studied, changes of the order of 0.1 micron are relatively significant. No attempt was made to compare theoretical and experimental results in the subthreshold region. This requires precise profile information so that the Region 1 model can be developed further. The present model is obviously not accurate in this region because the actual "weak channel" length decreases from y_1 and shrinks towards the point of peak doping as the gate voltage is increased. It may therefore become necessary to change Region 1 to a graded model similar to that used in Region 2. In this case, however, the doping would increase from the source junction and reach a maximum at the boundary between Region 1 and Region 2.

Work is required on the model to include the effects of mobile carriers in the channel shortening model of saturated regions. This caused some unusual effects in the computed results, as discussed in Chapter 6.

Although there has been no indication that there is a limitation when applying the model to any device regardless of its doping level, this needs to be done to sort out any user problems that may exist. This includes an extensive study using the model to predict the characteristics

of devices fabricated on a well-controlled process where gates are self-aligned and where gate oxide is grown before diffusion. This requires the use of a polysilicon gate ion implanted process (standard for NMOS LSI).

The algorithm as it appears in the listing in Appendix C requires optimization to make it suitable for CAD applications.

APPENDIX A

BOUNDARY MATCHING IN THE EL-MANSY MODEL AND THE RELATIONSHIP BETWEEN U_s and δ

Poisson's equation (2.1) for the surface space charge region may be written:

$$\frac{d^2U}{dx^2} = \frac{q^2}{kT\epsilon_s} (n+N) \quad (A.1)$$

where the GCA is assumed and the hole density is neglected. The electron density distribution may then be written:

$$n = \frac{kT\epsilon_s}{q^2} \frac{d^2U}{dx^2} - N \quad (A.2)$$

For this distribution, we have:

$$\begin{aligned} \int n dU &= \frac{kT\epsilon_s}{q^2} \int \frac{d^2U}{dx^2} \frac{dU}{dx} dx - \int N dU \\ &= \frac{kT\epsilon_s}{q^2} \int \frac{dU}{dx} \cdot d\left(\frac{dU}{dx}\right) - \int N dU \end{aligned}$$

Integrating from the surface to the neutral substrate,

$$\begin{aligned} \int_0^{U_s} n dU &= N \left[\frac{kT\epsilon_s}{2q^2 N} \left(\frac{dU}{dx}\right)_s^2 - U_s \right] \\ &= n_i e^{U_f} (n^2 + n/a - U_g) \end{aligned} \quad (A.3)$$

Since Eqn. (A.3) was obtained without knowledge of the detailed nature of the electron distribution, it must necessarily be true for any distribution that obeys Poisson's equation and therefore is a general expression which is invariant with respect to the type of distribution under consideration. It depends only on the boundary conditions of the space charge region which are determined from the application of charge neutrality and Gauss' law.

For the model distribution, given by Eqn. (2.42), which assumes that n is constant in the normal direction, we have:

$$\int_0^{U_s} n dU = n \int_0^{U_s} dU = n_i e^{U_f (n^2 + n/a - U_g)} \quad (A.4)$$

which gives further evidence that the model distribution is an appropriate representation of the actual distribution.

To establish the relationship between the 'channel potential' ϕ and the surface potential U_s , we use the above invariant property of $\int n dU$ to match the general distribution, Eqn. (A.3), to that at the source or drain junction boundary given by the p-n junction Boltzmann relationship:

$$n = n_i e^{U - U_n} \quad (A.5)$$

where $U_n = U_d + U_f$ at the drain boundary.

Therefore,

$$\begin{aligned} \int_0^{U_s} n dU &= \int_0^{U_s} n_i e^{U - U_d - U_f} dU \\ &= n_i e^{U_s - U_d - U_f} \end{aligned} \quad (A.6)$$

Equating (A.6) with (A.3), we have:

$$n^2 + \frac{n}{a} - U_g = e^{U_s - U_d - 2U_f} \quad (A.7)$$

Another expression similar to Eqn. (A.7) can be obtained by first integrating the current density equation

$$J_n = -q D_n n \frac{dU}{dy} + q D_n \frac{dn}{dy}$$

in a direction normal to the surface to obtain I_d , expressing the result in terms of the variables used in the model, and then identifying the result in terms of the corresponding quantities in the drain current, Eqn. (2.12):

$$I_d = -Z D_n Q_m \frac{d\delta}{dy} \quad (2.12)$$

The result is the definition of the channel potential ,

$$d\delta = \left(\frac{2}{3} + \frac{X_s}{18X_i} \right) dU_s - d \log n.$$

This may be integrated and n substituted from Eqn. (2.41) to give [7]:

$$n^2 + \frac{n}{a} - U_g = e^{U_g - \eta/a - \delta} \cdot f(n) \quad (A.8)$$

Comparing Eqn. (A.8) with Eqn. (A.7), we see that:

$$f(n) = e^{-2U_f}$$

and $\delta = U_d$, the applied drain potential.

A similar result is obtained at the source junction where $\delta=0$ for a grounded source configuration.

APPENDIX BDMOS TRANSISTOR FABRICATION PROCEDURE

The following is an outline of the process steps used to fabricate DMOS transistors at Carleton University on 200 Ω -cm (100), p-type silicon substrates:

<u>Step</u>	<u>Operation</u>	<u>Mask Number</u>	<u>Parameters</u>
1	Oxidation		4Hrs. O ₂ , 1150°C, 1.5 μ m
2	Etch windows for channel contact diffusion	1	
3	Boron channel contact diffusion predeposition		60 min. B ₂ N ₃ , 900°C
4	Boron channel contact diffusion drive-in		5-10-10 O ₂ , 1175°C
5	Etch source windows	2	
6	Boron channel diffusion predeposition		60 min. B ₂ N ₃ , 900°C
7	Boron channel diffusion drive-in		2 min. O ₂ , 110 min. N ₂ , 1175°C
8	Etch drain windows	3	
9	Phosphorous predeposition		15 min. POCl ₃ , 975°C
10	Phosphorous drive-in		10-50-20 O ₂ , 1000°C
11	Etch gate areas	4	
12	Gate oxidation		110 min. O ₂ , 1000°C, 0.1 μ m
13	Contact window etch	5	
14	Metallization		Al
15	Metal pattern etch	6	
16	Sinter		30 min. N ₂ , 450°C

15:14 AUG 09, '80 ID=0800 ***** TERMINAL **

JOB , GREEN , 7,
ACCT LAST USED AUG 10 AT 14:55

60.51 RESOURCE UNITS REMAIN
LIMIT (TIME,2),(L0,200),(CCRE,16)
ASSIGN FILE,(FILE,DATAIN),(IN),(SAVE)
ASSIGN M1S1,(FILE,DMS),(IN),(SAVE)
FLAG LS,DB,M2,F1=105
* FLAG VERSION DD4

* AVAILABLE MEMORY:
* PROGRAM 6 INITIALIZED VARIABLES = 8195 (WORDS)
* NON-INITIALIZED VARIABLES = 2044 (WORDS)
* TOTAL = 10239 (WORDS)

0001	C	DMS TRANSISTOR MODEL CALCULATIONS	0001.000
0002		IMPLICIT REAL*8(A-Z)	0001.500
0003		INTEGER I,IC,IT,IY,IZ,ISW,IS,IG,ISAT,ISM,ICD,IB	0002.000
0004		COMMON YL,CX,EP,EPX,IOX	0002.500
0005		READ(105,1C0) Z,TEX,QSS,EM08	0003.000
0006		READ(105,1C0) YP,YL2,YL3,YD	0003.500
0007		READ(105,1C0) CYP,CBULK,EM08D,VDM	0004.000
0008		READ(105,1C0)VGM,VGMIN	0004.500
0009	100	FORMAT(4G,C)	0005.000
0010		WRITE(1C8,120)	0005.500
0011	120	FORMAT(1H1)	0006.000
0012		OUTPUT,INFLT DATA	0006.500
0013		OUTPUT,Z,TEX,QSS,EP08,YP,YL2,YL3,YD	0007.000
0014		OUTPUT,CYP,CBULK,EP08D,VDM,VGM,VGMIN	0007.500
0015		CI=1.45E1C	0008.000
0016		CGT=1.5E15	0008.500
0017		VT=25.5E=03	0009.000
0018		Q=1.602E=15	0009.500
0019		VSL=1.E7	0010.000
0020		EPS=11.7*8.86E=14	0010.500
0021		EP0X=3.5*8.86E=14	0011.000
0022		C0X=EP0X/TEX	0011.500
0023		CD=EPS/CSGRT(VT*EPS/(P*Q*CI))	0012.000
0024		UFP=CLCG(DABS(CYP)/CI)	0012.500
0025		UFGT=CLCG(CABS(CGT)/GT)	0013.000
0026		UFR=DLGG(CABS(CBULK)/CI)	0013.500
0027		AS=C0X*DEXPX=UFP/2.1/CD	0014.000
0028		AGT=C0X*DEXPX=UFGT/2.1/CD	0014.500
0029		AD=C0X*DEXPX=UFR/2.1/CD	0015.000

0030	EM082=(EMCB+EM08D)/2.	0015.200
0031	DN=EMCB*VT	0015.500
0032	DN2=EMCB2*VT	0015.600
0033	DND=EMCB0*VT	0015.700
0034	EC=VSL/DN	0016.000
0035	EC2=VSL/DN2	0016.100
0036	ECD=VSL/DNC	0016.200
0037	UGFBS=C.6/VT + UFP + Q*QSS/(CBX*VT)	0016.500
0038	UGFBGT=UGFBS=UFP+UFGT	0017.000
0039	UGFBD=UGFBS=UFP+UFB	0017.500
0040	UGMIN=VGMIN/VT	0018.000
0041	UGS=UGFBS+UGMIN	0018.500
0042	UGGT=UGFBGT+UGMIN	0019.000
0043	UGD=UGFBD+UGMIN	0019.500
0044	UGM=UGFBS+VGM/VT	0020.000
0045	VG=VGMIN	0020.500
0046	VO=0.	0021.000
0047	UDM=VCP/VT	0021.500
0048	DUG=.5/VT	0022.000
0049	UD=0.	0022.500
0050	USR=0.	0023.000
0051	IDM=0.	0023.500
0052	YL1=2.*YP	0024.000
0053	L1=YL1	0024.500
0054	L2=YL2=YL1	0025.000
0055	L3=YL3=YL2	0025.500
0056	L4=YD=YL3	0026.000
0057	IF(L4*LT.TEX)GO TO 130	0026.500
0058	YL4=3.*TEX*(1.-TEX/L4)+YL3	0027.000
0059	UG4=UGFBD+UGMIN*TEX/L4	0027.500
0060	GO TO 135	0028.000
0061	YL4=YL3	0028.500
0062	UG4=UGD	0029.000
0063	CL4=1.0	0029.500
0064	L4A=YL4=YL3	0030.000
0065	L4B=YD=YL4	0030.500
0066	A1=AS	0031.000
0067	A2=AO	0031.500
0068	A1S=A1*A1	0032.000
0069	A2S=A2*A2	0032.500
0070	K1=(UFP=UFB)/L2	0033.000
0071	YGT=YL1+(UFP=UFGT)/K1	0033.500
0072	KM=DLCG(EMCB0/EMCB)/L2	0033.700

0073	B=Z*VT*CEX			0034.000
0074	B1=B*CN/A15			0034.500
0075	B3=B*CN/A25			0035.000
0076	B4=B3			0035.500
0077	ALPHA=10.			0036.000
0078	IF(LA.LI.TEX)GO TO 140			0036.500
0079	CL4=1.+ALPHA*TX/L4B			0037.000
0080	CL3=1.+ALPHA*TX/L3	140		0037.500
0081	CL1=1.+ALPHA*UFB*TX/(L1*UFP)			0038.000
0082	WRITE(108,150)			0038.500
0083	FORMAT(140)	150		0039.000
0084	OUTPUT,CALCULATED VALUES			0039.500
0085	OUTPUT,K1,CBX,CD,UFP,UFB,AS,AD			0040.000
0086	OUTPUT,LGFES,UGFBD,L1,L2,L3,L4			0040.500
0087	OUTPUT,EC,YL4,UGFBGT,YGT,AGT,EMAB2,KH			0041.000
0088	WRITE(108,120)			0041.500
0089	ZETD=LC			0042.000
0090	OUTPUT,YG,LGS,UGC,YD,ZETD,UG4			0042.500
0091	OUTPUT,CL1,CL3,CL4			0043.000
0092	C			0043.500
0093	200 CALL SOLVE(UGD,AC,UFB,ZETD,ET3,R3,QM3,US3,XS3)			0044.000
0094	IT=0			0044.500
0095	I2=0			0045.000
0096	ISAT=C			0045.500
0097	IDMIN=0.			0046.000
0098	ZETDP=C.			0046.500
0099	ZET4=ZETD			0047.000
0100	ZET3=ZETD			0047.500
0101	ISM=C			0048.000
0102	Z1MIN=C.			0048.500
0103	Z2MIN=C.			0049.000
0104	ZETMIN=C.			0049.500
0105	Z3MIN=C.			0050.000
0106	Z4MIN=C.			0050.500
0107	CALL SOLVE(UGS,AS,UFP,USR,ETS,RS,QMS,USS,XSS)			0051.000
0108	ET1=ETS			0051.500
0109	R1=RS			0052.000
0110	QM1=QMS			0052.500
0111	US1=LSS			0053.000
0112	XS1=XSS			0053.500
0113	ZET1=LGR			0054.000
0114	ZET2=LGR			0054.500
0115	CALL FLUM(LGS,AS,USM1)			0055.000

0116	CALL FUSH(LGGT,AGT,USMGT)	0055.500
0117	CALL FUSH(LGD,AD,USM2)	0056.000
0118	KSA=ILSFGT=USM1/(YGT-YL1)	0056.500
0119	KSB=(LSM2=LSMGT)/(YL2-YGT)	0057.000
0120	IF(L1A.LT.TOX)GO TO 202	0057.500
0121	CALL FLEM(LG4,AD,USM4)	0058.000
0122	KSC=(LSM2=LSM4)/L4A	0058.500
0123	K4=(UGD=UG4)/L4A	0059.000
0124	GO TO 203	0059.500
0125	USM4=LSM2	0060.000
0126	KSC=0.	0060.500
0127	K4=0.	0061.000
0128	203	0061.500
0129	OUTPUT,KSA,KSB,USM1,USMGT,USM2,USM4,K4,KSC	0062.000
0130	WRITE(108,150)	0062.500
0131	ZETI,ZET2	0063.000
0132	USMA=LSM1=UGS*VT	0063.500
0133	USMB=LSM2=UGD*VT	0064.000
0134	USMC=LSM4=UG4*VT	0064.500
0135	UST1=LSB+(LSM1=USS)/CI.1	0065.000
0136	OUTPUT,LST1,USMA,USMB,USMC	0065.500
0137	C *****	0066.000
0138	205	0066.500
0139	CALL SELVE(UG4,AD,UFB,ZETD,ETO,RD,QMD,USD,XSD)	0067.000
0140	DZTP=C.	0067.500
0141	DZTPP=0.	0068.000
0142	DZ1P=C.	0068.500
0143	DZ1PP=C.	0069.000
0144	DZ2P=C.	0069.500
0145	DZ2PP=C.	0070.000
0146	SZ1=0.	0070.500
0147	SZ2=0.	0071.000
0148	IS=0	0071.500
0149	IG=0	0072.000
0150	ICD=0	0072.500
0151	C	0073.000
0152	TO OBTAIN THE MAXIMUM CURRENT WHICH COULD FLOW	0073.500
0153	C	0074.000
0154	ID1 IS CALCULATED WITH ZET1=ZETD YIELDING IDM	0074.500
0155	CALL SELVE(UGS,AS,UFP,ZETD,ETAN,RIM,QM1M,USIM,XSIM)	0075.000
0156	IF(USIM*GT.UST1)ISY=1	0075.500
0157	ID1M=81*(RIM=RS)/(L1+(USIM=USS)/EC)	0076.000
0158	IF(ID1P*LE.IDM*AND.ZETD.GT.1.E=3)ISAT=1	0076.500
	IDM=ID1P	

0159		IF(I2.EG.0)GO TO 207	0077.000
0160		IF(IDMIN.GT.(L1>IDM/YD))GO TO 207	0077.500
0161		IDMIN=L1*ICH/YD	0078.000
0162	207	IF(DABS(QM1M).GT.DABS(QMD))IDMIN=IDMIN*QMD/QM1M	0078.500
0163		IF(ISM.EQ.1)GO TO 300	0079.000
0164	208	ISM=0	0079.500
0165		OUTPUT,IDM,IDMIN	0080.000
0166		IF(IDM.LT.1.E=9.AND.IRAT.EQ.1)GO TO 1100	0080.500
0167		WRITE(108,350)	0081.000
0168	350	FORMAT(1H0,2X,2HIT,4X,4HIDAV,11X,3HID1,10X,3HID2,	0081.500
0169		1 11X,3HID3,10X,4HZET1,7X,4HZET2,7X,4HZET3)	0082.000
0170	C		0082.500
0171	C	***** START OF ITERATION LOOP *****	0083.000
0172	C		0083.500
0173	C	SOLVING FOR ID2 (GRADED REGION)	0084.000
0174	210	I=0	0084.500
0175		ISW=0	0085.000
0176		LI=0.	0085.500
0177		LT2=0.	0086.000
0178		ZTMIN=ZET1	0086.500
0179		ZTMAX=ZET2	0087.000
0180		CALL SOLVE(UGD,AD,UFB,ZET2,ET2,R2,QM2,US2,XS2)	0087.500
0181		GAM2=EMCBC*QM2	0087.700
0182		IF(I2.GT.C.AND.US3.GT.US13)GO TO 212	0088.000
0183		UST3=LS2+(USMB=US2)/CL3	0088.500
0184	212	CALL SOLVE(UGS,AS,UFP,ZFT1,ET1,R1,QM1,US1,XS1)	0089.000
0185		GAM1=EMCBB*GM1	0089.200
0186		ID1=RI*(R1=RS)/(L1+(US1=USS)/EC)	0089.500
0187		QT1=QM1	0090.000
0188		QT2=QM2	0090.500
0189	C		0091.000
0190		IF(US1.GT.L6T1)GO TO 300	0091.500
0191		F1=ET1+2.*AS+1./AS+(1.=UGS)/ET1	0091.600
0192		ES1=(RS=R1)/(AS*F1+L1)	0091.700
0193		IF(US1.GE.(ZET1+2.*UFP))GO TO 217	0092.000
0194	214	IF(US2.GE.(ZET2+2.*UFB))GO TO 230	0092.500
0195	215	ZETT=ZET2	0093.000
0196		YT=YL2	0093.500
0197		UST=US2	0094.000
0198		ETAT=ET2	0094.500
0199		UFT=UFB	0094.700
0200		QMT=QM2	0095.000
0201		XST=XS2	0095.500

0202	LT1=L2		0096.000
0203	IF(US2.LE.(LST3)GO TO 220		0096.500
0204	ISM=2		0097.000
0205	GO TO 397		0097.500
0206	217 IF(US2.LT.(ZET2+2.*UFR))GO TO 225		0098.000
0207	218 ZET1=ZET1		0098.500
0208	YT=YL1		0099.000
0209	UST=US1		0099.500
0210	ETAT=ET1		0100.000
0211	UFT=UFP		0100.100
0212	QMT=QM1		0100.500
0213	XST=XS1		0101.000
0214	LT2=L2		0101.500
0215	220 KT=DLOG(QM2/QM1)/L2		0102.000
0216	KQ=KI+KM		0102.200
0217	IF(DABS(KG).LT.1.)GO TO 285		0102.500
0218	KG=KG+L2/(L2+(ZET2-ZET1)/EC2)		0102.700
0219	QT1=(QM2-QM1)/(KI+L2)		0103.000
0220	QT2=CT1		0103.500
0221	ID2=-Z*VT*GAM2*KG*(ZET2-ZET1)/(GAM2/GAM1-1.)		0104.000
0222	GO TO 250		0104.500
0223	C		0105.000
0224	225 ISW=1		0105.500
0225	YT=YL1+(US1-USMA+ZETT-ZET1)/(KI+KSA)		0106.000
0226	IF(YT.GT.YGT+YT*(KSB*YL2+KI*YL1+US1-USMB+ZETT-ZET1)/(KI+KSB)		0106.500
0227	GO TO 235		0107.000
0228	230 YT=(KSA*YL1+KI*YL2+US2-USMA+ZETT-ZET2)/(KI+KSA)		0107.500
0229	IF(YT.GT.YGT)YT=YL2=(USMB-US2+ZETT-ZET1)/(KI+KSB)		0108.000
0230	235 LT1=Y1-YL1		0108.500
0231	LT2=YL2-Y1		0109.000
0232	IF(LT1.LT.1.E=6)GO TO 218		0109.500
0233	IF(US2.GT.LSMB.AND.ISW.EQ.0)GO TO 215		0110.000
0234	UFT=UFP-KI*LT1		0110.500
0235	UGT=UGS-KI*LT1		0111.000
0236	AT=AS+DEXP(KI*LT1/2.)		0111.500
0237	CALL SELVE(UGT,AT,UFT,ZETT,ETAT,RT,QMT,UST,XST)		0112.000
0238	KT1=DLOG(GMT/QM1)/LT1		0112.500
0239	KGI=KI1+KM		0112.700
0240	GAMT=EXP(CB*DEXP(KM*LT1))*QMT		0112.800
0241	IF(DABS(KGI).LT.1.)GO TO 270		0113.000
0242	KGI=KGI*LT1/(LT1+(ZETT-ZET1)/ECP)		0113.200
0243	QT1=(GMT-QM1)/(KI1+LT1)		0113.500
0244	IDT1=-Z*VT*GAMT*KGI*(ZETT-ZET1)/(GAMT/GAM1-1.)		0114.000

0245	240	IF (ISH.EG.C) GO TO 242	0114.500
0246		IDT2=IDT1	0115.000
0247		GO TO 245	0115.500
0248	242	KT2=CLEG(GM2/QMT1)/LT2	0116.000
0249		KG2=KT2+KM	0116.200
0250		IF (DARS(KG2).LT.1.1) GO TO 280	0116.500
0251		KG2=KG2+LT2/(LT2+(ZET2-ZETT)/EC2)	0116.700
0252		QT2=(GM2-QMT1)/(KT2+LT2)	0117.000
0253		IDT2=-2*VT+GAM2+KG2*(ZET2-ZETT)/(GAM2/QMT1-1.1)	0117.500
0254	245	ID2=(IDT1+IDT2)/2.	0118.000
0255		IF (ID2.LT.C.1) GO TO 248	0118.500
0256		IF (J.LE.15) GO TO 247	0119.000
0257		WRITE(108,246) 1,ZETT,IDT1,IDT2,VT	0119.500
0258	246	FORMAT(6X,3H1=12,2X,6HZETT=,F10.5,2X,6HIDT1=,1P612.4,2X,	0120.000
0259		1 6HIDT2=,1P612.4,2X,4HYT=,1P612.4)	0120.500
0260	247	CONTINUE	0121.000
0261		IF (ZETC.LT.1.E-10) GO TO 290	0121.500
0262		IF ((ZET2-ZETT).LT.1.E-10) GO TO 320	0122.000
0263		IF (ID2.LT.1.E-9) GO TO 320	0122.500
0264		I=I+1	0123.000
0265		IF (J.LE.30) GO TO 250	0123.500
0266		IF (IT.EG.C) GO TO 290	0124.000
0267	248	WRITE(108,150)	0124.500
0268		OUTPUT GRACED REGION DID NOT CONVERGE+	0125.000
0269		OUTPUT,1,VT,US1,UST,US2,ID2	0125.500
0270		OUTPUT,ZET1,ZETT,ZET2,QM1,QMT,QM2,IDT1,IDT2	0126.000
0271		OUTPUT,GAM1,GAMT,GAM2,KG1,KG2	0126.200
0272		GO TO 476	0126.500
0273	C		0127.000
0274	250	IDT1=IDT1-ID2	0127.500
0275		IDT2=IDT2-ID2	0128.000
0276		ERR1=CABS(CIDT1/ID2)	0128.500
0277		ERR2=CABS(CIDT2/ID2)	0129.000
0278		EMAX=5.E-3	0129.400
0279		IF (ERR1.LT.EMAX.AND.ERR2.LT.EMAX) GO TO 290	0129.500
0280		IF (IDT1.GT.IDT2) GO TO 255	0130.000
0281		DZT=(ZET2-ZETT)*(IDT2/IDT1)	0130.500
0282		GO TO 260	0131.000
0283	255	DZT=(ZET1-ZETT)*(CIDT1/IDT1)	0131.500
0284	260	IF ((DZT+DZTP).GE.0.AND.(DZT+DZTPP).GE.0.) DZT=DZT+DZTP/2.	0132.000
0285		IF ((ZETT+CZT).GT.ZTMAX) DZT=(ZTMAX-ZETT)/2.	0132.500
0286		IF ((ZETT+CZT).LT.ZTMIN) DZT=(ZTMIN-ZETT)/2.	0133.000
0287		IF (DZT+DZTP).GE.0.) GO TO 265	0133.500

0288		IF(DABS(CZ1),GT,CABS(DZTP/2,1)DZ1=DZTP/2.	0134.000
0289	265	ERRZ=CABS(CZT/ZET1)	0134.500
0290		IF(ERRZ,LI,X,E=6)GO TO 290	0135.000
0291		DZTP=CZTP	0135.500
0292		DZTP=CZ1	0136.000
0293		IF(DZ1,LI,C,1)ZIMAX=ZET1	0136.500
0294		IF(DZ1,GT,C,1)ZIMIN=ZET1	0137.000
0295		ZET1=ZET1+CZ1	0137.500
0296		IF(JSA,EC,1)GO TO 225	0138.000
0297		GO TO 230	0138.500
0298	C		0139.000
0299	270	Q1=QM1	0139.500
0300		DUS=ZET1-ZET1	0140.000
0301		IDT1=-2*VT*GAM1*DUS/(LT1+DUS/EC2)	0140.500
0302		GO TO 240	0141.000
0303	280	Q2=QM2	0141.500
0304		DUS=ZET2-ZET1	0142.000
0305		IDT2=-2*VT*GAM2*DUS/(LT2+DUS/EC2)	0142.500
0306		GO TO 245	0143.000
0307	285	ID2=-2*VT*GAM2*(ZET2-ZET1)/(LT2+ZET2-ZET1)/EC2)	0143.500
0308	C		0144.000
0309	290	IG=IG+1	0144.500
0310		IF(IT,GT,0)GO TO 320	0145.000
0311		IF(IJ,GT,0)GO TO 320	0145.500
0312		LQ1=L1/GM1	0146.000
0313		LQ1=L1/GT1	0146.500
0314		LQ2=L1/GT2	0147.000
0315		LQ3=L3/GM2	0147.500
0316		IF(L4,LT,1)EX)GO TO 294	0148.000
0317		K14=DLEGICP3/QMD)/L4A	0148.500
0318		IF(DABS(K14),LT,1)GO TO 294	0149.000
0319		LQ4A=L4A+L4A*K14/(CMD-QM3)	0149.500
0320	292	LQ4B=L4B/CMD	0150.000
0321		LQ1=LQ1+LQ1+LQ2+LQ3+LQ4A+LQ4B	0150.500
0322		GO TO 320	0151.000
0323	294	LQ4A=L4A/CMD	0151.500
0324		GO TO 292	0152.000
0325	C		0152.500
0326	C	REGION 1 SATURATED	0153.000
0327	300	CALL FX(UST1,AS,UGS,ETT1,RT1,FT1,X11,AX1)	0153.500
0328		ID11=-(RT1-R8)	0154.000
0329		I11=BI+ID11/(LI1+(UST1-USS1)/EC)	0154.500
0330		ES11=IC11/(AS+FT1+LI1)	0155.000

0331	IF(ISP.EC.1)GO TO 315	0155.500
0332	DUS=ZET1-(LST1-USS)	0156.000
0333	SA=AX1+DUS/ES11	0156.500
0334	SQR=DSGR+SA*SA+1.	0157.000
0335	ID1=I11+(SGR+SA)*((1./(L1*AX1))	0157.500
0336	LS1=I11+L1/ID1	0158.000
0337	ESD1=ES11+EQR	0158.500
0338	VS=DN+ESD1	0159.000
0339	VSD1=VS/(1.+VS/VSL)	0159.500
0340	QM1=IC1/(2+VSD1)	0160.000
0341	GAM1=EPCB+CM1	0160.200
0342	US1=US11+DLS	0160.500
0343	XS1=X11	0161.000
0344	ET1=AS+(UGS=US1)	0161.500
0345	GO TO 214	0162.000
0346	C	0162.500
0347	DUS=ZETC-(LST1-USS)	0163.000
0348	SA=AX1+DLS/ES11	0163.500
0349	IDM=I11*(DEORT(SA*SA+1.)+SA)*((1./(L1*AX1))	0164.000
0350	GO TO 208	0164.500
0351	C	0165.000
0352	C SOLVING REGIONS 3 AND 4 FOR ZET3	0165.500
0353	I=0	0166.000
0354	CALL RX(US13,AD,UGD,ET13,RT3,FI3,XI3,AX3)	0166.500
0355	DZ3P=C.	0167.000
0356	DZ4P=C.	0167.500
0357	DZ4PP=C.	0168.000
0358	Z4MAX=ZETC	0168.500
0359	I=I+1	0169.000
0360	Z4MIN=ZET3	0169.500
0361	ISW=0	0170.000
0362	IB=0	0170.500
0363	IF(US2.GT.LST3)GO TO 395	0171.000
0364	CALL SOLVE(UGD,AC,UFB,ZET3,ET3,R3,GM3,US3,XS3)	0171.500
0365	CALL SOLVE(UG4,AC,UFB,ZET4,ET4,R4,GM4,US4,XS4)	0172.000
0366	IF(US3.GT.LST3)GO TO 370	0172.500
0367	ID3=B3+(R3-R2)/(L3+(US3-US2)/ECD)	0173.000
0368	F3=ET3+2.*AD+1./AD+(1.-UGD)/ET3	0173.500
0369	ES3=(R2-R3)/(AD*F3*L3)	0173.600
0370	IF(L4.LT.TCX)GO TO 400	0174.000
0371	USTA=L84+(LSMC-US4)/CL4	0174.500
0372	IF(US4.GT.LST4)GO TO 380	0175.000
0373	IF(USC.GT.LST4)GO TO 332	0175.500

0374	IDAB=B4*(RD=R4)/(LAB+(USD=US4)/ECD)	0176.000
0375	GO TO 3320	0176.500
0376	C	0177.000
0377	C REGION AB SATURATED	0177.500
0378	332 CALL RX(UST4,AD,UGFBD,ETT4,RT4,FT4,X14,AX4)	0178.000
0379	ID14=(RT4=R4)	0178.500
0380	I14=B4*IC14/(LAB+(UST4=US4)/ECD)	0179.000
0381	ES14=IC14/(AD*FT4*LAB)	0179.500
0382	DUS=ZETD-ZET4=(UST4=US4)	0180.000
0383	SA=AX4+CUS/ES14	0180.500
0384	SQR=DSQRT(SA*SA+1.)	0181.000
0385	IDAB=I14*(SQR+SA)**(1./(LAB*AX4))	0181.500
0386	LS4=I14*LAB/ID4	0182.000
0387	ESD=ES14*SQR	0182.500
0388	VS=DNC*ESC	0183.000
0389	VSD=VS/I1.*VS/VSL)	0183.500
0390	QMD=-IC4B/(Z*VSD)	0184.000
0391	USD=UST4+DLS	0184.500
0392	XSD=X14	0185.000
0393	IS=IS4	0185.500
0394	KT4=CLCG(QM3/QM4)/(LAB+(ZET4=ZET3)/ECD)	0186.000
0395	IF(DABS(KT4).LT.1.)GO TO 333	0186.500
0396	ID4A=-Z*DNC*QM3*KT4*(ZET4=ZET3)/(QM3/QM4=1.)	0187.000
0397	GO TO 334	0187.500
0398	ID4A=-Z*DNC*QM3*(ZET4=ZET3)/(LAB+(ZET4=ZET3)/ECD)	0188.000
0399	ID4=(ID4A+ID4B)/2.	0188.500
0400	DIDA=ID4-IC4A	0189.000
0401	DIDB=ID4-IC4B	0189.500
0402	IF(ID4.LT.1.E-9)GO TO 335	0190.000
0403	ERRA=CABS(CIDA/ID4)	0190.500
0404	ERRB=CABS(CIDB/ID4)	0191.000
0405	IF(ERRA.LT.1.E-3.AND.FRRB.LT.1.E-3)GO TO 335	0191.500
0406	DZ4=(ZET4=ZET3)*(DIDA/ID4A)	0192.000
0407	IF(ID4B.GT.ID4A)DZ4=(ZET4=ZETD)*(DIDB/ID4B)	0192.500
0408	IF(DZ4.LT.C.)Z4MAX=ZET4	0193.000
0409	IF(DZ4.GT.C.)Z4MIN=ZET4	0193.500
0410	IF(1B.GT.5)DZ4=(Z4MIN+Z4MAX)/2.*ZET4	0194.000
0411	IF(1B.LI.15)GO TO 387	0194.500
0412	WRITE(1C8,3340)1B,ZET4,1D4A,1D4B,QM3,QM4	0195.000
0413	FORMAT(1C8,4HIB,12,2X,6HZET4,10,5,2X,6HID4A,1,	0195.500
0414	1PG12,4,2X,6HID4B,1PG12,4,2X,5HQM3,1PG12,4,2X,	0196.000
0415	1 5HQM4,1PG12,4)	0196.500
0416		0197.000

0417		G0 T0 387		0197.500
0418	C			0198.000
0419	C			0198.500
0420	335	IAY=(ID3+IC4)/2.		0199.000
0421		DID3=IAY-IC3		0199.500
0422		DID4=IAY-IC4		0200.000
0423		IF((ZETC-ZET2).LT.1.E-6)G0 T0 400		0200.500
0424		IF(ID3.LT.1.E-9.ANC.ID4.LT.1.E-9)G0 T0 400		0201.000
0425		ERR3=CABS(CID3/IAY)		0201.500
0426		ERR4=CABS(CID4/IAY)		0202.000
0427		IF(ERR3.LT.1.E-3.AND.ERR4.LT.1.E-3)G0 T0 400		0202.500
0428		IF(ID4.GT.ID3)G0 T0 340		0203.000
0429		DZ3=(ZET3-ZET2)*(DID3/ID3)		0203.500
0430		G0 T0 360		0204.000
0431	340	DZ3=(ZETD-ZET3)*(CID4/ID4)		0204.500
0432	360	IF((DZ3+DZ3P).GT.0.1)G0 T0 365		0205.000
0433		DZ3=DZ3/4.		0205.500
0434	365	IF((ZET3+DZ3).LT.ZET2)DZ3=(ZET2-ZET3)/2.		0206.000
0435		IF((ZET3+DZ3).GT.ZETD)DZ3=(ZETD-ZET3)/2.		0206.500
0436		IF(DABS(DZ3).GE.CABS(DZ3P))DZ3=DZ3/2.		0207.000
0437		DZ3P=DZ3		0207.500
0438		ZET4=ZET4+DZ3*(ZETD-ZET4)/(ZETD-ZET3)		0208.000
0439		ID3=IAY		0208.500
0440		ZET3=ZET3+DZ3		0209.000
0441		IF(IAY.LT.IDMIN.ANC.I.GT.10)G0 T0 400		0209.500
0442		IF(I.LT.2C)G0 T0 330		0210.000
0443		WRITE(1,1C8,367)I,ZET3,ID3,ID4,QM3		0210.500
0444	367	FORMAT(6X,3H =,12,2X,6HZET3 =,F10.5,2X,5HID3 =,		0211.000
0445	1	1PG12.4,2X,5HID4 =,1PG12.4,2X,5HQM3 =,1PG12.4)		0211.500
0446	368	IF(I.LE.3C)G0 T0 330		0212.000
0447		OUTPUT,ZET3 DID NOT CONVERGE!		0212.500
0448		OUTPUT,ZET2,ZET3,IC3,ID4,GD3,GD4		0213.000
0449		OUTPUT,LS2,UST3,US3,US4,UST4		0213.500
0450		OUTPUT,ESD3,ESD,VSD3,VSD,QM3,QMD		0214.000
0451		OUTPUT,GM4,DUS,USD,ZET4,YT4		0214.500
0452		G0 T0 1500		0215.000
0453	C			0215.500
0454	C	REGION 3 IS SATURATED		0216.000
0455	370	ID13=(16I3.R2)		0216.500
0456		I13=83+ID13/(13+(UST3-US2)/ECD)		0217.000
0457		ES13=IC13/(AD*FT3*13)		0217.500
0458		DUS=ZET3-ZET2-(UST3-US2)		0218.000
0459		US3=UST3+DL9		0218.500

0460			XS3=X13		0219,000
0461			SA=AX3+CUS/ES13		0219,500
0462			SQR=DEGRT(EA*SA+1.)		0220,000
0463			ID3=I13+(SCR+SA)**(1./(L3*AX3))		0220,500
0464			LS3=I13+L3/ID3		0221,000
0465			FSD3=ES13*EQR		0221,500
0466	375		VS=DNC+ESD3		0222,000
0467			VSD3=V6/(1.+VS/VSL)		0222,500
0468			QM3=-IC3/17+VSD3		0223,000
0469			IF(14.LT.VEX)GO TO 400		0223,500
0470			GO TO 350		0224,000
0471	C				0224,500
0472	C	REGION 48 CEPLETED			0225,000
0473	380		IB=IB+1		0225,500
0474			DUS=ZE14-ZET3		0226,000
0475			ISW=0		0226,500
0476			YT4=YL3+(UEMB-US3-DUS)/KSC		0227,000
0477			IF(Y14.GT.YL4)YT4=YL4		0227,500
0478			IF(Y14.GT.YL3)GO TO 382		0228,000
0479			ZET4=ZET3+CUS/2.		0228,500
0480			GO TO 380		0229,000
0481	382		UGT4=LGC-K4*(YT4=YL3)		0229,500
0482			CALL SELVE(UGT4,AD,UFR,ZET4,ET4,R4,QM4,US4,XS4)		0230,000
0483			KT4=DLEG(GM3/QM4)/(YT4=YL3+DUS/ECD)		0230,500
0484			IF(DABS(KT4).LT.1.)GO TO 384		0231,000
0485			ID4=-2*CNC+QM3*KT4*DUS/(QM3/QM4=1.)		0231,500
0486			GO TO 386		0232,000
0487	384		ID4=-2*CNC+QM3*DUS/(YT4=YL3+DUS/ECD)		0232,500
0488	386		EST4=-IC4/(Z*DND*QM4)		0233,000
0489			AX4=DSGRT(1./(10X*XS4))		0233,500
0490			DUS=ZETC-ZET4		0234,000
0491			SA=AX4+CUS/EST4		0234,500
0492			L4D=YC-Y14		0235,000
0493			SQR=DSGRT(SA*SA+1.)		0235,500
0494			ESD=EST4*ECR		0236,000
0495			DZ4=DLS-(EST4+ESD)*L4D/2.		0236,500
0496			IF(DABS(DZ4).LT.1.E=3)GO TO 335		0237,000
0497			IF(18.LT.15)GO TO 387		0237,500
0498			WRITE(108,386D)18,ZET4,ID4,YT4,QM3,QM4		0238,000
0499	3860		FORMAT(6X,4H18=,12,2X,6HZET4=,F10.5,3X,5HID4=,		0238,500
0500		1	1PG12.4,3X,5HYT4=,1PG12.4,2X,5HQM3=,1PG12.4,2X,5HQM4=,1PG12.4)		0239,000
0501	387		IF(1DZ4*DZ4P).GT.0.)GO TO 388		0239,500
0502			DZ4=DZ4/4,		0240,000

0503	IF((DZ4+CZ4PP)*LT.C)GO TO 388	0240.500
0504	DZ4=DZ4/2.	0241.000
0505	388 IF((ZET4+CZ4)*LT.(ZET4+ZET3)/2.)DZ4=(ZET3-ZET4)/2.	0241.500
0506	IF((ZET4+DZ4)*GT.(ZET4+ZET0)/2.)DZ4=(ZET0-ZET4)/2.	0242.000
0507	IF(0ABS(DZ4)*GE.DABS(DZ4P))DZ4=DZ4/2.	0242.500
0508	ZET4=ZET4+CZ4	0243.000
0509	DZ4P=CZ4	0243.500
0510	DZ4PP=CZ4P	0244.000
0511	IF((18*GE+2C)GO TO 389	0244.500
0512	IF(18*EG+1)GO TO 331	0245.000
0513	GO TO 380	0245.500
0514	389 IF((ID4*LT.IDMIN)GO TO 335	0246.000
0515	IF((IT*EG+0)GO TO 335	0246.500
0516	OUTPUT,ZET4 DID NOT CONVERGE!	0247.000
0517	OUTPUT,ZET3,ZET4,QM3,QM4,EST4,ESD,ID4,YT4	0247.500
0518	OUTPUT,KT4,K4,KSC,YL3,YL4,US4,D74	0248.000
0519	GO TO 1100	0248.500
0520	C	0249.000
0521	C REGION 4 DEPLETED	0249.500
0522	390 DUS=ZETC-ZET3	0250.000
0523	XS4=XS3	0250.500
0524	XSD=XS3	0251.000
0525	GD3=IC3/(VT*L3*ESD3)	0251.500
0526	ID4=ID3	0252.000
0527	SB=6*(G*CEULK+ID4/(XS3*Z*VSL))/(VT*EPS)	0252.500
0528	SC=6*(IC4+L4/(VT*VT*EPS*XS3*EMORD*Z))+ESD3*ESD3	0253.000
0529	SGR=DSCRT(SB*DUS*SC)	0253.500
0530	GD4=IC4/(VT*L4*SGR)	0254.000
0531	QM4=IC4*(1./VSL+L4/(DND*DUS))/Z	0254.500
0532	ESD=SGR	0255.000
0533	VS=ESC*CND	0255.500
0534	VSD=VS/(1.+VS/VSL)	0256.000
0535	QMD=IC4/(Z*VSD)	0256.500
0536	US4=US3	0257.000
0537	USD=US4+DUS	0257.500
0538	DZ3=QLS=(ESD3+ESD)*L4/2.	0258.000
0539	IF(DZ3*LT.(1.E-3)GO TO 400	0258.500
0540	IF((IT*EG+0)GO TO 400	0259.000
0541	GO TO 360	0259.500
0542	C	0260.000
0543	C REGIONS 3 AND 4 DEPLETED	0260.500
0544	395 IF(US1*GT.LST1)GO TO 397	0261.000
0545	EST2=-IC2/(Z*QMT*DND)	0261.500

0546	DUS=ZET3-ZET1	0262.000
0547	AXT=DEGRT(1./(10X*YST))	0262.500
0548	SA=AXI*DU5/EST2	0263.000
0549	SQR=DSGRT(SA*SA+1.)	0263.500
0550	ESD3=EST2*EQR	0264.000
0551	LEQ=YL3-YL1	0264.500
0552	I2EQ=IC2+LT1/LEQ	0265.000
0553	ID3=I2EC+(SQR+SA)**(1./(LEQ*AX1))	0265.500
0554	US3=UET+DUE	0266.000
0555	XS3=XET	0266.500
0556	LS3=0.	0267.000
0557	GO TO 375	0267.500
0558	C	0268.000
0559	C	0268.500
0560	397 REGIONS 2,3 AND 4 DEPLETED	0269.000
0561	DUS=ZET3-ILST1-USS1	0269.500
0562	SA=AX1+CUB/ES11	0270.000
0563	SQR=DSGRT(SA*SA+1.)	0270.500
0564	ESD3=ES11+EQR	0271.000
0565	LEQ=YL3	0271.500
0566	ID2=I11*(SQR+SA)**(1./(LEQ*AX1))	0272.000
0567	ID3=IC2	0272.500
0568	ID1=IC2	0273.000
0569	US3=UST1+DL8	0273.500
0570	XS3=XE1	0274.000
0571	LS3=0.	0274.500
0572	IF(ID3.LT.IDMIN)GO TO 398	0275.000
0573	GO TO 375	0275.500
0574	C	0276.000
0575	398 ISM=2	0276.500
0576	DZ1=(Z1PIN-ZET1)/4.	0277.000
0577	DZ2=(Z2PIN-ZET2)/4.	0277.500
0578	II=II+1	0278.000
0579	WRITE(I08,450)IT,IDA V, ID1, ID2, ID3, ZET1, ZET2, ZET3	0278.500
0580	IF(II.LE.5C)GO TO 855	0279.000
0581	GO TO 475	0279.500
0582	C	0280.000
0583	C	0280.500
0584	400 IT=II+1	0281.000
0585	ICD=ICD+1	0281.500
0586	IDA V=(IC1+ID2+ID3)/3.	0282.000
0587	IF(II.LE.5)GO TO 420	0282.500
0588	IF(ID1.LT.IDA V1) GO TO 410	0282.600

0589		IF(ID2,LT,IDAV1) GC TO 415	0282.610
0590		IF(ID3,GT,IDAV1) GC TO 420	0282.630
0591	410	IF(ID2,LT,IDAV1,ANC,ID3,LT,IDAV1)GC TO 420	0282.640
0592	415	CONTINUE	0282.650
0593		IDAV=(2.0*ICAV+IDAV1)/3.	0283.000
0594	420	IF(IDAV,LT,DMIN,IDAV=DMIN)	0283.500
0595		IF(IDAV,GT,DM,ICAV=DM	0284.000
0596		IF(IT,GT,1.0AND,IT,LT,20)GC TO 470	0284.500
0597		WRITE(1,8,450)IT,ICAV,DM,DM2,ZET1,ZET2,ZET3	0285.000
0598	450	FORMAT(2X,I3,4(1P)G12.4,2X),4(OPF10.5,1X)	0285.500
0599	470	CONTINUE	0286.000
0600		IF(ZETD,LT,1.0E-10)GC TO 920	0286.500
0601		IF(IDP,LT,1.0E-9)GC TO 920	0287.000
0602		IF(IT,LE,3C)GC TO 500	0287.500
0603	475	WRITE(1,8,150)	0288.000
0604		OUTPUT CID NOT CONVERGE	0288.500
0605		WRITE(1,8,450)IT,ICAV,DM,DM2,ZET1,ZET2,ZET3	0289.000
0606		OUTPUT,IT,LS1,US1,LS2,US2,US3,DM1,DM2,DM3	0289.500
0607	476	IF(VO,GT,(VG+3.0))GC TO 1100	0290.000
0608		IF(US2,LT,LS3)GC TO 900	0290.500
0609		GO TO 1100	0290.600
0610	C		0291.000
0611	C	TEST FOR CONVERGENCE	0291.500
0612	C		0292.000
0613	500	IC=0	0292.500
0614		EMAX=5.0E-3	0293.000
0615		IF(IDAV,LT,1.0E-4)EMAX=10.0E-3	0293.200
0616		IF(IDAV,LT,1.0E-6)EMAX=2.0E-2	0293.500
0617		ERR1=CABS((ID1-IDAV)/IDAV)	0294.500
0618		IF(ERR1,GT,EMAX)GC TO 600	0295.000
0619		IC=IC+1	0295.500
0620	600	ERR2=CABS((ID2-IDAV)/IDAV)	0296.000
0621		IF(ERR2,GT,EMAX)GC TO 700	0296.500
0622		IC=IC+1	0297.000
0623	700	ERR3=CABS((ID3-IDAV)/IDAV)	0297.500
0624		IF(ERR3,GT,EMAX)GC TO 720	0298.000
0625		IC=IC+1	0298.500
0626		IF(1.0E-3)GC TO 900	0299.000
0627		GO TO 800	0299.500
0628	720	IF(IC,LT,2)GC TO 800	0300.000
0629	C		0300.500
0630	C	ADJUST POTENTIAL DISTRIBUTION	0301.000
0631	C		0301.500

0632	800	DID1=IDAV-ID1	0302.000
0633		DID2=IDAV-ID2	0302.500
0634		DID3=IDAV-ID3	0303.000
0635		DZ2=0.	0303.500
0636		DZ1=0.	0304.000
0637		DZ11=ZET11+CID11/ID1	0304.500
0638		DZ12=(ZET12-ZET11)*DID2/ID2	0305.000
0639		DZ22=(ZET12-ZETD)*DID3/ID3	0305.200
0640		IF(DID1.LT.0.,AND,CID2.LT.0.)GO TO 875	0305.500
0641		IF(ID3.LT.(.5*IDAV))GO TO 880	0306.000
0642		DZ2=DZ22	0307.000
0643		IF(ID3.GT.ID2)GO TO 805	0307.500
0644		IF(ID212+DZ22).LE.C.,AND,DZ11.GT.0.)DZ2=DZ12+DZ22	0308.000
0645	805	IF(DZ2.GT.(ZETD-ZET2)/2.)DZ2=(ZETD-ZET2)/2.	0308.500
0646		IF(ID2.LT.(.5*IDAV))GO TO 890	0309.500
0647		DZ1=-DZ12	0310.000
0648		IF(DZ1+DZ11).LE.0.)DZ1=DZ1+DZ11	0310.500
0649		IF(ERR3.LT.EMAX)DZ2=DZ22	0311.000
0650		IF(DIC2.LT.0.,AND,CID3.LT.0.)DZ1=DZ2-DZ12	0311.500
0651		IF(ERR1+ERR2).LT.C.02)DZ1=DZ1/2.	0312.000
0652	810	IF(ZET1+DZ1).LT.Z1MIN)DZ1=(Z1MIN-ZET1)/2.	0312.500
0653		IF(ZET2+DZ2).LT.Z2MIN)DZ2=(Z2MIN-ZET2)/2.	0312.700
0654		IF(ZET1+DZ1).GT.(ZET2+DZ2))DZ1=(ZET2-ZET1+DZ2)/2.	0313.000
0655			0313.500
0656	820	CONTINUE	0314.000
0657		IF(ERR1.GT.EMAX,OR,ERR3.GT.EMAX)GO TO 830	0314.500
0658		IF(ERR1.GT.ERR3)DZ1=2.*DZ1	0315.000
0659		IF(ERR3.GT.ERR1)DZ2=2.*DZ2	0315.500
0660	830	IF(DABS(DZ1).GT.2.*DABS(DZ1P))DZ1=DZ1/2.	0316.000
0661		IF(DABS(DZ2).GT.2.*DABS(DZ2P))DZ2=DZ2/2.	0316.500
0662		IF(IT.LE.3)GO TO 855	0316.700
0663		IF(DZ1+DZ1P).LT.0.)DZ1=-DZ1P/2.	0317.000
0664		IF(DZ2+DZ2P).LT.0.)DZ2=-DZ2P/2.	0317.500
0665		IF(IT.GT.4)GO TO 895	0318.000
0666	855	DZ1PP=DZ1P	0318.500
0667		IF(ERR1.GT.EMAX,OR,ERR3.LT.EMAX)GO TO 860	0319.000
0668		DZ1=DZ1/4.	0319.500
0669		IF(DZ2+DZ2P).GT.0.,AND,(DZ2+DZ2PP).GT.0.)DZ2=DZ2+0.5*DZ2P	0320.000
0670		IF(DIC2.GT.0.,AND,CID3.GT.0.)DZ2=DABS(DZ2+DZ2P)	0320.500
0671	860	DZ2PP=DZ2P	0321.000
0672		IF(ERR3.GT.EMAX,OR,ERR1.LT.EMAX)GO TO 865	0321.500
0673		DZ2=DZ2/4.	0322.000
0674		IF(DZ1+DZ1P).GT.0.,AND,(DZ1+DZ1PP).GT.0.)DZ1=DZ1+0.5*DZ1P	0322.500

0675	865	DZ1P=CZ1	0323.000
0676		ZET1=ZET1+CZ1	0323.500
0677		DZ2P=DZ2	0324.000
0678		ZET2=ZET2+CZ2	0324.500
0679		ZET1=ZET1+(ZET1-ZET1+DZ1)/(ZET2-ZET1)/(ZET2-DZ2-ZET1+DZ1)	0325.000
0680		ZET3=ZET3+CZ2*(ZETD-ZET3)/(ZETD-ZET2+DZ2)	0325.500
0681		ZET4=ZET4+CZ2*(ZETD-ZET4)/(ZETD-ZET2+DZ2)	0326.000
0682		IDAV1=ICAV	0326.500
0683		GO TO 210	0327.000
0684	C		0327.500
0685	875	DZ2=DZ22	0328.000
0686		DZ1=DZ22+CZ1/(DZ1+DZ12)	0328.500
0687		IF(ERR3.LT.EMAX)DZ1=DZ1-DZ12+DZ22	0328.510
0688		IF(DZ1.GT.CZ1)DZ1=(DZ1+DZ11)/2.	0328.600
0689		GO TO 810	0329.000
0690	880	IF(ID2.LT.(1.5*IDAV))GO TO 885	0329.500
0691		DZ2=(ZET1-ZET2)/2.	0330.000
0692		IF(ID3.GT.(1.5*IDAV))DZ2=DZ2/4.	0330.500
0693		IF((ZET2+CZ2).LT.Z2MIN)DZ2=(Z2MIN-ZET2)/2.	0331.000
0694		IF(ID2.GT.(1.5*ICAV))GO TO 820	0331.500
0695		DZ1=DZ2+ZET1/ZET2	0332.000
0696		GO TO 820	0332.500
0697	885	DZ1=(Z1MIN-ZET1)/4.	0333.000
0698		IF(DZ1.LT.(ZET1-ZETD)/10.)DZ1=DZ1/2.	0333.500
0699		IF(ID3.GT.ID2)GO TO 820	0334.000
0700		DZ2=DZ1*(ZETD-ZET2)/(ZETD-ZET1)	0334.500
0701		GO TO 820	0335.000
0702	890	DZ1=(Z1MIN-ZET1)/4.	0335.500
0703		IF(ID2.GE.ID1)DZ1=DZ2+ZET1/ZET2	0336.000
0704		GO TO 820	0336.500
0705	895	SZ1=SZ1+ZET1	0337.000
0706		SZ2=SZ2+ZET2	0337.500
0707		IS=IS+1	0338.000
0708		IF(IS.NE.4)GO TO 855	0338.500
0709		Z1AV=SZ1/4.	0339.000
0710		Z2AV=SZ2/4.	0339.500
0711		IS=0	0340.000
0712		SZ1=0.	0340.500
0713		SZ2=0.	0341.000
0714		IF((DZ1+DZ1P).GE.0..AND.(DZ1+DZ1PP).GE.0.)GO TO 898	0341.500
0715		DZ1=DZ1	0342.000
0716		DZ1=Z1AV-ZET1	0342.500
0717		IF((DZ1+DZ11).LT.0.)DZ1=DZ1+DZ11	0343.000

0718	IF(IID22+DZ2P) 1.0.0.AND.(DZ2+DZ2PP),GE.0.100 TO 899	0343.500
0719	DZ22=CZ2	0344.000
0720	DZ2=Z2AV-ZET2	0344.500
0721	IF(IID22+DZ22).LT.0.1072=DZ2+DZ22	0345.000
0722	GO TO 855	0345.500
0723	898 IF(IDAB8(DZ1)).LT.CAB8(DZ1P)IDZ1=DZ1+DZ1P/2.	0346.000
0724	GO TO 855	0346.500
0725	899 IF(IDAB8(CZ2)).LT.CAB8(DZ2P)IDZ2=DZ2+DZ2P/2.	0347.000
0726	GO TO 855	0347.500
0727	C	0348.000
0728	C *** END OF ITERATION LOOP ***	0348.500
0729	C	0349.000
0730	CONTINUE	0349.500
0731	WRITE(108,450)IT,ICAV,IN1,ID2,ID3,ZET1,ZET2,ZET3	0350.000
0732	IF(14.LT.TEX)GO TO 910	0350.500
0733	OUTPUT,ZET4	0351.000
0734	910 IF(12.EG.0)GO TO 920	0351.500
0735	GO=(ICAV-ICP1)/(DZD+VT)	0352.000
0736	OUTPUT,ZET1/ZETD,ZET2/ZETD,GO	0352.500
0737	IG=IG/IT	0353.000
0738	ICD=ICD/IT	0353.500
0739	WRITE(108,930)IG,YT,UFT,ICD,UST1,UST3	0354.000
0740	930 FORMAT(//,4X,4HIG=,12,2X,4HYT=,1PG12.4,2X,5HUFT=,	0354.500
0741	1 OPF9.5,2X,5HICD=,12,2X,6HUFT1=,F9.5,/,)	0355.000
0742	IF(US1.LE.(LST1)GO TO 934	0355.500
0743	ET1=AS*(UG5=US1)	0356.000
0744	ES1=ESD1	0356.100
0745	WRITE(108,932)I11,LS1,ES11,ESD1,VSD1	0356.500
0746	932 FORMAT(2X,5HI11=,1PG12.4,2X,5HLS1=,1PG12.4,2X,	0357.000
0747	1 6HES11=,1PG12.4,2X,6HESD1=,1PG12.4,2X,6HVS1=,1PG12.4,/,)	0357.500
0748	934 IF(US3.LE.(LST3)GO TO 938	0358.000
0749	ET3=AC*(UGC=US3)	0358.500
0750	ES3=ESD3	0358.600
0751	WRITE(108,936)I13,LS3,ES13,ESD3,VSD3	0359.000
0752	936 FORMAT(2X,5HI13=,1PG12.4,2X,5HLS3=,1PG12.4,2X,	0359.500
0753	1 6HES13=,1PG12.4,2X,6HESD3=,1PG12.4,2X,6HVS3=,1PG12.4,/,)	0360.000
0754	IF(14.GE.TEX)GO TO 939	0360.500
0755	IF(14.LT.TEX)GO TO 940	0361.000
0756	IF(US4.LE.(LST4)GO TO 940	0361.500
0757	OUTPUT,YT4,UGT4,EST4	0362.000
0758	VS=DND+ESD	0362.500
0759	VSD=VS/(1.+VS/VSL)	0363.000
0760	USD=US4+ZETD-ZET4	0363.500

0761		QMD=ID4/(2*VSD)		0364.000
0762		XSD=X54		0364.500
0763	939	OUTPUT,ESD,VSD		0365.000
0764	940	NS=QMS/(Q*XSS)		0365.500
0765		N1=QM1/(Q*XSI)		0366.000
0766		NT=QNT/(C*XST)		0366.500
0767		N2=QM2/(C*XSD)		0367.000
0768		N3=QM3/(C*XSD)		0367.500
0769		IF(L4,LT,TCX)GO TO 956		0368.000
0770		N4=QM4/(Q*XSD)		0368.500
0771		ND=QMD/(C*XSD)		0369.000
0772		ETD=AD*(UGFBD=USD)		0369.500
0773		ET=AD*(UGFBD=USD)		0370.000
0774	950	FORMAT(2X,1HY,7X,3META,10X,2HUS,10X,2HOM,11X,		0370.500
0775	1	1HN,12X,2HXS,12X,2PES)		0371.000
0776		IF(US4,GT,LS1)GO TO 956		0371.500
0777		IF(USD,LE,LS1)GO TO 956		0372.000
0778		WRITE(1CB,552,114,LS4,ES1,ESD,VSD)		0372.500
0779	952	FORMAT(2X,5H114=,1PG12.4,2X,5H1S4=,G12.4,2X,6HES14=,		0373.000
0780	1	G12.4,3X,5HESD=,G12.4,3X,5HVS D=,G12.4,/))		0373.500
0781	956	WRITE(1CB,550)		0374.000
0782		ESS=ID1/(2*EMGBB*QPS)		0374.100
0783		EST=ID2/(2*EMGBB2*QMT)		0374.200
0784		ES2=ID2/(2*EMGBB2*GM2)		0374.300
0785		IY=0		0374.500
0786		WRITE(1CB,560)IY,ETS,USS,QMS,NS,XSS,ESS		0375.000
0787		IY=1		0375.500
0788		WRITE(1CB,560)IY,ET1,US1,QM1,N1,XS1,ES1		0376.000
0789		WRITE(1CB,561)ETAT,UST,QMT,NT,XST,EST		0376.500
0790		IY=2		0377.000
0791		WRITE(1CB,560)IY,ET2,U52,QM2,N2,XS2,ES2		0377.500
0792		IY=3		0378.000
0793		WRITE(1CB,560)IY,ET3,U53,QM3,N3,XS3,ES3		0378.500
0794		IF(L4,LT,TCX)GO TO 963		0379.000
0795		IY=4		0379.500
0796		WRITE(1CB,560)IY,ET4,U54,QM4,N4,XS4		0380.000
0797		WRITE(1CB,562)ETC,USD,QMD,ND,XSD		0380.500
0798	960	FORMAT(2X,11,2X,2(F10.4,2X),4(1PG12.4,2X))		0381.000
0799	961	FORMAT(2X,1HT,2X,2(F10.4,2X),4(1PG12.4,2X))		0381.500
0800	962	FORMAT(2X,1HO,2X,2(F10.4,2X),4(1PG12.4,2X))		0382.000
0801	963	IF(USS,LT,CFPIGO TO 1100		0382.500
0802		IF(USP1,LT,11.5*UFP))GO TO 1100		0383.000
0803	C			0383.500

0804	C					0384.000
0805	C	INCREMENT CRAIN VOLTAGE				0384.500
0806		DVD=1				0385.000
0807		IF(I2*EG*0)IGG TO 965				0385.500
0808		IF(I2*EG*1)DVD=2				0386.000
0809		IF(I2*EG*2)DVD=3				0386.500
0810		IF(I2*EG*3)DVD=4				0387.000
0811		IF(I2*EG*5)DVD=5				0387.500
0812	965	DZDP=ZEID=2ETDP				0388.000
0813		DZD=DVD/VT				0388.200
0814		IF(DZDP*LE*E=10)IGG TO 967				0388.500
0815		MZ1=(ZEI1*MIN)/DZDP				0389.000
0816		MZ2=(ZEI2*MIN)/DZDP				0389.500
0817		MZ3=(ZEI3*MIN)/DZDP				0390.000
0818		MZ4=(ZEI4*MIN)/DZDP				0390.500
0819		Z1MIN=ZEI1				0391.000
0820		Z2MIN=ZEI2				0391.500
0821		Z3MIN=ZEI3				0392.000
0822		Z4MIN=ZEI4				0392.500
0823		ZETDP=ZETD				0393.000
0824		IF(ZETC*GE*1,E=10)IGG TO 970				0393.500
0825		ZEI1=LCI*CDZ/LQT				0394.000
0826	967	ZET1=LCI*CDZ/LQT				0394.500
0827		ZET2=LCI*CDZ/LQT				0395.000
0828		ZET3=LCI*CDZ/LQT				0395.500
0829		ZET4=LCI*CDZ/LQT				0396.000
0830		GG TO 980				0396.500
0831		ZEI4=ZEI1+Z2+DZD				0397.000
0832	970	ZEI3=ZEI1+Z2+DZD				0397.500
0833		ZEI2=ZEI1+Z2+DZD				0398.000
0834		ZEI1=ZEI1+Z2+DZD				0398.500
0835		ZEI0=ZEI0+CVC				0399.000
0836		IF(IEIC*LE*UDMIGG TO 1000				0399.500
0837		IF(IUS2*LT*ST3)IGG TO 1000				0400.000
0838		GG TO 1100				0400.200
0839		I7=1				0400.300
0840	980	IF(ZETC*GT*UDM)IGG TO 1100				0400.500
0841						0401.000
0842						0401.500
0843						0401.600
0844						0402.000
0845	1000					0402.500
0846						0402.600

0847	IT=0	0403.000
0848	IDMIN=ICAV	0403.500
0849	IDP=ICAV	0404.000
0850	WRITE(108,150)	0404.500
0851	OUTPUT,VD,VG,ZETD	0405.000
0852	GO TO 205	0405.500
0853	C	0406.000
0854	C	0406.500
0855	C INCREMENT GATE VOLTAGE IN ALTERNATELY	0407.000
0856	C LARGE AND SMALL STEPS	0407.500
0857	1100 IF(DUG*GT*(.2/VT))GO TO 1120	0408.000
0858	DUG=.4/VT	0408.500
0859	GO TO 1140	0409.000
0860	1120 DUG=.5/VT	0409.500
0861	1140 UGS=UGS+DUG	0410.000
0862	UGGT=UGGT+DUG	0410.500
0863	UGD=UGD+DUG	0411.000
0864	DUG4=DUG	0411.500
0865	IF(L4*GE*TOX)DUG4=DUG*TOX/L4	0412.000
0866	UG4=UG4+DUG4	0412.500
0867	VG=(UGS-UGFBS)*VT	0413.000
0868	IF(UGS*LE*LGM)GO TO 1200	0413.500
0869	GO TO 1500	0414.000
0870	1200 WRITE(108,120)	0414.500
0871	ZETD=C.	0415.000
0872	VD=0.	0415.500
0873	OUTPUT,VG,LGS,UGGT,UGD,UG4,ZETD	0416.000
0874	GO TO 200	0416.500
0875	1500 CONTINUE	0417.000
0876	END	0417.500

0001	SUBROUTINE FUSM(UG,A,USH)	0418.000
0002	IMPLICIT REAL*8(A-Z)	0418.500
0003	COMMON VT,CBX,EPS,TOX	0419.000
0004	UGA=UG+1./12.*A*A)	0419.500
0005	UGAS=LGA+UGA	0420.000
0006	USH=UGA*DSGRT(UGAS-UG*UG)	0420.500
0007	RETURN	0421.000
0008	END	0421.500

0001	SUBROUTINE SOLVE(UG,A,UF,X,ETA,R,QM,US,XS)	0422.000
0002	IMPLICIT REAL*8(A-Z)	0422.500
0003	COMMON VT,COX,EPS,TOX	0423.000
0004	INTEGER I	0423.500
0005	I=0	0424.000
0006	UGA=UG+1./(2.*A*A)	0424.500
0007	UGAS=LGA*UGA	0425.000
0008	USM=UGA*DSRT(UGAS*UG)	0425.500
0009	ET=A*(UG-X-2.*UF)	0426.000
0010	ET1=A*(UG-LSM)	0426.500
0011	IF(USM.GT.1X+2.*UF) ET1=ET-A*DLGG(ET*ET-X-2.*UF)	0427.000
0012		0427.500
0013	DO 10 I=1,20	0428.000
0014	CALL FX(ET1,F,FD,FCD,UG,A,UF,X)	0428.500
0015	ET1=ET1-F/FD-F*F*FDD/(FD*FD*FD)	0429.000
0016	IF(DABS(F).LE.1.E-10)GO TO 20	0429.500
0017	CONTINUE	0430.000
0018		0430.500
0019	ETA=ET1	0431.000
0020	R=ETA*ETA/2.+ETA*(2.*A+1./A)+(1.-UG)*DLGG(ETA)	0431.500
0021	FGD=ETA*ETA+ETA/A-UG	0432.000
0022	T=50.	0432.500
0023	QMZ=-CEXP(T)	0433.000
0024	QM=-VT*COX*FGD/(ETA*A)	0433.500
0025	IF(QM*GE.CPZ)QM=QMZ	0434.000
0026	US=UG-ETA/A	0434.500
0027	XS=2.*US*EPS*A/(COX*ETA)	0435.000
0028	RETURN	0435.500
0029	END	0436.000

0001	SUBROUTINE FX(ETT,FF,FFD,FFDO,UG,A,UF,X)	0436.500
0002	IMPLICIT REAL*8(A-Z)	0437.000
0003	COMMON VT,COX,EPS,TOX	0437.500
0004	FA=ETT/A	0438.000

0005	FAA=FA+UG=X=2.*UF	0438.500
0006	IF (FAA.LT.=160.) FAA=160.	0439.000
0007	FE=DEXP(FAA)	0439.500
0008	FF=ETI+ETI+FA-UG-FE	0440.000
0009	FFD=2.*ETI+(1.+FE)/A	0440.500
0010	FFDD=2.*FE/(A*A)	0441.000
0011	RETURN	0441.500
0012	END	0442.000

0001	SUBROUTINE RX(US,A,UG,ETA,R,F,X,AX)	0442.500
0002	IMPLICIT REAL*8(A-Z)	0443.000
0003	COMMON VT,CBX,EPS,TDX	0443.500
0004	ETA=A*(LG=LS)	0444.000
0005	R=ETA*ETA/2.+ETA*(2.*A+1./A)+(1.-UG)*DLOG(ETA)	0444.500
0006	F=ETA+2.*A+1./A+(1.-UG)/ETA	0445.000
0007	X=2.*US*EPS*A/(CBX*ETA)	0445.500
0008	AX=DSGT(1./((TDX*X))	0446.000
0009	RETURN	0446.500
0010	END	0447.000

* ACTUAL PROGRAM SIZE:
 * PROGRAM & INITIALIZED VARIABLES = 6961 (WORDS)
 * NON-INITIALIZED VARIABLES = 701 (WORDS)
 * TOTAL = 7662 (WORDS)

COMPILE TIME = 0008.53 SECONDS

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