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**LA THÈSE A ÉTÉ
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DESIGN AND PERFORMANCE OF MICROWAVE
AMPLIFIERS WITH GaAs FETs FOR LOW
NOISE FRONT-END RECEIVERS

by

M. Hari Sankar, M.E., M.Sc. (Eng.)

A thesis submitted to the Faculty of Graduate
Studies in partial fulfillment of the require-
ment for the degree of

Doctor of Philosophy

Carleton University

Ottawa, Canada

May 1976

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The undersigned recommend to the Faculty of Graduate
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WITH Ga As FETs FOR LOW NOISE FRONT-END RECEIVERS
submitted by M. Hari Sankar in partial fulfillment of the
requirements for the degree of Doctor of Philosophy

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ABSTRACT

A systematic design procedure for GaAs FET amplifiers intended for low noise front-end microwave receivers in microstrip form is developed. Such amplifiers are required to meet a large number of specifications such as gain, gain flatness, noise figure, gain-slope, input and output return losses, group delay and stability. Their practical realization without cut and try procedures requires accurate determination of S-parameters and noise parameters of FETs, a computing procedure for evaluating the dimensions of the microstrip elements used and an effective analysis and optimization program. The computer program developed for the design uses a unique combination of gradient and search for optimization and it is specifically suited for microstrip circuit designs, where the dimensions of the elements are constrained to lie within certain bounds. It is also capable of optimizing circuit elements for all the performance objectives cited above.

Computer studies using GAT-2 FETs show the following:

- i) two stage modules are superior to pairs of cascaded single stage modules for gain and group delay performance;
- ii) series transmission line elements provide better overall performance than matching sections using stubs and low pass filter structures;
- iii) tolerance in the dielectric constant and the dimensions of the commercially available substrates can significantly affect gain performance, producing as much as 2dB change in gain for single stage modules.

The effectiveness of the design procedure is tested by fabricating a two stage 3.5 to 4GHz amplifier using Plessey GAT-2 FETs.

Theoretical and experimental performances show good agreement with out post-fabrication alterations.

Return losses of the order of 10dB are normal with FET amplifiers. These return losses are responsible for group delay distortion on cascading. An analysis of such group delay problems and computer aided group delay equalization procedures are also presented.

A new method of estimating the noise parameters from the data provided by the manufacturers is proposed.

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CHAPTER 1

INTRODUCTION

1.1 Introduction

Design of broad-band, low-noise, solid state amplifiers is currently a subject of considerable interest to microwave engineers. This interest is the result of the commercial availability of microwave field effect transistors (FETs), which are capable of providing low noise figure and high current-gain band-width product over a frequency range of a few GHz to 15GHz.

Such low noise FETs have several areas of potential application. In radar receivers and microwave communication links, for instance, a low noise FET front end provides an increase in sensitivity making possible reduction in the output power requirement of the transmitter. This results in a reduction in the cost of the equipment. FET front ends also facilitate increasing the distance between the relay stations and thus reduce the number of relays required. An Electronic Counter Measure System (ECM) requires devices with a wide dynamic range and low distortion¹. FETs, with their low noise figure and linear transfer characteristics, are ideally suited for this purpose. Due to their light weight and superior performance, FETs are being considered for TWT replacements in satellite systems. The above examples are just a few of the many possible applications of FET amplifiers.

The existing design techniques of FET amplifiers used in receiver front-end applications necessitate considerable post fabrication alterations. For this reason, this thesis considers the development of a simple and effective computer-aided approach with the aim of realizing FET amplifiers of performance close to theoretical prediction.

This Chapter details the objective and the scope of the study undertaken in this thesis, setting the work in the context of current developments in the FET amplifier field.

1.2 Why FETs?

Until recently, low noise microwave amplification at X-band and above was limited to tunnel diodes, parametric amplifiers, travelling wave tubes (TWTs) and bipolar transistors. Fig. 1.1 shows a plot of noise temperature of low noise microwave devices as a function of frequency². FETs are superior to TWTs and tunnel diodes because they have less noise figure and 10 to 20dB more dynamic range. Further, they neither present isolation problems as in tunnel diodes nor are as complex and as space-consuming as TWTs. Above 4GHz, FETs have higher gain, low noise figure and about the same power capability as bipolar transistors^{3,4}. In short, FETs are superior to other microwave devices, for low noise amplifier design, because of their low noise figure, high gain, low intermodulation distortion, large dynamic range, high radiation resistance and better isolation.

Fig. 1.1. Noise temperature vs frequency for low-noise microwave devices². (updated)

1.3 State-of-the-Art: FETs

The microwave FET is currently undergoing rapid development. Due to its potential as a low noise device, improvements in both noise figure and power gain are being made. Fig. 1.2 indicates the present state-of-the-art for the microwave field effect transistors.⁵ All the devices shown in the figure have 1 μ m gate, except where indicated otherwise. The solid circles refer to buffered layer devices. The shaded area represents the theoretical range of noise figures encompassing a spread of parasitic resistance values typical of present devices. The figure also indicates that, over a frequency range of 4 to 12GHz, the noise figure typically increases from 2 to 4dB. For example, Nippon Type NEC 388 device, one of the best X-band low noise FETs available today, has a noise figure of 2.5dB at 8GHz and 3.5dB at 12GHz⁵. The specifications of low noise FETs are shown in Table 1.1.

The power FET, which is in the early stages of development, does not at present compete as a device of proven reliability. Part of the reason is the high thermal resistance of GaAs and it is necessary to use an interdigitated structure to achieve the desired power level. The most impressive development reported in this area is that of Fujitsu's 8GHz FET, which delivers 2.2 watts of power at 22% drain efficiency and 4.2dB gain.

1.4 State-of-the-Art: FET Amplifiers

The noise performance reported recently for FET amplifiers is indicated in Fig. 1.3. In the figure, solid lines represent narrow band

Fig. 1.2. Noise performance of GaAs FET devices obtained at various laboratories⁵.

- AV = AvanteK
- FA = Fairchild
- HI = Hitachi
- HP = Hewlett-Packard
- IBM = International Business Machines
- NEC = Nippon Electric Company
- PL = Plessey Company
- RAY = Raytheon

Fig. 1.3. Noise figure vs frequency summarizing the performance of experimental FET amplifiers. The circles show the noise figures of the FETs used in the front stages⁶.

AT = Avantek
 HP = Hewlett-Packard
 IBM = International Business Machines
 NEC = Nippon Electric Company
 WJ = Watkins Johnson
 PY = Plessey
 A = Amplica

Table 1.1. Low noise field effect transistors.

MAKE	TYPE	L (μm)	G dB	F dB ⁰	f GHz	f _{max} GHz	Availability
Hitachi	HCRC85	1	11	3	8	60	A
Hitachi	HCRC87	1/2	13	2.5	8	70	A
Daxel	-	1/2	9	3	18	-	NA
Nippon	NE388	1/2	13	2.5	8	80	A
Nippon	NE244	1	11	3	8	55	A
Plessey	GAT-3	1	6	5.5	8	20	A
Plessey	GAT-2	2	8.5	4.5	3	8	A
Hughes	-	1	9	5	17	-	NA

where

L = channel length

G = maximum available gain

F₀ = minimum noise figure

f = frequency at which F₀ and G are specified

f_{max} = maximum frequency of oscillation.

amplifiers and dotted lines, wide band amplifiers. The circles indicate the noise figure of one stage amplifiers which was designed for minimum noise figure. The dotted straight lines show the 1dB degradation in noise figure due to cascading.

Cryogenic cooling of FET amplifiers makes it possible to achieve even lower noise figures allowing the amplifier to compete with parametric amplifiers at frequencies up to 12GHz. For example, the reported noise figure of a cooled HP X-band FET amplifier is 1.6dB at a noise temperature of 130°K ⁶. For comparison, uncooled parametric amplifiers operating in this frequency range have about 100°K noise temperature, whereas cryogenically cooled parametric amplifiers offer noise temperature of 50°K (Fig. 1.1)².

1.5 The Objective

Low noise FET amplifiers can be designed either by graphical procedures using Smith chart or by computer-aided methods. At best, using Smith charts, they may be designed for a specified gain, stability and noise figure. Most of the low noise front end amplifiers used in airborne receivers and satellite systems are required to meet a large number of specifications such as gain, gain flatness, gain slope, input/output return loss, group delay variation, noise figure and stability. The graphical procedures cannot handle such complex objectives and hence computer-aided methods are used. The published design procedures^{7,8,9} optimize the circuit elements only for a few of the above-mentioned

specifications and this necessitates considerable post fabrication adjustments of the circuit. This is not only tedious, but time consuming and costly. Further, the available publications^{10,11,12,13} do not report optimization for noise figure, group delay variation and gain slope in amplifiers.

The aim of this design thesis is to:

- (a) develop a computer-aided procedure for designing FET amplifiers with a given set of specifications (e.g. Table 6.1) on gain, gain flatness, gain slope, input and output return losses, group delay variation and noise figure;
- (b) realize a two-stage FET amplifier using Plessey GAT-2 FET, in microstrip circuits, to determine the effectiveness of the design procedure;
- (c) study the problem encountered in cascading FET amplifiers of different impedance levels and to investigate methods of solving such design problems.

1.6 The Organization of the Thesis

The subsequent Chapters of the thesis are arranged as follows. Chapter 2 deals with the device description, scattering and noise parameter measurements and an error model for correcting the measured S-parameters. In the last section of Chapter 2, a method for calculating the device noise parameters from the manufacturers' data is described. Chapter 3 contains a summary of microstrip design equations obtained either

from available literature or compiled by measurements. Typical specification of a low noise amplifier, and available design procedures are summarized in Chapter 4. The program for the analysis and optimization of FETs is described in Chapter 5. The selection of best circuit configuration and the performance variation of the amplifier due to changes in the dielectric constant and the dimensions of the substrate are also treated in this Chapter. Chapter 6 gives the fabrication details, measurement procedure and the results of the experiments. Biasing consideration for the amplifier and optimum amplifier cascading schemes form a part of this Chapter. The high return losses of the FET amplifier result in large group delay variation, if the individual amplifier modules are directly connected. Such group delay problems and a generalized procedure for solving them are described in Chapter 7. Finally, conclusions and suggestions for the extension of the research are presented in Chapter 8.

CHAPTER 2

THE SCHOTTKY BARRIER GATE FET-CHARACTERIZATION AND MEASUREMENTS

2.1 Introduction

The high frequency limitations of the field-effect transistors arise partly due to carrier transit time effects in the active channel region and partly due to resistance/capacitance effects, associated with the device physical structure. The Schottky barrier gate FET described in this Chapter takes advantage of the high electron mobility and drift velocity of GaAs, to yield shorter transit time than that of silicon devices. By the use of a Schottky barrier gate, the junction resistance/capacitance effects are significantly reduced, thus extending the device high frequency performance to the X-band microwave region.

The following sections of this Chapter review the device literature of SBFETs and discuss its representation by an equivalent circuit model. They also include the measurements of the S-parameters and the noise parameters of the Plessey GAT-2 FET. A simple method to correct the measured S-parameters and a systematic procedure for evaluating the noise parameters of FETs, from the manufacturers' data sheet, are also presented.

2.2 Device Description

A schematic drawing of a Schottky barrier FET is shown in Fig.

2.1. This n-channel FET uses alloyed metal ohmic contacts to form source and drain and a metal semiconductor junction to form the gate. A finite spacing separates the gate contact from the source and drain electrodes.

Fig. 2.1. Cross-section of GaAs FET.

For microwave FETs, this spacing is limited to a lower value of approximately $1\mu\text{m}$, dictated by photo-lithographic limitations, but usually it is several times this value. The gate length, L , which is one of the crucial dimensions of the FET, is typically of the order of $1\text{-}4\mu\text{m}$. Because of the finite separation of the contacts, parasitic resistances of the order of 5 to 20 ohms are introduced between the edges of the gate electrode and source and drain electrodes²³. These parasitic resistances, although important, do not affect the intrinsic operation of the transistor. But, they affect strongly the noise performance of the FET¹⁸.

The behaviour of junction gate field-effect transistors, at drain potentials less than pinch-off, can be accurately described by means of Shockley's "gradual channel" approximation¹⁴. The gradual-channel model is based on the assumption that the longitudinal electric field gradients within the channel depletion layer are negligible compared to the transverse gradients. Consequently, the potential distribution, $V(x,y)$ (Fig. 2.3) within the depletion layer can be approximated from the solution of the Poisson equation in one dimension, as

$$\frac{\partial^2 V}{\partial y^2} = -q \frac{N(x,y)}{\epsilon} \quad (2.1)$$

where

- q = electron charge
- $N(x,y)$ = donor impurity concentration in the n channel
- ϵ = permittivity of the material.

If this theory is applied to FETs with small channel length L and devices operating beyond pinch-off, significant deviations are encountered between experiment and theory. For example, it was predicted that the maximum oscillation frequency $f_{\max}$ of the JFET was proportional to $1/L^2$ by Shockley's theory¹⁴. For short gate length FETs, operating in the saturation region, experiments indicated that $f_{\max}$ is proportional to $1/L$ rather than $1/L^2$.¹⁶

The first attempt to analyze velocity saturation effects in GaAs was made by Turner and Wilson¹⁵. These workers retained the gradual channel approximation of Shockley throughout the channel, but imposed the condition that the onset of velocity saturation always begins precisely at the drain end of the gate. Lehovec and Zuleeg¹⁶ modified this model by replacing the constant mobility with field dependent mobility, but they assumed the length of the velocity saturated region is small compared with channel thickness.

Grebene and Ghandhi¹⁷ analyzed the characteristics of the FET beyond pinch-off by treating the device channel as made up of two separate regions along the directions of current flow, as shown in Fig. 2.2a. In region I, in the vicinity of the source, the gradual channel approximation is used and the depletion layer profile is estimated, from the solution of one dimensional Poisson's equation. In region II, near the drain, the two-dimensional Poisson's equation $\left(\frac{\partial^2 V}{\partial x^2} + \frac{\partial^2 V}{\partial y^2} = -q \frac{N(x,y)}{\epsilon} \right)$ is solved to determine the potential distribution. The boundary values for the solution of Poisson's equation within regions I and II are chosen

Fig. 2.2. a) Depletion profile within the active channel in pinched operation, sectioned about the axis of symmetry.
 b) A simplified form of velocity field characteristics of GaAs FET.

to require the continuity of the potential distribution across the interface separating them. Since the drain current is finite, it is postulated that the channel is not fully depleted in region II and the current flow is constrained to a narrow conductive filament ϕ . For practical device geometries at high electric field strengths, the saturation of the carrier drift velocity is found to be the dominant factor in determining the dimensions of this region.

Following the procedure suggested by Grebene and Gandhi, Statz obtained the following results for short channel FETs¹⁸.

In region I ($\mu = \mu_0$), the source to drain current

$$I_d = \frac{g_0 Z W_{00}}{L_1} (p^2 - s^2 - (2/3)(p^3 - s^3)) \quad (2.2)$$

where

g_0 = ρa (asymmetric FET)

a = channel thickness

ρ = conductivity of the channel material

Z = gate width

L_1 = length of channel region I

W = gate to channel potential

$$p = \left(\frac{W_p}{W_{00}} \right)^{1/2}$$

$$s = \left(\frac{W_s}{W_{00}} \right)^{1/2}$$

W_{oo} = gate to channel potential required to deplete the channel carrier

W_s = effective potential difference between gate and the channel at the source side

W_p = W at the pinch-off point

In region II ($v=v_{sat}$),

$$I_d = g_o Z E_s (1-p) \quad (2.3)$$

where

E_s is the saturation field (Fig. 2.2b).

Similarly, for a short-gate device with $I_d/I_s > 0.1$, the ~~trans~~ conductance is given by¹⁸:

$$g_m = \frac{I_s}{2W_{oo}} \left(\frac{1}{1 - I_d/I_s} \right) \quad (2.4)$$

where

$$I_s = g_o Z E_s$$

= maximum possible drain current that could exist if the channel were fully undepleted.

These equations showed reasonable agreement between the theoretical and experimental results²³.

The assumption of a constant saturation velocity above the critical field disregards the bulk differential conductivity inherent in GaAs, which can cause instability in the FET. Recent¹⁹ computer simulation

studies have ruled out the possibility of high field domain transit, and stable current voltage characteristics are obtained as shown in Fig. 2.3. The only indication of the bulk negative differential conductivity is a slight decrease in the drain current against the drain voltage increase or the presence of a small negative resistance. But, these effects are seldom found in available practical devices.

Various fabrication procedures are currently in use.^{20,21,22}

In one process, the devices are fabricated in thin epitaxial films of GaAs typically 0.5 μm thick, with a carrier density of around 10^{17} and electron mobility of $5000 \text{ cm}^2 \text{ V}^{-1} \text{ S}^{-1}$. These films are grown by the Ga-AsCl₃-N₂ vapour transport methods on semi-insulating chromium doped, GaAs substrate. SiO₂ film of 3000 Å thick is then deposited on the wafer by chemical vapour deposition using SiH₄ and O₂. This deposition is carried out at a relatively low temperature of 350°C to avoid degradation of the electrical properties of GaAs. After the source and drain windows are made, Au-Ge is evaporated over the slice with the photoresist still in place. The unwanted metal is then lifted off by dissolving the photoresist. This method of metal definition is very simple, gives sharp edges and is capable of providing good dimensional control. These contacts are then alloyed into GaAs epilayer. The gate contacts are Cr/Au and they are formed by a similar photolithography and metal lifting process. The epitaxial film outside the active area is removed by mesa etching. Fig. 2.4 shows a photograph of a typical GaAs FET with a 2 μm gate length.

Fig. 2.3. Calculated drain current/drain voltage characteristics of GaAs FET.
 ($a=0.4\mu\text{m}$, $L=1\mu\text{m}$, $N_D=3 \times 10^{16}\text{cm}^{-3}$)
 (Ref.: S. Okazaki et al "Microwave oscillations with GaAs FET", Proceedings of the 6th Conference on Solid State Devices, Tokyo, pp. 157-162, 1975).

Fig. 2.4. Gallium arsenide microwave field effect transistor with $2\mu\text{m}$ gate length.

2.3 An Equivalent Circuit Model for GaAs FET^{24,25,26,27}

A small signal equivalent circuit of the microwave FET valid up to 12GHz is shown in Fig. 2.5. It also includes a perspective sketch which indicates the equivalent circuit parameters and the approximate region of FET responsible for such elements. These elements are defined as follows:

- C_{gs} = gate to channel capacitance
- C_{gd} = drain to gate feedback capacitance
- g_m = transconductance of the device
- g_d = output conductance
- R_i = effective channel resistance
- R_s = source to channel plus contact resistance
- R_g = gate spreading resistance
- R_d = drain to channel plus contact resistance
- C_2 = internal feedback capacitance²⁵

The transconductance g_m is the most important parameter in the model, being the major gain-contributing parameter.

The small signal transconductance g_m at the frequency of interest ω can be written as²⁸:

$$g_m = g_{mo} e^{-j\omega T_0} \quad (2.5)$$

where g_{mo} is the low frequency transconductance of the device and T_0 is the phase delay of the current generator. This delay corresponds to the time required for the electrons to traverse a portion of the gate length

Fig. 2.5. Small signal equivalent of GaAs FET.
 a) A perspective sketch indicating geometric region.
 b) Circuit schematic based on (a).

at the scattering limited velocity¹⁵. For example, for 1 μm gate FET,

$$T_o = \frac{L}{V_s} = \frac{10^{-4} \text{ cm}}{2 \times 10^7 \text{ cm/sec}} = 5 \text{ psec}$$

An increase in the value of g_{mo} with drain current, up to $I_d = I_{dss}$, as shown in Fig. 2.6, can be explained by the analysis of Statz¹⁸ (Eqn. 2.4). But the analysis fails to account for the sharp fall in g_m for currents above I_{dss} . This may be due to the enhancement of R_s due to current crowding²¹ and also due to a possible reduction in the mobility in the epitaxial layer near the surface²⁶.

In Fig. 2.5, C_2 represents the internal feedback capacitance which accounts for the contribution from the drain to channel feedback through the substrate²⁵ and L_s , L_g and L_d represent lead inductances of source, gate and lead. Several authors have suggested modifications for this equivalent circuit by the addition of output drain source capacitance C_d parallel with g_d , or by adding a resistance R_{gd} in series with C_{gd} in order to adequately interpret the behaviour of Y_{12} and Y_{21} ^{24,25}. The typical values of the equivalent circuit elements of GaAs FETs are shown in Table 2.1. The circuit model shown in Fig. 2.5 has been successfully used to determine the S-parameters of several FETs²⁷.

The method used for calculating the S-parameter from the equivalent circuit is to derive y-parameters of the intrinsic transistor and to obtain S-parameters from y. The y-parameters of the intrinsic transistor are as follows:²⁵

Fig. 2.6. The variation of low frequency transconductance as a function of drain current²⁴.
(Ref.: G.E. Brehm & G.D. Vendelin, "Biasing FETs for Optimum Performance", *Microwaves*, pp. 38-44, February 1974.)

Table 2.1. Typical equivalent circuit parameters of several FETs.

Parameters	NEC (Exp) $V_{DS}=3V, I_D=15mA$	Fairchild FMT981 $V_{DS}=5V, V_{GS}=0$	H.P. (Exp) $V_{DS}=5V, V_{GS}=0$	Plessey (GAT-2) $V_{DS}=5V, V_{GS}=0$
R_g/Ω	2.5	<1	3 Ω	5
R_v/Ω	2	10	3.5	5
R_s/Ω	5	15	5.5	15
R_D/Ω	8	-	7	5
C_{gs}/pF	0.75	0.4	0.5	0.5
C_{gd}/pf	0.035	0.05	0.06	0.05
g_d/mV	2.1	1.6	1.5	1.0
g_m/mV	22	20.	33	12
$L/\mu m$	1.5	2	1	2

$$g_{11} = \omega^2 C_{gs}^2 (R_i + R_s) / D \quad (2.6)$$

$$b_{11} = \omega [C_{gs} (1 + g_m R_s) + C_{gd}] / D \quad (2.7)$$

$$g_{12} = \omega^2 C_{gs} C_2 (R_i + R_s) / D \quad (2.8)$$

$$b_{12} = -\omega (C_{gd} + C_2 g_d R_s) / D \quad (2.9)$$

$$g_{21} = g_m / D \quad (2.10)$$

$$b_{21} = -\omega [(C_{gs} + C_2) g_m (R_s + R_i) + C_{gs} g_d R_s + C_{gd}] / D \quad (2.11)$$

$$g_{22} = g_d [1 + g_m R_s] / D \quad (2.12)$$

$$b_{22} = \omega [C_{gd} + C_2 (1 + g_m (R_s + R_i) + C_{gs} g_d R_s g_m (R_s + R_i))] \quad (2.13)$$

where

$$D = [1 + g_m R_s + \omega^2 (C_{gs} + C_2)^2 (R_s + R_i)^2]$$

In order to determine the value of the equivalent circuit elements from the measured S-parameters, several procedures are adopted^{22,24,25,28}. In the procedure suggested in reference 28, trial values of the components are selected and the S-parameters for this model are described by a two-port called JJ. A second two-port entered in the computer file as KK contains the measured S-parameters. When the parameter JJ is set to KK,

the program compares the S-parameters and varies selected elements in an effort to minimize the error function described by²⁸:

$$EF = \frac{1}{N} \sum_{F_1}^{F_N} \{W_1 |S_{11}^{JJ} - S_{11}^{KK}|^2 + W_2 |S_{22}^{JJ} - S_{22}^{KK}|^2 + W_3 |S_{21}^{JJ} - S_{21}^{KK}|^2 + W_4 |S_{12}^{JJ} - S_{12}^{KK}|^2\} \quad (2.14)$$

Vedelin and Omoni have published the equivalent circuit element values of several commercially available transistors using this procedure²⁸.

2.4 S-Parameter Measurements

The wave functions used to define S-parameters for a two-port network are shown in Fig. 2.7. The linear equations describing the two-port network are then:

$$\begin{aligned} b_1 &= S_{11}a_1 + S_{12}a_2 \\ b_2 &= S_{21}a_1 + S_{22}a_2 \end{aligned} \quad (2.15)$$

where

$$S_{11} = b_1/a_1 \big|_{a_2=0} = \text{input reflection coefficient}$$

$$S_{22} = b_2/a_2 \big|_{a_1=0} = \text{output reflection coefficient}$$

$$S_{21} = b_2/a_1 \big|_{a_2=0} = \text{forward transmission gain}$$

$$S_{12} = b_1/a_2 \big|_{a_1=0} = \text{reverse transmission gain}$$

Fig. 2.7. Two-port scattering parameter terminology.

It can also be shown that, the parameters $|S_{11}|^2$, $|S_{22}|^2$, $|S_{21}|^2$ and $|S_{12}|^2$ have the following important physical meaning when the terminating impedance $Z_i = Z_o$.

$$|S_{11}|^2 = \frac{\text{Power reflected from the network input}}{\text{Power incident on the network input}} \quad (2.16)$$

$$|S_{22}|^2 = \frac{\text{Power reflected from the network output}}{\text{Power incident on the network output}} \quad (2.17)$$

$$|S_{21}|^2 = \text{Forward power gain with } Z_o \text{ source and load} \quad (2.18)$$

$$|S_{12}|^2 = \text{Reverse power gain with } Z_o \text{ load and source.} \quad (2.19)$$

The setup normally used to measure the S-parameters of the transistor from 0.1 to 12GHz is the HP 8410 network analyzer system (HP 8746B S-parameter test set unit, HP 8717B transistor bias supply and HP 11608 test fixture). This arrangement is ideal for measuring the S-parameters of the transistors mounted in certain types of packages. Plessey GAT-2, used for amplifier design, is a LID mounted FET. The LID is a rugged ceramic carrier with metallized pads for attachment to a metallized substrate. The device-chip is die attached to the LID and the leads are bonded from the chip to the pads. This package offers low parasitic reactances. The test fixture HP 11608 cannot hold LID packages and hence a special test fixture was constructed in order to test the FETs.

The test fixture consists of two 50 ohm microstrip lines on an alumina substrate, which is fixed to the jig by microstrip coaxial adapter

mountings. The device is mounted using conductive epoxy. Fig. 2.8 shows a photograph of the transistor test fixture. The HP 8745A transmission and reflection test mount is used for the measurement, with test fixture and HP 11605A flexible arm. Such transmission and reflection measurement setups are shown in Figs. 2.9 and 2.10. In such setups, the measurement errors are usually caused by the launchers, bias structures, tolerance of 50 ohm lines and other imperfections of the jig. Accurate characterization of the jig is therefore essential for obtaining reliable values of device S-parameters. In particular, when microstrip circuits are used for fabricating the jigs, it is essential to include the susceptance of the truncated edges in the characterization of the jig. In the next paragraph, a simple procedure to characterize jig accurately and to correct the measured S-parameters is presented.

Different error models are in use for characterizing the jig and for evaluating the S-parameters of the transistors^{29,30,31}. In this procedure, the S-parameters of the jig are characterized with open, short and matched terminations in the place of the device. Transmission measurements are performed connecting the two ports together. The data thus obtained are used to correct the measured value of the S-parameters with the device mounted on the jig³¹. The complete error model is shown in Fig. 2.11 where the subscripts $S^{(1)}$ and $S^{(2)}$ refer to the S-parameters of the input and output ports alone.

If R_F and R_R represent the reflection coefficient and T_F and T_R the transmission coefficients of the input and output ports with the

Fig. 2.8. The jig for device parameter measurements.

Fig. 2.9. Reflection measurement set-up.

Fig. 2.11. Model for error analysis.

device, then the actual values of the S-parameters are given by (Appendix A):

$$S_{11} = \frac{(R_F - S_{11}^{(1)}) [S_{22}^{(2)} (R_R - S_{11}^{(2)}) + S_{21}^{(2)} S_{12}^{(2)}] - S_{22}^{(2)} T_R T_F}{D} \quad (2.20)$$

$$S_{12} = \frac{T_R S_{21}^{(1)} S_{12}^{(2)}}{D} \quad (2.21)$$

$$S_{21} = \frac{T_F S_{12}^{(1)} S_{21}^{(2)}}{D} \quad (2.22)$$

$$S_{22} = \frac{(R_R - S_{11}^{(2)}) [S_{22}^{(1)} (R_F - S_{11}^{(1)}) + S_{12}^{(1)} S_{21}^{(1)}] - S_{22}^{(1)} T_R T_F}{D} \quad (2.23)$$

$$D = [S_{12}^{(1)} S_{21}^{(1)} + S_{22}^{(1)} (R_F - S_{11}^{(1)})] [S_{21}^{(2)} S_{12}^{(2)} + S_{22}^{(2)} (T_R - S_{11}^{(2)})] - S_{22}^{(2)} S_{11}^{(1)} T_R T_F$$

where

$$S_{11}^{(1)} = R_{Fm}$$

$$S_{22}^{(1)} = \frac{R_{Fo} + R_{Fs} \Gamma_L - R_{Fm} (1 + \Gamma_L)}{(R_{Fo} - R_{Fs})}$$

$$S_{21}^{(1)} S_{12}^{(2)} = T_{F1} \left[1 - \left\{ \frac{R_{Fo} + R_{Fs} \Gamma_L - R_{Fm} (1 + \Gamma_L)}{(R_{Fo} - R_{Fs})} \right\} \left\{ \frac{R_{Ro} + R_{Rs} \Gamma_L - R_{Rm} (1 + \Gamma_L)}{(R_{Ro} - R_{Rs})} \right\} \right]$$

and

$$S_{12}^{(1)} S_{21}^{(1)} = \frac{(R_{Fs} - R_{Fm})}{(R_{Fs} - R_{Fo})} \left\{ 2R_{Fo} + R_{Fs} (\Gamma_L - 1) - R_{Fm} (1 + \Gamma_L) \right\}$$

where

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0}$$

Z_0 = characteristic impedance of microstrip line

Z_L = susceptance of the open end line

R_{Fo}, R_{Ro} = reflection coefficients with open termination in the forward and reverse directions

R_{Fs}, R_{Rs} = reflection coefficients with short termination in the forward and reverse directions

R_{Fm}, R_{Rm} = reflection coefficients with matched termination in the forward and reverse directions

T_{F1} = the forward transmission coefficient with two ports directly connected without the device.

Similar expressions can be obtained for $S_{11}^{(2)}, S_{22}^{(2)}, S_{12}^{(2)}, S_{21}^{(2)}$ and $S_{21}^{(2)} S_{12}^{(1)}$ (Appendix A).

Z_L is either determined experimentally³² or by using the available results on microstrip end capacitance³³.

Figures 2.12 and 2.13 show a plot of S-parameters obtained by this procedure for a GAT-2 FET sample as a function of frequency and drain current. It can be noted that S_{21} varies widely with drain current which is expected because of the dependence of g_m on drain current.

2.5 Measurement of Noise Parameters

The noise factor F of a linear transducer at a given input frequency is the ratio of signal to noise at the input of the transducer to

Fig. 2.12, A plot of S_{21} and S_{12} as a function of frequency for GAT-2 FET.
 $V_{DS}=5V$, $V_{GS}=0V$, $V_{GS}=-1.8V$

Fig. 2.13. A plot of S_{11} and S_{22} as a function of frequency for GAT-2 FET.
 $V_{DS}=5V$, $V_{GS}=0V$

the signal to noise ratio at the output.

$$\text{Noise factor} = \frac{S_i/N_i}{S_o/N_o} = \frac{N_o}{GN_i} = F \quad (2.24)$$

The advantage of defining a noise factor in this way is that the signal power cancels from the expression, leaving a measure which depends only on the transducer, but not on the signal level. Noise factor is often expressed in decibels and is termed as noise figure (NF).

$$NF = 10 \log_{10}(F) \text{ dB}$$

Noise factor depends upon the internal structure of the transducer as well as the input termination. Thus, the noise performance of a transducer is meaningfully characterized only if the input termination is specified. It is possible to refer all the noise of a linear transducer (two port) to a single noise voltage in series with the input termination, and a noise current generator parallel with the input termination. These noise sources together with the noise free transducer adequately represent the noise behaviour of the transistor. The mean square value of this voltage can be expressed as an equivalent noise resistance of a two port³⁴.

$$R_n = \frac{e_n^2}{4KT\Delta f}$$

where

K = Boltzmann's constant

T = absolute temperature (° Kelvin)

Δf = bandwidth

By varying the source admittance, it is possible to change the value of noise factor. The value of input admittance corresponding to the minimum noise factor F_0 of the device is known as the optimum source admittance Y_0 .

In a linear two-port, these parameters, Y_0 , F_0 and R_n , are related to the noise factor by the equation:^{34,35}

$$F = F_0 + \frac{R_n}{G_s} ((G_s - G_0)^2 + (B_s - B_0)^2) \quad (2.25)$$

where

$$Y_0 = G_0 + jB_0$$

$$Y_s = G_s + jB_s = \text{source admittance.}$$

The four parameters F_0 , G_0 , B_0 , and R_n , characterize the noise properties of the transducer and are independent of source admittance, Y_s .

Consider a simplified transducer noise figure measuring setup, shown in Fig. 2.14. It consists of an input termination, an excess noise source, a receiver under test and an output power detector. The noise power with the excess noise source off is N_1 and that with the excess noise source on is N_2 .

N_1 consists of the amplified input termination noise KT_0BG plus the noise generated within the amplifier $(F-1)KT_0BG$. N_2 consists of N_1 plus excess noise power $K(T_2 - T_0)BG$. Therefore, at $T=T_0$,

Fig. 2.14. A typical noise figure measuring system.

$$\frac{N_2}{N_1} = \frac{KT_0 BG + (F-1)KT_0 BG + K(T_2 - T_0)BG}{KT_0 BG + (F-1)KT_0 BG}$$

where G is the power gain of the amplifier.

$$\frac{N_2}{N_1} = \frac{FT_0 + (T_2 - T_0)}{FT_0}$$

Therefore, noise factor

$$F = \frac{(T_2 - T_0)}{T_0} \times \frac{1}{[(N_2/N_1) - 1]}$$

$$\text{Noise figure } F(\text{dB}) = 10 \log \frac{(T_2 - T_0)}{T_0} - 10 \log \left(\frac{N_2}{N_1} - 1 \right) \quad (2.26)$$

$10 \log \left(\frac{T_2 - T_0}{T_0} \right)$ is known as the "Excess noise ratio" (ENR) and its value is 15.2dB for the source used in this work.

The ratio (N_2/N_1) is known as the 'Y' factor.

The equation (2.26) then reduces to:

$$F(\text{dB}) = \text{ENR} - 10 \log(Y-1)$$

Noise measurements of the FETs are carried out using the 'Y' factor method, with the setup shown in Fig. 2.15. This method involves the use of a precision attenuator in the I.F system, which yields Y factor measurements that are accurate within $\pm 0.1\text{dB}$. Non-linearities and all other effects of circuit, after the attenuator, are of no consequence since the output is always adjusted to the same level. The attenuator

Fig. 2.15. Block diagram for the noise measurements of GaAs FETs.

is initially adjusted for a convenient reading on the meter with the noise source off. With the noise source on, the attenuator setting is changed to get the same reading on the meter. The difference in the attenuator setting gives the 'Y' factor in dB.

The measurement system uses a solid state noise source (Ailtech No. P/N 7616), 3dB pad, two low loss double stub tuners, a line stretcher, a resistive mixer, IF amplifier and precision noise monitor (Ailtech No. 7330). The stub tuners are for changing the source and load VSWR. The minimum noise figure of the device is measured using the standard 'Y' factor method suggested in references 22, 70, 36 and 37. By this procedure, the noise factor of the device F_1 is calculated from:

$$F_t = F_1 + \frac{F_2 - 1}{G_1}$$

where F_t is the total noise factor of the system with the device and F_2 is that without the device and G_1 is the gain of the device.

The reading corresponding to the minimum noise figure gives the first three parameters F_0 , B_0 and G_0 . The parameter, R_n ,

is computed from an additional measurement of Y factor for another source admittance Y_s . Care is taken to ensure that G_o and B_o are referred to the same input reference plane as the S-parameter data. In the actual measurement, the possibility of system errors caused by mismatch, temperature and relative error contribution of individual component is considered.

The specified value of ENR refers to the measurement at room temperature (290°K). The measurement seldom, if ever, is made at that temperature. For high noise figures, this contribution is quite small and is usually neglected, but for low NF, the correction is significant. Typically, a variation of 20° from the assumed 290° would cause an error of about 0.3dB in measured noise figure³⁷.

The noise figure of the network under test is sensitive to source impedance. So, if source impedance is not known very accurately, the network will be operating under different conditions from those under which the performance is desired. Typically, for a measured N.F. of 5dB, the source VSWR is 1.2:1, the maximum error that can be expected is 0.4dB.³⁷

The measured values of F_o and R_n are plotted as a function of frequency in Figs. 2.16 and 2.17 and R_o and X_o are plotted on Smith chart shown in Fig. 2.18.

2.6 Noise Parameter Calculations

One important parameter that is not supplied by the manufacturer's data sheet is the value of optimum source impedance with respect

Fig. 2.16. A plot of minimum noise figure as a function of frequency.

Fig. 2.17. A plot of noise resistance R_n as a function of frequency.

to minimum noise (Z_0). This parameter provides an insight to the performance of any transistor as a low noise device. If Z_0 and the impedance corresponding to S_{11}^* are very different, it is quite likely that both input return loss and gain will be poor, if the device is matched for minimum noise figure. This Section gives a simple procedure for calculating Z_0 from the Y parameters and from the minimum value of noise figure supplied by the manufacturers.

Fig. 2.19 shows the representation of a noisy FET by a noiseless FET, which is preceded by a noisy network^{18,23}. Here, r_n represents a thermal voltage generator at the standard temperature T_0 , g_n a shunt thermal current generator at the same temperature and Z_c the correlating impedance at absolute zero. The noise figure of the combined network is the same as that of the original FET.

The expressions for r_n , g_n and Z_c can be written in the form^{18,23}:

$$g_n = \left\{ \left| \frac{Y_{11}}{Y_{21}} (g_{dn})^{1/2} - jC(g_{gn})^{1/2} \right|^2 + (1-C^2)g_{gn} \right\} \quad (2.28)$$

$$r_n = R_m + R_f + \frac{g_{dn}(1-C^2)g_{gn}}{|Y_{21}|^2 g_n} \quad (2.29)$$

$$Z_c = R_m + R_f + \frac{g_{dn} Y_{11}^* / |Y_{21}|^2 + jC(g_{gn} g_{dn})^{1/2} / Y_{21}}{g_n} \quad (2.30)$$

where

Fig. 2.19. Representation of noisy FET by a noiseless FET, preceded by a noise network.

$$g_{gn} = \frac{\overline{i_g^2}}{4kT_o \Delta f}$$

$$g_{dn} = \frac{\overline{i_d^2}}{4kT_o \Delta f}$$

For a circuit designer, since the device details like doping channel thickness, etc. are not known, it is not possible to calculate both g_{dn} and g_{gn} . But they can be evaluated if the following assumptions are made^{18,23}:

(1) The value of the noise conductance g_{gn} is small compared to g_{dn} and the value of g_{gn} is unchanged with the variation of drain current. To illustrate, consider a FET with $L=2\mu m$, $a=0.2\mu m$, $Z=285\mu m$ and $N_D=10^{17} cm^{-3}$. For a diffusion constant (D) of $35 cm^2/sec$, g_{gn} has a typical variation 0.75 to 0.9m mho for a change in I_d/I_{dss} from 0.1 to 1 at 4GHz¹⁸. For the same FET and operating frequency, g_{dn} is typically above 40m mho.

(2) The conductance g_{dn} is a parameter which increases linearly with I_d/I_{dss} ¹⁸ and is a function of channel doping, channel thickness, channel length and gate bias. For the accurate calculation of g_{dn} , these parameter values are required.

(3) The correlation coefficient C is a fairly constant value and has a typical value range between 0.8 to 1 (for $1\mu m$, gate C approaches unity value over most of the current range) for the FET described in (1).

(4) It is assumed that the value of Y_{11} and Y_{21} are not effected significantly by neglecting C_{dg} .

(5) The parasitic resistance $R_s + R_g + R_i$ is adequately represented by the real part of Y_{11} .

Hence, all the parameters except g_{dn} are known in these equations, either from the manufacturer's data or by assumption.

The minimum noise figure F_o , optimum value of input resistance R_o and reactance X_o , for minimum noise figure, can be calculated using equation 18, 23:

$$R_o = \left((\text{Re } Z_c)^2 + \frac{r_n}{g_n} \right)^{1/2} \quad (2.31)$$

$$X_o = -\text{Im}(Z_c) \quad (2.32)$$

$$F_o = 1 + 2g_n(\text{Re } Z_c + R_o) \quad (2.33)$$

If the minimum noise figure specified by the manufacturer for a particular frequency and bias is known, the value of g_{dn} can be determined iteratively. Consequently, the parameter values R_o , X_o and F_o for other bias and frequency conditions can be evaluated.

The flow chart and the program 'NOISE' for calculating the R_o , X_o and F_o for various frequencies and current are shown in Appendix B. The results obtained are plotted in Figs. 2.16 and 2.18. It can be seen that both the measured and calculated values are in fairly good agreement.

The existing discrepancies may be either due to errors in the measurement of noise parameters or due to inconsistency between the parameters to be plotted and the F_o of the specific device under consideration.

2.7 Device Reliability

The GaAs FET³⁹ is a new device and one major concern for the circuit designer is device reliability. In currently available small signal GaAs FETs, several failure modes are present. They are:

- 1) Spike burn-out of the gate diode³⁸
- 2) Metal migration of ohmic contacts at high ambient temperature³⁸
- 3) Gradual degradation in drain current³⁹
- 4) Instability of characteristics³⁹

The occurrence of spike burn-out of the gate is due to either transient voltage spikes on the main supply or static discharge on handling. It is possible to reduce the occurrence of these failures by taking precautions in device handling and usage³⁸.

Just like in any other semiconductor devices, metal migration effects are observed in GaAs FETs at junction temperatures around 250°C and do not represent a serious hazard to high reliability usage. For optimum noise performance, FETs are normally biased to low drain current, which is beneficial to the device life since it reduces both the current density and junction temperature³⁸.

Life tests conducted in GaAs FETs show a gradual decrease of drain current I_{ds} , and it has been revealed that this is due to the increase of contact resistance in source and drain electrodes³⁹.

A drift in the useful properties of GaAs FETs, such as gain, noise figure and drain current, is observed when the device is turned on for operating conditions³⁹. Fig. 2.20 shows a bad example of such a drift where the drain current I_D , noise figure NF and associated gain Ga are varying against time. If the device is turned off, these parameters recover to their original value after some time. Obviously, such drift effects are undesirable in circuit applications. This phenomenon is closely related with the physical properties of the epitaxial layer, probably deep lying carrier trap centres at the interface between semi-insulating substrates and the active layer³⁹.

Mean-time to failure of FETs has been estimated to be about 10^7 hours for channel temperature of 80°C . This mean-time failure value is sufficiently high for most high reliability applications.

Fig. 2.20. An example of drift in the electrical parameters of GaAs FETs. ³⁹

CHAPTER 3

MICROSTRIP CIRCUIT ELEMENTS

3.1 Introduction

Advances in microwave integrated circuits have led to the widespread use of microstrip transmission line elements^{40,41,42}. The four basic requirements for the design of such elements are:

- 1) High quality substrate material
- 2) High definition pattern technology
- 3) Accurate design procedure for microstrip components
- 4) Availability of semiconductor devices in suitable packages which permit mounting on microstrip.

A good substrate material should have low loss, high degree of surface smoothness, high thermal conductivity, consistent uniformity and a fairly high value of dielectric constant. There are a few materials available with these properties, with alumina and sapphire heading the list^{41,46}. A 99.9% pure alumina has a loss tangent of 0.0002 and has a dielectric constant of 9.7 at 10GHz whereas sapphire has a tangent of 0.0001 and dielectric constant of 11 at 10GHz. The thermal conductivity of sapphire is twice that of alumina (0.2W/cm°C). But alumina is cheaper than sapphire and hence more popular. The conductor material is usually gold and it is produced by vacuum deposition or by electroplating. The typical specifications of a 99.5% alumina substrate are given in Table 3.1.

Table 3.1. Properties of TEK-WAVE substrates.

Material	Al_2O_3 99.5%
Thickness	0.025"±0.0025"
Surface finish	10 microinches
Dielectric constant	10.1±0.25
Metallization	Chrome-gold 2000A°, 250 microinches

The designer of microstrip circuits does not usually have the luxury of adjusting the circuits once they are fabricated. Therefore, the circuit design must be carefully carried out in order to eliminate the need for extensive post-fabrication alterations. It is thus important that the characteristics of the microstrip components are well understood. The following sections review the basic design equations of the microstrip elements and present some relevant experimental data.

3.2 The Basic Equations

The cross-section of a microstrip transmission line with the electric field distribution is shown in Fig. 3.1. As shown in the figure, line parameters are the strip width W , the substrate thickness H , the substrate dielectric constant ϵ_r , and conductor thickness t . At low frequencies ($t \ll \lambda$), most of the energy propagates in the dielectric below the strip conductor. The remainder of it is in a fringing field which extends in the air space above the dielectric. The presence of dielectric/air interface causes a discontinuity in the electric and magnetic fields. The discontinuity electric field at the interface implies surface charge. Under dynamic conditions, the electric and magnetic fields are modified so that both electric and magnetic fields are discontinuous at the dielectric air interface. Since there are components of both electric and magnetic fields in the direction of propagation, the propagation mode is not pure TEM.

Fig. 3.1. Electromagnetic field pattern in microstrips.

Three methods are commonly used for the analysis of microstrip transmission lines⁴². They are:

- 1) Method of conformal transformation
- 2) Relaxation method
- 3) Hybrid mode analysis.

The first two methods are based on a TEM mode which assumes that the dielectric thickness H is very small compared to the wavelength. The last method is more rigorous and considers non-TEM (hybrid) mode.

3.2.1 Characteristic Impedance and Effective Dielectric Constant

The conformal mapping technique for microstrip transmission line analysis was proposed by Wheeler⁴⁰, who derived the relationships for the phase velocity and the impedance of TEM microstrip propagation. This analysis was carried out for wide strips ($W/H \geq 1$) and for narrow strips ($W/H \leq 1$). The phase velocity V_{ph} in terms of the effective dielectric constant is given as^{41,44}:

$$V_{ph} = \frac{3 \times 10^{10}}{\sqrt{\epsilon_{eff}}} \quad (\text{cm/sec}) \quad (3.1)$$

where

$$\epsilon_{eff} = \frac{\epsilon_{r+1}}{2} + \frac{\epsilon_{r-1}}{2} \left(1 + \frac{10H}{W} \right)^{-1/2} \quad (3.2)$$

Since, in most of the design problems, one is interested in knowing the width of the line for a desired impedance, the implicit equations for deriving W/H in terms of impedance are given here⁴¹.

For $W/H \geq 1$

$$\begin{aligned} W/H \times \frac{\pi}{2} = & \left(\frac{377\pi}{2\sqrt{\epsilon_r} Z_0} \right) - \left(1 + \ln \left(\frac{377\pi}{\sqrt{\epsilon_r} Z_0} - 1 \right) \right) \\ & + \frac{\epsilon_r - 1}{2\epsilon_r} \left(\ln \left(\frac{377\pi}{2\sqrt{\epsilon_r} Z_0} - 1 \right) + 0.293 - \frac{0.517}{\epsilon_r} \right) \end{aligned} \quad (3.3a)$$

For $W/H \leq 1$

$$2H/W = \frac{1}{4} e^h - \frac{1}{2} e^{-h}$$

where

$$h = \left(\sqrt{\frac{\epsilon_r + 1}{2}} \times \frac{Z_0}{60} \right) + \frac{\epsilon_r - 1}{\epsilon_r + 1} (0.226 + 0.120/\epsilon_r) \quad (3.3b)$$

For operating frequencies above a certain frequency f_0 (Eqn. 2.4), the dispersion of non-TEM modes causes variation in the effective dielectric constant and phase velocity. The result of the dispersion studies by Jain⁵⁰ indicates that the dispersion is more pronounced for higher dielectric constant substrates, for thicker substrates and for wider lines. To illustrate, consider 25 ohms and 50 ohms lines in 0.025" thick alumina substrate ($\epsilon_r = 9.9$). For 50 ohms line, ϵ_{eff} varies between 6.9 and 7.2 for a frequency variation of 6 to 12GHz. Over the same range of frequency, ϵ_{eff} for 25 ohms line varies between 7.8 and 8.3. Jain showed both theoretically and experimentally that

$$f_o = \frac{6.0}{(\epsilon_r - 1)^{1/4}} \left(\frac{Z_o}{H} \right)^{1/2} \quad (3.4)$$

Let W' represent the effective width of the line due to finite thickness t of metallization⁴⁴; then,

$$W' = W + \Delta W$$

where

$$\Delta W = \frac{t}{W} \left(\ln \frac{2H}{t} + 1 \right) \quad (3.5)$$

Then, for frequencies $f > f_o$, the effective dielectric constant including dispersion is given by⁴³:

$$\epsilon_{eff} = 3 \times 10^6 (\epsilon_r^2 - 1) H \left(\frac{Z_o}{H} \right)^{1/2} (f - f_o) + \epsilon_{eff_o} \quad (3.6)$$

for

$$\frac{W'}{H} \leq 4$$

and

$$\epsilon_{eff} = 3 \times 10^{-6} (\epsilon_r^2 - 1) H \left(\frac{Z_o}{3} \left(\frac{W'}{H} \right)^2 \right)^{1/2} (f - f_o) + \epsilon_{eff_o} \quad (3.7)$$

for

$$\frac{W'}{H} \geq 4$$

In the above equation, f and f_o are given in GHz and H is given in mils.

The permittivity ϵ_r stated by the manufacturers is based on the measurement performed at 1.5KHz with capacitors printed on the substrate. The permittivity variations with respect to measured values at

1.5kHz of 99.5% alumina between DC to 10GHz is shown in Fig. 3.2⁴⁵.

The relative permittivity corresponding to operating frequency may be directly obtained from this graph if normalizing permittivity is known.

3.2.2 Losses in Microstrip

As in the case of other transmission lines, losses in microstrip are of two types: conductor losses and dielectric losses. The total loss per unit length of the line may be written as⁴²:

$$\alpha = \alpha_{c1} + \alpha_{c2} + \alpha_d$$

where α_{c1} and α_{c2} are the attenuation constants due to loss in the two conductors and α_d is due to dielectric loss in the substrate. α_c 's and α_d may be expressed in terms of the parameters of transmission line as:

$$\alpha_{c1} = r_1 / 2Z_0$$

$$\alpha_{c2} = r_2 / 2Z_0$$

and

$$\alpha_d = gZ_0 / 2$$

where r_1 and r_2 are the series resistances per unit length of ground plane and strip conductor, g is the shunt conductance per unit length and Z_0 is the characteristic impedance of the line.

Calculation of conductor loss α_c in microstrip is complicated because of the fact that the current distribution is not uniform across the width of the microstrip conductor. The current density at the edges

Fig. 3.2. Normalized permittivity against frequency for 99.5% alumina.

$$\text{Normalized permittivity} = \frac{\epsilon_r \text{ at operating frequency}}{\epsilon_r \text{ at 1.5kHz}}$$

of the strip is higher than that in the middle. The current distribution in the ground plane is also non-uniform. However, as a first order approximation, the current distribution in the microstrip ground plane can be equated to a uniform current which extends a substrate thickness H on each side of the centre strip's projection on the ground plane, as shown in Fig. 3.3. Thus;

$$r_1 = R_s / W$$

$$r_2 = R_s / (W + 2H)$$

where R_s is the surface resistivity in ohms per square. The resulting conductor loss $\alpha_c = \alpha_{c1} + \alpha_{c2}$ can be expressed as⁴⁶:

$$\alpha_c \text{ (dB}/\lambda_g) = 8.68 R_s \lambda_g f (W/H) \frac{\alpha_{CR}}{\alpha_{CO}} \pi \quad (3.8)$$

where

$$\lambda_g = \frac{\lambda_0}{\sqrt{\epsilon_{eff}}}$$

λ_0 = free space wavelength

f = frequency of operation

α_{CR} = the surface loss contribution because of surface roughness

α_{CO} = loss of smooth surface.

The ratio α_{CR}/α_{CO} is a function of both frequency and surface roughness and its value is typically between 1 and 1.8⁴⁶.

Fig. 3.3. The equivalent current distribution in microstrip.

The dielectric loss is simply related to the $\tan \delta$ of the substrate and the effective dielectric constant. Thus⁴⁶,

$$\alpha_d = (\text{dB}/\lambda_g) = 8.68 \frac{\epsilon_r}{\epsilon_{\text{eff}}} \frac{(\epsilon_{\text{eff}} - 1)}{(\epsilon_r - 1)} \tan \delta \quad (3.9)$$

This expression is relatively independent of frequency.

3.2.3 Microstrip End Effects

If a microstrip line is abruptly terminated, the end region will store considerably more accumulated charge than the remaining portion of the strip, due to fringe fields. Further, a measurable amount of energy will be radiated from this edge. Consequently, the open circuit end represents a parallel RC termination, where the resistive component accounts for the radiated energy, and capacitive components represent extra charges at the open end of the strip. The published results indicate that capacitive part of the open end effect is the predominant component of the two^{43,51,47}.

The open terminations have been modelled as pure equivalent capacitance or a length of transmission line which corresponds to that capacitance. The latter model seems to be preferable since it provides the correction length for end effects. In both cases, the edge capacitance is calculated by obtaining the capacitance for a finite section of the line, using matrix methods³³ or by the successive image technique⁴⁷, and subtracting from it the contribution of uniform line. The latter is

equal to the line capacitance per unit length multiplied by the length of the line. This excess capacitance, which is associated with the fringe effects, is then converted to equivalent length. These analytical methods are not often convenient for microstrip circuit design and hence the following empirical equations are used for end correction⁵⁰.

$$\Delta l = \frac{1}{K} \arccot \left[\frac{4C+2W}{C+2W} \cot(K_c) \right] \quad (3.10)$$

where

Δl = the apparent increase in length of the microstrip due to end effect

$$K = 2\pi/\lambda_g$$

$$C = 2H \ln(2/\pi)$$

Use of such an end correction is usually limited to stubs or resonators which are longer than at least two times the substrate thickness⁵¹.

In his equation for the characteristic impedance for wide lines, Wheeler used the expression $(H \ln 4)/\pi$ for edge correction of wide lines ($W/H \geq 1$) in order to account for the difference in characteristic impedance for narrow and wide lines, at $W/H=1$. Later, it was shown that the same empirical relations used to describe the open end effect

(Eqn. 3.10) could be used in Wheeler's general expression for the characteristic impedance of a wide line. It was demonstrated with this modification that the wide line approximation is valid over a much larger range of W/H ($1 \leq W/H \leq 20$) and that the distinct cross-over between wide

and narrow lines occur at $W/H=1$.

Hence, for $W/H > 1$ and $t < H/30$, the width correction is given by:

$$W = 1/K \arccot \left(\frac{4C+2W}{C+2W} \cot(KC) \right) \quad (3.11)$$

where

$$K = 2\pi/\lambda_g$$

and

$$C = 2H \ln(2/\pi)$$

for $1 \leq W/H \leq 3.5$ the value of W to be used in Eqn. 3.11 is derived using Eqn. 3.3b, whereas for $3.5 \leq W/H \leq 20$, the required value of W for Eqn. 3.11 is obtained using Eqn. 3.3a. These results have been experimentally verified⁵⁰ using alumina microstrips. If the condition ($t < H/30$) is not satisfied, the width correction defined by Eqn. 3.5 is applied before using Eqn. 3.11.

3.2.4 Interstage Coupling and Biasing Arrangement

Microwave amplifiers may be cascaded using D.C. or A.C. coupling. The D.C. coupling has the advantage in eliminating one planar bias network and the chip capacitor. It also allows reduced interstage separation⁵². But it necessitates the isolation of the source of the second FET from ground. Such source mounting with minimum parasitics is quite difficult to realize and hence A.C. coupling with chip capacitors or interdigitated capacitors is more practical. Below X-band, chip or deposited capacitors can be considered as lumped elements, but through

X-band, they become distributed elements and may introduce unwanted parasitics. Hence, interdigitated capacitors are used at X-band and above⁵³.

Three broadband bias structures in common use are illustrated in Fig. 3.4³². They are formed by combining high impedance (Z_g), $\lambda/4$ sections with low impedance $\lambda/4$ sections of different geometries. Points A are RF open circuits and points B are RF short circuits, at the central frequency for which they are designed. Syrett³² studied these configurations experimentally at X-band and showed all these structures have reflection coefficients near unity and that the half-moon bias structure is superior since it provides minimum change of phase for RF transmission. To feed the supply, a high impedance line is connected to the junction of two impedances as shown in Fig. 3.4. The studies also showed that the half-moon acts as an effective broadband short at radius (r) which is 35% less than a quarter wavelength. Fig. 3.5 shows the broadband reflection properties of a half-moon bias structure with $Z_g=50$ ohms and $r=0.65 \lambda_g/4$ around 3.75GHz.

A higher value of impedance Z_g is usually selected to reduce the insertion loss caused by this biasing network, to any active circuit to which it is connected. Hence, due to the minimum insertion loss and broadband reflection properties, it can be assumed that the performance alteration produced by this half-moon structure will be minimal.

(a)

(b)

(c)

Fig. 3.4 .. Examples of broadband bias lines currently in use.

- a) Bias line using $\lambda/2$ sections.
- b) Bias line with a quarter circle section.
- c) Bias line with half moon structure.

Fig. 3.5. Smith chart plot of impedance of half moon structure with $\ell = \lambda/4$, 50 ohm transmission line and $r = 0.65\lambda/4$.

3.3 Impedance Discontinuities

In the design of circuits using quarter wave transformers or series matching sections, the characterization of abrupt impedance discontinuities has always been a problem. Recently, several studies on the characterization of such discontinuities have been reported^{54,55,56}. These discontinuities are modelled by equivalent circuits containing one or a few reactive elements⁵⁴ or a short length of idealized transmission line⁵⁵ or a transmission line junction model⁵⁶ as shown in Fig. 3.6.

Let the 'step ratio' be defined as the ratio of the width W_1 corresponding to low impedance Z_{01} to the width W_2 as shown in Fig. 3.6a. As the step ratio is increased, the discontinuity capacitance, the inductive effect and the equivalent length also increases (Figs. 3.6b and 3.6c). In these cases, the discontinuity capacitance may be evaluated either by analytical methods^{33,47,55} or by using empirical relations⁵⁰. Following the latter method, the equivalent length corresponding to discontinuity capacitance is given by:

$$\Delta L = C \left(\frac{C+2W}{4C+2W} \right) \quad (3.12)$$

where

W = effective line width ($W_1 - W_2$)

$C = H \ln 4/\pi$

The measurement procedure suggested in reference⁵⁴, to determine the discontinuity impedance, assumes a prior knowledge of the error model for microstrip to coaxial transitions. But characterization of

(a)

(b)

(c)

(d)

Fig. 3.6. Equivalent models of abrupt discontinuities.
 a) An abrupt impedance step.
 b) Equivalent circuit with discontinuity inductance.
 c) Model with equivalent length.
 d) Transmission line junction model.

the abrupt discontinuity using resonant method is more direct since errors due to such transitions are reduced considerably⁵⁷.

Using the resonance method, the element values of the abrupt discontinuity models were obtained for various step ratios. This was necessary to verify the empirical equations which were developed for the experimental data at X-band and to confirm their validity at 3.75GHz. Fig. 3.7 shows the experimental setup for measuring the reflection properties of a $\lambda_g/2$ low impedance line with a step ratio of 10, the reference line and the results.

The measurement showed a resonance frequency shift from 3.75 to 3.12GHz for the resonant structure designed for 3.75GHz. This shift is attributed to the increase in the length due to discontinuity capacitance and also due to the change in frequency provided by the discontinuity inductance (Fig. 3.6). If the shift in frequency corresponding to discontinuity capacitance is accounted for using the formula presented in Eqn. 3.12, the resulting difference in frequency is attributed to the inductance effect. For the step ratio 10 on alumina, this inductive reactance is 6.5 ohms at 3.75GHz.

The empirical formula used for calculating the inductive reactance of the impedance step (Fig. 3.6b) is given by⁵⁴:

$$\omega L = \frac{2Z_0 W_1}{\lambda_g} \ln \left[\operatorname{cosec} \left(\frac{\pi}{2} \frac{W_2}{W_1} \right) \right] \quad (3.13)$$

where

ωL = impedance discontinuity series reactance

Fig. 3.7. Reflection measurements on $\lambda/2$ long line on alumina with a step ratio (w_1/w_2) of 18. Reference line of width w_2 (0.024") corresponding to 50 ohms and the resonant line are also shown in the figure. The designated $\lambda_{g/4}$ corresponds to 3.75GHz.

Z_{01} = characteristic impedance of the low impedance side

W_n^* = equivalent strip width ($n=1, L$)

$$= \frac{H R_c}{Z_{0n}} \left(\frac{1}{\epsilon_{eff}} \right)^{1/2} \text{ for } (n=1, 2)$$

R_c = free space wave impedance

H = substrate thickness

Z_{02} = characteristic impedance of high impedance side of discontinuity

Substituting the parameters of alumina microstrip in Eqn. 3.13, we get ωL as 7.72 ohms at 3.75GHz for a step ratio 10 and $Z_{02}=50$ ohms.

The difference in the measured and calculated values of the inductive reactance is small and it may be attributed to the error caused by the variation in the dielectric constant of the substrate and the variation in the thickness of the dielectric. The experiments were repeated for step ratios of 6 and 8 and similar agreements were obtained. The above measurements reveal that even though the frequency of operation is of the order of a few GHz, the inductive reactance can still be predominant if the step ratio is greater than 2.5³³.

A compensation for the discontinuity inductance can be provided either by incorporating the inductance in the actual analysis program of the circuit or by providing compensation for it in the final circuit. The latter method is more practical. Let $\Delta \ell'$ correspond to the inductive reactance and ℓ the length of the low impedance line, then the correction

angle is:

$$\phi = \left(\frac{\Delta \ell'}{\ell} \right) 360^\circ \quad (3.14)$$

In the experiment described above, ℓ corresponds to $\lambda_g/2$ at 3.75GHz. In Fig. 3.8, the correction angle is plotted as a function of W_1/W_2 for alumina microstrip. It is interesting to note that above the step ratio of 2.5 the correction angle can be expressed as:

$$\phi = 1.5 W_1/W_2 \quad (3.15)$$

The discontinuity effects can also be modelled as a series transmission line of finite length, impedance and attenuation⁵⁶ as shown in Fig. 3.3d. But more analytical information is required to use this model in circuit analysis.

3.4 Bend in Microstrip Line

Quite frequently in the design of microstrip circuits, it becomes necessary to insert bends in microstrip line in order to allow a convenient routing of the microstrip. Unfortunately, the bends constitute a discontinuity and it may produce sufficient mismatch and phase change to alter the performance of the microstrip structure. To date, only very limited results on microstrip bends have been reported and they are limited to right angled bends^{58,59}.

As in the case of step discontinuity, two types of equivalent circuits, for the bends, are in use. Both types use a T network with a capacitance in shunt, representing the additional capacitance associated

Fig. 3.8. A plot of correction angle as a function of step ratio.

2

OF/DE

4

with the bend. The series elements are represented either as discontinuity inductance^{59,61} or equivalent line lengths⁵⁸. To reduce the mismatch, the surface area of the corner is normally reduced by 'mitering' or 'matching'. Experimental results show⁶⁰ that for minimum VSWR the ratio of W/W_0 is 1.5 where W and W_0 are shown in Fig. 3.8. The results of the reflection and transmission measurements conducted on 50 ohm lines (on 99.5% alumina with $H=0.025''$) for $W/W_0=1.6$ (Fig. 3.9) show that the maximum VSWR is 1.16, attenuation is less than 0.2dB and correction angle is less than 1.2° . The bend was found to have quite broadband transmission properties as expected. Horton⁵⁸ reports a correction angle of less than 1° at $W/H=1$ for alumina microstrip of thickness 0.025". Since the effect of mitering is seen to increase the electrical length, the result obtained seems justifiable.

Since no information on 60° bend is available, reflection measurements for different percentage of mitre of 60° bend on 50 ohm lines were taken and they are plotted in Fig. 3.10. It can be seen that optimum value of mitre is around 40% which gives a VSWR of 1.16. Theoretically it should be possible to get a VSWR of one at the optimum mitre. Practically such VSWR values are difficult to obtain due to errors caused by launchers, 50 ohm lines and terminations. The transmission measurement conducted on 40% mitre line is plotted in Fig. 3.11. It shows that the bend has broadband transmission properties and that the correction angle is less than 1.2° .

Fig. 3.9. Transmission measurement on 90° bend.
(99.5% alumina, $H=0.025''$, $w_0=0.025''$)

Fig. 3.10. A plot of % mitre versus VSWR for 60° bends.

Fig. 3.11. Transmission measurement on 60° bend for 50 ohm lines on 99.5% alumina and $H=0.025''$.

3.5 The Tolerance of Microstrip Circuits

For an accurate realization of microstrip circuits, the following factors are to be considered in the design.

(1) Variation in the dielectric constant ϵ_r of the substrate:

The variations in dielectric constant ϵ_r lead to the impedance variations of microstrip lines. From the properties of the substrate given in Table 3.1 and from Fig. 3.2, a permittivity variation of 9.63 to 10.12 is expected for the alumina substrate used for circuit fabrication. Thus, for $W/H=1$, the impedance may vary $\pm 2.5\%$ with respect to the design impedance.

(2) Variation of substrate thickness (H):

The variation in substrate thickness also leads to the impedance variations. The data shown in Table 3.1 reveals that the thickness of the dielectric substrate may vary $\pm 10\%$ from the rated value of 0.025". Since the impedance is a function of (W/H) , a variation as high as $\pm 15\%$ in the designed impedance may be anticipated.

(3) Changes in surface finish:

The surface finish of the microstrip is important with respect to line definition and conductor attenuation. For illustration, the attenuation for 2 micro-inches finish alumina is about 35% less than that for 24 micro-inches finish and the smallest available line width varies between 0.001" and 0.006" for the two finishes.

Further changes in the dimensions of the microstrip line can also be expected due to non-homogeneity of a given dielectric substrate, non-uniformity of conductor thickness and also due to bad etching.

3.6 A Program for Calculating the Microstrip Circuit Elements

The program 'DIMENSION' was developed for calculating the dimensions of microstrip circuit elements on alumina for various types of circuit elements of prescribed performance. The need for such a program stemmed from the fact that it is always difficult to read the required data accurately from a chart and that the discontinuity correction becomes meaningless unless the element values are calculated accurately.

The main program reads the data, calls the subroutine 'PARA', and prints out the dimensions of the elements in inches. The subroutine calculates the width and length of the elements and provides the necessary corrections for discontinuities and end effects. The details of the program, flow chart and a program print out are included in Appendix B.

Apart from computing the dimensions of the circuit, the program could be used for finding the data such as the variation ϵ_{eff} with frequency, the variation of λ_g with line impedance Z_0 , etc. Fig. 3.12 shows a plot of wavelength λ_g as a function of line impedance for alumina substrates.

Fig. 3.12. A plot of the wavelength λ_g as a function of characteristic impedance Z_0 for alumina substrate.

CHAPTER 4

FET AMPLIFIER-DESIGN METHODS

4.1 Introduction

It has been stated earlier that the GaAs field effect transistors have low noise figure with high gain and large dynamic range. The successful realization of several FET amplifiers has been reported and they represent different design procedures, to suit individual device capabilities. The first section of this Chapter is concerned with the specifications of low noise satellite amplifiers and the amplifier design procedures which are currently in use. This is followed by a review of the limitations of conventional design procedures and the advantages of computer-aided methods.

4.2 Definitions

In a typical microwave amplifier specification, the required performance is expressed in terms such as intercept point, group delay, dynamic range, and compression point in addition to the more familiar gain and noise figure terminology. This section defines these terms and explains why they are important in the amplifier design.

4.2.1 Intercept Point⁶²

The intermodulation noise of any amplifier is caused by non-linear input/output characteristics and it may result in many different types of interference, all of which are in some way signal dependent.

To study the nature of these interferences, a brief mathematical analysis is presented.

The non-linear input/output equation can be expressed as a power series, having an infinite number of terms. Usually, the terms higher than the third order are small enough to be ignored, and the equation for output may be written as:

$$e_o = K_0 + K_1 e_i + K_2 e_i^2 + K_3 e_i^3 \quad (4.1)$$

where K_0 , K_1 , K_2 , K_3 are constant coefficients.

Consider the input signals:

$$e_i = a_0 + a_1 \cos(\omega_1 t) + a_2 \cos(\omega_2 t) \quad (4.2)$$

Substituting Eqn. (4.2) in (4.1) and expanding, the following terms are obtained:

Fundamental:

$$K_1 a_1 \cos 2\pi f_1 t \quad (4.3)$$

$$K_1 a_2 \cos 2\pi f_2 t$$

Second order:

$$K_2 a_1 a_2 \cos 2\pi (f_1 \pm f_2) t$$

$$(1/2) K_2 a_1^2 \cos 2\pi (2f_1) t \quad (4.4)$$

$$(1/2) K_2 a_2^2 \cos 2\pi (2f_2) t$$

Third order:

$$(3/4) K_3 a_1^2 a_2 \cos 2\pi (2f_1 \pm f_2) t$$

$$(3/4) K_3 a_1 a_2^2 \cos 2\pi (2f_2 \pm f_1) t \quad (4.5)$$

This partial list of terms reveals that:

1. The fundamental responses are directly proportional to the level of the input signals.
2. The second order responses are proportional to the square of the input amplitude.
3. The third order responses are proportional to the cube of the input amplitude.

Hence, it can be concluded that a plot of each response, on a dB scale, will be a straight line with a slope corresponding to the order of response, as shown in Fig. 4.1. It is therefore sufficient if we know the order of the response and its magnitude at one point alone, in order to be able to plot the level of each response.

That point at which the fundamental response and the third order spurious response intercept is used as a reference is called the "intercept point".

The reason for selecting the interception of the fundamental and the third order signals is that the third order intermodulation product is generally the one that poses the most serious problem in cases where the bandwidth of the device under consideration is less than an octave. In addition, it transpires that the second order plot intercepts the fundamental at the same point as the third order, except in some special cases⁶².

Fig. 4.1. A plot of output responses for calculating intermodulation products. (c represents 1dB compression point)

4.2.2 Group Delay⁶³

Envelope delay or group delay, commonly used in describing and measuring the phase characteristics of a system, is defined in terms of the slope of the phase/frequency characteristics. As shown in Fig. 4.2, group delay $t_d = d\phi/d\omega$ seconds, where $d\phi$ is the change in the phase of the transmitted signals corresponding to a small frequency difference $d\omega$.

The group delay, corresponding to the phase characteristics, is shown by the dotted curve and for the case illustrated, it varies with frequency. If a signal containing components throughout the frequency band shown is divided into a set of narrow band signals, each of these will be subjected to a different group delay in passing through the channel. The output signal must therefore have a different waveform from the input and distortion appears. The difference between the maximum and minimum value of the group delay over the prescribed operating frequency band is called the differential group delay and it provides a convenient numerical measure of the group delay distortion. The necessary condition for the absence of the group delay distortion is that group delay should be constant throughout the passband.

4.2.3 Dynamic Range⁶⁴

Dynamic range can be defined as the range of variation of the input signal over which the amplifier can perform its function effectively. The degree to which this is accomplished depends on the nature of the input signal. For a single frequency input signal, the dynamic

Fig. 4.2. - Phase and group delay variation of a system with frequency ω .

range is obtained as the difference between input signal level which produces saturation in the amplifier and the minimum input signal which can be discerned above the system noise of the amplifier. This system noise is equal to the thermal noise over the effective bandwidth, KT_0B , plus the noise generated within the amplifier. When multiple signals are applied, the above definition for dynamic range is not appropriate, since spurious signals generated within the amplifier will appear as false detectable signals at the output before the input power level reaches the value corresponding to 1dB compression. In this case, it is more appropriate to define the largest input signal allowable as that input where third order intermodulation products just begin to exceed the noise level, as shown by A in Fig. 4.1.

4.2.4 Compression Point

Fig. 4.1 shows a plot of output power in dBm as a function of input power in dBm. At higher input levels, the output power saturates and gain decreases. The power output corresponding to a decrease in gain of 1dB is termed as output power at 1dB compression⁶⁴ and it is plotted in Fig. 4.1 as point C. The output power of the linear amplifiers usually referred to the 1dB compression point.

4.2.5 Gain Slope

Fig. 4.3a shows a typical amplitude frequency curve of an amplifier. The presence of the ripple in the amplitude response curve is equivalent to the effect of echo on a flat amplitude/frequency char-

(a)

(b)

Fig. 4.3. A plot showing the multipath effect.
 a) Amplitude characteristics of channel with multipath effect.
 b) Phasor diagram for multipath effect.

acteristics of the amplifier. The term echo refers to a signal produced by reflection at one or more points in a transmission path. It is also generated by transmission irregularities, having sufficient magnitude and time difference, perceived as distinct from the signal received over the primary transmission path and it may be represented by the phasor shown in Fig. 4.3b. If the signal in the second path is weaker than that in the direct path and if it is delayed by Δt , the frequency difference between ripple maxima in the overall transmission characteristic is $1/\Delta t$. For satellite amplifiers, the gain slope is specified as 0.01dB/MHz from consideration of the echo type distortion^{63,65}.

4.3 Amplifier Specifications

The typical specifications of Watkins-Johnson FET amplifier for COMSAT is given in Table 4.1⁶⁵. The amplifier works in the satellite frequency range 5.9 to 6.4GHz and has a gain of 30dB. The amplifier noise figure is 4dB at an input VSWR of 1.2. A balanced amplifier configuration with low noise FETs (2.5dB) provides improvement in VSWR and noise figure at the same time. The gain slope is 0.01dB/MHz as described in the previous Section. The satellite system has a typical group delay specification of 20nSec. (peak to peak variation)⁶⁶. Since the group delay variation of the filters used is about 19nSec, the amplifier specification for group delay variation is limited to 1nSec. The intercept point is typically +20dBm. The specifications for the power output at 1dB compression point, the noise figure, gain and gain flatness are

Table 4.1. COMSAT FET amplifier test data.

1. Frequency operating range	5.9-6.4GHz
2. Amplifier gain	30dB (min.)
3. Gain variation	1dB (peak to peak)
4. Noise figure	4dB (max.)
5. Input/output VSWR	1.20:1
6. Gain slope	0.01dB/MHz
7. The third order intermodulation products at minimum detectable noise level	50dB below carrier
8. Group delay variation	1nSec
9. Power output at 1dB compression point	+6dBm
10. Power requirements	720mW

are dictated by the satellite system in which the amplifier is used.

4.4 Amplifier Design Using Graphical Methods

The basic problem in the design of broadband transistor amplifiers is the synthesis of suitable input and output matching networks to meet the desired specifications. The realization of such matching networks is accomplished either by graphical methods using Smith charts or by computer-aided methods. This Section deals with the graphical design procedure of amplifiers using Smith Charts, with the necessary theoretical background, leading to the concept of stability, gain and noise figure circles.

4.4.1 Transducer Power Gain^{67,68}

In the design of the amplifier, power gain is considered to be the most important factor. The transducer power gain is defined as the power delivered to the load divided by the power available from the source and it is derived as:

$$G_T = \frac{|S_{21}|^2 (1 - |r_1|^2) (1 - |r_2|^2)}{|(1 - S_{11}r_1)(1 - S_{22}r_2) - S_{12}S_{21}r_1r_2|^2} \quad (4.6)$$

where the reflection coefficient r_i

$$r_i = \frac{Z_i - Z_0}{Z_i + Z_0}, \quad i=1,2 \quad (4.7)$$

If we assume the network is unilateral, then the unilateral transducer gain is given by:

$$G_{TU} = |S_{21}|^2 \times \frac{(1-|r_1|^2)}{|1-S_{11}r_1|^2} \times \frac{(1-|r_2|^2)}{|1-S_{22}r_2|^2} \quad (4.8)$$

$$= G_o \times G_1 \times G_2$$

Maximum unilateral transducer gain is where $r_2 = S_{22}^*$, $r_1 = S_{11}^*$ and S_{11} and $S_{22} < 1$. Then,

$$G_U = \frac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)} \quad (4.9)$$

$$= G_o \times G_{1max} \times G_{2max}$$

where

$$G_{imax} = \frac{1}{1-|S_{ii}|^2}, \quad i=1,2 \quad (4.10)$$

4.4.2 Constant Gain Circles^{67,68}

It can be seen from Eqn. (4.8) that for the case in which S_{ii} is less than 1 and G_i constant, r_i is an equation of a circle on the Smith chart. The centre of these constant gain circles is on a line between the centre of Smith's chart and point representing S_{ii}^* , at radius C_i from the centre of the Smith chart, where

$$C_i = \frac{g_i |S_{ii}|}{1-|S_{ii}|^2(1-g_i)} \quad (4.11)$$

The radius of the gain circle is:

$$r_1 = \frac{\sqrt{1-g_i}(1-|S_{ii}|^2)}{1-|S_{ii}|^2(1-g_i)} \quad (4.12)$$

where

$$g_i = \frac{G_i}{G_{i \max}} = G_i(1-S_{ii}^2) \quad , i=1,2 \quad (4.13)$$

4.4.3 Stability Considerations^{67,68}

Stability is one of the most important parameters in the amplifier design and is determined from the S-parameters and the synthesized source and load impedances. Oscillations are only possible if either the input or the output point or both have negative resistance. This occurs if S_{11} or S_{22} is greater than unity. However, even with a negative resistance, the amplifier might still be stable.

For a device to be unconditionally stable, three conditions need to be satisfied. They are:

$$\begin{aligned} (a) \quad & |S_{11}| < 1 \\ (b) \quad & |S_{22}| < 1 \end{aligned} \quad (4.14)$$

and the transistor inherent stability factor K must be greater than unity.

Where

$$(c) \quad K = \frac{1+|\Delta|^2-|S_{11}|^2-|S_{22}|^2}{2|S_{12}S_{21}|} \quad (4.15)$$

and

$$\Delta = S_{11}S_{22} - S_{12}S_{21}$$

For finding the stability of the amplifier, the above conditions apply but the S-parameter will then be the overall S-parameters of the amplifier.

$K \geq 1$ ensures stability, although values of the K near 1 sometimes make transistors very sensitive to parameter changes.

4.4.4 Stability Circles^{67,68}

Stability circles can be plotted directly on a Smith chart which separate the input and output planes to stable and potentially unstable regions. Stability circles plotted on the output plane indicate the value of all the loads that provide negative real input impedance, thereby causing circuits to oscillate. A similar circle can be plotted for the input plane which indicates the value of the loads that provide negative real output impedances and again cause oscillations.

These regions of instability occur within the circles whose centres and radii are expressed by:

$$\text{Centre of the input plane} = C_{S_1} = \frac{C_1^*}{|S_{11}|^2 - |\Delta|^2} \quad (4.16)$$

$$\text{Radius of the input plane} = r_{S_1} = \left| \frac{|S_{12}S_{21}|}{|S_{11}|^2 - |\Delta|^2} \right| \quad (4.17)$$

$$\text{Centre of the output plane} = C_{S_2} = \frac{C_2^*}{|S_{22}|^2 - |\Delta|^2} \quad (4.18)$$

$$\text{Radius of the output plane, } r_{S_2} = \left| \frac{|S_{21}S_{12}|}{|S_{22}|^2 - |\Delta|^2} \right| \quad (4.19)$$

where

$$C_1 = S_{11} - \Delta S_{22}^*$$

$$C_2 = S_{22} - \Delta S_{11}^*$$

and

$$\Delta = S_{11}S_{22} - S_{12}S_{21}$$

If K is greater than unity, the maximum power gain possible is found from the relationship:

$$G_{\max} = \frac{|S_{21}|}{|S_{12}|} |K - \sqrt{K^2 - 1}| \quad (4.20)$$

4.4.5 Noise Figure^{68,69}

The noise figure and associated noise parameters were defined in Chapter 2, where the noise figure (ratio) of linear two-port is expressed by:

$$F = F_o + \frac{R_n}{G_s} [(G_s - G_o)^2 + (B_s - B_o)^2] \quad (4.21)$$

Hence,

$$F - F_o = \frac{R_n}{G_s} [(G_s - G_o)^2 + (B_s - B_o)^2] \quad (4.22)$$

If we now express Y_s and Y_o in terms of the reflection coefficients and substitute them in the expression (4.22), we get:

$$F - F_0 = 4R_n \frac{|\Gamma_s - \Gamma_0|^2}{(1 - |\Gamma_s|^2)(1 + |\Gamma_0|^2)} \quad (4.23)$$

where

$$Y_s = \frac{1 - \Gamma_s}{1 + \Gamma_s}$$

and

$$Y_0 = \frac{1 - \Gamma_0}{1 + \Gamma_0}$$

Equation (4.23) has the form of a circle. For a noise figure F the solution for Γ_s will be on a circle. The equation for the circle can be found, provided the parameters F_0 , Y_0 and R_n are given.

4.4.6 Noise Figure Circles^{68,69}

To determine a family of noise figure circles, let us first define a noise figure parameter N_i .

$$N_i = \frac{F_i - F_0}{4R_n} |1 + \Gamma_0|^2 \quad (4.24)$$

where the noise figure F_i defines the desired noise figure circle. Once the value of N_i is calculated, the centre and radius of the circle can be determined by:

$$C_{Fi} = \frac{\Gamma_0}{1 + N_i} \quad (4.25)$$

$$R_{Fi} = \frac{1}{N_i + 1} \sqrt{N_i^2 + N_i(1 - |\Gamma_0|^2)}$$

From these equations, we see that $N_i = 0$ where $F_i = F_0$ and the centre of the F_0 circle with zero radius is located at Γ_0 on the Smith chart.

The centres of other noise figure circles lie along the Γ_0 vector.

4.5 Broadband Amplifier Design Using Graphical Procedure

The goal of the designer of low noise solid state amplifiers is to realize the lowest possible noise figure while still meeting other performance objectives placed on the amplifier. To accomplish this in a logical manner, one must carry out each of the tasks in the flow chart, given in Fig. 4.4.

The first procedure is to obtain the value of the S-parameter and noise parameters of the transistors, either from the manufacturer's data sheet or by measurements. The stability factor defined by Eqn. (4.15) is directly calculated, since both S_{11} and S_{22} are usually less than one. If the device is conditionally stable at the frequency desired, stability circles are plotted on the Smith chart, both for input and output planes. This determines the selection of impedance for stable operation of the amplifier. To select the source impedance, both constant gain circles and constant noise figure circles are plotted on the same Smith chart. The resulting plot clearly indicates the trade-off between gain and noise figure, that has to be made in the design of low noise stages. In general, as explained in the second Chapter, the maximum gain and minimum noise figures cannot be obtained simultaneously. The relative importance of these two objectives will dictate the compromise. If the selected values

Fig. 4.4a. A flow chart for the graphical procedure for broadband amplifier design. ,

Fig. 4.4b. A flow chart for the graphical procedure for broadband amplifier design.

are in the unstable region, a new value of Z_1 may have to be selected. Similarly, the output impedance Z_2 is selected from the plot of stability and gain circles. Since the graphical design yields unilateral gain only, the transducer gain is calculated and performance deviation is determined. If the gain deviates much, the procedure of selection is repeated for the optimum performance.

Instead of plotting gain and noise figure circles, Eilseberg recommends⁷⁰ the use of constant noise measure circles, where the noise measure

$$M = \frac{NF-1}{1-1/G_a} \quad (4.26)$$

where G_a is the available gain. Noise measure is a convenient indicator of device noise performance and is invariant for a cascade of identical stages.

Mvungi⁷¹ suggests the use of several constant gain circles, representing several sample frequency points within the bandwidth of the amplifier. Loci of both source and load impedances are taken judiciously such that any combination of source and load impedance loci gives a constant gain with uncertain limits at all the frequency sample points.

The advantage of the graphical procedure is that it provides an excellent understanding of the device capabilities and limitations, for a particular application. The procedure is limited by the fact that the transistors are not unilateral devices and that the amplifiers may have to

meet many other specifications other than noise figure, gain and stability. Nevertheless, this procedure gives the basic data for computer-aided procedure which is described in the next Section.

4.6 Computer-Aided Design Methods

Over the last two decades, digital computers have been utilized as a tool in the analysis and synthesis of complex microwave networks. The computer-aided design has evolved, primarily to provide an accurate and rapid means to solve numerous circuit problems which are far too complex to be handled by means of the Smith chart. Used in conjunction with an efficient circuit configuration and device and microstrip characterization data, a circuit analysis program can provide the designer with an efficient means of working out a satisfactory circuit design.

Several two-port cascading analysis programs based on chain matrix and transfer scattering matrix are in use. These matrices are defined as follows.

Consider a 'black box' circuit representation with the direction of voltages and currents as indicated in Fig. 4.5. A set of linear equations that completely describes this two-port network is given by:

$$V_1 = AV_2 + B(-I_2)$$

$$I_1 = CV_2 + D(-I_2)$$

This may be represented in matrix form.

Fig. 4.5. Chain matrix $[ABCD]$ representation for a two-port network.

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \quad (4.27)$$

This matrix ABCD is known as the chain matrix.

Also consider Fig. 2.8. Representing the input port waves as a function of output port waves, we get:

$$b_1 = T_{11}a_2 + T_{12}b_2$$

$$a_1 = T_{21}a_2 + T_{22}b_2$$

In the matrix form, the above equation reduces to:

$$\begin{bmatrix} b_1 \\ a_1 \end{bmatrix} = \begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} \begin{bmatrix} a_2 \\ b_2 \end{bmatrix} \quad (4.28)$$

where T is known as the transfer scattering matrix.

Chain and transfer scattering matrices have similar cascading properties and both require the transfer of measured S-parameters to the corresponding parameters for analysis. Hence, they may be used with equal effectiveness in microwave circuit analysis programs.

Optimization subroutines form an important part of computer-aided design programs. In mathematical terms, optimization may be defined as a search process to find the optimum value of a specified function, by

controlled variation of the parameters upon which the function depends.

In practical terms, this means formulation of some function, which gives some measure of 'error' in the design objective. Then, repeatedly changing the component values, upon which the function depends, in a proper direction, a final value is achieved which satisfies the predetermined condition of excellence. One of the most commonly used error criterion is the so-called the mean squared error criterion and for the frequency domain operation the error function (also known as the objective function) may be written as:

$$E_{\text{error}} = K_1 \sum_{f_1}^{f_m} (\text{Objective}_1 - Y_1)^2 + \dots \dots \dots (4.29)$$

$$+ K_N \sum_{f_1}^{f_m} (\text{Objective}_N - Y_N)^2$$

where $K_1 \dots K_N$ are known as the weighting factors
and Y_N is the design variable.

It is quite possible that error function may have more than one minimum. The value of the error function which is least among various minima is known as the global minimum and the others are called local minima. Fig. 4.5a illustrates a surface which represents an error function with local and global minima. A large number of optimization techniques are currently in use with microwave computer-aided design programs¹¹. In this Section, a few of the important ones are briefly

discussed under two headings; namely, search and gradient methods.

(a) Search methods

Normally, these are the techniques which do not require the calculation of gradients; rather they depend on function evaluations at various combinations of the variables. A few of the important techniques in search method are the grid, the random and the pattern search^{7,72,8}. The least sophisticated method among them is the grid search⁷², where the value of the objective function is calculated at each grid point (Fig. 4.6a) and it is compared with the least value found before. If it is less than this least value, it replaces the former and is retained. If it is greater, it is rejected. The process has the advantage that it may find the least value of the function or the global minimum however irregular the function may be, provided the separation between grid is small. Usually, this result is attained at the expense of large computation time.

In random search method^{72,73}, the function is evaluated at points selected at random by a digital computer. After a sufficiently large number of such function evaluations have been performed, the least value is taken as the desired minimum. The random search is usually faster than the grid search and, in most cases, the final value is likely to represent a local minimum.

In pattern search, two strategies⁷, known as exploratory moves and pattern moves, are used alternately. Fig. 4.6b shows an example of

Fig. 4.6. Plots for illustrating the grid search (a) and pattern search (b).
A represents a local minima and B the global minimum.

pattern search strategy. The starting point p_1 is the first base point b_1 . In the example, the first exploratory move from b_1 begins by incrementing x and resulting in p_2 . Since the objective function $f_2 < f_1$, p_2 is retained and exploration is continued by incrementing y . Since $f_3 < f_2$, p_3 is retained in place of p_2 . The first set of exploratory moves being complete, p_3 becomes the second base point b_2 . A pattern move is now made to p_4 , with a step size $(2b_2 - b_1)$ in the direction of $(b_2 - b_1)$ in the anticipation that the previous success will be repeated. f_4 is not immediately compared with f_3 , but a set of exploratory moves are first made to improve the pattern direction. The best point found in the present example is p_5 and since $f_5 < f_3$, it becomes b_3 , the third base point. The search continues with the pattern move towards p_6 with a step size $(2b_3 - b_2)$.

When a pattern move and subsequent exploratory moves fail, the strategy is to return to the previous base point. If the exploratory move around the base point fails, the pattern is destroyed, the parameter increments are reduced and the whole procedure is restarted. At that point, the search is terminated when the parameter increment falls below the prescribed level.

Different variations of the pattern search known as 'Spider search', 'Razor search', and 'Direct search' have enjoyed success with microwave network optimization⁷.

(b) Gradient search

This method utilizes partial derivative information to determine the direction of search. The appropriate partial derivatives are obtained either by evaluating analytical expressions or by estimation. The first derivative can, for example, be estimated from the difference in objective functions produced by small perturbations in the parameter values. If the perturbations are too large, the estimation will be inaccurate and if they are too small, it can still be inaccurate, through numerical difficulties.

'Steepest descent',^{7,72,8,73} is a very straightforward gradient type of optimization and the basic application of this method would be as follows. By definition, a function $Z=F(x,y)$ will increase most rapidly in the direction of the gradient,

$$\nabla Z = |\partial F(x,y)/\partial x|_i + |\partial F(x,y)/\partial y|_j \quad (4.30)$$

where i and j are unit vectors on x and y axis respectively. The direction of the steepest descent at that point is then the negative of the gradient ∇Z . The process is iterative and the movement towards minimum is defined by:

$$p_{j+1} = p_j - \nabla Z(\alpha_j)$$

where α_j is a positive scale factor corresponding to the j th position, and p represents x, y directions. The value of α_j is usually estimated

either by quadratic or by cubic interpolation. To start with, initial moves are made in -VZ direction with an added step computed at each iteration. This process is repeated until either the function or the gradient are so small that it is safe to assume that the minimum of the function is reached. The gradient is a function of scaling and the convergence time is related to the scale of the parameters.

Fletcher-Powell^{7,72,9}, which is generally agreed to be one of the most powerful methods, utilizes second order derivative informations to search. Instead of searching along the negative gradient, it is made along a vector S_j , which is the product of the negative gradient and a positive definite matrix $|H|$. The value of $|H|$ usually approaches the inverse of the matrix of second derivative. A major difficulty with this method is that the procedure is time consuming. A well-known microwave CAD program 'SPEEDY'¹² uses the Fletcher-Powell method.

Another widely used program 'COMPACT'⁷⁴ has dual optimization capability. If the user is unable to estimate the initial component values of the circuit, the program is initiated with a search. In the vicinity of minima, the method is switched to the gradient technique to find the true minimum. With this combination of the two techniques, there is a high probability of finding a global minimum.

4.7 GaAs FET Amplifiers - A Review

In the first Chapter, typical specifications of the currently available GaAs FET amplifiers are presented. In this Section, some of

the FET amplifiers that have been published are reviewed.

Basically, three types of circuit arrangements are in use:

- (1) Matching network using transmission line elements such as stubs, series matching sections, etc.
- (2) Matching networks using filter structures
- (3) Balanced amplifier networks.

The conventional procedures for selecting the matching networks involve computer-aided performance evaluation of several circuits.

Usually, an error function of the form:

$$E_{\text{error}} = \Sigma_f \{ (K_1 |S_{11}|^2) + (K_2 |S_{22}|^2) + (K_3 (G_R - 20 \log |S_{21}|)) \} \quad (4.31)$$

is selected. In the above function, G_R is the reference gain and K_1 , K_2 and K_3 are the weighting factors. The $|S_{11}|^2$ and $|S_{22}|^2$ terms stand for input and output return losses and the third term represents the error in the calculated gain and the required gain. The error function of this form provides an effective amplifier design for gain and return losses only. If noise performance is the principal criterion, the S-parameters are characterized at low drain currents. The design is usually carried out with stubs, series matching sections and filter structures. Available literature indicates that series matching sections are the most favoured with FET amplifiers^{75,52}.

Currently, matching networks utilizing standard microwave filter prototypes are reported^{76,77}. The design steps in such cases are as

follows:

- (1) Model the input and output impedance of GaAs FET in lumped element form.
- (2) Synthesize a matching network whose frequency response and topological form will allow absorption of device parasitics.
- (3) Ensure proper impedance levels at the terminating end of the networks by utilizing impedance transformation available in the network.
- (4) Transform the lumped element solution to an equivalent transmission line network.

Using this procedure, several broadband FET amplifiers have been realized in the X-band^{76,77}.

Balanced amplifiers have certain definite advantages over conventional amplifiers⁷⁸, namely:

- (1) Improved input and output impedance matching, gain flatness, phase linearity, gain compression and intermodulation characteristics.
- (2) Possible design of the amplifiers simultaneously for minimum noise figure and good input match.
- (3) Relatively little effect on overall amplifier gain and matching by changes in the distribution of the transistor.

The disadvantage is that a second transistor is required for each amplifier stage. Recent investigations show that GaAs FET, X-band

balanced amplifier is preferred by manufacturers, mainly because it requires less post fabrication adjustment than other amplifier circuit arrangements⁷⁹.

Negative feedback is not normally used with microwave transistor amplifiers due to the practical realization difficulties of feedback circuits at microwave frequencies and also due to the insufficient gain available from microwave devices to sacrifice for feedback. Fairchild Laboratories have, however, reported the realization of a 3.1 to 3.5GHz FET feedback amplifier with the following results⁸⁰:

- (1) Potentially unstable FET circuits are made unconditionally stable.
- (2) Input/output impedances of the devices are lowered which makes impedance matching and circuit realization on micro-strip easier.
- (3) The effect of device parameter changes on the overall circuit is reduced.

But these advantages are gained at the expense of a reduction in amplifier gain, reverse isolation and an increase in noise figure. The increase in the noise figure may be attributed to the thermal noise contributions of the resistive feedback elements. The noise contribution may, however, be made very small by using the feedback only for stages other than the input stage.

Design of broadband amplifiers using dissipative matching elements are also reported⁹⁰. In this method, the network is matched at the highest frequency of the band which increases resistive losses with a decrease in frequency. Since the noise figure of the device is low at the lower end of the frequency band, the total noise contribution is also small⁹⁰.

CHAPTER 5

AN EFFICIENT COMPUTER-AIDED DESIGN PROGRAM

5.1 Introduction

A large number of microwave computer-aided design programs are commercially available^{11,12,13,82}. These general purpose programs are quite expensive and they require large storage facilities and execution time. The present design calls for a specialized program capable of optimizing circuit elements for a large number of specifics. Further, the program should be compact and should have a format for easy input and output. The input should also be organized in a manner meaningful for the designer. For this reason, a computer program, described in this Chapter, was developed.

5.2 Summary of Analysis

The circuit analysis program should be efficient since it is called several times during the optimization run. The chain matrix described in Section 4.6 forms the basis for the analysis program and it has the property that if two circuit black boxes, characterized by $(ABCD)_1$ and $(ABCD)_2$ respectively, are cascaded, the overall ABCD matrix will simply be the product of the two matrices.

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \times \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix}$$

$$= \begin{bmatrix} A_1 A_2 + B_1 C_2 & A_1 B_2 + B_1 D_2 \\ C_1 A_2 + D_1 C_2 & C_1 B_2 + D_1 D_2 \end{bmatrix} \quad (5.1)$$

Hence, the chain matrix corresponding to a long chain of network elements may rapidly be evaluated on the computer by simply multiplying their individual ABCD matrices from left to right. One of the interesting and powerful features of this method, other than the speed of computation, is its ability to represent matrices of individual network elements in the computer memory. The individual elements may be of different types. Once the type of the element is specified, an appropriate subroutine is called for computing the ABCD parameters of the element. ~~The matrices of~~ ABCD parameters for different types of elements are given in Reference 82. The chain matrix of the active device is obtained by the conversion of S to ABCD parameters. This is performed through an intermediate stage of computing the Y-parameters in order to facilitate the analysis of circuits with Y embedding or such circuits.

The overall ABCD matrix is evaluated for each sample frequency. This is then converted to S-parameters for computing the power gain, the input return loss, the output return loss and the stability factor as follows:

$$\text{Transducer gain} = 20 \log |S_{21}| \quad (5.2)$$

$$\text{Input return loss} = -20 \log |S_{11}| \quad (5.3)$$

$$\text{Output return loss} = -20 \log |S_{22}| \quad (5.4)$$

$$\text{Stability factor } K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2 |S_{12} S_{21}|} \quad (5.5)$$

where

$$\Delta = S_{11} S_{22} - S_{12} S_{21}$$

The details of the computing procedure for evaluating the noise figure of cascaded stages are as follows. For the sake of explanation, consider the two stage amplifier shown in Fig. 5.1 and assume that the noise parameters such as minimum noise figure F_o , noise resistance R_n , and noise conductance G_o and noise susceptance B_o for minimum noise figure of each device are known. To start with, matrix multiplication is continued from left to right until the reference plane A is reached. The overall ABCD matrix is then converted to Y parameters and both source conductance G_s and source susceptance B_s are evaluated. the noise factor of the 1st stage (F_1) is then calculated using Eqn. (2.25), that is:

$$F_i = F_o + \frac{R_n}{G_s} [(G_s - G_o)^2 + (B_s - B_o)^2] \quad (5.6)$$

$i=1,2,\dots$

with $i=1$ for the 1st stage.

The ABCD analysis is continued until the reference plane B is reached and the noise factor F_2 is calculated by Eqn. (5.6). An impedance which represents the S_{11} of 2nd stage devices is then substituted for load and the overall ABCD parameters, S-parameters and the transducer gain G are

Fig. 5.1. A block schematic to illustrate the calculation of NF of cascaded stages.

calculated. Since F_1 , F_2 and G_1 are known, the overall noise factor F_t may be evaluated from the equation:

$$F_t = F_1 + \frac{F_2 - 1}{G_1}$$

If the amplifier has multiple stages, then the overall noise factor is determined by:

$$F_t = F_1 + \frac{F_2 - 1}{G_2} + \frac{F_3 - 1}{G_1 G_2} + \dots \quad (5.7)$$

where G_1 , $G_1 G_2$, $G_1 G_2 G_3$, are known as combined gains. These gains are calculated by the substitution method suggested for G_1 . Since S_{12} is not zero, it is quite possible for the load to have a second order effect on effective S_{11} or Γ_{11} . The output return loss is usually greater than 10dB, and hence this loading does not have considerable effect on the overall noise factor evaluation.

To illustrate this point, consider the circuit 'black box' shown in Fig. 2.7 and assume that it is not terminated at its characteristic impedance at the output. Let the output reflection coefficient be Γ_L . Then, the reflection coefficient at port 1 becomes⁹⁴:

$$\Gamma_{11} = \frac{b_1}{a_1} = S_{11} + \frac{S_{12} S_{21} \Gamma_L}{1 - S_{22} \Gamma_L} \quad (5.8)$$

By terminating the two port with a matched load ($\Gamma_L = 0$), the output reflection coefficient equals the intrinsic reflection coefficient S_{11} .

Consider the following typical S-parameter values for the type,
GAT-2 FET:

$$S_{11} = 0.66 \angle -60^\circ$$

$$S_{12} = 0.1 \angle 70^\circ$$

$$S_{21} = 0.9 \angle 110^\circ$$

$$S_{22} = 0.9 \angle -20^\circ$$

With these values, the second term in Eqn. (5.8) reduces to $0.04 \angle -7.8^\circ$ which corresponds to 10dB return loss. It means that the change in Γ_{11} is less than 6% for all values of output return loss greater than 10dB. The load constituted by Γ_{11} is only a portion of the total load of the amplifier and hence the percentage change in gain is much less.

Assume that the typical noise factor and transducer gain of the GAT-2 FET amplifiers are 4.5 and 5.5dB, respectively. Using Eqns. (5.7), the noise figure reduces to 7.39dB and with 6% change in calculated gain, it is 7.44dB. The change in the calculated noise figure, corresponding to a 6% change in gain of the (usually it is much less) amplifier is 0.05dB and hence the assumption is valid.

Both group delay and gain slope are calculated by cubic spline curve fitting⁸³. The condition for a cubic spline fit is that if a set of cubics are passed through the points, using a new cubic in each interval, the slope and curvature should be the same for the pair of

cubics that joined each point. Spline fit interpolation consists of determining the two points (X_k, Y_k) and (X_{k+1}, Y_{k+1}) , from a set of points (X_1, Y_1) , (X_2, Y_2) , (X_3, Y_3) , between which lies the given value of X . The value of Y corresponding to this X is then given by the formula⁸³:

$$Y = C_{1,k}(X_{k+1}-X)^3 + C_{2,k}(X-X_k)^3 + C_{3,k}(X_{k+1}-X) + C_{4,k}(X-X_k) \quad (5.9)$$

where the constants can be determined by:

$$C_{1,k} = Z_k/6dk$$

$$C_{2,k} = Z_{k+1}/6dk$$

$$C_{3,k} = Y_k/dk - Z_k dk/6$$

$$C_{4,k} = Y_{k+1}/dk - Z_{k+1} dk/6$$

where Z_k and Z_{k+1} are the values of the second derivative of the third degree polynomial at k and $k+1$ points and dk is given by $(X_{k+1}-X_k)$.

The preliminary studies using the analysis program indicated that the curve of both the magnitude and phase of S_{21} of the overall amplifier as a function of frequency is suitable for spline curve fitting and hence it is used for calculating the gain slope and group delay of amplifiers. Another advantage of using this method is that the derivative information is readily available.

The flow charts shown in Fig. 5.2 clearly illustrate the various operations involved in the analysis program. The data required for the

Fig. 5.2a. Flow chart of computer-aided design (CAD) program.

Fig. 5.2b. Flow chart of CAD program. (continued)

Fig. 5.2c.. Flow chart of CAD program. (continued)

Fig. 5.2d. Flow chart for CAD program. (continued)

Fig. 5.2e. Flowchart for CAD program. (continued)

Fig. 5.2f. Flowchart for CAD program (continued).

program are the operating frequency (f), type of element (ET), number of elements ($NELM$), number of frequency sample points (N_1), and the initial values of the elements. Three types of elements are used with microstrip amplifiers, namely: transmission line elements, active elements, and lumped elements. The type of transmission line elements include series matching sections, open stubs and shorted stubs. The data required for computing the transmission line elements are the initial value of the impedance Z and length L . Provision for analyzing only a few of the elements for microstrip design is provided in order to make the program as compact as possible. The S-parameter values, provided in magnitude and angle, are converted to complex numbers as it is read. If optimization is not required, further reading of data is bypassed. If it is required, the data is read and optimized value of elements are determined using the subroutine 'EVAL'. The transducer gain, return loss, stability, and noise figure (Eqns. (5.2) to (5.7)) are calculated as stated before, for the specific frequencies. For each of these frequencies, the computation for the overall ABCD matrix, the ABCD parameter to S-parameter conversion and the calculation of the design objectives is performed in a sequential order. The advantage of this procedure is that the storage requirement is minimum¹¹.

5.3 The Objective Function

The objective function used in this work, which includes all the parameters of the design objective, is mainly a mean square error function and takes the form:

$$\begin{aligned}
 E = & \sum_f A_1 (G(f) - G_d(f))^2 + A_2 (G(f) - G_A(f))^2 + A_3 (R_{LI}(f) - C_1)^2 \\
 & + A_4 (R_{LO}(f) - C_2)^2 + A_5 (NF(f) - MN(f))^2 + A_6 \frac{10 \cdot \text{DEL}}{A - \text{DEL}} \\
 & + A_7 \frac{\text{Slope}(f)}{B - \text{Slope}(f)}
 \end{aligned} \tag{5.10}$$

where

A_1 = transducer gain weighting factor

A_2 = gain flatness weighting factor

A_3 = input return loss weighting factor

A_4 = output return loss weighting factor

A_5 = noise figure weighting factor

A_6 = group delay weighting factor

A_7 = gain-slope weighting factor

$G(f)$ = calculated transducer gain in dB

$G_d(f)$ = desired gain in dB (data)

$G_A(f)$ = calculated gain averaged over the frequency sample points

$R_{LI}(f)$ = input return loss in dB

$R_{LO}(f)$ = output return loss in dB

C_1 = reference input return loss in dB (20dB)

C_2 = reference output return loss in dB (20dB)

$MN(f)$ = calculated value of noise figure (dB)

$MN(f)$ = minimum value of noise figure in dB (data)

DEL = calculated maximum value of group delay variation (nSec)

A = upper limit of permissible group delay variation (nSec)

Slope(f) = calculated gain slope (dB/MHz)

B = permissible gain slope (dB/MHz)

The first five terms of the objective function follow the mean square error criterion. The two gain terms stand for the required gain, specified by G_d and for the gain flatness. The latter is calculated on the basis of reducing the deviations of the gain from the value averaged over the frequency points.

A reference value of 20dB is used for input/output return loss constants C_1 and C_2 . This is the upper limit of realizable return losses for FET amplifiers. But, during the optimization runs, if the return losses become greater than 20dB, that will be considered as an error due to the nature of the objective function. To overcome this, for any value of return loss greater than 20dB, the objective function is bypassed. For passive circuit optimization, instead of a fixed value, the average value of return losses over the frequency band may be a more suitable reference.

The noise figure error term is the difference between the average value of the calculated noise figures and that of minimum noise figures of the device. The minimum noise figures of the device as a function of frequency are provided as data.

It was described in Chapter 4 that the group delay variation is responsible for the delay distortion. The term 'DEL' used in the objective function represents maximum group delay variation. This is calculated in two steps: first, by storing the deviations of the group delay curve from the average value at each frequency point and then adding the maximum deviations in both directions of the average value.

In both cases of delay difference and gain-slope, instead of using mean square error, a function of the form $x/(a-x)$ is used where x is the calculated value of group delay variation or gain slope and a is a constant. The value of this constant used in the program for the group delay variation (A) is $\ln \text{Sec}$ and that for the gain slope (B) is 0.01 dB/MHz . These values are derived from the design specifications stated in Section 4.2. If the value of x approaches the constant a , the error term increases rapidly and it may provide an overflow during computation. In order to prevent it, as $(x-a)$ approaches zero, the denominator is set to a predetermined value (0.02) which is small enough to provide significance for the corresponding term in the objective function.

It was observed that the computations performed with unity weighting factors, ($A_1 = \dots = A_7 = 1$), satisfies most of the design requirements. Hence, for the first computer run, the weights are always selected as unity. By evaluating the results of the first computer run, the weight may be modified suitably to get the optimum performance (as discussed in Section 5.7). Experience indicates that by judicious selection of the

weighting factors, it is possible to obtain near-optimum performance with three or four computer runs.

5.4 A Compact Optimization

By definition, optimization stands for the search for a minima (local or global). This term, as currently used in microwave practices, stands for finding a combination of element values near the minimum to satisfy the design objective. The optimization term used here follows the latter meaning.

The optimization process used in the program consists of both the gradient and search methods. The derivative information required to find the gradient is obtained by perturbation method. Each element is perturbed by a predetermined value and the information of the direction of greatest improvement is stored. Since the microstrip elements are two-dimensional, nine vectors are compared for this (including zero vector). For the n element circuit, the computer stores n vectors after a sequence of perturbations. In the gradient method described in Chapter 4, the step size is selected by quadratic interpolation, followed by another sequence of perturbation for the direction of the next step. This procedure is quite time consuming especially when a large number of elements are involved. In a practical microstrip problem, circuit etching and tolerance of the substrates limits the usefulness of having step

size below a certain value. The lower limit in step size for impedance is then a fraction of an ohm, and for length, the wavelength corresponding to 0.001". Fixing the lower limit to values mentioned above is advantageous since it enhances computation time. Hence, once the n dimensional vectors are determined, the search is initiated with the given step size. In the direct search method used, the objective function is evaluated at some starting point, in the predetermined direction. The process of evaluating the objective functions and incrementing the step is repeated until a minimum is located. One special advantage of using gradient method followed by the direct search is that those elements whose values are in the optimum may be easily excluded from the search, thereby improving the efficiency of the optimization. The constrained minimization using the gradient method is complex and requires their transfer to unconstrained minimization for optimization. Subroutines like 'BOUND' are normally used¹¹ for such computations. In the direct search method, the element values are checked every time they are incremented, thereby ensuring their values to be within limits. If the minima lies outside this limit, the limiting values of the elements are chosen. This process is simple and efficient.

Once the minima is located by direct search, the perturbation process is repeated with a step size which is a predetermined fraction of the initial step size. The process of finding the gradients and the direct search for minima are repeated until the minimum value of step size is reached.

The objective function used for optimization (Section 5.3) is not unimodal (more than one minima). Most of the currently available multivariable optimization methods are not capable of guaranteeing the global minimum⁸² for such functions. The optimization procedure discussed above also does not guarantee a global minimum for non-unimodal functions. However, this does not become restrictive if the response using the optimized values meets the design objective. If the responses are not acceptable, a new set of starting variables are chosen and the computations are repeated. Further, since there are bounds put on the independent variables, the global minima could be outside the limits of the constraints and therefore that minimum could not have been located, even if attempted.

The flow chart of the optimization program is shown in Figs. 5.1d,e,f. The required step size, the elements to be optimized, the upper and lower limit of the element values to be realized, weighting factors and step sizes are provided as data. The initial value of the objective function E is calculated for the reference using subroutine 'EVAL'. These initial values are then perturbed, and the new objective function value is obtained. This value is compared with the original value and the direction of improvement is stored in terms of code numbers.

Figs. 5.1d and 5.1e show the gradient method. The symbol II represents the number of perturbations for impedance ZI and JJ represents that for LI . As can be seen in Fig. 5.1e, each element is tested for perturbation and the code numbers $C(I)$ are stored. Fig. 5.1f represents

the direct search procedure. To start, based on the code, the element values are incremented and the subroutine 'EVAL' is then called to compare the improvement in performance. If improvement is noted, the old element values are replaced by new ones and the process is continued. If no improvement is noted, the step is reduced and the whole process of finding the gradients and the search is repeated. After five iterations, the results are printed and the operation stops. This value is obtained as a compromise between performance improvement and computation time.

5.5 Subroutines

There are nine subroutines in the program. Their functions are explained in this Section.

Subroutine ABCD calculates the ABCD matrix of the individual elements and determines the overall ABCD matrix for each frequency point. It also determines the noise figure of the amplifier.

Subroutine CONV converts S to Y matrix and other way round.

Subroutine ABC converts Y parameters to ABCD parameters.

Subroutine YBC converts ABCD parameters to Y parameters.

Subroutine SPLINE calculates the magnitude of Y for any given X, by cubic spline curve fitting⁸³.

Subroutine GDGS evaluates the group delay and gain slope of the amplifier for each frequency point. Since the amplitude modulation technique is used for measuring the group delay of the amplifier, the group delay at ω_0 is given by:⁹¹

$$\frac{\partial \phi}{\partial \omega} = (\phi_1 - \phi_2) / (\omega_1 - \omega_2)$$

where ϕ_1 and ϕ_2 are phase shifts of frequencies ω_1 and ω_2 in passing through the amplifier. The reason for adopting the method is that it is the procedure by which the group delay measurements are made. The gain slope variation is also computed using GDGS.

Subroutine EVAL evaluates the objective function described in Section 5.3. The subroutine does the analysis, calculates the group delay variations and averages value of overall gain and noise figure over the frequency range of interest. The group delay variation is calculated by evaluating the maximum deviations of the group delay from its average value as described earlier.

A flow chart showing the relationship between various subroutines and the main program is given in Fig. 5.3.

5.6 Input-Output Data

The program requires the following input data:

- (1) Sample frequency points
- (2) Attenuating constant α 's of the microstrip
- (3) Number of elements

Fig. 5.3. A flowchart showing the connections between main program and subroutines.

- (4) Circuit topology (code numbers)
- (5) Starting values of elements (for central frequency)
- (6) S-parameters of the active circuit (for each frequency point)
- (7) The noise parameters of the transistor (for each frequency point)
- (8) Weighting factors
- (9) Element constraints
- (10) Elements to be optimized
- (11) Initial step size

The output data are as follows:

- (1) Data input
- (2) Power gain vs frequency
- (3) Input return loss vs frequency
- (4) Output return loss vs frequency
- (5) Group delay vs frequency
- (6) Noise figure vs frequency
- (7) Gain slope vs frequency
- (8) Stability factor vs frequency
- (9) Overall S-parameters in magnitude and angle vs frequency.

The complete computer program with an optimization run and the details of the input and output are given in Appendix D.

The language of the computer program is Fortran IV and it is written for use with Xerox Sigma 9. The program contains 748 cards and it takes approximately 16K core. On the average, an optimization run

for a one-stage amplifier design takes 0.6 seconds of CPU time on Xerox Sigma 9, for step sizes of the order of 0.5 ohms and $0.001\lambda_g$.

5.7 Selection of Topology

The most important step in the design of amplifier circuits is the selection of circuit configuration. Published results show that matching networks such as series matching sections, stubs and lumped elements are used with FET amplifiers^{75,84,85}.

In order to compare the performances of these matching sections, each of these circuit configurations shown in Fig. 5.4 were studied, using the program described in the previous Sections. The values of the gain-slope, return losses, group delay variations were chosen on the basis of the arguments presented in Section 5.3. To determine the value of reference gain, matching sections were designed by graphical methods using the Smith chart. These component values were then used in the analysis program to obtain the reference gain (5.2dB). The S-parameters, used for the computation, are shown in Figs. 2.12 and 2.13. The basis for selecting unit weighting factors for reference is also discussed in Section 5.3. The results of the computer studies are shown in Figs. 5.5 to 5.8.

Fig. 5.5 shows the transducer gain as a function of frequency. It indicates that the topology No. 2 shown in Fig. 5.4 provides the highest gain. It means that extra gain is available to sacrifice for

Fig. 5.4. Circuit configurations and symbols used in Figs. 5.5 to 5.8. Optimum performance is obtained with topology (2) with the following final values:

Element No.	1	2	3	4	5
L	0.248	0.152	0.219	0.248	0.248
Z	28.8	51.2	51.2	8	22.8

Fig. 5.5. A plot of gain vs frequency for different circuit configurations shown in Fig. 5.4.

Fig. 5.6. A plot of NF vs frequency for different circuit configurations shown in Fig. 5.4.

Fig. 5.7. A plot of input return loss vs frequency for different circuit configuration shown in Fig. 5.4.

Wt. factor = 1

Fig. 5.8. A plot of group delay vs frequency for different circuit configurations shown in Fig. 5.4.

the relative improvement of other design objectives. Fig. 5.6 and Fig. 5.7 indicate that this circuit has comparatively low noise figure and the input return loss is greater than 10dB. Group delay variation and gain slopes are less than 100p.sec and 0.005dB/MHz respectively. It is essential that the input circuits must be simple, since losses in the input matching network are directly added to the transistor noise figure. The circuit configuration under consideration satisfies the requirement. Hence, on the basis of performance evaluation, the topology with series matching sections both at the input and output were selected (No. 2, Fig. 5.4.).

A close look at the graph of 5.5 shows that gain response variation of the selected circuit is more than 1.4dB. Hence, the gain flatness weighting factor A_2 was increased to 2 without changing the other weighting factors. Improvement in the gain flatness was noted. On the higher frequency (4GHz) side, the output return loss showed a sharp drop with a return loss value less than 10dB. Hence, both A_2 and A_4 were changed to 5 and 2 with all other weights unchanged. The resulting performance curves are also plotted in Figs. 5.5 to 5.8. The optimum responses are 5 ± 0.25 dB gain, 10dB return loss, 7.6dB noise figure and 30p Sec group delay variation. The optimum values of the circuit elements are shown in Fig. 5.4.

5.8 Performance Variation Due to Circuit

It was pointed out in Section 3.5 that, even if the design is accurate, variations of dielectric constant and substrate thickness can cause considerable variations in the impedances and effective length of the microstrip lines. For example, for the commercially available microstrip substrates, a 10% change in impedances and 10 mil change in length of the circuit elements is quite normal. Consequently, the designer of the amplifier will be interested in the performance variation of the designed circuit, constructed using such substrates, in order to provide guidelines, governing the selection of substrates, etching process, etc. Fig. 5.8 shows the gain variations, that can be expected for the dimensional changes of the circuit mentioned in Section 5.7, evaluated as described in the next paragraph.

This performance variation is obtained by using the same computer program described in the previous section but the optimization process is altered as to obtain a maximum instead of a minimum. This can be easily done by changing the direction of the gradient and by altering the conditional statement of the direct search. The validity of the flow chart shown in Figs. 5.2d,e,f still holds except for change in signs such as ($E < E_{\min}$), etc. The dimensional variation of circuit elements is limited to 10% in impedance and 10 mils in length, based on the specifications of the substrate used. The initial computation finds the direction of greatest change and increments the steps in that direction

by 1% change in Z and 1 mil change in L . The process is repeated within the permissible limit to obtain the maximum. Calculations with only gain and gain flatness considered show a maximum of 2dB gain variation from the designed value and a gain flatness variation greater than $\pm 0.5\text{dB}$. Even though other design objectives are not optimized for their performance degradation, a deterioration of 1dB noise figure, 2dB input return loss and 120pSec group delay variation is noted. Fig. 5.9 shows a plot of power gain variation with frequency for different values of dimensional changes of Z and L . It shows that the change in gain varies linearly with changes of the dimensions of the circuit elements.

Graph 5.9 provides the following important information. Even if the design is accurate, unless the substrate thickness and dielectric constants are known accurately, considerable deviation from the theoretically predicted values can be expected if the circuit is fabricated and tested. If this deviation of gain has to be limited to $\pm 0.5\text{dB}$, the impedance and length variations of the microstrip elements should be better than $0.02Z$ and $0.002\lambda_g$, respectively. This means that the alumina substrate thickness should not vary more than 0.001" from the specified 0.025" and permittivity tolerance should be better than 1%. The etching process also should yield a line definition of the order of 0.0005".

Fig. 5.9. Performance variation in gain for one-stage FET amplifier due to substrate tolerance.

1. (10% change in Z_I , 0.01λ in L_I)
2. (5% change in Z_I , 0.005λ in L_I)
3. (2% change in Z_I , 0.002λ in L_I)

CHAPTER 6DESIGN CONSIDERATIONS AND EXPERIMENTATION6.1 Introduction

Any approach to the design of low noise microwave transistor amplifiers is strongly influenced by the absolute value and the range of spread of the transistor S-parameters. The absolute value may dictate the choice of a particular form of circuit realization and the spread in turn will determine the selection of design approach. Normally, three design approaches are possible.

The first approach is simply to design a fixed circuit, based on the design centre values of the transistor S-parameters. This would require a close control of S-parameters within some set of criteria, so that transistors would be "Plug-in replaceable" in the fixed circuit. The procedure will be quite expensive since the individual transistors have to be selected.

The second approach is to incorporate adjustable circuit elements, with the idea of accommodating fairly large spreads in the S-parameters. Though it looks promising at first sight, it is not practicable due to the large number of variable elements and automatic monitoring facilities required.

In the third approach, individual S-parameters of the transistors are measured and for each transistor a suitable circuit is realized. With the large spread of S-parameters of FETs available today, this seems

to be the logical solution and hence this procedure is adopted as the basis for the present work. It assumes that the useful life of the transistor is indefinitely long.

The first few Sections of this Chapter deal with the design consideration of transistor amplifiers, selection of the operating point of cascaded stages and optimum cascading method. The rest of the Chapter describes the experimental details and results of the amplifier designed using the program described in Chapter 5, measurement procedures for group delay and intermodulation and the calculation of the dynamic range.

6.2 Design Considerations

Fig. 6.1 shows a flow chart which indicates the various stages involved in the design of transistor amplifiers. Usually, transistor amplifiers are designed for specific applications and such applications determine the specification and the form of circuitry. Amplifiers are made using microstrip, strip line or thin film circuitry⁸⁶. The design procedure used in the case of thin film circuitry is not considered here. Microstrip circuits are popular since they are easier to fabricate than strip lines.

Different types of cascading schemes are in use. Amplifiers may be constructed by cascading single stage modules or by cascading a combination of a few amplifier stages, or they may be realized as a single unit. The considerations involved in the selection of the type of cascading are described in Section 6.4.

Fig. 6.1. A flowchart for amplifier design.

Fig. 6.1b. Flow chart for amplifier design (continued).

Once the specifications of the individual cascading modules are determined, based on the application and cascading considerations (Section 6.4), the selection of the active devices is made on that basis. After the device selection, the next step is to characterize the active device accurately for noise and gain parameters, and thus develop an appropriate device model. Care is taken to perform these measurements in the actual environment in which the device will eventually be operating. Since devices are not measured with an automatic network analyzer, an error correction is provided after measurement. The data for this correction is obtained from the characterization of the jig.

Upon completion of device selection and characterization phase, several circuits are explored to satisfy the required design objective. The optimum circuit for a particular device and amplifier specification is selected by the computer-aided evaluation of different circuits as described in Section 5.3. The objective function used for minimization should adequately reflect the design goals. It may be a mean square error function or some other form of minimax function with weighting factors. The selection of these factors is usually based on the design requirement. For example, if the designer is interested only in the return losses, gain and gain flatness of the amplifier, for the initial computer run, all the weighting factors A_1 to A_4 may be taken as unity and the rest as zero (Eqn. (5.10)). By evaluating the results, the weight may be modified suitably so as to bring the performance to near optimal values. Usually,

satisfactory results are obtained with three or four trial runs.

If the foregoing steps are carefully implemented, the program should yield an optimum design. If not, a change in the operating point of the transistor, a new circuit configuration, the use of a different active device and a change in cascading scheme may be considered in the sequential order.

6.3 Variation of Gain and Noise Figure with Bias of GaAs FETs⁸⁷

This Section reviews the selection procedure of the device and presents the characterization of GaAs FETs as a function of bias, to provide guidelines for the selection of device operating point.

The device selection is normally made on the basis of the information provided by the manufacturers. The data sheet provides typical values of the S-parameters as a function of frequency for a particular drain to source voltage V_{ds} and drain current I_d . The published results⁸⁷ and the experimental studies using the GAT-2 FETs show that for a constant drain current the gain is a function of V_{ds} . The gain usually peaks at a voltage V_d' (typically 4 to 5V for 2 μ m gate FETs) which is the same order of voltage as that used by manufacturers for specifying the FET S-parameter values.

The noise figure is relatively invariant to changes in V_{ds} , if the drain current is constant. The manufacturers usually provide only a spot noise figure at V_d' . The noise figure corresponding to other frequencies and drain current is normally determined by measurements. A

method of calculating these parameters from the manufacturer's data is described in Section 2.6.

A plot of scattering parameters as a function of drain current is shown in Fig. 6.2. It reveals that S_{21} is the most sensitive parameter to small changes in bias. This is expected since transconductance g_m increases with drain current. The other scattering parameters are relatively insensitive to the variation of bias.

Fig. 6.3 shows the variation of maximum stable gain and minimum noise figure as a function of drain current, for GAT-2 at 3.5GHz. An increase in the minimum noise figure with an increase of drain current is expected since the noise conductance g_n varies linearly with the drain current I_d . The device, whose parameters are shown in Fig. 6.3, is potentially unstable and hence the maximum available gain $|S_{21}/S_{12}|$ is plotted as a function drain current. An increase in drain current increases noise figure and also increases gain.

Since each stage of an amplifier has different function, the bias requirements of individual cascaded stages are different. For example, transistors used in gain stages, in which the noise figure or the saturated output power are not critical, have a much more relaxed bias requirement than low noise front end devices. Typical biasing considerations involved in the design of four stage amplifiers is shown in Fig. 6.4⁸⁸.

Fig. 6.2. A plot of S parameters with drain current for GAT2 FET.

GAT-2
 $V_{DS} = 5V$
 $f = 3.5GHz$

Fig. 6.3. A plot of maximum stable gain and N.F. as a function of drain current.

Fig. 6.4. Biasing conditions for each stage of a cascaded amplifier.

6.4 Amplifier Specification

The specification of the two stage amplifier with Plessey GAT-2 FETs are shown in Table 6.1. The transducer gain and noise figures are obtained using the graphical procedures outlined in Section 4.5. This procedure also provides for stability considerations. The specifications for noise figure and gain are estimated on the basis of noise measure M^{70} . The input and output return losses are taken from the published results for FET amplifiers without circulators^{76,85}. The specification for amplifier gain flatness, gain-slope and group delay variations are selected to satisfy the satellite amplifier specs⁶⁵.

The 1dB compression point is selected on the basis of the maximum linear power output available from the device at low frequencies⁸⁷. This is obtained by drawing the VI characteristics of the device and by choosing a load to provide maximum signal swing. From the value of drain current and drain voltage variation, the linear power output may be obtained. The 8dBm power output corresponds to this power level. The power output at 1dB compression point can be normally expected to be greater than this power. If the design requirement is for power output greater than 8dBm, two alternatives exist. The first one is to combine two transistors to give the required power. The second method is to select a device to give the required power output.

Table 6.1. Specification of two-stage amplifier with GAT-2 FETs.

1.	Operating frequency range	3.5-4GHz
2.	Amplifier gain	11dB
3.	Gain variation	± 0.5 dB (max)
4.	Noise figure	9dB max
5.	Input and output return losses	10dB (min)
6.	Gain slope	0.01dB/MHz (max)
7.	Group delay variation	1nsec (max)
8.	Power output at 1dB compression	+8dBm

6.5 Cascading Considerations

In practice, amplifiers with more than three stages are constructed, cascading single stage modules, since it has the following advantages⁷⁶:

- (1) The design and fabrication is limited to one stage.
- (2) In final cascading, the amplifiers may be selected according to their performance (e.g. lowest noise figure module is selected for first stage).
- (3) In case of device failure, each stage can be replaced with only minor alterations in the performance.

Figs. 6.5 and 6.6 compare the gain and group delay response of the two-stage amplifiers, one designed for optimum interstage match ($A_1=A_2=1$, $A_3=A_7=0$) and the other obtained by cascading two identical single stage amplifiers. The characteristics of single stage amplifiers are shown in Figs. 5.5 to 5.8. Cascading two stages by optimum interstage matching network is superior because it provides a higher gain of $11.5\text{dB} \pm 0.5\text{dB}$, compared to cascading of two identical stages which gives a gain of $9.8 \pm 0.4\text{dB}$. The two amplifiers show comparable performance for the input, output return loss, gain slope and noise figure.

Fig. 6.5 shows that the amplifier with two identical cascaded stages has a group delay variation of more than 1nSec , whereas that of optimized amplifiers is less than 100pSec . The large group delay variation in the former case is due to the presence of high standing waves

Fig. 6.5. A plot showing the variation of gain for two identical stages directly connected and another for using intermediate matching network (computed).

GAT-2 FET

Fig. 6.6. Group delay performance of two identical stages directly cascaded and two stage amplifiers designed for optimum performance (computed).

within the interstage network⁹⁰. This high internal VSWR is caused by the poor return loss of the single stage amplifier. The compensation for the group delay is considered in detail in Chapter 7.

Two stage amplifier modules are fairly easy to design and fabricate. They occupy less space and have superior gain and group delay characteristics, than amplifiers which use single stage modules. The design fabrication of a two-stage amplifier module is described in the next Section.

6.6 Experimental Work

This Section describes the result of an experimental study, conducted with the aim of validating the computer program developed in the previous Chapter.

The first step in the experimental study is obviously the fabrication of the amplifier. This requires the choice of the material for the substrate, the network configuration, the dimensions of the circuit elements and the layout of the amplifier. Based on the reasoning presented in Section 3.1, alumina was chosen as the material for the substrate.

In Section 5.7, it was shown that the series matching section provides the optimum performance for single stage amplifier. The performance studies using stubs and series matching elements were repeated for best interstage match. Based on those results, the topology shown in Figs. 6.7 and 6.8 was chosen. The initial value and weighting factors used for optimization are given in Table 6.2. The program 'DIMENSION' was

Fig. 6.7. Photo of two stage amplifier using GAT-2 field-effect transistors.

(a)

Element No.	Width in inches	Length in inches
1	0.024	-
2	0.062	0.266
3	0.023	0.184
4	0.016	0.197
5	0.105	0.130
6	0.235	0.235
7	0.025	0.170
8	0.023	0.266
9	0.318	0.280
10	0.088	0.282
11	0.024	-

(b)

Fig. 6.8- A plot showing the dimensions of the two stage FET amplifier circuit elements.

a) Topology

b) Dimensions of the circuit element in inches.

T - transistor.

($V_{DS}=5V$, $V_{GS1}=-1V$, $V_{GS2}=0V$)

Table 6.2. Initial values of the circuit elements for the optimization of the two-stage amplifiers and weighting factors.

Element No.	Z in ohms	L in λ_g
2	28.8	0.248
3	51.2	0.152
4	50.	0.150
5	15.	0.150
6	25.	0.200
7	50.	0.150
8	51.2	0.219
9	8.	0.248
10	22.8	0.248

$$A_2=5, A_4=2, A_1=A_3=A_5=A_6=A_7=1$$

then used to obtain the values of microstrip elements and they are given in Fig. 6.8.

The layout of the amplifier must be chosen so as to eliminate any unwanted coupling or parasitics. It should also permit the use of LID mounted devices. Experience indicates that the layout shown in Fig. 6.7 for 3.5 to 4GHz FET amplifiers meets these requirements. The amplifier was fabricated using 25mil thick 2"x2" alumina. The broadband half-moon bias structure and 330pf chip capacitors were used for biasing the circuit and coupling, respectively.

Type GAT-2, the FET used, is a LID mounted device and hence the source was connected to the microstrip ground plane through wrap-around metallization. This type of mounting does not provide a perfect signal-short for the source and it may be modelled as a piece of microstrip transmission line. Since the scattering parameter measurements were based on the same type of device mounting, such a modelling was not considered. Both chip capacitors and transistors were fixed by thermosetting, using silver epoxy. The computer program 'DIMENSION' accounts for all discontinuities and end effects and hence only the correction for the bends was applied during the circuit layout.

The transducer gain/frequency response of the two stage amplifier is shown in Fig. 6.9. The experimental curve track the theoretically predicted curve very well except at the highest frequency. This fall in experimental gain may be due to the following reasons:

Fig. 6.9. Theoretical and experimental gain of two stage FET amplifiers.

- (1) A change in dielectric constant of the substrate.
- (2) A variation in the microstrip element dimensions due to etching.
- (3) Parasitic coupling between the elements and rolled over ground.

As shown in Fig. 6.7, the experimental gain is $10.8 \pm 0.5\text{dB}$ and the theoretical gain is $11.2 \pm 2\text{dB}$.

Figs. 6.10 and 6.11 show the input and output return losses of the two stage amplifier. In both cases, the theoretically predicted and experimental curves agree well. The fairly low value of input return loss is due to the input being matched for optimum noise figure and that of output return loss is due to the high output impedance of the FET. Both return losses can be improved to about 20dB by using ferrite circulators, with a consequent degradation of noise figure by about 0.3dB.

In Fig. 6.12, the amplifier noise figure is plotted as a function of frequency. An increase in noise figure with frequency is expected since, as explained in Section 2.4, F_o is a frequency dependent parameter. The difference in the theoretical and experimental values is due to error in the noise parameter measurement of the device. An increase in the mismatch loss at the input increases the noise figure at the band edge, since input losses add directly to the noise figure. The noise figure measurement procedure using Y factor method is explained in Section 2.5.

Fig. 6.10. Theoretical and experimental input return loss of two stage FET amplifier.

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Fig. 6.11. Theoretical and experimental output return loss (dB) of two stage FET amplifier.

Fig. 6.12. Figure showing the noise figure of two stage FET amplifier as a function of frequency.

6.6 Measurement of Group Delay

In Chapter 4, the term group delay t_d was introduced, but no measurement method was described. A survey of available literature shows that four basic methods have been used to measure group delay and they are⁹¹:

- (1) The direct measurement of the phase shift through the device and the differentiation of phase frequency curve to give group delay.
- (2) Amplitude modulation of carrier frequency.
- (3) Frequency modulation of carrier frequency.
- (4) Measurement of pulse propagation time through the device.

The method used in this work for the initial measurement of group delay consists of first amplitude-modulating a CW signal, transmitting it through a test device and then measuring the phase shift of the envelope. Fig. 6.13 shows the block diagram of the measurement setup⁹². The group delay of the test device at the CW frequency will then be directly proportional to the envelope of the phase shift. This relationship of the group delay to the phase shift and modulation frequency is given by the equation below,

$$t_d = \frac{\phi_e}{f_m \times 360} \quad (6.1)$$

where

ϕ_e = envelope shift in degrees

Fig. 6.13. Group delay measuring setup.

f_m = modulation frequency in Hz

td = group delay in seconds.

For small group delay measurements, modulation frequencies between 1 and 10MHz are ideally suited. If a frequency of 2.778MHz is chosen, the group delay can be directly read in nanoseconds per degree of phase shift. This method of measurement is simple and convenient, but various sources of error limit the measurement to $\pm 0.3 \text{ nSec}^{91}$. Since the order of error for the designed amplifier is the same, the procedure is used only to verify whether any large group delay variation is present.

The direct measurement method⁹¹ is simple in principle and easy to implement if computer methods are used to differentiate. The method used in the Hewlett Packard "Automatic Network Analyzer" (Model 8540A) is to automatically shift the carrier frequency in known increments and measure the phase shift through the device at each frequency to obtain the increment in phase. The group delay is then given by the ratio of phase and frequency increments. With a programmed computer to perform the computations and supervise the increments in frequency, a measurement accuracy is better than $\pm 0.1 \text{ nSec}$, provided the frequency increments are small compared to the fine structure variations in the group delay curve. The smallest frequency increments are a few MHz.

In the present approach, the same principle is utilized in theoretically evaluating the group delay. The phase frequency characteristics of the amplifier were measured very accurately using the network

analyzer, and the program 'SLOPE', which uses the subroutine 'GDGS' and 'SPLINE' was used to find the group delay. Fig. 6.14 shows both experimental and theoretical curves of the group delay as a function of frequency and the maximum group delay variations are 250psec and 100psec, respectively. Considering the permissible group delay variation is 1nSec, these results are well within design limits.

6.7 Gain Slope

The program 'SLOPE' is also used to calculate the gain slope. The data required for computations are the experimental values of the gain and the corresponding sample frequencies. It can be seen from Fig. 6.15 that both theoretical and experimental gain slope drop sharply at about 3.9GHz. The theoretical curve is within the limits of 0.01dB/MHz, but the experimental curve is not. This is due to the sharp fall in gain beyond 3.9GHz, and reason for such a fall in gain is explained in Section 6.5.

6.8 Intermodulation Distortion

It was described in Chapter 4 that if the input signal level is increased beyond a certain range the fundamental input is no longer linearly related to the output level and the compression begins to take place. Fig. 6.17 shows that the output power of the two stage FET amplifier, plotted as a function of input power. An output power of +13dBm at 4GHz was obtained at 1dB compression with an efficiency of 7%.

As described in Chapter 3, the intercept description is recognized as the most convenient method of expressing the third order intermodulation products.

Fig. 6.14. A plot showing the variation of group delay with frequency for two stage FET amplifier.

Fig. 6.15. A plot showing the gain slope of two stage FET amplifier as a function of frequency.

In order to determine the intercept, it is necessary to know the third order product corresponding to at least one value of input. For this, the relative magnitude of the fundamental and third order intermodulation products are determined by two-tone intermodulation measurements.

Fig. 6.16 shows a typical setup for measuring the third order intermodulation products. Two signals of frequencies 3.62 and 3.72GHz are fed to the input of the amplifier through two circulators, a combiner and 20dB coupler. The output of the FET amplifier is fed to the 20dB coupler and 50 ohms termination. The output power at 20dB down is fed to a power meter and spectrum analyzer (AILTECH NO. 707). Since adequate input power levels were not obtained at the input of the amplifier due to limitation of the signal source, no third order products were visible in the spectrum analyzer. The available published data shows that it is fair to assume that the third order intercept point is 12dB above the power output at 1dB compression point. This means that the third order intercept is at +25dBm, as shown by 'A' in Fig. 6.17. A line drawn through the point A with slope 3:1 indicates the third order intermodulation products. For example, at 0dBm input power, the third order products are 38dB down with respect to fundamental signal power which is quite a good specification.

6.9 Calculation of Dynamic Range⁹²

The dynamic range is defined as the range of variation of input signal over which an amplifier can perform its function effectively. In

Fig. 6.16. A block diagram of the experimental setup to determine the third order intermodulation product.

GAT-2
 $V_{DS}=5V$

Fig. 6.17. A plot showing third order intermod products and gain compression of 2 stage FET amplifier.

the case of a single frequency input signal, the dynamic range is defined by the system thermal noise and the saturation power of the amplifier.

The system noise over the bandwidth of the signal may be expressed as the thermal noise N_s plus the noise generated within the amplifier.

$$\text{The thermal power } N_s = K T_o B F$$

where

K is Boltzmann's constant

T_o is the room temperature in degrees Kelvin

B is the bandwidth of the system.

In dBm, the system input noise is expressed as:

$$N_s = -114 \text{ dB/MHz} + B + NF$$

where

B is the bandwidth relative to MHz

NF is the noise figure of the amplifier in dB.

The minimum desirable signal at the input must be at some level above the system input noise level. It is fair to assume that signal twice as strong as the input noise level can just be detected, thus the minimum detectable signal MDS can be expressed in dBm as:

$$\text{MDS} = N_s + 3 \text{ dB}$$

$$\text{MDS} = -111 \text{ dB/MHz} + B + NF$$

The input signal level which produces amplifier saturation can be considered as the input at 1dB compression point. Therefore, from Fig. 6.15,

$$P_s = +4\text{dBm.}$$

Since the dynamic range for a single input signal DR_s is given by the difference between two input levels, P_s and MDS, the DR_s can be expressed in dB as:

$$DR_s = P_s - (-111\text{dB/MHz} + B + \text{NF}) \quad (6.2)$$

For a 500MHz bandwidth system,

$$B = 10 \log \frac{500}{1} = 27\text{dB}$$

The maximum noise figure of the FET amplifier is 10dB. Therefore,

$$\begin{aligned} DR_s &= 4 - (111 + 27 + 10) \\ &= 78\text{dB.} \end{aligned}$$

It is interesting to note that from Eqn. (6.2) the dynamic range is a function of bandwidth. If the bandwidth is less, dynamic range is more and vice-versa.

In the case of a multiple signal system, the upper limit of P_s is defined by the level where the third order intermodulation products just begin to exceed the noise level. The dynamic range-defined by such a condition is known as "Spurious Free Dynamic Range", which characterizes the effective performance of the amplifier with a multiple frequency input signal. For the case of two input signals of equal power level, the spurious free dynamic range DR_m can be expressed as^{64,92}:

$$DR_m = \frac{2}{3} (IMP - G - MDS) \quad (6.3)$$

where

IMP is the third order intercept in dBm

G is the small signal gain and

MDS is the minimum detectable signal defined previously for the amplifier under consideration.

$$DR_m = \frac{2}{3} (25 - 10 - (-111 + 27 + 10))$$

$$= 60\text{dB.}$$

In the case of a typical tunnel diode amplifier with 14dB gain, 4.4dB noise figure, 200MHz bandwidth and -30dBm input power at 1dB compression point, free dynamic range is:

$$DR_s = -30 - (-111 + 23 + 4.4)$$

$$= 111 - 57.4 = 53\text{dB}$$

Hence, the superiority of FET amplifiers over the tunnel diode amplifier is quite evident.

6.11 Performance Comparison

This Section illustrates the usefulness of the design and fabrication procedure suggested in this Chapter, by comparing the results obtained here with some published results. Fig. 6.19 shows⁵² the transducer gain response of one stage FET amplifiers developed by CRC, using Fairchild FMT941. This amplifier was designed to work in the satellite range

of 11.6 to 12.4GHz. The gain of the one stage GAT-2 FET amplifier shown in Fig. 6.19 is 5.5 ± 0.6 dB and that shown in Fig. 6.18 is 7.4 ± 0.5 dB, over the same bandwidth of 500MHz.

The results of a two stage bipolar transistor amplifier are shown in Fig. 6.18⁸⁹. The theoretical curve is obtained using pattern search and the amplifiers were designed using stub matching sections.

The gain of the two stage bipolar amplifier is 7.5 ± 1 dB over a frequency range of 2 to 4GHz whereas that of the GAT-2 FET two stage amplifier is 10.8 ± 1 dB over 500MHz bandwidth (Fig. 6.20). Octave bandwidth FET amplifiers can be easily designed if they are optimized for gain performance, not for optimum noise figure⁷⁵.

To conclude, the procedure suggested in this Chapter provides a method for designing amplifiers having gain/frequency characteristics similar to that reported with bipolar and other FET amplifiers. In addition, the program provides an efficient test bench where the circuit ideas could be tested for gain, gain flatness, noise figure, gain slope, input and output VSWR, group delay and stability. Further, it also helps the designer to design and realize the amplifier with minimum post fabrication alterations.

Fig. 6.18. A two stage bipolar transistor amplifier response⁸⁹.
(V.G. Gelnovatch & T.L. Chase, "DEMON - An Optimal Seeking Computed Program of Microwave Circuits", IEEE Journal of Solid State Circuits, pp. 303-307, December 1970)

Fig. 6.19. One stage FET amplifier performance using FMT941⁵².
(D.S. James et al, "A 12GHz Field Effect Transistor Amplifier for Communication Satellite Applications", Proceedings of the European Microwave Conference, pp. 97-101, 1974).

Fig. 6.20. Gain response of one stage GAT-2 FET amplifier.
($V_{DS}=5V$, $V_{GS}=0$)

CHAPTER 7

A STUDY OF GROUP DELAY IN CASCADED FET AMPLIFIERS

7.1 Introduction

The two most important requirements of the microwave communication systems are:

- (1) The amplitude response of the complex system should be a constant over the prescribed frequency band.
- (2) The phase shift through the system should be a linear function of frequency.

The second condition is responsible for the group delay or the envelope delay which is defined as the derivative of the phase characteristics with frequency. If the phase characteristics are linear, the group delay is constant, and no group delay distortion occurs.

One major contributor to the group delay distortion in systems using FET amplifiers is the high internal VSWR caused by mismatch. In such cases, the group delay ripples tend to exhibit random period and their magnitude depends on the mismatch at various interfaces. In this Chapter, the group delay problem caused by high input/output return losses of the FET amplifier is explained. An efficient group delay equalization procedure and the design of new microwave delay equalizers are then suggested.

7.2 Group Delay and VSWR

The dependence of group delay on the internal VSWR is a recognized fact in communication system design. A basic theoretical approach to establish this dependence of group delay on interstage VSWR is not currently available, and it is given in this section.

Consider the cascaded connection of two ports, as shown in Fig.

7.1⁹⁴. The scattering matrices of M and N are:

$$M = \begin{bmatrix} m_{11} & m_{12} \\ m_{21} & m_{22} \end{bmatrix}, N = \begin{bmatrix} n_{11} & n_{12} \\ n_{21} & n_{22} \end{bmatrix}$$

From Fig. 7.1 for the two port labelled M,

$$b_1 = m_{11}a_1 + m_{12}A_2$$

$$B_2 = m_{21}a_1 + m_{22}A_2$$

$$\frac{b_1}{a_1} = m_{11} + \frac{m_{12}m_{21}(A_2/B_2)}{1 - m_{22}(A_2/B_2)}$$

and

$$\frac{A_2}{B_2} = \frac{B_1}{A_1} = n_{11} + \frac{n_{12}n_{21}\Gamma_L}{1 - n_{22}\Gamma_L}$$

If $\Gamma_L = 0$ (50 ohms output),

$$\left. \Gamma_1 \right|_{\Gamma_L=0} = \left[\frac{b_1}{a_1} \right]_{a_2=0} = S_{11}$$

Fig. 7.1. Cascade connection of two ports.

$$S_{11} = m_{11} + \frac{m_{12}m_{21}n_{11}}{1-m_{22}n_{11}} \quad (7.1)$$

Similarly,

$$S_{22} = n_{22} + \frac{n_{12}n_{21}m_{22}}{1-m_{22}n_{11}} \quad (7.2)$$

The transmission coefficient S_{21} is obtained in the following way:

$$S_{21} = \left[\frac{b_2}{a_1} \right]_{a_2=0} = \left[\frac{B_2}{a_1} \cdot \frac{b_2}{A_1} \right]_{a_2=0} \quad (7.2a)$$

Since $B_2 = A_1$, the scattering equations of the two port labelled N are:

$$\begin{aligned} B_1 &= n_{11}A_1 + n_{12}a_2 \\ b_2 &= n_{21}A_1 + n_{22}a_2 \end{aligned} \quad (7.3)$$

From the equation for B_2 (7.0),

$$\begin{aligned} B_2 - m_{22}A_2 &= m_{21}a_1 \\ B_2 \left(1 - m_{22} \frac{A_2}{B_2} \right) &= m_{21}a_1 \end{aligned} \quad (7.4)$$

$$\frac{B_2}{a_1} = \frac{m_{21}}{1 - m_{22}(A_2/B_2)} \quad (7.5)$$

$$\left| \frac{A_2}{B_2} \right|_{a_2=0} = \left| \frac{B_1}{A_1} \right|_{a_2=0} = n_{11} \quad (7.6)$$

From Eqn. (7.3),

$$\left| \frac{b_2}{A_1} \right|_{a_2=0} = n_{21} \quad (7.7)$$

Using Eqns. (7.5) and (7.7) in Eqn. (7.2a), we get:

$$S_{21} = \frac{m_{21}}{1 - m_{22}n_{11}} \cdot n_{21}$$

$$S_{21} = \frac{m_{21}n_{21}}{1 - m_{22}n_{11}} \quad (7.8)$$

Similarly,

$$S_{12} = \frac{m_{12}n_{12}}{1 - m_{22}n_{11}} \quad (7.9)$$

Let M and N represent two single stage amplifier modules in cascade. For the calculation of group delay of the cascaded amplifier, we are interested only in S_{21} , as given in Eqn. (7.8).

If both output return loss of the amplifier M and the input return loss of the amplifier N_1 are greater than 20dB,

$$S_{21} = m_{21}n_{21}$$

or

$$\phi_{21} = \phi_{m_{21}} + \phi_{n_{21}}$$

or

$$\frac{d\phi_{21}}{d\omega} = \frac{d\phi_{m_{21}}}{d\omega} + \frac{d\phi_{n_{21}}}{d\omega}$$

$$T_g = T_{g1} + T_{g2} \quad (7.10)$$

which means that the group delay of the overall amplifier is the algebraic sum of each amplifier added at each sample frequency.

If M and N represent two single stage FET amplifiers with return losses of the order of 10dB or less, then Eqn. (7.8) applies as it stands. Therefore,

$$\phi_{S_{21}} = \phi_{m_{21}} + \phi_{n_{21}} - \phi(1-m_{22}n_{11})$$

$$\frac{d\phi_{S_{21}}}{d\omega} = \frac{d\phi_{m_{21}}}{d\omega} + \frac{d\phi_{n_{21}}}{d\omega} - \frac{d\phi(1-m_{22}n_{11})}{d\omega}$$

or

$$T_g = T_{g1} + T_{g2} - T_{gi} \quad (7.11)$$

where T_{gi} is the group delay due to interstage network. For FET amplifiers, return losses at band edges are poor (10dB) compared to mid-band return losses (20dB) and hence even if $T_{g1} + T_{g2}$ are constant, T_{gi} alone can produce considerable group delay variation as is the case shown in Fig. 6.6. The same type of reasoning holds for maximum gain slope variation at the band edges.

7.3 Group Delay Equalizer

Group delay equalizers are normally used in FDM systems for equalizing the delay variations present in the edges of bandpass filters. The equalizers considered in this Section are intended for the compensation

of group delay introduced by FET amplifiers on cascading, as a result of the poor VSWR of individual amplifier units. Computations indicate that this group delay variation can be as high as 3nSec. One important factor which is to be considered is that the delay equalizer should not deteriorate the gain characteristics of the amplifiers.

It is assumed in the formulation of the problem that the overall S matrices of the cascading amplifiers are not known. If they are known, the program described in Chapter 5 can be directly used for synthesizing the group delay equalizer. If S matrices are not known, the same program may be modified to find the network element values for a given group delay curve. Two types of group delay equalizers are considered, namely, transmission type and reflection type.

(a) Transmission type elements

For the transmission type group delay equalizer realization, the program given in Chapter 5 is modified as follows. The sample group delay points at known frequency steps are provided as data. A curve of group delay variation with frequency is then obtained subtracting the average value of group delay from the given data. This information is then stored in the computer. The rest of the program follows the main program described in Chapter 5 except for the objective function which is modified as follows:

$$E = A_1 (\text{Del}(C) - \text{Del}(st))^2 + A_2 (G(c) - G(av))^2$$

calculated stored calculated average

where DEL represents group delay variation, G represents the transducer gain and A_1 and A_2 are weighting factors. The second term in the above equation takes care of the gain flatness. Fig. 7.2 shows the initial and the optimized curves of group delay variation as a function of frequency. The equalization network studied here consists of a simple two stub matching section. The dimensions of the equalizing elements and the weighting factors are indicated in Fig. 7.2. If such an equalizer is connected in series with a circulator at the output of cascaded stages, it will improve both group delay and output VSWR at the same time.

(b) Reflection type elements

Consider the circulator given in Fig. 7.3. Here, a represents the incident wave and b the reflected wave. Following the arrows in the Fig. 7.3 the scattering parameter equations of the 3 port circulator may be written as:

$$b_1 = S_{11}a_1 + S_{12}a_2 + S_{13}a_3$$

$$b_2 = S_{21}a_1 + S_{22}a_2 + S_{23}a_3$$

$$b_3 = S_{31}a_1 + S_{32}a_2 + S_{33}a_3$$

The individual S-parameters may then be defined as:

$$S_{11} = \left. \frac{b_1}{a_1} \right|_{a_2=a_3=0} = \alpha_1$$

Fig. 7.2. Group delay equalized response with stubs.
 (L is the length and Z is the impedance of the matching section.)

Fig. 7.3. Y junction circulator.

where α is the reflection coefficient;

$$S_{12} = \left. \frac{b_1}{a_2} \right|_{a_2=a_3=0} = \beta_1$$

where β is the transmission coefficient from port 2 to port 1;

$$S_{13} = \left. \frac{b_1}{a_3} \right|_{a_1=a_2=0} = \gamma_1$$

where γ is the transmission coefficient from port 3 to port 1.

Similarly, finding the other terms, we get the scattering matrix of the circulator as:

$$S = \begin{bmatrix} \alpha & \beta & \gamma \\ \gamma & \alpha & \beta \\ \beta & \gamma & \alpha \end{bmatrix}$$

where

$$\alpha = \alpha_1 = \alpha_2 = \alpha_3$$

$$\beta = \beta_1 = \beta_2 = \beta_3$$

$$\gamma = \gamma_1 = \gamma_2 = \gamma_3$$

For a perfect circulator, it is necessary that $\alpha=\beta=0$ and $\gamma=1$. In that case:

$$S = \begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix}$$

In actual practice, α and β are not zero and γ is not equal to unity. The performance of loss free circulators can then be predicted by calculating the following quantities:

$$\text{Return loss} = 20 \log_{10} |\alpha|$$

$$\text{Isolation} = 20 \log_{10} |\beta|$$

$$\text{Insertion loss} = 20 \log_{10} |\gamma|$$

For a reflection type equalizer with input connected to port 1 and output to port 3, the scattering matrix reduces to:

$$S = \begin{bmatrix} \alpha & \gamma \\ S_{31} & \alpha \end{bmatrix} \quad (7.12)$$

where S_{31} is the transmission coefficient from port 1 to port 3.

$$S_{31} = T_2 = \frac{Z_{L2} - Z_0}{Z_{L2} + Z_0} \quad (7.13)$$

The computation for designing the reflection type equalizer is carried out under the following assumptions:

- (1) The return loss is 20dB.
- (2) The insertion loss is zero.
- (3) Reverse isolation is better than 20dB.

The main program described in Chapter 5 is used to determine the reflection coefficient S_{31} . The magnitude and phase of this reflection

coefficient is then used to find the gain and group delay variation, which are used in the objective function for optimization as:

$$E = A_1 (\text{DEL}(C) - \text{DEL}(St))^2 + A_2 (G(C) - G(AV))^2$$

+ calculated stored calculated averaged

where A_1 and A_2 are weighting factors.

The initial group delay curve and the compensated group delay curve using the two stub line reflectors are shown in Fig. 7.4. The final values of the stub sections and the weighting factors are also given in the figure. An excellent review of the microstrip forms of ferrite circulators is given in reference 96.

7.4 Delay Equalization by Interstage Matching

Consider three cascaded two port networks whose S-parameters are given by L, M and N as shown in Fig. 7.5. Then, the transmission coefficient S_{21} of the overall two port may be derived as follows.

Following Eqns. (7.1), (7.2), (7.8) and (7.9), the S-parameters of the first two stages are given by:

$$F_{11} = L_{11} + \frac{L_{12}L_{21}M_{11}}{1-L_{22}M_{11}} \quad (7.14)$$

$$F_{22} = M_{22} + \frac{M_{12}M_{21}L_{22}}{1-L_{22}M_{11}} \quad (7.15)$$

$$F_{21} = \frac{L_{21}M_{21}}{1-L_{22}M_{11}} \quad (7.16)$$

Fig. 7.4. Group delay equalized response with reflection type equalizer. (L is the length and Z is the impedance of the matching section.)

Fig. 7.5. Two amplifiers L and N in cascade with delay equalizer M.

$$F_{12} = \frac{L_{12}M_{12}}{1-L_{22}M_{11}} \quad (7.17)$$

The overall S_{21} of three cascaded stages is then:

$$S_{21} = \frac{F_{21}N_{21}}{1-F_{22}N_{11}}$$

Substituting for F_{21} and F_{22}

$$S_{21} = \frac{\frac{L_{21}M_{21}N_{21}}{(1-L_{22}M_{11})}}{\left\{ 1 - \left(M_{22} + \frac{M_{12}M_{21}L_{22}}{1-L_{22}M_{11}} \right) N_{11} \right\}}$$

$$= \frac{(L_{21}M_{21}N_{21})}{[(1-L_{22}M_{11})(1-M_{22}N_{11}) + M_{12}M_{21}L_{22}N_{11}]} \quad (7.18)$$

(a) Circulator as matching network

Assume that L and N represent FET amplifiers of poor return losses and M is a non-ideal circulator. It is also assumed that both L and M are individually optimized for optimum group delay and gain performances.

Let the typical S-parameter of the circulator be:

$$M_{11} = 0.01$$

$$M_{22} = 0.01$$

$$M_{21} = 1$$

$$M_{12} = 0.01$$

Substituting these values in Eqn. (7.18), we get:

$$S_{21} = \frac{L_{21}N_{21}}{[(1-0.01L_{22})(1-0.01N_{11})+0.01L_{22}N_{11}]} \quad (7.19)$$

Assume a worst case reflection coefficient of 0.5 for both the cascading amplifiers. Then,

$$S_{21} = 1.007L_{21}N_{21}$$

This means that even with 6dB return losses, if circulators are used for interstage matching, the overall effect of return losses on gain and group delay will still be quite negligible. Hence, group delay and gain variation produced by interstage mismatch can be avoided by using circulators.

(b) Transmission line matching network

It is often inconvenient to use circulators because of fabrication difficulties and bandwidth problems. Hence, it is desirable to provide group delay equalization by simple transmission line elements. The design method suggested in this section assumes that L_{22} and N_{11} (Fig. 7.5) are available as a function of frequency. The advantage of this formulation is the direct applicability of such methods in many practical situations. For example, if the FET amplifier is to be cascaded to another device with poor return losses, this procedure could be easily used.

From Eqn. (7.18), we get:

$$S_{21} = \frac{L_{21}M_{21}N_{21}}{[(1-L_{22}M_{11})(1-M_{22}N_{11})+M_{12}M_{21}L_{22}N_{11}]}$$

It is assumed in the problem that both amplifiers L and N do not introduce group delay problems. Hence, for group delay calculation, the equation reduces to:

$$S_{21} = \frac{M_{21}}{[(1-L_{22}M_{11})(1-M_{22}N_{11})+M_{12}M_{21}L_{22}N_{11}]} \quad (7.20)$$

The only unknown parameters in this equation are S-parameters of the group delay equalizer network (M).

The first step in the design procedure is to select a topology and assign initial values to the elements of the network. The data required for initiating the program are the values of L_{22} and N_{11} , as a function of frequency. They are then translated to complex values and stored. Using the program described in Chapter 5, the computer calculates the scattering parameters (M) and substitutes these values in Eqn. (7.20), with the stored values of L_{22} and N_{11} . From the S_{21} values, corresponding to each sample frequency, gain and group delay variation are calculated. These values are then used in the optimization with the objective function:

$$E = \sum_f A_1 (\text{DEL}(C) - \text{DEL}(St))^2 + A_2 (G(C) - G(Av))^2$$

For example, assume typical return losses L_{22} and N_{11} as shown in Figs. 6.10 and 6.11. Using a two stub transmission line section, the

overall group delay variation may then be reduced to 0.2nSec , as shown in Fig. 7.6. The result is obtained with the first optimization run for weighting factors equal to unity.

Fig. 7.6. Interstage group delay compensation by stubs and transmission lines for cascaded amplifiers whose return losses are as shown in Figs. 6.8 and 6.9. (L represents the length and Z represents the impedance of the matching section.)

CHAPTER 8

SUMMARY AND CONCLUSION

8.1 Summary

The design and fabrication of GaAs field effect transistors is a field of current interest and its importance in satellite and other low-noise front end applications cannot be over-emphasized. A fitting and timely contribution will then be an effective and systematic method for the design and realization of such amplifiers. The thesis outlines a successful method. The work presented in the thesis is summarized under the following headings:

- (1) FET Device Characterization
- (2) Microstrip Circuit Design
- (3) Amplifier Design Program
- (4) Amplifier Design Details
- (5) Group Delay Performance and Interstage Losses.

8.1.1 FET Device Characterization

An important part of the design procedure is the characterization of the device and circuit elements. For reliable results, the test fixture used for that purpose should simulate the configuration as used in the amplifier. For an accurate S-parameter data, it is essential to provide an error correction of the results obtained by swept frequency measurements. An error model described in Chapter 2 is quite effective,

since it also accounts for the end effects of microstrip line on which the device is placed. The noise parameters can be accurately measured using the Y factor method, if an average over several readings is taken, in order to eliminate errors due to mismatches and system fluctuations. As to provide an insight to the noise properties of the device and to verify the measured results, the noise parameters are calculated from the manufacturers' data. The computations based on Pucel's⁹⁵ model shows agreement between the theoretical and experimental results for minimum noise figure, F_0 , but it does not give such a close agreement in the case of optimum noise admittance, Y_0 . If F values corresponding to three frequency points are specified in the manufacturer's data sheet, it is possible to provide an iteration scheme to obtain the value of noise conductances g_{gn} and g_{dn} and correlation coefficient C, accurately. In that case, closer agreement between the theoretical and experimental results for Y_0 can be expected. Since the manufacturers' data are based on the mean value of a large number of sampled data, it is, however, quite possible that individual transistors may still exhibit deviations from the predicted values.

8.1.2 Microstrip Circuit Design

Microstrip components, especially in regard to the effects of bends, can cause problems on circuit realization. Hence, the data required for the characterization of bends were experimentally obtained; it was found that they agree within reasonable limits with the results predicted by Horton⁵⁸, for right angle bends. The computer program 'DIMENSION'

calculates the values of alumina microstrip elements and provides corrections for end effects, discontinuities, and dispersion, for the specified circuit configuration. This program is particularly useful at X-band and above where the component tolerance effect on the performance of the amplifier is more significant.

8.1.3 Amplifier Design Program

The computer program consists of a main program and seven sub-routines. The main program reads all the data, optimizes the circuit elements, analyzes the circuit and provides a response plot. The required data are the initial value of circuit elements, the measured S-parameters, the measured noise parameters, constraints on the realizable impedance Z length L of the elements and step size D_z and D_L for initial iterations. The analysis part of the program is based on the ABCD cascading matrix approach. As for optimization, a novel method which combines the advantage of both direct search and slope following method is used. The optimization is initiated by finding an n dimensional gradient corresponding to n elements by perturbation method. An equal interval search is conducted in the direction of the negative gradient to find the minima. The evaluation of gradient and search for minima is repeated five times by using reduced step sizes. Both group delay variation and gain slope are calculated using cubic spline curve fitting.

An advantage of this amplifier design program is that it may be used as a general purpose program for the synthesis of passive microstrip

components, with little or no alteration, and for the compensation of gain ripple, group delay and gain slope. The input/output matching networks are selected by comparing the performance of different topologies which are normally used with transistor amplifiers.

8.1.4 Amplifier Design Details

In order to test the effectiveness of the design procedure, a 3.5 to 4GHz, two stage amplifier was designed and built using GAT-2 FETs. The amplifier was fabricated as a single module with an interstage matching network since this was found to give better gain and group delay performance than two single stage cascaded amplifiers. The experimental results showed excellent correlation with those predicted by computation. This indicates that low noise front end FET amplifiers can be successfully designed using the amplifier design program, if substrates of low tolerance specifications are used. If such substrates are not used, considerable deviations from the predicted results may be anticipated on fabrication and testing. As an example, the computer studies show a gain variation of more than 2dB, if commercially available alumina substrates are used for fabrication. In such cases, extensive post-fabrication alterations may be required unless the substrates are individually characterized.

8.1.5 Group Delay Performance and Interstage Losses

It was stated in Chapter 7 that both group delay variation and transducer gain of cascaded amplifiers are functions of interstage mismatch. Since the return losses of FET amplifiers are of the order of 10dB,

an increase in group delay variation above 1nsec may be expected to result on cascading amplifiers. A fundamental analysis shows the relation between return losses of the individual stages, and the transmission coefficients S_{21} of the cascaded stages. This analysis not only gives an insight to the dependence of gain and group delay on the interstage return losses of the amplifiers, but also provides methods for reducing group delay and gain ripple. The design of the group delay equalizer for cascaded FET amplifiers is illustrated.

8.2 Conclusion

The following major conclusions can be derived from this research:

- (a) Multi-stage FET amplifiers with certain specifications on gain, gain flatness, gain slope, input and output return losses, noise figure and group delay can be designed by using computer-aided design approach.
- (b) Tolerance in the dielectric constant and the dimensions of the commercially available substrates (Table 3.1) can significantly affect the gain performance, producing as much as 2dB change in gain for single stage moduli.
- (c) Two-stage FET amplifier module using GAT-2 FETs are superior to pairs of single stage modules using the same FETs for gain and group delay performance if the design aim is for two stage amplifier specification.

- (d) Series transmission line elements provide better overall performance of amplifiers, designed using GAT-2 FETs, than matching sections using stubs and low pass filter structures.
- (e) When input and output return losses are of the order of 10dB, group delay and gain variation performance deteriorates, on cascading. The group delay variation can be greater than 1nsec limit specified for satellites under such conditions. By designing transmission line equalizers following the design procedure given in Chapter 8, it is possible to reduce such group delay variations to less than 200nsec.
- (f) Minimum noise figure of the FET for the frequency and drain current can be predicted accurately using Pucel's⁹⁵ noise model. This requires the spot noise figure information provided by the manufacturers.

8.3 Recommendations for Further Work

An efficient method for designing low-noise FET amplifiers for front-end applications is presented in the thesis. The method assumes conventional topologies using stubs and series matching sections. However, it is quite possible that another topology may provide superior performance. Hence, the synthesis of an optimum topology for a given specification remains to be done.

When large scale fabrications are involved, the network sensitivities could be the basis for the selection of topologies. The adjoint network method of evaluating the responses seems to be a proper step in that direction. The main advantage of using the adjoint network method is that all the first order partial derivatives for sensitivity analysis can be obtained using the results of the complete analysis of the circuit, regardless of the number of parameters involved, without actually perturbing them.

Cooled FET amplifiers show marked improvement in noise figure performance. A detailed analysis of FET amplifier performance as a function of temperature is of interest.

As reported in the first Chapter of the thesis, FETs may have appreciable power handling capabilities. This could lead to transmitter applications by paralleling a number of amplifiers. The analytical prediction of 1dB compression point of power amplifiers from the basic device parameter still remains a challenging problem.

Extensive reliability studies have been recently reported on GaAs FETs³⁸. Such detailed reliability studies on FET amplifiers is of current interest.

FET oscillators look promising for local oscillator applications. As an oscillator, it has low power consumption and low FM noise. Since the FET is a high impedance device, it does not lower the Q of the resonance circuit and hence good spectral purity signals can be obtained.

As a microwave mixing element, the FET exhibits large dynamic range with conversion gain, thus combining the best features of Schottky and tunnel diode mixers. Since it is a three terminal device, the FET provides better isolation between RF and IF ports than diode mixers.

Combining the design techniques of oscillators and mixers with that of amplifiers, presented in the thesis, it is possible to provide an integrated low noise front end design using only FETs. Such a compact front end could easily be mounted at the antenna, thus eliminating large signal losses in cables prior to pre-selection and down conversion.

APPENDIX ATHE COMPLETE SIGNAL FLOW GRAPH ANALYSIS FOR THE ERROR
MODEL

The signal flow graph which forms the basis for the analysis is given in Fig. 2.11. For the analysis of the input port, a unit reference signal is introduced from the left port and a similar application of signal is considered while the right port is analyzed. The open end effects of the transmission line are considered as a load with reflection coefficient Γ_L .

For the termination of input port with open, short and matched load, the following values are measured.

$$R_{FO} = S_{11}^{(1)} + \frac{S_{21}^{(1)} S_{12}^{(1)} \Gamma_L}{1 - S_{22}^{(1)} \Gamma_L} \quad (A.1)$$

$$R_{FS} = S_{11}^{(1)} - \frac{S_{21}^{(1)} S_{12}^{(1)}}{1 - S_{22}^{(1)}} \quad (A.2)$$

$$R_{Fm} = S_{11}^{(1)} \quad (A.3)$$

From the above equations, we can derive $S_{11}^{(1)}$, $S_{22}^{(1)}$ and $S_{12}^{(1)} S_{21}^{(1)}$ in terms of R_{FO} , R_{FS} , R_{Fm} .

From Eqn. (A.3),

$$S_{11}^{(1)} = R_{Fm} \quad (A.4)$$

From Eqns. (A.1) and (A.4),

$$S_{12}^{(1)} S_{21}^{(1)} = \frac{(R_{FO} - R_{FM})(1 - S_{22}^{(1)}) \Gamma_L}{\Gamma_L} \quad (A.5)$$

From Eqns. (A.2) and (A.4),

$$S_{12}^{(1)} S_{21}^{(1)} = -(R_{FS} - R_{FM})(1 + S_{22}^{(1)}) \quad (A.6)$$

From Eqns. (A.5) and (A.6),

$$(R_{FO} - R_{FM})(1 - S_{22}^{(1)}) \Gamma_L = -(R_{FS} - R_{FM})(1 + S_{22}^{(1)}) \Gamma_L$$

$$(R_{FO} - R_{FM})(-S_{22}^{(1)} \Gamma_L) + (R_{FS} - R_{FM}) S_{22}^{(1)} \Gamma_L$$

$$= -R_{FO} + R_{FM} - \Gamma_L (R_{FS} - R_{FM})$$

$$S_{22}^{(1)} \Gamma_L (R_{FS} - R_{FO}) = -R_{FO} - R_{FS} \Gamma_L + R_{FM} (1 + \Gamma_L)$$

$$S_{22}^{(1)} = \frac{R_{FO} + R_{FS} \Gamma_L - R_{FM} (1 + \Gamma_L)}{(R_{FO} - R_{FS})} \quad (A.7)$$

From Eqn. (A.6),

$$S_{21}^{(1)} S_{12}^{(1)} = -(R_{FS} - R_{FM})(1 + S_{22}^{(1)})$$

$$= -(R_{FS} - R_{FM}) \left(1 + \frac{R_{FO} + R_{FS} \Gamma_L - R_{FM} (1 + \Gamma_L)}{(R_{FO} - R_{FS})} \right)$$

$$= -(R_{FS} - R_{FM}) \left(\frac{R_{FO} - R_{FS} + R_{FO} + R_{FS} \Gamma_L - R_{FM} (1 + \Gamma_L)}{(R_{FO} - R_{FS})} \right)$$

Therefore,

$$S_{21}^{(1)} S_{12}^{(1)} = \frac{(R_{FS} - R_{Fm})}{(R_{FS} - R_{FO})} \{2R_{FO} + R_{FS}(\Gamma_L - 1) - R_{Fm}(1 + \Gamma_L)\} \quad (A.8)$$

Similarly, using the same procedure,

$$S_{11}^{(2)}, S_{22}^{(2)}, S_{12}^{(2)}, S_{21}^{(2)}$$

can be derived.

Applying the non-touching loop rule, the transmission coefficients with ports directly connected are:

$$T_{F1} = \frac{S_{21}^{(1)} S_{12}^{(2)}}{1 - S_{22}^{(1)} S_{22}^{(2)}} \quad (A.9)$$

in the forward direction and

$$T_{R1} = \frac{S_{12}^{(1)} S_{21}^{(2)}}{1 - S_{22}^{(1)} S_{22}^{(2)}} \quad (A.10)$$

in the reverse direction.

From Eqn. (A.9),

$$S_{21}^{(1)} S_{12}^{(2)} = T_{F1} (1 - S_{22}^{(1)} S_{22}^{(2)})$$

Substituting for $S_{22}^{(1)}$ from Eqn. (A.7) and similarly for $S_{22}^{(2)}$, we get:

$$S_{21}^{(1)} S_{12}^{(2)} = T_{F1} \left[1 - \left\{ \frac{R_{FO} + R_{FS} \Gamma_L - R_{Fm}(1 + \Gamma_L)}{(R_{FO} - R_{FS})} \right\} \left\{ \frac{R_{RO} + R_{RS} \Gamma_L - R_{Rm}(1 + \Gamma_L)}{(R_{RO} - R_{RS})} \right\} \right] \quad (A.11)$$

Similarly for $S_{12}^{(1)} S_{21}^{(2)}$ in Eqn. (A.10).

With the unknown two port inserted as shown in Fig. 2.11 and a unit reference signal introduced from the left, the following relationship applies:

$$a_1 = S_{21}^{(1)} + S_{22}^{(1)}(a_4) \quad (\text{A.12})$$

$$a_3 = S_{22}^{(2)}(a_2) \quad (\text{A.13})$$

The second term in a_3 is zero since no signal is applied from the right while unit signal is present at the input port.

$$R_F = S_{11}^{(1)} + S_{12}^{(1)} a_4 \quad (\text{A.14})$$

$$T_F = S_{12}^{(2)} a_2 \quad (\text{A.15})$$

where R_F and T_F represent the reflection coefficient at the input port and forward transmission coefficient with the device connected.

From Fig. 2.11,

$$\left. \begin{aligned} a_4 &= S_{11} a_1 + S_{12} a_3 \\ a_2 &= S_{21} a_1 + S_{22} a_3 \end{aligned} \right\} \quad (\text{A.16})$$

From Eqns. (A.14) and (A.15),

$$\left. \begin{aligned} a_4 &= \frac{R_F - S_{11}^{(1)}}{S_{12}^{(1)}} \\ a_2 &= T_F / S_{12}^{(2)} \end{aligned} \right\} \quad (\text{A.17})$$

Substituting Eqn. (A.17) in Eqns. (A.12) and (A.13),

$$a_1 = S_{21}^{(1)} + S_{22} \frac{(R_F - S_{11}^{(1)})}{S_{12}^{(1)}} \quad (A.18)$$

$$a_3 = S_{22}^{(2)} T_F / S_{12}^{(2)}$$

From Fig. 2.11,

$$\left. \begin{aligned} b_4 &= S_{11} b_1 + S_{12} b_3 \\ b_2 &= S_{21} b_1 + S_{22} b_2 \end{aligned} \right\} \quad (A.19)$$

Applying unit reference signal from right and evaluating b_s as for $a's$:

$$\begin{aligned} b_1 &= S_{22}^{(1)} \frac{T_R}{S_{12}^{(1)}} \\ b_2 &= \frac{R_R - S_{11}^{(2)}}{S_{12}^{(2)}} \\ b_3 &= S_{22}^{(2)} \left[\frac{R_R - S_{11}^{(2)}}{S_{12}^{(2)}} \right] + S_{21}^{(2)} \\ b_4 &= \frac{T_R}{S_{12}^{(1)}} \end{aligned} \quad (A.20)$$

From Eqns. (A.16) and (A.19),

$$\frac{a_4}{a_1} - \frac{a_3}{a_1} S_{12} = S_{11} = \frac{b_4}{b_1} - \frac{b_3}{b_1} S_{12}$$

$$\frac{a_4}{a_1} - \frac{b_4}{b_1} = \left(\frac{a_3}{a_1} - \frac{b_3}{b_1} \right) S_{12}$$

or

$$S_{12} = \frac{a_4 b_1 - b_4 a_1}{a_3 b_1 - a_1 b_3} \quad (\text{A.21})$$

Similarly,

$$S_{11} = \frac{a_3 b_4 - a_4 b_3}{a_3 b_1 - a_1 b_3} \quad (\text{A.22})$$

$$S_{22} = \frac{a_2 b_1 - b_2 a_1}{a_3 b_1 - a_1 b_3} \quad (\text{A.23})$$

$$S_{21} = \frac{a_2 b_3 - a_3 b_2}{a_3 b_1 - a_1 b_3} \quad (\text{A.24})$$

Consider the parameters of the Eqn. (A.21) and Eqns. (A.17), (A.18) and (A.20). Then,

$$a_3 b_1 = S_{12}^{(2)} S_{22}^{(1)} \frac{T_F T_R}{S_{12}^{(2)} S_{12}^{(1)}}$$

$$a_1 b_3 = [S_{12}^{(1)} S_{21}^{(1)} + S_{22}^{(1)} (R_F - S_{11}^{(1)})] \times \\ \frac{[S_{21}^{(2)} S_{12}^{(2)} + S_{22}^{(2)} (R_R - S_{11}^{(2)})]}{S_{12}^{(2)} S_{12}^{(1)}}$$

$$a_3 b_1 - a_1 b_3 = \frac{D}{S_{12}^{(2)} S_{12}^{(1)}}$$

where

$$D = \left\{ [S_{12}^{(1)} S_{21}^{(1)} + S_{22}^{(1)} (R_F - S_{11}^{(1)})] \times \right. \\ \left. [S_{21}^{(2)} S_{12}^{(2)} + S_{22}^{(2)} (R_R - S_{11}^{(2)})] \right. \\ \left. - S_{22}^{(2)} S_{22}^{(1)} T_R T_F \right\} \quad (A.25)$$

Similarly,

$$a_4 b_1 = \left(\frac{R_F - S_{11}^{(1)}}{S_{12}^{(1)}} \right) S_{22}^{(1)} \frac{T_R}{S_{12}^{(1)}} \\ a_1 b_4 = \frac{T_R}{S_{12}^{(1)}} \left(S_{21}^{(1)} + S_{22}^{(1)} \left(\frac{R_F - S_{11}^{(1)}}{S_{12}^{(1)}} \right) \right)$$

Therefore,

$$a_4 b_1 - b_4 a_1 = T_R \frac{S_{21}^{(1)}}{S_{12}^{(1)}}$$

Therefore,

$$S_{12} = \frac{a_4 b_1 - b_4 a_1}{a_3 b_1 - a_1 b_3} = \frac{T_R S_{21}^{(1)} S_{12}^{(2)}}{D} \quad (A.26)$$

Following similar steps,

$$S_{21} = \frac{T_F S_{12}^{(1)} S_{21}^{(2)}}{D} \quad (A.27)$$

$$S_{11} = \frac{(R_F - S_{11}^{(1)})[S_{22}^{(2)}(R_F - S_{11}^{(2)}) + S_{21}^{(2)}S_{12}^{(2)}] - S_{22}^{(2)}T_R T_F}{D} \quad (A.28)$$

$$S_{22} = \frac{(R_F - S_{11}^{(2)})[S_{22}^{(1)}(R_F - S_{11}^{(1)}) + S_{12}^{(1)}S_{21}^{(1)}] - S_{22}^{(1)}T_R T_F}{D} \quad (A.29)$$

The above equations are derived based on the method suggested by Kruppa³¹. The analysis presented here is more general and is suited for microstrip circuit applications.

APPENDIX BTHE COMPUTER PROGRAM 'NOISE'Purpose

This program determines the value of $F_{\min}$, R_o and X_o for various values of drain current and frequency of Schottky barrier FETs.

Language

Fortran IV

Availability

A listing with examples is included in this Appendix.

Description

The program follows the description of noise model and equations described in Section 2.6 of the main text. A flow chart summarizing the program is given in Figs. B.1 and B.2. After reading the required data, the S-parameter values corresponding to the required drain current and operating frequency are converted to the Y parameters. The program then determines the value of K corresponding to the given value of optimum noise figure within a tolerance limit Δ by iteration without exceeding the upper limit k_M . Once k is known, the other parameters can be easily evaluated using Eqns. (2.28) to (2.33).

Fig. B.1. Flow chart for program noise.

Fig. B.2. Flow chart for program noise.

Input Data

1) The first set of data required in G format are:

N_1 = number of sets of data

F_N = minimum noise factor F corresponding to some known drain current I_d and frequency F

C_R = correlation factor

$R = R_g + R_s$ (Fig. 2.5)

2) The second set of data in G format are:

C_D = operating drain current of the device

C_{DSS} = drain saturation current when $V_{GS}=0$

F = operating frequency of interest

3) The third set of data are the magnitude and angle of S-parameters in G format in the order S_{11} , S_{12} , S_{21} , S_{22} .

The first set of data is required only for the initial run. Once k is determined for the rest of the runs only the second and the third sets of data are required.

Output Data

The output is in F format for R_o , X_o , F_{min} , R_n , G_n and Z_c where

R_o = optimum source resistance for minimum noise figure

X_o = optimum source reactance for minimum noise figure

$F_{\min}$ = minimum noise factor corresponding to the required I_{DSS}
and F

R_n = noise resistance of the device

G_N = noise conductance of the device

Z_c = correlation noise impedance.

```

001 C *****
002 C THIS PROGRAM CALCULATES THE NOISE PARAMETERS OF FET FROM THE
003 C GIVEN SET OF DEVICE DATA
004 C *****
005 IMPLICIT REAL*8(A-H,O-Z)
006 DOUBLE COMPLEX S11,S12,S21,S22,Y11,Y12,Y21,Y22,Q,ZC
007 DOUBLE COMPLEX HC,AR,AI
008 READ(105,88) N1,FN,CR,R
009 OUTPUT N1,FN,CR,R
010 88 FORMAT(5G,0)
011 PI=3.1415692D0
012 N=1
013 100 READ(105,61) CD,CDSS,F
014 61 FORMAT(4G,0)
015 OUTPUT CD,CDSS,F
016 GG=PI/180.D0
017 READ(105,39) SM11,SA11,SM12,SA12,SM21,SA21,SM22,SA22
018 39 FORMAT(8G,0)
019 S11=SM11*DCMPLX(DCOS(GG*SA11),DSIN(GG*SA11))
020 S12=SM12*DCMPLX(DCOS(GG*SA12),DSIN(GG*SA12))
021 S21=SM21*DCMPLX(DCOS(GG*SA21),DSIN(GG*SA21))
022 S22=SM22*DCMPLX(DCOS(GG*SA22),DSIN(GG*SA22))
023 CALL CONV(S11,S12,S21,S22,Y11,Y12,Y21,Y22)
024 GGN=0.001D0
025 IF(N.GT.1) GO TO 47
026 CDNS=1.D0
027 47 GDN=CDNS*CD/CDSS*0.001D0
028 HC=Y11/Y21*(GDN**0.5D0)
029 HI=-((CR*(GGN**0.5D0))
030 HR=DREAL(HC)
031 HM=DIMAG(HC)
032 HI=HM+HI
033 Q=DCMPLX(HR,HI)
034 P=CDABS(Q)
035 GN=((P**2)+((1.D0-(CR**2))*GGN))

```

```

AY=CDABS(Y21)
D1=GDV/((AY**2)*((1.00-(CR**2))*GGN/GN*50.00
AR=GDV*DCONJG(Y11)/((AY**2)*GN)
AI=CR*((GGN*GDV)**0.500)/(Y21*GN)

```

```

FA=DREAL(AR)
FB=DIAG(AR)
GR=DREAL(AI)
GI=DIAG(AI)
FA=FA-GI
FB=FB+GR

```

```

Z=COMPLEX(FA,FB)*50.00

```

```

RN=R+DT
ZC=R+Z
DR=DREAL(ZC)
RSDP=((DR)**2.00+RN/GN)**0.500
FR=1.00+2.00*GN*(RSDP+DR)

```

```

IF(N.GT.1) GO TO 86

```

```

FD=FR-FN

```

```

DF=DABS(FD)

```

```

IF(DF.LE.0.100) GO TO 60

```

```

CONS=CONS+1.00

```

```

IF(CONS.GT.100.) GO TO 48

```

```

GO TO 47

```

```

60 OUTPUT CONS,D1,3,GN

```

```

86 ROP=((DR**2.00)+RN/GN)**0.500

```

```

XDP=-DIAG(ZC)

```

```

FMIN=1.00+(2.00*GN*(DR+ROP))

```

```

PRINT 404

```

```

404 FORMAT(6X,'F',5X,'ROP',5X,'XDP',5X,'FMIN',5X,'RN',5X,'GN',5X,'ZC')

```

```

WRITE(108,55)F,ROP,XDP,FMIN,RN,GN,ZC

```

```

55 FORMAT(6F8.3)

```

```

IF(N.EQ.N1) GO TO 48

```

```

N=N+1

```

```

GO TO 100

```

```

48 STOP

```

```

END

```

```

SUBROUTINE CONV(X1,X2,X3,X4,Y1,Y2,Y3,Y4)
IMPLICIT REAL*8(A-H,O-Z)

```

```
006      DOUBLE COMPLEX X1,X2,X3,X4,Y1,Y2,Y3,Y4,D
007      D=((1,D0+X1)*((1,D0+X4)-X2*X3)
008      Y1=((1,D0-X1)*((1,D0+X4)+X3*X2)/D
009      Y4=((1,D0-X4)*((1,D0+X1)+X2*X3)/D
010      Y2=-2.D0*X2/D
011      Y3=-2.D0*X3/D
012      RETURN
013      END
```

APPENDIX CPROGRAM 'DIMENSION'Purpose

This program is used for calculating the dimensions of microstrip circuit elements in alumina substrates.

Language

Fortran IV

Availability

A listing is included in this Appendix.

Description

A flowchart of the program is shown in Figs. C1, C2 and C3. The main program reads the data, calls the subroutine 'PARA' and prints out the dimensions of the circuit element in inches. The data includes the code numbers corresponding to the type of elements used in the circuit, from left to right. The first step in the subroutine is to test whether the element is a stub or a series matching section. If it is a stub, the program evaluates the dimensions of the stub with Eqns. (3.2) to (3.7) and end corrections (for open stubs) with Eqn. (3.10). The dimensions of the series matching sections are similarly calculated and the width corrections are made using Eqn. (3.11).

Once all the dimensions of the elements are thus computed, the

Fig. C1. Flow chart of the program for calculating microstrip elements in inches.

Fig. C2: Flow chart for subroutine para.

Fig. C3. Flow chart for Subroutine para (continued).

correction for abrupt impedance steps are then applied for series matching sections (Eqns. (3.12) to (3.15)).

Input Data

- (a) The first card reads C and NELM in G format where
- C = central frequency in GHz
 - NELM = number of elements.
- (b) The second card reads the type of elements (ET) in G format where
- ET=2 for series matching sections
 - =3 for open stubs
 - =4 for shorted stubs.
- (c) The third set of data in G format are Z and L where
- Z = the impedance of the elements in ohms
 - L = the length of the elements in wavelength.

Output Data

- (a) The first set of outputs consists of the input data, such as impedance Z and length L, in F9.3 format.
- (b) The second set of outputs are the dimensions corresponding to Z and L, namely WM and LM, after all the corrections for end effects and discontinuities are applied, in F8.3 format, where
- WM = width of elements in inches
 - LM = length of elements in inches

```

0001 - C *****
0002 C MICROSTRIP CIRCUIT ELEMENT DESIGN
0003 C *****
0004 IMPLICIT REAL*8(A-H,O-Z)
0005 REAL*8 L,LM
0006 DIMENSION LM(25),WM(25)
0007 COMMON PI,Z(25),L(25),ET(25),C,NELM
0008 PI=3.141500
0009 READ (105,51) C,NELM
0010 51 FORMAT(6G.0)
0011 OUTPUT C,NELM
0012 READ(105,99) (ET(I),I=1,NELM)
0013 99 FORMAT(25G.0)
0014 PRINT 77
0015 77 FORMAT(5X,'Z(I)',5X,'L(I)')
0016 DO 79 I=1,NELM
0017 READ (105,66) Z(I),L(I)
0018 66 FORMAT (2G.0)
0019 WRITE (108,71) Z(I),L(I)
0020 71 FORMAT(2F9.3)
0021 79 CONTINUE
0022 DO 264 I=1,NELM
0023 IF(ET(I).LT.6.00) GO TO 383
0024 LM(I)=0.00
0025 WM(I)=0.00
0026 GO TO 264
0027 383 CALL PARA(I,LM,WM)
0028 264 CONTINUE
0029 884 PRINT 823
0030 823 FORMAT(2X,'ET',5X,'WM-INCH',5X,'LM-INCH')
0031 DO 824 I=1,NELM
0032 WRITE(108,825) ET(I),WM(I),LM(I)
0033 825 FORMAT(3F8.3)
0034 824 CONTINUE
0035 STOP

```

END

```

=====
THIS PROGRAMME CALCULATES THE ALUMINA MICROSTRIP CIRCUIT
ELEMENTS IN INCHES
=====

```

```

SUBROUTINE PARA(I,LM,WM)
IMPLICIT REAL*8(A-H,O-Z)
REAL*8 L,LM
DIMENSION LM(25),WM(25),WL(25)
COMMON PI,Z(25),L(25),ET(25),C,NELM
ER=9.88
RH=0.025
F=C
DO 33 I=1,NELM
IF(ET(I).GT.6.00) GO TO 35
T1=(376.81900*PI)/(2.00*DSQRT(ER)*Z(I))
W1=(2.00*T1-1.00)
T2=LOG(W1)
W2=T1-1.00
Q1=(LOG(W2)+0.29300-(0.51700/ER))
T3=((ER-1.00)*Q1)/(2.00*ER)
T4=T1-(1.00+T2-T3)
WM=(2.00*T4)/PI
W1(I)=WM*WM
IF(W1.GE.1.00) GO TO 44
T1=(ER-1.00)/(ER+1.00)
T2=T1*(0.22600+0.1200/ER)
EP=ER+1
T3=(DSQRT(EP)*Z(I))/85.00
T4=T3+T2
W1=((DEXP(T4)/8.00)-(DEXP(-T4)/4.00))
WM=1.00/W1
W1(I)=WM*WM
44 Q1=1.00/DSQRT(1.00+(10.00*WM)/W1(I))
EE=((ER+1.00)/2.00+((ER-1.00)/2.00*Q1)*0.9800)
FD=6.00/(ER-1.00)*0.25
FO=FD*DSQRT(Z(I)/WM)
IF(F.LT.FO) GO TO 47

```

```

0001      IF(WH.LT.4) GO TO 57
0002      EZ=(ER**2-1.D0)*WH*3.D0*(10.**(-6.))
0003      ED=Z(I)*(WH**2)/3.D0
0004      ED=DSQRT(ED)*(F-FD)
0005      EE=(EZ*ED)+EE
0006      GO TO 47
0007      57      EZ=(ER**2-1.D0)*WH*3.D0*(10.**(-6.))
0008      ED=DSQRT(Z(I)*WH)*(F-FD)
0009      EE=EE+(EZ*ED)
0010      47      R1=30.D0/(2.54D0*C)
0011      R2=R1/DSQRT(EE)
0012      WL(I)=R2
0013      LM(I)=L(I)*R2
0014      IF (ET(I).EQ.2.D0) GO TO 34
0015      BR=2.D0*PI/R2
0016      BZ=2.D0*WH*DLOG(2.D0/PI)
0017      BS=BR*BZ
0018      B*=(4.*BZ+2.D0*WH(I))/((BZ+2.D0*WH(I))*DTAN(BS))
0019      DLH=1.D0/BR*DATAN(1.D0/B*)
0020      DL=DLH*WH
0021      IF(ET(I).EQ.4.D0) GO TO 33
0022      IF (LM(I).LT.0.05) GO TO 33
0023      LH(I)=LM(I)-DL
0024      GO TO 33
0025      35      LM(I)=0.
0026      WH(I)=0.
0027      GO TO 33
0028      34      IF(WH.GT.2.) GO TO 33
0029      BR=2.D0*PI/R2
0030      BZ=2.D0*WH*DLOG(2.D0/PI)
0031      BS=BR*BZ
0032      B*=(4.*BZ+2.D0*WH(I))/((BZ+2.D0*WH(I))*DTAN(BS))
0033      DWH=1.D0/BR*DATAN(1.D0/B*)
0034      DWH=DABS(DWH)
0035      IF (WH(I).LT.0.05) GO TO 33
0036      WH(I)=WH(I)-DWH*2.D0*WH
0037      33      CONTINUE
0038      CR=WH*DLOG(4.D0)/PI
0039      I=1
0040      99      IF(ET(I).EQ.2.D0) GO TO 55
0041      GO TO 66
0042      55      J=I+1
0043      IF(ET(J).EQ.2.D0) GO TO 77

```

```

GO TO 66
77 IF (WM(I).GE.WM(J)) GO TO 88
   WR=(WM(J)-WM(I))
   DK=((CR+2.DD*WR)/(4.DD*CR+2.DD*WR)*CR)
   PHI=1.5DD*WM(J)/WM(I)
   EL=PHI/360.*L(J)
   IF (LM(J).LT.0.075) GO TO 66
   LM(J)=LM(J)-DK-EL
   GO TO 66
88 WR=(WM(I)-WM(J))
   DK=((CR+2.DD*WR)/(4.DD*CR+2.DD*WR)*CR)
   PHI=1.5DD*WM(I)/WM(J)
   EL=PHI/360.*L(I)
   IF (LM(I).LT.0.075) GO TO 66
   LM(I)=LM(I)-DK-EL
   GO TO 66
66 IF I=I
   IF (I.LE.NELM) GO TO 99
   RETURN
END

```


APPENDIX DFET AMPLIFIER DESIGN PROGRAM

The details of the program are described in Chapter 5. This Appendix contains the details of the input data, the printout and the listing of the program.

The program requires input data in the following order.

- (a) The number of sets of data NU in G format.
- (b) The parameters C, NELM, $F_{\min}$, $F_{\max}$, N_1 and ATEN in G format where
 - C = central frequency GHz
 - NELM = number of elements on topology
 - $F_{\min}$ = minimum frequency in GHz for which analysis begins
 - $F_{\max}$ = maximum frequency in GHz for which analysis ends
 - N_1 = number of frequency sample points
 - ATEN = attenuation constant (dB/wavelength)
- (c) The code numbers of the type of elements ET(I) in G format where
 - ET=2 for series matching sections
 - =3 for open stubs
 - =4 for shorted stubs
 - =8 for series capacitance
 - =13 for the device S-parameters.

(d) The initial values of the elements in G format.

If ET=2,3,4, they are

Z = characteristic impedance in ohms

L = length in wavelength.

If ET=8, it is

Z = value of capacitance in p-farads.

If ET=13, they are

S_{11} (Mag, Angle), S_{12} (Mag, Angle), S_{21} (Mag, Angle), S_{22} (Mag, Angle)

where S_{11} , S_{22} , S_{12} , S_{21} are the measured S-parameters (total N_1 cards).

R_N , G_o , B_o , F_M

where

R_N = noise resistance (normalized)

G_o = optimum source conductance for minimum noise figure

B_o = optimum source susceptance for minimum noise figure

F_M = minimum noise figure

(total N_1 cards)

(e) The term N_{opt} , N_{MAG} in G format where

N_{opt} = 0 if optimization is not required

N_{opt} = 1 if optimization is required

N_{MAG} = 0 if the overall S-parameter printout is required in
magnitude, angle

NMAG = 1 if not

If $N_{opt} = 0$, the required data ends here.

- (f) The parameters $A_1, A_2, A_3, A_4, A_5, A_6, A_7, S_{FR}$ and G_R in G format where

A_1 = gain flatness weighting factor

A_2 = weighting factor for input return loss

A_3 = weighting factor for output return loss

A_4 = transducer gain weighting factor

A_5 = group delay weighting factor

A_6 = noise figure weighting factor

A_7 = gain-slope weighting factor

S_{FR} = lower limit in stability factor

G_R = the required gain.

- (g) The parameters ZU, ZD, LU and LD in G format where

ZU = upper limit in realizable impedance in ohms

ZD = lower limit in realizable impedance in ohms.

LU = upper limit in realizable length in wavelength

LD = lower limit in realizable length in wavelength.

- (h) The code number ' E_{opt} ' corresponding to the selection of elements for optimization in G format where

$E_{opt} = 1$ if both Z and L are to be optimized

$E_{opt} = 0$ if element is not to be optimized

(total NELN entires in one card).

(i) The parameters DZ and DL in G format where

DZ = step size in ohms for initial iteration

DL = step size in wavelength for initial iteration

The output contains the following:

- 1) C, NELM, $F_{\min}$, $F_{\max}$, N_1 and ATEN in F format.
- 2) Element number, Z, L in F format for each element.
- 3) All the input data from e to i in G format.
- 4) Optimized value of each element in G format if optimization is sought for, and the following responses in F format:
 - a) Power gain vs frequency
 - b) Input return loss vs frequency
 - c) Output return loss vs frequency
 - d) Group delay vs frequency
 - e) Noise figure vs frequency
 - f) Gain slope vs frequency
 - g) Stability factor vs frequency.
- 5) Overall S-parameters in magnitude and angle with frequency, if asked for.

THIS PROGRAM MAY BE USED FOR THE ANALYSIS AND OPTIMIZATION OF
MICROSTRIP CIRCUIT ELEMENTS AND FOR TRANSISTOR AMPLIFIER DESIGN

IMPLICIT REAL*8(A-H,O-Z)

REAL*8 L,LU,LD,LI,LP

DOUBLE COMPLEX S,Y11,Y12,Y21,Y22,S1,S2,S3,S4,AB,S11,S12,S21,S22

DIMENSION D(20,5),B(20,5),ZC(20,5),AV(20,5),S(20)

DIMENSION IRET(20),DELAY(20),GAIN(20),STBL(20),ORET(20)

DIMENSION X(20),T(20),Q(20),SLOPE(20)

DIMENSION XX(25),ZP(25),LP(25),FNOISE(25),FNF(25)

COMMON S11(5,10),S12(5,10),S21(5,10),S22(5,10)

1 ,RN(5,10),GO(5,10),BO(5,10),FM(5,10)

1 ,AB(4),PI,Z(25),L(25),ET(25),ATEN,SF,C,SFR,FMAX,FMIN,U(10)

1 ,EOPT(25),GR,A1,A2,A3,A4,A5,A6,A7,N1,NELM,MW

NU=NUMBER OF SET OF DATA

READ (105,59) NU

59 FORMAT(G,0)

DO 700 INDEX=1,NU

PI=3.141569200

MW=0

=====

READ IN THE FOLLOWING PARAMETERS

1) C=CENTER FREQUENCY

2)=== NUMBER OF THE ELEMENTS

3) FMIN=MINIMUM FREQUENCY FOR WHICH ANALYSIS BEGINS

4) FMAX= MAXIMUM FREQUENCY AT WHICH ANALYSIS ENDS

5) N1=NUMBER OF FREQUENCY SAMPLE POINTS

6) ATEN=ATTENUATION CONSTANT (DB/WAVELENGTH)

=====

READ(105,51)C,NELM,FMIN,FMAX,N1,ATEN

```

031      51      FORMAT(7G,0)
032      C      *****
033      C      READ IN ELEMENT TYPES, STARTING WITH LEFT MOST ELEMENT
034      C      *****
035      READ (105,99) (ET(I), I=1,NELM)
036      99      FORMAT(25G,0)
037      DO 40 I=1,NELM
038      C      *****
039      C      NOW READ IN THE ELEMENT VALUES
040      C      *****
041      IF(ET(I).LE.6.00) GO TO 21
042      IF(ET(I).EQ.13.00) GO TO 22
043      C      READ IN THE LUMPED VALUE
044      C      FOR RESISTANCE-OMHS ,CAPC-PEFARADS ,INDUC-MHENRY
045      READ(105,25) Z(I)
046      L(I)=0.00
047      25      FORMAT(G,0)
048      GO TO 40
049      C      READ 1)IMPEDANCE 2)LENGTH(WAVELENGTH) OF LINE OR STUB
050      21      READ(105,66) Z(I),L(I)
051      66      FORMAT(2G,0)
052      GO TO 40
053      22      CONTINUE
054      IF(MV.GT.0) GO TO 272
055      MV=I
056      272      GG=PI/180.00
057      Z(I)=0.00
058      L(I)=0.00
059      C      READ S MATRIX IN THE ORDER S11(MAG,DEG),S12(MAG,DEG)
060      C      S21(MAG,DEG),S22(MAG,DEG),ONE SET FOR N1 FREQUENCIES
061      DO 20 J=1,N1
062      READ(105,39) SM11,SA11,SM12,SA12,SM21,SA21,SM22,SA22
063      39      FORMAT(8G,0)
064      S11(I,J)=SM11*DCMPLX(DCOS(GG*SA11),DSIN(GG*SA11))
065      S21(I,J)=SM21*DCMPLX(DCOS(GG*SA21),DSIN(GG*SA21))
066      S12(I,J)=SM12*DCMPLX(DCOS(GG*SA12),DSIN(GG*SA12))
067      S22(I,J)=SM22*DCMPLX(DCOS(GG*SA22),DSIN(GG*SA22))
068      20      CONTINUE
069      C      RV=NOISE RESISTANCE
070      C      GO=OPTIMUM SOURCE CONDUCTANCE
071      C      BO=OPTIMUM SOURCE SUSCEPTANCE FOR N.F
072      C      FM=MIN NF AT THE LOWEST FREQ
073      DO 588 J=1,N1

```

```

074      READ(105,788) RN(I,J),GO(I,J),RO(I,J),FM(I,J)
075      788      FORMAT(4G,0)
076      588      CONTINUE
077      40       CONTINUE
078      715      WRITE(108,31) C,NELM,FMIN,FMAX,N1,ATEN
079      31       FORMAT(/'CENTER FREQ=' , F6.2, ' * ELEMENTS=' , I3,
080      1         ' FMIN=' , F6.2, ' FMAX=' , F6.2, ' FREQS=' , I3,
081      2         ' ATEN=' , F6.2)
082      OUTPUT ELEMENT #      ELEMENT TYPE      Z(I)      L(I)
083      WRITE(108,32) (I,ET(I),Z(I),L(I),I=1,NELM)
084      32       FORMAT( I6,F13.1, F15.3, F12.3)
085      C
086      C *****
087      C NOPT=0 IF OPTIMIZATION IS NOT REQUIRED
088      C NOPT=1 IF OPTIMIZATION IS REQUIRED
089      C NMAG=0 IF S PARAMETERS ARE TO CONVERTED INTO MAG,ANGLE
090      C AND NMAG=1 IF NOT
091      READ(105,789) NOPT,NMAG
092      789      FORMAT(2G,0)
093      OUTPUT NOPT,NMAG
094      IF(NOPT.EQ.0) GO TO 822
095      C
096      C -----
097      C READ DATA FOR OPTIMISATION
098      C -----
099      C SFR=LOWER LIMIT IN STABILITY FACTOR
100      C A1=GAIN FLATNESS WEIGHTING FACTOR
101      C A2=WEIGHTING FACTOR FOR INPUT RETURN LOSS
102      C A3=WEIGHTING FACTOR FOR OUTPUT RETURN LOSS
103      C A4=TRANSJUSER GAIN WEIGHTING FACTOR
104      C A5=GROUP DELAY WEIGHTING FACTOR
105      C A6=NOISE FIGURE WEIGHTING FACTOR
106      C A7=GAIN SLOPE WEIGHTING FACTOR
107      C GR=THE REQUIRED GAIN
108      READ(105,499) A1,A2,A3,A4,A5,A6,A7,SFR,GR
109      499      FORMAT(9G,0)
110      OUTPUT A1,A2,A3,A4,A5,A6,SFR,GR
111      C
112      C ZU=UPPER LIMIT OF REALIZABLE IMPEDENCE
113      C ZD=LOWER LIMIT OF REALIZABLE IMPEDENCE
114      C LJ=UPPER LIMIT REALYZABLE LENGTH WAVELENGTH
115      C LD=LOWER LIMIT REALYZABLE LENGTH WAVELENGTH
116      READ (105,599) ZU,ZD,LJ,LD

```

```

117 599 FORMAT (4G,0)
118      OUTPJT ZU,ZD,LU,LD
119 C
120 C      EDPT=1. IF BOTH Z(I) AND L(I) ARE TO BE OPTIMISED
121 C      EDPT=0 IF NO ELEMENT IS TO BE OPTIMISED
122      READ (105,699)(EDPT(I), I=1,NELM)
123 599 FORMAT(25G,0)
124      PRINT 444
125 444 FORMAT('EDPTI IS AS FOLLOWS')
126      WRITE(108,30)(EDPT(I), I=1,NELM)
127 30 FORMAT(20F4,0)
128 C
129 C      DZ=STEP SIZE IN OHMS FOR INITIAL ITERATION
130 C      DL=STEP SIZE IN WAVELENGTH FOR INITIAL ITERATION
131      READ (105,785) DZ,DL
132 785 FORMAT (2G,0)
133      OUTPUT DZ,DL
134 C
135 C      *****
136 C      OPTIMISATION PROGRAMME BEGINS HERE
137 C      *****
138 C
139      KK=1
140      LL=0
141      K=0
142      CALL EVAL(K,LL,SFFI,E,ZI,LI)
143      ES=E
144      ED=E
145      F=FMIN
146      DF=(FMAX-FMIN)/(N1-1)
147      DO 687 I=1,NELM
148          ZP(I)=Z(I)
149          LP(I)=L(I)
150 687 CONTINUE
151 330      K=1
152          LL=1
153 300      ZI=Z(K)
154          LI=L(K)
155          IF (EDPT(K).EQ.0.) GO TO 150
156          ZI=ZI+DZ
157          CALL EVAL(K,LL,SFFI,E,ZI,LI)
158          EPMIN=E
159          ZI=ZI-(2*DZ)

```



```

160 CALL EVAL(K,LL,SFFI,E,ZI,LI)
161 ENMIN=E
162 IF (EPMIN,GE,ENMIN) GO TO 260
163 IF (EPMIN,GT,ED) GO TO 146
164 YY=1.
165 GO TO 140
166 260 IF (ENMIN,GT,ED) GO TO 146
167 YY=2.
168 GO TO 140
169 146 YY=3.
170 140 ZI=ZI+DL
171 LI=LI+DL
172 CALL EVAL(K,LL,SFFI,E,ZI,LI)
173 EPMIN=E
174 LI=LI-(2*DL)
175 CALL EVAL(K,LL,SFFI,E,ZI,LI)
176 ENMIN=E
177 LI=LI+DL
178 IF (EPMIN,GE,ENMIN) GO TO 360
179 IF (EPMIN,GT,ED) GO TO 362
180 IF (YY,EQ,3.) XX(K)=5.
181 IF (YY,EQ,1.) XX(K)=1.
182 IF (YY,EQ,2.) XX(K)=2.
183 GO TO 150
184 360 IF (ENMIN,GT,ED) GO TO 362
185 IF (YY,EQ,1.) XX(K)=3.
186 IF (YY,EQ,3.) XX(K)=6.
187 IF (YY,EQ,2.) XX(K)=4.
188 150 IF (EDPT(K),EQ,0.) XX(K)=0.
189 Z(K)=ZI
190 L(K)=LI
191 K=K+1
192 IF (K,LE,NELM) GO TO 300
193 GO TO 270
194 362 IF (YY,EQ,1.) XX(K)=7.
195 IF (YY,EQ,2.) XX(K)=8.
196 IF (YY,EQ,3.) XX(K)=0.
197 GO TO 150
198 270 DO 200 I=1,NELM
199 ZI=Z(I)
200 LI=L(I)
201 IF (XX(I),EQ,1.) GO TO 210
202 IF (XX(I),EQ,2.) GO TO 220

```

```

3      IF (XX(I).EQ.3.) GO TO 230
4      IF (XX(I).EQ.0.) GO TO 203
5      IF (XX(I).EQ.5.) GO TO 213
6      IF (XX(I).EQ.6.) GO TO 223
7      IF (XX(I).EQ.7.) GO TO 233
8      IF (XX(I).EQ.8.) GO TO 243
9      Z(I)=ZI-DZ
10     L(I)=LI-DL
11     IF (Z(I).LT.ZD) Z(I)=ZD
12     IF (L(I).LT.LD) L(I)=LD
13     GO TO 200
14     210 Z(I)=ZI+DZ
15     L(I)=LI+DL
16     IF (Z(I).GT.ZU) Z(I)=ZU
17     IF (L(I).GT.LU) L(I)=LU
18     GO TO 200
19     220 Z(I)=ZI-DZ
20     L(I)=LI+DL
21     IF (Z(I).LT.ZD) Z(I)=ZD
22     IF (L(I).GT.LU) L(I)=LU
23     GO TO 200
24     203 Z(I)=ZI
25     L(I)=LI
26     GO TO 200
27     213 Z(I)=ZI
28     L(I)=LI+DL
29     IF (L(I).GT.LU) L(I)=LU
30     GO TO 200
31     223 Z(I)=ZI
32     L(I)=LI-DL
33     IF (L(I).LT.LD) L(I)=LD
34     GO TO 200
35     233 Z(I)=ZI+DZ
36     L(I)=LI
37     IF (Z(I).GT.ZU) Z(I)=ZU
38     GO TO 200
39     243 Z(I)=ZI-DZ
40     L(I)=LI
41     IF (Z(I).LT.ZD) Z(I)=ZD
42     GO TO 200
43     230 Z(I)=ZI+DZ
44     L(I)=LI-DL
45     IF (Z(I).GT.ZU) Z(I)=ZU

```

```

246      IF (L(I).LT.LD) L(I)=LD
247      200  CONTINUE
248          LL=0
249          K=0
250          CALL EVAL(K,LL,SFF1,E,ZI,LI)
251          IF (E.GT.ES) GO TO 265
252          ES=E
253          DO 333 I=1,NELM
254              ZP(I)=Z(I)
255              LP(I)=L(I)
256          333 CONTINUE
257              GO TO 270
258          265 DO 267 I=1,NELM
259              Z(I)=ZP(I)
260              L(I)=LP(I)
261          267 CONTINUE
262              ED=ES
263              KK=KK+1
264              IF (KK.LE.2.) GO TO 330
265              IF (KK.GE.5.) GO TO 828
266              DZ=DZ/2,1600
267              DL=DL/2,1600
268              GO TO 330
269      C      THE OPTIMISED Z(I) AND L(I) ARE AS FOLLOWS
270      828 PRINT 212
271      212 FORMAT (9X,'I',5X,'OPT Z(I)',8X,'OPT L(I)')
272          DO 777 I=1,NELM
273              WRITE (108,215) (I,Z(I),L(I))
274          215 FORMAT(3G10.3)
275          777 CONTINUE
276      C
277      C -----
278      822 F=FMIN
279          DF=(FMAX-FMIN)/(N1-1)
280      C =====
281      C COMPUTE THE GAIN, STABIL. FAC, AND RETURN LOSS AS FUNC OF THE FRE
282      C Q. AT THE SAME TIME OBTAIN THE S21 OF THE CGT AS FUNCTION OF FREQ
283      C IN PREP. FOR GROUP DELAY ANALYSIS (S(I))
284      C =====
285          LL=0.
286          K=0
287          DO 101 J=1,N1
288          CALL ABCD(F,J,LL,K,ZI,LI,FNF)

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289 CALL YBC(AB,Y11,Y12,Y21,Y22)
290 CALL CONV(Y11,Y12,Y21,Y22,S1,S2,S3,S4)
291 S(J)=S3
292 GAIN(J)=20.*DLOG10(CDABS(S3))
293 IRETL(J)=-20.*DLOG10(CDABS(S1))
294 DRETL(J)=-20.*DLOG10(CDABS(S4))
295 STBL(J)=(1+CDABS(S1)*S4-S3*S2)**2-CDABS(S1)**2-CDABS(S4)**2)
296 /((2*CDABS(S3)*CDABS(S2)))
297 FNOISE(J)=10.*DLOG10(FNF(J))
298 IF(NMAG.EQ.1) GO TO 849
299 D(J,1)=DREAL(S1)
300 D(J,2)=DREAL(S2)
301 D(J,3)=DREAL(S3)
302 D(J,4)=DREAL(S4)
303 B(J,1)=DIMAG(S1)
304 B(J,2)=DIMAG(S2)
305 B(J,3)=DIMAG(S3)
306 B(J,4)=DIMAG(S4)
307 849 F=F+DF
308 101 CONTINUE
309 C *****
310 X(1)=FMIN
311 DO 155 I=2,N1
312 X(I)=X(I-1)+DF
313 155 CONTINUE
314 DO 869 I=1,N1
315 TA1=DIMAG(S(I))
316 TA2=DREAL(S(I))
317 T(I)=ATAN2(SNGL(TA1),SNGL(TA2))
318 869 CONTINUE
319 CALL GDGS(X,T,N1,DELAY)
320 DO 889 I=1,N1
321 D(I)=20.*DLOG10(CDABS(S(I)))
322 889 CONTINUE
323 CALL GDGS(X,D,N1,SLOPE)
324 DO 979 I=1,N1
325 SLOPE(I)=(SLOPE(I))*2.*PI/1000,
326 979 CONTINUE
327 C *****
328 F=FMIN
329 WRITE(108,235)
330 235 FOR*AT(1 FREQ, GAIN STBL, GRP,DEL, IRETL, FNOISE.
331 1 SLOPE, DRETL, 1/1 (GHZ) (DB) (NUM.) (NSEC) (DB)

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0332      1  I(DB)  (DB/MHZ)  (DB)  I)
0333      DO 996 I=1,N1
0334      WRITE (108,234) F,GAIN(I),STBL(I),DELAY(I),IRETL(I),FNOISE(I)
0335      1  ,SLOPE(I),ORETL(I)
0336      F=F+DF
0337      996  CONTINUE
0338      234  FORMAT (2X,F4.2,5F8.3,F10.4,F8.3)
0339      IF(NMAG.EQ.1) GO TO 177
0340      PRINT 477
0341      477  FORMAT(9X,'SM11',5X,'SA11',5X,'SM12',5X,'SA12',5X,'SM21',5X,
0342      1  'SA21',5X,'SM22',5X,'SA22')
0343      J=1
0344      176  DO 145 I=1,4
0345      ZC(J,I)=DSORT(D(J,I)**2+B(J,I)**2)
0346      AN(J,I)=180./(PI)*ATAN2(B(J,I),D(J,I))
0347      145  CONTINUE
0348      WRITE(108,578) J,ZC(J,1),AN(J,1),ZC(J,2),AN(J,2),ZC(J,3),AN(J,3),
0349      1  ZC(J,4),AN(J,4)
0350      578  FORMAT(12,8F4.3)
0351      J=J+1
0352      IF(J.GT.N1) GO TO 177
0353      GO TO 176
0354      177  GO TO 700
0355      700  CONTINUE
0356      STOP
0357      END

```

```

0001      C
0002      C
0003      C  *****
0004      C  THIS SUBROUTINE COMPUTES ABCD MATRIX OF CASCADED ELEMENTS
0005      C  *****
0006      SUBROUTINE ABCD(F,J,LL,K,ZI,LI,FNF)
0007      IMPLICIT REAL*8(A-M,G-Z)
0008      REAL*8 L,LI
0009      DOUBLE COMPLEX S11,S12,S21,S22,AB,BL,A,AC,YS
0010      1  ,Y1,Y2,Y3,Y4,S1,S2,S3,S4,FF,AD,ZC,ZS,AA
0011      DIMENSION AC(4),A(4),AA(4),AD(4),FV(10),FNF(20)
0012      COMMON S11(5,10),S12(5,10),S21(5,10),S22(5,10)
0013      1  ,RV(5,10),GO(5,10),BO(5,10),FM(5,10)
0014      ,AB(4),PI,Z(25),L(25),ET(25),ATEN,SF,C,SFR,FMAX,FMIN,U(10)
0015      1  ,EDPT(25),GR,A1,A2,A3,A4,A5,A6,A7,V1,VELM,M
      JJ=1

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```

016      KK=1
017      FNF(J)=1.00
018      ZD=50.00
019      FF=DCMPLX(0.00,1.00)
020      C =====
021      C THIS PART DETERMINES THE ELEMENT TYPES ET(I) AND PROCEEDS
022      C TO THE RIGHT PART OF THE ROUTINE TO COMPUTE THE THE ELEMENT
023      C ARCS
024      CC =====
025      AB(1)=DCMPLX(1.00,0.00)
026      AB(2)=DCMPLX(0.00,0.00)
027      AB(3)=DCMPLX(0.00,0.00)
028      AB(4)=DCMPLX(1.00,0.00)
029      IF (LL.EQ.0.) GO TO 100
030      Z(K)=ZI
031      L(K)=LI
032      100 DO 55 I=1,NELM
033      BL=L(J)*F/C*DCMPLX(ATEV/8.68600,2.*PI)
034      A(1)=DCMPLX(1.00,0.00)
035      A(4)=DCMPLX(1.00,0.00)
036      IF(ET(I).EQ.2.00) GO TO 2
037      IF(ET(I).EQ.3.00) GO TO 3
038      IF(ET(I).EQ.4.00) GO TO 4
039      IF(ET(I).EQ.8.00) GO TO 5
040      IF(ET(I).EQ.13.00) GO TO 11
041      C =====
042      C THE ELEMENT IS A SERIES TRANS. LINE
043      C =====
044      2 A(1)=CDCOSH(BL)
045      A(4)=A(1)
046      A(2)=Z(I)/70*CDSINH(BL)
047      A(3)=70/Z(I)*CDSINH(BL)
048      GO TO 30
049      C =====
050      C THE ELEMENT IS AN OPEN CCT SHUNT STUB
051      C =====
052      3 A(2)=DCMPLX(0.00,0.00)
053      A(3)=Z0*CDTANH(BL)/Z(I)
054      GO TO 30
055      C =====
056      C THE ELEMENT IS A SHORT CIRCUITED SHUNT STUB
057      C =====
058      4 A(2)=DCMPLX(0.00,0.00)

```

A(3)=50./(Z(I)*COTAN4(BL))

GO TO 30

C =====

C COMPUTE ABCD OF SERIES CAPAC.

C Z(I)=THE CAPAC. VALUE IN PF

C =====

5 A(2)=-FF/(2.00*PI*F*Z(I)*Z0)

A(3)=0.

GO TO 30

C =====

C THIS SEC COMPUTES THE ABCD OF THE TRANSISTOR GIVEN (S) MATRIX

C =====

11 S1=S11(I,JJ)

S2=S12(I,JJ)

S3=S21(I,JJ)

S4=S22(I,JJ)

JJ=JJ+1

CALL CONV(S1,S2,S3,S4,Y1,Y2,Y3,Y4)

CALL ABC(A,Y1,Y2,Y3,Y4)

30 AC(1)=AB(1)*A(1)+AB(2)*A(3)

AC(2)=AB(1)*A(2)+AB(2)*A(4)

AC(3)=AB(3)*A(1)+AB(4)*A(3)

AC(4)=AB(3)*A(2)+AB(4)*A(4)

AB(1)=AC(1)

AB(2)=AC(2)

AB(3)=AC(3)

AB(4)=AC(4)

C =====

C THE NOISE FIGURE FOR EACH FREQUENCY IS CALCULATED BELOW

C =====

M=J+1

IF(ET(M).LT.13.00) GO TO 55

FD=FM(M,J)

FD=DEXP(2.3025900*FD/10.00)

RD=S11(M,J)

ZC=(1.00+RD)/(1.00-RD)*Z0

AA(1)=DC*PLX(1.00,0.00)

AA(2)=DC*PLX(0.00,0.00)

AA(3)=Z0/ZC

AA(4)=DC*PLX(1.00,0.00)

AD(1)=AB(1)*AA(1)+AB(2)*AA(3)

AD(2)=AB(1)*AA(2)+AB(2)*AA(4)

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02      AD(3)=AB(3)*AA(1)+AB(4)*AA(3)
03      AD(4)=AB(3)*AA(2)+AB(4)*AA(4)
04      CALL YBC(AD,Y1,Y2,Y3,Y4)
05      CALL CONV(Y1,Y2,Y3,Y4,S1,S2,S3,S4)
06      U(KK)=(CDABS(S3))*2
07      CALL YBC(AB,Y1,Y2,Y3,Y4)
08      CALL CONV(Y1,Y2,Y3,Y4,S1,S2,S3,S4)
09      ZS=(1.00+S4)/(1.00-S4)*Z0
10      YS=Z0/ZS
11      GS=DREAL(YS)
12      BS=DIMAG(YS)
13      IF (GS.LT.0.01) GS=0.01
14      FN(KK)=FD+(RN(M,J))*((GS-GO(M,J))*2+(BS-BO(M,J))*2))/GS
15      IF(KK.LE.1) GO TO 979
16      FNF(KK)=FNF(KK-1)+((FN(KK)-1.00)/U(KK))
17      GO TO 969
18      979 FNF(KK)=FN(KK)
19      969 KK=KK+1
20      FNF(J)=FNF(KK-1)
21      55 CONTINUE
22      RETURN
23      END

```

```

001      C
002      C
003      C =====
004      C THIS SUBROUTINE CONVERTS X TO Y MATRIX OR THE OTHER WAY ROJD
005      C =====
006      SUBROUTINE CONV(X1,X2,X3,X4,Y1,Y2,Y3,Y4)
007      IMPLICIT REAL*8(A-H,O-Z)
008      DOUBLE COMPLEX X1,X2,X3,X4,Y1,Y2,Y3,Y4,D
009      D=((1.00+X1)*(1.00+X4)-X2*X3)
010      Y1=((1.00-X1)*(1.00+X4)+X3*X2)/D
011      Y4=((1.00-X4)*(1.00+X1)+X2*X3)/D
012      Y2=-2.00*X2/D
013      Y3=-2.00*X3/D
014      RETURN
015      END

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0001      C
0002      C

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003 C
004 C =====
005 C CONVERTS (Y) PARAMETERS TO ABCD MATRIX
006 C (Y) PARAMETERS MUST BE NORMALISED
007 C =====
008 C SUBROUTINE ABC(A,Y1,Y2,Y3,Y4)
009 C IMPLICIT REAL*8(A-H,I-Z)
010 C DOUBLE COMPLEX A,Y1,Y2,Y3,Y4
011 C DIMENSION A(4)
012 C A(1)=-Y4/Y3
013 C A(2)=-1.00/Y3
014 C A(3)=Y2-Y4*Y1/Y3
015 C A(4)=-Y1/Y3
016 C RETURN
017 C END

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001 C
002 C =====
003 C THIS SUBROUTINE CONVERTS ABCD MATRIX TO (Y)
004 C =====
005 C SUBROUTINE YBC(A,Y1,Y2,Y3,Y4)
006 C IMPLICIT REAL*8(A-H,I-Z)
007 C DOUBLE COMPLEX A,Y1,Y2,Y3,Y4
008 C DIMENSION A(4)
009 C Y1=A(4)/A(2)
010 C Y3=-1.00/A(2)
011 C Y4=A(1)/A(2)
012 C Y2=A(3)-A(1)*A(4)/A(2)
013 C RETURN
014 C END
015 C

```

```

001 C
002 C
003 C
004 C
005 C *****
006 C THIS SUBROUTINE CALCULATES SPLINE COEFFICIENTS AND SLOPE
007 C *****
008 C SUBROUTINE GSGS(X,Y,M,G)
009 C IMPLICIT REAL*8(A-H,I-Z)

```

```

010 REAL*8 KP, KM
011 DIMENSION X(20), Y(20), D(20), P(20), E(20), C(4,20), A(20,3), B(20)
012 , Z(20), G(20)
013 PI=3.141569
014 KM=-1
015 DO 2 K=1, KM
016 D(K)=X(K+1)-X(K)
017 P(K)=D(K)/6
018 2 E(K)=(Y(K+1)-Y(K))/D(K)
019 DO 3 K=2, KM
020 3 P(K)=E(K)-E(K-1)
021 A(1,2)=-1.-D(1)/D(2)
022 A(2,3)=P(2)-P(1)*A(1,3)
023 A(2,2)=2.*(P(1)+P(2))-P(1)*A(1,2)
024 A(2,3)=A(2,3)/A(2,2)
025 B(2)=B(2)/A(2,2)
026 DO 4 K=3, KM
027 A(K,2)=2.*(P(K-1)+P(K))-P(K-1)*A(K-1,3)
028 B(K)=B(K)-P(K-1)*B(K-1)
029 A(K,3)=P(K)/A(K,2)
030 4 B(K)=B(K)/A(K,2)
031 D= D(4-2)/D(4-1)
032 A(4,1)=1.+2+A(4-2,3)
033 A(4,2)=-D-A(4,1)*A(4-1,3)
034 B(4)=B(4-2)-A(4,1)*B(4-1)
035 Z(4)=B(4)/A(4,2)
036 KM=K-2
037 DO 6 I=1, KM
038 K=K-I
039 Z(K)=B(K)-(A(K,3)*Z(K+1))
040 6 CONTINUE
041 Z(1)=-A(1,2)*Z(2)-A(1,3)*Z(3)
042 DO 7 K=1, KM
043 Q=1./(6.*D(K))
044 C(1,K)=Z(K)*Q
045 C(2,K)=7(K+1)*Q
046 C(3,K)=Y(K)/D(K)-7(K)*P(K)
047 C(4,K)=Y(K+1)/D(K)-Z(K+1)*P(K)
048 7 CONTINUE
049 DO 50 I=2, KM
050 XINT=X(I)-0.0027800
051 CALL SPLINE(X,Y,M,C,XINT,YINT)
052 KM=YINT

```

```

0053      XINT=X(1)+0.0027800
0054      CALL SPLINE(X,Y,M,C,XINT,YINT)
0055      KP=YINT
0056      G(1)=(KP-KM)/(4.*PI*0.0027800)
0057 50      CONTINUE
0058      XINT=X(1)+0.0027800
0059      CALL SPLINE(X,Y,M,C,XINT,YINT)
0060      G(1)=(YINT-Y(1))/(2.*PI*0.0027800)
0061      XINT=X(M)-0.0027800
0062      CALL SPLINE(X,Y,M,C,XINT,YINT)
0063      G(M)=(Y(M)-YINT)/(2.*PI*0.00278)
0064      RETURN
0065      END

```

```

0001      C
0002      C
0003      C
0004      C
0005      C
0006      C
0007      *****
0008      THIS SUBROUTINE CALCULATES CURVE POINTS FOR ANY FREQUENCY
0009      *****
0010      SUBROUTINE SPLINE(X,Y,M,C,XINT,YINT)
0011      IMPLICIT REAL*8(A-H,O-Z)
0012      DIMENSION X(20),Y(20),C(4,20)
0013      IF(XINT-X(1))7,1,2
0014      1      YINT=Y(1)
0015      GO TO 11
0016      2      K=1
0017      IF(XINT-X(K+1))6,4,5
0018      3      YINT=Y(K+1)
0019      GO TO 11
0020      4      K=K+1
0021      IF(M-K)7,7,3
0022      5      YINT=(X(K+1)-XINT)*(C(1,K)*(X(K+1)-XINT)**2+C(3,K))
0023      YINT=YINT+(XINT-X(K))*(C(2,K)*(XINT-X(K))**2+C(4,K))
0024      GO TO 11
0025      6      PRINT 101
0026      101      FORMAT(2X,'OUT OF RANGE FOR INTERPOLATION')
0027      RETURN
0028      END

```

0001 C

```

02 C
03 C
04 C *****
05 C SUBROUTINE EVAL COMPUTES THE OBJECTIVE FUNCTION WHICH
06 C IS TO BE MINIMISED AND ALSO MINIMUM STBLTY FACTOR
07 C *****
08 SUBROUTINE EVAL(K,LL,SFFI,E,ZI,LI)
09 IMPLICIT REAL*8(A-H,O-Z)
10 REAL*8 L,LI
11 DOUBLE COMPLEX S1,S2,S3,S4,S11,S12,S21,S22,AB,Y11,Y12,Y21,Y22,S
12 DIMENSION S(20),SFF(20),X1(20),X2(20),X3(20),DELAY(20),FNF(20)
13 1 ,FR(20),X(20),T(20),Q(20),SLOPE(20)
14 COMMON S11(5,10),S12(5,10),S21(5,10),S22(5,10)
15 1 ,RN(5,10),GO(5,10),RO(5,10),FM(5,10)
16 1 ,AB(4),PI,Z(25),L(25),ET(25),ATEN,SF,C,SFR,FMAX,FMIN,U(10)
17 1 ,EOPT(25),GR,A1,A2,A3,A4,A5,A6,A7,N1,NEL4,MW
18 H=0.D0
19 F=FMIN
20 E=0.D0
21 FD=0.D0
22 DE=0.D0
23 S=0.D0
24 DF=(FMAX-FMIN)/(N1-1)
25 DO 10 J=1,N1
26 CALL ABCD(F,J,LL,K,ZI,LI,FNF)
27 CALL YBC(AB,Y11,Y12,Y21,Y22)
28 CALL CONV(Y11,Y12,Y21,Y22,S1,S2,S3,S4)
29 S(J)=S3
30 SFF(J)=(1+CDABS(S1+S4-S3*S2)**2-CDABS(S1)**2-CDABS(S4)**2)
31 1 /((2*CDABS(S3)*CDABS(S2))
32 X1(J)=-20.*DLOG10(CDABS(S1))
33 X2(J)=20.*DLOG10(CDABS(S3))
34 X3(J)=-20.*DLOG10(CDABS(S4))
35 FR(J)=DEXP(2.30259D0*FM(MW,J)/10.D0)
36 H=H+X2(J)/N1
37 G=G+FNF(J)/N1
38 FD=FD+FR(J)/N1
39 F=F+DF
40 10 CONTINUE
41 C *****
42 X(1)=FMIN
43 DO 155 I=2,N1
44 X(I)=X(I-1)+DF

```

```

045 155 CONTINUE
046 DO 869 I=1,N1
047 T1=DIMAG(S(I))
048 T2=DREAL(S(I))
049 T(I)=ATAN2(SNGL(T1),SNGL(T2))
050 869 CONTINUE
051 CALL GDGS(X,T,N1,DELAY)
052 DO 889 I=1,N1
053 Z(I)=20.*DLOG10(CDABS(S(I)))
054 889 CONTINUE
055 CALL GDGS(X,Z,N1,SLOPE)
056 DO 979 J=1,N1
057 SLOPE(I)=(SLOPE(I))*2.*PI/1000.
058 979 CONTINUE
059 C *****
060 DO 81 J=1,N1
061 DE=DE+DELAY(J)/N1
062 81 CONTINUE
063 DTN=0.00
064 DTN=0.00
065 DO 65 J=1,N1
066 DT=(DELAY(J)-DE)
067 IF(DT.LE.0.00)GO TO 45
068 IF(DT.GT.DTN) GO TO 55
069 GO TO 65
070 55 DTN=DT
071 GO TO 65
072 45 DT=(DE-DELAY(J))
073 IF(DT.GT.DTN) GO TO 75
074 GO TO 65
075 75 DTN=DT
076 GO TO 65
077 65 CONTINUE
078 DEL=DTN+DTN
079 SFFI=SFF(I)
080 A=GR
081 DO 20 I=1,N1
082 IF(X1(I).GT.20.) X1(I)=20.
083 IF(X3(I).GT.20.) X3(I)=20.
084 IF(DEL.GT.1) DEL=0.95
085 IF(SLOPE(I).GT.0.04) SLOPE(I)=0.0095
086 E=E+A1*(X2(I)-4)**2+A2*(X1(I)-20.0)**2+A3*(X3(I)-20.0)**2
087 1 +A4*(X2(I)-W)**2+10.*DEL/(1.0-DEL)+A6*(G-FD)**2+A7*SLOPE(I)/

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```

0088      1 (0.01-SLOPE(I))
0089      IF(SFF(I).LT.SFFI) SFFI=SFF(I)
0090      20 CONTINUE
0091      RETURN
0092      END

```

FILE TIME = 0004.46

```

R FREQ= 3.75      # ELEMENTS= 9      FMIN= 3.50
MAX= 4.00# FREQS= 6      ATEN= .10
ENT #      ELEMENT TYPE      Z(I)      L(I)
1          2.0          15.000          .150
2          2.0          50.000          .150
3          2.0          15.000          .150
4          2.0          50.000          .150
5          13.0          .000          .000
6          2.0          50.000          .150
7          2.0          15.000          .150
8          2.0          50.000          .150
9          2.0          15.000          .150

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= 1
= 1
1.0000000000000000
1.0000000000000000
1.0000000000000000
1.0000000000000000
1.0000000000000000
1.0000000000000000
1.0000000000000000
= 1.0000000000000000
5.0000000000000000
70.0000000000000000
7.0000000000000000
.2500000000000000
9.999999999999999E-03
1 IS AS FOLLOWS
1. 1. 1. 0. 1. 1. 1. 1.

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5.000000000000000

5.000000000000000E-02

1 OPT Z(I) OPT L(I)

1	23.4	.661E-01
2	45.2	.893E-01
3	15.6	.134
4	53.8	.166
5	.000	.000
6	55.4	.211
7	21.1	.876E-01
8	41.6	.876E-01
9	13.9	.876E-01

0	GAIN	STBL	GRP DEL	IRETL	FNOISE	SLOPE	DRETL
Z)	(DB)	(V/M.)	(VSEC)	(DB)	(DB)	(DB/MHZ)	(DB)
0	5.113	1.305	-.459	21.000	10.113	.0012	5.430
0	5.101	1.306	-.441	27.000	10.304	-.0012	5.653
0	4.904	1.307	-.423	23.000	10.401	-.0027	5.445
0	4.573	1.309	-.398	20.000	10.724	-.0038	4.981
0	4.161	1.310	-.374	18.000	11.348	-.0044	4.444
0	3.710	1.312	-.351	17.000	11.951	-.0046	3.938

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