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**A Low-Current Amplifier for Mobile Radio
and Monolithic Microwave Integrated Circuit
Design Techniques in the UHF and L Bands**

by
Langis Roy

This thesis is submitted to the Faculty of Graduate Studies and
Research in partial fulfillment of the requirements for the degree of

Master of Electrical Engineering

Department of Electronics
Carleton University
Ottawa, Canada
20 November, 1989

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**"A Low-Current Amplifier for Mobile Radio and
Monolithic Microwave Integrated Circuit Design
Techniques in the UHF and L Bands"**

submitted by Langis Roy, in partial fulfillment of the requirements
for the degree of Master of Engineering.

Professor J.S. Wight,
Thesis Supervisor

Professor A.R. Boothroyd,
Chairman, Dept. of Electronics

November 1989

ABSTRACT

Analytical transfer functions are developed to represent all commonly used FET subcircuits found in low frequency GaAs monolithic microwave integrated circuit (MMIC) amplifier design, and a method is given to describe their noise behaviour. Using these techniques, a 0.1 to 2.1 GHz low current MMIC amplifier suitable for mobile radio is designed, fabricated and measured. A gain of 19 dB is achieved along with a power dissipation of 63 mW, which compares favourably with other reported amplifiers. A noise figure of 7.5 dB is obtained. Experimental and simulated results are found to be in good agreement.

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LIST OF SYMBOLS

C_{dg}	drain-gate capacitance of space-charge region
C_{ds}	drain-source substrate capacitance
C_{gs}	gate-source capacitance of space-charge region
C_{in}	input capacitance
e_n	FET equivalent input noise voltage
e_{ss}	equivalent noise voltage of signal source
F	noise figure
f	frequency
f_{3dB}	3-dB roll-off frequency
f_c	cutcfff frequency
f_{max}	maximum frequency of oscillation
f_p	frequency of transfer function pole
f_T	unity current-gain frequency
f_z	frequency of transfer function zero
G	gain
GBW	gain-bandwidth product
g_L	load conductance
g_m	transconductance
I_{ds}	FET drain current
I_{dss}	FET drain saturated current
K	low frequency FET common source gain
ω_p	angular frequency of pole ($2\pi f_p$)
ω_z	angular frequency of zero ($2\pi f_z$)
P_{diss}	DC power dissipation
R_d	drain resistance
R_{ds}	active channel resistance beneath the depletion region
R_f	feedback resistance ($1/g_f$)

R_g	gate metallization resistance
R_s	source resistance
R_n	equivalent FET noise resistance
R_{ss}	signal source resistance
S_{ij}	S parameters ($i,j=1,2$)
V_c	AC signal voltage across C_{gs}
V_{dd}	DC supply voltage
V_{ds}	DC voltage between drain and source
V_{eq}	equivalent input noise voltage
V_g	DC gate voltage
V_{gs}	DC voltage between gate and source
V_i	input AC signal voltage
V_o	output AC signal voltage
V_p	pinch-off voltage
W	normalized gate width of a FET
W'	gate width of a FET
X_{ss}	signal source reactance
Y_{in}	input admittance
Y_o	characteristic admittance of line
Y_{out}	output admittance
Z_{in}	input impedance (Z_{11})
Z_o	characteristic impedance of line
Z_{out}	output impedance (Z_{22})

CHAPTER 1. INTRODUCTION

1.1 Motivation

Over the past several years, Monolithic Microwave Integrated Circuit technology has been used to miniaturize microwave systems of all types. The ability to combine the passive and active circuit elements on a single GaAs semi-insulating substrate has the potential to lead to smaller, more reliable, and lower cost products in the areas of phased array radar, electronic warfare, satellite communications, gigabit data rate optical communications, instrumentation, and mobile radio, among others. All are characterized by the need for the same component or circuit to be reproduced many times, which is a major advantage provided by integrated circuit technology. The operating frequencies of these systems is from DC to 60 GHz, but a growing number of applications such as MSAT and mobile phone communications are emerging in the 0.5 to 2 GHz range, i.e. the UHF and L bands.

In the case of mobile radio (0.6 to 2.1 GHz), size reduction is needed to make possible the next generation of stand-alone pocketable telephones operating from a small battery and offering the same performance as their receiver-in-the-trunk counterparts. With a small battery and reduced dimensions comes the need for low power dissipating MMIC components. The transmitter, for example, could include MMICs for its phase-locked synthesizer, local oscillator, mixer, and amplifier which are needed for modulation, frequency upconversion and amplification of the signal being radiated. The most critical component in terms of power consumption is the transmit amplifier, which must exhibit maximum

efficiency. Similarly for the receiver, special attention must be given to the design of the high-gain receive amplifier so that it draws as little current as possible. It must be capable of producing 15 to 20 dB of gain across the band with less than 100 mW DC power consumption.

Of particular importance in this thesis is the requirement for a low current amplifier. Although mobile radio is the intended application, low power consumption is a desirable feature in any system. Such an amplifier could also find use as an IF amplifier in a higher frequency receiver front end, or as a general-purpose RF amplifier.

1.2 Objectives

The primary objective of this thesis is to design, manufacture and measure a low current MMIC amplifier covering the UHF and L bands. Since low DC power, low microwave frequency, and MMIC technology are all issues being dealt with at once, it is also the objective to first highlight the special amplifier design techniques used in low frequency MMICs and identify those that lead to low power consumption.

The proposed amplifier has been fabricated at TriQuint Semiconductor, a commercial foundry, using the recently introduced 3A process. Thus a final objective of this thesis is to verify experimentally the accuracy of the GaAs MMIC models, in particular those of the field effect transistors.

1.3 Thesis Organization

The various topics leading to the design of a low current amplifier are presented in a logical sequence throughout this thesis. In Chapter 2 a general overview of GaAs MMIC technology is given along with the specific characteristics of the TriQuint 3A Process. The principles of low frequency MMIC design are also addressed. Chapter 3 is concerned with amplifier design at UHF and L band. All of the commonly used subcircuits found in MMIC amplifiers are studied analytically and a technique for evaluating their noise performance is described. This is followed by the low-current amplifier design in Chapter 4, in which the low power considerations are treated first, followed by the design details relating to the gain, bandwidth and noise figure of the amplifier. The layout process and MMIC implementation steps are also discussed in Chapter 4. In Chapter 5 the measurement apparatus and test jig are described along with the experimental performance of the amplifier. From this a discussion of the discrepancies between predicted and measured results is given. Finally, in Chapter 6 conclusions are drawn from the results obtained and suggestions for further work are made.

CHAPTER 2. BACKGROUND

2.1 Introduction

Before being able to design a MMIC one must first become familiar with the circuit elements and design principles of this technology. These issues are treated in this chapter along with a description of the TriQuint 3A process. The simplifications and design approaches arising from low frequency operation are also discussed.

2.2 GaAs MMIC Technology

2.2.1 Overview

Due to its attractive electrical properties Gallium Arsenide is an ideal material for MMIC fabrication. Its ability to become semi-insulating and the emergence of the GaAs FET are the two factors primarily responsible for the major role played by GaAs in the development of MMICs. In 1964 Cronin et al. reported on the use of Cr doping to reproducibly grow semi-insulating GaAs crystals [1]. Shortly afterwards, Mead, in 1966 fabricated the first GaAs MESFET (MEtal Semiconductor FET) using a simpler Schottky barrier for the gate instead of a p-n junction [2]. Although microwave operation was not possible with this device, it demonstrated the feasibility of his approach. The first microwave GaAs MESFET with an $f_{\max}$ of 3 GHz was produced by Hooper et al. in 1967 [3], however its performance was still below that of Si bipolar transistors available at the time. It was not until 1970, when Dangreid et al. reported a GaAs FET with a 1 μm gate and an $f_{\max}$ of 30 GHz, that this device

was clearly established as being superior to transistors of any other type [4].

The first MMIC, constructed by Mehal et al. in 1968, did not contain a MESFET as an active device, but rather a Gunn diode operating as an oscillator at 94 GHz [5]. The first fully monolithic GaAs X-band amplifier was reported by Pengelly et al. in 1976 and consisted of a single FET with lumped matching elements, providing a gain of 4.5 dB over the 7.5 to 11.5 GHz frequency band [6]. Since then extensive efforts have led to the development of other monolithic components such as high-efficiency and high-power amplifiers through Ku-band, low-noise amplifiers, variable-gain dual-gate amplifiers, FET mixers with gain, voltage-controlled oscillators, phase shifters and couplers [7].

Compared to other forms of microwave circuitry the main advantages of GaAs MMICs are their small size, light weight, high reliability, multifunctional capability, low-cost potential, broad bandwidth capability, and reproducible performance. Among some of this technology's disadvantages are its long development cycle, lack of tuning capability, extensive CAD modeling requirement, expensive mask set, and relatively low Q [8].

2.2.2 Electrical Properties of GaAs

The physical and electrical properties of GaAs make it an excellent material for high frequency device applications. In GaAs the conduction electrons have a 6 times larger mobility than that found in Si while the peak drift velocity is twice that of Si [9]. The

electron drift velocity as a function of electric field for GaAs and Si is shown in Figure 2.1.

Figure 2.1. Equilibrium electron drift velocity in Si and GaAs [9].

One sees that the drift velocity of GaAs reaches a peak value of 2×10^7 cm/s at 3 kV/cm, then decreases and levels off to a saturated velocity that approaches the limiting velocity in Si. Since electron velocity in n-type material is directly related to current density, this higher velocity leads to devices having lower parasitic resistances, larger transconductances, and shorter electron transit times than for Si-based devices [9].

The resistivity of intrinsic GaAs is inherently very high (greater than 10^7 Ω cm compared to 30 Ω cm for Si) making it semi-insulating (SI) and hence an attractive substrate for applications in which low parasitic capacitances are desirable. Furthermore, its SI properties allow active and passive elements to be incorporated on the same substrate without the need for isolation implants between them, as is the case for Si. Since the relative dielectric constant of GaAs is 12.9, this makes it ideal for inter-digitated capacitors and

transmission lines (coplanar or microstrip) in the 30 to 100 Ω characteristic impedance range [8].

Due to the large fundamental bandgap of GaAs (1.4 eV compared to 1.0 eV for Si), devices made of this material are able to function up to higher temperatures and hence to higher power levels. Also, its large resistance to ionizing radiation allows GaAs devices to operate in harsher radiation environments [8].

2.2.3 The Schottky Barrier MESFET

The MESFET (metal semiconductor field-effect transistor) is by far the most widely used device in both digital and microwave ICs [10]. The basic MESFET structure, illustrated schematically in Figure 2.2, consists of a semi-insulating GaAs substrate into which an n-doped active channel is implanted. Two ohmic contacts to the active layer are placed on either side of the semiconductor, forming the source and drain terminals of the device. A narrow metal layer, the gate contact, is deposited at the centre and forms a Schottky barrier with an underlying depletion region that changes the thickness of the conductive channel depending on the applied gate voltage.

The FET can be fabricated either as an enhancement-mode device (E-FET), in which case the channel is fully depleted at zero gate bias so that it must be forward biased in order to conduct, or as a depletion-mode device (D-FET) which conducts current at zero bias and must be reverse biased to cut off current flow. E-FETs are also called "normally-off" devices and offer lower power dissipation than

Figure 2.2. Structure of an n-type MESFET [10].

(a)

(b)

Figure 2.3. (a) Three-dimensional FET schematic, (b) FET equivalent circuit [8].

"normally-on" D-FETs, but at the expense of reduced speed and lower noise margins [10]. They are used primarily for LSI-VLSI digital ICs since power dissipation is a major design consideration in these applications. D-FETs are mostly used for MMICs where speed and power handling capability are the primary concerns.

Figure 2.3 depicts a MESFET cross section showing the position and source of the various circuit elements in the equivalent model for this device. The total gate to channel capacitance due to the space charge region is $C_{gd} + C_{gs}$, while the channel resistance is represented by R_i in the gate to source region, and R_{ds} beneath the depletion region. The voltage between the gate and source, V_G , controls the drain to source current given by $i_d = V_a g_m \exp(-j\omega t_0)$, where g_m is the transconductance and t_0 is the time delay associated with the carrier transit time. Parasitic resistances R_d and R_s are a result of the ohmic drain and source contacts, whereas R_g is the gate metallization resistance. C_{ds} is the drain to source substrate capacitance [10].

The small signal lumped model adequately describes the FET behaviour up to about 20 GHz before transmission line elements would have to be added. Generally the equivalent circuit element values of the device are determined through discrete frequency S-parameter measurements in the common source configuration. It is desirable to use the equivalent circuit representation instead of S parameters for greater design flexibility when analyzing linear circuitry since the FETs may not always be in the common source configuration and the frequency may be outside the range covered by the S parameters.

The FET's drain current as a function of drain and gate voltage is

shown in Figure 2.4. The three regions of operation are seen to be the linear, saturation and breakdown regions.

Figure 2.4. Drain current characteristics of a FET.

FETs operating as linear devices function in the saturated region (not in the linear region as the name would indicate). In this region the drain current I_{DS} can be between 0 and I_{DSS} , corresponding to gate voltages between V_P and 0 V, where $I_{DS} = I_{DSS}$ at $V_{GS} = 0\text{ V}$.

Two fundamental figures of merit are used to compare the microwave performance of FETs. These are the current gain cutoff frequency f_T and the maximum frequency of oscillation, f_{max} [8]. The current gain cutoff frequency is defined by

$$f_T = g_m / 2\pi C_{gs}$$

and is the frequency at which the output current is equal to the input

current. The maximum frequency of oscillation is given by

$$f_{\max} = f_T / 2\sqrt{R_{\text{out}}/R_{\text{in}}}$$

and is the frequency at which the input power equals the output power.

2.2.4 Passive MMIC Elements

Passive circuit elements include transmission lines, capacitors, inductors, and resistors, and can be realized in a variety of ways. Microstrip is normally chosen for transmission lines although coplanar geometries are sometimes used. Capacitors may be of either the metal-insulator-metal (MIM) overlay or interdigitated types, inductors are either high-impedance transmission line sections or spiral geometries, while resistors consist of an ion-implanted layer or thin-film metal. The approximate range of values achievable for each element are given in Table 2.1.

Table 2.1 Approximate Range of Values for Passive MMIC Elements.

Element	Value
Resistor	0 - 100 k Ω
Capacitor	0 - 25 pF
Inductor	0 - 5 nH
Transmission line	30 - 110 Ω (Z_0)

As was the case for active devices, accurate modeling of passive elements is also required. Equivalent circuit representations exist that characterize the various microwave parasitics associated with each element. The key to achieving a successful first time design resides in the quality of these equivalent models. For example, a small MIM capacitor might be adequately modeled using only a lumped-element capacitor with appropriate resistance to account for losses, whereas a larger one would require a lossy transmission line representation with additional inductances and capacitances. A more complete treatment of the modeling of MMIC passive elements is given by [8,11].

Figure 2.5 illustrates a three dimensional section of a GaAs MMIC showing the integration of passive and active components on the semi-insulating substrate. Apart from the elements already described, the figure shows other structures that can be present in a typical monolithic circuit, such as airbridge crossovers and through-substrate via holes for grounding.

Figure 2.5. Three-dimensional MMIC schematic [8].

2.2.5 Design Principles

Due to the very nature of MMICs, tweaking of a completed circuit cannot be done and therefore both active and passive components must be modeled very accurately along with any stray parasitics and coupling. Thus the design of GaAs MMICs requires extensive use of computer aided design techniques. A strong emphasis is placed on minimizing the chip size as this is necessary to realize the advantages of high yield, low cost and multifunctional capability that are inherent in MMIC technology. In MMIC design, "FETs are free" since ten or a hundred FETs cost the same as one FET (excluding power considerations) [12]. Hence FETs are used wherever possible, even to replace passive components such as resistors and inductors. Also FET-based structures for impedance matching, active loads and biasing are the preferred design approaches since FETs also use GaAs area very efficiently.

2.3 TriQuint 3A Process

TriQuint Semiconductor is a commercial foundry which fabricates tailor-made MMICs according to a customer's specifications provided in the form of a circuit layout. The layout follows a set of design rules established by the foundry for specifying circuit elements in a given fabrication process.

The Gallium Arsenide 3A process available from TriQuint is based on a $0.5\text{ }\mu\text{m}$ gate length depletion-mode MESFET device with a typical f_T of 26 GHz. In addition to D-FETs the process can fabricate diodes,

implanted and thin-film resistors, MIM capacitors and airbridge inductors. Interconnections are achieved through two levels of metallization, first level and second level, the latter being airbridge metal.

TriQuint FETs consist of interdigitated gate, source, and drain fingers as shown in Figure 2.6. The total gate width W' is the product of the gate finger width (W) and the number of gate fingers (N). The standard 300 μm FET for which equivalent circuits have been developed has $N = 6$ fingers each of width $W = 50 \mu\text{m}$.

Figure 2.6. Interdigitated 300 μm FET layout [12].

It is recommended by the foundry that W be limited to 20 to 60 μm and that N be limited to 1 to 6. The small signal equivalent circuit values for this device are given in Figure 2.7 below.

Equivalent Circuit

Equivalent Circuit Element Values

(0.5 μm x 300 μm FET, $I_{\text{dss}} = 77 \text{ mA}$, $T_a = 25 \text{ deg. C}$)

Element (units)	Vds=2.5Volts			Vds=3.0 Volts			Vds=4.0Volts		
	Idss	Idss/2	Idss/5	Idss	Idss/2	Idss/5	Idss	Idss/2	Idss/5
gm1 (mS)	65.93	56.34	43.50	64.52	55.86	42.71	62.00	52.97	41.18
Cgs (fF)	472.83	367.73	297.50	497.36	383.27	307.51	535.15	411.20	322.59
Cgd (fF)	56.02	64.43	71.02	47.59	57.81	65.93	38.88	49.31	59.49
Cds (fF)	93.19	92.37	89.40	90.60	90.89	88.81	87.68	86.63	87.35
Rds (ohms)	200.49	196.92	223.51	247.79	225.91	242.80	322.43	275.66	270.40
Rin (ohms)	1.8	1.98	2.20	1.98	2.18	2.42	2.19	2.56	2.87
Rs (ohms)	1.96	2.43	2.79	1.89	2.41	2.80	1.86	2.40	2.76
Rgs (ohms)	100K	100K	100K	100K	100K	100K	100K	100K	100K
Rg (ohms)	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
Rd (ohms)	2.54	3.24	3.19	2.43	3.15	3.13	2.06	2.88	2.88
Lg (pH)	38.50	38.50	38.44	38.16	37.97	37.97	37.72	37.48	37.66
Ls (pH)	2.93	1.34	0.63	2.93	1.18	0.55	2.73	0.99	2.63
Ld (pH)	24.32	24.10	24.67	19.94	21.71	22.98	13.28	16.87	20.66
Tt (pS)	2.16	1.86	1.84	2.57	2.16	2.09	3.17	2.67	2.47

Figure 2.7. Small signal equivalent circuit and element values for a Triquint 300 μm FET [12].

The scaling rule for obtaining the circuit element values for any other size of FET in the allowed range is described in Table 2.2. Apart from small fringing capacitances all capacitor values are proportional to W' , as are g_m and I_{dss} . All resistor values except R_g and R_{gs} are inversely proportional to W' . The effects of the fringing

capacitances become important at very small values of W' but can generally be ignored when $W' > 100 \mu\text{m}$. Since the scaling is always referenced to the standard $300 \mu\text{m}$ width and the parameter W , the width of each finger, is almost never mentioned, the remainder of this text will employ W as a newly defined parameter called the normalized gate width, where now $W = W'/300 \mu\text{m}$. Thus W is a dimensionless quantity and simply indicates the factor by which the standard width has been multiplied.

Table 2.2. Determination of the FET equivalent circuit values for arbitrary FET widths [12].

Element	Equation
$gmrf$ (mS)	$= gmrf (W'/300)$
Cgs' (fF)	$= Cgs (W'/300) + (Cgsf \cdot N)$
Cgd' (fF)	$= Cgd (W'/300) + (Cgdg \cdot N)$
Cds' (fF)	$= Cds (W'/300) + (Cdsf \cdot N)$
Rds' (ohms)	$= Rds (300/W')$
Rin' (ohms)	$= Rin (300/W')$
Rs' (ohms)	$= Rs (300/W')$
Rgs' (ohms)	$= \text{fixed constant, } 100 \text{ Kohms}$
Rg' (ohms)	$= Rg (W/50)(6/N)$
Rd' (ohms)	$= Rd (300/W')$
Lg' (pH)	$= Lg (W/50)(6/N)$
Ls' (pH)	$= Ls (W/50)(6/N)$
Ld' (pH)	$= Ld (W/50)(6/N)$
Tt (ps)	$= \text{constant, dependant on gate length}$
Where:	
$gmrf$, etc	$= \text{scaled model value}$
$gmrf$, etc	$= 300 \mu\text{m FET model value from the tables}$
W'	$= \text{total width of the scaled device, } NxW$
N	$= \text{Number of fingers, } 1 \text{ to } 6$
W	$= \text{width of each finger, } 5 \text{ to } 60 \mu\text{m}$
$Cgsf$	$= \text{fringing } Cgs \text{ per gate finger, } 1.0 \text{ fF}$
$Cgdg$	$= \text{fringing } Cgd \text{ per gate finger, } 1.0 \text{ fF}$
$Cdsf$	$= \text{fringing } Cds \text{ per gate finger, } 0.3 \text{ fF}$

2.4 Low Frequency Design Principles

The complete equivalent model in Figure 2.7 with 14 parameters is accurate up to above 20 GHz. However, the scope of the work undertaken in this thesis is limited to frequencies below a few gigahertz, where many of the equivalent circuit elements, such as L_g , L_s , etc., have a negligible effect. This study has found that a simpler model requiring only the 5 parameters shown in Figure 2.8 adequately represents the FET small signal behaviour at frequencies below 4 GHz. This is demonstrated in Figure 2.9, in which the S parameters generated by the complete and simplified models are compared.

Figure 2.8. Simplified FET equivalent circuit.

The considerable simplification afforded by the low frequency approximation enables the designer to obtain manageable analytical expressions describing FET circuits, as will be seen in later sections.

For further reductions in frequency the remaining capacitors in Figure 2.8 start to behave as open circuits. Thus, below approximately 1 GHz, the FET equivalent circuit would only require

Figure 2.9. S parameters for the complete and simplified FET models.

the transconductance and output resistance R_{ds} to model the device performance, as shown in Figure 2.10. This illustrates the fact that at very low frequencies the FET only samples the input voltage (i.e. no power is transferred to it) and then produces an amplified version of V_i at the output, with a voltage gain of $g_m R_{ds}$ in the unloaded case.

Maximum power gain is achieved when the input voltage to the FET is maximized. Since the FET's input can only be matched to a $50\ \Omega$ source by using a shunt resistor at its gate (thereby creating a loss), any input matching will reduce the overall gain. Therefore, in low frequency amplifier design, input matching is not necessary to achieve maximum gain.

Figure 2.10. Low frequency FET equivalent circuit and gain.

3. MMIC AMPLIFIER DESIGN TECHNIQUES AT UHF AND L BAND

3.0 Introduction

At frequencies above 4 GHz, solid-state microwave amplifiers generally consist of FETs with input, output and interstage matching to achieve good gain. These matching blocks may take the form of distributed transmission lines or lumped elements, the latter being preferred in MMIC technology. At frequencies below approximately 3 GHz, the reactances associated with the FET's parasitic elements are small enough that the FETs may be considered as being essentially transconductance devices with known drain conductances, as described in Chapter 2. FETs can therefore be directly cascaded without matching components to produce amplifiers. This is the technique most often reported in the literature, although interstage inductance is occasionally added to improve bandwidth [13,14,15].

Amplifiers designed this way provide excellent gain but also exhibit high input and output reflection coefficients when left unmatched. Lossless passive matching cannot be used since the distributed-element lengths or lumped-element values required at these frequencies are unrealistically large for MMICs. As will be seen, FET-based active matching techniques exist to overcome this problem.

With the exception of Hornbuckle [16], most authors reporting on UHF and L band amplifiers describe their work with little analytical detail [15,17,18], thus making reproduction of their results difficult when FETs with different characteristics are employed. Estreich

gave good analytical expressions for low frequency gain and input resistance of several FET configurations, but ignored bandwidth considerations [19]. In many cases [20,21], the desired frequency response is arrived at through successive simulations with different FET sizes or circuit component values, an approach that offers only limited insight into the effect of each parameter. As a result, it is appropriate to review the principal building blocks used in low frequency MMIC design and provide theoretical expressions describing their gain, bandwidth and input or output impedances. This will allow a judicious choice of configurations to be made later on for the low power amplifier design.

Both Hornbuckle and Estreich use the concept of "FET equivalent input noise voltage" to predict the noise figure of a multi-FET amplifier. This approach is well suited to low frequency circuits and will also be described below.

3.1 Design Philosophy

As mentioned previously, a direct-cascade approach is suitable for low frequency MMIC design with active input and output matching. If one considers for example the input matching of a 300 μm FET to 50 Ohms at 1 GHz, one would find that the distributed line lengths required for a single stub match are on the order of 6 or 7 cm, which is excessively large for MMICs, or that a match simply cannot be achieved with lossless passive lumped elements. Active input matching however would require only a single FET connected in the common gate configuration to produce the desired result.

In order to keep GaAs area usage to a minimum, active loads are

also used in place of passive elements such as inductors and resistors. An active load consists of a FET with its gate and source connected together so as to produce a two-terminal element which acts as an area-efficient large resistor. Thus the philosophy employed here is an "all-active" one whereby amplifiers make use primarily of FETs with associated capacitors for DC isolation or RF grounding, and occasionally resistors for DC biasing. Since FETs are completely described by their gate width, W , and a set of standard-width values representing the equivalent circuit resistors, capacitors and transconductance (g_m), the designer is left with R , C , W and g_m as parameters in terms of which transfer functions of single- or multi-FET structures may be developed. In these "modular transfer functions", W is a true variable whereas R , C and g_m are effectively constants which change only for different FET bias points, as was seen in Table 2.1.

The modular transfer function method can be extended to cascades of two or more stages by adding the input impedance of the second stage, which is normally represented by an equivalent combination of resistor and capacitor, as a load onto the first stage. Thus it is necessary to also calculate input and output impedances along with the transfer functions, as is done in the next section.

3.2 Building Blocks Used in MMIC Amplifiers

This section provides V_o/V_i transfer functions and input or output impedances for various structures which can be combined to make amplifiers. The structures range from a single FET configured as an

active load, to multi-FET blocks performing the functions of gain, matching and feedback which are required in an amplifier.

3.2.1 Gate-to-Source Connected FET

Shown in Figure 3.1(a), this multi-purpose structure is referred to as a current source, active load or high-impedance FET, depending on its application.

From a DC current source point of view, the FET operates on the $V_{GS} = 0$ V curve of its I-V characteristics shown in Figure 3.1(b) and provides a nearly constant current equal to I_{DSS} as long as V_{DS} is sufficiently high to be in the saturated region ($V_{DS} > 1.5$ V). The current I_{DSS} can be set to any desired value by appropriate scaling of the gate width, and is only limited by the maximum allowable W . For example, a 150 μm FET has $I_{DSS} = 0.233 \cdot 150 = 35$ mA.

The small signal equivalent circuit of the current source FET is found by taking the the low-frequency FET model of Chapter 2 and connecting the gate to the source. This results in C_{gs} being shorted out, which causes the ac current source to disappear since its value is given by $g_m \cdot V_C$ and $V_C = 0$. All that remains therefore is the parallel combination of a large resistor (R_{DS}) and capacitor ($C_{DS} + C_{GD}$) as shown in Figure 3.1(c). The two-terminal device behaves essentially as a resistor at frequencies well below the transition frequency f_C at which the reactance of the capacitors becomes equal to R_{DS} . For a 300 μm FET ($W = 1$) in the TriQuint 3A process with $R_{DS} = 200$ Ohms, $C_{GD} = 56$ fF and $C_{DS} = 93$ fF, the

(a)

(b)

(c)

Figure 3.1. (a) Gate-to-source connected FET, (b) I-V characteristics, (c) Equivalent circuit.

transition frequency is

$$f_c = 1/[2\pi R_{ds}(C_{ds}+C_{gd})] = 5.3 \text{ GHz}$$

Thus at UHF or L band, an AC signal effectively sees a resistance R_{ds} , whose value may be varied by changing the gate width.

The circuit of Figure 3.2 illustrates the three main functions of the G-S connected FET. The common source FET1 of width W_1 has an active load FET2 of width $W_2 = W_1/5$. Since the saturation drain current is proportional to gate width, then FET2, acting as a current source, fixes the current through both devices at $I_{dss2} = I_{dss1}/5$, which is suitable for low noise operation of FET1. This requires a negative bias voltage V_{gs1} at the gate of FET1. If for example $W_1 = 1$ (300 μm), the value of resistance for the active load is, by scaling, $R_{ds2} = 5 \cdot 200 = 1\text{k}\Omega$. The common-source FET exhibits maximum voltage gain when it has as its load an infinitely large impedance; here the active load resistance is several times that of FET1's R_{ds} and thus high gain is assured using FET2 in this configuration. Its high impedance also provides RF isolation from any non-zero voltage supply impedance and is an example of the RF blocking function of this structure.

Figure 3.2. Application of the gate-to-source connected FET.

Since FETs are essentially free and occupy a small amount of area on a wafer, they provide an efficient means for replacing inductors when a large RF impedance is required.

3.2.2 Gain Stages

Two types of gain stages will be discussed, the common source and cascode configurations. Both employ active loads although resistors may be used instead without affecting the general conclusions.

The most frequently encountered configuration is the common-source amplifier, CS, shown in Figure 3.3(a). To appreciate its inherent behaviour, the circuit is assumed to have no loading on the output other than its active load.

For both FETs, V_{DS} must be kept at a value for which the equivalent circuit parameters are known. In the TriQuint case this is $V_{DS} = 2.5$ V, so that V_{DD} in Figure 3.3 is equal to 5 V. The widths of FET1 and FET2, designated as W_1 and W_2 on the circuit diagram, are related by the multiplying factor n ($0 < n < 1$). FETs with different gate widths also have different I_{DSS} values; thus to keep the currents through both FETs equal when $W_1 \neq W_2$, it is necessary to bias FET1 at less than I_{DSS1} by means of an appropriate negative gate voltage. The choice is again limited by the number of bias conditions given by the foundry for the equivalent circuit. Table 3.1 summarizes the different possibilities for the CS amplifier.

(a)

(b)

Figure 3.3. (a) Common source amplifier, (b) equivalent circuit.

Table 3.1 Bias Conditions for the CS Amplifier with Different FET Widths.

n	FET1 % I_{DSS1} operation	FET2 % I_{DSS2} operation	V_{GS1} (V)
1	100	100	0
0.5	50	100	-1.0
0.2	20	100	-1.5

For the voltage transfer function calculations, the CS amplifier stage can be represented by the equivalent circuit shown in Figure 3.3(b). Straightforward circuit analysis gives

$$V_o/V_i = (SC_{gd1} - g_{m1})/[S(C_{gd1} + C_{gd2} + C_{ds1} + C_{ds2}) + g_{ds1} + g_{ds2}]$$

where S is the complex frequency variable and all other terms are shown in Figure 3.3 ($g_{ds} = 1/R_{ds}$). Supposing that the standard-width values are represented by C_{gd}' , g_{m}' , etc.; then $C_{gd1} = WC_{gd}'$, $C_{gd2} = W_2C_{gd}' = nWC_{gd}'$, etc., and the above transfer function can be rewritten as

$$V_o/V_i = (SWC_{gd1}' - Wg_{m1}')/[S(WC_{gd1}' + nWC_{gd2}' + WC_{ds1}' + nWC_{ds2}') + Wg_{ds1}' + nWg_{ds2}']$$

Three important results are immediately seen from these two expressions. Both the numerator and denominator scale with FET gate width and hence the overall transfer function is independent of the actual value of W , once the ratio n between W_1 and W_2 is chosen. At low frequencies the voltage gain is

$$V_o/V_i|_{S=0} = g_{m1}/(g_{ds1} + g_{ds2})$$

and the pole and zero are located at

$$\omega_p = (g_{ds1} + g_{ds2})/(C_{gd1} + C_{gd2} + C_{ds1} + C_{ds2})$$

$$\omega_z = g_{m1}/C_{gd1}$$

For the various bias conditions given in Table 3.1 the three expressions above can be evaluated with the Triquint 3A process values to produce the results shown in Table 3.2.

Table 3.2 Gain and Pole-Zero Locations for the Common-Source Stage.

n	G	$f_p = \omega_p/2\pi$	$f_z = \omega_z/2\pi$
1	6.5 V/V	5.3 GHz	187 GHz
0.5	7.5	5.1	138
0.2	7.9	5.0	97.5

Given that f_z is much greater than f_p (it is outside the range of validity for the simplified equivalent circuit), the bandwidth of the common source stage is to a good approximation equal to f_p . Thus the CS stage provides a voltage gain of between 6.5 and 7.9 and a bandwidth of approximately 5 GHz, depending on the relative FET widths.

The second gain stage to be considered is the cascode amplifier shown in Fig. 3.4(a) along with its small signal equivalent circuit in Fig. 3.4(b). It consists of a common source FET1 feeding into a common gate FET2 with FET3 as an active load.

Figure 3.4. (a) Cascode amplifier, (b) equivalent circuit, (c) separation of C_{gd1} into C_a and C_b .

To keep V_{DS} of each FET at 2.5 V, V_{DD} must be set at 7.5 V. The allowed DC modes of operation for the cascode are as listed in Table 3.3.

Table 3.3 Bias Conditions and Performance of the Cascode Stage

n	m	% I_{DSS1}	% I_{DSS2}	% I_{DSS3}	K	V_O/V_i	f_{3dB}
1	1	100	100	100	1.6	11.4	3.3 GHz
0.5	0.5	50	100	100	2.5	17.2	3.3
0.2	0.2	20	100	100	3.8	26.5	3.2
1	0.5	50	50	100	2.2	17.8	2.2
1	0.2	20	20	100	3.3	28.7	1.5
0.4	0.2	20	50	100	3.5	28.5	2.5
2.5	0.5	50	20	100	2.1	17.9	1.4
2	1	100	50	100	1.4	11.6	2.4
5	1	100	20	100	1.3	11.6	1.3

To facilitate the analysis Miller's Theorem is used to split the series capacitor C_{gd1} into two shunt capacitors as shown in Figure 3.4(c). The values of C_a and C_b are

$$C_a = (1-K)C_{gd1}$$

$$C_b = (1-1/K)C_{gd1}$$

where K is the low frequency gain of FET1. Since this common source FET is connected to FET2, whose common gate input impedance is g_{in} , the gain of FET1 is

$$K = -g_{m1}/(g_{ds1} + g_{in}) \quad (3.1)$$

with the input conductance given by (Sec. 3.2.3)

$$g_{in} = (g_{m2} + g_{ds2})g_{ds3}/(g_{ds2} + g_{ds3})$$

As before K depends only on the relative gate widths of the three FETs and not on the actual value of W used in the circuit. For each allowed combination of n and m , K is evaluated in Table 3.3 using equation 3.1 and the TriQuint 3A values.

The transfer function in terms of K and the other circuit components is now found to be

$$V_o/V_i = -g_{m1}(g_{m2} + g_{ds2})/(AS^2 + BS + C)$$

where

$$A = C_o(C_L + C_{ds2}) + C_{ds2}C_L$$

$$B = C_L(g_{ds3} + g_{ds2}) + C_{ds2}(g_{ds3} + g_{ds1}) + C_o(g_{ds1} + g_{ds2} + g_{m2})$$

$$C = g_{ds3}(g_{ds1} + g_{ds2} + g_{m2}) + g_{ds2}g_{ds1}$$

with

$$C_o = C_{dg2} + C_{dg3} + C_{ds3}$$

$$C_L = C_{ds1} + (1 - 1/K)C_{dg1} + C_{gs2}$$

Thus the low frequency gain is

$$V_o/V_i|_{S=0} = -g_{m1}(g_{m2} + g_{ds2})/C$$

and the poles are located at

$$f_{p1,2} = [-B \pm \sqrt{B^2 - 4AC}]/2A/2\pi$$

It can be verified that f_{p2} is much greater than f_{p1} so that the 3 dB bandwidth is essentially equal to f_{p1} . Substituting in the numerical values yields the cascode's gain and bandwidth performance shown in the last two columns of Table 3.3. These results indicate that the cascode exhibits a much wider range of gains and bandwidths than does the common source amplifier. The combination providing the largest gain-bandwidth product (GBW) is that represented by $n=m=0.2$, whereas the worst gain and bandwidth are obtained with $n=5$, $m=1$. On the other hand the input capacitance given by

$$C_{in} = C_{gs1} + C_a = C_{gs1} + (1-K)C_{gd1}$$

is minimized for $n=5$, $m=1$ ($K=-1.3$) and maximized for $n=m=0.2$ ($K=-3.8$). The fact that C_{in} varies in an opposite way to GBW must therefore be taken into account in multi-stage amplifiers, where C_{in} is desired to be as small as possible to achieve the broadest bandwidth. It should be noted that the input capacitance of the common source amplifier is described by the same equation with K replaced by V_O/V_i .

Based on the above it is now possible to compare the merits of the two amplifying structures by way of their maximum gain-bandwidth products. For the common source configuration $GBW_{CS} = 7.9 \cdot 5.0 = 39.5$ GHz and for the cascode $GBW_{casc} = 26.5 \cdot 3.2 = 84.8$ GHz, which suggests that the cascode is a more efficient gain block. At this point power dissipation does not enter the picture as both transfer functions are independent of W and hence independent of current.

3.2.3 Input Matching

The amplifying stages discussed above have high input and output impedances and hence normally require some form of matching for use in a 50 ohm environment. Active matching can be achieved using a FET in the common gate configuration while passive matching can consist of a simple resistor either shunted to ground or inserted in a feedback loop.

Figure 3.5(a) illustrates a common gate FET and its associated load conductance g_l , which may represent a simple resistor or an active load. In practice this circuit requires DC current flow and therefore demands that the source of the FET be connected to a DC supply through, for example, a high-impedance current source FET. For simplicity the source is left open and the equivalent circuit of Figure 3.5(b) is obtained, where all capacitors are omitted so as to represent the low frequency case.

Analyzing this configuration in the same manner as before leads to the voltage gain

$$V_o/V_i = (g_m + g_{ds})/(g_l + g_{ds})$$

and the input conductance

$$g_{in} = g_l(V_o/V_i) = g_l(g_m + g_{ds})/(g_l + g_{ds})$$

(a)

(b)

(c)

Figure 3.5. (a) Common gate FET, (b) low frequency equivalent circuit, (c) equivalent circuit for bandwidth calculations.

Substituting into the above $g_m = W \cdot g_m'$ and $g_d = W \cdot g_{ds}'$ (primed quantities indicate the standard 300 μm values) leads to

$$g_{in} = g_l(Wg_m' + Wg_{ds}')/(g_l + Wg_{ds}')$$

which, for a match to the system impedance, is equated to Y_0 . After some rearrangement the following equation is obtained

$$Y_0(1/W + g_{ds}'/g_l) = g_m' + g_{ds}' \quad (3.2)$$

If for example the FET is biased at 100% I_{DSS} (such that $g_m' = 65 \text{ mS}$ and $g_{ds}' = 5.0 \text{ mS}$) and Y_0 is taken to be $1/50 \text{ Ohms} = 20 \text{ mS}$, then eqn (3.2) reduces to

$$70 = 20/W + 100/g_l \quad (3.3)$$

which shows how g_l and W are related to provide a perfect match. Eqn (3.3) also shows that the equality will not hold for $W < 20/70$ and hence places a lower limit on the size of FET used to match to 50 Ohms. Table 3.4 lists various combinations of $R_l (= 1/g_l)$, W and associated gain which give $g_{in} = 20 \text{ mS}$.

With further analysis it can be shown that the gain and the match of the common gate configuration are very broadband. To do so the capacitors previously removed must now be reinserted into the equivalent circuit along with a load capacitance C_l in parallel with g_l , as shown in Figure 3.5(c). The capacitor C_l is to account for the possible input capacitance of a following stage or an active load.

Table 3.4. Relationship between load resistance, gate width and gain for a common gate FET with 50 Ohms input resistance.

R_L	W	V_o/V_i
500 Ohm	1	10
300	0.5	6
200	0.4	4

The resulting expressions for gain and input admittance as functions of frequency are:

$$V_o/V_i = (g_{ds} + g_m + S C_{ds}) / (g_{ds} + g_l + S(C_l + C_{ds})) \quad (3.4)$$

$$Y_{in} = (g_{ds} + g_m + S C_{ds})(S C_l + g_l) / (g_d + g_l + S(C_l + C_{ds})) \quad (3.5)$$

For the condition given in the last entry of Table 3.4, where $g_l = 1/200 \Omega$ and $W = 0.4$, and taking C_l to be the input capacitance C_{gs} of a following stage (again with $W = 0.4$ so that $C_l = W \cdot C_{gs}' = 0.4 \cdot 0.473 = 0.19 \text{ pF}$), one obtains the gain bandwidth as

$$\begin{aligned} f_p &= [(0.4 \cdot g_{d'} + g_l) / (C_l + 0.4 \cdot C_{ds}')] / 2\pi \\ &= [(2+5) \cdot 10^{-3} / (190 + 37) \cdot 10^{-15}] / 2\pi \\ &= 4.9 \text{ GHz} \end{aligned}$$

since the zero at $f_z = [(g_d + g_m) / C_{ds}] / 2\pi = 119 \text{ GHz}$ can be ignored. Thus the bandwidth typically extends well beyond the frequencies of interest in this work, a result which holds true for load

capacitances up to 5 or 6 times the value of C_{ds} (by eqn 3.4).

In the case of the input admittance, substituting in the appropriate values produces an expression containing the same zero at 119 GHz and pole at 4.9 GHz as above, with an additional zero at $f_z = (g_l/C_l)/2\pi = 4.2$ GHz which effectively cancels out the pole. Y_{in} is therefore almost independent of frequency in this example, and a very broadband match is obtained since Y_{in} remains close to the low frequency g_{in} value. In general the bandwidth of the input match is the frequency at which some maximum allowable return loss is obtained, and has no precise definition as is the case for the 3 dB gain bandwidth; thus the broadness of the match depends on the extent to which eqn (3.5) is independent of frequency, a condition that is increasingly satisfied as g_{ds} and C_{ds} become small compared to g_l and C_l , respectively.

Passive matching in its simplest form consists of shunting a resistor with the input of an amplifying stage as shown in Figure 3.6. The overall input impedance will then be $R//C_{in}$ which is approximately equal to R when the input FET is chosen small enough. The actual size depends on the frequency range over which a match is desired. For example, a 60 μm input FET ($W=0.2$) biased at 20% I_{dss} (so that $C_{gd}' = 0.07$ pF and $C_{gs}' = 0.3$ pF) has

$$C_{in} = W[C_{gs}' + (1+K) \cdot C_{gd}'] = 0.2[0.3 + (1+7.9) \cdot 0.07] = 0.18 \text{ pF}$$

where K is taken to be 7.9 from Table 3.2. Choosing $R=50$ Ohms for a match to this value, an input impedance of

$$Z_{in} = R \parallel (1/j\omega C_{in}) = 49.4 - j5.58 \text{ Ohms}$$

is obtained at 2 GHz, corresponding to a -25 dB return loss, whereas

an input FET twice the size, with $C_{in} = 0.36$ pF and $Z_{in} = 47.5 - j10.8$ Ohms, would give a return loss of -19 dB at the same frequency. This technique only offers simplicity as an advantage. It has the obvious disadvantages of wasting RF power and increasing the noise figure.

Figure 3.6. Passive input matching using a shunt resistor.

Another alternative is to employ the resistor in a feedback loop around a common source FET as shown in Fig. 3.7(a). Analysis of this configuration using the model in Fig. 3.7(b) leads to the following expressions:

$$V_o/V_i = [S C_{gd1} + g_f - g_{m1}] / [S(C_{gd1} + C_{gd2} + C_{ds1} + C_{ds2}) + g_f + g_{ds1} + g_{ds2}]$$

$$\omega_p = [g_f + g_{ds1} + g_{ds2}] / [C_{gd1} + C_{gd2} + C_{ds1} + C_{ds2}]$$

$$Y_{in} = g_f + [g_f(g_{m1} - g_f) / (g_f + g_{ds1} + g_{ds2})] \quad (3.6)$$

where Y_{in} contains no capacitors, a low frequency approximation shown by Ulrich to be valid up to about 4 GHz [22].

Figure 3.7. (a) Passive matching with a feedback resistor, (b) equivalent circuit.

The condition for a perfect match obtained by setting equation 3.6 to Y_o is

$$g_f = (Y_o \cdot g_d) / (g_d + g_{m1} - Y_o)$$

where $g_d = g_{ds1} + g_{ds2}$. Inserting this back into the V_o/V_i gain expression reduces it to a simple form:

$$V_o/V_i \text{ (matched)} = -[g_{m1}/g_d] \cdot [1 - Y_o/(g_d + g_{m1})] \text{ to } Y_o$$

As an example using 300 μm FETs with $g_m = 66 \text{ mS}$ and $g_{ds} = 5 \text{ mS}$, the value of feedback resistance required is 280 Ohms for $1/Y_o = Z_o = 50 \Omega$, while the associated gain is 4.9.

Further analysis would show that Y_{out} is almost equal to Y_{in} . Thus with a high enough value of g_m this configuration can be used as a one-stage amplifier with input and output matched simultaneously [22,23].

3.2.4 Output Matching

Many of the techniques used for input matching are directly applicable to matching on the output. The simplest method uses a resistor in parallel with a common source output FET as shown in Figure 3.8. To provide DC current flow the drain could be connected to the voltage supply through a high impedance current source FET, however it is left open here for simplicity.

Figure 3.8. Output matching using a shunt resistor.

Without drawing the equivalent circuit it is possible to write the output impedance as

$$Z_{out} = R_{ds} || C_{ds} || R$$

which approximates to

$$Z_{out} = R_{ds} || R$$

at sufficiently low frequencies or values of gate width. Once the size of the FET and hence R_{ds} is determined (depending on how broad a match is desired), R must be chosen so that Z_{out} equals Z_0 , the characteristic impedance. The gain of this stage, which feeds into a load impedance of Z_0 , is

$$V_o/V_i = -g_m Z_0 / 2$$

and its input capacitance can be calculated using the same equation as for the common source amplifier. Thus a 300 μm FET with $g_m = 66 \text{ mS}$ and $R_{ds} = 200 \text{ Ohms}$ would require $R = 70 \text{ Ohms}$ to provide a match to $Z_0 = 50 \text{ Ohms}$, with a gain of $0.066 \cdot 50 / 2 = 1.7$.

A more common output matching stage is the source follower, or common drain, configuration shown with a current-source load in Figure 3.9(a). Analysis of the equivalent circuit in Figure 3.9(b) yields the following expressions for gain, Z_{in} and Z_{out} :

$$V_o/V_i = (g_{m1} + S C_{gs1}) / [(g_{ds1} + g_{ds2} + g_{m1}) + S(C_{gs1} + C_{ds1} + C_{ds2} + C_{gd2})] \quad (3.7)$$

$$Z_{out} = 1 / [(g_{m1} + g_{ds1} + g_{ds2}) + S(C_{gs1} + C_{ds1} + C_{ds2} + C_{gd2})] \quad (3.8)$$

Figure 3.9. (a) Source follower stage, (b) equivalent circuit.

$$Z_{in} = 1/S(C_{gd1} + [1 - V_o/V_i]C_{gs1}) \quad (3.9)$$

or

$$C_{in} = C_{gd1} + [1 - V_o/V_i]C_{gs1}$$

The derivation for Z_{out} assumes the gate of FET1 to be connected to some negligibly small impedance compared to that of C_{gs1} . This condition can easily be met at UHF and L band since $Z_c = 1/j\omega C_{gs1}$ remains large compared to other impedances likely to be attached to the gate, such as R_{ds} from a preceding gain stage.

The transfer functions for both V_o/V_i and Z_{out} contain the same pole

$$\omega_p = (g_{m1} + g_{ds1} + g_{ds2}) / (C_{gs1} + C_{ds1} + C_{ds2} + C_{gd2})$$

which is located in the 15 to 17 GHz range, depending on the choice of W_1 and W_2 . Thus for all practical purposes equations 3.7 and 3.8 can be written in their approximate low-frequency form:

$$V_o/V_i = g_{m1} / (g_{m1} + g_{ds1} + g_{ds2})$$

$$Z_{out} = 1 / (g_{m1} + g_{ds1} + g_{ds2})$$

By equating $1/Z_{out}$ to Y_o , the characteristic admittance, the condition for a perfect output match is obtained:

$$Y_o = g_{m1} + g_{ds1} + g_{ds2}$$

or

$$Y_o = W(g_{m1}' + g_{ds1}' + g_{ds2}')$$

where the primed parameters represent the standard-width values. Once the % I_{dss} operation of the two FETs has been chosen, as determined by n , the value of W is uniquely defined. For $Y_o = 20 \text{ mS}$ the possible combinations of n , W and resulting gain into 50Ω are given in Table 3.5.

Table 3.5 Bias Conditions and Performance of the Source Follower Stage.

n	% I_{dss1}	% I_{dss2}	W (for 50Ω match)	V_o/V_i (into 50Ω)
1	100	100	0.26	0.43
0.5	50	100	0.32	0.44
0.2	20	100	0.41	0.45

One sees that the FET size ranges from 78 μm ($W=0.26$) to 123 μm ($W=0.41$) for the various bias points without affecting the gain, which remains at approximately 0.44. Thus using this value of gain it is now possible to evaluate Z_{in} . From equation 3.9

$$C_{in} = W(C_{gd1}' + [1 - V_o/V_i]C_{gs1}')$$

which for $n=1$ gives an equivalent input capacitance of $C_{in} = 0.26(56 + 0.56 \cdot 473) = 0.08 \text{ pF}$, considerably less than the minimum $0.26 \cdot 0.473 = 0.12 \text{ pF}$ input capacitance that would have been obtained with a common source output stage. Hence the source follower has the desirable property of providing a very wide band output match without introducing excessive load capacitance to the preceding stage. For this reason it is sometimes called an "interstage buffer" since C_{in} is also very insensitive to load capacitances that may be placed at the output. This is important when bandwidth is to be maximized.

3.2.5 Direct-Coupled Amplifier and Active Feedback

First introduced by Hornbuckle and Van Tuyl [16], this MMIC building block has found widespread use due to its ability to provide broad bandwidth amplification from DC frequency. This is achieved by connecting FETs of different stages directly together without coupling capacitors, as shown in Figure 3.10(a).

A common source FET with active load is used as the amplifying element, followed by a buffer stage consisting of a source-follower and level-shifting diodes. The active load fixes the quiescent current of the CS FET at half its saturation current which

(a)

(b)

Figure 3.10. Direct-coupled amplifier. (a) Open loop configuration, (b) with active feedback.

corresponds to $V_{GS} = -1$ volt. The source follower (FET3) and its active load (FET4) are both the same size and hence $V_{GS3} = 0$ V for operation at 100% I_{DSS} . The voltage drop across a GaAs diode with series resistance is about 1 V. Therefore approximately 4 volts of level shifting is provided by the four diodes in the buffer circuit so that a +3 V drain voltage at the CS FET results in a -1 V level at the

output. This is a suitable voltage for direct DC-coupling to the next amplifying stage, identical to the first one and requiring $V_{GS} = -1$ V for its common source FET.

Feedback can be added to this stage to produce the circuit of Figure 3.10(b) which has improved bandwidth and reduced gain. Active feedback is obtained with a FET typically one-quarter the width of the CS FET ($\alpha = 0.75$, $\beta = 0.25$) and is used with the advantage that it provides larger gain-bandwidth products than are attainable with resistive feedback [16].

Analysis of the open loop and feedback stages is done using the small signal equivalent circuits as before. Ignoring the diode series resistance for simplicity, the low frequency gains obtained by Hornbuckle are

$$(V_o/V_i)_{o/l} = -g_{m1}g_{m3}/[(g_{ds3}+g_{ds4}+g_{m3})(g_{ds1}+g_{ds2})]$$

$$(V_o/V_i)_{f/b} = -\alpha g_{m1}g_{m3}/[(g_{ds1}+g_{ds2})(g_{ds3}+g_{ds4}+g_{m3})+g_{d3}\beta g_{m1}]$$

while the poles are at

$$\omega_{p1,2} = (-B \pm \sqrt{B^2 - 4AC})/2A$$

where

$$A = C_{gs3}(C_S + C_L) + C_S C_L$$

$$B = g_S(C_L + C_{gs3}) + g_L(C_S + C_{gs3}) + g_{m3}C_L + \beta g_{m1}C_{gs3}C_{gs3}$$

$$C = (g_S + g_{m3})g_L + \beta g_{ds3}g_{m1}$$

in which

$$C_L = C_{ds1} + C_{ds2} + C_{dg2} + C_{dg3} + (1 + g_L/g_{m1})C_{dg1}$$

$$C_S = C_{ds3} + C_{ds4} + C_{dg4} + \beta C_{gs1}$$

$$g_L = g_{ds1} + g_{ds2}$$

$$g_S = g_{ds3} + g_{ds4}$$

Bandwidth is controlled by the size of the feedback FET (increasing with larger β) and additional gain can always be obtained by cascading more stages. Thus when the output buffer's source-follower is suitably chosen so as to match to 50 Ω (Sec. 3.2.4) this topology is capable of simultaneously satisfying gain, bandwidth and output matching.

3.3 Noise Representation at UHF

Although noise performance is not a major consideration in this work, it is important to get an estimate of what the noise figure will be so that this parameter may be optimized wherever possible. To this end, a simple technique for noise analysis of an arbitrary circuit at low frequencies will be described.

3.3.1 Equivalent Input Noise Voltage of a FET

In general the noise behaviour of a FET in the common source configuration is completely described by three noise parameters:

F_{min} , the minimum obtainable noise figure; Z_{opt} , the signal source impedance (equal to $R_{opt} + jX_{opt}$) required to achieve F_{min} ; R_n , the equivalent noise resistance. For any signal source impedance $Z_{ss} = R_{ss} + jX_{ss}$ other than Z_{opt} , the noise figure is given by [24]

$$F = F_{min} + (R_n/R_{ss})[(R_{ss}-R_{opt})^2 + (X_{ss}-X_{opt})^2]/[R_{opt}^2 + X_{opt}^2]$$

For the case of a FET connected directly to the source in a 50 Ω system this expression becomes

$$F_{50} = F_{min} + (R_n/R_{ss})[((50-R_{opt})^2 + X_{opt}^2)/(R_{opt}^2 + X_{opt}^2)] \quad (3.10)$$

The noise parameters can be obtained from one's own measurements or from data provided by the foundry. In the latter case the noise information is normally limited to a few FET bias points and one gate width, and is of little use in MMIC designs with widely varying FET sizes. To alleviate this problem, several authors have represented the noise parameters in terms of the FET small signal equivalent circuit elements and empirical fitting factors [25,26,27]. Such a representation is completely general in that the noise properties of a FET of any size operating under any bias condition may be characterized.

The work of Fukui in this area [26], which has received widespread acceptance, resulted in the following relationships:

$$F_{min} = 1 + K_1 f C_{gs} \sqrt{(R_g + R_s)/g_m}$$

$$R_n = K_2/g_m$$

$$R_{opt} = K_3[1/(4g_m) + R_g + R_s]$$

$$X_{opt} = K_4 / (f C_{gs})$$

for R_n , R_{opt} , R_g , R_s , X_{opt} in Ohms, g_m in Siemens, C_{gs} in pF, and f in GHz. The equivalent circuit parameters are those corresponding to zero gate bias (the 100% I_{dss} values) while the experimentally obtained constants K_1 to K_4 vary slightly with gate bias and provide the dependency of noise on % I_{dss} drain current. Typically, $K_1 = 0.016$, $K_2 = 0.8$, $K_3 = 2.2$ and $K_4 = 160$.

Since R_g and R_s are inversely proportional to gate width W , and C_{gs} and g_m scale proportionally to W , it is easily deduced from the above expressions that F_{min} is independent of W whereas R_n , R_{opt} and X_{opt} vary inversely with W . This fact will be made use of at a later stage to show how the equivalent FET noise voltage varies with W .

From the foundry noise data given for the standard 300 μm wide TriQuint FET, the three noise parameters at 1 GHz are $F_{min} = 1.2$, $R_n = 45.1 \Omega$, and $Z_{opt} = 70 + j310 \Omega$. Substituting these into eqn (3.10) gives the unmatched noise figure

$$\begin{aligned} F_{50} &= 1.2 + 45/50[(50-70)^2 + (310)^2 / (70^2 + 310^2)] \\ &= 1.2 + 45/50[0.96] = 2.1 \text{ or } 3.1 \text{ dB} \end{aligned}$$

For FETs having F_{min} close to 1 and $X_{opt} \gg R_{opt}$ such that the term in square brackets in eqn (3.10) approaches unity, the following approximation becomes valid:

$$F_{50} \approx 1 + R_n/R_{ss} = 1 + 45/50 = 1.9 \text{ or } 2.8 \text{ dB} \quad (3.11)$$

Given that $X_{opt} = K_4/fC_{gs}$, the second condition is only met at sufficiently low frequencies. This is the case up to L band for most 0.5 and 1 μm long FETs currently available [12,28].

The approximate noise representation with only R_n as a parameter allows the FET to be treated as a noiseless device having a single equivalent input noise generator e_n at its gate, as shown in Figure 3.11, where $e_n = \sqrt{4kT\Delta f R_n}$ represents the equivalent thermal noise due to R_n .

Figure 3.11. Equivalent input noise voltage (e_n) of a FET.

Since the thermal noise of a $50\ \Omega$ source is $e_{ss} = \sqrt{4kT\Delta f R_{ss}}$ the noise figure is

$$F_{50} = 1 + (e_n/e_{ss})^2 = 1 + R_n/R_{ss}$$

which is identical to the approximate form given in eqn (3.11). By using equivalent voltages to represent the noise of a FET, multi-FET structures whose voltage transfer functions are known may be easily analyzed as will be seen in the next section. Also, from the definition of e_n the effect of gate width W on F_{50} is readily appreciated: e_n is proportional to $\sqrt{R_n}$ and hence is proportional to $1/\sqrt{W}$. Thus the lowest F_{50} is obtained with the largest size of FET.

3.3.2 Noise Figure of an Arbitrary FET Circuit

In a multi-FET circuit the contribution of each FET to the overall noise figure can be calculated using the input noise representation and the technique described below. First, a noise equivalent circuit must be drawn showing the locations of the various noise generators. This is followed by a low frequency circuit analysis to determine what each source's noise voltage would be if it were placed at the input of the circuit. The resulting quantities are squared and summed together to obtain the total equivalent input noise voltage, V_{eq}^2 , from which the overall noise figure can then be found:

$$F = 1 + V_{eq}^2/e_{ss}^2$$

To illustrate this method more clearly the noise figure of a gain stage consisting of a common source FET with active load (Figure 3.12a) will be evaluated as an example. The analysis is based on Hornbuckle's paper [16].

The amplifier's noise equivalent circuit is shown in Figure 3.12(b). For the low frequency analysis all capacitors are treated as open circuits and need not be shown; however, for clarity in representing the voltages, C_{gs} is left in the diagram.

Since noise voltage e_{n1} is already at the input of the circuit only e_{n2} 's input equivalent must be found. This is done by calculating the output voltage due to e_{n2} and dividing the result by the voltage gain of the complete amplifier stage. Thus, with e_{n1} shorted out,

Figure 3.12. Example of noise figure analysis. (a) Common source FET with active load, (b) noise equivalent circuit.

$$(e_{n2})_{out} = e_{n2} \cdot g_{m2} \cdot g_L$$

and

$$V_o/V_i = g_{m1} \cdot g_L$$

so that

$$(e_{n2})_{in} = (e_{n2})_{out}/(V_o/V_i) = e_{n2} \cdot g_{m2}/g_{m1}$$

The equivalent input noise voltage is

$$(V_{eq})^2 = (e_{n1})^2 + (e_{n2})_{in}^2 = e_{n1}^2 + [e_{n2} \cdot g_{m2}/g_{m1}]^2$$

and hence the noise figure is

$$F = 1 + V_{eq}^2/e_{ss}^2 = 1 + R_{n1}/R_{ss} + R_{n2}/R_{ss}[g_{m2}/g_{m1}]^2$$

which is the desired result showing how each parameter affects the overall noise behaviour.

3.4 S Parameters from Voltage Transfer Functions

The performance of microwave circuits is normally given in terms of S parameters rather than voltage transfer functions. If the transfer function expression is modified to take into account the characteristic impedance Z_0 of the source, the equivalent S parameters can be obtained. Referring to Figure 3.13, V_o/V_{ss} is found instead of V_o/V_i .

Figure 3.13. Circuit representation for S parameter calculations.

Then [29],

$$S_{21} = 2 \cdot V_o / V_{ss}$$

$$S_{11} = (Z_{in} - Z_o) / (Z_{in} + Z_o)$$

$$S_{22} = (Z_{out} - Z_o) / (Z_{out} + Z_o)$$

and S_{12} is assumed to be 0 for circuits which don't employ feedback since S_{12} of the individual FETs is practically zero at these frequencies. The reason for multiplying the voltage gain by 2 to obtain S_{21} is that this parameter represents the insertion gain. Without the factor of 2 a simple short circuit between source and load would give an attenuation of 1/2 instead of 1 as expected.

4. A LOW-CURRENT MMIC AMPLIFIER

Having become familiar with MMIC amplifiers in Chapter 3, the design of a low-current amplifier to meet specific goals may now be undertaken. This task consists of the following points: (1) low DC power considerations, in which the most efficient circuit topology must be chosen, (2) bandwidth considerations, where feedback is used to achieve a sufficiently broad bandwidth, and (3) noise considerations, where the input stage is optimized to obtain the lowest possible noise figure. After presenting the amplifier specifications, each of these aspects of the design will be discussed in the following sections.

4.1 Goals

In a mobile phone, the low-current amplifier is situated between the receiver's antenna and its mixer stage, and provides RF amplification of the received signal before it is downconverted to a lower IF frequency. The amplifier's performance requirements are partly defined by a cellular phone manufacturer, whose specifications call for a gain of 18 dB into a $50\ \Omega$ load at 800 ± 50 MHz, with a noise figure of 5 dB. The remaining specifications come from a variety of papers dealing with MMIC low-current amplifiers for mobile radio. Thus, a DC power consumption of less than 100 mW is required along with an output return loss of -15 dB [23,30,31]. No specification is put on the input return loss since the amplifier is connected directly to the antenna and any reflected power is simply reradiated.

Without altering the minimum goals set out so far, a number of additional requirements must be met. For the amplifier to be used as a general purpose IF gain block, and to include the future mobile radio band at 2 GHz, a bandwidth covering at least 0.5 to 2.5 GHz is needed [14,31,32]. (IF amplifiers being normally driven from a high impedance mixer output, an input match to 50 Ω is still not necessary).

Several amplifiers reported in the literature achieve low power dissipation and wide bandwidth through the use of interstage peaking inductors and large load inductors, which often consume more GaAs area than the rest of the circuitry combined [13,16,30]. Since Colleran has shown that a bandwidth extending beyond 3 GHz is possible without inductors [33], although at a cost of higher DC power, a further requirement that no inductors be allowed in the amplifier design is made. This allows the chip size and ultimately the cost of the amplifier to be reduced.

Off-chip capacitors are also needed to keep GaAs area usage to a minimum. These are normally large-valued RF coupling capacitors or DC supply bypass capacitors. Placing them off the chip is acceptable for a single function design, as they may be easily incorporated into irregular free spaces which arise in larger multi-function chips. It is expected that the amplifier circuit will eventually form only a part of a completely integrated MMIC receiver front end, thereby satisfying this condition. Table 4.1 gives a summary of all the amplifier requirements.

Table 4.1. Amplifier Specifications

Parameter	Goal
Gain	18 dB
Bandwidth	0.5 to 2.5 GHz
Noise Figure	5 dB
Power Consumption	<100 mW
Inductors	not allowed
Off-chip caps.	allowed

4.2 Low-Power Considerations

DC power dissipation, being defined as $V \cdot I$, can only be made small by minimizing voltage, current, or both of these together. The following discussion describes how this simple concept may be applied to all aspects of amplifier design, and what tradeoffs are involved in the process. This will establish the necessary guidelines for selecting a suitable topology for the low current amplifier.

4.2.1 General Techniques

There are a variety of ways to minimize an amplifier's power dissipation. The most obvious one is to reduce the size of the FET since, as was seen in Ch. 2, the voltage gain of an amplifying stage is independent of gate width whereas the current through it is proportional to W . Thus by reducing W to as small a value as possible one can obtain increasingly better efficiency, as defined by the gain to DC power ratio. However, this comes at the expense of increased input noise voltage (e_n is proportional to $1/\sqrt{W}$) and

hence involves a tradeoff between noise and power. Also, W cannot be chosen arbitrarily small for active matching as this requires a uniquely defined value of g_m (approximately 20 mS) to achieve a match to 50 Ohms.

Another way of reducing the current through a FET without altering its gate width is to bias it close to its pinchoff region. This entails a tradeoff between gain and noise and will be discussed in the next section.

The direct-coupled circuit approach (Sec.3.2.5) relies on level-shifting diodes to produce appropriate DC voltages so as to eliminate coupling capacitors. This approach is not conducive to low power circuits as the $(V \cdot I)_{\text{diode}}$ power is wasted in that the diodes do not contribute to RF gain [16]. Thus capacitive coupling between independently biased stages is the preferred technique, and is all the more viable when used with the small W approach since the required capacitor values are much smaller.

The gain of an amplifying stage depends on the magnitude of its load impedance. In the absence of load inductors, the only way to obtain high gain is by using large load resistors with correspondingly large voltage drops. Active loads are therefore required as they are more power efficient. This is readily seen by comparing the power dissipation of an active load and an equivalent resistor. For a 300 μm FET connected as an active load ($V_{ds} = 2.5$ V, $I_{ds} = I_{dss} = 70$ mA), the resistance provided is $R_{ds} = 200 \Omega$ while the power dissipated in it is

$$P_{\text{diss}} = V_{ds} \cdot I_{ds} = 2.5 \cdot (70 \text{ mA}) = 175 \text{ mW}$$

For an equivalent 200 Ω resistor with the same current flowing through it

$$P_{\text{diss}} = R \cdot I^2 = 200 \cdot (70 \text{ mA})^2 = 980 \text{ mW}$$

which is approximately 5 times greater than in the active load case.

In multi-FET structures careful attention must be paid to the relative gate widths in order to obtain optimum efficiency. For example the common source amplifier stage gives a gain of 6.5 when both FETs are of equal size, and 7.9 when the active load (FET2) is 5 times larger than FET1 (Sec. 3.2.1). In both cases the DC power dissipation can be made the same, thus the second case is more power efficient. This is important when the minimum allowable FET size has been reached, as illustrated in the following example.

A common source amplifier (Figure 4.1) can be designed with 12 μm FETs (i.e. $W_1 = W_2 = 0.04$) so that its gain is 6.5. Since from Sec. 3.2.1, $V = V_{\text{DD}} = 5$ Volts and $I = W_2 \cdot 70 \text{ mA} = 2.8 \text{ mA}$, the power dissipation is

$$P_{\text{diss}} = V \cdot I = 5 \cdot 2.8 = 14 \text{ mW}$$

and the gain-to-DC power efficiency is

$$\eta = \text{gain}/P_{\text{diss}} = 6.5/14 = 0.46 \text{ mW}^{-1}$$

No further reduction in FET width to increase η is possible since $W = 0.04$ is the smallest size allowed by the foundry.

Figure 4.1. Common source amplifier example

If FET2 remains at $12\ \mu\text{m}$ and W_1 is chosen to be 5 times larger for operation of FET1 at 20% I_{DSS} , the amplifier gain becomes 7.9. Following the same DC power calculation, P_{Diss} remains unchanged and the efficiency is

$$\eta = 7.9/14 = 0.56\ \text{mW}^{-1}$$

an increase of 20 %. Thus, strictly speaking optimum efficiency is achieved for $W_1 = 5 \cdot W_2$. However this is only the case when no further power is required to generate the negative V_{GS1} voltage at the gate of FET1, an assumption which may not always be valid.

Another means of reducing power consumption is to reduce the drain-to-source bias voltage, V_{DS} . This has the effect of providing less gain per stage but is still more efficient overall [12]. Although no complete FET models for low voltage bias are currently available from the foundry, measured curves contained in the TriQuint manual indicate that R_{DS} remains constant while g_m decreases by approximately 10% for a drop in V_{DS} from 2.5 to 1.5 V. This would imply that the common source stage of the previous example would have a gain of 5.8 instead of 6.5, a power dissipation of 8.4 mW instead of 14 mW and, as a result, an efficiency of 0.69

instead of 0.46.

Finally, appropriate selection of circuit topology can lead to a low power design. The most recurring theme in the literature is the "drain current saving technique" which allows the currents of two or more stages to be combined in such a way that the amplifying FET receives a larger drain current [30,34]. This is shown in Figure 4.2 where the three diodes in the source-follower output stage of Fig. 4.2(a) are removed in Fig. 4.2(b) by feeding this stage's current to a larger common source FET. The bias circuitry required at the gate of the source follower FET is not shown, but remains the same in both cases. Generalizations on other topologies cannot be made since the choice of a particular configuration is highly dependent on the application.

Figure 4.2. Application of drain current saving technique to circuit in (a), resulting in circuit shown in (b).

4.2.2 Tradeoff Between Gain and Noise Figure for a FET Biased Close to Pinchoff

As mentioned earlier, low power dissipation can be achieved with small FET bias currents. This requires either a small FET operating at a high percentage of its saturation current, a large FET biased at a low percentage of I_{DSS} , or some combination in between.

Inherently, a FET's minimum noise figure (F_{min}) decreases with decreasing bias current, down to approximately $I_{DSS}/5$. Below this value F_{min} begins to increase but very little information is available to quantify the extent of this increase. For example the TriQuint design manual gives no noise information for FETs biased at $I_{DSS}/20$. Similarly, no small signal equivalent model is available under this bias condition and hence the gain is also unknown.

In order to determine the low current gain and noise figure, and evaluate the tradeoffs involved, a 300 μm wide, 0.5 μm long Harris FET was measured experimentally. Although this is not the same type of FET as the one used in the amplifier design, the basic characteristics are similar and the conclusions still apply.

A Noise Figure meter which also displays associated gain was used for the measurement. The FET was mounted in a jig designed to accomodate input and output matching stubs for obtaining the minimum noise figure. At an initial test frequency of 1 GHz it was found that as the optimum noise match was approached, the FET became unstable due to the proximity of its unstable region to the minimum NF match on the Smith Chart.

The test was repeated at 8 GHz without the stability problem giving the results shown in Fig. 4.3. It is seen that a minimum noise figure of 2.0 dB is obtained between 15 and 20% I_{DSS}

and that less than 1 dB deterioration occurs when the current is reduced to 5% I_{DSS} ($I_{DSS}/20$). However, the associated gain drops more significantly over this range, starting at 8.6 dB at $I_{DSS}/5$ and decreasing to 6.3 dB at $I_{DSS}/20$. This bias point marks the start of a rapid loss of gain for any further reduction in bias current.

Based on the above observations it is felt that although I_{DS} can be reduced to very low levels with almost no noise penalty, the FET should not be biased below $I_{DSS}/20$. This is because the resulting gain would be insufficient to ensure that the contribution to the overall noise figure of the amplifier is effectively limited to that of the first FET.

Figure 4.3. Tradeoff between a FET's gain and noise figure when biased close to pinchoff.

The loss of gain is also apparent in the equivalent circuit corresponding to the $I_{DSS}/20$ bias condition. S parameters were measured and the model was then extracted to give the element values shown in Table 4.2. A set of values for $I_{DSS}/5$ is also given for comparison. It is noted that the transconductance decreases to approximately half its $I_{DSS}/5$ value, a result which will be important when discussing the unmatched noise figure.

Table 4.2. Equivalent Circuit Elements for Harris 300 μm FET ($V_{DS}=3\text{V}$).

Parameter	$I_{DSS}/20$	$I_{DSS}/5$
g_m	16.3 mS	31.1 mS
C_{gs}	0.194 pF	0.229 pF
C_{gd}	0.151 pF	0.044 pF
C_{ds}	0.069 pF	0.070 pF
R_{ds}	273 Ω	177 Ω

4.2.3 Preliminary Selection of Amplifier Topology

From the various guidelines set out earlier a general circuit topology is now apparent. The amplifier is to be made up of capacitively-coupled stages to avoid the power loss associated with the direct-coupled approach. Biasing of the individual stages is to be achieved with the necessary power supplies, as opposed to the less power-efficient self-biasing technique.

The optimum output stage is a source follower with active load

as shown in Figure 4.4 to provide a match to 50 Ohms with minimum power dissipation, broad bandwidth and low input capacitance.

Figure 4.4. Output source follower (SF) stage of amplifier.

The widths of the two FETs are to be selected appropriately from the design equations given in Ch. 3 in such a way that power dissipation is minimized. As mentioned earlier, such a stage has a voltage attenuation of approximately 0.44.

The gain stage is to consist of a cascode amplifier due to its greater efficiency than the Common Source configuration. Since the load capacitance of the output stage will reduce its bandwidth from the 3 GHz range calculated earlier, bandwidth extension is to be provided by means of negative feedback as shown by the Casc1 circuit (with resistive feedback) in Figure 4.5. The widths of these FETs are to be as small as possible as it is known that the gain provided by the cascode, equal to approximately 11 without feedback, is independent of W . TriQuint's minimum recommended FET width is $10\text{ }\mu\text{m}$ and thus the cascode gate widths should be near this value ($W=0.04$ corresponds to a gate width of $12\text{ }\mu\text{m}$). All three FETs are chosen to operate at 100 % of I_{DSS} for ease of biasing, since the required V_{GS} of 0 V is easily obtained by inserting a large

resistor (not shown) between the gate and source of each of the two lower FETs.

Figure 4.5. Cascode (Casc1) gain stage of the amplifier.

Using the very approximate figures for the Source Follower and Cascode stages the gain of the amplifier so far is $11(0.44) = 5$, or 14 dB, which indicates another gain stage is required to achieve the design goal of at least 18 dB. A second Cascode with feedback, designated as Casc2 in Figure 4.6, should be cascaded directly with Casc1 to provide the remaining 4 dB and compensate for the loss of gain associated with the use of feedback. In reality, the gain of the cascode stages will be less than 11 due to feedback and loading effects; however, it is still useful to evaluate the upper limit on the total available low frequency gain, which is given by the open loop gains of the three stages:

$$G_{\max} = G_{\text{casc1}} \cdot G_{\text{casc2}} \cdot G_{\text{sf}} = 11 \cdot 11 \cdot 0.4 = 48 \text{ or } 34 \text{ dB}$$

Figure 4.6. Three capacitively-coupled stages of the amplifier.

Since no input matching is required, the input stage is actually the casc2 circuit. The noise figure of the complete amplifier is largely dependent on the noise figure of this stage and hence the input FET's width should be chosen as large as possible to achieve the greatest value of transconductance. Thus the overall amplifier circuit is as shown in Figure 4.7.

Figure 4.7. Preliminary version of complete amplifier.

The DC power dissipation of this amplifier can be roughly estimated as follows. For the source follower stage with $W1 = 0.3$ at $20\%I_{DSS}$, the current through FET1 and FET2 (Fig.4.4) is

$$I_{sf} = 20\%(0.3)(70) \text{ mA} = 4.2 \text{ mA}$$

and

$$V_{dd2} = 2 \times 2.5 \text{ V} = 5 \text{ V}$$

thus

$$P_{sf} = 5(4.2) = 21 \text{ mW}$$

For each cascode stage with $W=0.04$ and biased at $100\%I_{dss}$, the current through the three FETs is

$$I_{casc} = 100\%(0.04)(70) \text{ mA} = 2.8 \text{ mA}$$

and

$$V_{dd1} = 3 \times 2.5 \text{ V} = 7.5 \text{ V}$$

therefore

$$P_{casc} = 7.5(2.8) = 21 \text{ mW}$$

Thus the amplifier as shown consumes a total power of

$$P_{tot} = 2P_{casc} + P_{sf} = 2(21) + 21 \text{ mW} = 63 \text{ mW}$$

which is well within the 100 mW design goal.

4.3 Bandwidth Considerations

The amplifier topology chosen in section 4.2.3 is capable of producing more than the required 18 dB of gain as given by the open loop gains of the individual stages, which total up to 34 dB.

However, with multi-stage construction bandwidth shrinkage inevitably results due to the capacitive loading of a given stage by the following one. The object of this section is to evaluate the frequency response of each stage separately and determine how feedback can best be employed to achieve the desired 2.5 GHz bandwidth for the overall amplifier.

The approach taken here is to first analyze the output (third) stage as its capacitive loading will determine the amount of feedback required for the preceding cascode stage, and repeat the procedure for the first and second stages. Since one can no longer treat bandwidth independently of gain and dc power dissipation, the following analyses take into account all of these aspects.

4.3.1 Source Follower

A complete analysis of the source follower output stage gives the following results, where FET1 is chosen to operate at 20% I_{dss} to minimize the current of the SF stage.

From Table 3.5, the value of W_1 required is 0.41 for a perfect output match. However, by choosing a slightly smaller FET width, an output return loss of -15 dB can still be met while reducing the drain current. Thus with $W_1 = 0.38$,

$$Z_{out} = 1/[W_1(g_{m1}' + g_{ds1}' + n g_{ds2}')] = 67.6 \text{ Ohms (or } S_{22} = -16 \text{ dB)}$$

and

$$C_{in} = W_1(C_{gd1}' + 0.56 C_{gs1}') = 0.094 \text{ pF}$$

It should be mentioned that the value of the output impedance Z_{out} is valid only when the source follower FET's gate terminal is connected to ground or some low impedance which is negligible compared to that of its gate-source capacitance C_{gs} . If this condition is not satisfied the output impedance will be larger than predicted.

4.3.2 Cascode with Feedback

From Chapter 3 the bandwidth of the unloaded open-loop cascode with all three FETs having the same width was 3.5 GHz, independently of the actual value of W . When small FETs are used (less than 50 μm), the simple scaling rule is no longer entirely respected, as was seen in Table 2.1, and the fringing capacitances which are added to C_{gs} , C_{gd} , and C_{ds} become a significant portion of these quantities, especially in the case of C_{gd} . This reduces the cascode's bandwidth to only 2.5 GHz for 12 μm FETs ($W = 0.04$), as shown in Fig. 4.8. When the input capacitance of the source follower stage is added as a load onto the cascode stage the bandwidth is further reduced to 0.3 GHz (Fig. 4.8 (b) and (c)). By adding active or passive feedback its bandwidth can be extended. The cascode with passive (resistive) feedback whose small signal equivalent circuit is drawn in Fig. 4.9 will be considered first.

After a lengthy but straightforward circuit analysis the following transfer function is obtained.

$$V_o/V_i = [\alpha S + g_f(g_{ds1} + g_{ds2} + g_{m2}) - g_{m1}(g_{ds2} + g_{m2})]/[AS^2 + BS + C]$$

where

(c)

Figure 4.8. Cascode with $12 \mu\text{m}$ FET widths. (a) unloaded case, (b) 0.094 pF load capacitance, (c) frequency response.

Figure 4.9. (a) Cascode with feedback. (b) Equivalent circuit.

$$\alpha = C_{dg1}(g_{ds2}+g_{m2})+(C_{ds1}+C_{gs2}+C_{dg1})g_f$$

$$A = C_t(C_{ds1}+C_{gs2}+C_{dg1})$$

$$B = C_t(g_{ds1}+g_{ds2}+g_{m2})+(C_{ds1}+C_{gs2}+C_{dg1})(g_{ds3}+g_f+g_{ds2})$$

$$C = (g_{ds3}+g_f)(g_{ds1}+g_{ds2}+g_{m2})+g_{ds2}g_{ds1}$$

with

$$C_t = C_{ds3}+C_{dg2}+C_{dg3}+C_{in}$$

The dominant pole of this expression is approximated by

$$w_p \approx -C/B = [(g_{ds3}+g_f)(g_{ds1}+g_{ds2}+g_{m2}) + g_{ds2}g_{ds1}] / [C_t(g_{ds1}+g_{ds2}+g_{m2}) + (C_{ds1}+C_{gs2}+C_{dg1})(g_{ds3}+g_f+g_{ds2})]$$

Substituting in the values for $W = 12 \mu m$ and g_f in mS gives

$$f_p \approx [1/2\pi][1.73g_f+0.3]/[145.6+68.7g_f] \times 10^{12} \text{ Hz}$$

which is plotted as a function of g_f in Figure 4.10. The plot shows that increasing g_f from 0 (i.e. adding resistive feedback) causes the bandwidth to increase, although with diminishing returns for large values of g_f .

The low-frequency gain is given by

$$V_o/V_i|_{S=0} = [g_f(g_{ds1}+g_{ds2}+g_{m2}) - g_{m1}(g_{ds2}+g_{m2})] / [(g_{ds3}+g_f)(g_{ds1}+g_{ds2}+g_{m2}) + g_{ds2}g_{ds1}]$$

For $W = 0.04$ and g_f in mS, this reduces to

$$V_o/V_i = [g_f-2.427]/[g_f+0.213]$$

Figure 4.10. Gain and bandwidth of the Casc1 stage as a function of feedback conductance g_f .

which is also plotted in Figure 4.10, showing that an increase in g_f causes the gain to decrease as expected. One sees that by choosing $g_f = 0.4$ mS (or $R_f = 2.5$ k Ω) the bandwidth of the Casc1 stage is extended to approximately 1 GHz while the gain is reduced to 9.4 dB. The gain could be made larger by increasing g_{m1} with little effect on the bandwidth, as this parameter does not appear in the expression for ω_p .

To take into account the loading of this cascode stage (Casc1) on the Casc2 stage it is necessary to calculate its input impedance Z_{in} .

A more complicated analysis leads to

$$Z_{in} = 1 / \{ S[C_{gs1} + (1-G)C_{gd1}] + (1-H)g_f \}$$

where

$$H = V_o / V_i$$

and

$$G = [H(SC_t + g_{ds3} + g_f + g_{ds2}) - g_f] / [g_{ds2} + g_{m2}]$$

Evaluating Z_{in} with SuperCompact an interesting frequency dependence is found to exist: its magnitude increases with frequency up to beyond 3 GHz as shown in Fig. 4.11. This result suggests that resistive feedback around the Casc1 stage can be used not only to broaden its bandwidth but also to present an input impedance that tends to increase the open loop bandwidth of the Casc2 stage. The increased bandwidth is a result of the cascode's transfer function (Sec. 3.2.2) showing the gain to increase with diminishing load conductance, thereby offsetting to a certain extent the gain fall-off which occurs beyond f_p since g_{load} (effectively equal to $1/Z_{in}$) decreases with frequency in this range. This is shown more clearly in Fig. 4.12 which plots the voltage gain frequency response of the Casc2 stage for different values of R_f corresponding to the Z_{in} curves of Fig. 4.11.

Figure 4.11. Input impedance variation of Casc1 stage with frequency.

Figure 4.12. Frequency response of open loop Casc2 stage when loaded with the Casc1 stage.

The effect of Casc1's loading is to extend the bandwidth of the Casc2 stage in much the same way an inductor provides peaking near the upper edge of the frequency response. This has the following two implications: (1) the Casc2 stage does not require feedback resistor R_{f2} to achieve the bandwidth target, and (2) it is not necessary that Casc1's bandwidth be as wide as 2.5 GHz since the peaking of the Casc2 stage will compensate for the shortfall and allow an overall bandwidth of 2.5 GHz to be obtained (Fig. 4.13).

Figure 4.13. Achievement of a 2.5 GHz bandwidth from the Casc1 and Casc2 stages combined.

It should be mentioned that active feedback around the cascode stage can also broaden its bandwidth as shown in Figure 4.14. This technique allows a bandwidth comparable to that in the resistive feedback case to be obtained, but has the disadvantage of presenting a capacitive load (Fig. 4.14(b)) to the preceding cascode stage. Its bandwidth therefore tends to shrink as opposed to being enhanced as is the case with resistive feedback.

(a)

$$C_{in} = \alpha C_{gs1} + C_a = \alpha C_{gs1} + (1 - 1/K) \alpha C_{gd1}$$

(b)

Figure 4.14. (a) Cascode with active feedback, (b) equivalent input capacitance.

4.4 Simplified Complete Circuit

The previous section identified the important variables affecting the gain and bandwidth of the three stages and showed how the behaviour of the Casc2 stage is dependent on the choice of g_f in the

Casc1 stage. As a result it is necessary to consider both these stages together when determining the final value of g_f . Before this parameter is selected however, the Casc1 and SF stages will be treated together so that their combined gain may be optimized.

Figure 4.15 illustrates the principle of the drain-current saving technique in which the current flowing through the SF stage is combined with the drain current of the common source FET in the Casc1 stage.

Figure 4.15. Drain current saving technique applied to the Casc1 and SF stages.

The extra current through FET1 requires that its gate width be made larger. With FET1 operating at 100% I_{dss} , W_1 must equal the sum of W_3 (0.04) and W_5 (0.08) so that W_1 now becomes 0.12, three times its original value. Since transconductance is proportional to gate width, g_{m1} also increases by a factor of three and the condition for increasing the gain of the cascode without affecting its

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bandwidth (Sec. 4.3.2) is satisfied. The low frequency gain as a function of g_f , plotted in Figure 4.16 for $W_1 = 0.04$ and 0.12 shows that this technique offers an increase of 7 to 9 dB in gain.

Figure 4.16. Gain of Casc1 stage as a function of feedback conductance for an increased width of FET1.

It must be verified that the preceding circuit modification does not degrade the Casc2-SF block's other desirable characteristics, namely its input and output impedances. In general, a large change in RF performance would not be expected to arise from the connection of a high impedance FET structure to any point in a circuit; in this particular case, it is intuitively seen that moving FET5 from ground

to the input of FET2 in the Casc1 stage will have little effect on circuit behaviour since FET2 is in the common gate configuration and is itself a low impedance. This fact is confirmed by a SuperCompact analysis producing the familiar Z_{in} curves of Figure 4.11, with a slight reduction in Z_{in} 's magnitude. Although a lower Z_{in} translates into a lower Casc2 gain, the added gain obtained from the Casc1 stage more than compensates for this loss.

The Casc2 stage can now be cascaded with the SF-Casc1 block for final selection of g_f . The resulting complete circuit is shown in Figure 4.17(a) and the associated gain curves for various g_f values are plotted in Figure 4.17(b). Figure 4.17 is a simplified form of the final amplifier as the bias circuitry required around the individual FETs, which is essentially transparent to RF performance in the desired frequency band, still remains to be added. Instead of voltage gain, the parameter S_{21} is plotted to take into account the 50 Ω source and load impedances that will be present in the circuit. The interstage coupling capacitors are taken to be infinitely large for the time being so as not to mask the general characteristics of the response; actual values will be incorporated in the final circuit simulation.

(a)

(b)

Figure 4.17. Simplified complete amplifier. (a) Circuit schematic, (b) S_{21} response.

The value of g_f that is seen to produce a greater than 2.5 GHz bandwidth with over 18 dB of gain is 0.4 mS, or $R_f = 2.5 \text{ k}\Omega$. For this R_f the output return loss curve in Figure 4.18 is obtained, showing that a good match ($S_{22} < -15 \text{ dB}$) exists only over the narrower range of 0.1 to 1.1 GHz.

Figure 4.18. S_{22} response of complete amplifier with $R_f = 2.5 \text{ k}\Omega$.

The absolute minimum requirement of the amplifier is to provide a match to 50 Ohms at 0.8 GHz only, but the achievement of a 2.5 GHz gain bandwidth now makes it desirable to obtain an equally broadband output match. However, the gain broadness is due to the

Cascade's input and output impedance characteristic (both $|Z_{11}|$ and $|Z_{22}|$ increase with frequency as shown in Figure 4.19). This is the very factor limiting the broadness of the output match since the gate of the SF stage must see a decreasing impedance with frequency, as was described in Sec. 4.3.1

Figure 4.19. Input ($|Z_{11}|$) and output ($|Z_{22}|$) impedances of the Casc1 stage in the complete circuit.

Because Z_{11} and Z_{22} vary with g_f it is possible in principle to trade off gain bandwidth for output match bandwidth by proper selection of g_f . It was deemed more appropriate to maximize the gain bandwidth in this work as a wider output match is easily

achieved by adding a second source follower stage after the first one.

4.5 Noise Considerations

The amplifier design so far has ignored the issue of noise performance in the belief that the 5 dB Noise Figure (F) requirement could easily be met. As was mentioned earlier, the overall F is mostly determined by that of the first stage, or more precisely, by that of the first FET. Within the limits allowing the gain and the bandwidth performance of the amplifier to be maintained, optimization of the first (Casc2) stage for noise will be done in this section. The noise analysis techniques developed in chapter 3 will then be used to predict the F of the Casc2 stage to get an optimistic estimate of the complete amplifier's noise figure.

4.5.1 Selection of Input FET Width

From Chapter 3 the noise figure of a FET in the common source configuration with its gate connected directly to the signal source is defined as

$$F = 1 + R_n/R_{ss}$$

in which R_{ss} is the source impedance (50 Ohms), R_n is the FET's equivalent noise resistance, and

$$R_n = \text{constant}/g_m$$

To achieve the lowest possible noise figure, R_n must be minimized, which is equivalent to increasing g_m as much as possible. This requirement goes against the condition for low power consumption whereby primarily small FETs having low currents and transconductances are used in the amplifier design. The question therefore is how to increase the g_m of the input FET without adversely affecting the amplifier's RF performance or DC power consumption.

The power dissipation of the input FET in its present form ($W = 0.2$, $I_{ds} = 20\%I_{dss}$, $V_{ds} = 2.5$ V) is

$$P_{FET1} = V \cdot I = 2.5 \cdot (0.2) \cdot (0.2) \cdot (70) = 7 \text{ mW}$$

whereas its transconductance is

$$g_m = 43.5 \text{ mS} / 5 = 8.7 \text{ mS}$$

For the same amount of DC power W can be made smaller or larger by varying the fraction of I_{dss} at which the FET operates, with the result that g_m varies in each case. Thus all the conditions in Table 4.2 below represent the same power consumption, but g_m is maximized for the largest value of W .

The gain of the input FET depends not only on its own characteristics but also on the impedance Z_{in} , essentially resistive, seen looking into FET2 of the Casc2 stage (Figure 4.20). If Z_{in} is much smaller than R_{ds} of FET1, then FET1's gain would be largely independent of its own R_{ds} since

$$\text{gain}_{FET1} = g_m \cdot (R_{ds} || Z_{in}) = g_m \cdot Z_{in} \text{ for } Z_{in} \ll R_{ds}$$

Table 4.2. Possible widths and bias conditions for the input FET.

W	%Idss	g_{m300} (width=300 μm)	$g_m = W \cdot g_{m300}$ (width = W)
0.04	100	65 mS	2.6 mS
0.08	50	56 mS	4.5 mS
0.20	20	43.5 mS	8.7 mS
0.80	5	22.9 mS	18.3 mS

Figure 4.20. (a) Input FET and (b) equivalent circuit.

and hence FET1's gain would tend to increase with a larger value of g_m .

Rather than evaluate Z_{in} explicitly and observe whether this condition exists, it is simpler to analyze the effect of increasing the input FET width with SuperCompact, which will also show any change in bandwidth.

Figure 4.21 shows the change in the S_{21} response of the amplifier when W_1 is increased from 0.2 to 0.8. It is observed that both the gain and the bandwidth are enhanced by increasing the input FET width. Thus $W_1 = 0.8$, corresponding to a 240 μm gate width, will be used for optimized noise performance.

Figure 4.21. S_{21} response of the amplifier with a 240 μm input FET width.

4.5.2 Overall Noise Figure

Using the techniques of Chapter 3 the noise figure of the first stage (Casc2), which gives a good indication of the overall noise figure, is evaluated at 1 GHz as follows.

The noise equivalent circuit is drawn in Figure 4.22, where g_L represents the input conductance of the Casc1 stage. From Fig. 4.19

Figure 4.22. Noise equivalent circuit for the amplifier first stage.

$Z_{11} = 500 \, \Omega$ (real) so that $g_L = 2 \, \text{mS}$. Starting with FET2, the noise voltage at node A due to e_{n2} when e_{n1} and e_{n3} are shorted out can be found by circuit analysis to be

$$V_1 = g_{m2}e_{n2}/(g_{m2}+g_{ds2}g_{ds1}/(g_{ds3}+g_L) + g_{ds2}+g_{ds1})$$

This must be divided by the gain G_1 of FET1 to find the equivalent of V_1 at the input. For the common source configuration,

$$G_1 = g_{m1}/(g_{ds1}+g_{in})$$

$$\text{where } g_{in} = (g_{ds3}+g_L)(g_{m2}+g_{ds2})/(g_{ds3}+g_L+g_{ds2})$$

Thus, the noise due to e_{n2} at the input is

$$V_{n2} = V_1/G_1$$

For FET3, the equivalent of e_{n3} at node B is found to be

$$V_2 = g_{m3}e_{n3}/(g_{ds3}+g_L+g_d)$$

$$\text{where } g_d = g_{ds1}g_{ds2}/(g_{ds1}+g_{ds2})$$

This must be divided by the total gain G_2 of FET1 and FET2 together, which is the cascode gain:

$$G_2 = G_1(g_{m2}+g_{ds2})/(g_{ds3}+g_L+g_{ds2})$$

Hence, the noise equivalent of e_{n3} at the input is

$$V_{n3} = V_2/G_2$$

and the total equivalent input noise is

$$V_{eq}^2 = e_{n1}^2 + V_{n2}^2 + V_{n3}^2$$

Finally, the noise figure is obtained as

$$F = 1 + V_{eq}^2/V_{ss}^2$$

From the noise data provided by TriQuint for the 300 μm FET, $R_n = 35 \Omega$ for 20% I_{dss} bias current (used for FET1 even though it is operating at 5% I_{dss}) and $R_n = 45 \Omega$ for 100% I_{dss} (FET2 and FET3). These values can be scaled and used with the equivalent circuit element values given in Ch. 2 (scaled as well) to evaluate the above expressions. The resulting noise figure is found to be 5.66 dB, which is slightly above the 5 dB target value.

4.6 Complete Amplifier

As a final step in the amplifier design, the circuitry required to properly bias each FET at the prescribed operating point must be included. Also, the inductances of the lines feeding RF and DC power to or from the amplifier, as well as the DC supply decoupling capacitances, need to be added so that their effect may be known. This will produce a circuit which is complete in every respect and whose simulated response can be compared directly with measurements.

Six of the eight FETs operate at 100% I_{dss} , which is the simplest

case in terms of biasing. Since V_{GS} must be zero and negligible DC current flows into the gate, a large resistor connected between the gate and source can be used. The RF signal sees a high impedance, and hence is unaffected, while $V_G = V_S$ is maintained. A 10 k Ω resistor is sufficiently large for this purpose.

The remaining two transistors, the input FET and the source follower FET, require negative V_{GS} voltages for operation at 5% I_{DSS} and 20% I_{DSS} respectively. The appropriate gate voltages are generated by external supplies and brought into the circuit via large resistors. For the source follower FET, a 10 k Ω resistor is used to ensure adequate RF isolation. A 150 Ω resistor is used to bias the gate of the input FET, providing attenuation of the incoming RF signal to the amplifier in order to bring its overall gain closer to the 18 dB design goal.

DC blocking between stages is accomplished by means of 1 pF coupling capacitors, as is the RF grounding of the two gates in the cascode stages. A 1 pF capacitor is also used for DC isolation between the two points of the resistive (R_f) feedback path.

Figure 4.23(a) is the resulting complete amplifier schematic. Not shown in the Figure are the external (off-chip) elements such as the 0.8 nH bonding wire inductances in series with all DC and RF inputs and outputs of the amplifier, the 20 pF RF coupling (series) capacitors, and the separate 10 pF decoupling (shunt) capacitors for

$R = 10 \text{ k}\Omega$; $C = 1 \text{ pF}$ (all); $R_f = 2.5 \text{ k}\Omega$

(a)

(

Figure 4.23. (a) Complete amplifier schematic, (b) simulated S parameter response including external inductors and capacitors.

each supply. These are nonetheless included in the complete simulation, giving the performance shown in Figure 4.23(b).

Comparing with Figure 4.21, it is seen that the S_{21} response is generally unaffected by the additional circuit components, except at the lower frequencies where the gain is lower. This is to be expected due to the finite size of the capacitors. Also, the midband gain is reduced to approximately 20 dB as a result of the 150 Ω input resistor. The S_{11} and S_{22} parameters are affected in a similar way at low frequencies, showing that a poorer match is obtained below 0.5 GHz.

A recalculation of the amplifier's DC power dissipation, following the method of Sec. 4.2.3 with the final FET widths, results in a total current of 11.2 mA giving $P_{\text{diss}} = 83$ mW.

4.7 MMIC Implementation

With the design of the circuit completed it may now be implemented in MMIC technology using the TriQuint GaAs 3A process. This consists of first laying out the amplifier and then repeating the circuit simulation with SuperCompact to take into account any changes introduced in the layout step.

The layout of the amplifier, representing the 14 mask layers of the TriQuint process, is shown in Figure 4.24. The design considerations pertaining to each component are discussed below.

Figure 4.24. MMIC layout of amplifier circuit.

FET layout: Figure 4.25 shows the layout of the 240 μm FET. The device consists of five identical 48 μm -wide FET cells ($5 \times 48 \mu\text{m}$) placed side by side. This arrangement has the advantage of lowering gate resistance (R_g) because the signal is fed to the gate at five points along its width rather than only at one end. Another advantage is that the five sub-FETs share common source and drain terminals so as to minimize C_{ds} , with the resulting box-like structure exhibiting good area efficiency. It should also be mentioned that this layout closely follows the standard $6 \times 50 \mu\text{m}$ one provided by TriQuint and for which the equivalent circuit parameters have been extracted. Any large variation from it (e.g. using a 3×80

um geometry) would introduce unaccounted variations in the equivalent circuit. The 120 μm Source Follower FET follows the same principle and is made up of two 60 μm -wide gate fingers, while the remaining 12 μm , 24 μm , and 36 μm FETs are all single-fingered (Figure 4.24).

Figure 4.25. Layout of a 240 μm wide FET.

Passive Elements: Due to area limitations only the 1 pF capacitors can be placed on-chip. The larger coupling capacitors required at the input and output of the circuit, as well as the power supply decoupling capacitors, have to be left off-chip and will be considered in a later section. From the TriQuint manual the MIM capacitor has a capacitance per unit area of $0.275 \text{ fF}/\mu\text{m}^2$ and thus the dimensions required to achieve 1 pF are $60 \mu\text{m} \times 60 \mu\text{m}$. All resistors except the 150 Ohm input resistor are chosen to be of the N^- implant type as these have the highest sheet resistance (500 Ohms/square), which is most suitable for large values. The 10 kOhm resistors must therefore be 20 times longer than they are wide, where the width is determined by the amount of current flow. In this case the 10 kOhm resistors are simply for maintaining DC voltages without any appreciable current flowing through them, and hence the minimum allowable 3 μm width is used. As a result these resistors are 60 μm in length.

Interconnects: The lengths of the various microstrip lines are kept extremely short so as to have a negligible effect on the amplifier's overall frequency response. Distributed effects, in which an undesired phase shift along a conductor contributes significantly to the overall phase shift, are insignificant since all of the connecting lengths except one are less than 100 μm (a thousandth of a wavelength at 3 GHz). Only the 230 μm line between the current source of the SF stage and FET1 of the Casc1 stage is long enough to justify modelling it as a distributed element. The width of the interconnects is chosen to be 7 μm , which is sufficiently wide to ensure low parasitic self-inductances. There are no conductors of sufficient length and closeness to warrant special attention to the mutual inductance caused by wire to wire coupling, since a worst-case analysis showed this parasitic to be nonexistent.

Grounding: A ground bar located on one side of the chip is used to connect the circuit ground to the test jig ground via bond wires. This approach is more area efficient than using via holes as each through-the-substrate hole requires an area of $75 \times 75 \mu\text{m}^2$, approximately half the total area required for the ground bar.

Overall circuit layout: To avoid unwanted feedback from the output of the amplifier to the input, the circuit is laid out in such a way that no components of one stage are located in the vicinity of another stage. Also, a minimum spacing between components must be maintained to minimize FET "backgating". This phenomenon is the result of adjacent active and passive devices residing on the GaAs substrate, and which cause voltage fluctuations in the FET's active channel. TriQuint's recommendation of a 3 μm spacing per volt

between the gate of a FET and another structure at a different potential was followed. The FETs which require their source to be grounded are placed next to the ground bar. For all FETs there exists the danger of increasing the C_{gs} or C_{ds} capacitances since the gate fingers extend outside the FETs and terminate in pads close to the source and drain terminals. To minimize this the source and drain terminal conductors were laid out to avoid the gate pads as much as possible. The input and output RF signals as well as the various voltage supplies are also brought in via bond wires to pads situated along the chip's edge. The minimum area required for bonding is $75 \times 75 \mu\text{m}^2$ and hence pads of this size were used. To maintain full DC biasing flexibility, a separate bias pad was provided for each stage of the amplifier, even though all three stages operate from the same 7.5 V supply. Thus, in Figure 4.24 V_{dd1} , V_{dd2} and V_{dd3} correspond to the first, second and third stages of the amplifier, respectively.

The result of the layout process is a $500 \times 350 \mu\text{m}^2$ IC requiring several off-chip capacitors and bond wires to the test jig. The lengths of the bond wires and the values of the capacitors have already been taken into account, but a final circuit simulation was performed to assess the impact of the extra line length introduced between the second and third stages.

Figure 4.26 gives the final S parameters of the complete amplifier, which represent the expected performance to be measured in Chapter 5. No significant change has occurred other than a slight flattening of the S_{21} response in the 2 to 2.5 GHz range.

Figure 4.26. S parameters from the final amplifier simulation including layout effects.

CHAPTER 5. EXPERIMENTAL RESULTS

In this chapter the test results of the MMIC amplifier are presented. Since the amplifier chip must be mounted in a test jig for measurement purposes, a description of this fixture is first given. The performance of the amplifier is then given in the form of S parameter measurements, noise figure, and DC power dissipation. From these results, deviations from the predicted values are explained.

5.1 Test Jig

The primary purpose of a test jig is to allow the miniaturized circuit to be connected to an outside world whose dimensions are more compatible with those of laboratory test equipment. The jig, or mount, must not interfere with the amplifier's operation to any extent greater than has already been accounted for with the use of bond wires and off-chip capacitors. Thus what is needed is a transparent means of feeding in and out the RF signal, and supplying the necessary DC voltages to the chip. This has been accomplished with the test jig shown schematically (without connectors) in Figure 5.1.

A single $2.5 \times 2.5 \text{ cm}^2$ Duroid substrate is used with printed 50-Ohm and bias lines leading to its centre, where the chip is placed. Along the middle of the substrate a 1.5 mm wide channel, which exposes the underlying ground plane, is made so that the chip and the 10 pF decoupling capacitors may be grounded. The eight DC supplies and sensing points are first brought to the edge of the channel via the printed lines originating at the connectors on either side of the

Figure 5.1. Test jig schematic without connectors.

jig. Bond wires are then used to provide the connections from the substrate to the decoupling capacitors and again from the capacitors to the appropriate pads on the chip. The lengths of this last set of bonds must be minimized as they contribute parasitic inductance to the circuit before reaching RF ground, whereas the lengths of the remaining bonds are without consequence. To account for this fact, the capacitors were placed as closely to the chip as possible but the printed DC lines were terminated approximately 1 mm away from them so as to also avoid coupling to the neighbouring RF line.

The RF line was made 30 mil wide to produce a 50 Ohm characteristic impedance on 10mil thick Duroid ($\epsilon_r = 2.25$). It is attached at each side of the jig to a "Radiall" launcher which provides a microstrip-to-coax (SMA) transition with minimal discontinuity. The ends of the line reaching the chip at the channel edges have the 20 pF coupling capacitors placed on them. The connections from the top side of the capacitors to the RF input and output pads of the chip are then made by means of bond wires. A

photograph of the complete assembly is given in the following section.

Before creating the channel, the jig was tested to ensure that the continuous 50 Ohm line joining the input and output connectors did not alter the RF signal, and that no coupling occurred to the DC bias lines located close by. Figure 5.2 shows the S parameter measurements of the test jig in the straight-through configuration over the complete frequency range of the HP8510 network analyzer.

As one would expect, the reverse and forward transmission or reflection characteristics are identical, i.e. the jig is symmetrical. The S₂₁ curve shows an increasing attenuation with frequency, reaching a maximum of 0.15 dB at 3 GHz. This is due mostly to connector loss, but is of little significance when compared to the expected 20 dB S₂₁ magnitude of the amplifier. Similarly, the input reflection coefficient S₁₁, which has a magnitude of less than -25 dB up to 3 GHz, is not likely to mask the S₁₁ or S₂₂ performance of the amplifier as these quantities are expected to be no less than -15 dB. Thus the test jig can effectively be ignored when analyzing the measured results.

5.2. Amplifier Performance

The measurement apparatus used to characterize the amplifier consists of a HP8510 network analyzer and an array of DC power supplies, voltmeters, and ammeters. The network analyzer is capable of accurately extracting the S parameters of the device over the 45 MHz to 26.5 GHz frequency band, but a narrower range extending from 45 MHz to 5 GHz is sufficient in this case. Standard laboratory voltmeters and ammeters were used to monitor the DC

Figure 5.2. S parameter measurements of the test jig.

behaviour of the circuit. The measurement setup is shown schematically in Figure 5.3, and a photograph of the test jig with the amplifier chip mounted in it is given in Figure 5.4.

Figure 5.3. S parameter measurement and DC monitoring apparatus.

Figure 5.4. Photograph of test jig containing amplifier chip.

Although the simulated responses of the amplifier presented in Ch. 4 are expected to match closely with the measurements, they do not take into account fabrication errors. Each FET parameter (I_{dss} , g_m , etc.) is subject to processing variations during fabrication, and average values appropriate to the delivered chips were supplied by the foundry. Thus, before undertaking the measurements it is necessary to regenerate the predicted response, taking this average data into account as shown in Figure 5.5.

Figure 5.5. Expected S parameter response of the amplifier with process variations taken into account.

Due in large part to greater capacitor values (40% increase in the C_{gd} equivalent circuit parameter) and larger transconductance (10% increase) the S_{21} response exhibits a higher gain, but with a narrower 3 dB bandwidth. Comparing with Figure 4.26, the maximum gain is increased by approximately 1 dB to 22.2 dB while the bandwidth is shrunk to 2.5 GHz from 2.7 GHz. It can be seen that S_{11} and S_{22} are relatively insensitive to the process variations.

A complete DC test of the amplifier revealed that the desired 2.5 V drop between the drain and source of each FET was not obtained in all cases. Specifically, V_{DS} of both the source follower FET and the Casc1 common source FET were found to be 1.4 V and 1.5 V, respectively. All other measureable voltages in the circuit were as expected. Such a substantial difference in these two FETs' bias points will lead to variations in their small signal equivalent circuits, and hence in the overall circuit performance.

The process variation data also indicated a reduction in I_{dss} from 70 mA to 57 mA for the standard 300 μ m FET. This corresponds well with the smaller bias currents measured in the circuit. From Sec. 4.6, the total amplifier current was 11.2 mA giving an expected power dissipation of 83 mW. The currents into each cascode stage and the source follower stage were found to be 2.2 mA and 4.1 mA respectively, giving a total of 8.5 mA for the amplifier and a power dissipation of 63 mW. This is a substantial improvement over the designed value.

Measurements of the S_{21} parameter are shown in Figure 5.6(a), with the simulated S_{21} response of Figure 5.5 redrawn to the same scale in Figure 5.6(b) for comparison. It can be seen that the measured low- and mid-frequency gain is approximately 2 dB lower,

although similar in shape, to the simulated curve. At the higher end of the band, the 3 dB bandwidth of the measured response is only 2.1 GHz as compared to 2.5 GHz in the simulated case. An explanation of these discrepancies is given in the following section.

Referring to Figures 5.7(a) and (b) where the measured and simulated S_{22} parameters are compared in a similar way, the same general agreement is seen to exist. However, two resonant peaks are also present in the measured response. These were found to be related to the the test jig and therefore do not represent an inherent characteristic of the amplifier.

The first peak, occurring at approximately 440 MHz, is due to the parallel resonance of the output stage's decoupling capacitor with the narrow inductive microstrip line feeding in the 7.5 V bias voltage. At this frequency, an open circuit (or some high impedance) is presented to the drain of the source follower FET, not a short circuit to ground as is required for the simulated response. Thus the 10 pF capacitors used for decoupling would have to be increased in size to solve this problem.

The second resonance, smaller in magnitude, takes place in the vicinity of 1.1 GHz. Although its cause was not attributable to any one dominant mechanism, the height of the peak could be varied by placing small pieces of RF absorbing material on the DC bias lines of the jig. Since these lines are spaced closely together, and some RF signal escapes through them, it is suspected that coupling effects give rise to larger unwanted impedances at this frequency than at others.

Figure 5.6. (a) Measured S₂₁ response and (b) simulated S₂₁ response of the amplifier.

Figure 5.7. (a) Measured S_{22} response and (b) simulated S_{22} response of the amplifier.

A similar effect is seen to perturb an otherwise perfect agreement between the measured and simulated S_{11} response, shown in Figures 5.8(a) and (b) respectively. This time the resonance (at 460 MHz) is due to the insufficient size of the decoupling capacitor for the input FET's gate bias supply.

Various other measurements were performed for which graphical data is not available. The 7.5 V voltage supplies were reduced to 5 V, resulting in only a 2.5 dB drop in gain with improved gain flatness, while the bandwidth decreased to 1.9 GHz. Thus the DC power consumption can be reduced by a third with a small loss in gain. The 1 dB compression point and saturated output power were measured as 3 dBm and 5 dBm respectively.

Finally, the amplifier's noise figure was measured using the same setup as in Figure 5.3 with the network analyzer replaced by the HP8970A noise figure meter. In order not to include the noise associated with the 150 Ω input matching resistor, the bias to the input FET's gate was supplied directly on the RF line with a bias tee. Thus, the input resistor is effectively removed from the amplifier. At 0.8, 1, and 1.5 GHz, the noise figure was 7.4 dB, 7.8 dB, and 7.5 dB respectively. This represents a 2 dB poorer performance than that calculated in Ch. 4, and will be explained in the next section.

Figure 5.8. (a) Measured S_{11} response and (b) simulated S_{11} response of the amplifier.

5.3. Discussion of Measured Results

In the previous section the measured results were compared with simulations that did not properly reflect the actual circuit bias conditions, as it was found that two FETs were operating near or at $V_{DS} = 1.5$ V. It is therefore preferable to correct the simulated curves for the known change in bias, and explain any discrepancies with the measurements on the basis of these new responses.

Additional FET models for $V_{DS} = 1.5$ V from TriQuint were used to produce the corrected S_{21} response shown in Figure 5.9. The R_{ds} parameter changes by more than 50 % compared to the $V_{DS} = 2.5$ V condition used earlier, and is responsible for the large change observed in the resimulated curve. The bandwidth is now reduced to 2.2 GHz, within 5 % of the 2.1 GHz measured result, and the midband gain is reduced to 20 dB, which is also much closer to the measured 19 dB. Thus, with the actual FET biases taken into account, the performance of the amplifier can be predicted quite accurately and in fact almost perfectly if g_m of the input FET (biased at 5 % I_{dss} , for which the equivalent circuit was estimated through extrapolation) is also reduced by 10%.

The question that must be addressed is why the DC biasing does not conform with the designed conditions. The amplifier was provided with ample bias control through the use of separate voltage supplies for each stage, and for each gate of FETs requiring a non-zero V_{gs} . Yet no amount of adjustment in these voltages could rectify the problem, which is contrary to a DC SPICE analysis (not included) that showed the correct values to exist for a proper combination of V_{g1} and V_{g2} (Fig. 4.24).

Figure 5.9. Simulated S_{21} response with bias variation included.

A closer look at the individual currents flowing through each branch, denoted I_1 to I_3 in Figure 5.10, leads to a possible explanation of the DC behaviour. As was mentioned earlier, I_1 and I_2 were measured to be 2.2 mA, while I_3 was 4.1 mA. Since these values are dictated by the current sources in each of the three branches, one expects

$$I_1 = I_2 = 2.2 \text{ mA}$$

which was verified.

Also, due to the current source in the third branch being twice as large as the other two, one expects

$$I_3 = 2I_2 = 4.4 \text{ mA}$$

However, the measured I_3 falls short of this value by 0.3 mA. I_2 and I_3 combine at the common source (36 μm) FET in the Casc1 stage. From scaling of the 300 μm FET I-V curves, it can be shown that the 36 μm FET at $V_{gs} = 0$ bias requires a drain current of 6.6 mA for V_{ds} to be 2.5 V, and a current of 6.4 mA for $V_{ds} = 1.5$ V. Since in the measured circuit this FET is only receiving a current of $I_2 + I_3 = 6.3$ mA, operation at $V_{ds} \approx 1.5$ V results.

Figure 5.10. Circuit diagram of amplifier showing DC bias values.

Thus the problem is further reduced to demonstrating why I_3 is less than it should be. There appears to be no other phenomenon than

backgating which can explain this situation. To recall, backgating refers to voltages elsewhere in the circuit affecting the channel depth, and hence the current, of a given FET. It is often difficult to provide definite proof that this is occurring in a MMIC circuit, but it is known that the TriQuint 3A process is prone to backgating in closely-spaced FET circuits [35]. In this amplifier, it is suspected that the 24 μm current source FET is submitted to a slight unwanted negative V_{gs} voltage, which causes the lower than expected current.

In the case of noise performance, the 2 dB difference between measurements and calculations is more easily explained. In Sec. 4.5.2, the calculated first stage noise figure of 5.7 dB was taken as an estimate for the complete amplifier's noise figure. This estimate was overly optimistic for two reasons. First, the 20% I_{dss} noise data was used for the input FET biased at 5% I_{dss} since no closer values were available. From section 4.2.2, an approximate 1 dB penalty in the single FET's noise figure results from such a reduction in current. This increases the FET's equivalent input noise voltage to a larger value than was used in the calculations.

Second, the first stage noise figure is only a good prediction of the overall noise figure when the gain of this stage is large, a condition which is not met in this amplifier. In chapter 4, it was seen that the first stage gain is less than 7 dB at 1 GHz, which is low enough to allow substantial contributions to be made to the total noise power from the second stage noise. This was confirmed by a simple recalculation of the noise figure, in which the second stage noise contribution was assumed to be limited to that of its input FET (an underestimation). A new value of 6.8 dB was obtained, which is already within 1 dB of the measured result.

5.4 Comparison with Other Amplifiers

In Table 5.1 are listed a number of GaAs MMIC amplifiers reported in the literature since 1982, along with their main performance characteristics, for comparison with the the results of this work. To the author's knowledge, references [21,23,30,31,34] are the only attempts to achieve low DC power dissipation.

Table 5.1. Performance of Reported GaAs MMIC Amplifiers

Reference	Gain (dB)	Bandwidth (GHz)	DC Power (mW)	Area (mm ²)	Inductors	Matched input	Noise Figure Output (dB)

This work	19	0.2-2.1	63	0.2	no	no	yes 7
[33]	26	0 - 3.2	750	0.42	no	yes	yes 7
[20]	20	0.3-1.5	1000	?	no	no	yes 2
[21]	23	0.2-2.0	170	0.63	no	yes	yes 2
[36]	15	0.1-4.0	>500	?	no	yes	yes ?
[30]	16	0.01-2.0	180	?	no	no	yes 3
[23]	15	0.1-2.0	120	0.55	no	yes	yes ?
[34]	12	0.1-1.8	96	0.49	yes	yes	yes 3
[13]	22	0 - 2.7	960	0.96	yes	yes	no 6
[31]	17	0.01-3.9	170	0.96	yes	yes	yes 3
[14]	19	0.8-1.8	405	?	yes	yes	yes 3

It is seen that the amplifier developed in this thesis has the largest Gain-Bandwidth to DC power ratio of all entries. Among the low power designs, it provides the broadest bandwidth without the use of inductors. The chip size is also the smallest known to be reported. However, as amplifier design involves tradeoffs between several factors, the performance parameter which tends to offset these benefits is the noise figure, which is seen to be the highest of all amplifiers.

CHAPTER 6. CONCLUSIONS AND RECOMMENDATIONS

On the basis of the amplifier results obtained in the previous chapter, several conclusions pertaining to the various aspects of this thesis may be drawn.

The design techniques of Chapter 3, consisting of the use of transfer functions developed from simplified FET models, were validated. In conjunction with SuperCompact, they provided valuable insight into the behaviour of the low power amplifier, and allowed accurate predictions to be made. Also, the noise representation method described in Chapter 3 was confirmed. Thus, a complete method for designing UHF and L band amplifiers has been proposed and verified.

From Chapter 4, it was found that a low power dissipating amplifier is achievable through the use of small FETs, active loads, FETs biased at 5% I_{DSS} , capacitive coupling of stages, and the drain current saving technique. The cascode gain block was found to be more efficient than the common source configuration, and the source follower proved to be the most efficient output matching structure. Finally, the bandwidth of a double cascode gain stage (two cascodes in series) was found to be broadened with the use of resistive feedback around the second cascode.

In Chapter 5, a low power amplifier providing 18 to 20 dB of gain and covering the UHF and L bands was successfully demonstrated. Thus, a major objective of this thesis was accomplished. The experimental results were found to be in good agreement with the simulations, except for a DC biasing problem which was attributed to backgating. In addition, the DC bias lines on the test jig were

seen to affect the low frequency response as a result of the insufficient size of the decoupling capacitors. The amplifier's noise figure was 2 dB poorer than expected due to inadequate modelling of the noise contribution from the second stage. From the generally good agreement of the experimental results, the FET equivalent models for the TriQuint 3A process were verified and found to be sufficiently accurate.

Without further work, the amplifier would be better suited to general-purpose IF applications where a low noise figure is not critically important. The following recommendations to improve the noise performance and other aspects of the amplifier are made.

Larger FETs should be used throughout the amplifier's gain stages since their equivalent input noise voltages are inherently lower. This was done for the input FET without increasing the drain current, and could be extended to the other FETs with appropriate gate biasing.

Implementation of the above would require the individual FETs to be biased at negative gate-to-source voltages without the need for external supplies, as these would become too numerous. Thus techniques should be investigated to self-bias FETs accurately and with minimal added DC power dissipation. This would also be of benefit to the present amplifier where two gate voltages must be applied externally.

The TriQuint QED process offers FETs with equivalent gain to those in the 3A process for lower DC power consumption, and should therefore be used to further reduce the amplifier's power requirements. Also, FETs should be characterized at very low V_{ds}

voltages (below 1 Volt) to allow greater flexibility in designing low power circuits with their equivalent models.

To eliminate the low frequency resonances caused by the test jig, larger decoupling capacitors should be used. A twentyfold increase of their values to 200 pF would ensure that a RF short circuit to ground is provided above 0.2 GHz. Finally, further investigations should be carried out on the amplifier to identify whether backgating was the only cause of the incorrect DC biasing, and to properly establish under what conditions it occurs.

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