

A Phase-scaled Vernier Time-to-Digital Converter Architecture with Switchable Coarse/Fine Resolutions, Wide Range and Ultra Low Power Consumption

by

Tuoxin (Tony) Wang

A thesis submitted to the Faculty of Graduate and Postdoctoral Affairs in partial fulfillment of the requirements for the degree of

Master of Applied Science

in

Electrical and Computer Engineering

Ottawa-Carleton Institute for Electrical and Computer Engineering
Carleton University
Ottawa, Ontario

© 2016, Tuoxin (Tony) Wang

Abstract

A novel phase-scaled Vernier time-to-digital converter (TDC) architecture with a switchable coarse/fine (16ps/2ps) time resolution function is presented to achieve large phase (time) detection range (32.7ns in 14 bits), fine time resolution (2ps), compact size and super low power consumption simultaneously. The phase noise (caused by the TDC) can also be improved due to it allowing a higher reference frequency compared to other types of TDC architectures. A phase-regulator has been created and embedded into traditional Vernier TDC core circuitry for the purpose of separating a new-defined mandatory fine-granularity phase length (normal-length phase) (80ps) from the random phase (time) difference (up to 32ns) to be measured. The mandatory phase length will be the only part to use a fine-resolution (2ps) measurement and the rest of the phase length will be counted in large intervals (80ps). By doing so, the required number of stages of the traditional Vernier TDC core can be remarkably reduced from 6250 to 40 at a fixed 2ps time resolution. Furthermore, compared to a typical Vernier ring TDC, the proposed architecture being combined with a reverse-triggered pre-logic unit and the coordinated-determination scheme facilitates a much simpler and faster determination procedure, which allows the power consumption to be greatly reduced and the reference frequency to be increased in order to achieve a 2~3dB improvement of the phase noise performance.

Acknowledgements

I would like to thank Microsemi Inc. Kanata site as well as the people in PLL department from the United States for their generous support of my research. Microsemi has been providing all of the design tools I needed and the people in the group also provided the specifications of the requirement, valuable suggestions and the feedback on my research progress in the past year. In particular, I want to thank Krste Mitric and Kobe Situ for their constant support of my work. Krste Mitric was the one who launched this partnership of the collaborated research and has been playing as a pilot to drive the project moving forward. He even spent a big proportion of his vacation time on reading and understanding the progress report and the corresponding literature, providing valuable enquiry, suggestion and comment those make the research work more comprehensive and clear. He also pointed out the flaws in the research and the places in the literature which may confuse readers. Kobe helped a lot in technic support in terms of setting up and maintaining the simulation environments like, Linux server, Matlab and Simulink, Virtuoso etc. I would have been spent ten times of my time on the working environments if I had no Kobe's work. I also pleased to acknowledge Peter who ever helped to retrieve a Cadence Library Crash, avoiding a disaster to me.

This work would not have been possible without the support of my supervisor John Rogers. In addition to coordinating our partnership with Microsemi, he provided essential oversight and support for me, inside and outside of the context of my thesis and publications. Furthermore, he encouraged me when I got stuck somewhere and sharing his experience, ideas with positive view. His support has been solid and powerful to drive this research going forward.

I am very grateful to having every one of my family, who brings deep happiness and a feeling of satisfaction to me.

Table of Contents

Abstract	i
Acknowledgements	ii
Table of Contents	iv
List of Tables	vii
List of Figures	viii
Chapter 1: Introduction	1
1.1 All Digital Phase Locked Loop	1
1.2 Time-to-Digital Converter	2
1.3 TDC Key Performances summary	4
1.4 TDC detection range expression.....	5
1.5 Thesis Outline.....	5
Chapter 2: Background	7
2.1 Inverter Based TDC (Traditional)	7
2.2 Ring Oscillator TDC.....	9
2.3 Vernier TDC.....	10
2.4 Vernier Ring TDC	11
2.5 Phase-scaled Vernier TDC	13
Chapter 3: System Level Design and Implementations	14
3.1 Architecture Illustration of Phase-Scaled Vernier TDC.....	14
3.2 System Level Design Considerations	15
3.3 System Specification Assumption	19
3.4 Phase Regulator & TDC Core	20
3.5 Coarse/Fine Configuration & Optimization	24
3.6 Evaluator.....	28

3.7	Pre-logic Circuit with Reversed-Trigger Solution.....	31
Chapter 4: TDC Timing Considerations for Higher Reference Frequency 37		
4.1	General Operating-Time Procedure.....	38
4.2	Operating-Period Performance Comparison.....	39
Chapter 5: Circuit Implementation and Simulation..... 44		
5.1	Technology Process and Basic model parameters.....	44
5.2	Vernier TDC Core Circuit.....	46
5.2.1	Slow path inverter delay chain.....	46
5.2.2	D Flip Flops.....	49
5.3	Differential RRD and Trigger Clock.....	51
5.4	Encoding Circuit.....	52
5.5	Phase Regulator and Simulation.....	54
5.6	TDC Core Circuit Simulation Results and Optimization.....	58
5.7	Evaluator Implementation and Simulation.....	62
5.7.1	Coordinated-Determination Device.....	62
5.7.2	Even-rotation Compensation and optimization.....	63
5.8	The Whole TDC Architecture and Simulation.....	68
Chapter 6: ADPLL System Calculation and Simulation..... 71		
6.1	ADPLL System Specifications.....	71
6.2	Phase Noise Contribution and Distribution.....	73
6.3	ADPLL System Modeling and Simulation in Simulink.....	77
6.4	Comparison between different Loop types and parameters.....	79
6.5	Preferred Solution of ADPLL System Operation.....	81
Chapter 7: Conclusion and Future Work 83		
7.1	Completed Work.....	83

7.2	Future Work.....	83
7.3	Contributions and Conclusions.....	84
	References	85

List of Tables

Table1: Feature of different types of TDCs	12
Table2: Specifications of the TDC	19
Table 3: Performance Analysis at a Fixed 25MHz Reference Frequency (40ns period) .	23
Table 4: Improvement of the Phase Noise Performance with Different Accepted Reference Frequency (1GHz of DCO output)	42
Table 5: Comparison of Several TDC Architectures	43
Table 6: D Flip Flop initial parameters configuration.	50
Table 7: Sections, Outputs and Coding Result Index	59
Table 8: Examples of Final output calculation	64
Table 9: Truth table of updated even rotation word for alignment.....	67
Table 10: Type I and type II loop feature contrast.....	80
Table 11: Type I and type II loop feature contrast.....	82

List of Figures

Fig. 1 ADPLL system level operation diagram	2
Fig. 2 Illustration of integer and fractional counting [2]	2
Fig. 3 Noise Contributions of TDC and DCO in an ADPLL.....	3
Fig. 4 Inverter Based TDC (Traditional)	7
Fig. 5 Operating Principle of a Traditional TDC	8
Fig. 6 Ring Oscillator TDC Structure.....	9
Fig. 7 Vernier TDC Structure	10
Fig. 8 Vernier Ring TDC Structure.....	11
Fig. 9 Simplest Illustration of the Phase-scaled Vernier TDC Structure.....	14
Fig. 10 TDC module diagram.....	15
Fig. 11 Phase regulator illustration in time domain.....	16
Fig. 12 Block diagram of Phase-scaled Vernier TDC (Phase regulator and TDC core) ..	20
Fig. 13. A modified version of the phase-scaled Vernier TDC.	22
Fig. 14. Degree of activities of the VRTDC and Phase-scaled Vernier TDC.	25
Fig. 15. (a) Logical modification for rising-edge only phase counter, (b) True table of (a) circuitry.	27
Fig. 16. (a) Evaluator and Coordinated-Determination Device, (b) and their operations in time domain.	31
Fig. 17. Waveform illustration of reversed-triggered pre-logic unit.	32
Fig. 18 (a) Reverse-triggered pre-logic unit block, (b) Arbiter unit block, (c) D Flip-Flop block, (d) D Flip-Flop transistor level block	33
Fig. 19 The Proposed ADPLL system operation diagram	35

Fig. 20 ADPLL timing and computation example (FCW=3.25).....	36
Fig. 21 Operating-period Performance Comparison Between (a) VRTDC and (b) Phase-Scaled Vernier TDC.....	39
Fig. 22. Propagation delay of inverters with various W_p/W_N ratios and C_{load}	45
Fig. 23 Static Inverter's DC Transfer simulation.....	46
Fig. 24 Slow path inverter delay chain circuit schematic and associated system level diagram.	48
Fig. 25. NAND Optimization for equal length of odd and even rotations.....	49
Fig 26. (a) A D Flip Flop circuit and (b) illustration of non-ideal issue. [10].....	50
Fig. 27. Differential RRD and differential fast path clock trigger.....	52
Fig. 28. (a) 8/3 priority encoding circuit and (b) it's truth table.....	53
Fig. 29. Circuit diagram of an edge finder consisting of XOR Gates.	54
Fig. 30. Vernier core circuit and phase regulator.....	55
Fig. 31. Diagram of the TDC core and coding output.	56
Fig. 32. Ideal Simulation Conditions with REF and Phase Regulator Output.....	57
Fig. 33. Real simulation conditions with REF and phase regulator output.	58
Fig. 34 Vernier core output.....	59
Fig. 35. Vernier Core Output in First Rotation of the Phase Regulator.....	61
Fig. 36. 8-bit 5-1multiplexer and corresponding determination diagram.	63
Fig. 37. (a)5-1multiplexer and corresponding determination diagram (b) logic of fi.....	63
Fig. 38. Simulation of Final Output of the TDC and alignment issue A	66
Fig. 39. Simulation of Final Output of the TDC and alignment issue B	66

Fig. 40. Logic implementation of alignment between even rotation word and core output.	68
Fig. 41. TDC system block diagram.	69
Fig. 42. Final Simulation of Final Output of the TDC.....	70
Fig. 43. ADPLL System Specifications from Microsemi.....	71
Fig. 44. Original Phase noise & RMS jitter conversion of the ADPLL	72
Fig. 45. Updated Phase noise & RMS jitter conversion of the ADPLL	73
Fig. 46. ADPLL phase noise contribution and distribution.	74
Fig. 47. ADPLL phase noise calculator and analyzer.....	77
Fig. 48. Basic integer PLL system simulation platform.	77
Fig. 49. ADPLL control voltage convergence with the time.	78
Fig. 50. Diagram of a fractional digital type I PLL system.	79
Fig. 51. Diagram of a fractional digital type II PLL system.	79
Fig. 52. ADPLL phase noise comparison between different loop parameters.	80
Fig. 54. ADPLL operation with combination of type I and type II. [1].....	82

Chapter 1: Introduction

1.1 All Digital Phase Locked Loop

An all-digital phase locked loop (ADPLL) is a PLL where all components are implemented with digital signals present at their inputs and outputs. Even the low-pass filter located between the phase (frequency) detector and the digitally-controlled oscillator (DCO) (which traditionally would have been an analog voltage-controlled oscillator) is completely digital. An ADPLL has the potential advantage of size and cost reduction which will scale with process technology (say from 90nm to 45 nm) compared to its analog counterpart, which includes an analog filter implemented by passive capacitors and resistors, not being able to shrink in size at smaller geometries or be fully integrated on chip [1] [2] [3].

Commonly, an ADPLL consists of a phase comparator, a type-I or type-II digital low-pass filter, a DCO and a time-to-digital converter (TDC), as shown in Fig. 1. FCW stands for Frequency-Command-Word indicating the desired number of DCO periods in one reference period. An integral counter is used to count the real integer part of how many DCO periods in the current reference period (or system timing period). The TDC is created to measure the fractional part of DCO period (ε), as shown in Fig. 2. When the loop has settled, ideally the PLL system will make the sum of the comparator zero, which means:

$$\sum FCW = i + \varepsilon \quad \text{Eq.(1)}$$

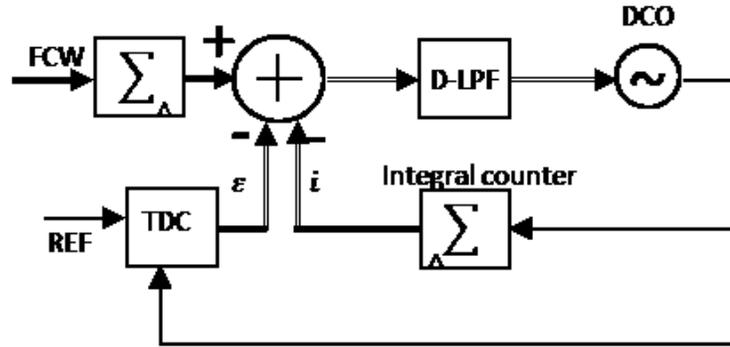


Fig. 1. ADPLL system level operation diagram.

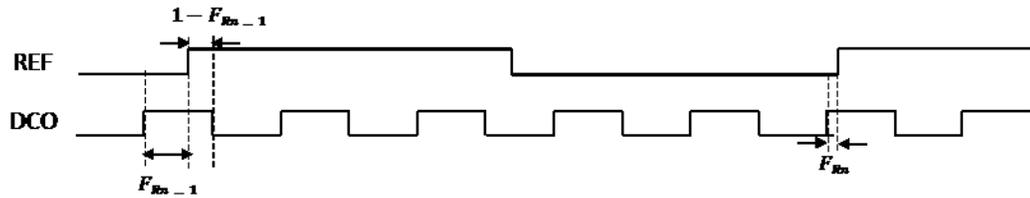


Fig. 2. Illustration of integer and fractional counting. [5]

1.2 Time-to-Digital Converter

To realize an ADPLL, a high performance time-to-digital converter (TDC) is crucial due to TDC mostly dominating the in band phase noise of the system (Fig. 3). A TDC can measure and quantize the phase (time) difference (ΔT_{Tot}) between the reference clock and the DCO clock (feedback of the ADPLL), which corresponds to F_{R_n} shown in Fig. 2. The digital output of the TDC allows for an accurate arithmetic operation in the comparator (Fig. 1), avoiding the issue of noise injection compared to an analog PLL's charge pump.

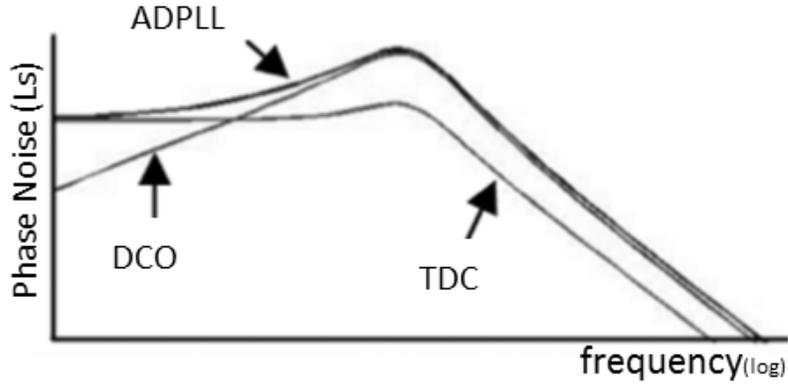


Fig. 3 Noise Contributions of TDC and DCO in an ADPLL

The time resolution of the TDC (T_{res}) is one of the most important TDC performance metrics, indicating the accuracy of resolving the timing difference of the reference (REF) and DCO edges. Therefore with a linear conversion, the RMS phase error ϕ_{error} will be:

$$\phi_{error} = 2\pi \cdot \frac{T_{res}/\sqrt{12}}{T_{DCO}} \quad \text{Eq.(2)}$$

where T_{DCO} is the period of the DCO output [5]. This noise will be spread from dc to the sampling frequency (REF frequency, f_{ref}). Thus the in-band phase noise of the TDC is:

$$L_{\{\Delta f\}} = 10 \log_{10} \left[\frac{(2\pi)^2}{12} \cdot \left(\frac{T_{res}}{T_{DCO}} \right)^2 \cdot \frac{1}{f_{ref}} \right] \quad \text{Eq.(3)}$$

In order to reduce the phase noise caused by a TDC, a finer time resolution is needed [4]. In addition to being able to achieve a competitive phase-noise performance, the synthesizer (ADPLL) still needs to produce a wide frequency range of DCO outputs [5] especially for demanding wireless applications. Considering the requirements of state-of-the-art ADPLL

applications in the wireless field (television broadcast, mobile phones, wireless LAN, Bluetooth, ZigBee, GPS, microwave devices/communications, etc.), the novel integrated ADPLL design considered should cover the frequency range from sub-100MHz to 20GHz (or even broader), which requires a wide phase detection range of tens-ns. This means that the TDC phase detection range needs to be able to cover the period of the lowest frequency of the DCO. Therefore, a fine TDC time resolution combined with a wide phase detection range ($\Delta T_{\text{Tot_max}}$) are the most important performance specifications in most wireless applications.

Note from Eq.(3), a higher reference frequency would improve the in-band phase noise performance of the ADPLL (decreasing the phase noise value). Thus, a TDC solution that allows a higher reference frequency is desired. This topic and research will be discussed in Chapter 4.

Low power consumption and small chip area are always the key performance specifications in order to achieve a relatively low cost solution and production.

1.3 TDC Key Performances Specifications Summary

The followings are the TDC key performance specifications to be considered in highest priority of the research:

- Time resolution, T_{res} (2ps).
- Phase (time) detection range, $\Delta T_{\text{Tot_max}}$ (12.5ns).
- Highest available reference frequency, 100~200MHz.
- Low power consumption, compared to current art.
- Small chip area, compared to current art.

1.4 TDC detection range expression

The other way to digitally express the phase (time) detection range of a TDC is by how many output bits it produces, X . The relationship between X and ΔT_{Tot_max} is:

$$\Delta T_{Tot_max} = T_{res} \cdot (2^X - 1) \quad \text{Eq.(4)}$$

For instance, a 10 bit TDC with 2ps resolution is able to detect 2ns of the phase (time) detection range, while a 14 bit one can cover more than 32ns. Eq.(4) implies that in the case of a fixed number of digital bits, the phase detection range gets narrower with the finer TDC time resolution, which means that a TDC design must trade-off time resolution for phase detection range, or vice versa.

1.5 Thesis Outline

Chapter 2 will discuss the background literature of the research and illustrate the progress of TDCs addressing the time resolution issue and phase (time) detection range. The advantages and disadvantages of TDCs will be discussed as well. Chapter 3 will introduce the Phase-scaled Vernier TDC architecture and describe the system level design including the system specifications provided and the circuit level specifications required for successful operation. A couple of advanced options of the TDC implementations will be provided for various purposes. In Chapter 4 we will discuss TDC timing considerations in order to achieve best phase noise performance by allowing a higher reference clock in the ADPLL system. Chapter 5 provides the circuit level implementation of the TDC core, phase regulator and the surrounding blocks of the TDC system. The simulation results and corresponding optimization for optimal performance

will also be performed in this chapter. Chapter 6 provides ADPLL system implementation for simulation and evaluation of TDC performance. All the work will be done in both Matlab and Cadence platforms. Chapter 7 will conclude the thesis. Also the future work on the topic to verify the research in physical level will be briefly discussed.

Chapter 2: Background

2.1 Inverter Based TDC (Traditional)

To date a number of types of TDCs have been studied, such as the basic inverter-based TDC (traditional TDC), the ring oscillator TDC, the Vernier TDC and the Vernier ring TDC.

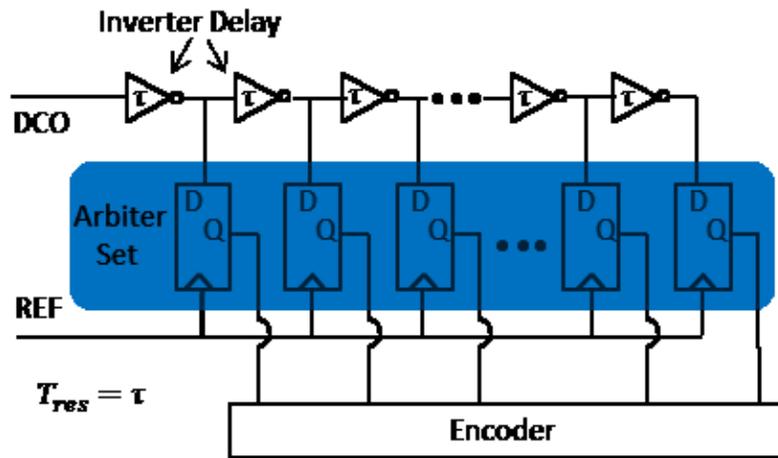


Fig. 4 Inverter Based TDC (Traditional)

The traditional TDC (Fig. 4) has a simple structure, which only consists of an N-stage delay chain and N D flip-flops (as an arbitrator set/array) [6]. In this type of TDC, the DCO signal propagates through the delay chain with the time delay (τ) for each stage of inverters. As shown in Fig. 5, a duplicated delayed version of the DCO edge is produced at the output of each inverter stage. The delay at each output is proportional to the number of inverters between the DCO input and the corresponding node. Once the reference (REF) edge arrives, the values of those nodes (data terminals of the arbiters) at that moment are stored as $Q\langle 0:N \rangle$. The location (k) where the values of $Q\langle 0:N \rangle$ transits, quantitatively determines the phase difference (ΔT_{Tot}) between the edge of the DCO and of the REF by:

$$\Delta T_{Tot} = k \cdot \tau, \quad k = 1, 2, \dots, N \quad \text{Eq.(5)}$$

where N is the number of stages of the TDC. Note that the the phase detection range (ΔT_{Tot_max}) is determined by:

$$\Delta T_{Tot_max} = N \cdot T_{res} = N \cdot \tau \quad \text{Eq.(6)}$$

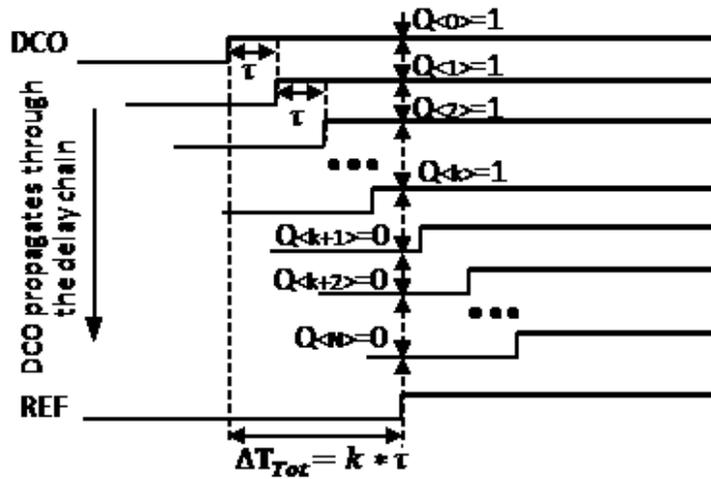


Fig. 5 Operating Principle of a Traditional TDC

Obviously, the phase detection range (ΔT_{Tot_max}) increases with the propagation delay (τ) of each inverter and the number of stages (N). As mentioned, τ also limits the TDC time resolution performance, thus increasing N is mostly the only way to meet a larger phase detection range in the case of a fixed T_{res} . For instance, to detect a 1GHz DCO ($\Delta T_{Tot_max}=1000\text{ps}$) with 10ps of T_{res} , 100 stages of a delay chain are needed. Similarly, to detect an 80MHz DCO ($\Delta T_{Tot_max}=12.5\text{ns}$), the required number of stages (N) should be 1250. The lower the frequency of the signal produced by the DCO, the more stages are required of a

delay chain at a constant inverter-delay (τ). Obviously, large N leads to large chip area and high power consumption, resulting in a less competitive or even impractical TDC solution.

2.2 Ring Oscillator TDC

To avoid a very large N, the ring oscillator TDC was developed (Fig. 6). It reuses a small odd-number of delay stages to achieve a wide phase detection range. It breaks the relationship of Eq.(6) and provides a classic solution for a large phase detection range requirement [7].

However, T_{res} is still equal to τ which should be from 10ps to 100ps in a 65nm process, making the traditional TDC or ring oscillator TDC still limited in time resolution performance for the most demanding wireless applications. A multipath gated ring oscillator (GRO) structure was still a valuable field of the research to improve the TDC performance [8].

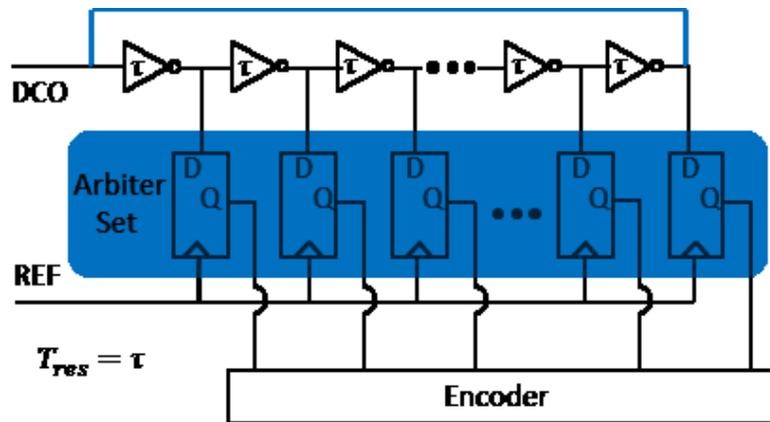


Fig. 6 Ring Oscillator TDC Structure

2.3 Vernier TDC

One way to improve the time resolution performance is to use a Vernier type TDC [9], as shown in Fig. 7, where the time resolution is equal to:

$$T_{res} = \Delta\tau = \tau_2 - \tau_1 \quad \text{Eq.(7)}$$

where τ_1 and τ_2 are the time propagations of the inverters for the slow delay chain and the fast delay chain, which are driven by the DCO and the REF respectively. Theoretically, $\Delta\tau$ could be reduced to almost zero and practically Vernier TDCs with T_{res} as low as a few ps have been implemented and verified such as [10].

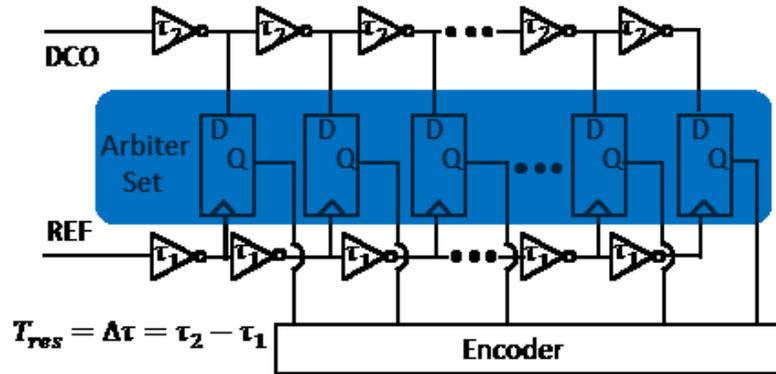


Fig. 7 Vernier TDC Structure

However, the Vernier type TDC improves the time resolution at the expense of the phase detection range or area cost due to the huge number of stages needed in the delay chains. For example, aiming for T_{res} of 2ps and ΔT_{Tot_max} of 12.5ns, a Vernier TDC will require 6250 stages. The Vernier TDC has a resolution 5 times better than that of the traditional TDC at expense of 5 times the number of stages, which will cause an even worse area & power

performance compared to the traditional TDC. In addition, it will take an extremely long time period ($\tau_1 \cdot N$) to guarantee all arbiters' values ($Q < 0:N >$) can be captured and stored correctly for determination. In the case of $\tau_1 = 35ps$, the capture period could be as long as $35 \cdot 6250 = 218.75ns$ which is impractical as well.

2.4 Vernier Ring TDC

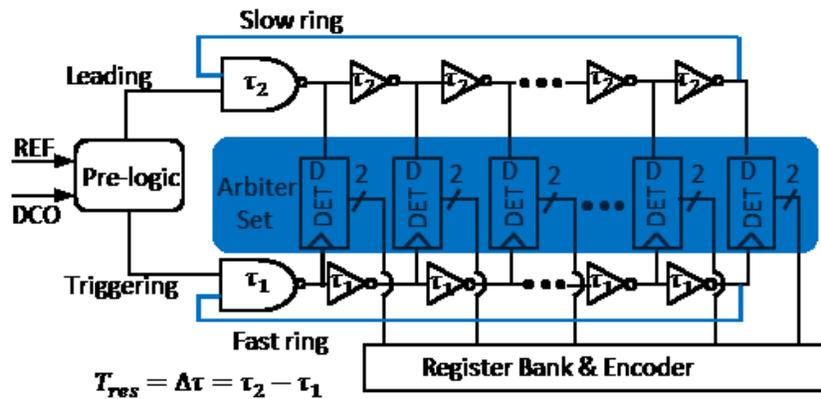


Fig. 8 Vernier Ring TDC Structure

By employing similar ring structures of the ring oscillator TDC into a Vernier TDC, an advanced type of TDC called the Vernier Ring TDC (VRTDC) was developed aiming at both a fine time resolution performance and a wide phase detection range, [11], [12]. The principle of the VRTDC (Fig. 8) is to connect the output end terminal to the input terminal of each Vernier delay chain which has only a finite small number of stages. The leading signal and the triggering signal run laps (rotations) along their own delay chains until the judgment of the arbiters shows that the triggering signal has caught up with the leading signal. The reuse of the delay chains in the VRTDC greatly reduces the number of delay stages, facilitating area and power cost reduction. Two counting units need to be introduced to record how many times the triggering

signal and the leading signal traverse the entire loop before the triggering signal catches up with the leading signal. The ring structure in the VRTDC requires a couple of extra demanding logic operations, which include negative pulse generation of the reference clock and the DCO clock, pre-logic operations (identifying and routing separately two inputs for the fast-ring and the slow-ring), double-scaled arbiter-sets for odd-rotation and even-rotation [13] and [14], and a registration bank with fast reading and decision logical operations. The VRTDC works correctly only if the above comprehensive considerations and corresponding complex logical operations can be performed with very high precision. However, a phase error due to finite width of the negative pulse degrades the performance of the TDC occasionally. On the whole, a VRTDC is one of the most effective and efficient TDC solutions, possessing fine time resolution performance, wide phase detection range and compact size due to a small number of delay stages. On the other hand, a VRTDC also requires a large amount of high speed circuitry due to its principle of two rings structure and usage of the multi-capturing & multi-updating or the large register bank. Table1 summaries the performances contrast among the variety of TDC solutions.

Table1: Feature of different types of TDCs

	Time Resolution $T_{res} = \Delta\tau$	Phase Detection Range $\Delta T_{Tot,max}$	Stages of Delay chains N
Traditional TDC	Coarse	Narrow	Large
Ring-Oscillator TDC	Coarse	Wide	Small
Vernier TDC	Fine	Narrow	Super Large

Vernier Ring TDC (VRTDC)	Fine	Wide	Small
Phase-scaled Vernier TDC	Fine	Wide	Small

2.5 Phase-scaled Vernier TDC

The purpose of this paper is to present a new TDC architecture which parallels the VRTDC counterpart in aspects of addressing the common limitation of the confliction between fine time resolution and wide phase detection range. Meanwhile, it avoids potential phase error and complicated logic determination in the VRTDC. Furthermore, its advantage of improved inverter-reverse frequency facilitates even less power consumption and a higher possible REF frequency for a better phase noise performance of the TDC, compared to the VRTDC.

Chapter 3: System Level Design and Implementations

3.1 Architecture Illustration of Phase-Scaled Vernier TDC

As shown in Fig. 9, the simplest topology of the phase-scaled Vernier TDC can be created by employing a partial-ring connection in a slow delay chain, such that the Vernier TDC core can be restarted periodically when the signal carried on the ring reverses. By being combined with this partial-ring structure (phase regulator) into a Vernier TDC, no matter how long the phase difference ΔT_{Tot} is, it will be scaled into a remarkably shorter length, T_R (say <80ps), called the new defined mandatory fine-granularity phase length which will be the only part being measured with a very fine time resolution. While the rest of the phase ($\Delta T_{Tot} - T_R$) is not necessary for a tiny-granularity measurement and can be measured in large granularity (80ps). Based on this scheme, a 2ps 14 bits (32ns) TDC with only 40 stages will be implemented, maintaining compact area, low power consumption and tolerating higher possible reference frequency.

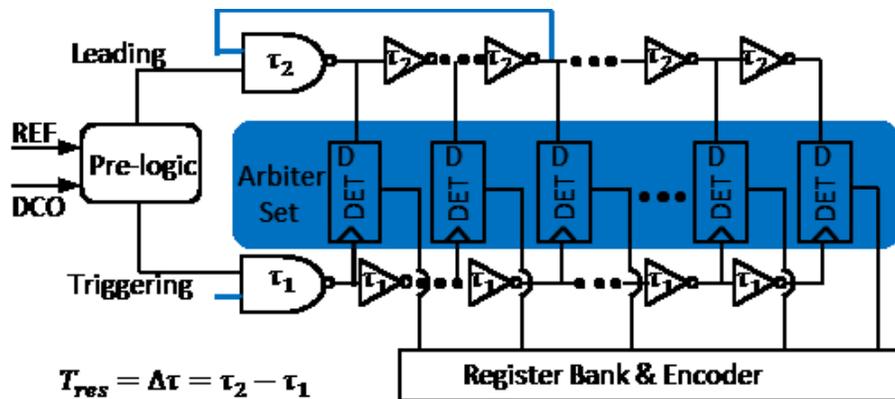


Fig. 9 Simplest Illustration of the Phase-scaled Vernier TDC Structure.

3.2 System Level Design Considerations

Usually, a TDC module is comprised of a TDC core section and a couple of peripheral sections for logical operations, decisions and calculations. As shown in Fig. 10, the proposed TDC architecture consists of a phase regulator, a fine resolution Vernier TDC core, a normal-phase counter, a pre-logic unit and an evaluator.

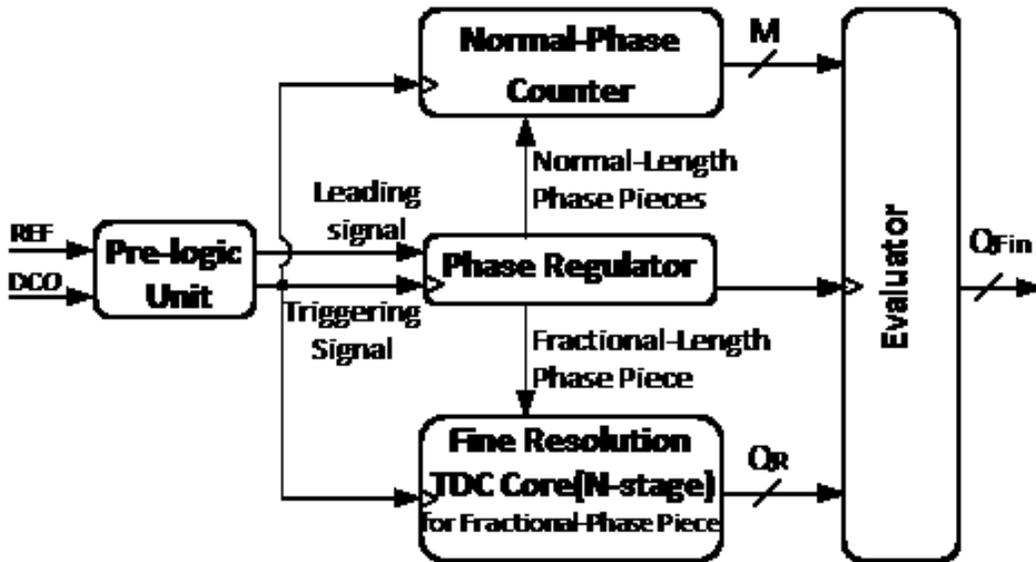


Fig. 10 TDC module diagram

The reference clock and DCO clock are processed by the pre-logic unit and then are fed into the phase regulator as the leading signal and triggering signal. The purpose of the phase regulator is to measure and cut the phase difference (ΔT_{Tot}) (between the rising edge of the leading signal and the rising edge of the triggering signal) into pieces (as shown in Fig. 11). Except for the last piece (T_R), all the time pieces will have an identical normal-length (T_{Nor}) which should be set less than 100ps in order to take the most advantage in reducing the stage

number of the delay chains. Now the phase difference (ΔT_{Tot}) is supposed to be broken into 2 parts, the last piece (T_R) and the rest of the phase ($\Delta T_{Tot} - T_R$).

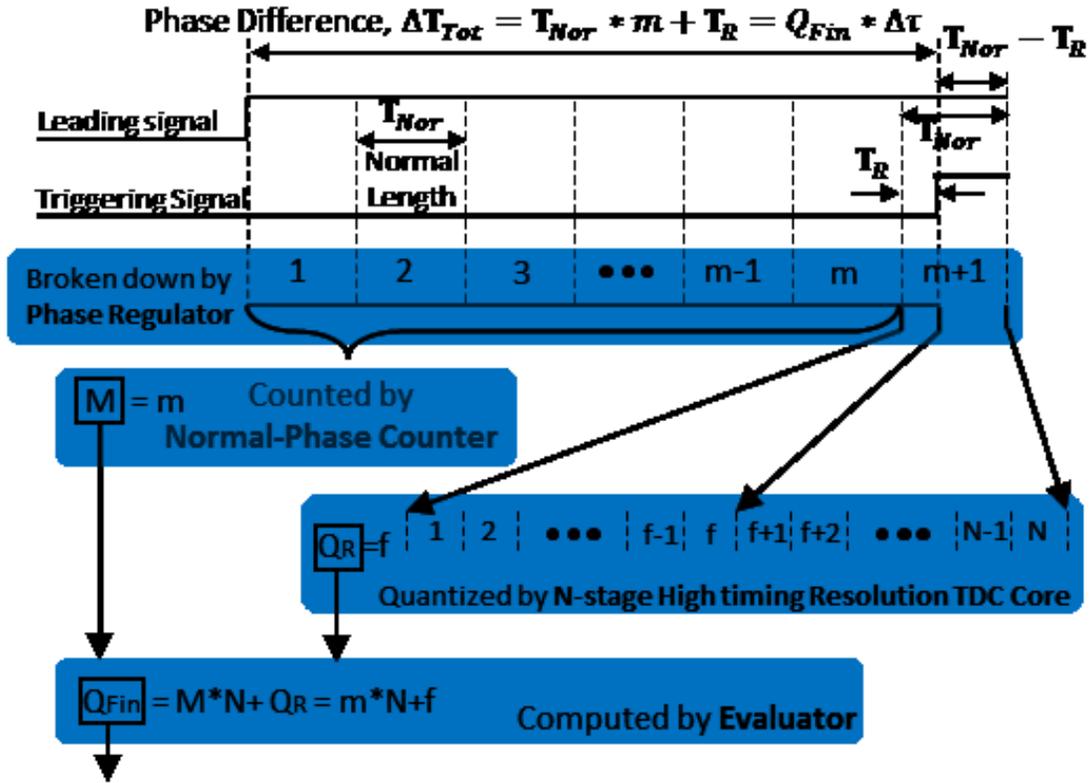


Fig. 11 Phase regulator illustration in time domain

The last piece, T_R being shorter than T_{Nor} (as a fractional part of T_{Nor}), is supposed to be the only part for a very fine time resolution measurement. And it will be quantized as Q_R by a N-stage fine resolution Vernier TDC core. Note that the value of N should be picked by allowing the fine resolution Vernier TDC to just cover the normal-length phase, T_{Nor} (i.e. new defined fine-granularity phase detection range). That means:

$$N = \frac{T_{Nor}}{T_{res}} = \frac{T_{Nor}}{\Delta\tau} \quad \text{Eq.(8)}$$

For instance, if T_{Nor} is set to be 60ps and the desired T_{res} equals 5ps, N (number of stages) should be 12. And the output of the Vernier TDC (Q_R) is determined by:

$$Q_R = T_R/\Delta\tau \quad \text{Eq.(9)}$$

where the value (f) of Q_R should locate between 0 and N.

While the rest of the phase ($\Delta T_{Tot} - T_R$) is not necessary for a tiny-granularity measurement so that it will be measured in large granularity (80ps). The normal-phase counter is used to record how many normal-length phase pieces are contained in the phase difference between leading and triggered signals, and then outputs a binary number (M) to the evaluator. Thus, the phase difference is given by:

$$\Delta T_{Tot} = M \cdot T_{Nor} + T_R \quad \text{Eq.(10)}$$

Substituting equation Eq.(8) and Eq.(9) into Eq.(10) gives:

$$\begin{aligned} \Delta T_{Tot} &= M \cdot N \cdot \Delta\tau + Q_R \cdot \Delta\tau \\ &= (M \cdot N + Q_R) \cdot \Delta\tau \end{aligned} \quad \text{Eq.(11)}$$

The definition of the final output of TDC (Q_{Fin}) therefore is:

$$Q_{Fin} = \frac{\Delta T_{Tot}}{\Delta \tau} = M \cdot N + Q_R \quad \text{Eq.(12)}$$

The result of Q_{Fin} is computed in the evaluator based on the given M (from the normal-phase counter), N (the number of the fine TDC core stages) and Q_R (from the N -stage fine resolution Vernier TDC).

Note from the comparison between Eq.(6) and Eq.(8), the number of stages in the phase-scaled Vernier TDC can be flexibly set as desired, unlike the traditional (Vernier) TDC solutions, in which the number of stages of the delay chains is proportional to the maximum period of the applied DCO clock. To what degree the stages of the former can be shrunk over the latter is determined by dividing Eq.(6) by Eq.(8):

$$\begin{aligned} \frac{N_{common\ law}}{N_{this\ work}} &= \left(\frac{\Delta T_{Tot_max}}{T_{res}} \right) / \left(\frac{T_{Nor}}{T_{res}} \right) \\ &= \frac{\Delta T_{Tot_max}}{T_{Nor}} \end{aligned} \quad \text{Eq.(13)}$$

For instance in order to target a time resolution of 5ps and phase difference of 12.5ns, a traditional Vernier TDC needs 2500 stages while a phase-scaled TDC only needs 16 stages (set T_{Nor} as 80ps). Actually, the TDC core in Fig. 10 can also be implemented in another fine resolution style (such as time-amplifier TDC) provided its time resolution performance is sufficiently good.

Theoretically, the set of the normal-length phase in the phase regulator can be as short as desired, resulting in a smaller TDC core. However, making this length shorter than 60ps is not

cost-efficient, because (as shown in Eq.(10)) a shorter T_{Nor} also increases the number of normal-length phase pieces (M), resulting in a larger number of binary bits in the phase counter, which also consumes more area and power. In this thesis, choosing M up to 256 (8 bits) can cover a phase detection range of 20ns in terms of $T_{Nor}=80ps$, that is accepted for an ADPLL in wireless applications from sub-hundred MHz to tens-GHz.

3.3 System Specification Assumption

Considering the requirements of state-of-the-art ADPLL applications, a set of specifications was chosen for the design of the proposed phase-scaled Vernier TDC and is present in Table2.

Table2: Specifications of the TDC

Specification	Symbol	Value
TDC Time Resolution	$T_{res}(\Delta\tau)$	2ps
DCO Output Frequency (Period)	f_{DCO} (P_{DCO})	80MHz~20GHz (50ps~12.5ns)
Phase-Detection Range	$\Delta T_{Tot,max}$ or $Max(P_{DCO})$	>12.5ns
Reference Frequency(Period)	f_{REF}	10~50MHz (the higher the better)
Large-Size-Inverter Delay	$\tau_{2\ fast}$	15ps
Normal-Inverter Delay	τ_{2_normal}	30ps

Note that a shorter time delay of inverters would cause a bigger size of the transistors, considerably increasing the area of the layout in the case of a large number of stages.

3.4 Phase Regulator & TDC Core

Fig. 12 shows a specific implementation of the phase-scaled Vernier TDC architecture and highlights the phase regulator part and the fine time resolution TDC core part. The phase regulator in this paper is realized by a ring oscillator of a few stage of inverters, those are also multi-used as the front part of the slow-path delay chain of the Vernier TDC core.

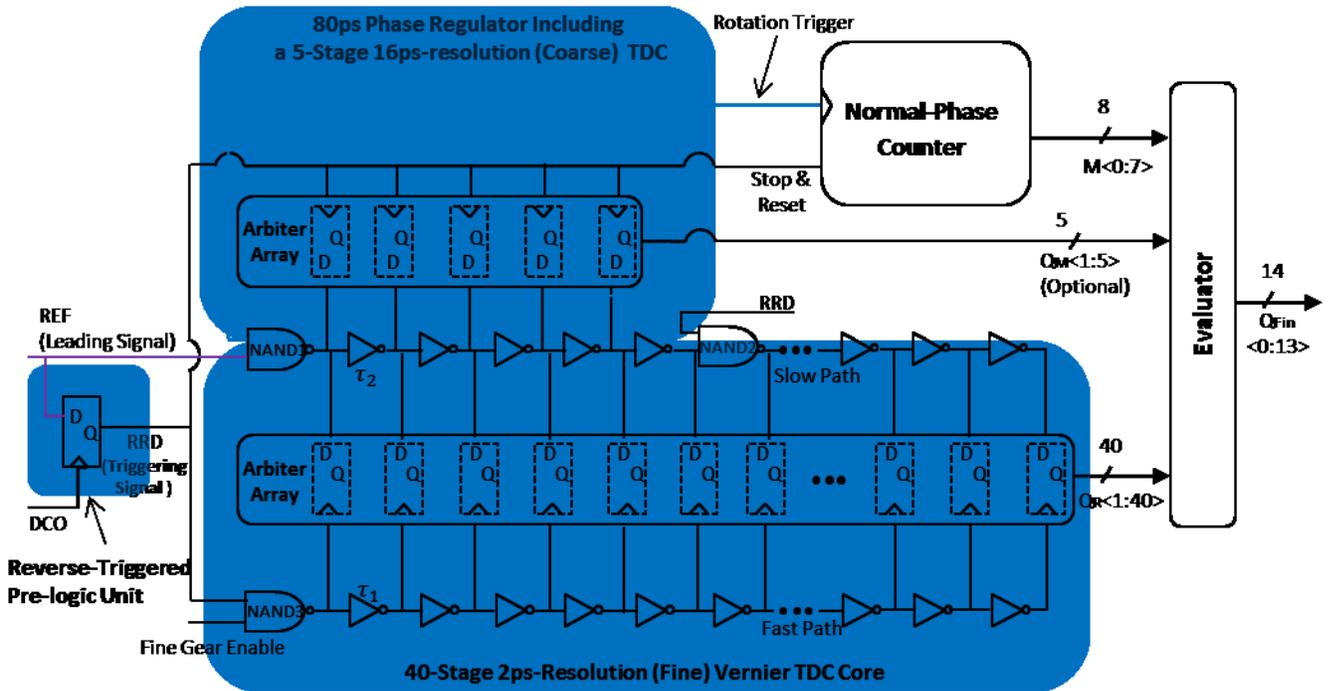


Fig. 12 Block diagram of Phase-scaled Vernier TDC (Phase regulator and TDC core)

The rising edge of the leading signal (REF) enables the gate NAND1, launching the run of the leading signal along the ring oscillator (Note that the other input terminal of NAND1 has become high already). Since this moment, the leading signal starts travelling in the loop of the ring oscillator and it triggers the counting of the normal-phase counter each time when it

completes a rotation (passes the last stage of the loop). The travelling on the ring will not stop until the triggering signal (RRD) come up. And then the counter can tell how many rotations (M) of the leading signal have been experienced along this ring structure. Note that the time period of a single rotation around the ring is actually the mentioned normal-length phase (T_{Nor}), which is set to be 80ps in this case. The number of the stages of the phase regulator can be 3 or 5 or 7 (odd) to make ring oscillator work correctly and efficiently. In this case the stages of the ring oscillator (N_{ring}) is set to be 5, thus the propagation delay of each stage of the inverter in the phase regulator (Δt_{ring}) can be determined by:

$$\Delta t_{ring} = \frac{T_{Nor}}{N_{ring}} = \frac{80ps}{5} = 16ps = \tau_2 \quad \text{Eq.(14)}$$

Note that τ_2 equals to Δt_{ring} .

As mentioned, the Vernier core is spared during most time of the phase detection operation, and it is only used to measure the last fractional piece, T_R . The arrival of the triggering signal (RRD) is used not only to start the run of the RRD signal along the fast path delay chain but also activate the sixth stage of the inverter in the slow path delay chain (RRD control gate NAND2). Then the triggering signal starts chasing the leading signal; and as in the common Vernier type TDC, the position where the triggering signal just caught up with the leading signal is indicated by the transition of the arbiters' output (Q_R). The number of stages of the Vernier TDC core (N_{core}) is determined by (Eq.(8)) the desired normal-length phase and the desired resolution:

$$N_{core} = \frac{T_{Nor}}{\Delta\tau} = \frac{80ps}{2ps} = 40 \quad \text{Eq.(15)}$$

And the slow-path inverter delay (τ_2) and the fast-path inverter delay (τ_1) should be equal to 16ps (as Eq.(14)) and 14ps ($\tau_1 = \tau_2 - \Delta\tau = 16ps - 2ps$) respectively. Therefore, the final

TDC output Q_{Fin} can be determined by the acquired M , $N=40$ and Q_R by Eq.(12). Compared to the Vernier Ring TDC solution where two arrays of arbiters are needed for odd-rotation and even-rotation respectively [13], this solution only needs one array of arbiters due to the ring-less structure of the fast path. This means that the complexity of a 40-stage Vernier core in this solution is actually equivalent to that of a 20-stage Vernier ring solution.

Because the completion of the odd rotation corresponds to the rising edge of the input signal of the normal-phase counter and even rotation corresponds to the falling edge of the input signal. Thus the phase counter should be a both-edge triggered counter to record each rotation of the signal. According to the phase detection range of 12.5ns in the Table2's specifications and 80ps of T_{Nor} , the Phase Counter may record 156 rotations maximum. Thus, an 8 bits normal-phase Counter (256) is sufficient.

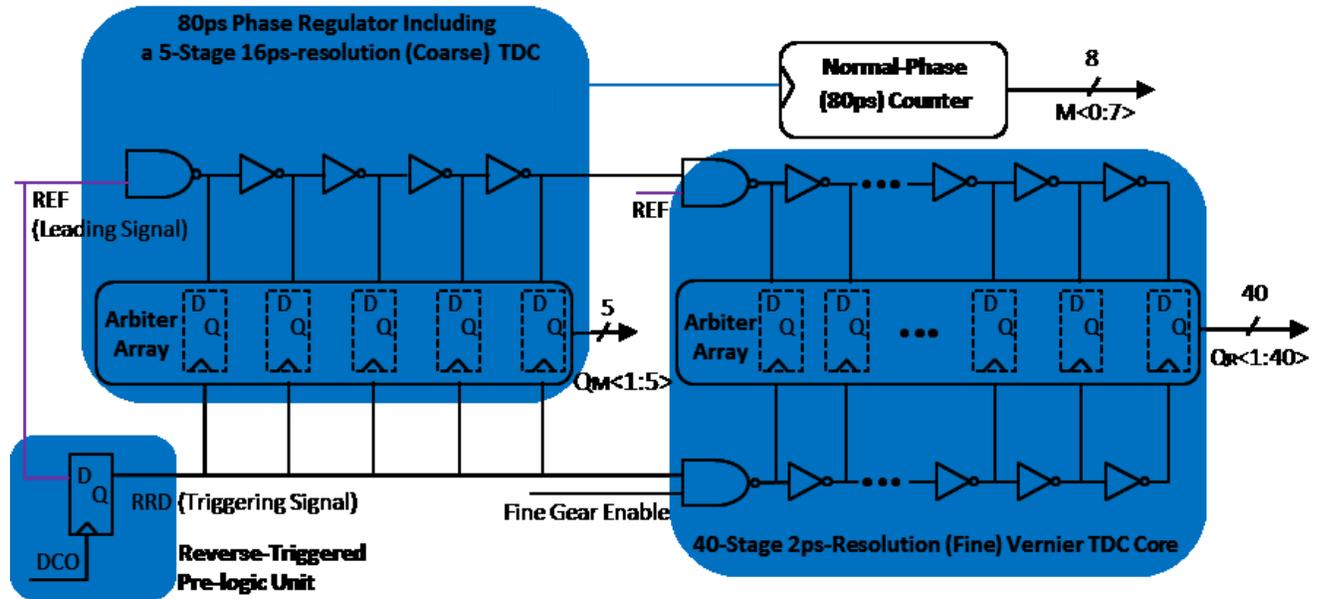


Fig. 13. A modified version of the phase-scaled Vernier TDC.

Fig. 13 shows a modified version of the phase-scaled Vernier TDC solution. It decouples the phase regulator circuitry and the fine TDC core circuitry of the solution shown in Fig. 12,

making the implementation easier. For example, in the former architecture, τ_2 has to be equal to Δt_{ring} of 16ps; while in the latter one, τ_2 can be set to 30ps for the purpose of the area reduction of the transistors in the TDC core circuit.

Table 3: Performance Analysis at a Fixed 25MHz Reference Frequency (40ns period)

Specification	Symbol	Vernier	15-stage Vernier Ring	Phase-scaled Vernier
TDC Time Resolution	$T_{res}(\Delta\tau)$	2ps	2ps	2ps
Phase-Detection Range	ΔT_{Tot_max}	12.5ns	12.5ns	12.5ns
Normal-Inverter Delay	$\tau_2 \& \tau_1$	30ps&28ps	30ps&28ps	30ps&28ps
Mandatory Fine Resolution Phase Length (Normal-length phase)	T_{NOR}	12.5ns	$(2*N-1)*\tau_1=870ps$	80ps
Effective N stages	N_e	6250	30	40
Max Capture Period	P_{C_max}	$6250*28ps=175ns$	$(870ps/2ps)*28ps=12ns$	$40*28ps=1.12ns$
Inverter output transitions in the Vernier TDC core in one reference period (inversely to Power consumption)	F_Power	$6250*2=12500$	$435*2=870$	$40*2=80$
Plus suppositional delay by evaluation period and pre-logic circuit: 4ns	$P_E + P_C$	$175+4=179ns$ Exceed one REF period (40ns)	$12+4=16ns < 40ns$	$1+4=5n < 20ns$
Conclusion		Impractical	Ok for time window, but medium power consumption	Good

3.5 Coarse/Fine Configuration & Optimization

Researching TDCs with switchable coarse/fine functions are popular in order to achieve optimal performances [15] and [16]. Similar to the current solution, as shown in Fig. 12 and Fig. 13, both of the two phase-scaled Vernier solutions illustrate a switchable coarse/fine time resolution function by employing an arbiter array (5 D Flip-Flops) into the phase regulator. The refined phase regulator is also functioning as a TDC with a coarse time resolution of 16ps (80ps/5). By replacing the seventh inverter (in slow path) and the first inverter (in fast path) with NAND gates (the other input terminal of the NAND is triggered by the RRD signal), the time window of the activity of the fine resolution Vernier TDC core can be easily managed. The circuitry is supposed to be active only when the last fractional phase piece is coming through.

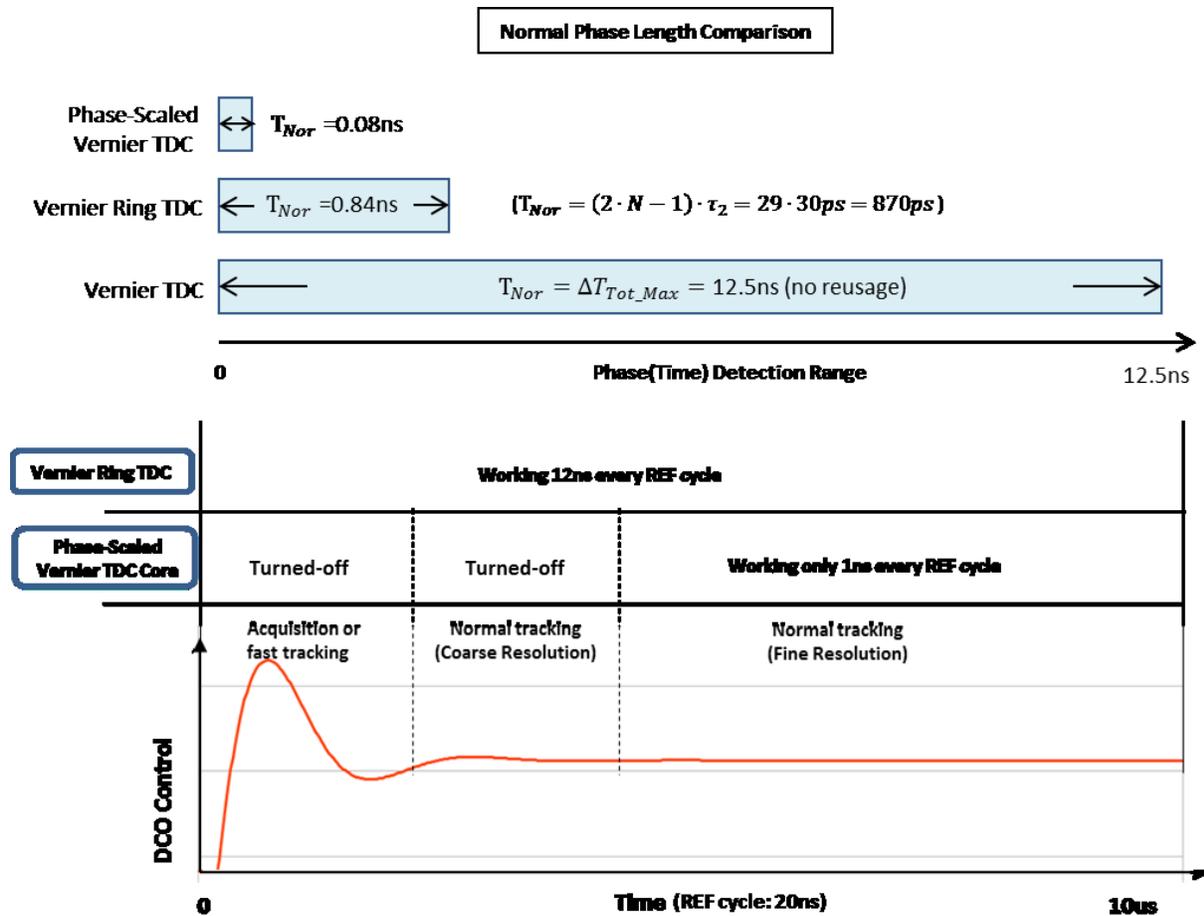


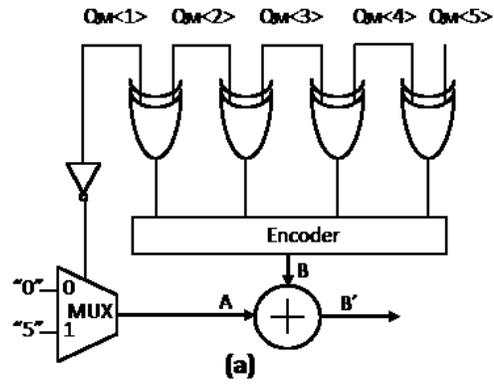
Fig. 14. Degree of activities of the VRTDC and Phase-scaled Vernier TDC.

In practice, the 2ps fine resolution TDC core can be turned off in most less demanding scenarios. For a demanding requirement, the fine resolution TDC core can still be off in the acquisition & coarse-resolution tracking period, until the ADPLL requests it to turn on (Fig. 14). Even during fine-resolution tracking, the real-working period of the phase-scaled Vernier TDC is only around 1ns (Table 3), 12 times shorter than that of a 15-stage VRTDC. That difference causes a huge difference in the number of times of inverters transition between the VRTDC (840 times) and the phase-scaled TDC (80 times). The above characteristic allows the phase-scaled Vernier TDC to have even lower (over 10 times) power consumption compared to the Vernier Ring counterpart. Therefore, the scheme of two steps (coarse-fine resolution) phase-scaled TDC

provides a super low power consumption solution without trading off other crucial performance parameters.

Note that the introduction of the 5 arbiters in the phase regulator also facilitates a smart determination called the coordinated-determination device, which could remarkably simplify circuits in the evaluation unit. The coordinated-determination device will be described later. The output of 5 arbiters $Q_M < 1:5 >$ can also be used to optimize the counter circuit and up-scaled the phase detection range. Specifically, the both-edge triggered counter is used to record every rotation on the ring oscillator; however it can be simplified to a one-edge triggered counter which only record every other rotation in order to loosen the demand on the response-speed of the counter circuitry. In that case, the LSB of the 8-bit counter will correspond to 160ps instead of 80ps, and for an even number of rotations the final result needs a 80ps compensation. In addition, this modification would double the range of the phase detection, from 20ns (256*80ps) to 40ns (256*160ps) at a fixed 8 bits. This optimization can be realized by the following steps (Fig. 15):

1. The outputs of 5 D Flip-Flops $Q_M < 1:5 >$ are processed by a set of XOR gates to determine the position of the transition $Q'_M < 1:5 >$.
2. A simple encoder produces a binary number (B) basing on $Q'_M < 1:5 >$.
3. By distinguishing the state of $Q_M < 1 >$, it will be aware of whether there is an even number of rotations or not. A is used to correct the final output B' with value of 5 (corresponding to one more rotation 80ps) in the case of an even number rotation.
4. B' is the sum of A and B.



QM1	QM2	QM3	QM4	QM5	A+B=B'
1	0	0	0	0	0+1=1
1	1	1	1	0	0+4=4
1	1	1	1	1	0+5=5
0	1	1	1	1	5+1=6
0	0	0	1	1	5+3=8
0	0	0	0	0	5+5=10

(b)

Fig. 15. (a) Logical modification for rising-edge only phase counter, (b) True table of (a) circuitry.

3.6 Evaluator

Functionally, as shown in Eq.(12) the evaluator calculates the output of the normal-phase counter, M (the number of normal length phase pieces between phase difference) and the output of the Vernier core unit in thermometer-code format ($Q_r<1:40>$) which is determined by Eq.(9). Thus Q_{Fin} for a 40 stage fine TDC core is decided by:

$$Q_{Fin} = M \cdot 40 + Q_R \quad \text{Eq.(16)}$$

Usually a 40/6 bits thermometer-to-binary encoder may be employed to convert Q_R from thermometer code to binary code. The complexity of the thermometer-to-binary encoder increases exponentially with the digit number of the thermometer code; although it is already much simpler than that of a priority type decoder, which is commonly used in a Vernier Ring TDC due to the possibility of the presence of multiple fake transitions. However, in this thesis a 40/6 bits thermometer-to-binary encoder is still viewed as a complicated conversion and deserves for further simplification into an 8/3 bit simple encoder by applying the coordinated-determination device in the evaluator. From Fig. 16, $Q_M<1:5>$ is the output of the arbiters located in the phase-regulator (5-stage ring-oscillator), that actually can be regarded as arbiters of a ring-oscillator TDC. As mentioned, the setting of T_{Nor} (normal-length phase) of 80ps is covered by a 5-stage ring-oscillator with a propagation delay of each stage at 16ps (i.e. coarse resolution); also covered by a 40 stages Vernier TDC core with 2ps resolution (fine resolution). $Q_M<1:5>$ and $Q_R<1:40>$ indicate the quantitative measurement value of T_R with 16ps and 2ps resolution respectively, and every bit in $Q_M<1:5>$ sequentially corresponds to eight bits in $Q_r<1:40>$ (Fig. 16(b)). In the coordinated-determination device (Fig. 16(a)), the exact position of the transition can be determined by the following steps:

a) $Q_M<1:5>$ gets through an array of XOR gates (Fig. 15 (a)) to find the position of its values' transition (transferring the thermometer code format of data to simple code format $Q'_M<1:5>$). $Q_R<1:40>$ can be distributed into five sections, which correspond to $Q'_M<1>$ ~ $Q'_M<5>$.

b) Second, the exclusive bit of “high” in $Q'_M<1:5>$ is used to select the corresponding section of $Q_r<1:40>$ which should be the section that contains the position of the edge transition in higher precision (labeled $Q'_r<1:8>$).

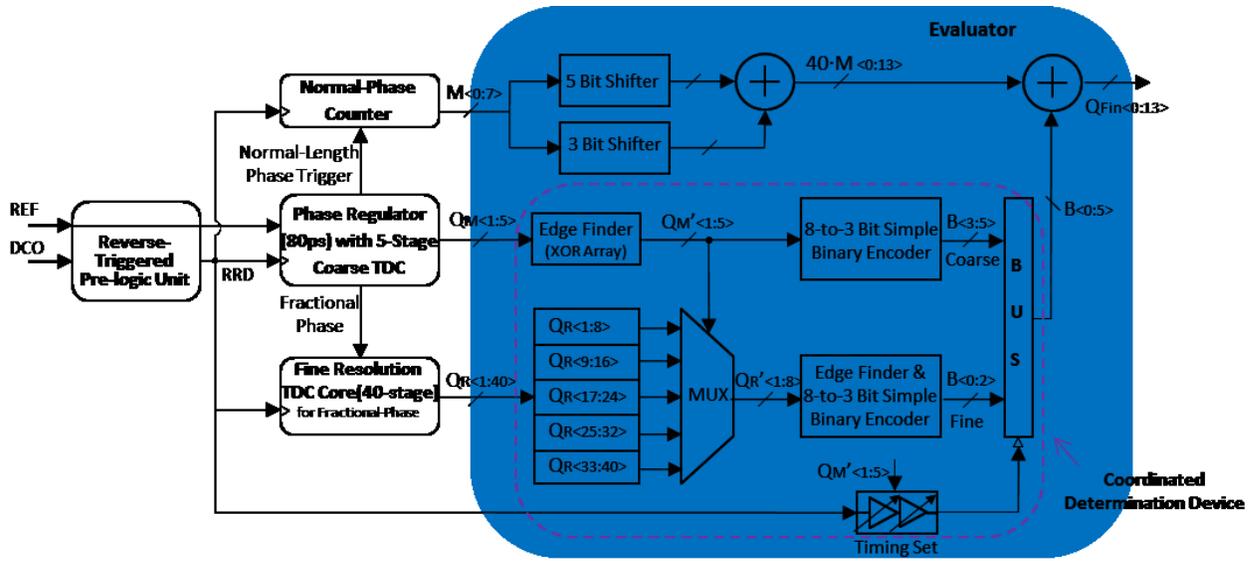
c) Third, $Q'_M<1:5>$ is converted by a simple encoder (8/3) into a three bit output, $B<3:5>$ which represent the three most significant bits of a 6 bit binary number which shows the effective remaining phase difference (T_R) in coarse resolution of 16ps.

d) Meanwhile, $Q'_r<1:8>$ is converted by an edge finder and a simple encoder (8/3) into a three bit output, $B<0:2>$ which represent the three least significant bits of the above mentioned 6 bit binary number to exhibit the fine part of T_R in 2ps resolution.

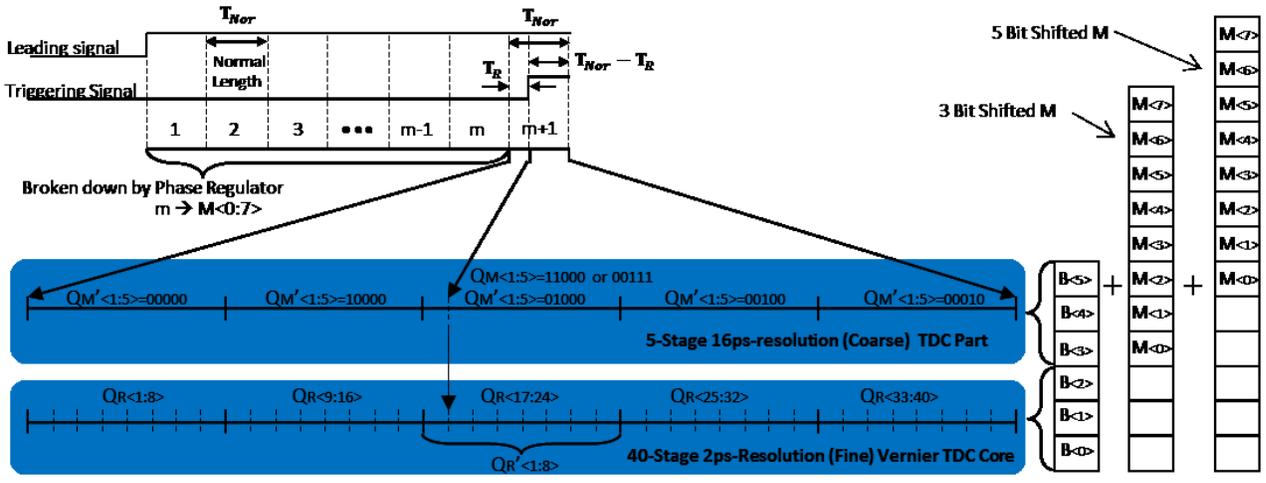
e) The key point is the 3-bit output of the coarse-detection ($B<3:5>$) from arbiters of the phase regulator can be just easily stacked onto the 3-bits of the fine-detector ($B<0:2>$), avoiding additional computation and conversion, provided the equation $N_{core}/N_{ring} = 2^K$ is the case (where K is a positive integer).

Note that the coordinated- determination device reducing the processed bit number by 5 times (from 40 bits in $Q_R<1:40>$ to 8 bits in $Q'_R<1:8>$) and not only facilitates the simplification of logic circuitry in the evaluator but also removes the possibility of the error due to the appearance of the fake transitions in other sections.

The multiplication arithmetic ($M \cdot N_{core}$) is implemented with an addition arithmetic between two bits-shifted by M as shown in Fig. 16(a) Because 40 is expressed as 101000 in binary format, which shifts M by 3-bits and 5-bits respectively, and then add two items up to get a 13-bit binary number of $M \cdot 40$. Finally, Q_{Fin} will be determined by adding $M \cdot 40$ to Q_R .



(a)



(b)

Fig. 16. (a) Evaluator and Coordinated-Determination Device, (b) and their operations in time domain.

3.7 Pre-logic Circuit with Reversed-Trigger Solution

Generally, a reference signal is used as a triggering signal of arbiters to latch the instantaneous state of each node of the delay chain along which the DCO signal is travelling. The

reference signal and the DCO signal cannot be exchanged due to the fact that the triggering and latching of the arbiters should be performed only once per period of the reference clock. Multi-transitions of the triggering signal would lead to an error, especially for the Vernier type TDC. In a common Vernier Ring TDC, a pre-logic circuit with pulse-generators needs to be embedded into the front-end of the circuit to avoid the transition behavior of the leading signal and triggering signal during the rest of the TDC determination cycle. However, a phase error may be present when the phase difference is narrower than the width of the pulse, although the width is designated to be a tiny value like 10ps. The pre-logic circuit is also used to identify and distribute the REF signal and the DCO signal into the slow path and the fast path respectively, as the leading signal and the triggering signal. The operation will also face a meta-stability issue occasionally while the two edges of the REF and DCO are very close to each other, causing extra unknown phase error.

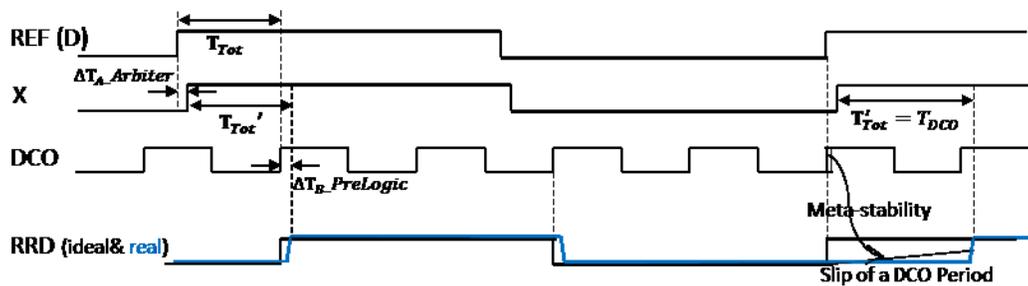


Fig. 17. Waveform illustration of reversed-triggered pre-logic unit.

In the present solution, a super concise style of pre-logic circuit, named the reversed-trigger pre-logic unit is introduced to steer the whole phased-scale Vernier TDC for accurate operation with low power consumption. In Fig. 18(a), the reference signal is oversampled by the high rate DCO signal, yielding a “reference-retimed-by-DCO” signal (RRD). As shown in Fig. 17, the rising edge of the RRD is aligned in the time domain with the first DCO rising edge

which follows the presence of the reference signal. Conversely to the traditional triggering strategy, the reference signal in this case is regarded as the leading signal to be injected into the TDC directly, launching the TDC operation procedure, while the RRD signal is viewed as the triggering signal to trigger the arbiters of the TDC (Fig. 18(b)), symbolizing the end of the phase difference. The main advantage of the reversed-trigger solution is to eliminate the high rate DCO signal's multiple transitions (reversals) avoiding the usage of the pulse generator which leads to a phase error as mentioned above.

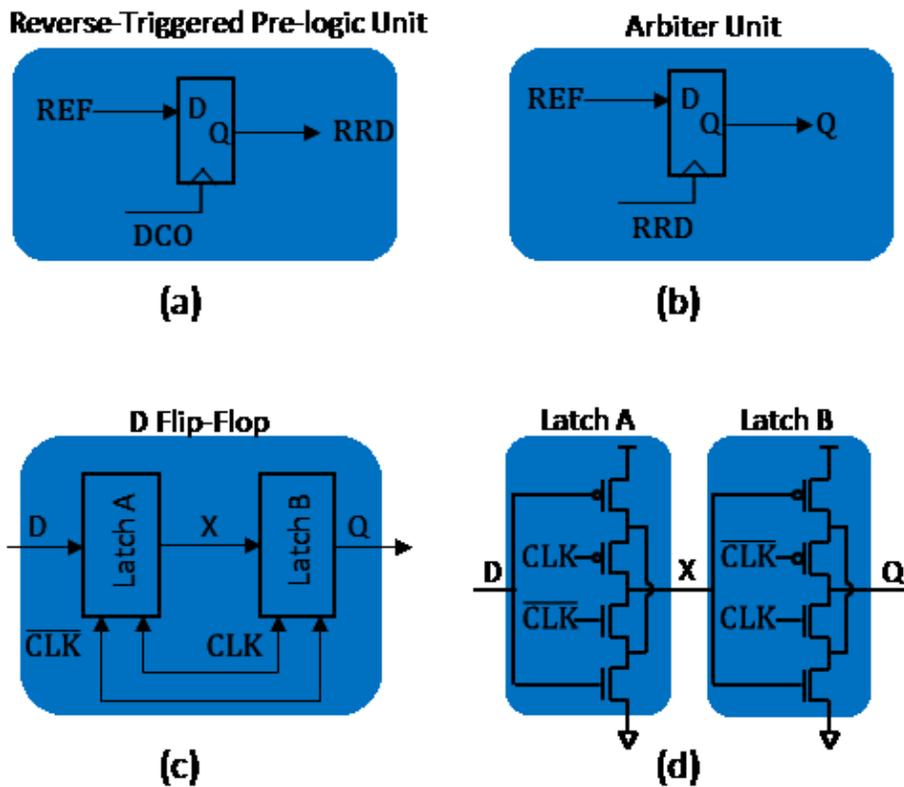


Fig. 18. (a) Reverse-triggered pre-logic unit block, (b) Arbiter unit block, (c) D Flip-Flop block, (d) D Flip-Flop transistor level block.

Additionally, the reverse-triggered pre-logic circuit is being combined with a function of phase-offset cancelation. In Fig. 18(c), the arbiter is actually a D flip-flop which consists of two latches staged up. When the clock triggers the D flip-flop, the arbiters do not capture the state of the REF but the state of the X node. And X is a duplicated REF with the delay of ΔT_A due to latch A's propagation. That means the arbiters always capture the reference a short time (ΔT_A) before it is triggered by the DCO signal due to the propagation delay of the transistors of latch A. This time-offset causes a constant phase error during the quantization measurement in many popular TDC solutions. Fig. 17 shows that there is another time-offset delay between the RRD and corresponding DCO rising edges (ΔT_B), which is caused by latch B of the reversed-trigger pre-logic unit (Fig. 18(b)(c)). Note that the real phase difference ($\Delta T'_{Tot}$) is determined by:

$$\Delta T'_{Tot} = \Delta T_{Tot} + \Delta T_{Bprelogic} - \Delta T_{Aarbiter} \quad \text{Eq.(17)}$$

If one of the offsets can be set (by choosing proper parameters of the transistors) to be equal to the other one (i.e. $\Delta T_{Bprelogic} = \Delta T_{Aarbiter}$), the phase offsets will be canceled out, making the triggering signal capture the current state of the REF signal with no phase error (i.e. $\Delta T'_{Tot} = \Delta T_{Tot}$).

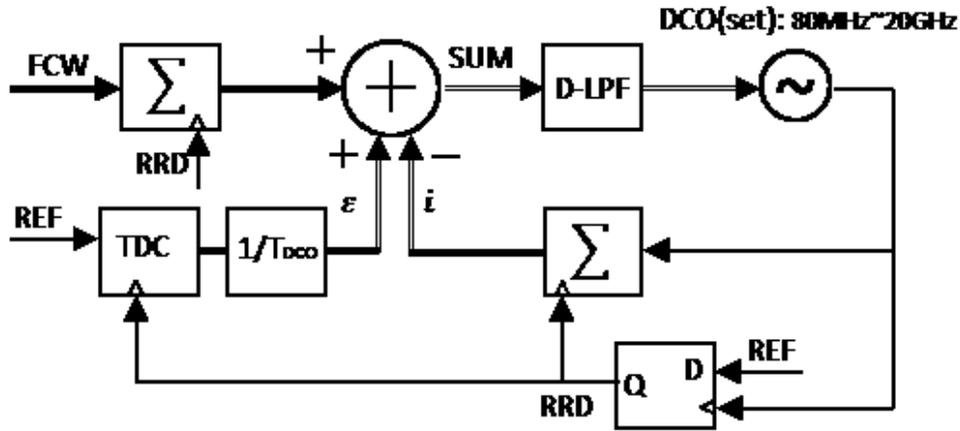


Fig. 19 The Proposed ADPLL system operation diagram

The third advantage of the reverse-triggered pre-logic unit comes from the fact that it can perfectly match the ADPLL system oversampling-time strategy, which means both system and TDC use RRD as the synchronous trigger (Fig. 19). The reference signal is introduced directly into the leading signal path of the TDC, compared to the complicated processing of the pre-logic circuit in the common Vernier Ring TDC. In the VRTDC, if the REF edge and DCO edge rise simultaneously, at least one of the outputs of the pre-logic unit will lead to a meta-stability state, resulting in an extra phase offset between the leading signal and the triggering signal. While in the phase-scaled Vernier TDC, as shown in Fig. 17, when the transitions of the REF and DCO happen simultaneously in the reversed-trigger pre-logic circuit, the second DCO rising edge would overcome the occurrence of the meta-stability and setup the RRD to the “1” state instead. In this situation, the detected phase difference will be roughly a DCO period instead of close to zero, which means that a slip with the length of a DCO period occurs. Fortunately, there is no need to be concerned, because this slip can be tolerated even without any additional computation by applying the proposed ADPLL system solution in Fig. 19. Fig. 20 shows an example of the

ADPLL system level operation in the time domain based on the principle in Fig. 19. Note that the REF edge and DCO edge rise simultaneously at the thirteenth period of the DCO and a slip occurs. However the DCO period counting and TDC measurement extents by the same value and the output of the SUM will still be zero, which means the occurrence of the slip has no impact on the aggregate operation in the system level.

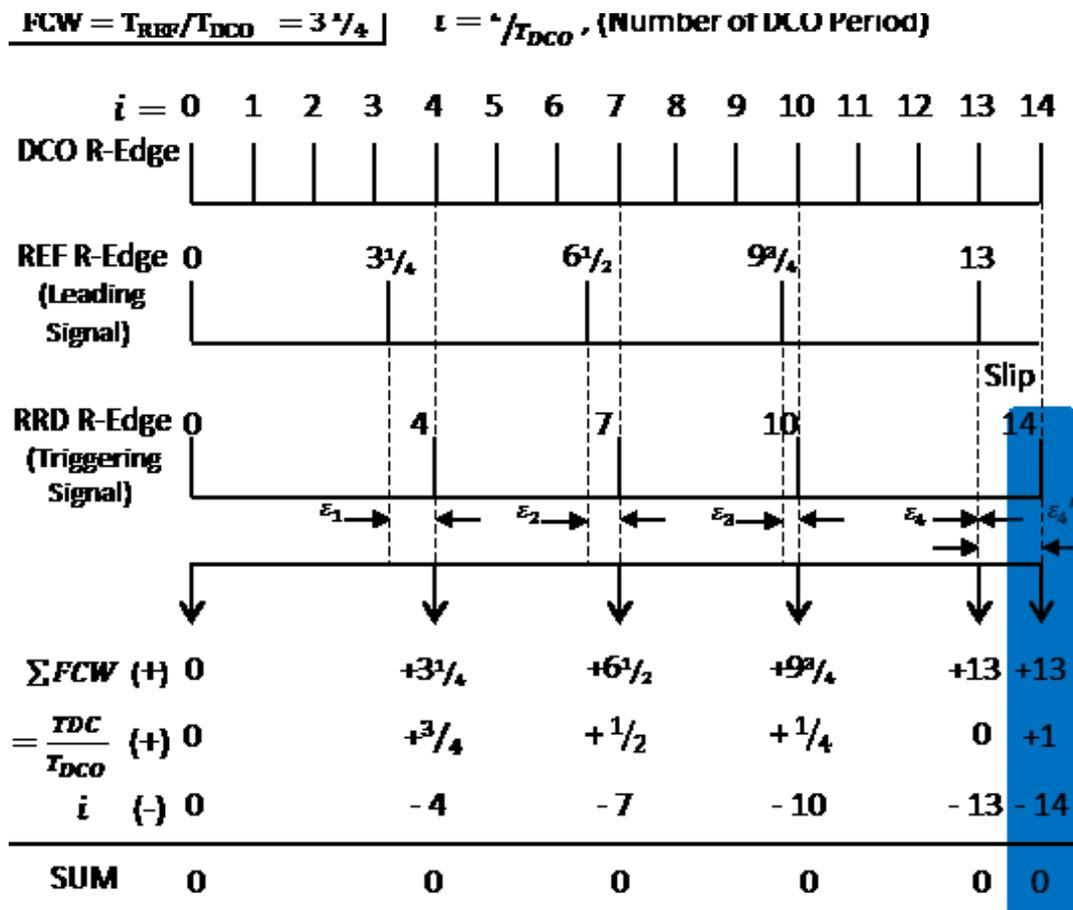


Fig. 20 ADPLL timing and computation example (FCW=3.25)

Chapter 4: TDC Timing Considerations for Higher Reference Frequency

TDC operating-period performance is seldom discussed due to sufficient time margins in most applications under low REF frequency circumstances. However, a high REF frequency requirement trends to be becoming more popular in order to achieve better phase noise performance. Therefore, the operating period performance will play a more important role in TDC research to achieve an optimal solution, especially in scenarios which need a high reference frequency (>50MHz). Operating-period (P_L) is defined as a time period starting from the moment of the rising edge of the triggering signal and ending with the guaranteed moment when the TDC can accomplish a final output for the ADPLL system computation. The purpose of the operating-period performance is primarily to estimate whether a certain kind of TDC solution is feasible for a specific applied reference frequency. Meanwhile, it can also predict the upper limit of the frequency of the reference signal being used by this TDC solution. Moreover, by learning about the time margin of a TDC solution, a comprehensive optimization is available for the purpose of obtaining an optimal solution not only of the TDC but also of the end-to-end synthesizer design.

4.1 General Operating-Time Procedure

Prior to a detailed discussion of the operating-period performance analysis, a general operating procedure of a TDC is described as follows (Fig. 21):

a) P_A : The active period starts with the rising edge of the leading signal and stops at the moment of the rising edge of the triggering signal. The active period corresponds to the phase difference of a TDC.

b) P_C : The capturing period is regarded as the time period that a TDC takes to ensure all necessary states of arbiters have been stored.

c) P_E : The evaluation period indicates how long a TDC spends to process the output of the arbiters and produce a final quantitative binary number which shows the measured phase difference. Usually this period is relatively stable and less than a few ns in a variety of TDC solutions, unless the number of the arbiters is too large (more than 200) or the computations are complicated. 4ns of P_E is assumed for all TDCs for comparison in this thesis.

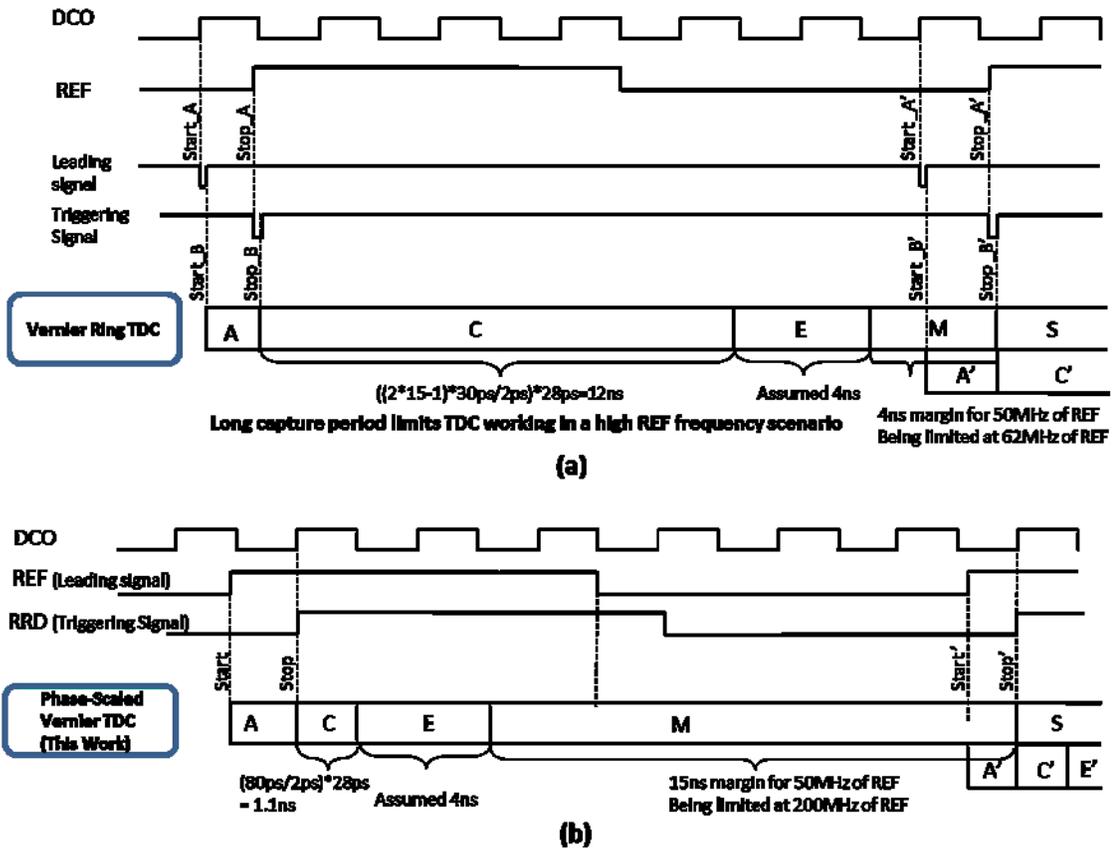
d) P_M : The margin period is the remaining time length after subtracting P_C and P_E from the REF period P_{REF} .

e) P_S : The period for ADPLL system computation and operation. P_S is expected to occupy the next REF period.

Therefore the REF period, P_{REF} and the maximum value of f_{REF} , f_{REF_MAX} can be expressed by:

$$P_{REF} = P_C + P_E + P_M \quad \text{Eq.(18)}$$

$$f_{REF_MAX} = 1/(P_C + P_E) \quad \text{Eq.(19)}$$



A: Active Period. C: Capturing Period. E: Evaluating Period. M: Margin Period. S: System Operation Period. A': Next Active Period.

Fig. 21 Operating-period Performance Comparison Between (a) VRTDC and (b) Phase-Scaled Vernier TDC.

4.2 Operating-Period Performance Comparison

First, a quantitative operating period analysis is performed for the presented phase-scaled Vernier TDC. According to the principle of the phase-scaled Vernier TDC, the mandatory fine-resolution phase length (i.e. normal length, T_{nor}) is 80ps in this case and the Vernier TDC core will need 40 stages with each stage having a resolution of 2ps (30ps-28ps). The guaranteed capturing period is determined by:

$$P_c = \left(\frac{T_{nor}}{\Delta\tau} \right) \cdot \tau_1 = \left(\frac{80ps}{2ps} \right) \cdot 28ps \quad \text{Eq.(20)}$$

$$= 1.1ns$$

The length of the evaluating period depends on the complexity and the parameters of the evaluator. Choosing 4ns for the evaluation period will be adequate in most modern CMOS processes for a moderate number of inverter stages. Thus, for a 25MHz REF, the margin period is:

$$P_M = P_{REF} - P_C - P_E \quad \text{Eq.(21)}$$

$$= 40n - 1.1n - 4n \approx 35n$$

Also note that the highest accepted reference frequency is:

$$f_{REF_MAX} = \frac{1}{P_C + P_E} = 200MHz \quad \text{Eq.(22)}$$

As for a 15-stage Vernier Ring TDC, the mandatory fine-resolution phase length (i.e. normal length, T_{nor}) is $(2*N-1)*\tau_1=870ps$. The guaranteed capturing period is determined by:

$$P_c = \left(\frac{T_{nor}}{\Delta\tau} \right) \cdot \tau_1 = \left(\frac{870ps}{2ps} \right) \cdot 28ps = 12ns \quad \text{Eq.(23)}$$

Similarly, for a 25MHz REF, the margin period will be only 4ns and highest accepted reference frequency will be 62MHz. The above results and performances are summarized in Table 4, which also includes the result of a traditional Vernier TDC. Note from Table 3 and Table 4 that a traditional Vernier TDC may need an extremely large number of delay stages in the case of demanding specifications (fine resolution and wide phase-detection range), resulting in an impractical solution. Thus, for a Vernier type, the phase-detection range performance and corresponding stages of delay chains would be a tough limitation, although it can achieve a fine resolution. Compare to the VRTDC, the phase-scaled Vernier TDC can accept a f_{REF_MAX} 3 times higher (200MHz/62MHz), which can improve the phase noise performance (caused by the TDC time resolution) by over 5 dB. In fact, the phase-scaled Vernier due to its ring-less structure of the triggering path enables one-off latching action, compared to the ring structure of the triggering path in a Vernier ring TDC where the multiuse of the delay chains and arbiters needs a multi-latching and updating function which demands longer operating-period performance.

Table 4: Improvement of the Phase Noise Performance with Different Accepted Reference Frequency (1GHz of DCO output)

Specification	Symbol	Vernier	15-stage Vernier Ring	Phase-scaled Vernier
TDC Time Resolution	$T_{res}(\Delta\tau)$	2ps	2ps	2ps
Normal-Inverter Delay	$\tau_2\&\tau_1$	30ps&28ps	30ps&28ps	30ps&28ps
Mandatory Fine Resolution Phase Length	T_{NOR}	NO	$(2*N-1)*\tau_2=870ps$	$3*\tau_2=90ps$
Effective N stages	N_e	500	30	40
Max Capture Period	P_{C_max}	$500*28ps=14ns$	$(870ps/2ps)*28ps=12ns$	$40*28ps=1ns$
Operating-period	$P_E + P_C$	$14n+4n=18ns$	$12n+4n=16ns$	$1n+4n=5ns$
Highest REF Frequency	REF_{max}	$1/(14n+4n)=55MHz$	$1/(12n+4n)=62MHz$	$1/(1n+4n)=200MHz$
Phase noise performance Improvement		0	0.5dB	5.6dB

Table 5: Comparison of Several TDC Architectures

Specification	Traditional TDC	Ring-Osci TDC (9-stage)	Vernier TDC	Vernier Ring TDC (15-stage) [13]	Phase-scaled Vernier TDC
Resolution 2ps	10ps	10ps	2ps*	2ps	2ps
Effective stages	12.5n/10p= 1250	9	6250	30*	40
Operating-Period (Assume PE=4ns)	4ns	4ns	183ns	16ns	5ns
Highest f_REF	250MHz	250MHz	5.5MHz	62MHz	200MHz
Phase Noise***	0dB	0dB	2.6dB worse	7.9dB better	13dB better
Area Cost	High	Low	Super high	Medium	Medium
Power Consumption	High	Low	High	Medium	Low
Applied field		Wide range, coarse resolution, low cost	Narrow range, high resolution	Wide range, high resolution, medium cost	Wide range, fine resolution, low cost

*: effective stages doubles due to ring type of triggering path completing a rotation every other rotation.

Chapter 5: Circuit Implementation and Simulation

5.1 Technology Process and Basic model parameters

The most importance of the implementation of TDC is to reduce the propagation delay of the transistors especially of delay chain due to the requirement its time resolution performance which is at ps generally. The technology used in this research will be a 65nm CMOS process with low V_T deep well NMOS and PMOS transistors. The delay unit of the delay chain is used inverter which consists of a PMOS transistor and a NMOS transistor. The propagation delay of a inverter depends on the output capacitance plus load capacitance, voltage change and drain current [17], as shown below (Eq.(24)):

$$t \propto \frac{C}{I} \Delta V \quad \text{Eq.(24)}$$

Thus, to shrink the delay time of a logic gate, the following parameters could be tuned:

1. Decrease the swing (supply) voltage, ΔV .
2. Reduce loaded capacitance (C_{Load} is a part of C in Eq.(24)).
3. Increase current by increasing the channel width-to-length ratio. In this case, because the length of the transistors has been fixed at 60nm, the width of channel could be increased to reduce the influence of parasitic or load capacitance and decrease the delay.
4. The ratio of PMOS width (W_P) and NMOS width (W_N) influences the transition response of the inverter as well.

From Fig. 22 transition response gets slow with low W_p/W_n of the inverters, the capacitive load value (C_{load}) at a constant voltage supply and W/L value. In order to get a sharp transition in the time domain, a large W_p/W_n ratio and small loading are desired.

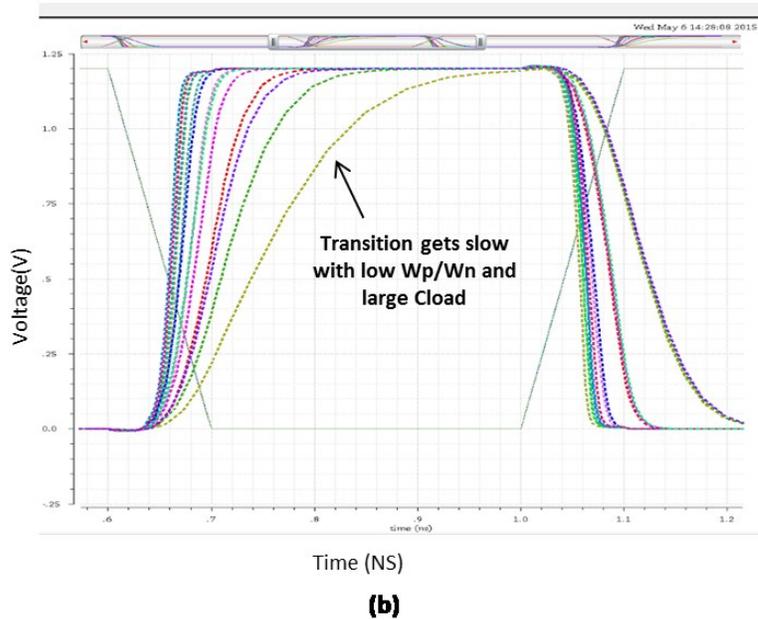
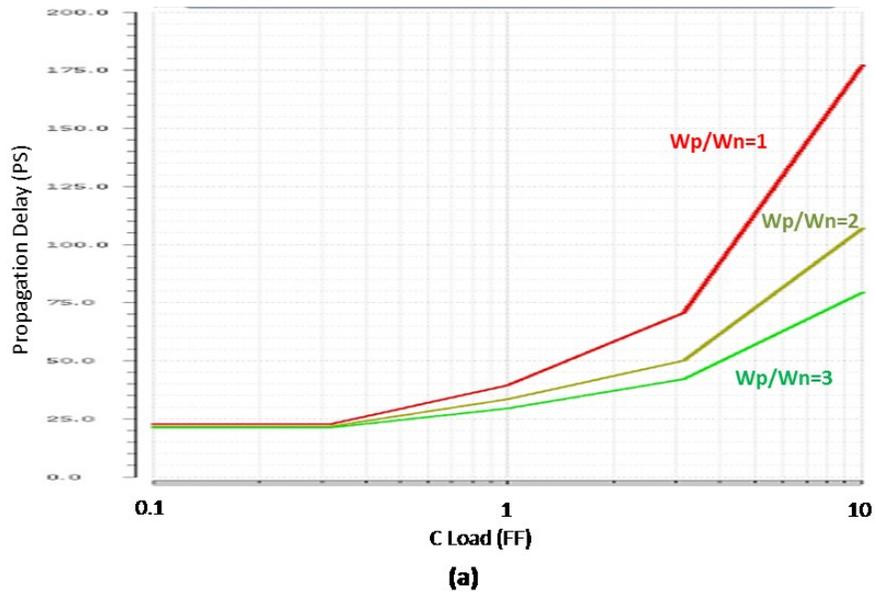


Fig. 22. Propagation delay of inverters with various W_p/W_n ratios and C_{load} .

Fig. 23 shows an inverter's DC transfer simulation sweeping the ratio W_P/W_N . A ratio of 3:1 for the width of PMOS to NMOS is a good starting point for the size of inverters because with this choice, a 600mV input corresponds to a 600mV output.

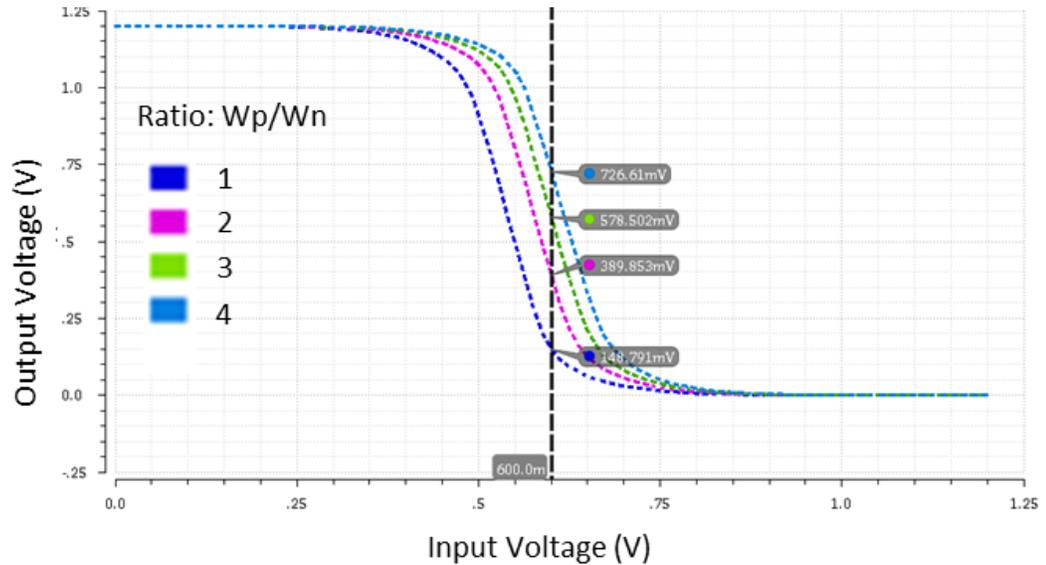


Fig. 23 Static Inverter's DC Transfer simulation.

5.2 Vernier TDC Core Circuit

As mentioned in the previous chapter, a Vernier TDC core consists of a slow path inverter delay chain, a fast path inverter delay chain, and a set of D Flip-Flops.

5.2.1 Slow path inverter delay chain

The implementation of an inverter delay chain as shown in

Fig. 24 should follow these guidelines:

- Identical propagation delay time in each stage.

- Rise time and fall time should be identical to make the delay chain's behavior in odd rotations similar to that in even rotations.
- Reduce the effect of the load from the D Flip-Flop as much as possible. Do this by making the stage transistors at least three times larger than the D Flip-Flop buffer transistors. For example assuming a W/L of 200nm/60nm for the D Flip-Flop buffer transistors, the stage should have a W/L \geq 600nm/60nm to get a reasonably small impact of load on the inverter delay chain.

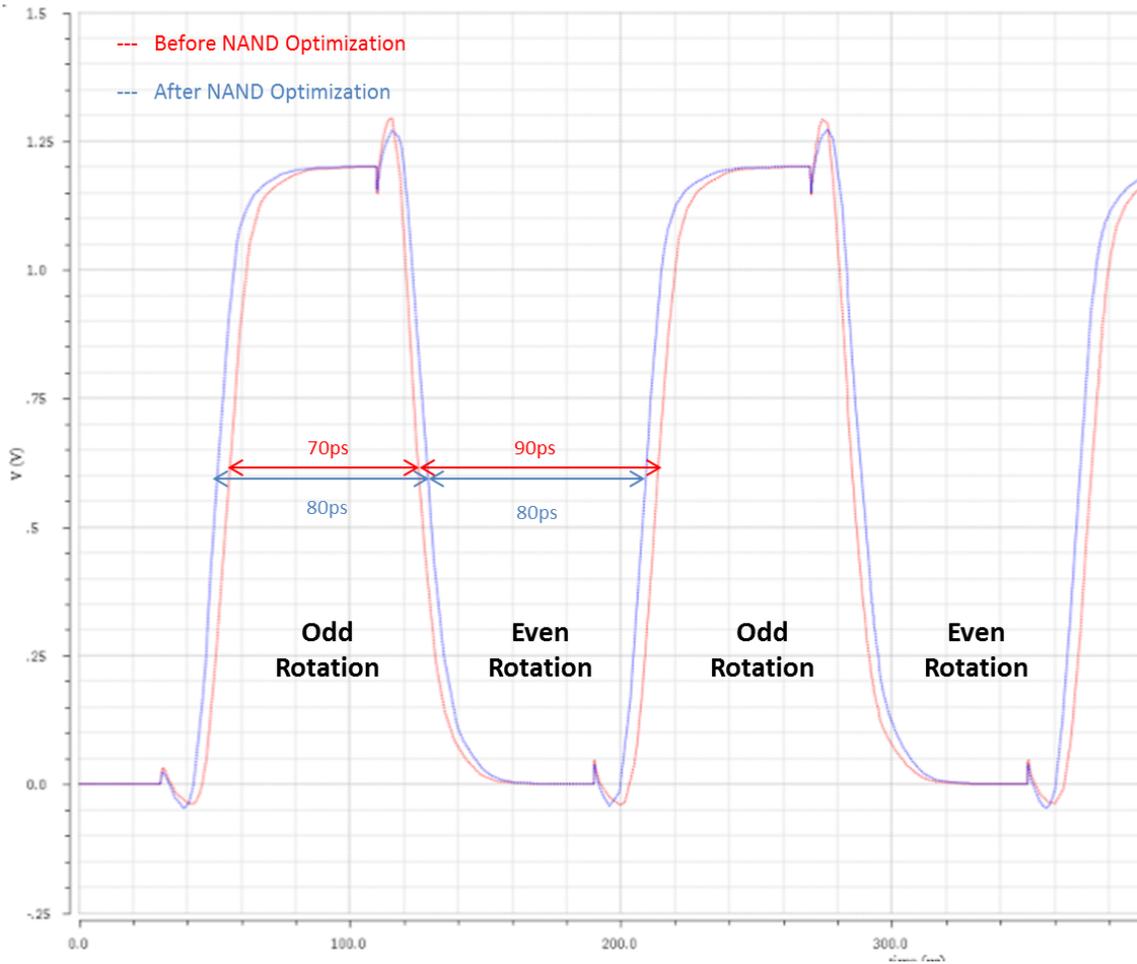


Fig. 25. NAND Optimization for equal length of odd and even rotations.

5.2.2 D Flip Flops

Fig 26(a) shows a dynamic inverting flip-flop built from two back-to-back dynamic latches [18]. To reduce the delay of the circuit, there is no buffer at node Q. Flip-Flops usually use a single clock ϕ and generate its complement $\bar{\phi}$ locally. Obviously, there will be some delay in $\bar{\phi}$ relative to ϕ , which will lead both the clock and its complement to be in intermediate state (Fig 26(b)). Consequently, both latches will be transparent or meta-

stable for a certain period. To avoid the above mentioned issue, a differential clock pair is needed in this research and will be introduced in the next section.

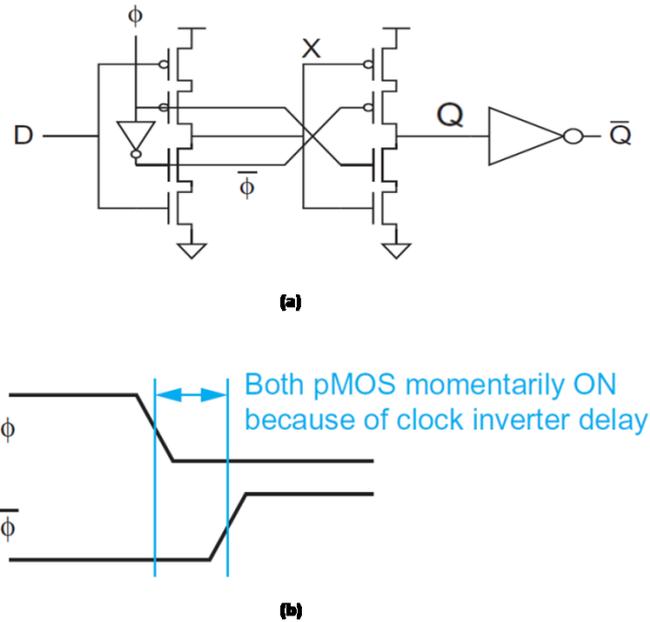


Fig 26. (a) A D Flip Flop circuit and (b) illustration of non-ideal issue. [18]

In this research, two types of D Flip-Flops are needed, one for the arbiter array and the other for RRD generation. The arbiter array consists of 40 D Flip-Flops which are used to capture the output state of each stage of the slow path inverter delay chain. Thus, those D Flip-Flops are the load of the delay chains and the value of their input capacitance impacts the speed of the circuit response. The clock load should be kept as small as possible aiming at fast speed and low power consumption. Table 6 indicates the initial configuration of the design parameters.

Table 6: D Flip Flop initial parameters configuration.

Static Transistors Width	Transmission Gate Width	
--------------------------	-------------------------	--

PMOS	NMOS	PMOS	NMOS	Fingers
600nm	200nm	300nm	300nm	1

The RRD generator's D Flip-Flops should be fast and heavy duty because they drive the fast path delay chain which drives the clock load of the arbiter-array in turn.

5.3 Differential RRD and Trigger Clock

As discussed in 5.2.2, the clock with its synchronous complement will remove the possibility of the error and intermediate state when capturing the state of the D Flip-Flops. To realize the simultaneous clock and its complement, internal conversion by inverter will no longer be used due to the delay from \emptyset to $\overline{\emptyset}$. Instead, a differential trigger system has been set up. As shown in Fig. 27, the RRD and its complement are generated respectively by two identical fast D Flip-Flops, each of which has a reference signal and its complement as an input. Thus, RRD and \overline{RRD} drive the differential fast path delay chain together for simultaneous generation of \emptyset_i and $\overline{\emptyset}_i$.

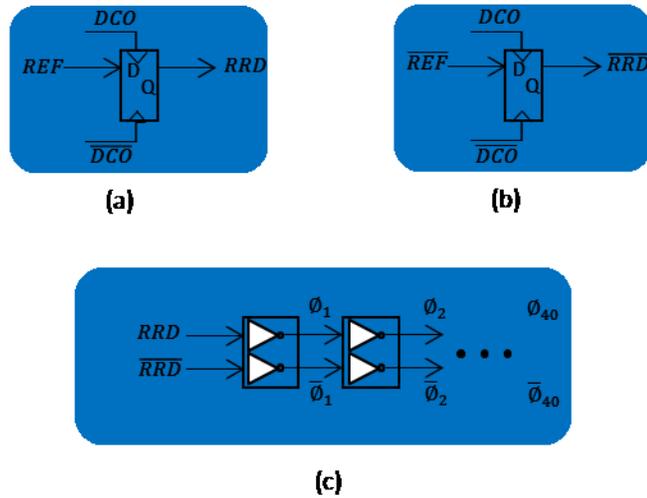
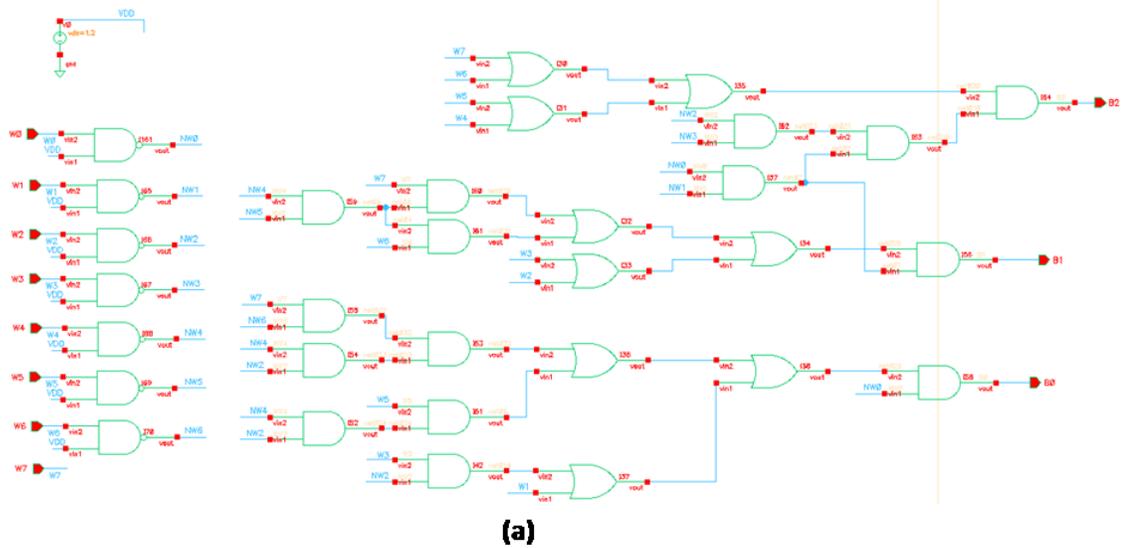


Fig. 27. Differential RRD and differential fast path clock trigger.

5.4 Encoding Circuit

As described in the previous chapter 3.6, a coordinated-determination device is used to distribute 40 outputs into 5 sections sequentially and only one of the 5 sections is useful and valid at any moment, by doing which the encoding operation can be simplified from a 40/6 priority encoder to a 8/3 priority encoder, that will scale down the circuit complexity exponentially. Fig. 28 is a schematic circuit (a) and truth table (b) of an 8/3 priority encoder.



Inputs								Outputs		
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	Y ₂	Y ₁	Y ₀
1	0	0	0	0	0	0	0	0	0	0
x	1	0	0	0	0	0	0	0	0	1
x	x	1	0	0	0	0	0	0	1	0
x	x	x	1	0	0	0	0	0	1	1
x	x	x	x	1	0	0	0	1	0	0
x	x	x	x	x	1	0	0	1	0	1
x	x	x	x	x	x	1	0	1	1	0
x	x	x	x	x	x	x	1	1	1	1

(b)

Fig. 28. (a) 8/3 priority encoding circuit and (b) it's truth table.

Note that using a set of XOR gates to implement the edge finder (Fig. 29) can further simplify the priority encoder.

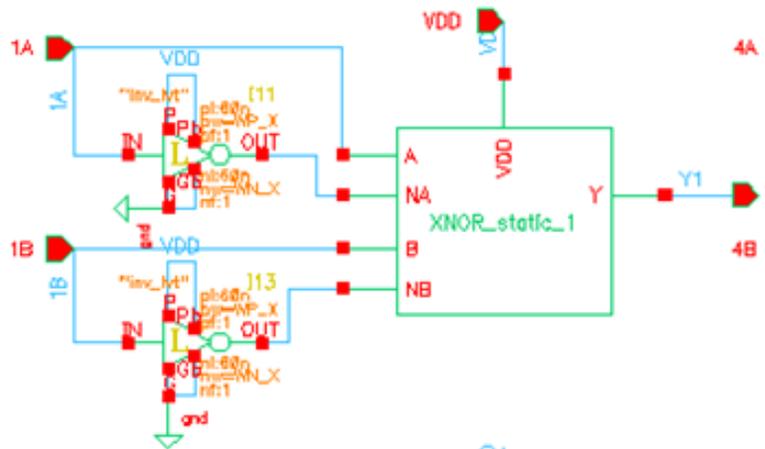


Fig. 29. Circuit diagram of an edge finder consisting of XOR Gates.

5.5 Phase Regulator and Simulation

The circuit structure and their parameters of the slow delay chain, the arbiter array, the fast path delay chains and differential RRD generator have been discussed and determined. In this section the Vernier TDC core will be combined with the phase regulator circuit. As mentioned, the core idea of this research is to employ a phase regulator device to convert the random phase (time) difference into normal-length phase pieces, in this case 80ps long pieces. In the previous chapter a couple of options to realize the phase regulator have been introduced such as a) reuse partially the slow delay chain (Fig. 12), or b) insert an independent ring oscillator in front of the Vernier core circuit (Fig. 13). Here option b) is chosen for the next step for the simulation due to decoupling between the phase regulator circuit and the core circuit being easily attainable.

Fig. 30 illustrates the combined schematic circuit of the phase regulator and the Vernier Core, and in Fig. 31 edge finders and priority encoders are introduced to get the 5 section outputs in 3 bits and one carry out bit.

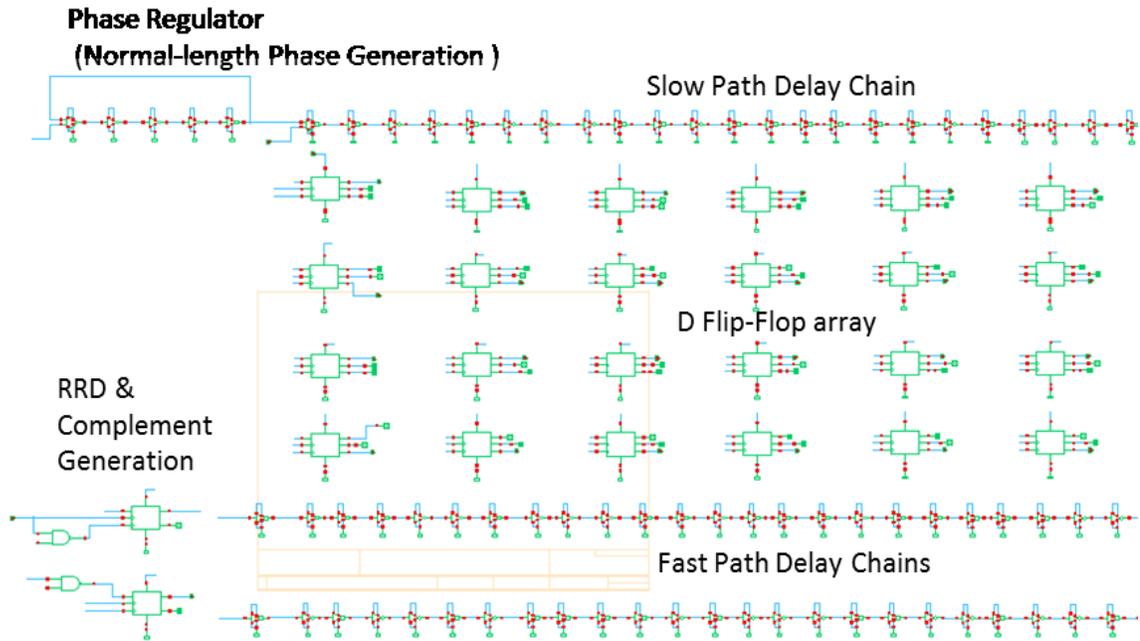


Fig. 30. Vernier core circuit and phase regulator.

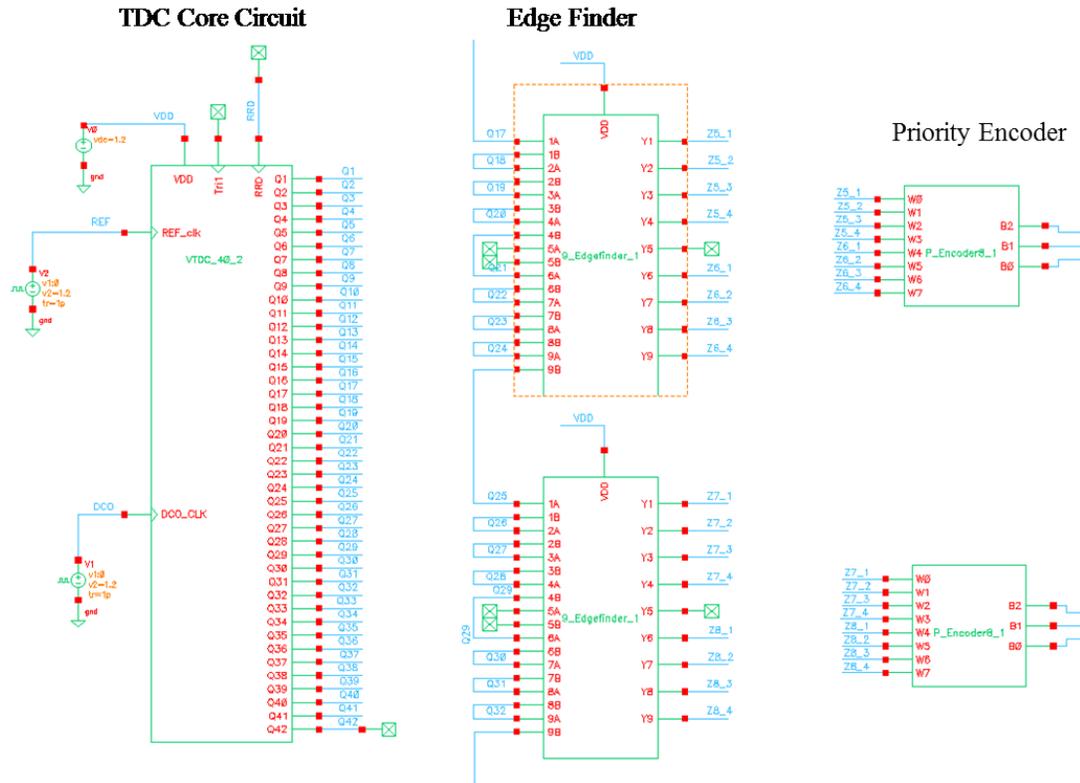


Fig. 31. Diagram of the TDC core and coding output.

Fig. 32 indicates the ideal initial conditions of the simulation which includes the reference signal rising at 30ps and the phase regulator reversing every 80ps. This configuration is to set rotations with an 80ps period. When the DCO comes at any certain time spot, ideally the Vernier TDC core can quantify the last fractional phase piece accurately. However, in practice this is not the case. Fig. 33 shows the simulation of the real waveform of REF and the phase regulator output. Except for the first transition which is driven by REF, all transitions are triggered by the ring-structure feedback. By optimizing the parameters of the ring circuit of the phase regulator, 80ps of the transition period could be achieved (being measured from one middle voltage to the next one)

except the first transition period which is about 86ps. This difference is obviously due to offset between the REF trigger and the ring-structure feedback trigger of the NAND gate. Thus this 6ps (around) difference could be regarded as an offset of phase measurement which can be canceled out later in the final calculation procedure. Alternatively, this offset of phase can be removed by tuning the parameters of the pre-logic timing circuit as discussed in 3.7.

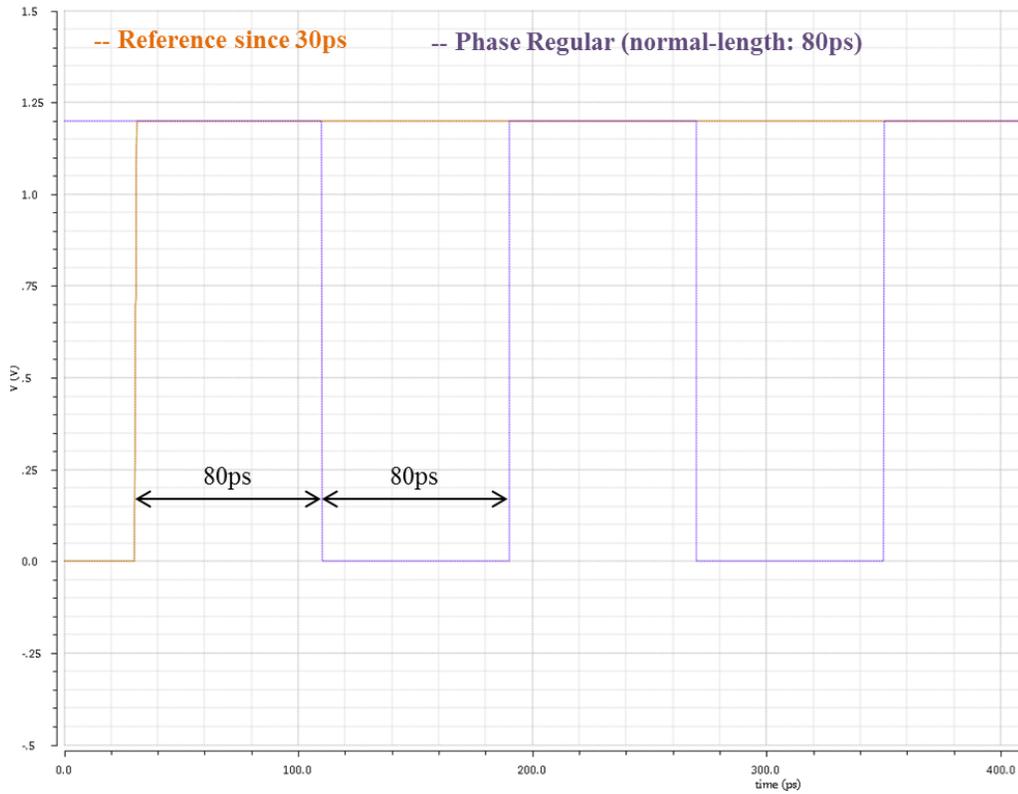


Fig. 32. Ideal Simulation Conditions with REF and Phase Regulator Output.

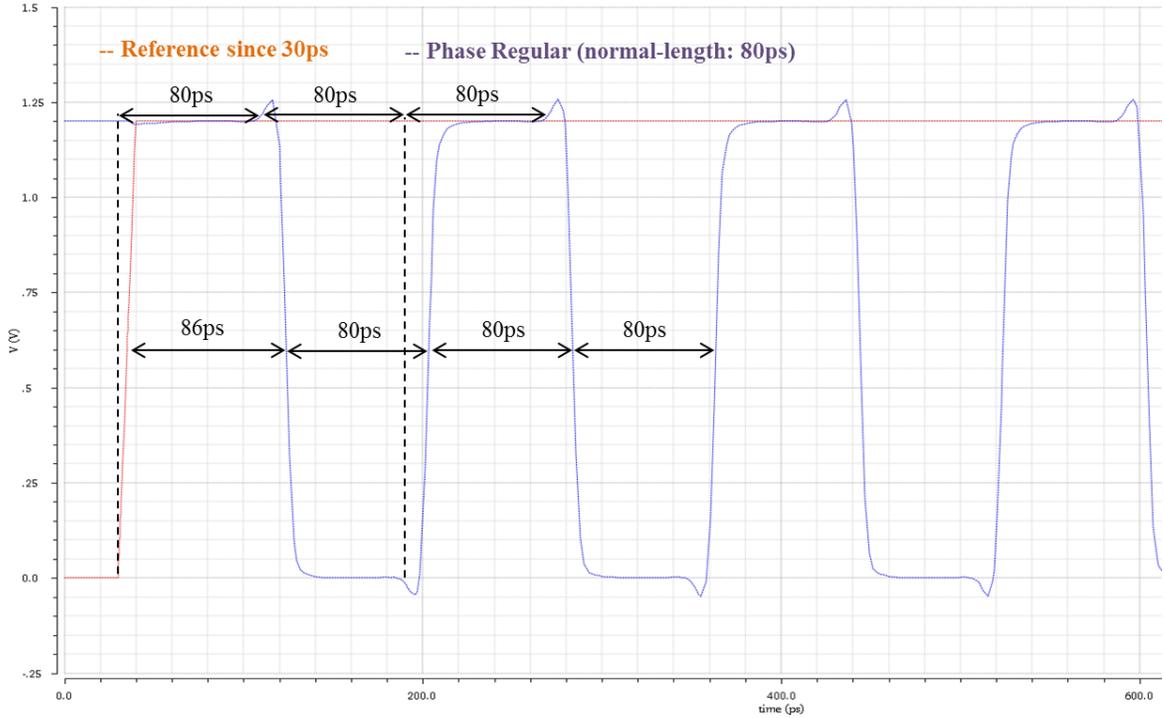


Fig. 33. Real simulation conditions with REF and phase regulator output.

5.6 TDC Core Circuit Simulation Results and Optimization

Now the simulation of the TDC core circuit is complete. In Fig. 34, sweeping the parameter of the DCO arriving time spots covering the second and third rotations ($2 \times 80\text{ps} = 160\text{ps}$) has been performed in the x axis. The result in the y axis shows the output of the 40-stage Vernier core circuit by showing 5 sections with 5 curves respectively and each of them corresponds to eight outputs as shown in Table 7. The two rising ramps (covering from 0 to 39) in the simulation result, present the output in an 80ps range, which illustrates that 40 outputs identify 80ps of phase piece in an almost linear trend. Therefore, the concept and its implementation of the phase-scaled Vernier TDC have been set up and verified.

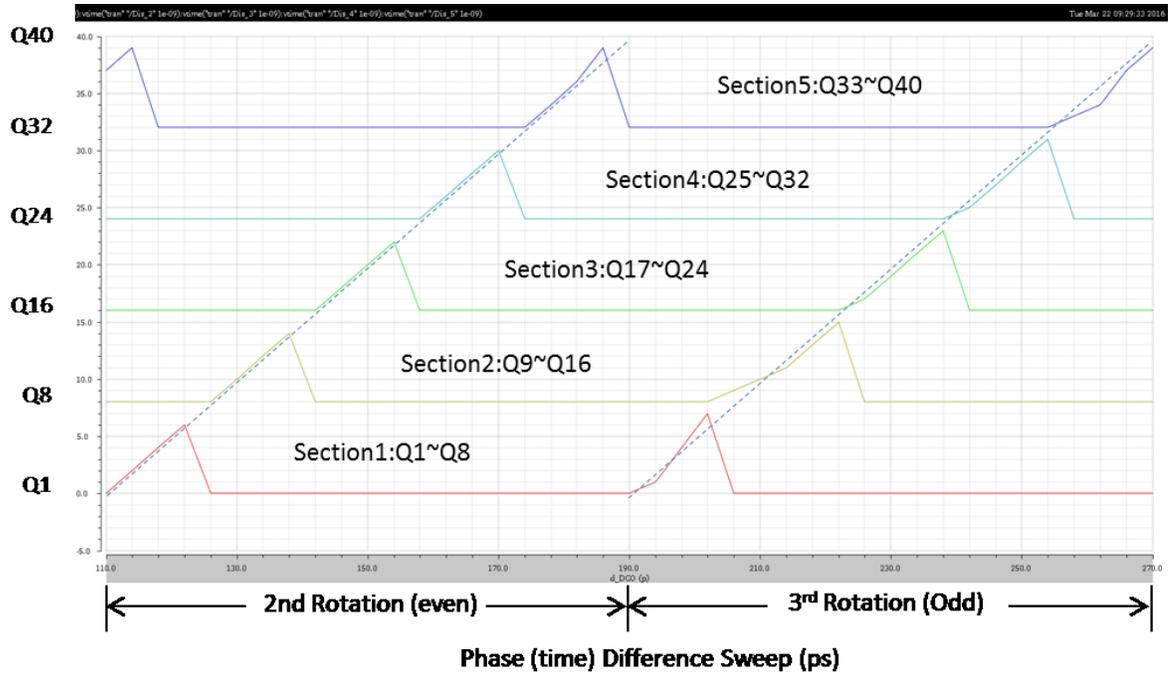


Fig. 34 Vernier core output.

Table 7: Sections, Outputs and Coding Result Index

Distribution	Section 1	Section 2	Section 3	Section 4	Section 5
Node	Q1~Q8	Q9~Q16	Q17~Q24	Q25~Q32	Q33~Q40
Coding Result	0~7	8~15	16~23	24~31	32~39

A zone during the first rotation of the phase regulator deserves special attention, because it is the only rotation triggered by the REF signal rather than the ring-structure feedback signal. As discussed, this will have a 6ps longer than a normal length (80ps) due to phase offset between REF trigger and ring-structure feedback trigger of the NAND gate.

Fig. 35 presents the Vernier Core output changes with different DCO arriving times during the first rotation, i.e. from 0ps to 86ps later than the REF signal edge.

According to the simulation result, it can be separated into 3 regions of the plot:

1. The linear region is from 16ps to 86ps away from the REF edge, which is the region where the circuit is able to indicate the result of the measurement accurately.
2. The offset region is from 0ps to 6ps away from the REF edge. This 6ps offset will be cancelled out in the calculation process.
3. The error zone is from 7ps to 16ps away from the REF edge. This error is due to impact of the meta-stability causing by the edge of the DCO signal being very close to that of REF. Note that the slip issue caused by this meta-stability has been considered and dealt with already as described in Chapter 4.

The operation of the ADPLL system can tolerate this error without significant performance degradation due to the following two reasons:

- The possibility of the occurrence of this error is very low, in addition there could be some way to try to push the DCO edge away from this tiny region or identify this occurrence then avoid counting it.
- The attenuation factor in DLF will almost relieve the impact from this one-time small error.

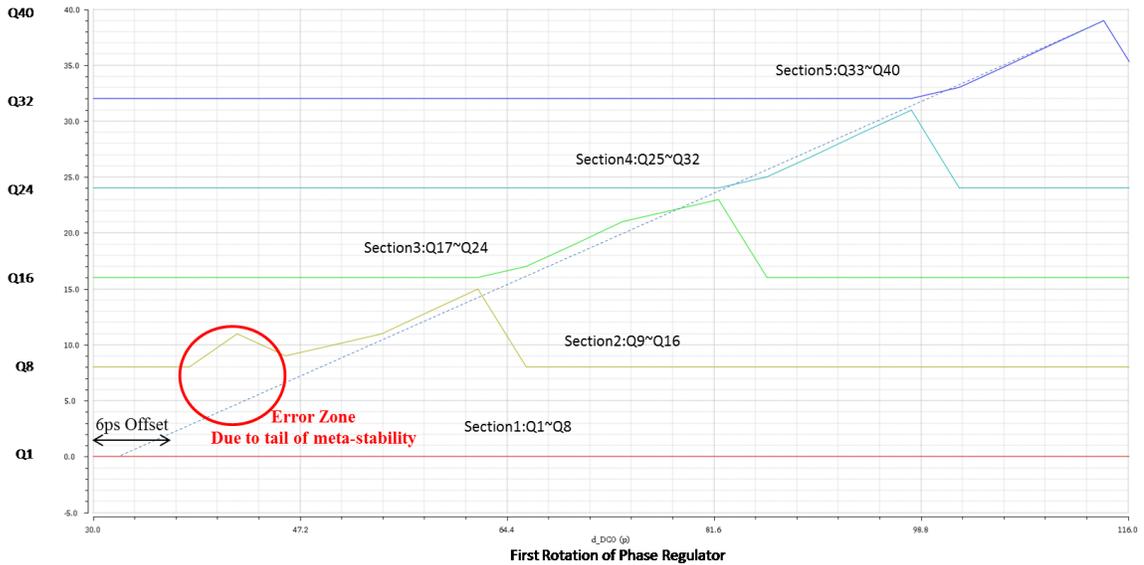


Fig. 35. Vernier Core Output in First Rotation of the Phase Regulator.

Now the implementation of the combination between the phase regulator and Vernier TDC core has been completed and the result of the simulation shows that it works as expected. Only one of 5 sections has non-zero output at any time and the overall trend of the outputs of the 5 sections rises linearly. The next step is the implementation of the evaluator unit which will be designed to achieve the following functions: a) Coordinated-determination device (5-1multiplexer and corresponding determination); b) Odd-even rotation compensations determination; c) Normal-length phase counter determination; d) TDC final output calculation.

5.7 Evaluator Implementation and Simulation

5.7.1 Coordinated-Determination Device

In this section, a part of evaluator called the coordinated-determination device will be discussed and implemented. As discussed in section 3.6, in order to simplify the complexity of the priority encoder from 40/6 bits to 8/3 bits, Q_R should be separated into 5 sections, each of which covers 16ps with 8 outputs (corresponding to the lower 3 bits of the core output, $B<0:2>$) (Fig. 36). The value of the section number is used in a multiplexer to decide which of 5 inputs will become the output; as well this number corresponds to the higher 3 bits of the core output ($B<3:5>$). Fig. 37 shows the logic implementation of the coordinated-determination device. Note that the advantage of the implementation over the initial diagram (Fig. 36) is to use Q_R itself rather than Q_M to determine the multiplexer and the higher 3 bit core output, by taking advantage of the exclusive feature of the active section. The OR gate f_i operation (Fig. 37(b)) is used to distinguish which section is active (non zero).

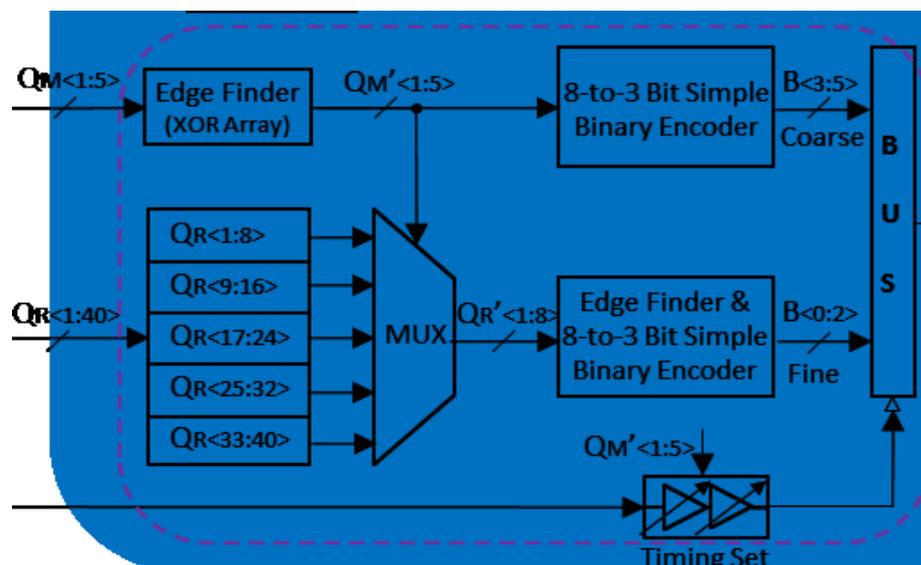
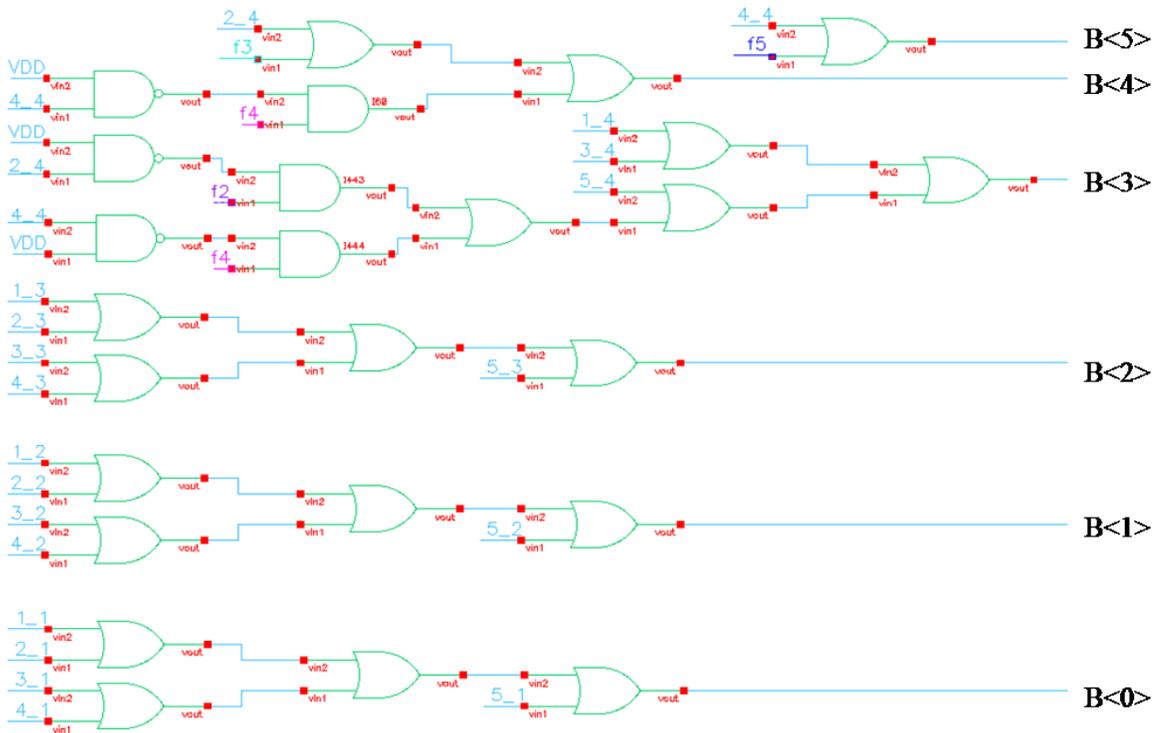
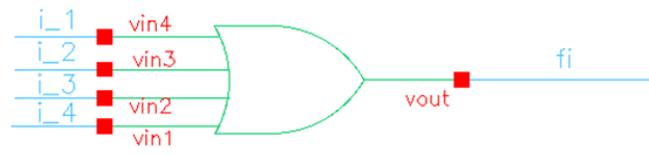


Fig. 36. 8-bit 5-1multiplexer and corresponding determination diagram.



Section4,<1>

(a)



Section i

(b)

Fig. 37. (a) 5-1multiplexer and corresponding determination diagram (b) logic of fi.

5.7.2 Even-rotation Compensation and optimization

In section 3.5, the both-edge triggered counter which is used to record every rotation on the ring oscillator can be optimized to a one-edge (rising) triggered counter which only records every other rotation so that it can loosen the demand on response-

speed of the counter circuitry, as well as to double the phase detection range of the TDC. Therefore, for the updated phase counter, it counts every 160ps instead of 80ps. To implement this advanced solution, as shown in Fig. 15, an even-rotation compensation operation is needed. Then the examples in Table 8 show how the final TDC result could be calculated by taking advantage of the word of the odd/even rotation and the words of normal phase counter. Thus, the evaluator unit should be modified as shown in Fig. 38. The realization of the circuit of the evaluator will follow this version. The word of even rotation compensation will be zero at the odd rotation time period and will be in the high state during even rotation to forward the value of 40 in binary to the final result. Also every time the double-phase counter is triggered, one more “80” will be added into the final result.

Table 8: Examples of Final output calculation

	Example1	Example2	Example3
Core output (0~40)	15	15	15
Original Rotation Number	1	2	6
Odd/Even Rotation (0/1)	0	1	1
Normal Phase Counter (0~255)	0	0	2
Final output	$15+0*40+0*80=15$	$15+1*40+0*80=55$	$15+1*40+2*80=215$
Phase(time) Difference	$2ps*15=30ps$	$2ps*55=110ps$	$2ps*215=430ps$

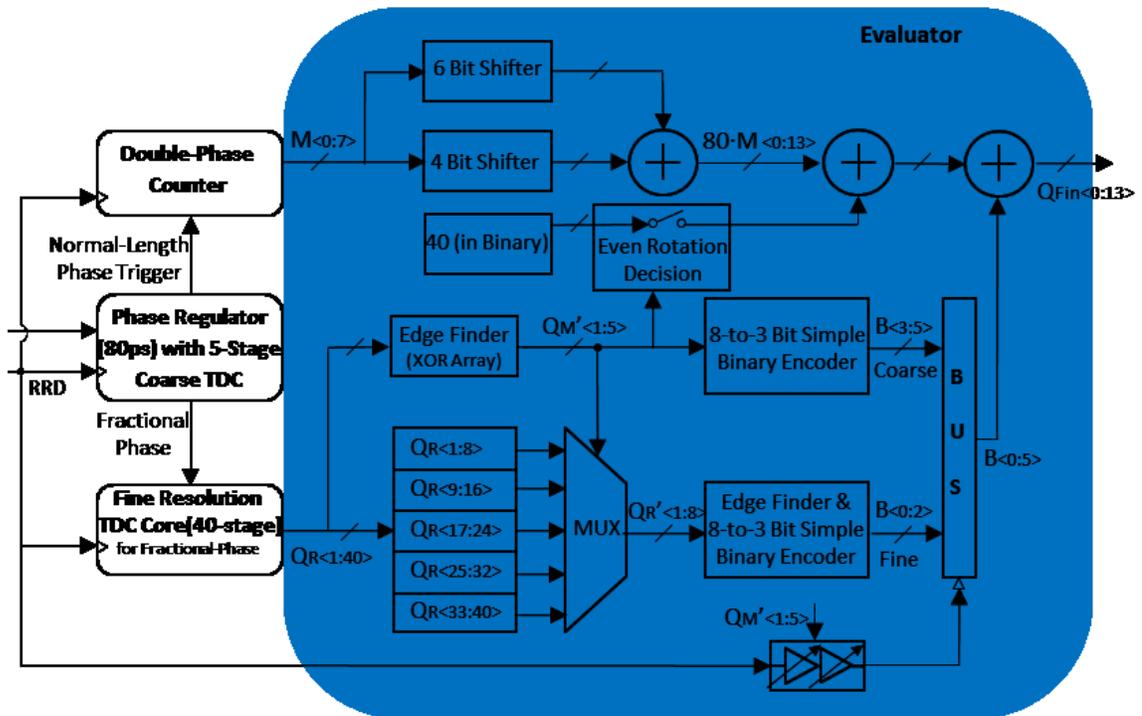


Fig. 38. Diagram of the modified TDC evaluator.

Fig. 39 and Fig. 40 present the simulation result of the final output of the TDC based on the new evaluator solution. The trend of the final output curve is as expected except for two unwanted spurs which happen around the places of the transition between two adjacent rotations. Note that the spurs that happen in Fig. 39 are due to the occurrence of the even rotation word not being aligned in the time domain with that of the TDC core output. Similarly, the spur in Fig. 40 is due to non-alignment in time domain of the double-phase counter, even rotation word and the TDC core output. In other words, ideally the decision of the rotation edge by the phase regulator should happen at the time when the decision of the completion of the fifth section by the Vernier TDC core is made, however practically they are not aligned due to the difference in time delays between the different determination circuits.

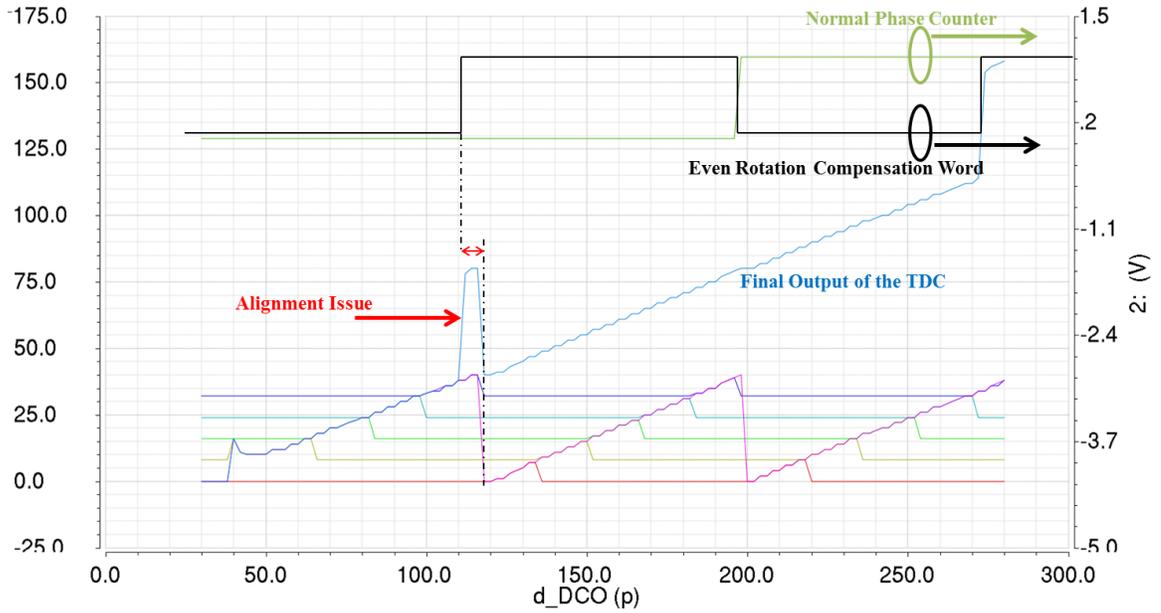


Fig. 39. Simulation of the Final Output of the TDC and the alignment issue.

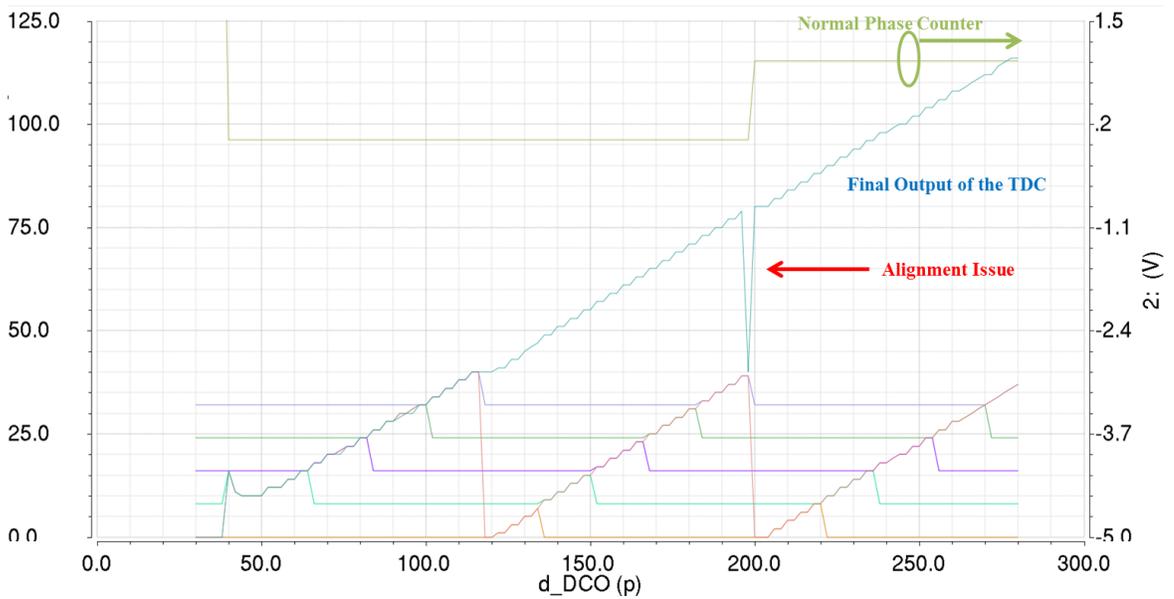


Fig. 40. Simulation of the final output of the TDC and the alignment issue.

One way to tackle the alignment issue is to introduce a logic determination circuit to link the three events and to force their output actions to be simultaneous. Notice that

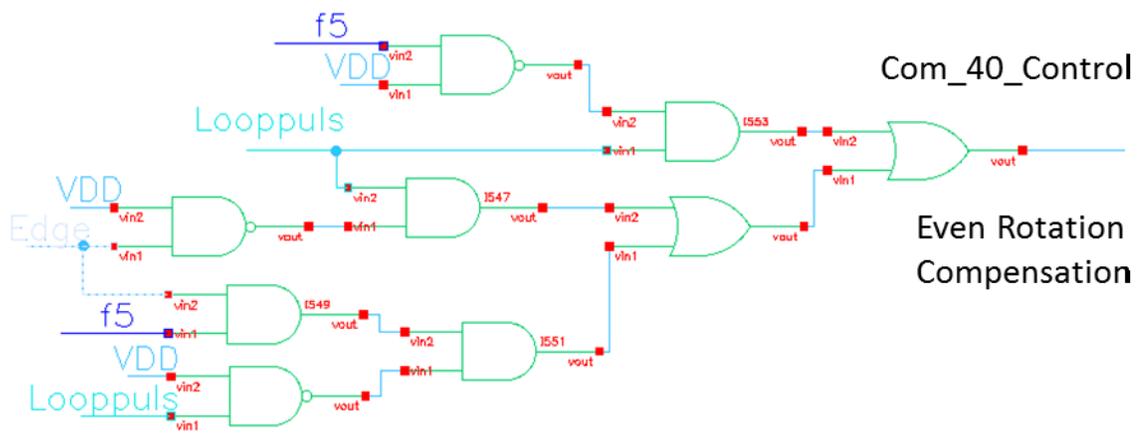
the occurrence of the rotation word is always prior to that of the completion of section 5. Therefore, it sometimes wrongly starts the compensation early. If we can predict this situation, we can avoid the compensation from being added to the output. Therefore, we introduce a couple of detection conditions including: a) if this compensation control word just came 20ps ago (edge word); b) if the Vernier TDC core circuit is experiencing the fifth section and is not completed yet (f5 word). If both these conditions are met, the even compensation word should not to be considered and the output is its complement ($\overline{W_{loop}}$). The truth table of these logical determinations is shown in Table 9. By taking advantage of a Karnaugh map, a sum of products expression can be figured out as:

$$W_{evenrotation} = W_{loop} \cdot \overline{edge} + W_{loop} \cdot \overline{f5} + f5 \cdot edge \cdot \overline{W_{loop}} \quad \text{Eq.(25)}$$

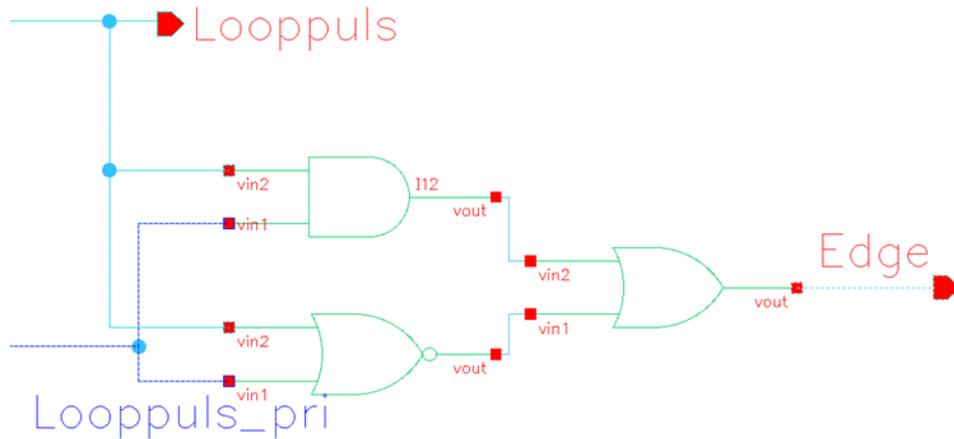
Fig. 41 is the logic implementation of Eq.(25), in which looppuls stands for the W_{loop} .

Table 9: Truth table of updated even rotation word for alignment

Original rotation word, W_{loop}	During Edge zone? ($edge$)	During section 5? (f5) (see Fig. 37(b))	Updated even rotation word, $W_{evenrotation}$
0	0	X	0
1	1	0	1
1	1	1	0
1	0	X	1
0	1	0	0
0	1	1	1



(a)



(b)

Fig. 41. The logic implementation of the alignment between the even rotation word and the core output.

5.8 The Whole TDC Architecture and Simulation

Fig. 42 is the optimized TDC system circuit diagram which includes the Vernier TDC core and phase regulator, the edge finder and priority encoders, the coordinated-determination device (5-1 multiplexer), even-rotation alignment and compensation

device, loop counter alignment and compensation device and final TDC output calculation unit. Fig. 43 illustrates the optimal simulation result in which the final TDC output curve is as expected.

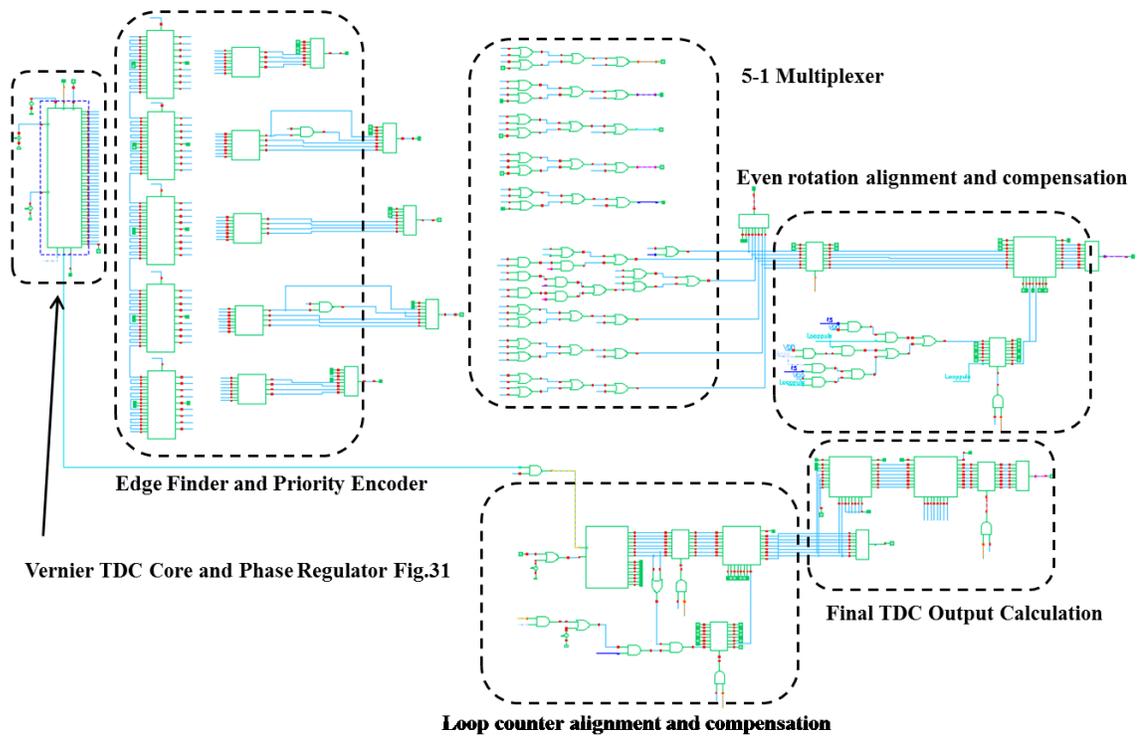


Fig. 42. TDC system block diagram.

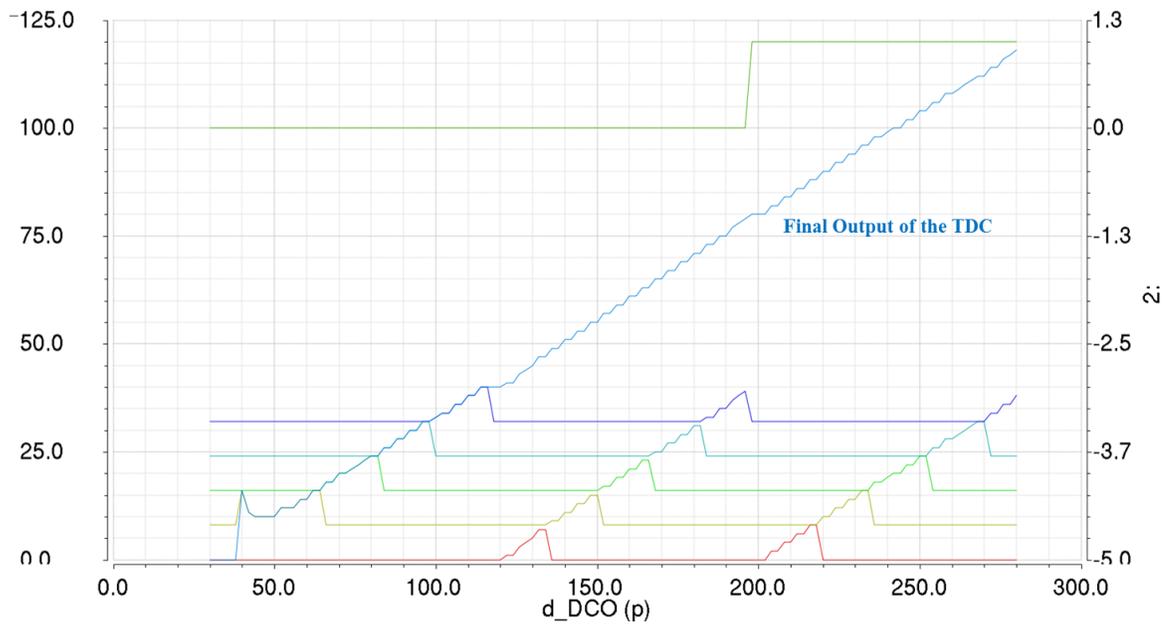


Fig. 43. Final simulation of the final output of the TDC.

Chapter 6: ADPLL System Calculation and Simulation

6.1 ADPLL System Specifications

Based on the future potential requirement of the wireless communication industry, the collaborating company has provided a demanding specification (Fig. 44) of ADPLL performance requirements. In order to achieve this, the ADPLL specification needs to be broken down into a couple of sub-system specifications for the desired TDC, DCO and DLF.

Research topic

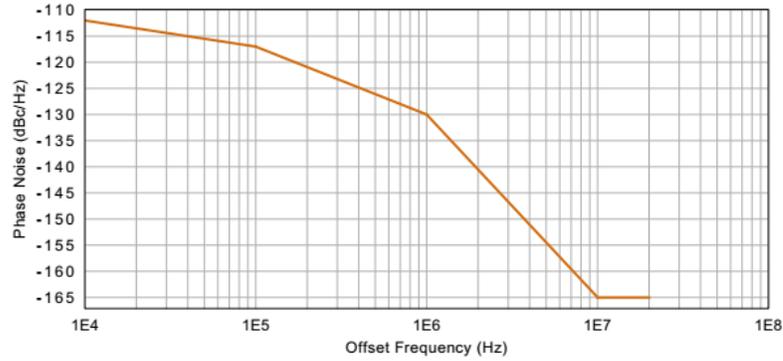
- All digital PLL based on TDC with the following targeted performance
 - Reference frequency: 10-50 MHz
 - Output Carrier frequency: min 3GHz, max 20GHz
 - Tuning range: min 1GHz
 - Phase noise @3GHz carrier frequency:
 - -112dBc/Hz @ 10kHz,
 - -117dBc/Hz @ 100kHz,
 - -130dBc/Hz @ 1MHz,
 - -165dBc/Hz @ 10MHz
 - Max PLL bandwidth: 3MHz
 - RMS jitter: 60fs RMS @ 12kHz to 20MHz, 80fs RMS @ 1kHz to 20MHz
 - Power dissipation: 100mW
 - Factor of Merit: -242dB
 - Area: 1mm²
 - Process: not lower than 55nm

Fig. 44. ADPLL System Specifications.

Fig. 45 shows the conversion from phase noise performance to RMS jitter performance. It shows that the desired phase noise performance can meet 60fs of RMS jitter. However, a common capability of a VCO's phase noise at 10MHz offset is around -155dBc/Hz for high frequency (>10GHz) applications. A reasonable thermal noise floor is -165dBc/Hz. Secondly, note that the difference between 1MHz offset and 10MHz offset is 30dB, exceeding the typical value of -20dB/decade slope for phase noise.

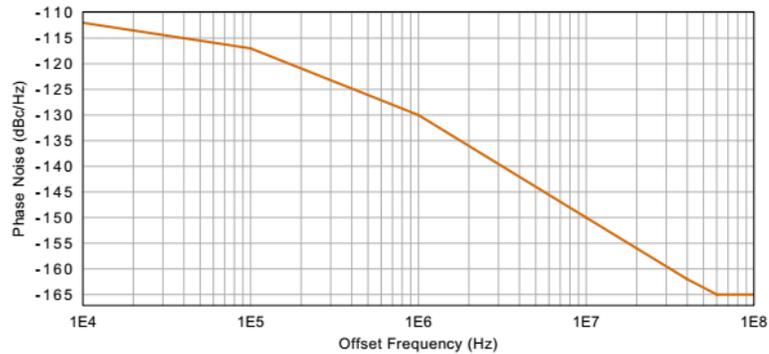
Therefore, the phase noise performance has been modified to $-150\text{dBc/Hz}@10\text{MHz}$ offset and -165dBc/Hz for the noise floor. Fig. 46 updates the contrast between phase noise and RMS jitter performances and it turns out that RMS phase Jitter is worse at 63fs.

Phase Noise & RMS Jitter @ 3GHz



Clock Frequency = 3 000 000 000 Hz				
#	Offset Frequency (Hz)	Phase Noise (dBc/Hz)		Phase Jitter per Segment (ps RMS)
1	10000	-112		
2	100000	-117	>>>	3.919e-02
3	1000000	-130	>>>	4.321e-02
4	10000000	-165	>>>	1.498e-02
5	20000000	-165	>>>	1.330e-03
Total phase jitter = 0.06024 ps RMS				

Fig. 45. Original Phase noise & RMS jitter conversion of the ADPLL



Clock Frequency = 3 000 000 000 Hz				
#	Offset Frequency (Hz)	Phase Noise (dBc/Hz)		Phase Jitter per Segment (ps RMS)
1	10000	-112		
2	100000	-117	>>>	3.919e-02
3	1000000	-130	>>>	4.321e-02
4	10000000	-150	>>>	2.251e-02
5	20000000	-156	>>>	5.310e-03
6	40000000	-162	>>>	3.760e-03
7	60000000	-165	>>>	2.240e-03
8	100000000	-165	>>>	2.670e-03
Total phase jitter = 0.06296 ps RMS				

Fig. 46. Updated Phase noise & RMS jitter conversion of the ADPLL

6.2 Phase Noise Contribution and Distribution

The total phase noise is contributed by the raw VCO noise, TDC time resolution noise and DCO quantization noise (Eq.(26)).

$$PN_{\text{Total}} = \text{Noise}_{\text{rawVCO}} + \text{Noise}_{\text{TDC_Resolution}} + \text{Noise}_{\text{DCO_Quantization}} \quad \text{Eq.(26)}$$

In general, the TDC noise is supposed to be equal to VCO noise at the corner frequency. The TDC noise is flat in-band and rolls off at 20dB/decade out of band. The noise of VCO in-band has an extra suppression which relies on the type of DLF employed. Fig. 47 shows the contribution of the various elements at various frequency offsets and the total phase noise that can be achieved by integrating all of them. If we work this calculation backwards, it can guide us to a distribution of the phase noise of each element by knowing the system phase noise performance.



Fig. 47. ADPLL phase noise contribution and distribution.

In order to achieve the above specifications, the following guidelines will be fulfilled:

- Ensure raw VCO phase noise between 0.1 MHz and 20MHz (out of band) at least 3dB better than the overall phase noise due to the lack of out of band suppression of the loop filter to raw VCO phase noise (High pass filter characteristic).

- Needs sufficiently fine DCO frequency resolution (Δf_{res}) to make quantization-noise appreciably smaller than the VCO's raw phase noise in the out of band region, to make it a negligible contribution. The expression of DCO quantization phase noise contribution to the system is:

$$L\{\Delta f\} = \frac{1}{12} \left(\frac{\Delta f_{res}}{\Delta f} \right)^2 \frac{1}{f_R} \quad \text{Eq.(27)}$$

- Ensure in band DCO quantization phase noise is 3dB better than the overall phase noise (-112dB), according the equation below:

$$L_{DCO-IN} = \frac{(2\pi)^2}{12} \left(\frac{\Delta f_{res}}{f_R} \right)^2 \frac{1}{f_R} \frac{1}{\alpha^2} \quad \text{Eq.(28)}$$

- Ensure the in band TDC resolution phase noise is 3dB better than the overall phase noise (-112dB), according the equation below:

$$L_{TDC-IN} = \frac{(2\pi)^2}{12} \left(\frac{\Delta t_{res}}{T_{DCO}} \right)^2 \frac{1}{f_R} \quad \text{Eq.(29)}$$

- For optimal in-band phase noise performance, a second-order DLF is needed to reduce the impact of the raw VCO phase noise contribution in band due to nearly 40dB/decade of suppression from the corner frequency to DC of the VCO noise by the loop filter.
- The optimal values for Alpha and Rho aiming at achieving the proper loop bandwidth must be determined so that the phase noise of the TDC is equal to the phase noise of the DCO in-band.

Fig. 48 illustrates an ADPLL performance calculation and analysis in which the performance of an ADPLL can be determined by inputting the required parameters and specifications. The yellow-filled elements stand for the desired input parameters. Some of the green-filled elements are the performance specifications that an ADPLL can achieve, the others are the requirements which need to be realized in the implementation such as Alpha and Rho. According to the calculator a 2ps time resolution for the TDC can meet the system phase noise performance requirement as long as the DCO resolution can meet the 1kHz requirement. Fig. 48 also indicates the requirement of the VCO and Alpha Rho values, etc.

PLL Frequency performance Calculation							
Fref	FDCO	Wn	Damping factor	Alpha	Rho	TDC Resolution	DCO resolution
MHz	GHz	MHz	non	non	non	ps	kHz
50	2.5	0.1	0.7	0.0028	0.000004	2	1
Period(ns)	Period(ps)			2 ⁻⁸	2 ⁻¹⁷		
20	400						
DCO WF Dithingwordlength		DCO WI wordlength		DCO rough range wordlength	DCO freq fine-tuning range		DCO freq whole tuning range
6		18		4	16.777216 GHz		268.435456
In-band TDC PN							
-117.839 dBc/Hz							
DCO phase noise of quatization							
-114.74 dBc/Hz		in-band					
-127.782 dBc/Hz		0.1 MHz offset					
-147.782 dBc/Hz		1 MHz offset					
-167.782 dBc/Hz		10 MHz offset					
-187.782 dBc/Hz		100 MHz offset					
RAW VCO Noise							
Q factor of VCO	Power of Carrier	Niose Factor of Osc	Noise Floor	Freq Offset	RAW VCO Noise		
	dBm		dBc/Hz	kHz	dBc/Hz		
15	0	1	-165	100	-118.4529714		
RAW VCO Noise			Slope of Curve				
-155			10 MHz offset		20 dB/Decade		

Fig. 48. ADPLL phase noise calculator and analyzer.

6.3 ADPLL System Modeling and Simulation in Simulink

Building up a Simulink simulation platform is necessary and important in order to estimate and evaluate a certain type of TDC and to verify the performance of a certain TDC and/or PLL. In addition, it is an effective and efficient way to improve the performance of a PLL or a TDC.

Fig. 49 shows a diagram of a basic integer PLL system operation platform. Fig. 50 indicates that the control voltage of the DCO is working as expected. This simulation structure will be improved and refined step by step to a type II all digital PLL.

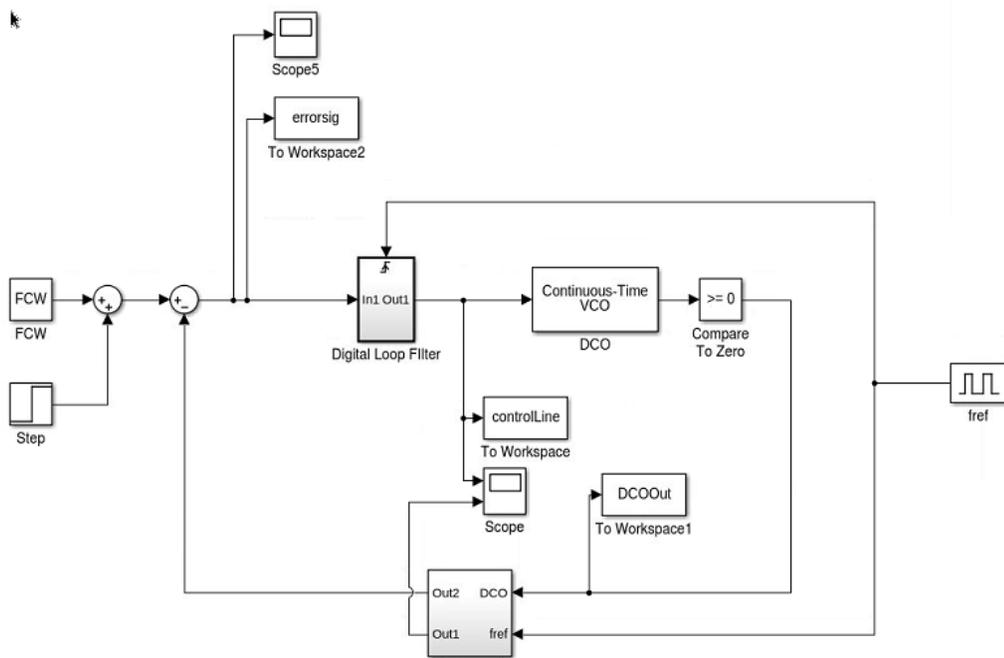


Fig. 49. Basic integer PLL system simulation platform.

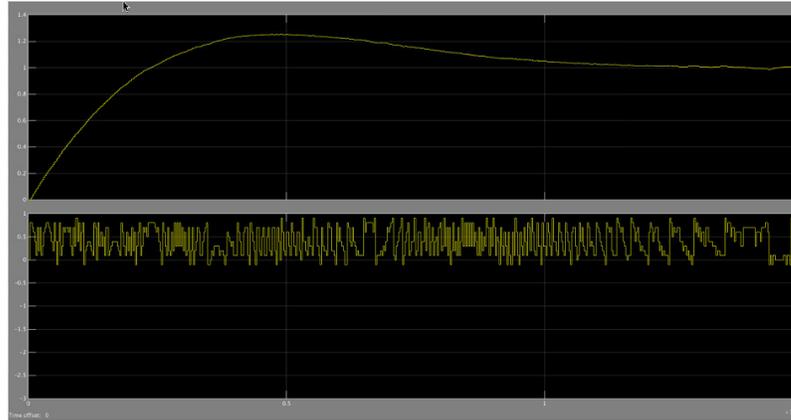


Fig. 50. ADPLL control voltage convergence with time.

Fig. 51 shows a diagram of a PLL system in which a TDC unit and a type I digital filter have been employed based on the basic PLL structure. Fig. 52 illustrates a type II ADPLL with a second pole achieving better noise rejection in band (a further 20dB/decade) compared to the type I counterpart. In addition, a type II filter removes flicker noise and VCO noise. Another advantage of the type II loop is that it removes steady-state frequency error.

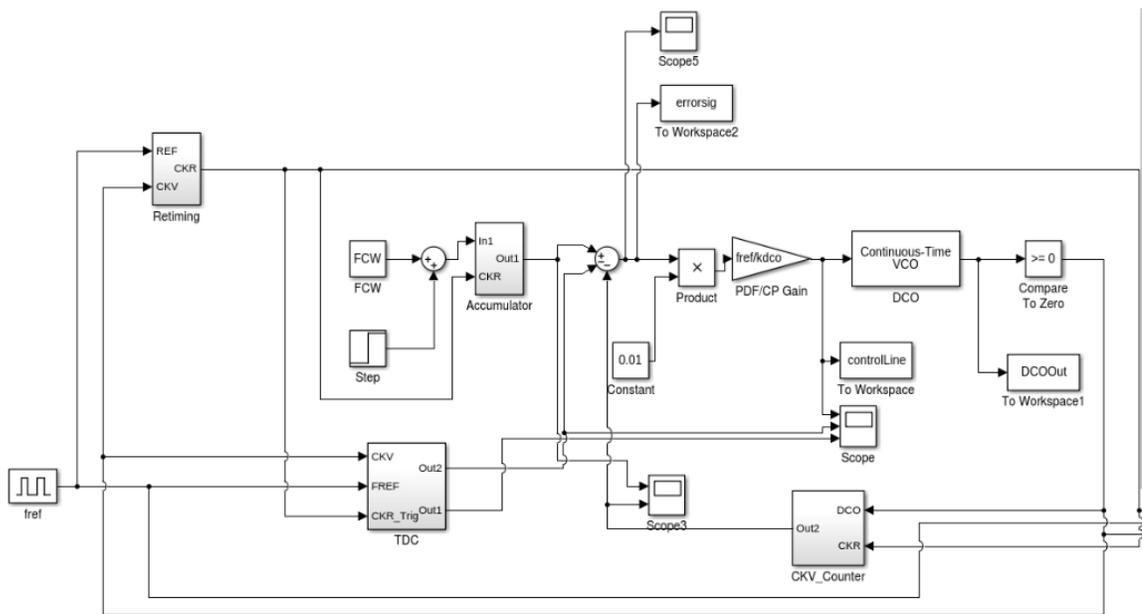


Table 10 summarizes the advantages and disadvantages of type I and type II ADPLLs. We will discuss in the next section the preferred mode of the operation of an ADPLL based on the conclusions from this table.

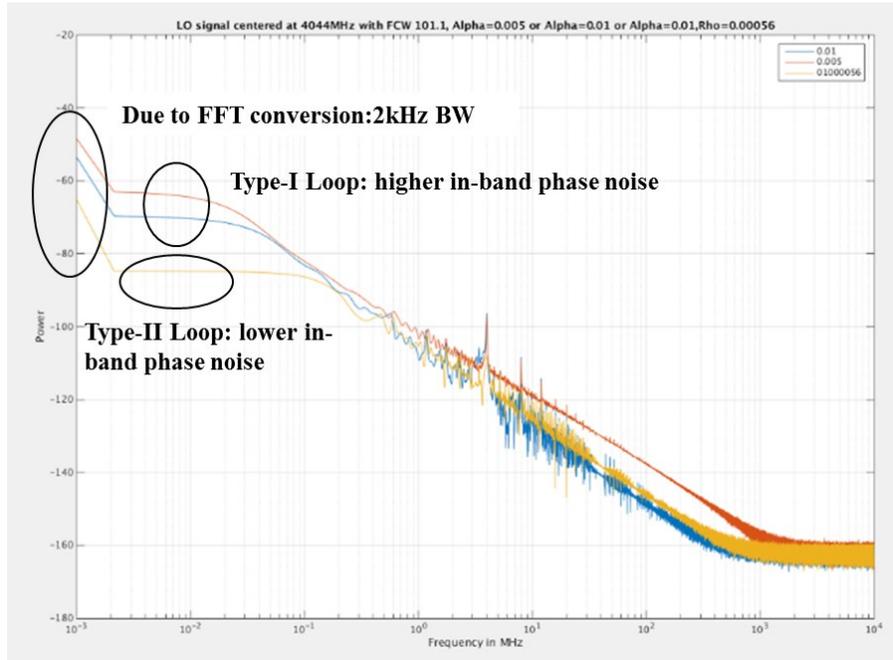


Fig. 53. ADPLL phase noise comparison between different loop parameters.

Table 10: Type I and type II loop feature contrast

	Type I Loop [20]	Type II Loop
Advantage	Fast frequency/phase acquisition	No frequency/phase error Better phase noise performance
Disadvantage	Steady-state frequency error Poor in-band phase noise	Slow due to ripple of control word of DCO

6.5 Preferred Solution of ADPLL System Operation

According to the analysis of the different types of ADPLLs in section 6.4, it is obvious to conclude that a combination of type I and type II ADPLL loop operation is the optimal solution to achieve better phase noise performance as well as reasonable acquisition time. Specifically, the operation of an ADPLL can be separated into three periods:

1. Acquisition mode period: Use a type I with high gain for fast acquisition. It requires a wide loop bandwidth.
2. Tracking mode period: Use a Type I with low gain for tracking. It requires a narrow bandwidth.
3. Performance mode period: Use a Type II with Proportional-integral controller for the best phase noise performance.

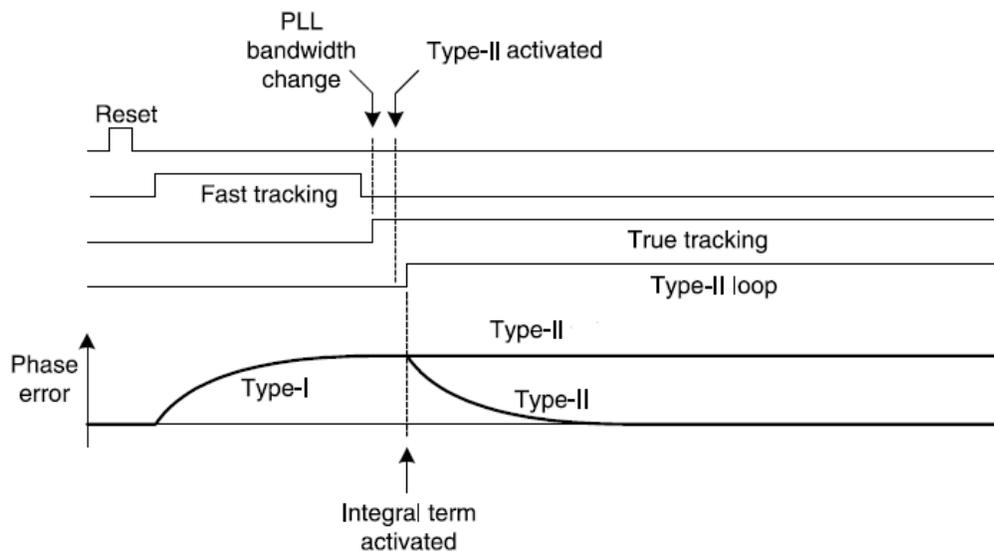


Fig. 54. ADPLL operation with combination of type I and type II. [1]

Table 11: Type I and type II loop feature contrast

	Alpha	Rho	Note
Acquisition mode	Large (0.1)	0	Type I Loop
Tracking mode	Small (0.01)	0	Type I Loop
Performance mode period	Small (0.01)	Non zero Rho	Type II Loop

Chapter 7: Conclusion and Future Work

7.1 Completed Work

Much research has been done including: TDC architecture & technologies evaluation (Chapter2), TDC architecture analysis and design (Chapters 3 and 4), TDC implementation, simulation and optimization (Chapter 5), and ADPLL system specification analysis & distribution down-to the TDC sub-block level (Chapter 6). This research has verified that:

- The proposed TDC architecture is able to meet the specifications from the ADPLL requirement (by system behavior level simulation, Simulink).
- The proposed TDC architecture has advantages in terms of high performance, low power consumption and small chip area over the other solutions.
- The proposed TDC is capable of being implemented in the physical level (Virtuoso schematic) and the characteristics are as good as expected after optimization.

7.2 Future Work

From the perspective of the end-to-end process of a chip, a real implementation should be fabricated, so that a physical chip can be measured and evaluated to verify its functionality. While some of the preliminary work and simulation for this has been done it is far from complete. Therefore, future work should include the physical implementation part, system verification and optimization. Specifically, a layout and tape-out of a chip should be done, as well as measurements performed. In addition, a circuit level ADPLL simulation platform it would better to set up for virtual verification

due to the TDC being part of an ADPLL system. Also from the simulation result shown in section 5.8 the linearity of the TDC output has room for optimization, as well as differential D Flip-Flop circuits for higher time accuracy.

7.3 Contributions and Conclusions

The phase-scaled Vernier TDC design and results were submitted to and approved by the Microsemi Patent Council in March 2016. The corresponding paper is holding for submission now and it will be sent out once the patent file number has been received from US Patent and Trademark Office.

The phase-scaled Vernier TDC achieves comparable time resolution and phase detection range performances to the Vernier Ring TDC, but a few times better in core circuit power consumption, phase noise performance due to higher frequency of the applied reference clock. The TDC time resolution performance can be improved at expense of circuit scale and power consumptions.

References

- [1] R. B. Staszekwski, P.T. Balsara, *All-Digital Frequency Synthesizer in Deep-Submicron CMOS*, Wiley, 2006.
- [2] B. Wang, Y. H. Liu, P. Harpe, J. Heuvel, B. Liu, H. Gao, R. B. Staszewski, "A Digital to Time Converter with Fully Digital Calibration Scheme for Ultra-Low Power ADPLL in 40 nm CMOS", *ISCAS*, pp. 2289-2262, 2010.
- [3] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuit*, Cambridge University Press, Cambridge, first published 1998.
- [4] J. W. M. Rogers, C. Plett, I. Marsland, *Radio Frequency System architecture and design*, Artech House, 2013, ch. 4-6, pp. 129-262.
- [5] B. Razavi, *Phase-Locking in High-Performance Systems: From Device to Architectures*, Wiley-IEEE Press, 2013.
- [6] S. Henzler, *Time-to-Digital Converter*, Springer, 2009.
- [7] W. Altabban, P. Desgreys, "Merged Digitally Controlled Oscillator and Time to Digital Converter for TV band ADPLL," *International Symposium on Circuits and Systems*, pp. 1987-1990, 2010.
- [8] M. Z. Straayer, M. H. Perrott, "An efficient high-resolution 11-bit noise-shaping multipath gated ring oscillator TDC," *Digest of the International Symposium on VLSI Circuits*, pp. 82-83, Jun. 2008.

- [9] P. Dudek, S. Szczepanski, J.V. Hatfield, "A high-resolution CMOS time-to-digital converter utilizing a Vernier delay line" *IEEE J. Solid-state Circuit*, vol. 35, no. 2, pp 240-247, Feb. 2000.
- [10] L. Vercesi, A. Liscidini, R. Castello, "Two-Dimensions Vernier Time-to-Digital Converter" *IEEE J. Solid-state Circuit*, vol. 45, no. 8, pp 1504-1512, Aug. 2010.
- [11] R. B. Staszewski, C. M. Hung, K. Maggio, J. Wallberg, D. Leipold, and P. T. Balsara, "All-digital phase-domain TX frequency synthesizer for blue tooth radios in 0.13um CMOS," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, ol. 1, pp. 272-527, Feb. 2004.
- [12] R. B. Staszewski, S. Vemulapalli, P. Vallur, J. Wallerg, P. T. Balsara, "1.3v 20ps Time-to-digital Converter for Frequency Synthesis in 90-nm CMOS" *IEEE Tran.on Circuits and Systems II express briefs*, vol. 53, no. 3, pp 220-224, March 2006.
- [13] J. Yu, F. F. Dai, R. C. Jaeger, "A 12-Bit Vernier Ring Time-to-Digital Converter in 0.13um CMOS Technology" *IEEE J. Solid-state Circuit*, vol. 45, no. 4, pp 830-842, Apr. 2010.
- [14] P. Lu, A. Liscidini, P. Andreani, "A 3.6mW 90nm CMOS Gated-Vernier Time-to-Digital Converter with an Equivalent Resolution of 3.2ps" *IEEE J. Solid-state Circuit*, vol. 47, no. 7, pp 1626-1635, July 2012.
- [15] M. Lee and A. A. Abidi, "A 9b, 1.25ps resolution coarse-fine time-to-digital converter in 90nm CMOS that amplifies a time residue," *Digest of the International Symposium on VLSI Circuits*, pp.168-169, Jun. 2007.

- [16] A. Samarah, A. C. Carusone, "A Digital Phase-Locked Loop With Calibrated Coarse and Stochastic Fine TDC," *IEEE J. Solid-state Circuit*, pp.1829-1841, 2013.
- [17] J. M. Rabaey, A. Chandrakasan, B. Nikolic, *Digital Integrated Circuit*, Pearson, 2011.
- [18] N. H. E. Weste, D. M. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, Pearson, 2011.
- [19] Roland E. Best, *Phase-Locked Loops: Design, Simulation and Applications*, McGraw-Hill, 2003.
- [20] J. Shen, F. Jonsson, J. Chen, H. Tenhunen, L. Zheng "Phase noise improvement and noise modeling of type-I ADPLL with non-linear quantization effects," *NORCHIP*, pp.1-4, 2014.