Optimal Pin-Assignment for Signal Integrity Optimization in IC Packages and Connectors

by

Lihong Zhang

A thesis submitted to the Faculty of Graduate Studies and Research
in partial fulfillment of the requirements for the degree of
Master of Engineering

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**Optimal Pin-Assignment for Signal Integrity Optimization in IC
Packages and Connectors**

submitted by Lihong Zhang
in partial fulfillment of the requirements for
the degree of Master of Engineering

Q.J. Zhang, Thesis Supervisor
J. Wight, Chair, Department of Electronics

Abstract

With the rapid increase in operating frequency in today's VLSI systems, signal integrity due to VLSI packages and interconnects becomes one of the critical factors in the overall design. This thesis addresses the signal integrity based pin-assignment optimization of packages and connectors by using simulated annealing and genetic algorithms. A genetic algorithm capable of handling 1- and 2-dimensional crossover is developed to accommodate 2-dimensional pin-assignment required in the connector case. A new and simple algebraic model for fast approximation of crosstalk and ground noise is proposed which is suitable for highly repetitive use in optimization. A worst case formulation to predict the worst possible signal integrity problem under various source excitations is developed based on two types of models: an approximate algebraic model and a detailed integration model. Six examples are presented for ground noise and crosstalk minimization using 1- and 2-dimensional pin-assignment optimization techniques, verifying the proposed approach and demonstrating the effect of signal integrity improvement in package and connector design.

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List of Symbols

$\mathbf{x}$	pin-assignment pattern
N	number of pins
N_{row}	number of rows of pins
N_{col}	number of columns of pins
N_s	number of signal sources
N_g	number of grounds
N_d	number of differential sources
N_a	number of absolute sources
$\#(m, n)$	pin at row $\#m$ and column $\#n$
$\mathbf{L}$	inductance matrix
$\mathbf{E}$	source signal
$\dot{\mathbf{E}}$	rate of change of the source signal
E_p	the p th source signal
V_g	ground noise
$V_{crosstalk}$	crosstalk
R_L	load resistance
R_S	source resistance
V_{mn}	voltage across the pin at row $\#m$ and column $\#n$

x

V_A	vector including the voltages across ground pins
V_B	vector including the voltages across source pins
I	current of source signal
$\dot{I}$	rate of change of the current of source signal
$\dot{I}_A$	vector including the di/dt of all ground pins
$\dot{I}_B$	vector including the di/dt of source pins
$\dot{I}_\Sigma$	total di/dt for all ground pins
$\dot{E}_{max}$	the maximum rate of the change of the input signal
t_r	rise time of the signal
h	time step in Backward Euler simulation
C	matrix representing the inductive elements
G	matrix representing the non-inductive elements
X	variable vector in Backward Euler
$F(x)$	objective function for the pin-assignment x
w_1, w_2	weighting factors
$f(x^i)$	fitness for chromosome x^i
a, b	coefficients for fitness scaling

Chapter 1

Introduction

1.1 Motivation of the Research Work

With the rapid increase in operating frequency of today's VLSI systems, signal integrity due to VLSI packages and interconnects becomes one of the critical factors in the overall design[1]. As part of the signal integrity problem of an electronics system, signal integrity due to connector design has recently received attention from the industry, e.g., [2][3]. Improperly designed packages and connectors lead to signal integrity degradations such as increased crosstalk and ground noise, limiting high-speed system performance[4].

Ground noise is an important aspect of signal integrity in IC packages, and has been a subject of significant research in recent years. Many papers in the literature have addressed the electrical modeling, e.g., [5][6][7], and measurement, e.g., [8] of ground noise in IC packages. Accurate and efficient estimation of ground noise has been one of the important issues, e.g., the use of 3-D characterization techniques for inductance extraction[9][10][11], and macromodeling techniques[12] for improved speed in modeling computation. Crosstalk occurs due to coupling between pins in

packages and connectors. Methods for modeling and simulation of crosstalk in coupled multiconductor transmission lines have been developed, e.g., [13][14][15]. Crosstalk is also an important signal integrity issue due to the increased signal speed and large number of signal pins in packages and connectors[16]. In [17], factors that affect ground noise and crosstalk in IC packages, and guidelines for package design are discussed. The method in [18] shows how ground planes in IC packaging should be connected to the IC ground in order to make the ground plane current density uniform and thereby minimize ground noise. In [19], an automatic optimization approach using simulated annealing is developed to minimize ground noise through optimal pin-assignment. It demonstrates that significant reduction in ground noise is possible beyond physical/geometrical considerations in package design.

Since the coupling between connector pins can occur in 2 dimensions, the existing 1-dimensional formulation of pin-assignment optimization, e.g., [19] is not adequate. Since pin-assignment in packages and connectors has an impact on both the ground noise and crosstalk, optimizing one aspect of the signal integrity may adversely affect other aspects. Therefore a pin-assignment algorithm including simultaneous ground noise and crosstalk optimization is necessary. The problem is further complicated by the fact that the magnitude of crosstalk is dependent not only on pin-assignment, but also on the source excitation patterns. Since the number of signal pins in real operation is usually large, and since each signal can be either high or low, there exists a large number of different source excitation patterns. For example, for 100 signal pins, there are $2^{100} = 1.27 \times 10^{30}$ excitation patterns leading to 1.27×10^{30} different crosstalk situations. Crosstalk estimation through exhaustive analysis is extremely computation intensive. The problem becomes even more challenging when ground noise and crosstalk estimation is embedded into an automatic optimization

process requiring highly repetitive simulations with different pin assignments. The pin-assignment problem has a large number of local optimum which can trap the optimization procedure and produce solutions far from the global optima. The use of efficient optimization algorithms becomes very critical. These challenges have not been adequately addressed in the existing literature.

1.2 Objective of the Thesis

The objective of this thesis is to develop an automatic optimization approach applicable to both 1- and 2-dimensional pin-assignment optimization in IC packages and connectors. The technique is formulated to allow ground noise, crosstalk or both to be the optimization objective.

First, a fast modeling method is needed allowing both crosstalk and ground noise to be concurrently evaluated from a common pin-assignment and a common set of matrix equations. An approach to evaluate the worst case crosstalk under different source excitation patterns is necessary, which must be much faster than the exhaustive search method since it will be used iteratively in optimization. Two worst case algorithms, one formulated with the fast algebraic model, the other formulated with the detailed integration-based circuit simulation model, will be derived.

Second, optimization approaches, based on two types of global optimization algorithms, i.e., Simulated Annealing(SA) and Genetic Algorithm(GA), will be investigated. The incorporation of these optimization algorithms into the pin-assignment framework will be studied. Pins in connectors are usually arranged in 2-dimensions and crosstalk is affected by couplings in both dimensions. The overall pin-assignment needs to consider both dimensions concurrently. We need to expand the 1-dimensional

Partially Matched Crossover(PMX) technique in GA to 2-dimensional PMX in order to handle the connector case.

Finally the effectiveness of the proposed methods are confirmed by examples.

1.3 Outline of the Thesis

This thesis is organized as follows.

In Chapter 2, a review of the literature is presented. This includes a review of signal integrity of IC packages and interconnects, a review of the worst case design and a review of relevant optimization techniques.

Chapter 3 introduces the encoding schemes which represent the different pin-assignment for both 1- and 2-dimensional cases. Two types of sources, i.e., differential signal source and absolute signal source are included.

In Chapter 4, a fast model for crosstalk and ground noise estimation is developed. The modeling problem is to compute the crosstalk and ground noise from a given pin-assignment pattern, the inductance matrix and the input source excitation pattern. An example is presented to illustrate the proposed method.

Chapter 5 describes an approach for worst case analysis of crosstalk. The approach can predict worst possible signal integrity problem under various source excitations. Based on this approach, two worst case algorithms, one formulated with the fast algebraic model, the other formulated with the detailed integration-based model are developed.

In Chapter 6, two types of pin-assignment optimization techniques, i.e., genetic algorithm and simulated annealing, are introduced. A new 2-dimensional crossover scheme in GA is developed allowing pin-assignment exploration in either 1- or 2-

dimensions. A constraint is applied to both genetic algorithm and simulated annealing in order to handle the differential signal source.

In Chapter 7, six examples are used to illustrate the usefulness and efficiency of the proposed methods. Both optimization algorithms can produce quality solutions within practical CPU time.

Finally, Chapter 8 describes the conclusions and offers suggestions for future work and research.

Chapter 2

Literature Review

2.1 Signal Integrity Analysis of High-Speed IC Packages and Interconnects

As signal speeds increase, interconnect effects such as signal delay, distortion, reflection and crosstalk become dominant factors limiting the performance of VLSI systems[1]. These problems can be found at chip level, printed circuit board(PCB) level, multichip modules(MCM) and chip packaging where the number of interconnects can be very large[20]. Design optimization of the interconnects has attracted the attention of many researchers[13][20][21]. In order to analyze or design a high-speed, high-density interconnect system, a battery of software modules needs to be developed. But due to the complexity of the analysis models needed in today's circuit, design optimization with highly repetitive circuit analysis is very computationally demanding[13]. Researchers are developing both extremely accurate but computationally expensive methods, and fast but approximate methods for simulation of interconnect behavior. The signal integrity analysis can be performed at electromagnetic level, e.g., [22][1], or at equivalent circuit level, e.g., [23][24]. Many papers have been published in this topic area. In this section, a review of some of the important

aspects of signal integrity which are related to the thesis work is conducted.

Since interconnect networks usually consist of hundreds or thousands of lumped and distributed components, the computational cost of conventional simulation tools can be prohibitive. Recently, there have been many publications on the simulation of VLSI interconnects. Among the various simulation techniques, moment matching techniques such as Asymptotic Waveform Evaluation(AWE), Complex Frequency Hopping(CFH) and Padé Via Lanczos(PVL), e.g., [23][24][15][25][26] have received much attention. These methods have been proven to be both efficient and accurate, yielding a very high CPU advantage. In [23], a generalization of the AWE technique has been presented to handle linear interconnect models that contain lossy coupled transmission lines. In [24], an approach has been proposed to improve the accuracy and stability of the AWE technique, particularly for high-frequency application where high order approximations are required. An alternative method is proposed in [15]. It extends the AWE method to handle VLSI interconnects that contain both lossy coupled transmission lines and nonlinear components. [25] describes an alternative CFH technique. The new technique expands the network response at multiple frequency points and generates multiple sets of moments. This method can be applied for frequency and time domain analysis of large lumped and distributed networks. In order to accurately characterize dispersive systems of VLSI interconnects at higher frequency, a new method which extends the CFH to the case of interconnects modeled with full wave analysis is described in [26]. A speed up of one to three orders of magnitude is achieved compared to the conventional circuit simulation.

Besides the above methods, some other approaches have been developed for solving different problems, e.g., [27][16][28]. A specialized packaging simulator is presented by Basel *et al* [27]. It uses an impulse response model of the interconnect network

to model high-speed digital systems. A hierarchical strategy is developed which uses point modeling of discontinuities and the concept of coupling groups to facilitate tradeoff between accuracy and CPU time. It also can handle large distributed interconnect networks. With this technique, impulse response thresholding provides a smooth transition from delay modeling of interconnects to full distributed circuit simulation. In [16], an efficient method for analog simulation of high-speed printed circuit board system is proposed. It is based on the transmission line model derived from the analysis of electromagnetic fields in a 2-dimensional cross-section of device. Chowdhury *et al*[28] presented a method which allows monitoring of voltage and current at discrete time intervals at user designated points on an interconnect system of any topology. Computing time is linear with respect to the number of nodes and also linear with respect to the number of time points for which simulation is desired.

Ground noise is an important aspect of signal integrity in IC packages. Primarily, ground noise is due to parasitic inductance in the ground return path and the rate at which current through those parasitics is changing. It has been a subject of significant research in recent years. Currently, there exist numerous methods for the simulation of ground noise at the IC and PCB level. There are two types of modeling approaches to estimate Simultaneous Switching Noise(SSN). One is a complex and detailed modeling technique, e.g., [29][5][30][12][31]. This kind of approach is helpful for understanding the physical meaning of simultaneous switching noise phenomena. In particular, it is useful for verifying solutions from optimizing I/O pin-assignment of the package.

Reference [29] deals primarily with ground noise due to the simultaneous switching of CMOS devices. Great care is taken to accurately characterize the ground return structures and the CMOS drivers in order to predict the ground noise resulting from their integration. In [5], the authors indicate that the CMOS circuits exhibit sublinear

behavior(due to the negative feedback influence) of power/ground noise as a function of the number of outputs. In [30], the work based on circuit analysis techniques with simple interconnect models is used to analyze the effects of switching noise, whereas electromagnetic computational techniques are focused on rigorous modeling of power and ground packaging structures. Huang *et al* provide in [12] a design technique which enables an accurate estimation of the maximum SSN and the required numbers of power and/or ground pins for prespecified SSN limits early in the design stage. In [31], modeling of the current distribution in the package reference (power and ground) planes and the extraction of the associated parasitics are presented. Electrical networks and equivalent circuits are developed to model the chip-package interface including the effect of V_{DD}/V_{SS} planes.

Another type of approaches is simple and synthetic modeling approach, e.g., [6][7][32]. This kind of approach is useful in that it provides the package selection criteria although accuracy is sacrificed to some extent. In [6], a fast and accurate methodology for SSN simulation of thin film packaging structure using a macro-modeling technique is presented. The combination of interconnect macromodels and SPICE simulation for non-linear drivers makes this technique attractive for large SSN simulation. This technique results in one order of magnitude improvement in the simulation speed for SSN when compared with SPICE CPU time. New electrical modeling approaches are proposed in [7]. Through the circuit analysis using the new modeling approaches and SSN measurements for C-LGA(ceramic land grid array) and C-PGA(ceramic pin grid array), it was shown that the segment model approach is simple and accurate enough. These approaches can be applied to various types of package structures such as multilayer and leadframe packages. The difference in SSN characteristics among different types of packages can be estimated and compared at

the package design stage. In [32], a methodology for rapid estimation of substrate coupled switching noise in mixed-signal chips is presented. This methodology differs from existing approaches in that it does not require full chip, SPICE level transient or frequency domain simulations or long user-specified test vectors at the chip I/O. Instead, it relies on power dissipation data which is available from system-level power estimators and determines an estimation of the substrate coupled switching noise profile on the chip-substrate. This method trades off the accuracy available in existing approaches for improved execution times and significantly simpler user-inputs.

Some experimental studies and measurements on SSN are also presented, e.g., [33][8]. In [33], the experimental studies on the switching noise in power and ground planes is presented. A board is designed for measuring the properties of noise in the power/ground plane of high-speed system. By using this board, they can quantitatively evaluate the noise diffused from a noise source, and estimate the effects of SSN by superimposing the noise from each of the devices. In [8], the electrical characteristics of SSN for MCM's were measured by using a switching noise generating test chip. It has been observed that the largest noise occurred at the position nearest to the active load lines.

Crosstalk is also an important signal integrity issue due to the increased signal speed and large number of signal pins in packages and connectors. Methods for modeling and simulation of crosstalk noise in coupled multiconductor transmission lines have been developed, e.g., [14][34][35][36].

In [14], an accurate computer model for lossy transmission line system which can be implemented in conventional circuit simulator such as SPICE is presented. This model in conjunction with active device models is applied to the simulation of delay and crosstalk in the interconnect lines of high speed GaAs integrated circuits. You

and Soma studied crosstalk of interconnect lines and packages in high-speed IC in [34]. They present an approach for the analysis of crosstalk propagation delay and pulse distortion of interconnects in high-speed integrated circuit, packages and circuit board. The studies show that ground conductors need to be placed on both sides of each of the signal lines to effectively reduce crosstalk. In [35], El-Zein and Chowdhury formulate the crosstalk in a system containing n lossless microstrip transmission lines as a linear function of time. Crosstalk appears on a line as a noise component. For reliable operation, the worst case crosstalk should be limited within certain bounds. Thus, the pattern of input voltages maximizing the crosstalk could be used in testing logic circuits during the design stage. In [36], a technique requiring a minimum of computational effort is presented for providing engineering estimation of the effects of package mismatch, line loss and crosstalk. The technique entails modifying the Fourier series of a symmetrical trapezoid by transfer functions representing mismatch, loss, or crosstalk.

Crosstalk occurs due to coupling between pins in packages and connectors. Coupling between power distribution planes and signal traces have a significant effect on the noise[37]. The magnitude of the noise is strongly dependent on the relative positions of the signal conductors and the power and ground plane pin connections. Power and ground planes sufficiently close to each other also have significant mutual inductive coupling. This coupling will cause noise to be observed in both distribution planes. To accurately estimate the switching noise, the mutual inductance effect between signal pins and ground pins cannot be neglected. In [38], Nakamura *et al* indicate that the mutual inductances must be included in an accurate simulation model for conductors in conventional plastic packages or sockets because the effective inductance, to which mutual inductances contribute, affects the noise. The

accuracy of a circuit simulation for the noise was significantly improved by using a mutual inductance network based on the three dimensional arrangement of conductors. A comprehensive computer analysis of noise in a digital system would include all inductive, capacitive and resistive effects including all coupling terms.

The determination of inductance from physical and geometrical information has been a subject of serious research. Methods base on 3-D electromagnetic analysis, e.g., [9][10][11] , and semi-analytical approaches[19][39] have been proposed. There are also some other methods to obtain the inductance. A useful inductance evaluation method is obtained by using a quasi-TEM electromagnetic field analysis and matrix operations[40]. Young presents a technique for the measurement of resistance, inductance, conductance, and capacitance matrices of large pin count electronic packages in [41]. In [42], the inductance of the power and ground planes and associated vias is investigated for a new high performance single chip package.

Factors that affect ground noise and crosstalk in IC packages are discussed, which provide guideline for designers, e.g., [17][18][43][44][45]. In [17], variety of parameters such as the arrangement of conductors, the dielectric, the logic voltage swing and the length of coupling of two lines that affect the crosstalk are discussed. There are also a number of package pin and power plane layout rules that help to minimize the ground noise. Reduction of capacitive loading, limiting the number of output buffers, and decoupling capacitors also can reduce the ground noise. The method discussed in [18] shows how ground planes in IC packaging should be connected to the IC ground in order to make the ground plane current density uniform and thereby minimize ground noise. In [43], two possible solutions are studied to reduce coupling effects and to improve the transmission of signals on the lines. These solutions are to earth some lines between active lines or to add a second ground plane over the line. Guide-

lines for grouping and optimal skewing of CMOS output drivers to reduce the total effective power/ground noise are discussed in [44]. Performance trade-offs in using an additional damping resistor in the output driver circuit to reduce power/ground noise is analyzed. In [45], Hough *et al* propose two approaches for on-chip power switching noise reduction. The first approach aims at reducing noise by inserting decoupling capacitors in an optimized manner. The second approach reduces the switching noise by wire-sizing power bus segments near each power pin.

An automatic optimization approach using simulated annealing is developed to minimize ground noise through optimal pin-assignment[19]. It demonstrates that significant reduction in ground noise can be achieved through optimal pin-assignment. It also shows that significant reduction in ground noise is possible beyond physical/geometrical considerations in package design.

2.2 Worst Case Design

Worst case analysis is one of the most often used techniques for verifying that the sensitivity of integrated circuit performances to changes in manufacturing conditions is minimized. Worst case analysis refers to the process of determining the value of the noise parameters in worst case conditions and the corresponding worst case circuit performance values. It is a very important subject in circuit design and has been widely studied, e.g., [46][47][48]. A general approach based on a sensitivity analysis of the circuit is presented in [46]. Expending little simulation effort, this approach leads to reliable and meaningful results. A theory and its implementation in a user-oriented computer program package is described in [47] for solving continuous or discrete worst case tolerance assignment problems. A new algorithm is presented in

[48] for the solution of optimum tolerance assignment problems. The advantage of this approach is that the worst case calculations and the minimization are linked together such that each worst case calculation affects the minimization problem immediately.

Worst case analysis is very efficient in terms of computational time and designer effort, and thus has become one of the most widely practiced techniques for statistical analysis and verification. However, it has been long recognized that conventional worst case analysis approaches suffer from a number of shortcomings and several new approaches have been developed for overcoming the defects, e.g., [49][50][51].

Worst case analysis is often carried out in terms of a *correlated* set of parameter, which results in a design that is unnecessarily pessimistic. A new approach to the worst case analysis of integrated circuits that results in more realistic estimates of variations in device and circuit performances is presented in [49]. Compared to the Monto Carlo simulation, the proposed approach is accurate and computationally efficient.

Worst case analysis is also carried out using an approximate worst case parameter set that do not consider fluctuations in the operating conditions. In [50] a new approach to the worst case design of integrated circuits that takes into account the fluctuations in the operating conditions is presented. It provides unique and realistic worst case manufacturing conditions and worst case operating conditions for given circuit specifications.

Worst case analysis approaches are too pessimistic and lead to extremely conservative designs. In fact, design bottlenecks have been caused by too pessimistic simulation results due to inaccurate worst case models. Dharchoudhury and Kang[51] present a new approach for realistic worst case estimation of VLSI circuit performance and a novel methodology for circuit performance optimization. Worst case

analysis in [51] proceeds by first computing the worst case circuit performance values and then determining the worst case noise parameter values by solving a nonlinear programming problem. A new circuit optimization technique was developed to find an optimal design point at which all of the circuit specifications are met under worst case conditions.

2.3 Optimization Techniques – Genetic Algorithm and Simulated Annealing

The task of optimizing a complex system presents at least two levels of problems for the system designer. First, a class of optimization algorithms must be chosen that is suitable for application to the system. Second, various parameters of the optimization algorithm need to be tuned for efficiency[52].

Genetic algorithm(GA) is an optimization algorithm based on Darwinian models of natural selection and evolution[53][54][55]. It was invented by John Holland[56] and is now among the most promising optimization and machine learning techniques. The basic idea behind GA is that an initial population of candidate chromosome of size n are chosen at random, and each chromosome is evaluated according to the optimization function. Iteratively, a small set of elite individuals of the population are chosen by a selection procedure according to their “fitness value”, which is derived from an individual’s relative functional performance(a measure of how well they satisfy the optimization function)[57]. Under certain reasonable conditions, the value of the objective function increases from generation to generation and converges to an optimal value. The class of GA’s is distinguished from other optimization techniques by the use of concepts from population genetics to guide the search. However, like

other classes of algorithms, GA's differ from one another with respect to several parameters and strategies. Experiments that search a parameterized space of GA's has been carried out[52] in order to identify efficient GA's for the task of optimizing a set of numerical formulations. In order to search other points in the search space, some variation is introduced into the new population by means of idealized genetic recombination operators. The most important recombination operators are called *crossover* and *mutation*.

One-point and two-point crossover have been widely presented in the literature. Traditionally, each has been defined in terms of cross points, place between location where a chromosome can be split. Some new modified crossover operators were recently presented. Uniform crossover is presented in [58]. It is compared theoretically and empirically with one-point and two-point crossover and is shown to be superior in most cases. An adaptive crossover is proposed in [59] with empirical evidence that it is as good as or better than the traditional genetic algorithms across a range of search problems. Three types of permutation crossovers (order crossover, partially matched crossover and cycle crossover) are analyzed in [60] to characterize what type of problems they may be applicable to. Two types of bias (positional bias and distributional bias) were identified in [61]. The bias in crossover is used to help direct the search.

Holland[56] has introduced mutation to genetic algorithms as a "background operator", which assumes the principle possibility to recover from lost alleles. But traditional GA underestimated the power of mutation. Search by mutation appears to be fairly robust and can be analyzed with statistical methods. In most of the case, the optimal mutation rate is proportional to the length of the chromosome[62]. For deceptive functions an evolutionary algorithm with a good hill-climbing strategy and a reasonable mutation rate performs best. Back indicates in [63] that the mutation

rate should not be constant but should decrease over time during the search.

Optimal setting of genetic algorithm parameters has been the subject of numerous studies; however, the optimality of a population size is still a controversial subject. Under a constant computation cost, [64] claims that there exists an optimal population size for the optimization problem. An initial population for a GA is usually chosen at random; one random trial is made to produce each individual. In [65], each member of the initial population is chosen as the best of n randomly chosen individuals. This *extended random initialization* is a generalization of the GA. Some modification of the genetic algorithm for improving its performance in function optimization were also presented and evaluated by Bramlette[65]. The modified methods pertain to deletion of initial populations, mutation, and competition in producing new generations. They were evaluated by using one genetic algorithm to select near-optimal values for parameters controlling another genetic algorithm. Optimal parameter selection was sensitive not only to the particular object function but also to a limit on the number of times it can be evaluated, derived from applications which limit search time severely[65].

The performance of genetic algorithms can be significantly improved by using fitness scaling. The efficiency of fitness scaling depends on the choice of the scaling function. In [66], the problem of choosing scaling functions is formulated as a mathematical optimization problem and solved under different optimality criteria. A list of scaling functions that are optimal under these criteria are obtained.

The convergence characteristics of different GA selection schemes were discussed by using the normal distribution theory as a tool in [67]. The models predict the proportion of optimal alleles as a function of the number of generations when optimizing the bit-counting function.

Simulated annealing is an optimization technique which was introduced in 1982 by Kirkpatrick et al[68]. It is motivated by an analogy to the statistical mechanism of annealing in solids. Simulated annealing techniques use an analogous set of “controlled cooling” operations for nonphysical optimization problems, in effect transforming a poor, unordered solution into a highly optimized desirable solution. Thus, simulated annealing offers an appealing physical analogy for the solution of optimization problems, and more importantly, the potential to reshape mathematical insights from the domain of physics into insights for optimization problems[69]. Upon the normal SA techniques, a combination of simulated annealing and a specific logarithmic exploration has been developed in [70]. This algorithm, called “log simulated annealing” allows handling of continuously valued variables within arbitrary large exploration domains.

Simulated annealing and genetic algorithms represent powerful optimization methods with complementary strengths and weaknesses. They are both motivated by natural phenomena, and are general purpose optimization methods that share many similarities. Both methods require little knowledge of the problem to be optimized other than a fitness or cost function. The two techniques initially begin the search with random points in the solution space then incrementally generate new points by applying operators. Which points are pursued is controlled by a probabilistic decision procedure that guides the method into optimal regions of the solution space[71].

Although GA and SA are similar, there are some important differences between the two methods. First, SA has a formal proof of convergence to the global optimal, which GA does not have. Second, GA maintains a population of candidate solution while SA maintains only one solution. Third, SA accepts newly generated solution probabilistically based on their fitness and only accepts inferior solutions some of the

time, while GA always accepts new solutions even if they are significantly inferior to the older solutions. Finally, and most importantly, GA can easily be adapted to run on passively parallel computers, while SA is an inherently serial algorithm and attempts to use parallel computer have led to relatively small speedups[72].

Chapter 3

Formulation of Pin-Assignment

The work in this thesis is concerned with signal integrity problem in IC packages and connectors. Signals come from the outside of the packages(Figure 3.1) (or connectors Figure 3.2) to the device or circuit inside via metal tracks each of which possesses self inductance and mutual inductance with every other track. Ground noise and crosstalk will occur due to the coupling between pins. For a given structure, such noise depends on the assignment of signal and ground to various pins. For connector design where the pins are usually arranged in 2 dimensions, the couplings between pins can occur in both dimensions. In this case the pin-assignment variations are also 2-dimensional.

The 1-dimensional pin-assignment problem was studied in [19] through a simulated annealing process. In this thesis, we extend the pin-assignment problem to multi-dimension to accommodate both package and connector cases. Also, multi-dimensional optimization algorithms for both simulated annealing and genetic algorithm are developed and incorporated into the pin-assignment problem.

Usually, there are a large number of pins, so the number of possible assignments is huge. In order to use automatic optimization, we use an encoding scheme to represent

Figure 3.1: Top view of package

Figure 3.2: Example of connector

Figure 3.3: One-dimensional pin-assignment

the different pin assignments. At the package level, pin-assignment between different signal and ground pins are performed using a 1-dimensional optimization algorithm with the information from inductance couplings between pins. Each assignment pattern is encoded using a vector $\mathbf{x}$. Suppose there are N pins in the package, and the number of signal sources to be connected to the pins is N_s . Suppose N_g is the number of ground pins. The element in vector $\mathbf{x}$ is defined as:

$$x_n = \begin{cases} p & \text{if source signal \#} p \\ & \text{is connected to pin \#} n \\ & 1 \leq p \leq N_s \\ N_s + l & \text{if ground \#} l \text{ is} \\ & \text{connected to pin \#} n \\ & 1 \leq l \leq N_g \end{cases} \quad (3.1)$$

For example, in Figure 3.3, $N_s = 5$, and $x_2 = 4$ indicates that source E_4 is connected to pin #2. $x_4 = 6$ means that ground #1 is connected to pin #4.

Consider the connector case in which signal and ground pins are distributed in a 2-dimensional configuration with couplings in both dimensions as shown in Figure 3.4. In this case the crosstalk between pins in either dimensions will occur. Therefore instead of using a vector, a 2-dimensional matrix is needed. Let N_{row} and N_{col} be the number of rows and columns of pins, respectively. So $N = N_{row} \times N_{col}$. Pin # (m, n)

Figure 3.4: Two-dimensional pin-assignment with absolute source signals, e.g., $E_{\tau\tau}$ and differential source signals, e.g., E_2 .

represents the pin at row $\#m$, and column $\#n$. We define a matrix $\mathbf{x}$ to represent the pin-assignment pattern:

$$\mathbf{x} = [x_{mn}], \quad m = 1, 2, \dots, N_{row}, \quad n = 1, 2, \dots, N_{col}. \quad (3.2)$$

where x_{mn} is defined as:

$$x_{mn} = \begin{cases} +p & \text{if the positive terminal of source signal} \\ & \#p \text{ is connected to the pin} \\ & \text{in row } \#m \text{ and column } \#n \\ & 1 \leq p \leq N_s \\ -p & \text{if the negative terminal of source signal} \\ & \#p \text{ is connected to the pin} \\ & \text{in row } \#m \text{ and column } \#n \\ & 1 \leq p \leq N_s \\ N_s + l & \text{if ground } \#l \text{ is connected to the} \\ & \text{pin in row } \#m \text{ and column } \#n \\ & 1 \leq l \leq N_g \end{cases} \quad (3.3)$$

Figure 3.4 shows an example of 2-dimensional pin-assignment configuration. Two types of sources, i.e., differential signal source (e.g. source E_2) and absolute signal source (e.g. source $E_{\tau\tau}$) are included.

We formulate our work using 2-dimensional formulation which can be used for both package and connector applications. 1-dimensional pin-assignment is a special case of 2-dimensional pin-assignment when the row number m is fixed at 1.

Chapter 4

A Fast Algebraic Model for Crosstalk and Ground Noise Estimation

A standard approach to crosstalk and ground noise calculation requires the simulation of an equivalent circuit. This approach, although fast enough if the circuit needs to be solved only once, is now computationally prohibitive for our pin-assignment optimization purpose since the circuit has to be repetitively solved many times. In this chapter, we present a fast model suitable for highly repetitive use inside optimization.

4.1 Formulation of Crosstalk and Ground Noise Calculation

Let N_d and N_a be the number of differential sources and absolute sources, respectively.

$$N_s = N_d + N_a \quad (4.1)$$

The inductance matrix $\mathbf{L}$ for the pins is an $N \times N$ matrix, where

$$N = 2N_d + N_a + N_g \quad (4.2)$$

and

$$\mathbf{L} = [L_{mn,m'n'}], \quad m, m' = 1 \cdots N_{row}, \quad n, n' = 1 \cdots N_{col}. \quad (4.3)$$

where $L_{mn,m'n'}$ is the mutual inductance between the pin $\#(m, n)$ and pin $\#(m', n')$.

The determination of $\mathbf{L}$ from physical and geometrical information has been a subject of serious research. Methods based on 3-D electromagnetic analysis, e.g., [9][10][11], and semi-analytical approaches, e.g., [19][39] have been developed. In our work, we address the pin-assignment problem under given physical/geometrical design of packages and connectors. In this context, the $\mathbf{L}$ matrix is first determined through existing inductance extraction methods and is then used as input information to our pin-assignment problem. For example, according to [19], the inductance matrix $\mathbf{L}$ of each package can be extracted and then a system of linear equations can be derived to calculate the ground noise voltage V_g for a given arrangement of pins. Once $\mathbf{L}$ has been extracted, it remains constant: the optimization process involves only pin-assignment. However, the model in [19] can only be used for ground noise estimation in packages. Here we formulate a model for both ground noise and crosstalk estimation.

Let:

$$\mathbf{E} = \begin{bmatrix} E_1 \\ E_2 \\ \vdots \\ E_{N_s} \end{bmatrix} \quad (4.4)$$

where $E_p = E_p(t)$ is the p th source signal, $p = 1, 2, \dots, N_s$.

We use the equivalent circuit of Figure 4.1 to represent the signal integrity problem from package/connector pins. The equivalent circuit includes self and mutual

inductances of pins, source and load impedances, source signals and grounds. The modeling problem is to compute the crosstalk $V_{\text{crosstalk},mn}$ and ground noise $V_{g,mn}$ at pin $\#(m,n)$ from a given pin-assignment pattern $\mathbf{x}$, the inductance matrix $\mathbf{L}$ and the source signal $\mathbf{E}$. The solution to this problem requires time domain simulation of the equivalent circuit as shown in Figure 4.1. This approach, although fast enough if the circuit needs to be solved only once, is now computationally prohibitive for our pin-assignment optimization purpose since the circuit has to be repetitively solved many times. In this chapter, we present a fast model. A digital signal consists of high and low levels and transitions from high to low or from low to high. Crosstalk and ground noise occur mainly due to the transitions between high/low states of the signal. Under the simplifying assumption that such rise/fall times are the main factors in the source signal waveforms that affect ground noise and crosstalk, we represent the signal sources by their rate of change, i.e.,

$$\dot{\mathbf{E}} = \frac{\partial \mathbf{E}}{\partial t} = \begin{bmatrix} \dot{E}_1 \\ \dot{E}_2 \\ \vdots \\ \dot{E}_N \end{bmatrix} \quad (4.5)$$

The exact $\dot{\mathbf{E}}$ changes with time. But the dominant portion of $\dot{\mathbf{E}}$ which is non-zero can be computed from rise and fall times of the original signal. In our case, we further simplify the problem by using constant $\dot{\mathbf{E}}$.

Figure 4.2 and 4.3 show 3 types of pin connections for 2- and 1-dimension cases respectively, i.e., pins connected to differential sources, absolute sources and grounds. For notational simplicity, the sources are numbered beginning with absolute sources followed by differential sources.

Let V_{mn} represent the voltage across pin $\#(m,n)$ as show in Figure 4.2. First, the

Figure 4.1: Equivalent circuit for crosstalk estimation, (a) external circuit for packages/connectors, and (b) equivalent circuit for ground noise and crosstalk estimation.

Figure 4.2: Source connections in 2-dimensional pin-assignment, (a) absolute source, (b) differential source, and (c) ground.

Figure 4.3: Source connections in 1-dimensional pin-assignment, (a) absolute source, (b) differential source, and (c) ground.

di/dt of each pin is calculated:

$$\dot{I}_{mn} = \frac{di_{mn}}{dt} = \begin{cases} +\frac{\dot{E}_{|x_{mn}|}}{R_{mn}}, & \text{if } 1 \leq x_{mn} \leq N_s \\ -\frac{\dot{E}_{|x_{mn}|}}{R_{mn}}, & \text{if } -N_s \leq x_{mn} < -N_a \end{cases} \quad (4.6)$$

where R_{mn} is the equivalent source/load resistance of pin $\#(m, n)$ defined as:

$$R_{mn} = \begin{cases} R_{S,x_{mn}} + R_{L,mn}, & \text{for absolute source} \\ R_{S,x_{mn}} + 2R_{L,mn}, & \text{for differential source} \end{cases} \quad (4.7)$$

and where $R_{S,p}$ is source resistance for source $E_p(t)$, and $R_{L,mn}$ is load resistance for pin $\#(m, n)$ as shown in Figure 4.2.

Let $\dot{I}$ be a N -vector representing the di/dt of all pins:

$$\dot{\mathbf{I}} = \begin{bmatrix} di_{11}/dt \\ di_{12}/dt \\ \vdots \\ di_{mn}/dt \\ \vdots \\ di_{N_{row}N_{col}}/dt \end{bmatrix}_N \quad (4.8)$$

Voltage across each pin is calculated by the following equations:

$$\begin{bmatrix} L_{11,11} & L_{11,12} & \dots & L_{11,N_{row}N_{col}} \\ L_{12,11} & L_{12,12} & \dots & L_{12,N_{row}N_{col}} \\ \vdots & \vdots & \ddots & \vdots \\ L_{N_{row}N_{col},11} & L_{N_{row}N_{col},12} & \dots & L_{N_{row}N_{col},N_{row}N_{col}} \end{bmatrix} \dot{\mathbf{I}} = \begin{bmatrix} V_{11} \\ V_{12} \\ \vdots \\ V_{N_{row}N_{col}} \end{bmatrix} \quad (4.9)$$

Crosstalk on a pin is due to the coupling. In real operation, the signals on various pins will induce noises on various pins including signal pins themselves. We define the crosstalk as the total voltage on the load resistor of a pin when the source on the

pin is set to zero. According to the Figure 4.2(a), the crosstalk of an absolute source which is connected to pin $\#(m, n)$ can be calculated as:

$$V_{\text{crosstalk}, x_{mn}} = \frac{R_{L, mn}}{R_{S, x_{mn}} + R_{L, mn}} \cdot V_{mn} \Big|_{E_{x_{mn}}=0}, \quad \text{for } 1 \leq x_{mn} \leq N_a \quad (4.10)$$

From Figure 4.2(b), the crosstalk of a differential source between pins $\#(m, n)$ and $\#(m', n')$ is:

$$V_{\text{crosstalk}, x_{mn}} = \frac{2R_{L, mn}}{R_{S, x_{mn}} + 2R_{L, mn}} \cdot (V_{mn} - V_{m'n'}) \Big|_{E_{x_{mn}}=0},$$

$$\text{for } N_a < |x_{mn}| \leq N_s, \quad N_a < |x_{m'n'}| \leq N_s \quad (4.11)$$

Also from Figure 4.2(c), the ground noise of pin $\#(m, n)$ is:

$$V_{g, mn} = V_{mn}, \quad \text{for } N_s < x_{mn} \leq N_s + N_g \quad (4.12)$$

4.2 Model Reduction

A model reduction is necessary to solve the modeling problem. According to Equation (4.9), (4.10) and (4.11), the inductances of two pins which are connected to the same differential source can be combined as:

$$\begin{aligned} L_{mn, yz} &= L_{mn, yz} - L_{m'n', yz} \\ L_{yz, mn} &= L_{yz, mn} - L_{yz, m'n'} \end{aligned} \quad (4.13)$$

where, $1 \leq y \leq N_{\text{row}}$, $1 \leq z \leq N_{\text{col}}$. The new $\mathbf{L}$ matrix is a $(N - N_d) \times (N - N_d)$ matrix.

In Equation (4.9), the vector $\dot{I}$ includes the di/dt of all the pins, but only the di/dt of source pins are available using Equation (4.6). The di/dt of each ground pin is not known. According to Figure 4.1, the total di/dt of all ground pins are the sum of the di/dt of the pins which are connected to the absolute sources:

$$\sum_{N_s < x_{mn} \leq (N_s + N_g)} \dot{I}_{mn} = - \sum_{1 \leq x_{mn} \leq N_a} \dot{I}_{mn} \quad (4.14)$$

Rearrange the modified $\mathbf{L}$ matrix obtained by using Equation (4.13):

$$\begin{bmatrix} \mathbf{L}_{11} & \mathbf{L}_{12} \\ \mathbf{L}_{21} & \mathbf{L}_{22} \end{bmatrix} \begin{bmatrix} \dot{\mathbf{I}}_A \\ \dot{\mathbf{I}}_B \end{bmatrix} = \begin{bmatrix} \mathbf{V}_A \\ \mathbf{V}_B \end{bmatrix} \quad (4.15)$$

where

$$\begin{cases} \mathbf{L}_{11} = [L_{mn,m'n'}], & \text{for } N_s < x_{mn} \leq N_s + N_g, \quad N_s < x_{m'n'} \leq N_s + N_g \\ \mathbf{L}_{12} = [L_{mn,m'n'}], & \text{for } N_s < x_{mn} \leq N_s + N_g, \quad 1 \leq x_{m'n'} \leq N_s \\ \mathbf{L}_{21} = [L_{mn,m'n'}], & \text{for } 1 \leq x_{mn} \leq N_s, \quad N_s < x_{m'n'} \leq N_s + N_g \\ \mathbf{L}_{22} = [L_{mn,m'n'}], & \text{for } 1 \leq x_{mn} \leq N_s, \quad 1 \leq x_{m'n'} \leq N_s \end{cases} \quad (4.16)$$

$\dot{\mathbf{I}}_A$ includes the di/dt of all ground pins. $\dot{\mathbf{I}}_B$ includes the di/dt of all sources. $\mathbf{V}_A$ includes the ground noise, $\mathbf{V}_B$ includes the voltages across source pins:

$$\begin{cases} \dot{\mathbf{I}}_A = [di_{mn}/dt], & \text{if } N_s < x_{mn} \leq N_s + N_g \\ \dot{\mathbf{I}}_B = [di_{mn}/dt], & \text{if } 1 \leq x_{mn} \leq N_s \\ \mathbf{V}_A = [V_{mn}], & \text{if } N_s < x_{mn} \leq N_s + N_g \\ \mathbf{V}_B = [V_B], \quad V_B = \begin{cases} V_{mn}, & \text{if } 1 \leq x_{mn} \leq N_a \\ (V_{mn} - V_{m'n'}), & \text{if } N_a < x_{mn} \leq N_s \end{cases} \end{cases} \quad (4.17)$$

Equation (4.15) can be rewritten as:

$$\mathbf{L}_{11}\dot{\mathbf{I}}_A + \mathbf{L}_{12}\dot{\mathbf{I}}_B = \mathbf{V}_A \quad (4.18)$$

$$\mathbf{L}_{21}\dot{\mathbf{I}}_A + \mathbf{L}_{22}\dot{\mathbf{I}}_B = \mathbf{V}_B \quad (4.19)$$

$\dot{\mathbf{I}}_A$ can be symbolically solved from (4.18) as:

$$\dot{\mathbf{I}}_A = \mathbf{L}_{11}^{-1}(\mathbf{V}_A - \mathbf{L}_{12}\dot{\mathbf{I}}_B) \quad (4.20)$$

Because the individual value of $\dot{\mathbf{I}}_A$ is unknown, the total current from (4.14) is used.

Let:

$$\dot{I}_\Sigma = \sum_{N_s < x_{mn} \leq (N_s + N_g)} \dot{I}_{mn} = [1 \ 1 \dots 1]\dot{\mathbf{I}}_A \quad (4.21)$$

and $\mathbf{V}_A$ includes identical values which are the ground noise:

$$\mathbf{V}_A = \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix} V_g \quad (4.22)$$

Equation (4.21) becomes:

$$\begin{aligned} \dot{I}_\Sigma &= [1 \ 1 \dots 1]\mathbf{L}_{11}^{-1} \left(\begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix} V_g - \mathbf{L}_{12}\dot{\mathbf{I}}_B \right) \\ &= [1 \ 1 \dots 1]\mathbf{L}_{11}^{-1} \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix} V_g - [1 \ 1 \dots 1]\mathbf{L}_{11}^{-1}\mathbf{L}_{12}\dot{\mathbf{I}}_B \end{aligned} \quad (4.23)$$

Let:

$$\frac{1}{\beta} = [1 \ 1 \dots 1]\mathbf{L}_{11}^{-1} \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix} \quad (4.24)$$

Then Equation (4.23) can be written as:

$$\beta \dot{I}_\Sigma = V_g - \beta [1 \ 1 \ \dots \ 1] \mathbf{L}_{11}^{-1} \mathbf{L}_{12} \dot{\mathbf{I}}_B \quad (4.25)$$

or

$$\underbrace{\beta}_{\mathbf{L}'_{11}} \dot{I}_\Sigma + \underbrace{\beta [1 \ 1 \ \dots \ 1] \mathbf{L}_{11}^{-1} \mathbf{L}_{12}}_{\mathbf{L}'_{12}} \dot{\mathbf{I}}_B = V_g \quad (4.26)$$

Substitute (4.20) to (4.19) results in:

$$\mathbf{L}_{21} \mathbf{L}_{11}^{-1} (\mathbf{V}_A - \mathbf{L}_{12} \dot{\mathbf{I}}_B) + \mathbf{L}_{22} \dot{\mathbf{I}}_B = \mathbf{V}_B \quad (4.27)$$

Combine Equations (4.22) and (4.26) with Equation(4.27):

$$\mathbf{L}_{21} \mathbf{L}_{11}^{-1} \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix} \beta \dot{I}_\Sigma + \beta \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix} [1 \ 1 \ \dots \ 1] \mathbf{L}_{11}^{-1} \mathbf{L}_{12} \dot{\mathbf{I}}_B - \mathbf{L}_{12} \dot{\mathbf{I}}_B + \mathbf{L}_{22} \dot{\mathbf{I}}_B = \mathbf{V}_B \quad (4.28)$$

then

$$\underbrace{\beta \mathbf{L}_{21} \mathbf{L}_{11}^{-1} \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix}}_{\mathbf{L}'_{21}} \dot{I}_\Sigma + \underbrace{(\beta \mathbf{L}_{21} \mathbf{L}_{11}^{-1} \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix} [1 \ 1 \ \dots \ 1] \mathbf{L}_{11}^{-1} \mathbf{L}_{12} - \mathbf{L}_{12} \mathbf{L}_{11}^{-1} \mathbf{L}_{12} + \mathbf{L}_{22})}_{\mathbf{L}'_{22}} \dot{\mathbf{I}}_B = \mathbf{V}_B \quad (4.29)$$

Now, V_g and $\mathbf{V}_B$ can be calculated by:

$$\begin{bmatrix} V_g \\ \mathbf{V}_B \end{bmatrix} = \begin{bmatrix} \mathbf{L}'_{11} & \mathbf{L}'_{12} \\ \mathbf{L}'_{21} & \mathbf{L}'_{22} \end{bmatrix} \begin{bmatrix} \dot{I}_\Sigma \\ \dot{\mathbf{I}}_B \end{bmatrix} \quad (4.30)$$

where

$$\begin{aligned}
 \mathbf{L}'_{11} &= \beta \\
 \mathbf{L}'_{12} &= \beta[1 \ 1 \ \dots \ 1]\mathbf{L}_{11}^{-1}\mathbf{L}_{12} \\
 \mathbf{L}'_{21} &= \beta\mathbf{L}_{21}\mathbf{L}_{11}^{-1} \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix} \\
 \mathbf{L}'_{22} &= \beta\mathbf{L}_{21}\mathbf{L}_{11}^{-1} \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix} [1 \ 1 \ \dots \ 1]\mathbf{L}_{11}^{-1}\mathbf{L}_{12} - \mathbf{L}_{21}\mathbf{L}_{11}^{-1}\mathbf{L}_{12} + \mathbf{L}_{22} \quad (4.31)
 \end{aligned}$$

and

$$\dot{I}_{\Sigma} = - \sum_{1 \leq m, n \leq N_a} \dot{I}_{mn} \quad (4.32)$$

4.3 Summary of Computation

Now the ground noise and crosstalk can be calculated by following steps:

Step 1: Combine the inductances of the pins which are connected to the same differential source according to Equation (4.13).

Step 2: Compute the new equivalent $\mathbf{L}'$ matrix in the form of Equation (4.31).

Step 3: Calculate di/dt for each source according to Equation (4.6) to obtain $\dot{\mathbf{I}}_B$.

Step 4: Compute total di/dt of all ground pins using Equation (4.32) to obtain $\dot{I}_{\Sigma}$.

Step 5: Calculate the voltages across the ground and signal pins, i.e., V_g and V_B using Equation (4.30).

Step 6: Calculate the final crosstalk and ground noise by Equation (4.10),(4.11) and (4.12).

Major computation effort includes LU decomposition of matrix L_{11} as needed in Equation (4.31). The size of L_{11} is equal to the number of the ground pins N_g . This computation effort is much less than a full circuit level simulation which requires at least one or many LU decompositions of a much larger matrix. Since L_{11} could be a dense matrix, the computational complexity is proportional to N_g^3 . For circuit simulation, the computational complexity is proportional to $(N + N_d)^\alpha$, where $1 \leq \alpha \leq 3$.

4.4 An Example

Figure 4.4 shows an example of the equivalent circuit of a connector. It has eight pins($N=8$), 2 absolute sources($N_a = 2$), 2 differential sources($N_d = 2$) and 2 grounds($N_g = 2$). $N_{row} = 2$, $N_{col} = 4$. Matrix x is the pin-assignment pattern. Values 1 and 2 for elements of x represent the two absolute sources. Values 3 and 4 represent the two differential sources. Values 5 and 6 represent the two grounds.

$$x = \begin{bmatrix} -3 & 1 & 4 & -4 \\ 3 & 5 & 2 & 6 \end{bmatrix} \quad (4.33)$$

L matrix was obtained following [19] which is:

Figure 4.4: Example of crosstalk estimation model, (a) signal/ground pin-assignment, and (b) equivalent circuit model.

$$\mathbf{L} = \begin{bmatrix} 12.7 & 3.79 & 2.46 & 1.82 & 5.43 & 4.51 & 3.39 & 2.65 \\ 3.79 & 12.7 & 3.79 & 2.46 & 4.51 & 5.43 & 4.51 & 3.39 \\ 2.46 & 3.79 & 12.7 & 3.79 & 3.39 & 4.51 & 5.43 & 4.51 \\ 1.82 & 2.46 & 3.79 & 12.7 & 2.65 & 3.39 & 4.51 & 5.43 \\ 5.43 & 4.51 & 3.39 & 2.65 & 22.1 & 7.70 & 5.34 & 4.12 \\ 4.51 & 5.43 & 4.51 & 3.39 & 7.70 & 22.1 & 7.70 & 5.34 \\ 3.39 & 4.51 & 5.43 & 4.51 & 5.34 & 7.70 & 22.1 & 7.70 \\ 2.65 & 3.39 & 4.51 & 5.43 & 4.12 & 5.34 & 7.70 & 22.1 \end{bmatrix} (nH) \quad (4.34)$$

Let $R_{Sp} = R_{L,mn} = 50\Omega$. Let the sources be described by $\dot{E}_1 = \dot{E}_3 = 1.75e9(V/s)$, and $\dot{E}_2 = \dot{E}_4 = 9e8(V/s)$.

From all these given information, the crosstalk and the ground noise calculation using our model can be performed by the following steps.

Step 1 and 2: Reduction of the inductance matrix due to differential sources. The new $\mathbf{L}$ matrix is:

$$\mathbf{L} = \begin{bmatrix} 12.70 & 1.33 & 0.72 & 5.43 & 4.51 & 3.39 \\ 1.33 & 17.72 & 0.10 & 1.12 & 0.92 & -0.92 \\ 0.72 & 0.10 & 23.94 & 3.19 & 1.95 & 1.47 \\ 5.43 & 1.12 & 3.19 & 22.10 & 7.70 & 5.34 \\ 4.51 & 0.92 & 1.95 & 7.70 & 22.10 & 7.70 \\ 3.39 & -0.92 & 1.47 & 5.34 & 7.70 & 22.10 \end{bmatrix} (nH) \quad (4.35)$$

Compute the new equivalent $\mathbf{L}'$ matrix after model reduction in the form of Equation (4.31).

$$\mathbf{L}' = \begin{bmatrix} 13.74 & 4.41 & 0.09 & 2.33 & 7.70 \\ 4.41 & 12.53 & 1.20 & 0.61 & 4.51 \\ 0.09 & 1.20 & 17.59 & -0.01 & 0.92 \\ 2.33 & 0.61 & -0.01 & 23.85 & 1.95 \\ 7.70 & 4.51 & 0.92 & 1.95 & 22.14 \end{bmatrix} (nH) \quad (4.36)$$

Step 3,4: Calculate di/dt for each pin according to Equation (4.6) and the total di/dt of the ground pins using Equation (4.32). Suppose the input sources are

all positive:

$$\dot{\mathbf{I}} = \begin{bmatrix} -(I_1 + I_4) \\ \frac{dE_{x12}/dt}{R_{S,x12} + R_{L,12}} \\ \frac{dE_{x13}/dt}{R_{S,x13} + 2R_{L,13}} \\ \frac{dE_{x21}/dt}{R_{S,x21} + 2R_{L,21}} \\ \frac{dE_{x23}/dt}{R_{S,x23} + R_{L,23}} \end{bmatrix} = \begin{bmatrix} -(I_1 + I_4) \\ \frac{dE_1/dt}{50 + 50} \\ \frac{dE_4/dt}{50 + 100} \\ \frac{dE_3/dt}{50 + 100} \\ \frac{dE_2/dt}{50 + 50} \end{bmatrix} = \begin{bmatrix} -2.65e7 \\ 1.75e7 \\ 6e6 \\ 1.17e7 \\ 9e6 \end{bmatrix} \quad (A/s) \quad (4.37)$$

Step 5: Calculate the voltages across all the pins using Equation (4.30). For example the voltage across the pin # (1,2) is:

$$V_{12} = \begin{bmatrix} 4.41 & 12.53 & 1.20 & 0.61 & 4.51 \end{bmatrix} (nH) \times \begin{bmatrix} -9e6 \\ 0 \\ 6e6 \\ 1.17e7 \\ 9e6 \end{bmatrix} (A/s) = 0.0152(V) \quad (4.38)$$

The voltages across the other pins are:

$$\begin{aligned} V_{13} &= 0.0268(V) \\ V_{21} &= -0.0336(V) \\ V_{23} &= -0.0275(V) \\ V_g &= -0.1898(V) \end{aligned} \quad (4.39)$$

Step 6: Calculate the crosstalk and ground noise by Equation (4.10), (4.11) and (4.12).

$$\begin{aligned}
 V_{crosstalk,1} &= 0.0076(V) \\
 V_{crosstalk,2} &= -0.0138(V) \\
 V_{crosstalk,3} &= -0.0224(V) \\
 V_{crosstalk,4} &= 0.0179(V) \\
 V_g &= -0.1898(V)
 \end{aligned} \tag{4.40}$$

Chapter 5

An Approach for Worst Case Analysis of Crosstalk

The magnitude of crosstalk is dependent on the source excitation patterns, and also on which pin we selected for crosstalk minimization. Without a systematic formulation, pin-assignment optimized for crosstalk on a fixed pin and a fixed source excitation pattern will not be optimal for crosstalks on other pins, or other source excitation patterns. In our work, we propose a worst case optimization approach such that the worst crosstalk under various situations are minimized. Since the number of signal pins in real operation is usually large, and since each signal can be either high or low, there exist a large number of different source excitation patterns. For example, for 100 signal pins, there exist $2^{100} = 1.27 \times 10^{30}$ excitation patterns leading to 1.27×10^{30} different crosstalk situations. Crosstalk estimation through exhaustive analysis would be extremely computation intensive. In this section, we derive a fast worst case estimation approach based on sensitivity information[47], a concept which is used for statistical and manufacturability driven design of circuits[49][51].

For our optimization problem, the worst case of all possible crosstalks is used as the objective function. Worst crosstalk in our problem has two meanings. First, for

a given pin, the crosstalk is determined by reducing the source on itself to zero while allowing other signal pins to have various excitation patterns (the signal is positive or negative). There are great number of such source excitation patterns. For each excitation pattern, there is a corresponding crosstalk. Second, the process defined above is applied to each and every signal pin, again leading to many possible levels of crosstalks. The worst case is the maximum crosstalk of all these values.

5.1 Worst Case Analysis Based on Fast Algebraic Model

Let $\dot{\mathbf{E}}$ be a N_s -vector representing the source excitation pattern:

$$\dot{\mathbf{E}} = \begin{bmatrix} \dot{E}_1 \\ \dot{E}_2 \\ \vdots \\ \dot{E}_{N_s} \end{bmatrix} \quad -\dot{E}_{max} \leq E_p \leq +\dot{E}_{max} \quad (5.1)$$

where $\dot{E}_{max}$ is defined as the absolute value of the maximum rate of change of the input signal. Voltage across pin $\#(m, n)$ is a function of pin-assignment pattern $\mathbf{x}$ and excitation pattern $\dot{\mathbf{E}}$:

$$V_{mn} = V_{mn}(\mathbf{x}, \dot{\mathbf{E}}) \quad (5.2)$$

First, for pin $\#(m, n)$, the worst case is:

$$(V_{crosstalk, mn}(\mathbf{x}))_{worstcase} = \max_{\dot{\mathbf{E}}} V_{crosstalk, mn}(\mathbf{x}, \dot{\mathbf{E}}) \quad (5.3)$$

Second, after the noise of each source pin has been calculated, the maximum of all these values becomes the worst crosstalk:

$$(V_{\text{crosstalk}}(\mathbf{x}))_{\text{worstcase}} = \max_{m,n} (V_{\text{crosstalk},x_{mn}}(\mathbf{x}))_{\text{worstcase}} \quad (5.4)$$

To determine $(V_{\text{crosstalk}})_{\text{worstcase}}$ by examining all possible cases of $\dot{\mathbf{E}}$ and m, n in (5.3) and (5.4) will be extremely computational intensive. A fast way to estimate the corresponding worst case signal pattern is proposed in the following. According to Equations (4.10) and (4.11), the crosstalk of pin $\#(m, n)$ is:

$$V_{\text{crosstalk},x_{mn}} = k \left(\sum_{1 \leq x_{m'n'} \leq N_s} L'_{mn,m'n'} \dot{I}_{m'n'} + L'_{mn,g} \dot{I}_\Sigma \right) \quad (5.5)$$

where $L'_{mn,m'n'}$ is selected from $\mathbf{L}'_{11}$ corresponding to pins $\#(m, n)$ and $\#(m', n')$, and $L'_{mn,g}$ is selected from column vector $\mathbf{L}'_{21}$ corresponding to pin $\#(m, n)$ and ground. k is the ratio of the resistance defined as:

$$k = \begin{cases} \frac{R_{L,mn}}{R_{S,x_{mn}} + R_{L,mn}}, & \text{for absolute source} \\ \frac{2R_{L,mn}}{R_{S,x_{mn}} + 2R_{L,mn}}, & \text{for differential source} \end{cases} \quad (5.6)$$

The sensitivity of $V_{\text{crosstalk},x_{mn}}$ to the di/dt of source $x_{m'n'}$ is:

$$\frac{\partial V_{\text{crosstalk},x_{mn}}}{\partial \dot{I}_{m'n'}} = \begin{cases} k L'_{mn,m'n'}, & N_a < x_{m'n'} \leq N_s \\ k (L'_{mn,m'n'} - L'_{mn,g}), & 1 \leq x_{m'n'} \leq N_a \end{cases} \quad (5.7)$$

The source excitation pattern which leads to a worst case crosstalk on pin $\#(m, n)$ is estimated as:

$$\dot{E}_{x_{m'n'}} = \begin{cases} +\dot{E}_{\text{max}}, & \text{if } \frac{\partial V_{\text{crosstalk},x_{mn}}}{\partial \dot{I}_{m'n'}} > 0 \\ -\dot{E}_{\text{max}}, & \text{if } \frac{\partial V_{\text{crosstalk},x_{mn}}}{\partial \dot{I}_{m'n'}} < 0 \end{cases} \quad (5.8)$$

As an example, we show the worst case analysis for the example in section 4.4. For V_{13} , the worst case excitation pattern $\dot{\mathbf{E}}$ determined from Equation (5.8) is:

$$\dot{\mathbf{E}} = \begin{bmatrix} +\dot{E}_{1,max} \\ +\dot{E}_{2,max} \\ -\dot{E}_{3,max} \\ 0 \end{bmatrix} \quad (5.9)$$

Then the worst case of $V_{crosstalk,13} = V_{crosstalk,4}$ is:

$$\begin{aligned} (V_{crosstalk,4})_{worstcase} &= \begin{bmatrix} 0.09 & 1.20 & 17.59 & -0.01 & 0.92 \end{bmatrix} \\ &\times \begin{bmatrix} -2.65e7 \\ 1.75e7 \\ 0 \\ -1.17e7 \\ 9e6 \end{bmatrix} \cdot \frac{50}{100} = 0.0270(V) \end{aligned} \quad (5.10)$$

Similarly, the worst case of excitation pattern $\dot{\mathbf{E}}$ for the crosstalk at sources #1, 2, and 3 are:

$$\dot{\mathbf{E}} = \begin{bmatrix} 0 \\ +\dot{E}_{2,max} \\ +\dot{E}_{3,max} \\ +\dot{E}_{4,max} \end{bmatrix}, \quad \dot{\mathbf{E}} = \begin{bmatrix} -\dot{E}_{1,max} \\ 0 \\ +\dot{E}_{3,max} \\ +\dot{E}_{4,max} \end{bmatrix}, \quad \dot{\mathbf{E}} = \begin{bmatrix} -\dot{E}_{1,max} \\ -\dot{E}_{2,max} \\ 0 \\ -\dot{E}_{4,max} \end{bmatrix} \quad (5.11)$$

respectively. The negative sign means that the signal changes from high to low, and the positive sign means that the signal changes from low to high. If it is zero, it means that there is no change. For example, the second vector in (5.11) represents a source excitation pattern in which source #1 changes from high to low, and source #3 and 4 change from low to high. Source #2 doesn't change. The worst case of $\dot{\mathbf{E}}$ for ground noise is:

$$\dot{\mathbf{E}}_g = \begin{bmatrix} -\dot{E}_{1,max} \\ -\dot{E}_{2,max} \\ +\dot{E}_{3,max} \\ +\dot{E}_{4,max} \end{bmatrix} \quad (5.12)$$

The worst crosstalk from each of the signal pins and the worst ground noise under various source excitation patterns are:

$$\begin{aligned} V_{crosstalk,1} &= 0.0075(V) \\ V_{crosstalk,2} &= 0.0421(V) \\ V_{crosstalk,3} &= 0.0224(V) \\ V_{crosstalk,4} &= 0.0180(V) \\ V_g &= 0.2455(V) \end{aligned} \quad (5.13)$$

According to the (5.4) the overall worst crosstalk is:

$$(V_{crosstalk}(\mathbf{x}))_{worstcase} = V_{crosstalk,2}(\mathbf{x}) = 0.0421(V) \quad (5.14)$$

5.2 Worst Case Analysis Using Integration-Based Circuit Simulation

The worst case estimation method proposed above is a fast approach and is suitable for repetitive use during optimization. To verify the worst case crosstalk of an optimization solution, a more accurate but slower worst case analysis should be carried out. In this section, we develop a worst case analysis method derived from integration-based circuit simulation. First, a system of linear equations for solving the ground noise and crosstalk can be formatted into a set of linear ordinary differential equations. For the example of Figure 4.4, the equations in the s-domain are:

$$\begin{bmatrix}
sL_{11,11} + R_2 & sL_{11,12} & sL_{11,13} & sL_{11,14} & sL_{11,21} \\
sL_{12,11} & sL_{12,12} + R_1 + R_2 & sL_{12,13} & sL_{12,14} & sL_{12,21} \\
sL_{13,11} & sL_{13,12} & sL_{13,13} + R_1 + R_2 & sL_{13,14} & sL_{13,21} \\
sL_{14,11} & sL_{14,12} & sL_{14,13} & sL_{14,14} + R_2 & sL_{14,21} \\
sL_{21,11} & sL_{21,12} & sL_{21,13} & sL_{21,14} & sL_{21,21} + R_1 + R_2 \\
sL_{22,11} & sL_{22,12} & sL_{22,13} & sL_{22,14} & sL_{22,21} \\
sL_{23,11} & sL_{23,12} & sL_{23,13} & sL_{23,14} & sL_{23,21} \\
sL_{24,11} & sL_{24,12} & sL_{24,13} & sL_{24,14} & sL_{24,21} \\
0 & 1 & 0 & 0 & 0 \\
-1 & 0 & 0 & 0 & -1 \\
0 & 0 & -1 & -1 & 0
\end{bmatrix}$$

$$\begin{bmatrix}
sL_{11,22} & sL_{11,23} & sL_{11,24} & 0 & -1 & 0 \\
sL_{12,22} & sL_{12,23} & sL_{12,24} & 0 & 0 & 0 \\
sL_{13,22} & sL_{13,23} & sL_{13,24} & 0 & 0 & -1 \\
sL_{14,22} & sL_{14,23} & sL_{14,24} & 0 & 0 & -1 \\
sL_{21,22} & sL_{21,23} & sL_{21,24} & 0 & -1 & 0 \\
sL_{22,22} & sL_{22,23} & sL_{22,24} & 1 & 0 & 0 \\
sL_{23,22} & sL_{23,23} + R_1 + R_2 & sL_{23,24} & 0 & 0 & 0 \\
sL_{24,22} & sL_{24,23} & sL_{24,24} & 1 & 0 & 0 \\
1 & 1 & 1 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0
\end{bmatrix}
\begin{bmatrix}
I_{11} \\
I_{12} \\
I_{13} \\
I_{14} \\
I_{21} \\
I_{22} \\
I_{23} \\
I_{24} \\
V_g \\
v_1 \\
v_2
\end{bmatrix}
=
\begin{bmatrix}
0 \\
E_1 \\
E_4 \\
0 \\
E_3 \\
0 \\
E_2 \\
0 \\
0 \\
0 \\
0
\end{bmatrix} \quad (5.15)$$

Let $\mathbf{C}$ and $\mathbf{G}$ be $M \times M$ matrices representing inductive and non-inductive elements in the above equation and $\mathbf{b}(t)$ be a vector that includes the source waveforms $\mathbf{E}(t)$.

Let $\mathbf{X}(t)$ be a M -vector including $X_{mn} = I_{mn}$, the current through pin $\#(m, n)$ for $1 \leq m \leq N_s$, the ground noise voltages of the circuit and an additional voltage variable for each differential source (e.g., v_1, v_2 in Fig.4.4). Then the equation can be written in general as:

$$\mathbf{C}\dot{\mathbf{X}}(t) + \mathbf{G}\mathbf{X}(t) = \mathbf{b}(t) \quad (5.16)$$

Integration formula, for example Backward Euler[73], is applied to (5.16) resulting in:

$$\mathbf{X}(t_{q+1}) = (\mathbf{C} + h\mathbf{G})^{-1} \cdot \mathbf{C} \cdot \mathbf{X}(t_q) + (\mathbf{C} + h\mathbf{G})^{-1} \cdot h \cdot \mathbf{b}(t_{q+1}) \quad (5.17)$$

Let $\mathbf{A}$ and $\mathbf{B}$ be $M \times M$ matrices defined as:

$$\mathbf{A} = (\mathbf{C} + h\mathbf{G})^{-1} \quad (5.18)$$

$$\mathbf{B} = (\mathbf{C} + h\mathbf{G})^{-1} \cdot \mathbf{C} \quad (5.19)$$

Assume that the source signals are step functions with finite rise time t_{ri} :

$$\mathbf{b}(t_q) = \text{diag}\{\gamma_1, \gamma_2, \dots, \gamma_M\} \dot{\mathbf{b}}(t_0) \cdot h \quad (5.20)$$

where

$$\gamma_i = \begin{cases} q, & \text{if } t_q < t_{ri} \\ t_{ri}/h, & \text{if } t_q > t_{ri} \end{cases} \quad (5.21)$$

Then Equation (5.17) can be written as:

$$\mathbf{X}(t_{q+1}) = \mathbf{B} \cdot \mathbf{X}(t_q) + \mathbf{A} \cdot h \cdot \text{diag}\{\gamma_1, \gamma_2, \dots, \gamma_M\} \dot{\mathbf{b}}(t_0) \cdot h \quad (5.22)$$

Again, the purpose is to calculate the worst crosstalk.

$$(V_{\text{crosstalk}})_{\text{worstcase}} = \max_{\mathbf{E}} \max_{m,n} \max_t R_0 \cdot X_{mn}(t) \quad (5.23)$$

where R_0 is:

$$R_0 = \begin{cases} R_{L,mn}, & \text{for absolute source} \\ 2R_{L,mn}, & \text{for differential source} \end{cases} \quad (5.24)$$

We develop an efficient approach for estimating worst crosstalk without performing the integrating for solving (5.22) repetitively for all possible excitation patterns $\mathbf{E}$, and for all pins (m, n) . First, compute the worst case on pin $\#(m, n)$ at a certain time t :

$$(X_{mn}(t))_{worstcase} = \max_{E_p, p=1,2,\dots,N_s} X_{mn}(t) \quad (5.25)$$

Second, the maximum one of all the worst crosstalk of each pin at time t :

$$X(t)_{worstcase} = \max_{1 \leq m, n \leq N_s} X_{mn}(t)_{worstcase} \quad (5.26)$$

Last, the maximum of all the crosstalks at different time:

$$X_{worstcase} = \max_{0 \leq t \leq t_{max}} X(t)_{worstcase} \quad (5.27)$$

is the ultimate worst case value.

According to Equation (5.22), each $\mathbf{X}(t_q)$ is calculated from the previous solution $\mathbf{X}(t_{q-1})$, we have to derive a formula to compute the worst-case for Equation (5.25):

$$\begin{aligned} \mathbf{X}(t_0) &= \mathbf{0} \\ \mathbf{X}(t_1) &= \mathbf{A} \cdot h \cdot \text{diag}\{1, 1, \dots, 1\} \cdot \dot{\mathbf{b}}(t_0) \cdot h \\ &= \mathbf{F}(t_1) \cdot h \cdot \dot{\mathbf{b}}(t_0) \cdot h \\ \mathbf{F}(t_1) &= \mathbf{A} \\ \mathbf{X}(t_2) &= \mathbf{B} \cdot \mathbf{X}(t_1) + \mathbf{A} \cdot h \cdot \text{diag}\{2, 2, \dots, 2\} \cdot \dot{\mathbf{b}}(t_0) \cdot h \\ &= \mathbf{B} \cdot \mathbf{A} \cdot h \cdot \dot{\mathbf{b}}(t_0) \cdot h + \mathbf{A} \cdot h \cdot \dot{\mathbf{b}}(t_0) \cdot 2h \end{aligned}$$

$$\begin{aligned}
&= (\mathbf{B}\mathbf{A} + 2\mathbf{A}) \cdot h \cdot \dot{\mathbf{b}}(t_0) \cdot h \\
&= \mathbf{F}(t_2) \cdot h \cdot \dot{\mathbf{b}}(t_0) \cdot h \\
\mathbf{F}(t_2) &= \mathbf{B}\mathbf{A} + 2\mathbf{A} = \mathbf{B}\mathbf{F}(t_1) + 2\mathbf{A} \\
\mathbf{X}(t_3) &= \mathbf{B} \cdot \mathbf{X}(t_2) + \mathbf{A} \cdot h \cdot \text{diag}\{3, 3, \dots, 3\} \cdot \dot{\mathbf{b}}(t_0) \cdot h \\
&= (\mathbf{B}^2\mathbf{A} + 2\mathbf{B}\mathbf{A} + 3\mathbf{A}) \cdot h \cdot \dot{\mathbf{b}}(t_0) \cdot h \\
&= \mathbf{F}(t_3) \cdot h \cdot \dot{\mathbf{b}}(t_0) \cdot h \\
\mathbf{F}(t_3) &= (\mathbf{B}^2\mathbf{A} + 2\mathbf{B}\mathbf{A} + 3\mathbf{A}) = \mathbf{B}\mathbf{F}(t_2) + 3\mathbf{A} \\
&\vdots \\
\mathbf{X}(t_q) &= \mathbf{F}(t_q) \cdot h \cdot \dot{\mathbf{b}}(t_0) \cdot h \\
\mathbf{F}(t_q) &= \mathbf{B}\mathbf{F}(t_{q-1}) + \mathbf{A} \begin{bmatrix} \gamma_1 & 0 & \dots & 0 \\ 0 & \gamma_2 & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \dots & \gamma_M \end{bmatrix}, \text{ for } q = 1, 2, \dots \quad (5.28)
\end{aligned}$$

where $\mathbf{F}$ is a $M \times M$ matrix computed at each time step. γ_i is decided by (5.21). So the $\mathbf{X}$ of step t_q can be calculated by:

$$\mathbf{X}(t_q) = \begin{bmatrix} F_{11} & F_{12} & \dots & F_{1M} \\ F_{21} & F_{22} & \dots & F_{2M} \\ \vdots & \vdots & \ddots & \vdots \\ F_{M1} & F_{M2} & \dots & F_{MM} \end{bmatrix}_{t_q} \begin{bmatrix} \dot{b}_1 \\ \dot{b}_2 \\ \vdots \\ \dot{b}_M \end{bmatrix}_{t_0} \cdot h^2 \quad (5.29)$$

then

$$X_i(t_q) = h^2 \cdot \sum_{j=1}^M F_{ij}(t_q) \dot{b}_j(t_0) \quad (5.30)$$

Since $\mathbf{b}(t)$ consists of sources $\mathbf{E}(t)$, each $b_j(t)$ is equal to either, $E_p(t)$ or 0. The worst case source signal pattern is defined as:

$$\begin{cases} E_p(t_q) > 0, & \text{if } b_j = E_p \text{ and } F_{ij} > 0 \\ E_p(t_q) < 0, & \text{if } b_j = E_p \text{ and } F_{ij} < 0 \end{cases} \quad (5.31)$$

For the example of section 4.4, the worst crosstalks of each pin calculated by the proposed approach are:

$$\begin{aligned}
 V_{\text{crosstalk},1} &= 0.0076(V) \\
 V_{\text{crosstalk},2} &= 0.0421(V) \\
 V_{\text{crosstalk},3} &= 0.0224(V) \\
 V_{\text{crosstalk},4} &= 0.0180(V) \\
 V_g &= 0.2455(V)
 \end{aligned} \tag{5.32}$$

This result is consistent with that in (5.13). Figure 5.1 shows the time-domain response by using fast algebraic and detailed simulation, respectively.

Here, we only implemented the Backward Euler to the worst case analysis. Other integration methods such as the trapezoidal method can also be applied to the worst case analysis. We can derive equations similarly by using the same method as used for the derivation of Equation (5.28). In general, different time step sizes can be used during the simulation. For our problem, we simplified the simulation process by using the constant time step size. Equation (5.31) can be used to determine the source excitation pattern which corresponds to the worst crosstalk. Similar method can also be used to determine the source excitation pattern corresponding to the worst ground noise.

Figure 5.1: Time-domain response of the example in section 4.4

Chapter 6

Pin-Assignment Optimization

Having developed worst case analysis models for crosstalk and ground noise estimation, we will formulate the worst case optimization problem for package and connector pin-assignment optimization. Two-dimensional pin-assignment optimization algorithms based on genetic algorithm and simulated annealing are also developed.

6.1 Formulation of Optimization

Let $\mathbf{x}$ represent a pin-assignment pattern defined as in Equation (3.3). Let $F(\mathbf{x})$ be the objective function for optimization. For ground noise and crosstalk optimization:

$$\begin{aligned} F(\mathbf{x}) &= \max\{w_1 V_{g, \text{worstcase}}(\mathbf{x}), w_2 V_{\text{crosstalk, worstcase}}(\mathbf{x})\} \\ &= \max_{m, n, \dot{E}_p} \{w_1 V_g(\mathbf{x}, \dot{\mathbf{E}}), w_2 V_{\text{crosstalk}, x_{mn}}(\mathbf{x}, \dot{\mathbf{E}})\} \end{aligned} \quad (6.1)$$

where $1 \leq m \leq N_{\text{row}}$, $1 \leq n \leq N_{\text{col}}$, $-\dot{E}_{\text{max}} \leq \dot{E}_p \leq \dot{E}_{\text{max}}$, and $1 \leq p \leq N_s$. w_1 and w_2 are the weighting factors. The optimization problem is to find a pin-assignment pattern $\mathbf{x}$ such that:

$$\min_{\mathbf{x}} F(\mathbf{x}) \quad (6.2)$$

i.e., the worst possible crosstalk and ground noise from all signal pins or ground pins under various source excitation patterns are minimized.

6.2 Genetic Algorithm and Simulated Annealing

Two types of global optimization algorithms, i.e. simulated annealing(SA) and genetic algorithm(GA), are incorporated into this work. For differential signal sources, the sources are between adjacent pins in either dimensions. In this case the pair of signal pins for a source must always remain adjacent in either horizontal or vertical dimensions during optimization. To address this issue, we incorporated a constraint into the simulated annealing so that a new pin-assignment pattern will be created subject to the constraint. For the genetic algorithm, this constraint is applied during the creation of two-dimensional Partially Matched Crossover(PMX).

Simulated annealing[19][69][74] is used to determine the pin configuration yielding the lowest crosstalk and/or ground noise voltage. Simplistically, if F_n and F_{n-1} constitute respectively the current and previous objective function values and $F_n < F_{n-1}$ then the current set of variable values(the current pin configuration) will replace the previous set. On the other hand, if $F_n > F_{n-1}$ the current set of values will still be accepted over the previous set if:

$$P_0 e^{-D/T} > P \quad (6.3)$$

is satisfied, where P is a random value between 0 and 1, P_0 is a proportionality constant, D is the difference between the current and previous function values and T is a resolution constant analogous to temperature in actual annealing.

New iteration in the algorithm requires the swapping of entries in the x matrix. For differential source in the 2-dimensional case, pairs of adjacent entries of the x matrix have to be swapped simultaneously with other pairs of entries in the matrix.

Genetic algorithm[53][54][55] is a search algorithm based on the mechanism of natural selection and natural genetic. Here pin-assignment x is interpreted as a chromosome. First, a population of random chromosomes(x^i) which are candidate solutions is initialized. Each chromosome in the population is evaluated and then assigned a fitness:

$$f(x^i) = -a * F(x^i) + b \quad (6.4)$$

where a , b are the coefficients and $F(x^i)$ is the objective function value obtained from Equation (6.1). In reproduction, *roulette wheel selection* technique is used to pick two parent chromosomes, then *crossover* and *mutation* operators are applied to those two parents to generate a new chromosome called offspring. The offspring with its fitness calculated replaces the worst chromosome in the population. In this way the chromosomes evolve so that later generations contain individuals that are better than the earlier generations. Genetic algorithm use probabilistic transition rules to guide its search, so it can avoid the local minimum and find the global minimum.

6.3 Two-Dimensional PMX in GA for Pin-Assignment

Pins in connectors are usually arranged in 2 dimensions and crosstalk is affected by couplings in both dimensions. The overall pin-assignment needs to consider both dimensions concurrently, and optimization should search alternative pin-assignment in both dimensions. The conventional 1-dimensional formulation, e.g., [59][60] is not adequate in this case.

Crossover, e.g., Partially Matched Crossover(PMX), is a crucial step in GA to generate new solution from old ones for optimization if non-binary codes are used for chromosome representations. The purpose of the PMX is to preserve parts of the elements from both parents to the offspring and at the same time to avoid the duplication of the elements. In this section, we expand the 1-dimensional PMX crossover technique in GA[59][60] to 2-dimensional PMX in order to handle the connector case.

Step 1: Two chromosomes(matrix $x^{(1)}$ and $x^{(2)}$) are chosen as the parents, and four crossing sites are picked uniformly at random, two for row sites, two for column sites. Let the matrix size of x be N_{row} and N_{col} . Let c_1 and c_2 represent the column sites 1 and 2. Let r_1 and r_2 represent the row sites 1 and 2. These four sites define a match window. This is used to effect a cross through position-by-position exchange operation.

Step 2: Let the offspring be represented by $x^{(3)}$. Match window of the first parent(matrix $x^{(1)}$) is completely copied to the offspring(matrix $x^{(3)}$):

$$\begin{aligned} x_{mn}^{(3)} &= x_{mn}^{(1)}, & m &= r_1 \cdots r_2 \\ & & n &= c_1 \cdots c_2 \end{aligned} \quad (6.5)$$

Step 3: The elements excluding the match window of the second parent(matrix $x^{(2)}$) are copied to the offspring, but the number which already exists in the match window of the first parent should not be copied. In this case the corresponding space of the offspring is left out empty:

$$\begin{aligned} x_{mn}^{(3)} &= x_{mn}^{(2)}, & m &= 0 \cdots r_1 \text{ and } m = r_1 + 1 \cdots N_{row} \\ & & n &= 0 \cdots c_1 \text{ and } n = c_1 + 1 \cdots N_{col} \\ & & \text{for } x_{mn}^{(2)} &\notin \text{match window of matrix } x^{(1)} \end{aligned} \quad (6.6)$$

Step 4: Mapping match windows of the two parents to find the correct pair of element for switching:

- 4.1 If an entry in $x^{(3)}$ is empty, and the m_1 and n_1 are the row and column indices of this entry, i.e., $x_{m_1 n_1}^{(3)}$ is empty, then find an element a whose position is m_1 and n_1 in matrix $x^{(2)}$, i.e., $x_{m_1 n_1}^{(2)} = a$.
- 4.2 Find the same value a in matrix $x^{(1)}$, and record the position of a as m_2 and n_2 , i.e., $x_{m_2 n_2}^{(1)} = a$.
- 4.3 Find another element b whose position is m_2 and n_2 in matrix $x^{(2)}$, i.e., $x_{m_2 n_2}^{(2)} = b$.
- 4.4 If $x_{m_2 n_2}^{(2)}$ is not included in the match window of matrix $x^{(1)}$, then let $x_{m_1 n_1}^{(3)} = x_{m_2 n_2}^{(2)} = b$. Go back to step 4.1 until all the empty entries of matrix $x^{(3)}$ are filled.
- 4.5 If $x_{m_2 n_2}^{(2)}$ is included in the match window of matrix $x^{(1)}$, then let $a = b$, and go back to step 4.2.

After PMX, the absolute positions of some elements of both the first and second parents are preserved to the offspring. The offspring replaces the chromosome with the least fitness in the population, and the evolution keeps going. After many generations, the optimal pin-assignment can be obtained.

6.4 An Example of Two-Dimensional PMX

Figure 6.1 describes the 2-dimensional PMX step by step. First, the four crossing sites are rows 2 and 3, and columns 2 and 4. These four sites define a match window. Second, the match window of first parent is completely copied to the offspring, then

the elements excluding the match window of the second parent are copied to the offspring. Since the elements 8, 14 and 15 from the second parent is found common to the match window of the first parent, the corresponding space of the offspring is left out empty. Last, match windows of the two parents are mapped and following couple are replaced by each other:

$$8 \leftrightarrow 20,$$

$$(14 \leftrightarrow 10, 10 \leftrightarrow 9, 9 \leftrightarrow 3) \text{ resulting in } 14 \leftrightarrow 3$$

$$(15 \leftrightarrow 16, 16 \leftrightarrow 22) \text{ resulting in } 15 \leftrightarrow 22$$

The value at the left side of the arrows is from parent 1 while the value at the right side of the arrows is from the corresponding location in parent 2. Consequently, the empty spaces of the offspring are all filled.

Step 1:

Step 2:

Step 3:

Step 4:

Offspring X^3

Figure 6.1: Example of two-dimensional PMX

Chapter 7

Examples

In this chapter, six examples are presented for ground noise and crosstalk minimization using 1- and 2-dimensional pin-assignment optimization techniques. The worst case analysis with the fast algebraic model is used during optimization. The results are checked by worst case analysis using integration based simulations. Both the simulated annealing and the genetic algorithms are used. The signal types of these six examples are summarized in Tables 7.1 and 7.2.

Example	No. of Pins	Abso. Source		Diff. Source		Noise Type
		No.	di/dt(A/s)	No.	di/dt(A/s)	
1	12	8	11.3e7			Ground Noise
2	4 × 25	42	3.5e7			Ground Noise
		36	1.8e7			
		2	7.0e7			
3	4 × 25	30	3.5e7	5	3.5e7	Ground Noise
		30	1.8e7	5	1.8e7	

Table 7.1: Signal types for Examples 1-3.

Example	No. of Pins	Abso. Source		Diff. Source		Noise Type
		No.	$dv/dt(V/s)$	No.	$dv/dt(V/s)$	
4	4×90			90	1.75e9	Crosstalk
				90	9e8	
5	4×90	30	1.75e9	70	1.75e9	Crosstalk
		30	9e8	70	9e8	
6	4×90	30	1.75e9	70	1.75e9	Crosstalk & Ground Noise
		30	9e8	70	9e8	

Table 7.2: Signal types for Examples 4-6.

	GA	SA
Initial $V_g(v)$	1.08	1.62
Optimized $V_g(v)$	1.06	1.06
Real CPU time(sec)	0.32	0.65

Table 7.3: Average results over 18 optimizations for Example 1.

7.1 Example 1: A Simple Illustrative Example

Example 1 is a 1-dimensional pin-assignment of a 12-pin QFP. It consists of eight signals and four grounds, i.e., $N_s = 8, N_g = 4, N = 12$. Initially, the grounds are assigned to pins 9-12 for SA. For GA, we generate a random population of initial solutions. Practical guidelines for pin-assignment, e.g., grounds should not be together but distributed to separate signals, can be used as the initial solutions or applied as constraints during optimization. The initial assignment has been simulated and the V_g is calculated. Computational results using GA and SA for pin-assignment are shown in the Table 7.3. Resulting ground noise reduction of 35% is obtained for SA.

	GA	SA
Initial $V_g(v)$	0.636	1.240
Optimized $V_g(v)$	0.196	0.202
Real CPU time(sec)	547.68	689.27

Table 7.4: Average results over 18 optimizations for Example 2.

7.2 Example 2: A 100-Pin Package with Only Absolute Sources

Example 2 includes one-hundred pins arranged in 4 by 25 two-dimensional configuration with only absolute sources for signal pins. 80 out of 100 pins are connected to three different types of signals. The initial pin-assignment has pins 1-42 carrying the high-speed signal($di/dt = 3.5e7 A/s$), pins 43-78 carrying the low-speed signal($di/dt = 1.8e7 A/s$), and pins 79-80 carrying the very high-speed signal($di/dt = 7e7 A/s$). The results are shown in Table 7.4.

Optimal pin-assignment resulted in average noise reduction of 69.2% and 83.7% for GA and SA respectively. Pin-assignment optimizations were repeated about 18 times for this example for using different conditions in optimization, e.g., different starting/finishing temperature and temperature reduction factors for SA, different population size and number of generations for GA. Table 7.5 gives the results from GA for Example 2.

Population Size	No. of Generation		Mutation Probability		
			0.3	0.4	0.5
50	4e4	CPU	555.04	538.76	526.51
		$V_g(v)$	0.196	0.196	0.196
100	4e4	CPU	522.04	502.63	497.55
		$V_g(v)$	0.196	0.196	0.196
150	4e4	CPU	467.82	457.02	480.55
		$V_g(v)$	0.196	0.196	0.196
200	5e4	CPU	549.57	589.58	596.56
		$V_g(v)$	0.196	0.196	0.195
250	5e4	CPU	600.99	627.87	587.98
		$V_g(v)$	0.196	0.198	0.204
300	5e4	CPU	601.39	607.54	548.80
		$V_g(v)$	0.196	0.195	0.196

Table 7.5: CPU and minimized ground noise by Genetic Algorithm for Example 2.

7.3 Example 3: A 100-Pin Package with Both Absolute and Differential Sources

Example 3 is similar to the second example except that both absolute and differential sources are included. The initial pin-assignment has pins 1-30 carrying the high-speed absolute signals, pins 31-60 carrying the low-speed absolute signals, pins 61-70 carrying the high-speed differential signals, and pins 71-80 carrying the low-speed differential signals. Computation times for the two algorithms are 827.99 and 594.35 seconds respectively. The bottleneck of the CPU time is the model evaluation. The average noise reductions are 71.9% and 91.9% for each algorithm as in Table 7.6.

Pin-assignment optimizations were repeated about 14 times by SA. Table 7.7 shows the results for Example 3.

Comparing GA and SA, GA exhibits implicit parallelism and can exploit massively parallel architectures, but it suffers from disruption and poor convergence properties.

	GA	SA
Initial $V_g(v)$	0.372	0.934
Optimized $V_g(v)$	0.097	0.075
Real CPU time(sec)	827.99	594.35

Table 7.6: Average results over 18 optimizations for Example 3.

Start Temperature	End Temperature		control factor	
			0.95	0.98
1e-3	1e-8	CPU	210.00	898.92
		$V_g(v)$	0.093	0.074
3e-3	1e-8	CPU	175.56	1085.91
		$V_g(v)$	0.086	0.071
5e-3	1e-8	CPU	188.54	1163.81
		$V_g(v)$	0.078	0.063
1e-2	1e-8	CPU	210.95	322.88
		$V_g(v)$	0.070	0.075
3e-2	1e-8	CPU	201.56	997.73
		$V_g(v)$	0.077	0.073
5e-2	1e-8	CPU	259.38	583.64
		$V_g(v)$	0.080	0.074
1e-1	1e-8	CPU	286.93	1735.15
		$V_g(v)$	0.073	0.065

Table 7.7: CPU and minimized ground noise by Simulated Annealing for Example 3.

SA, on the other hand, has good convergence properties and is somewhat immune to disruption, but it cannot easily exploit either explicit or implicit parallelism[71]. In our experiment, it is also observed that genetic algorithm performs better when more absolute sources are presented, and the simulated annealing is better with differential sources.

	Initial Value	After Optimization
Temperature	5e-7	1e-12
$V_{\text{crosstalk, worstcase}}$	0.645(V)	0.285(V)
Switching pair	10	2
Control factor	0.98	
Iteration	132,310	
CPU time(sec)	112.583	

Table 7.8: CPU and minimized crosstalk by Simulated Annealing for Example 4.

7.4 Example 4: A 360-Pin Connector with Only Differential Sources

Example 4 has 360 pins in 4 by 90 2-dimensional configuration with only differential sources. The source signals include 90 high-speed differential signals with $dE/dt = 1.75e9V/s$, and 90 low-speed differential signals with $dE/dt = 9e8V/s$. The initial pin-assignment has pins 1-180 carrying the high-speed differential signals, and pins 181-360 carrying the low-speed differential signals. Only the crosstalk is computed and optimized using simulated annealing. Table 7.8 shows the results of optimization. The average noise reduction is 55.8% for simulated annealing. In the table, the switching pair is a user controllable parameter in SA that represents number of the pairs that can be switched in each iteration, and the control factor is a parameter that represents the temperature reduction rate.

7.5 Example 5: A 360-Pin Connector with Both Absolute and Differential Sources

Example 5 is similar to the Example 4 but both absolute and differential sources are included. 340 out of the 360 pins are signal pins with two different magnitudes of

	GA	SA
Initial $V_{cross}(v)$	0.595	0.577
Optimized $V_{cross}(v)$	0.385	0.200
Real CPU time(sec)	246.087	113.970

Table 7.9: Average results over 16 optimizations for Example 5.

dE/dt values. The initial pin assignment has pins 1-30 carrying the high-speed absolute signals, pins 31-60 carrying the low-speed absolute signals, pins 61-200 carrying the high-speed differential signals, and pins 200-340 carrying the low-speed differential signals. Table 7.9 shows the average results of the optimization.

For SA, pin-assignment optimizations were repeated about 16 times with different conditions. Table 7.10 gives the results of all these optimization.

For GA, pin-assignment optimizations were repeated about 18 times with different conditions as shown in Table 7.11.

The average noise reductions are 35.3% for GA and 65.3% for SA. Tables 7.12 and 7.13 show one example of the source excitation pattern before and after the worst case estimation.

In order to verify the worst case crosstalk estimated from fast algebraic model, Backward Euler integration is used to calculate the crosstalk of the optimal pin-assignment after SA optimization. Table 7.14 confirms that the worst case analysis of fast model is consistent with that from detailed simulation. SA is rerun 16 times and the $V_{crosstalk, worstcase}$ for each SA is listed in the Table 7.14.

Figure 7.1 shows the time-domain response of the simulation by Backward Euler.

If the speed of the input signal is increased, the difference between the two types of simulations are increased as shown in Table 7.15. SA is rerun 16 times and the

Start Temperature	End Temperature		control factor	
			0.95	0.98
1e-4	1e-9	CPU	33,365	192,918
		$V_c(v)$	0.200	0.204
5e-4	1e-9	CPU	43,397	268,063
		$V_c(v)$	0.206	0.173
1e-5	1e-10	CPU	33,365	206,825
		$V_c(v)$	0.206	0.193
5e-5	1e-10	CPU	43,397	141,088
		$V_c(v)$	0.206	0.205
1e-6	1e-10	CPU	22,081	133,523
		$V_c(v)$	0.208	0.197
5e-6	1e-10	CPU	29,916	123,944
		$V_c(v)$	0.206	0.197
1e-7	1e-12	CPU	33,365	206,825
		$V_c(v)$	0.208	0.190
5e-7	1e-12	CPU	43,397	268,057
		$V_c(v)$	0.207	0.190

Table 7.10: CPU and minimized crosstalk by Simulated Annealing for Example 5.

Population Size	No. of Generation		Mutation Probability		
			0.3	0.4	0.5
200	10e4	CPU	156,342	163,416	170,542
		$V_c(v)$	0.435	0.393	0.428
400	10e4	CPU	158,688	164,678	170,684
		$V_c(v)$	0.394	0.387	0.393
600	15e4	CPU	234,513	245,124	255,813
		$V_c(v)$	0.367	0.380	0.395
800	15e4	CPU	238,032	247,016	256,026
		$V_c(v)$	0.362	0.393	0.362
1000	20e4	CPU	312,684	326,832	341,084
		$V_c(v)$	0.345	0.390	0.392
1200	20e4	CPU	317,376	329,356	341,368
		$V_c(v)$	0.370	0.382	0.368

Table 7.11: CPU and minimized crosstalk by Genetic Algorithm for Example 5.

Row no.	Source number at each column location
1	54 16 215 21 56 48 33 6 218 50 52 23 47 213 24 20 25 217 26 31 76 -76 60 55 17 39 214 14 22 9 210 3 27 18 12 219 4 -137 43 53 44 51 203 59 183 37 -142 142 188 -188 35 167 -167 140 -140 34 209 36 41 49 99 -99 45 57 2 28 42 212 8 30 19 207 38 40 32 205 29 10 201 11 206 5 1 202 58 46 15 208 7 220
2	-113 113 87 -87 121 -121 163 -163 198 -198 124 -124 -200 200 -78 78 -179 179 117 -117 -130 130 73 -73 -187 187 -141 141 178 -178 -148 148 -123 123 170 -84 84 137 -138 138 195 -195 -189 189 -183 -151 151 13 -152 152 -144 144 192 -192 165 -165 186 -186 -86 86 106 -106 -147 147 177 -177 171 -171 -157 157 -145 145 127 -127 110 -110 -120 120 -71 71 -135 135 -158 158 -193 193 102 -102 -107 107
3	90 -90 -63 63 -75 75 -166 166 -119 119 -125 125 61 -61 64 -64 -194 194 -160 160 82 -82 92 -92 -155 155 -104 104 94 -94 72 -72 -66 66 -170 216 88 -88 -129 129 -150 150 172 -172 -156 156 -190 190 -182 182 169 -169 161 -161 -185 185 89 -89 -133 133 -159 159 101 -101 132 134 -175 175 -118 118 -174 174 -109 109 -62 62 80 -80 -79 79 93 -93 -81 81 95 -95 115 -115 -103 103
4	122 -122 -65 65 69 -69 -77 77 -70 70 -108 108 196 -196 74 -74 97 -97 116 -116 -91 91 -98 98 -139 139 96 -96 -83 83 -85 85 -68 68 -112 112 126 -126 149 -149 162 -162 -131 131 199 -199 173 -173 197 -197 184 -184 -136 136 -154 154 146 -146 164 -164 -191 191 111 -111 -132 -134 153 -153 -67 67 -180 180 -105 105 128 -128 -181 181 204 168 -168 -114 114 143 -143 -176 176 211 -100 100

Table 7.12: Source excitation pattern for Example 5 before worst case estimation. Each row has ninety pins(i.e., ninety columns per row). Each value in the table represents the index of the source connected to the pin in a column.

Row no.	Source number at each column location
1	54 16 215 21 56 48 33 6 218 50 52 23 47 213 24 20 25 217 26 31 -76 76 60 55 17 39 214 14 22 9 210 3 27 18 12 219 4 137 43 53 44 51 203 59 183 37 -142 142 -188 188 35 167 -167 140 -140 34 209 36 41 49 -99 99 45 57 2 28 42 212 8 30 19 207 38 40 32 205 29 10 201 -11 206 -5 -1 202 -58 46 -15 208 -7 220
2	113 -113 -87 87 -121 121 163 -163 -198 198 124 -124 200 -200 -78 78 179 -179 -117 117 -130 130 73 -73 187 -187 -141 141 178 -178 -148 148 -123 123 170 -84 84 -137 -138 138 195 -195 -189 189 -183 -151 151 13 -152 152 144 -144 192 -192 165 -165 -186 186 -86 86 106 -106 147 -147 177 -177 171 -171 157 -157 145 -145 127 -127 110 -110 120 -120 -71 71 135 -135 158 -158 193 -193 -102 102 -107 107
3	90 -90 63 -63 75 -75 166 -166 119 -119 125 -125 61 -61 -64 64 -194 194 -160 160 -82 82 92 -92 155 -155 104 -104 94 -94 -72 72 -66 66 -170 216 -88 88 -129 129 150 -150 -172 172 -156 156 -190 190 182 -182 169 -169 161 -161 185 -185 -89 89 -133 133 159 -159 101 -101 132 134 175 -175 118 -118 174 -174 109 -109 62 -62 80 -80 79 -79 93 -93 81 -81 95 -95 -115 115 -103 103
4	122 -122 65 -65 69 -69 77 -77 70 -70 108 -108 196 -196 74 -74 -97 97 -116 116 -91 91 98 -98 139 -139 96 -96 83 -83 -85 85 -68 68 -112 112 126 -126 -149 149 162 -162 -131 131 -199 199 -173 173 197 -197 184 -184 136 -136 154 -154 146 -146 164 -164 191 -191 -111 -111 -132 -134 153 -153 67 -67 180 -180 105 -105 128 -128 -181 181 204 168 -168 114 -114 143 -143 -176 176 211 -211 100 100

Table 7.13: Source excitation pattern for Example 5 after worst case estimation. Each row has ninety pins(i.e., ninety columns per row). Each value in the table represents the index of the source connected to the pin in a column.

SA rerun	$V_{\text{crosstalk, worstcase}}(V)$ from algebraic model	$V_{\text{crosstalk, worstcase}}(V)$ from integration based simulation
before SA	0.555707	0.554618
1	0.199567	0.199527
2	0.204002	0.203962
3	0.205989	0.205924
4	0.173108	0.173168
5	0.206128	0.206059
6	0.193098	0.193069
7	0.205989	0.205924
8	0.204513	0.204460
9	0.208289	0.208176
10	0.196623	0.196537
11	0.206229	0.206230
12	0.196708	0.196670
13	0.207898	0.206055
14	0.190029	0.189985
15	0.207475	0.207420
16	0.189989	0.189946

Table 7.14: Comparison of the worst case solution from approximate algebraic model and detailed integration-based simulation for Example 5 after Simulated Annealing optimization.

Figure 7.1: Time-domain response of the detailed integrated-based simulation and fast algebraic model for Example 5.

SA rerun	$V_{\text{crosstalk, worstcase}}$ from algebraic model	$V_{\text{crosstalk, worstcase}}$ from integration based simulation
Before SA	1.111415	1.047971
1	0.399134	0.396641
2	0.408004	0.403664
3	0.505272	0.489303
4	0.346360	0.344362
5	0.412256	0.406536
6	0.386196	0.383222
7	0.511978	0.502846
8	0.409026	0.404696
9	0.416578	0.408294
10	0.393246	0.387203
11	0.412458	0.406575
12	0.393416	0.389388
13	0.415396	0.406738
14	0.380058	0.375035
15	0.414950	0.409932
16	0.379978	0.375576

Table 7.15: Comparison of the approximate algebraic model and detailed integration-based simulation by increasing the speed of input signal for Example 5 after Simulated Annealing optimization.

$V_{\text{crosstalk, worstcase}}$ for each SA is listed in the Table.

7.6 Example 6: Minimization of Crosstalk and Ground Noise for the 360-Pin Connector

Example 6 has the same configuration as Example 5 and both absolute and differential sources are included. The initial pin-assignment is also the same as Example 5, but besides the crosstalk, ground noise is also included in optimization. The weighting factors of ground noise and crosstalk is 0.5 and 2 respectively. Table 7.16 shows

	Initial Value	After Optimization
Temperature	5e-7	1e-12
$V_{crosstalk, worstcase}$	0.555(V)	0.295(V)
$V_{g, worstcase}$	7.114(V)	0.398(V)
Overall Object Function F	3.557(V)	0.589(V)
Switching pair	10	2
Control factor	0.98	
Iteration	217.425	
CPU time(sec)	281.459	

Table 7.16: CPU and minimized crosstalk and ground noise by Simulated Annealing for Example 6.

the results of simulated annealing optimization. The pin-assignment optimization resulted in 55.9% reduction in crosstalk and at same time 94.4% reduction in ground noise.

Chapter 8

Conclusion

8.1 Conclusion

This research was motivated by the need for an efficient approach for the optimal pin-assignment for signal integrity optimization in IC packages and connectors. An automatic pin-assignment optimization technique has been developed allowing concurrent ground noise and crosstalk minimization in both packages and connectors. Several contributions have been presented in this thesis to address the problems:

1. An equivalent circuit was presented for the signal integrity problem from package and connector pins. The circuits include self and mutual inductances of package pins, source and load impedances, source signal and ground. A fast algebraic model based on this circuit is developed for the crosstalk and ground noise estimation. The modeling problem is to compute the crosstalk and ground noise from a given pin-assignment pattern, the inductance matrix and the input signal excitation pattern.
2. Efficient methods for worst case analysis of crosstalk are developed, one based on fast algebraic model and the other based on detailed integration-based circuit

simulation. Worst case analysis with fast algebraic models can be used during optimization and its solution can be verified using the detailed integration simulation based worst case analysis.

3. Our techniques offer two types of optimization approaches, i.e., simulated annealing and genetic optimization, which are developed for both 1- and 2-dimensional pin-assignments. Both optimization algorithms can produce quality solutions within a practical CPU time limit.
4. The proposed approach has been implemented into a computer program for pin-assignment optimization. This program has been verified by all the six examples presented in this thesis. The inputs of the program are the L matrix, number of rows(N_{row}) of pins, number of columns(N_{col}) of pins, number of the absolute sources(N_a) and differential sources(N_d). The output of the program is optimal pin-assignment x . Users can control the parameters for the optimization process, e.g., starting/finishing temperature, switching pairs and temperature reduction factor for SA, population size, number of generation and mutation probability for GA.

In general, this work provided a design automation methodology to further enhance signal integrity beyond physical/geometrical design of packages and connectors and should be valuable in designing high-speed electronic systems.

8.2 Suggestions for Future Research

1. The equivalent circuit of the packages and connectors only includes the linear driver/receiver. However in many practical case, the driver/receiver is nonlin-

ear rather than linear. A model which can be applied to both the linear and nonlinear driver/receiver will be a possible new direction.

2. The fast model for the crosstalk and ground noise estimation should be extended to more complex cases where the transmission line model is considered. The model we are using now neglects the interconnect capacitance which results in errors less than 5%. This error could be higher as signal speeds becomes higher. For more accurate crosstalk and ground noise estimation, a full model of the pin is needed.
3. The integration-based simulation is much slower than the fast algebraic model, but it is more accurate and reliable. In the future research, a fast integrated-based simulation model can be exploited. For example, the major computation effort is the LU decomposition. The matrices C and G of Equation (5.17) only have small changes when the pin-assignment pattern is changed. A modified LU decomposition method needs to be developed that can solve the equations without re-doing the entire LU decomposition for each pin-assignment pattern.
4. This thesis applied two optimization techniques, GA and SA, to the pin-assignment optimization problem. A comparison of the GA and SA through the six examples have been presented. More detailed comparison of these two techniques will be a further research direction. Another possible research direction is how to chose the parameter of these two optimization techniques so that the best optimization result can be obtained.

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